

MODEL NAME : *QBR00*

PCB NO : *LA-8341P*

BOM P/N : *TBD*

Compal Confidential

Voyager MLK

Schematic Document

Rev: A00

2012-02-16

@ : Nopop Component

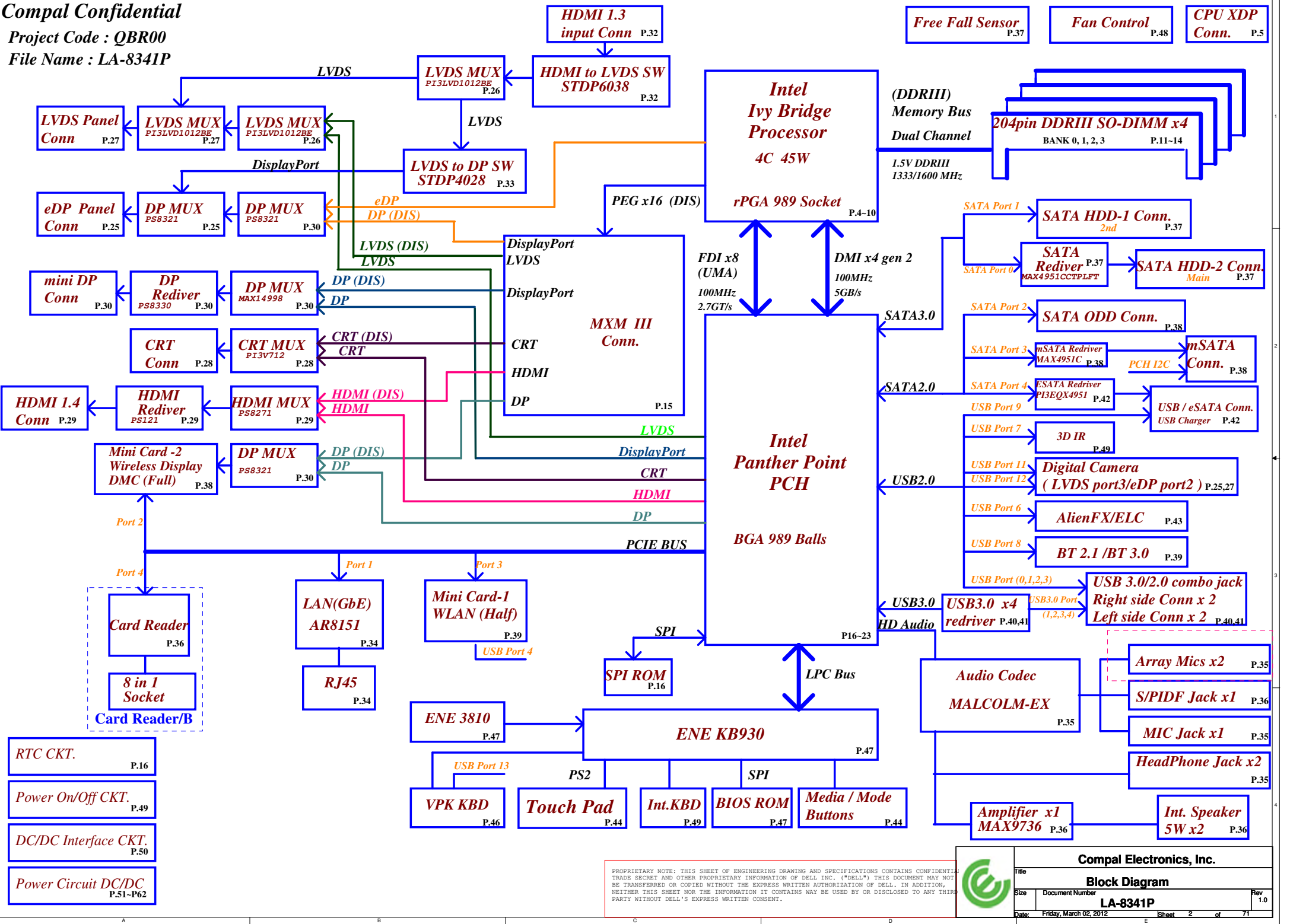
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

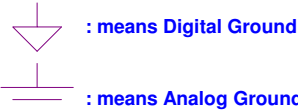
BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (Pre-ST)
3	0.4 (ST)
4	1.0 (QT)
5	
6	
7	

POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Symbol Note :



PM TABLE

State	power plane	+1.5V	+5VS +3VS +1.8VS +1.5VS +0.75VS +3VMXM +5VMXM +VCCP +VCCSA +VCC_CORE +1.5V_CPU_VDDQ
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB 2.0

USB PORT#	DESTINATION
0	JUSB1(USB3.0 P1)
1	JUSB2(USB3.0 P2)
2	JUSB3(USB3.0 P3)
3	JUSB4(USB3.0 P4)
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	JESATA
7	IR SENSOR
8	Bluetooth
9	AlienFX/ELC
10	None
11	eDP CAMERA
12	LVDS CAMERA
13	VPK K/B

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 DMC	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

Power plane	Voltage
+3VALW +3V_PCH +3VS +3VMXM	3.3V

SATA	DESTINATION
SATA0	HDD2
SATA1	HDD1
SATA2	ODD
SATA3	mSATA
SATA4	ESATA
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

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Connector Location	Source	Strap pin setting									
JUSB1	1st PERICOM	U628 P13EQX7502 X76_Pericom@ SA000056E0L	R12 4.7K_0402_5%~D @	R53 4.7K_0402_5%~D X76_Pericom@	R25 4.7K_0402_5%~D @	R49 4.7K_0402_5%~D X76_Pericom@	R337 4.7K_0402_5%~D @	R413 4.7K_0402_5%~D @	R412 4.7K_0402_5%~D @	R1828 D3.3K_0402_5%~D X76_Pericom@	
	2nd PARADE	U628 PS8710B X76_Parade@ SA00004VQ00	R12 4.7K_0402_5%~D @	R53 4.7K_0402_5%~D @	R25 4.7K_0402_5%~D @	R49 4.7K_0402_5%~D @	R337 4.7K_0402_5%~D @	R413 4.7K_0402_5%~D @	R412 4.7K_0402_5%~D @	R1828 3.3K_0402_5%~D X76_Parade@	
	3rd ASMedia	U628 ASM1464 X76_Asmidia@ SA000054400	R12 4.7K_0402_5%~D @	R53 4.7K_0402_5%~D @	R25 4.7K_0402_5%~D @	R49 4.7K_0402_5%~D @	R337 D2K_0402_5%~D X76_Asmidia@	R413 0_0402_5%~D X76_Asmidia@	R412 0_0402_5%~D X76_Asmidia@	R1828 4.7K_0402_5%~D @	

BOM Control	POP	NC
1st PERICOM	X76_Pericom@	@
2nd PARADE	X76_Parade@	@
3rd ASMedia	X76_Asmidia@	@

0224 note-

- 1, QT build only use Pericom.
- 2, Parade need to wait for the new revision.
- 3, Need to got DM permission, then can use Asmedia.

Connector Location	Source	Strap pin setting									
JUSB2	1st PERICOM	U629 P13EQX7502 X76_Pericom@ SA000056E0L	R47 4.7K_0402_5%~D @	R81 4.7K_0402_5%~D X76_Pericom@	R46 4.7K_0402_5%~D @	R67 4.7K_0402_5%~D X76_Pericom@	R314 4.7K_0402_5%~D @	R415 4.7K_0402_5%~D @	R414 4.7K_0402_5%~D @	R1833 D3.3K_0402_5%~D X76_Pericom@	
	2nd PARADE	U629 PS8710B X76_Parade@ SA00004VQ00	R47 4.7K_0402_5%~D @	R81 4.7K_0402_5%~D @	R46 4.7K_0402_5%~D @	R67 4.7K_0402_5%~D @	R314 4.7K_0402_5%~D @	R415 4.7K_0402_5%~D @	R414 4.7K_0402_5%~D @	R1833 3.3K_0402_5%~D X76_Parade@	
	3rd ASMedia	U629 ASM1464 X76_Asmidia@ SA000054400	R47 4.7K_0402_5%~D @	R81 4.7K_0402_5%~D @	R46 4.7K_0402_5%~D @	R67 4.7K_0402_5%~D @	R314 D2K_0402_5%~D X76_Asmidia@	R415 0_0402_5%~D X76_Asmidia@	R414 0_0402_5%~D X76_Asmidia@	R1833 4.7K_0402_5%~D @	

Connector Location	Source	Strap pin setting									
JUSB3	1st PERICOM	U630 P13EQX7502 X76_Pericom@ SA000056E0L	R192 4.7K_0402_5%~D @	R120 4.7K_0402_5%~D X76_Pericom@	R187 4.7K_0402_5%~D @	R105 4.7K_0402_5%~D X76_Pericom@	R343 4.7K_0402_5%~D @	R420 4.7K_0402_5%~D @	R419 4.7K_0402_5%~D @	R1834 D3.3K_0402_5%~D X76_Pericom@	
	2nd PARADE	U630 PS8710B X76_Parade@ SA00004VQ00	R192 4.7K_0402_5%~D @	R120 4.7K_0402_5%~D @	R187 4.7K_0402_5%~D @	R105 4.7K_0402_5%~D @	R343 4.7K_0402_5%~D @	R420 4.7K_0402_5%~D @	R419 4.7K_0402_5%~D @	R1834 3.3K_0402_5%~D X76_Parade@	
	3rd ASMedia	U630 ASM1464 X76_Asmidia@ SA000054400	R192 4.7K_0402_5%~D @	R120 4.7K_0402_5%~D @	R187 4.7K_0402_5%~D @	R105 4.7K_0402_5%~D @	R343 D2K_0402_5%~D X76_Asmidia@	R420 0_0402_5%~D X76_Asmidia@	R419 0_0402_5%~D X76_Asmidia@	R1834 4.7K_0402_5%~D @	

Connector Location	Source	Strap pin setting									
JUSB4	1st PERICOM	U631 P13EQX7502 X76_Pericom@ SA000056E0L	R197 4.7K_0402_5%~D @	R183 4.7K_0402_5%~D X76_Pericom@	R196 4.7K_0402_5%~D @	R182 4.7K_0402_5%~D X76_Pericom@	R344 4.7K_0402_5%~D @	R424 4.7K_0402_5%~D @	R421 4.7K_0402_5%~D @	R1835 D3.3K_0402_5%~D X76_Pericom@	
	2nd PARADE	U631 PS8710B X76_Parade@ SA00004VQ00	R197 4.7K_0402_5%~D @	R183 4.7K_0402_5%~D @	R196 4.7K_0402_5%~D @	R182 4.7K_0402_5%~D @	R344 4.7K_0402_5%~D @	R424 4.7K_0402_5%~D @	R421 4.7K_0402_5%~D @	R1835 3.3K_0402_5%~D X76_Parade@	
	3rd ASMedia	U631 ASM1464 X76_Asmidia@ SA000054400	R197 4.7K_0402_5%~D @	R183 4.7K_0402_5%~D @	R196 4.7K_0402_5%~D @	R182 4.7K_0402_5%~D @	R344 D2K_0402_5%~D X76_Asmidia@	R424 0_0402_5%~D X76_Asmidia@	R421 0_0402_5%~D X76_Asmidia@	R1835 4.7K_0402_5%~D @	

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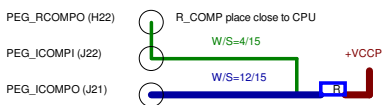


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USB3.0 Config setting			
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Trace length Max is 500 mils



18 DMI_CRX_PTX_N0 <<< DMI_CRX_PTX_N0 B27
18 DMI_CRX_PTX_N1 <<< DMI_CRX_PTX_N1 B25
18 DMI_CRX_PTX_N2 <<< DMI_CRX_PTX_N2 A25
18 DMI_CRX_PTX_N3 <<< DMI_CRX_PTX_N3 B24
18 DMI_CRX_PTX_N4 <<< DMI_CRX_PTX_N4 B23

18 DMI_CRX_PTX_P0 <<< DMI_CRX_PTX_P0 B26
18 DMI_CRX_PTX_P1 <<< DMI_CRX_PTX_P1 A24
18 DMI_CRX_PTX_P2 <<< DMI_CRX_PTX_P2 A24
18 DMI_CRX_PTX_P3 <<< DMI_CRX_PTX_P3 B23

18 DMI_CTX_PRX_N0 <<< DMI_CTX_PRX_N0 G21
18 DMI_CTX_PRX_N1 <<< DMI_CTX_PRX_N1 E22
18 DMI_CTX_PRX_N2 <<< DMI_CTX_PRX_N2 F21
18 DMI_CTX_PRX_N3 <<< DMI_CTX_PRX_N3 D21

18 DMI_CTX_PRX_P0 <<< DMI_CTX_PRX_P0 G22
18 DMI_CTX_PRX_P1 <<< DMI_CTX_PRX_P1 D22
18 DMI_CTX_PRX_P2 <<< DMI_CTX_PRX_P2 F20
18 DMI_CTX_PRX_P3 <<< DMI_CTX_PRX_P3 C21

18 FDI_CTX_PRX_N0 <<< FDI_CTX_PRX_N0 A21
18 FDI_CTX_PRX_N1 <<< FDI_CTX_PRX_N1 H19
18 FDI_CTX_PRX_N2 <<< FDI_CTX_PRX_N2 E19
18 FDI_CTX_PRX_N3 <<< FDI_CTX_PRX_N3 F18
18 FDI_CTX_PRX_N4 <<< FDI_CTX_PRX_N4 B21
18 FDI_CTX_PRX_N5 <<< FDI_CTX_PRX_N5 C20
18 FDI_CTX_PRX_N6 <<< FDI_CTX_PRX_N6 D18
18 FDI_CTX_PRX_N7 <<< FDI_CTX_PRX_N7 E17

18 FDI_CTX_PRX_P0 <<< FDI_CTX_PRX_P0 A22
18 FDI_CTX_PRX_P1 <<< FDI_CTX_PRX_P1 G19
18 FDI_CTX_PRX_P2 <<< FDI_CTX_PRX_P2 E20
18 FDI_CTX_PRX_P3 <<< FDI_CTX_PRX_P3 G18
18 FDI_CTX_PRX_P4 <<< FDI_CTX_PRX_P4 B20
18 FDI_CTX_PRX_P5 <<< FDI_CTX_PRX_P5 C19
18 FDI_CTX_PRX_P6 <<< FDI_CTX_PRX_P6 D19
18 FDI_CTX_PRX_P7 <<< FDI_CTX_PRX_P7 F17

18 FDI_FSYNC0 <<< FDI_FSYNC0 J18
18 FDI_FSYNC1 <<< FDI_FSYNC1 J17
18 FDI_INT <<< FDI_INT H20
18 FDI_LSYNC0 <<< FDI_LSYNC0 J19
18 FDI_LSYNC1 <<< FDI_LSYNC1 H17

24 EDP_AUXP <<< EDP_AUXP C15
24 EDP_AUXN <<< EDP_AUXN D15

24 EDP_TX0P <<< EDP_TX0P C17
24 EDP_TX1P <<< EDP_TX1P F16
24 EDP_TX2P <<< EDP_TX2P C16
24 EDP_TX3P <<< EDP_TX3P G15

24 EDP_TX0N <<< EDP_TX0N C18
24 EDP_TX1N <<< EDP_TX1N E16
24 EDP_TX2N <<< EDP_TX2N D16
24 EDP_TX3N <<< EDP_TX3N F15

DMI_RX#0
DMI_RX#1
DMI_RX#2
DMI_RX#3
DMI_RX#4
DMI_RX#5
DMI_RX#6
DMI_RX#7
DMI_RX#8
DMI_RX#9
DMI_RX#10
DMI_RX#11
DMI_RX#12
DMI_RX#13
DMI_RX#14
DMI_RX#15
DMI_TX#0
DMI_TX#1
DMI_TX#2
DMI_TX#3

FDIO_TX#0
FDIO_TX#1
FDIO_TX#2
FDIO_TX#3
FDIO_TX#4
FDIO_TX#5
FDIO_TX#6
FDIO_TX#7
FDIO_TX#8
FDIO_TX#9
FDIO_TX#10
FDIO_TX#11
FDIO_TX#12
FDIO_TX#13
FDIO_TX#14
FDIO_TX#15

FDIO_LSYNC
FDIO_LSYNC1
FDIO_LSYNC2
FDIO_LSYNC3
FDIO_LSYNC4
FDIO_LSYNC5
FDIO_LSYNC6
FDIO_LSYNC7
FDIO_LSYNC8
FDIO_LSYNC9
FDIO_LSYNC10
FDIO_LSYNC11
FDIO_LSYNC12
FDIO_LSYNC13
FDIO_LSYNC14
FDIO_LSYNC15

eDP_COMPIO
eDP_ICOMPIO
eDP_HPDS
eDP_AUX
eDP_AUX#
eDP_TX0
eDP_TX1
eDP_TX2
eDP_TX3
eDP_TX#0
eDP_TX#1
eDP_TX#2
eDP_TX#3
eDP_TX#4
eDP_TX#5
eDP_TX#6
eDP_TX#7
eDP_TX#8
eDP_TX#9
eDP_TX#10
eDP_TX#11
eDP_TX#12
eDP_TX#13
eDP_TX#14
eDP_TX#15

DMI

Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

TYCO_2134146-3_IVYBRIDGE-D

PEG_ICOMPI	J21	PEG_COMP
PEG_ICOMPO	H22	
PEG_RCOMPO		
PEG_RX#0	K33	PEG GTX C HRX N0 CC1 1 2 0.22U 0402 16V7K-D PEG GTX HRX N0
PEG_RX#1	M35	PEG GTX C HRX N1 CC2 1 2 0.22U 0402 16V7K-D PEG GTX HRX N1
PEG_RX#2	L34	PEG GTX C HRX N2 CC3 1 2 0.22U 0402 16V7K-D PEG GTX HRX N2
PEG_RX#3	J35	PEG GTX C HRX N3 CC4 1 2 0.22U 0402 16V7K-D PEG GTX HRX N3
PEG_RX#4	J32	PEG GTX C HRX N4 CC5 1 2 0.22U 0402 16V7K-D PEG GTX HRX N4
PEG_RX#5	H34	PEG GTX C HRX N5 CC13 1 2 0.22U 0402 16V7K-D PEG GTX HRX N5
PEG_RX#6	H31	PEG GTX C HRX N6 CC6 1 2 0.22U 0402 16V7K-D PEG GTX HRX N6
PEG_RX#7	G33	PEG GTX C HRX N7 CC7 1 2 0.22U 0402 16V7K-D PEG GTX HRX N7
PEG_RX#8	G30	PEG GTX C HRX N8 CC8 1 2 0.22U 0402 16V7K-D PEG GTX HRX N8
PEG_RX#9	F35	PEG GTX C HRX N9 CC9 1 2 0.22U 0402 16V7K-D PEG GTX HRX N9
PEG_RX#10	E34	PEG GTX C HRX N10 CC10 1 2 0.22U 0402 16V7K-D PEG GTX HRX N10
PEG_RX#11	E32	PEG GTX C HRX N11 CC11 1 2 0.22U 0402 16V7K-D PEG GTX HRX N11
PEG_RX#12	D33	PEG GTX C HRX N12 CC12 1 2 0.22U 0402 16V7K-D PEG GTX HRX N12
PEG_RX#13	D31	PEG GTX C HRX N13 CC14 1 2 0.22U 0402 16V7K-D PEG GTX HRX N13
PEG_RX#14	B33	PEG GTX C HRX N14 CC15 1 2 0.22U 0402 16V7K-D PEG GTX HRX N14
PEG_RX#15	C32	PEG GTX C HRX N15 CC16 1 2 0.22U 0402 16V7K-D PEG GTX HRX N15
PEG_RX#0	J33	PEG GTX C HRX P0 CC17 1 2 0.22U 0402 16V7K-D PEG GTX HRX P0
PEG_RX#1	L35	PEG GTX C HRX P1 CC18 1 2 0.22U 0402 16V7K-D PEG GTX HRX P1
PEG_RX#2	K34	PEG GTX C HRX P2 CC19 1 2 0.22U 0402 16V7K-D PEG GTX HRX P2
PEG_RX#3	H35	PEG GTX C HRX P3 CC20 1 2 0.22U 0402 16V7K-D PEG GTX HRX P3
PEG_RX#4	H32	PEG GTX C HRX P4 CC21 1 2 0.22U 0402 16V7K-D PEG GTX HRX P4
PEG_RX#5	G34	PEG GTX C HRX P5 CC22 1 2 0.22U 0402 16V7K-D PEG GTX HRX P5
PEG_RX#6	G31	PEG GTX C HRX P6 CC23 1 2 0.22U 0402 16V7K-D PEG GTX HRX P6
PEG_RX#7	F33	PEG GTX C HRX P7 CC24 1 2 0.22U 0402 16V7K-D PEG GTX HRX P7
PEG_RX#8	F30	PEG GTX C HRX P8 CC25 1 2 0.22U 0402 16V7K-D PEG GTX HRX P8
PEG_RX#9	E35	PEG GTX C HRX P9 CC26 1 2 0.22U 0402 16V7K-D PEG GTX HRX P9
PEG_RX#10	E33	PEG GTX C HRX P10 CC27 1 2 0.22U 0402 16V7K-D PEG GTX HRX P10
PEG_RX#11	F32	PEG GTX C HRX P11 CC28 1 2 0.22U 0402 16V7K-D PEG GTX HRX P11
PEG_RX#12	D34	PEG GTX C HRX P12 CC29 1 2 0.22U 0402 16V7K-D PEG GTX HRX P12
PEG_RX#13	E31	PEG GTX C HRX P13 CC30 1 2 0.22U 0402 16V7K-D PEG GTX HRX P13
PEG_RX#14	C33	PEG GTX C HRX P14 CC31 1 2 0.22U 0402 16V7K-D PEG GTX HRX P14
PEG_RX#15	B32	PEG GTX C HRX P15 CC32 1 2 0.22U 0402 16V7K-D PEG GTX HRX P15
PEG_TX#0	M29	PEG HTX C GRX N0 CC33 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N0
PEG_TX#1	M32	PEG HTX C GRX N1 CC34 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N1
PEG_TX#2	M31	PEG HTX C GRX N2 CC35 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N2
PEG_TX#3	L32	PEG HTX C GRX N3 CC36 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N3
PEG_TX#4	L29	PEG HTX C GRX N4 CC37 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N4
PEG_TX#5	K31	PEG HTX C GRX N5 CC38 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N5
PEG_TX#6	K28	PEG HTX C GRX N6 CC39 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N6
PEG_TX#7	J30	PEG HTX C GRX N7 CC40 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N7
PEG_TX#8	J28	PEG HTX C GRX N8 CC41 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N8
PEG_TX#9	H29	PEG HTX C GRX N9 CC42 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N9
PEG_TX#10	G27	PEG HTX C GRX N10 CC43 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N10
PEG_TX#11	E29	PEG HTX C GRX N11 CC44 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N11
PEG_TX#12	D27	PEG HTX C GRX N12 CC45 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N12
PEG_TX#13	D26	PEG HTX C GRX N13 CC46 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N13
PEG_TX#14	F26	PEG HTX C GRX N14 CC47 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N14
PEG_TX#15	E25	PEG HTX C GRX N15 CC48 1 2 0.22U 0402 16V7K-D PEG HTX C GRX N15
PEG_TX#0	M28	PEG HTX C GRX P0 CC49 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P0
PEG_TX#1	M33	PEG HTX C GRX P1 CC50 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P1
PEG_TX#2	M30	PEG HTX C GRX P2 CC51 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P2
PEG_TX#3	L31	PEG HTX C GRX P3 CC52 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P3
PEG_TX#4	K28	PEG HTX C GRX P4 CC53 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P4
PEG_TX#5	K30	PEG HTX C GRX P5 CC54 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P5
PEG_TX#6	K27	PEG HTX C GRX P6 CC55 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P6
PEG_TX#7	J29	PEG HTX C GRX P7 CC56 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P7
PEG_TX#8	J27	PEG HTX C GRX P8 CC57 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P8
PEG_TX#9	H28	PEG HTX C GRX P9 CC58 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P9
PEG_TX#10	G28	PEG HTX C GRX P10 CC59 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P10
PEG_TX#11	E28	PEG HTX C GRX P11 CC60 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P11
PEG_TX#12	D27	PEG HTX C GRX P12 CC61 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P12
PEG_TX#13	D27	PEG HTX C GRX P13 CC62 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P13
PEG_TX#14	E26	PEG HTX C GRX P14 CC63 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P14
PEG_TX#15	D25	PEG HTX C GRX P15 CC64 1 2 0.22U 0402 16V7K-D PEG HTX C GRX P15

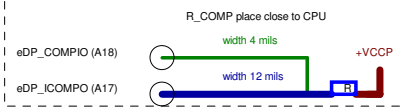
Near MXM Connector

0811: Need to check with ME connector list

Link CIS OK

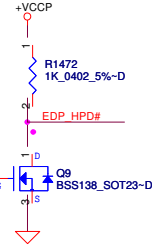


Trace length Max is 500 mils

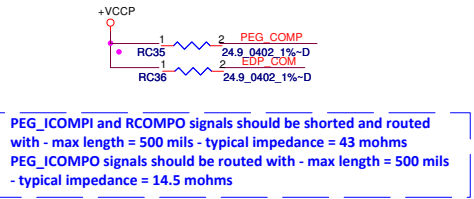


eDP_COMPIO (A18)
eDP_ICOMPIO (A17)

HPD Inversion for eDP



Note: Place pull up resistor within 2 inches of CPU

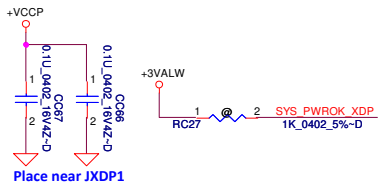


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

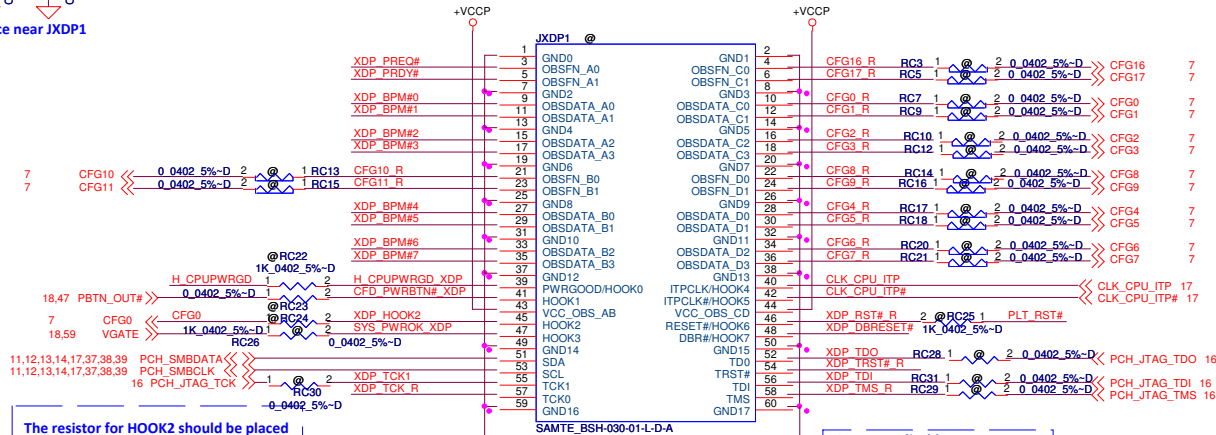
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PROCESSOR(1/6) DMI,FDI,PEG	
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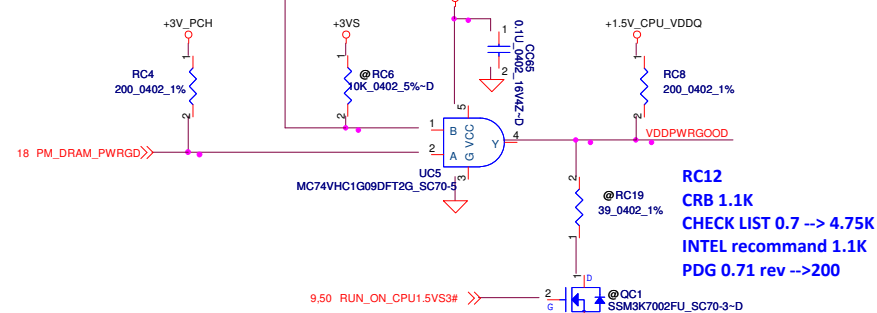
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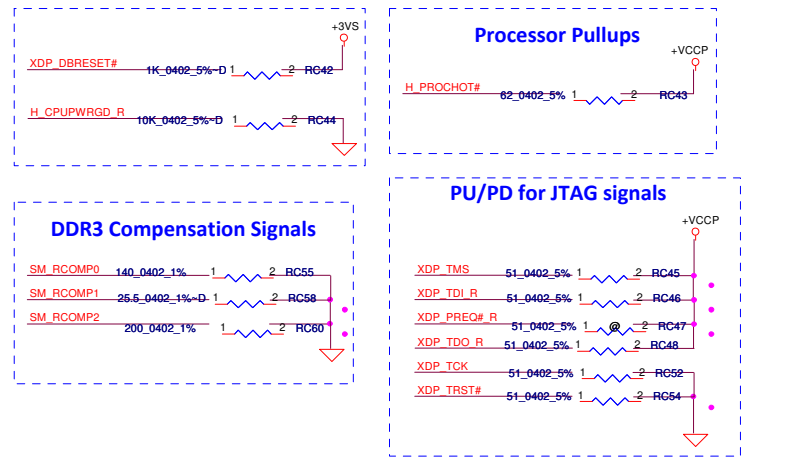
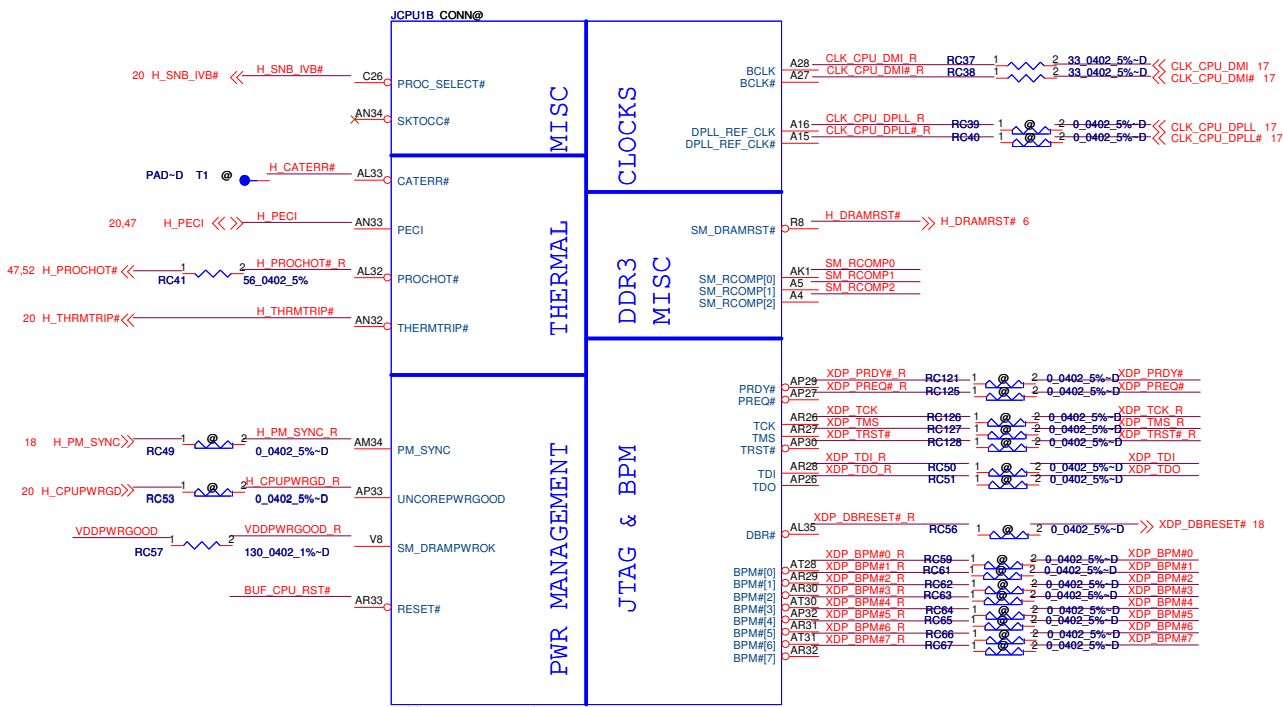
Place near JXDP1



18.47 PCH_PWR0K >> @RC113 1 2 0.0402 5%-D
18.47 SYSTEM_PWR0K >> @RC74 1 2 0.0402 5%-D
18.59 VGATE >> @RC119 1 2 0.0402 5%-D



The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net



0811: Need to check with ME connector list

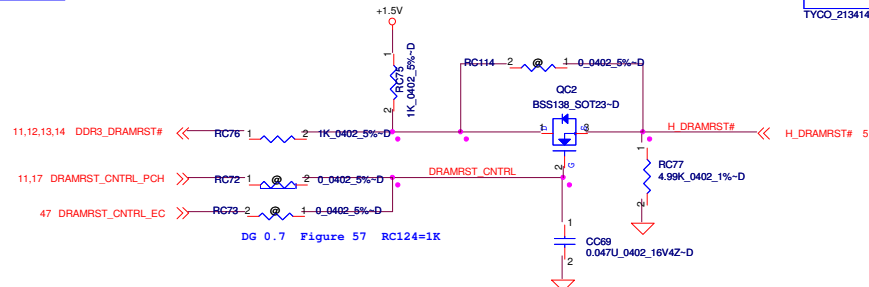
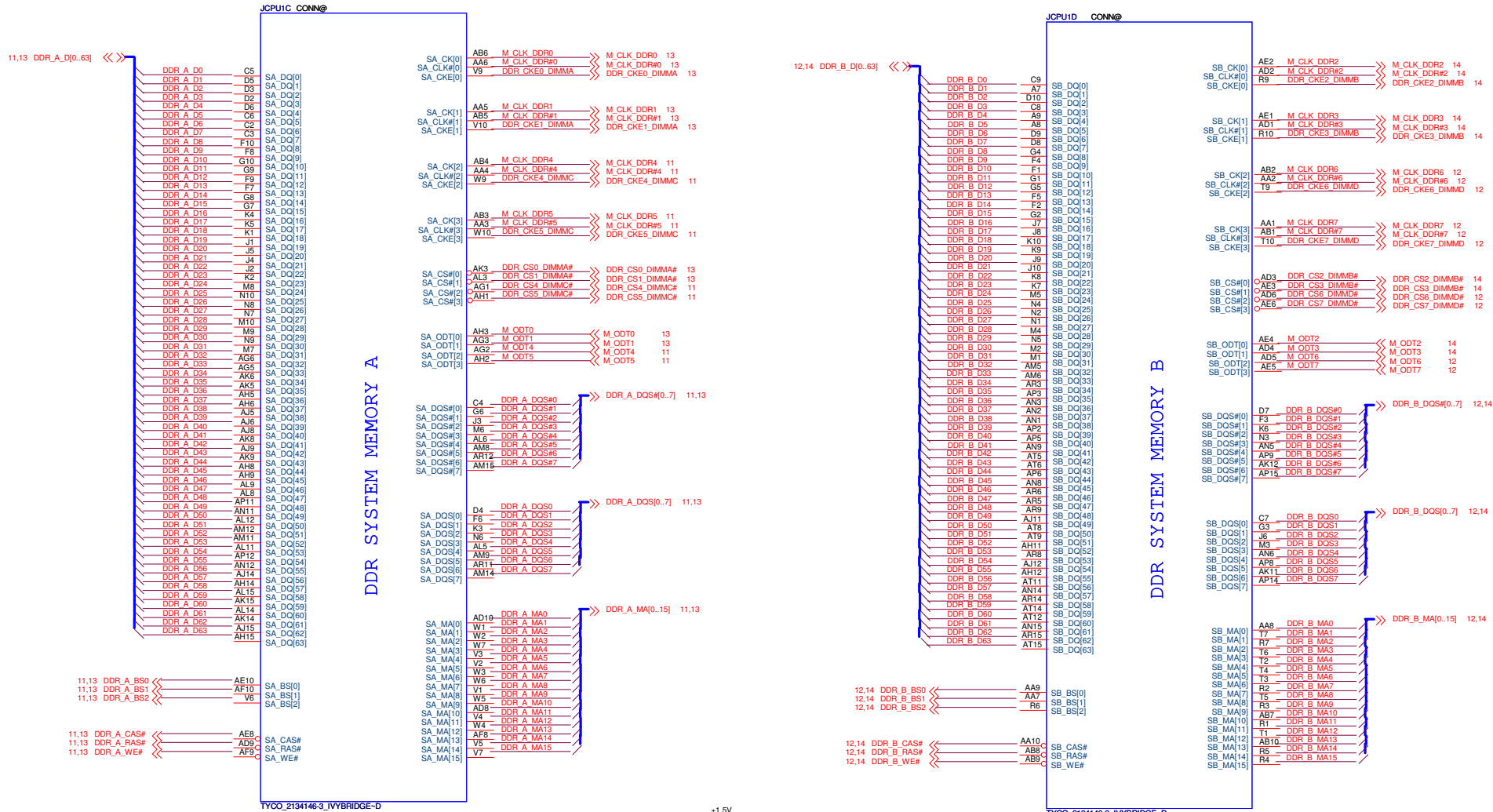
Link CIS OK

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		Compal Electronics, Inc.	
		PROCESSOR(2/6) PM,XDP,CLK	
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Need to confired
when Intel spec release.



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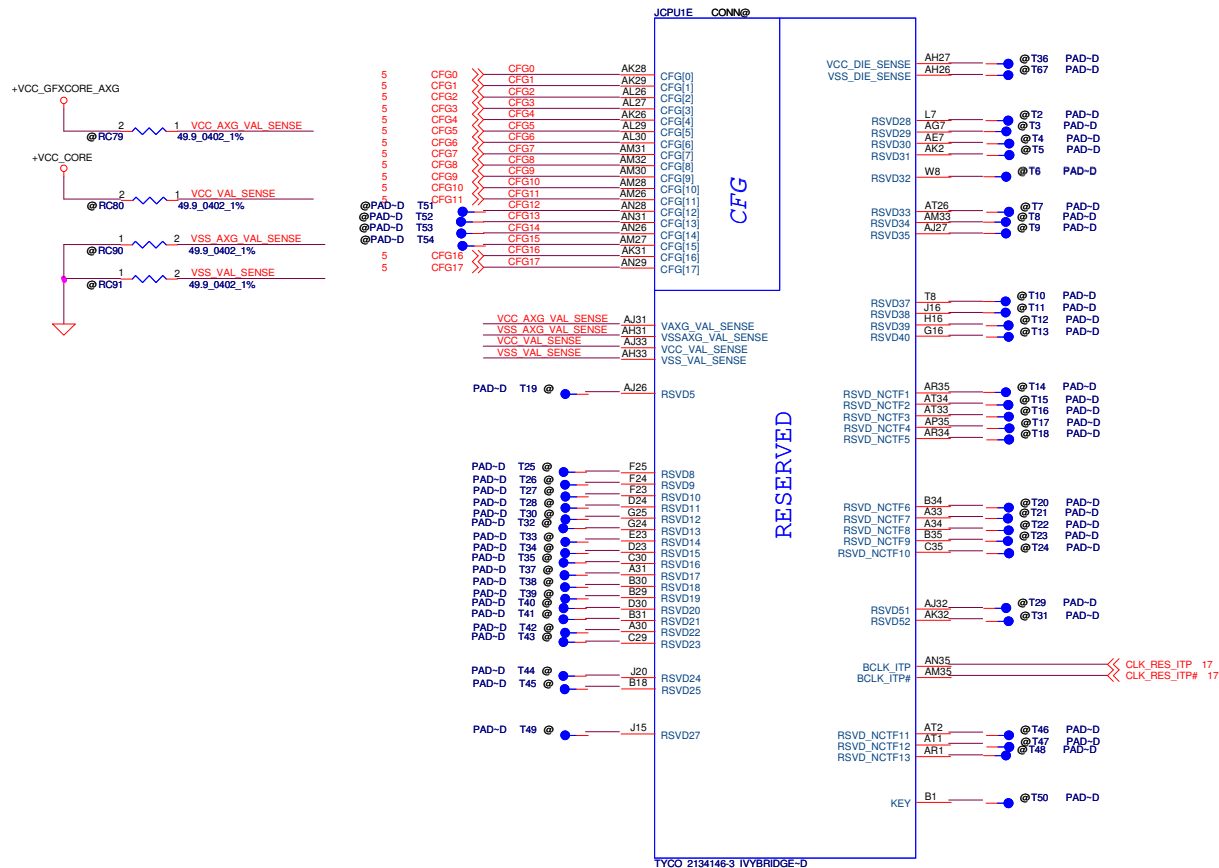
Compal Electronics, Inc.

PROCESSOR(3/6) DDRIII

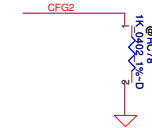
LA-8341P

Rev 1.0

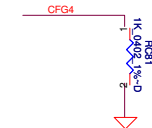
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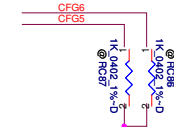
CFG Straps for Processor



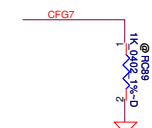
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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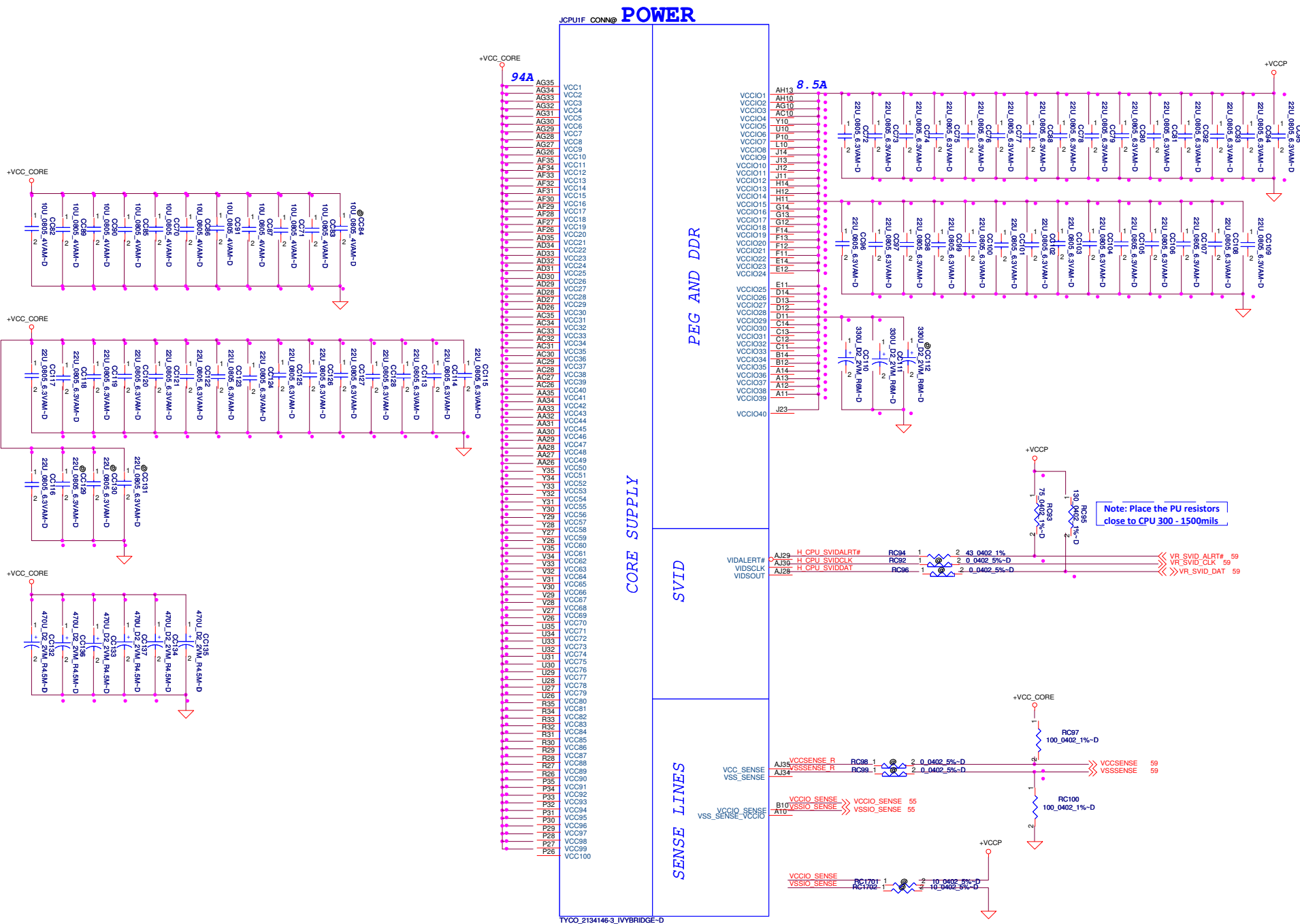
Compal Electronics, Inc.

Title
PROCESSOR(4/6) RSVD,CFG

Size Document Number
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POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

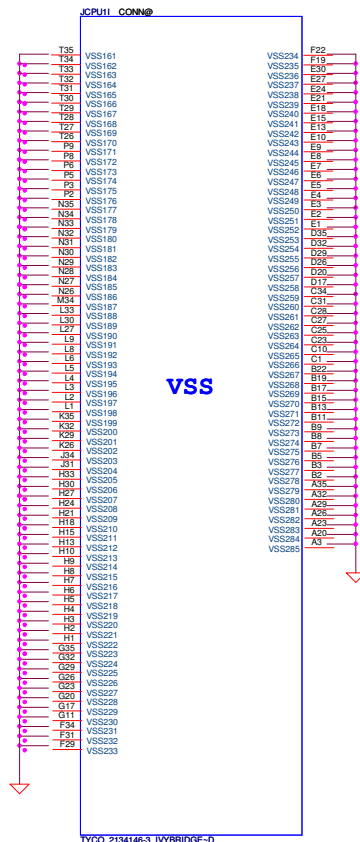
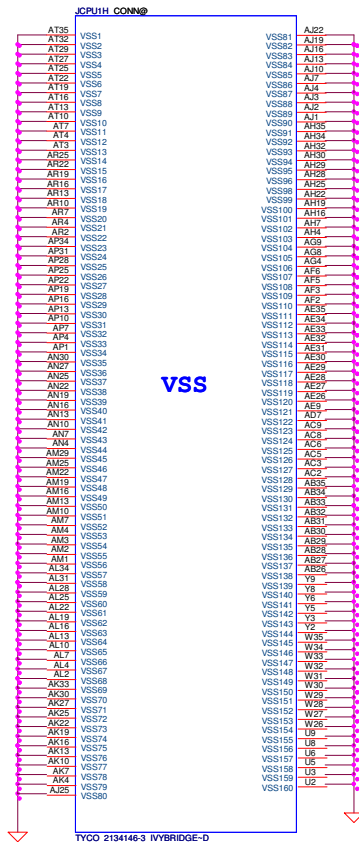
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PROCESSOR(5/6) PWR,BYPASS

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PROCESSOR(6/6) PWR,VSS			
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6.13 DDR_A_DQS#0..7
6.13 DDR_A_DQS#0..7
6.13 DDR_A_DQS#0..7
6.13 DDR_A_DQS#0..7

+V_DDR_REFA RD21 2 0.0402 5%-D

+1.5V

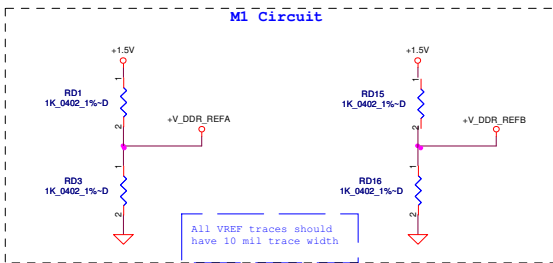
+1.5V

JDIMM2 (H8)A6
JDIMM1 (H4)A2

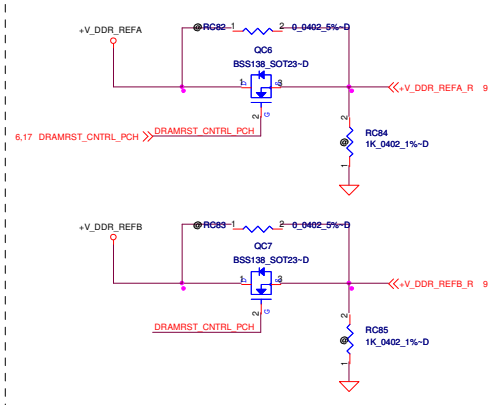
CPU

JDIMM3 (H5.2)A0
JDIMM4 (H9.2)A4

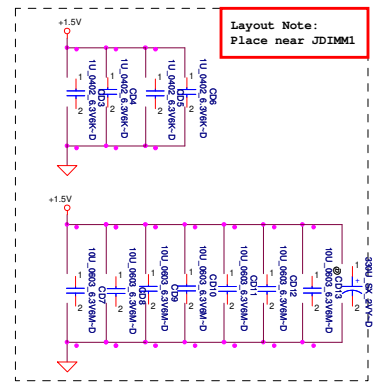
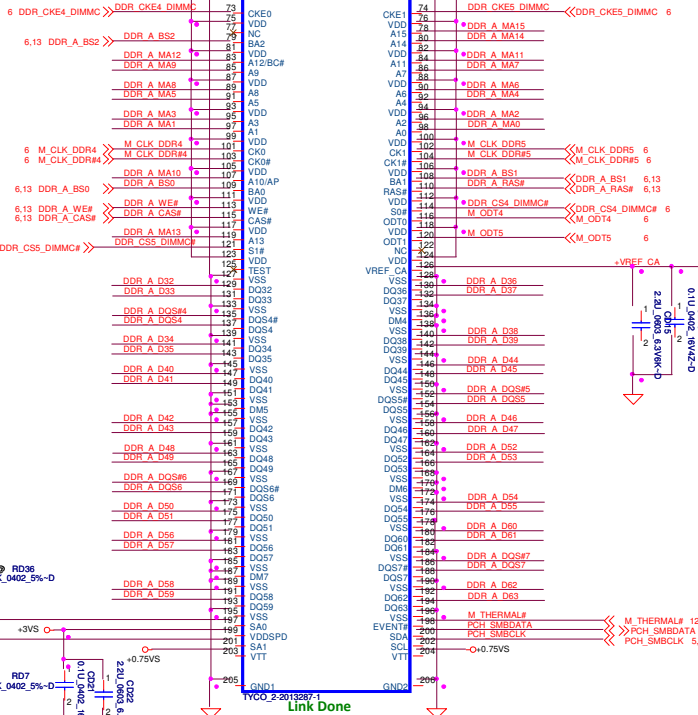
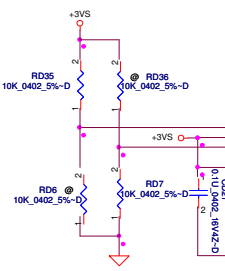
M1 Circuit



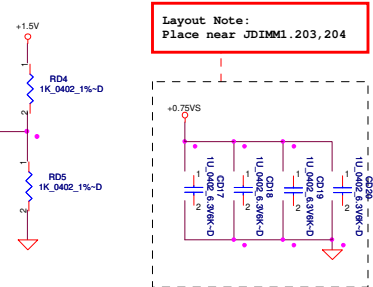
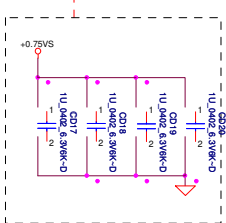
M3 Circuit (Processor Generated SO-DIMM VREF_DQ)



SA1	SA0	
0	1	DIMM1
1	1	DIMM2
0	0	DIMM3
1	0	DIMM4



Layout Note:
Place near JDIMM1.203,204



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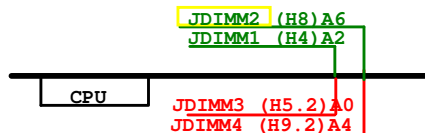
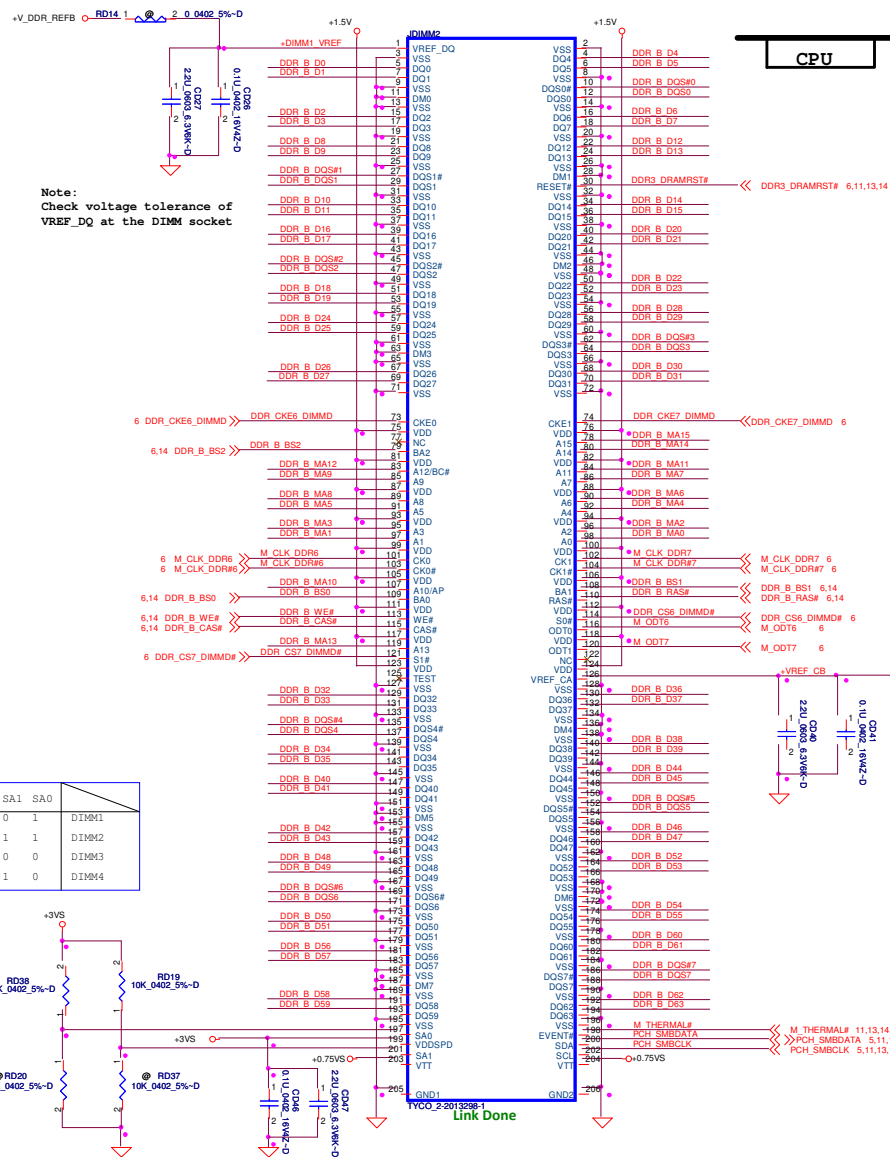
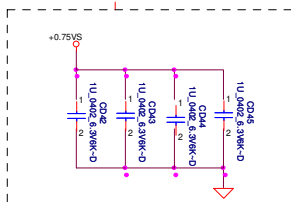
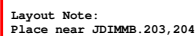
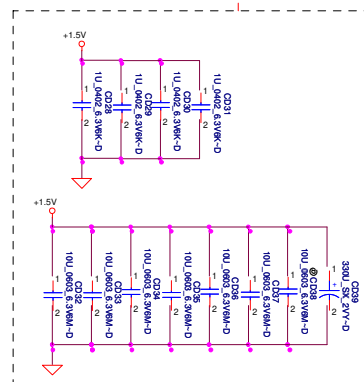
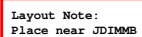
DDR3 DIMM

LA-8341P

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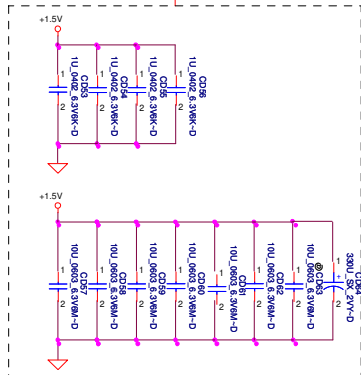


File	Document Number	Rev
LA-8341P	LA-8341P	1.0
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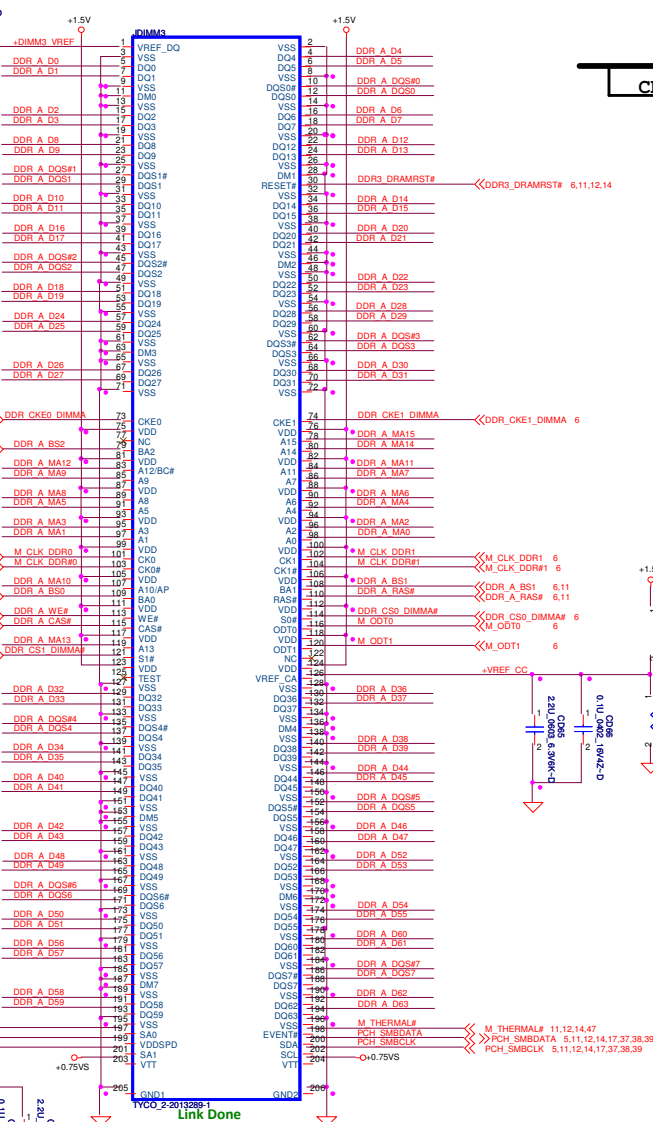
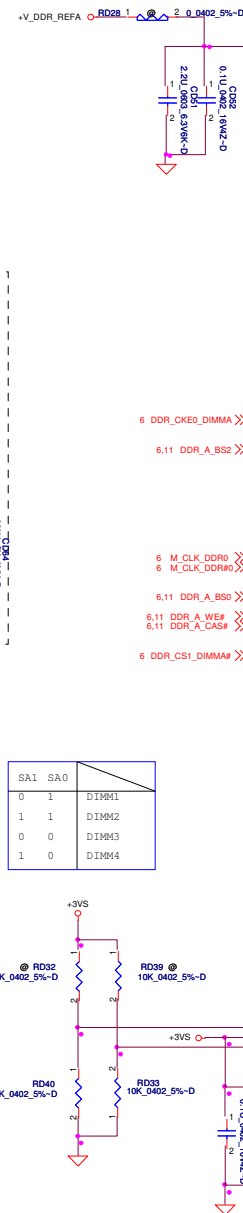
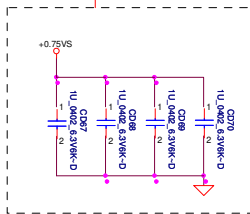


6.11 DDR_A_DQS#(0..7) <<>>
 6.11 DDR_A_DQS(0..7) <<>>
 6.11 DDR_A_D(0..63) <<>>
 6.11 DDR_A_MA(0..15) <<>>

Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



JDIMM2 (H8)A6
JDIMM1 (H4)A2

CPU

JDIMM3 (H5.2)A0
JDIMM4 (H9.2)A4

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DDRIII DIMMC

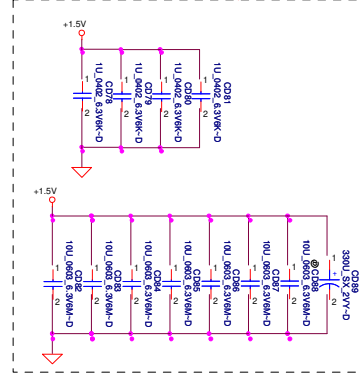
LA-8341P

File	Document Number	Rev
Size	LA-8341P	1.0
Date	Friday, March 02, 2012	Sheet 14 of 21

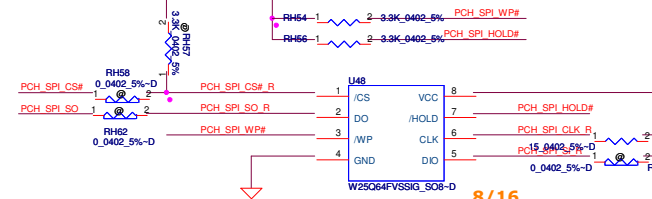
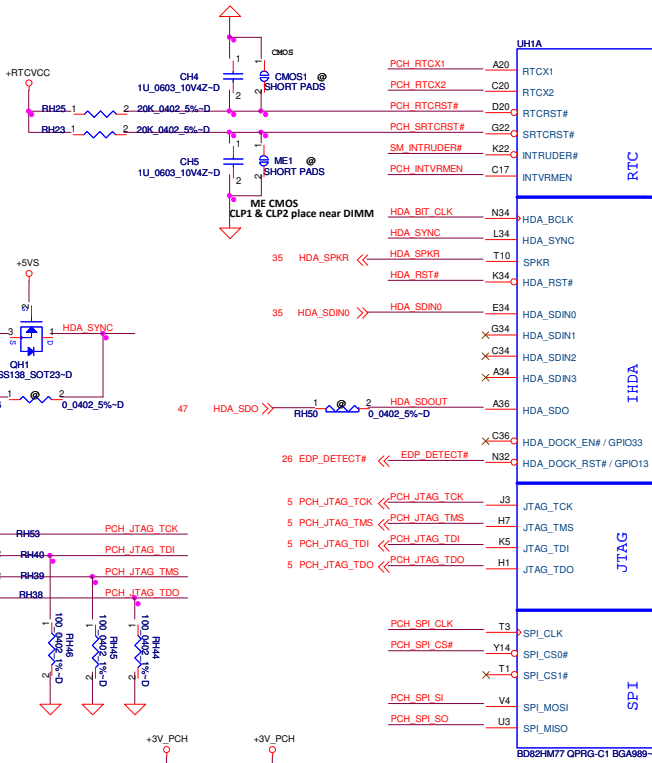
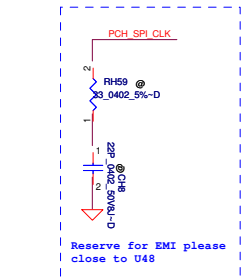
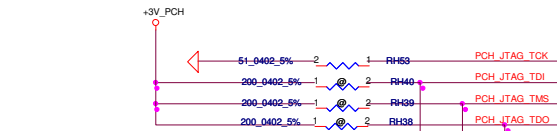
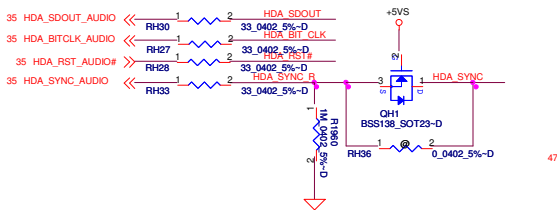
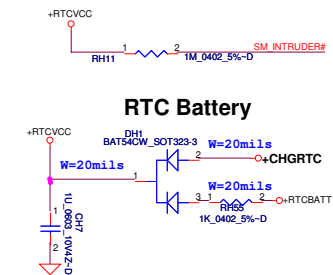
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6.12 DDR_B_DQS#(0..7) >>>
 6.12 DDR_B_DQS#(8..15) >>>
 6.12 DDR_B_DQ(0..63) >>>
 6.12 DDR_B_MA(0..15) >>>

Layout Note:
Place near JDIMMB





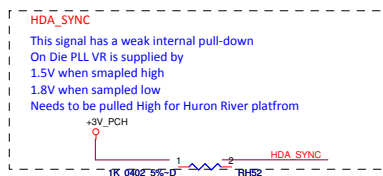
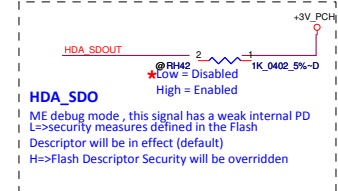
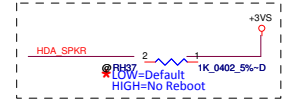
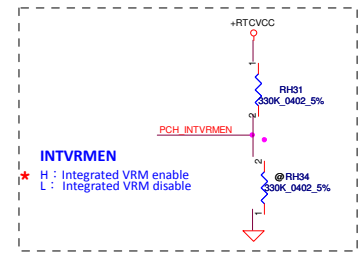
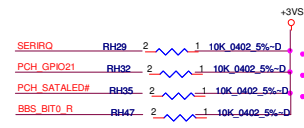
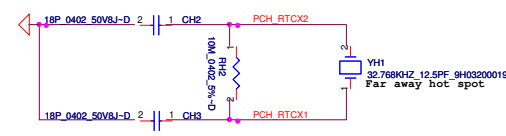


SPI BIOS Pinout

(1) CS#	(5) DIO
(2) DO	(6) CLK
(3) WP#	(7) HOLD#
(4) GND	(8) VCC

SPI ROM FOR ME (8MByte)

8/16
Change to 8Mbyte to achieve win8 request.



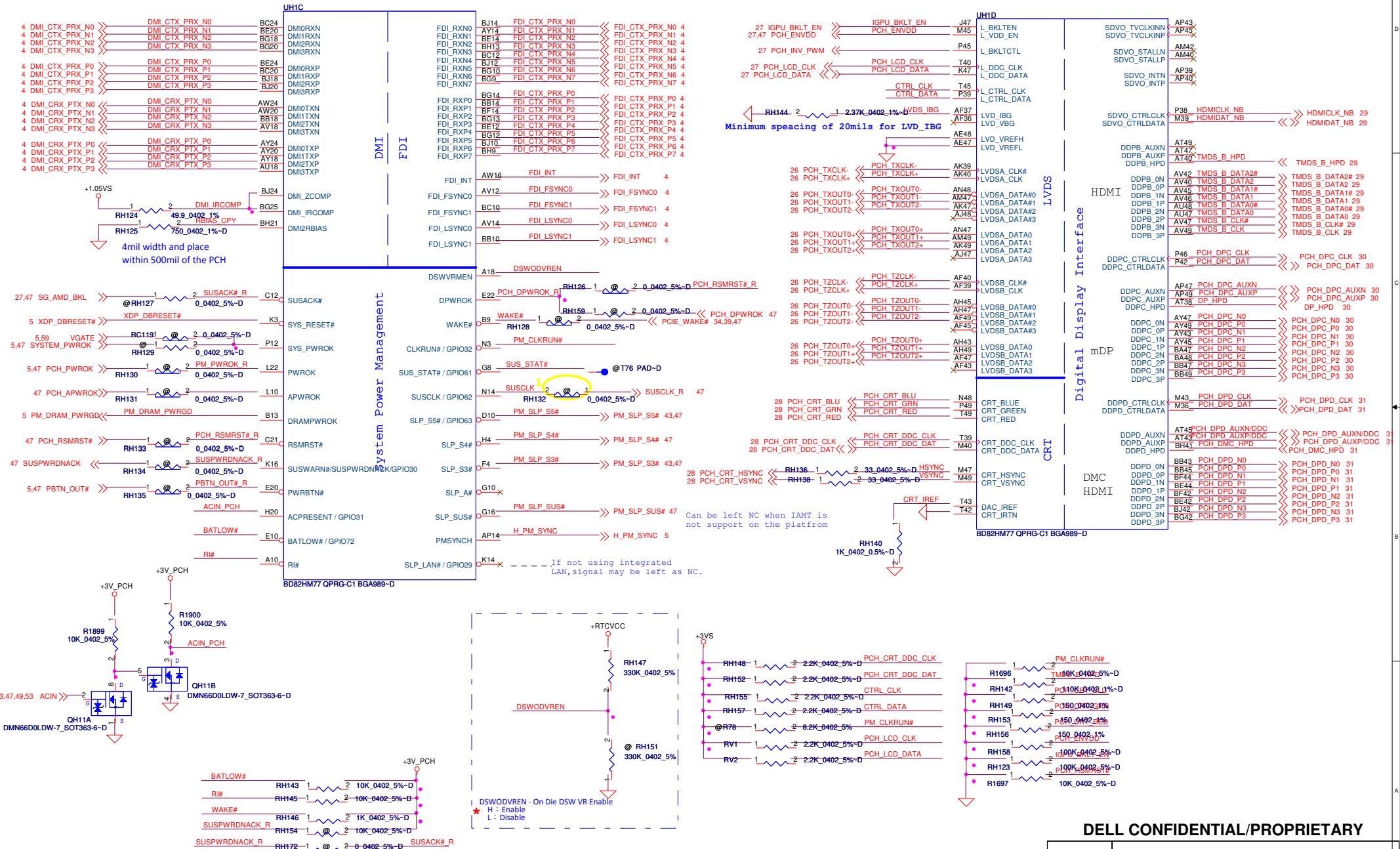
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Title	PCH (1/8) SATA,HDA,SPI, LPC
Size	Document Number
Date	LA-8341P
Rev	1.0

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0811: Intel request DDPB can not support eDP

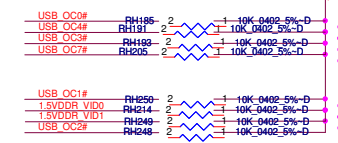
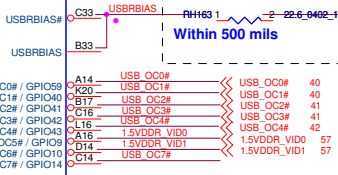
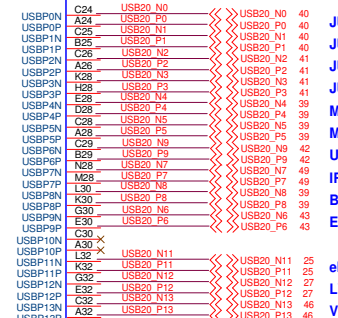
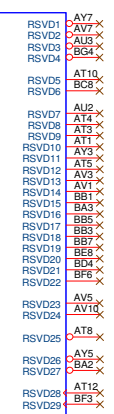
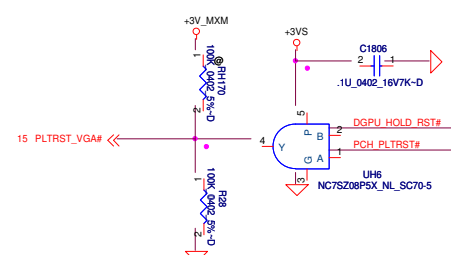
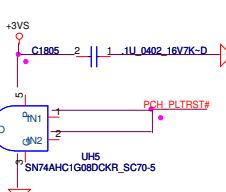
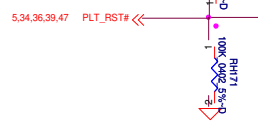
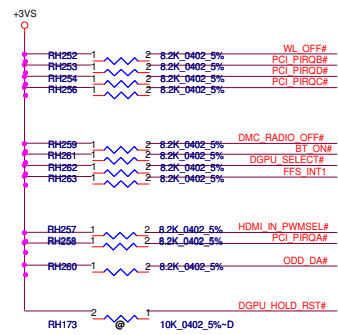
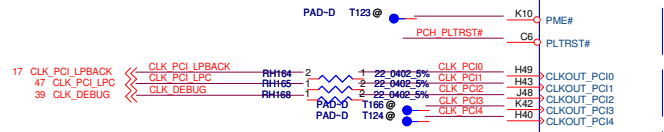
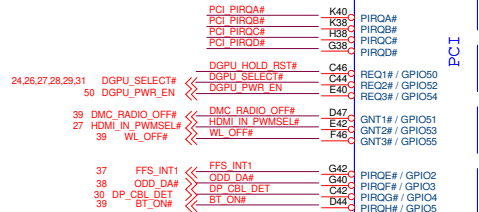
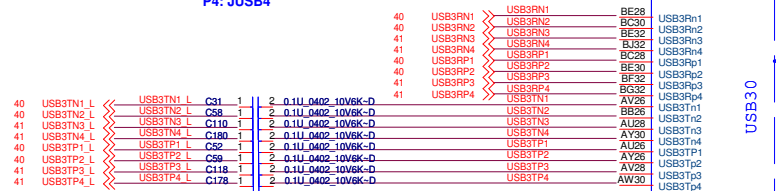


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PCH (3/8) DMI,FDI,PM,GFX,DP	LA-8341P
Rev 1.0	Friday, March 02, 2012

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P1: JUSB1
P2: JUSB2
P3: JUSB3
P4: JUSB4

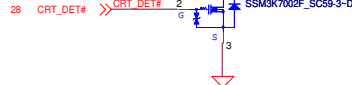


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Compal Electronics, Inc.	
PCH (4/8) PCI, USB, NVRAM	
Size	Document Number
LA-8341P	
Date	Friday, March 02, 2012
Sheet	20 of 71

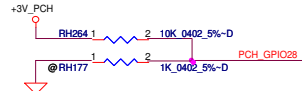
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High: CRT Plugged



GPIO28

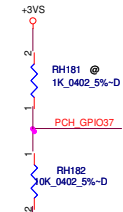
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



PCH_GPIO37

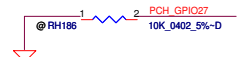
FDI TERMINATION VOLTAGE OVERRIDE

★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)



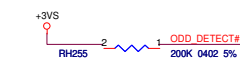
GPIO27

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable



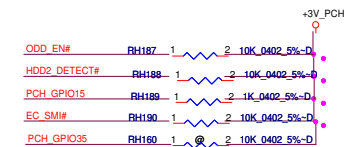
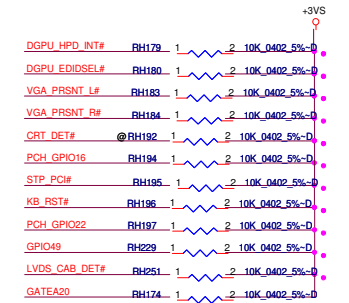
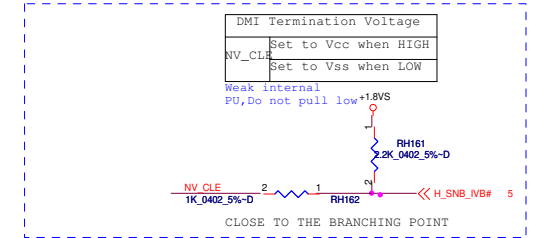
SATA2GP/GPIO36

When Used as SATA2GP/SATA3GP for Mechanical Presence detect
- Use a weak external pull-up (150K-200K ohms) to Vcc3_3
★ check list Rev 1.0



BD82HM77 QPRG-CT BGA989-D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

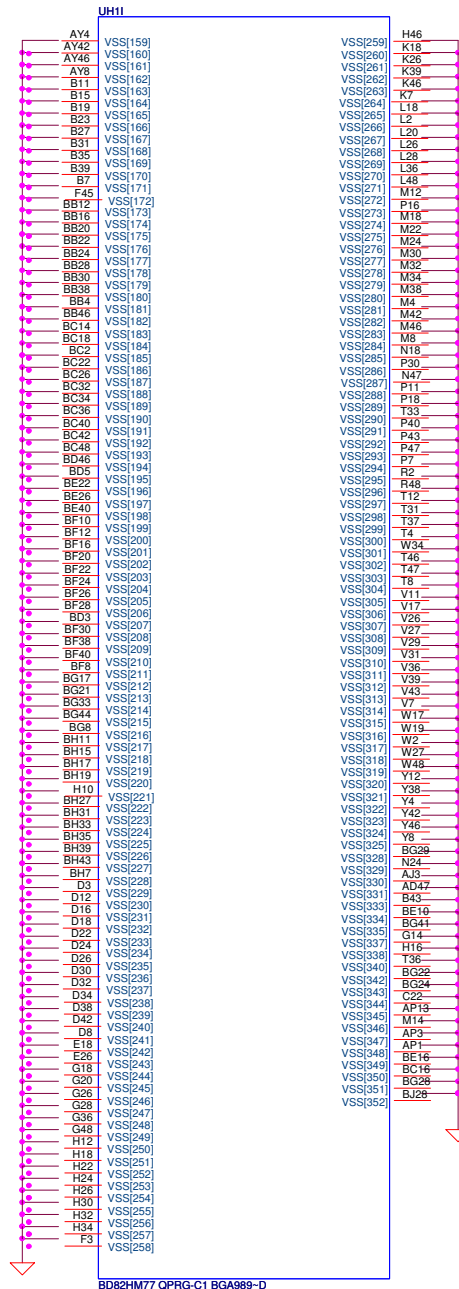
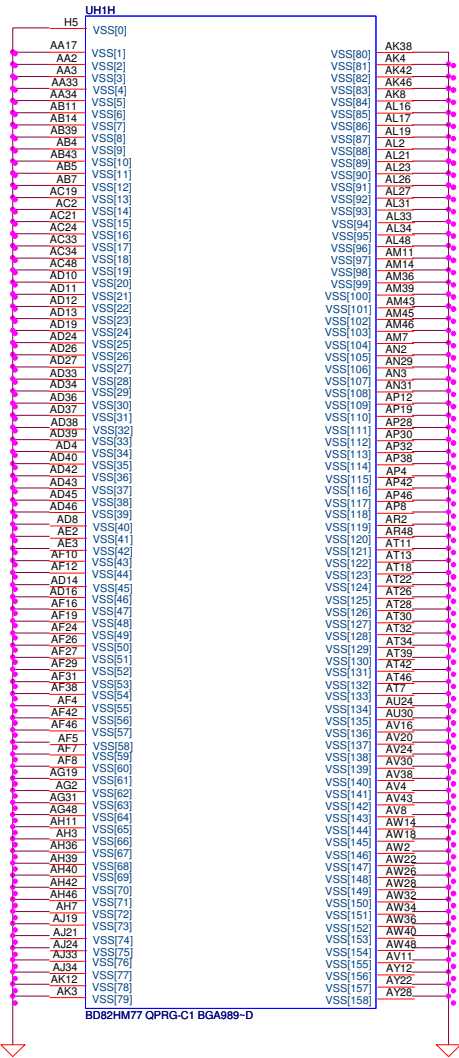


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Title				Rev 1.0
PCH (5/8) GPIO, CPU, MISC				
Size	Document Number			
	LA-8341P			
Date:	Friday, March 02, 2012	Sheet	21	of 71

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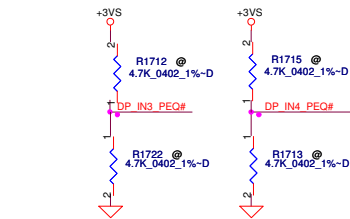
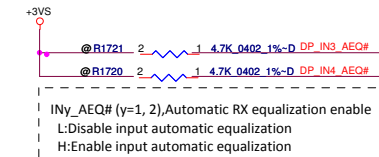
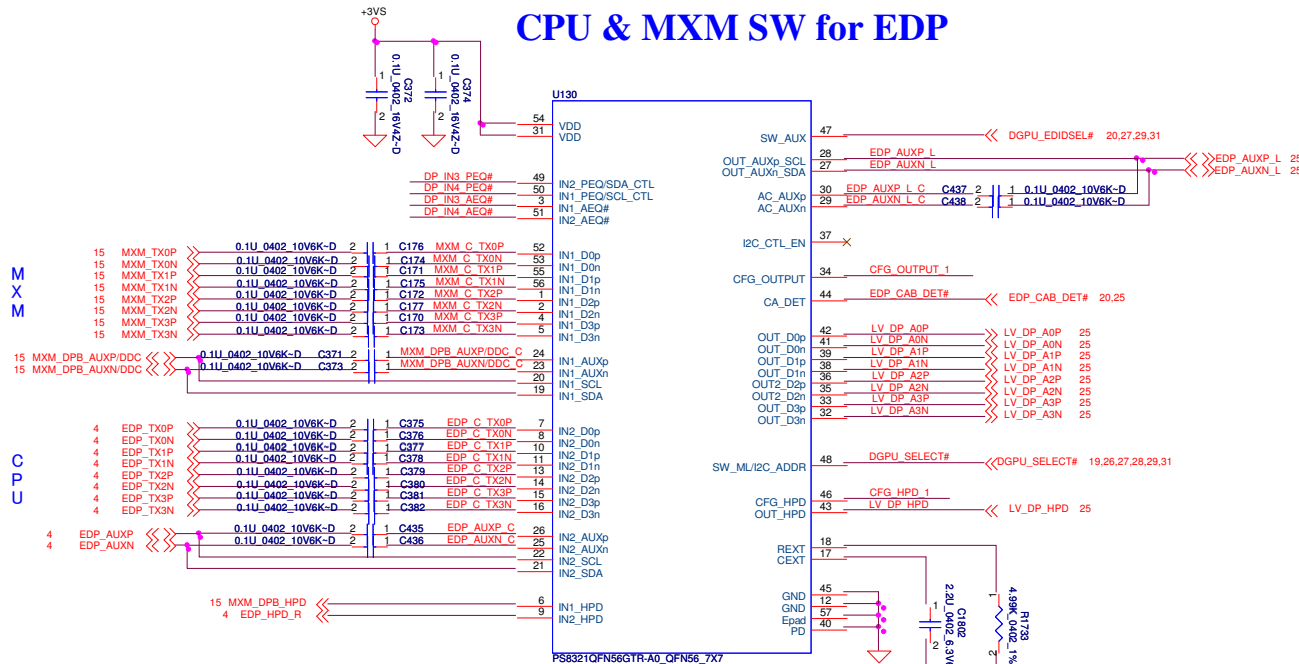
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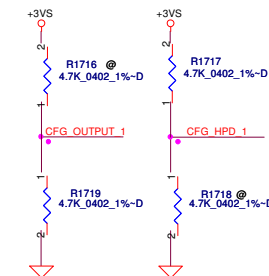
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Title			
PCH (8/8) VSS			
LA-8341P			
Date: Friday, March 02, 2012	Sheet 24	of 71	Rev 1.0

CPU & MXM SW for EDP



CFG_OUTPUT: output configuration
L: Output is tracking DPCD register setting (auto interception)
H: Output swing level fixed at 600mV and no pre-emphasis
M: Output swing level is fixed at 400mV and no pre-emphasis



MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

AUX_SEL/SEL1&2	Channel	Source
0	A	CPU
1	B	MXM

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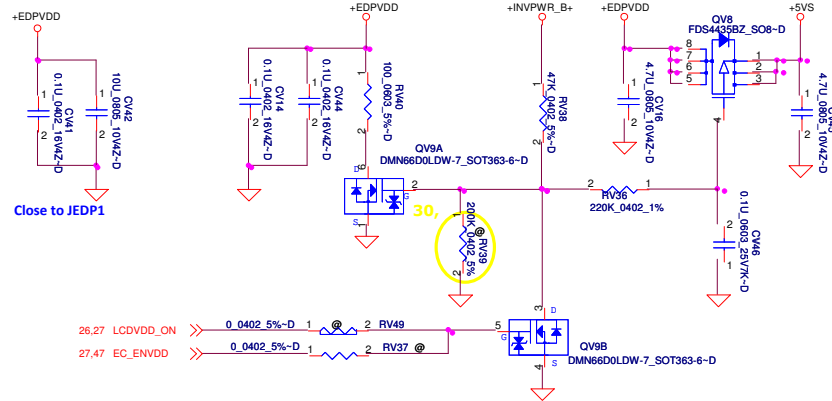


eDP SW- GPU & CPU			
Size	Document Number	Rev 1.0	
LA-8341P			
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eDP POWER

W=60mils



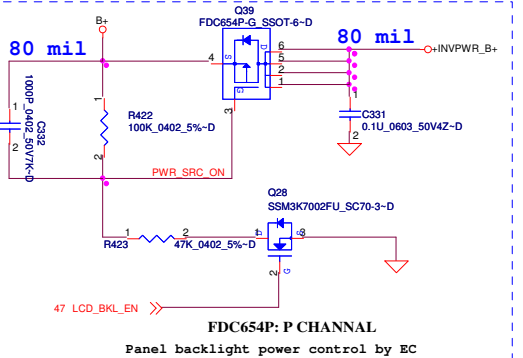
Back light power

80 mil

80 mil

Inverter power

FBMA-L11-201209-221MA30T_0805
80 mil



4028

CPU/MXM



CPU/MXM

0908 pin 28 with new feature, different with ex-version

Reserve

Link Done

IP4223C26_S06-D

DMIC0 DMIC0 DMIC0 DMIC0

DMIC0 DMIC0 DMIC0 DMIC0

DMIC0 DMIC0 DMIC0 DMIC0

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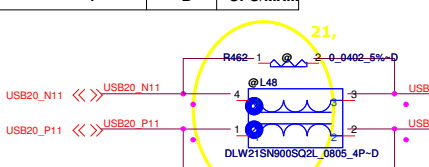
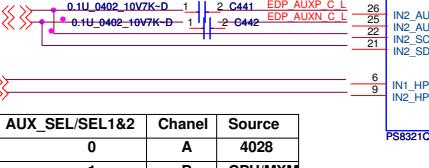
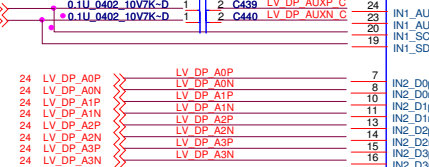
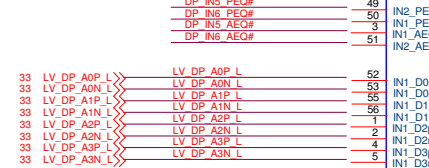
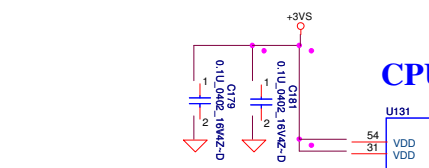
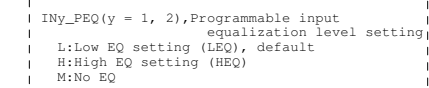
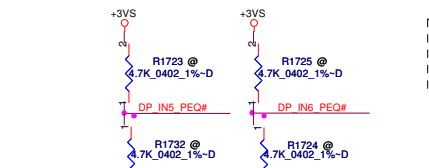
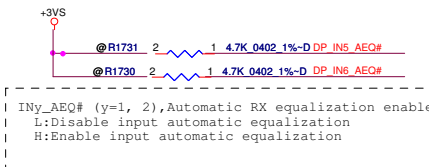
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DMIC0 DMIC0 DMIC0 DMIC0

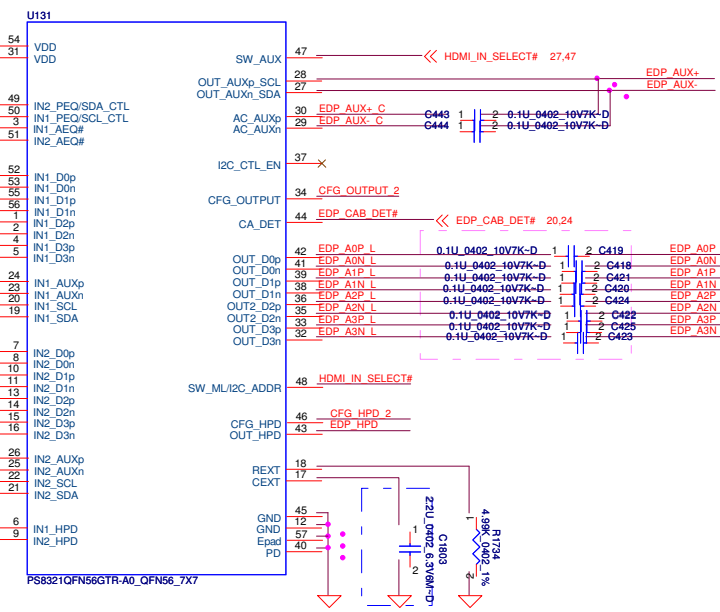
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DMIC0 DMIC0 DMIC0 DMIC0

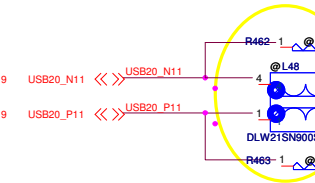
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CPU/GPU & 4028 SW for DPB



AUX_SEL/SEL1&2	Chanel	Source
0	A	4028
1	B	CPU/MXM



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Title	eDP SW- 4028 & eDP CONN
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Date	Friday, March 02, 2012
Sheet	26 of 71
Rev	1.0

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS

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Compal Electronics, Inc.

Title **LVDS SW- 1 to 2 & GPU/PCH**

LA-8341P

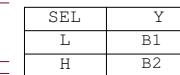
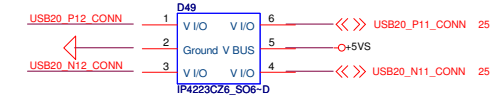
Rev
1.0

Date: Friday, March 02, 2012

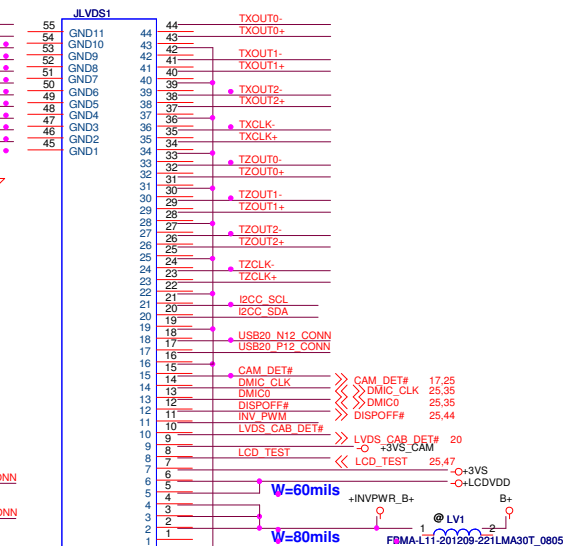
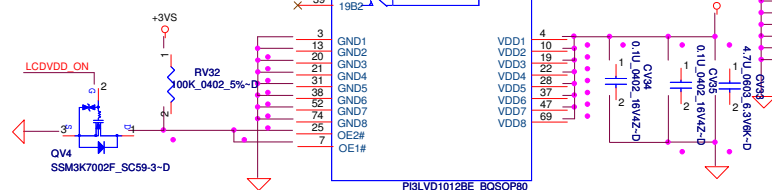
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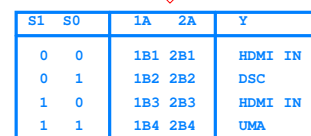
PCH/GPU MUX & 6038 MUX SW for LVDS



LVDS Conn.



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**LVDS SW- 6038/SYSTEM & CONN**

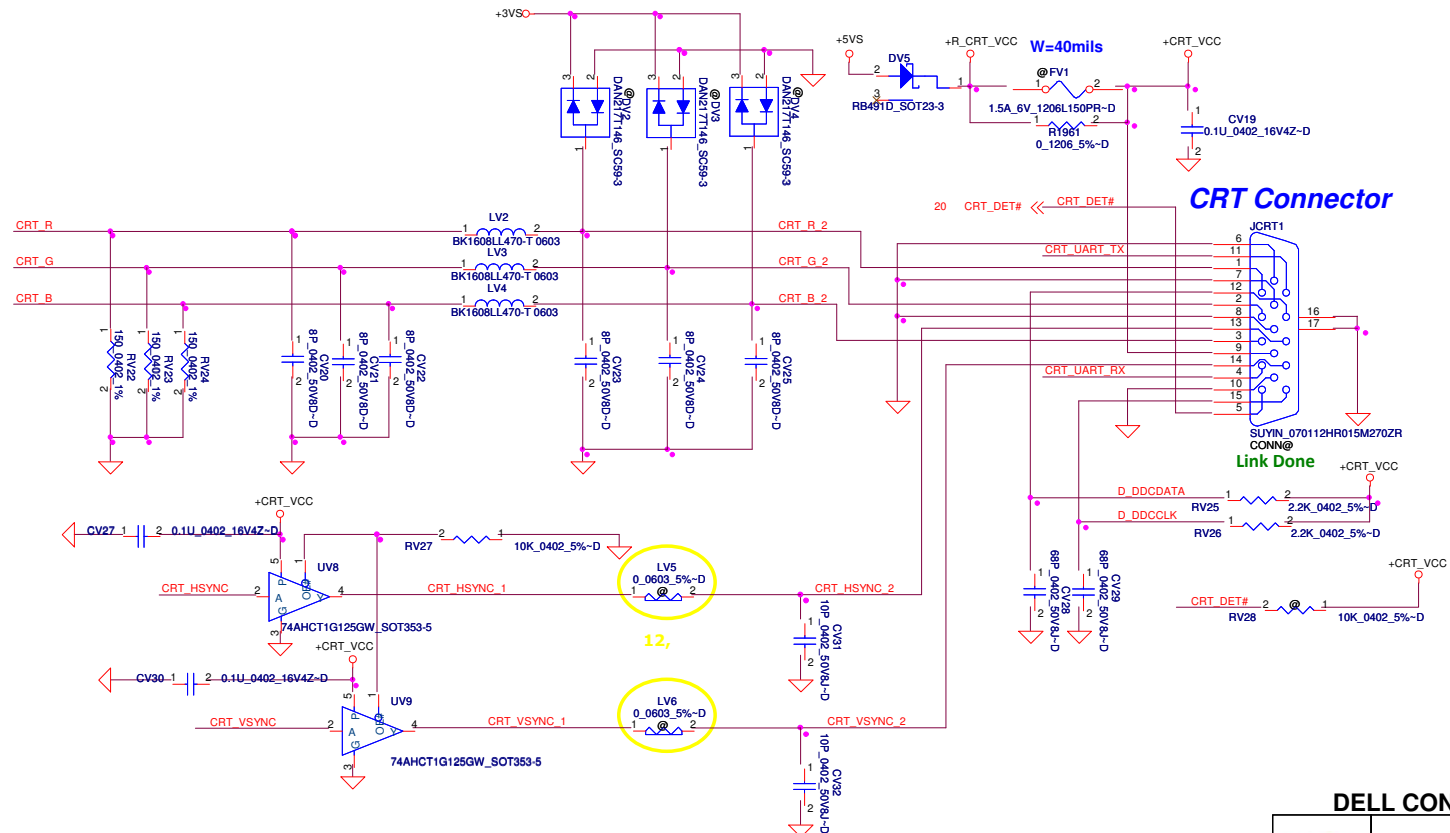
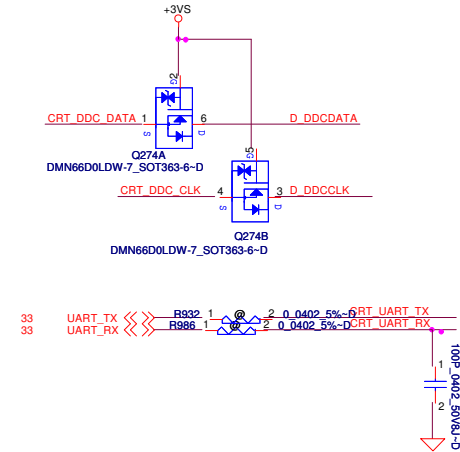
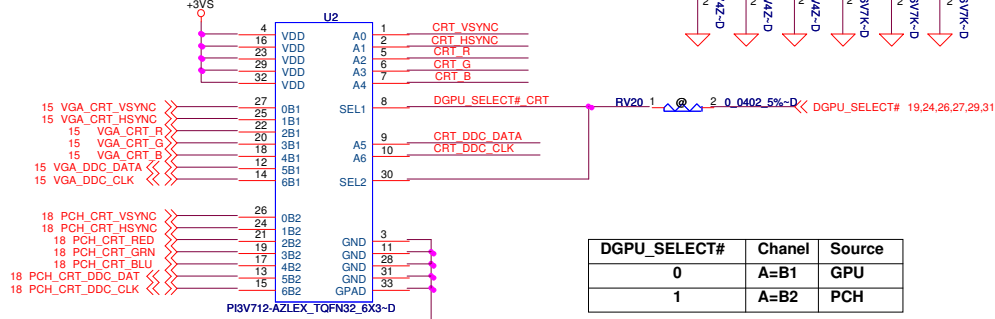
Size	Document Number
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LA-8341P

Rev	
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Date: Friday, March 02, 2012 Sheet 28 of 71

VGA SW for PCH / GPU

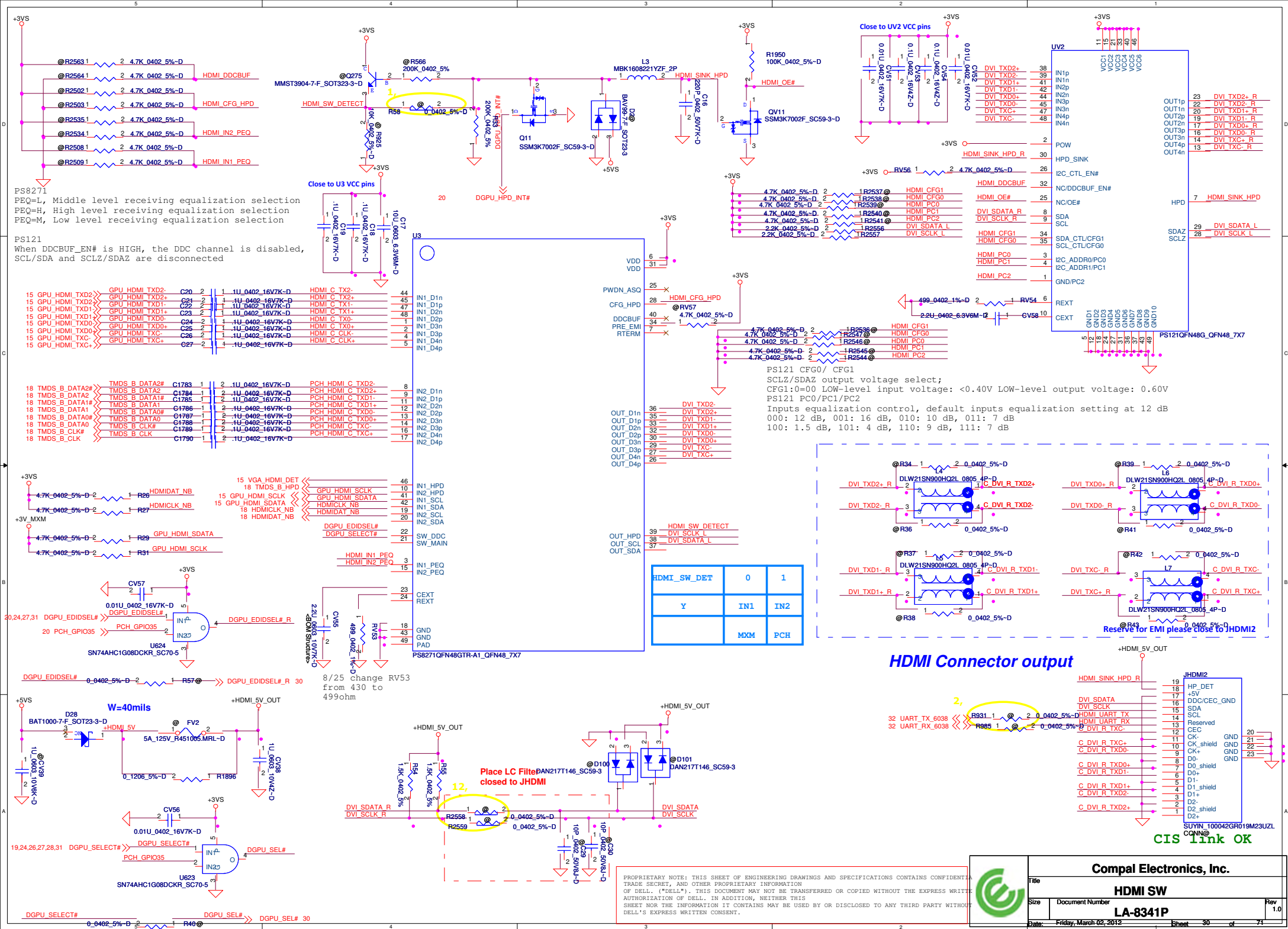


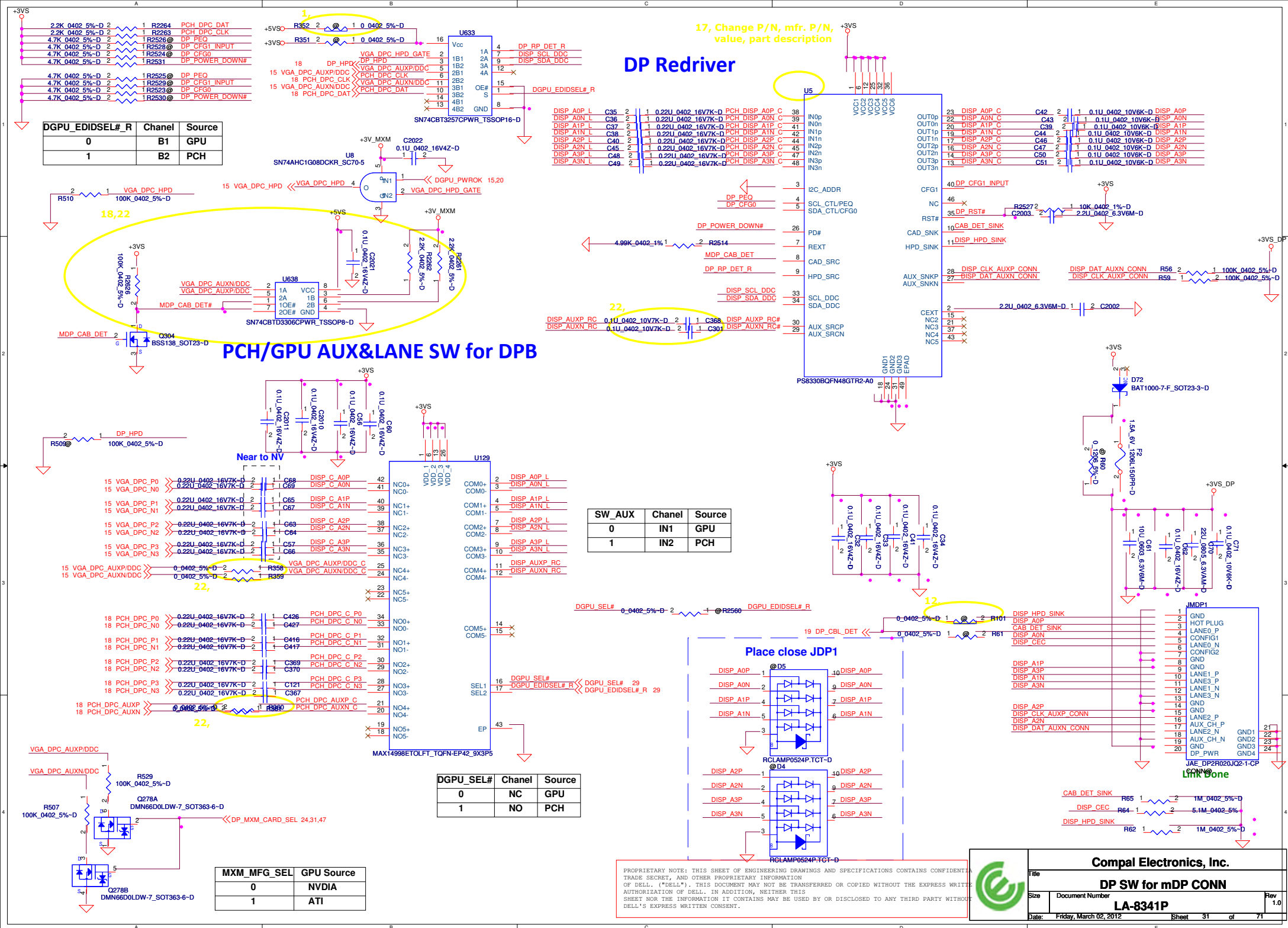
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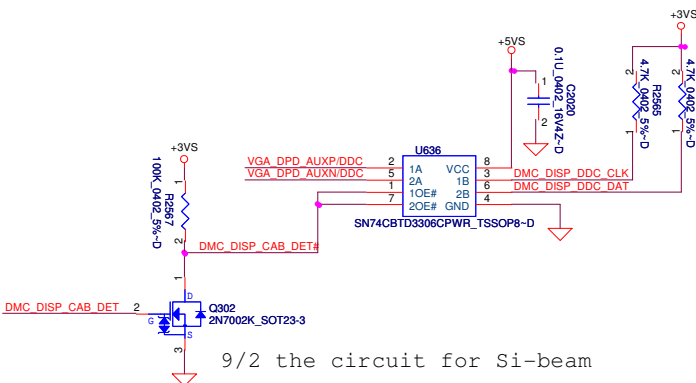
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Title			
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Size	Document Number	Rev	
	LA-8341P	1.0	
Date	Friday, March 02, 2012	Sheet	29 of 71

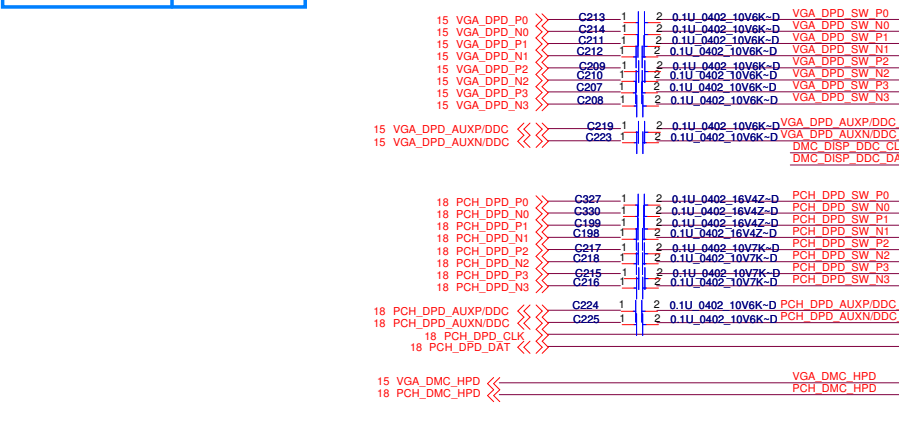




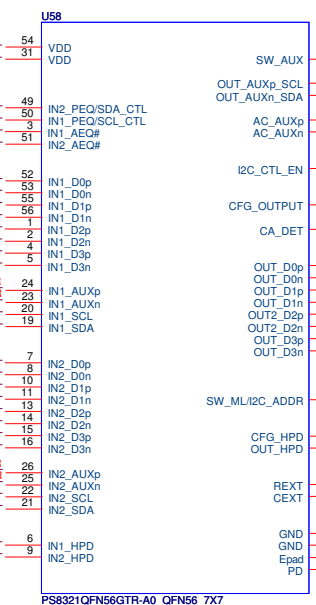


DMC_DISP_CAB_DET	DMC_card
0	Cavium
1	Si-beam

9/2 the circuit for Si-beam



PCH/GPU AUX&LANE SW for DPB

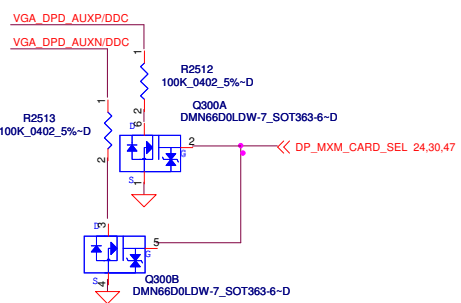
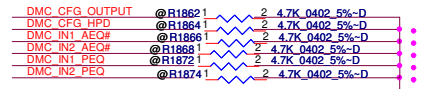
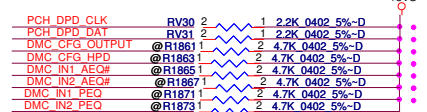


SW_ML/I2C_ADDR	Chanel	Source
0	IN1	GPU
1	IN2	PCH

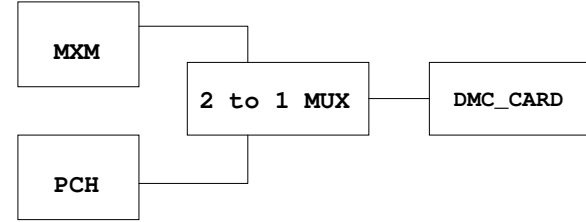
PIN46: CFG_HPD (Internal pull-down 150K), Currently setting : HPD is switched by SW_ML pin.

PS8321
Iny_PEQ1=
L: Low EQ setting (LEQ), default
H: High EQ setting (HEQ)
M: No EQ
Iny_AEQ# (y=1, 2) =:
L: Enable input automatic equalization
H: Disable input automatic equalization

CFG_OUTPUT =:
L: Output is tracking DPCD register setting (auto interception)
H: Output swing level fixed at 600mV and no pre-emphasis
M: Output swing level is fixed at 400mV and no pre-emphasis



MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

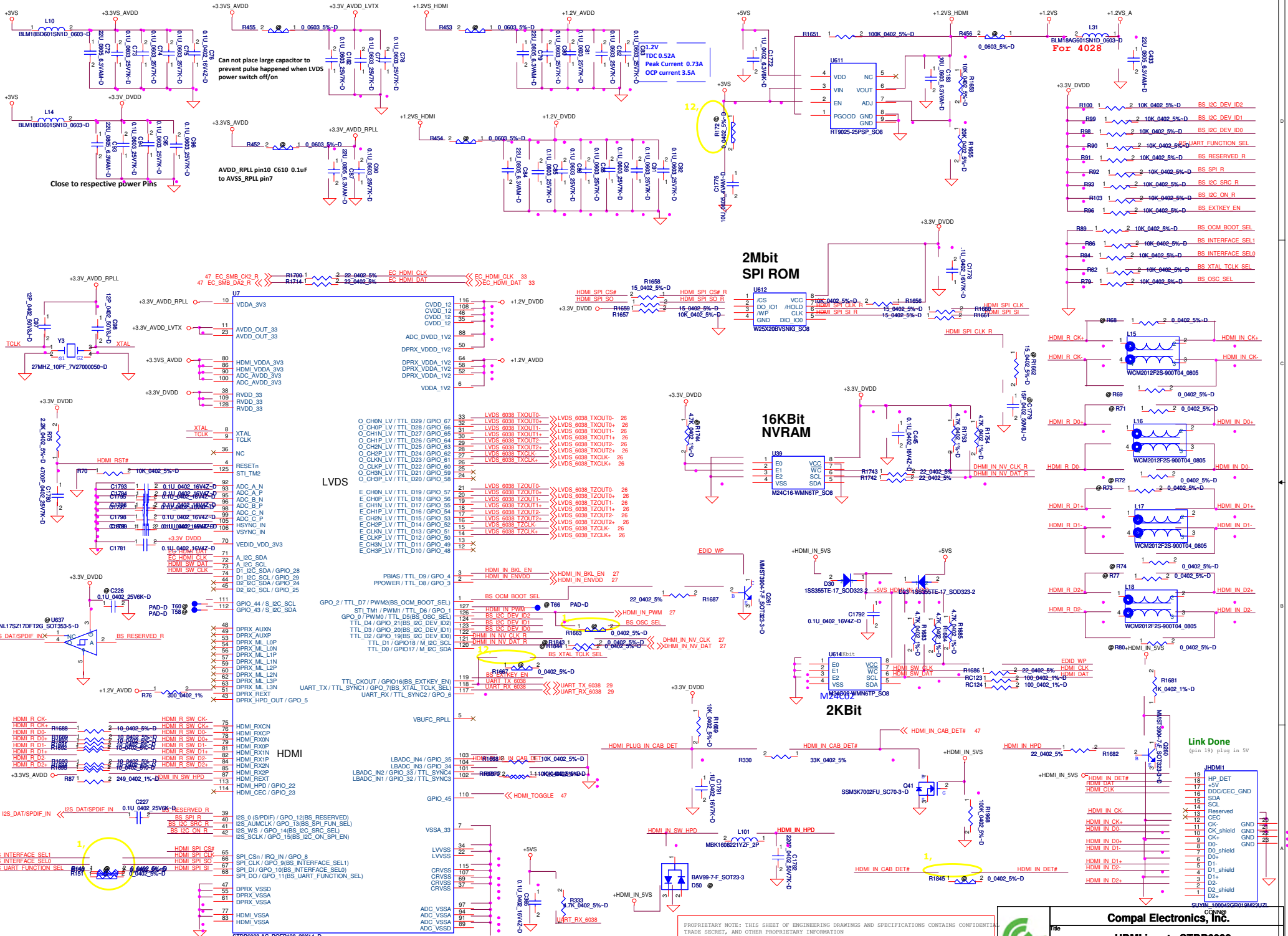


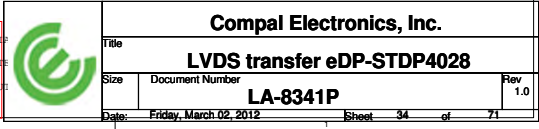
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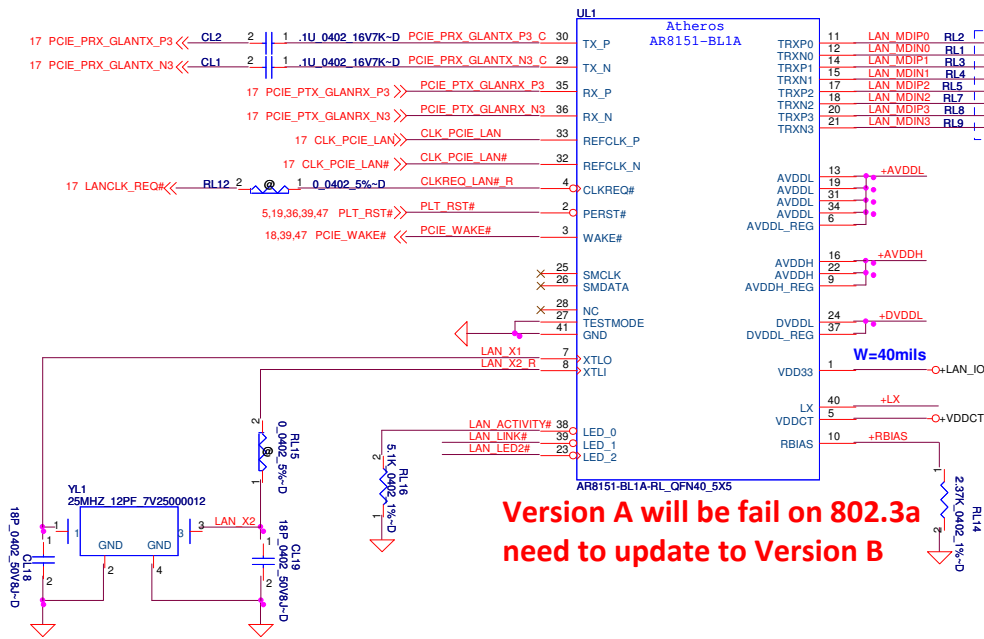


Compal Electronics, Inc.			
HDMI SW for DMC			
Title	Document Number	Rev	1.0
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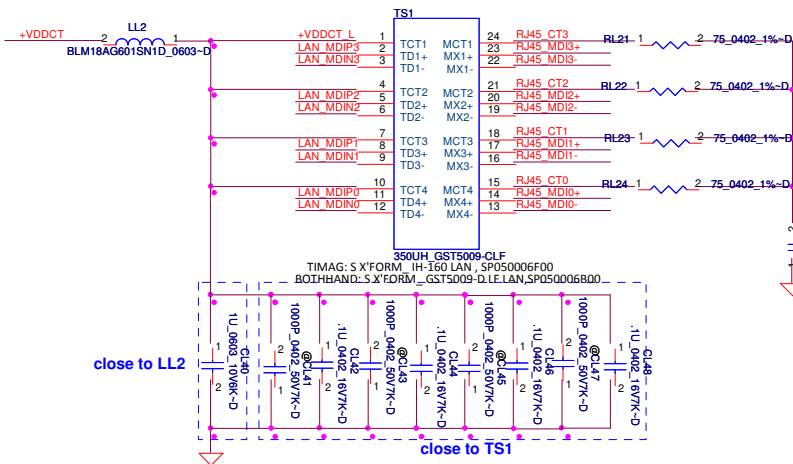
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Version A will be fail on 802.3a
need to update to Version B

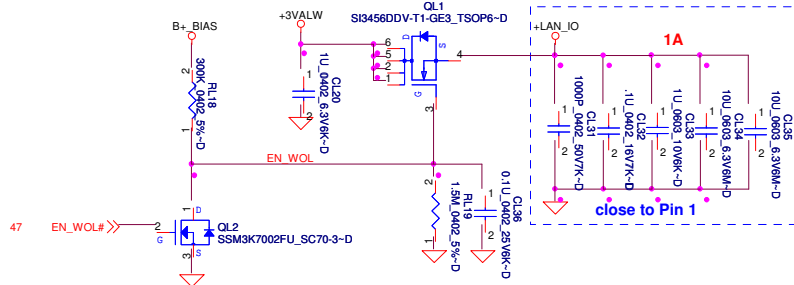


close to LL2

close to TS1

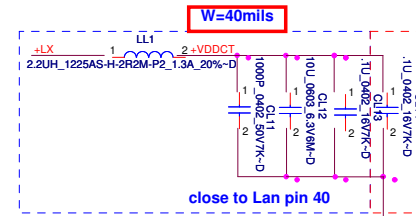
W=40mils

W=40mils



close to Pin 1

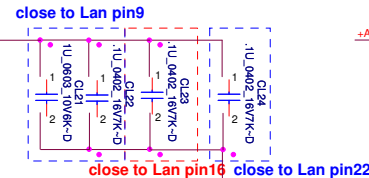
close to Lan chip 1000p reserved for EMI



close to Lan pin 40

close to Lan pin5

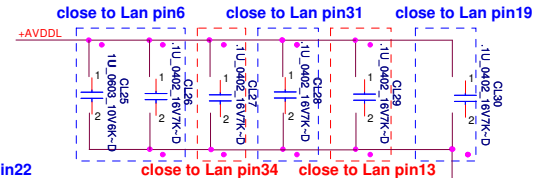
W=20mils



close to Lan pin9

close to Lan pin22

W=20mils



close to Lan pin6

close to Lan pin31

close to Lan pin19

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Compal Electronics, Inc.

GLAN AR8151 AL1A

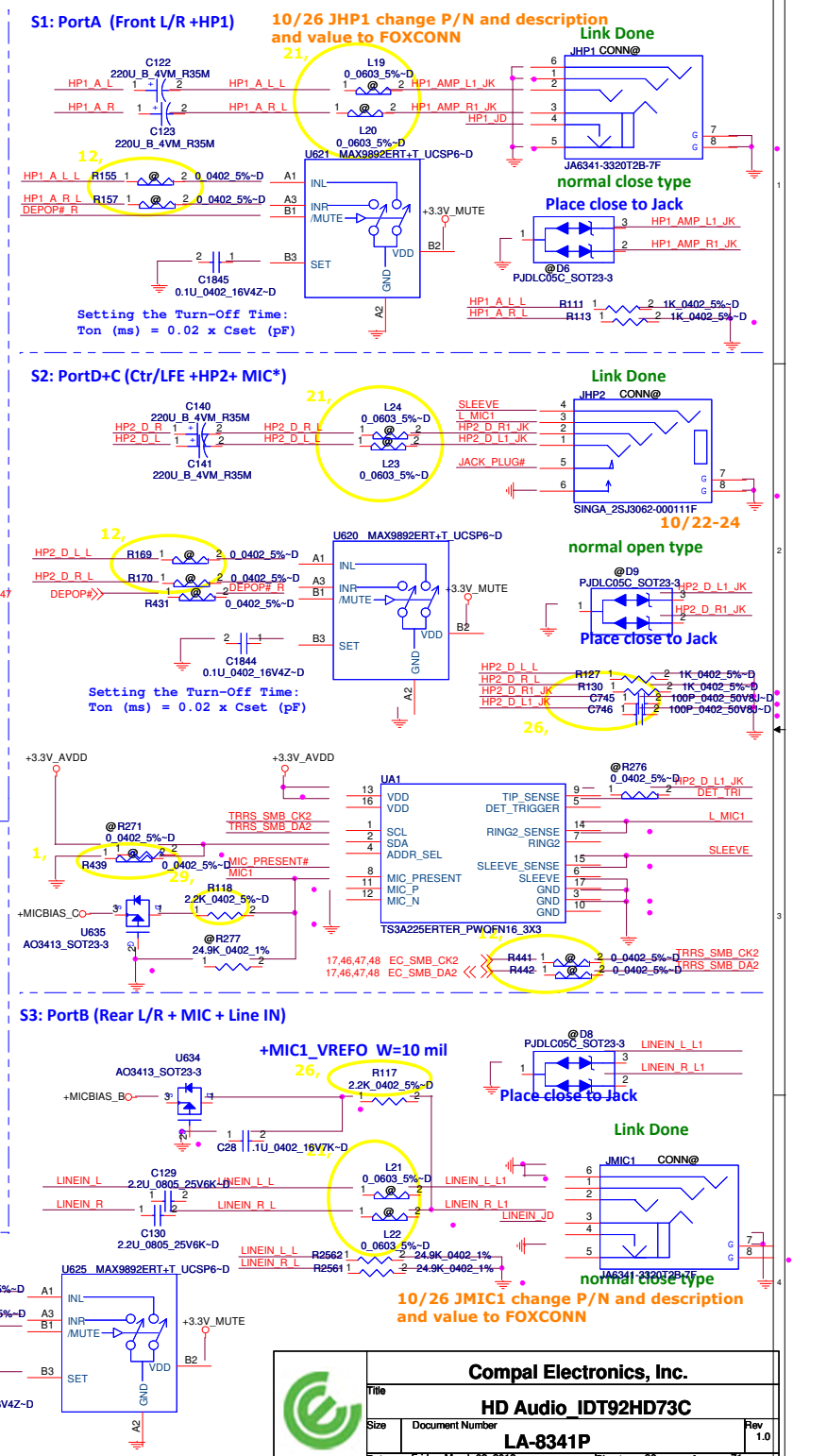
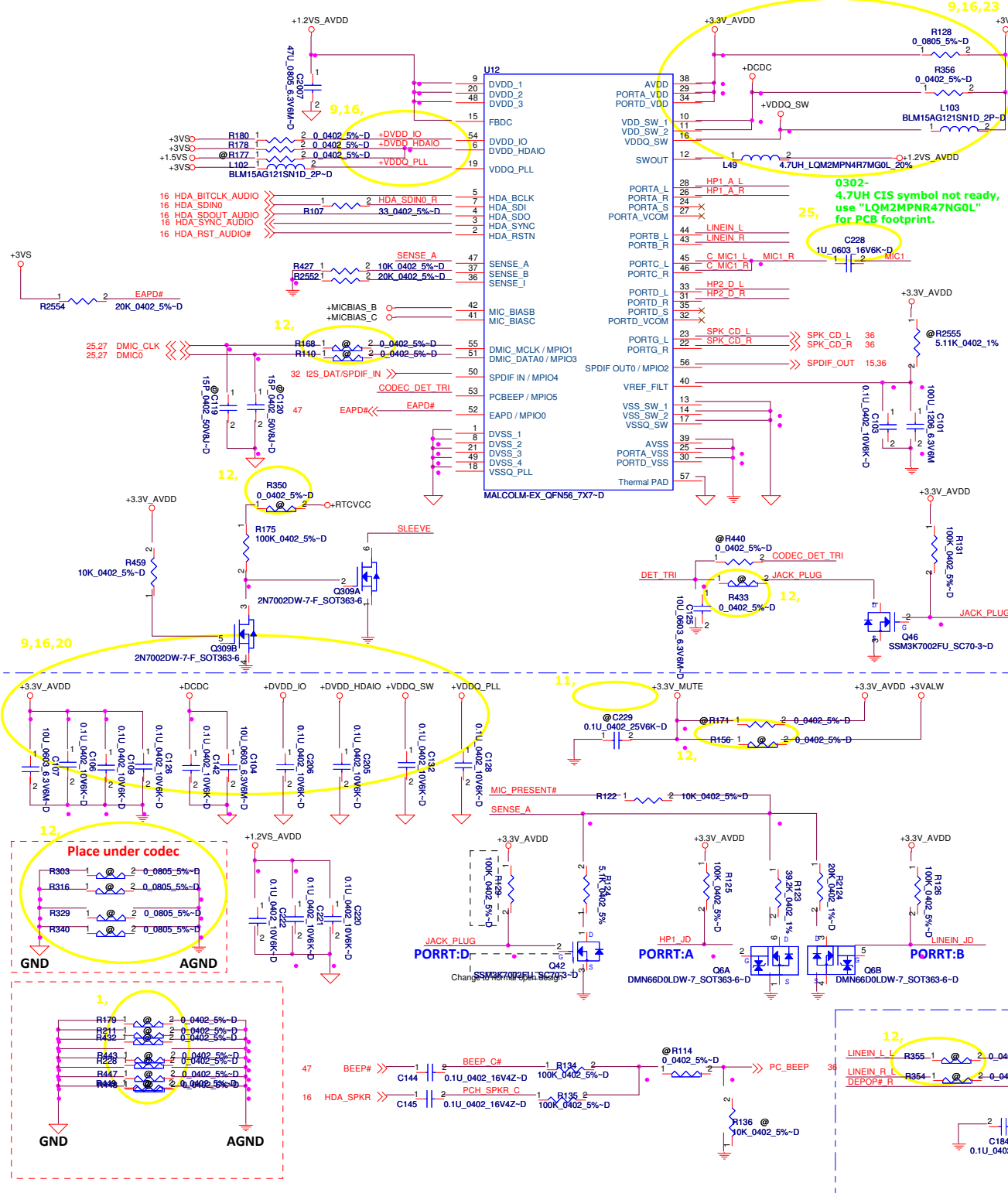
LA-8341P

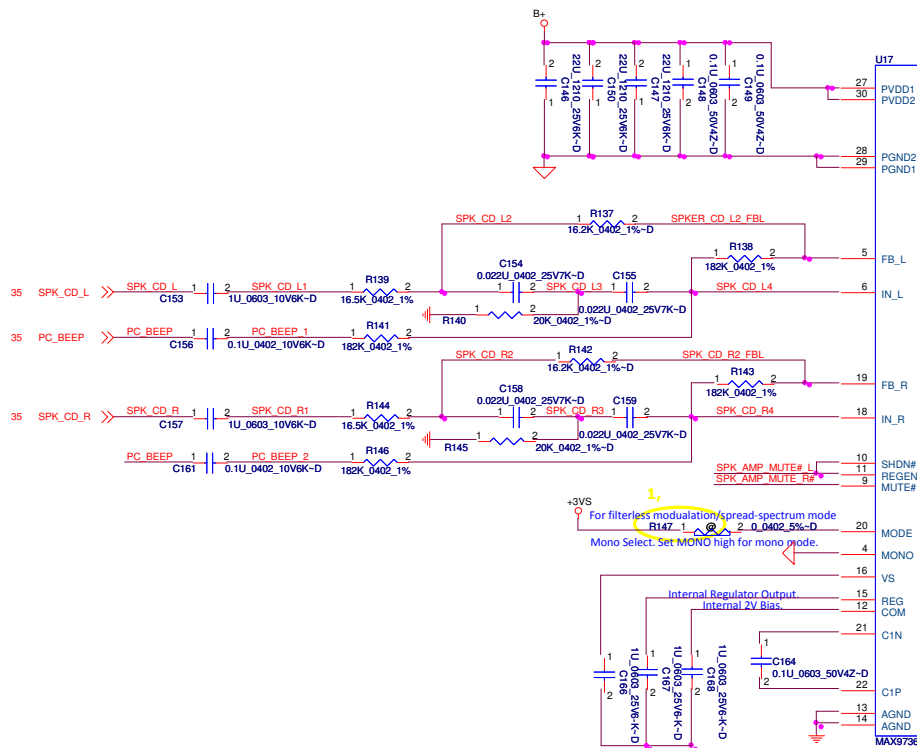
Rev 1.0

Date: Friday, March 02, 2012

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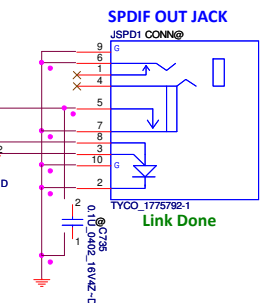
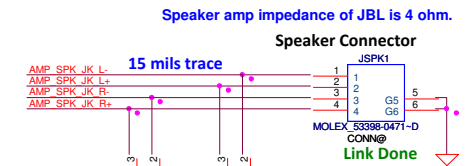
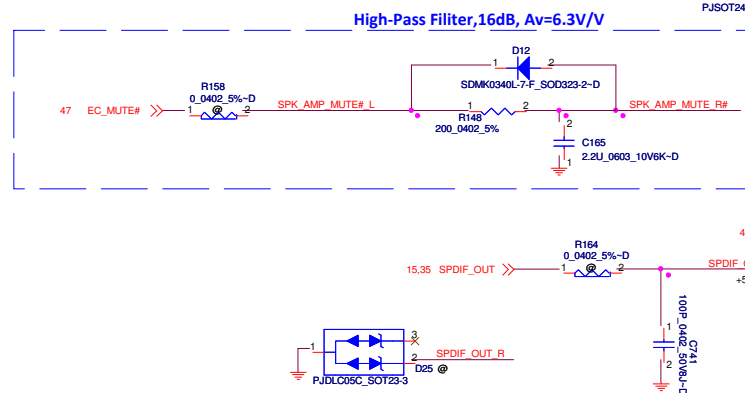
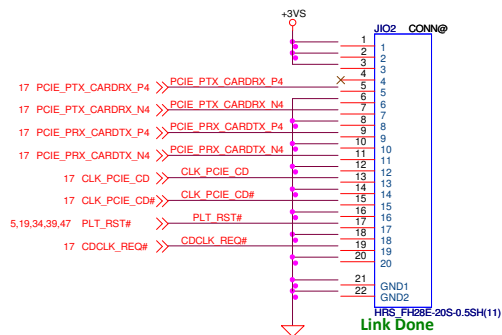
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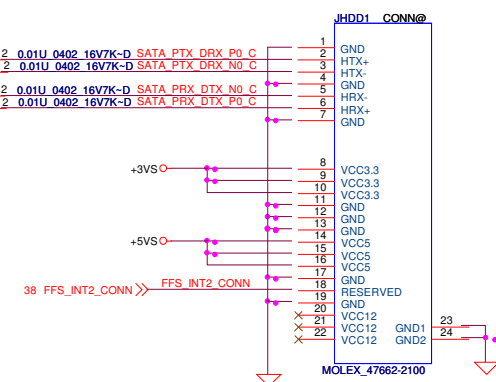
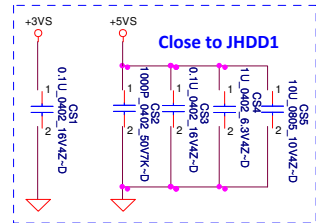
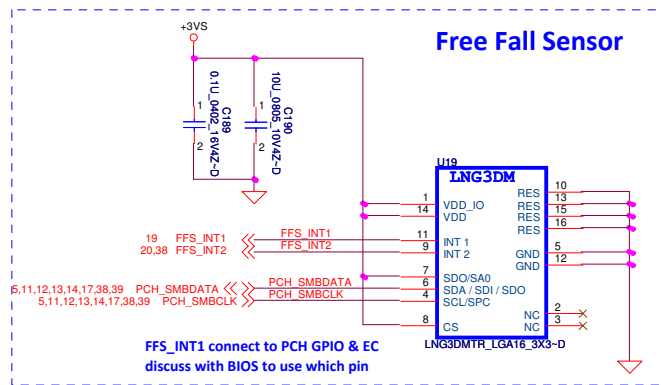
Layout note:
Please place below components on moat
between A GND and D GND.
(R119, R147, R155, R157, R158, R164)

Card Reader/B CONN

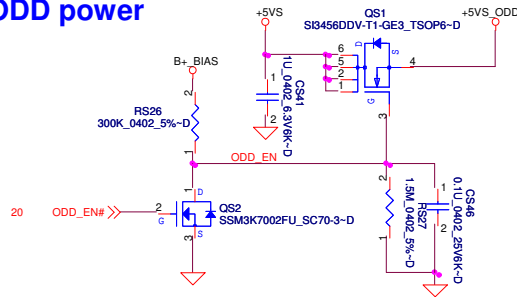


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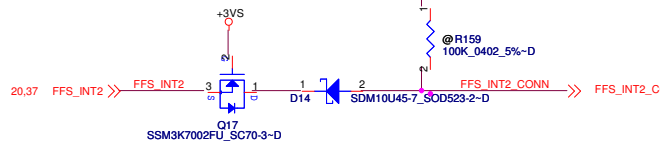
		Compal Electronics, Inc.	
		Speaker AMP / CardReader B conn	
Size	Document Number	LA-8341P	
File	Friday, March 02, 2012	Sheet	37 of 71



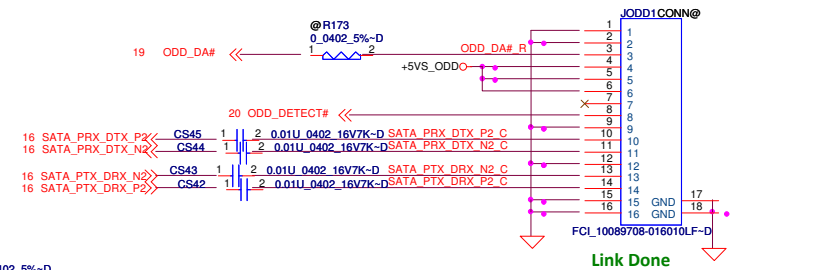
ODD power



Placea caps. near ODD CONN.

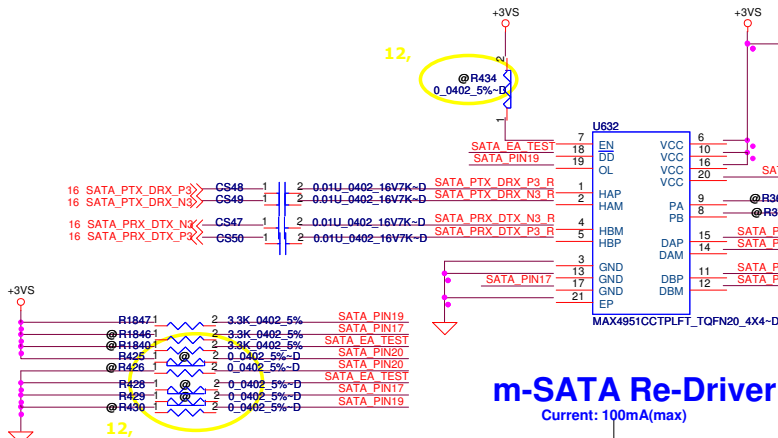
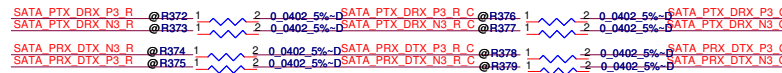
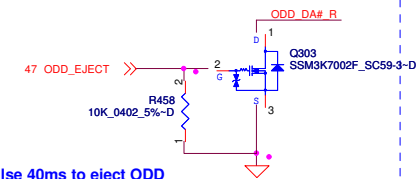


SATA ODD Conn.



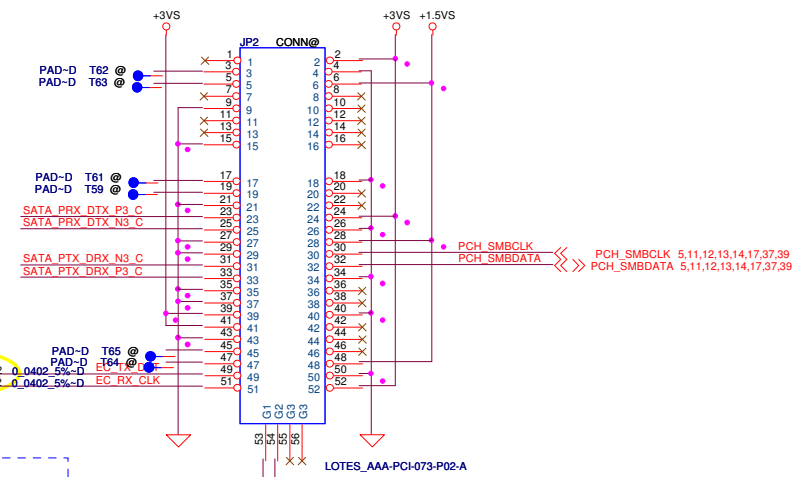
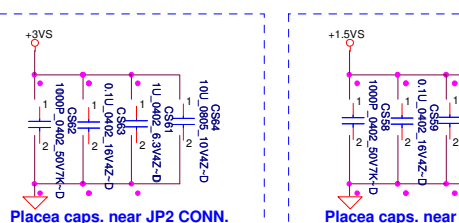
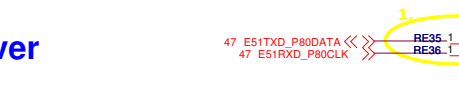
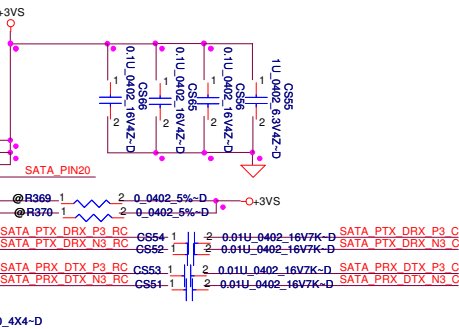
- 1, Host generate Low pulse 40ms to eject ODD
- 2, After this pulse, signal remain high and no pulse is allowed within 7s

9/5 follow JMINI1 connector usage



m-SATA Re-Driver

Current: 100mA(max)



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SATA HDD3 & ODD & FFS

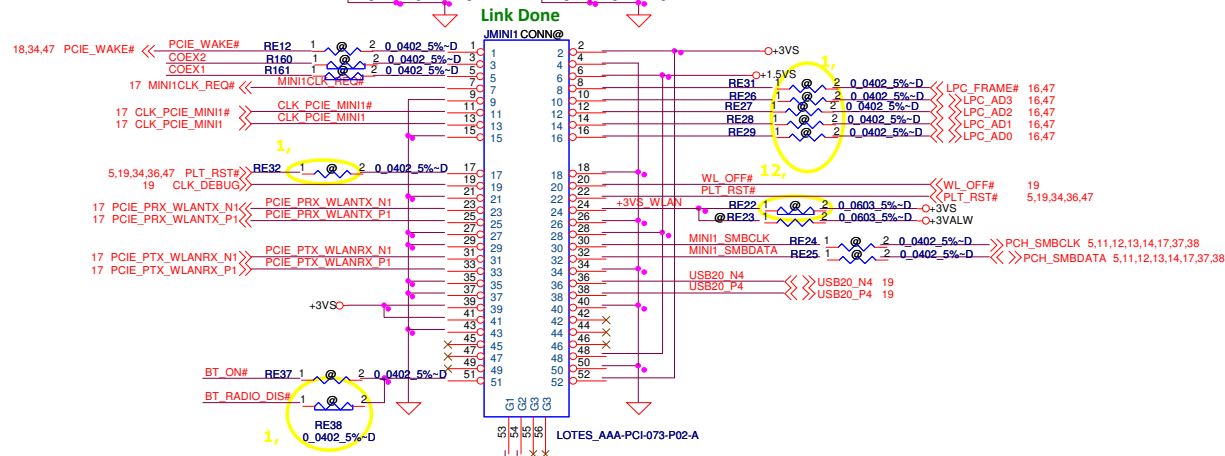
LA-8341P

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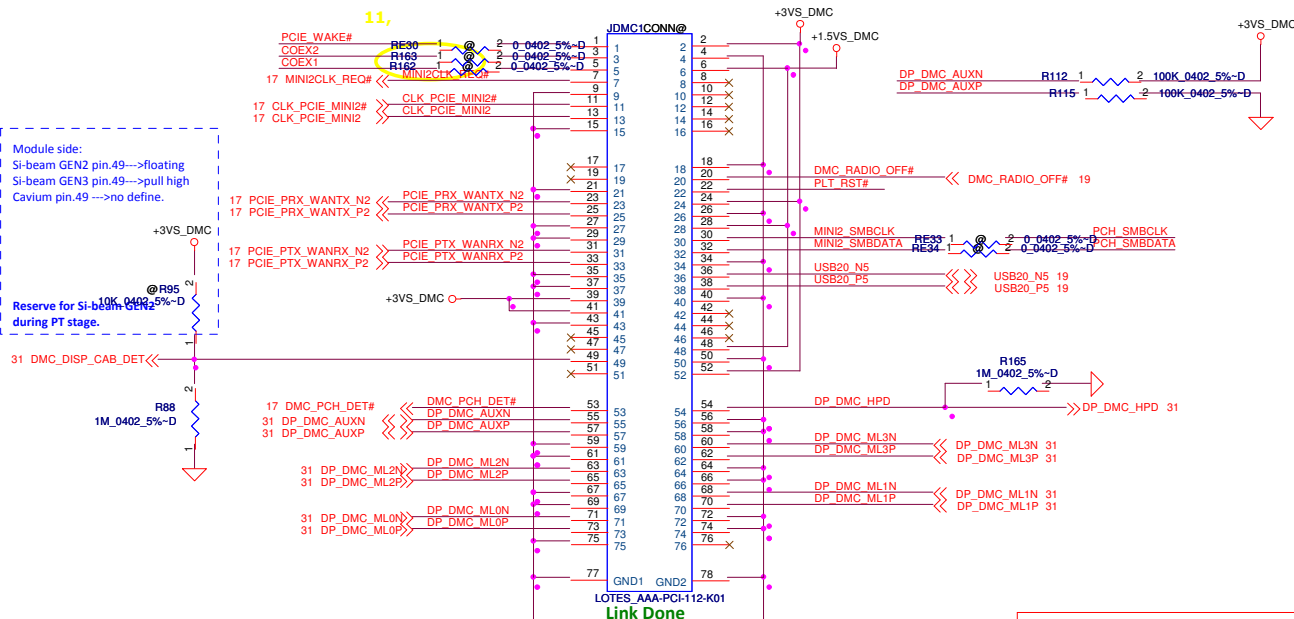
WLAN



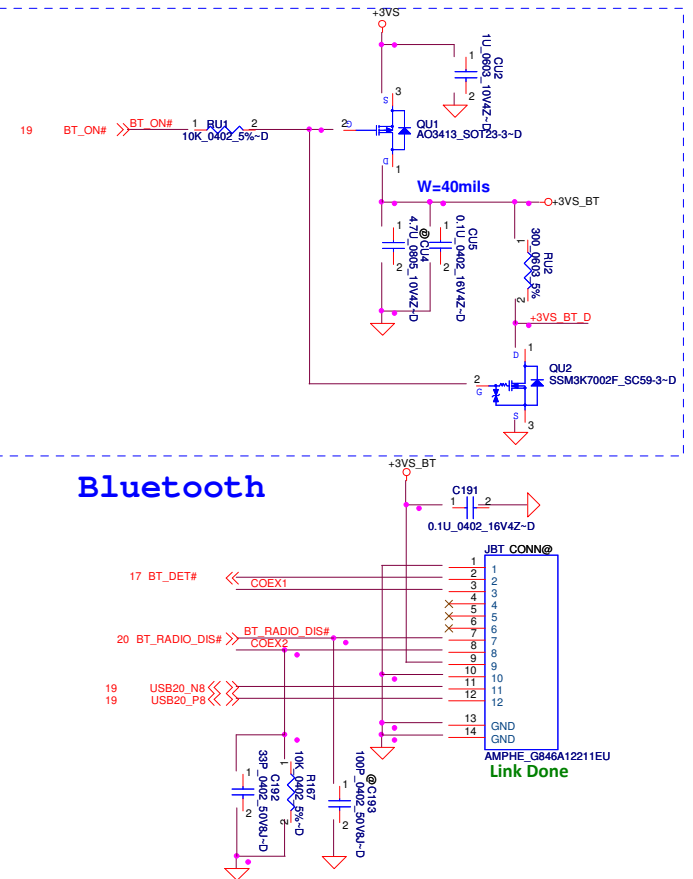
Display Mini Card (DMC)

Module side:
Si-beam GEN2 pin.49-->floating
Si-beam GEN3 pin.49-->pull high
Cavium pin.49 -->no define.

Reserve for Si-beam GEN2 during PT stage.

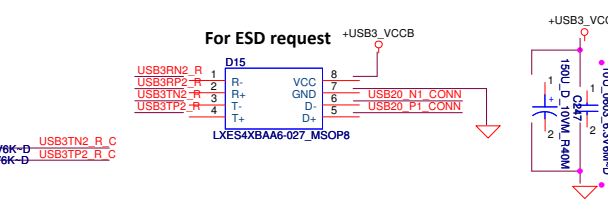
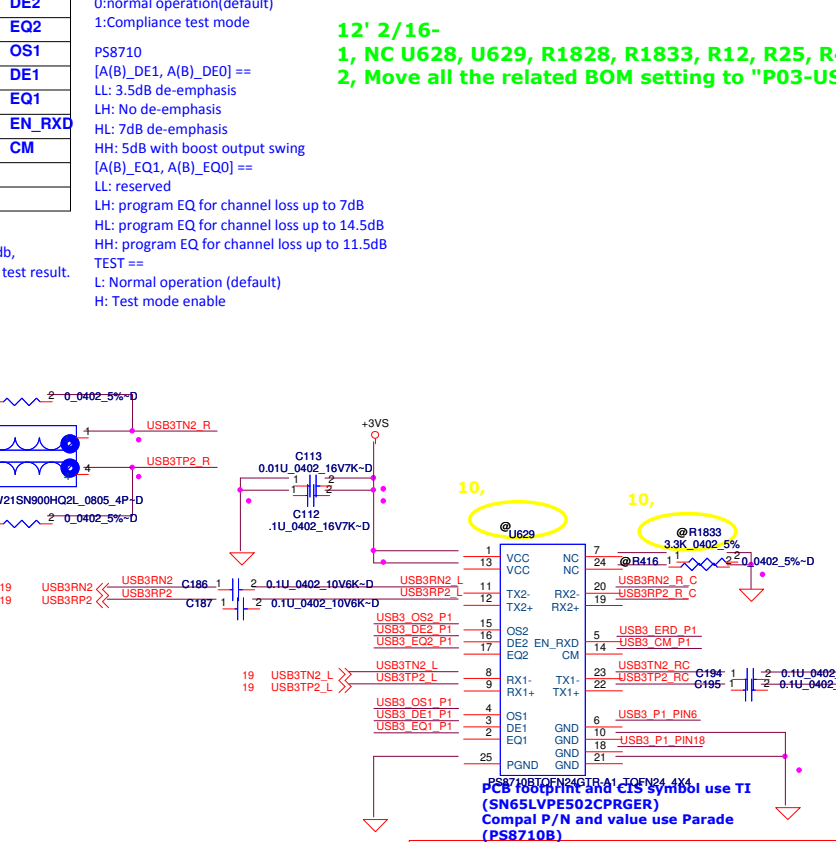
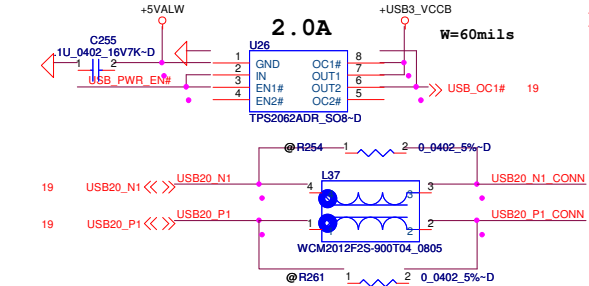


Bluetooth



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Compal Electronics, Inc.			
Mini Card WLAN / DMC / BT			
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Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

[Parade suggest]
PS8710 AEQ0,BEQ0 adjust 7db,
REXT use 3.3 K well get btter test result.

```

SN65LVPE502
EN==
1:normal operation(default)
0:sleep mode
CM==
0:normal operation(default)
1:Compliance test mode

PS8710
[A(B)_DE1,A(B)_DE0] ==
L1: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis
HH: 5dB with boost output swing
[A(B)_EQ1,A(B)_EQ0] ==
LH: reserved
LH: program EQ for channel loss up to 7dB
HH: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB
TEST ==
L: Normal operation (default)
H: Test mode enable

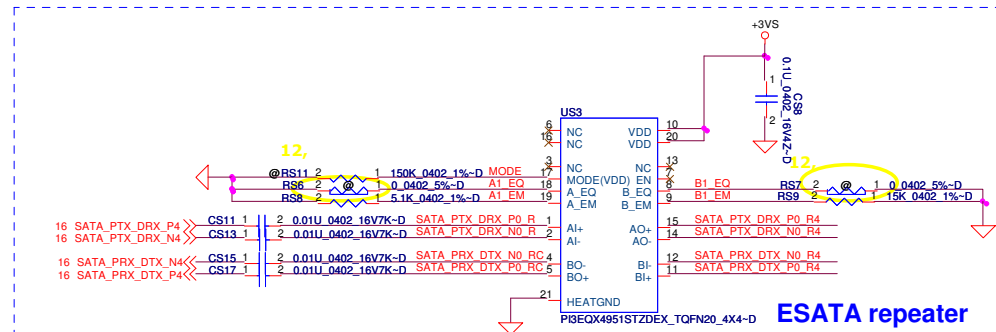
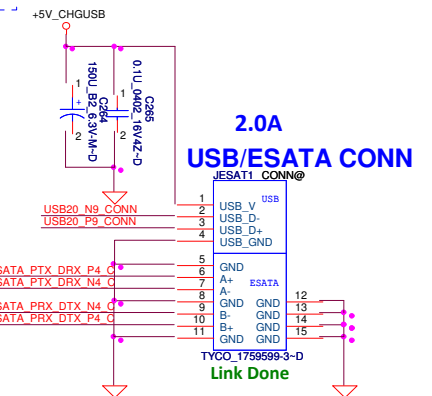
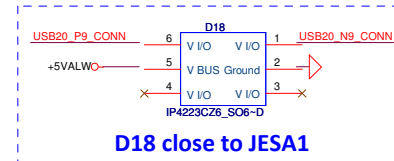
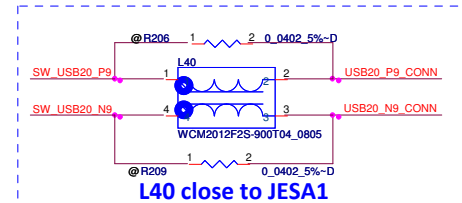
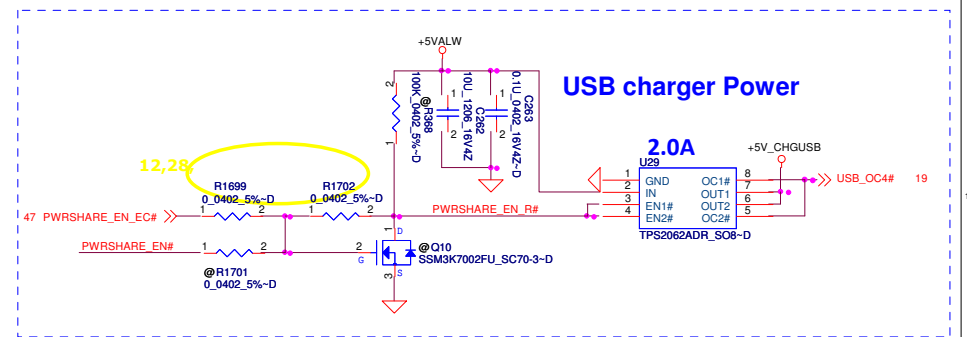
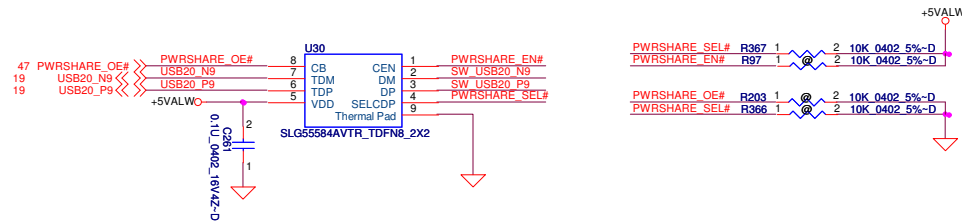
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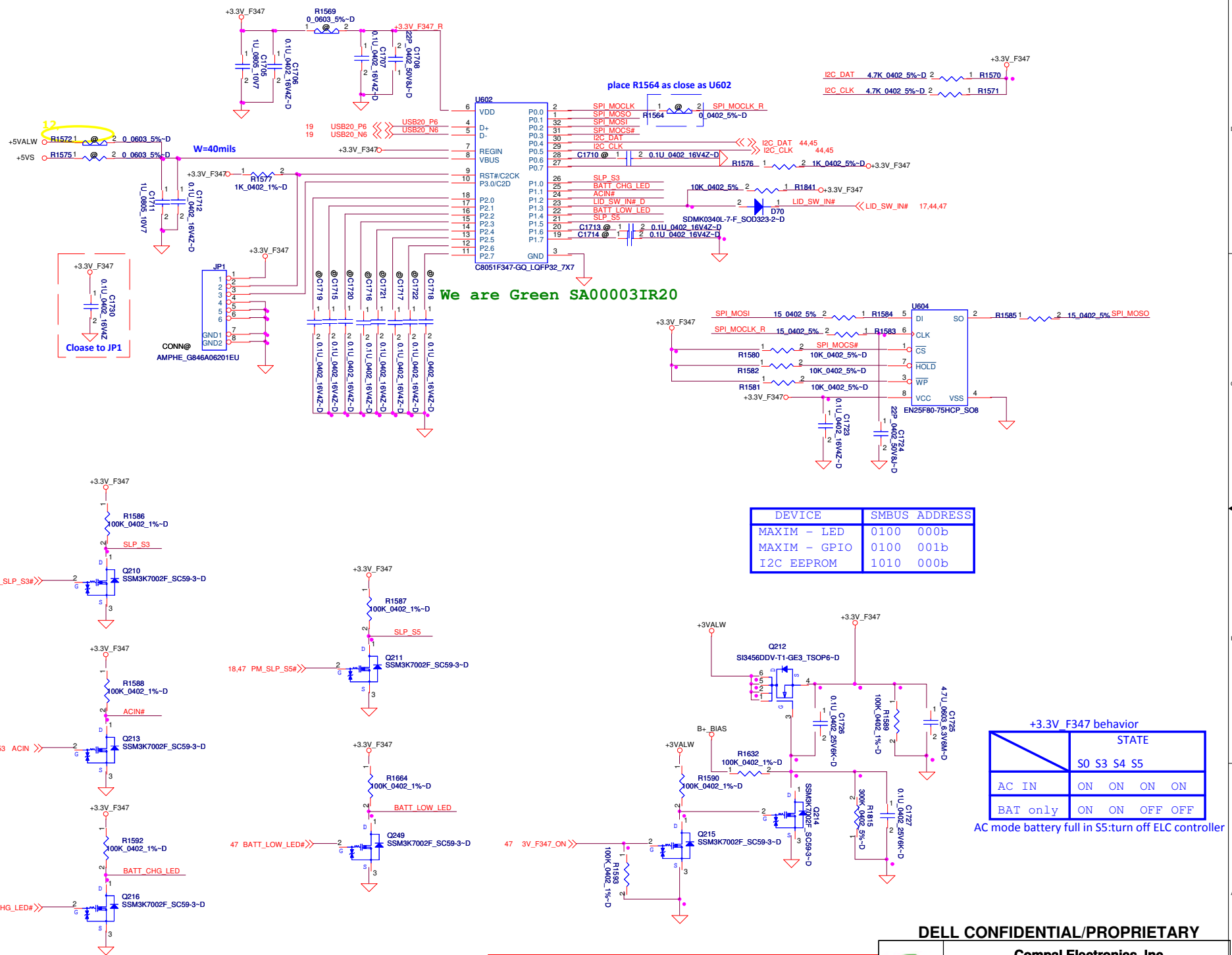
12' 2/16-
1, NC U628, U629, R1828, R1833, R12, R25, R47, R46
2, Move all the related BOM setting to "P03-USB 3.0 Config setting"

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Power share



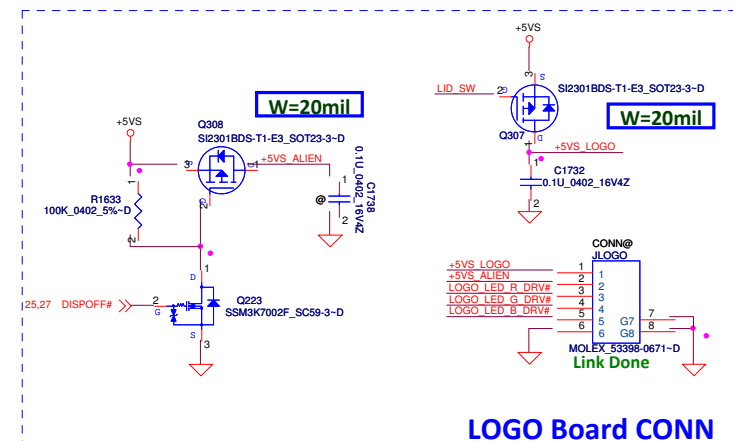
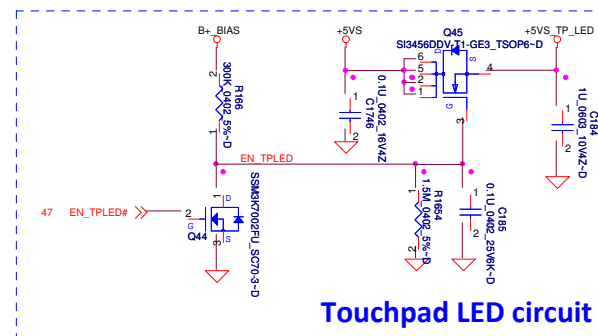
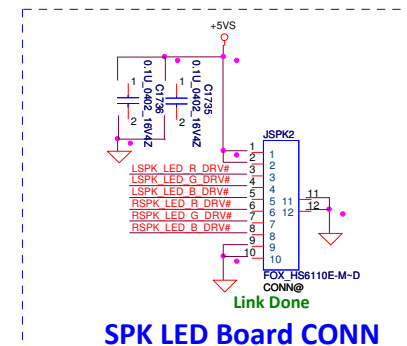
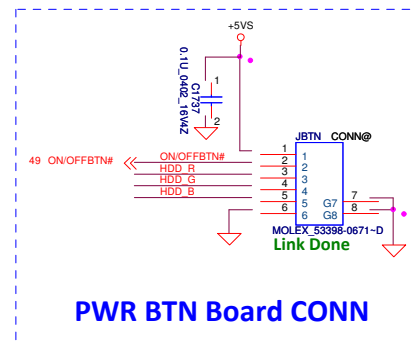
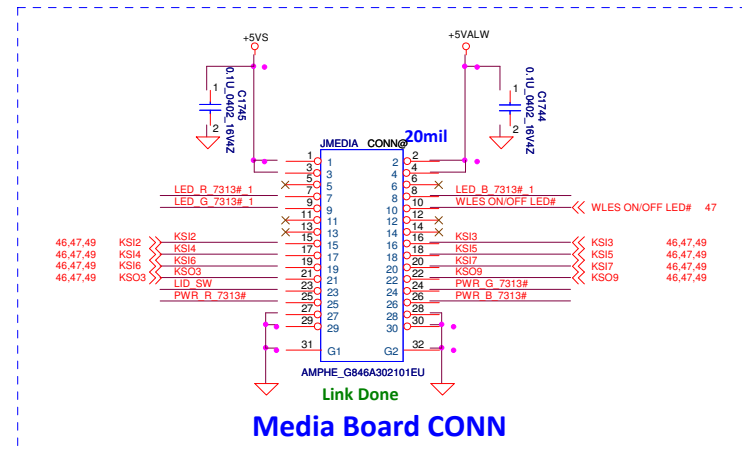
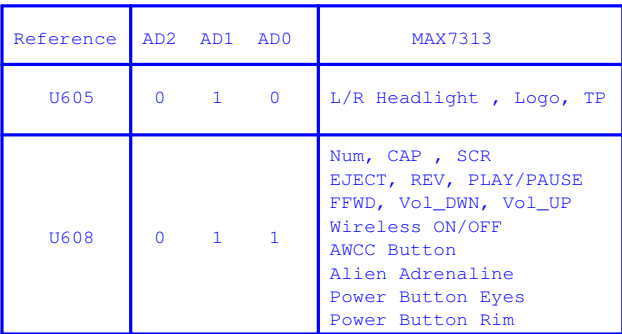


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Title			
ELC (1)			
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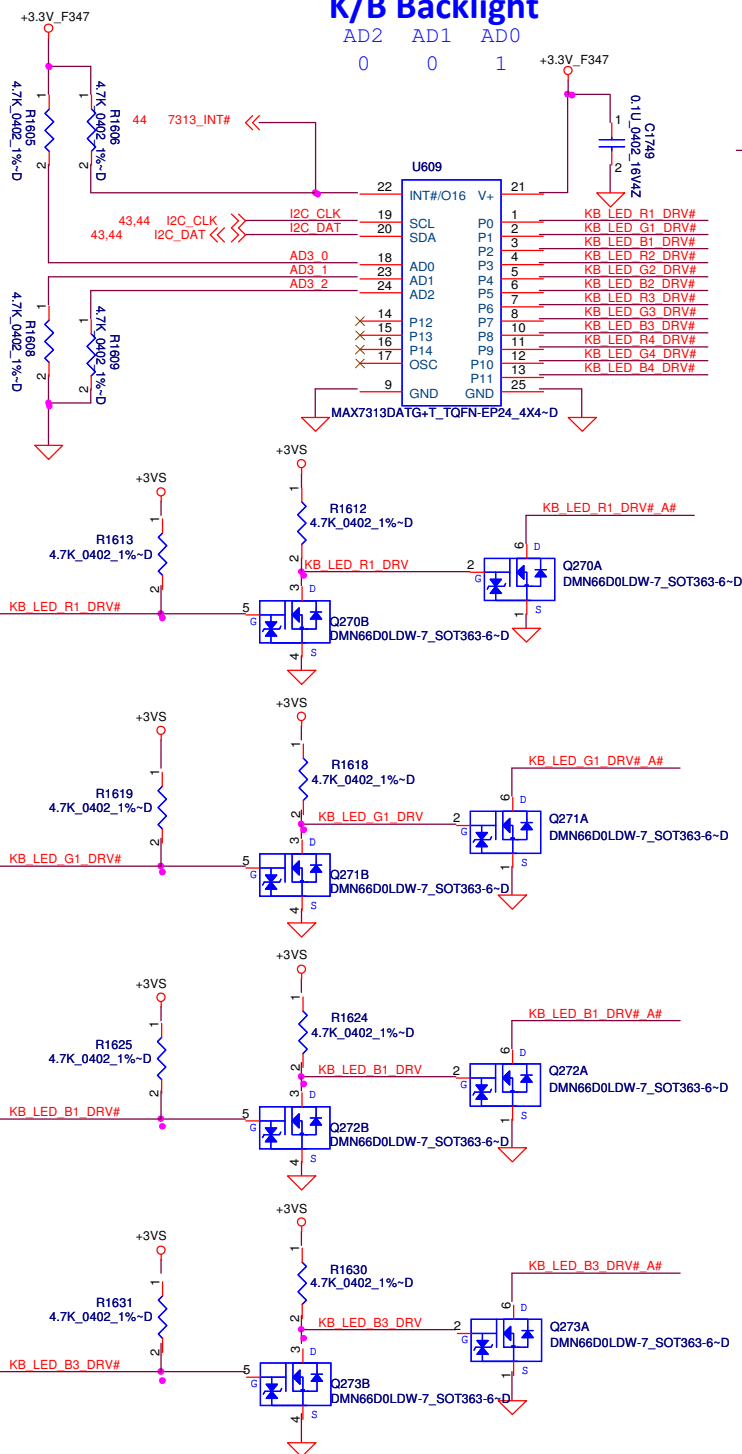


	Compal Electronics, Inc.			
	Title			
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	Size	Document Number		
	LA-8341P			Rev
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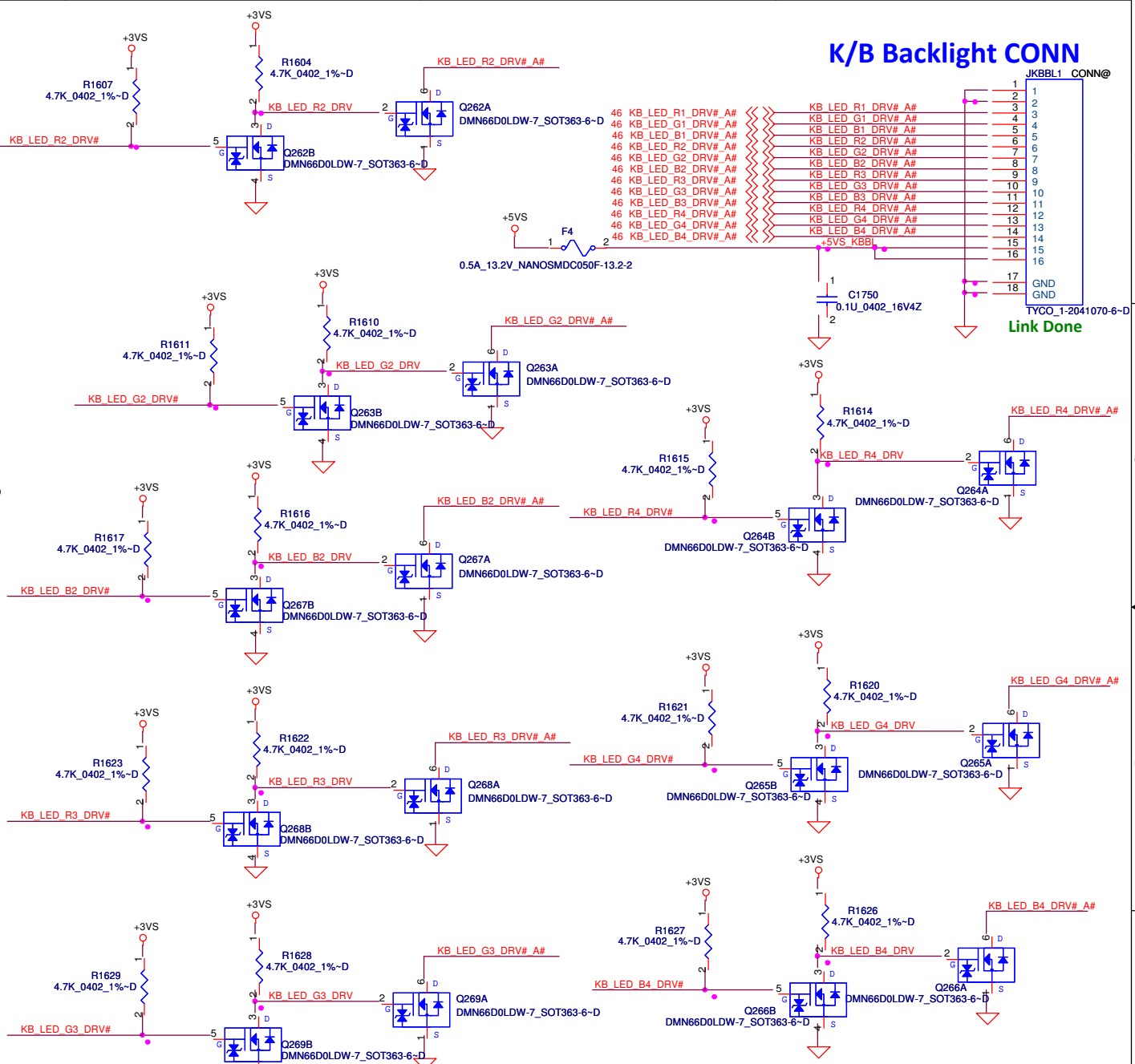
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K/B Backlight

AD2 AD1 AD0
0 0 1



K/B Backlight CONN

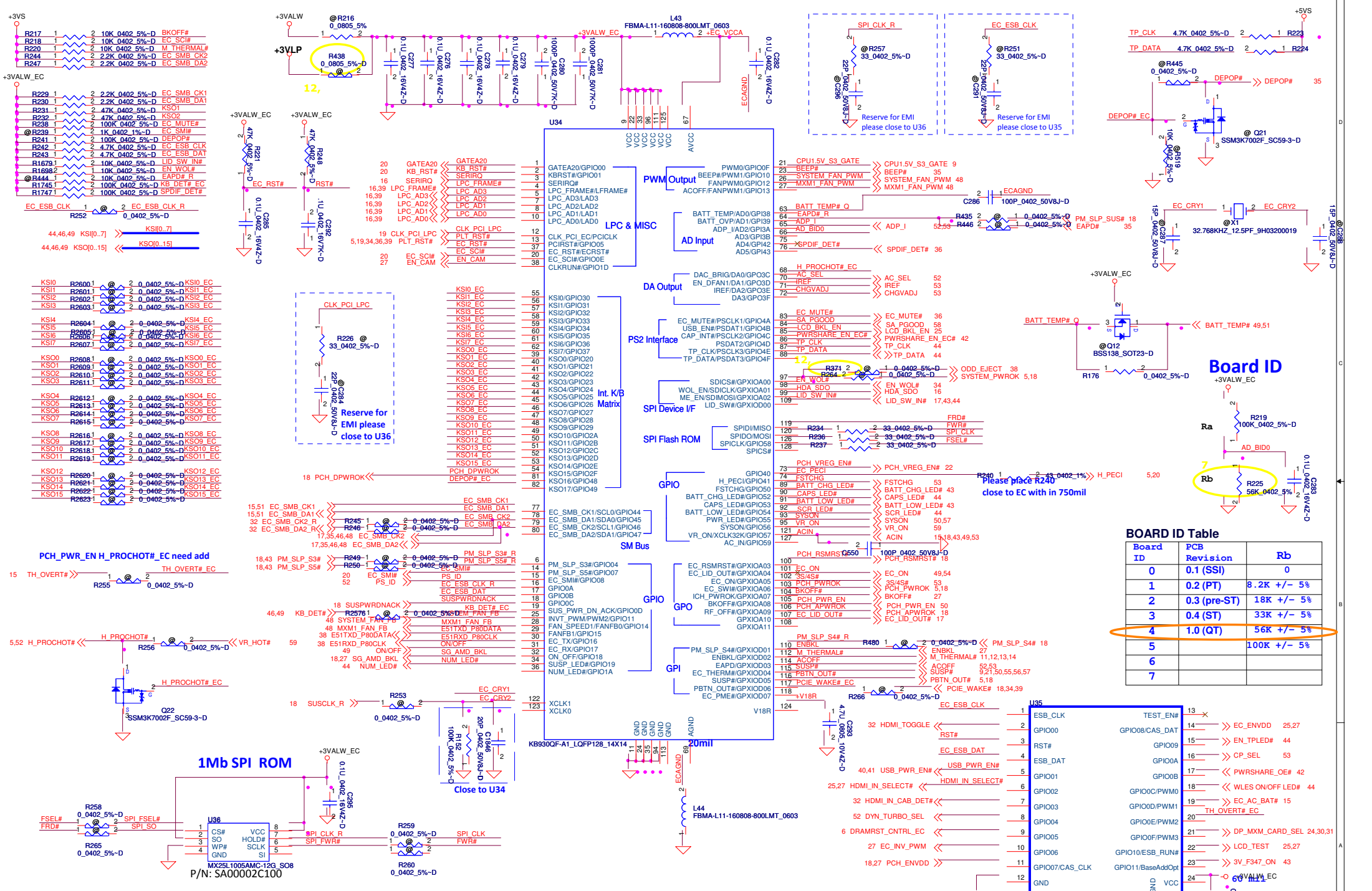


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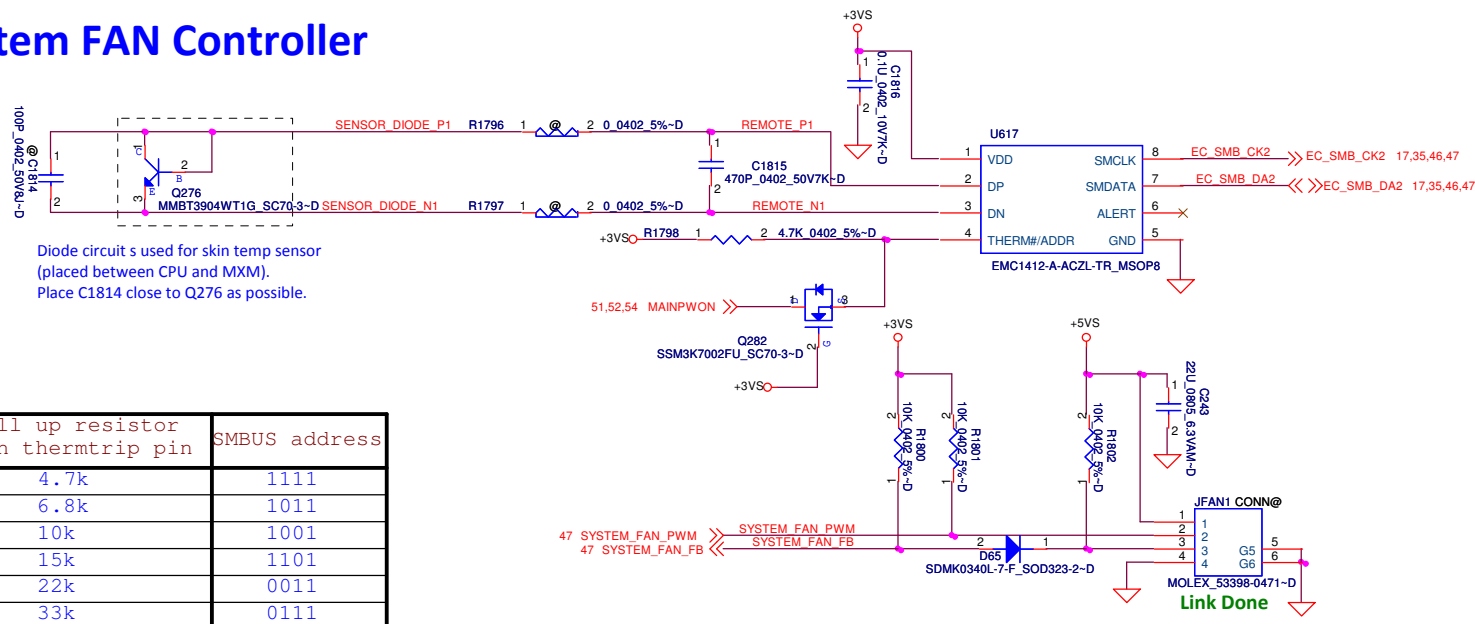
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	Size	Document Number LA-8341P	Rev 1.0
	Date: Friday, March 02, 2012		
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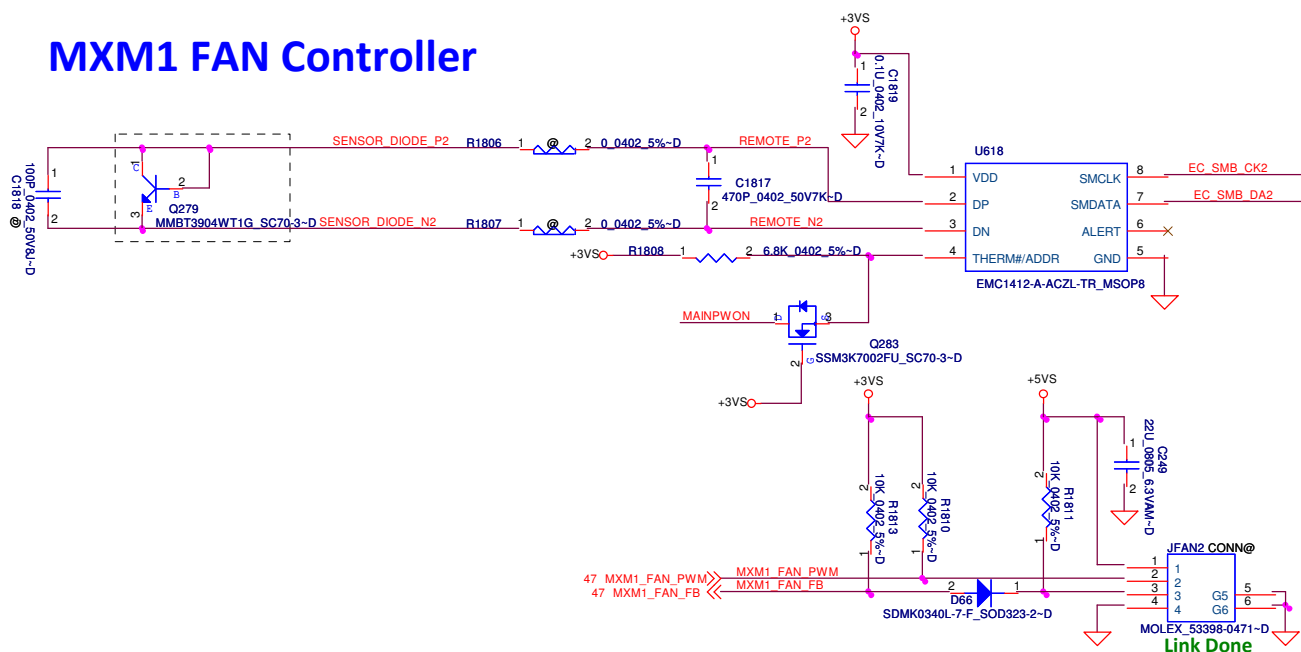


System FAN Controller



Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111

MXM1 FAN Controller



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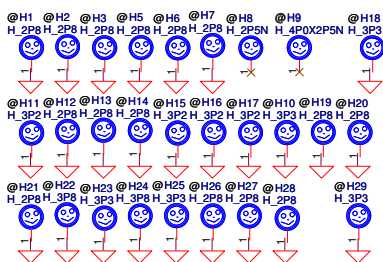
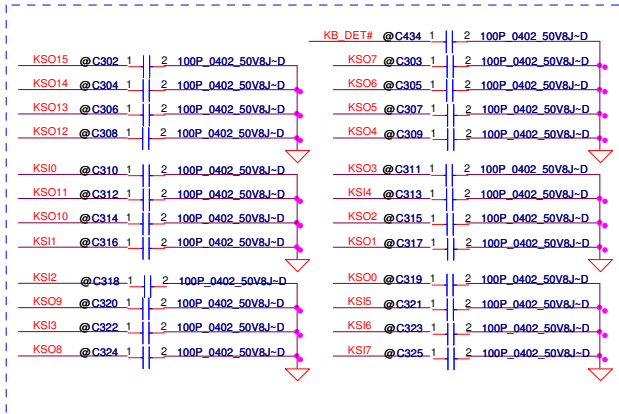
Thermal Sensor & FAN

LA-8341P

Date: Friday, March 02, 2012

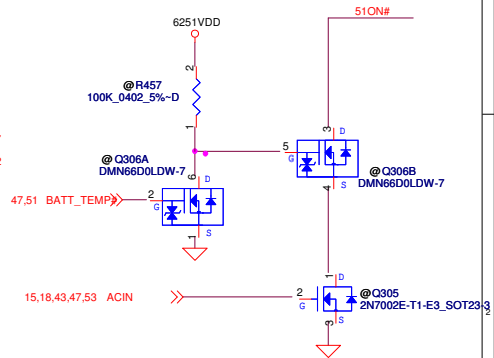
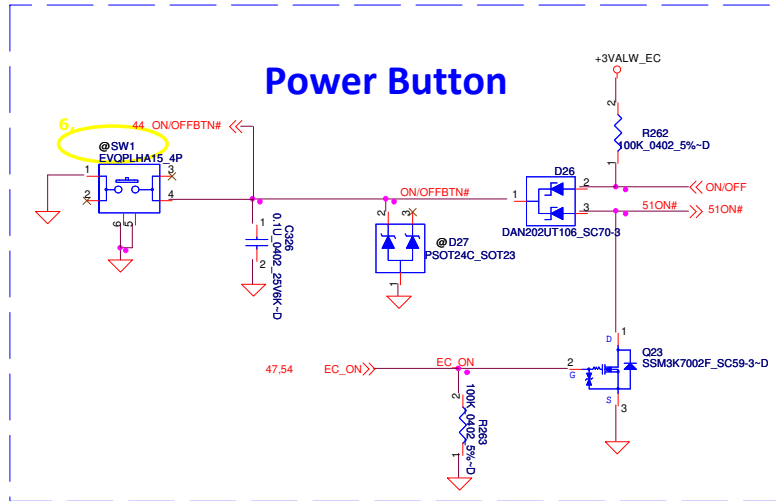
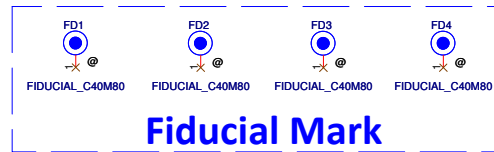
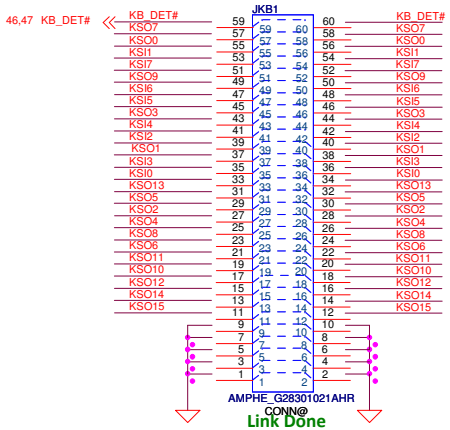
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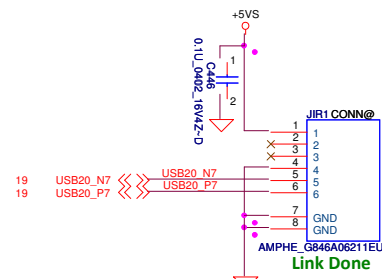


INT_KBD Conn.

KSIO[0..7] << KSIO[0..7] 44,46,47
KSIO[0..15] >> KSIO[0..15] 44,46,47



IR SENSOR connector



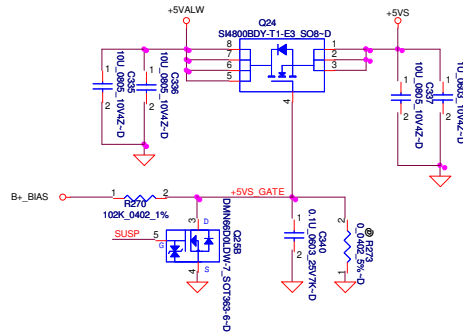
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Compal Electronics, Inc.			
KB & Power Button & IR			
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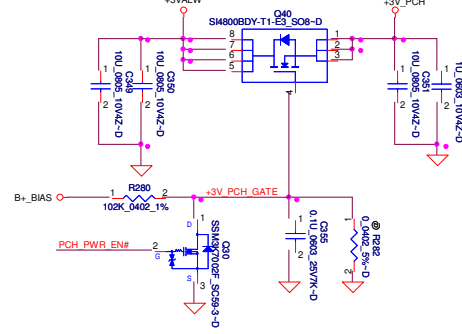
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DC to DC

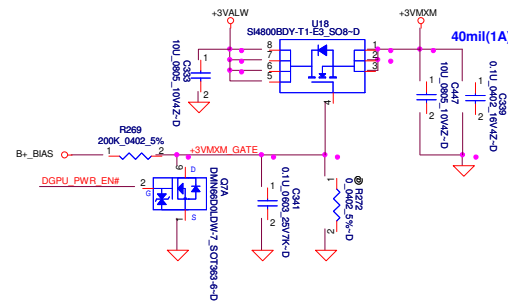
+5VALW to +5VS



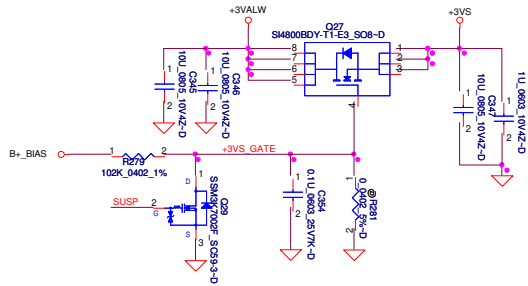
+3VALW to +3V_PCH



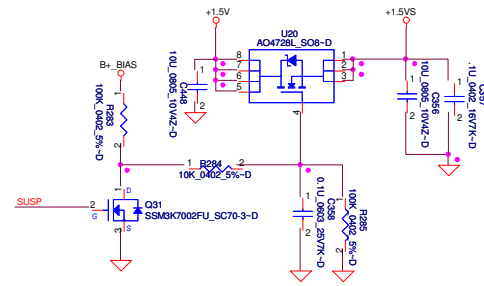
+3VALW to +3VMXM Transfer



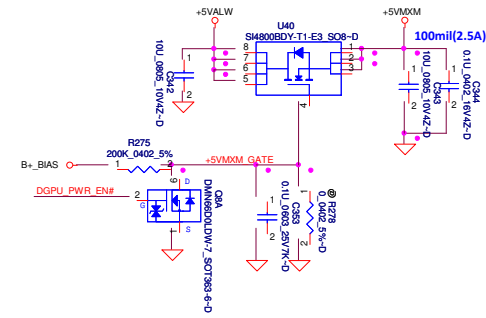
+3VALW to +3VS



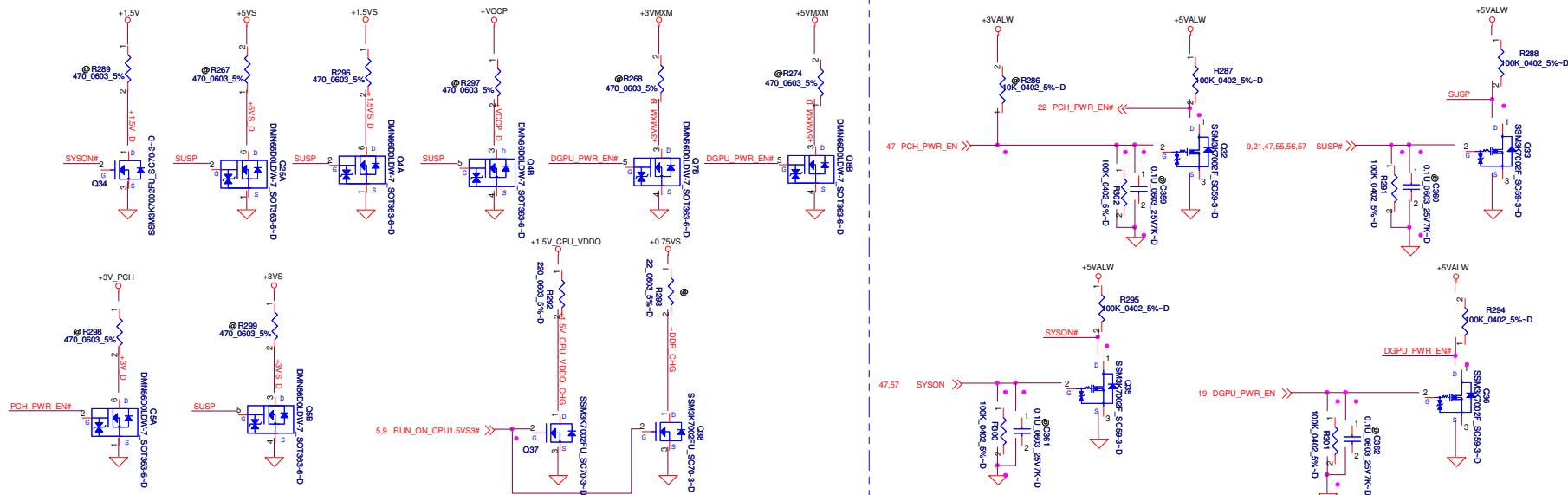
+1.5V To +1.5VS



+5VALW to +5VMXM



Discharge Circuit

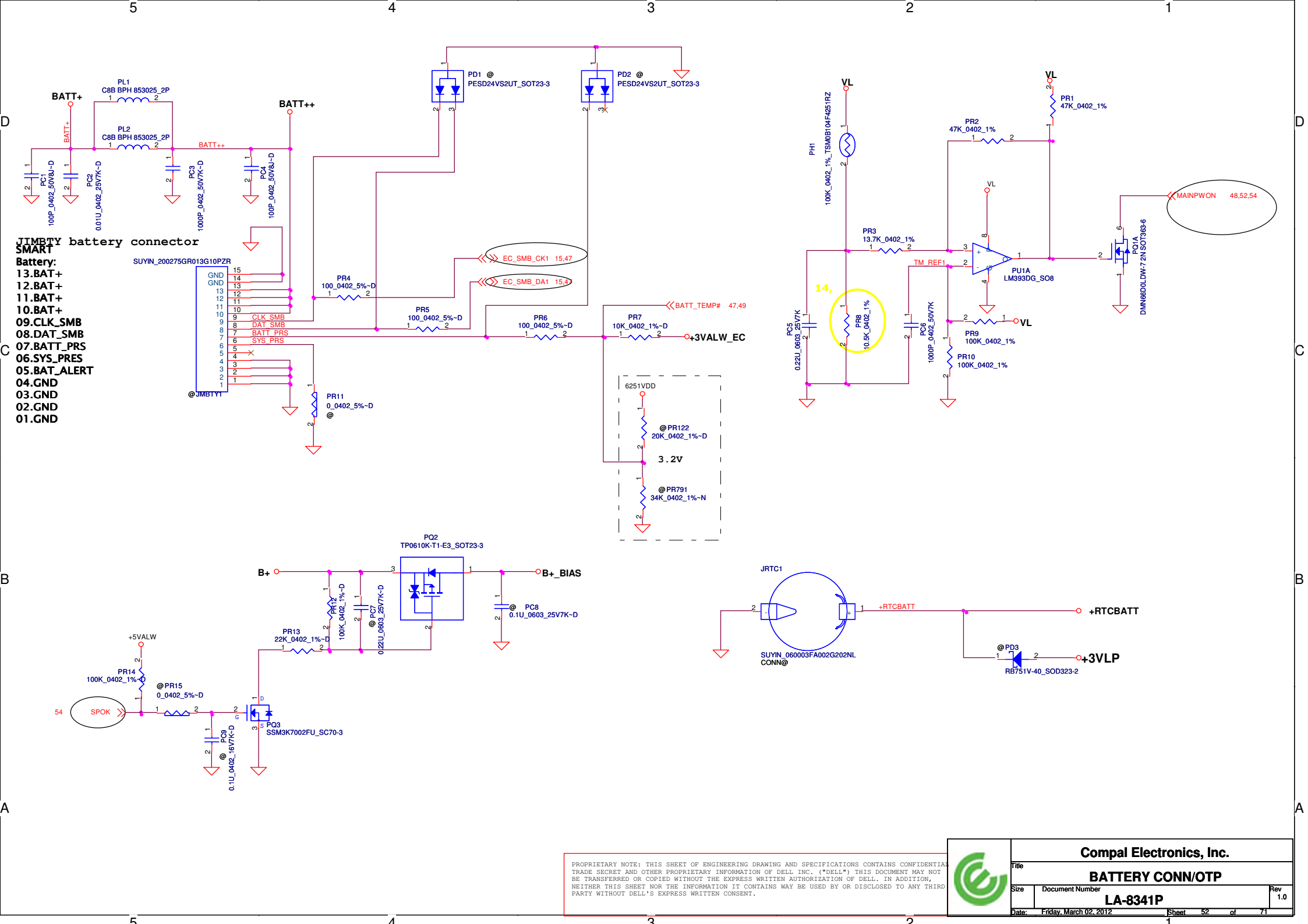


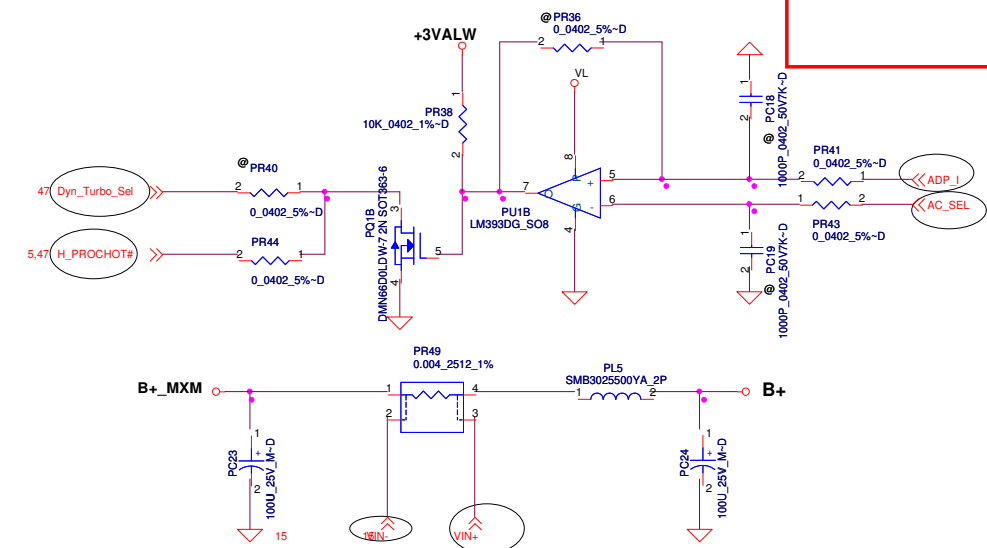
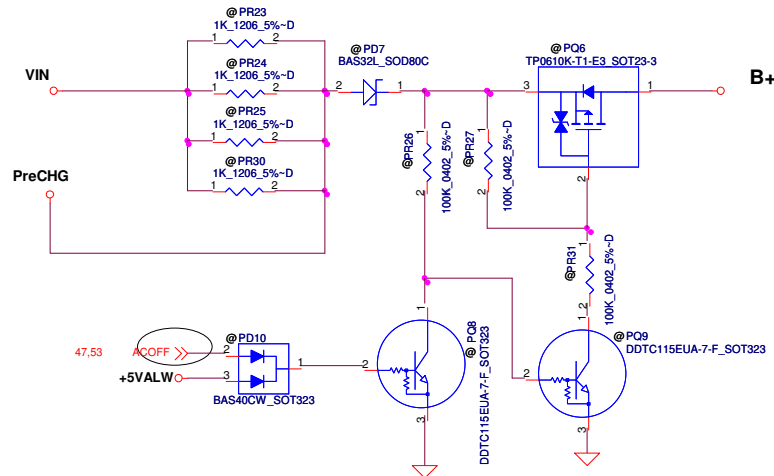
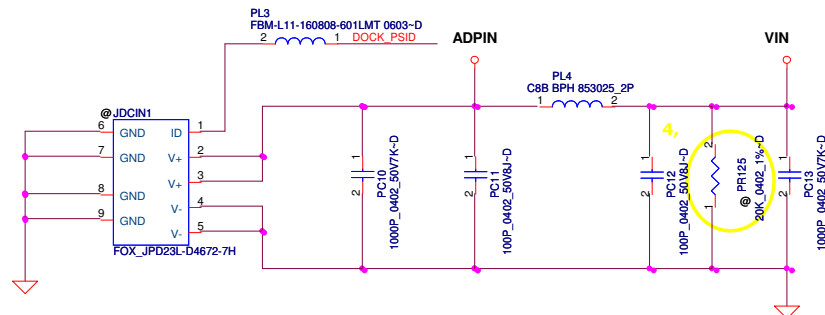
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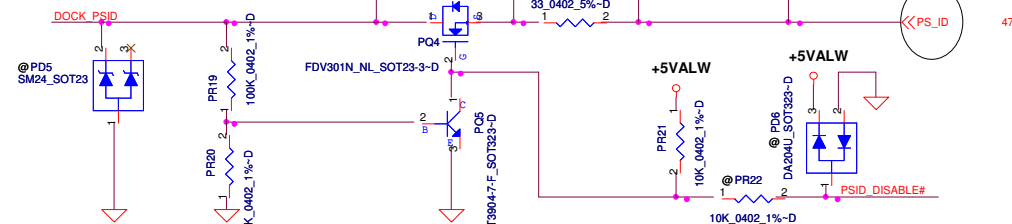
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Title			
DC/DC Interface			
Size	Document Number	Rev	
	LA-8341P	1.0	
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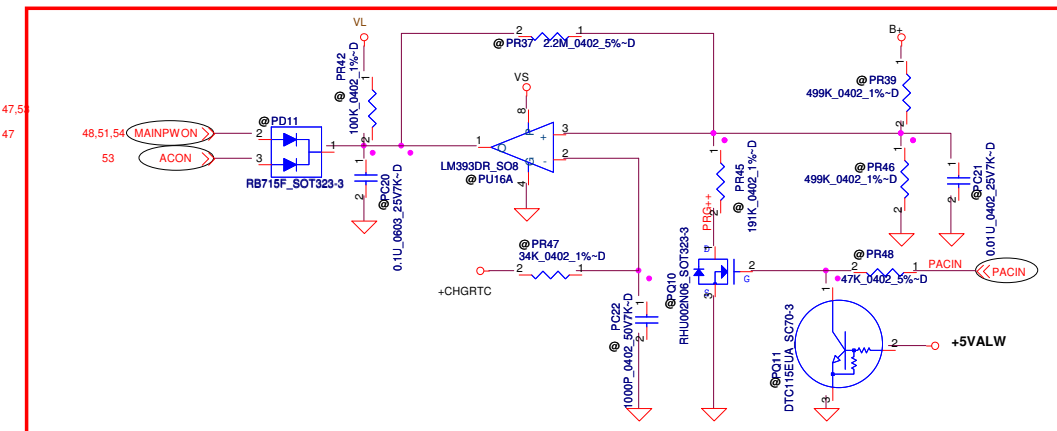
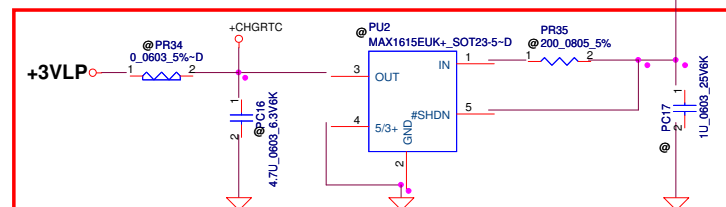


Add MXM power net for HW request.



ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max
H-->L	4.92V	6.1V	5.25V
L-->H	6.062V	6.244V	6.43V



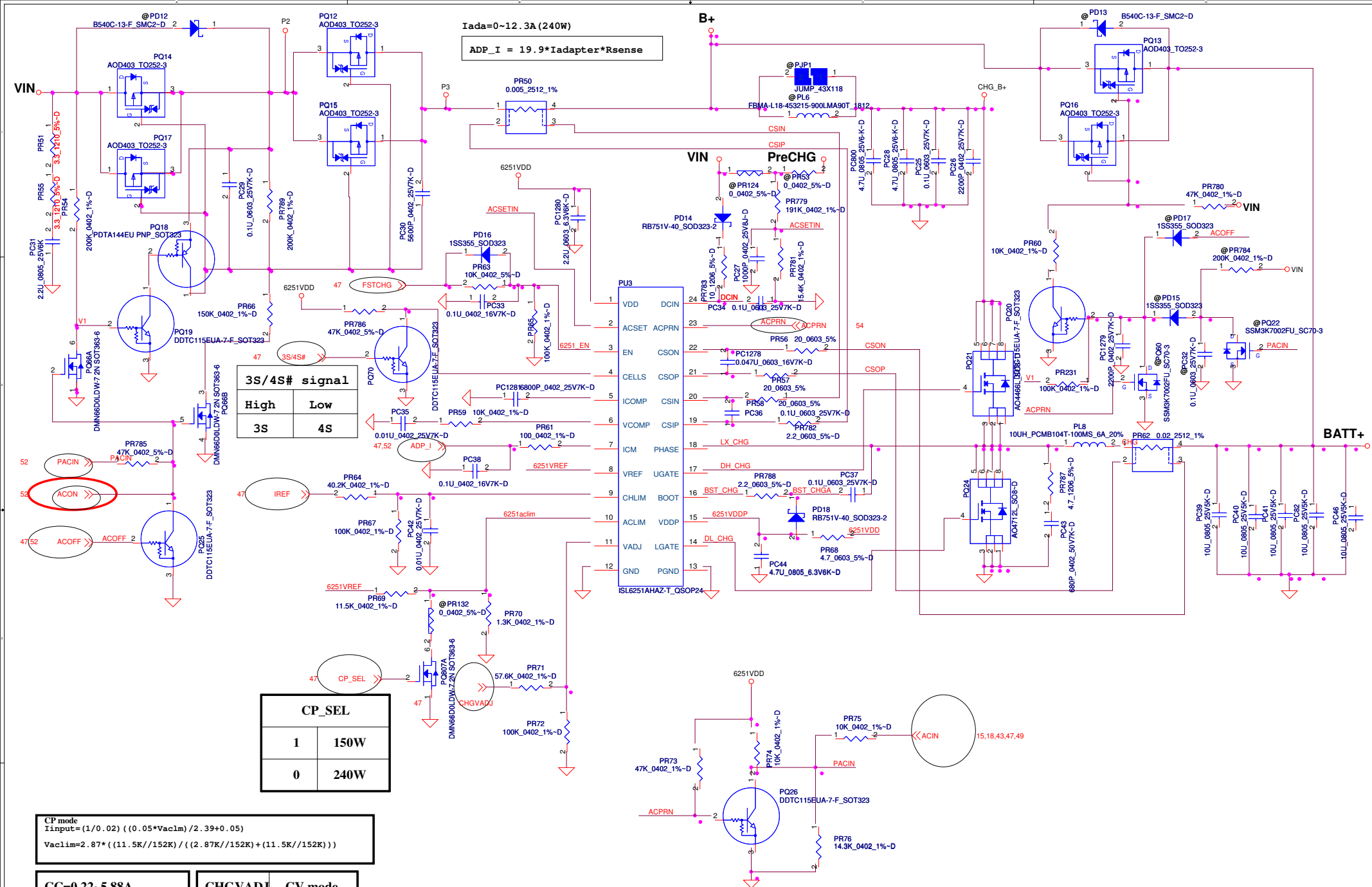
"US California Energy Efficiency"
(Reserve 130mW for no battery mode)

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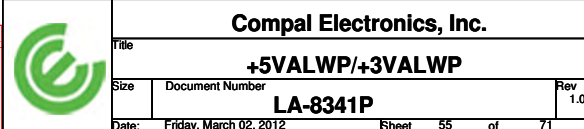
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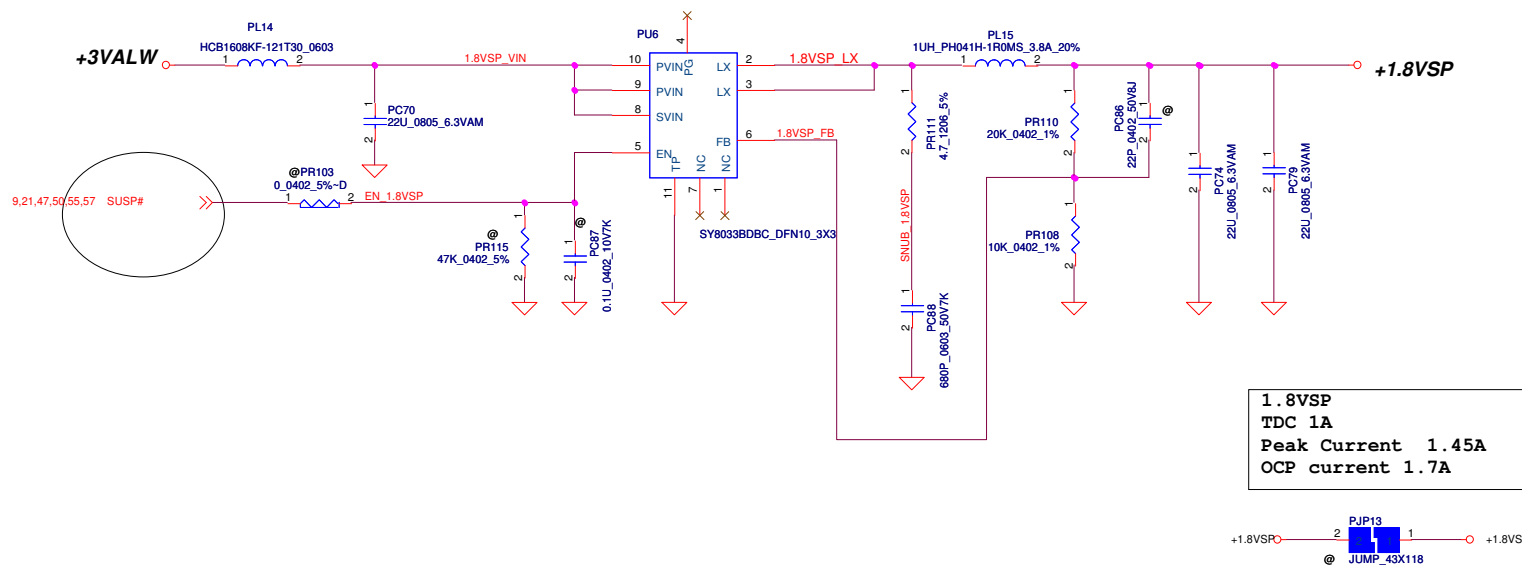
Title			
DCIN & DETECTOR			
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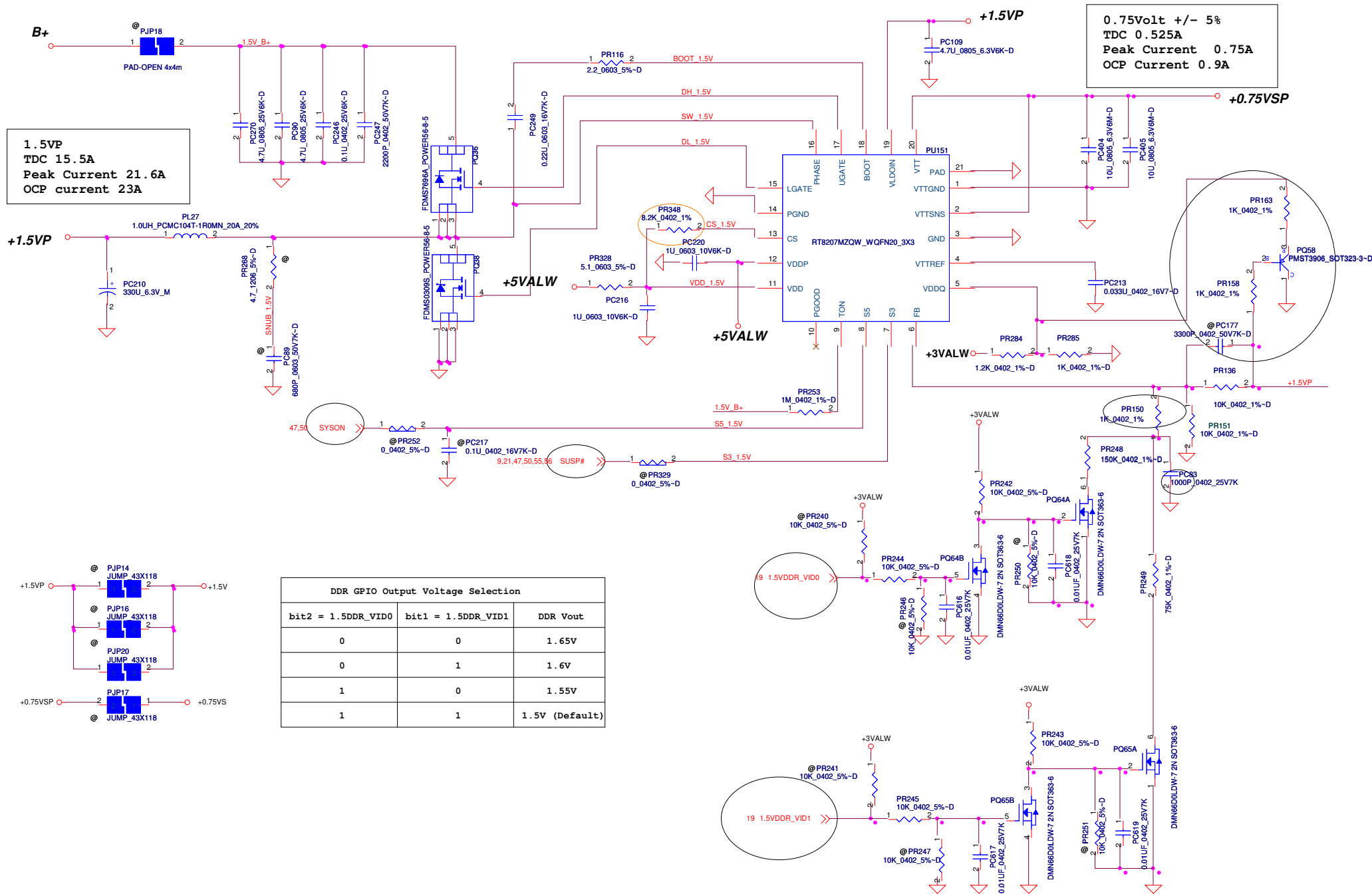
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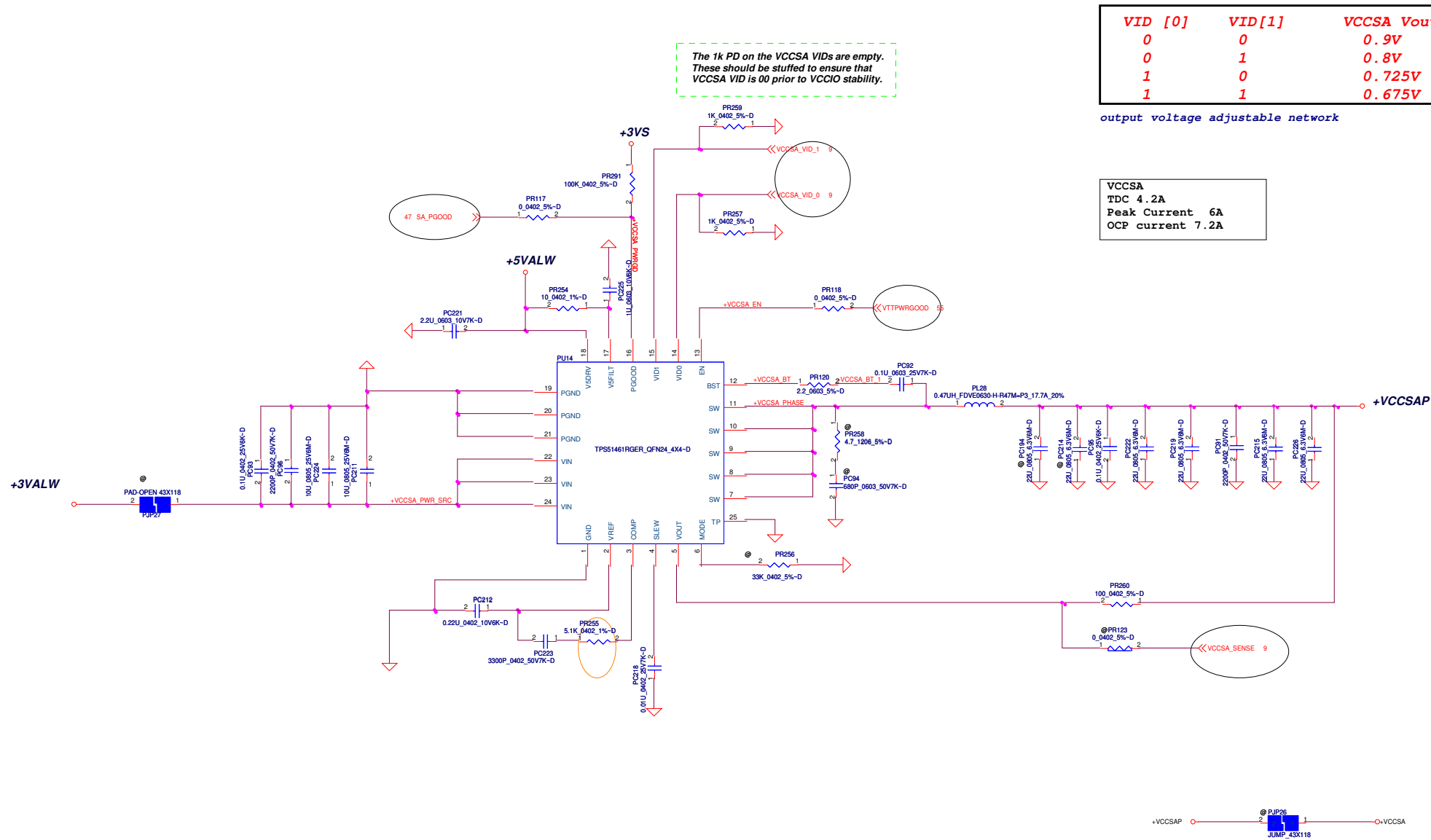




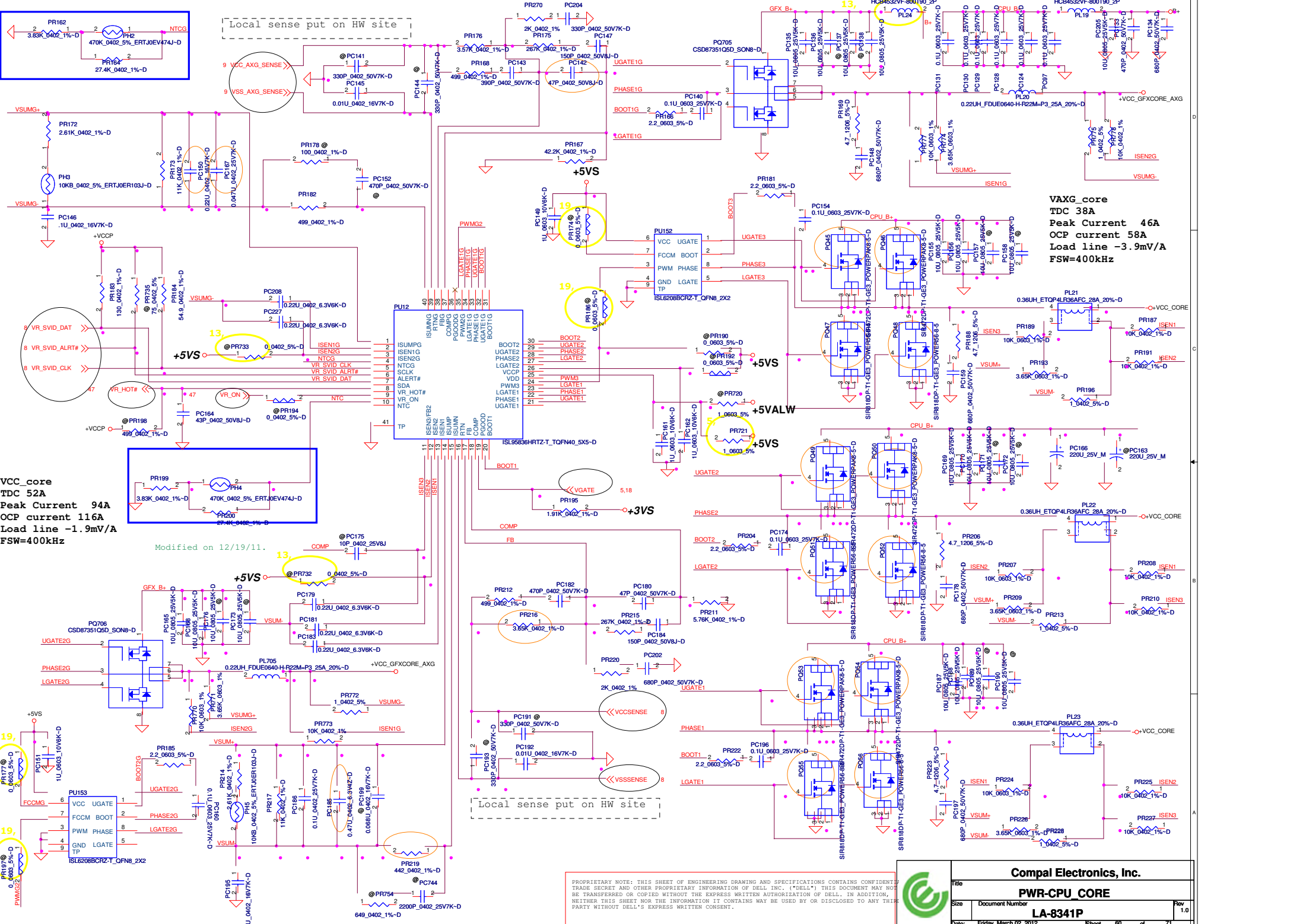
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VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line -1.9mV/A
FSW=400kHz

VXG_core
TDC 38A
Peak Current 46A
OCP current 58A
Load line -3.9mV/A
FSW=400kHz

Modified on 12/19/11.

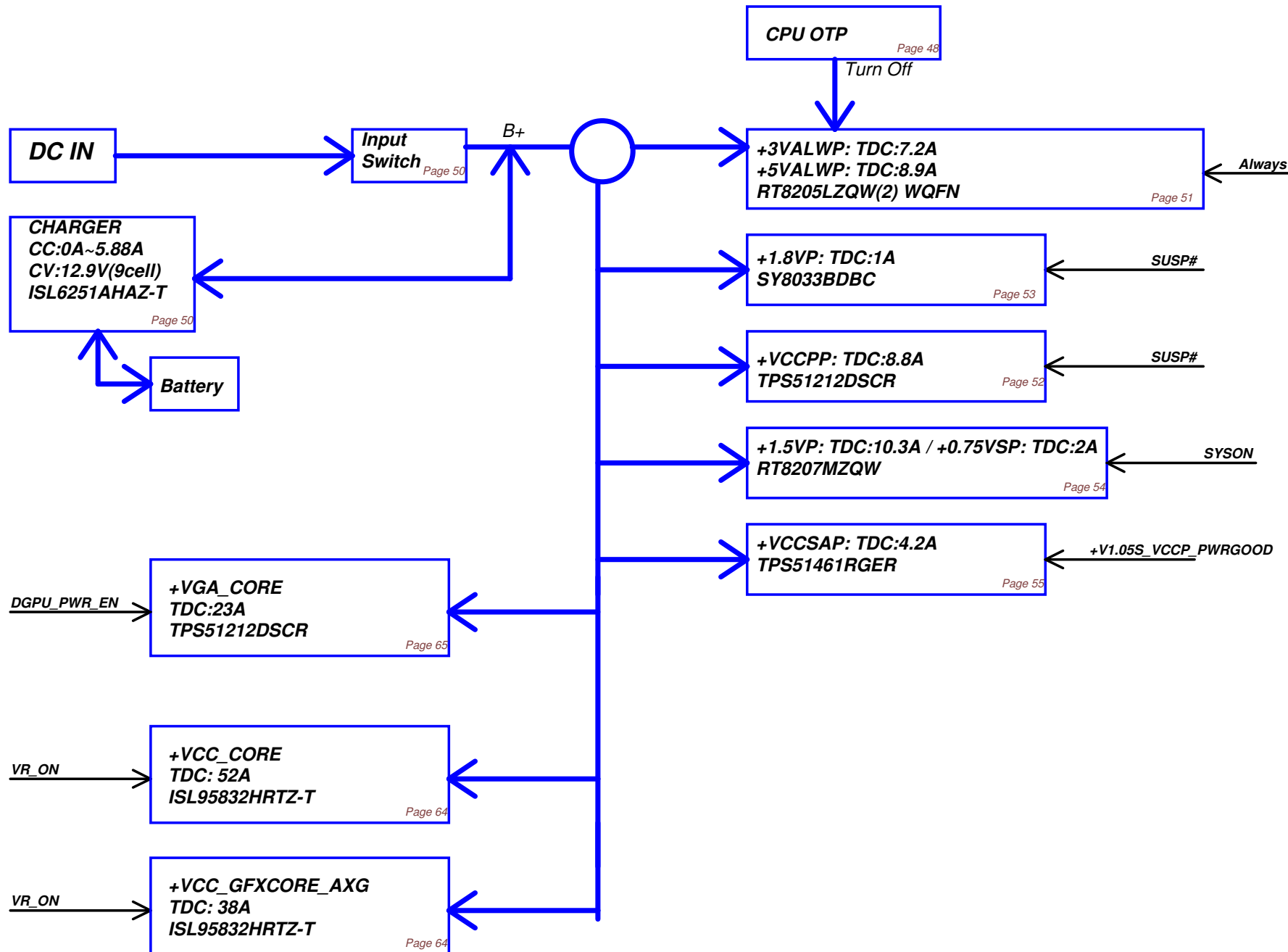
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			Compal Electronics, Inc.		
Title			PWR - PROCESSOR DECOUPLING		
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Power block

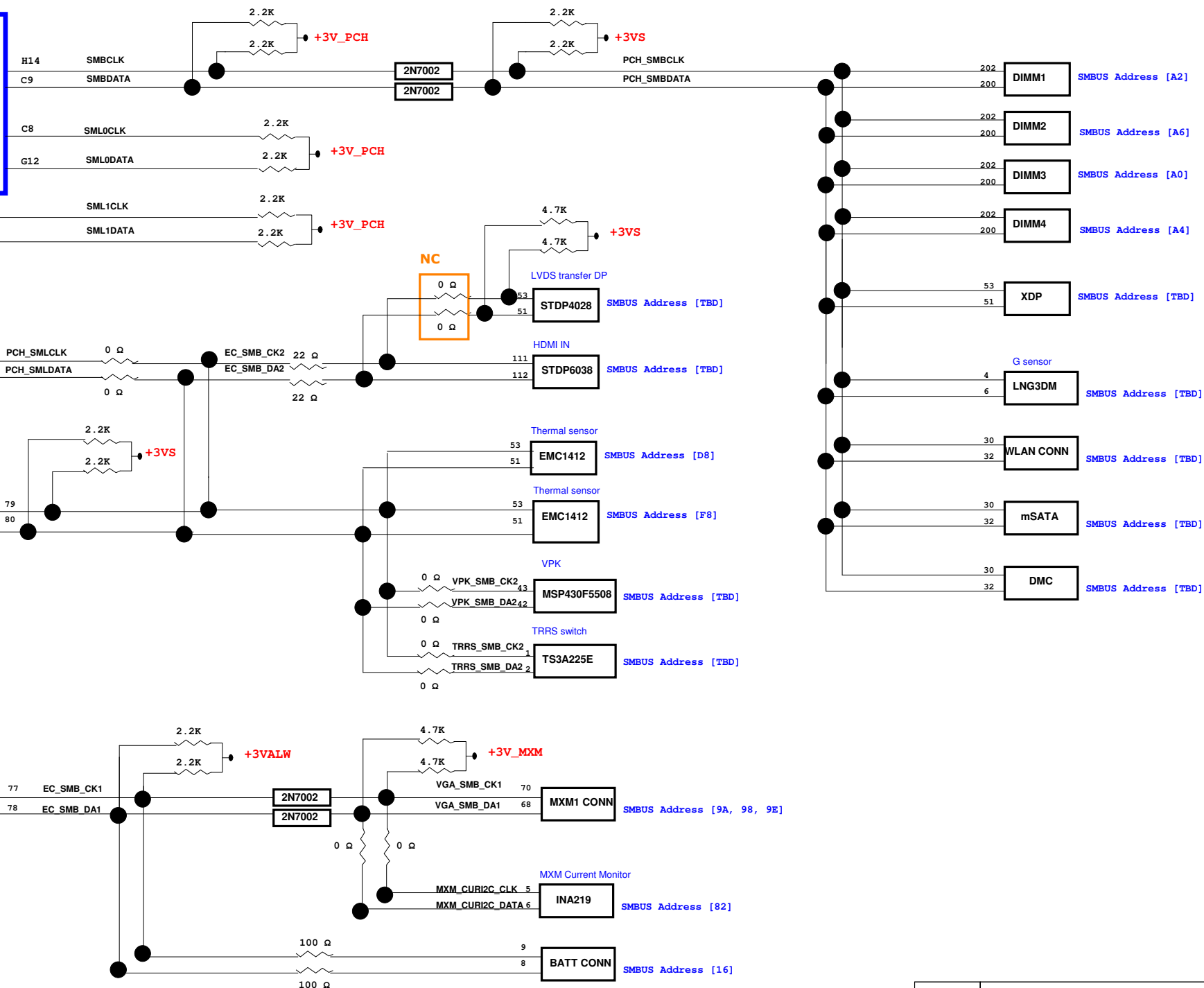
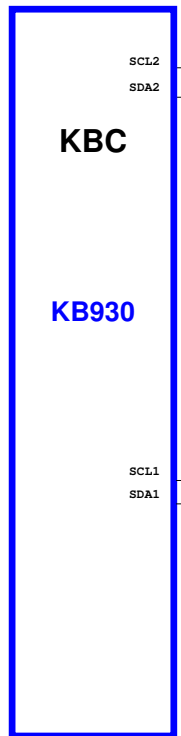
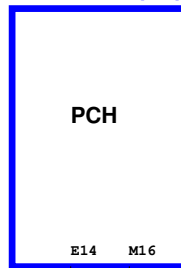


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Compal Electronics, Inc.			
Title		POWER BLOCK DIAGRAM	
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SMBUS Address [TBD]



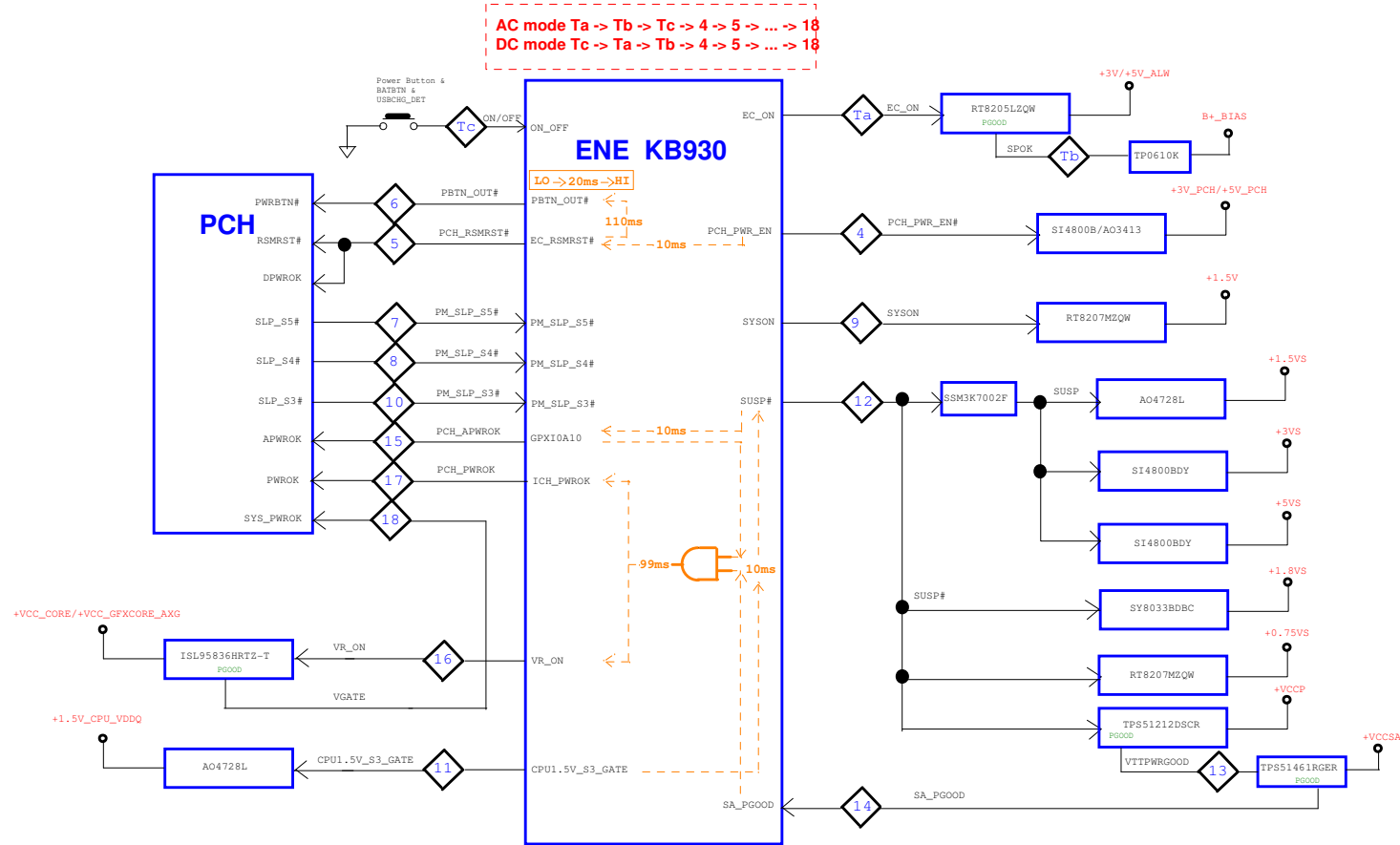
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Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30		11'10/11		Only need to reserve one AC coupling cap for the DP signals from PCH (MXM) to DP redriver.	1,Remove C68, C69, C65, C67, C63, C64, C57, C66, C297, C298, C426, C427 C416, C417, C369, C370, C121, C367, C299, C300 related circuits. 2, Add C368, C301related circuits.	X01
2	29		11'10/11		Reserve pull HI circuit for TMDS output driver pre-emphasis and EMI setting.	Reserve RV57 pull HI to +3VS and NC.	X01
3	4, 24		11'10/11			Change EDP_HPD# to EDP_HPD_R	X01
4	25		11'10/12		Solve QV9A derating issue.	Add RV39 to devide voltage.	X01
5	50		11'10/18		To solve two step issue for PCH_PWR_EN#	NC R286 and pop R302.	X01
6	30		11'10/18		For DP function from PCH port.	Pop R2263 and R2264	X01
7	50		11'10/18		Modify discharge circuits for back drive improve.	1, NC R289, R267, R297, R268, R274, R298, R299, R292, R293. 2, Change Q7B, Q8B enable signals to DGPU_PWR_EN#.	X01
8	32, 35		11'10/18		Remove HDMI_IN_AUDIO_CODEC signals.	Remove "HDMI_IN_AUDIO_CODEC" related signals and remove R1842.	X01
9	19, 46, 47		11'10/18		For material shortage issue, change all array resister to single resister	RP1-> R2580~ R2583, RP2-> R2584~ R2587, RP3-> R2588~ R2591 RP4-> R2592~ R2595, RP5-> R2596~ R2599, RP7-> R2600~ R2603 RP8-> R2604~ R2607, RP9-> R2608~ R2611, RP10-> R2612~ R2615 RP11-> R2616~ R2619, RP11-> R2620~ R2623, RPH1->RH185, RH191, RH193, RH205 RPH2-> RH250, RH214, RH249, RH248, RPH3-> RH252, RH253, RH254, RH256 RPH4-> RH257, RH258, RH260, RPH5-> RH259, RH261, RH262, RH263	X01
10	47, 51, 54		11'10/19		ERP lot6 implementation	1, NC R216 and pop R438. 2, NC PR273 and pop PR790. 3, change PR7 pull Hi to +3VALW_EC.	X01
11	38		11'10/19		Update zero power ODD circuit for leakage prevent.	Pop R173	X01
12	16, 17, 32, 33, 34, 46, 47		11'10/19		Update crystal usage.	1, change crystal components for YH3, YH2, YL1, Y3, Y4, X1, YH1 2, change C97, C98, CH23, CH24=15pF, Change CL18, CL19=18pF	X01
13	47		11'10/20		Update Board ID to PT stage.	Change R225 to 8.2K.	X01
14	20		11'10/20		Follow INTEL review list: All unused GPIOs, which are GPI by default needs to be pulled up to their respective power wells through 8.2 kohm to 10 kohm resistor	1, Add RH264 and pull HI to +3V_PCH 2, Pop RH194	X01
15	22		11'10/20		Follow INTEL review list: VCCASW[22-23] do not require series resistors.	NC RH240, RH241 and RH243 and use short pad.	X01
16	21		11'10/20		Follow INTEL review list: VCCCLKDMI filter is no longer required. Keep the Cdecap, but remove the Cfitler/Lfilter.	Change LH11 to RH265 and use short pad.	X01
17	9		11'10/20		Follow INTEL review list: +1.5V voltage divider for SM_VREF uses 1K Ohm	RC112,RC116 change to 1K and NC.	X01
18	20, 57		11'10/20		Solve Back drive issue for +3VS and +3V_PCH	NC PR240, PR241, RH192	X01
19	5, 50		11'10/20		Follow INTEL review list suggestion.	NC RC19 and QC1 and pop R292	X01
20	32, 33		11'10/20		Follow vendor suggestion change L to 0 ohm.	Change L11, L12, L13, L32, L46, L48, L52 to R452, R453, R454, R455, R450, R451, R456 and pop them.	X01
21	32		11'10/21		Delete HDMI_IN_AUDIO_CODEC pull HI resitors.	Remove R1665.	
22	9		11'10/21			Remove J8.	
23	21, 22		11'10/22		Remove short jump usage.	Remove RH240, RH241, RH243, RH265 and short directly between +1.05VS and PCH.	
24	35		11'10/22		1, Update combo jack to normal open type. 2, EAPD# pull high to prevent floating status to EC.	1, Update JHP2 to CIS symbol, and add R457 between Q42 pin1 and pin2. NC R129 and Q42 2, add R2554 pull HI to +3VS.	

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	49		11*10/22		Add one power switch for debug purpose.	Add SW1.	X01
26	39		11*10/22		Follow INTEL review list: PDG recommends 100K PD on AUXP and 100K PU o AUXN	1, Add R112 pull HI to +3VS_DMC. 2, Add R115 pull Low to GND.	X01
27	28		11*10/22		Modify CRT_DET# circuits.	Reserve RV28 pull HI to +CRT_VCC for CRT_DET# and NC.	X01
28	35		11*10/25		Update combo jack to normal open type.	1, Remove R457, add Q46, R116, R131, only NC R116 2, Change R2553 to C228. 3, Reserve R171, R156, R174, C229 related circuits and only pop R171. and modify U620, U621.pinB2 connect to +3.3V_MUTE.	X01
29	30		11*10/25		Prevent DP leakage.	Add D72 related circuits and pop it.	X01
30	30		11*10/25		1, After Maxim FAE review, change to DP mux to SSI design. 2, Change decoupling cap to 220nF. 3, For DP to HDMI dongle function.	1, Add C68, C69, C65, C67, C63, C64, C57, C66, C297, C298, C426, C427,C416, C417, C369, C370, C121, C367, C299, C300 related circuits back and change the value to 220nF and pop all the componets . 2, Change C35, C36, C37, C38, C40, C45, C48, C49 to 220nF. 3, Reserve U638,Q304, R2626, C2021 and pop componets.	X01
31	49		11*10/25		Modify SW1 circuits to avoid SMT error.	NC SW1 pin2 and pin 3	X01
32	32		11*10/25		After ST FAE feedback: 1, STDP6038 doesn't need to read / write the panel EDID 2, Keep I2S_DAT/SPDIF_IN has better performance 3, Avoid I2S_DAT/SPDIF_IN signal has attenuation problem duo to long trance	1, NC R1843 and R1844 2, change R156 to C227 3, reserve U637 and C226 related circuits and NC.	X01
33	35		11*10/25		1, Fix fast hot plug and Headset no sound issue. Also improve external speaker Power down pop noise. 2, Improve Power on pop noise at external speaker.	1, Change R111, R113 from "No stuff" to "stuff 1k ohm". 2, Change R155, R157 from 100 ohm to 0 ohm.	X01
34	15		11*10/25		Follow sourcer suggestion.	Change U51 from INA219AIDCNRG4 to HPA00900AIDCNR .	X01
35	18		11*10/25		For BIOS verify SUSACK# function.	Add RH172 between SUSACK#_R and SUSPWRDNACK_R	X01
36	36		11*10/26		For PC_BEEP no warning sound during boot up process.	Change R148 to 200 ohm.	X01
37	42		11*10/26		Follow CIS suggestion, change ESATA footprint to "TAIWI_EU093-117CRL-TW_11P-T"		X01
38	59		11*10/26		Layout space concern.	change PL19, PL24 to HCB4532KF-800T90.	X01
39	49,51, 52		11*10/26		Fulfill "US California Energy Efficiency" standard that reserve 130mW for no battery mode.	1, PWR: Reserve PR122, PR791, PQ23, PR114, PR121 related circuits and NC. Only Add PR119 2, EE: Reserve Q305, Q306, R457 related circuits and NC.	X01
40	42		11*10/26		Change ESATA footprint back to TYCO.		X01
41	51		11*10/26		change PR791 to from "R_0402-N" to "R_0402 footprint"		X01
42	35		11*10/26		change net name from "JACK_PLUG#_R" to "JACK_PLUG"		X01
43	47,49,51		11*10/26		change net name from "BATT_TEMP" to "BATT_TEMP#"		X01
44	35		11*10/26		Follow JHP1 solution to JHP2.	1, Change R127, R130 from "No stuff" to "stuff 1k ohm". 2, Change R169, R170 from 100 ohm to 0 ohm.	X01
45	31,39		11*10/26		1, Reserve for SI-BEAM GEN2 card usage for PT build. 2, Change the MOS to protect ESD.	1, Reserve R95 pull HI to +3V_DMC and NC. 2, Change Q302 to 2N7002K.	X01
46	35		11*10/27		Follow vendor suggest.	Change C129, C130 to 0805 size.	X01
47	59		11*10/27		For Layout interference concern.	Change PL24 to original footprint same as SSI stage. But still use HCB4532KF-800T90.	X01
48	28		11*10/27		Due to CRT EA fail.	Change bead LV2,LV3,LV4 from BLM18BB600SN1D to TAIYO BK1608LL470-T	X01
49	59		11*10/27			Connect PU12.pin41 to GND	X01
50	55, 59		11*11/07		Correct both IGPU and VCCP OCP setting.	Change PR182 from 357 ohm to 499 ohm, and PR101 from 33k ohm to 43k ohm.	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47		11*12/07		Change Board ID setting for ST stage.	Change R225 to 18K/5%	X02
2	25		11*12/07		For EDP power sequence EA.	Change RV40 to 100 ohm (0603) size.	X02
3	21		11*12/07		Adding a 1uF at U47 for +VCCAFDI_VRM		X02
4	32,33		11*12/07		For PASS crystal EA test, finetune cap setting.	1, Change C97 and C98 from 15pF to 12pF. 2, Change C407 and C408 from 10pF to 12pF.	X02
5	28		11*12/07		Per CRT EA, HSYNC and VSYNC undershoot and overshoot over spec.	Change LV5 and LV6 from bead to 0 ohm.	X02
6	25,27		11*12/07		ESD Vbus setting different between USB and DMIC/DCLK.	Move USB20_P(N)11 to D49, Change D48 power rail to +3VS_CAM.	X02
7	44		11*12/07		Modify Logo board related circuits.		X02
8	30		11*12/07		For Optimus, mDP output from dGPU.		X02
9	17,47		11*12/07			Chang KB_DET# from PCH to EC(pin 25)	X02
10	28		11*12/07			Change FV1 footprint to F_1206L150PR(F2's footprint)	X02
11	46		11*12/07		VPK function no implement, NC related components.		X02
12	42		11*12/07		Per sourcer suggestion, change USB charger IC to PI5USB1457A.		X02
13	32		11*12/07		Per reference spec and 2nd source consideration.	Change C183 from 0.1uF to 10uF.	X02
14	35		11*12/07		Avoid noise during S5 & G3 mode, add a circuit at sleeve pin.		X02
15	30		11*12/13		To prevent floating by other source.	Add a 100K PD at U8 pin 4 net "VGA_DPC_HPD".	X02
16			11*12/13		Change some option setting 0 ohm to short pad.		X02
17	42		11*12/13		Update USB power share circuits.	Move R1701 and keep NC, add R1702, NC R368.	X02
18	47		11*12/13		Change Board ID setting back to PT stage.	Change R225 back to 8.2K/5%	X02
19	19		11*12/13		For Intel chipset Hub1 EMI issue, swap USB port9 and port6		X02
20	25,27		11*12/13		Per EMI request.	Adding 0 ohm and 90ohm CM-mode choke colayout on USB port 11 and port12.	X02
21	16		11*12/13		Vendor improve their production.	U48 change to W25Q64FVSSIG(58nm)from W25Q64CVSSIG(90nm)	X02
22	28		11*12/13			Change FV1 part same as F2.	X02
23	27		11*12/13		For LVDS power sequence EA.	Change RV3 to 100 ohm (0603) size.	X02
24	47		11*12/13		Reduce power consumption on S5 mode.	Change R238 and R241 from 10K to 100K.	X02
25	47		11*12/13		Update "US California Energy Efficiency" circuits.	1, Add Q12 and NC. 2, Add R176 and POP.	X02
26	59		11*12/13			POWER PC164 change 0402 type	X02
27	25,27		11*12/20			NC L46,L48, Pop R462,R463,R460 and R461.	X02
28	16~23		11*12/20		Update PCH PN to QS sample	Change MFR.P/N, Compal P/N, Part description and value of PCH.	X02
29	59		11*12/20		Update power 2nd source usage for ISL6208BCRZ-T	Add PU152, PU153 and pop, NC PU11, PU15	X02

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EE PIR (3)			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
30	47		11'12/20		Change Board ID setting for ST stage.	Change R225 to 18K/5%	X02
31	35		11'12/20			change Q309 to 2N7002DW-7	X02
32	35		11'12/20		Reserve for pop noise	change HP mute IC's power rail to +3VALW, pop R156, depop R171.	X02
33	35		11'12/20		Update combo jack circuits.	Add C745, C746 to GND.	X02
34	40,41		11'12/20		For signal jitter noise tolerance consideration, remove USB3.0 redriver 0 ohm co-layout resistor.	Remove R362~R365, R358~R361, R399~R402, R395~R398, R350~R357, R403~R410	X02
35	35		11'12/20		Solve iPHONE Can't record issue	NC R277.	X02
36	59		11'12/21		Update power 2nd source usage for ISL6208BCR2-T	Delete PU11, PU15	X02
37	35		11'12/21		Per EMI suggest, avoid noise effect.	Add R350 and pop.	X02
38	39		11'12/21		Solve combo card (WIFI+BT) BT function cannot be recognized.	Add RE37 and NC.	X02
39	30		11'12/22		Correct SN74CBT3257CPWR supply voltage.	Add R351 and R352, NC R351 and POP R352.	X02
40	15		11'12/22		Update MXM relate circuits.	Add R353 and NC.	X02
41			12'01/02		Change some option setting 0 ohm to short pad.		X02
42	43		12'01/02			Remove PJP J11.	X02
43	39		12'01/02		Update combo card (WIFI+BT) BT function enable circuits.	Add RE38 and pop.	X02
44	28		12'01/05		Due to material shortage issue.	Change DV5 to 2nd source "RB491D_SOT23-3".	X02
45	36, 47		12'01/05		ADD SPDIF detect pin	1, Connect JSPD1 pin 5 to EC pin 76. 2, Adding 100K PU(+3VALW_EC) at pin76. NC C735.	X02
46	35		12'01/05		AP measurement fine tune.	Change C129 and C130 to "S CER CAP 2.2U 25V K X5R 0805 H1.25"	X02
47	40, 41		12'01/05		Due to material shortage issue.	1, Change C122,C123,C140,C141 to 2nd source material "220U_B_4VM_R35M". 2, Change C244,C247,C268,C269 source to "150U_D_10VM_R40M".	X02
48	38		12'01/05		Due to common parts issue.	Change Q303 to "SSM3K7002F_SC59-3~D"	X02
49	47		12'01/05		Update Board ID setting to formal ST stage.	Change R225 to 33K ohm.	X02
50	20, 29		12'01/05		Correct NET- name	Change GPIO30 net name to PCH_GPIO35.	X02
51	5		12'01/05		NC unnecessary parts.	RC27 and RC23 NC.	X02
52	39		12'01/05		Change some short pad back to 0 ohm.	Change RE26,RE27,RE28,RE29,RE31,RE32 and R162, R163 back to 0 ohm.	X02
53	35		12'01/05		Delete unnecessary parts.	Remove R116.	X02
54			12'01/05		Change some option setting 0 ohm to short pad for power parts.		X02
55	22,32,33, 35,38,47		12'01/06		Change some option setting 0 ohm to short pad.		X02
56	35		12'01/06		Reserve for de-pop circuits.	Add U625, R354, R355, C1847 related circuits.	X02
57	35		12'01/09		Follow vendor suggest, improve THD+N measurement test.	Add C28 between U634 pin1 and pin2.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	18,32,33, 35,36,38, 39		12'02/15		1, NC Unnecessary parts. 2, Short 0 ohm for MP	1, NC RE26, RE27, RE28, RE29, RE31, RE32, RE35, RE36 2, Change RH132, RV41, RV44, RV9, RV16, R58, R352, R1663, R1845, R179, R211, R432, R443, R228, R447-R449, R439, R147, R309-R311, R149-R151, RE38 to short pad.	A00
2	29		12'02/15		Remove HDMI BITS debug option 0 ohm near connector.	R931 and R985 change to 0 ohm and NC.	A00
3	17,34		12'02/15		For WOL support and prevent leakage.	Populate RH95 and change from 10K to 4.7K. RL13 change to NC.	A00
4	52		12'02/15		For Erp lot 6 adapter issue	Adding a 20K at ADPIN (default NC)	A00
5	59		12'02/15		According PWR team suggestion to modify circuits.	PR720 power rail change from +5VALW to +5VS.	A00
6	49		12'02/15		NC Unnecessary parts.	NC SW1 for MP	A00
7	47		12'02/15		Change Board ID setting for QT stage.	Change R225 to 56K ohm.	A00
8	34		12'02/16		For PASS LAN ISN and EMI test in Chinese new regulation.	Change CL39 to 150pF.	A00
9	35		12'02/16		Follow vendor suggestion to reserve 0 ohm location for ripple noise reduce.	1, R180 change to 0402 0ohm. 2, R178 change to 0402 0ohm. 3, Add 0603 0ohm for (U12 Pin 10,11) 4, Add 0402 0ohm for (U12 Pin 16) 5, Add 0402 0ohm for (U12 Pin 19) 6, R128 change to 0603 0ohm.	A00
10	40,41,63		12'02/16		1, For BITS issue solve, USB3 Re-driver change to Pericom 2, Create strap pin table for USB3.0 redriver IC control.	1, NC U628, U629, R1828, R1833, R12, R25, R47, R46 2, NC U630, U631, R1834, R1835, R192, R187, R197, R196 3, Move all the related BOM setting to "P63-USB 3.0 Config setting"	A00
11	39		12'02/17		1, Remove Unnecessary audio circuits. 2, NC Unnecessary DMC circuits.	1, Delete R174 2, NC R162, R163	A00
12	28,29,30, 32,35,37, 38,39,42, 43,47		12'02/17		Short 0 ohm for MP	1, Change R303, R316, R329, R340 to 0805 short pad 2, Change RS7, RS6, RE22, R441, R442, R438, R434, R433, R425, R428, R429, R371, R354, R255, R350, R2572, R5103, R2568, R2559, R172, R1702, R1699, R169, R170, R1667, R1572, R156, R155, R157, R110, R168, R101, LV5, LV6 to short pad.	A00
13	51		12'02/17		According PWR team suggestion, fine tune material usage	1, Change PL24 component same as PL19, but footprint keep the same. 2, Change PR89, PR119, PR732, PR733 component same as PR36.	A00
14	52,54,59		12'02/17		According Thermal and PWR team suggestion, fine tune OTP resistor setting.	Change PR8 to 10.5Kohm /1%.	A00
15	15		12'02/21		Prevent PCH GPIO38 ESD damage.	Reserve ESD protector for VGA_PRSNT_R# and VGA_PRSNT_L#. Pop D102 and NC D103.	A00
16	35		12'02/21		Follow vendor suggestion to modify.	1, Change R128 to 0805 size and R356 to 0402 size. 2, Separate U12.pin54,pin6,pin19 to different power rail. 3, Change R358 to L102 "BLM15AG121SN1D_2P"	A00
17	30		12'02/21		Per EIA and factory requirement.	Update U5 chip version to "PS8330BQFN48GTR2-A0"	A00
18	30		12'02/21		For BITS HDCP warning message issue.	NC R2261, R2262, C2021, U638, R2626 and Q304.	A00
19	59		12'02/21		According PWR team suggestion, fine tune material usage	Change PR174, PR177, PR186, PR197 to short pad.	A00
20	35		12'02/21		Follow Audio reference circuits to add one more cap for AVDD power.	Add C126 and pop it.	A00
21	25,27,35		12'02/22		According EMI team suggestion, fine tune material usage	Change L19, L20, L21, L22, L23, L24 and R460, R461, R462, R463 to 0 ohm short pad.	A00
22	30		12'02/23		For BITS HDCP warning message issue.	1, Pop R2261, R2262, C2021, U638, R2626 and Q304. 2, Change R2261 and R2262 to 2.2K. 3, Delete C297, C298, C299 and C300 and add R358-R361. 4, C368 and C301 change to 0.1uF(X7R).	A00
23	35		12'02/23		Follow vendor suggestion to modify.	1, Delete R357 and add L103, and pop it 2, change L49 to "4.7UH_LQM2MPN4R7MG0L_20%"	A00
24	54		12'02/23		According PWR team suggestion, fine tune material usage	Change PR264 to short pad.	A00

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