Model Name : SAGE 3G
Compal Project Name : V1JB1
File Name : LA-A041P

Compal Confidential

V1JB1 UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor
/Panther Point 989p PCH
/ DDR3L Memory Down *8

2013-03-26

REV:2.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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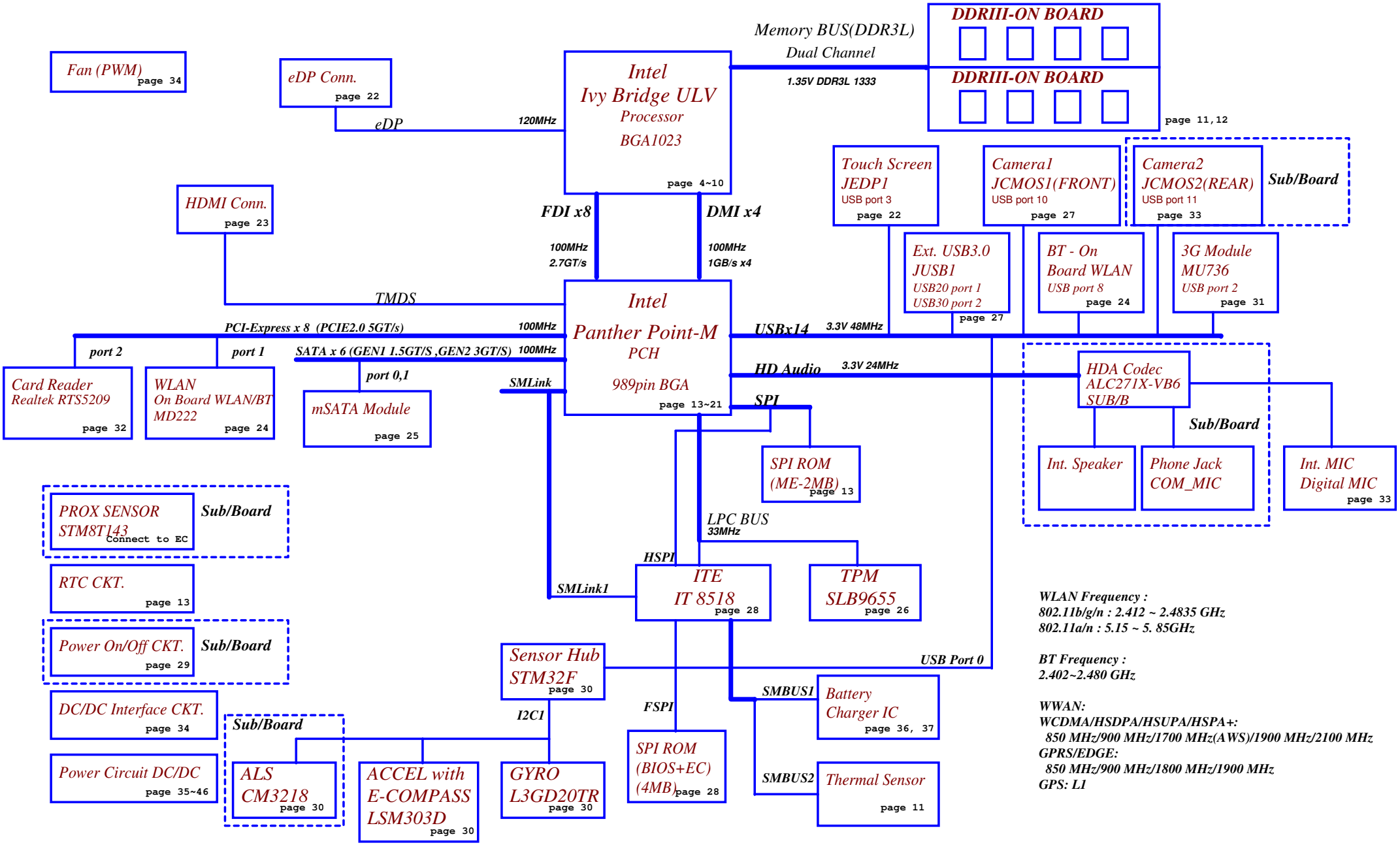
Title: *Cover Page*

Size: Custom | Document Number: *V1JB1 M/B LA-A041P Schematic* | Rev: 2.0

Date: Tuesday, March 26, 2013 | Sheet 1 of 52



WLAN Frequency :
802.11b/g/n : 2.412 ~ 2.4835 GHz
802.11a/n : 5.15 ~ 5. 85GHz

BT Frequency :
2.402~2.480 GHz

WWAN:
WCDMA/HSDPA/HSUPA/HSPA+:
850 MHz/900 MHz/1700 MHz(AWS)/1900 MHz/2100 MHz
GPRS/EDGE:
850 MHz/900 MHz/1800 MHz/1900 MHz
GPS: L1

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Title: **Block Diagrams**

Size: Custom | Document Number: **V1JB1 M/B LA-A041P Schematic** | Rev: 0.1

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+V5REF_SUS	+5VALW to +V5REF_SUS power rail for PCH	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device		Address
ChannelA	A0	1010 000X
ChannelB	A4	1010 010X

Sensor HUB SM Bus address

Device		Address
Gyroscope	D1	1101 000X b
	D3	1101 001X b
E-compass + G sensor	33	0011 001X b
ALS sensor	21	0010 000X b

BOM Config

Sensors List

Connect to	Function	Device
Sensor Hub	Gyroscope	ST - L3GD20TR
Sensor Hub	Accel+E-Compass	ST - LSM303DLHCTR
PCH(USB P3)	Sensor Hub	ST - STM32F103RCY6TR
Sensor Hub	ALS	Capella - CM3218
EC	Prox	ST-STM8T143AU62TTRC06

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	2.0*
5	
6	
7	

Note :

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
Dual Channel DDR	128@
eDP	eDP@
PCH	HM77@
Normal S3	S3@
Deep S3	DS3@
TPM	TPM@
Non TPM SKU	WOTPM@
Hall Sensor	LID@
Foxconn MD222	FOXMD222@
Lite-On MD222	LIONMD222@
For EMI/RF(Pop)	EMC@
For EMI/RF(Unpop)	XEMC@
Sensor(Intel F/W)	INTEL@
Sensor(ST F/W)	ST@
3G SKU	3G@
3G SKU(EMC part)	3GEMC@

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	Sensor Hub
		1	Ext. USB Connector
	UHCI1	2	3G Module - MU736/ME906
		3	Touch Screen
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	BlueTooth(WLAN Module)
		9	Debug Port(Reserve)
	UHCI5	10	Camera(Front)
		11	Camera(Rear)
	UHCI6	12	
		13	

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Issued Date	2011/06/24	Deciphered Date 2012/06/02	Title: Notes List
			Size: Custom; Document Number: V1JB1 M/B LA-A041P Schematic; Rev: 0.1
			Date: Wednesday, March 13, 2013; Sheet 3 of 52

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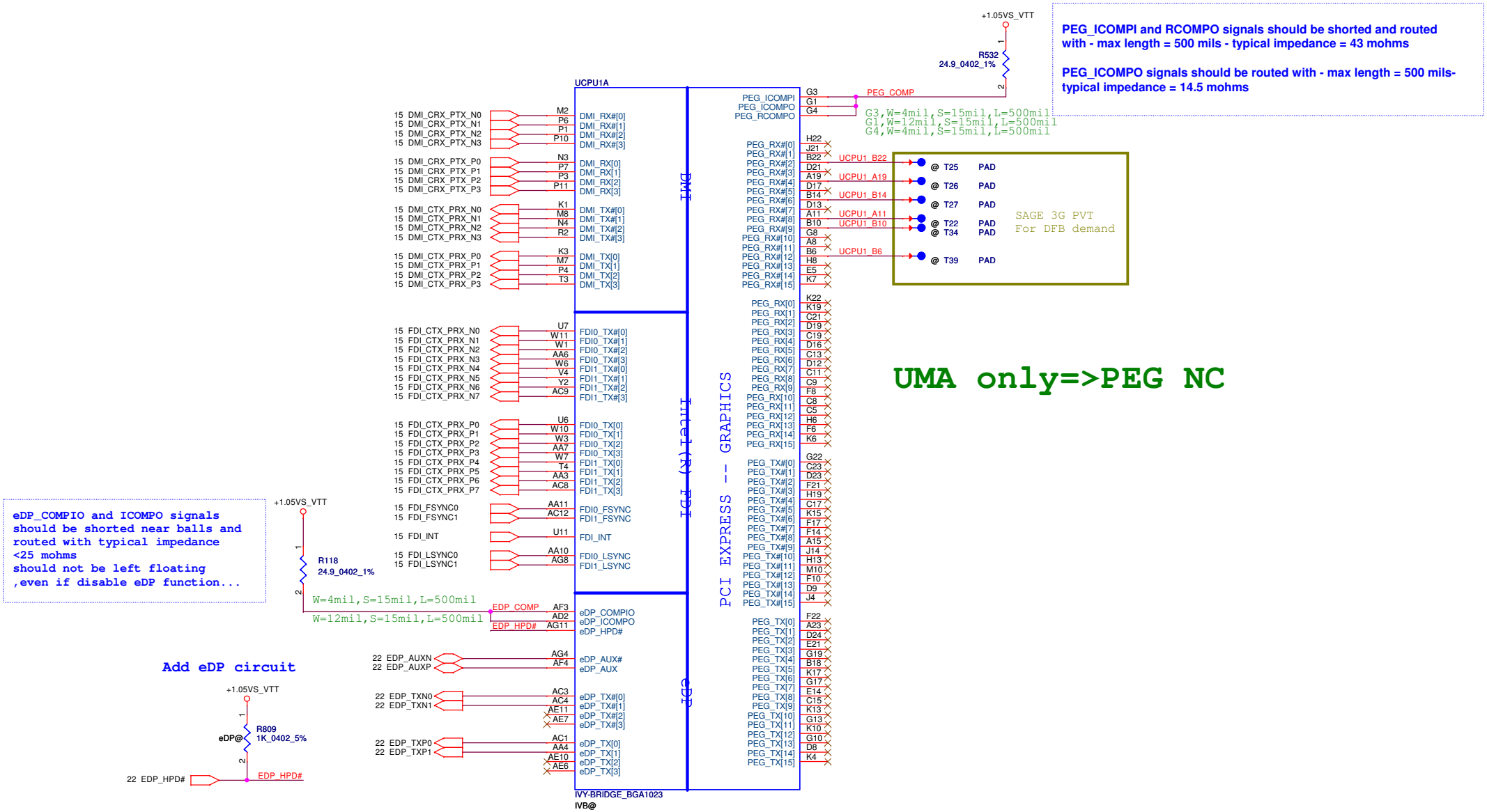

CPU P/N:

1.I3-3217 SA00005L5C0:S IC AV8063801058401 SR0N9 L1 1.8G ABO!
2.I5-3317 SA00005K6B0:S IC AV8063801058002 SR0N8 L1 1.7G ABO!
3.I3-2365 SA000051H60:S IC AV8062701047904 SR0CV J1 1.4G ABO!

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Issued Date	2011/06/24	Deciphered Date 2012/06/02	Title PROCESSOR(1/7) DMI,FDI,PEG
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PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

PROC_SELECT#
Future platforms,PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

Follow DG 1.2 & CRB1.0

C784 2 @ 1 0.1U_0201_10V6K H_CPUPWRGD
R223 2 1 10K_0402_5% H_CPUPWRGD

Processor Pullups follow CRB1.0

+1.05VS_VTT R220 2 1 62_0402_5%
28,36 H_PROCHOT# H_PROCHOT# R216 56_0402_5% 1 2 H_PROCHOT#_R

Follow DG 1.2 & CRB1.0
Buffered reset to CPU

SAGE 3G

+3VS C396 0.1U_0402_16V4Z U15
17,26,28,31,32 PLT_RST# NC A Y 4 BUFO_CPU_RST# SN74LVC1G07DCKR_SC70-5

Use open drain MOS:
+1.05VS_VTT PH pop 75ohm
series resister pop 43ohm

+1.05VS_VTT R226 75_0402_5% R227 43_0402_1% 1 2 BUF_CPU_RST#

RESET#:都ok後請CPU做reset

SAGE 3G

UCPU1B

17 H_SNB_IVB#	F49	PROC_SELECT#	MISC
	C57	PROC_DETECT#	
T1 PAD @ H_CATERR#	C49	CATERR#	THERMAL
28 H_PECI H_PECI	A48	PECI	
H_PROCHOT#	C45	PROCHOT#	
18 H_THRMTRIP#	D45	THERMTRIP#	
15 H_PM_SYNC	C48	PM_SYNC	PWR MANAGEMENT
18 H_CPUPWRGD R80 0_0402_5% 1 @ 2 H_CPUPWRGD_R	B46	UNCOREPWRGOOD	
PM_DRAM_PWRGD_R	BE45	SM_DRAMPWROK	
BUF_CPU_RST#	D44	RESET#	

UNCOREPWRGOOD:除了CPU_CORE以外的電OK

SM_DRAMPWROK:DRAM power ok

IVY-BRIDGE_BGA1023
IVB@

CLOCKS

BCLK J3	CLK_CPU_BCLK	CLK_CPU_DMI 14
BCLK# H2	CLK_CPU_BCLK#	CLK_CPU_DMI# 14
DPLL_REF_CLK AG3	CLK_CPU_DPLL	CLK_CPU_DPLL 14
DPLL_REF_CLK# AG1	CLK_CPU_DPLL#	CLK_CPU_DPLL# 14

DDR3 MISC

SM_DRAMRST# AT30	SM_DRAMRST#	SM_DRAMRST# 6
SM_RCOMP[0] BF44	SM_RCOMP0	R149 2 1 140_0402_1%
SM_RCOMP[1] BE43	SM_RCOMP1	R486 2 1 25.5_0402_1%
SM_RCOMP[2] BG43	SM_RCOMP2	R484 2 1 200_0402_1%

DDR3 Compensation Signals
Trace:10mil ,Spacing:13mil, Max.Length:500mil

JTAG & BPM

PRDY# N53		
PREQ# N55		
TCK L56	XDP_TCK	@ PAD T2
TMS L55	XDP_TMS	@ PAD T3
TRST# J58	XDP_TRST#	@ PAD T4
TDI M60	XDP_TDI	@ PAD T5
TDO L59	XDP_TDO	@ PAD T6
DBR# K58	XDP_DBRESET#	XDP_DBRESET# 15
BPM#[0] G58		
BPM#[1] E55		
BPM#[2] E59		
BPM#[3] G55		
BPM#[4] G59		
BPM#[5] H60		
BPM#[6] J59		
BPM#[7] J61		

C102 XEMC@ 100P_0402_50V8J
For EMI

SAGE 3G

+1.05VS_VTT
CLK_CPU_DPLL# R116 2 @ 1 1K_0402_5%
CLK_CPU_DPLL R117 2 @ 1 1K_0402_5%

Checklist1.0 P.64 Processor Graphis Disable Guide
DIS only SKU or UMA eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

+3VS
XDP_DBRESET# R569 2 1 1K_0402_5%

CRB1.0 PH 1K +3VS
Check list 1.0 PH 5K +3VS
Check list 1.2 PH 10K +3VS
Debug port DG1.1-1.2 50~5K ohm

Follow DG 1.2 & CRB1.0

+3VALW C101 0.1U_0402_16V4Z

28,42 VR_ON R82 1 @ 2 0_0402_5%
15 SYS_PWROK R81 1 @ 2 0_0402_5%
15 PM_DRAM_PWRGD

U5 MC74VHC1G09DFT2G_SC70-5
4 PM_SYS_PWRGD_BUF

+1.35VS R88 200_0402_5%

Use open drain MOS:
+1.35VS PH pop 200ohm
series resister pop 130ohm

R97 1 2 130_0402_5% PM_DRAM_PWRGD_R

SAGE 3G

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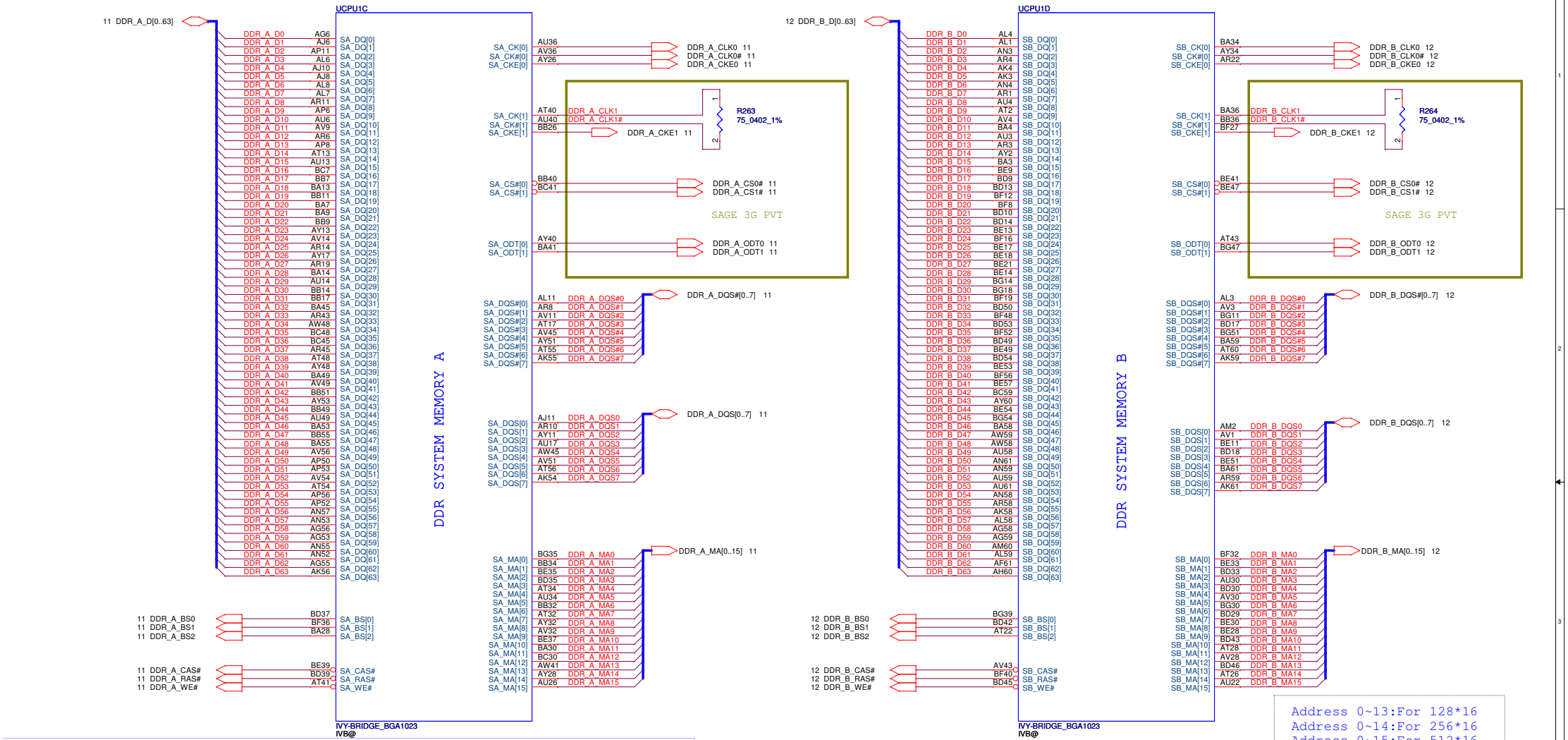
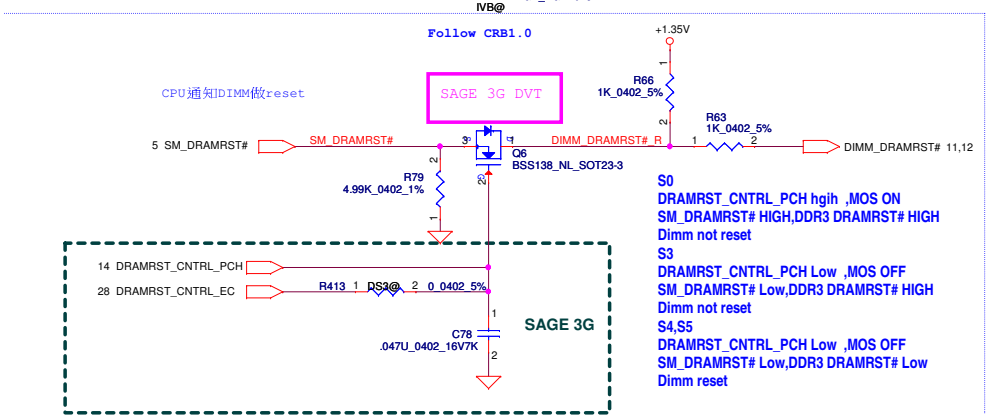
Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 5 of 52





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Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title: PROCESSOR(3/7) DDRIII

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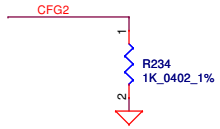
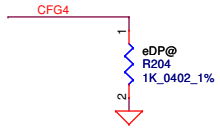
Default "1",EDS R1.0 P.88

CFG Straps for Processor

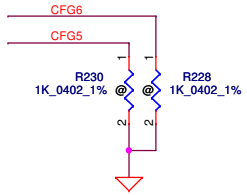
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



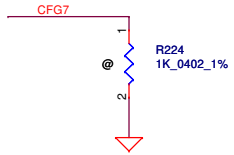
eDP enable	
CFG4	★ 1:Disable 0:Enable

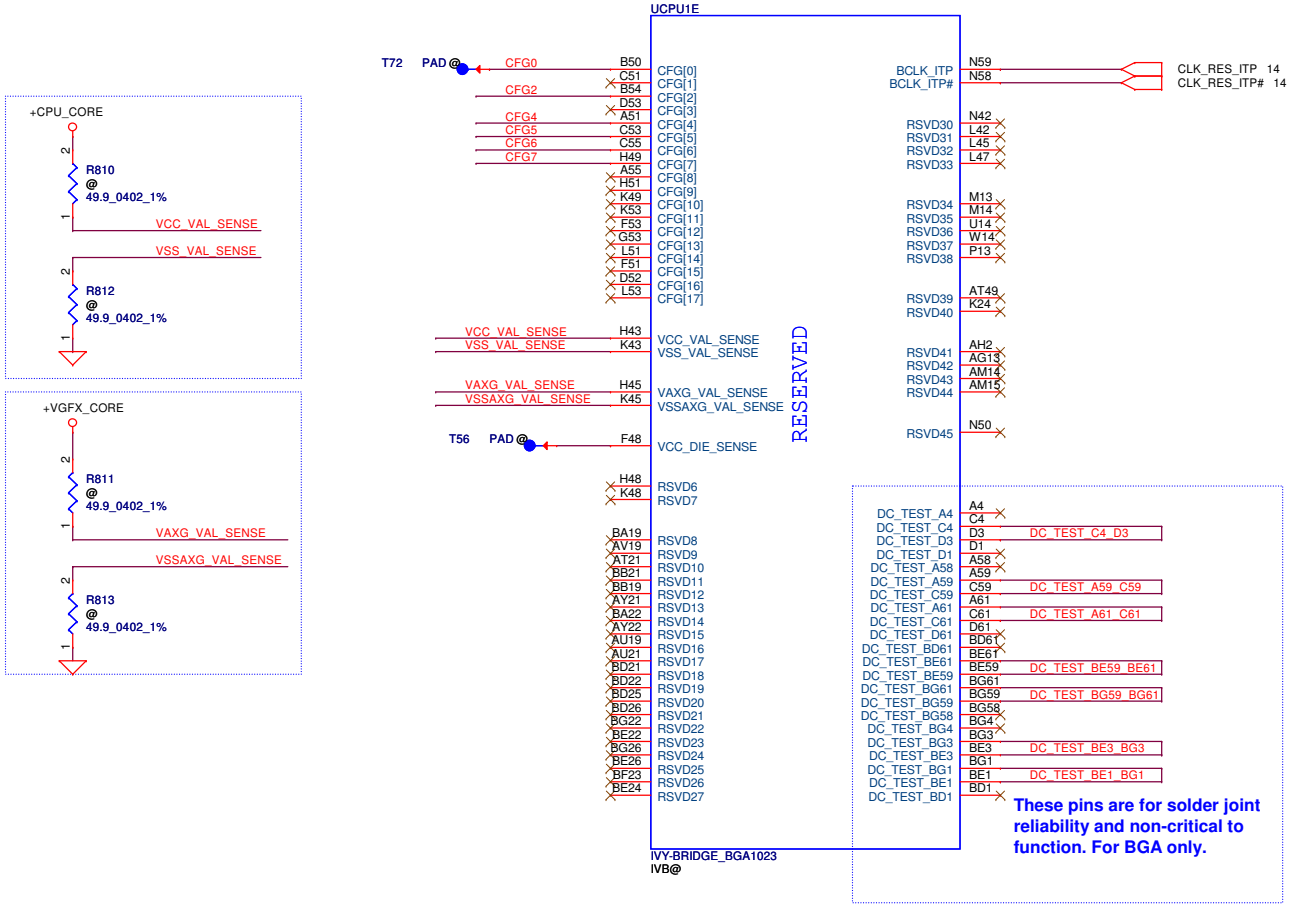


PCIE Port Bifurcation Straps	
CFG[6:5]	★11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	CRB1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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POWER

ULV SC/DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
3*330uF,12*22uF(0805),16*2.2uF(0402)
PD0.9

CORE SUPPLY

A26	VCC[1]
A29	VCC[2]
A31	VCC[3]
A34	VCC[4]
A35	VCC[5]
A38	VCC[6]
A39	VCC[7]
A42	VCC[8]
C26	VCC[9]
C27	VCC[10]
C32	VCC[11]
C34	VCC[12]
C37	VCC[13]
C39	VCC[14]
C42	VCC[15]
D27	VCC[16]
D32	VCC[17]
D34	VCC[18]
D37	VCC[19]
D39	VCC[20]
D42	VCC[21]
E26	VCC[22]
E28	VCC[23]
E32	VCC[24]
E34	VCC[25]
E37	VCC[26]
E38	VCC[27]
F25	VCC[28]
F26	VCC[29]
F28	VCC[30]
F32	VCC[31]
F34	VCC[32]
F37	VCC[33]
F38	VCC[34]
F42	VCC[35]
G42	VCC[36]
H25	VCC[37]
H26	VCC[38]
H28	VCC[39]
H29	VCC[40]
H32	VCC[41]
H34	VCC[42]
H35	VCC[43]
H37	VCC[44]
H38	VCC[45]
H40	VCC[46]
J25	VCC[47]
J26	VCC[48]
J28	VCC[49]
J29	VCC[50]
J32	VCC[51]
J34	VCC[52]
J35	VCC[53]
J37	VCC[54]
J38	VCC[55]
J40	VCC[56]
J42	VCC[57]
K26	VCC[58]
K27	VCC[59]
K29	VCC[60]
K32	VCC[61]
K34	VCC[62]
K35	VCC[63]
K37	VCC[64]
K39	VCC[66]
K42	VCC[67]
L25	VCC[68]
L28	VCC[69]
L33	VCC[70]
L36	VCC[71]
L40	VCC[72]
N26	VCC[73]
N30	VCC[74]
N34	VCC[75]
N38	VCC[76]

PEG IO AND DDR IO

+1.05VS_VTT

VCCIO[1]	AF46
VCCIO[3]	AG48
VCCIO[4]	AG50
VCCIO[5]	AG51
VCCIO[6]	AJ17
VCCIO[7]	AJ21
VCCIO[8]	AJ25
VCCIO[9]	AJ43
VCCIO[10]	AJ47
VCCIO[11]	AK50
VCCIO[12]	AK51
VCCIO[13]	AL14
VCCIO[14]	AL15
VCCIO[15]	AL16
VCCIO[16]	AL20
VCCIO[17]	AL22
VCCIO[18]	AL26
VCCIO[19]	AL45
VCCIO[20]	AL48
VCCIO[21]	AM16
VCCIO[22]	AM17
VCCIO[23]	AM21
VCCIO[24]	AM43
VCCIO[25]	AM47
VCCIO[26]	AN20
VCCIO[27]	AN42
VCCIO[28]	AN45
VCCIO[29]	AN48

INTEL Recommend VCCIO
PD 0.9

330uF 1+1
10uF (0603) *5
1uF (0201) *16

+1.05VS_VTT

VCCIO[30]	AA14
VCCIO[31]	AA15
VCCIO[32]	AB17
VCCIO[33]	AB20
VCCIO[34]	AC13
VCCIO[35]	AD16
VCCIO[36]	AD18
VCCIO[37]	AD21
VCCIO[38]	AE14
VCCIO[39]	AE15
VCCIO[40]	AF16
VCCIO[41]	AF18
VCCIO[42]	AF20
VCCIO[43]	AG15
VCCIO[44]	AG16
VCCIO[45]	AG17
VCCIO[46]	AG20
VCCIO[47]	AG21
VCCIO[48]	AJ14
VCCIO[49]	AJ15

330uF 1
10uF (0603) *5
1uF (0201) *10

+1.05VS_VTT

VCCIO50	W16
VCCIO51	W17

+3VALW

R521 10K_0402_5%

VCCIO_SEL

R520 10K_0402_5% @

VCCIO_SEL For 2012 CPU support		
A19	*	1 : +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL — BC22 VCCIO_SEL_R — R582 @ 0_0402_5%

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

SAGE 3G

C951 1U_0402_6.3V6K

+1.05VS_VTT

R574 130_0402_5%

Check List R1.5
VIDALERT#:75ohm ±5% pull-up to VCCIO close to IMVP7
VIDSCLK: 55ohm ±5% pull-up to VCCIO close to IMVP7
VIDSOUT: 130ohm ±5% pull-up to VCCIO close to CPU
130ohm ±5% pull-up to VCCIO close to IMVP7

SVID

VIDALERT#	A44	H_CPU_SVIDALRT#	R576 43_0402_1%	VR_SVID_ALRT# 42
VIDSCLK	B43	H_CPU_SVIDCLK	R577 @ 0_0402_5%	VR_SVID_CLK 42
VIDSOUT	C44	H_CPU_SVIDDAT	R578 @ 0_0402_5%	VR_SVID_DAT 42

SENSE LINES

+CPU_CORE

R588 100_0402_1%

Place the PU,PD
resistors close to CPU

VCC_SENSE	F43	VCCSENSE_R	R579 @ 0_0402_5%	VCCSENSE 42
VSS_SENSE	G43	VSSSENSE_R	R581 @ 0_0402_5%	VSSSENSE 42

+1.05VS_VTT

R107 10_0402_5%

R589 100_0402_1%

VCCIO_SENSE	AN16	VCCIO_SENSE	VCCIO_SENSE 40
VSS_SENSE_VCCIO	AN17	VSSIO_SENSE	

Check List R1.5
VCCSENSE:100ohm ±1% pull-up to VCC near processor.
VSSSENSE:100ohm ±1% pull-down to GND near processor.

R105 10_0402_5%

Should change to connect from
power cirucit & layout differential
with VCCIO_SENSE.

IVY-BRIDGE_BGA1023
IVB@

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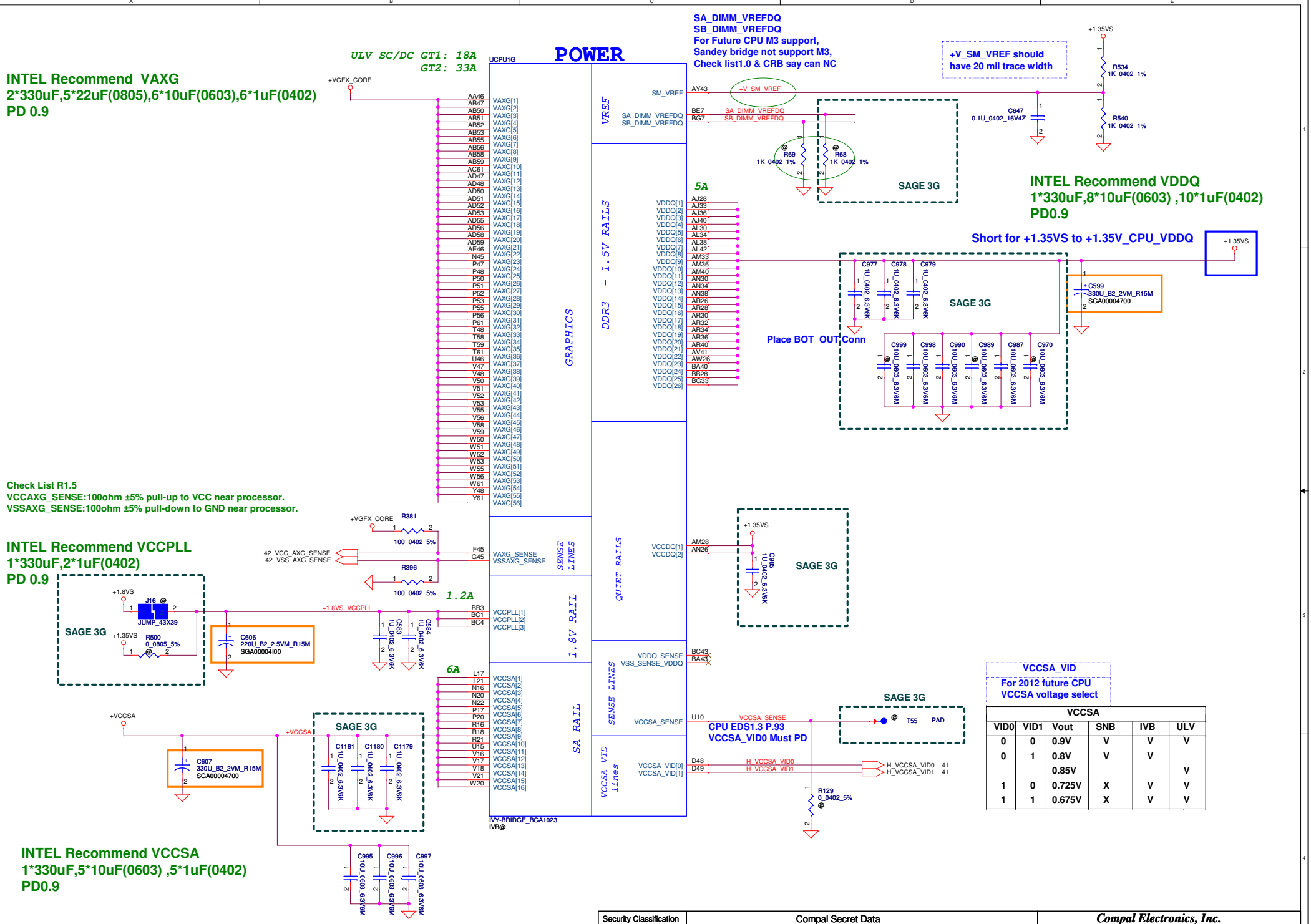
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 8 of 52



VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	
		0.85V			V
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V

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Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

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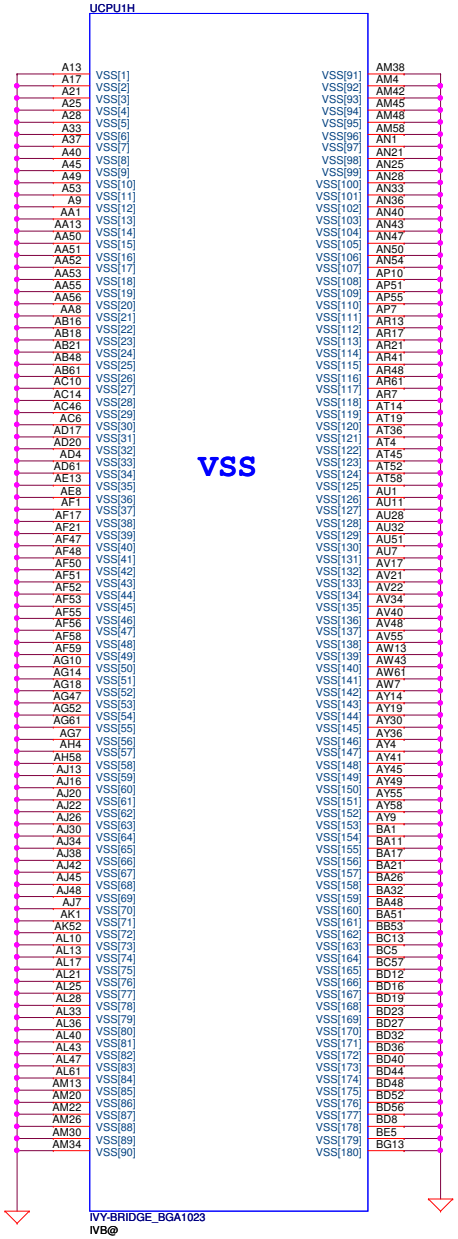
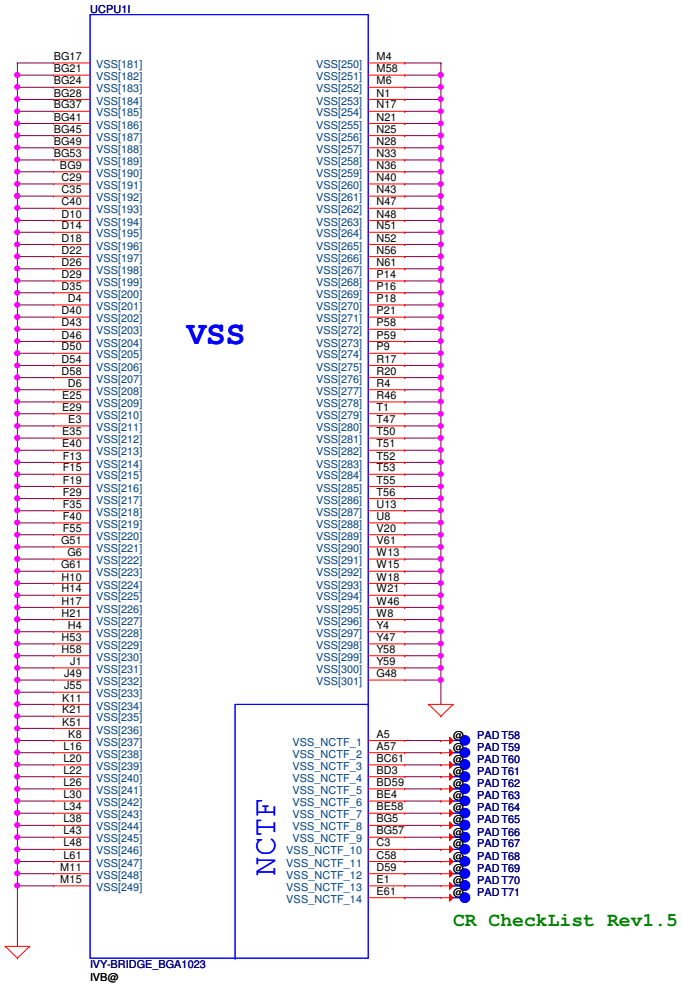
Date: Wednesday, March 13, 2013 | Sheet 9 of 52





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Issued Date	2011/06/24	Deciphered Date	2012/06/02

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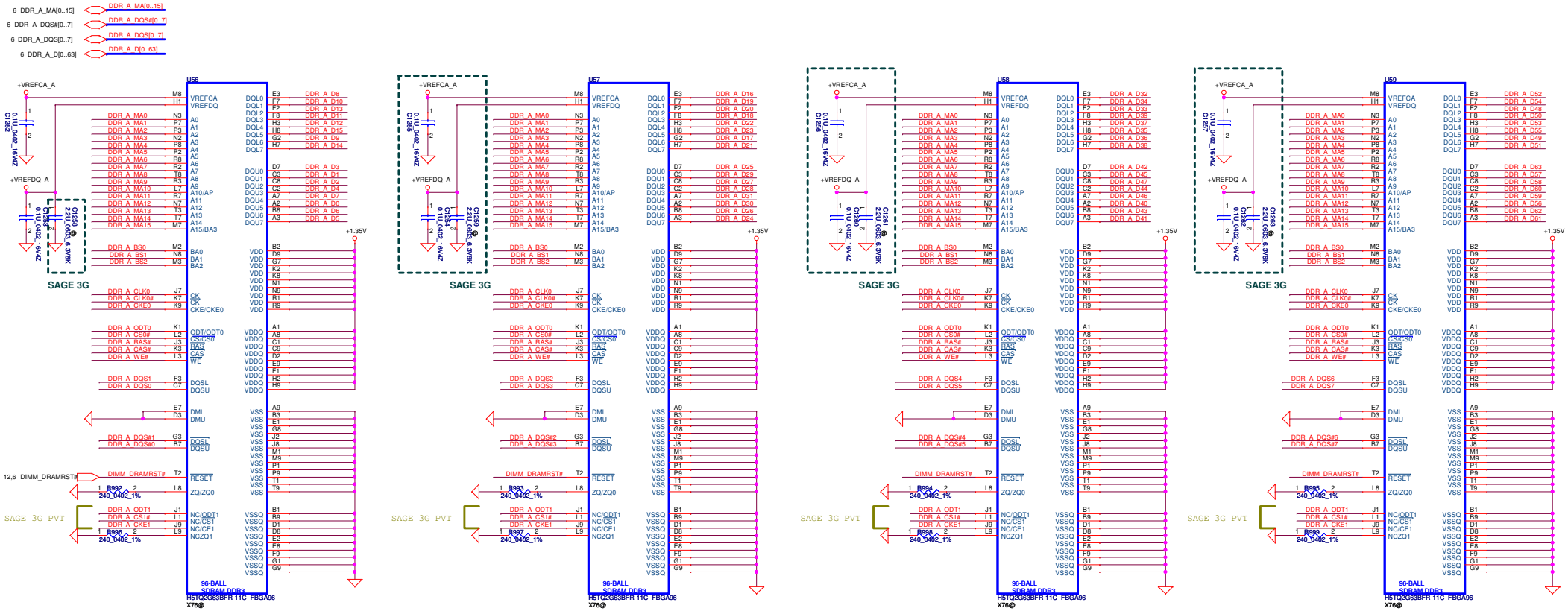
Compal Electronics, Inc.

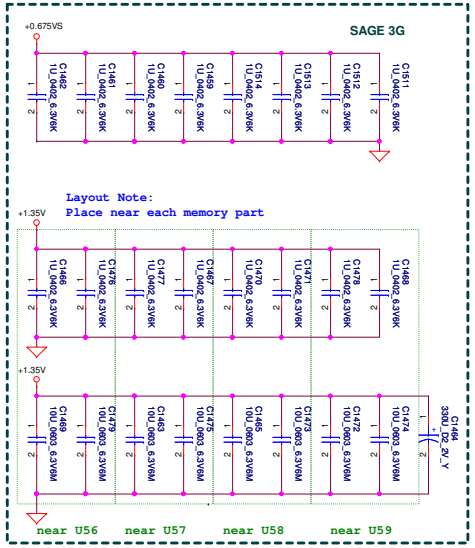
Title: **PROCESSOR(7/7) VSS**

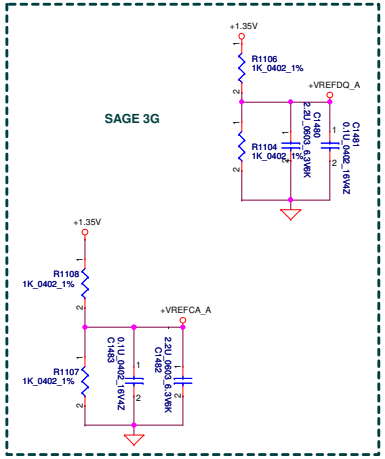
Size: Custom | Document Number: **V1JB1 M/B LA-A041P Schematic** | Rev: 0.1

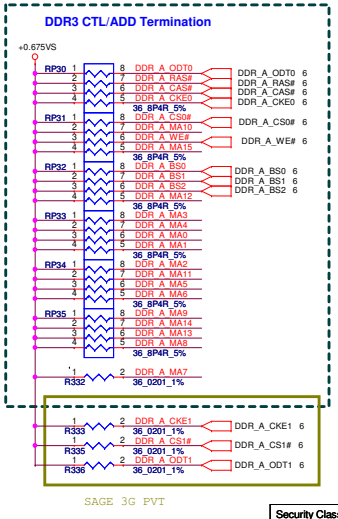
Date: Wednesday, March 13, 2013 | Sheet 10 of 52

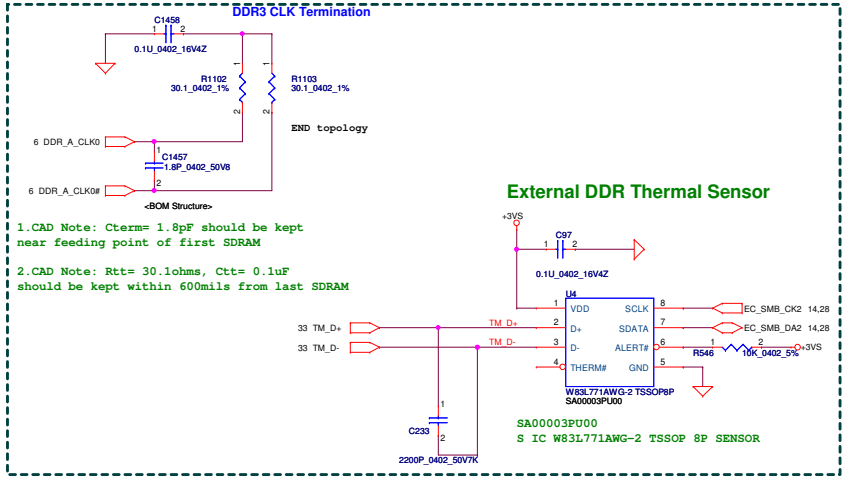
Channel A











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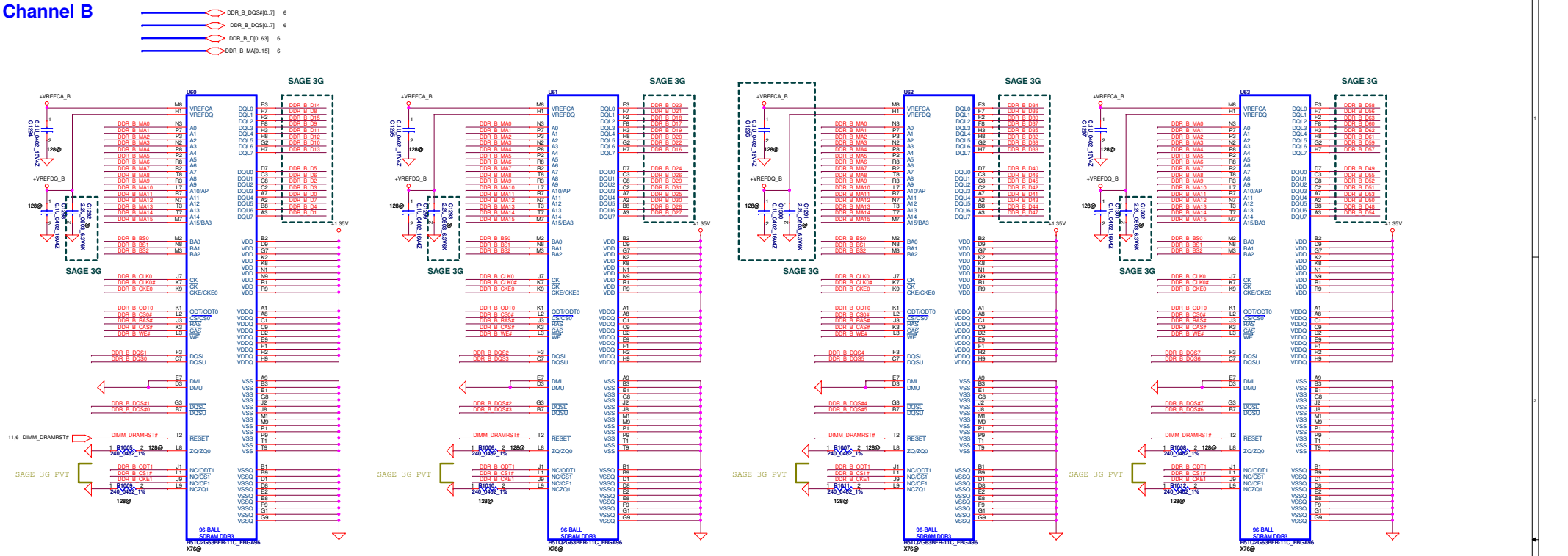
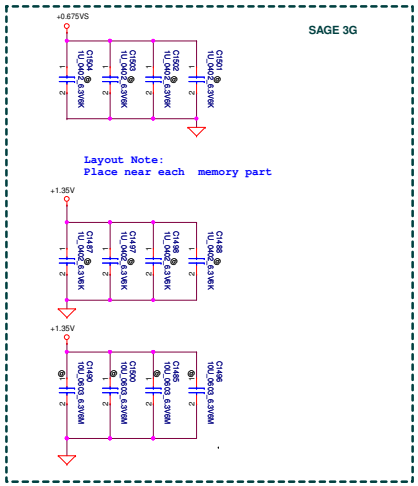
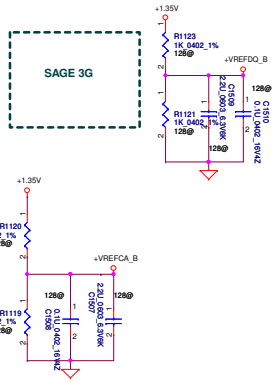
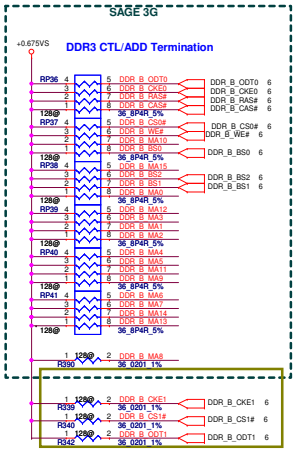
Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1
Date: Wednesday, March 13, 2013	Sheet 11 of 52	

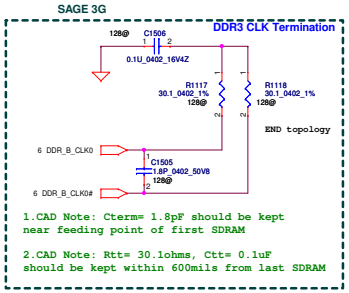
Channel B











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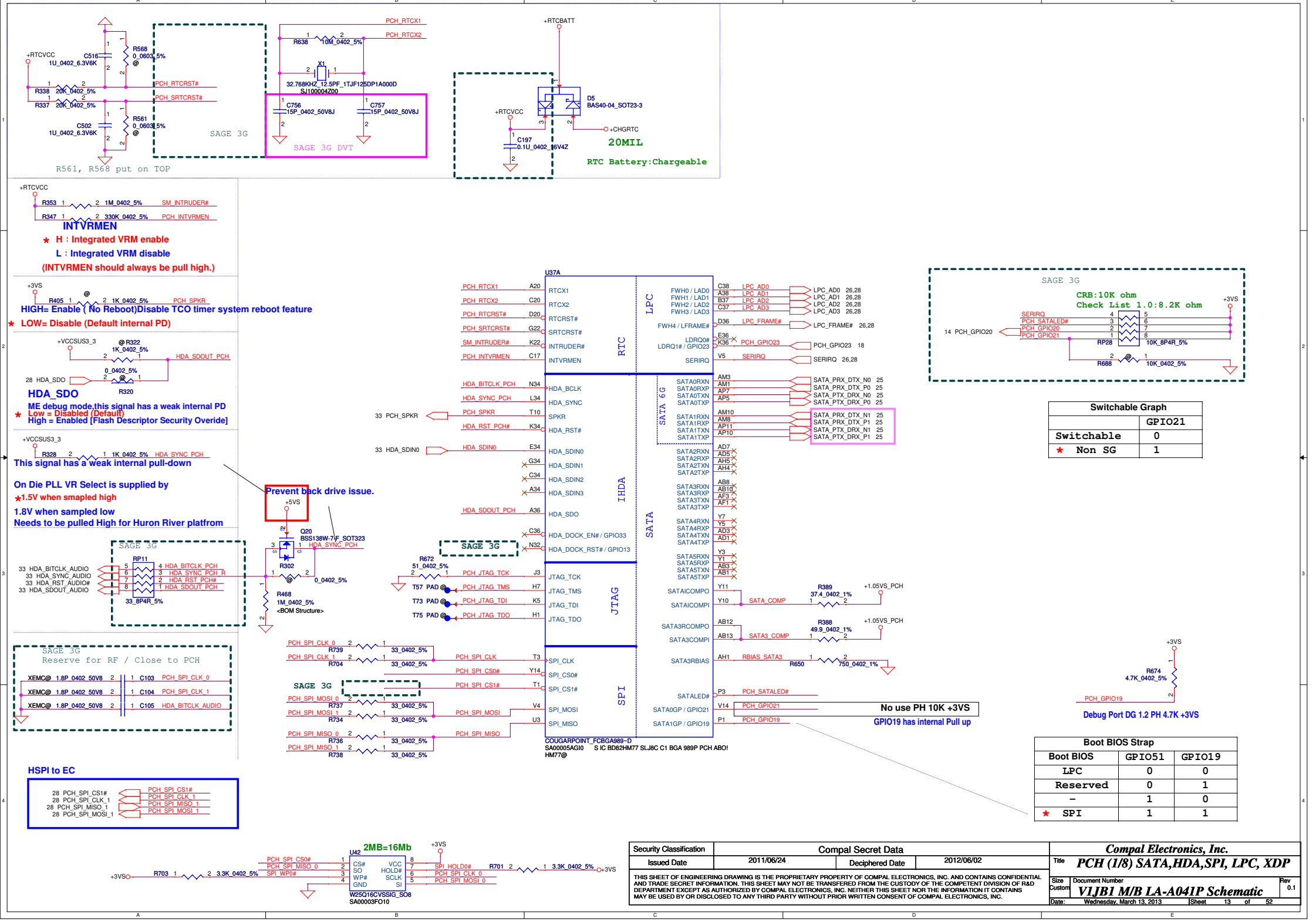
Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1
Date: Wednesday, March 13, 2013	Sheet 12 of 52	



SAGE 3G

Switchable Graph	
	GPIO21
Switchable	0
★ Non SG	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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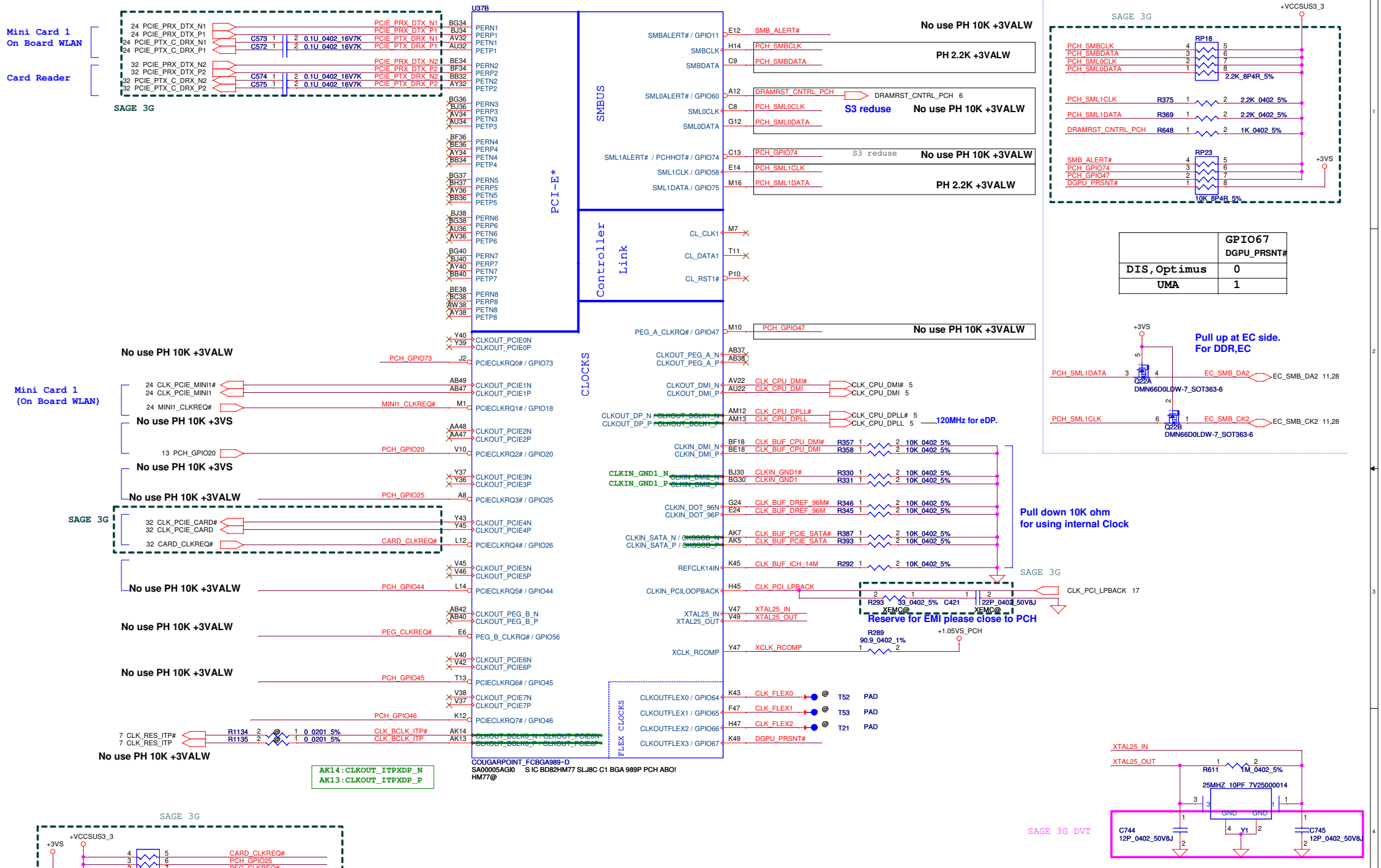
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 13 of 52



	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

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Issued Date	2011/06/24	Deciphered Date	2012/06/02

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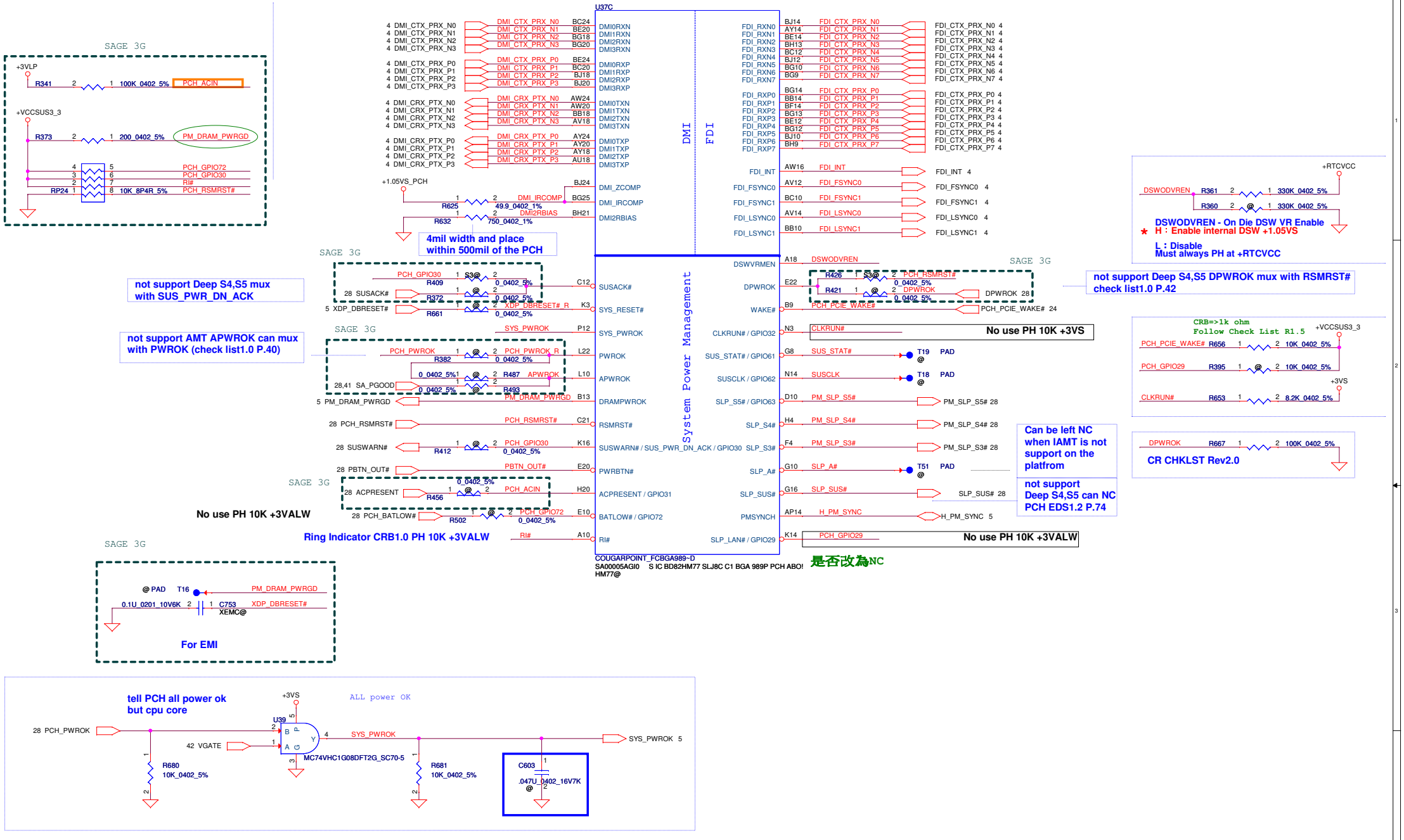
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 14 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title: PCH (3/8) DMI,FDI,PM
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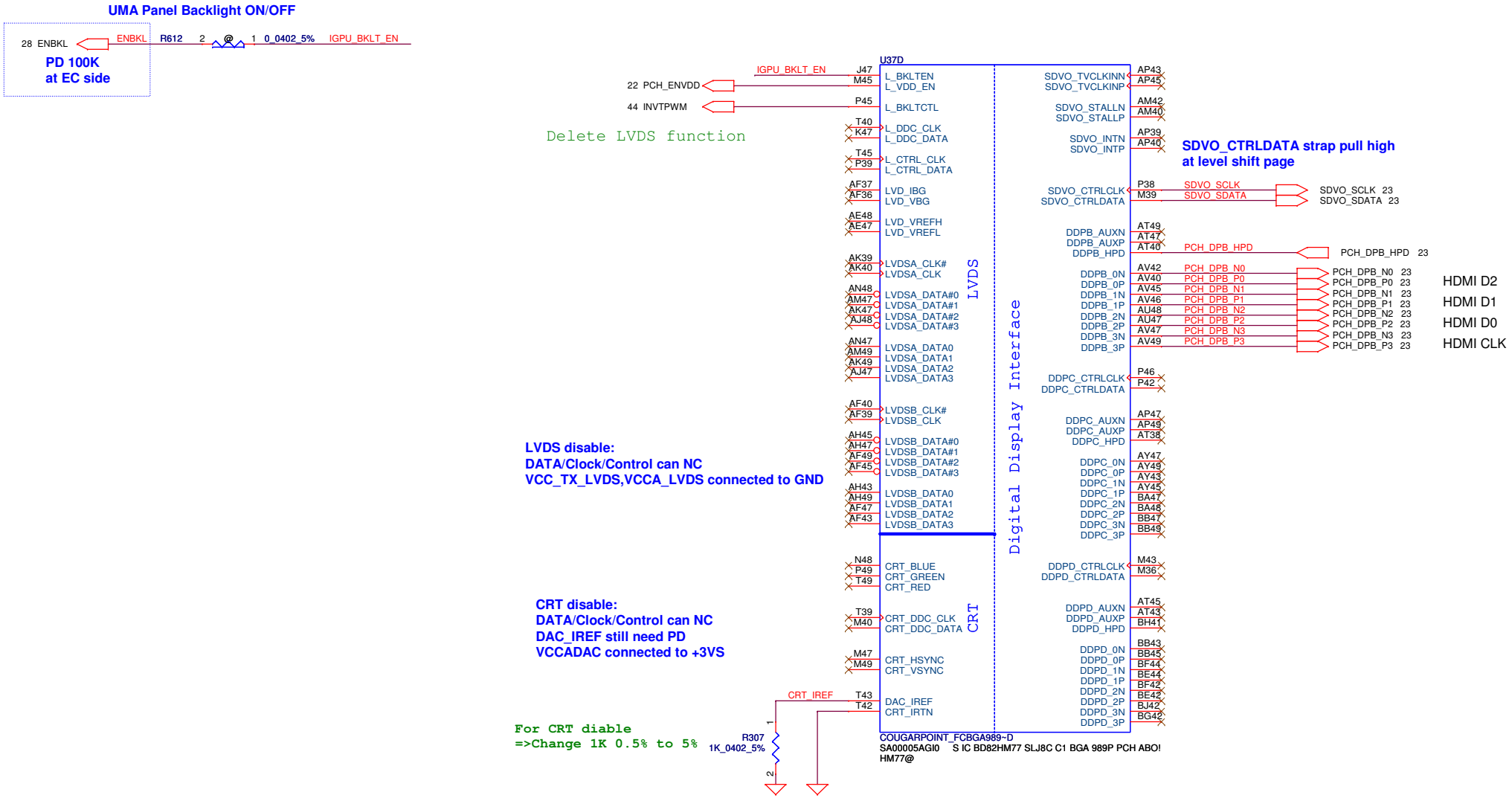
				Date: Wednesday, March 13, 2013; Sheet 15 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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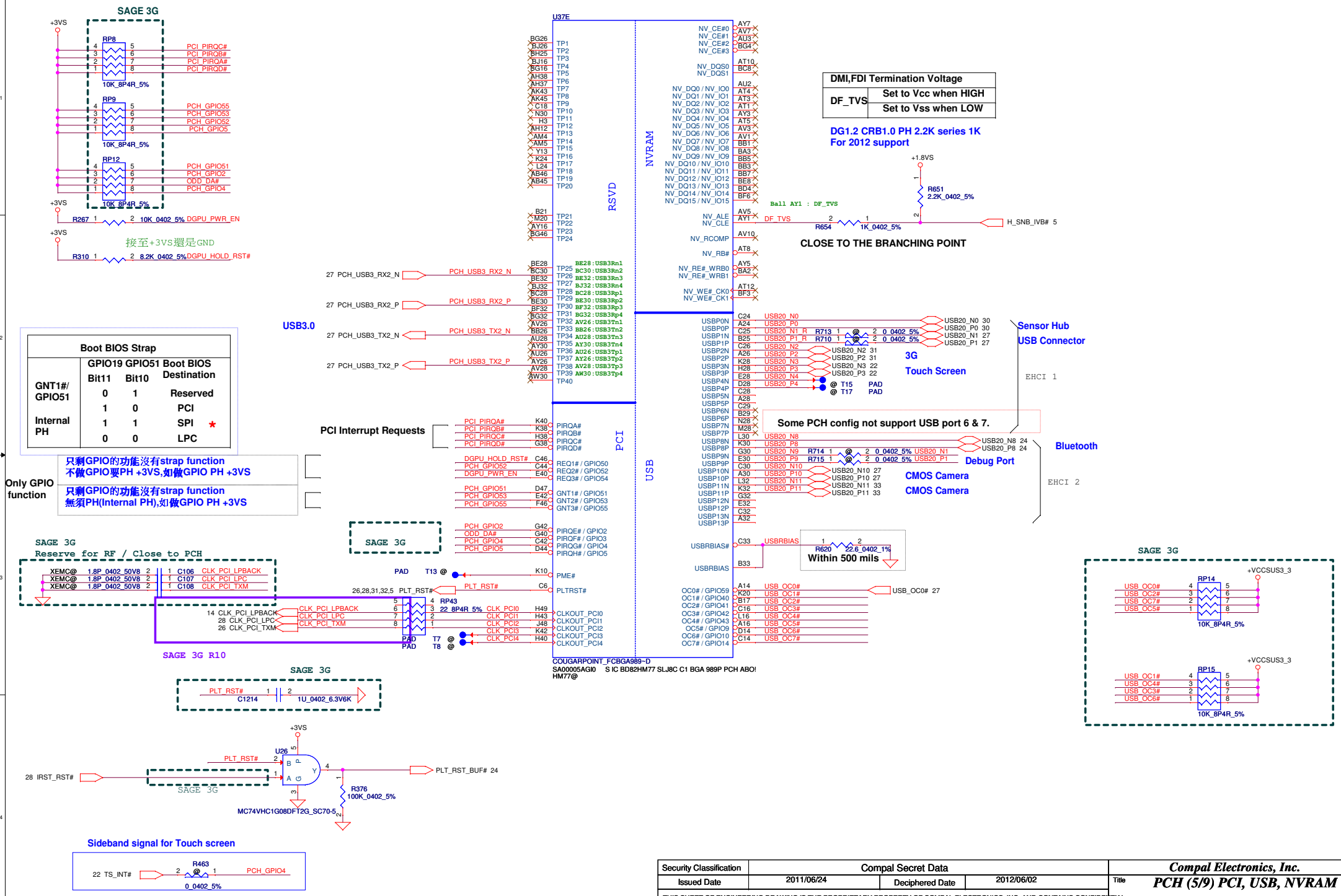
Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size: Custom | Document Number: **V1JB1 M/B LA-A041P Schematic** | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 16 of 52



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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 17 of 52

HDA_SYNC PH(PLL =+1.5VS)

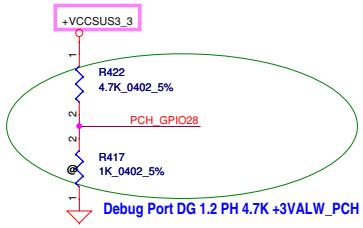
GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable

L : On-Die PLL Voltage Regulator disable



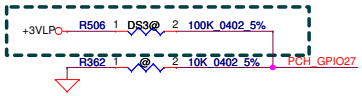
Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal

RTC alarm,Power BTN,GPIO27

PCH_GPIO27 (Have internal Pull-High)

SAGE 3G



SATA2GP/GPIO36,SATA3GP/GPIO37

1.Used as for Mechanical Presence detect -

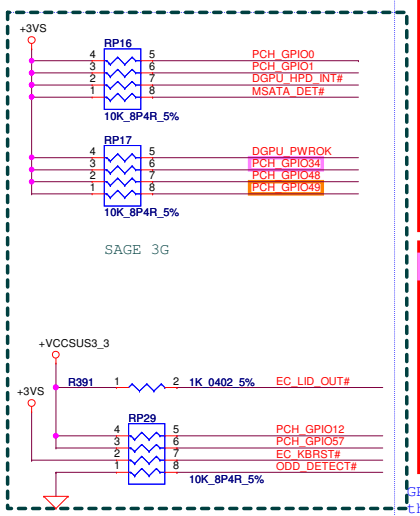
Use a weak external pull-up (150K-200k Ohms) to Vcc3_3 or use 10K external pull-up that is enabled only after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -

Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA*GP -

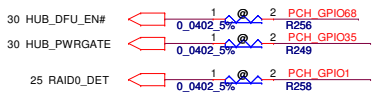
Use 8.2K-10K pull-down to ground.

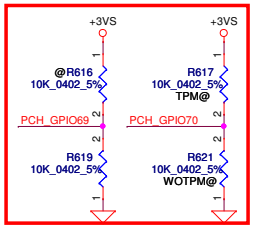


GPIO24 Unmultiplexed

NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

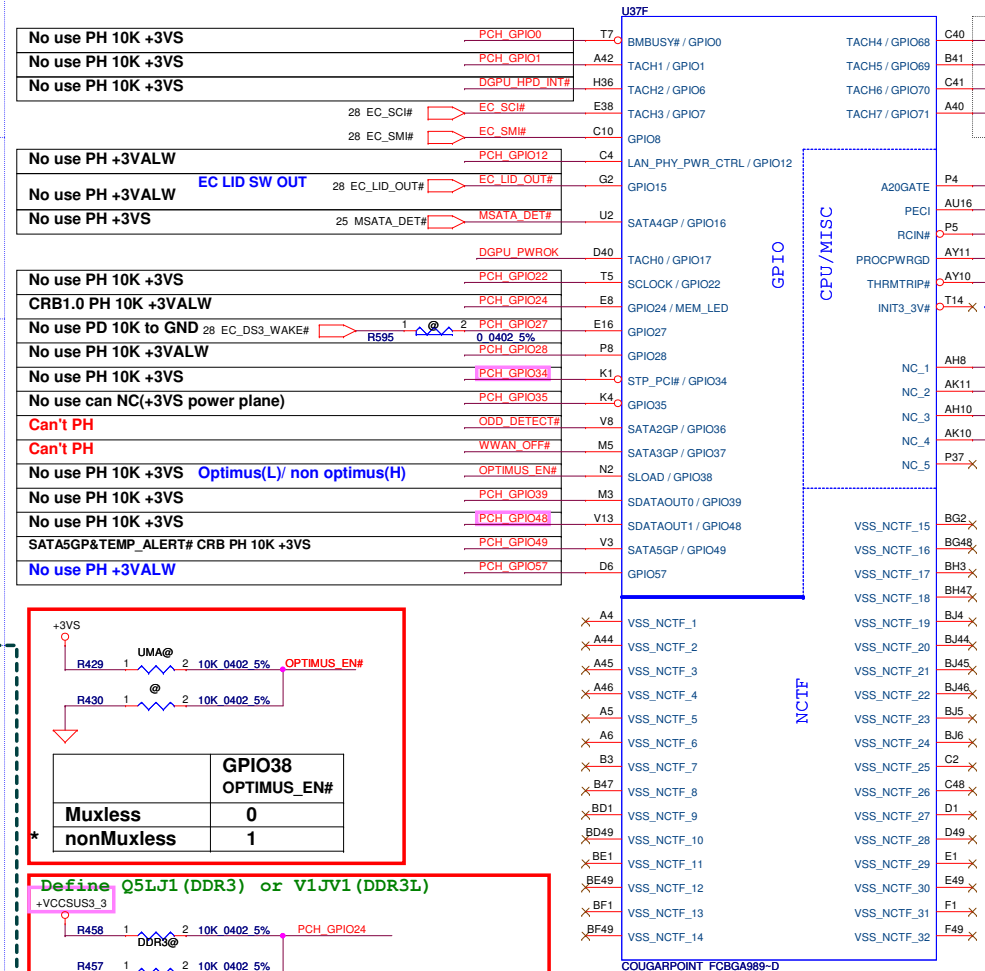
CRB1.0 PH10K to +3VALW





SW base on TPM table to detect HW TPM status

TPM Status	GPIO69	GPIO70
HW, SW without support TPM	0	0
Infineon TPM SLB9655	0	1
x	1	0
x	1	1



INIT3_3V Check list1.0 P.59

This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4

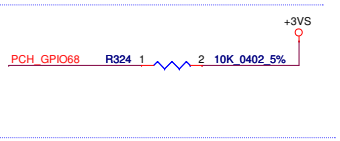
PD to GND

PECI CPU-EC

CTRL+ALT+DEL

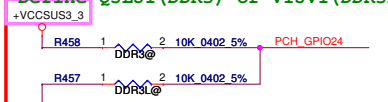
non CPU power ok

130c shut sown



	GPIO38 OPTIMUS_EN#
Muxless	0
* nonMuxless	1

Define Q5LJ1(DDR3) or V1JV1(DDR3L)



	GPIO24 PCH_GPIO24
* DDR3L(V1JV1)	0
DDR3	1

GPIO36/GPIO37 is Strap functionality

that requires internal pull down to be sampled at rising PWROK.

When uses as SATA2GP/SATA3GP for mechanical presence detect

-use a external pull up 150K-200K ohm to Vcc3_3

When used as GP input

-ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA*GP

-use 8.2K-10K pull-down

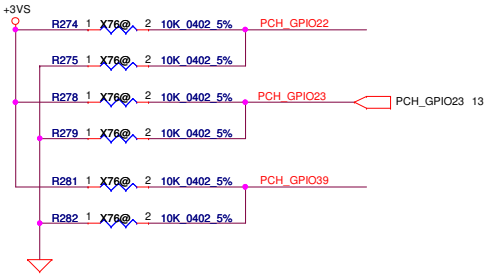
check list page 47

SA000059110 / ELPIDA DDR3L-1333

SA00005FV10 / HYNIX DDR3L-1333

SA00005HT80 / ELPIDA DDR3L-1600

		GPIO39	GPIO23	GPIO22
DDR3L-1333	Elpida Mono 512MB*4(Ch A)	0	0	0
DDR3L-1333	Hynix Mono 512MB*4(Ch A)	0	0	1
DDR3L-1333	Elpida Mono 512MB*8(Ch A,B)	0	1	0
DDR3L-1333	Hynix Mono 512MB*8(Ch A,B)	0	1	1
DDR3L-1600	Elpida Mono 512MB*4(Ch A)	1	0	0
DDR3L-1600		1	0	1
DDR3L-1600	Elpida Mono 512MB*8(Ch A,B)	1	1	0
DDR3L-1600		1	1	1



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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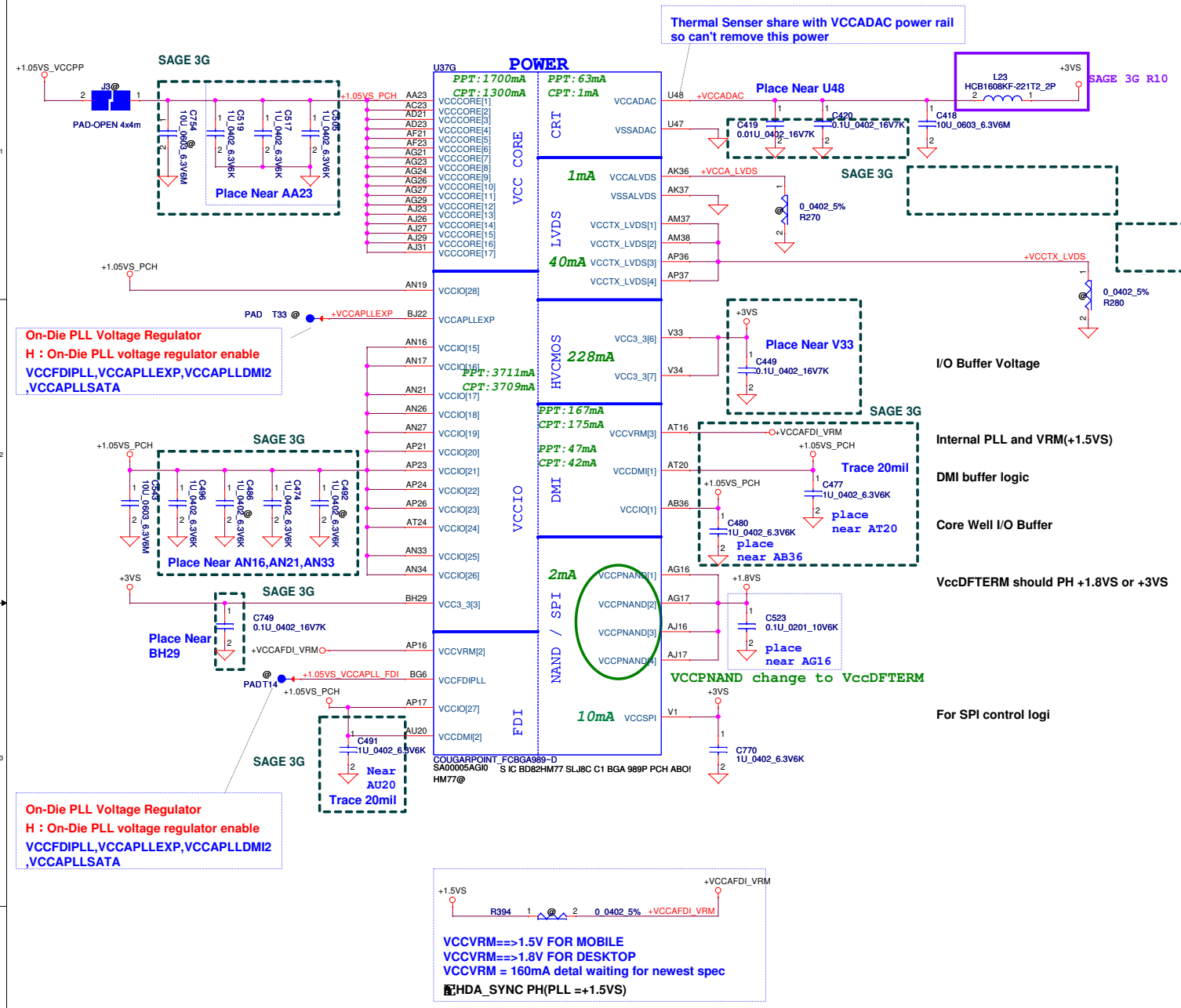
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 18 of 52



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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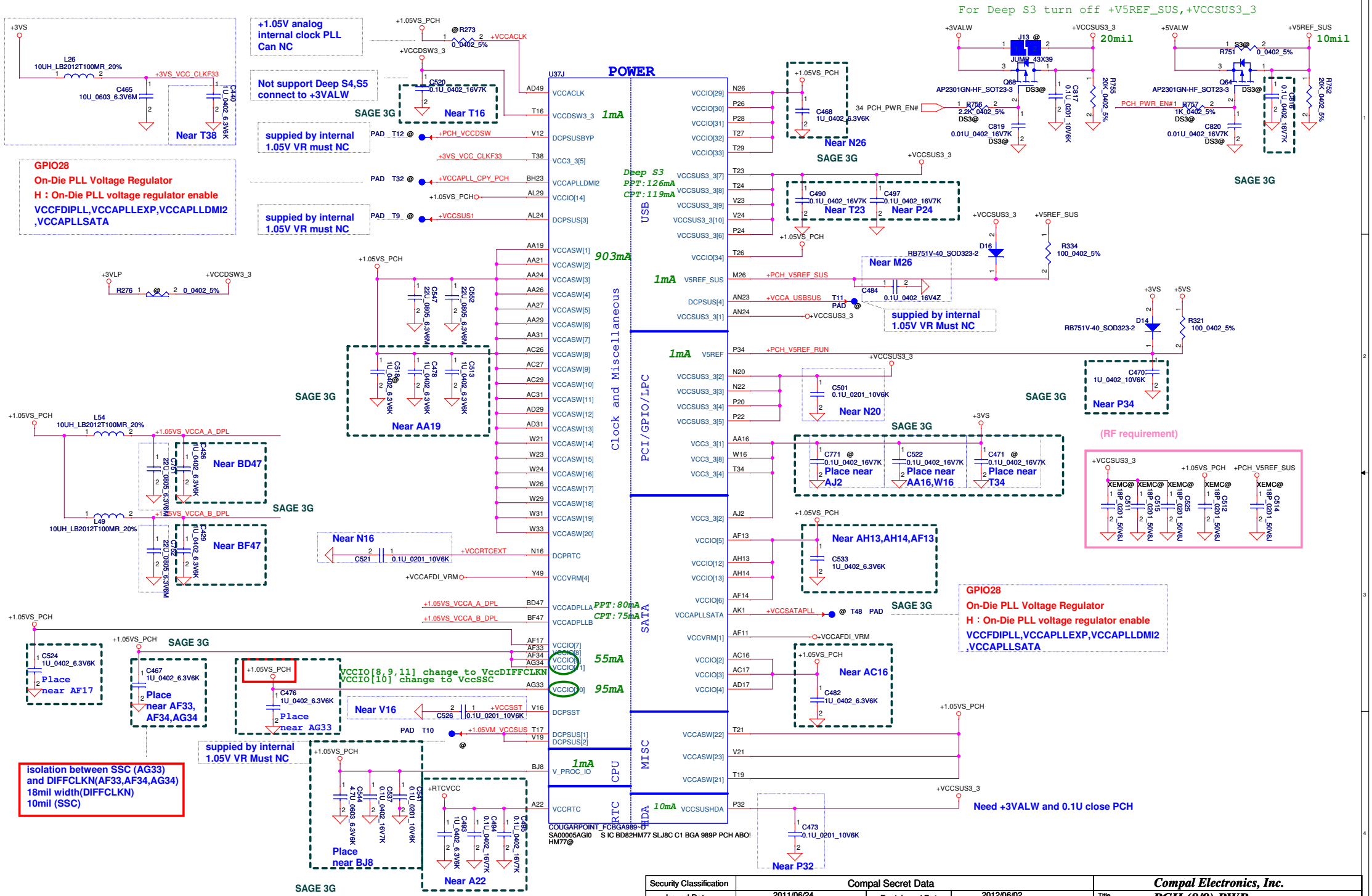
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Tuesday, March 26, 2013 | Sheet 19 of 52



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Issued Date	2011/06/24	Deciphered Date	2012/06/02

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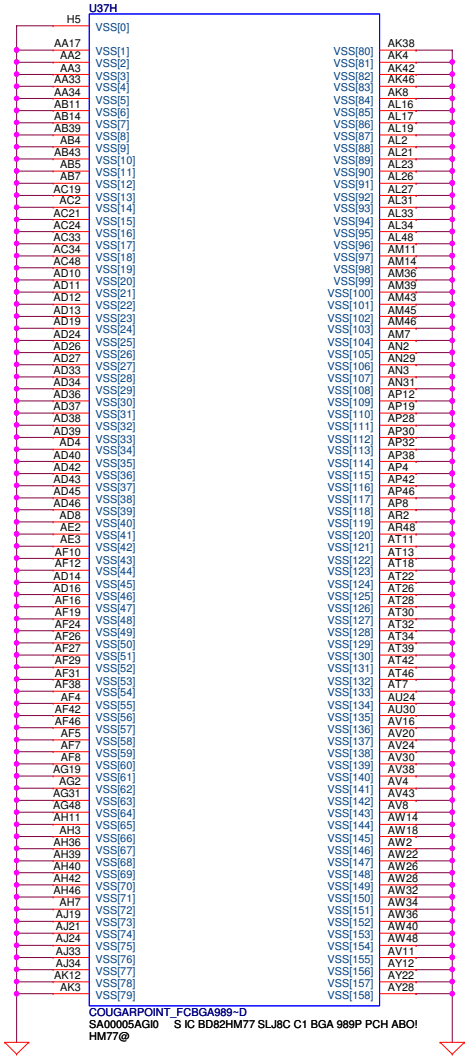
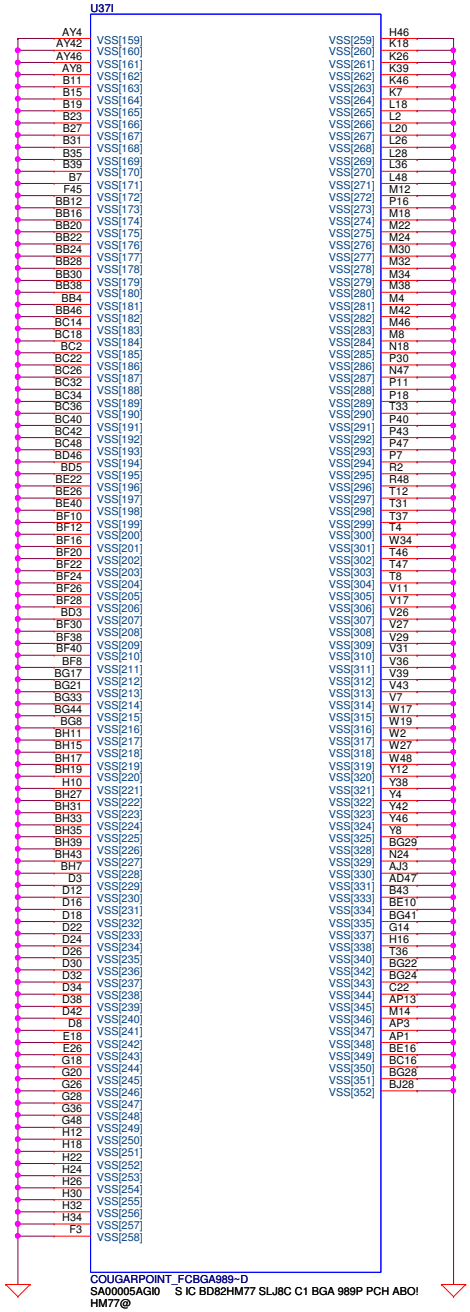
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 20 of 52





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Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title: PCH (9/9) VSS
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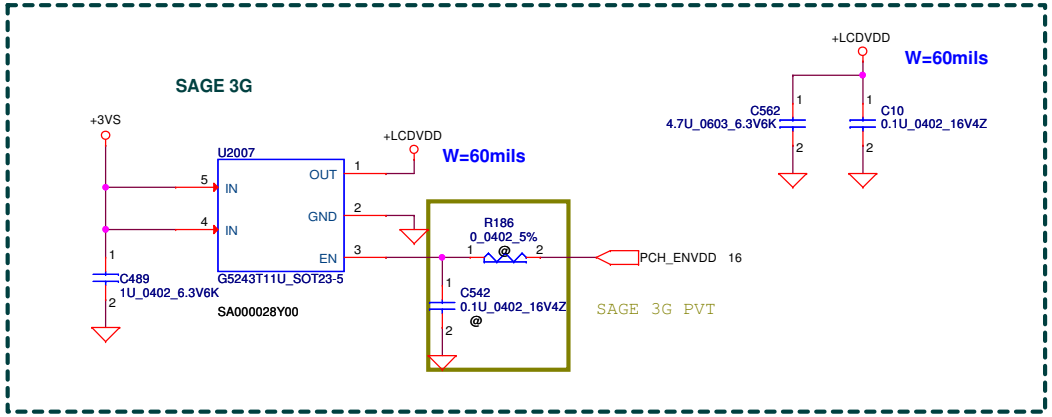
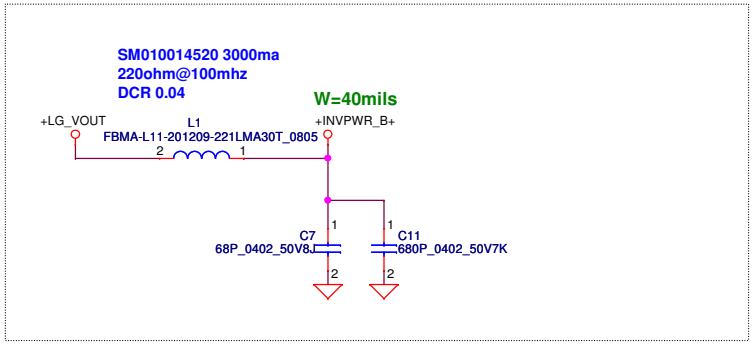
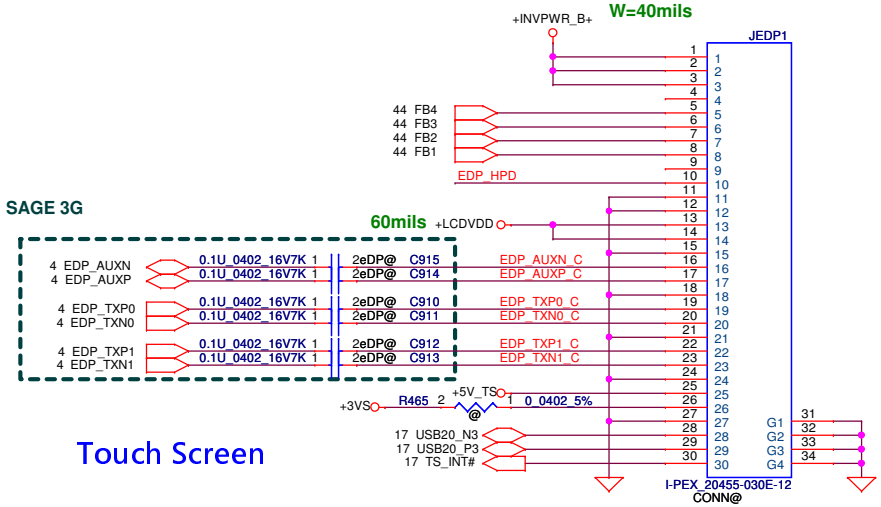
				Date: Wednesday, March 13, 2013; Sheet 21 of 52

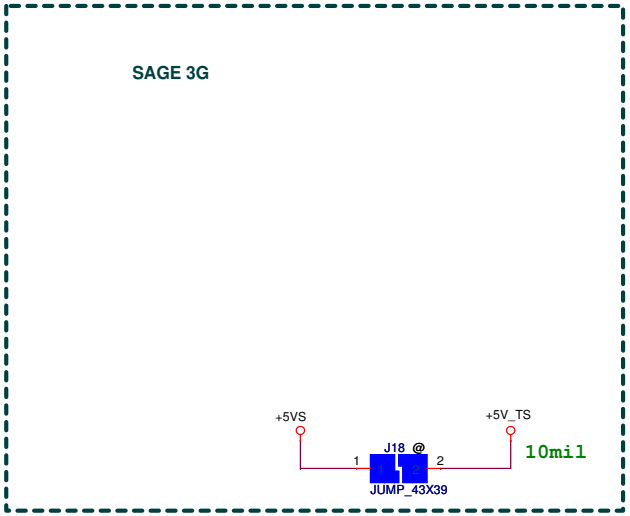
Panel POWER CIRCUIT

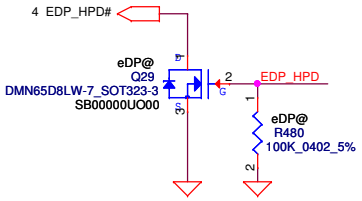


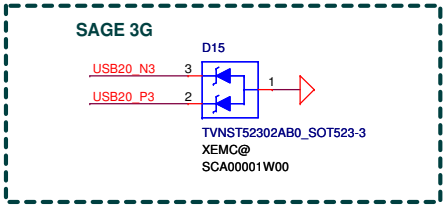


eDP PANEL Conn.









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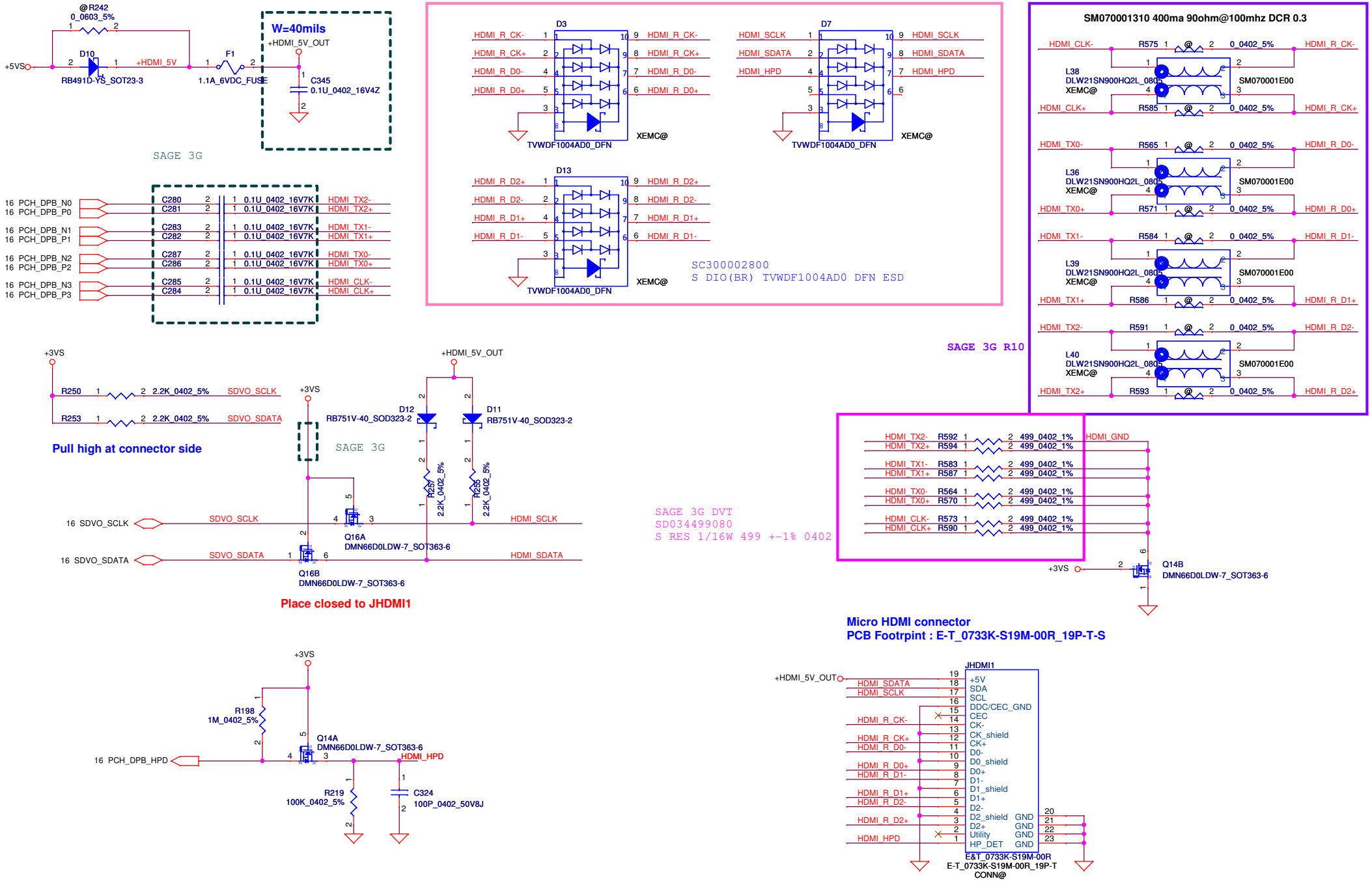
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 22 of 52



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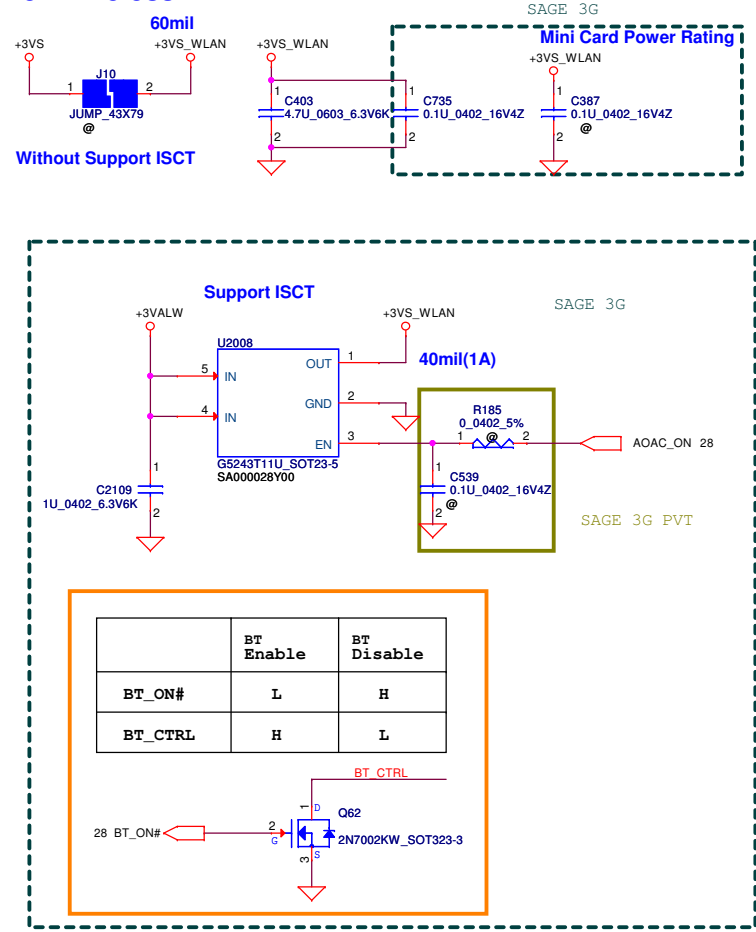
Compal Electronics, Inc.

Title: HDMI Connector

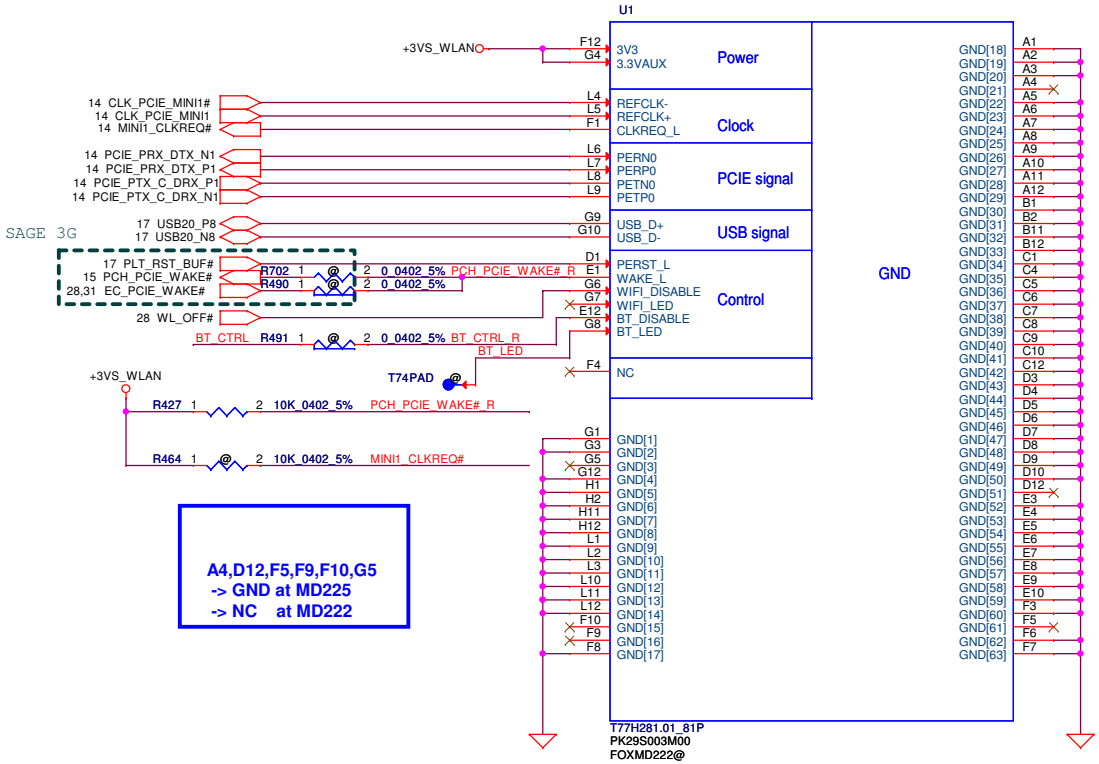
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Tuesday, March 26, 2013 | Sheet 23 of 52

For Wireless LAN



	BT Enable	BT Disable
BT_ON#	L	H
BT_CTRL	H	L



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Compal Electronics, Inc.

Title: On Board WLAN

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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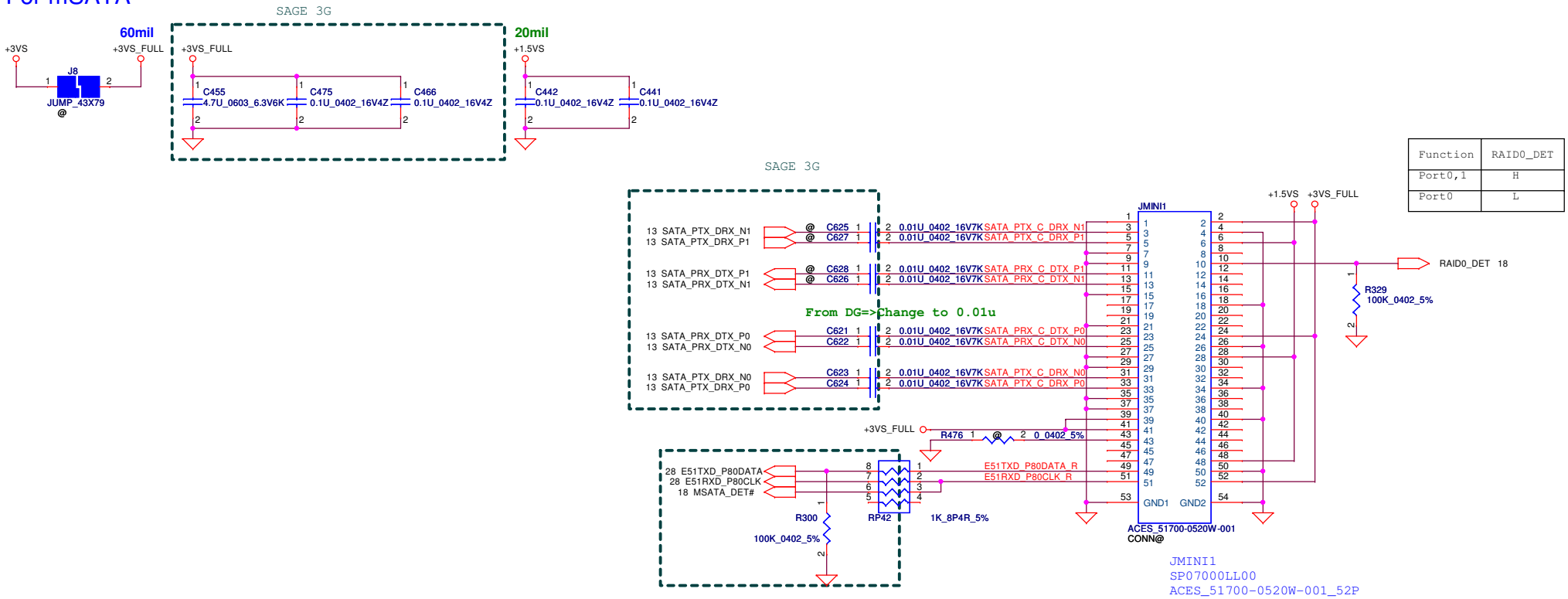
For mSATA



Function	RAID0_DET
Port0,1	H
Port0	L

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: mSATA HDD Connector

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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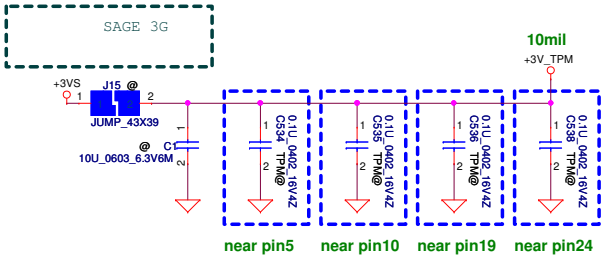
TPM



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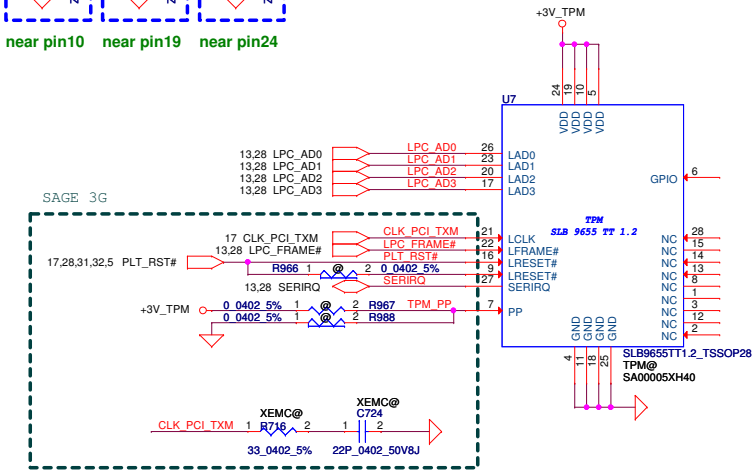
S IC SLB9655TT1.2 FW4.31 TSSOP 28P TPM



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Compal Electronics, Inc.

Title: TPM Infineon-SLB9655

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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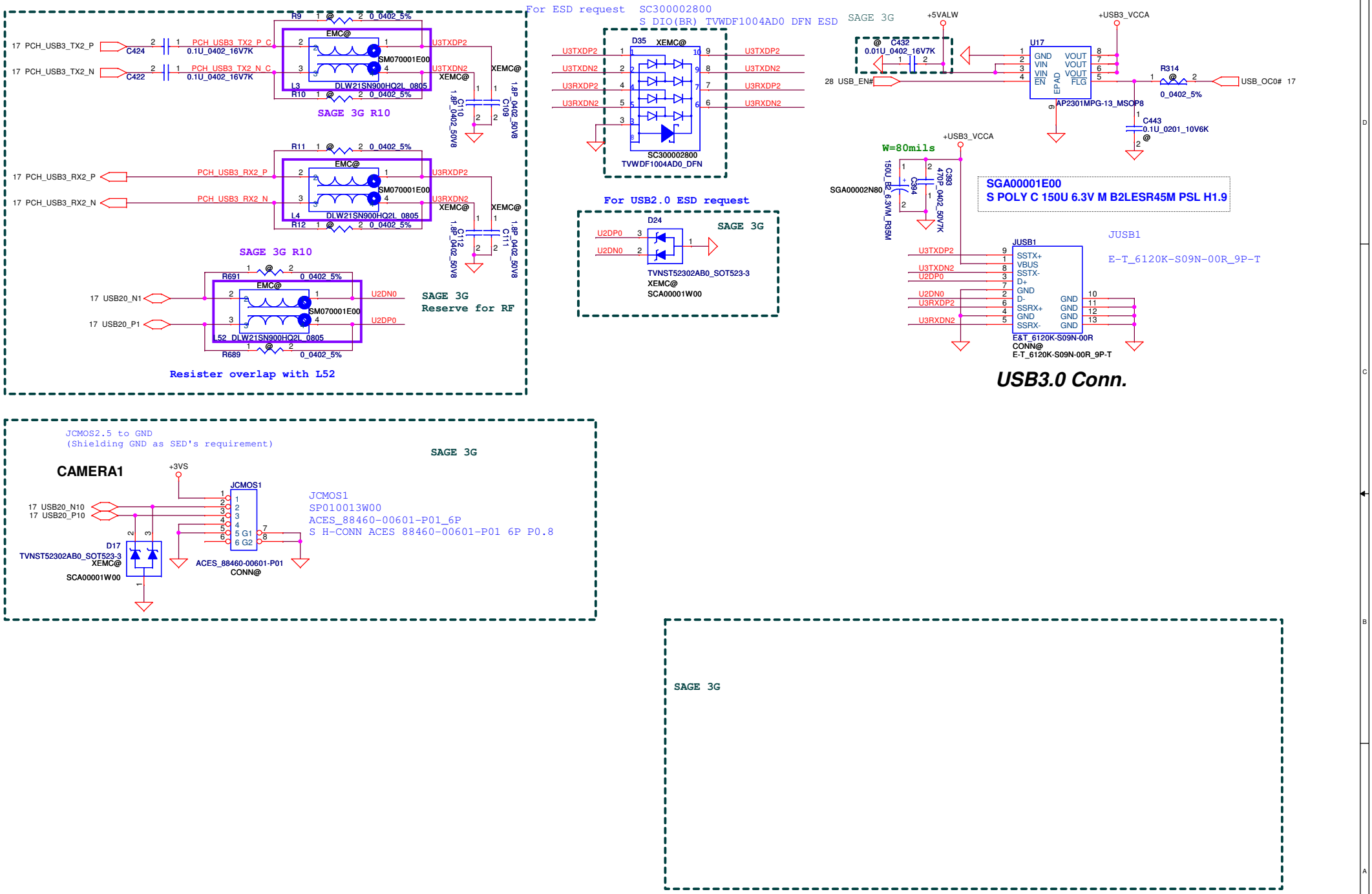

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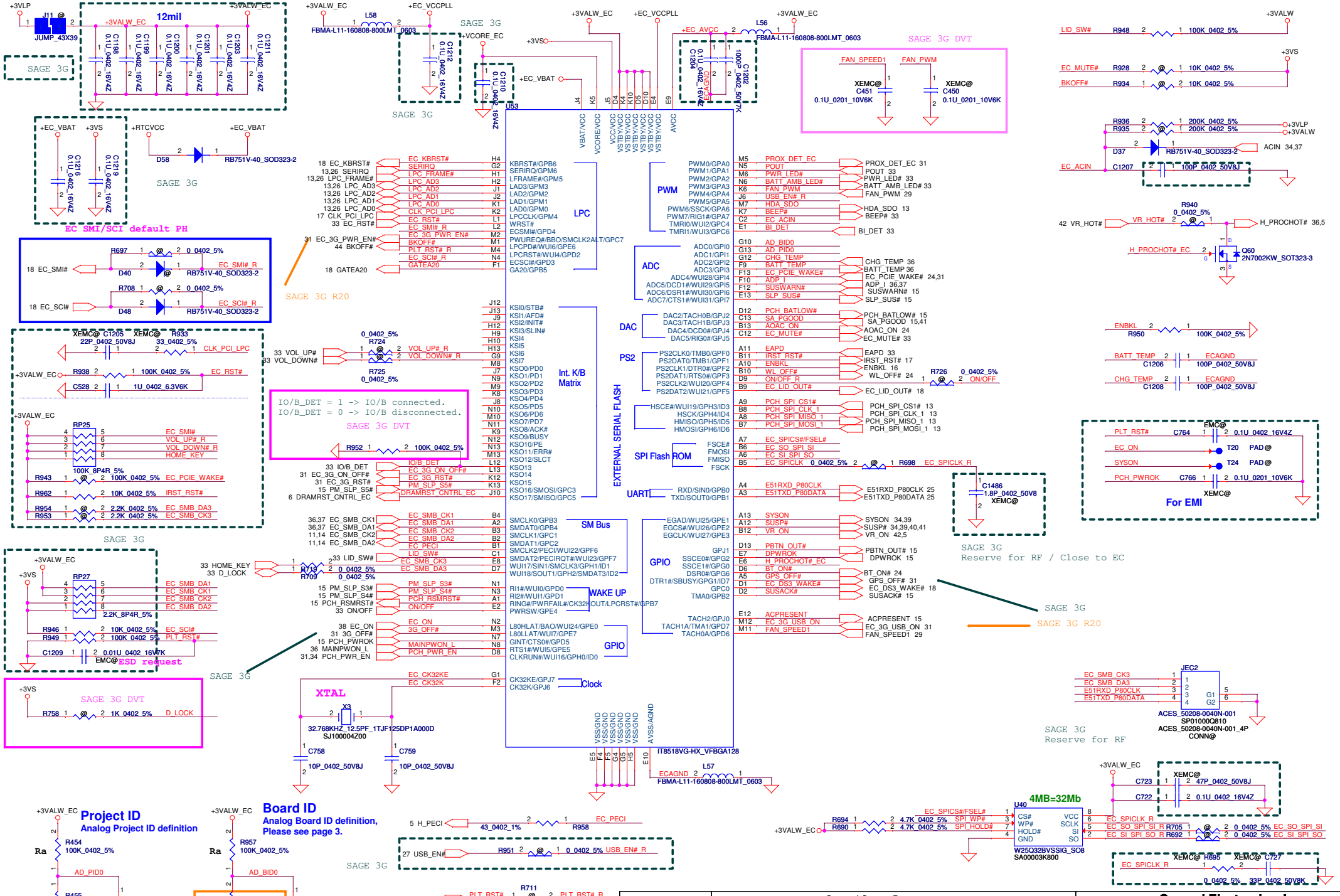
Title: USB3.0

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Tuesday, March 26, 2013 | Sheet 27 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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Compal Electronics, Inc.

Title: EC ITE-IT8518

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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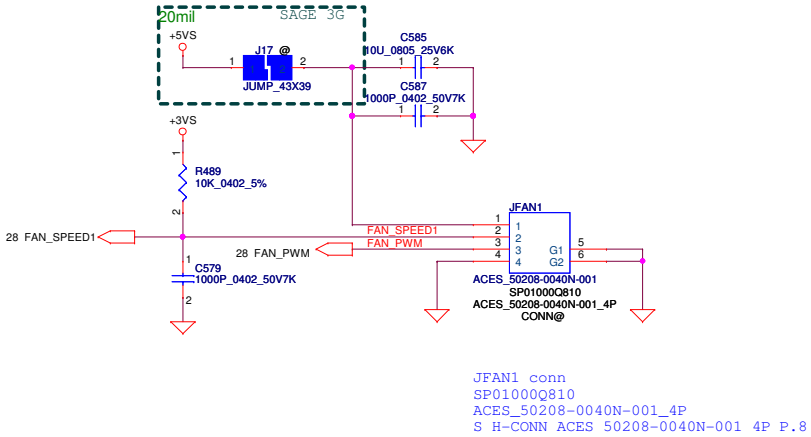
FAN Conn



JFAN1 conn
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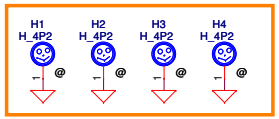
ACES_50208-0040N-001_4P
S H-CONN ACES 50208-0040N-001 4P P.8

定位孔

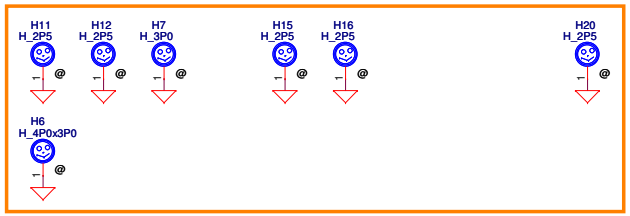
Thermal module

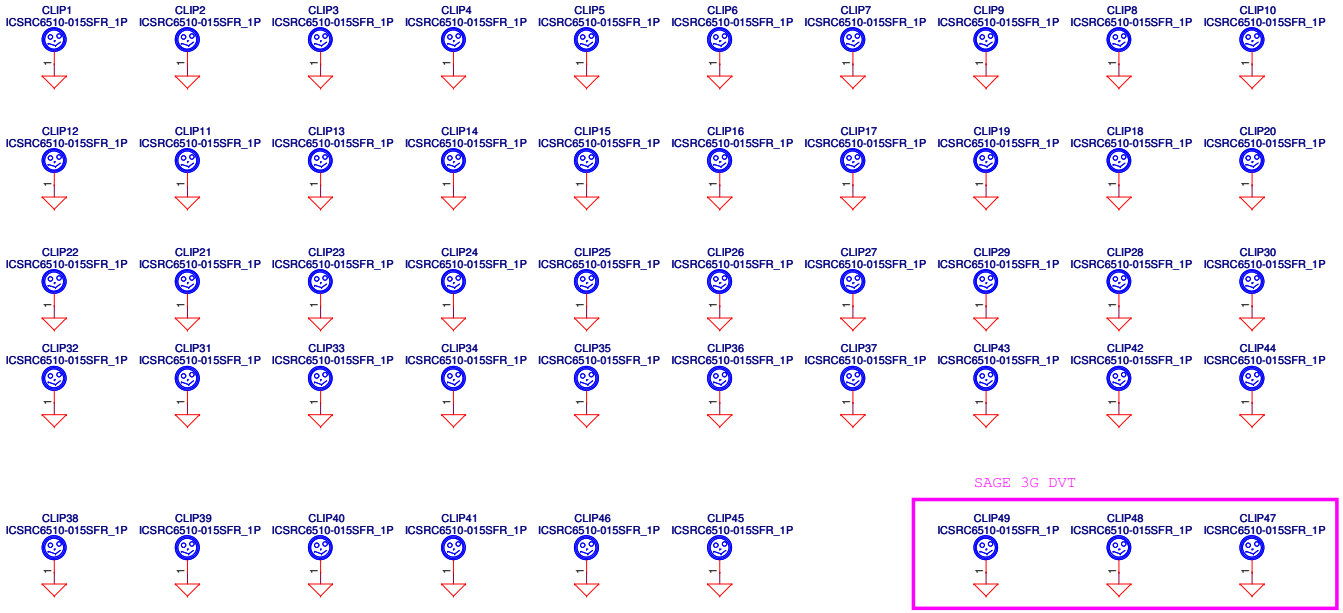


mSATA Stand-Off

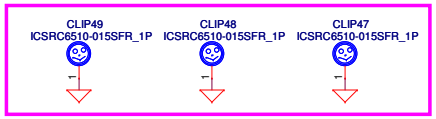
3G Stand-Off

螺孔





SAGE 3G DVT



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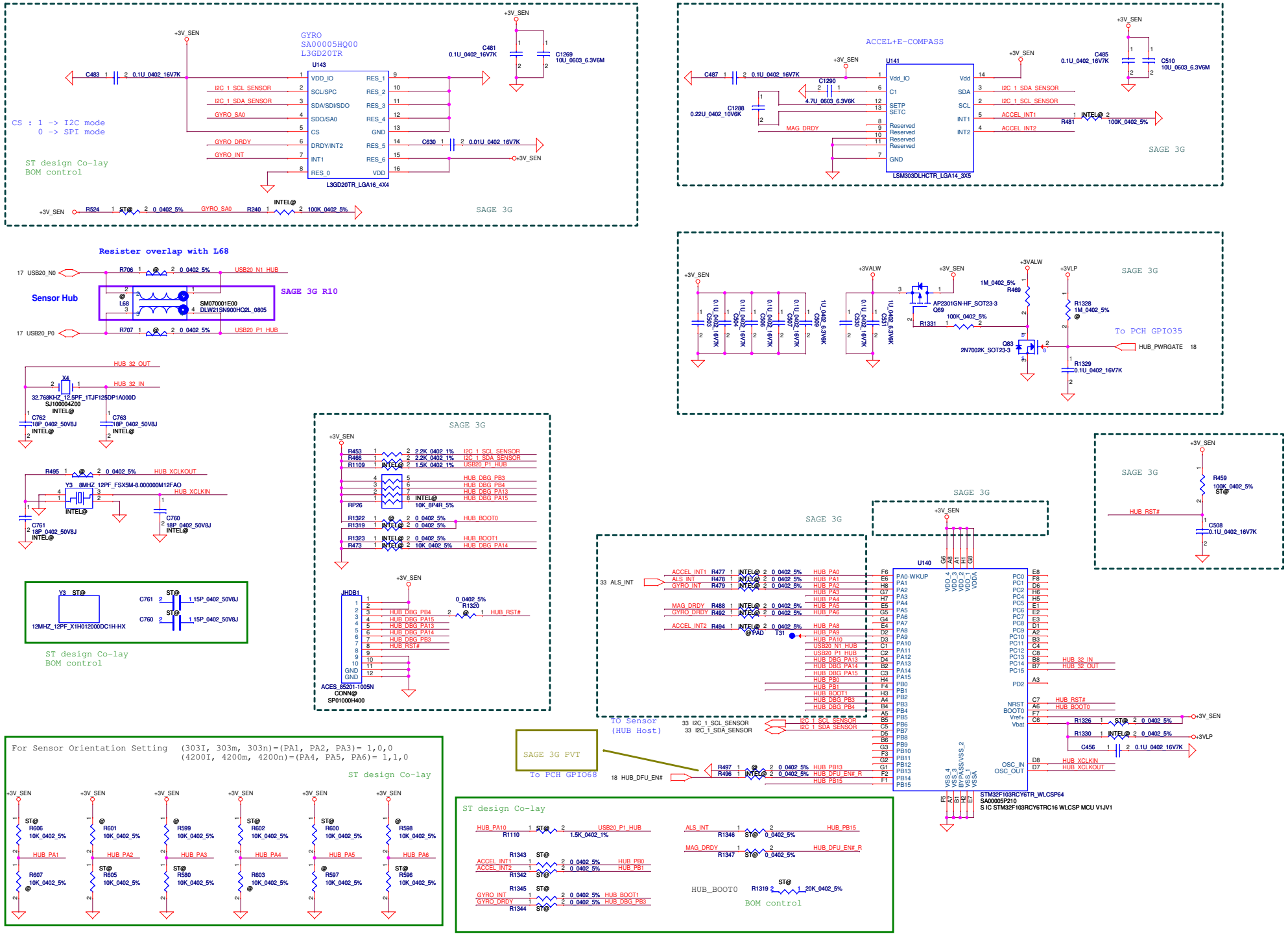
				Date: Wednesday, March 13, 2013; Sheet 29 of 52



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Compal Electronics, Inc.

Title: SENSOR

Size: C | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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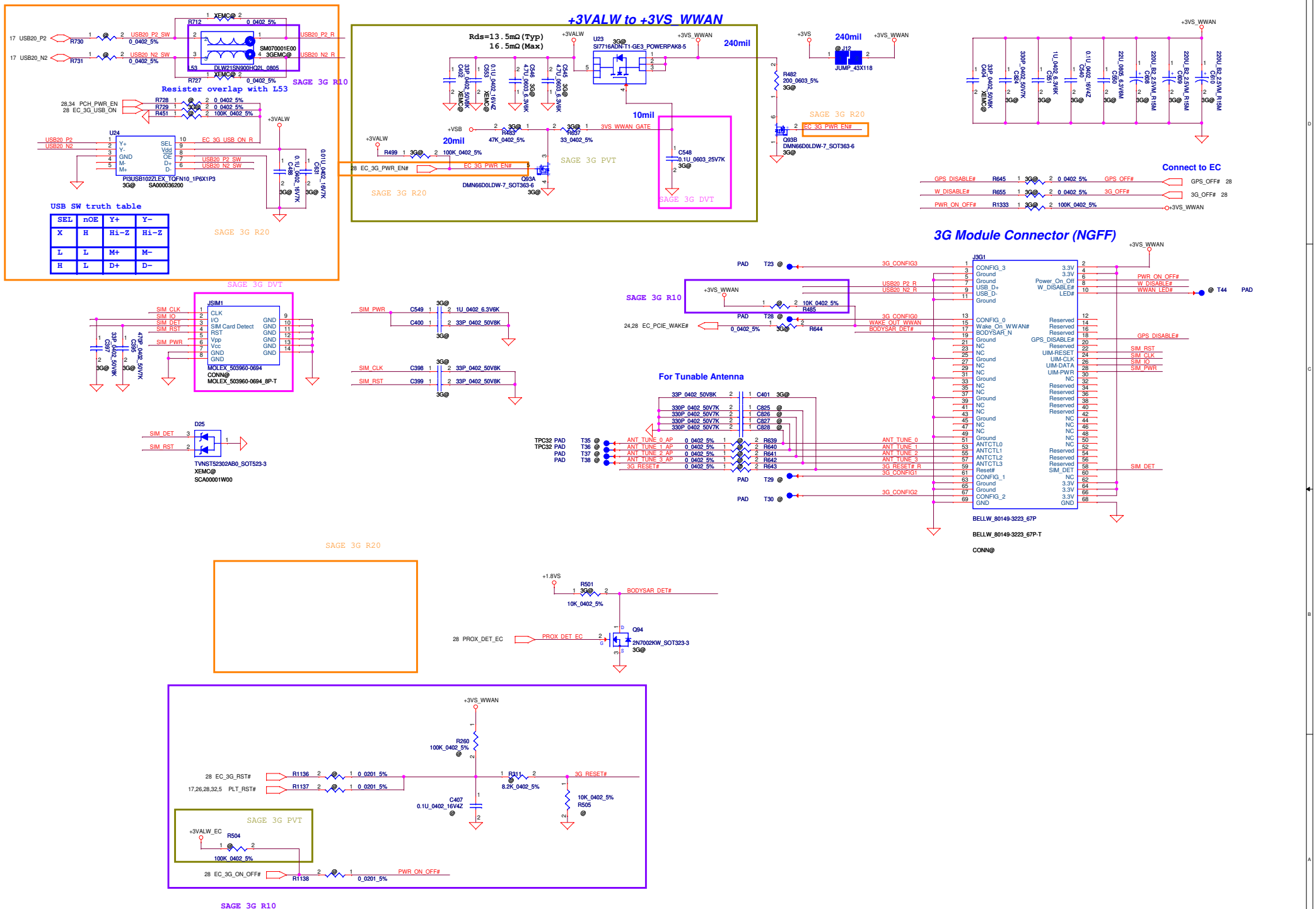

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Compal Electronics, Inc.

Title: 3G/GPS HUAWEI MU736

Size: C | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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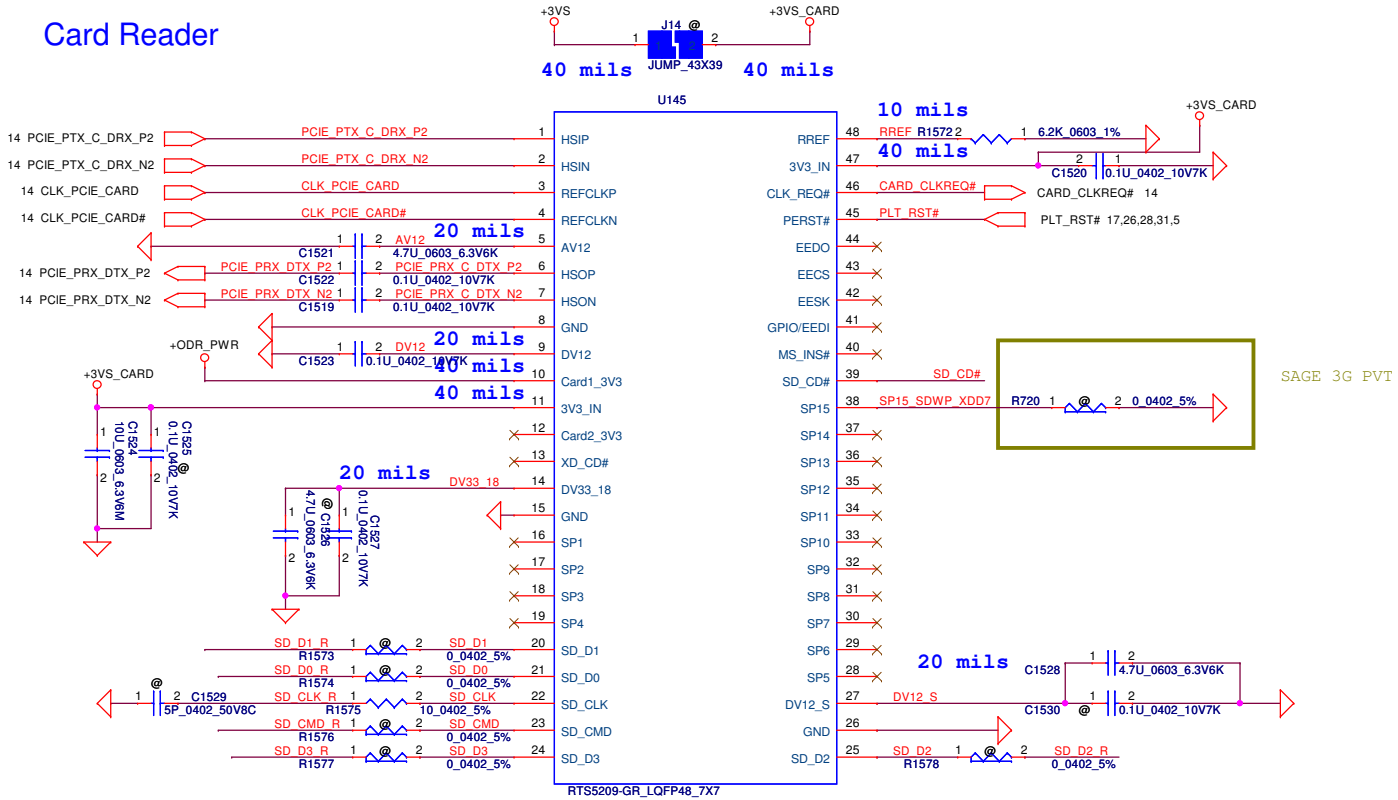
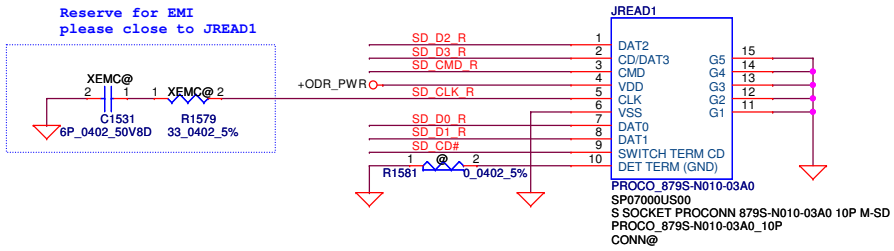
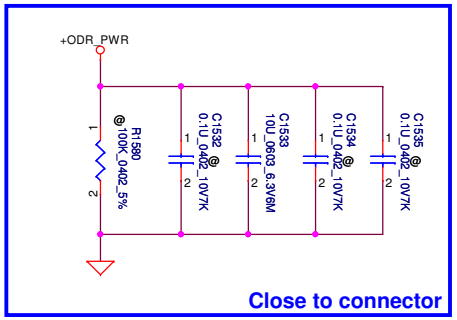
Card Reader







Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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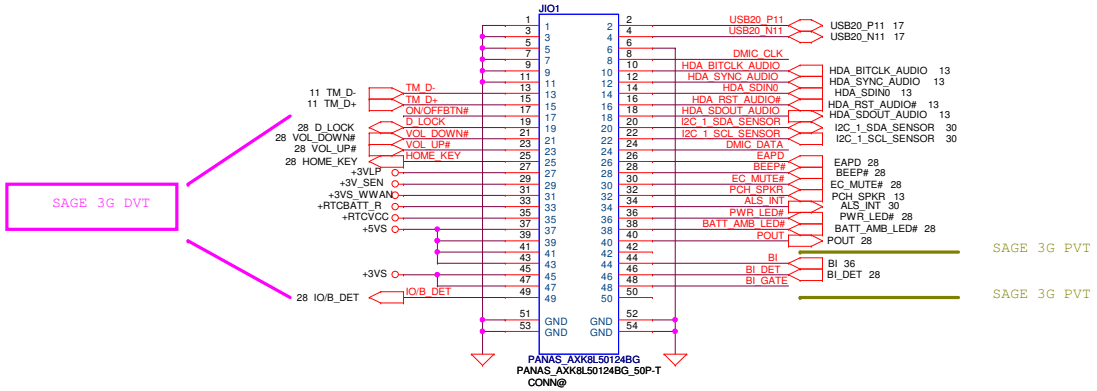
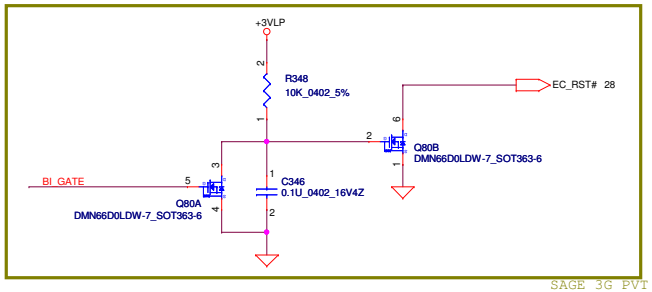
Compal Electronics, Inc.

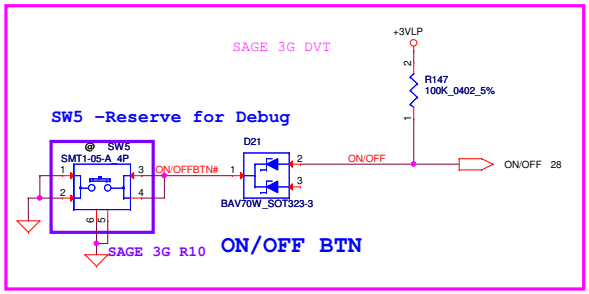
Title: Card Reader RTS5209

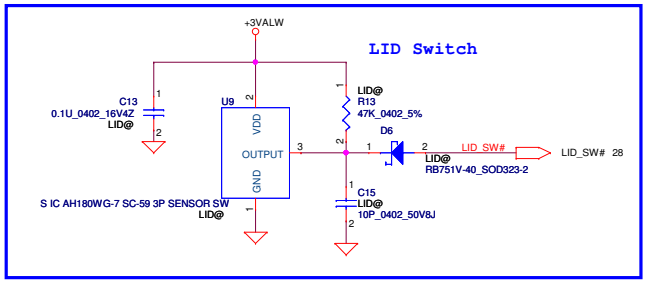
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

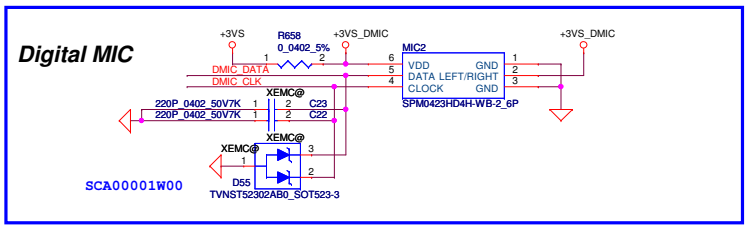
Date: Wednesday, March 13, 2013 | Sheet 32 of 52











Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

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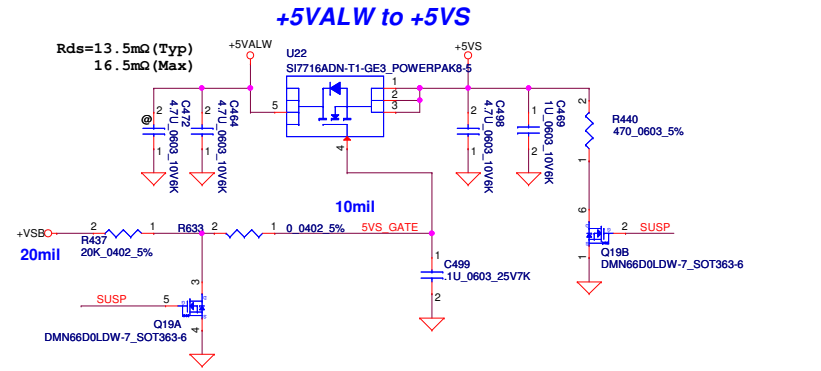
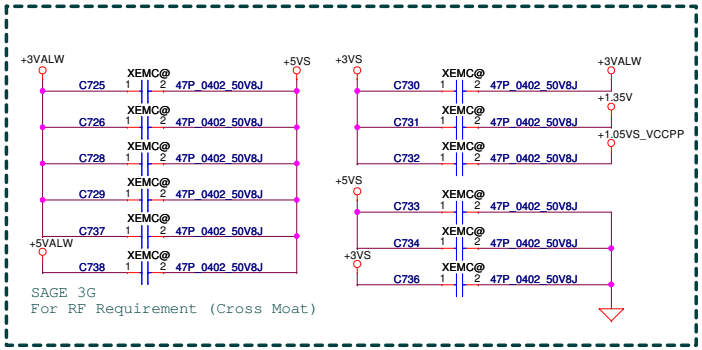
Compal Electronics, Inc.

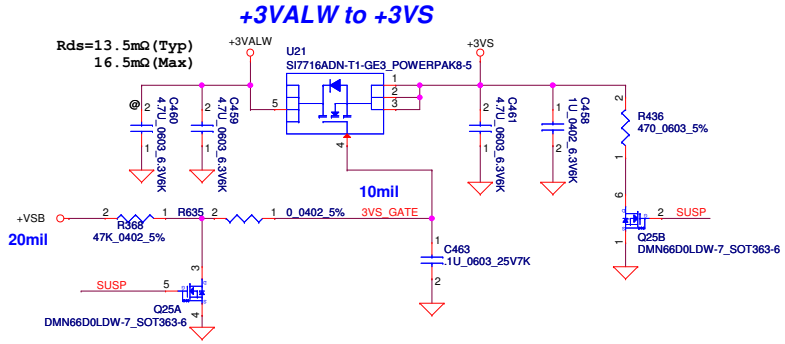
Title: IO Board (Audio / WIN / RST/ LED)

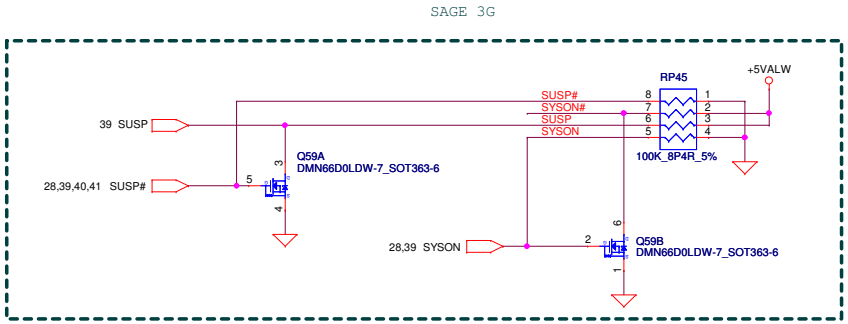
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

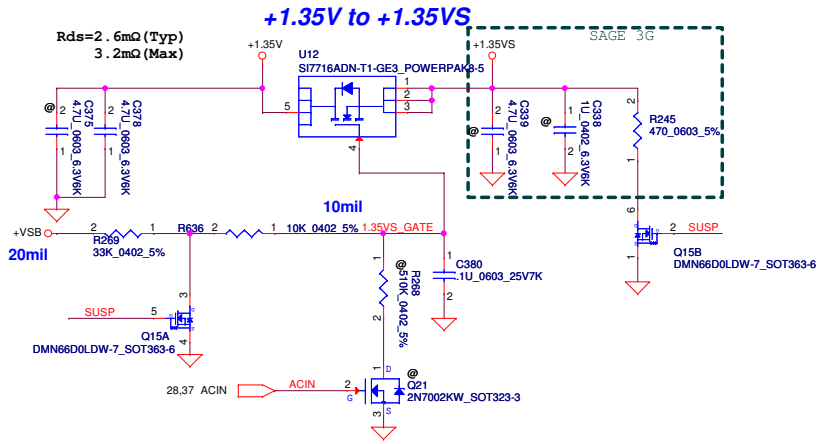
Date: Thursday, March 14, 2013 | Sheet 33 of 52

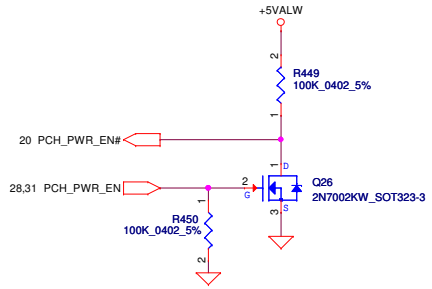


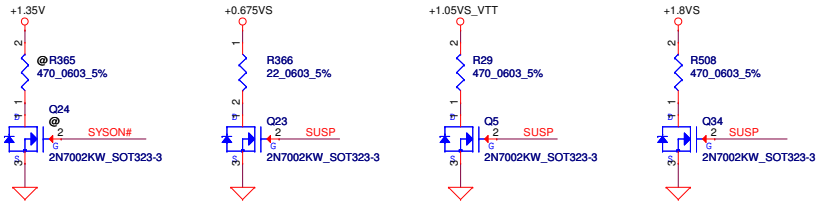












Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/06/02	Title: DC Interface
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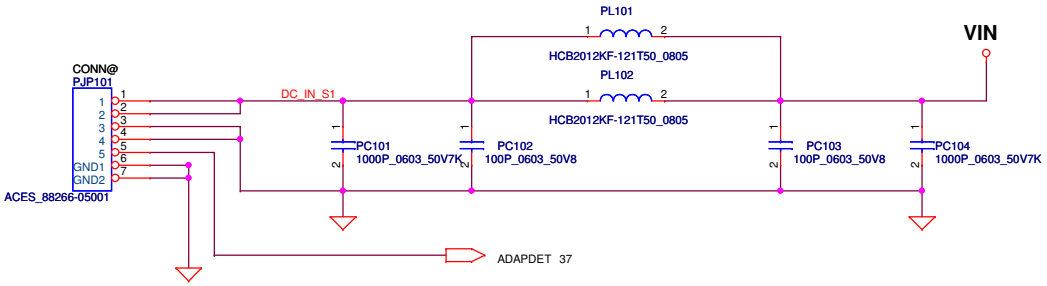
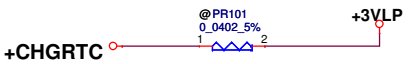
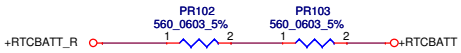
				Date: Wednesday, March 13, 2013; Sheet 34 of 52







Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title: DCIN/PRECHARGE
				Size: Custom; Document Number: SAGE 3G; Rev: 1.0
				Date: ; Sheet 35 of 52

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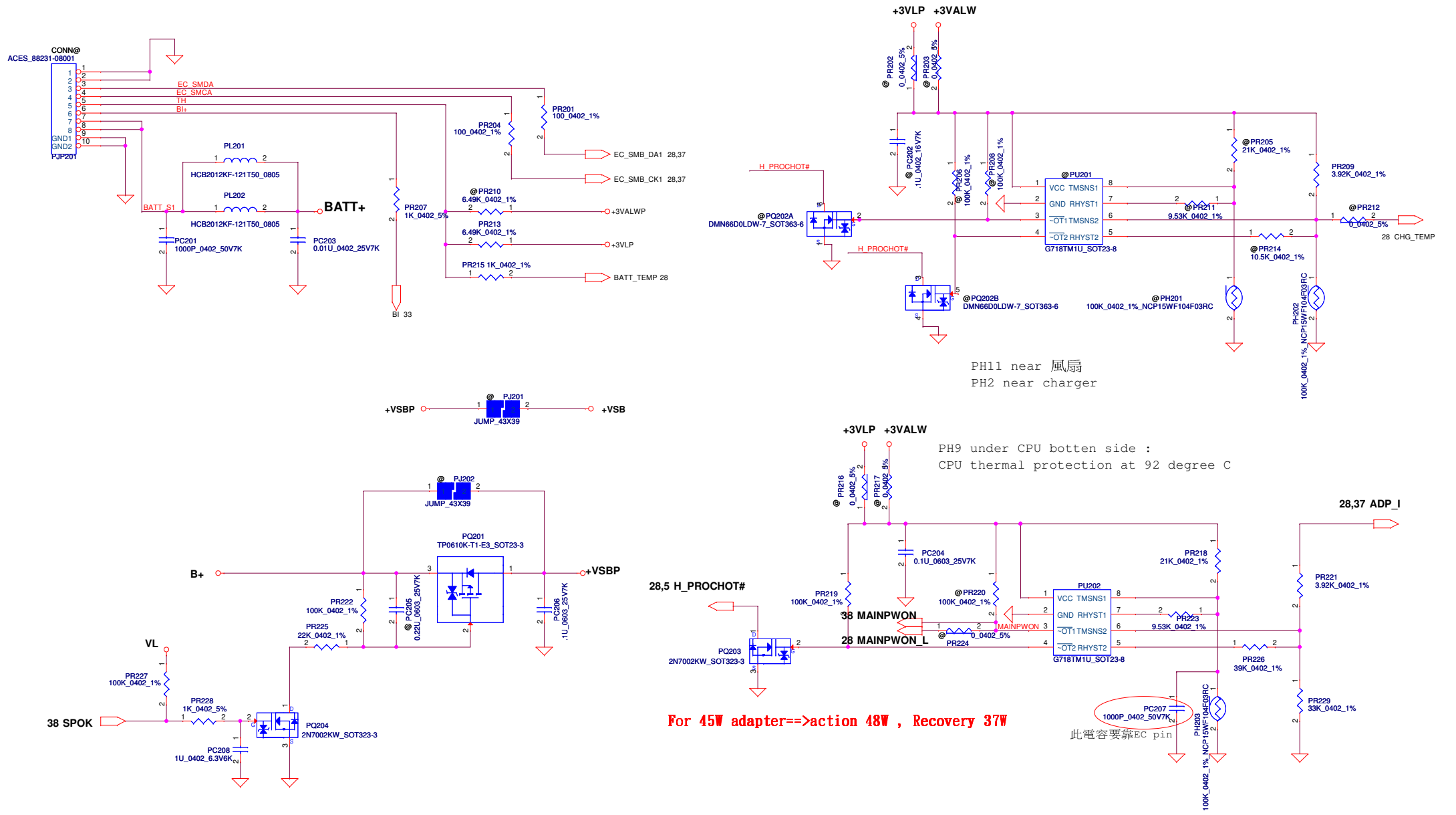

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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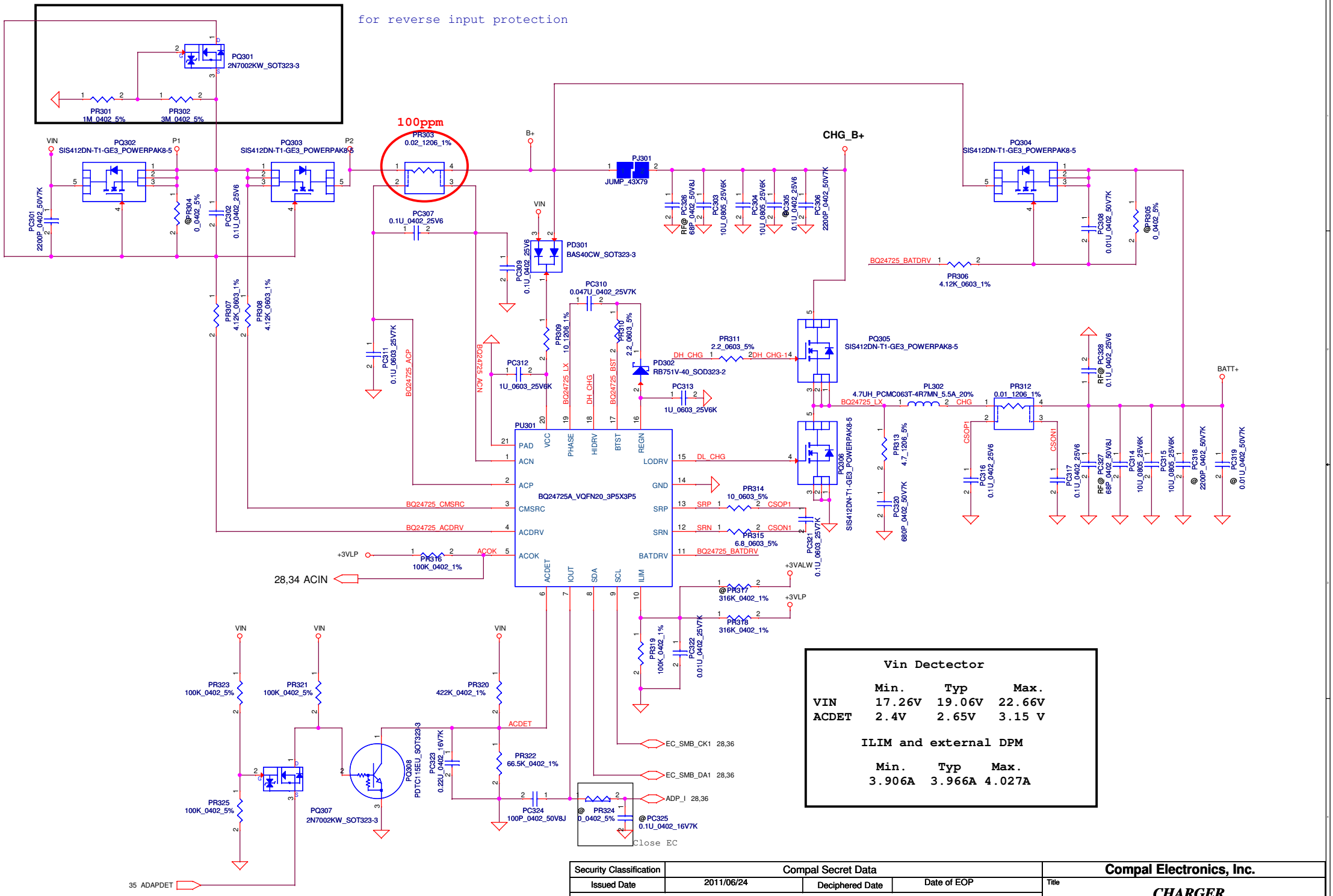
Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 36 of 52



Vin Dectector

	Min.	Typ	Max.
VIN	17.26V	19.06V	22.66V
ACDET	2.4V	2.65V	3.15 V

ILIM and external DPM

Min.	Typ	Max.
3.906A	3.966A	4.027A

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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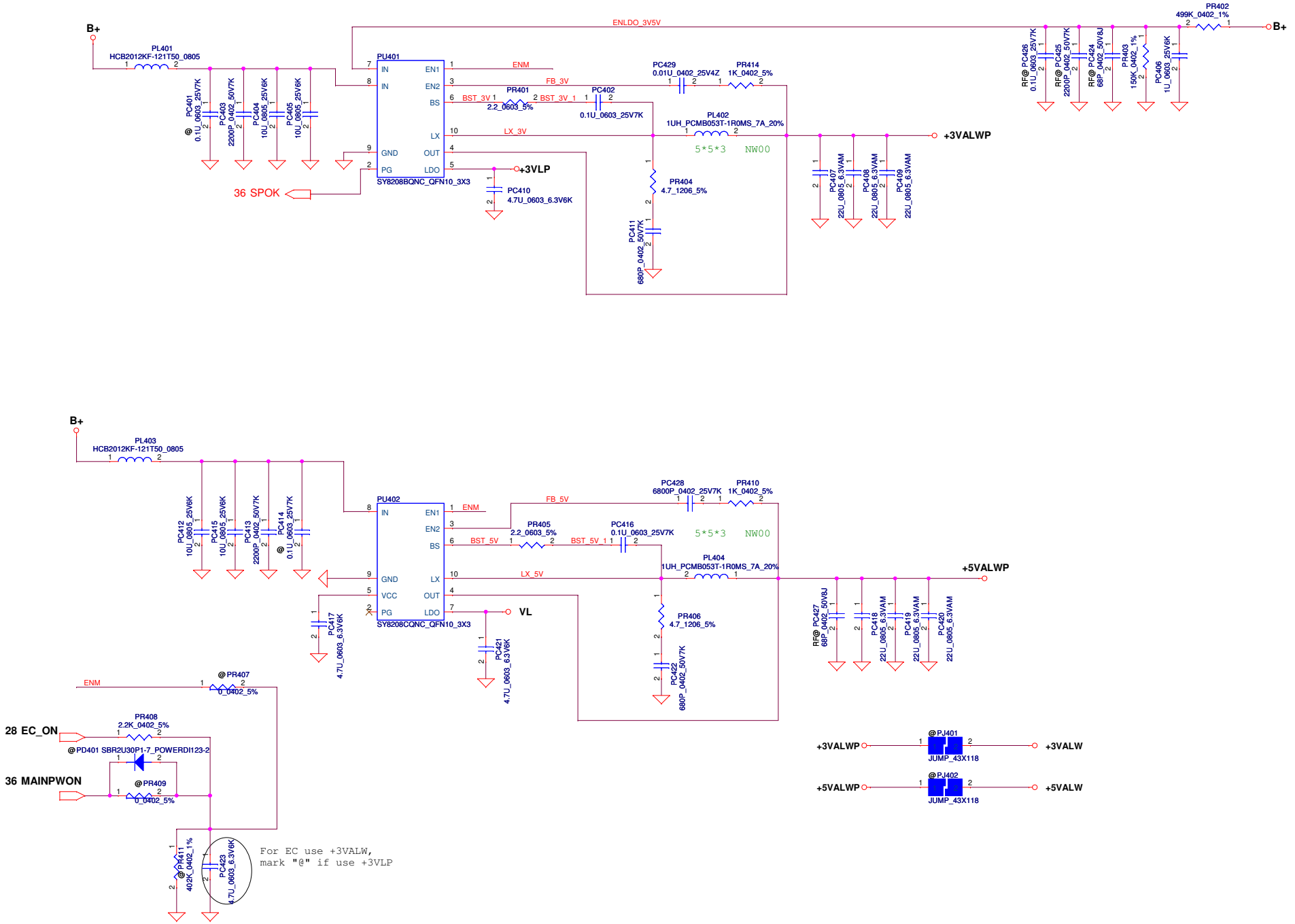
Compal Electronics, Inc.

Title: *CHARGER*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 37 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title: 3VALW/5VALW
				Size: Custom; Document Number: SAGE 3G; Rev: 1.0
				Date: ; Sheet 38 of 52

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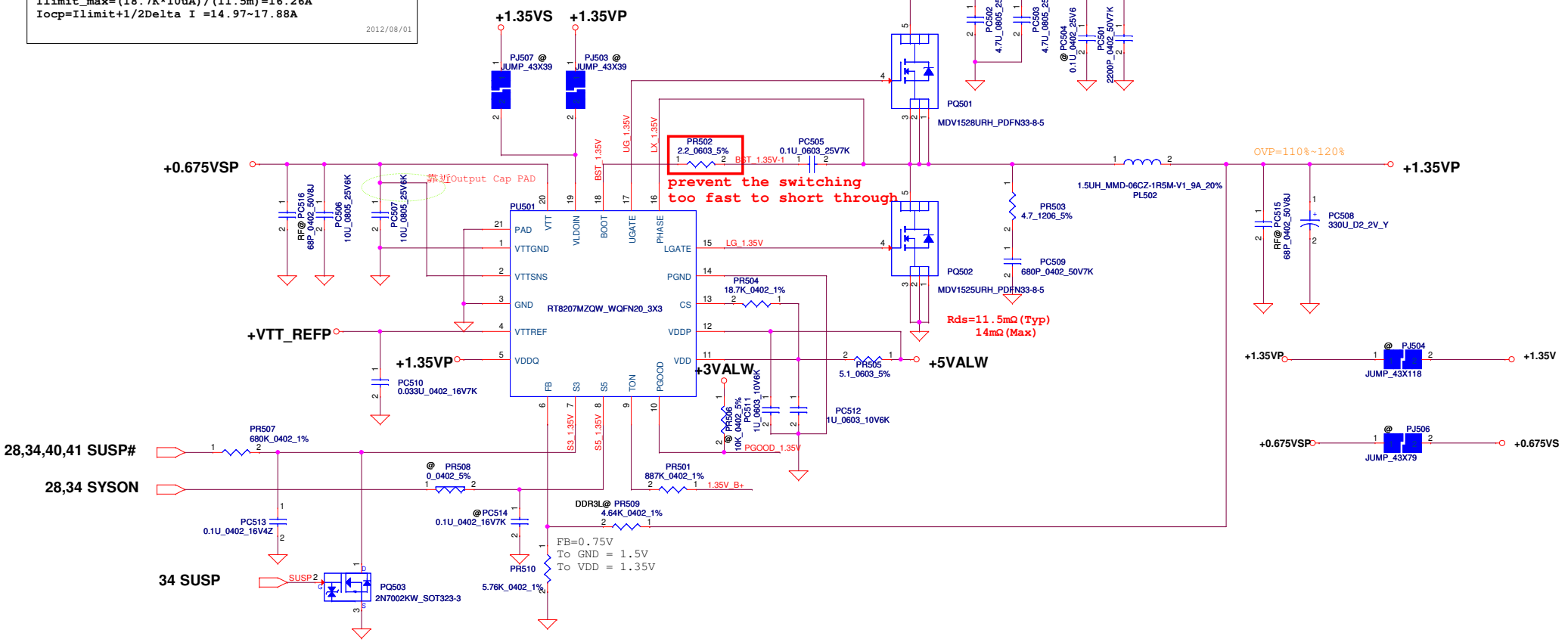
```
Ipeak=12.2A ; Imax=8.54A ;Iocp=14.64A
Delta I=3.23=>1/2Delta I=1.62A (F=285K Hz)
Rds(on)=14m ohm(max) ; Rds(on)=11.5m ohm(typical)
Ilimit_min=(18.7K*10uA)/(14m)=13.36A
Ilimit_max=(18.7K*10uA)/(11.5m)=16.26A
Iocp=Ilimit+1/2Delta I =14.97~17.88A
2012/08/01
```



STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title: 1.5VP/0.75VSP/1.8VSP

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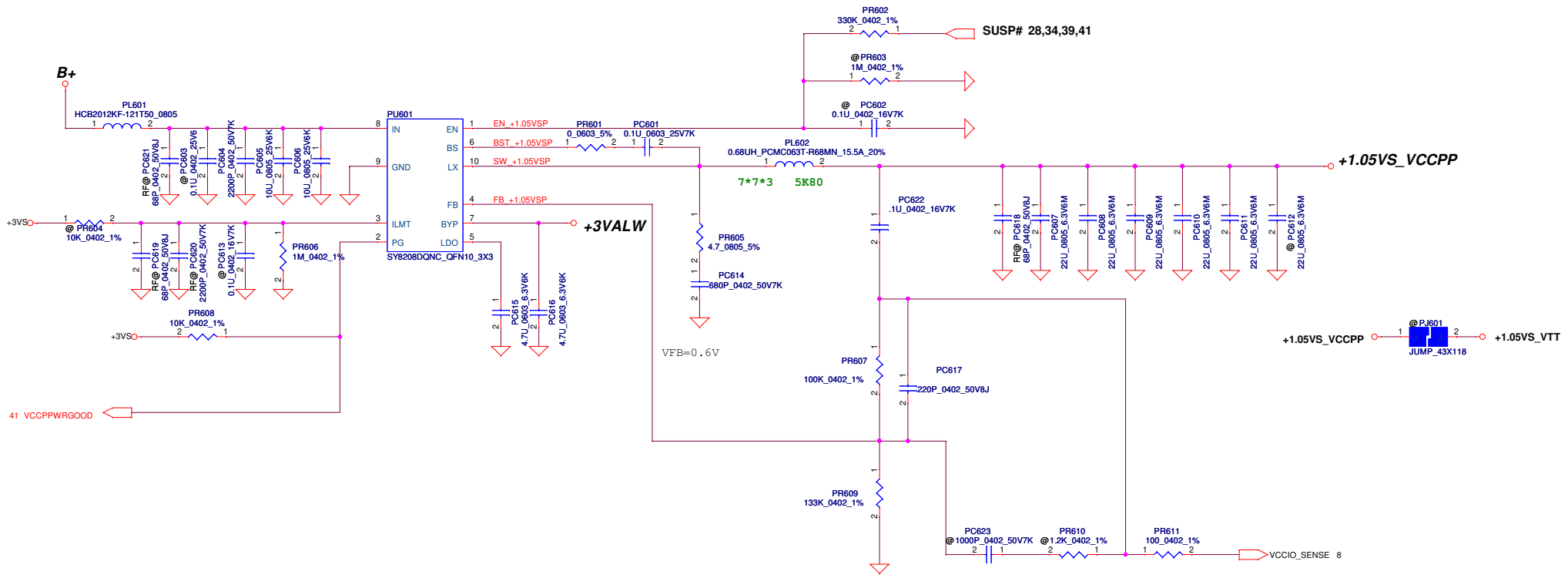
Size	Document Number	Rev
Custom	SAGE 3G	1.0

Date: Sheet 39 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title: 1.05VS_VTTP

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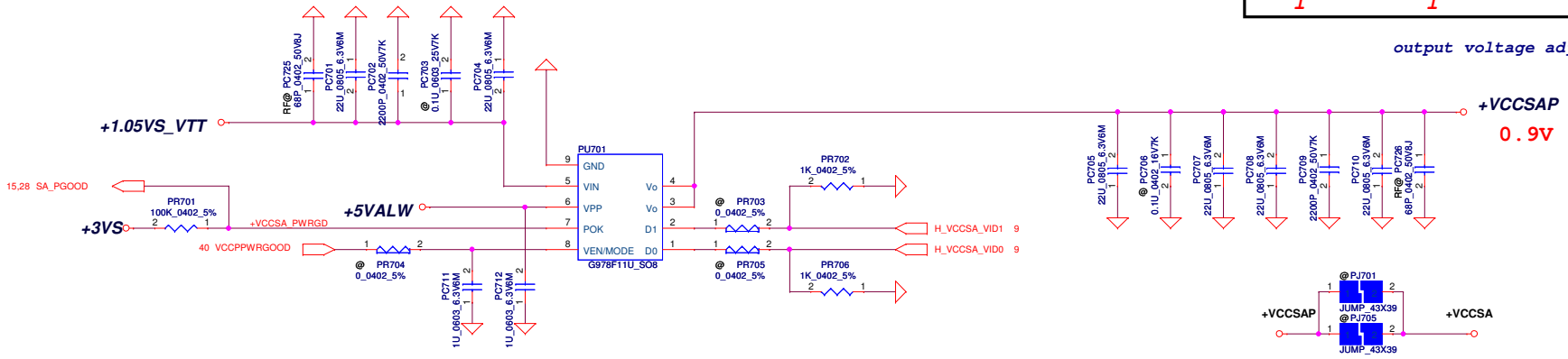
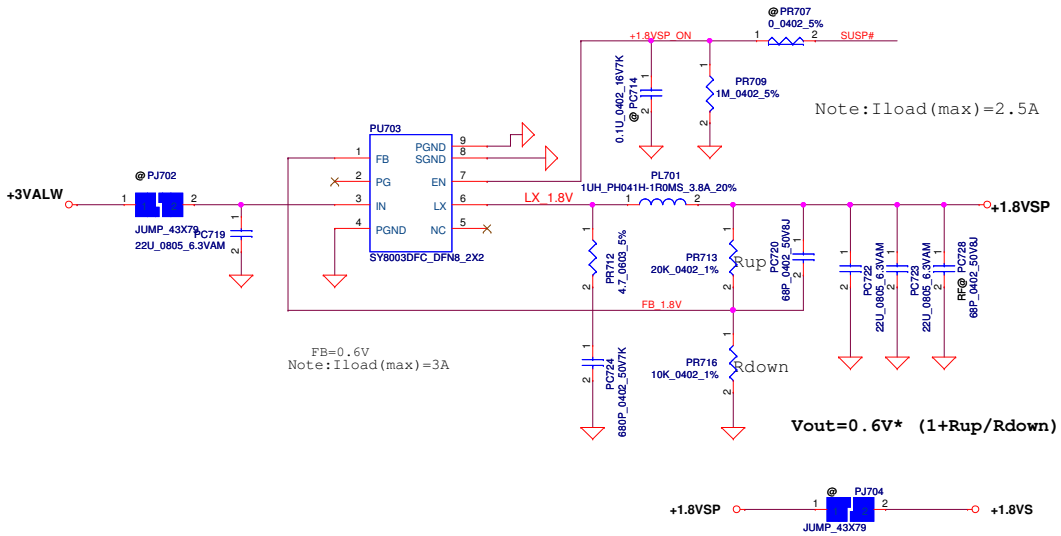
Size	Document Number	Rev
Custom	SAGE 3G	1.0

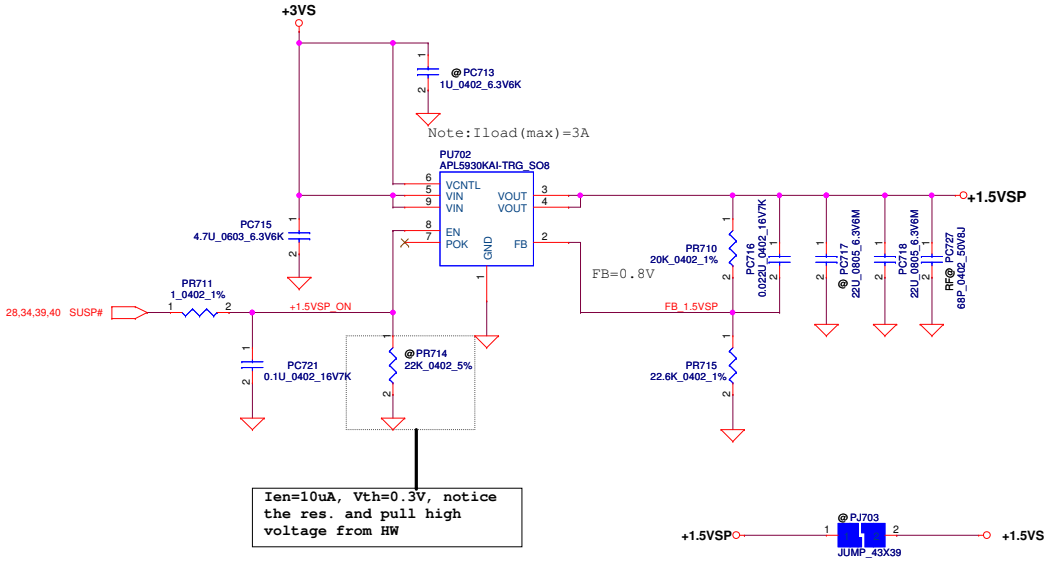
Date: | Sheet 40 of 52

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network







Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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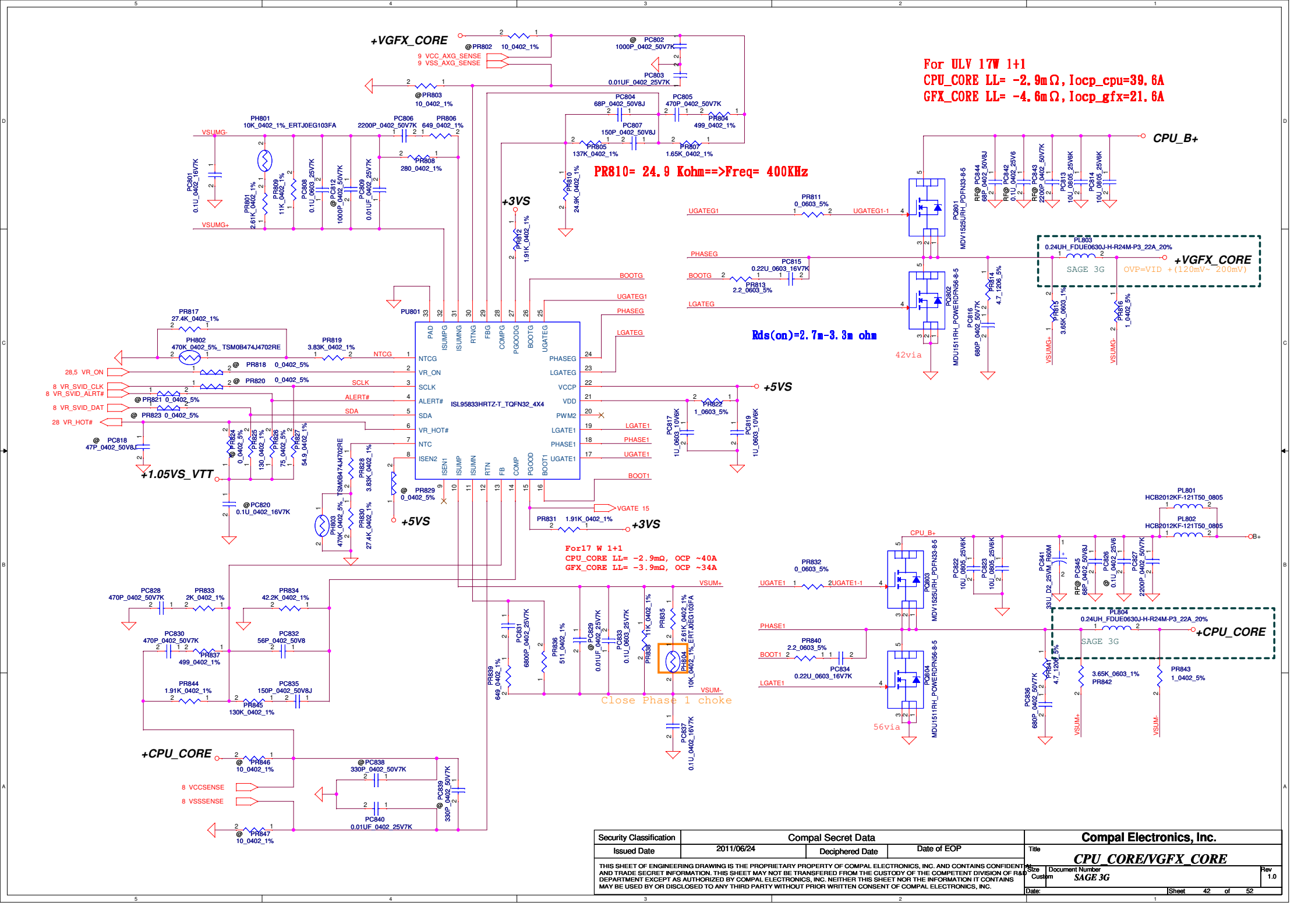
Compal Electronics, Inc.

Title: *VCC_SAP*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 41 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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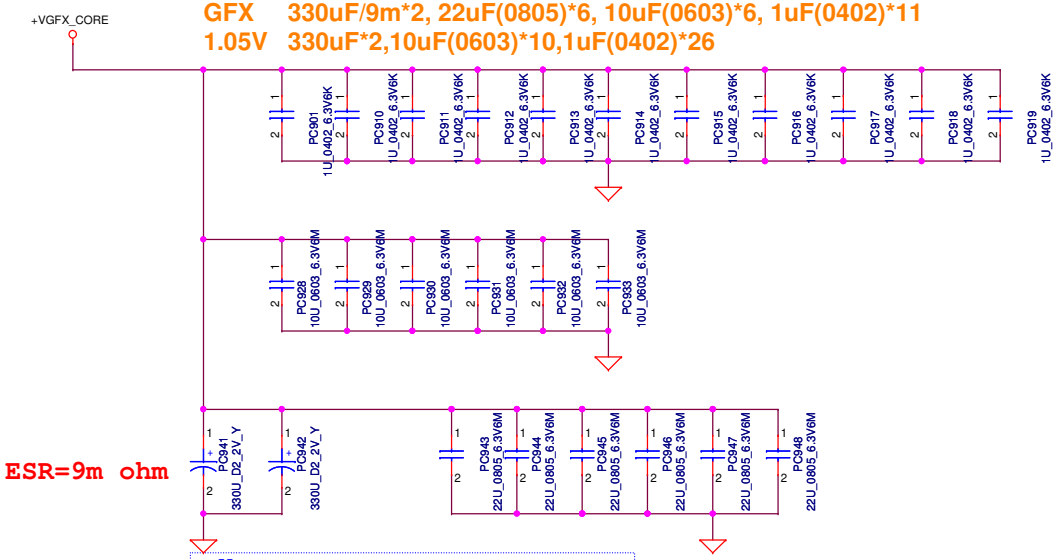
Compal Electronics, Inc.

Title: *CPU_CORE/VGFX_CORE*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

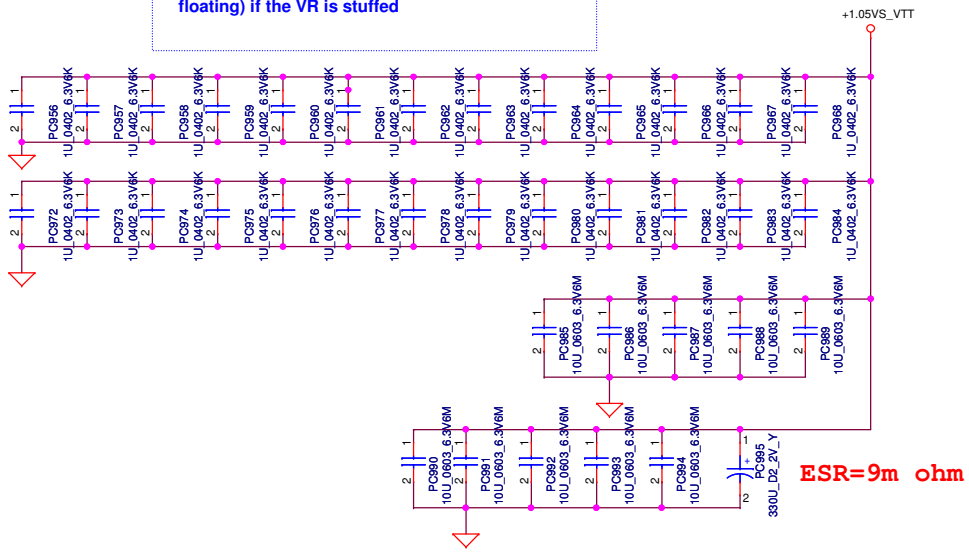
Date: | Sheet 42 of 52

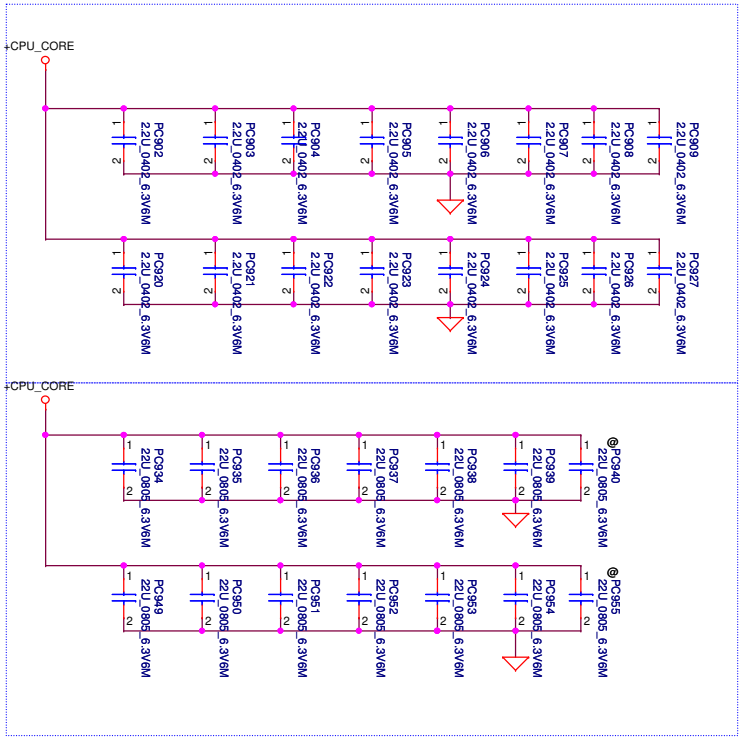
PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFX 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26

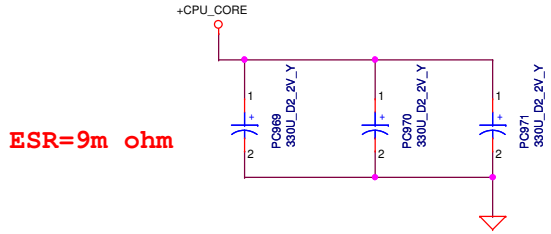


Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**







Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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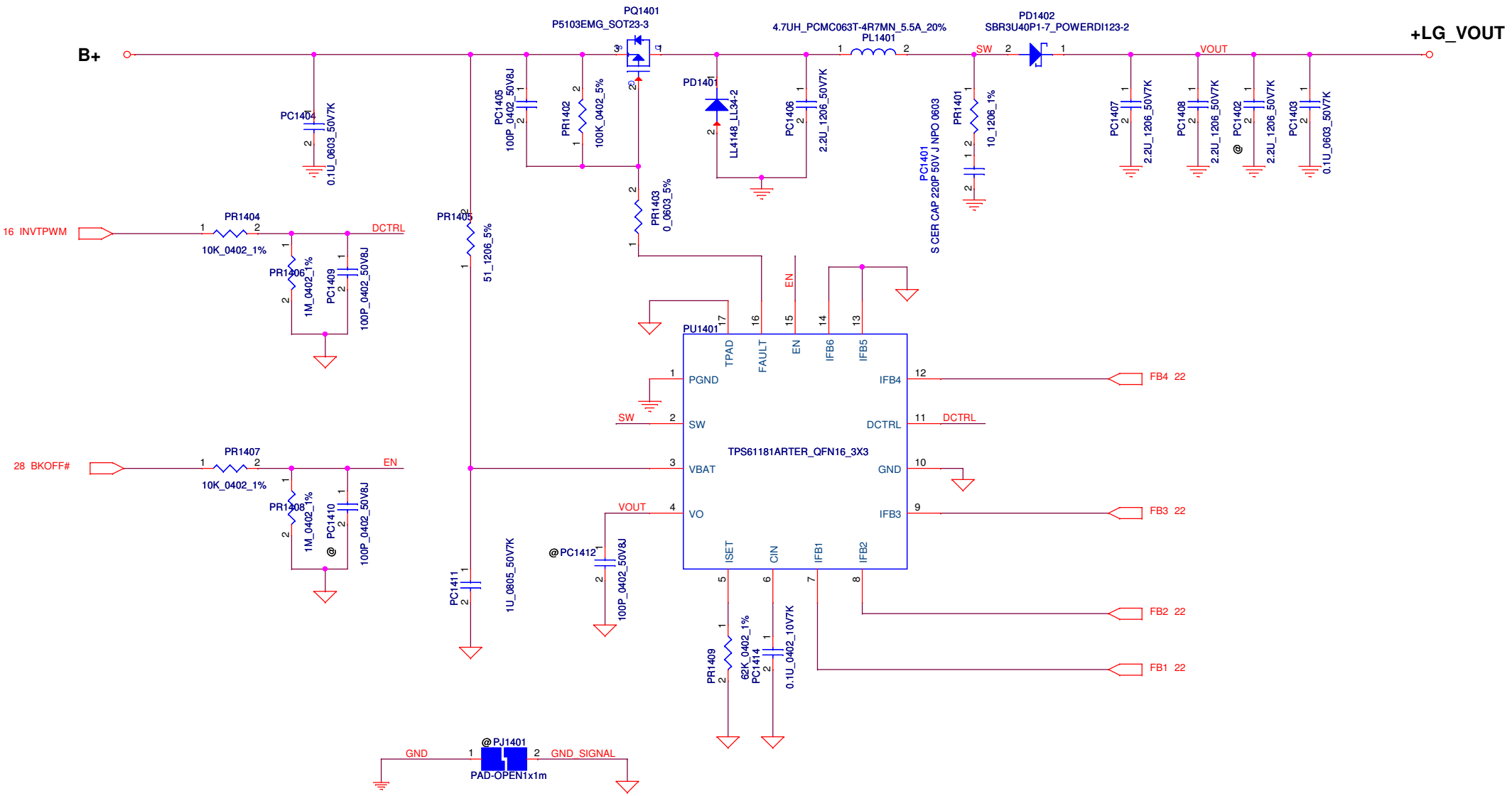
Compal Electronics, Inc.

Title: ***CPU_CORE_CAP***

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 43 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

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Compal Electronics, Inc.

Title: *LED Converter*

Size: Custom | Document Number: *SAGE 3G* | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 44 of 52

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of IC Application.	0.2	38	Add @PR410.@PR414 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC429 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC428 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR412.@PR413.PR415 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/13	DVT
2	Design Change.	Design Change of IC Application.	0.2	44	Delete PC1413.	2012/12/13	DVT
3	Add Adapter Detection Circuit.	Design Change of DC Jack Application.	0.2	35 37	Add PR325 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PR321.PR323 to SD028100380(S RES 1/16W 100K +-5% 0402) Add PQ307 to SB201440000(S TR PDTA144EU PNP SOT323) Add PQ308 to SB301150200(S TR PDTC115EU NPN SOT323)	2012/12/13	DVT
4	Design Change.	Design Change of IC Application.	0.2	42	Change PC831 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC832 to SE071560J80(S CER CAP 56P 50V J NPO 0402)	2012/12/24	DVT
5	Change Component Part Number.	Factory lack of material.	0.2	44	Change PL1401 to SH000006J80 (S COIL 4.7UH +-20% PCMC063T-4R7MN 5.5A)	2012/12/24	DVT
6	Change Component Part Number.	Factory lack of material.	0.2	42	Change PC841 to SGA00007I00 (S POLY C 33U 25V M D2 ESR60M TQC H1.9)	2012/12/26	DVT
7	Change Component Part Number.	X1 Code.	0.2	44	Change PD1402 to SCS00005Y00 (S SCH DIO SBR3U40P1-7 POWERDI123-2)	2012/12/26	DVT
8	Design Change.	Design Change of IC Application.	0.3	38	Delete PR412.PR413.PR415.	2012/01/29	PVT
9	Design Change.	Design Change of IC Application.	0.3	38	Change @PR410.@PR414.@PC428.@PC429 to PR410.PR414.PC428.PC429.	2012/01/29	PVT
10	Design Change.	Design Change of IC Application.	0.3	38	Change PC428 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC429 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402)	2013/02/22	PVT
11	Design Change.	Design Change of Adapter Detection.	0.4	37	Change PQ307 to SB000009Q80(S TR 2N7002KW 1N SOT323-3) Add PR325 to SD028100380(S RES 1/16W 100K +-5% 0402)	2013/02/23	Pre MP

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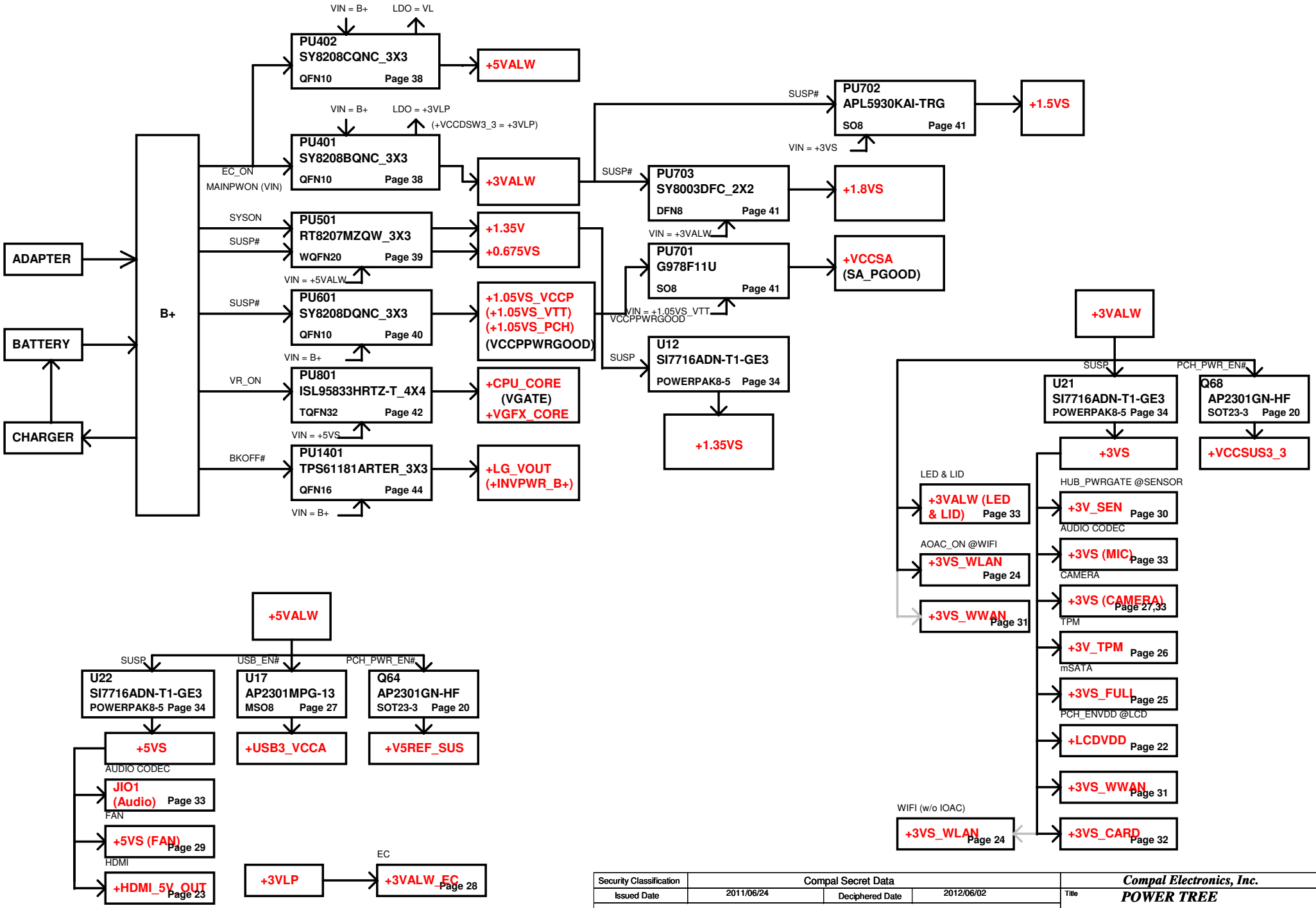
Size: Custom	Document Number: EG51_HX M/B LA-9491P Schematics		Rev: 1.0
Date:	Sheet 45 of 52		



Security Classification	Compal Secret Data		
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Title: **POWER TREE**

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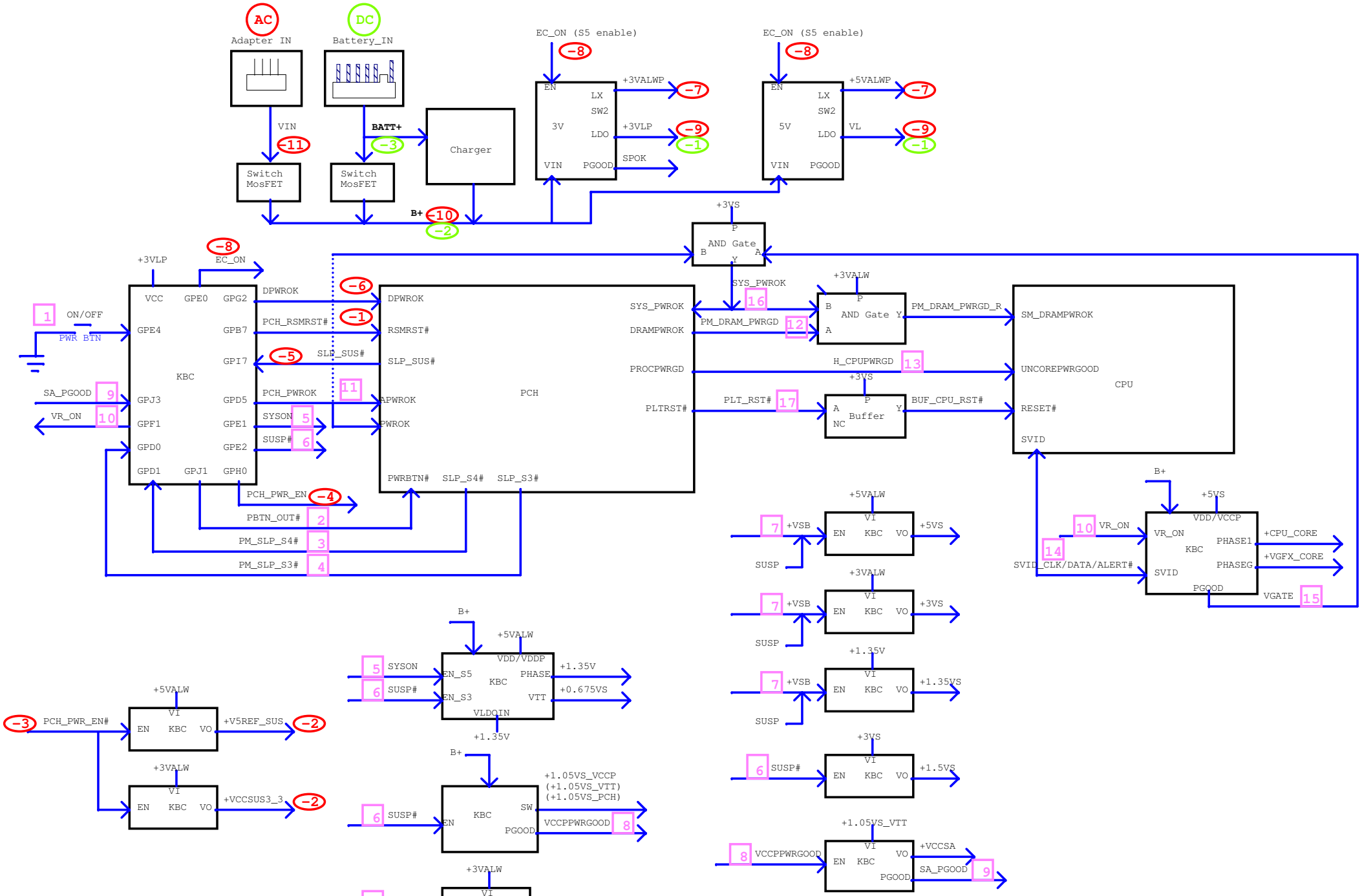
Date: Wednesday, March 13, 2013 | Sheet 46 of 52



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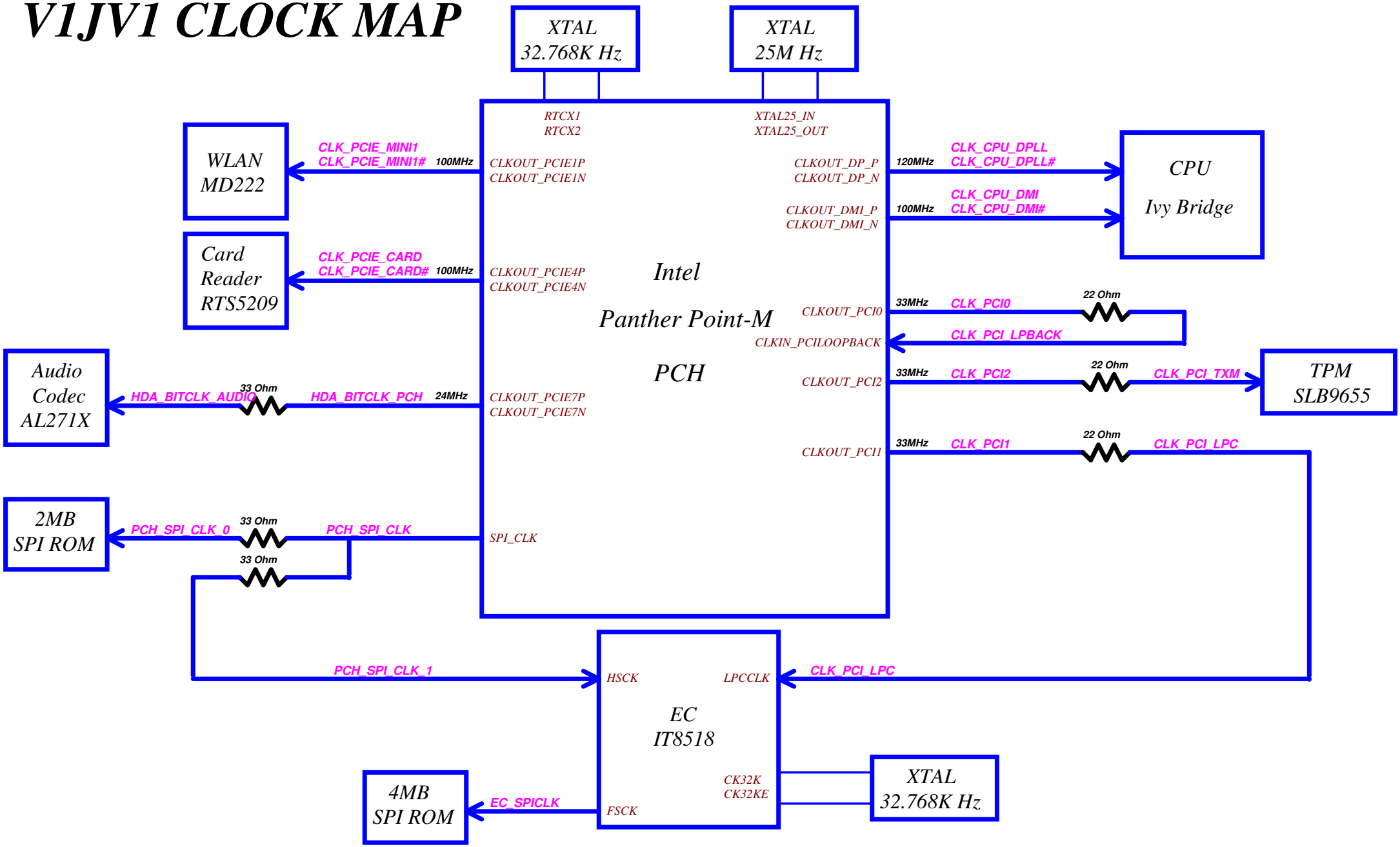
V1JV1 CLOCK MAP



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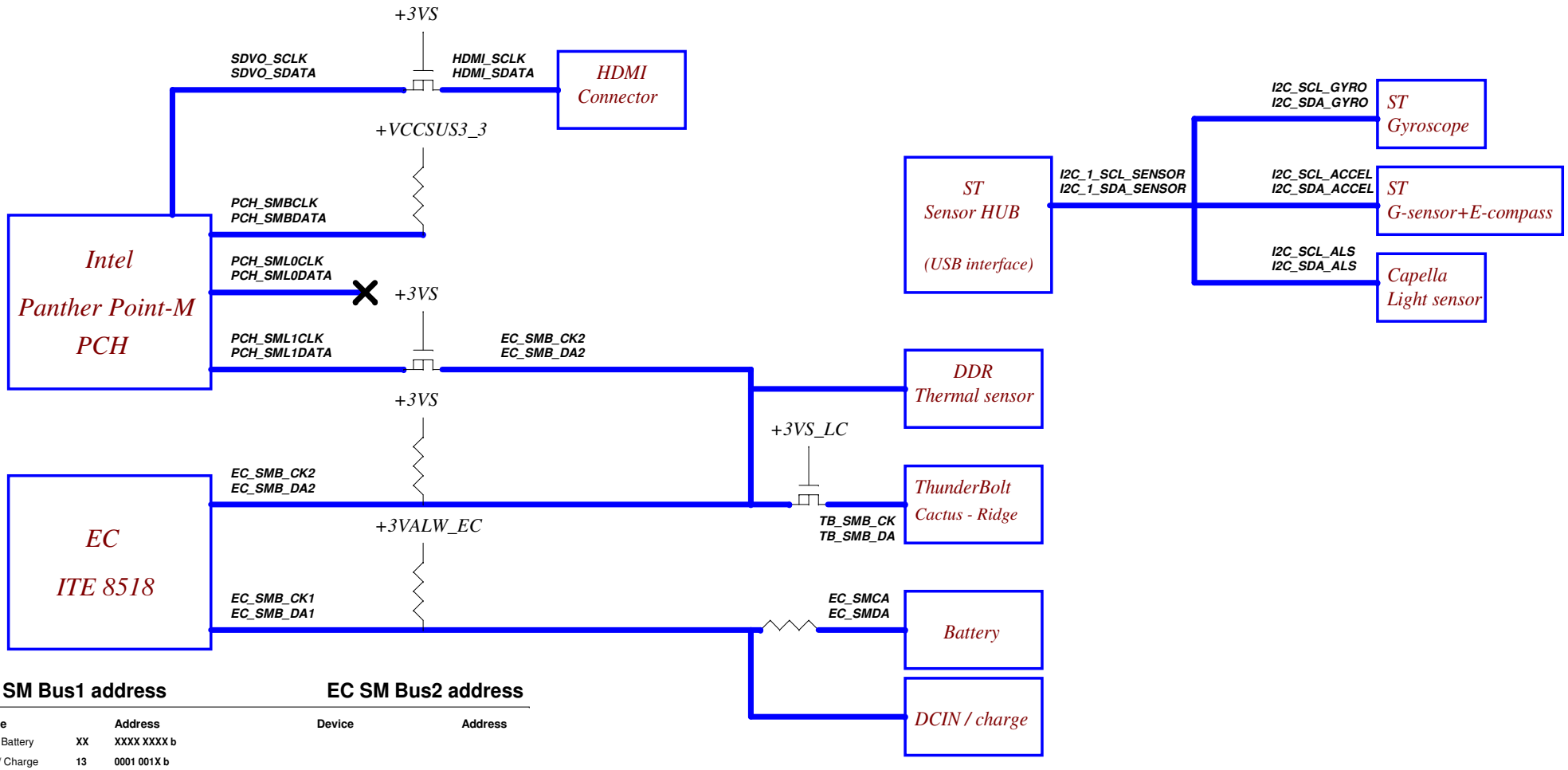
Title: **CLOCK MAP**

Size: Custom | Document Number: **V1JB1 M/B LA-A041P Schematic** | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 48 of 52

SMBUS Block Diagram



EC SM Bus1 address

Device		Address
Smart Battery	XX	XXXX XXXX b
DCIN / Charge	13	0001 001X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device		Address
ST sensor HUB	XX	XXXX XXXX b

PCH SM Bus address(Link 1)

Device		Address
DDR Thermal sensor	99	1001 101X b
Thunderbolt	29	0010 100X b(CIO P1)
	2B	0010 101X b(CIO P2)
	2D	0010 110X b(CIO P3)
	2F	0010 111X b(CIO P4)

Sensor HUB SM Bus address

Device		Address
Gyroscope	D1	1101 000X b
	D3	1101 001X b
E-compass + G sensor	33	0011 001X b
ALS sensor	21	0010 000X b

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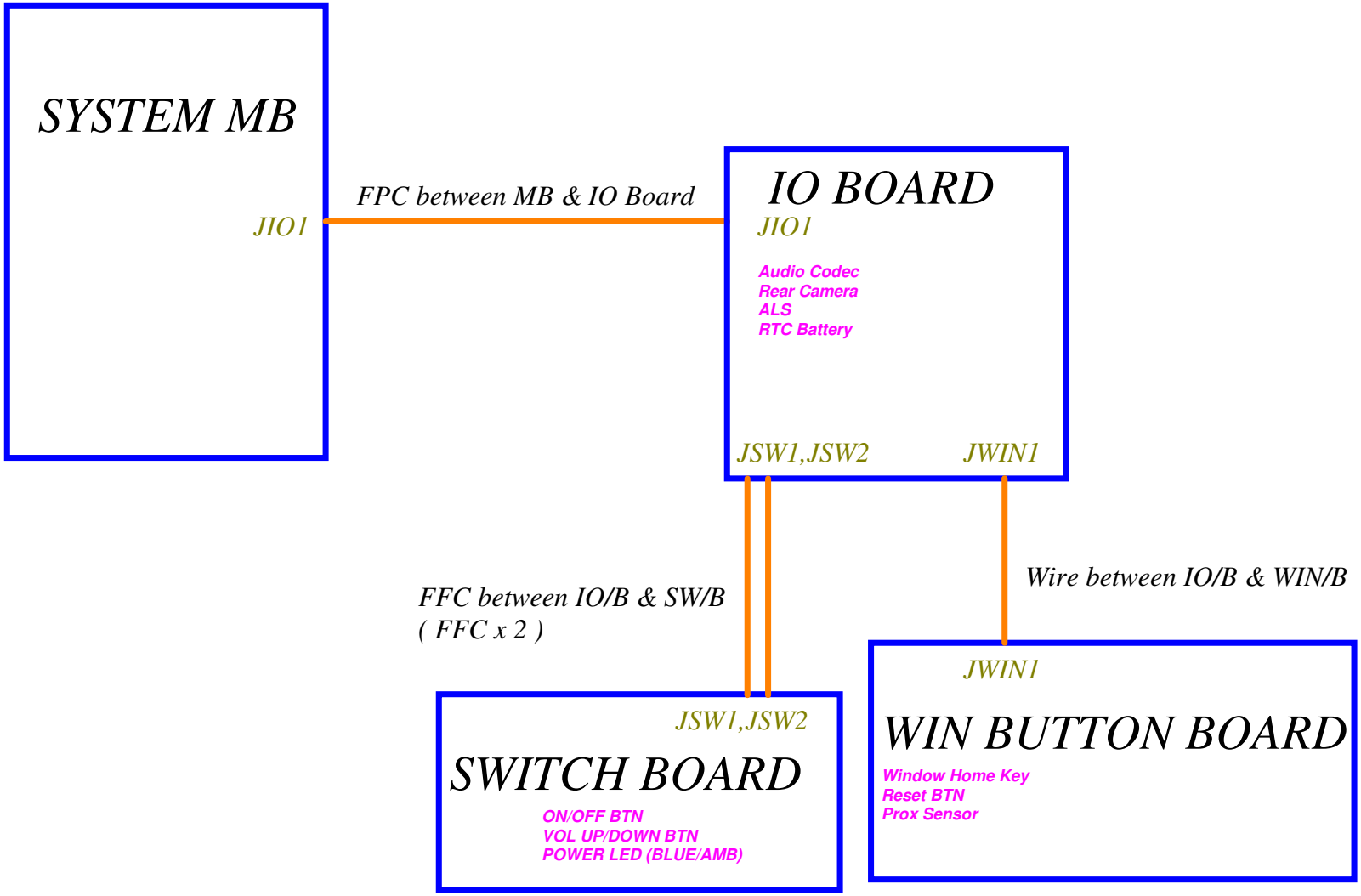
Title: SMBUS Block Diagrams

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 49 of 52

V1JB1 SYSTEM Diagram



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Title: **SYSTEM MAP**

Size: Custom | Document Number: **V1JB1 M/B LA-A041P Schematic** | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 50 of 52

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

DVT

01. Add net " IO/B_DET" to detect IO/B
    - Avoid thermal sensor wrong action by remote mode cause system auto shut down
02. Add 3 clips at ext USB area (RF requirement)
03. Move D_LOCK pull up resistor from IO/B to M/B side (Reserve function)
04. Move ON/OFFBTN# circuit from IO/B to M/B side(Sub/B just SW BTN only)
05. Change R960 to 8.2k ohm (Board ID update)
06. Change RP19, RP20 package to R_0402*8 (HDMI signal fine tune requirement)
07. Change C451,C450 BOM structure to XEMC@
08. Delete R78 for Layout components reduce
09. Change SIM Card Connecotor as MOLEX_503960-0694 (ME requirement)
10. Change C548 to 0 ohm resistor (3G power from +3VS, not +3VALW)
11. Base on crystal vender suggest, change C756, C757 to 15pF, C744 & C745 to 12pF

PVT

01. Add test point at CPU pin B22, A19, B14, A11, B10, B6 (DFB requirement)
02. Modify EC_RST# circuit for Reset Button (Dual Mosfet)
03. Add ODT1, CKE1, CS1# net to DDR for 8Gb DRAMs
04. Remove EC_ON, MAINPWON net from JIO1 (un-used net)
05. Change R960 to 18k ohm (Board ID update)
06. Change R185, R186, R720 to short pad
07. Change R637 to 33 ohm (3G PWR SEQ)
08. Reserve 0 ohm resistor to GND for sensor PB13 as ST suggestion
09. Remove Screw "H18" (ME outline modify)
10. Unstuff 3G power switch circuit (un-used -> 3G power source tie to +3VS directly)
11. Add 3G@ BOM option for WiFi only sku
12. Change R499, R503, R504 from 10k to 100k for DS5 power consumption

R10

01. Change RP43 part number from SD302220A00(22 ohm) to SD309220A80 (22 ohm) for Green BOM request
02. Unstuff component of reserve circuit (un-used function) ->
    R503, Q7 (SIM_DET# to EC), R504 (EC_3G_ON_OFF#), R260, R311, R505, C407 (3G Ext. RST#)
03. Change R960 to 33k ohm (Board ID update)
04. Unstuff R485 to avoid leakage to wlan module (3G provide power when S3/DS3)
05. Unstuff SW5 (for test phase only, MP remove)
06. Update PCB PN to R10
07. As source request (cancel vender-Cheng Hann), change below parts~
    1. Change L23 PN from SM01000AX00 to SM01000EP00
    2. Change L3, L4, L36, L38, L39, L40, L53, L68 PN from SM070001600 to SM070001E00
    3. Change L52 PN from SM070001310 to SM070001E00

R20

01. Add USB switch to 3G USB signals for avoid DS3 leakage
02. Delete Q7, R503 (un-used component)
03. Rename EC_SIM_DET# to EC_3G_PWR_EN# (correct net name to meet actual function)
04. Change EC GPD7 (U53.M12) to EC_3G_USB_ON for 3G USB switch
05. Change R960 to 56k ohm (Board ID update)
06. Update PCB PN to R20

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Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Tuesday, March 26, 2013	Sheet 51 of 52		

PCB

ZZZ1

LA-A041P MB Rev0: DAA0006P000
LA-A041P MB Rev1: DAA0006P010
LA-A041P MB Rev2: DAA0006P020

LA-A041P REV2
DAA0006P020

WLAN/BT Module

U1

LIONMD222@

PK29S004B00
S_W/L_MOD WCBN3501A W/BT MD222 ABO!

WCBN3501A W/BT MD222

CPU

UCPU1

I33217@

S IC AV8063801058401 SR0N9 L1 1.8G ABO!
SA00005L5C0

AV8063801058401 SR0N9 L1 1.8G ABO!

UCPU1

I53317@

S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0

AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1

I32365M@

S IC AV8062701313000 SR0U3 J1 1.4G ABO!
SA00005UH40

AV8062701313000 SR0U3 J1 1.4G ABO!

UCPU1

I33227@

S IC AV8063801119500 SR0XF L1 1.9G ABO!
SA00006D990

AV8063801119500 SR0XF L1 1.9G ABO!

UCPU1

I53337@

S IC AV8063801129900 SR0XL L1 1.8G ABO!
SA00006D860

AV8063801129900 SR0XL L1 1.8G ABO!

UCPU1

I32375M@

S IC AV8062701313100 SR0U4 J1 1.5G ABO!
SA00006ED50

AV8062701313100 SR0U4 J1 1.5G ABO!

SAGE 3G

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Option Component

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Thursday, March 14, 2013 | Sheet 52 of 52