ZZZ1 PCB 14"DAZ@

ZZZ2 LA-7011P 14"DA@

ZZZ3 LS-7011P 14"DA@

ZZZ4 LS-7013P 14"DA@

ZZZ5 LS-7014P 14"DA@

Compal Confidential

Schematics Document

PAW10

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Title: Cover Sheet

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 1 of 41

Compal confidential
File Name :

For 14"	For 15"
LS-7011P 4PIN PWR/B	LS-7012P 8PIN PWR/B
LS7013P Audio/B	LS7013P Audio/B
LS7014P Touch/B	LS7014P Touch/B

Clock Generator
SLG8SP556VTR
page16

Mobile Penryn
uPGA-478 CPU
page4,5,6

H_A#(3..35)
H_D#(0..63)
FSB
667/800MHz

CRT Connector page21

LVDS Connector page22

Intel Cantiga GMCH
GM45
uFCBGA 1329
page 7,8,9,10,11,12,13

Dual Channel
DDR3-667/800(1.5V)

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3 page 14,15
up to 4G

DMI *4
C-Link

Intel ICH9-M
page 17,18,19,20

AZALIA

Audio Codec
CONEXTAN
CX20671 page26

2Channel Speaker page26

Analog MIC_Int page26

Wire Less Mini card Slot 1 page23

6*PCI-E BUS

14*USB2.0

6*SATA serial

SPI ROM BIOS

LPC BUS

CMOS Camera page22

BlueTooth CONN page30

USB CONN X1(Right) page29

USB PORT X1(Left) page29

USB PORT X1(Left) page29

Audio Jack SB CONN
HP X 1+
MIC_Ext X1 page30
Card Reader RTS5139

AR8151/8152
10/100/Giga LAN
page24

RJ45 CONN page25

EC
ENE KB926 E0
page27

Int.KBD page32

SPI ROM BIOS page28

Touch Pad page32

SATA HDD CONN page28

SATA ODD CONN page32

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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Therml
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT(ESATA)
8	
9	
10	
11	
12	
13	

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Title: MB Notes List

Size: B | Document Number: LA7011P | Rev: 1.0

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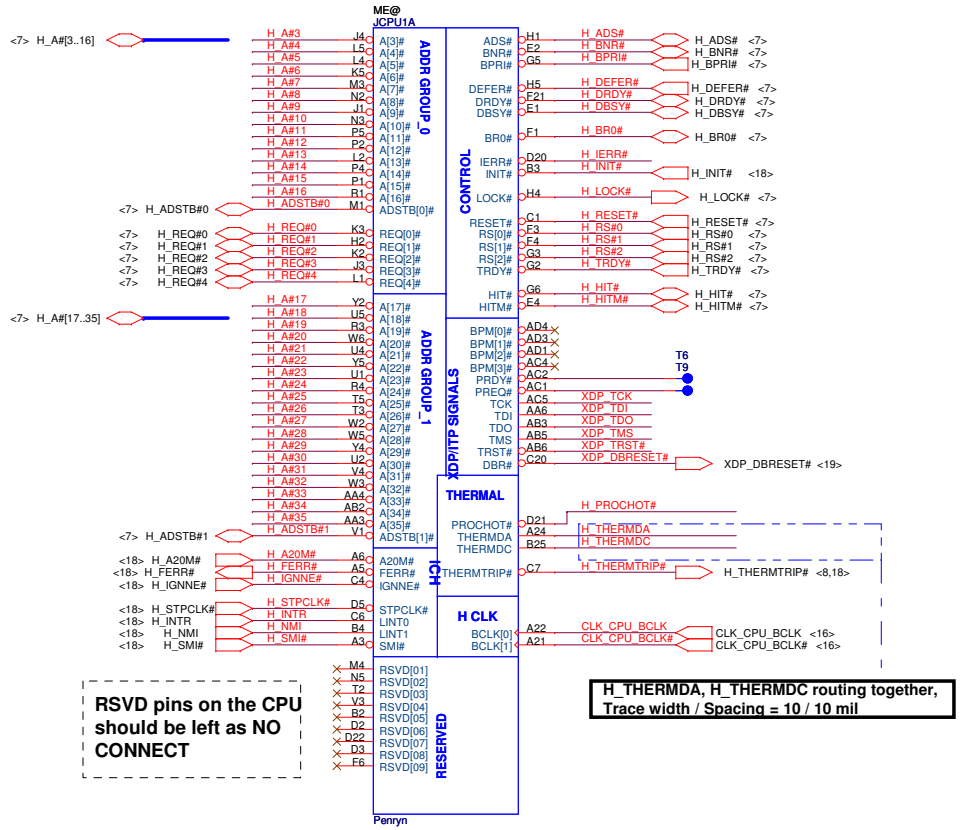
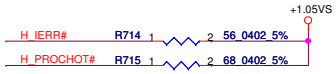
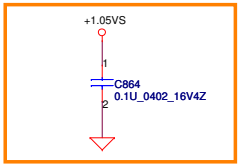
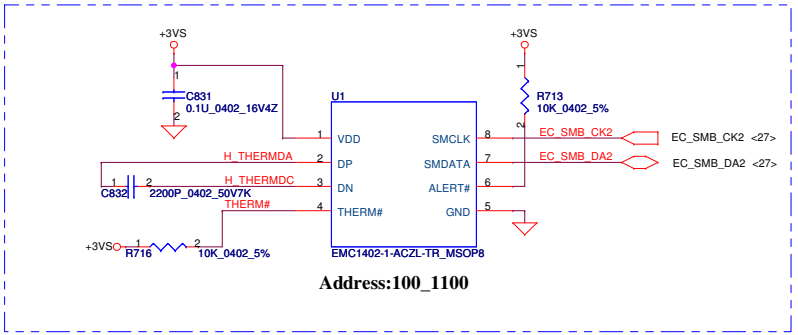




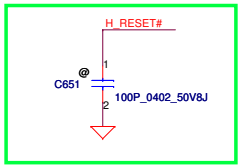
PVT ESD solution.
Please close to R715





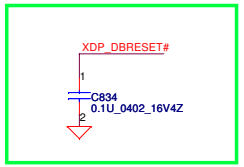
Address:100_1100

10/01 Add for reduce noise



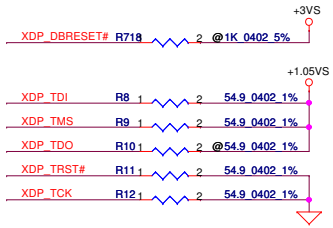
Place closely pin C1

09/16 Add C834 For ESD



Place closely pin C20

XDP Reserve for debug , Please close to CPU side



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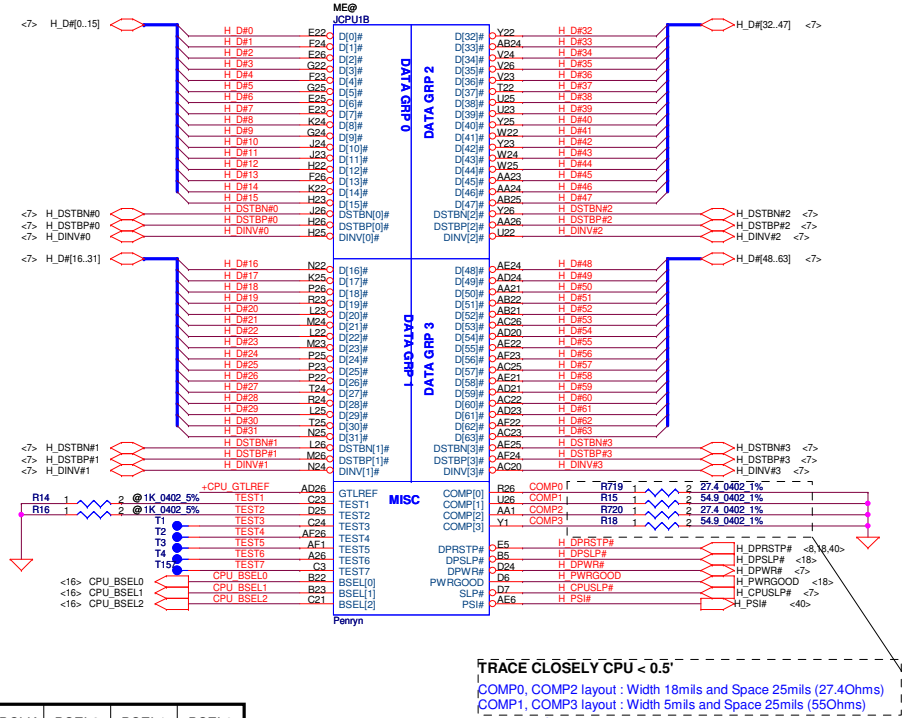
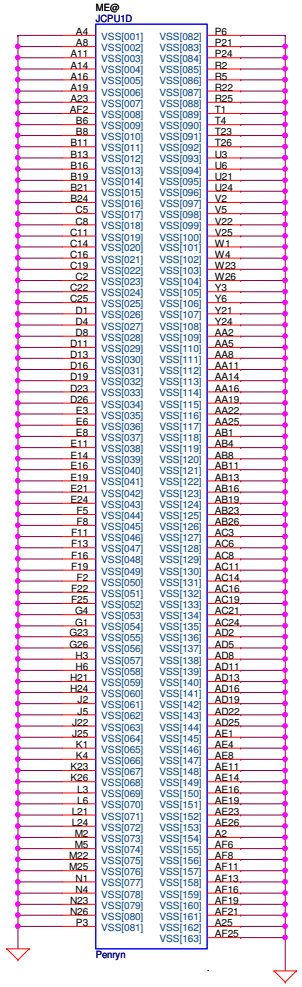
Compal Electronics, Inc.

Title: Penryn(1/3)-AGTL+THM,FAN

Size	Document Number	Rev
Custom	LA7011P	1.0

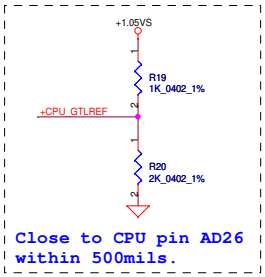
Date: Friday, December 24, 2010 Sheet 4 of 41



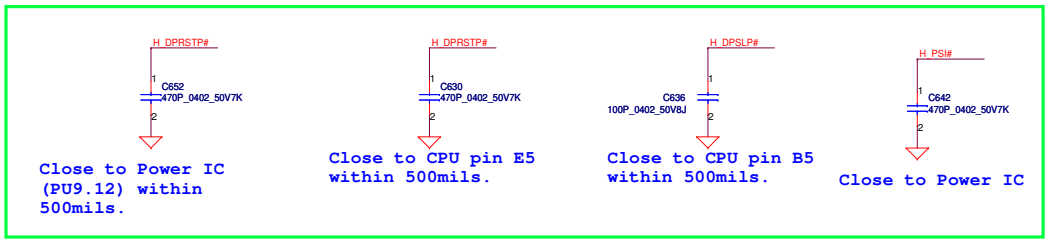


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

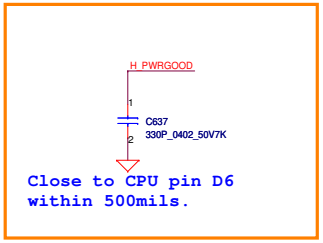
Layout note: Z0=55 ohm
0.5" max for GTLREF.



09/29 Add for power noise



PVT for ESD solution



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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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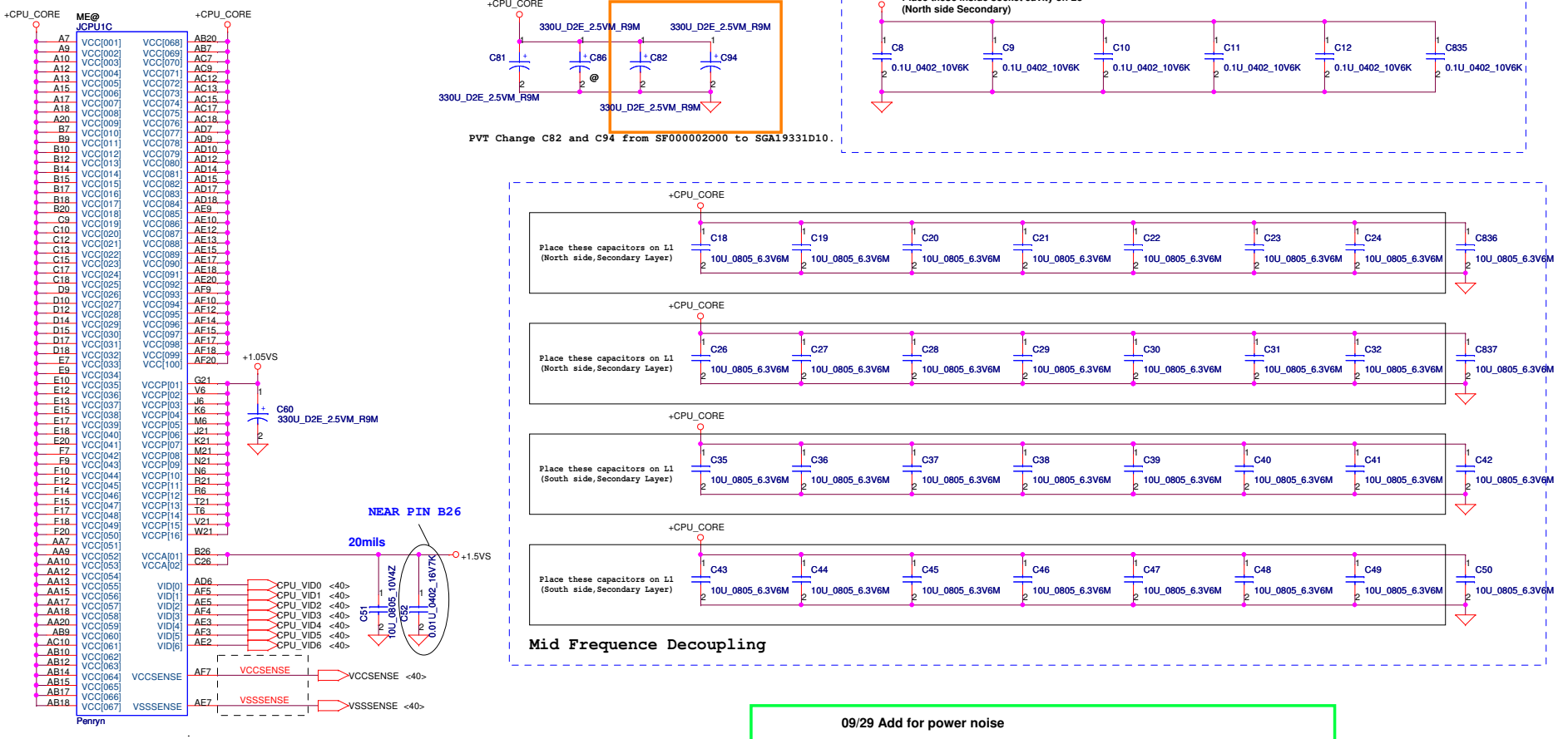
Compal Electronics, Inc.		
Title	Penryn(2/3)-AGTL+GND	
Size: Custom	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 5 of 41	



The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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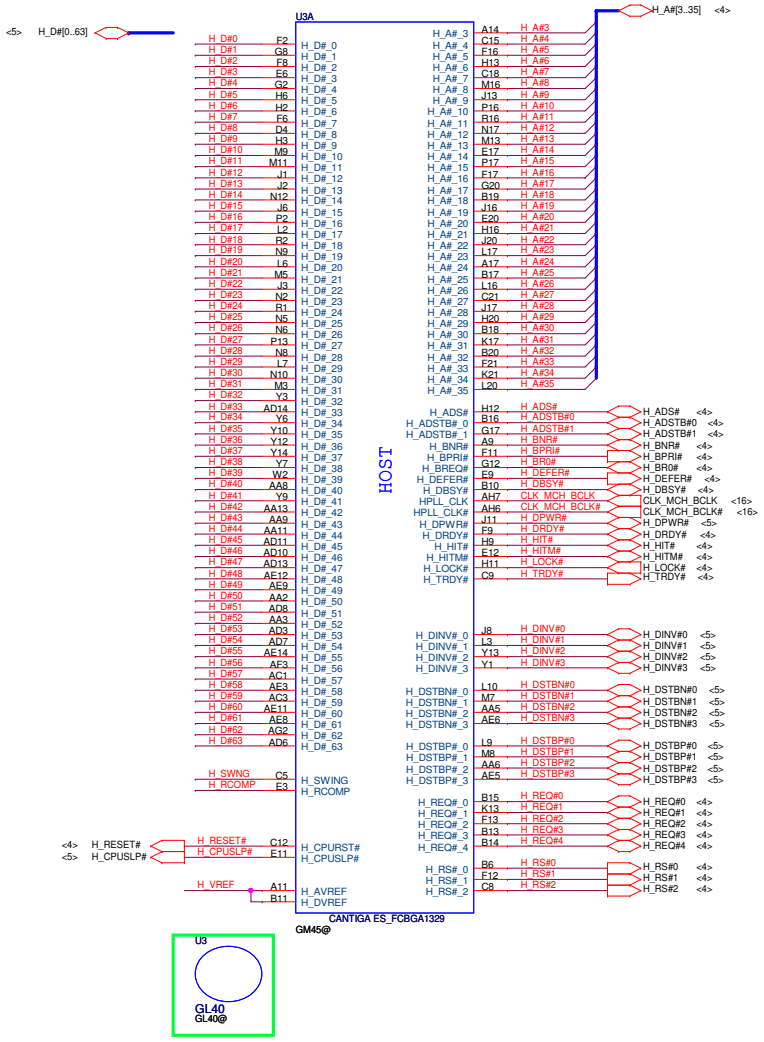
Compal Electronics, Inc.

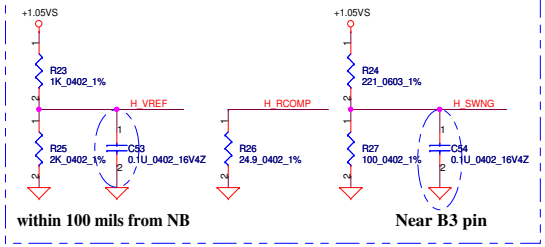
Title: Penryn(3/3)-PWR+Bypass

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 6 of 41



Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

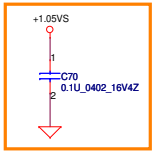


within 100 mils from NB

Near B3 pin

PVT ESD solution.

Please close to R23



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.		
Title: Cantiga(1/7)-AGTL+		
Size: Custom	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 7 of 41	

Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation *(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

U3B

RSVD: RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#

CLK: DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#

DMI: DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3

CFG: CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

EM: PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

GRAPHICS VID: GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN

ME: CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

MISC: DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#

HDA: HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

NC: NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

CANTIGA ES_FCBGA1329

GM45@

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20. CLOSE TO PIN.AV42

+DDR_MCH_REF — R58 10K_0402_1% — C61 0.1U_0402_16V4Z — R64 10K_0402_1%

For DDR3 : 1.5V power rail
For DDR2 : 1.8V power rail

+1.5V — R28 80.6_0402_1% — 20mil — R29 80.6_0402_1%

For Crestline: 20ohm
For Calero: 80.6ohm
For Cantiga: 80.6ohm

SM_RCOMP_VOH — R30 0_0402_5% — R53 @12K_0402_5% — 1.5V_PGOOD <39> DDR3_SM_PWROK <27>

SM_VREF — +DDR_MCH_REF

SM_PWROK — R721 @10K_0402_5%

SM_REXT — R32 499_0402_1%

SM_DRAMRST# — SM_DRAMRST# <14,15>

SM_DRAMRST# is only for DDR3. DDR2 left it No Connect

+1.5V — R34 1K_0402_1% — SMRCOMP_VOH — C55 0.01U_0402_25V7K — C56 2.2U_0603_6.3V4Z — R724 3.01K_0402_1%

SMRCOMP_VOL — C57 0.01U_0402_25V7K — C58 2.2U_0603_6.3V4Z — R43 1K_0402_1%

+1.05VS — R33 1K_0402_5% @ — R722 54.9_0402_1% @ — +3VS — R723 1K_0402_5% @ — MCH_TSATN# — Q42 MMBT3904_SOT23-3 @ — TSATN# <27>

+3VS — R47 10K_0402_5% — R48 10K_0402_5% — PM_EXTTS#0 — PM_EXTTS#1

<16> MCH_CLKSEL0 — MCH_CLKSEL0 — T25 CFG_0
<16> MCH_CLKSEL1 — MCH_CLKSEL1 — R25 CFG_1
<16> MCH_CLKSEL2 — MCH_CLKSEL2 — P25 CFG_2
P20 CFG_3
P24 CFG_4
C25 CFG_5
N24 CFG_6
M24 CFG_7
E21 CFG_8
C23 CFG_9
C24 CFG_10
N21 CFG_11
P21 CFG_12
T21 CFG_13
R20 CFG_14
M20 CFG_15
L21 CFG_16
H21 CFG_17
P29 CFG_18
R28 CFG_19
T28 CFG_20

R725 @2.21K_0402_1% — MCH_CFG_5
R39 @2.21K_0402_1% — MCH_CFG_6
R40 @2.21K_0402_1% — MCH_CFG_7
R41 @2.21K_0402_1% — MCH_CFG_9
R42 @2.21K_0402_1% — MCH_CFG_10
R44 @2.21K_0402_1% — MCH_CFG_12
R45 @2.21K_0402_1% — MCH_CFG_13
R46 @2.21K_0402_1% — MCH_CFG_16
+3VS — R49 @4.02K_0402_1% — MCH_CFG_19
R50 @4.02K_0402_1% — MCH_CFG_20

<19,27> ICH_POK — R51 0_0402_5% — PM_POK_R
<19,40> VGATE — R727 @0_0402_5%
<17,23,24> PLT_RST# — R728 100_0402_5% — PLT_RST#_R

<19> PM_BMBUSY# — PM_BMBUSY# — R29
<5,18,40> H_DPRSTP# — H_DPRSTP# — B7
<14,15> PM_EXTTS#0 — PM_EXTTS#0 — N33
PM_EXTTS#1 — P32
PM_POK_R — AT40
PLT_RST#_R — AT11
<4,18> H_THERMTRIP# — H_THERMTRIP# — T20
<19,40> DPRSLPVR — DPRSLPVR — R32

For independent Power Rail : connect to PWM CORE VID
For Common Power Rail : left it No Connect

+1.05VS — R726 1K_0402_1% — C59 0.1U_0402_16V4Z — R729 499_0402_1%

For AMT function

CL_CLK — CL_CLK0 <19>
CL_DATA — CL_DATA0 <19>
CL_PWROK — M_PWROK <19>
CL_RST# — CL_RST# <19>

DDPC_CTRLCLK — T110
DDPC_CTRLDATA — T109
SDVO_CTRLCLK — N28
SDVO_CTRLDATA — M28
SDVO_SCLK — G36
CLKREQ# — E36 — MCH_CLKREQ# — MCH_CLKREQ# <16>
ICH_SYNC# — K36 — MCH_ICH_SYNC# — MCH_ICH_SYNC# <19>

TSATN# — B12 — MCH_TSATN# — R57 56_0402_5% — +1.05VS

SDVO_SCLK — R56 @ 2.2K_0402_5% — +3VS

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled *(Default 1 = Digital display (iHDMI/DP) interface enabled

Place closely pin U3.R32 — DPRSLPVR — C861 1000P_0402_50V7K
Place closely pin PR132.2 — DPRSLPVR — C862 1000P_0402_50V7K

09/16 Add C838 For noise

Place closely pin AT11 — PLT_RST#_R — C838 0.1U_0402_16V4Z
Place closely pin B7 — H_DPRSTP# — C631 470P_0402_50V7K
Place closely pin AR36 — SM_PWROK — C638 100P_0402_50V8J

Notice: Please check HDA power rail to select HDA controller.

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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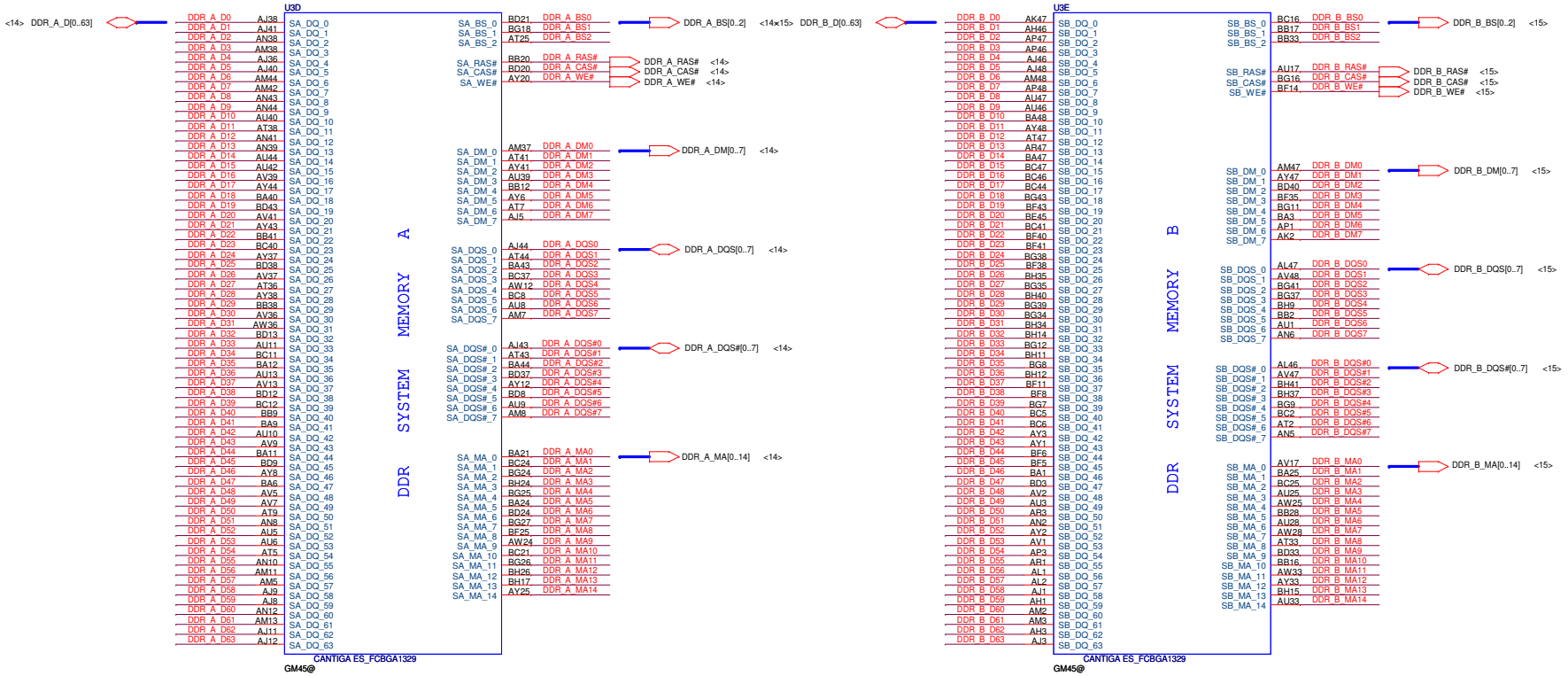
Compal Electronics, Inc.

Title: Cantiga(2/7)-DMI/DDR/STRP

Size: Custom | Document Number: LA7011P | Rev: 1.0

Date: Friday, December 24, 2010 | Sheet 8 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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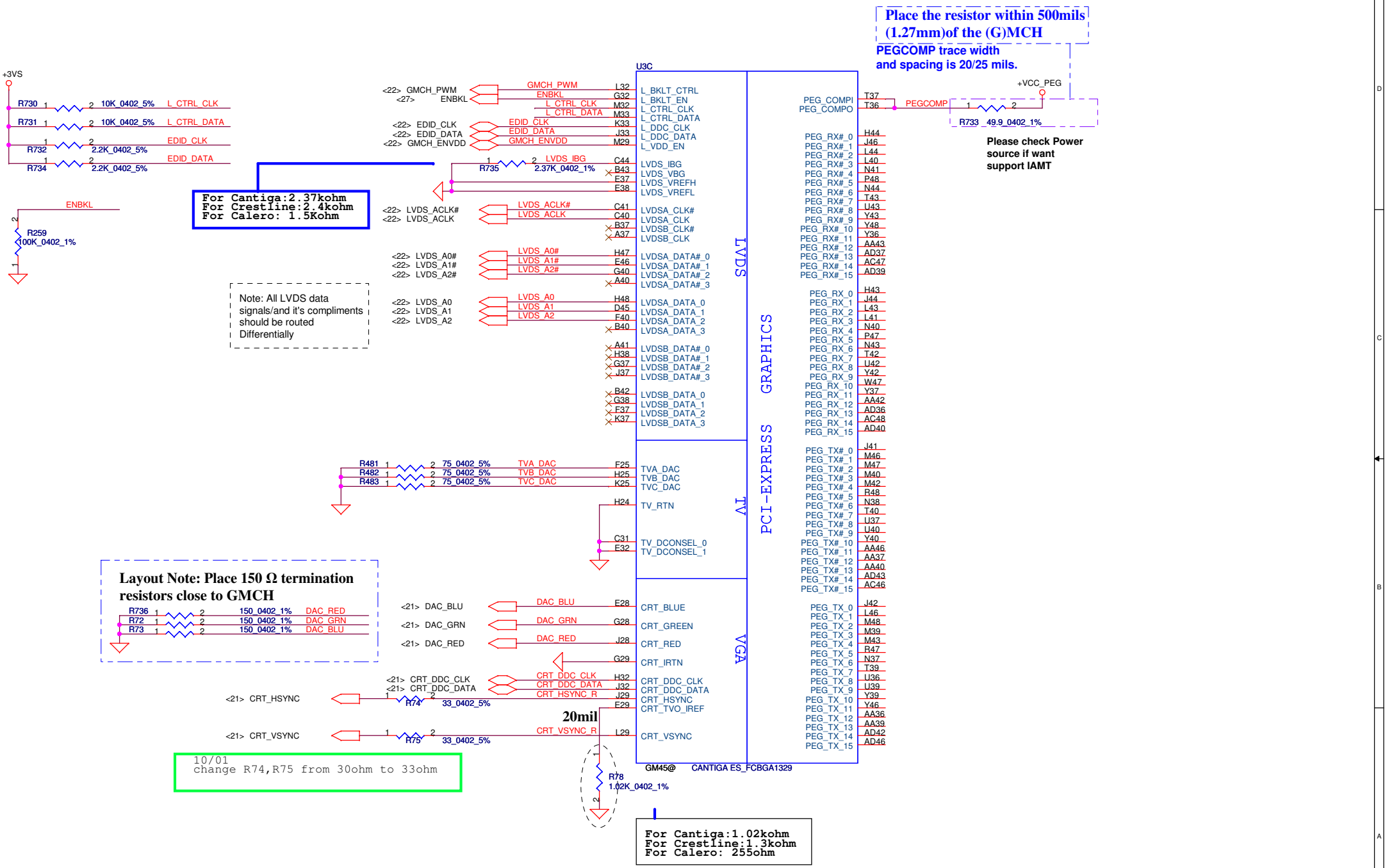
Compal Electronics, Inc.

Title: **Cantiga(3/7)-DDR3 A/B CH**

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 | Sheet 9 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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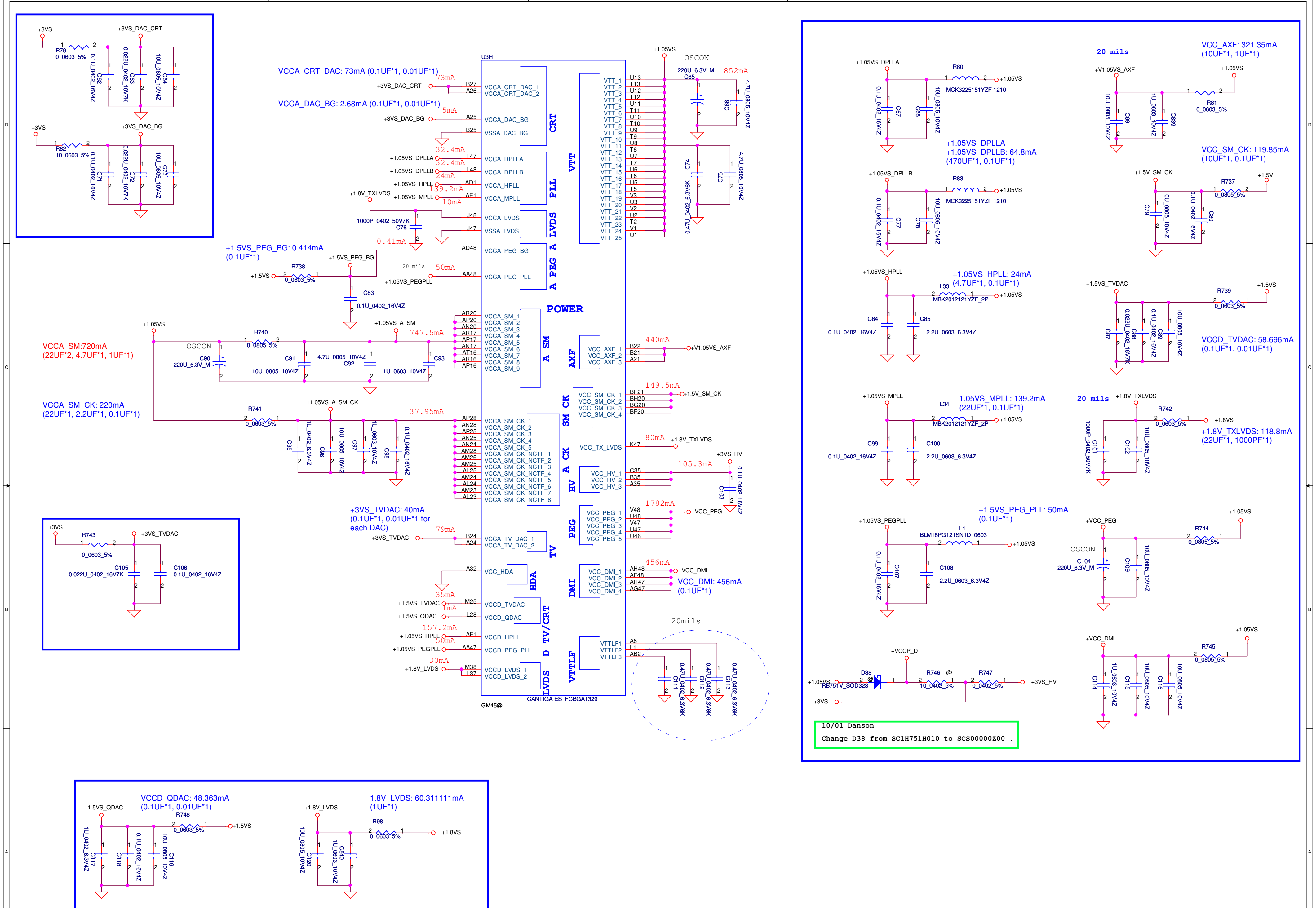
Compal Electronics, Inc.

Title: **Cantiga(4/7)-VGA/LVDS**

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 10 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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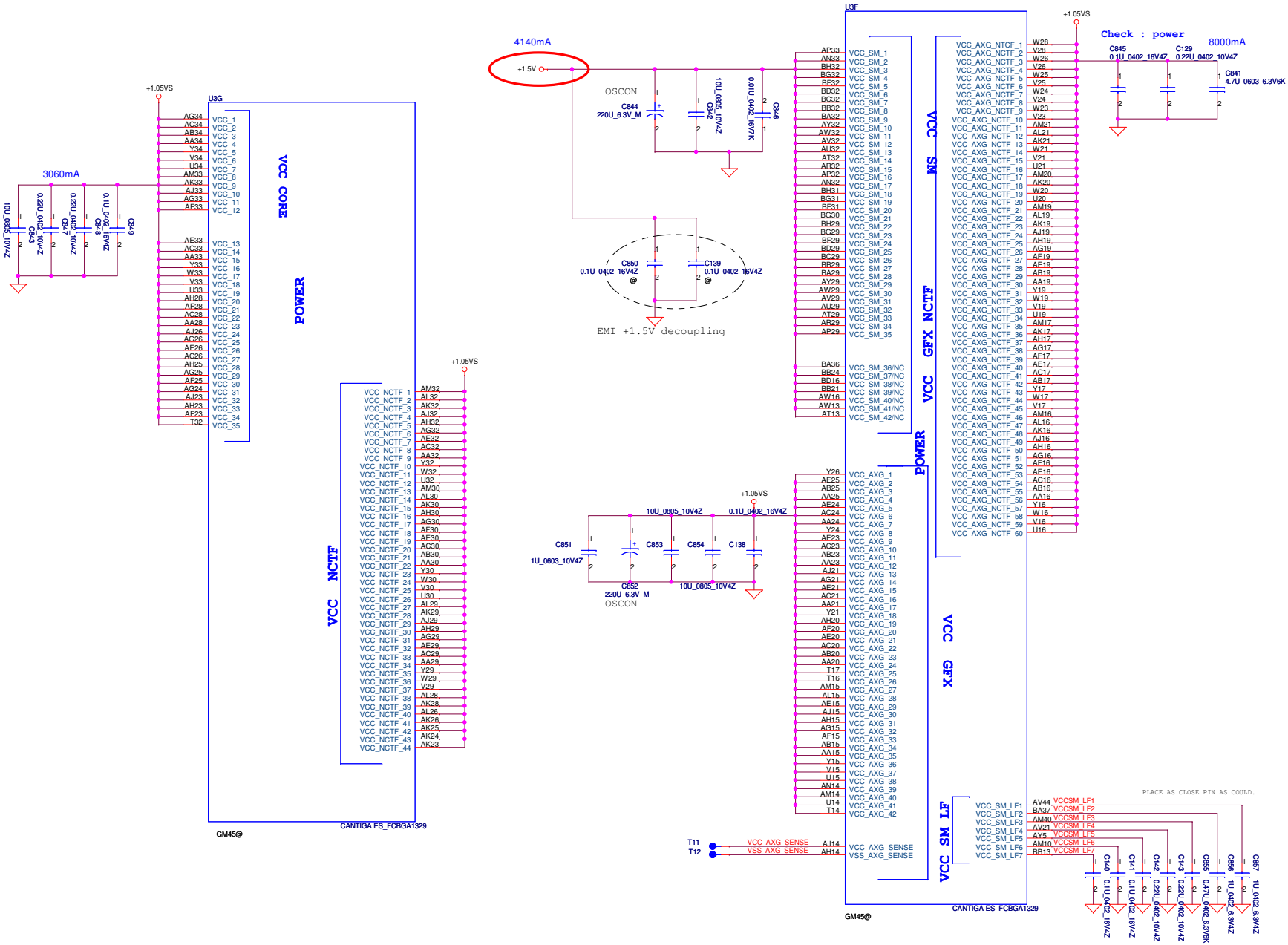
Compal Electronics, Inc.

Title: **Cantiga(6/7)-VCC-1**

Size | Document Number: LA7011P | Rev 1.0

Date: Friday, December 24, 2010 | Sheet 11 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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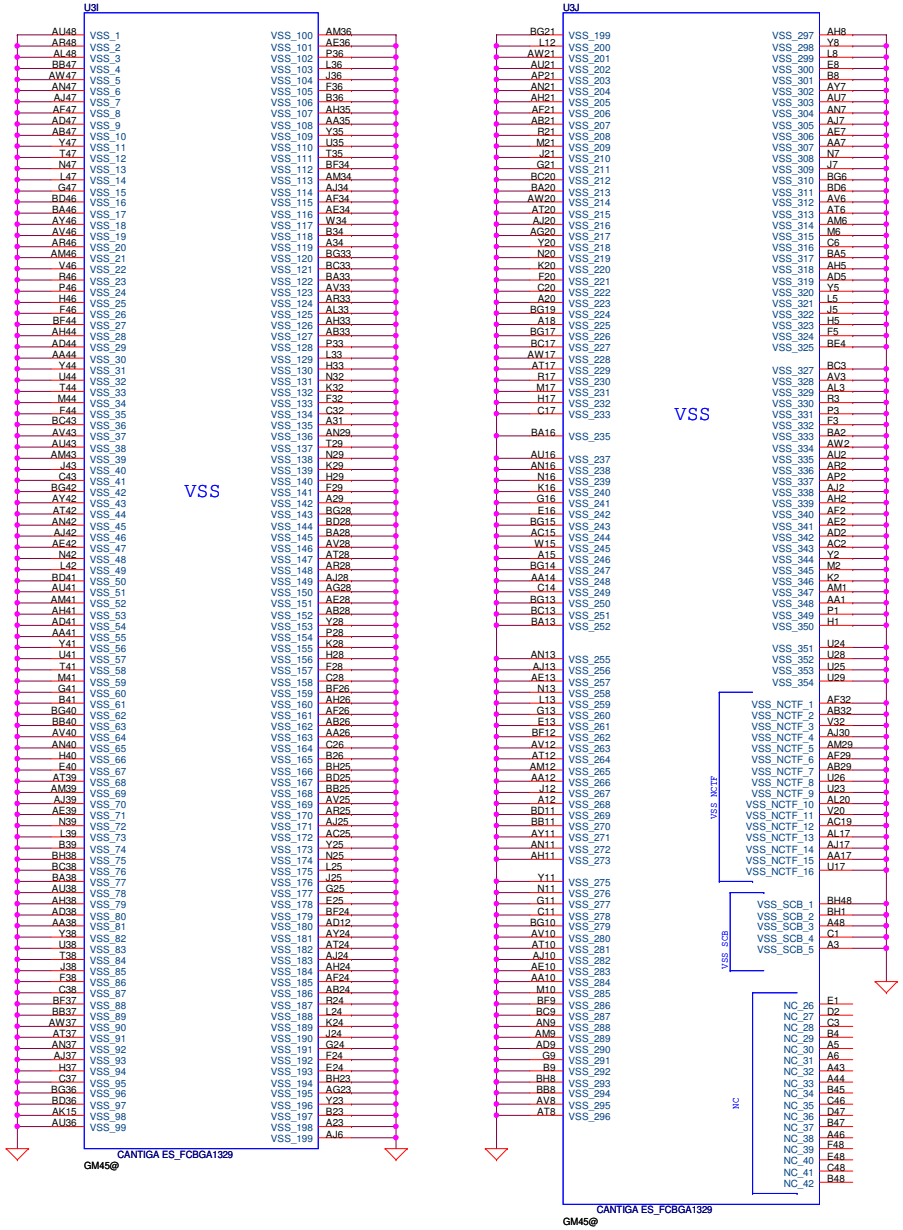
Compal Electronics, Inc.

Title: Cantiga(6/7)-VCC-1

Size	Document Number	Rev
	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 12 of 41



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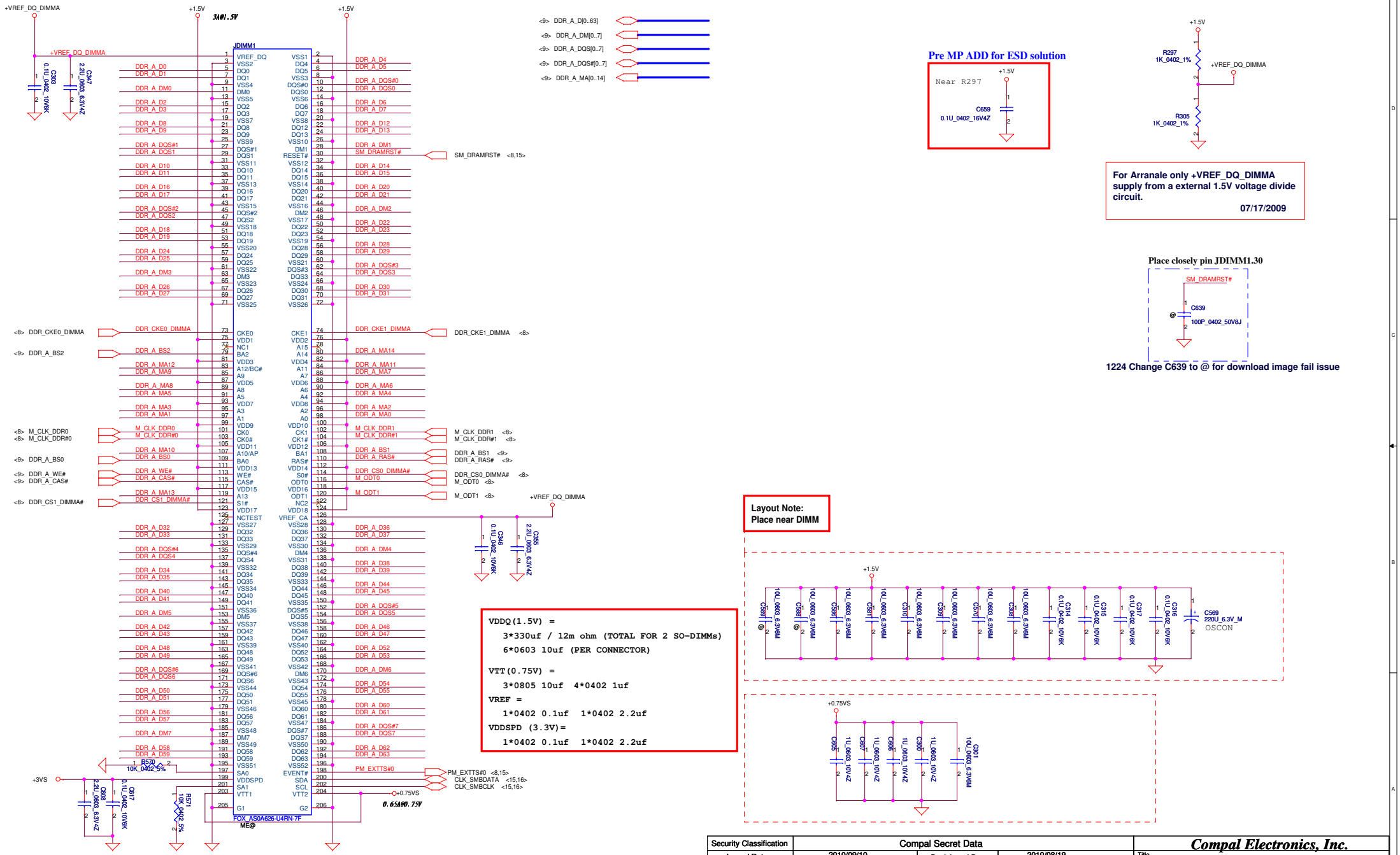
Compal Electronics, Inc.

Title: **Cantiga(7/7)-GND**

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 | Sheet 13 of 41


JDIMM1
FOX_AS0A626-U4RN-7F
ME@
DDR3 SO-DIMM A H=4mm Reverse type
Pre MP ADD for ESD solution
Near R297
C659
0.1U_0402_16V4Z
For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.
07/17/2009
Place closely pin JDIMM1.30
SM_DRAMRST#
C639
100P_0402_50V8J
1224 Change C639 to @ for download image fail issue
Layout Note:
Place near DIMM
VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)
VTT(0.75V) =
3*0805 10uf 4*0402 1uf
VREF =
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf
Security Classification
Compal Secret Data
Issued Date
2010/09/10
Deciphered Date
2010/08/19
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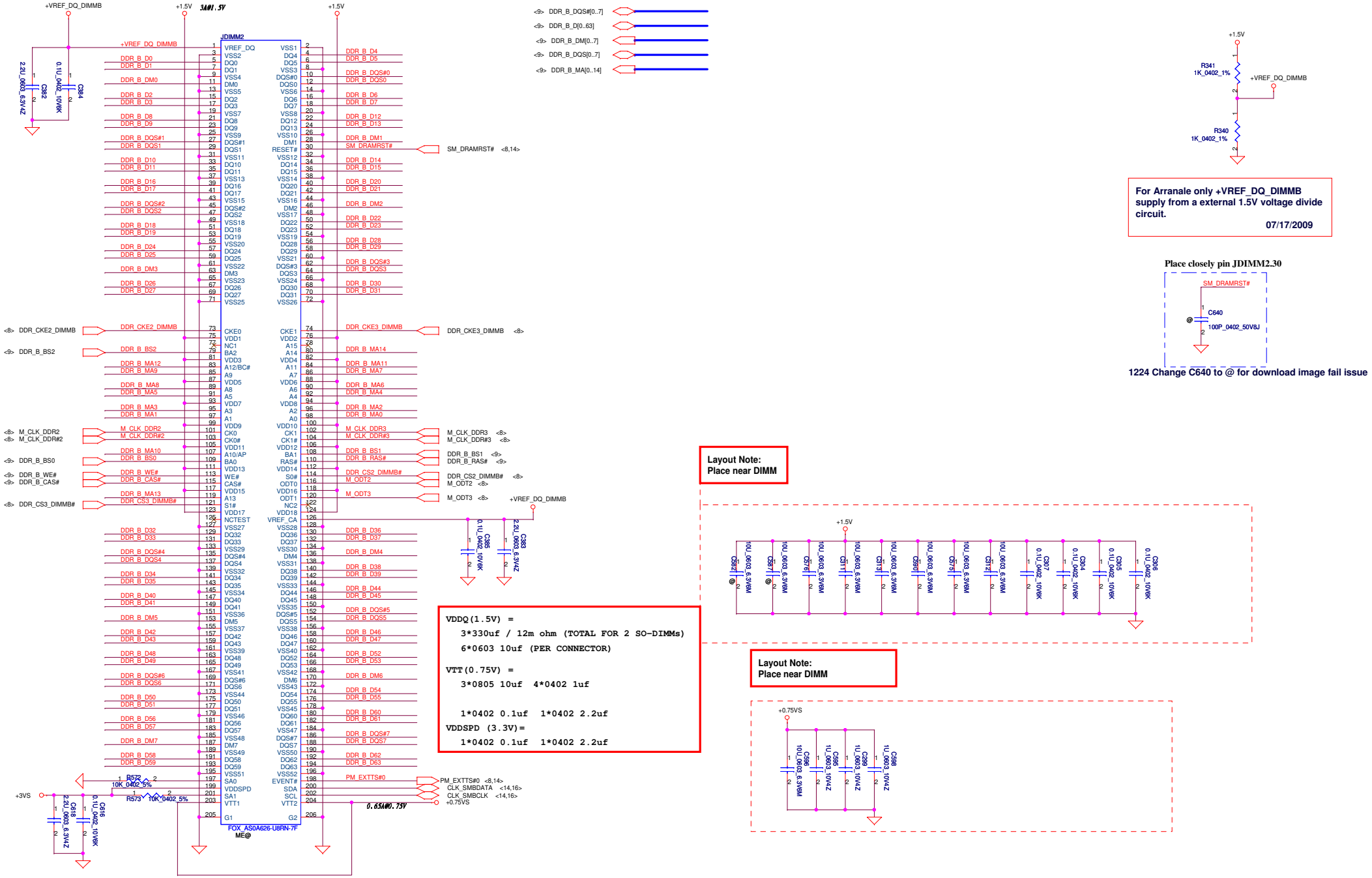
Compal Electronics, Inc.
Title
DDRIII SO-DIMM A
Size Custom
Document Number
LA7011P
Rev 1.0
Date: Friday, December 24, 2010
Sheet 14 of 41



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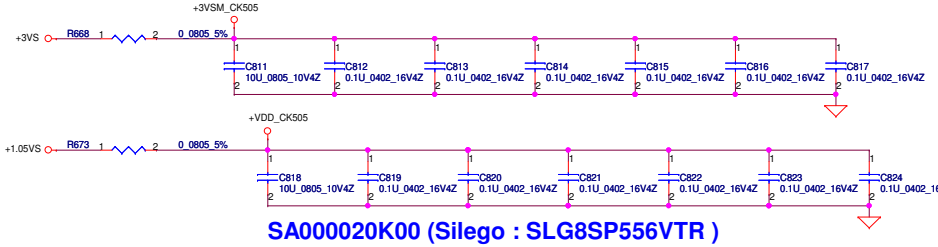
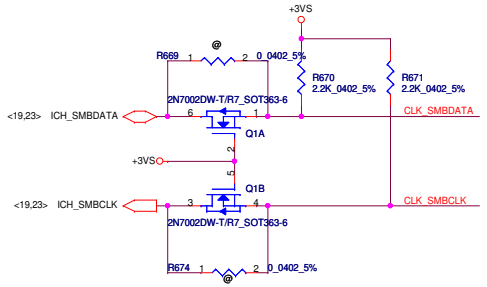
Compal Electronics, Inc.			
Title: DDRIII SO-DIMM B			
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 15 of 41		

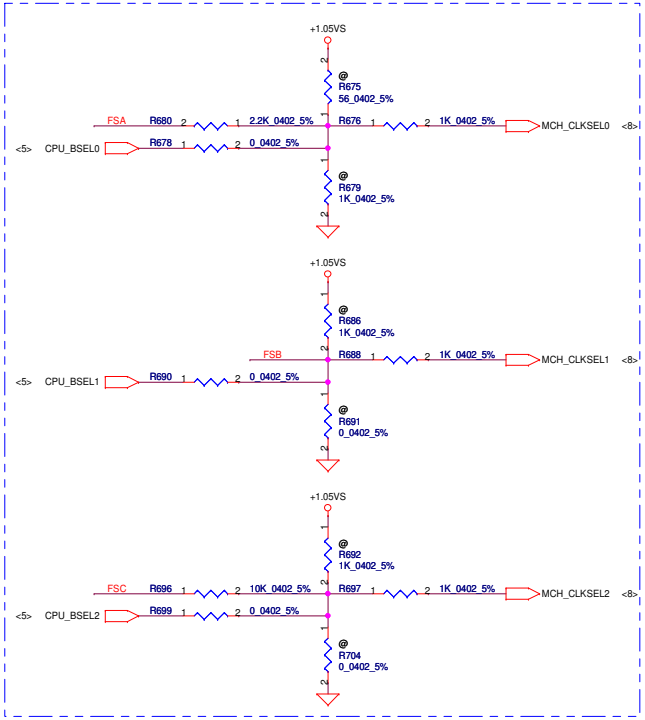
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

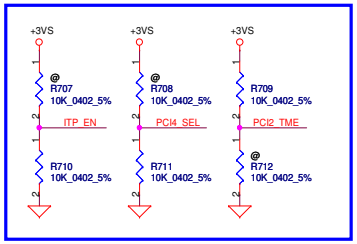




SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)

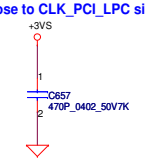




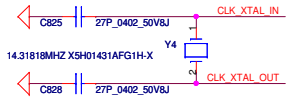
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

PVT

Close to CLK_PCI_LPC signal.



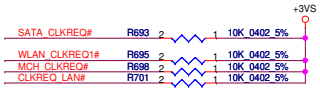
Change Y4 from SJ114P3M720 to SJ100002600.



Routing the trace at least 10mil

SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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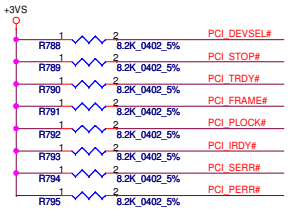
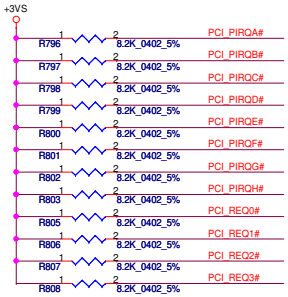
Compal Electronics, Inc.

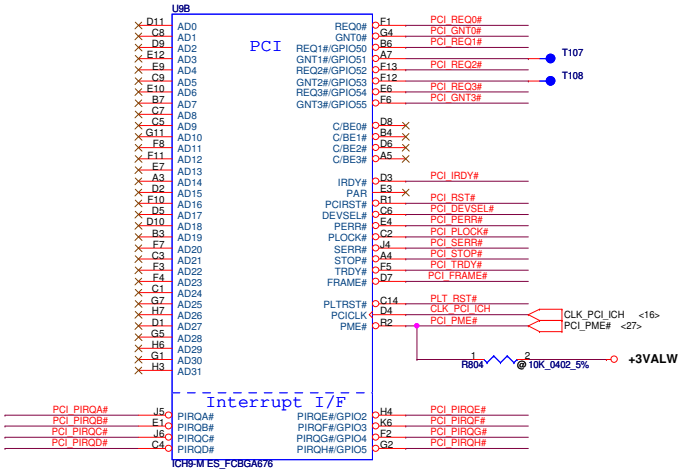
Title: **Clock Generator CK505**

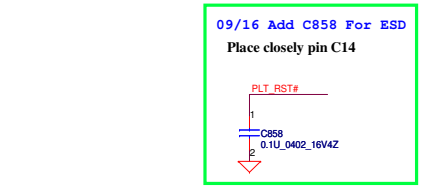
Size: Custom | Document Number: **LA7011P** | Rev: 1.0

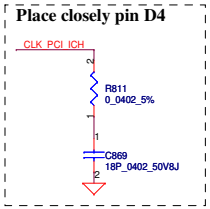
Date: Friday, December 24, 2010 | Sheet 16 of 41

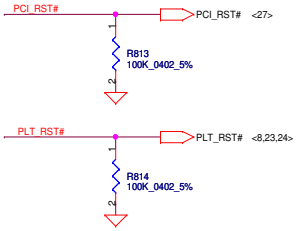


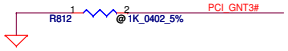












A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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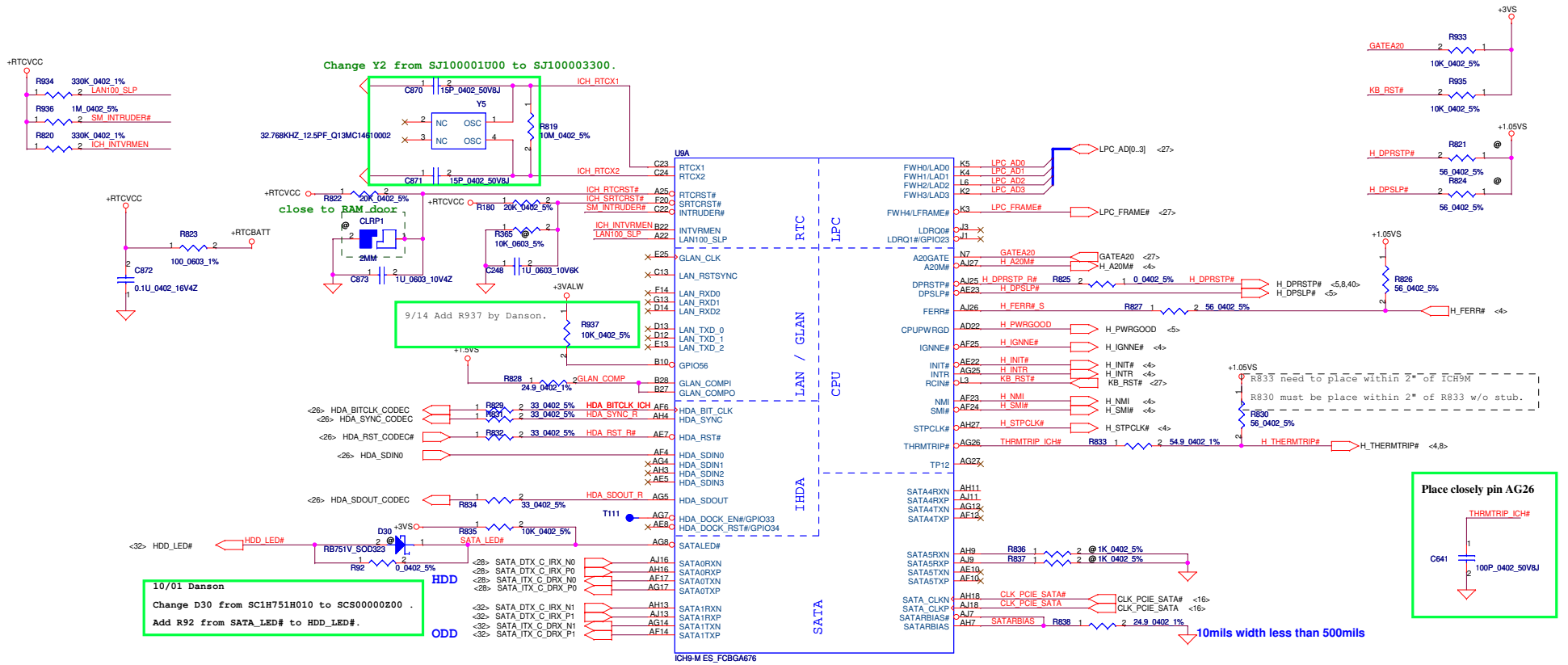
Compal Electronics, Inc.			
Title: ICH9M(1/4)-PCI			
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 17 of 41		



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	
5	

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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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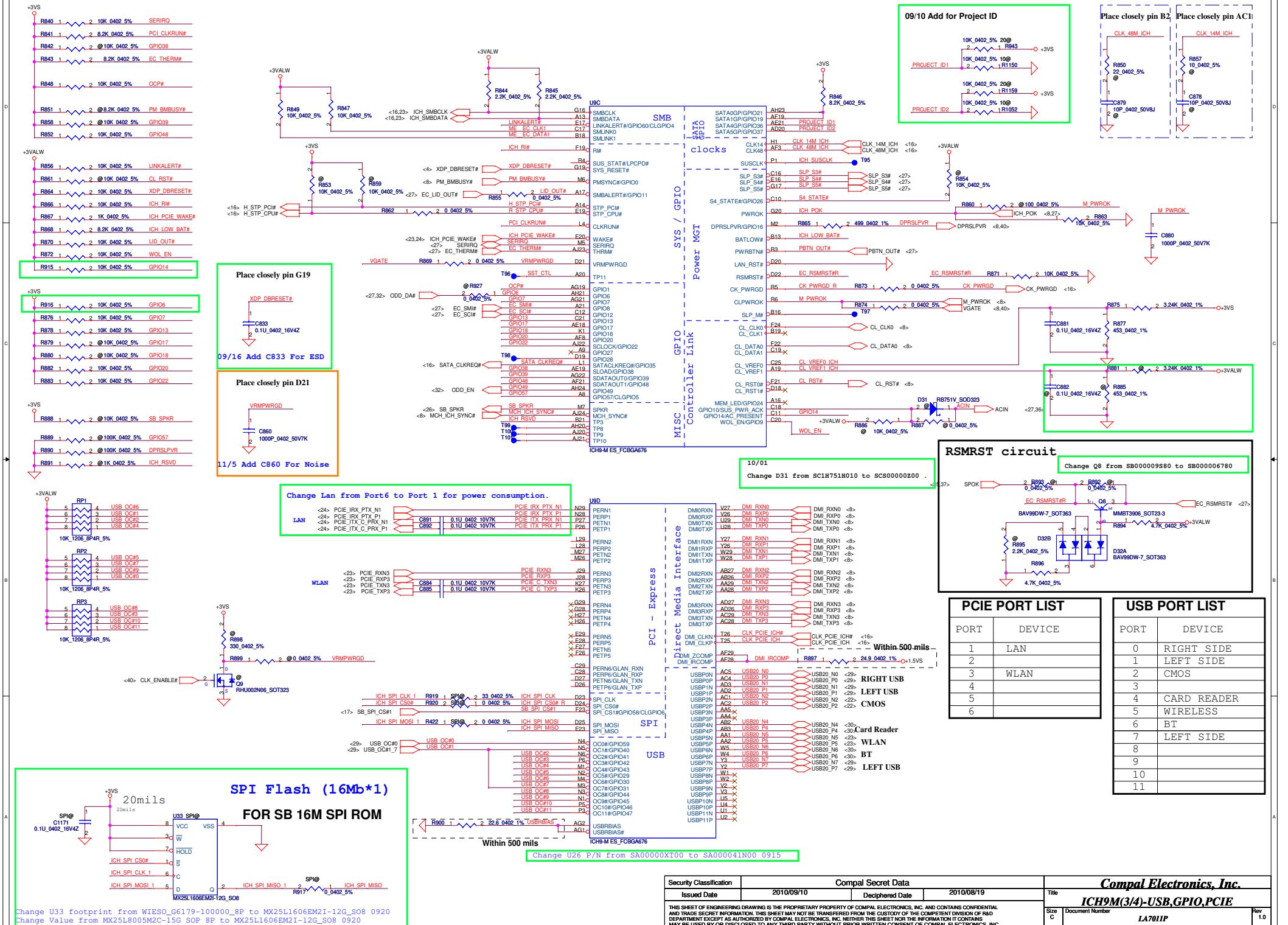
Compal Electronics, Inc.			
Title	ICH9M(2/4)-LAN,ATA,LPC,RTC		
Size: Custom	Document Number: LA7011P		Rev: 1.0
Date: Friday, December 24, 2010	Sheet 18 of 41		



PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	LEFT SIDE
8	
9	
10	
11	

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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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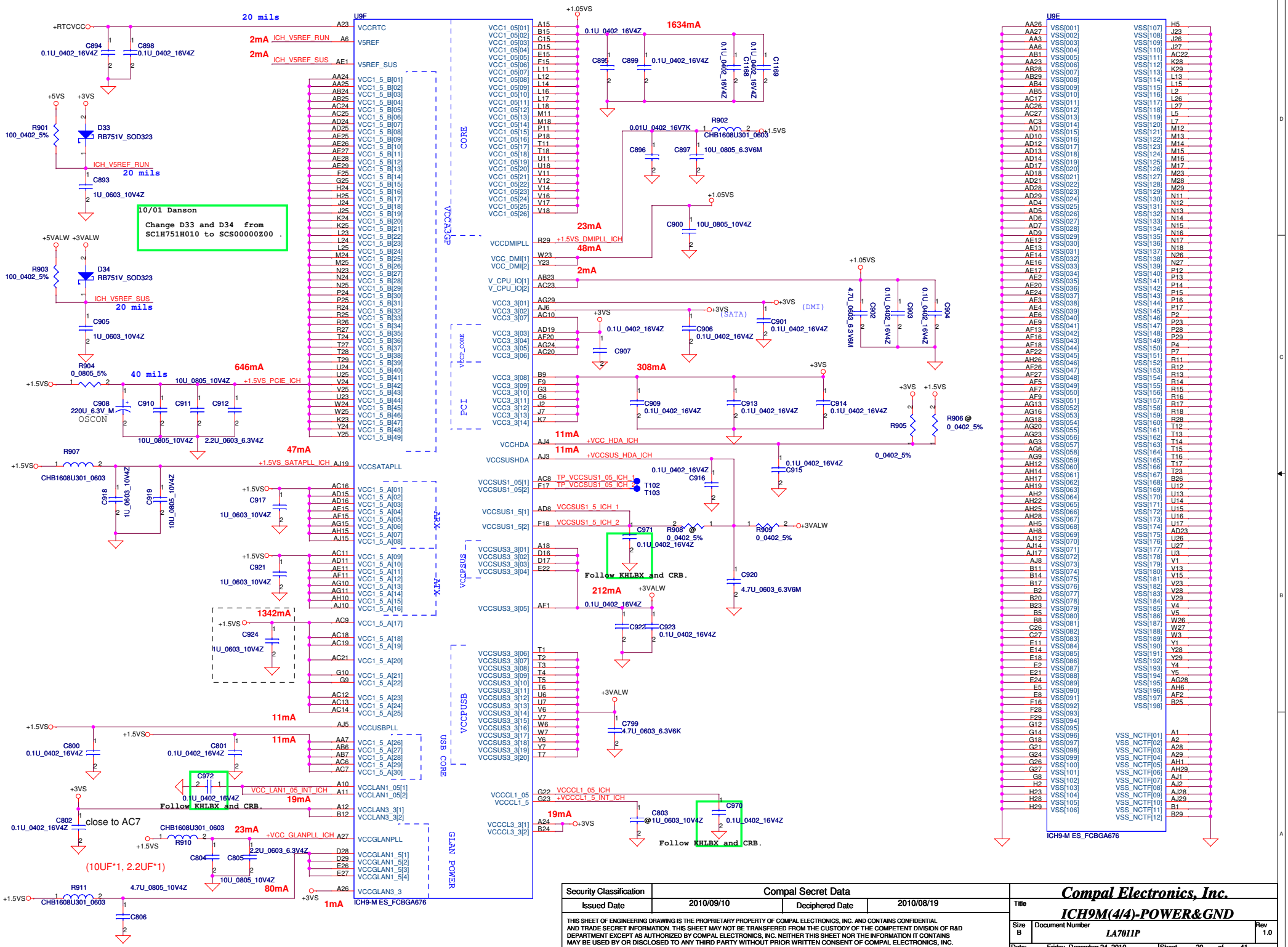
Compal Electronics, Inc.			
Title	ICH9M(3/4)-USB,GPIO,PCIE		
Size C	Document Number LA7011P		Rev 1.0
Date: Friday, December 24, 2010	Sheet 19 of 41		


U9F
U9E
20 mils
2mA
ICH_V5REF_RUN
ICH_V5REF_SUS
10/01 Danson
Change D33 and D34 from SC1H751H010 to SCS00000Z00 .
646mA
47mA
1342mA
11mA
19mA
23mA
80mA
1mA
1634mA
48mA
308mA
212mA
Follow KHLBX and CRB.
close to AC7
(10UF*1, 2.2UF*1)
ICH9-M ES_FCBGA676
Compal Secret Data
2010/09/10
2010/08/19
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Compal Electronics, Inc.
ICH9M(4/4)-POWER&GND
LA7011P
Rev 1.0
Friday, December 24, 2010
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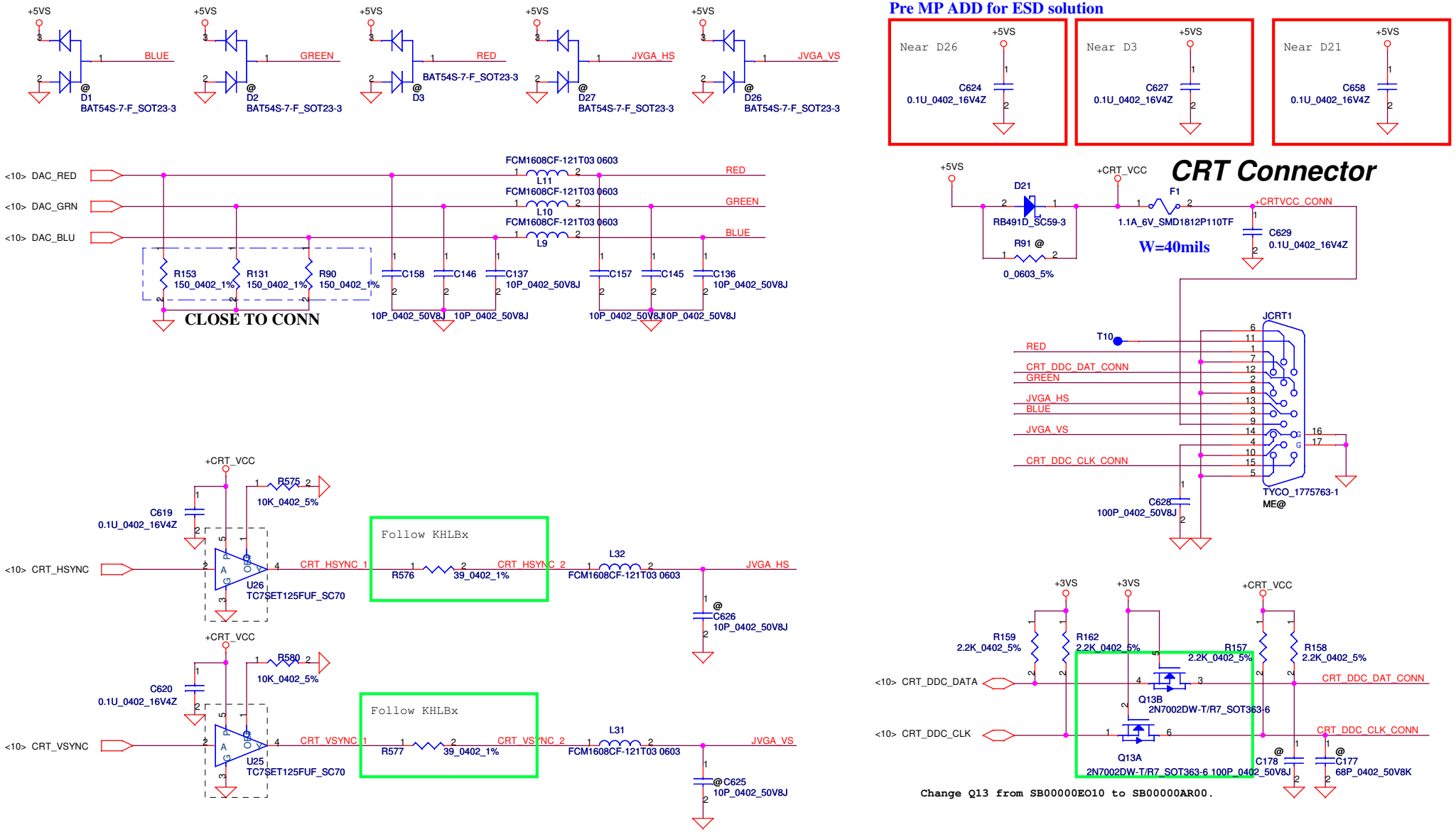

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Issued Date	2010/09/10	Deciphered Date	2010/08/19

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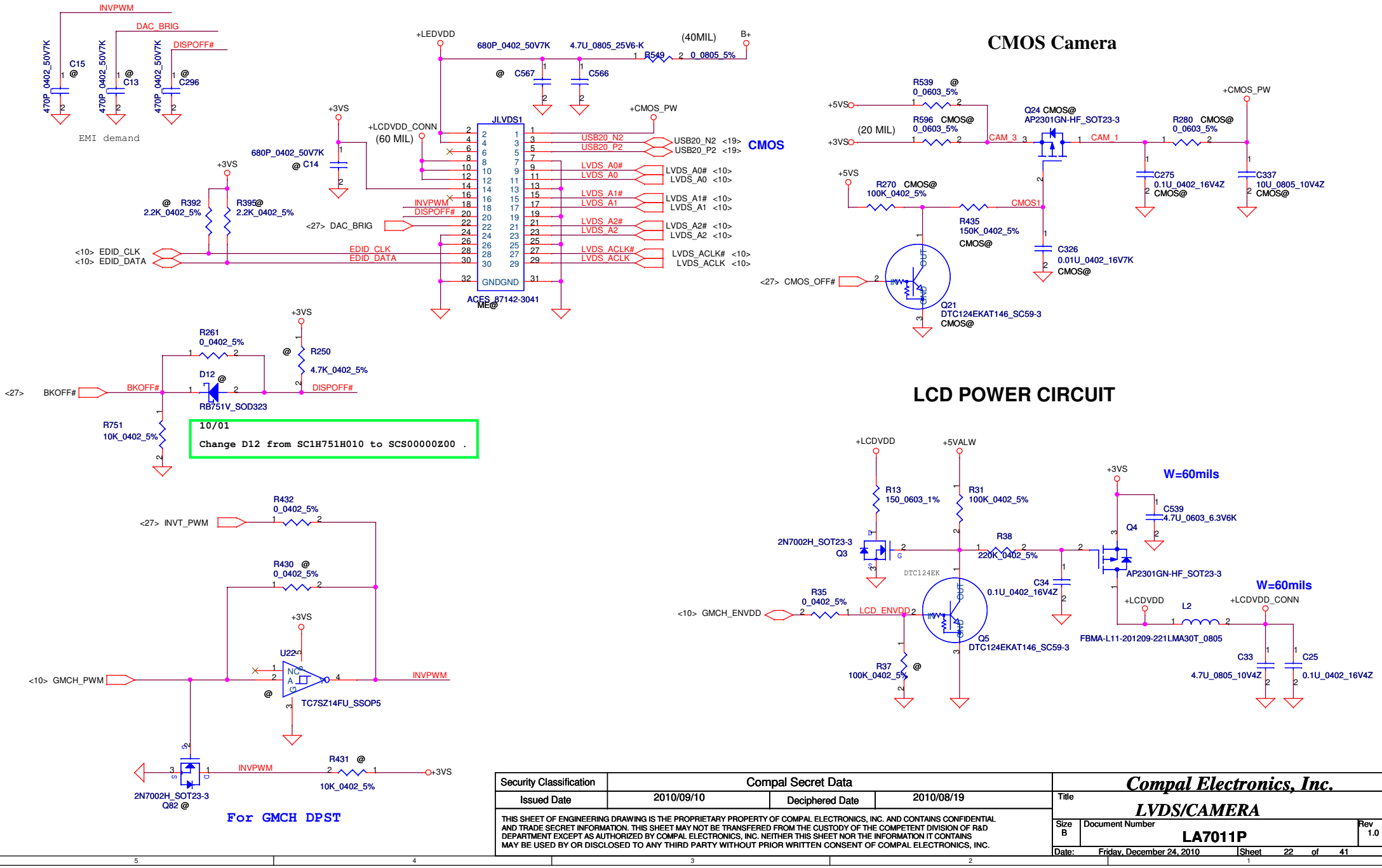
Compal Electronics, Inc.

Title: **CRT Connector**

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 21 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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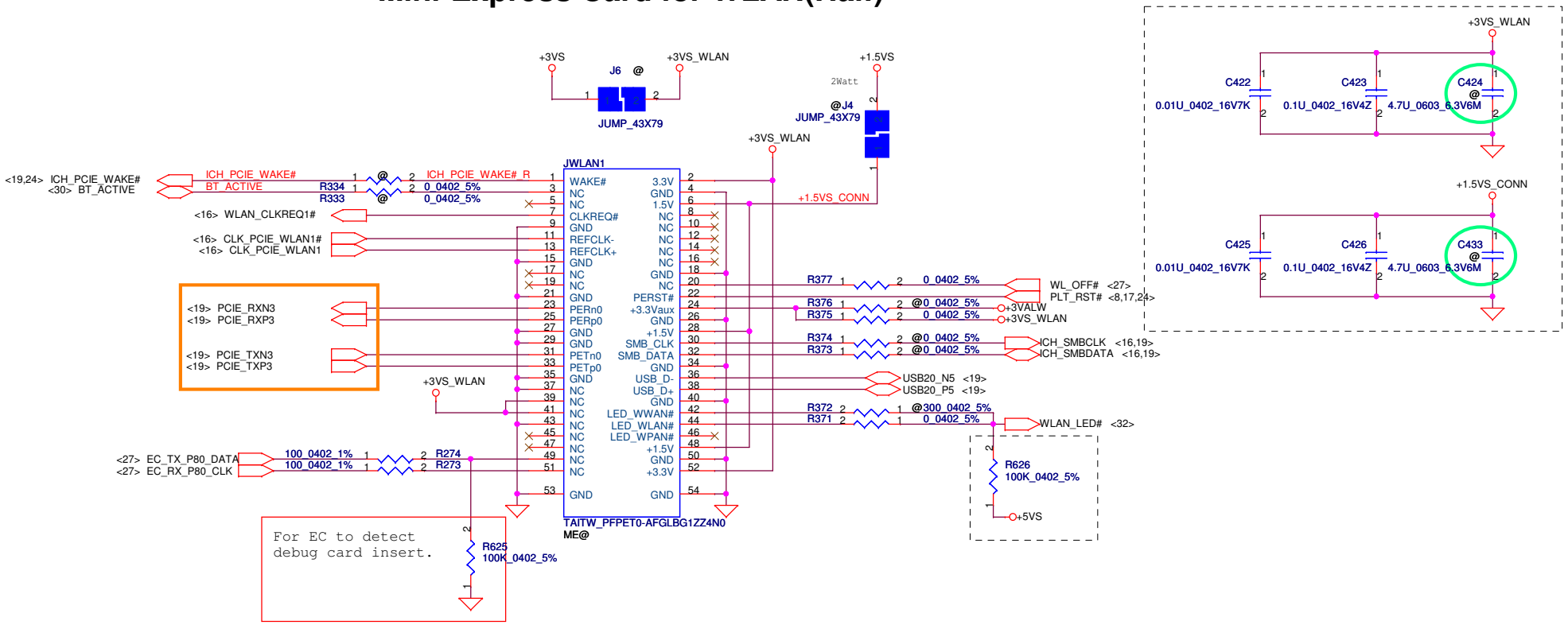
Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
B	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 22 of 41

Mini-Express Card for WLAN(Half)



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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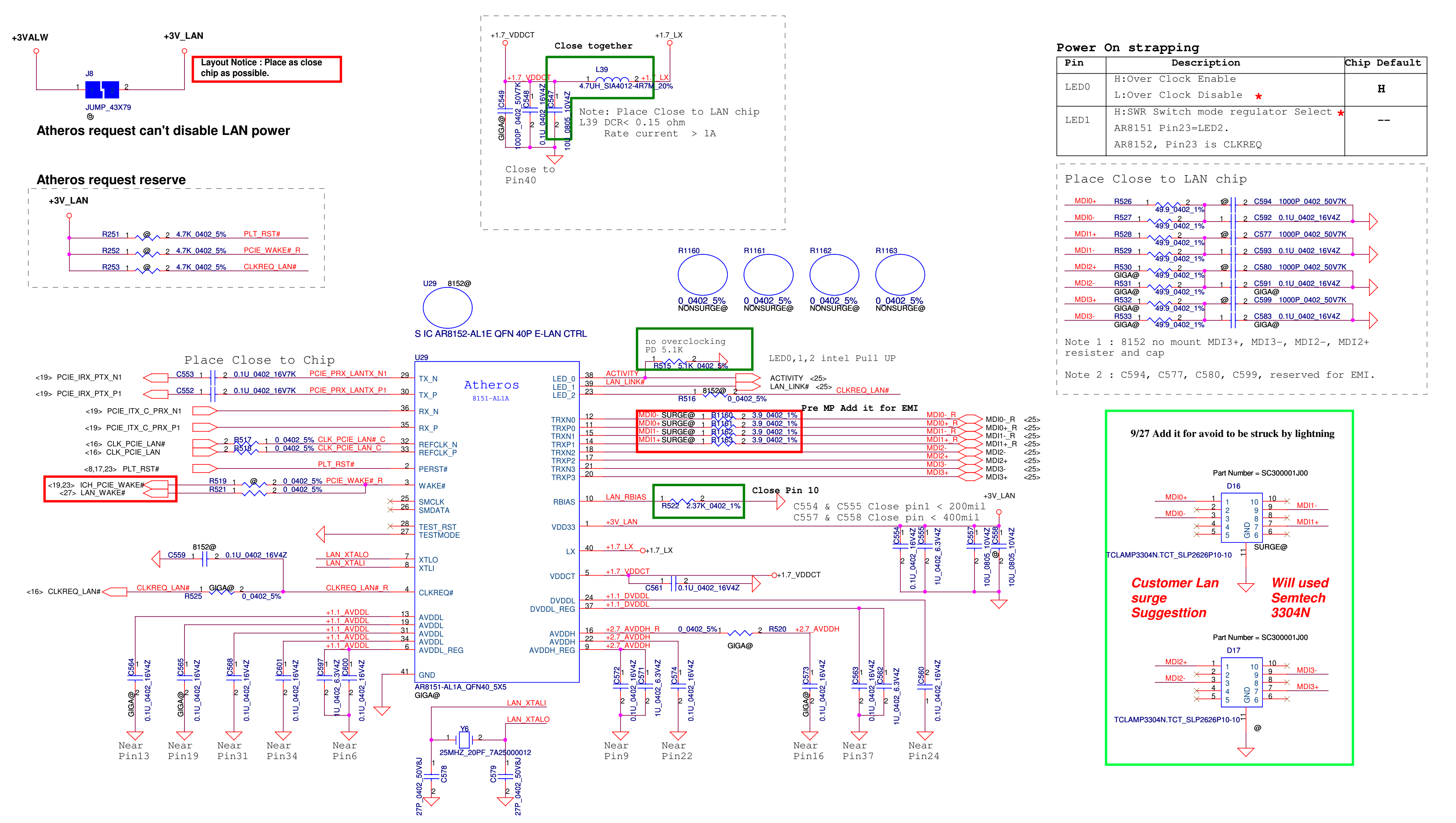
Compal Electronics, Inc.

Title: **Mini-Card/DEBUG-PORT**

Size	Document Number	Rev
	LA7011P	1.0

Date: Friday, December 24, 2010 Sheet 23 of 41


+3VALW
+3V_LAN
Layout Notice : Place as close chip as possible.
J8
JUMP_43X79
Atheros request can't disable LAN power
Atheros request reserve
+3V_LAN
R251 4.7K_0402_5% PLT_RST#
R252 4.7K_0402_5% PCIE_WAKE#_R
R253 4.7K_0402_5% CLKREQ_LAN#
+1.7_VDDCT
+1.7_LX
Close together
L39
4.7UH_SIA4012-4R7M_20%
C549 1000P_0402_50V7K
C548 0.1U_0402_16V4Z
C547 10U_0805_10V4Z
Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A
Close to Pin40
R1160 R1161 R1162 R1163
0_0402_5% NONSURGE@
U29 8152@
S IC AR8152-AL1E QFN 40P E-LAN CTRL
no overclocking
PD 5.1K
R515 5.1K_0402_5%
LED0,1,2 intel Pull UP
Place Close to Chip
U29
Atheros
8151-AL1A
<19> PCIE_IRX_PTX_N1
<19> PCIE_IRX_PTX_P1
C553 0.1U_0402_16V7K PCIE_PRX_LANTX_N1
C552 0.1U_0402_16V7K PCIE_PRX_LANTX_P1
<19> PCIE_ITX_C_PRX_N1
<19> PCIE_ITX_C_PRX_P1
<16> CLK_PCIE_LAN#
<16> CLK_PCIE_LAN
R517 0_0402_5% CLK_PCIE_LAN#_C
R518 0_0402_5% CLK_PCIE_LAN_C
<8,17,23> PLT_RST#
<19,23> ICH_PCIE_WAKE#
<27> LAN_WAKE#
R519 0_0402_5% PCIE_WAKE#_R
R521 0_0402_5%
TX_N TX_P RX_N RX_P REFCLK_N REFCLK_P PERST# WAKE# SMCLK SMDATA TEST_RST TESTMODE XTLO XTLI CLKREQ# AVDDL AVDDL AVDDL AVDDL AVDDL_REG GND
LED_0 LED_1 LED_2 TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3 RBIAS VDD33 LX VDDCT DVDDL DVDDL_REG AVDDH AVDDH AVDDH_REG
ACTIVITY <25>
LAN_LINK# <25>
R516 8152@ 0_0402_5% CLKREQ_LAN#
Pre MP Add it for EMI
MDI0- SURGE@ R1160 3.9_0402_1%
MDI0+ SURGE@ R1161 3.9_0402_1%
MDI1- SURGE@ R1162 3.9_0402_1%
MDI1+ SURGE@ R1163 3.9_0402_1%
MDI0-_R MDI0+_R MDI1-_R MDI1+_R MDI2- MDI2+ MDI3- MDI3+ <25>
LAN_RBIAS R522 2.37K_0402_1%
Close Pin 10
C554 & C555 Close pin1 < 200mil
C557 & C558 Close pin < 400mil
+3V_LAN
8152@ C559 0.1U_0402_16V4Z
LAN_XTALO LAN_XTALI
<16> CLKREQ_LAN#
R525 GIGA@ 0_0402_5% CLKREQ_LAN#_R
C561 0.1U_0402_16V4Z
+1.1_DVDDL
+2.7_AVDDH_R 0_0402_5% R520 +2.7_AVDDH GIGA@
AR8151-AL1A_QFN40_5X5
GIGA@
Y6 25MHZ_20PF_7A25000012
C578 27P_0402_50V8J
C579 27P_0402_50V8J
Near Pin13 Near Pin19 Near Pin31 Near Pin34 Near Pin6
Near Pin9 Near Pin22 Near Pin16 Near Pin37 Near Pin24
Place Close to LAN chip
R526 R527 R528 R529 R530 R531 R532 R533 49.9_0402_1%
C594 1000P_0402_50V7K
C592 0.1U_0402_16V4Z
C577 1000P_0402_50V7K
C593 0.1U_0402_16V4Z
C580 1000P_0402_50V7K
C591 0.1U_0402_16V4Z
C599 1000P_0402_50V7K
C583 0.1U_0402_16V4Z
Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap
Note 2 : C594, C577, C580, C599, reserved for EMI.
9/27 Add it for avoid to be struck by lightning
Part Number = SC300001J00
D16
D17
TCLAMP3304N.TCT_SLP2626P10-10
SURGE@
Customer Lan surge Suggesttion
Will used Semtech 3304N

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED1	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

	Pin4	Configure R525	C559	Pin23	Configure R516
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED[2]	

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

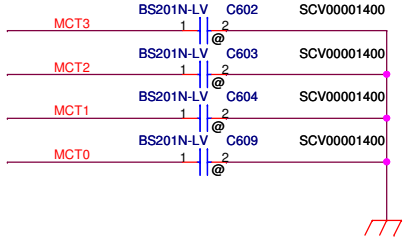
Title: LAN-AR8151/8152

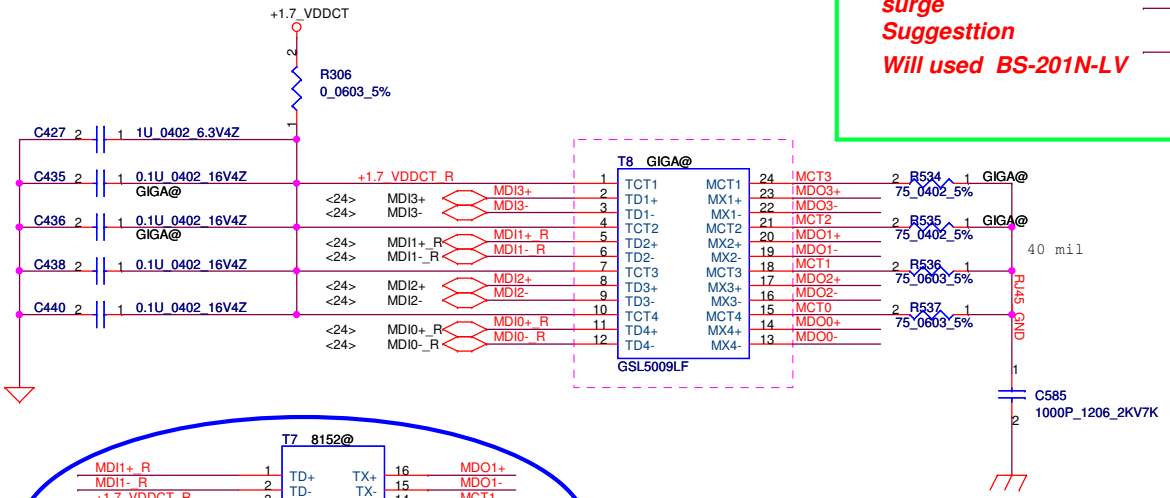
Size: Custom | Document Number: LA7011P | Rev: 1.0

9/27 Add it for avoid to be struck by lightning

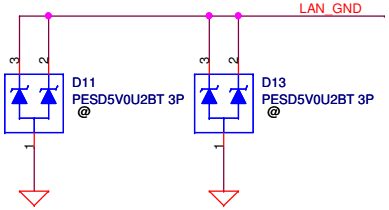
Customer Lan surge Suggesttion

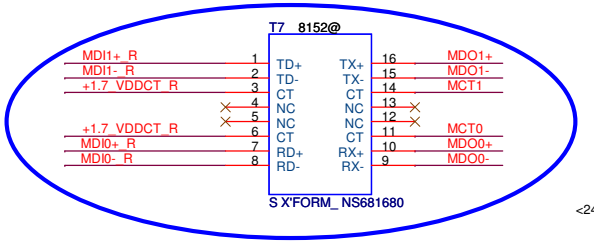
Will used BS-201N-LV





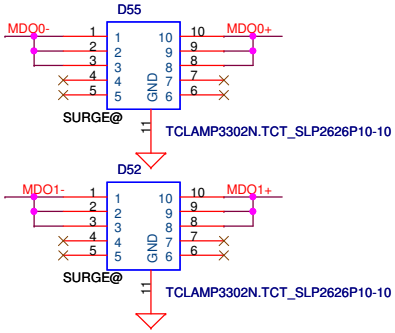
Place closely JRJ45



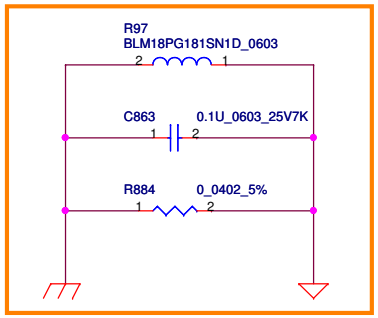


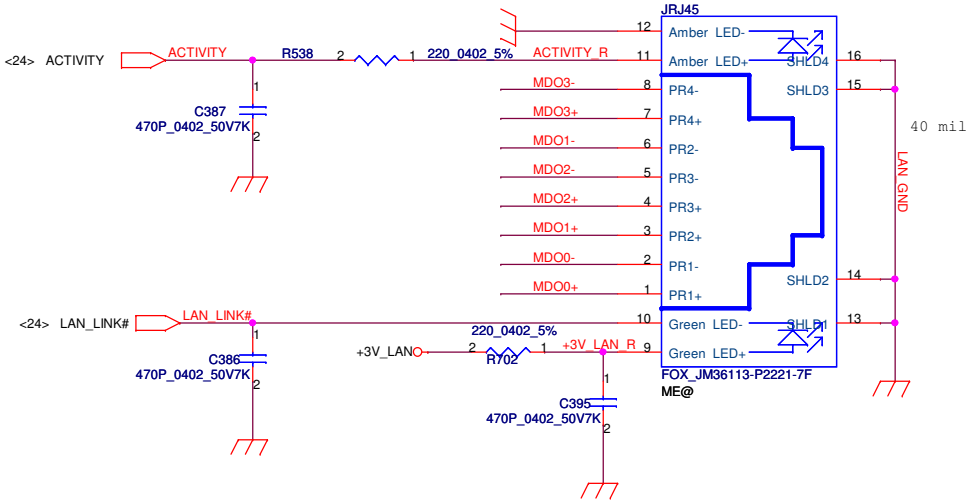
12/13 PreMP Add it for avoid to be struck by lightning

Near to near JRJ45.



PVT Add EMI solution.





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Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
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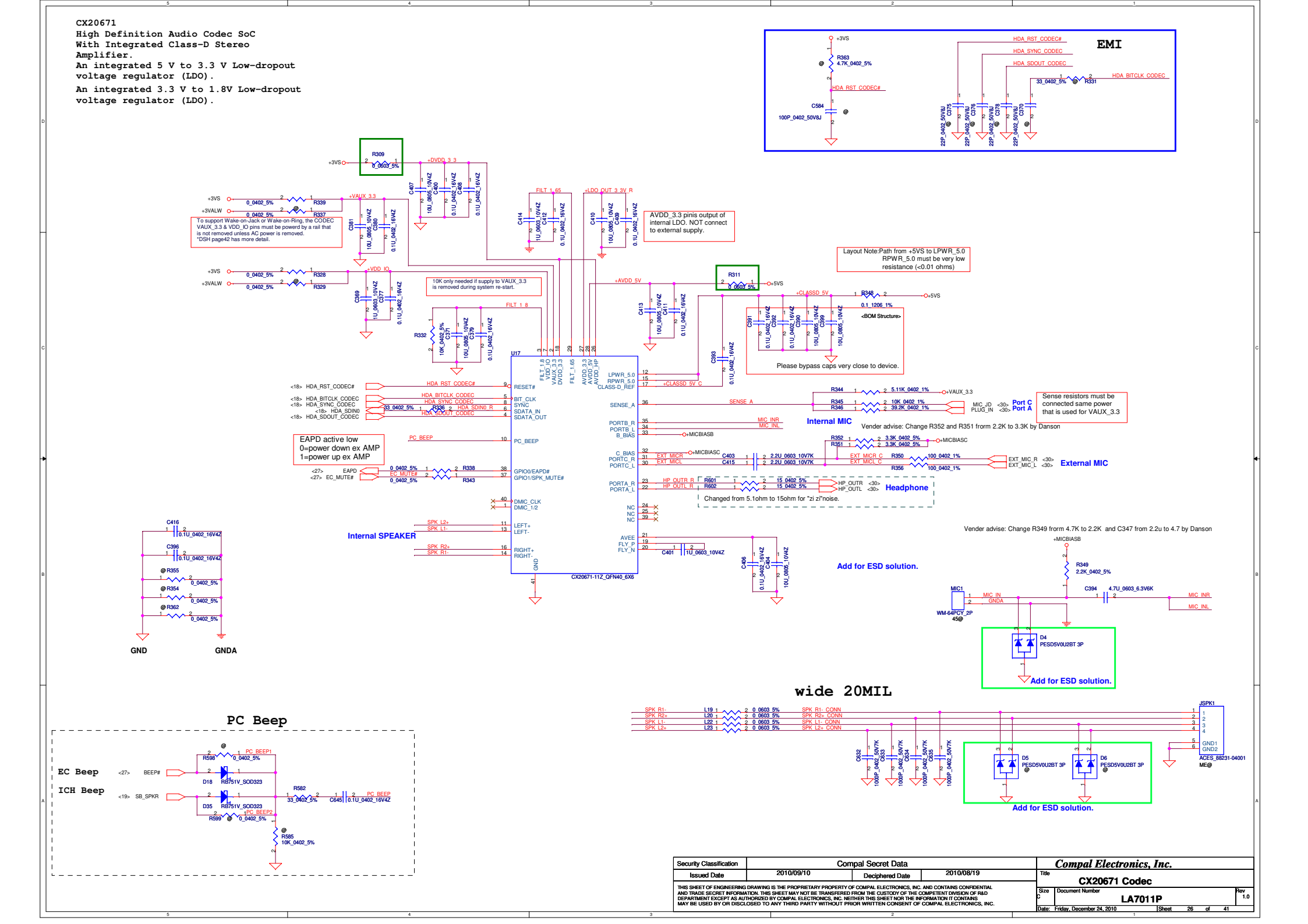
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: CX20671 Codec

Size: C | Document Number: LA7011P | Rev: 1.0

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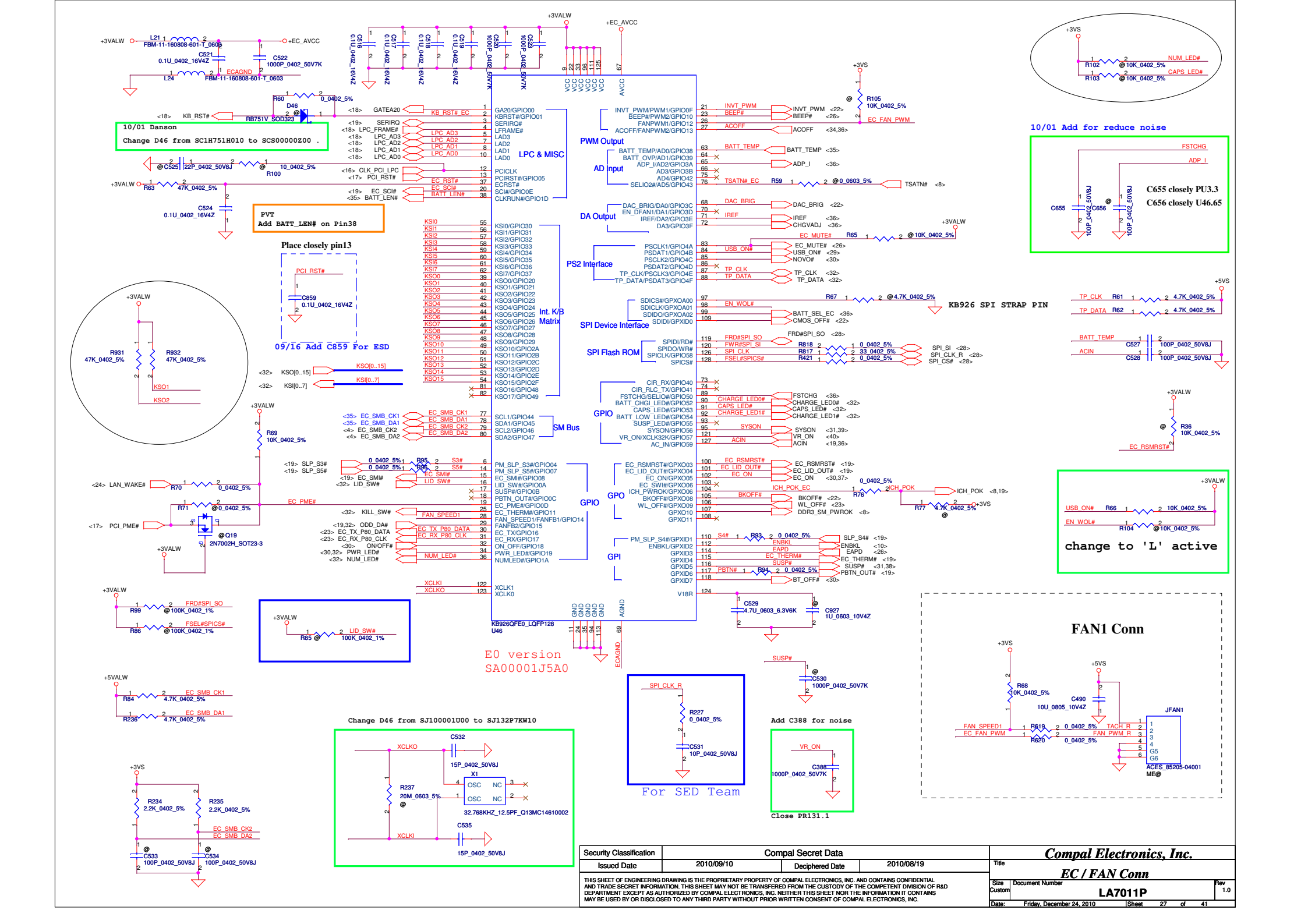
10/01 Danson
Change D46 from SC1H751H010 to SCS00000Z00 .
PVT
Add BATT_LEN# on Pin38
Place closely pin13
09/16 Add C859 For ESD
10/01 Add for reduce noise
C655 closely PU3.3
C656 closely U46.65
KB926 SPI STRAP PIN
change to 'L' active
E0 version
SA00001J5A0
Change D46 from SJ100001U00 to SJ132P7KW10
For SED Team
Add C388 for noise
Close PR131.1
FAN1 Conn
KB926QFE0_LQFP128
U46
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
Security Classification
Compal Secret Data
Issued Date
2010/09/10
Deciphered Date
2010/08/19
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Compal Electronics, Inc.
Title
EC / FAN Conn
Size
Custom
Document Number
LA7011P
Rev
1.0
Date:
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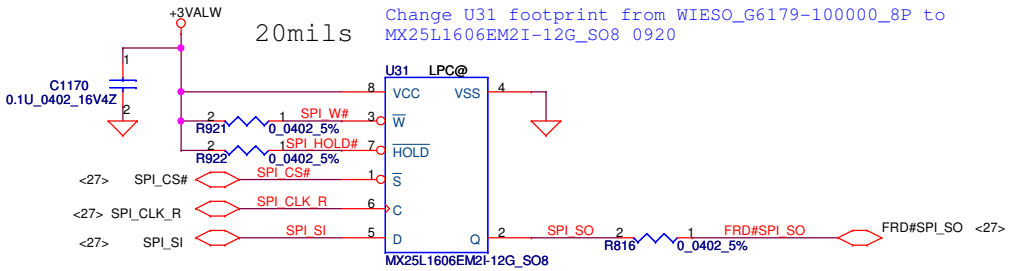
41

SPI Flash (16Mb*1)

FOR EC 16M SPI ROM

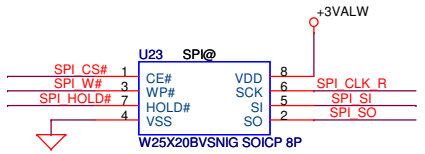
Change U31 P/N from SA00000XT00 to SA000041N00 0915

Change U31 footprint from WIESO_G6179-100000_8P to MX25L1606EM2I-12G_SO8 0920



FOR EC 256K SPI ROM (NONShare ROM)

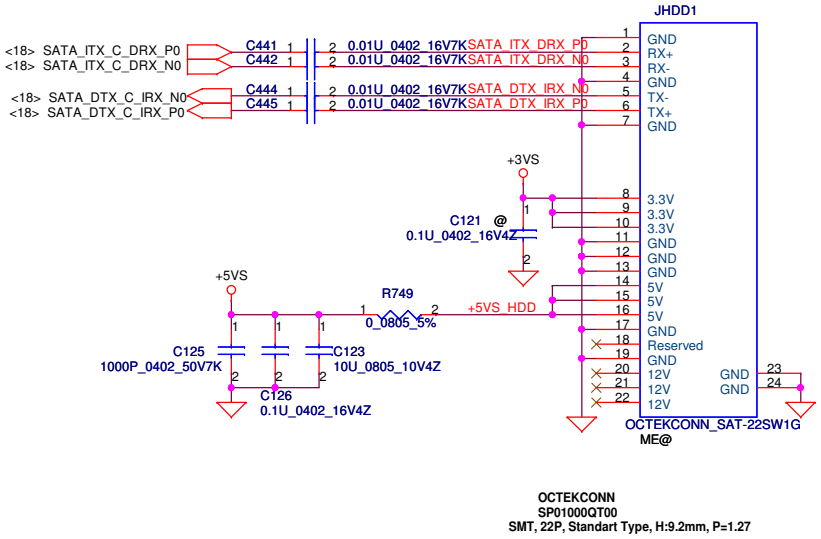
2010/09/24 Add U23 for NONShare SPI ROM.



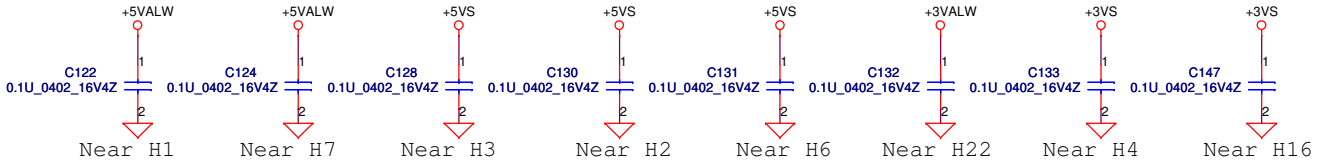
SA00003GM10

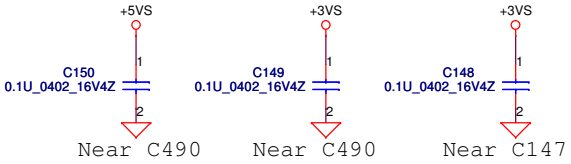
256kB(NAU00 2nd)

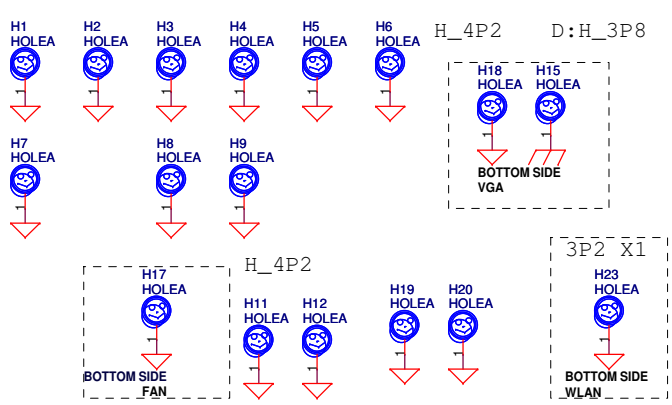
SATA HDD Conn.

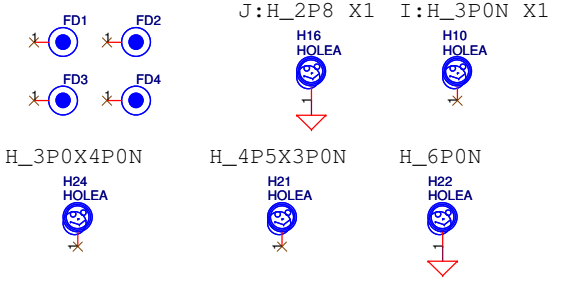


OCTEKCONN
SP01000QT00
SMT, 22P, Standart Type, H:9.2mm, P=1.27









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Compal Electronics, Inc.

Title: **HDD / SPI ROM / Hold**

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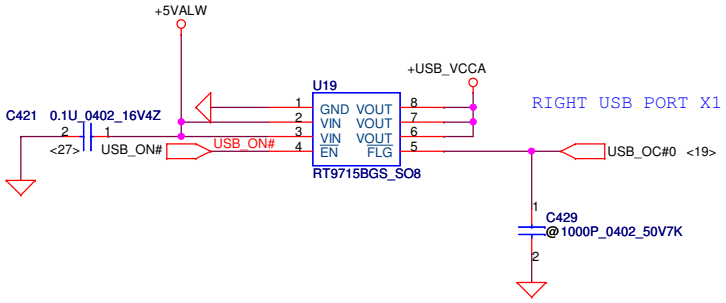
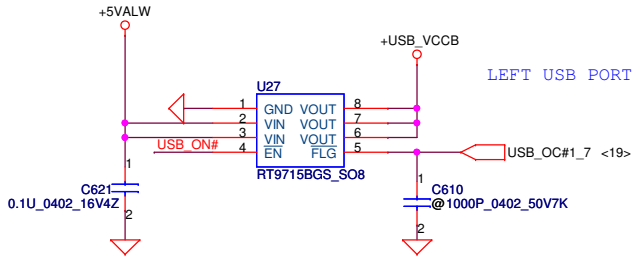
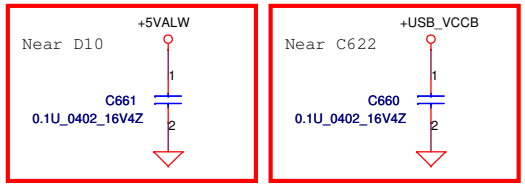
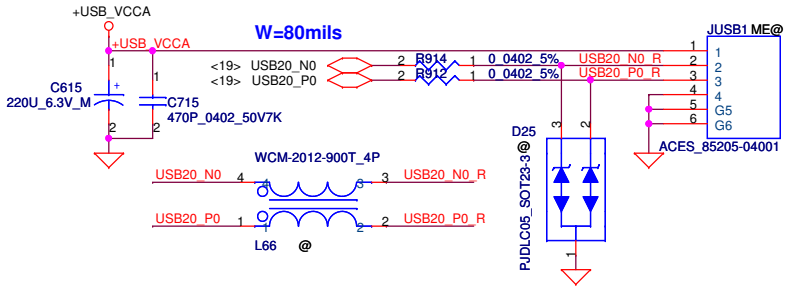
PVT Change U19 and U27 part number from SA000039E00 to SA00002XX00



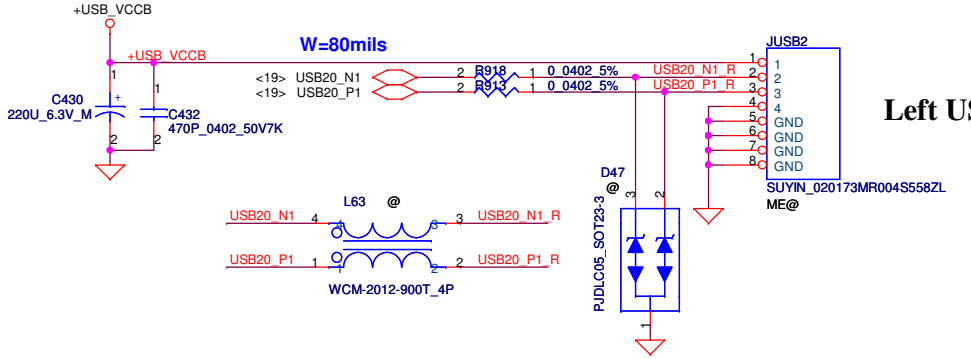


Pre MP ADD for ESD solution



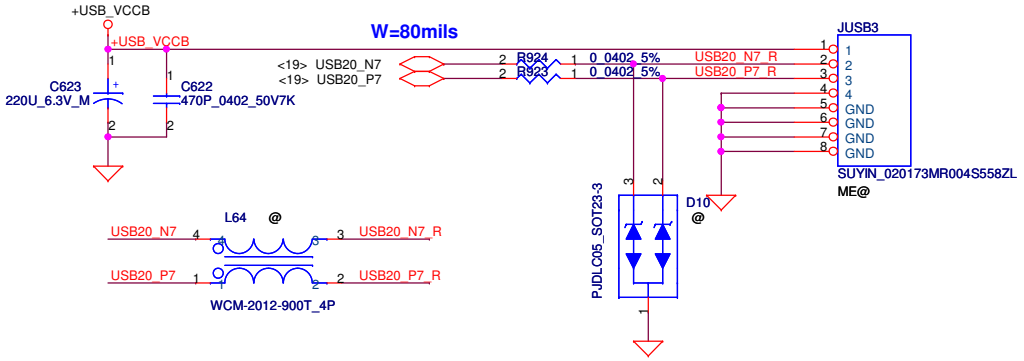


Right USB Conn.



Left USB Conn.

Change JUSB3 connector from ESATA to USB



Left2 USB Conn.

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: USB ports/BT

Size	Document Number	Rev
B	LA7011P	1.0

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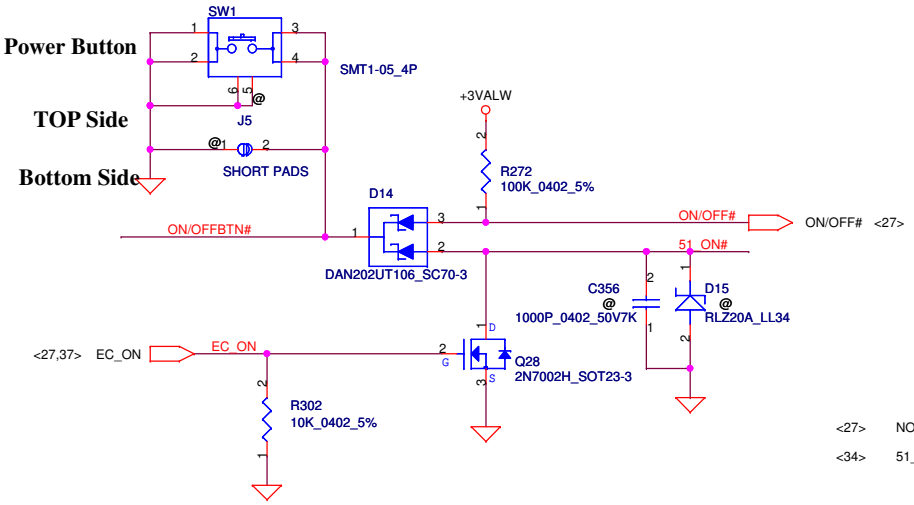
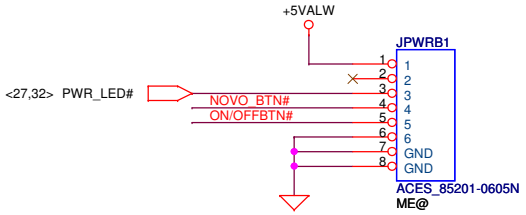
ON/OFF switch

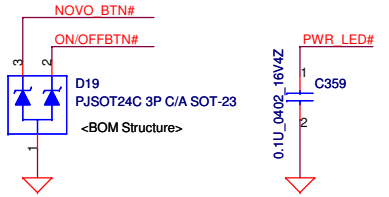


Power Bottom Board Conn. 6pin

10/11 Change JPWRB1 P/N from SP010009O10 to SP01000LB00

Add C359 to PWR_LED# for ESD solution.

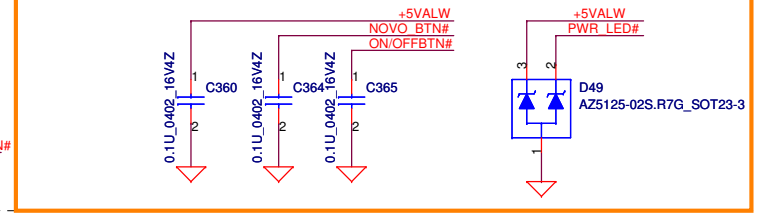


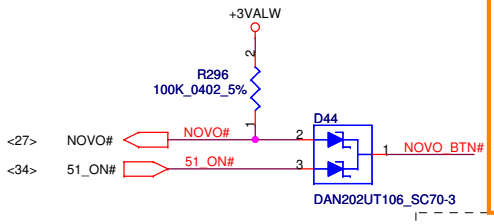


EMI REQUEST 1ST = SCA00000E00

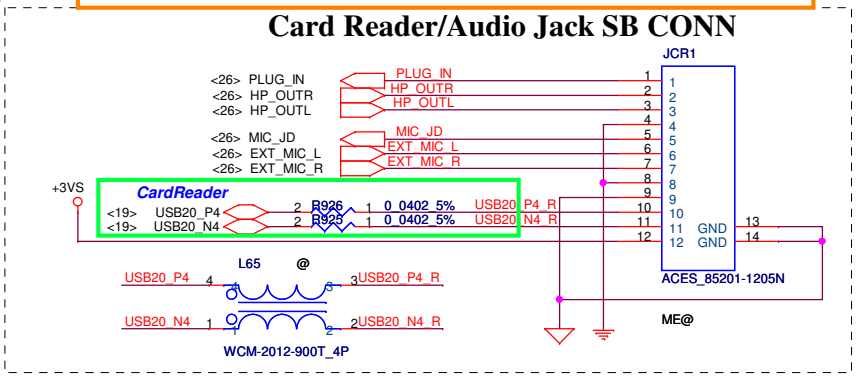
2ST = SCA00000R00

PVT ESD solution.

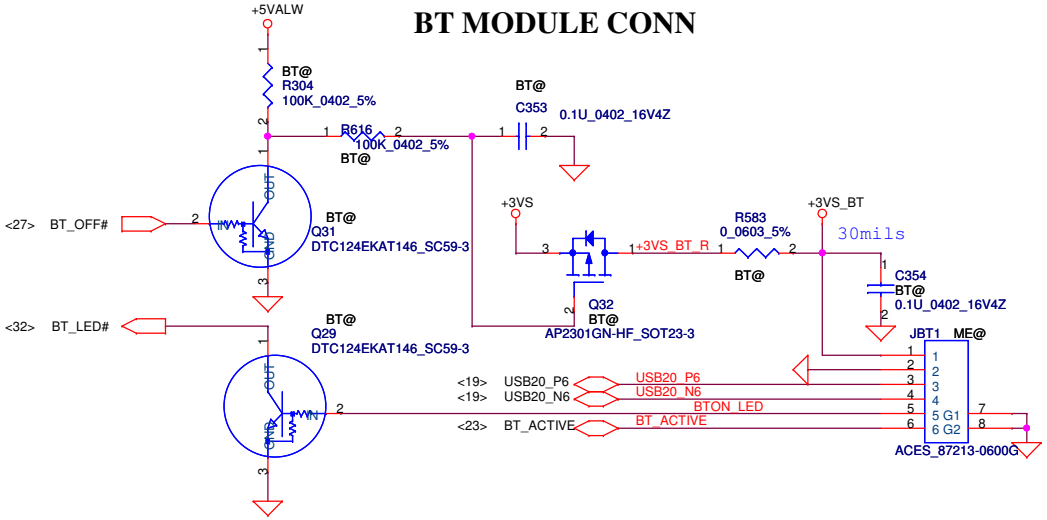


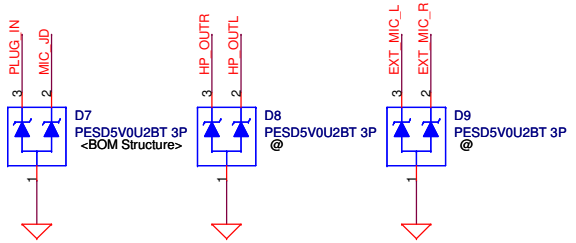


Card Reader/Audio Jack SB CONN



BT MODULE CONN





Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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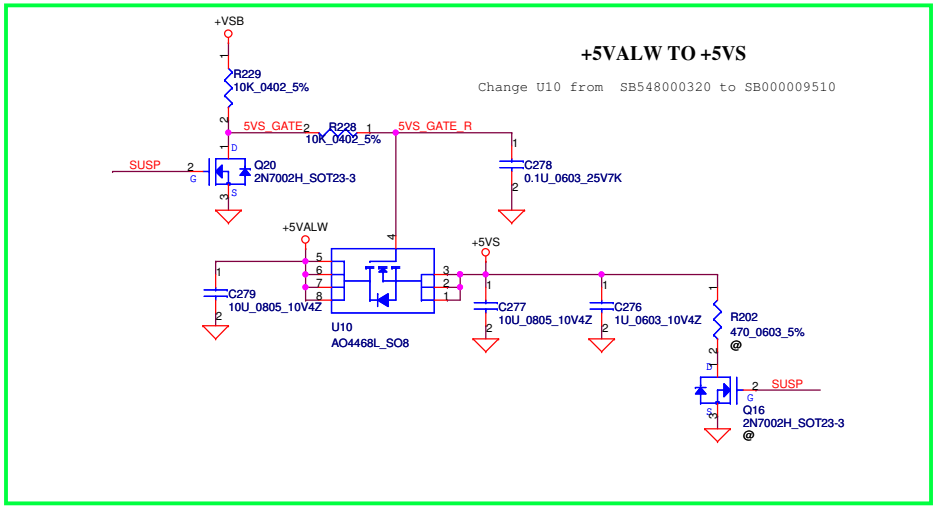
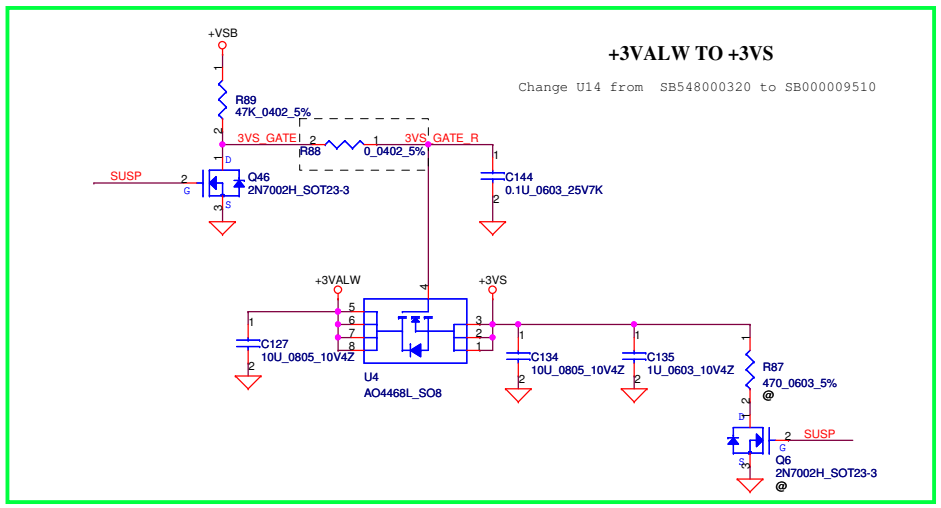
Compal Electronics,Ltd.

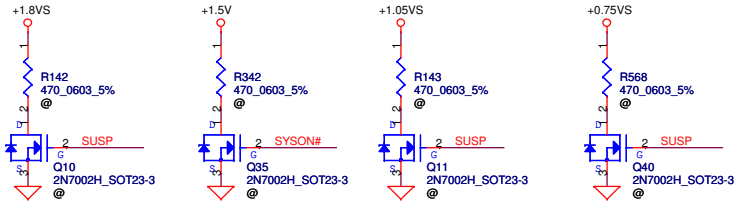
Title: **Audio Jack & SW & BT Conn.**

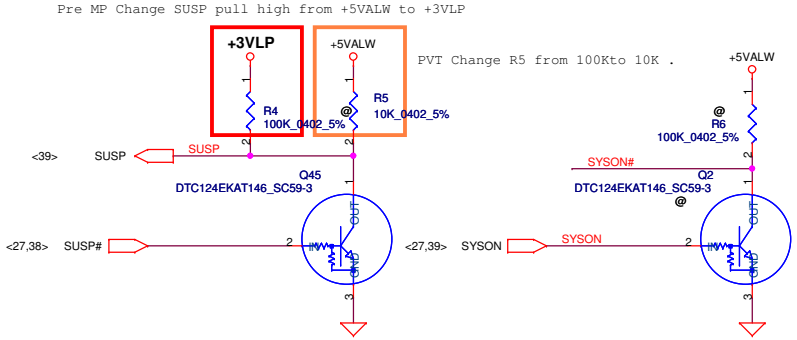
Size	Document Number	Rev
B	LA7011P	1.0

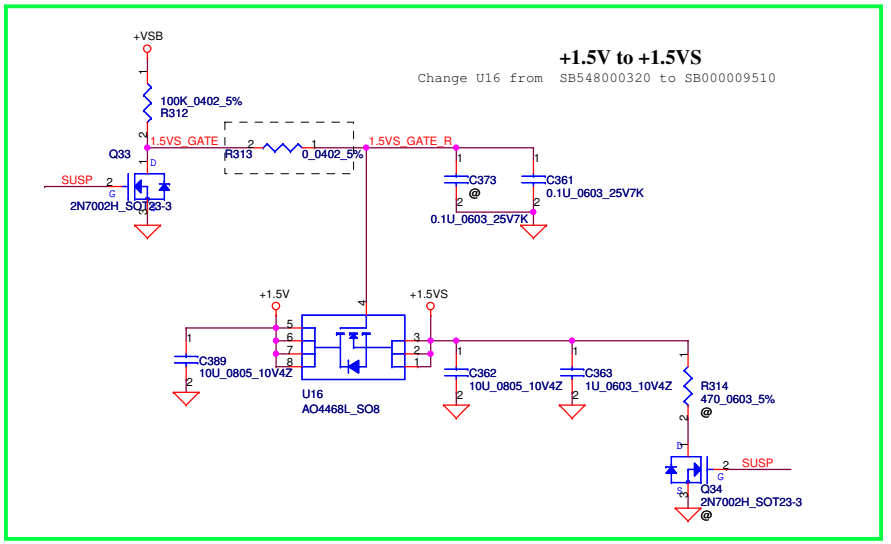
Date: Friday, December 24, 2010 Sheet 30 of 41











Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA7011P	1.0

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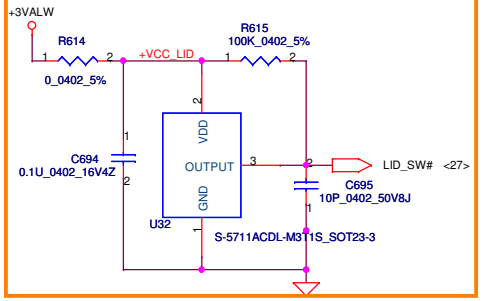
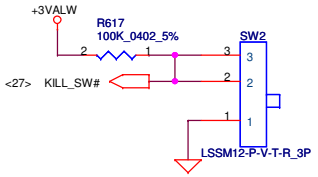
Lid Switch



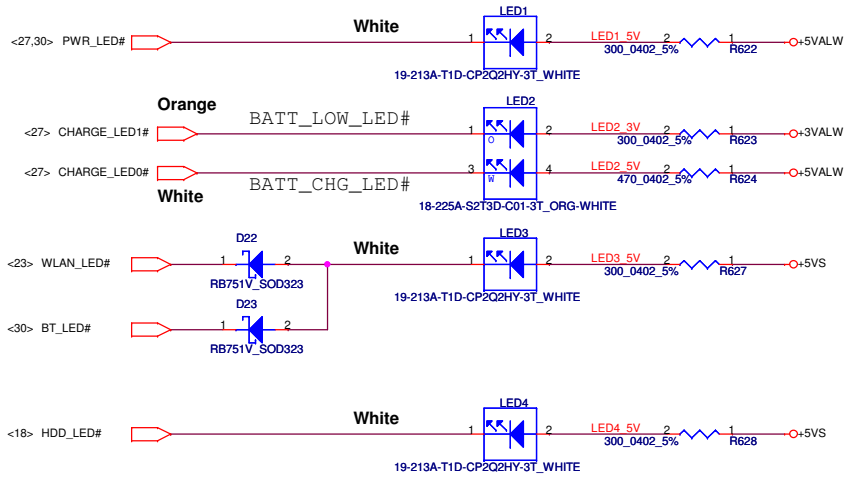
PVT Change U32 part number from SA032120010 to SA000031C00

Kill Switch

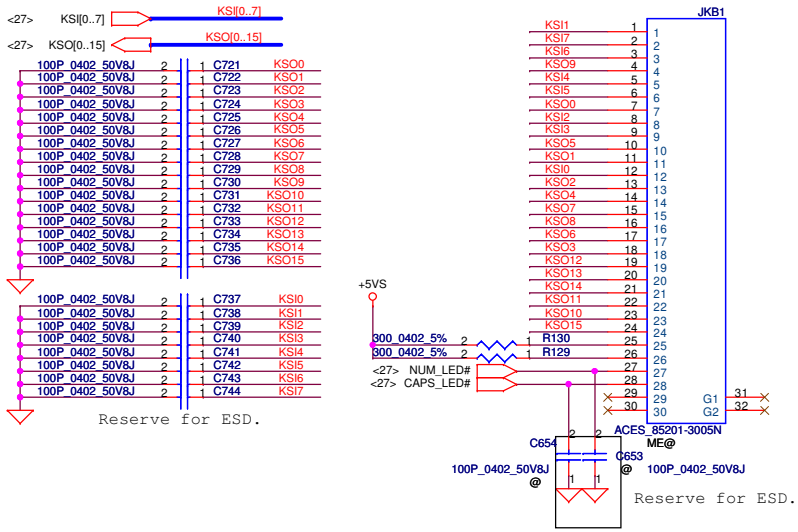
STATUS	
1,2(LOW)	OFF
2,3(HI)	ON



LED



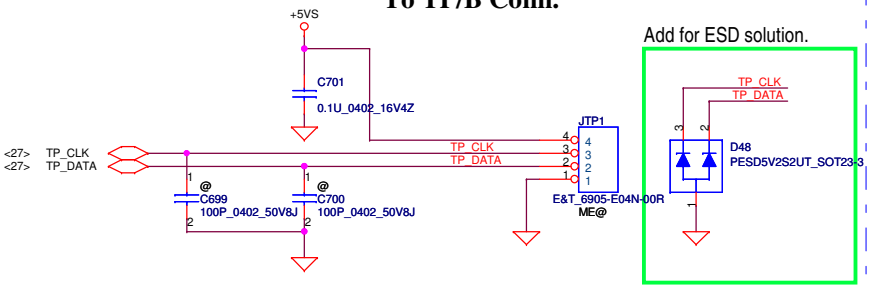
INT_KBD Conn.



check connector & pin define.

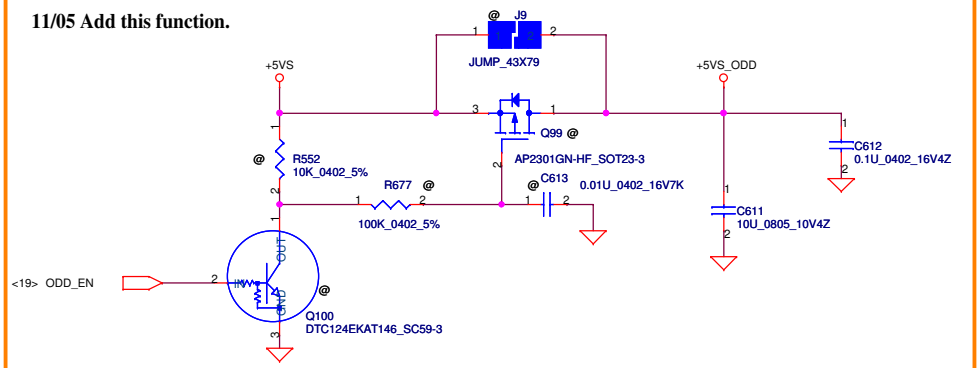
CONN PIN define need double check

To TP/B Conn.

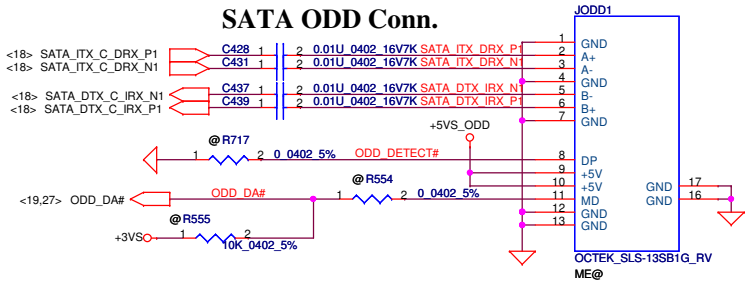


ODD Power Control

11/05 Add this function.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: KB/TP/LID/KLL/ODD/LED FOR 14

Size	Document Number	Rev
Custom	LA7011P	1.0

Date: Friday, December 24, 2010 | Sheet 32 of 41

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
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Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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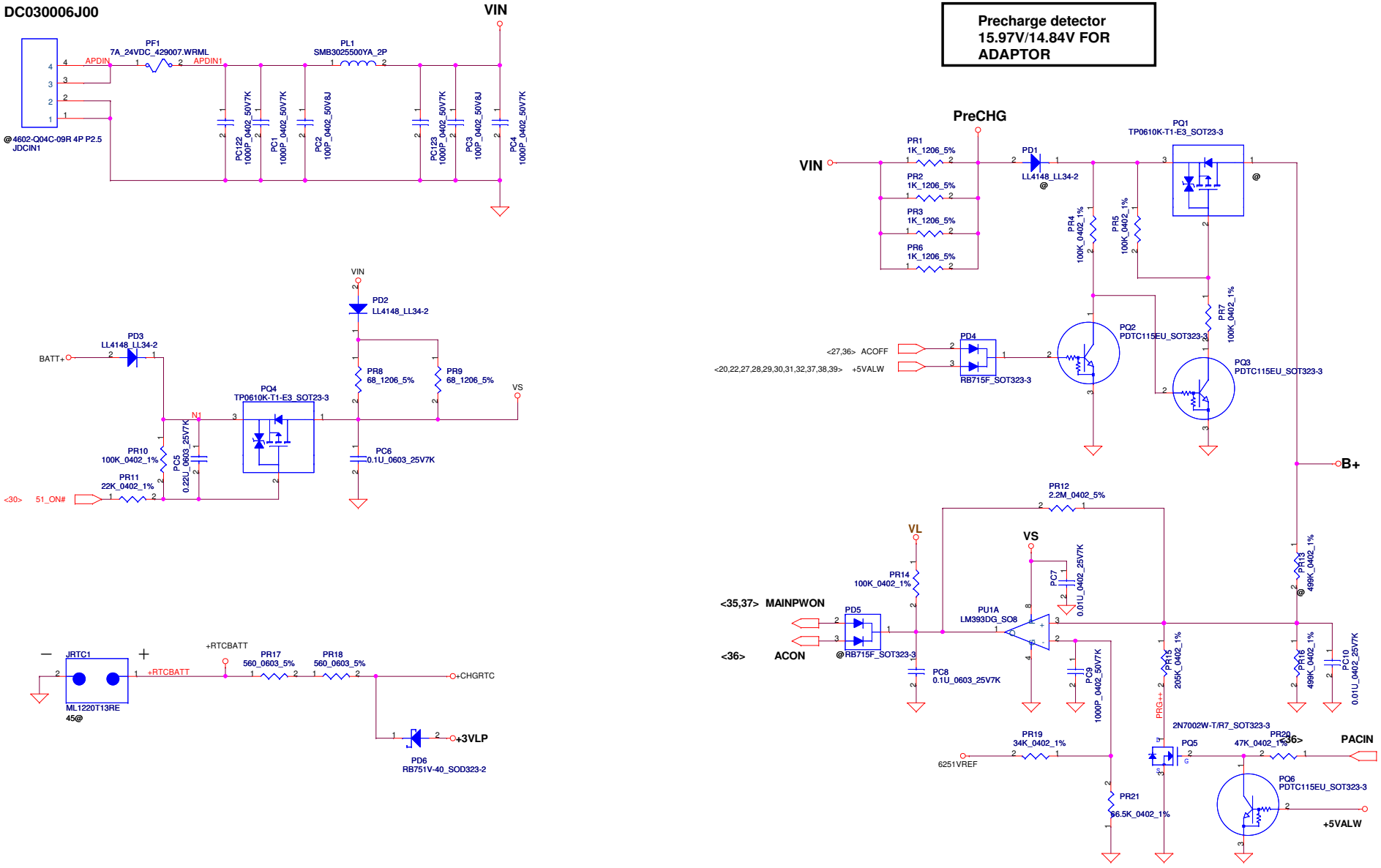
Compal Electronics, Inc.

Title	HW PIR	
Size: Custom	Document Number: LA7011P	Rev: 1.0
Date: Friday, December 24, 2010	Sheet 33 of 41	

DC030006J00

Precharge detector
15.97V/14.84V FOR
ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: ***DCIN / Vin Detector /Pre-charge***

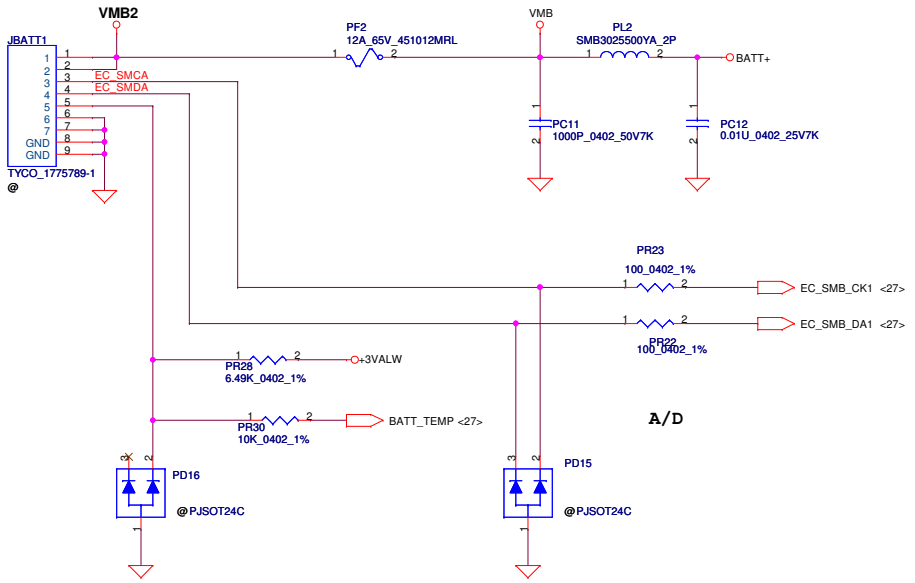
Size	Document Number	Rev
Custom		1.0

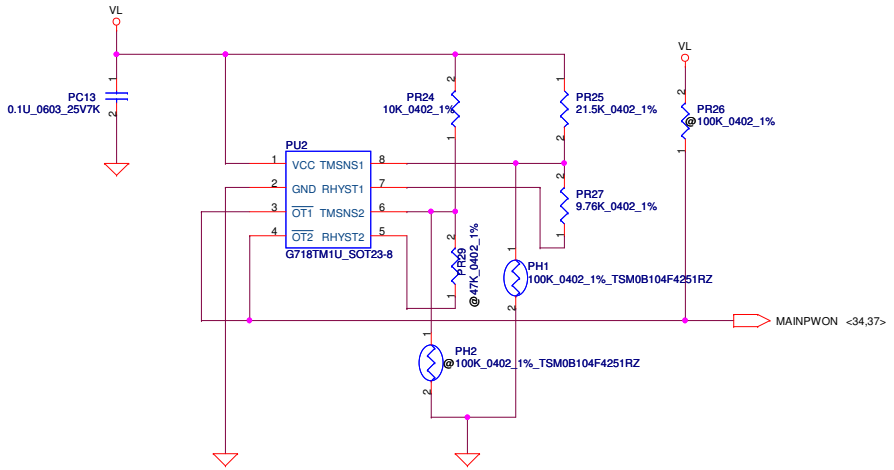
Date: Friday, December 24, 2010 | Sheet 34 of 41

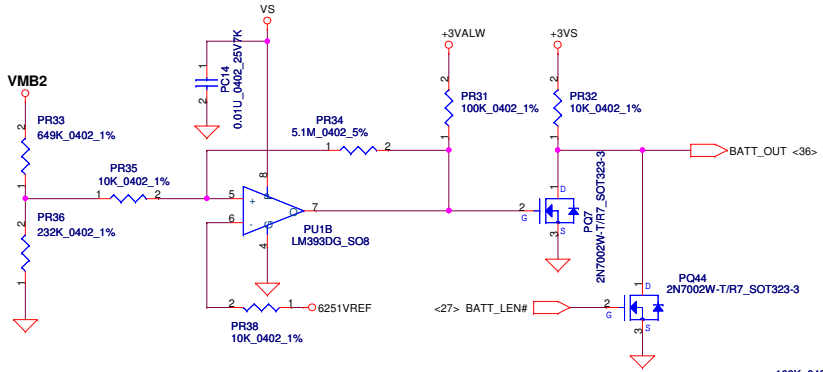
PH1 under CPU botten side :

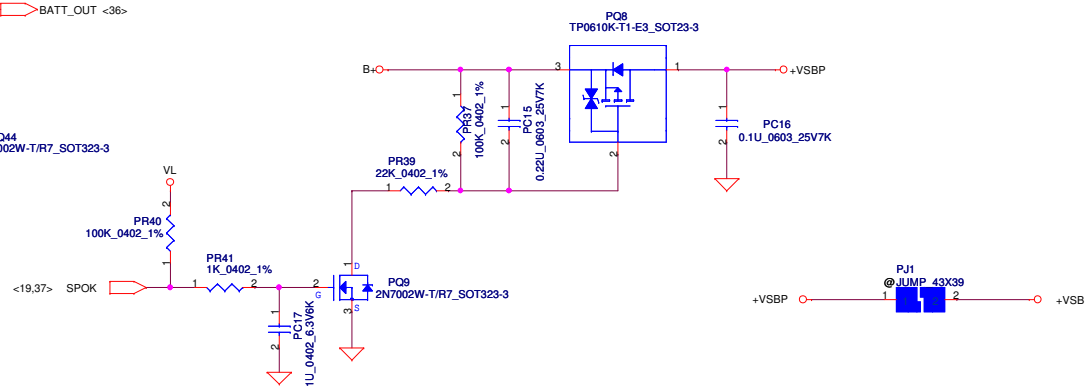
CPU thermal protection at 92 degree C

Recovery at 56 degree C









Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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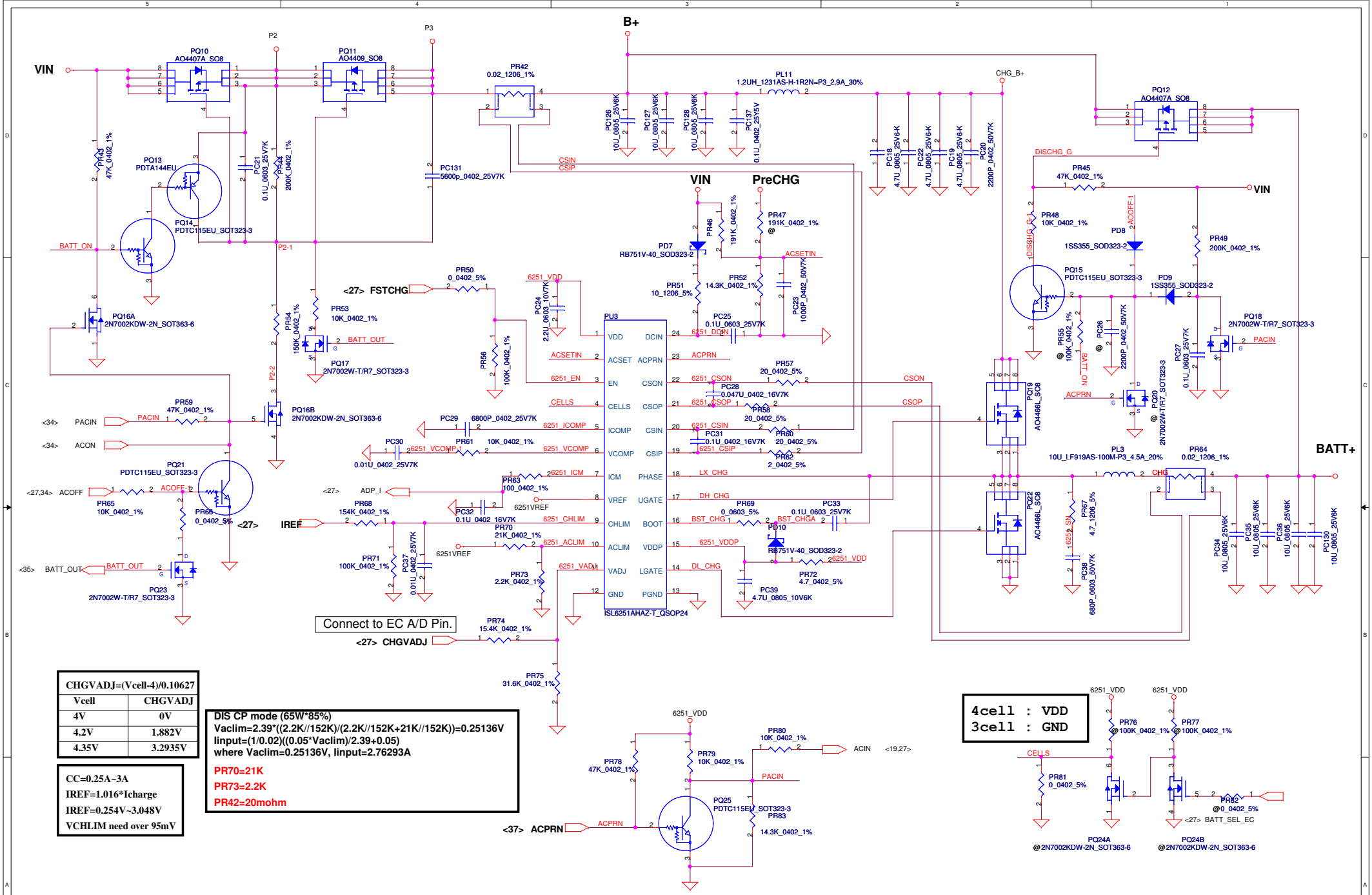
Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size	Document Number	Rev
Custom		1.0

Date: Friday, December 24, 2010 Sheet 35 of 41



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

DIS CP mode (65W*85%)
Vaclim=2.39*((2.2K//152K)/(2.2K//152K+21K//152K))=0.25136V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.25136V, Iinput=2.76293A
PR70=21K
PR73=2.2K
PR42=20mohm

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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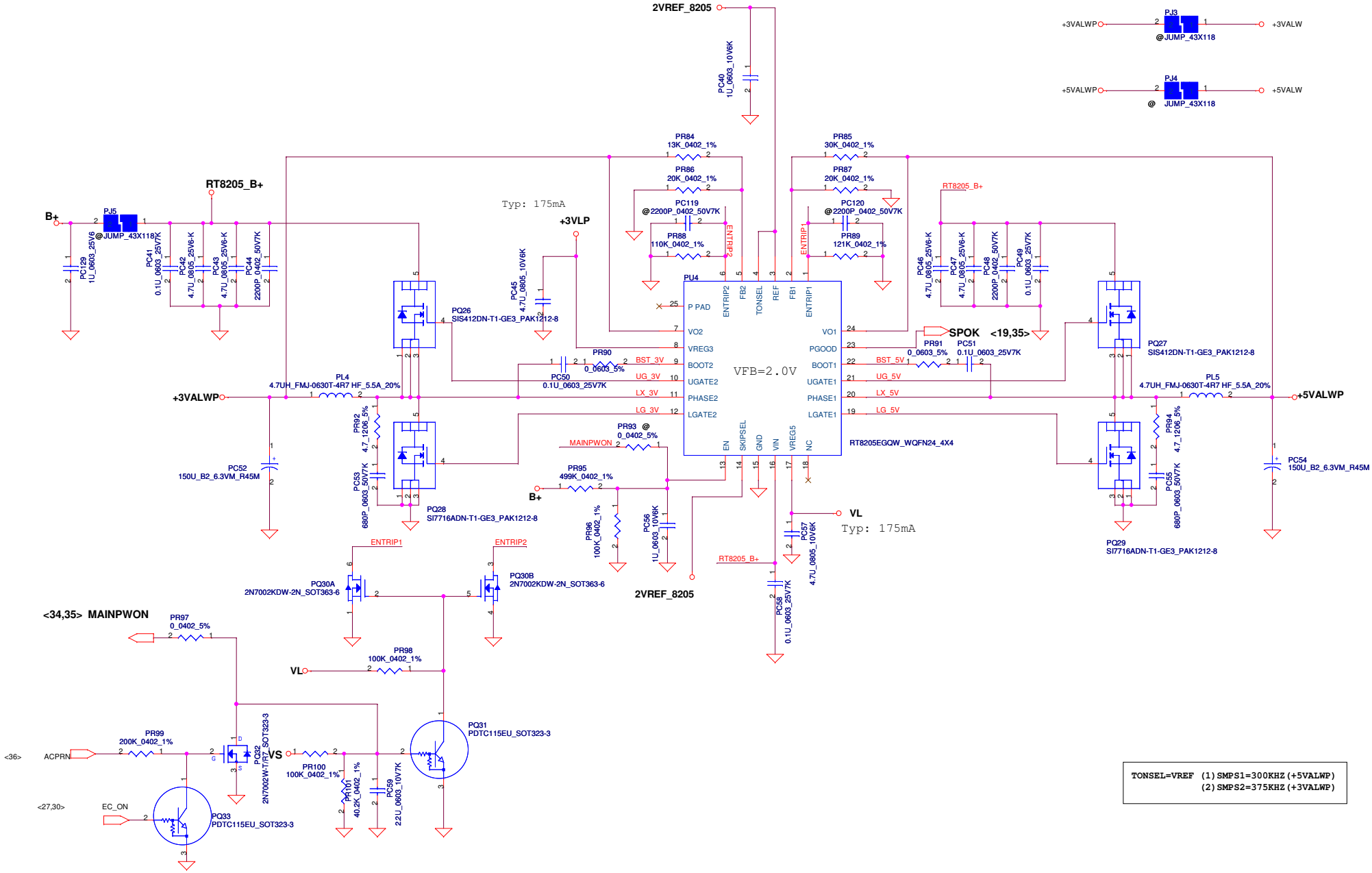
Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 Sheet 36 of 41

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom		1.0

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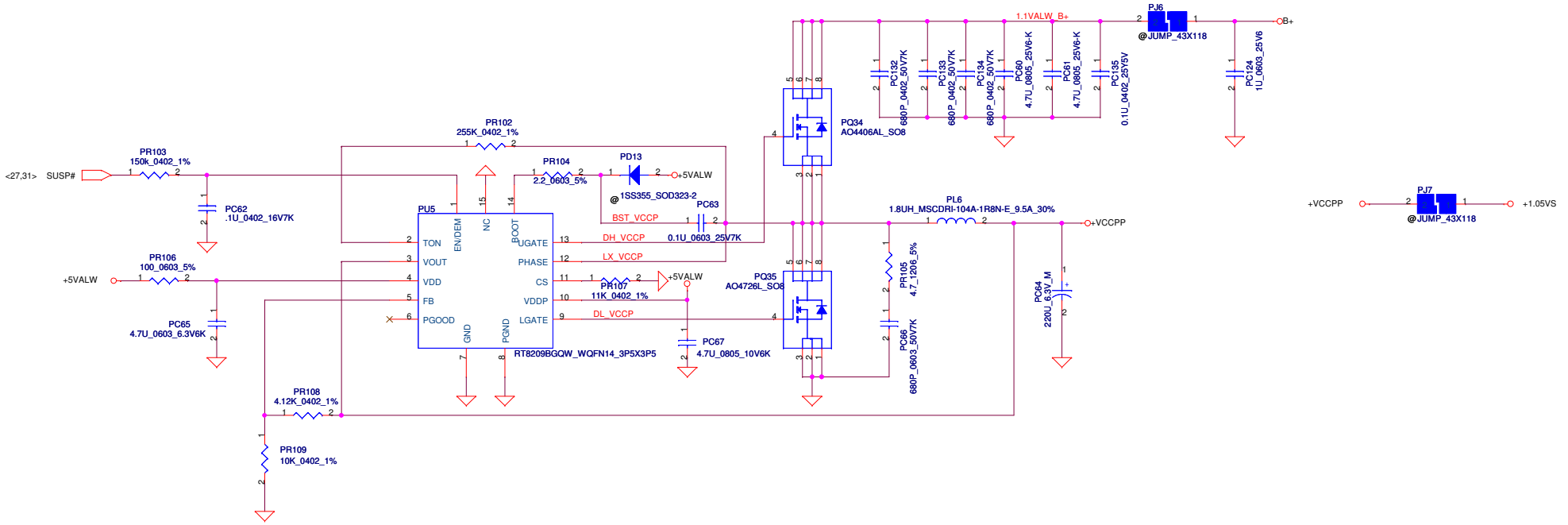

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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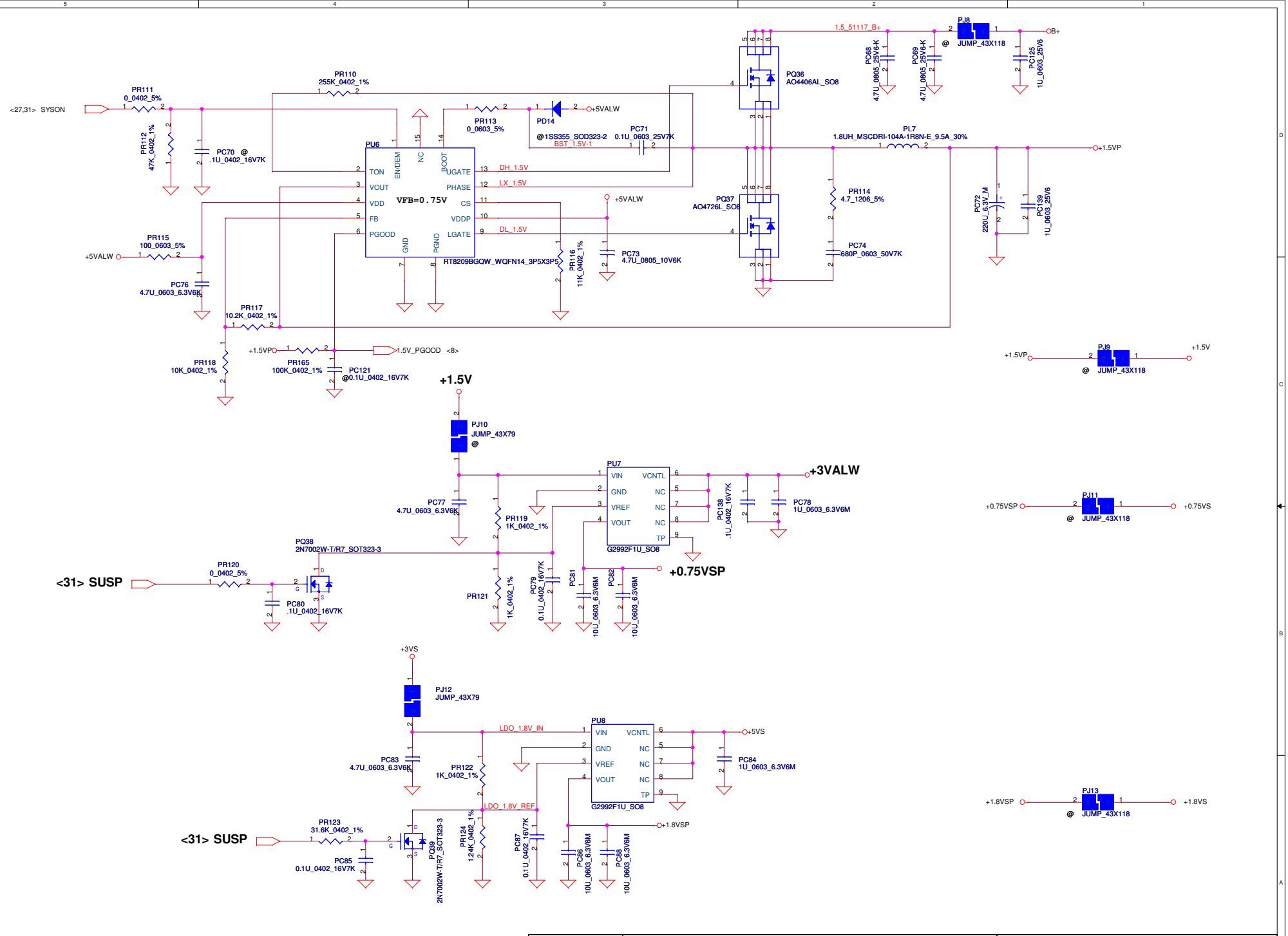
Compal Electronics, Inc.

Title: **VCCP**

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 | Sheet 38 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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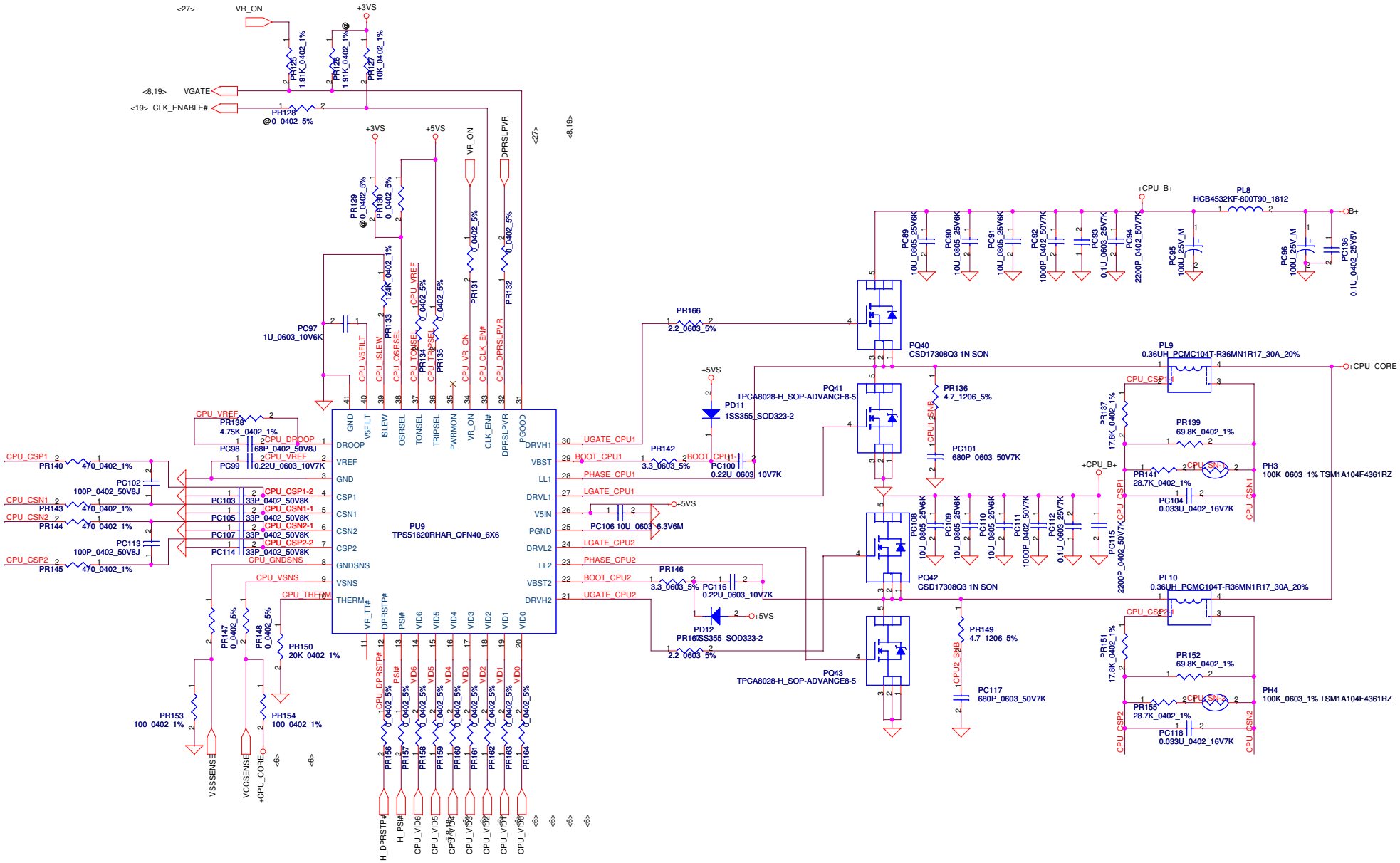
Compal Electronics, Inc.

Title: **1.5VP/1.8VSP/0.75VSP**

Size	Document Number	Rev
		1.0

Date: Friday, December 24, 2010 | Sheet 39 of 41



Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		1.0

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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transitor, the design margin of PQ11 is not enough.	Add PQ44
P39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

Security Classification	Compal Secret Data		
Issued Date	2010/09/10	Deciphered Date	2010/08/19

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Compal Electronics, Inc.

Title: Power PIR

Size: Custom | Document Number: LA7011P | Rev: 1.0

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