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Schematics Document

Intel Huron River Platform
Sandy Bridge (Dual Core BGA 1023) With
Couger Point Core Logic

LA-7401P

2011-03-24

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: Cover Page		
Size: Custom	Document Number	Rev: 1.0
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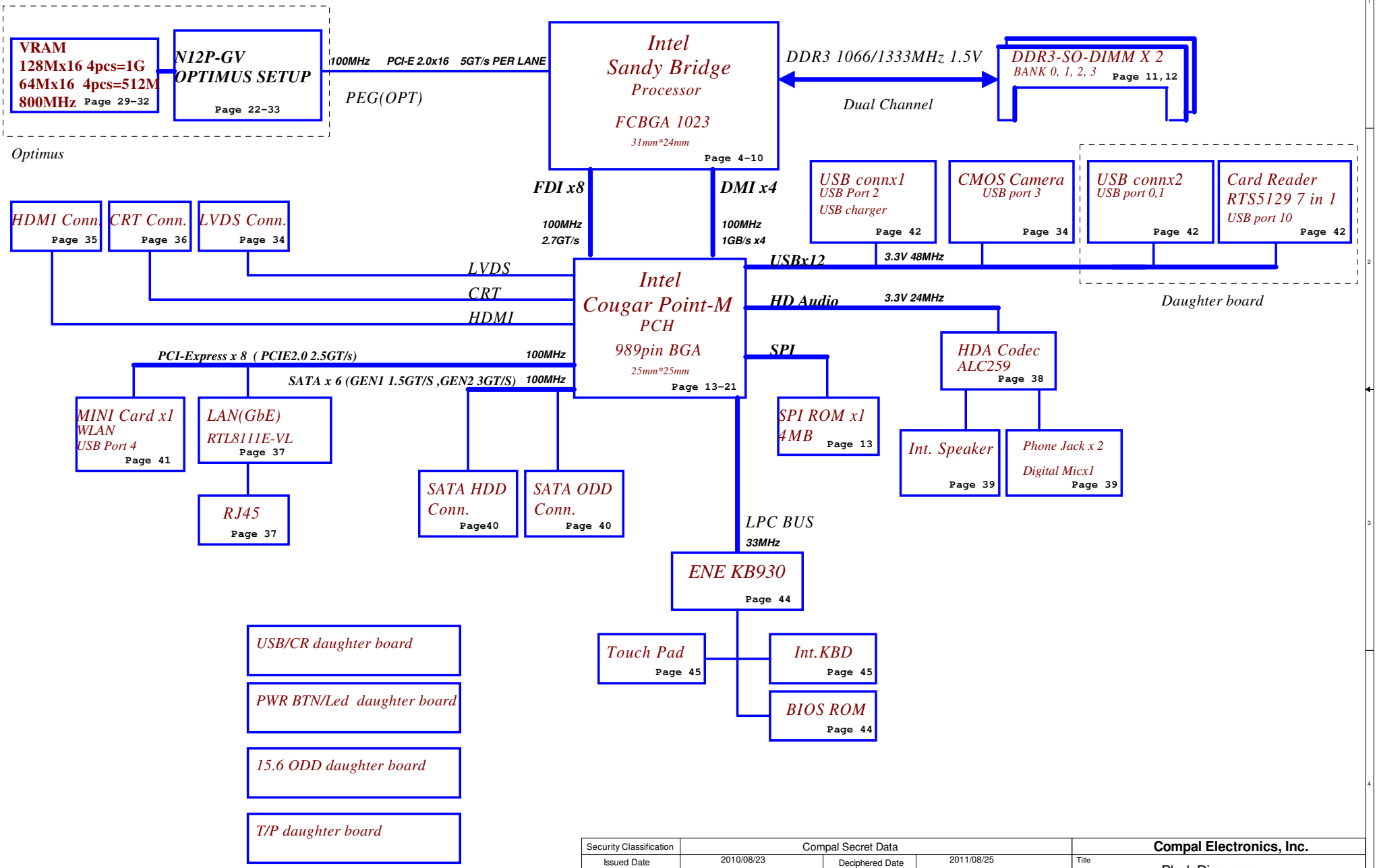
Model Name : PAJ80(14" UMA/Dis)/PAJ90(15.6" UMA/Dis)
File Name : LA-7401P



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Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: Block Diagrams

Size	Document Number	Rev
Custom	LA-7401P	1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_DGPU	+1.05VS to +1.05VS_DGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS	+VCCPP to +1.05VS switched power rail for CPU,PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+VRAM_1.5VS	+1.5V to +VRAM_1.5VS power rail for GPU	ON	OFF	OFF
+1.8VS	+5VALW to 1.8VS switched power rail to CPU,PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	CONN
		1	CONN
	UHCI1	2	CONN
		3	Camera
	UHCI2	4	Mini Card(WLAN/BT)
		5	NA
	UHCI3	6	
		7	
EHCI2	UHCI4	8	NA
		9	NA
	UHCI5	10	Card Reader
		11	
	UHCI6	12	
		13	

BTO Option Table

BTO Item	BOM Structure
Optimus	OPT@
Connector	CONN@
Unpop	@
14" PCB	14@
15.6" PCB	15@
UMA PCB	UMA@
Dis PCB (Optimus)	OPT@
X76 512M	512M@
X76 1G	1G@

2410M mean 2.3G CPU 2540M mean 2.6G CPU 2520M mean 2.5G CPU 2310M mean 2.2G CPU 2620M mean 2.7G CPU 2330M mean 2.2G CPU PCH R3 GPU R3

U2 2410MR3@ 2410M CPU
U2 2540MR3@ 2540M CPU
U2 2520MR3@ 2520M CPU
U2 2310MR3@ 2310M CPU
U2 2620MR3@ 2620M CPU
U14 PCHR3@ PCH B3
UV1 GPUR3@ GPU

U2 2410MR1@ 2410M CPU
U2 2540MR1@ 2540M CPU
U2 2520MR1@ 2520M CPU
U2 2310MR1@ 2310M CPU
U2 2620MR1@ 2620M CPU
U2 2330M@ 2330M CPU
U14 PCHR1@ PCH B3
UV1 GPUR1@ GPU

PCB DAZ
ZZZ1
PCB_LA-7401P

X7613432L03
ZZZ3
X76-VRAM
1G@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1110 b

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0 SODIMM 1	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	PCH	GPU
EC_SMB_CK1 EC_SMB_DA1	KB930	V							
EC_SMB_CK2 EC_SMB_DA2	KB930							V	V
PCH_LCD_CLK PCH_LCD_DATA	PCH					V			
SDVO_SCLK SDVO_SDATA	PCH						V		
PCH_SMBCLK PCH_SMBDATA	PCH			V	V				

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Title: Notes List

Size: Custom | Document Number | Rev: 1.0

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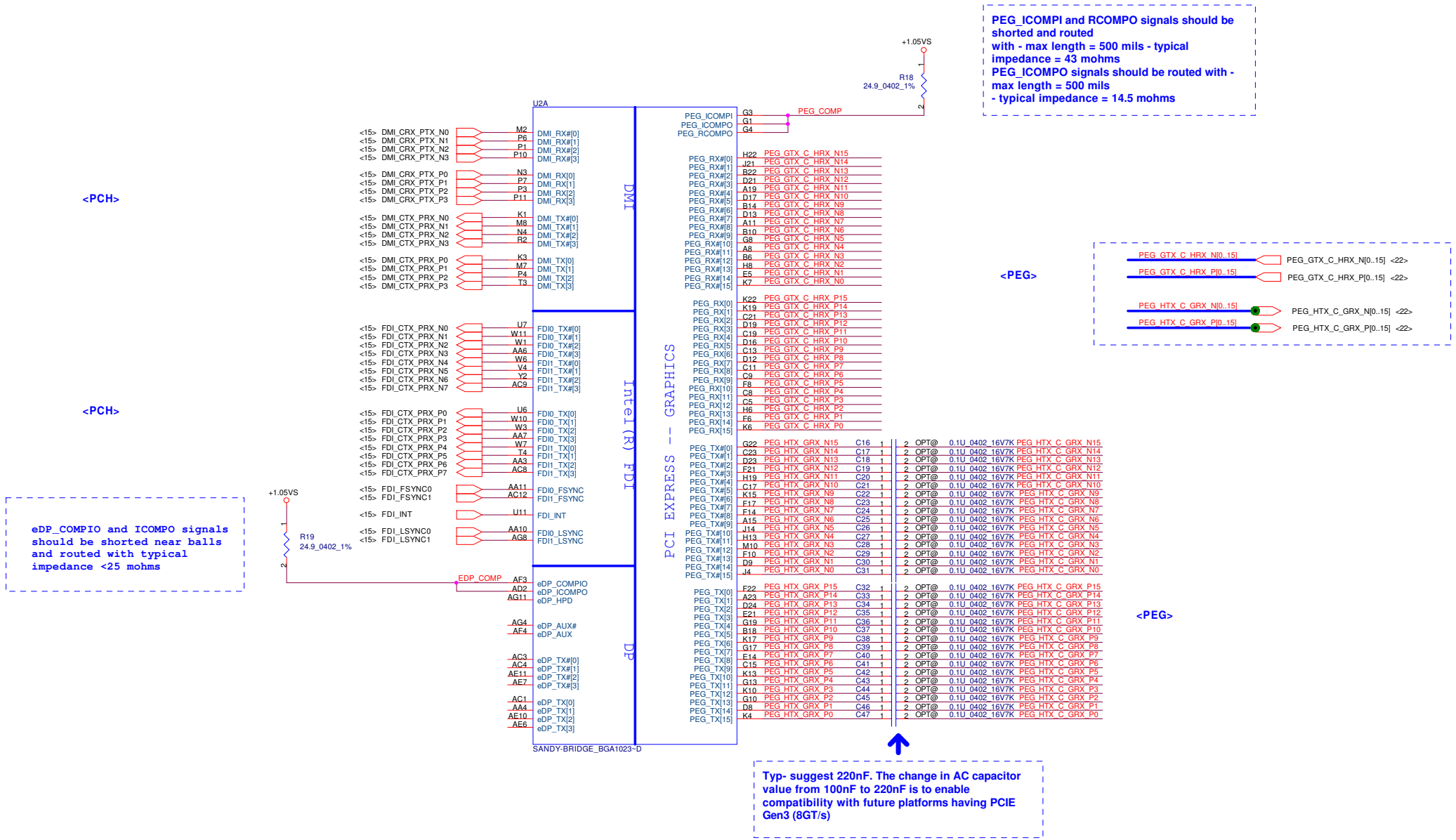

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom		1.0

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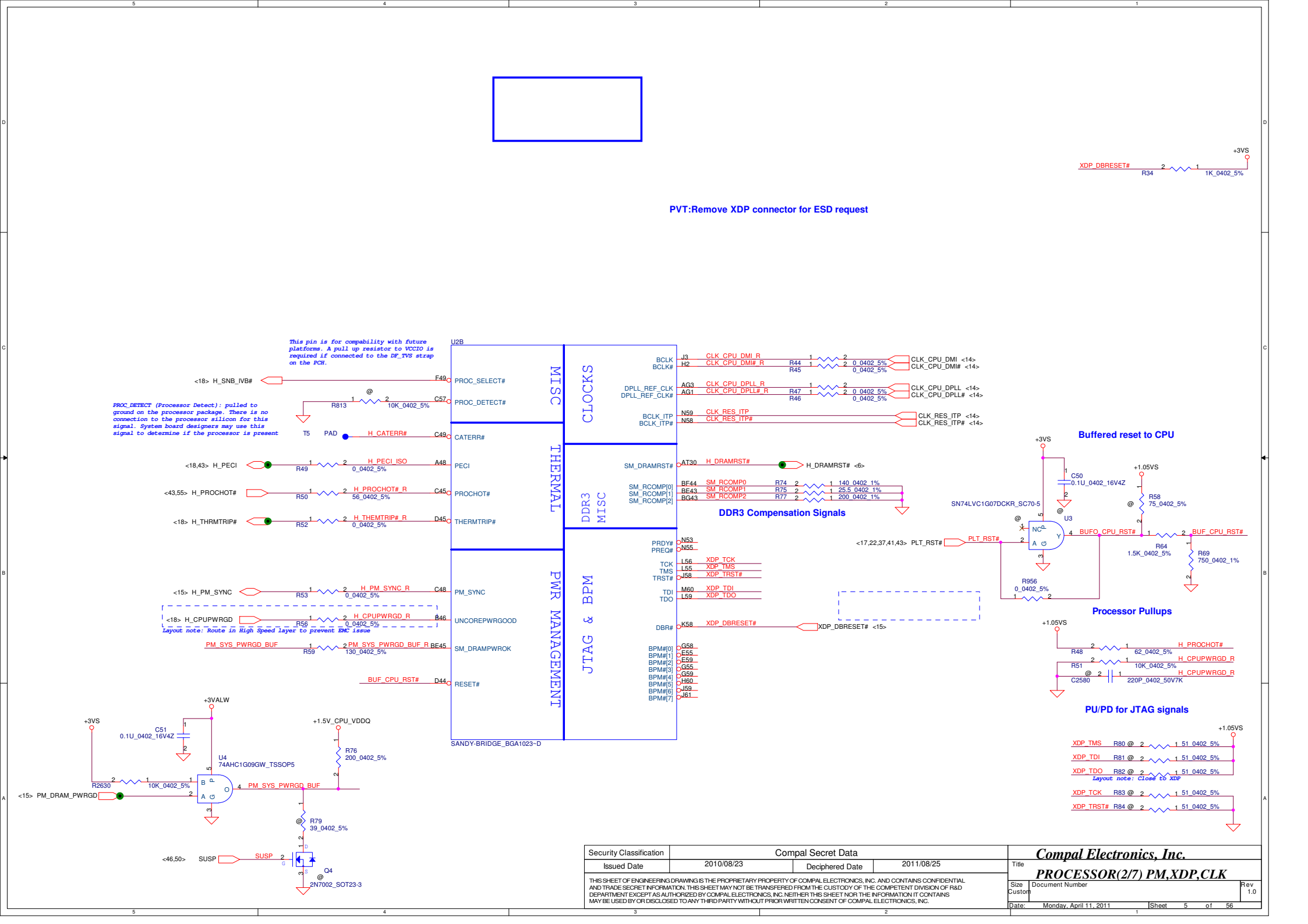

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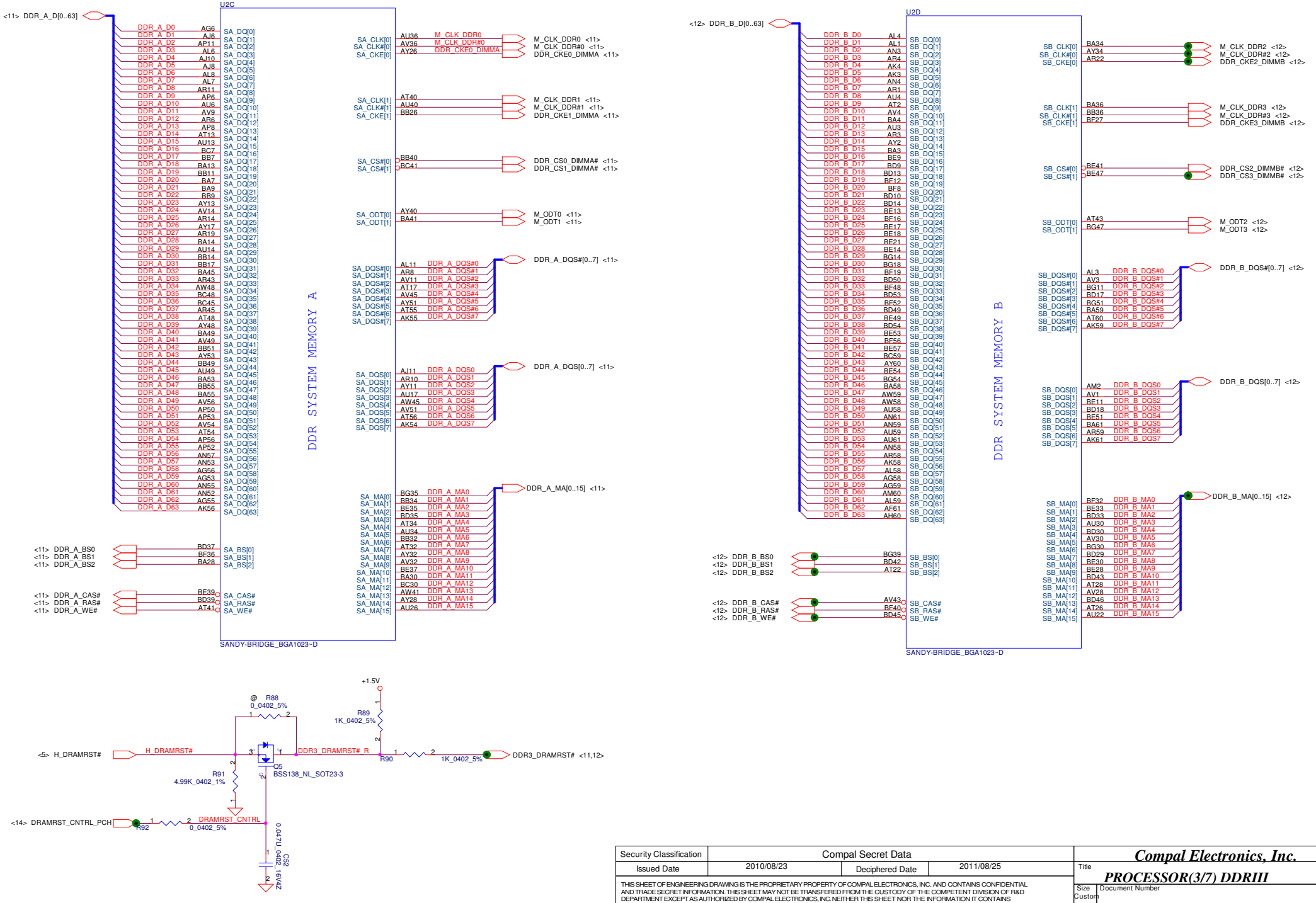
Compal Electronics, Inc.			
Title	PROCESSOR(2/7) PM,XDP,CLK		
Size	Custom	Document Number	Rev 1.0
Date:	Monday, April 11, 2011	Sheet	5 of 56



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
Custom		1.0

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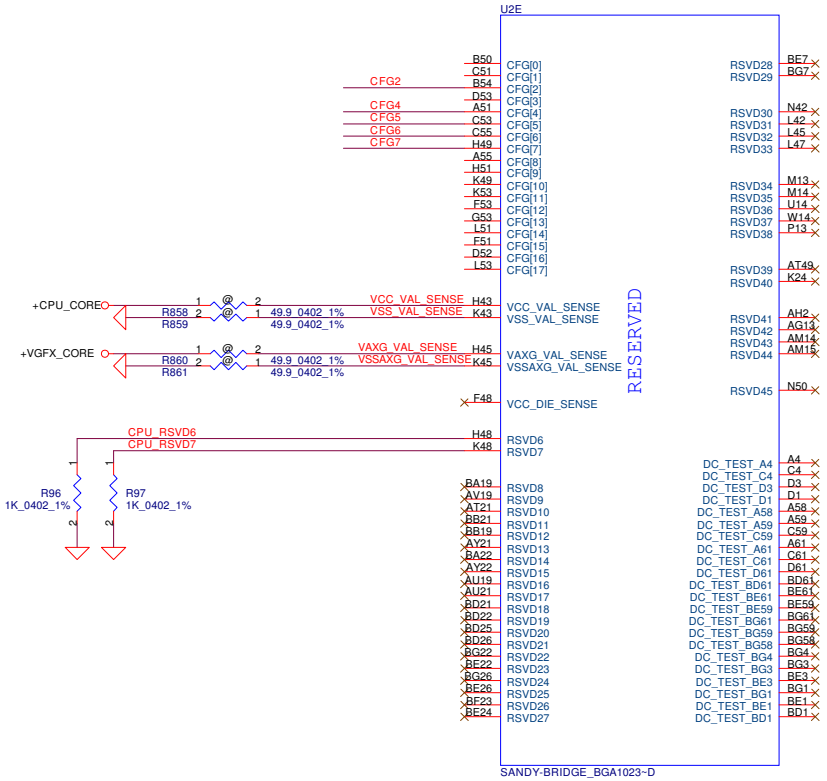
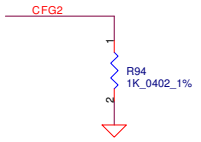
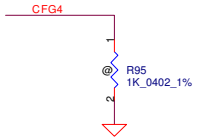
CFG Straps for Processor

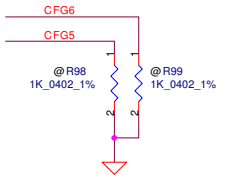




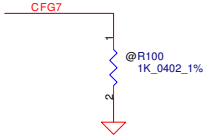
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: **PROCESSOR(4/7) RSVD,CFG**

Size	Document Number	Rev
Custom		1.0

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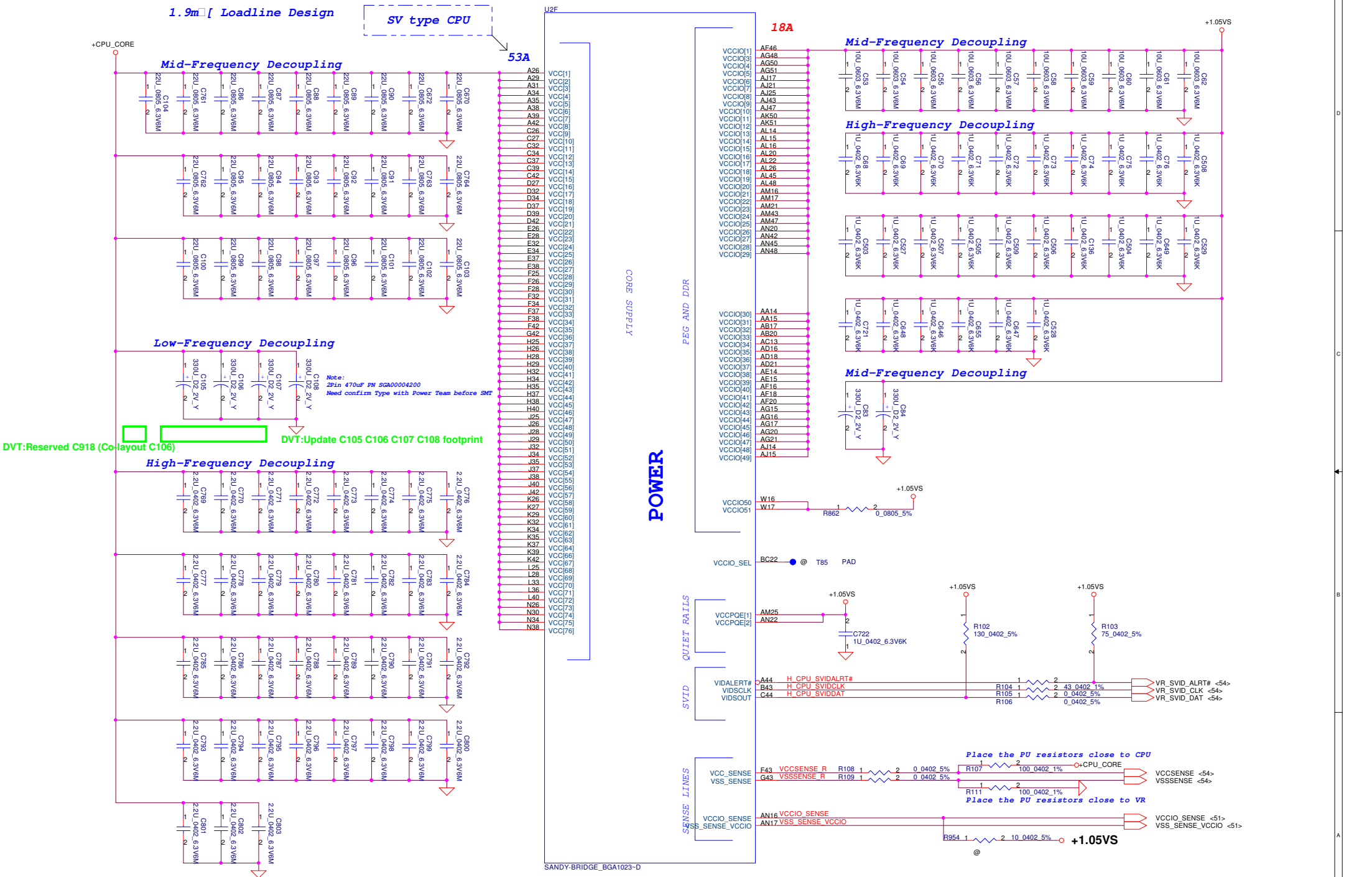

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom		1.0

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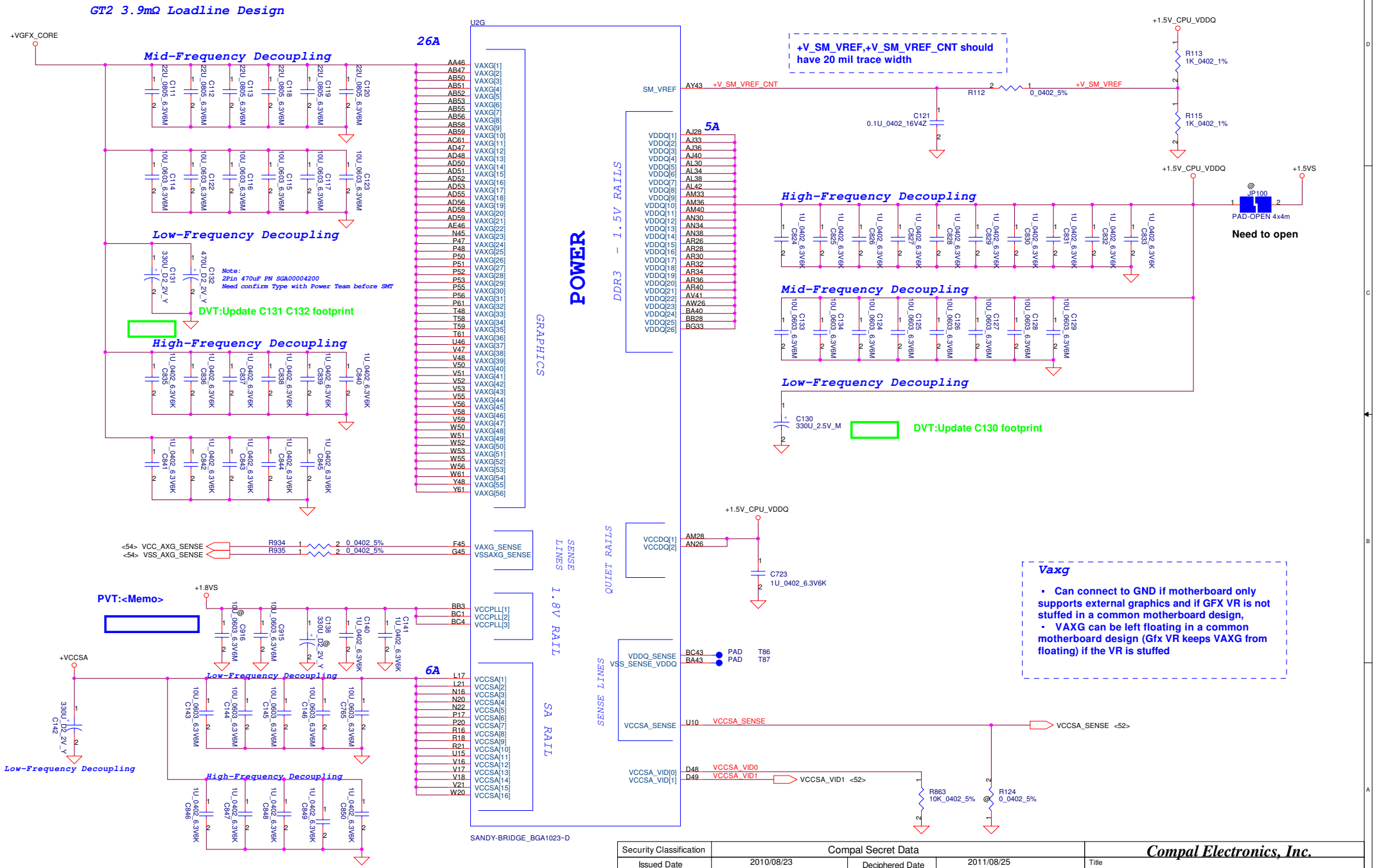

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Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number | Rev: 1.0

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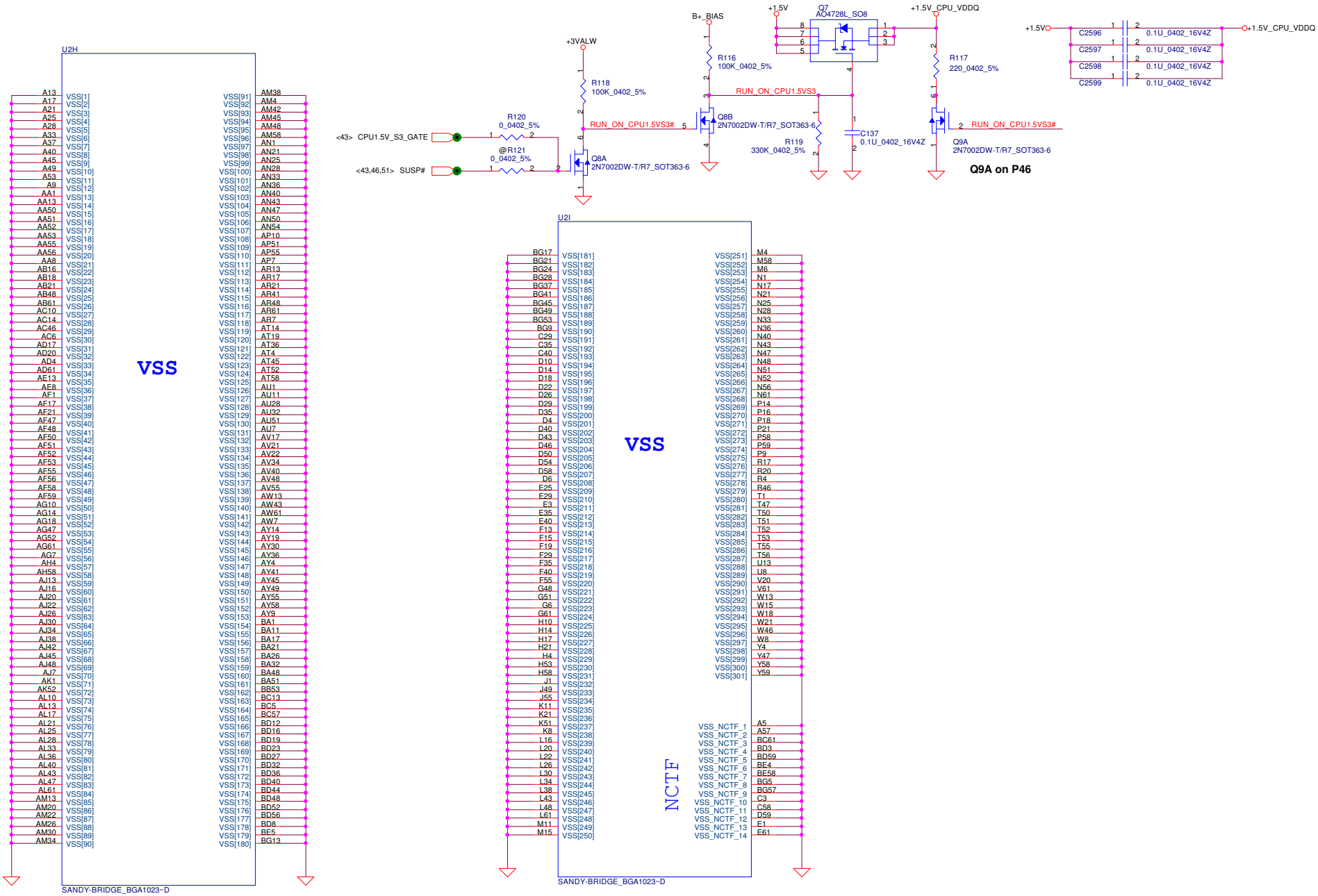
+1.5V_CPU_VDDQ Source



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Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: **PROCESSOR(7/7) VSS**

Size	Document Number	Rev
Custom		1.0

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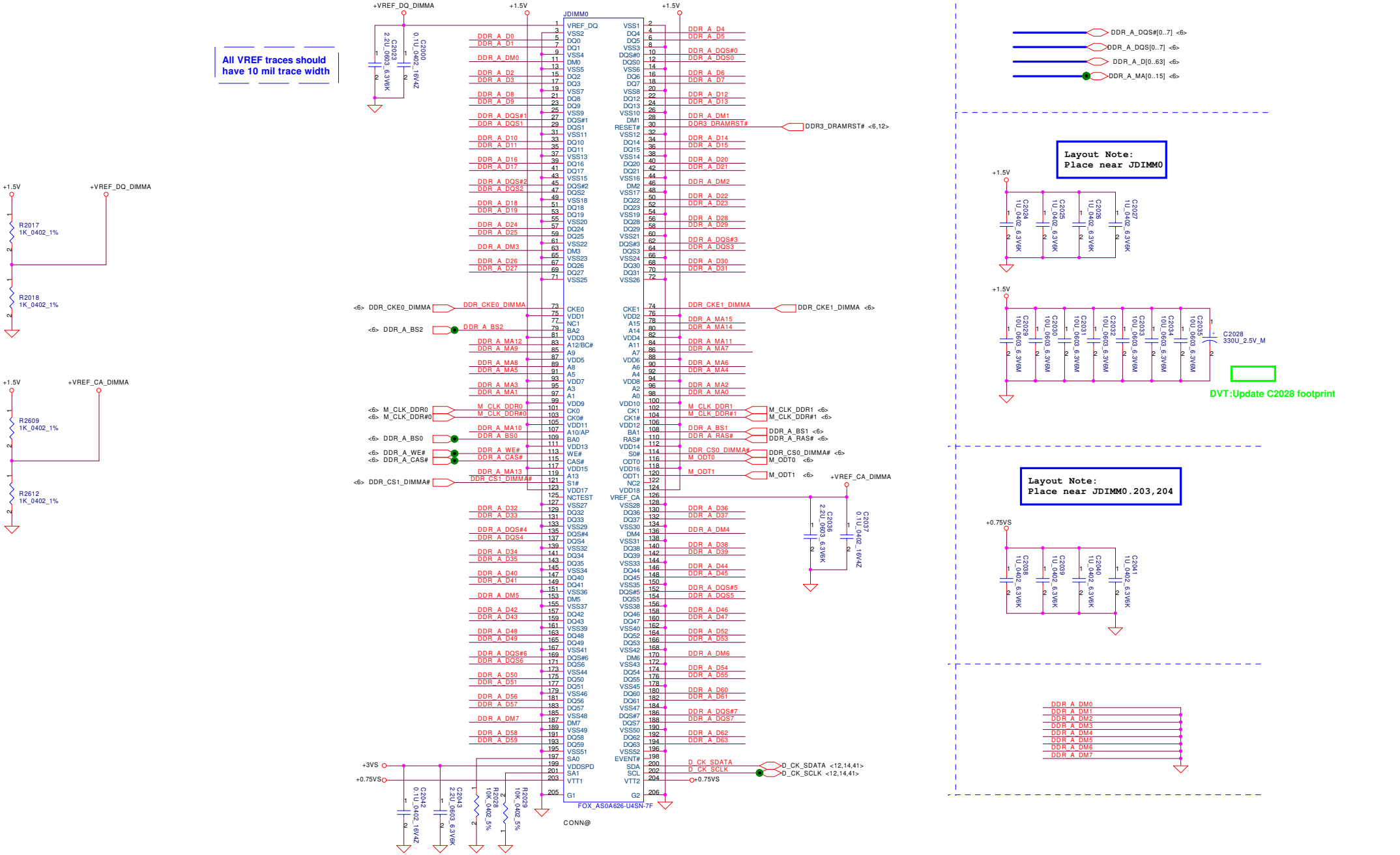
All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM0

DVT:Update C2028 footprint

Layout Note:
Place near JDIMM0.203,204

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: **DDRIII DIMMA**

Size	Document Number	Rev
Custom	LA-7141P	1.0

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All VREF traces should have 10 mil trace width

+1.5V
+VREF_DQ_DIMMB
R165 1K_0402_1%
R166 1K_0402_1%
C165 2.2U_0603_6.3V6K
C166 0.1U_0402_16V4Z

+1.5V
+VREF_CA_DIMMB
R167 1K_0402_1%
R168 1K_0402_1%

JDIMM1

1	VREF_DQ	VSS1	2		
3	VSS2	DQ4	4	DDR_B_D4	
5	DQ0	DQ5	6	DDR_B_D5	
7	DQ1	VSS3	8		
9	VSS4	DQS#0	10	DDR_B_DQS#0	
11	DM0	DQS0	12	DDR_B_DQS0	
13	VSS5	VSS6	14		
15	DQ2	DQ6	16	DDR_B_D6	
17	DQ3	DQ7	18	DDR_B_D7	
19	VSS7	VSS8	20		
21	DQ8	DQ12	22	DDR_B_D12	
23	DQ9	DQ13	24	DDR_B_D13	
25	VSS9	VSS10	26		
27	DQS#1	DM1	28	DDR_B_DM1	
29	DQS1	RESET#	30	DDR3_DRAMRST#	DDR3_DRAMRST# <6,11>
31	VSS11	VSS12	32		
33	DQ10	DQ14	34	DDR_B_D14	
35	DQ11	DQ15	36	DDR_B_D15	
37	VSS13	VSS14	38		
39	DQ16	DQ20	40	DDR_B_D20	
41	DQ17	DQ21	42	DDR_B_D21	
43	VSS15	VSS16	44		
45	DQS#2	DM2	46	DDR_B_DM2	
47	DQS2	VSS17	48		
49	VSS18	DQ22	50	DDR_B_D22	
51	DQ18	DQ23	52	DDR_B_D23	
53	DQ19	VSS19	54		
55	VSS20	DQ28	56	DDR_B_D28	
57	DQ24	DQ29	58	DDR_B_D29	
59	DQ25	VSS21	60		
61	VSS22	DQS#3	62	DDR_B_DQS#3	
63	DM3	DQS3	64	DDR_B_DQS3	
65	VSS23	VSS24	66		
67	DQ26	DQ30	68	DDR_B_D30	
69	DQ27	DQ31	70	DDR_B_D31	
71	VSS25	VSS26	72		
73	CKE0	CKE1	74	DDR_CKE3_DIMMB	DDR_CKE3_DIMMB <6>
75	VDD1	VDD2	76	DDR_B_MA15	
77	NC1	A15	78	DDR_B_MA14	
79	BA2	A14	80		
81	VDD3	VDD4	82	DDR_B_MA11	
83	A12/BC#	A11	84	DDR_B_MA7	
85	A9	A7	86		
87	VDD5	VDD6	88	DDR_B_MA6	
89	A8	A6	90	DDR_B_MA4	
91	A5	A4	92		
93	VDD7	VDD8	94	DDR_B_MA2	
95	A3	A2	96	DDR_B_MA0	
97	A1	A0	98		
99	VDD9	VDD10	100		
101	CK0	CK1	102	M_CLK_DDR3	M_CLK_DDR3 <6>
103	CK0#	CK1#	104	M_CLK_DDR#3	M_CLK_DDR#3 <6>
105	VDD11	VDD12	106		
107	A10/AP	BA1	108	DDR_B_BS1	DDR_B_BS1 <6>
109	BA0	RAS#	110	DDR_B_RAS#	DDR_B_RAS# <6>
111	VDD13	VDD14	112		
113	WE#	S0#	114	DDR_CS2_DIMMB#	DDR_CS2_DIMMB# <6>
115	CAS#	ODT0	116	M_ODT2	M_ODT2 <6>
117	VDD15	VDD16	118		
119	A13	ODT1	120	M_ODT3	M_ODT3 <6>
121	S1#	NC2	122		
123	VDD17	VDD18	124		
125	NCTEST	VREF_CA	126		+VREF_CA_DIMMB
127	VSS27	VSS28	128		
129	DQ32	DQ36	130	DDR_B_D36	
131	DQ33	DQ37	132	DDR_B_D37	
133	VSS29	VSS30	134		
135	DQS#4	DM4	136	DDR_B_DM4	
137	DQS4	VSS31	138		
139	VSS32	DQ38	140	DDR_B_D38	
141	DQ34	DQ39	142	DDR_B_D39	
143	DQ35	VSS33	144		
145	VSS34	DQ44	146	DDR_B_D44	
147	DQ40	DQ45	148	DDR_B_D45	
149	DQ41	VSS35	150		
151	VSS36	DQS#5	152	DDR_B_DQS#5	
153	DM5	DQS5	154	DDR_B_DQS5	
155	VSS37	VSS38	156		
157	DQ42	DQ46	158	DDR_B_D46	
159	DQ43	DQ47	160	DDR_B_D47	
161	VSS39	VSS40	162		
163	DQ48	DQ52	164	DDR_B_D52	
165	DQ49	DQ53	166	DDR_B_D53	
167	VSS41	VSS42	168		
169	DQS#6	DM6	170	DDR_B_DM6	
171	DQS6	VSS43	172		
173	VSS44	DQ54	174	DDR_B_D54	
175	DQ50	DQ55	176	DDR_B_D55	
177	DQ51	VSS45	178		
179	VSS46	DQ60	180	DDR_B_D60	
181	DQ56	DQ61	182	DDR_B_D61	
183	DQ57	VSS47	184		
185	VSS48	DQS#7	186	DDR_B_DQS#7	
187	DM7	DQS7	188	DDR_B_DQS7	
189	VSS49	VSS50	190		
191	DQ58	DQ62	192	DDR_B_D62	
193	DQ59	DQ63	194	DDR_B_D63	
195	VSS51	VSS52	196		
197	SA0	EVENT#	198		
199	VDDSPD	SDA	200	D_CK_SDATA	D_CK_SDATA <11,14,41>
201	SA1	SCL	202	D_CK_SCLK	D_CK_SCLK <11,14,41>
203	VTT1	VTT2	204		+0.75VS
205	G1	G2	206		

FOX_AS0A626-U8SN-7F
CONN@

<6> DDR_CKE2_DIMMB
<6> DDR_B_BS2
<6> M_CLK_DDR2
<6> M_CLK_DDR#2
<6> DDR_B_BS0
<6> DDR_B_WE#
<6> DDR_B_CAS#
<6> DDR_CS3_DIMMB#

+3VS
+0.75VS
R177 10K_0402_5%
R178 10K_0402_5%
C185 0.1U_0402_16V4Z
C186 2.2U_0603_6.3V6K

C183 2.2U_0603_6.3V6K
C184 0.1U_0402_16V4Z

DDR_B_DQS#[0..7] <6>
DDR_B_DQS[0..7] <6>
DDR_B_D[0..63] <6>
DDR_B_MA[0..15] <6>

+1.5V
C167 1U_0402_6.3V6K
C168 1U_0402_6.3V6K
C169 1U_0402_6.3V6K
C170 1U_0402_6.3V6K

Layout Note:
Place near JDIMM1

+1.5V
C171 10U_0603_6.3V6M
C172 10U_0603_6.3V6M
C173 10U_0603_6.3V6M
C174 10U_0603_6.3V6M
C175 10U_0603_6.3V6M
C176 10U_0603_6.3V6M
C177 10U_0603_6.3V6M
C178 330U_2.5V_M @

DVT:Update C178 footprint and SMT memo

Layout Note:
Place near JDIMM1.203,204

+0.75VS
C179 1U_0402_6.3V6K
C180 1U_0402_6.3V6K
C181 1U_0402_6.3V6K
C182 1U_0402_6.3V6K

DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7

Security Classification	Compal Secret Data		
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Title: DDRIII DIMMB

Size	Document Number	Rev
Custom		1.0

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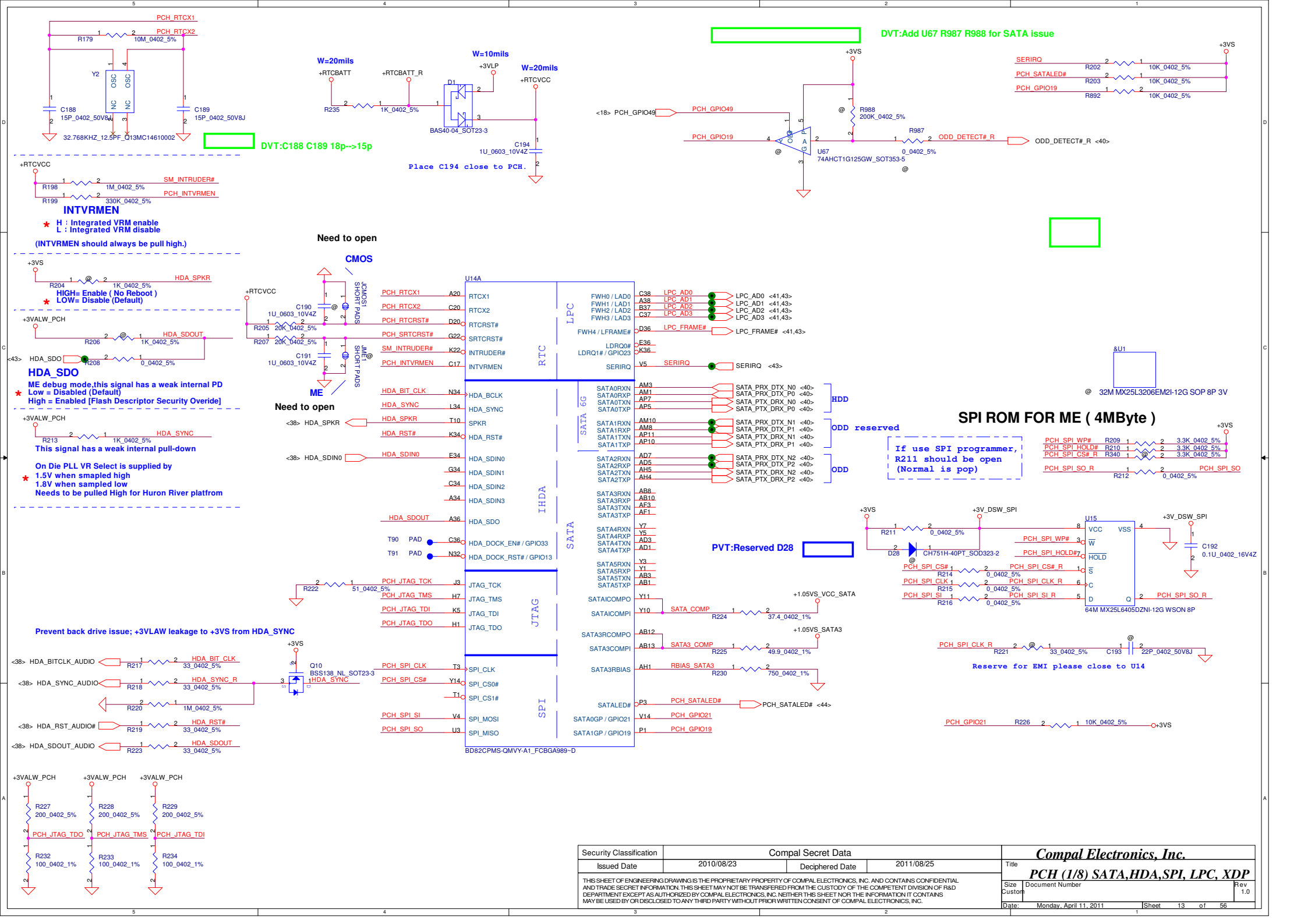

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

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Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom		1.0

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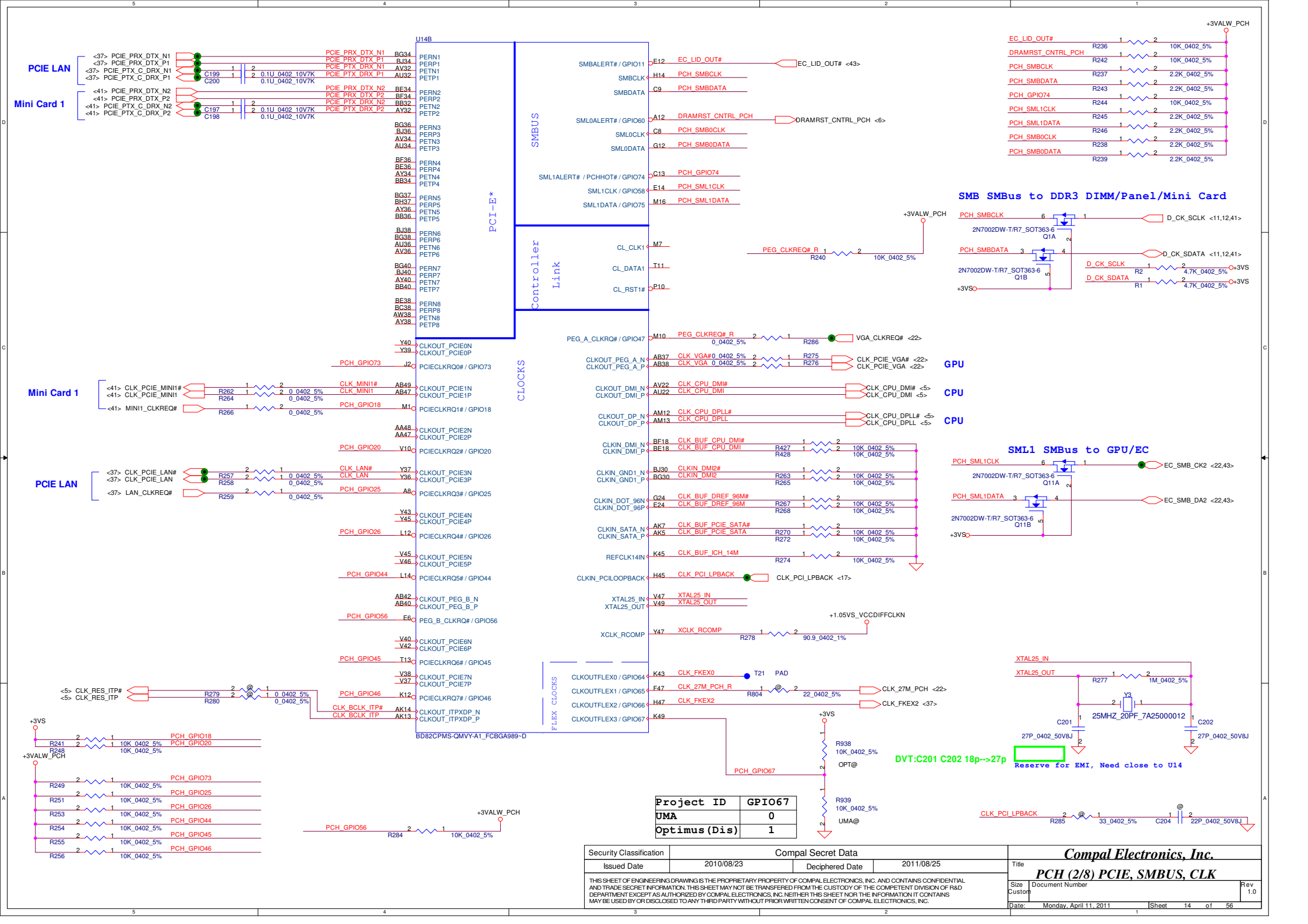
PCIE LAN
Mini Card 1
U14B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
BD82CPMS-QMVY-A1_FCBGA989~D
SMB SMBus to DDR3 DIMM/Panel/Mini Card
SML1 SMBus to GPU/EC
GPU
CPU
CPU
Reserve for EMI, Need close to U14
DVT:C201 C202 18p-->27p
Project ID | GPIO67
UMA | 0
Optimus(Dis) | 1
Compal Secret Data
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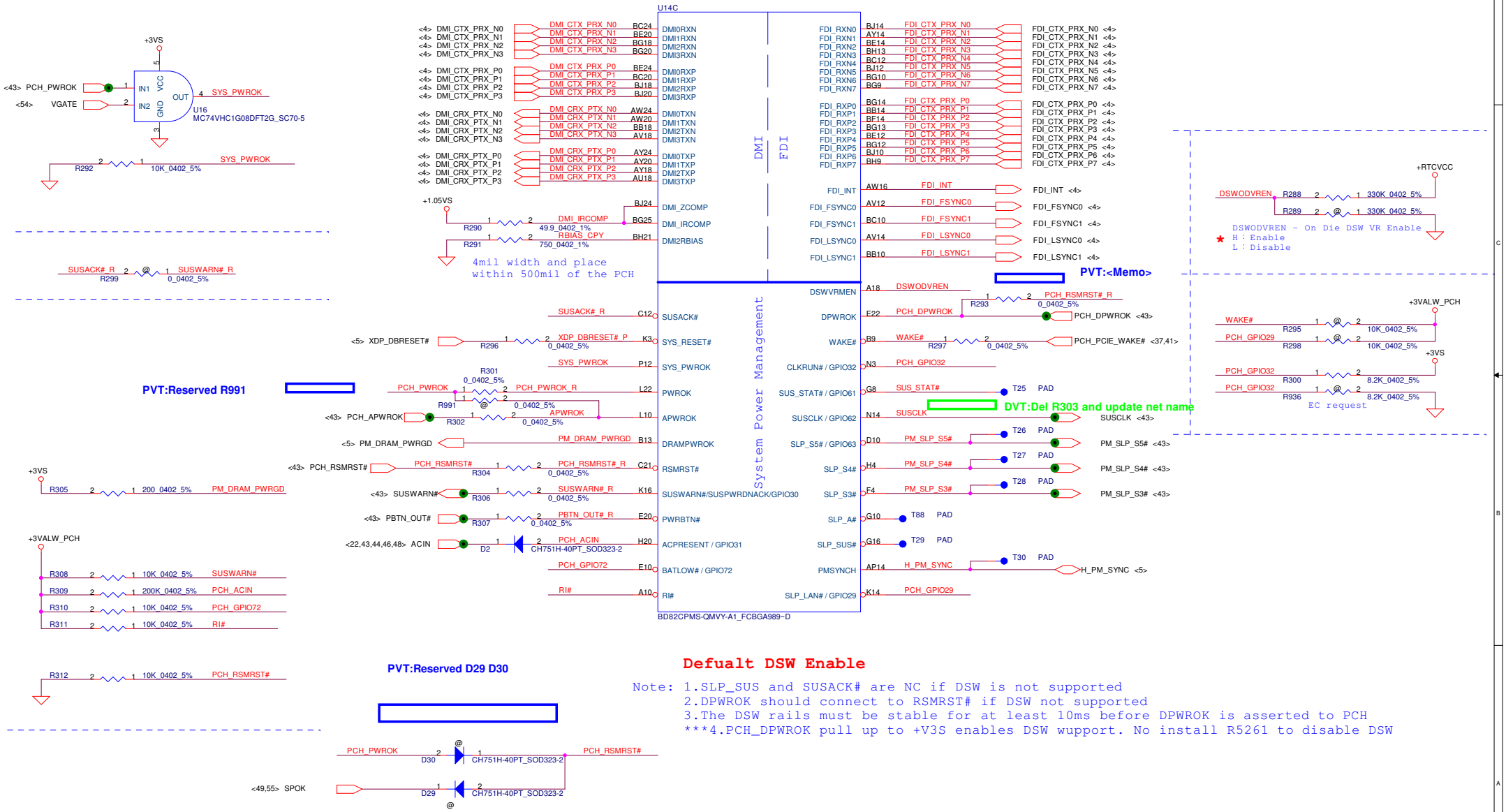
PCH (2/8) PCIE, SMBUS, CLK
Issued Date 2010/08/23
Deciphered Date 2011/08/25
Monday, April 11, 2011



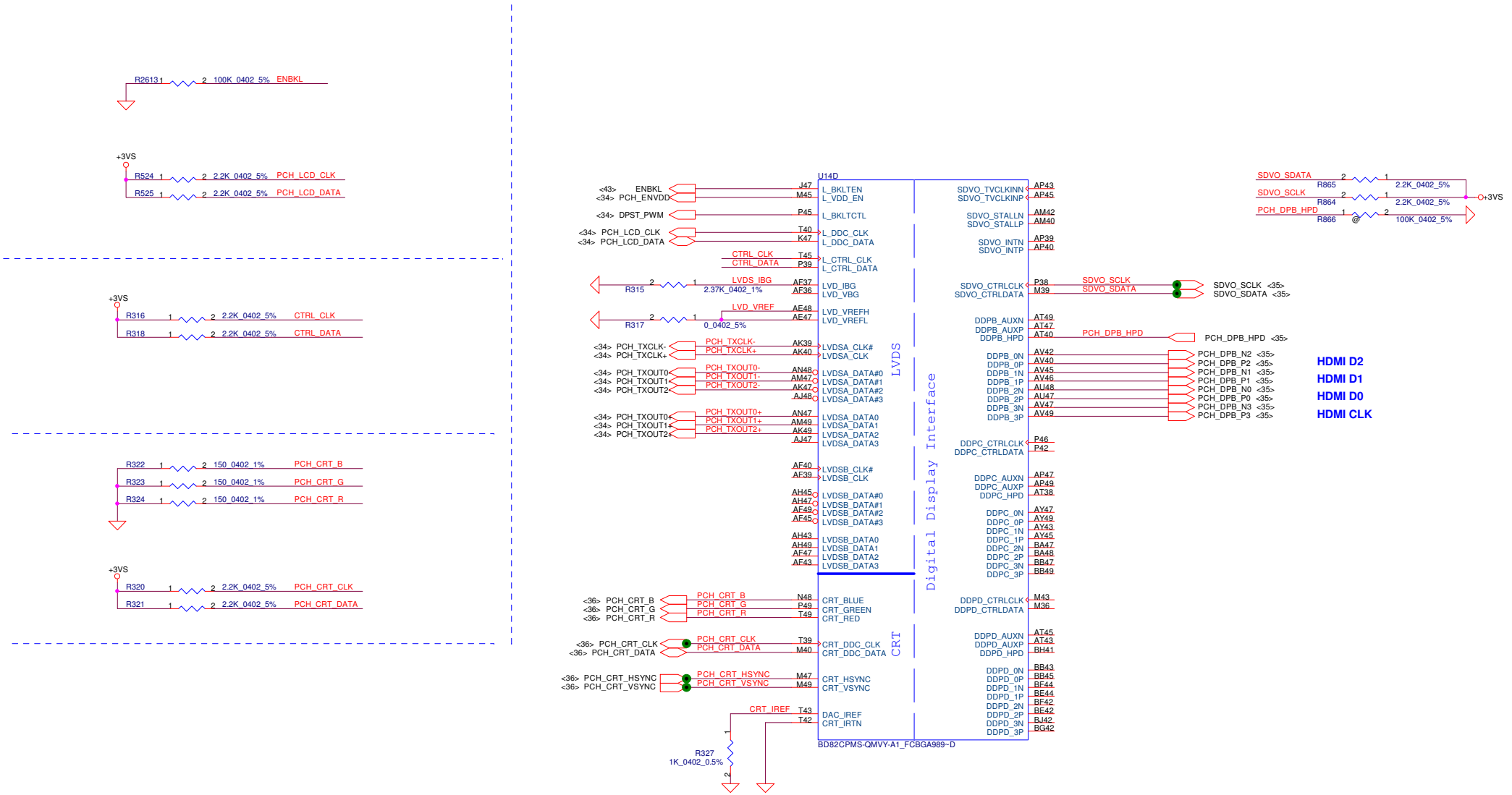
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 15 of 56



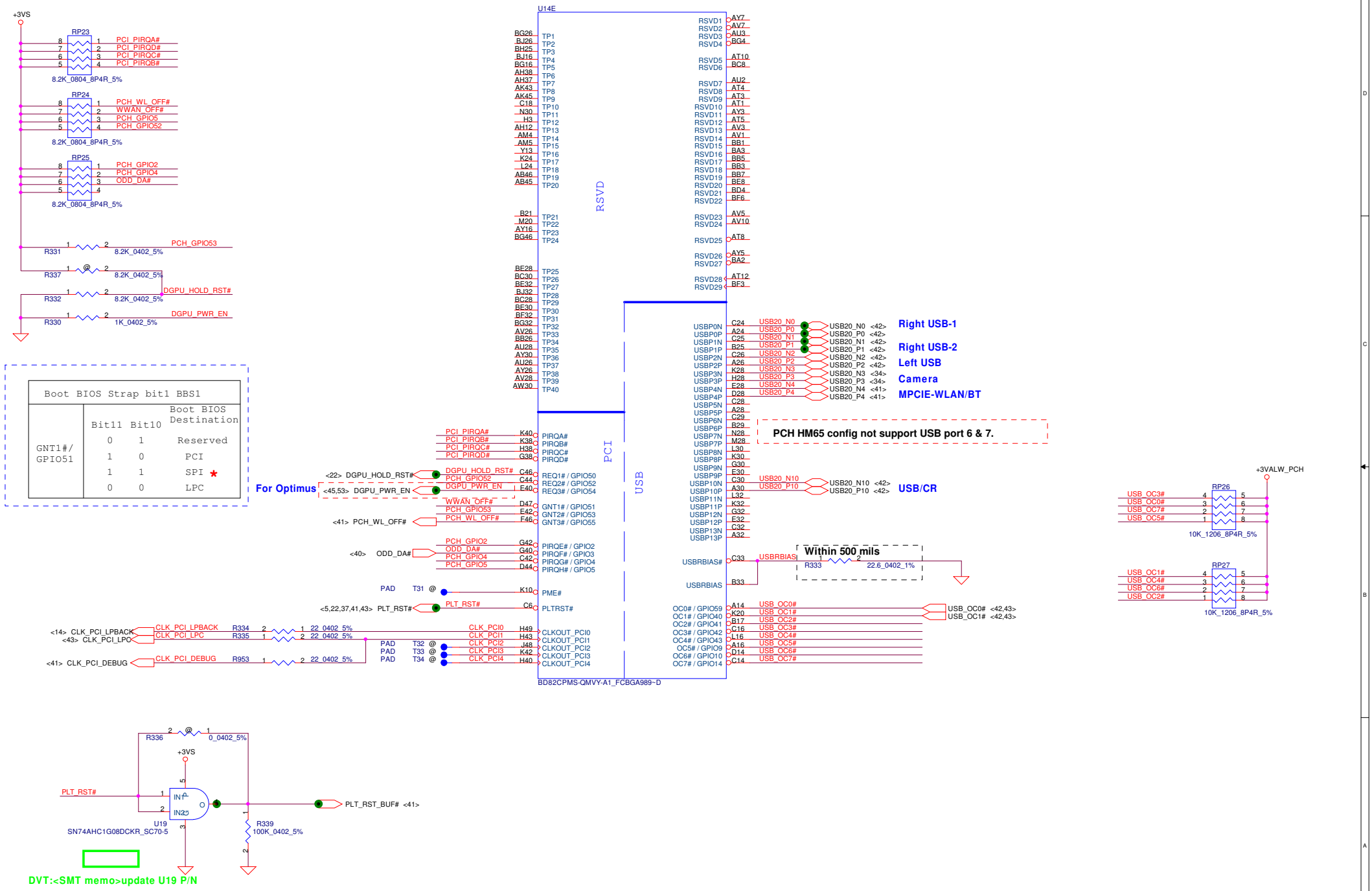
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size	Document Number	Rev
Custom		1.0

Date: Monday, April 11, 2011 Sheet 16 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 17 of 56

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R343 1K_0402_5% PCH_GPIO28

GPIO27
PCH_GPIO27 (Have internal Pull-High)

* High: VCCVRM VR Enable
  Low: VCCVRM VR Disable

R344 10K_0402_5% PCH_GPIO27

+3VS

Note: High - CRT Plugged

R342 10K_0402_5%

CRT_DET

<36> CRT_DET# Q12 2N7002_SOT23-3

+3VS

ODD_EN# R2614 10K_0402_5%

PCH_GPIO70 R2616 10K_0402_5%

PCH_GPIO71 R2617 10K_0402_5%

GATEA20 R346 10K_0402_5%

EC_KBRST# R345 10K_0402_5%

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

+3VS

R357 200K_0402_1% ODD_DETECT#

+3VS

R801 1K_0402_5% PCH_GPIO37

R776 100K_0402_5%

U14F

CRT_DET	T7	BMBUSY# / GPIO0	
PCH_GPIO1	A42	TACH1 / GPIO1	
PCH_GPIO6	H36	TACH2 / GPIO6	
<43> EC_SCI#	E38	TACH3 / GPIO7	
<43> EC_SMI#	C10	GPIO8	
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12	
USB30_SMI#	G2	GPIO15	
PCH_GPIO16	U2	SATA4GP / GPIO16	
For Optimus <45,53> DGPU_PWROK	D40	TACH0 / GPIO17	
PCH_GPIO22	T5	SCLOCK / GPIO22	
PCH_GPIO24	E8	GPIO24 / MEM_LED	
PCH_GPIO27	E16	GPIO27	
PCH_GPIO28	P8	GPIO28	
<41> BT_ON#	K1	STP_PCI# / GPIO34	
PCH_GPIO35	K4	GPIO35	
<40> ODD_DETECT#	V8	SATA2GP / GPIO36	
PCH_GPIO37	M5	SATA3GP / GPIO37	
PCH_GPIO38	N2	SLOAD / GPIO38	
PCH_GPIO39	M3	SDATAOUT0 / GPIO39	
PCH_GPIO48	V13	SDATAOUT1 / GPIO48	
<13> PCH_GPIO49	V3	SATA5GP / GPIO49	
PCH_GPIO57	D6	GPIO57	

GPIO

	C40	TACH4 / GPIO68	ODD_EN# <40>
	B41	TACH5 / GPIO69	PCH_GPIO69
	C41	TACH6 / GPIO70	PCH_GPIO70
	A40	TACH7 / GPIO71	PCH_GPIO71
	P4	A20GATE	GATEA20 <43>
	AU16	PECI	PCH_PECI_R R348 0_0402_5% H_PECI <5,43>
	P5	RCIN#	EC_KBRST# <43>
	AY11	PROCPWRGD	H_CPUPWRGD <5>
	AY10	THRMTRIP#	PCH_THRMTRIP#_R R351 390_0402_5% H_THRMTRIP# <5>
	T14	INIT3_3V#	
	AY1	DF_TVS	NV_CLE R329 1K_0402_5% H_SNB_IVB# <5>
	AH8	TS_VSS1	
	AK11	TS_VSS2	
	AH10	TS_VSS3	
	AK10	TS_VSS4	
	P37	NC_1	

CPU/MISC

Note: This signal has weak internal PU, can't pull low

Layout note: CLOSE TO THE BRANCHING POINT

Project ID	GPIO69
14"	0
15.6"	1

+3VS R2615 10K_0402_5% 15@ PCH_GPIO69 R940 10K_0402_5% 14@

+1.8VS R328 2.2K_0402_5%

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) *

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BF49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	F49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

NCTF

BD82CPMS-QMVY-A1_FCBGA989-D

DVT:Add PCH_GPIO49 net off page

+3VS

R421 10K_0402_5% PCH_GPIO6
R420 10K_0402_5% PCH_GPIO1
R352 10K_0402_5% PCH_GPIO16
R353 10K_0402_5% DGPU_PWROK_R
R354 10K_0402_5% PCH_GPIO22
R347 10K_0402_5% PCH_GPIO38
R356 10K_0402_5% PCH_GPIO39

R358 10K_0402_5% BT_ON#
R359 10K_0402_5% PCH_GPIO48
R360 10K_0402_5% PCH_GPIO49

+3VALW_PCH

R361 10K_0402_5% PCH_GPIO12
R362 1K_0402_5% USB30_SMI#
R363 10K_0402_5% PCH_GPIO28
R364 10K_0402_5% PCH_GPIO57
R429 10K_0402_5% PCH_GPIO24
R365 10K_0402_5% PCH_GPIO35

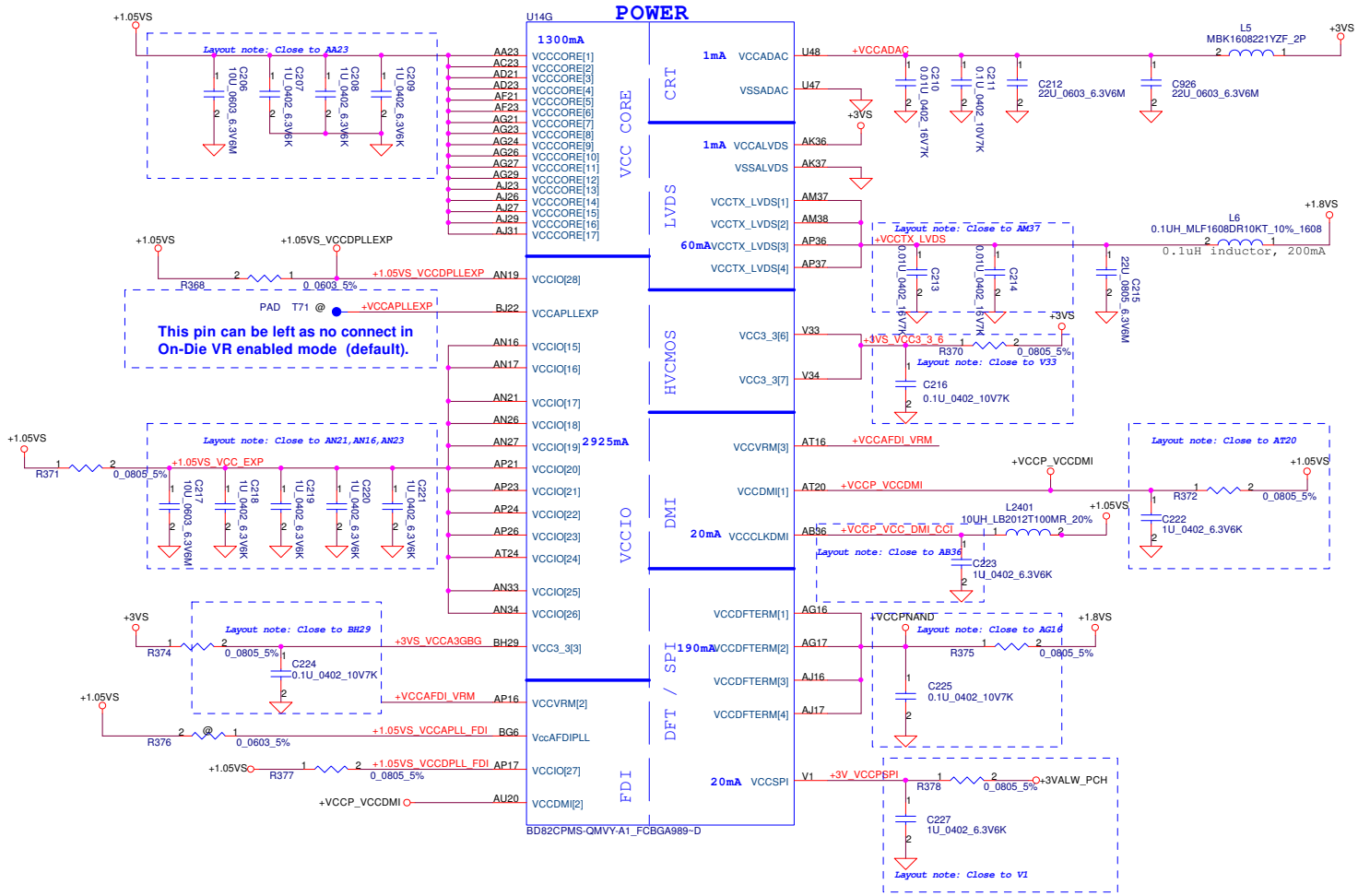
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **PCH (6/9) GPIO, CPU, MISC**

Size	Document Number	Rev
Custom		1.0

Date: Monday, April 11, 2011 Sheet 18 of 56



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 19 of 56

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

12/29 change SC1H751H010 to SCS00003500

DVT:Reserved C913 C914

PVT:<Memo>

POWER

U14J

BD82CPMS-QMVY-A1_FCBGA989~D

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

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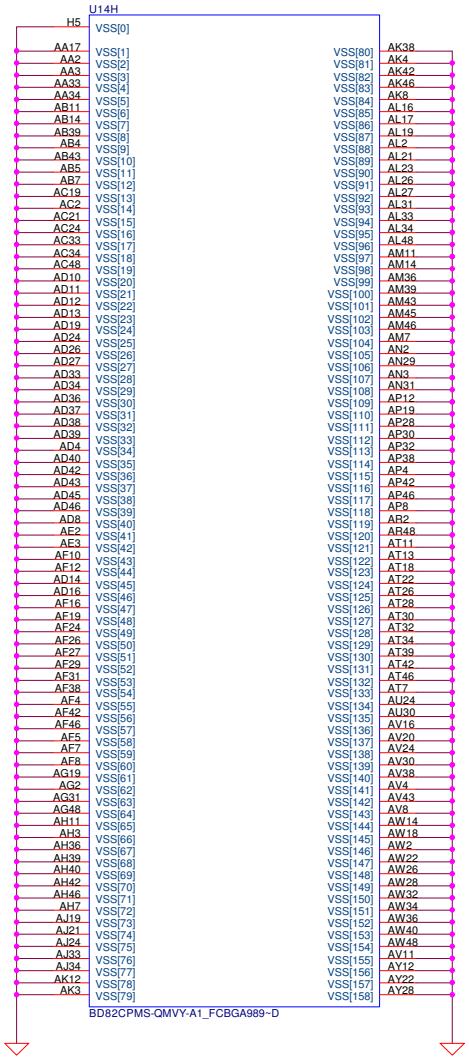
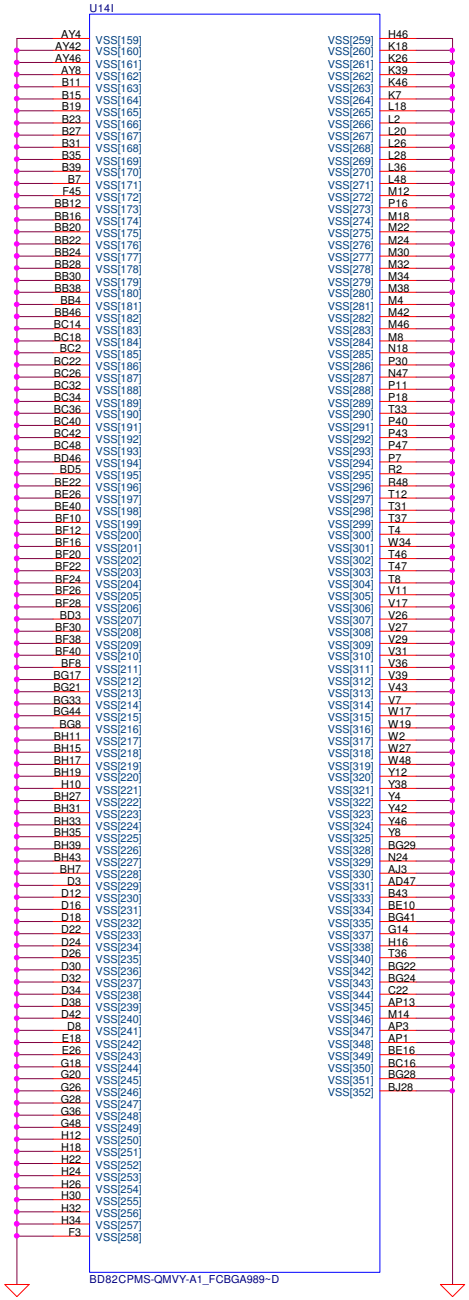
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 20 of 56





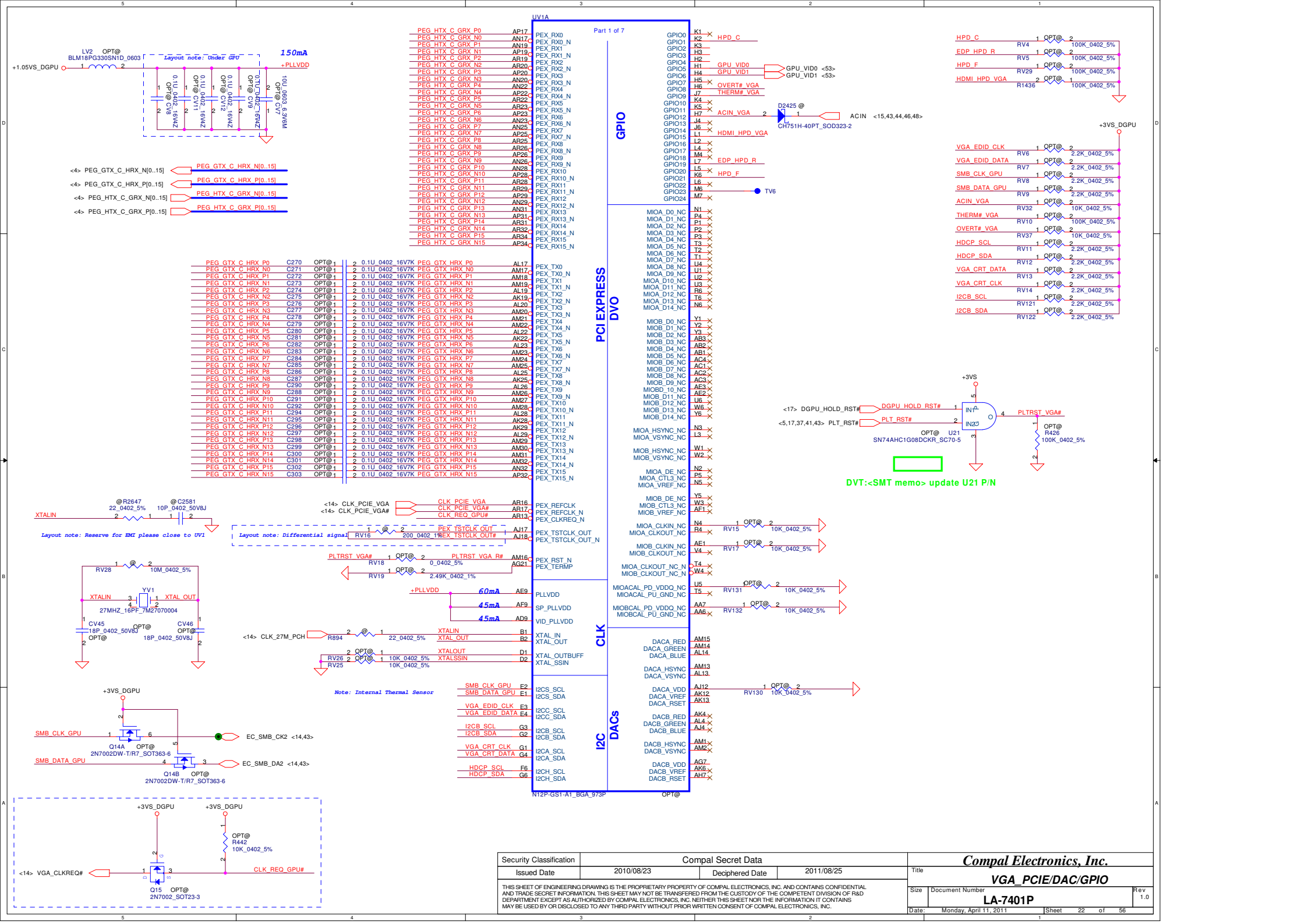
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

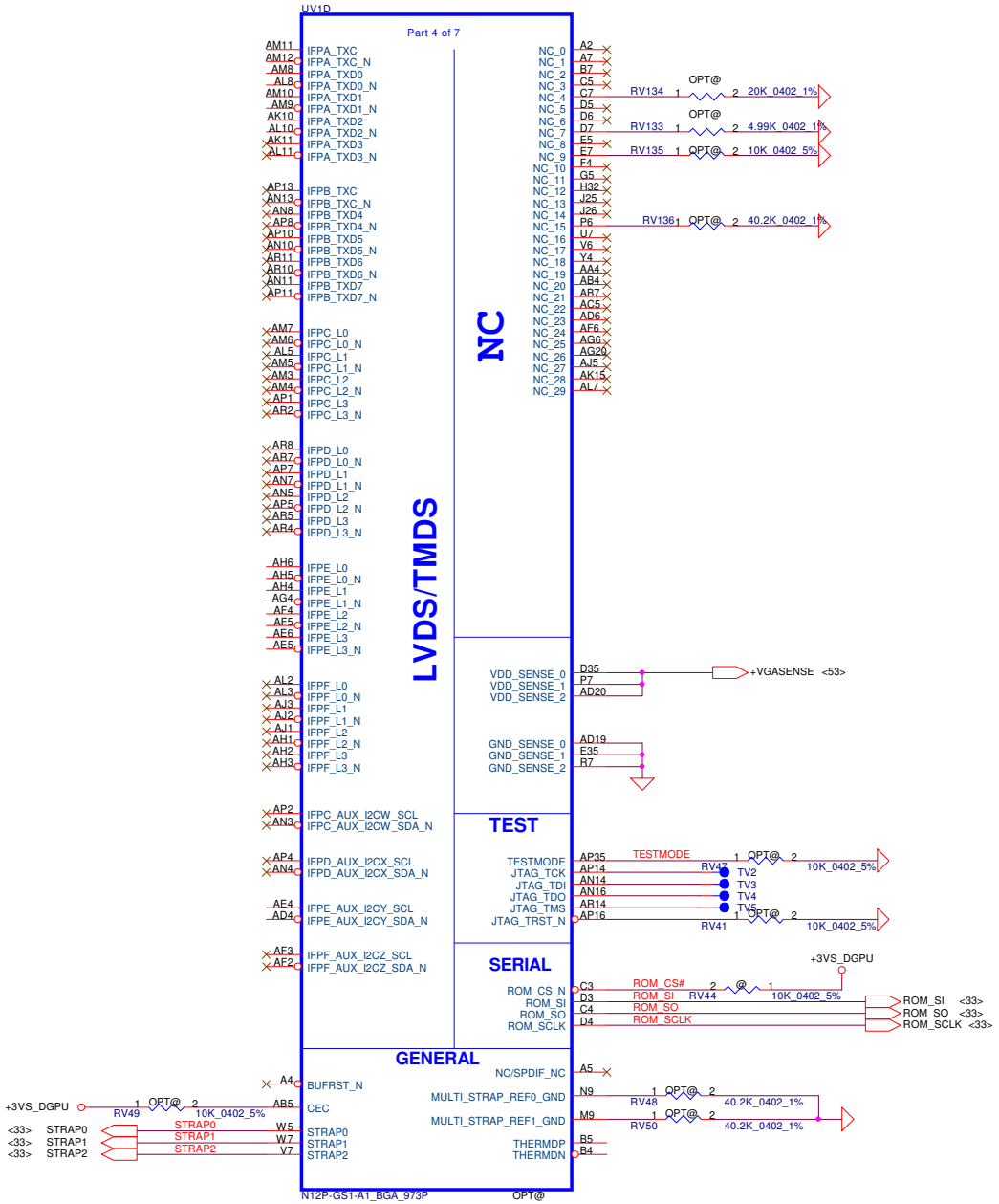
Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
Custom		1.0

Date: Sunday, April 10, 2011 Sheet 21 of 56


UV1A
Part 1 of 7
PCI EXPRESS
DVO
GPIO
CLK
I2C
DACs
N12P-GS1-A1_BGA_973P
OPT@
150mA
Layout note: Under GPU
+1.05VS_DGPU
+PLLVDD
LV2 OPT@ BLM18PG330SN1D_0603
Layout note: Reserve for EMI please close to UV1
Layout note: Differential signal
Note: Internal Thermal Sensor
DVT:<SMT memo> update U21 P/N
SN74AHC1G08DCKR_SC70-5
+3VS_DGPU
+3VS
EC_SMB_CK2 <14,43>
EC_SMB_DA2 <14,43>
CLK_REQ_GPU#
<14> VGA_CLKREQ#
Security Classification
Compal Secret Data
Issued Date
2010/08/23
Deciphered Date
2011/08/25
Compal Electronics, Inc.
VGA_PCIE/DAC/GPIO
LA-7401P
Rev 1.0
Monday, April 11, 2011
Sheet 22 of 56



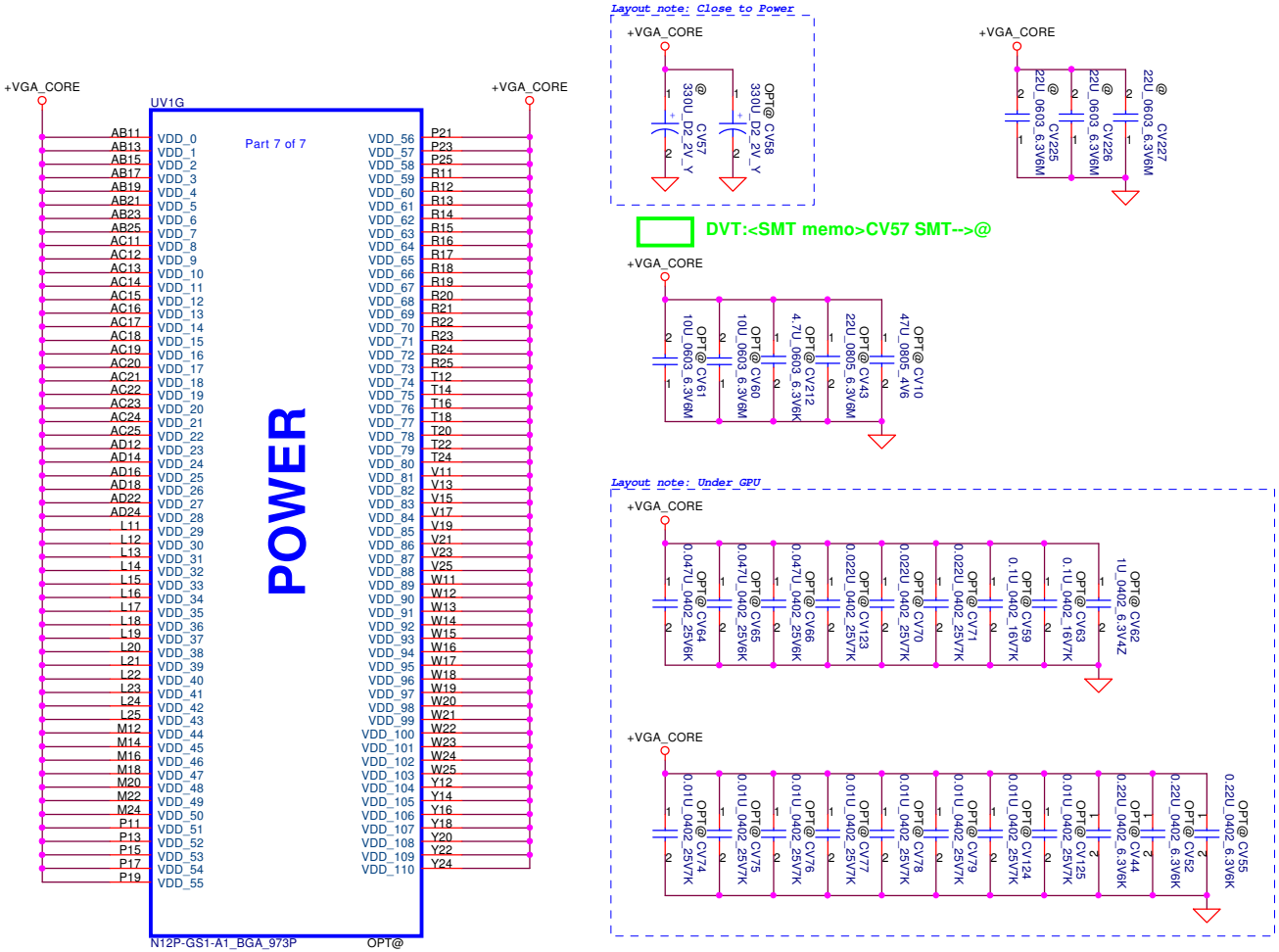
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_STRAPS**

Size	Document Number	Rev
	LA-7401P	1.0

Date: Sunday, April 10, 2011 Sheet 23 of 56



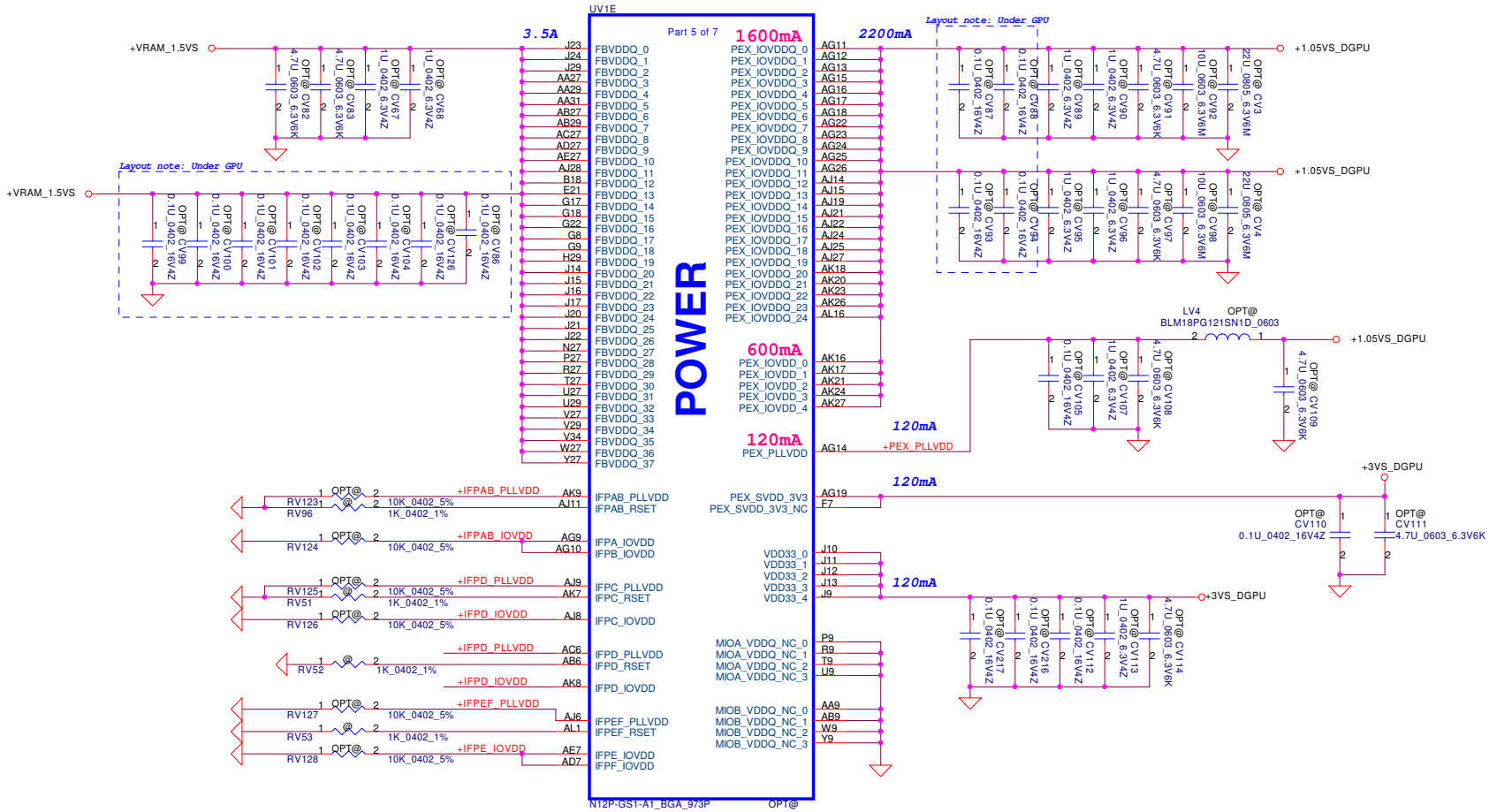
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_VGA CORE**

Size | Document Number: **LA-7401P** | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 24 of 56



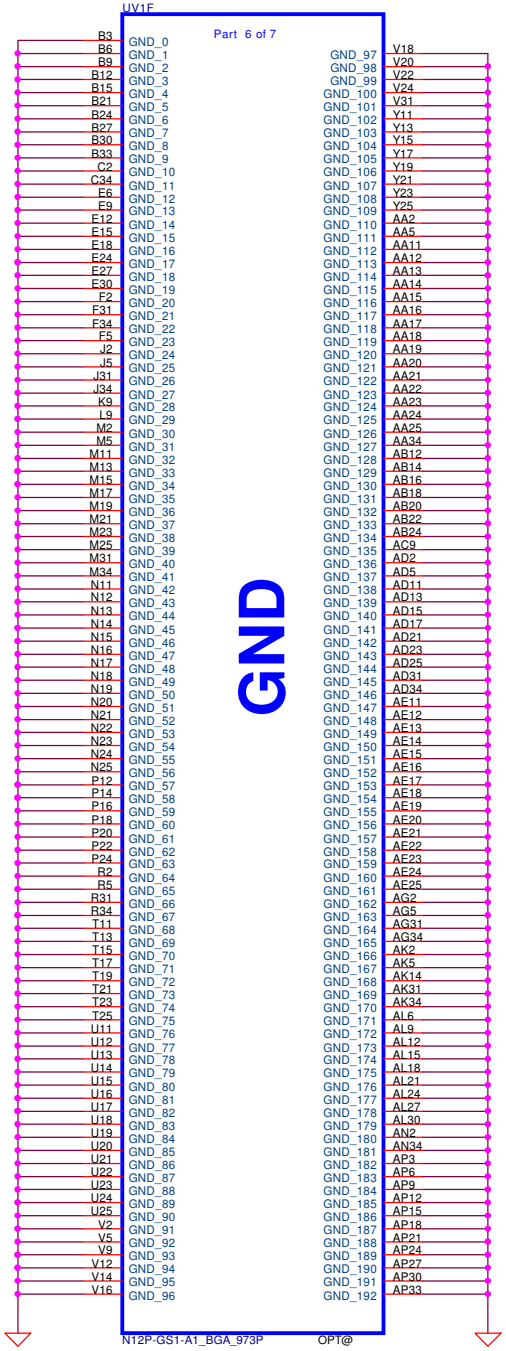
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_POWER**

Size	Document Number	Rev
	LA-7401P	1.0

Date: Sunday, April 10, 2011 Sheet 25 of 56



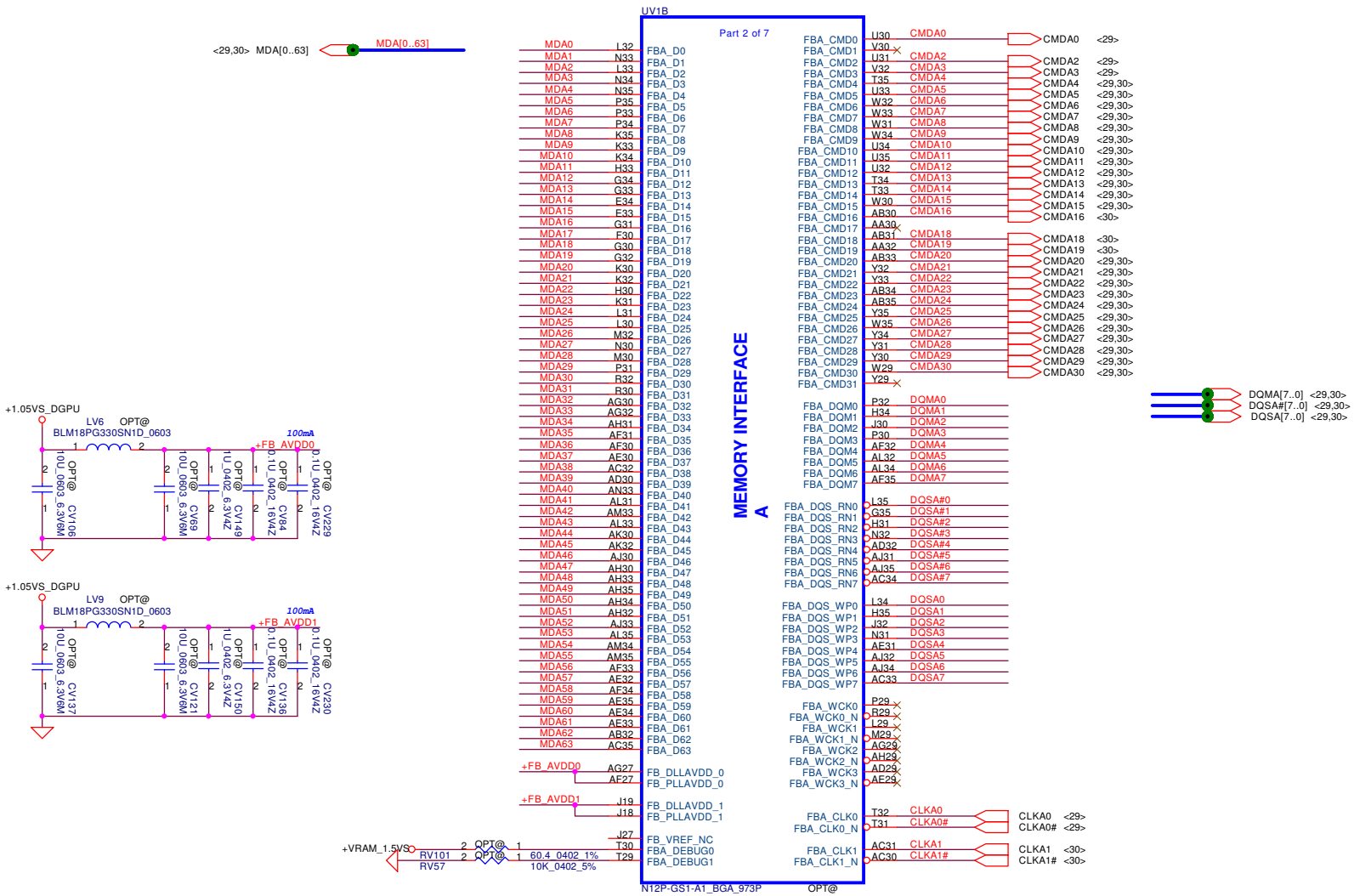
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_GND**

Size | Document Number: **LA-7401P** | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 26 of 56



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

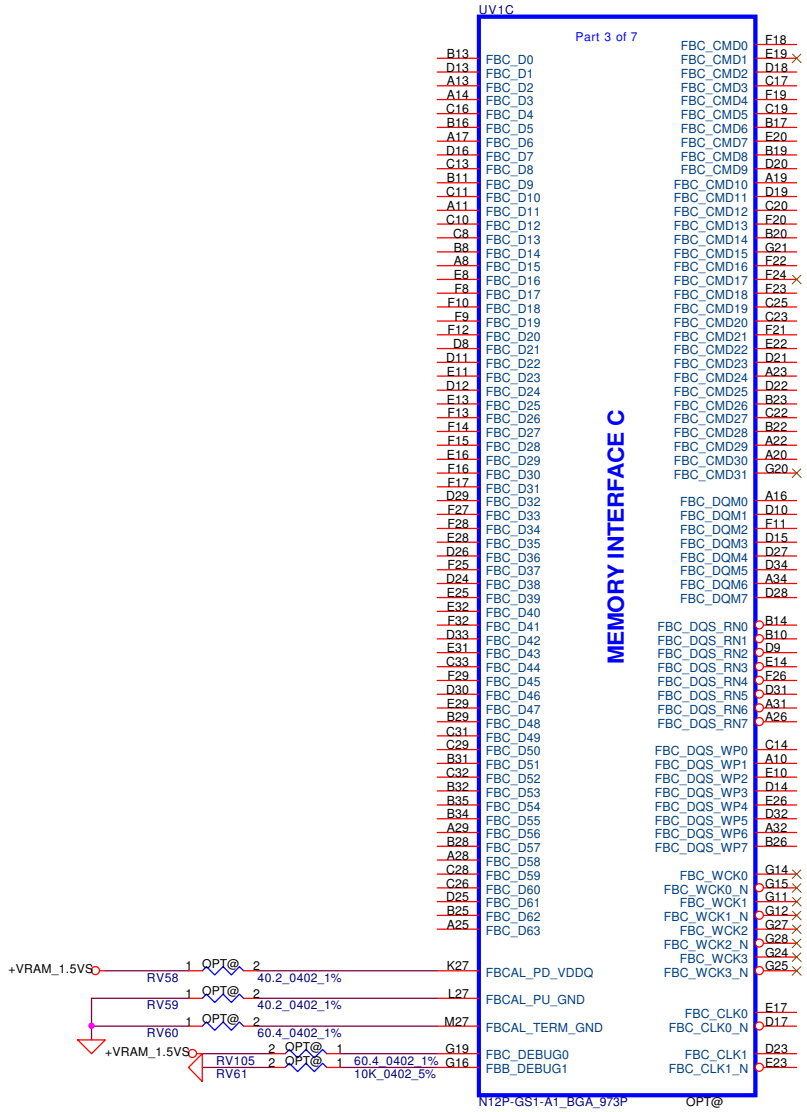
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: VGA_MEM Interface A

Size | Document Number: LA-7401P | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 27 of 56



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

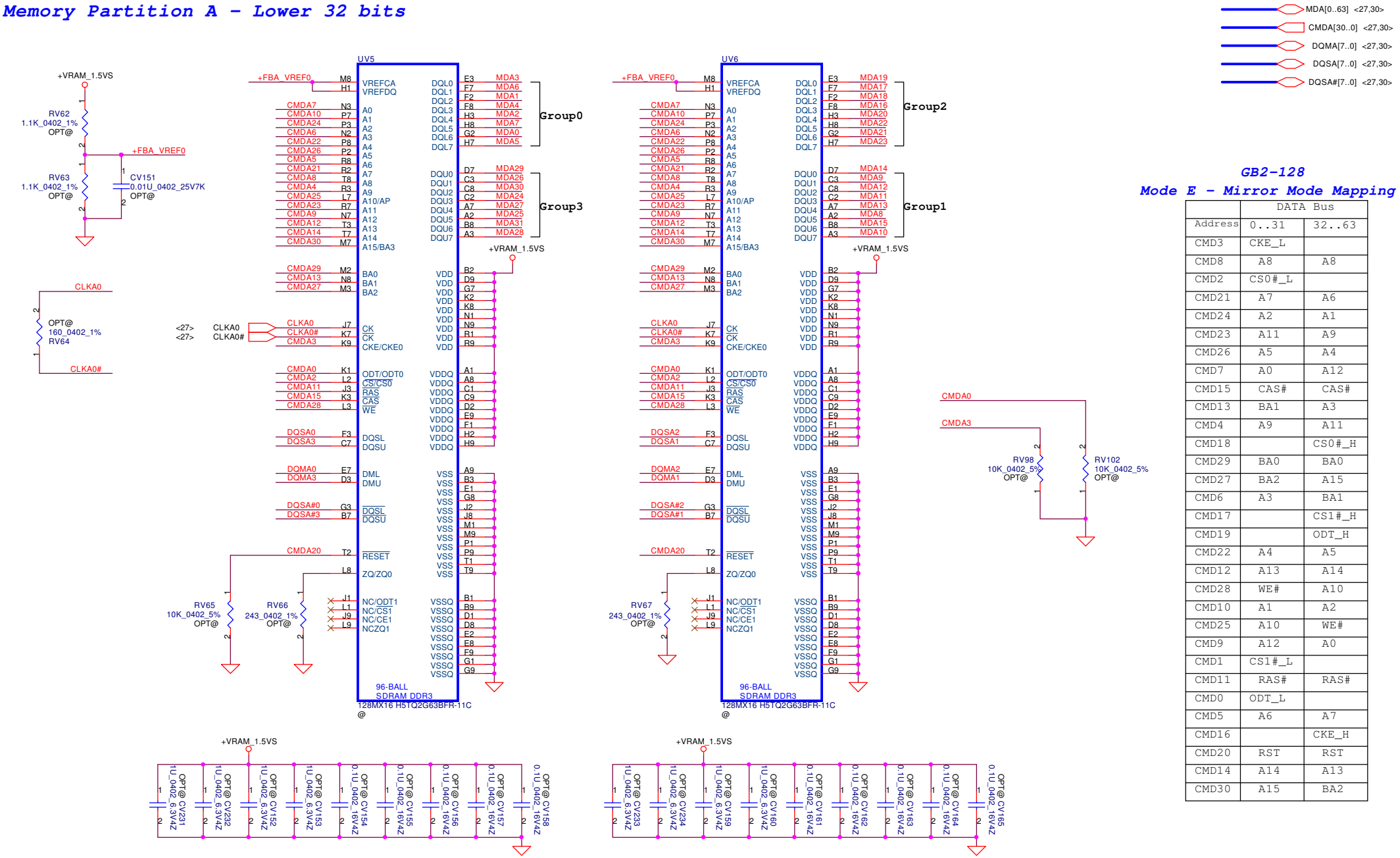
Compal Electronics, Inc.

Title: VGA_MEM Interface C

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 28 of 56

Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

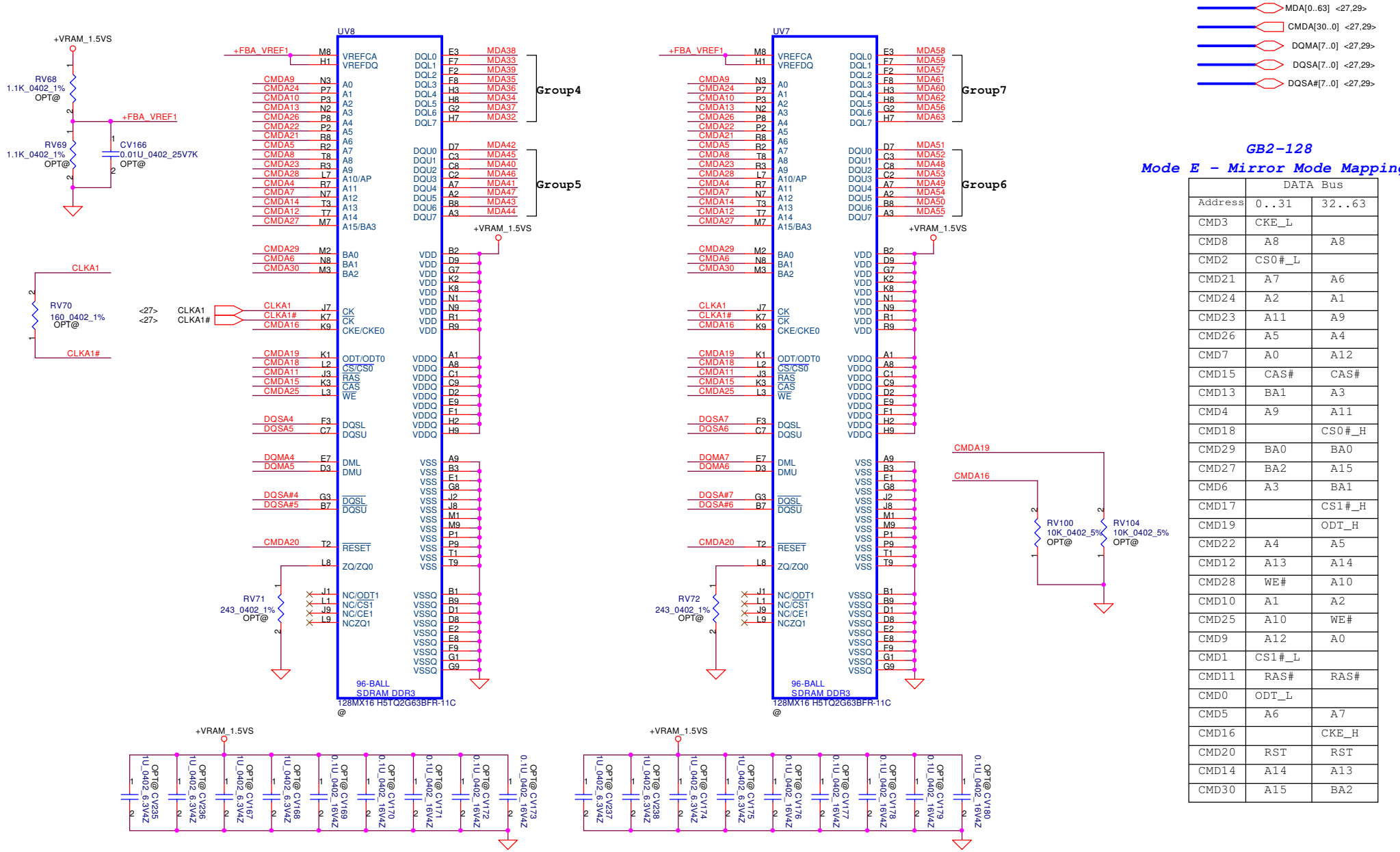
Compal Electronics, Inc.

Title: VGA_VRAM_A Lower

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 29 of 56

Memory Partition A - Upper 32 bits



GB2-128

Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: VGA_VRAM_A Upper

Size | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 30 of 56

Memory Partition C - Lower 32 bits

EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA_VRAM_C Lower

Size: Custom | Document Number: LA-7401P | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 31 of 56

Memory Partition C - Upper 32 bits

EVT:Del B ch VRAM

GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA_VRAM_C Upper

Size: Custom | Document Number: LA-7401P | Rev: 1.0

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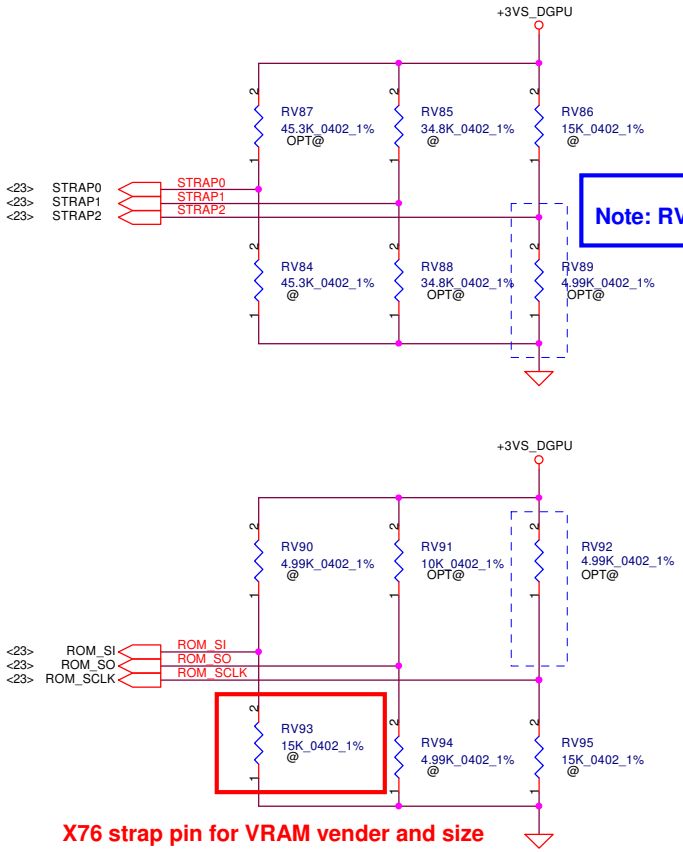

Note: RV89 = 5K for set N12P-GV ,ID=1050)

X76 strap pin for VRAM vender and size

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

ROM_SI net for VRAM strap

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM_SI net setup	PD or PU (RV93)	RP/N
N12P-GV (29x29) 64bit (Layout 4pcs only)	PAJ80(14")	512M(X4)	CHA	DDR3 Hynix 64Mx16 1.5V	SA0000324C0	H5TQ1G63DFR-12C 800MHz	0010	PD 15K	SD034150280(15K)
		512M(x4)	CHA	DDR3 Samsung 64Mx16 1.5V	SA00004HS00	K4W1G1646G-BC12 800MHz	0011	PD 20K	SD034200280(20K)
	PAJ90(15.6")	1G(x4)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00003VS00	H5TQ2G63BFR-12C 800MHz	0110	PD 35K	SD034348280(34.8K)
		1G(x4)	CHA	DDR3 Samsung 128Mx16 1.5V	SA00003MQ40	K4W2G1646C-HC12 800MHz	0111	PD 45K	SD034453280(45.3K)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **VGA_MSIC**

Size: Custom | Document Number: **LA-7401P** | Rev: 1.0

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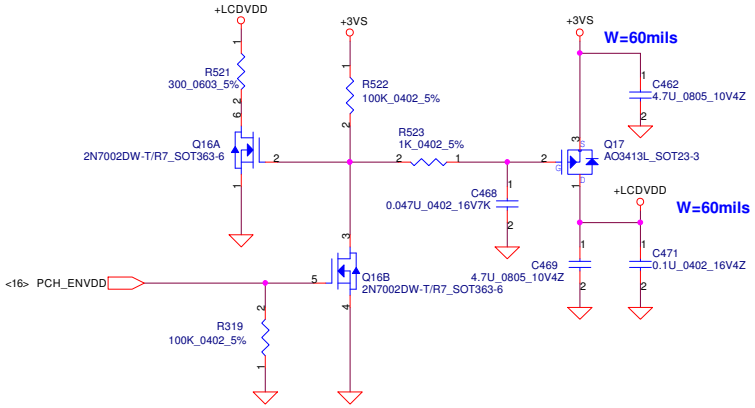
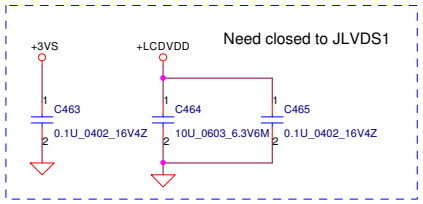
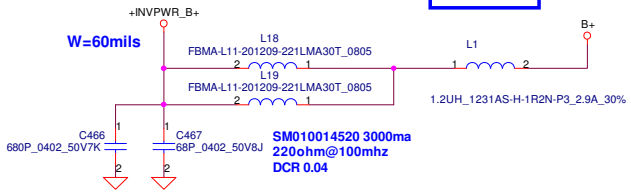
LCD POWER CIRCUIT

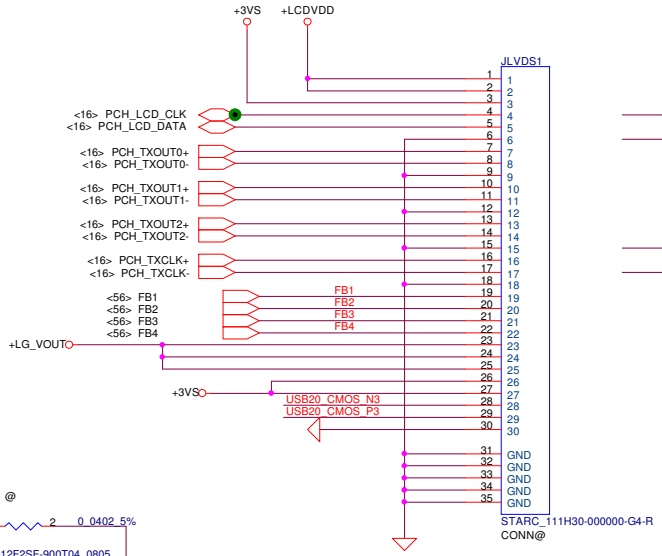


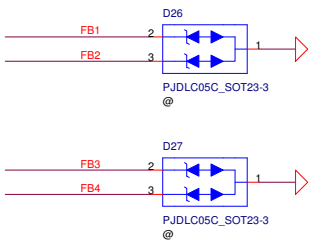


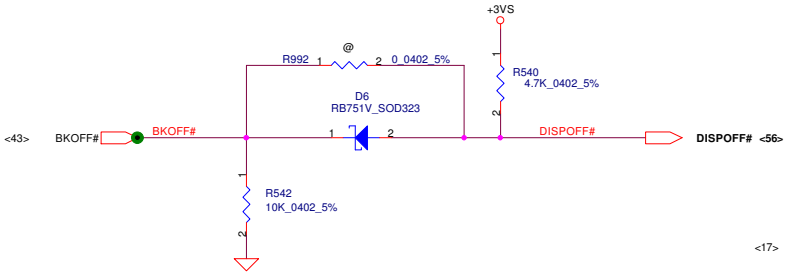
PVT:Add L1 for ESD reuqest



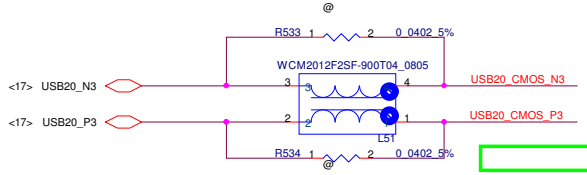
LCD/LED PANEL Connector



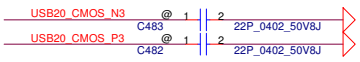


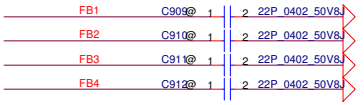


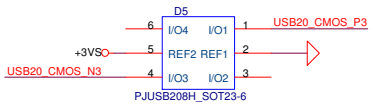
Driver IC



DVT:<EMI>L51 @-->SMT







DVT:<EMI>D5 @-->SMT

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

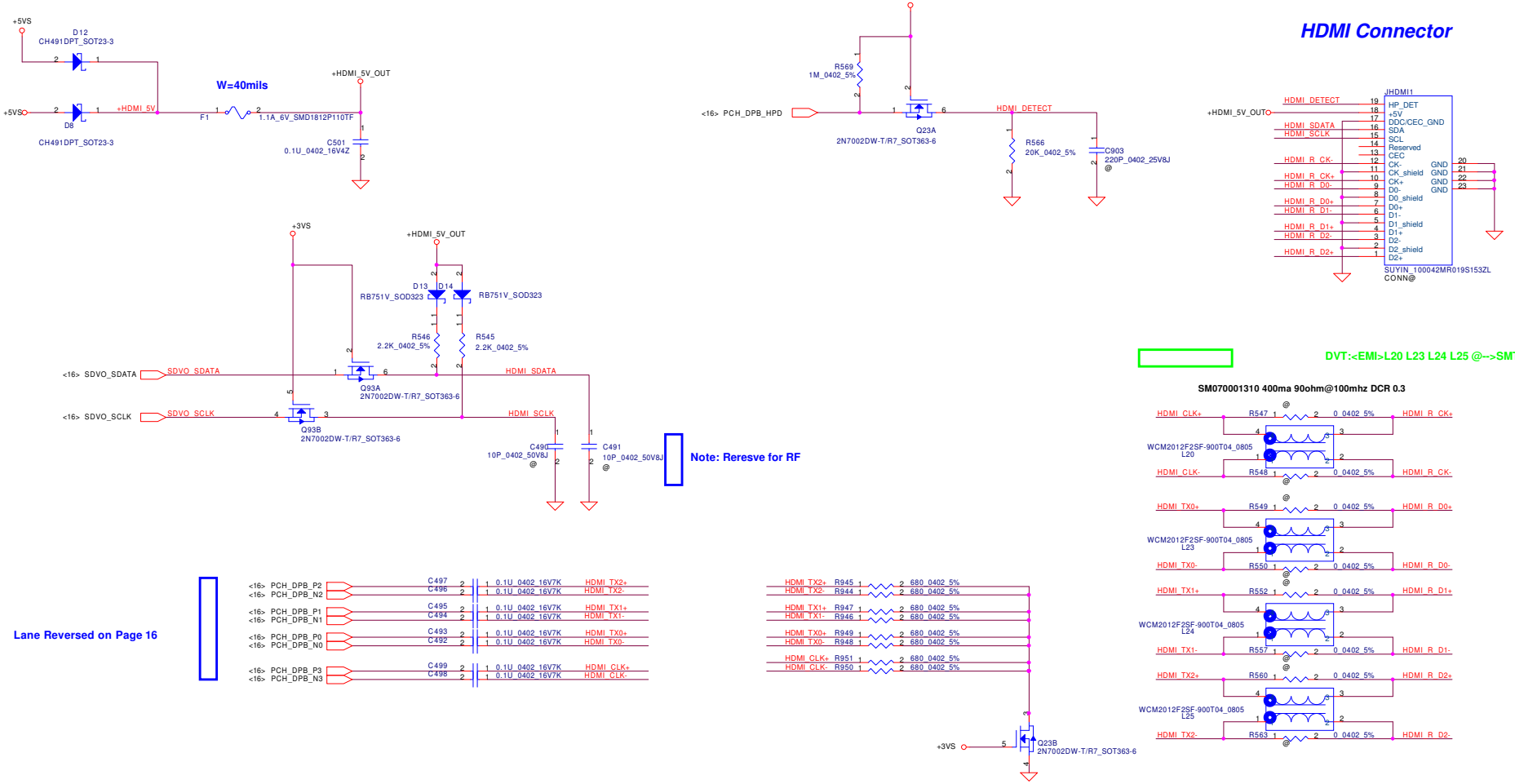
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 34 of 56

HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

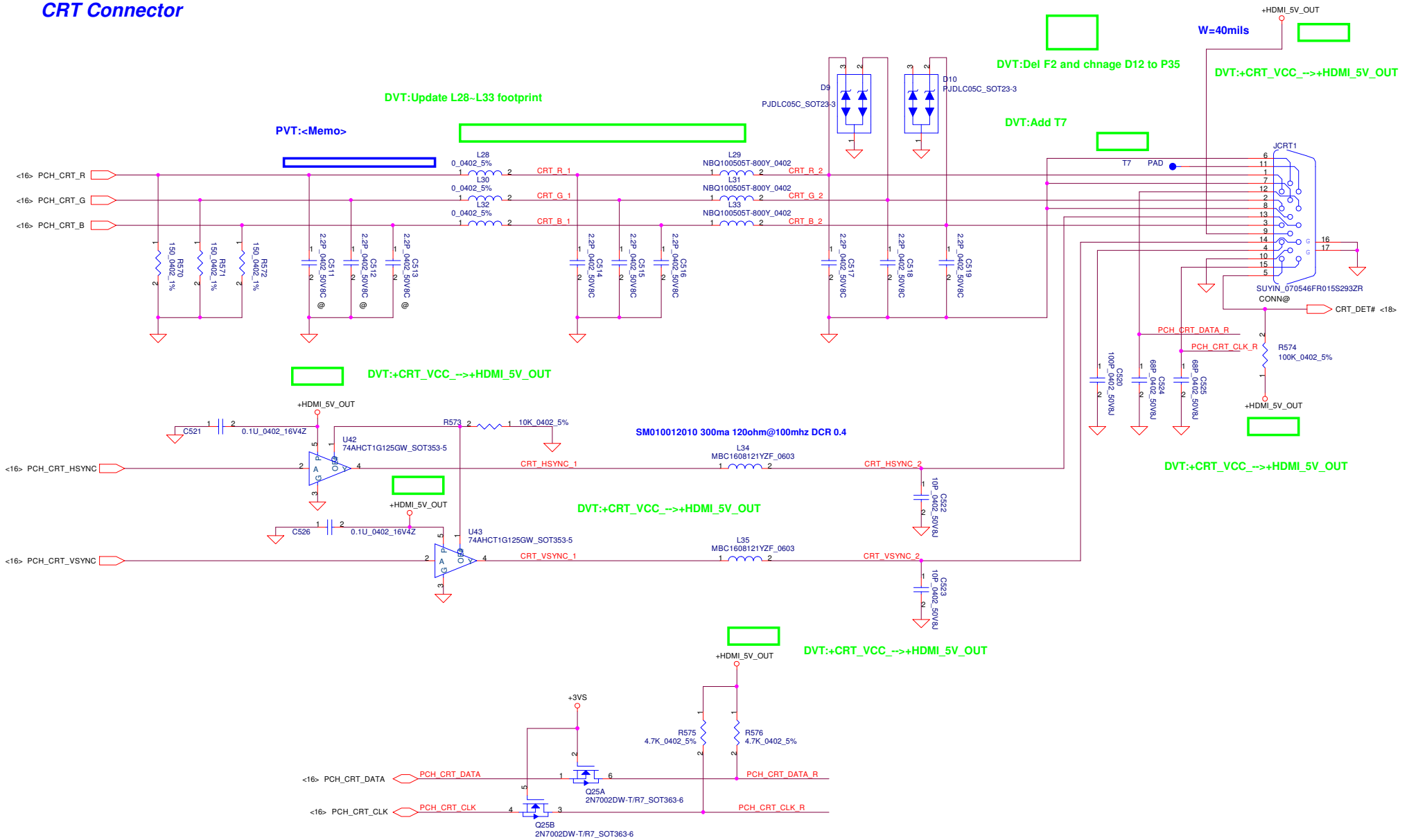
Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
C		1.0

Date: Sunday, April 10, 2011 | Sheet 35 of 56

CRT Connector



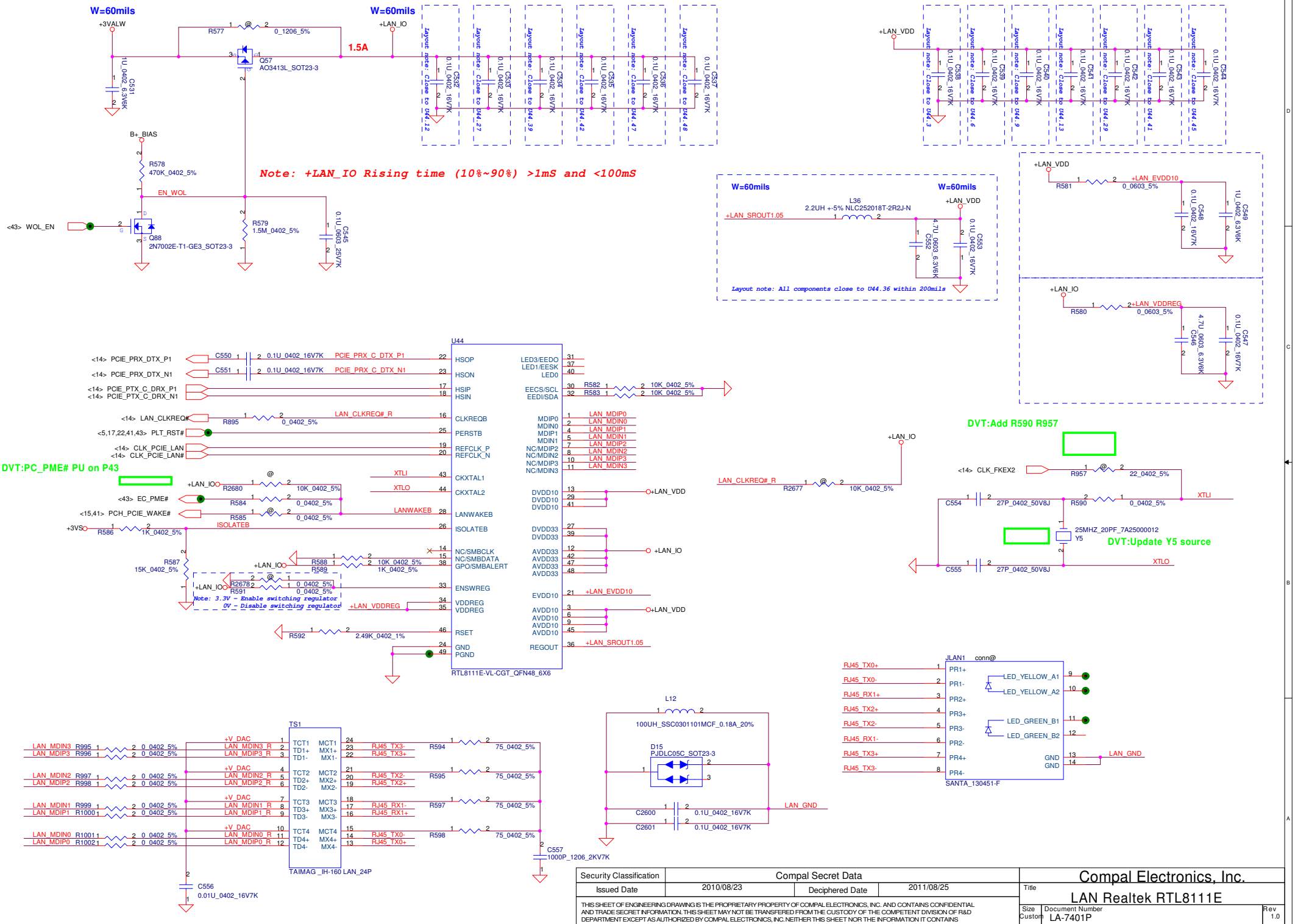
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: LAN Realtek RTL8111E

Size	Document Number	Rev
Custom	LA-7401P	1.0

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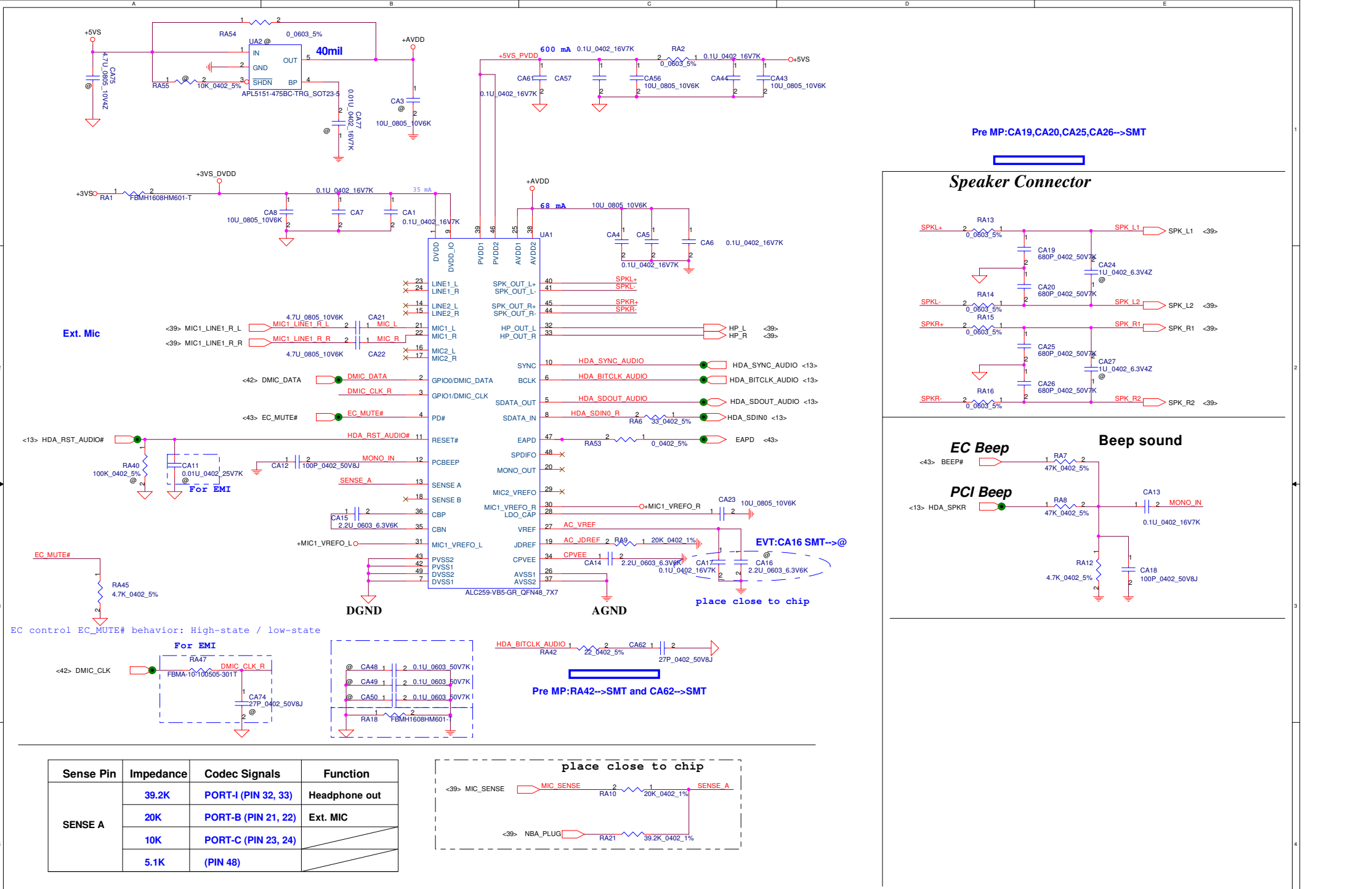


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

Security Classification	Compal Secret Data		
Issued Date	2010/04/28	Deciphered Date	2011/04/28

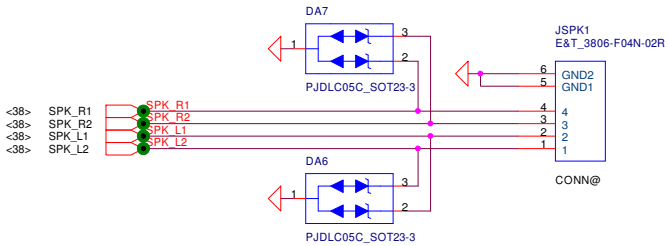
Compal Electronics, Inc.

Title: Audio ALC259

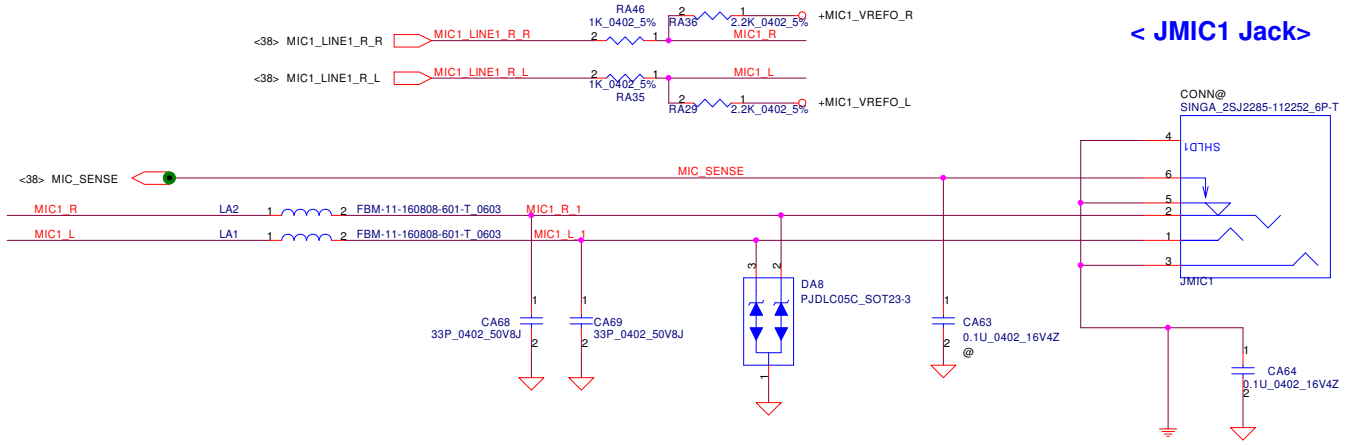
Size: Custom | Document Number: LA-7401P | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 38 of 56

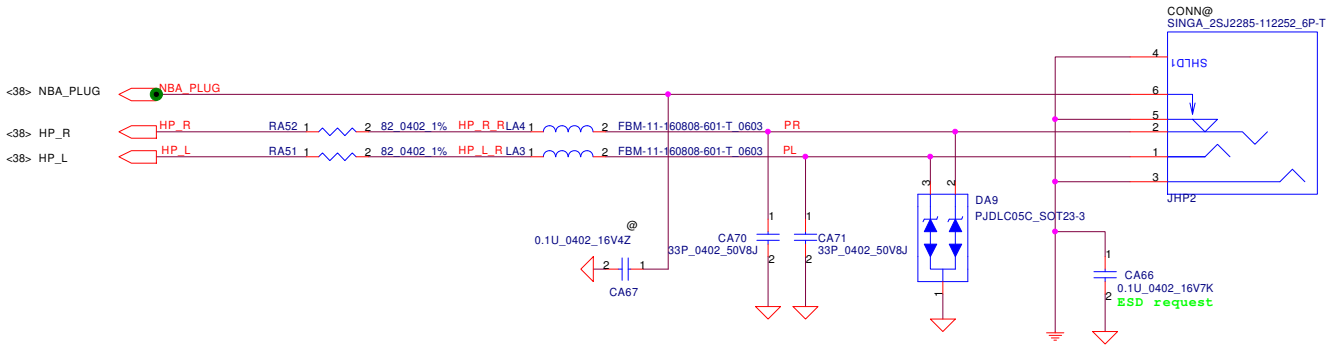
< SPK connector >



< JMIC1 Jack>



<JHP2 Head phone >



Security Classification	Compal Secret Data		
Issued Date	2009/04/07	Deciphered Date	2012/10/21

Compal Electronics, Inc.

Title: SPK/Jack

Size	Document Number	Rev
	LA-7401P	1.0

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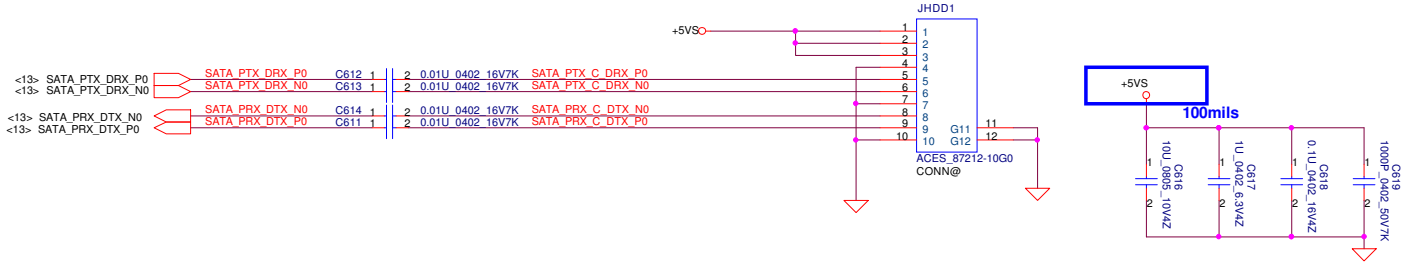
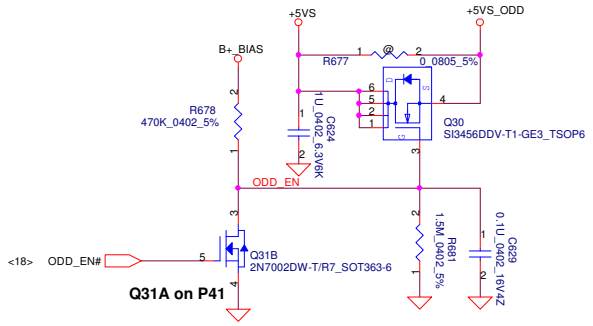
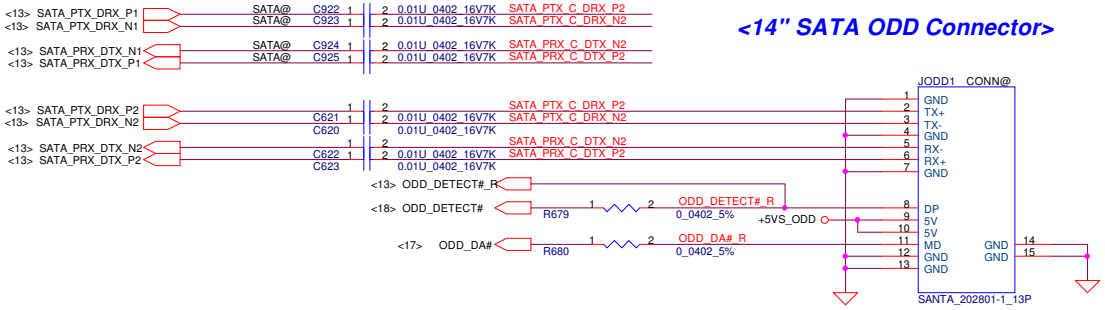
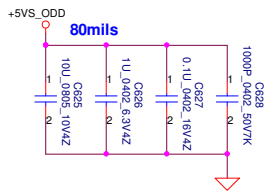
SATA HDD1 Connector







<14" SATA ODD Connector>



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: HDD/ODD Connector

Size: Custom | Document Number | Rev: 1.0

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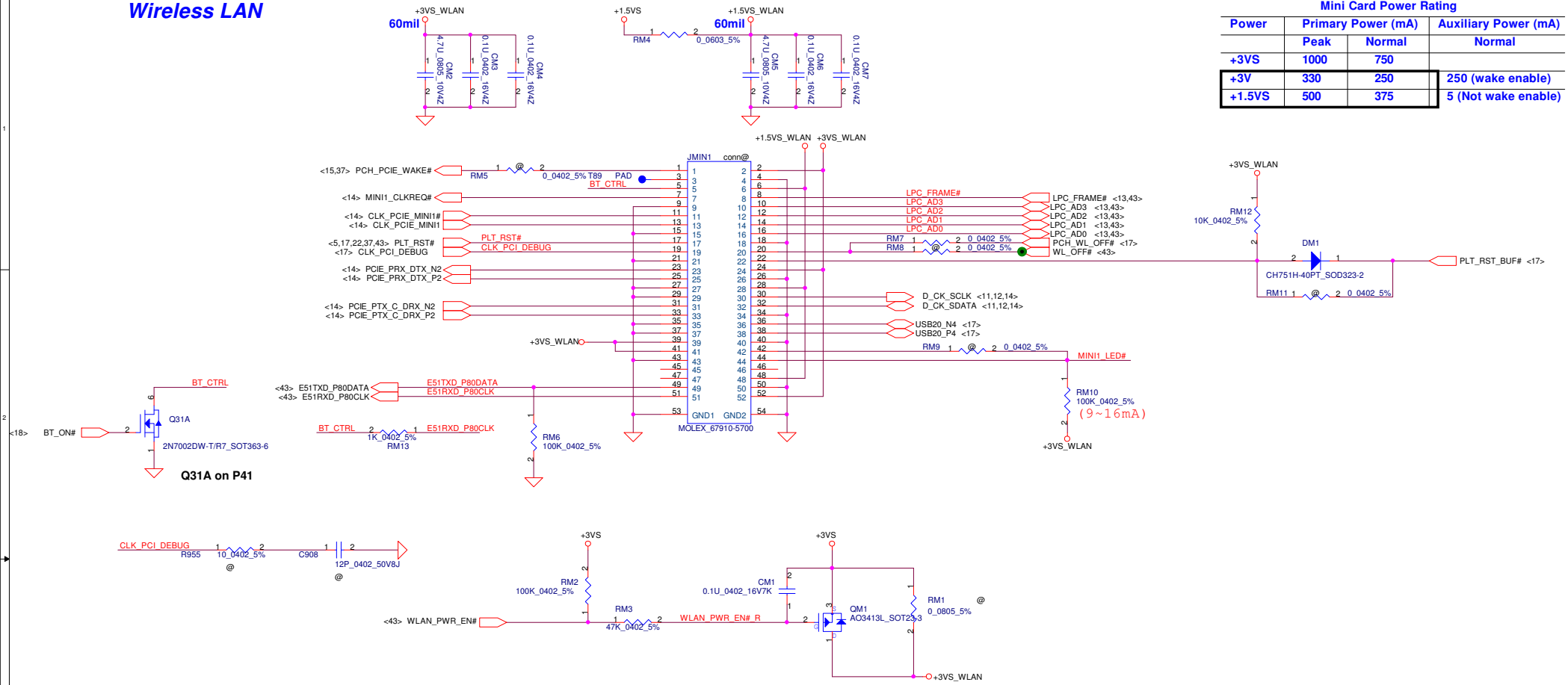
Wireless LAN



Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

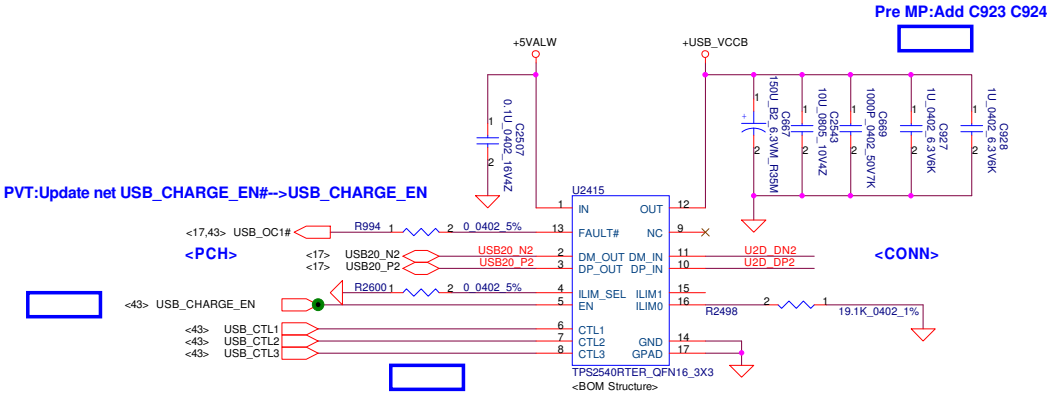
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: MINI CARD WLAN & WWAN

Size: Custom | Document Number | Rev: 1.0

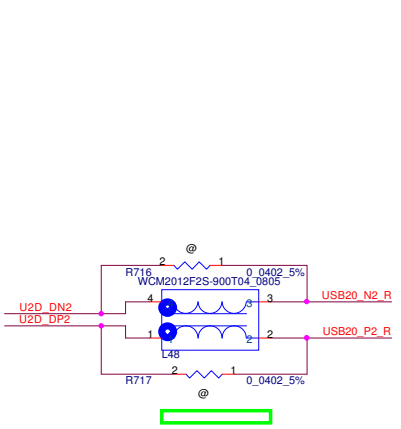
Date: Monday, April 11, 2011 | Sheet 41 of 56

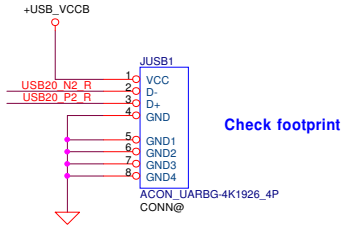


PVT:Update net USB_CHARGE_EN#-->USB_CHARGE_EN

Pre MP:Add C923 C924

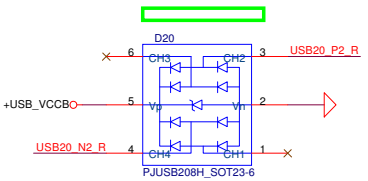
PVT:Remove R2664 R2499 R2500 R2501 for DFX issue





Check footprint

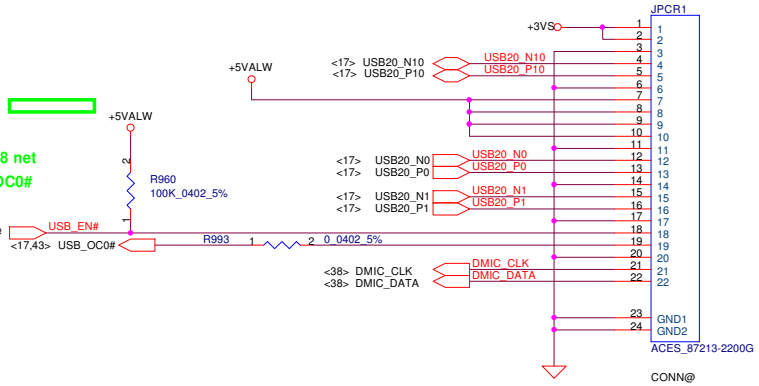
DVT:<EMI>L48 D20 @-->SMT

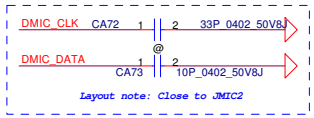


DVT:Add R560 and update JPCR1 pin18 net

DVT:Update USB_OC1#-->USB_OC0#

PVT:Add R993





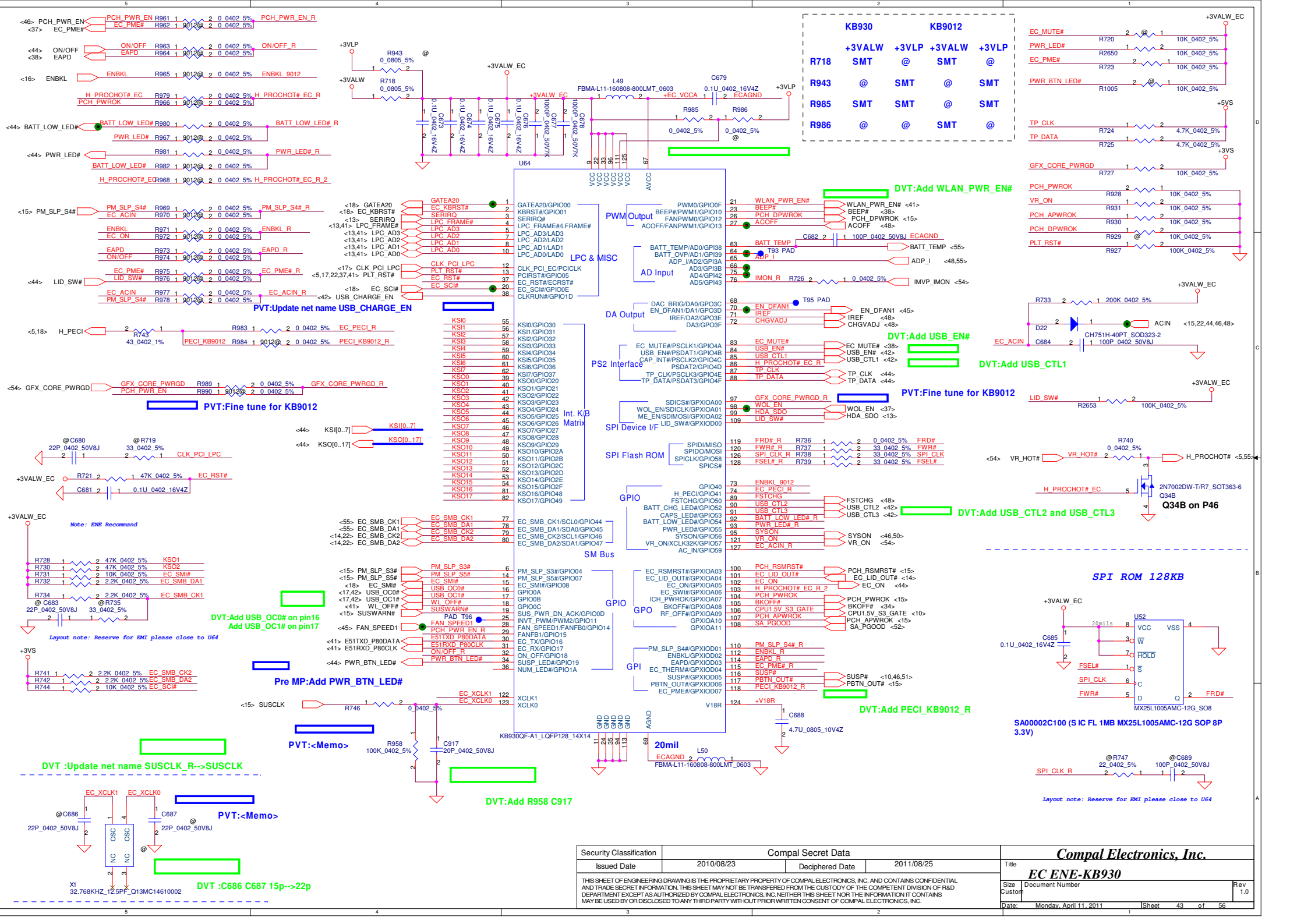
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: USB Combo Connector

Size: Custom | Document Number | Rev: 1.0

Date: Monday, April 11, 2011 | Sheet 42 of 56



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number | Rev: 1.0

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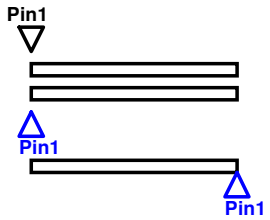
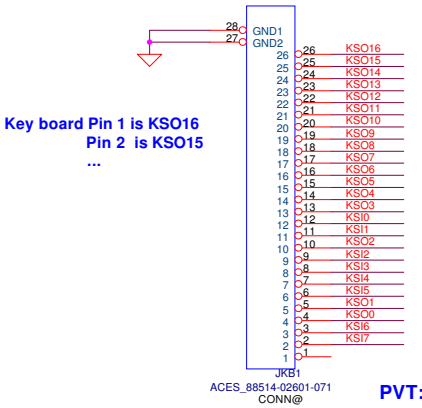
INT_KBD Connector
New key board

Key board pin define (Down)

CIS symbol (DVT)

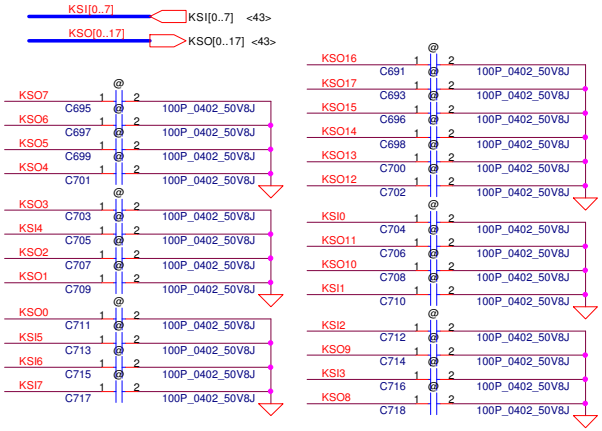
CIS symbol (PVT need reverese pin define)



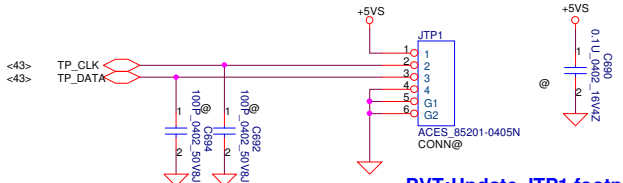


Key board Pin 1 is KSO16
Pin 2 is KSO15
...

PVT:Update JKB1 footprint

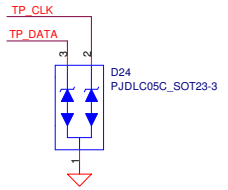


<T/P conn>

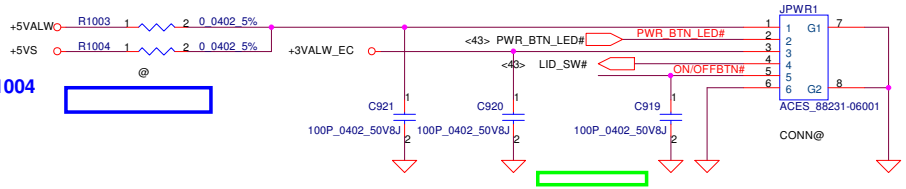


PVT:Update JTP1 footprint

EVT:Check pin define



<Power Button/Lid B conn>

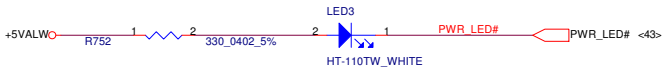


Pre MP:Add R1003 R1004

DVT:Update JPWR1 footprint and pin define

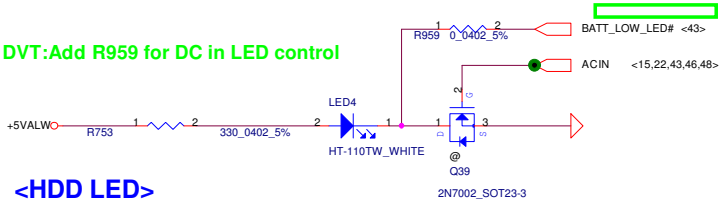
Pre MP:Update JPWR1 pin define

<Power on LED>

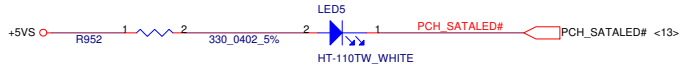


<AC in LED>

DVT:Add R959 for DC in LED control

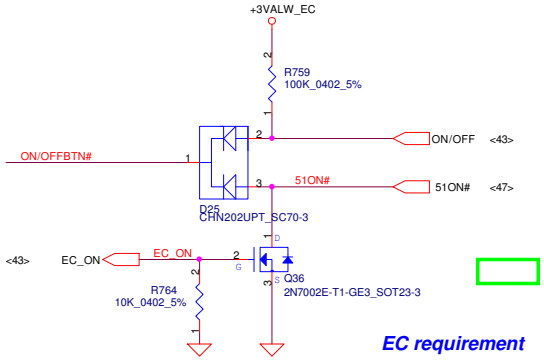


<HDD LED>



Power Button

DVT:R759 pin1 +3VALW-->+3VALW_EC



DVT:Del R937

EC requirement

Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: KB/TP/LED/FUNC

Size	Document Number	Rev
B		1.0

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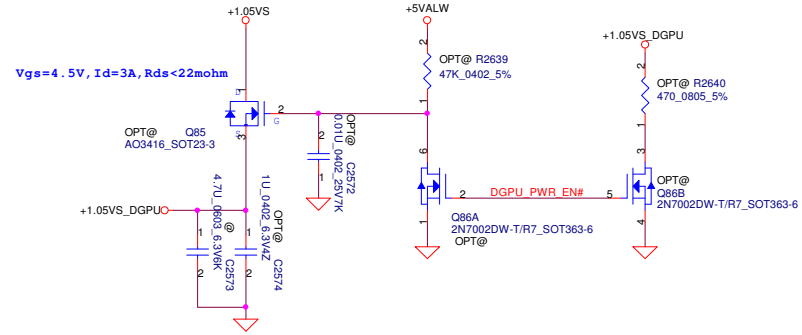
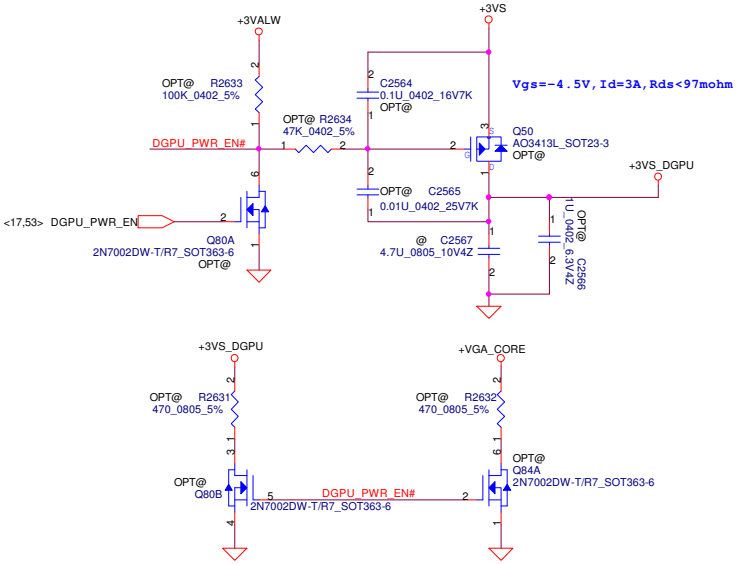
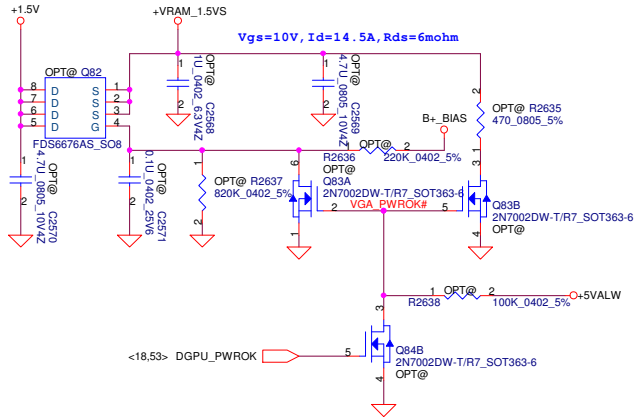
+1.05VS to +1.05VS_DGPU



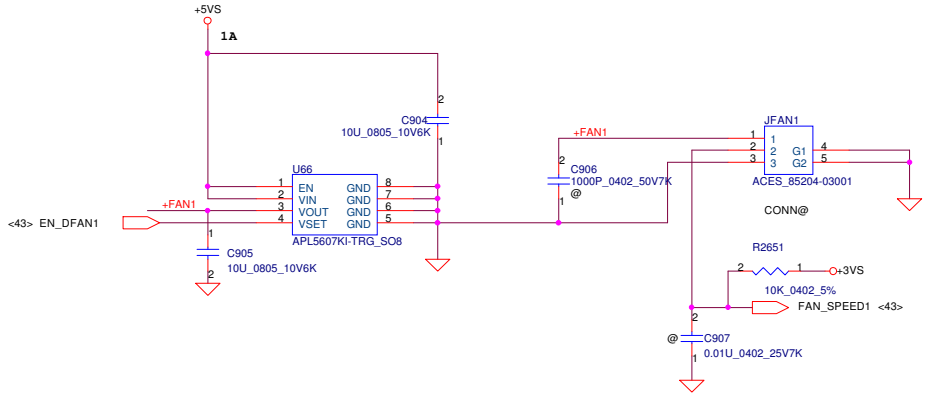
+3VS TO +3VS_DGPU



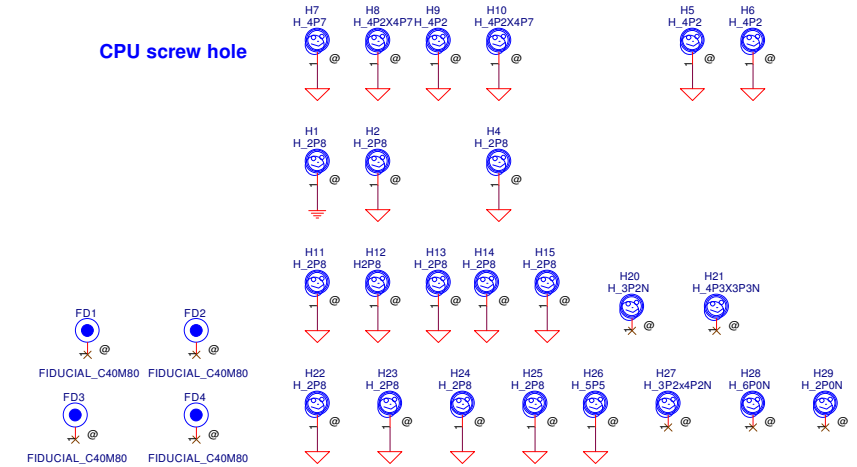
+1.5V to +VRAM_1.5VS



FAN Connector



CPU screw hole



Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: Optimus Power/FAN/Screw Hole

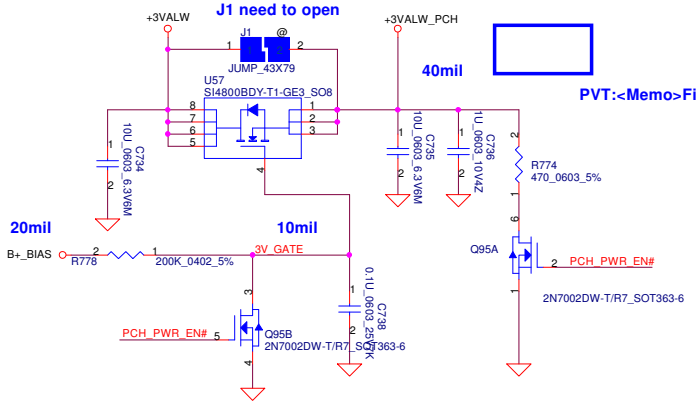
Size	Document Number	Rev
Custom		1.0

Date: Sunday, April 10, 2011 | Sheet 45 of 56

+3VALW TO +3VALW(PCH AUX Power)

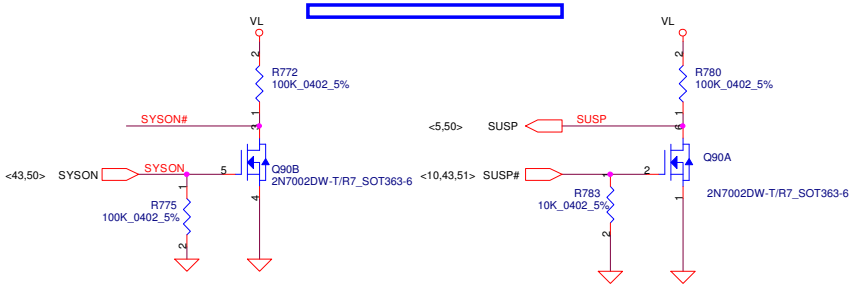
Short J1 for PCH VCCSUS3.3

J1 need to open

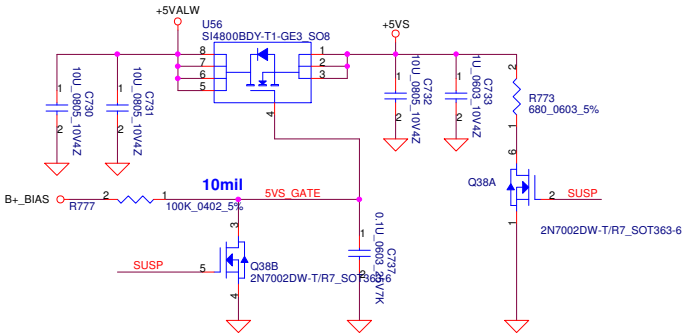


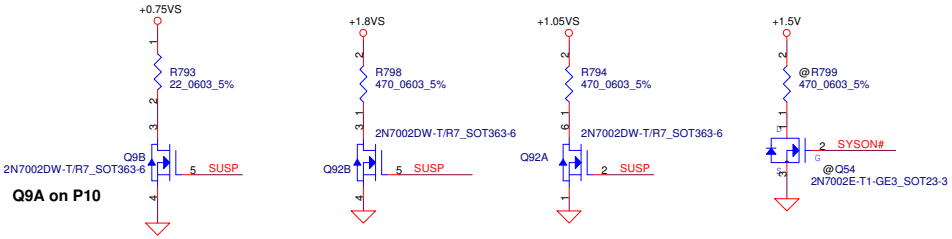
PVT:<Memo>Fine tune +3VALW_PCH power

PVT:R780 R772 +5VALW-->VL

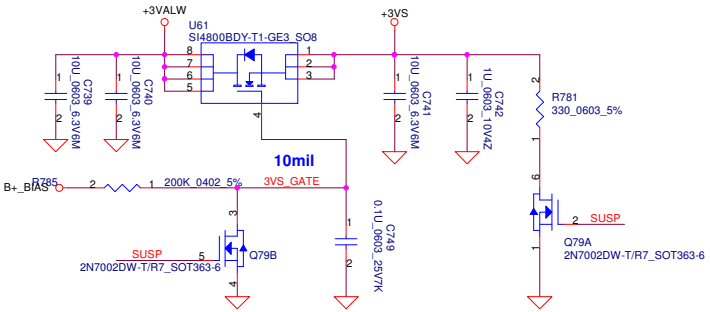


+5VALW TO +5VS

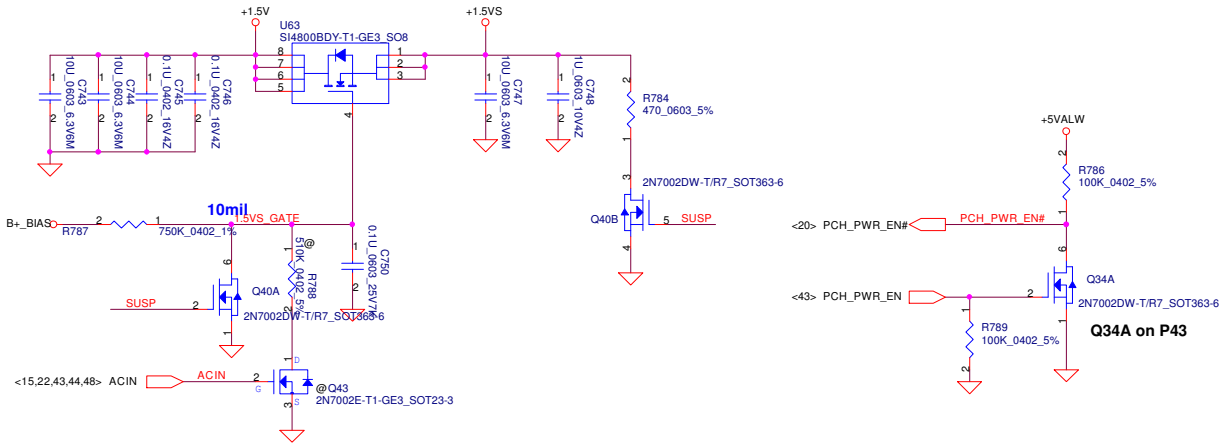




+3VALW TO +3VS



+1.5V to +1.5VS



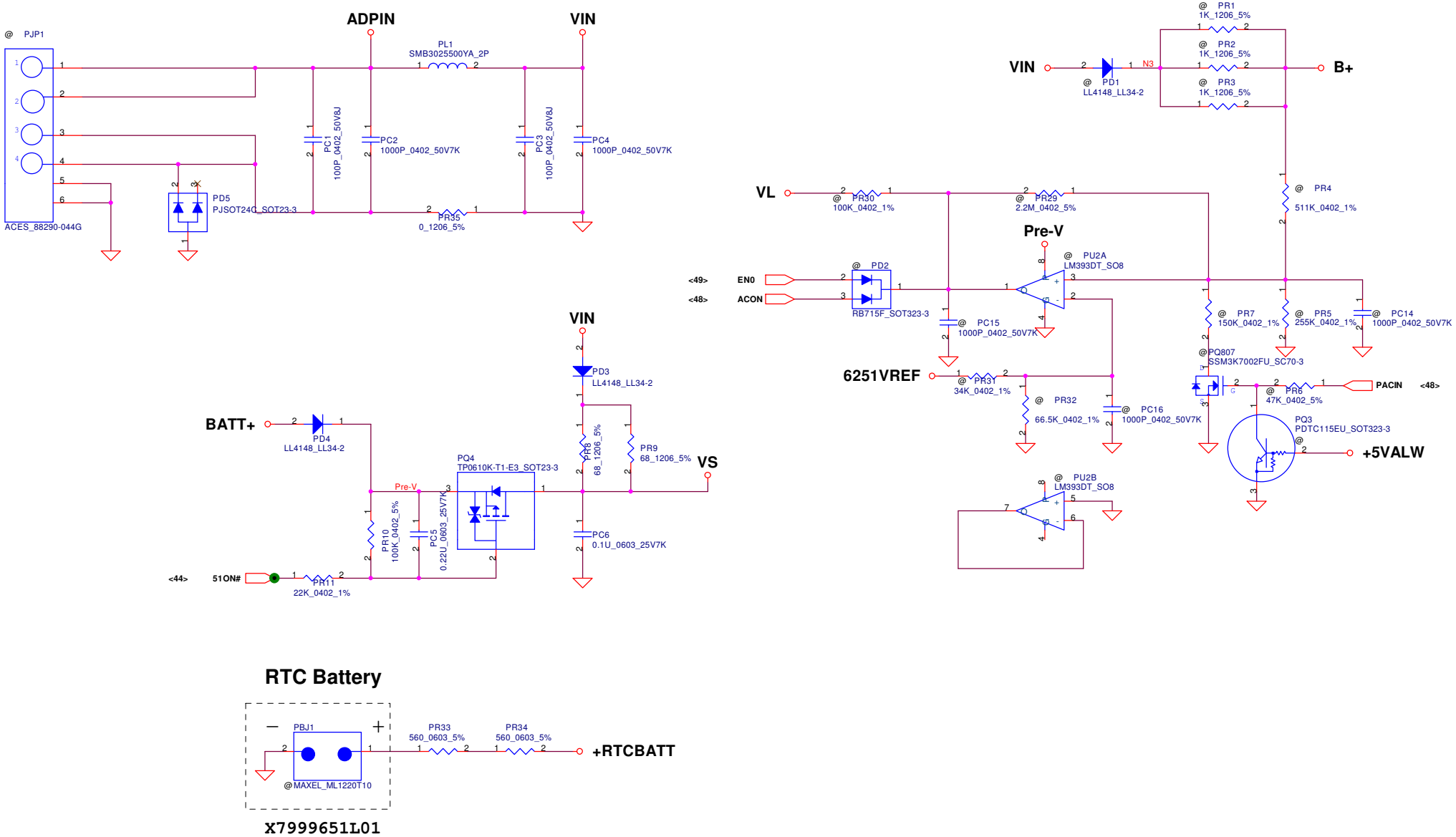
Security Classification	Compal Secret Data		
Issued Date	2010/08/23	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: DC-DC Interface

Size: Custom | Document Number | Rev: 1.0

Date: Sunday, April 10, 2011 | Sheet 46 of 56

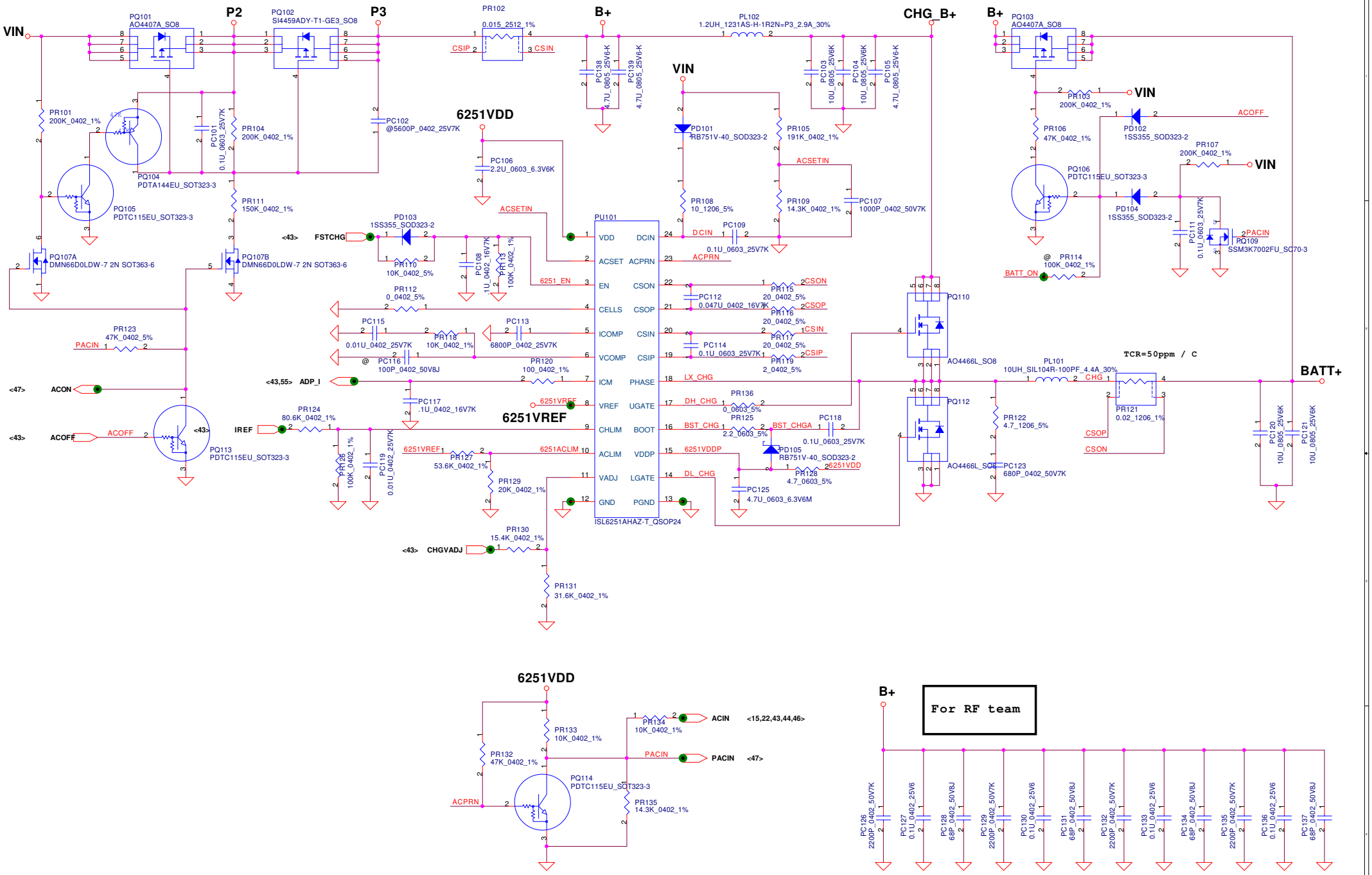


Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title: **PWR-DCIN / Pre-Charge / RTC**

Size	Document Number	Rev
Custom	DB-806P	0.1

Date: Monday, April 11, 2011 Sheet 47 of 56



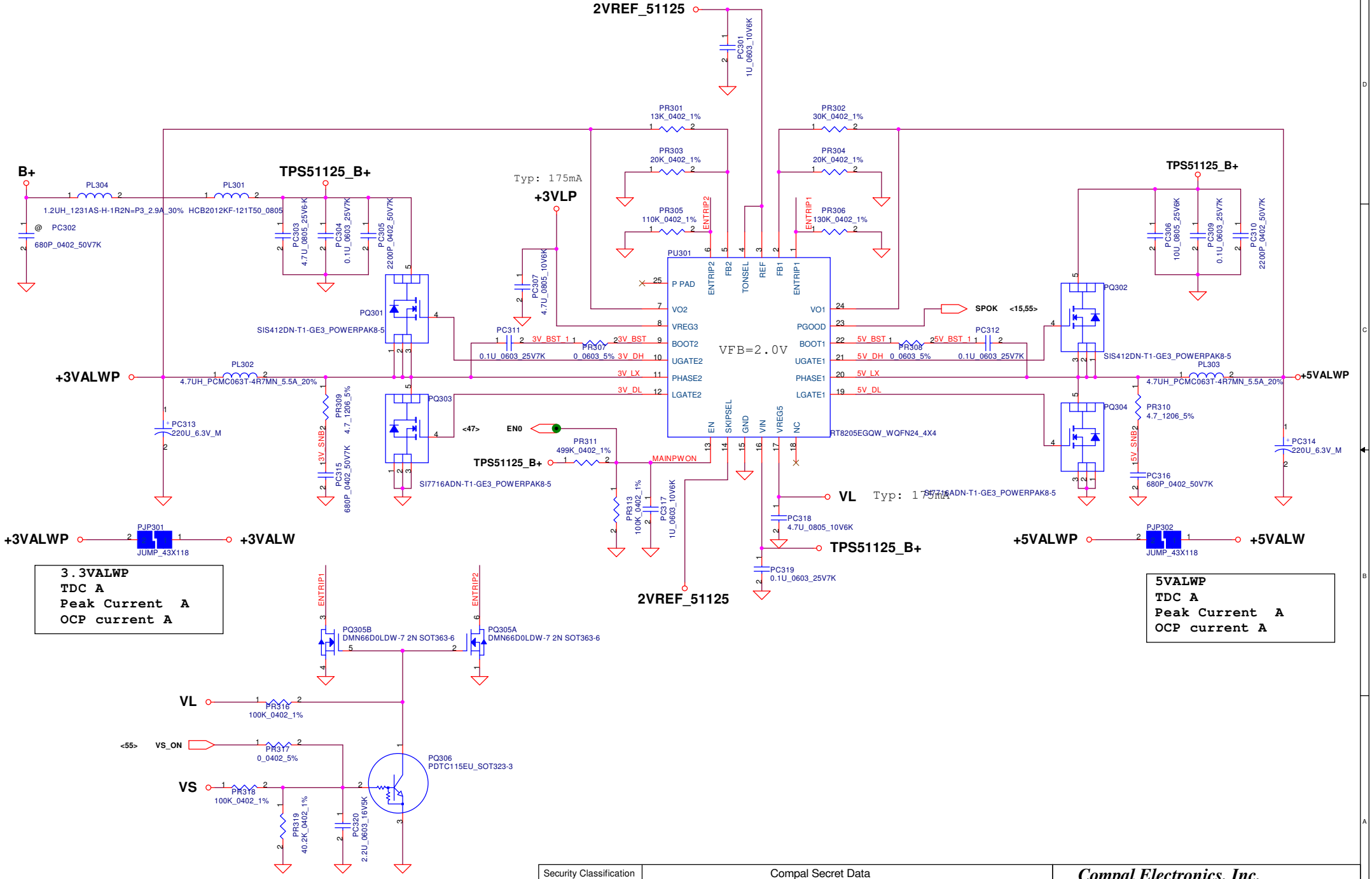
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **PWR-CHARGER**

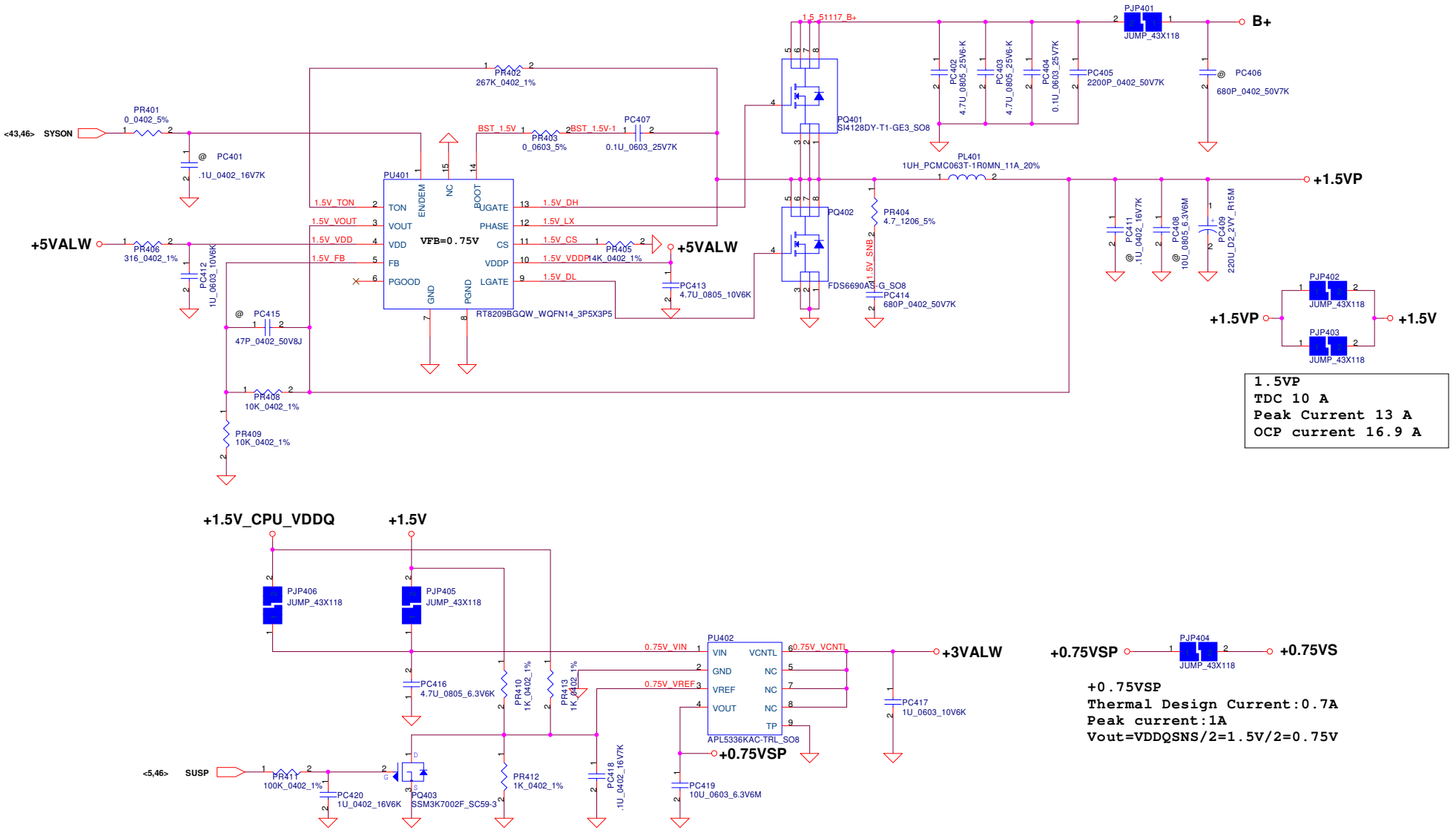
Size: Custom | Document Number: **DB-806P** | Rev: 0.1

Date: Monday, April 11, 2011 | Sheet 48 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: PWR-3VALWP/5VALWP			
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011		Sheet 49 of 56	



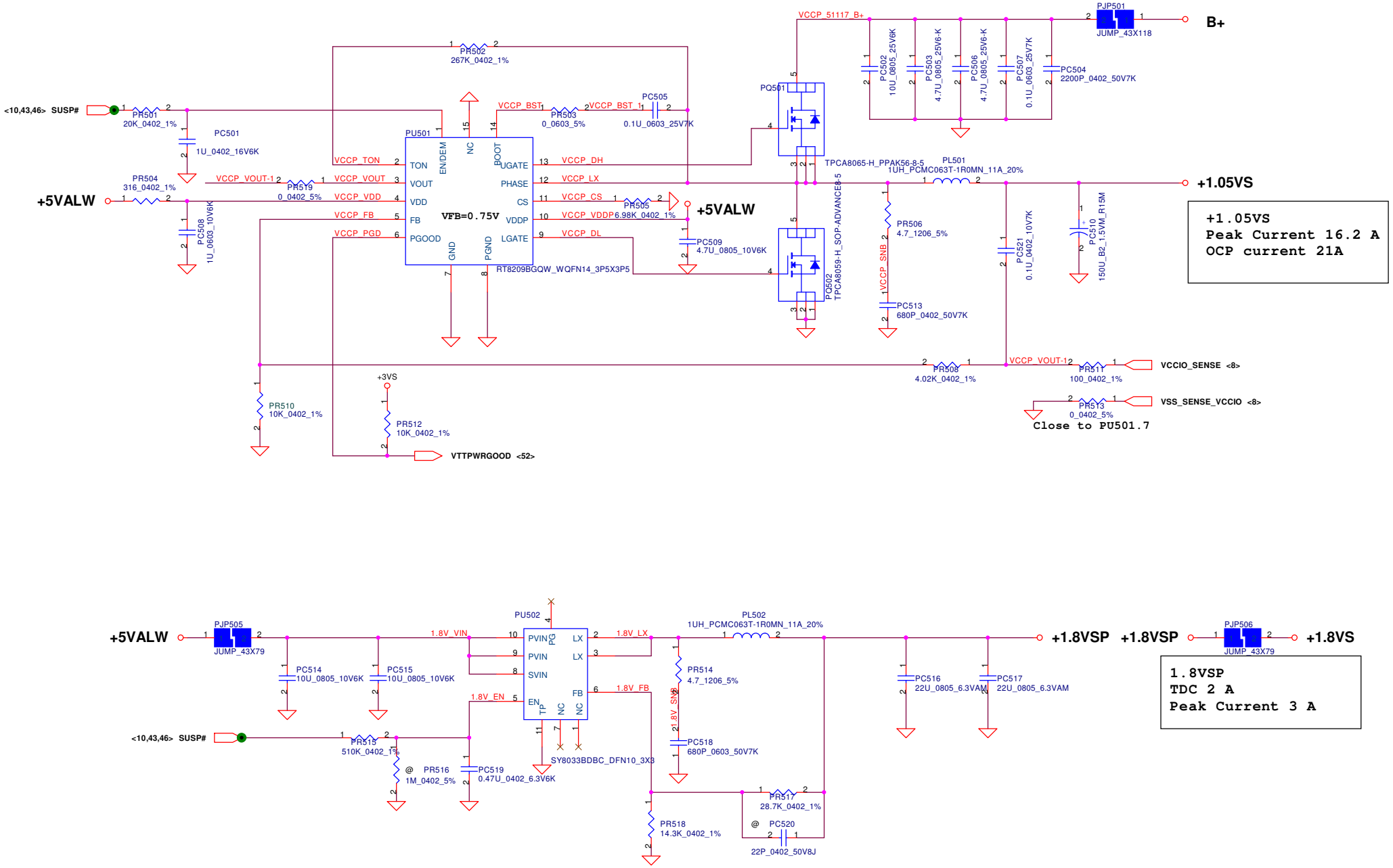
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PWR-1.5VP/0.75VSP

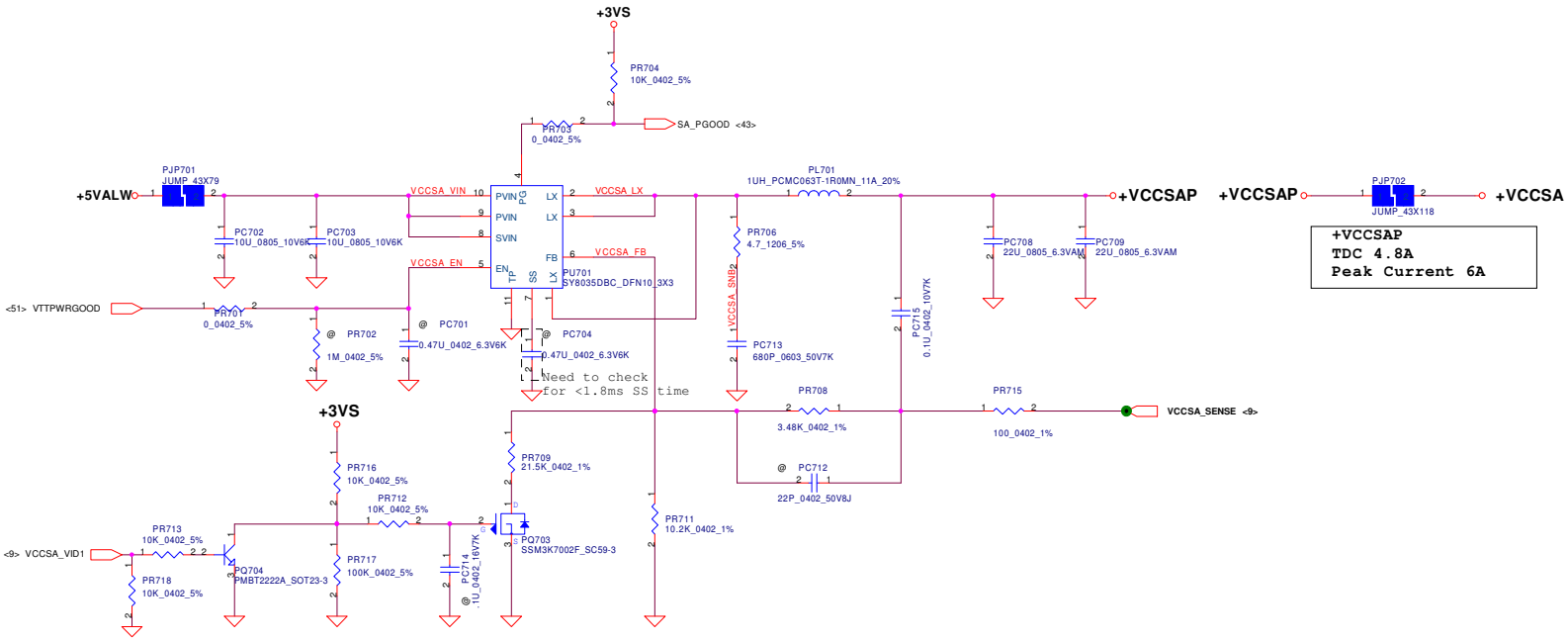
Size	Document Number	Rev
Custom		0.1

Date: Sunday, April 10, 2011 | Sheet 50 of 56



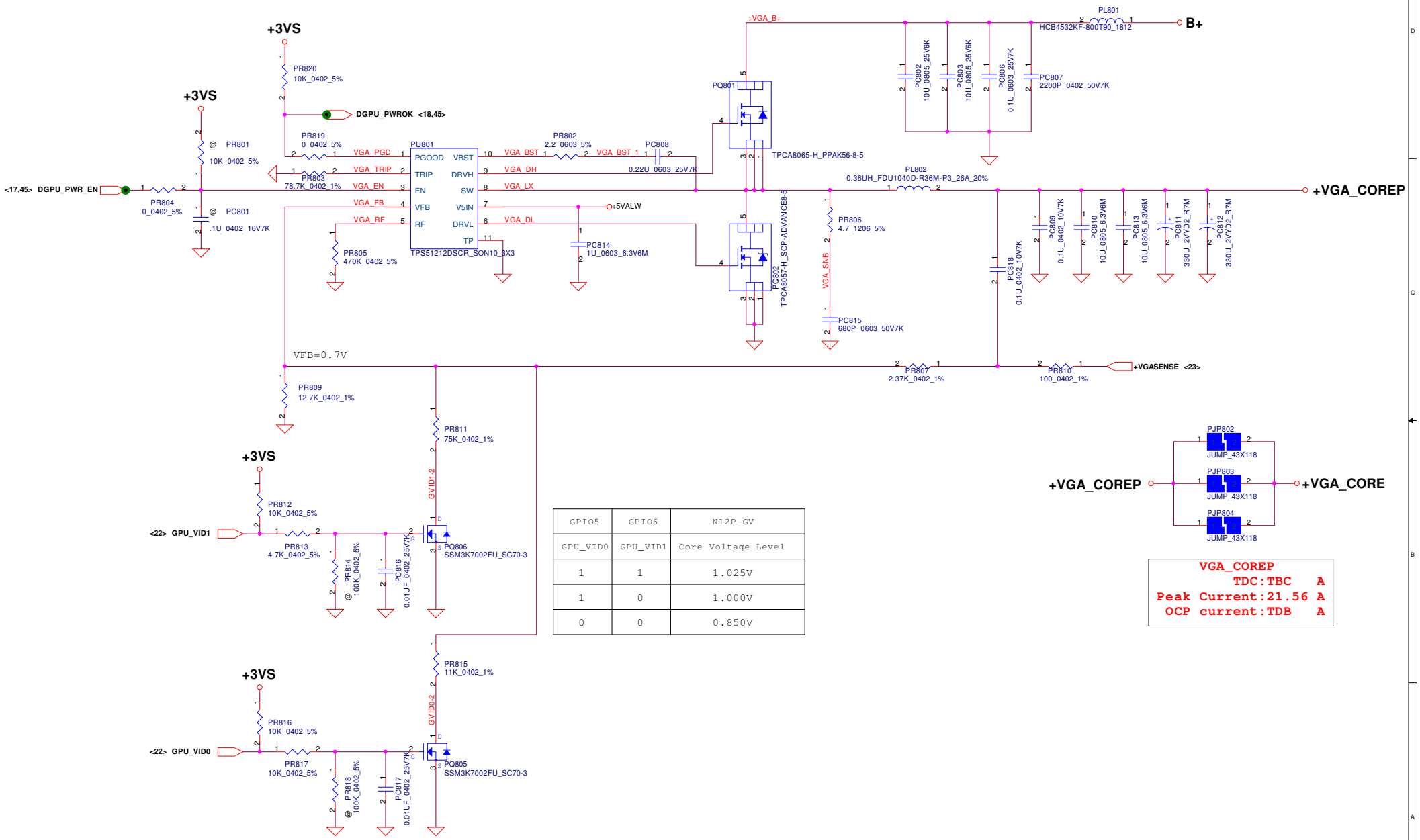
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: PWR-VCCPP/1.8VSP			
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011		Sheet 51 of 56	



VID[1]	VCCSA Vout	Required	Require on 2012	
0	0.9V		Yes	Yes
1	0.8V		Yes	Yes

Compal Electronics, Inc.			
Title: PWR-VCCSAP			
Size: C	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011		Sheet 52 of 56	



GPIO5	GPIO6	N12P-GV
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	1.025V
1	0	1.000V
0	0	0.850V

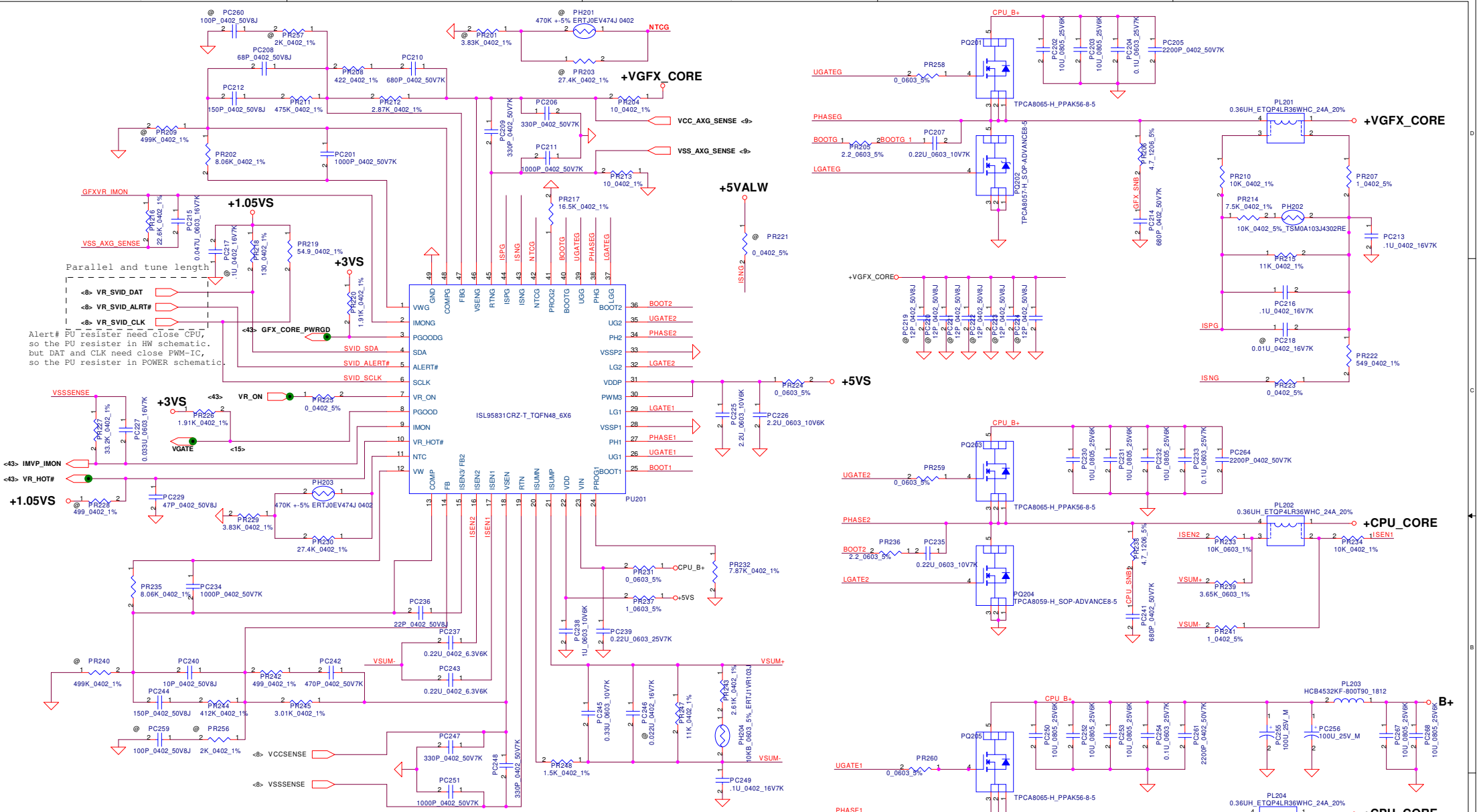
VGA_COREP
TDC:TBC A
Peak Current:21.56 A
OCP current:TDB A

Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title: ***PWR-VGA_CORE***

Size	Document Number	Rev
Custom	***DB-806P***	0.1

Date: Monday, April 11, 2011 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title: **PWR-CPU_CORE/GFX_CORE**

Size	Document Number	Rev
Custom	DB-806P	0.1

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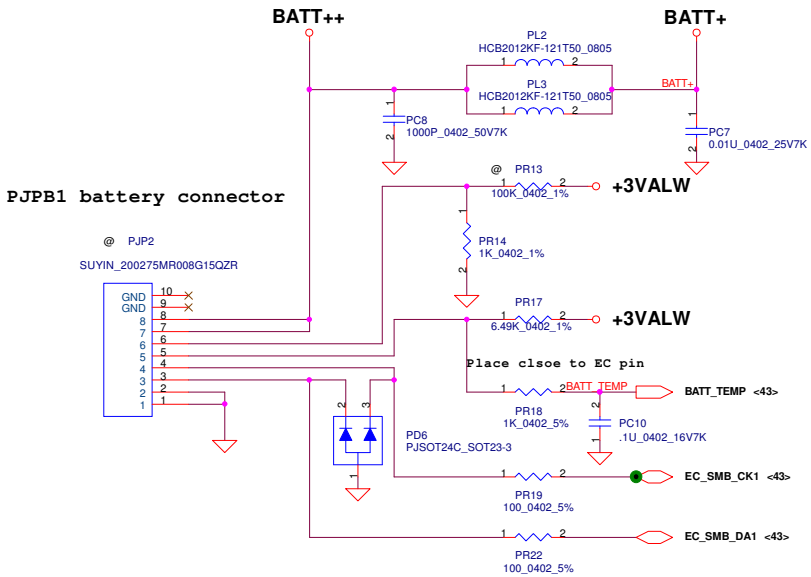
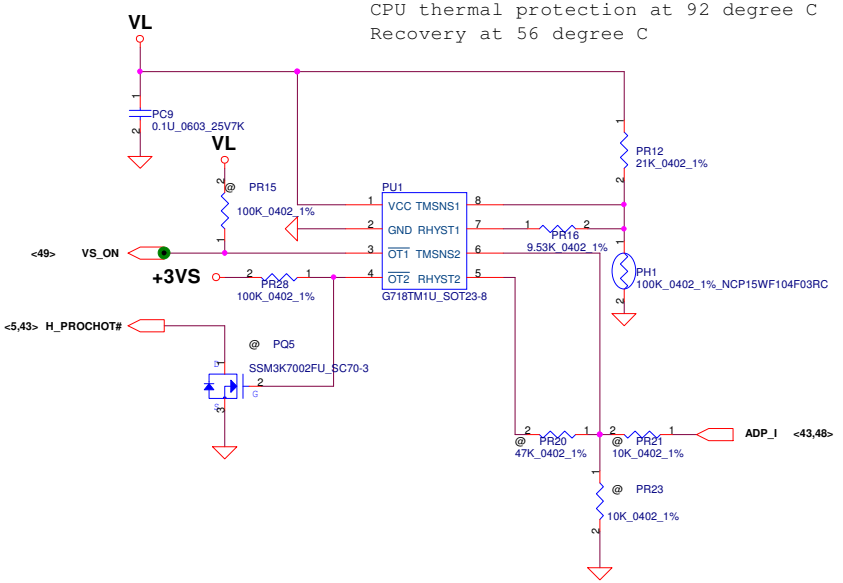
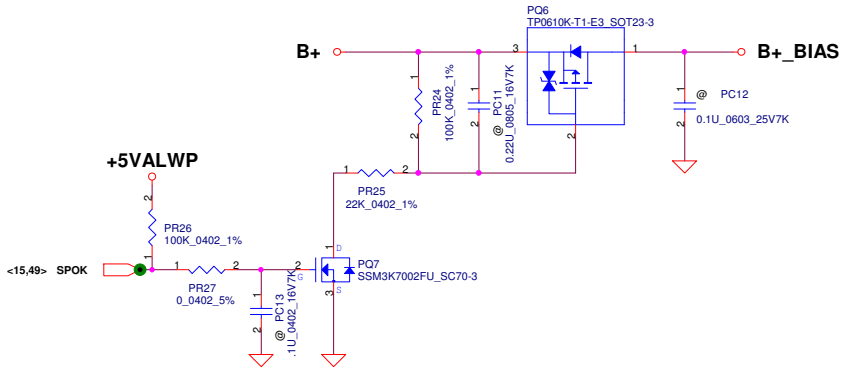


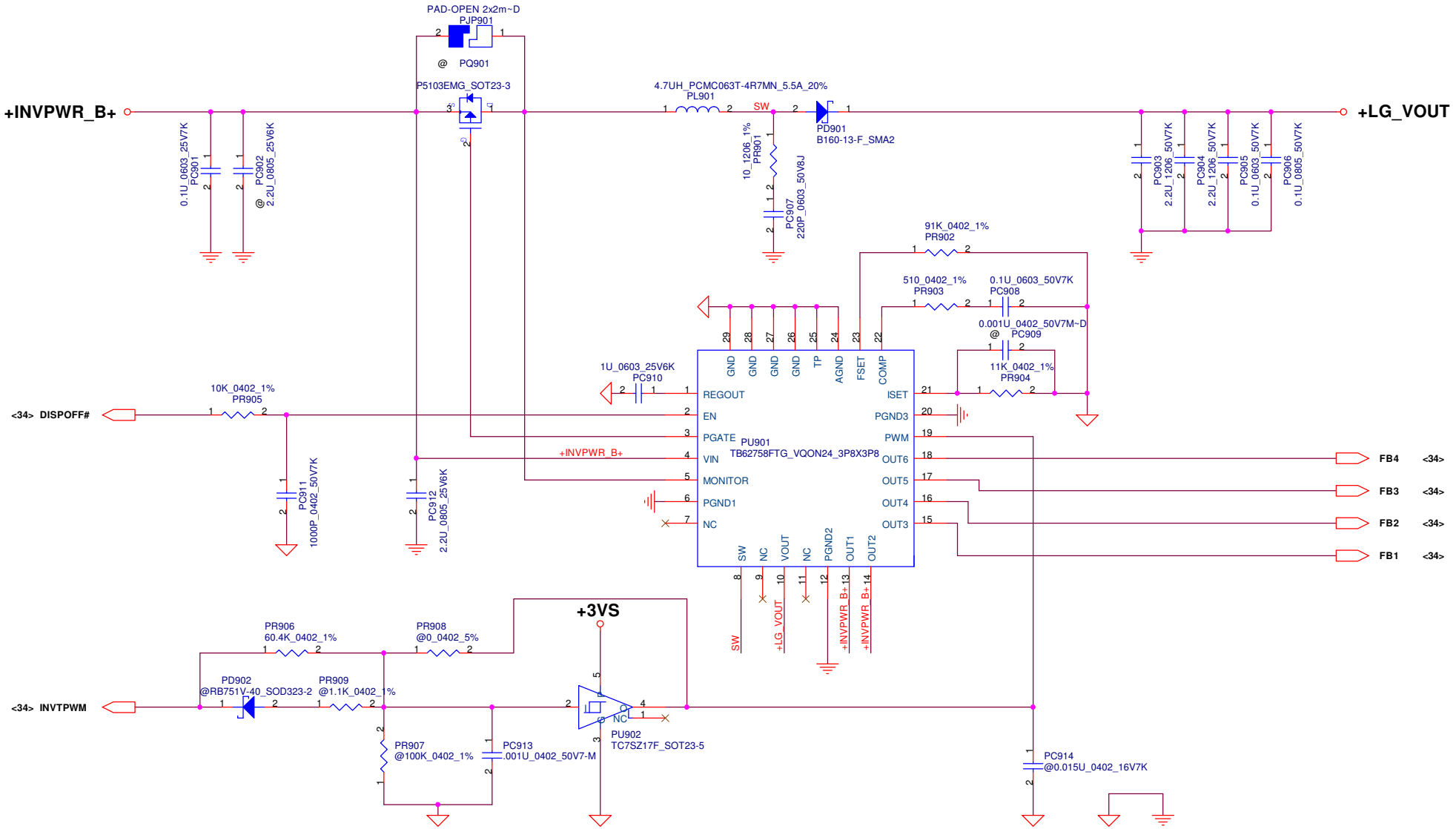
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN		
Size: Custom	Document Number: DB-806P		Rev: 0.1
Date: Monday, April 11, 2011	Sheet 55 of 56		



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Title	PWR-LED Converter		
Size B	Document Number DB-806P		Rev 0.1
Date: Sunday, April 10, 2011	Sheet 56 of 56		