

Compal Confidential

PAWGC/D Schematics Document

AMD APU Ontario-FT1 + FCH Hudson-M1 + GPU Roberson XT

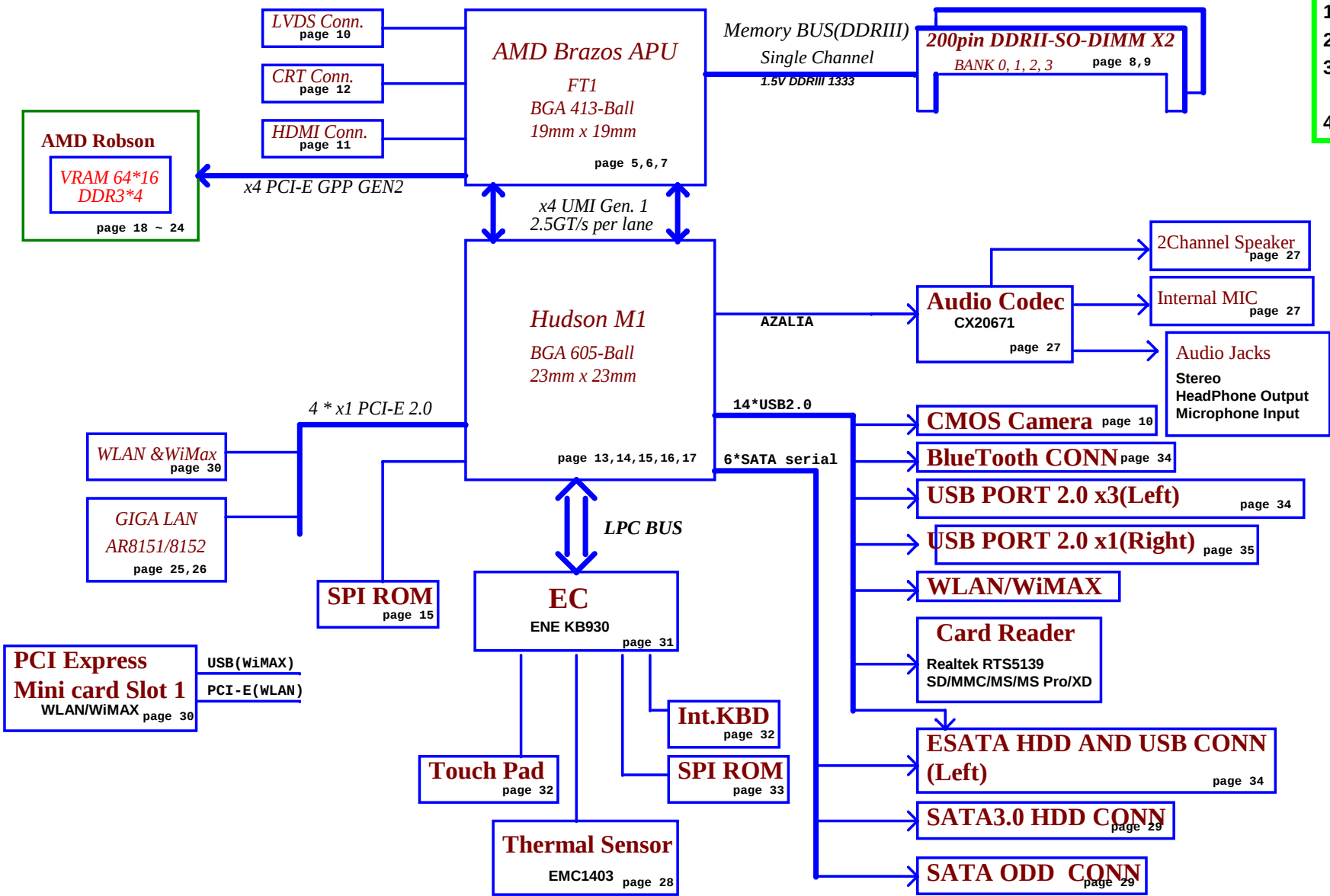
2010-11-10

REV:1.0

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For PAWGC
1. POWER BOARD
2. Card Reader BOARD

For PAWGD
1. POWER BOARD
2. Card reader BOARD
3. 4*LED+SW(3pin)
+SW(4pin) BOARD
4. ODD BOARD



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	EMC1412-2 (dGPU)	1111-100xb	F8H
			EMC1403-2(DDR,WLAN)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left USB1
Port1	USB Camera
Port2	Left(Combo)
Port3	Left USB2
Port4	Right USB
Port5	BT
Port6	CardReader
Port7	Mini-PCIE
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

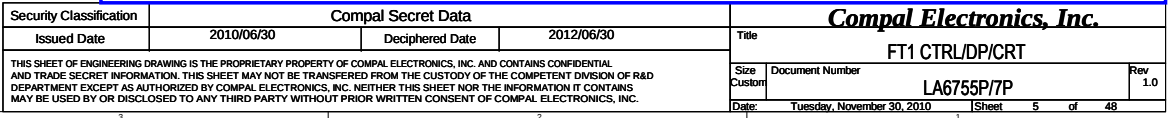
FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	eSATA
SATA3	NC
SATA4	NC
SATA5	NC

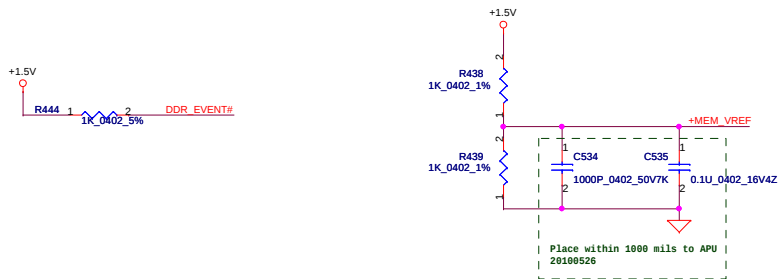
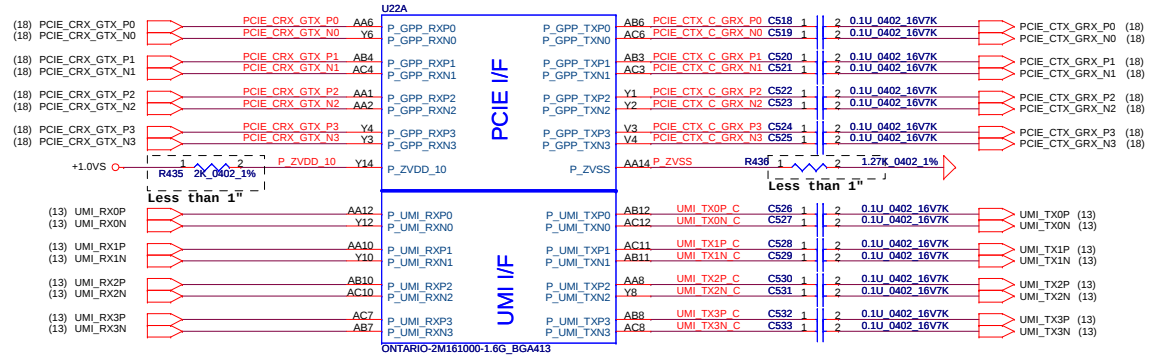
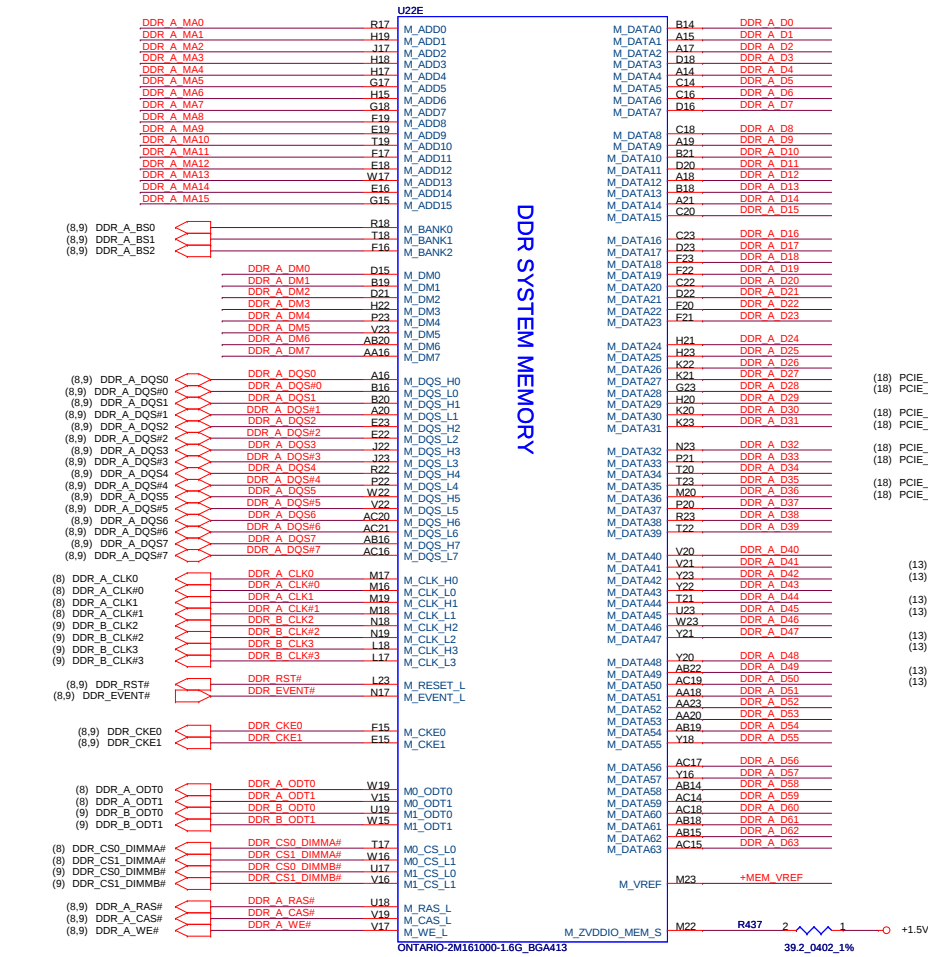
BOM Structure

UMA@ : UMA only
PX@ : DIS muxluss
 - PX3@ : PX3.0 only
 - BACO@ : Baco only

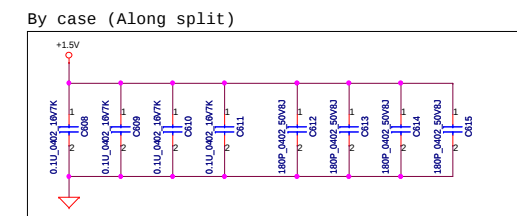
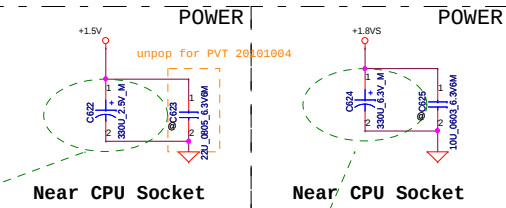
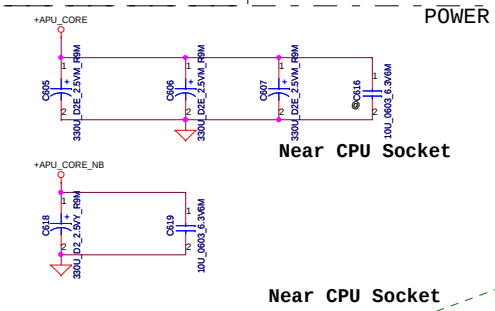
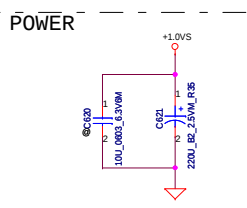
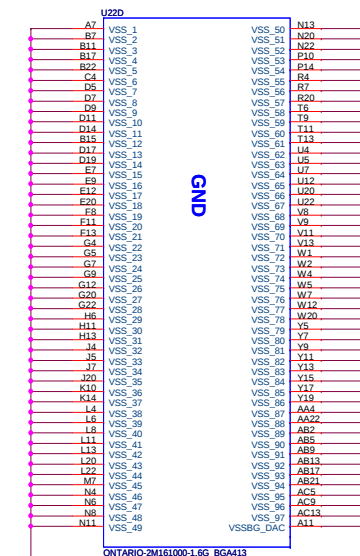
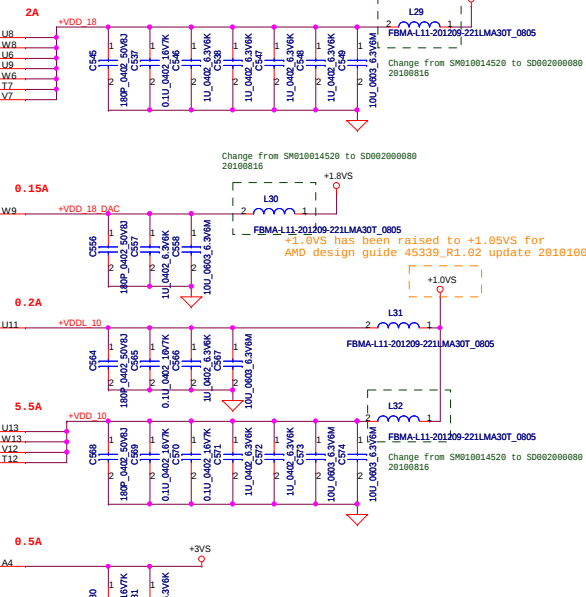
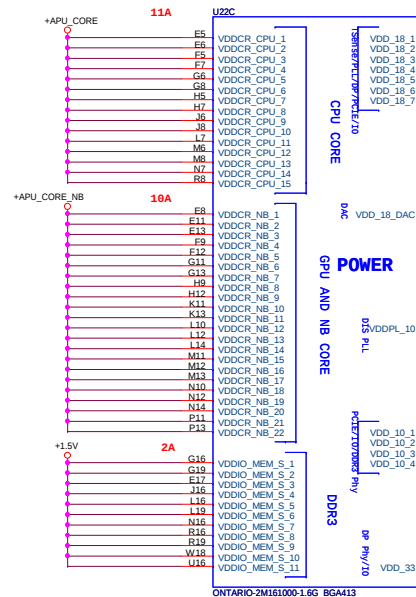
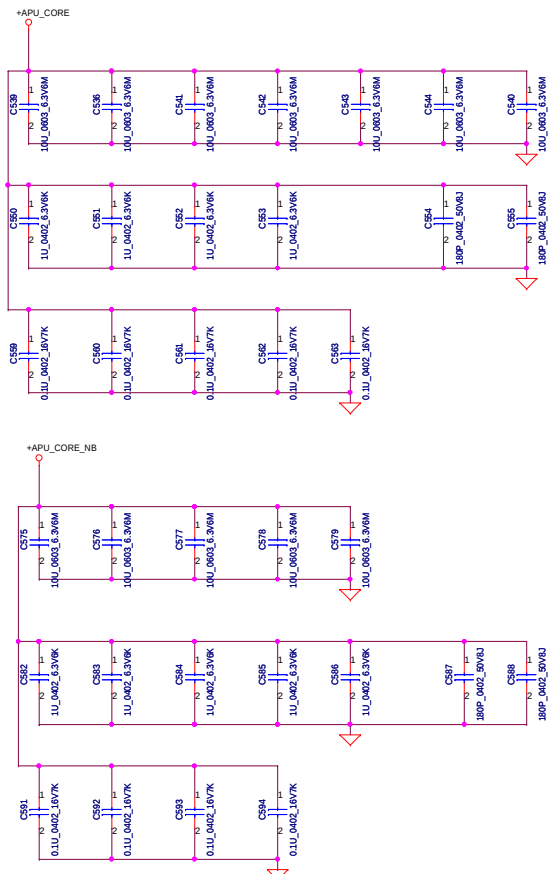
GIGA@ : AR8151
8152@ : AR8152
CMOS@ : USB camera
HDMI@ : HDMI function
nonHDMI@ : w/o HDMI function
ESATA@: eSATA function
BT@ : BT function
ME@ : ME components
X76@, H1G@, H512@, S1G@, S512@ : VRAM
45@ : 45 Level
HWM@ : hardware monitor function
nonHWM@: w/o hardware monitor function

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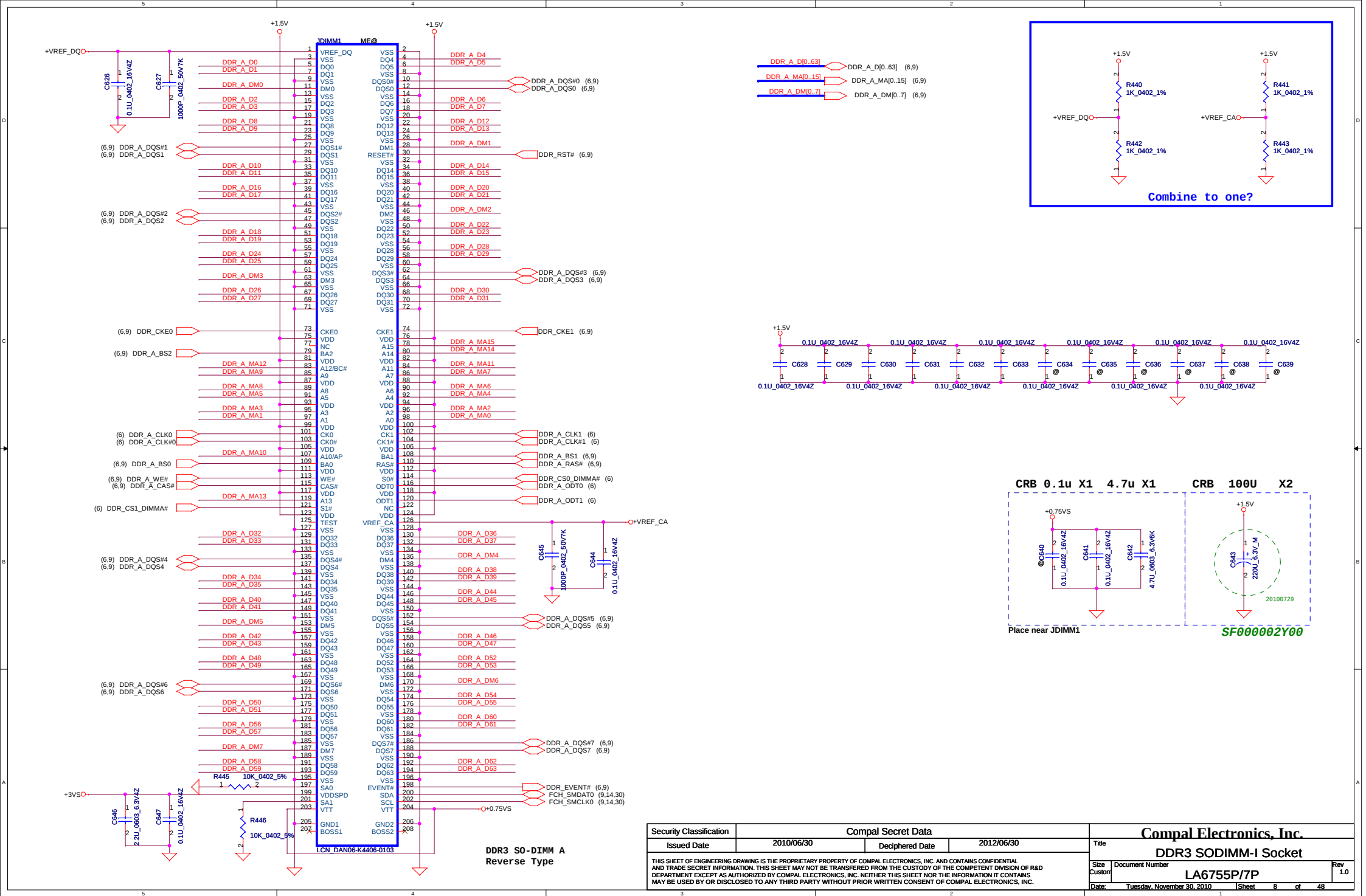


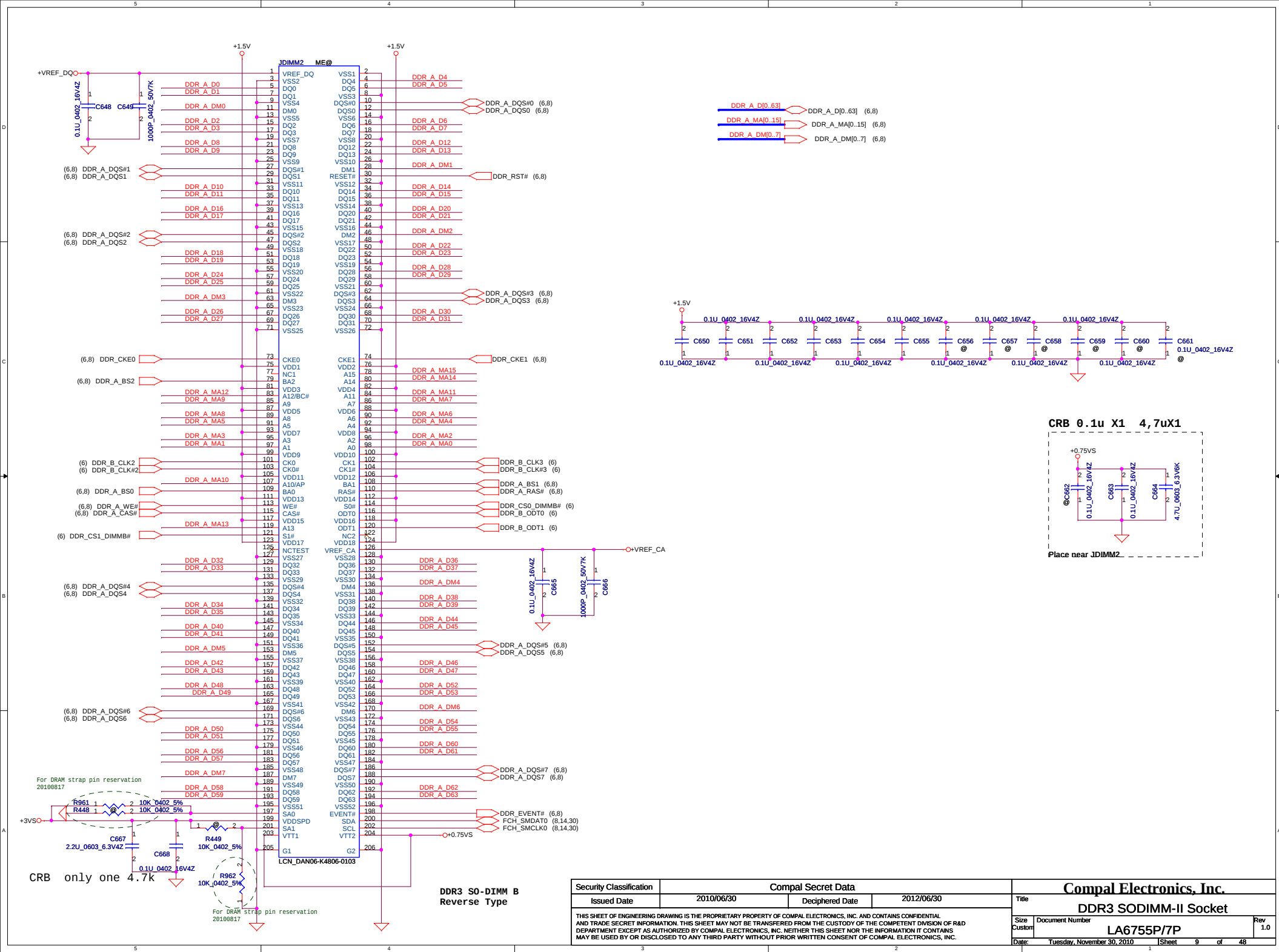
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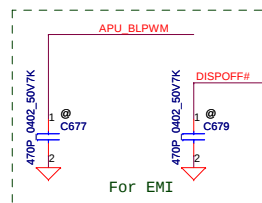
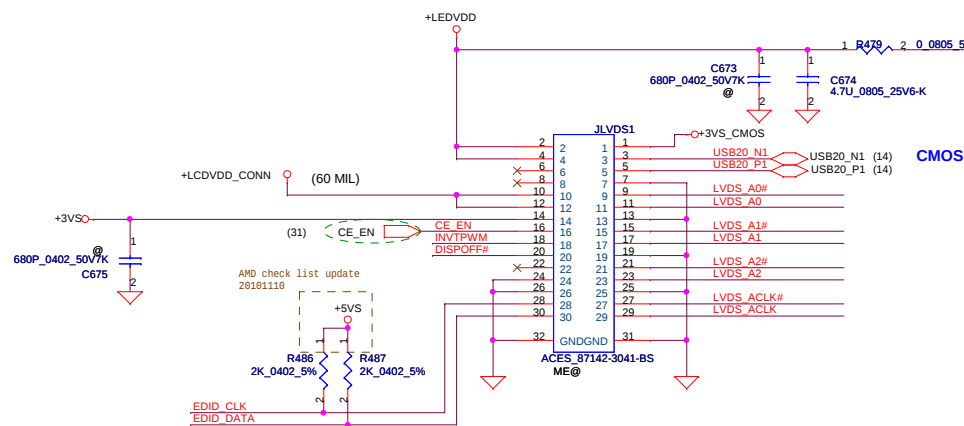
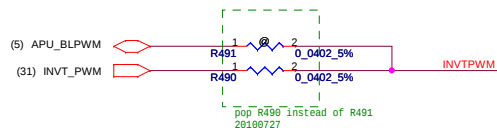
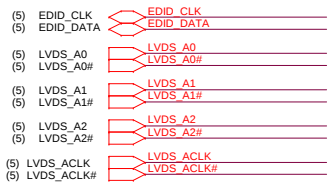
$(330\mu F \ 6.3V \ 4.2L \ ESR17m) * 1 = (SF000002200)$
 $(S \ ELE \ CAP \ 330\mu \ 6.3V \ M \ 6.3X5.9 \ LESR15M \ VU) * 1 = (SF000002000)$
 20100813

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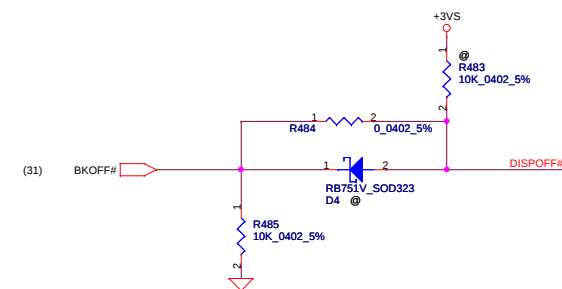
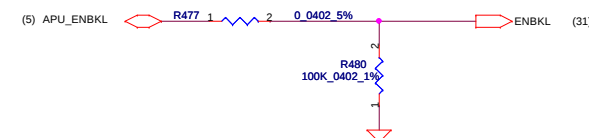
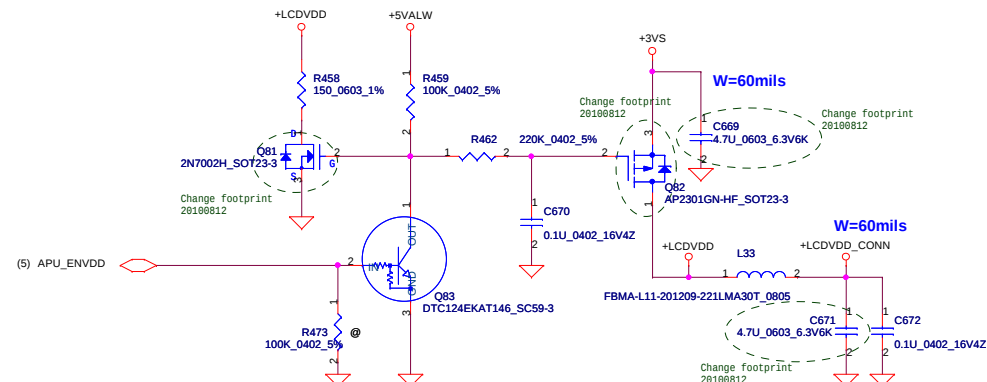




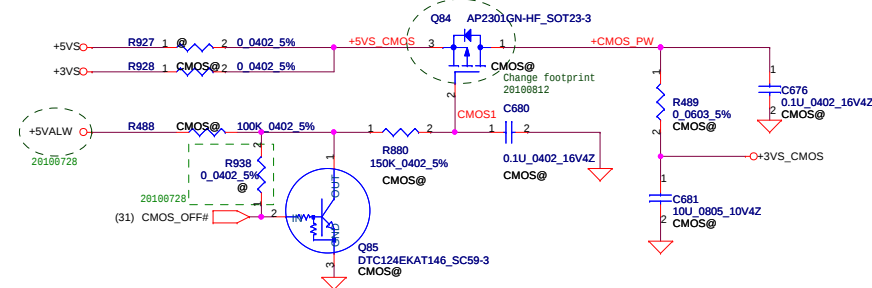
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								DDR3 SODIMM-II Socket					
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LCD POWER CIRCUIT

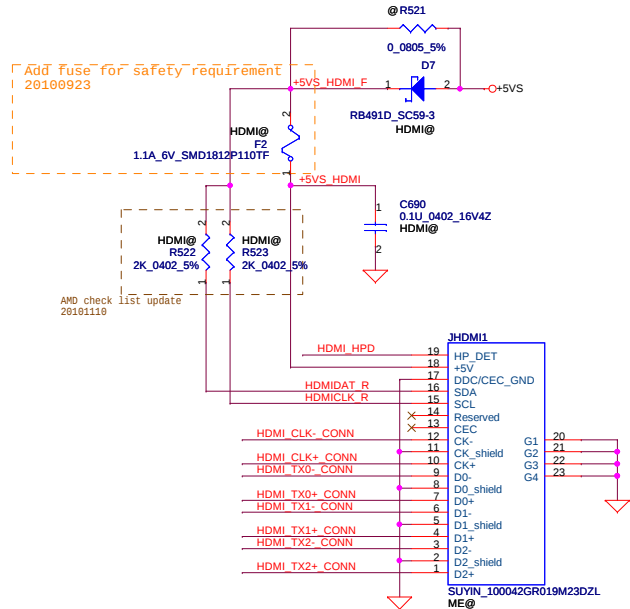
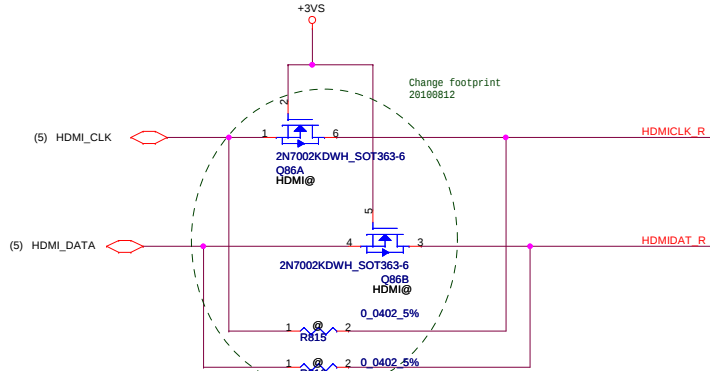
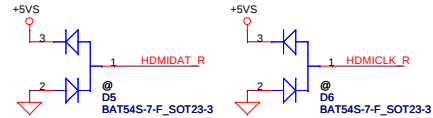
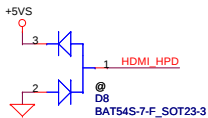
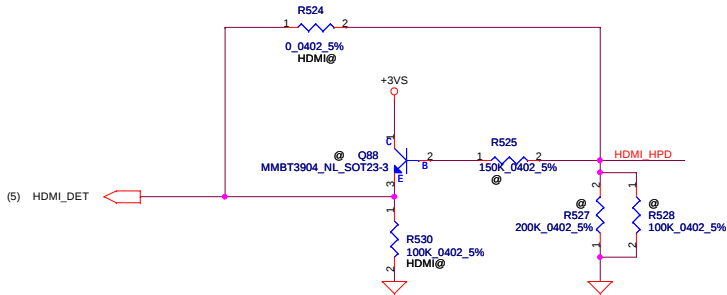
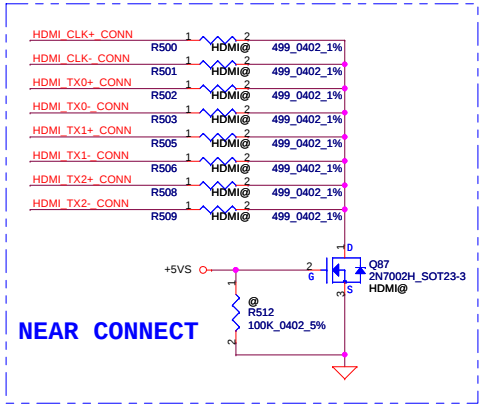
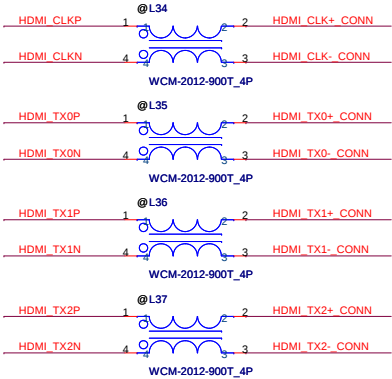


CMOS Camera

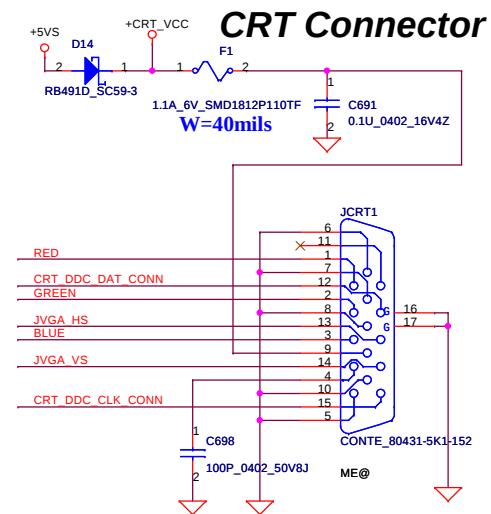
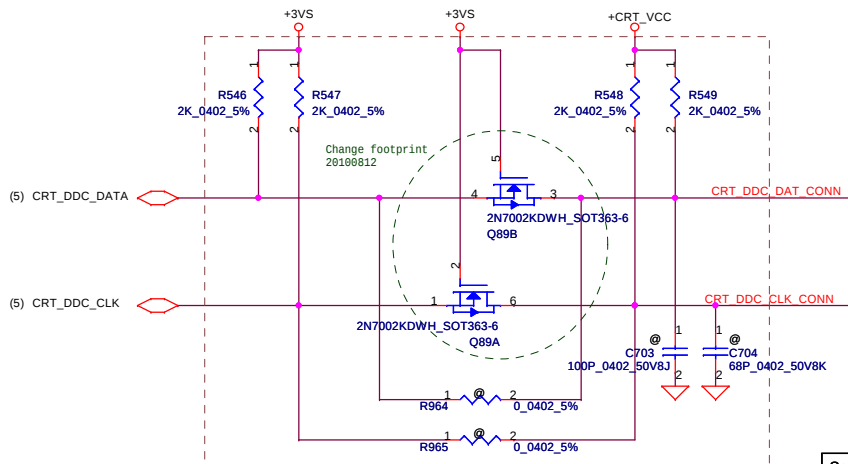
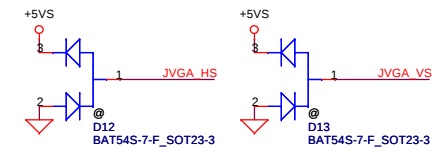
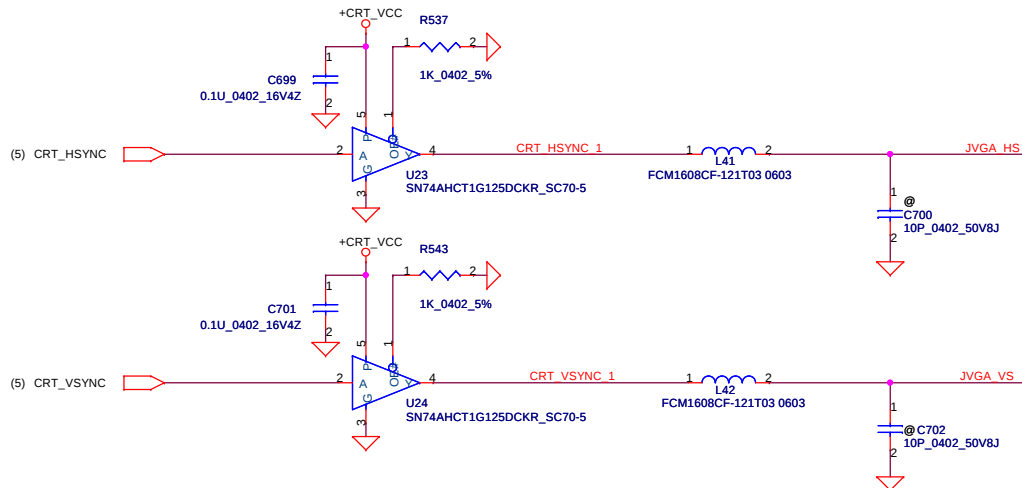
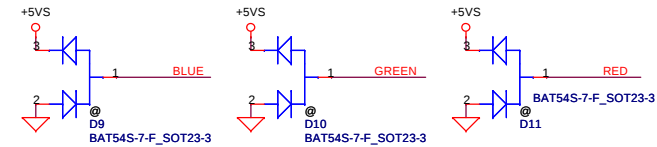
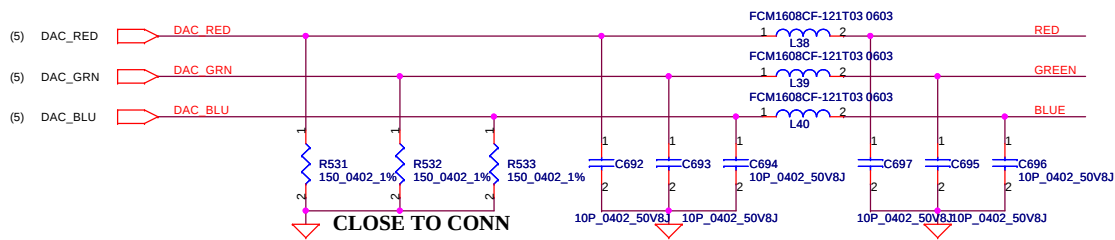


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								LVDS/CAMERA	
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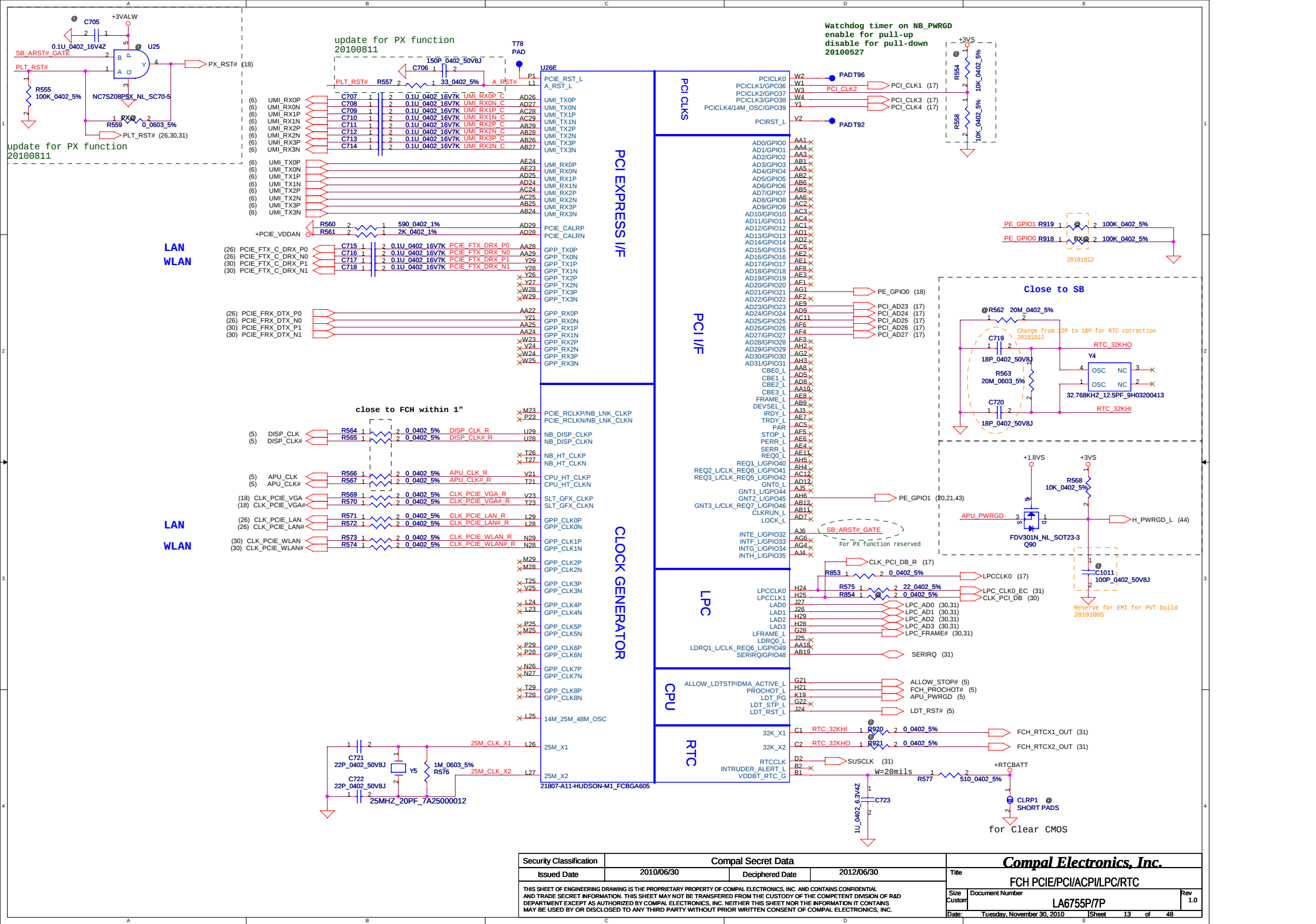
(5) HDMI_CLKP	R513	1	HDMI@	2	0_0402_5%	HDMI_CLK+ CONN
(5) HDMI_CLKN	R514	1	HDMI@	2	0_0402_5%	HDMI_CLK- CONN
(5) HDMI_TX0P	R515	1	HDMI@	2	0_0402_5%	HDMI_TX0+ CONN
(5) HDMI_TX0N	R516	1	HDMI@	2	0_0402_5%	HDMI_TX0- CONN
(5) HDMI_TX1P	R517	1	HDMI@	2	0_0402_5%	HDMI_TX1+ CONN
(5) HDMI_TX1N	R518	1	HDMI@	2	0_0402_5%	HDMI_TX1- CONN
(5) HDMI_TX2P	R519	1	HDMI@	2	0_0402_5%	HDMI_TX2+ CONN
(5) HDMI_TX2N	R520	1	HDMI@	2	0_0402_5%	HDMI_TX2- CONN

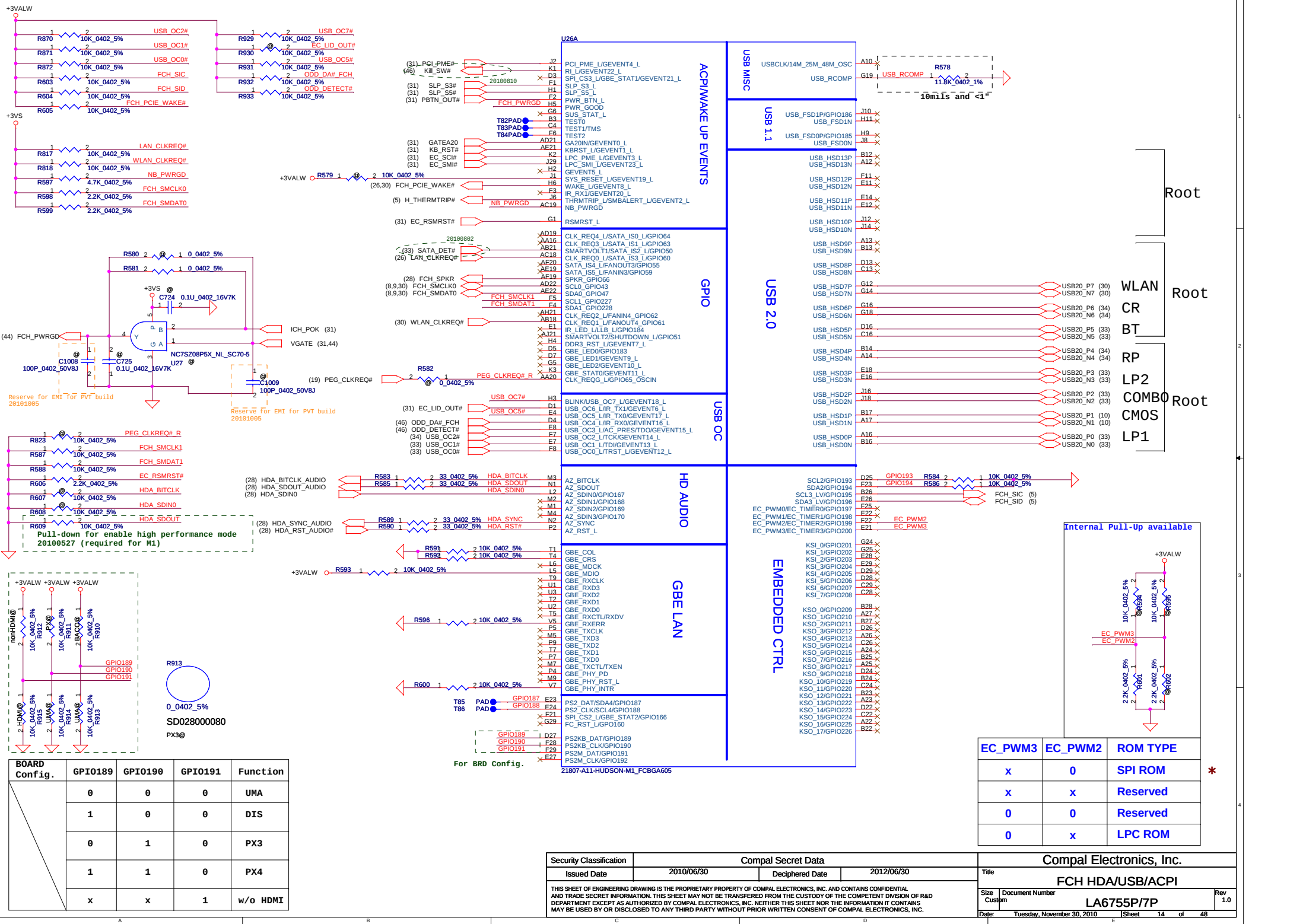


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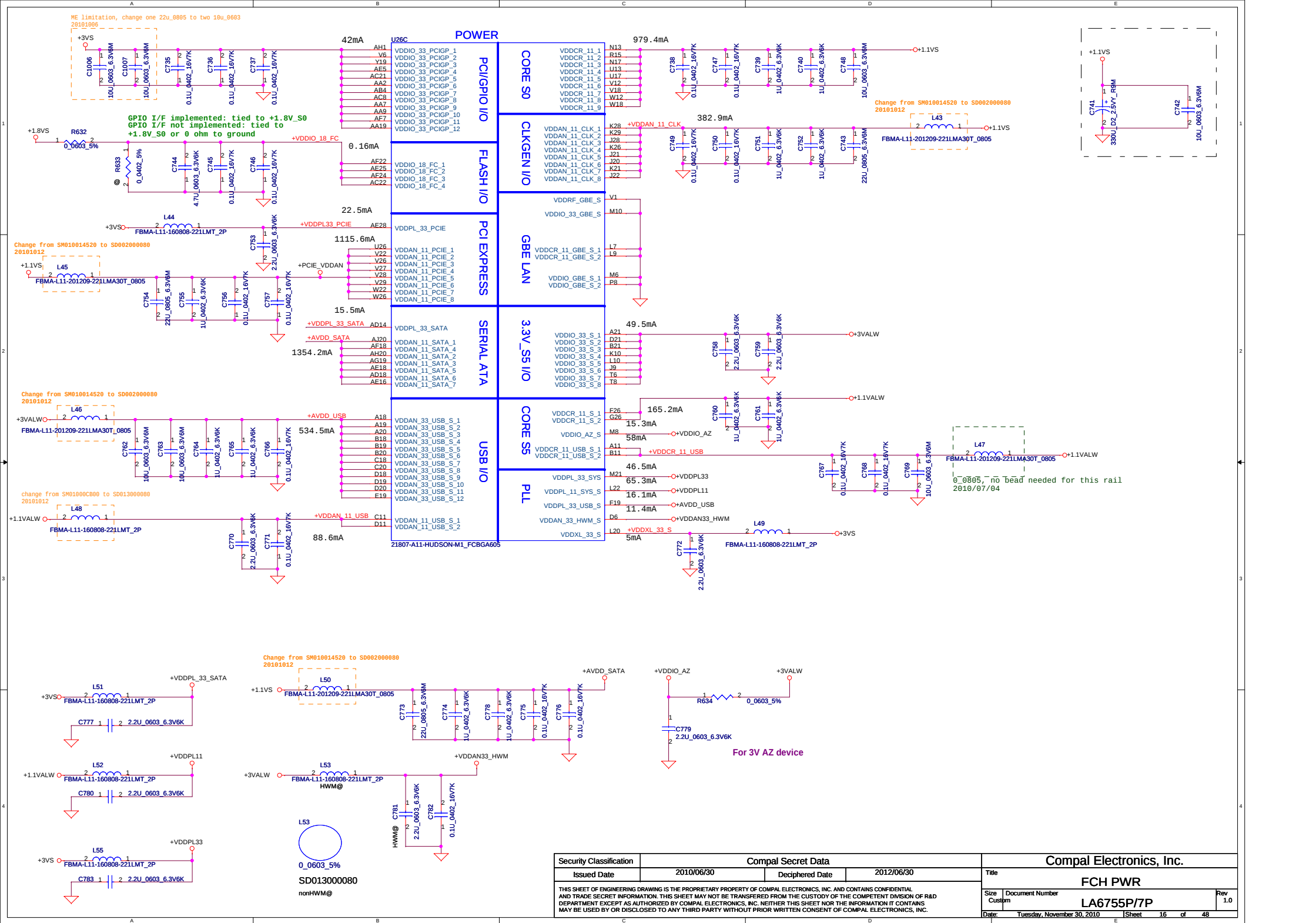




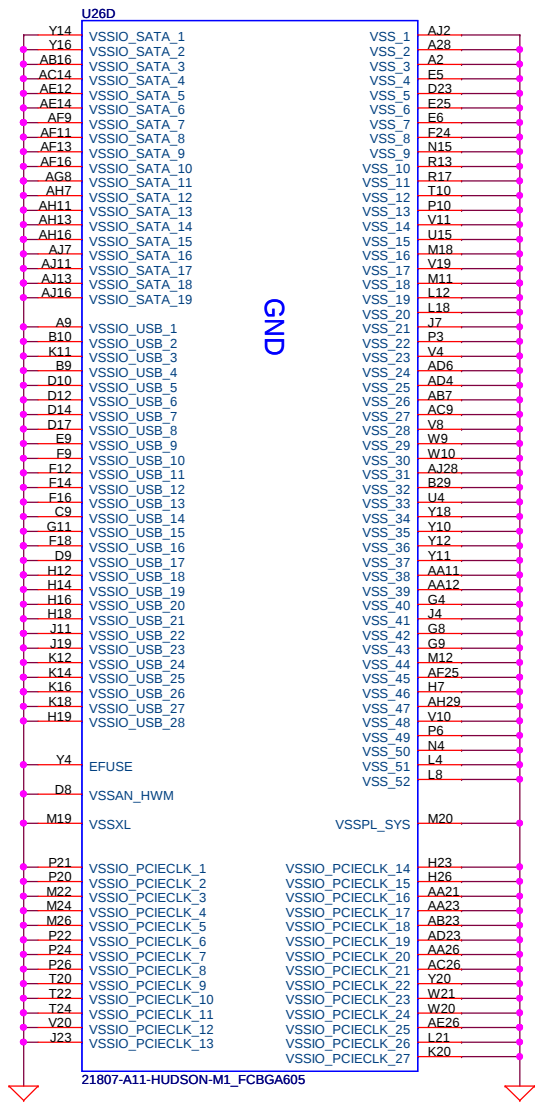
BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	0	UMA
	1	0	0	DIS
	0	1	0	PX3
	1	1	0	PX4
	x	x	1	w/o HDMII

EC_PWM3	EC_PWM2	ROM TYPE
x	0	SPI ROM
x	x	Reserved
0	0	Reserved
0	x	LPC ROM

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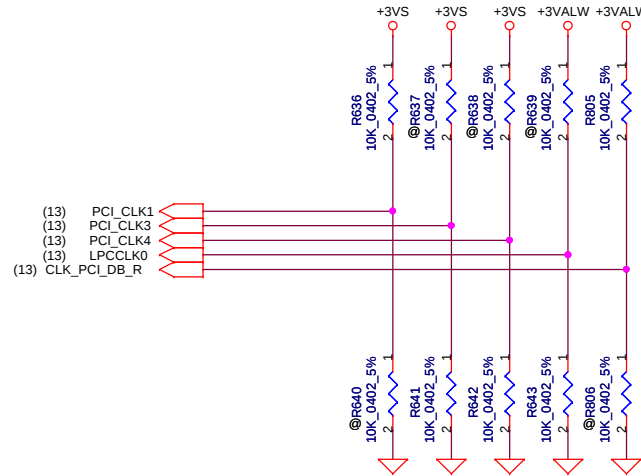
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REQUIRED STRAPS

Check Internal PU/PD

PULL HIGH	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode DEFAULT				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	CLKGEN Mode Internal DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode				



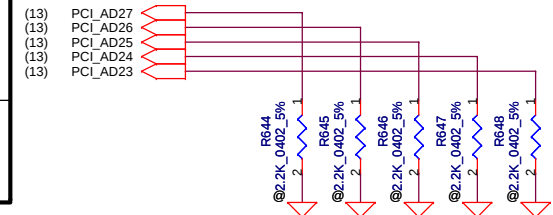
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default



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								Size B	Document Number						Rev 1.0
								LA6755P/7P							
								Date:		Tuesday, November 30, 2010		Sheet	17	of	48

(6) PCIE_CTX_GRX_P[3..0]
(6) PCIE_CTX_GRX_N[3..0]

PCIE_CTX_GRX_P[3..0]
PCIE_CTX_GRX_N[3..0]

PCIE_CTX_GRX_P0
PCIE_CTX_GRX_N0

PCIE_CTX_GRX_P1
PCIE_CTX_GRX_N1

PCIE_CTX_GRX_P2
PCIE_CTX_GRX_N2

PCIE_CTX_GRX_P3
PCIE_CTX_GRX_N3

AB30
AA31

AA29
Y28

Y30
W31

W29
V28

Y30
U31

U29
T28

T30
R31

R29
P28

P30
N31

N29
M28

M30
L31

L29
K30

(13) CLK_PCIE_VGA
(13) CLK_PCIE_VGA#

CLK_PCIE_VGA
CLK_PCIE_VGA#

(20,40,43) VGA_PWRGD

R936
R299
10K_0402_5%
PX@

update for PX function
20100811

GPU_RST#
R957
100K_0402_5%
PX@

U8A
PCIE_RX0P
PCIE_RX0N

PCIE_RX1P
PCIE_RX1N

PCIE_RX2P
PCIE_RX2N

PCIE_RX3P
PCIE_RX3N

PCIE_RX4P
PCIE_RX4N

PCIE_RX5P
PCIE_RX5N

PCIE_RX6P
PCIE_RX6N

PCIE_RX7P
PCIE_RX7N

PCIE_RX8P
PCIE_RX8N

PCIE_RX9P
PCIE_RX9N

PCIE_RX10P
PCIE_RX10N

PCIE_RX11P
PCIE_RX11N

PCIE_RX12P
PCIE_RX12N

PCIE_RX13P
PCIE_RX13N

PCIE_RX14P
PCIE_RX14N

PCIE_RX15P
PCIE_RX15N

CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

PWRGOOD

PERSTB

216-0774207-A11ROB_FCBGA631 PX@

PCI EXPRESS INTERFACE

PCIE_TX0P
PCIE_TX0N

PCIE_TX1P
PCIE_TX1N

PCIE_TX2P
PCIE_TX2N

PCIE_TX3P
PCIE_TX3N

PCIE_TX4P
PCIE_TX4N

PCIE_TX5P
PCIE_TX5N

PCIE_TX6P
PCIE_TX6N

PCIE_TX7P
PCIE_TX7N

PCIE_TX8P
PCIE_TX8N

PCIE_TX9P
PCIE_TX9N

PCIE_TX10P
PCIE_TX10N

PCIE_TX11P
PCIE_TX11N

PCIE_TX12P
PCIE_TX12N

PCIE_TX13P
PCIE_TX13N

PCIE_TX14P
PCIE_TX14N

PCIE_TX15P
PCIE_TX15N

PCIE_CALRP
PCIE_CALRN

PCIE_CALRN

216-0774207-A11ROB_FCBGA631 PX@

PCIE_CRX GTX P[3..0]
PCIE_CRX GTX N[3..0]

PCIE_CRX GTX_P[3..0] (6)
PCIE_CRX GTX_N[3..0] (6)

AH30 PCIE_CRX C GTX P0 0.1U 0402 10V7K 2 1 C273 PX@ PCIE_CRX GTX_P0
AG31 PCIE_CRX C GTX N0 0.1U 0402 10V7K 2 1 C272 PX@ PCIE_CRX GTX_N0

AG29 PCIE_CRX C GTX P1 0.1U 0402 10V7K 2 1 C274 PX@ PCIE_CRX GTX_P1
AE28 PCIE_CRX C GTX N1 0.1U 0402 10V7K 2 1 C275 PX@ PCIE_CRX GTX_N1

AE27 PCIE_CRX C GTX P2 0.1U 0402 10V7K 2 1 C276 PX@ PCIE_CRX GTX_P2
AF26 PCIE_CRX C GTX N2 0.1U 0402 10V7K 2 1 C277 PX@ PCIE_CRX GTX_N2

AD27 PCIE_CRX C GTX P3 0.1U 0402 10V7K 2 1 C278 PX@ PCIE_CRX GTX_P3
AD26 PCIE_CRX C GTX N3 0.1U 0402 10V7K 2 1 C279 PX@ PCIE_CRX GTX_N3

AC25
AB25

Y23
Y24

AB27
AB26

Y27
Y26

W24
W23

V27
U26

U24
U23

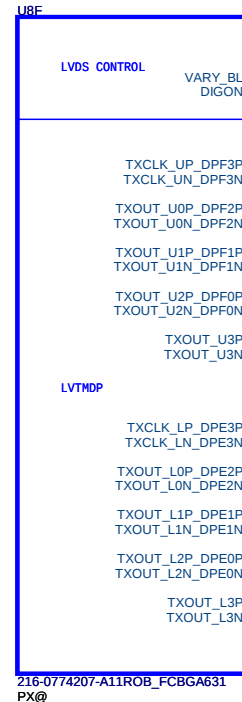
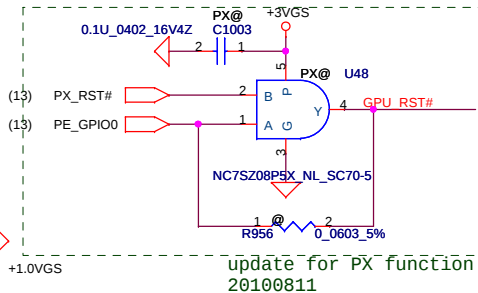
T26
T27

T24
T23

P27
P26

P24
P23

M27
M26



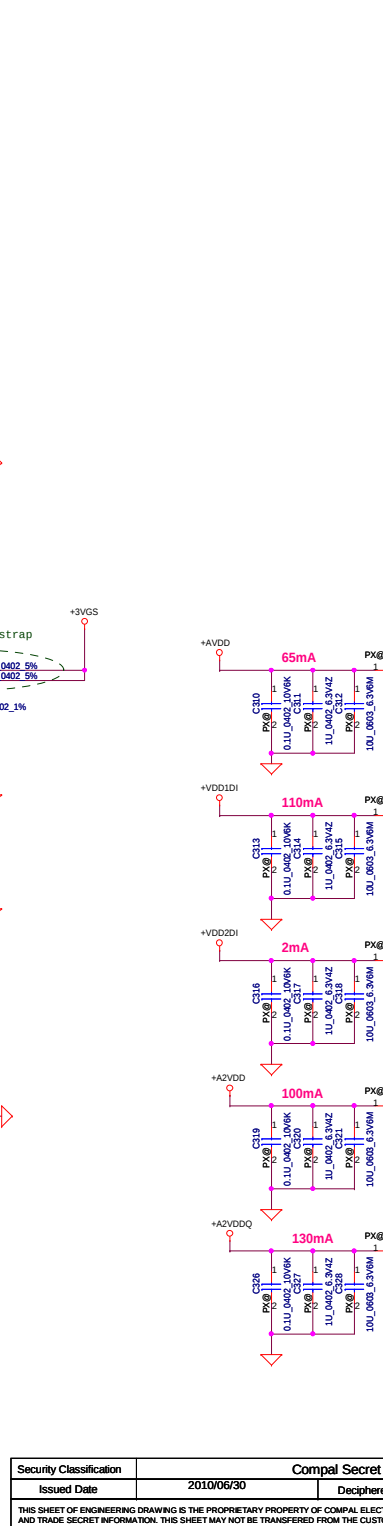
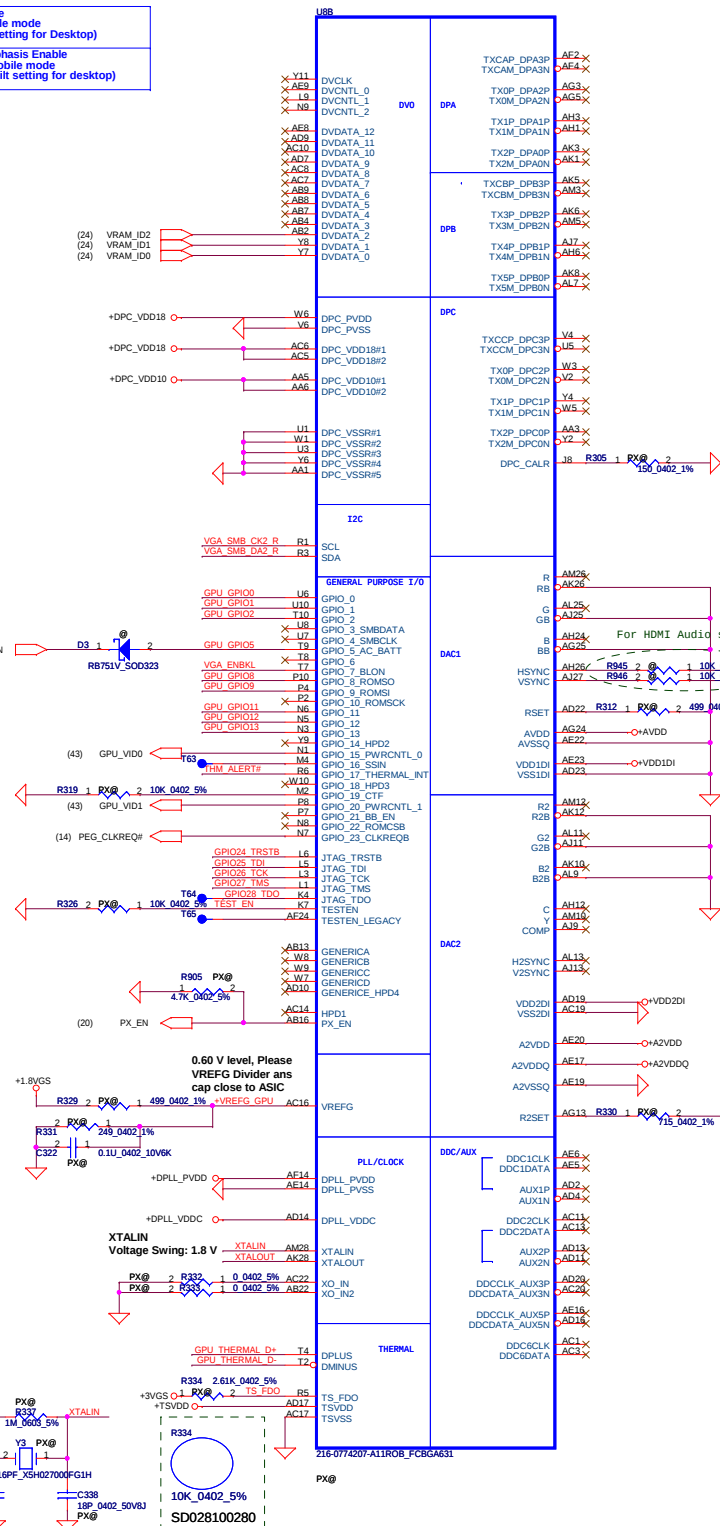
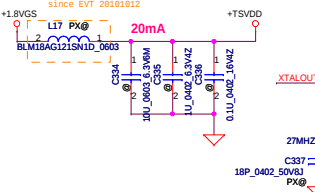
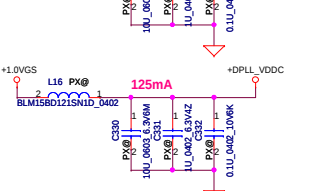
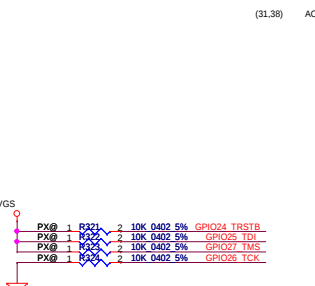
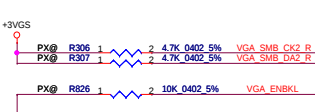
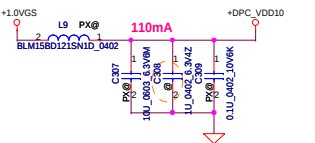
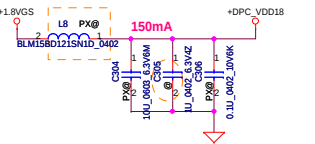
LVDS

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								RobsonXT-S3 PCIE/LVDS		
								Size	Document Number	Rev
								B	LA6755P/7P	1.0
								Date: Tuesday, November 30, 2010		
								Sheet 18 of 48		

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TX_PWRS_ENB	GPI00	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

change from SM01000900 to SD02800080
20101012

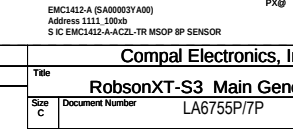
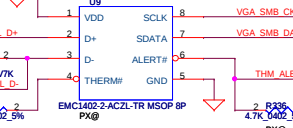
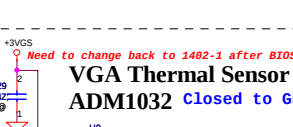
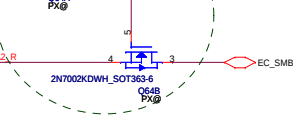
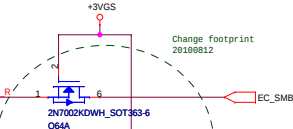
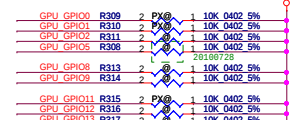


CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIS ARE USED, THEY MUST NOT CONFLICT DURING RESET Internal pull down			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPI00	PCI FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPI01	PCI TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPI02	0: 2.5GT/s; 1: 5.0GT/s, internal PD.	0
RSVD	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RSVD	GPI021	RESERVED	0
BIOS_ROM_EN	GPI022_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPI0(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[0]	HSYNC	AUD[0] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

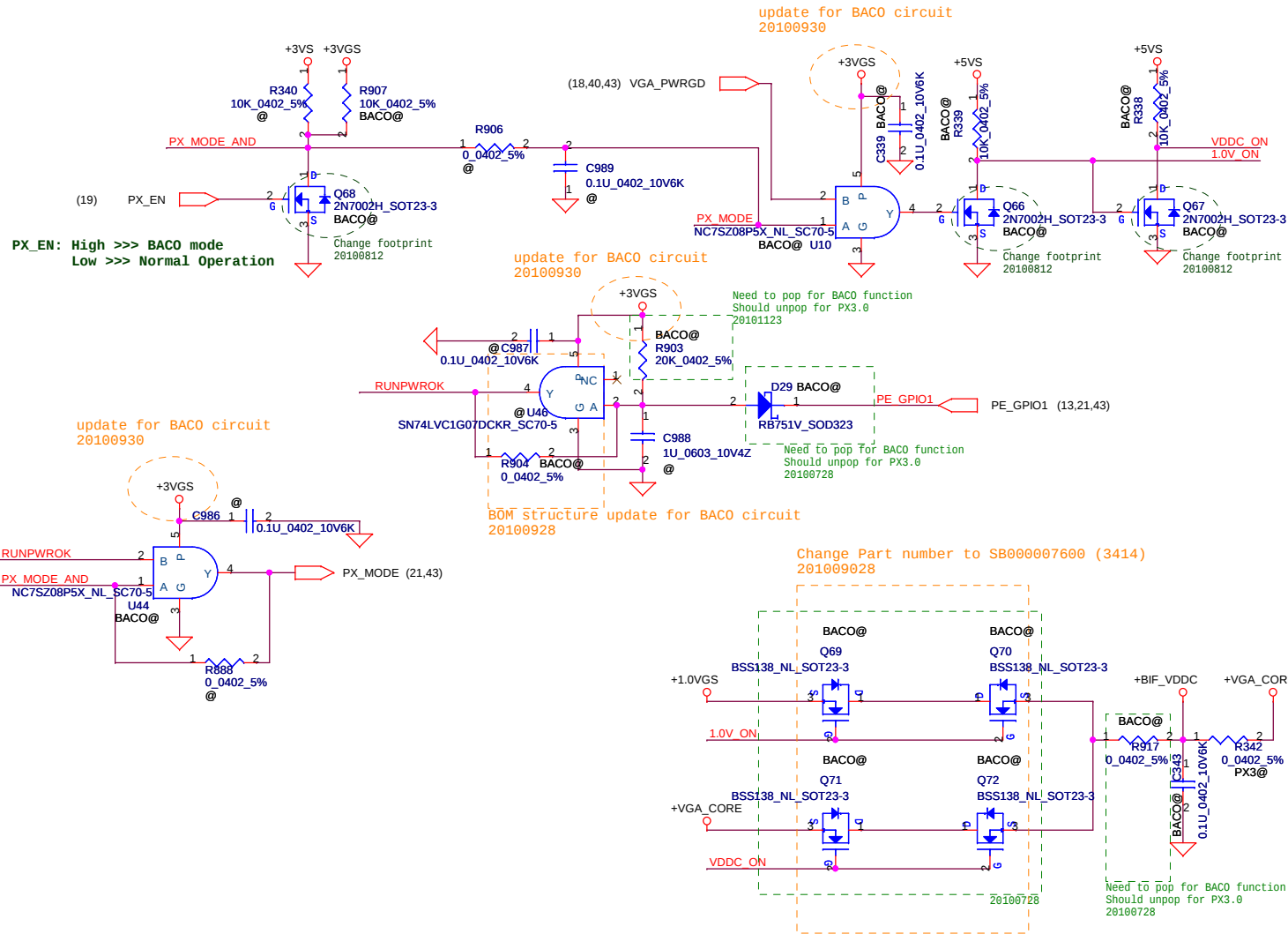
AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL
RESISTOR. IF THESE GPIS ARE USED, THEY MUST KEEP "LOW" AND
NOT CONFLICT DURING RESET If we meet some issue on bring up, we can check this item during reset.

GPI021	H2SYNC	GENERICC	GPI02	GPI08
--------	--------	----------	-------	-------

STRAPS

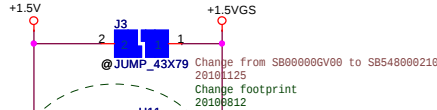


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				Date:	Tuesday, November 30, 2010
				Sheet	19 of 48

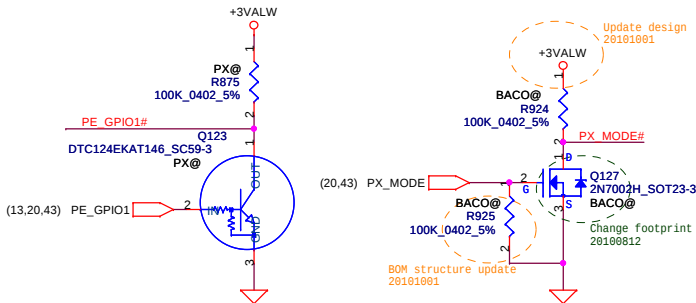


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				Size B	Document Number
				LA6755P/7P	
				Date:	Tuesday, November 30, 2010
				Sheet	20 of 48
				Rev	1.0

For VGA power sequence
20100816



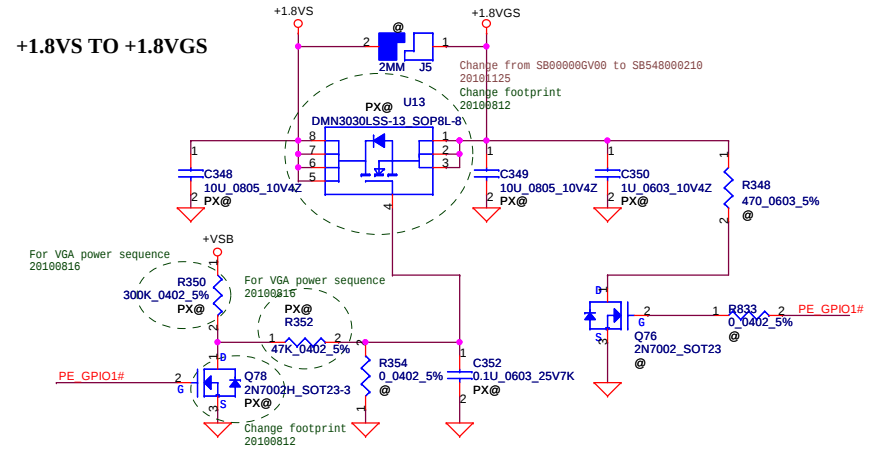
Need to pop for BACO function
Should be unpop for PX3.0
20100728



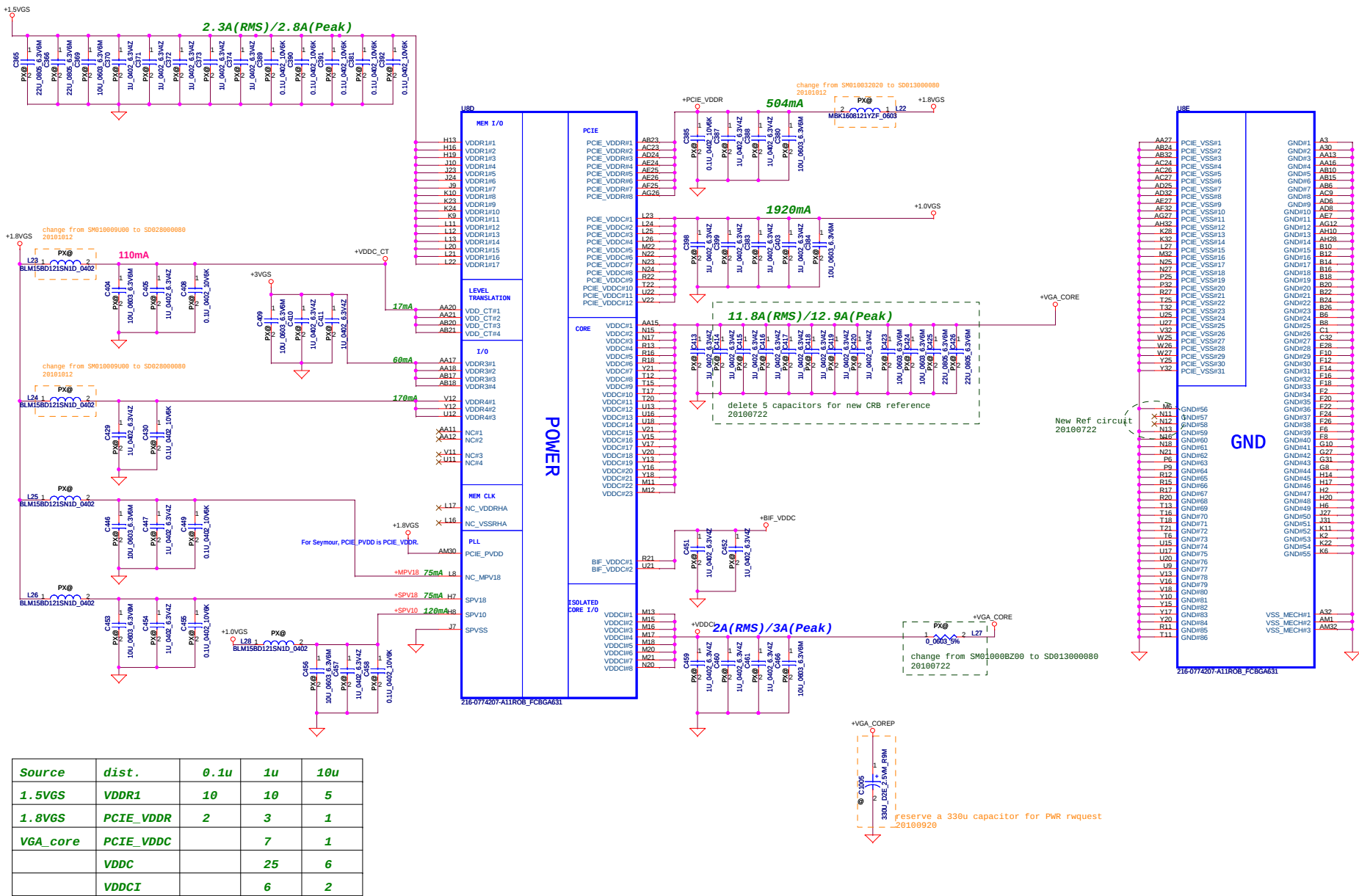
For VGA power sequence

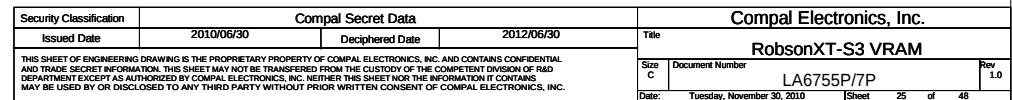
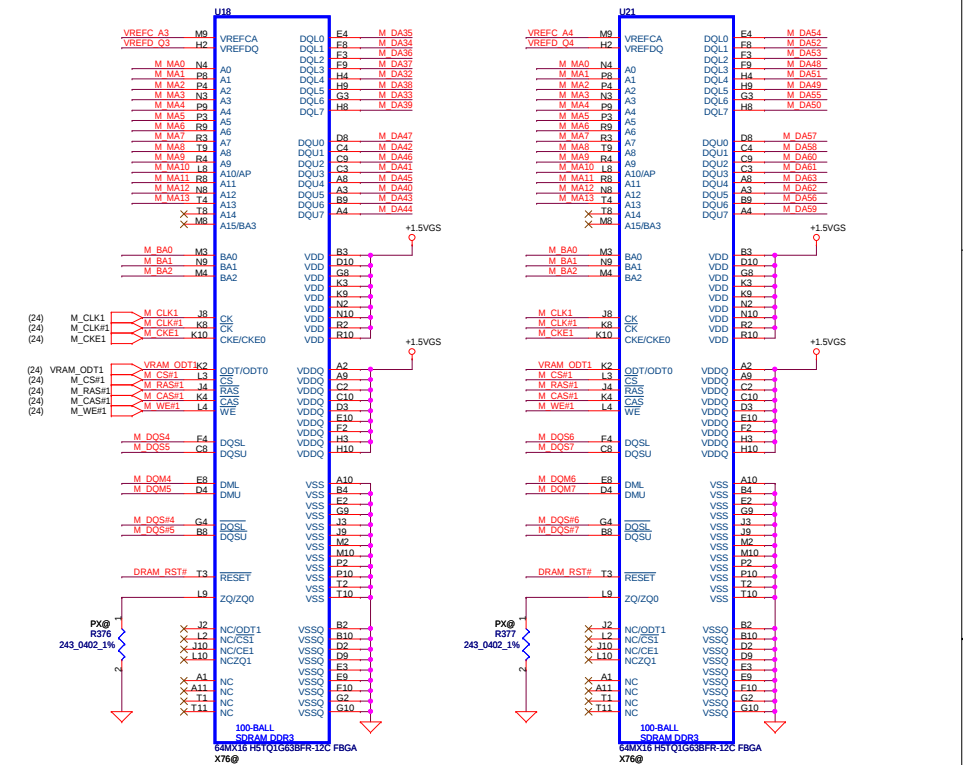
20K_0402_5% R839 PX@

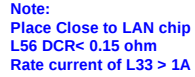
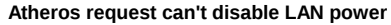
For VGA Pwr sequence



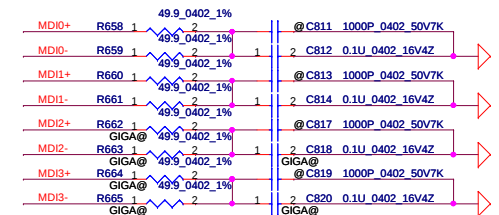
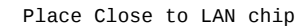
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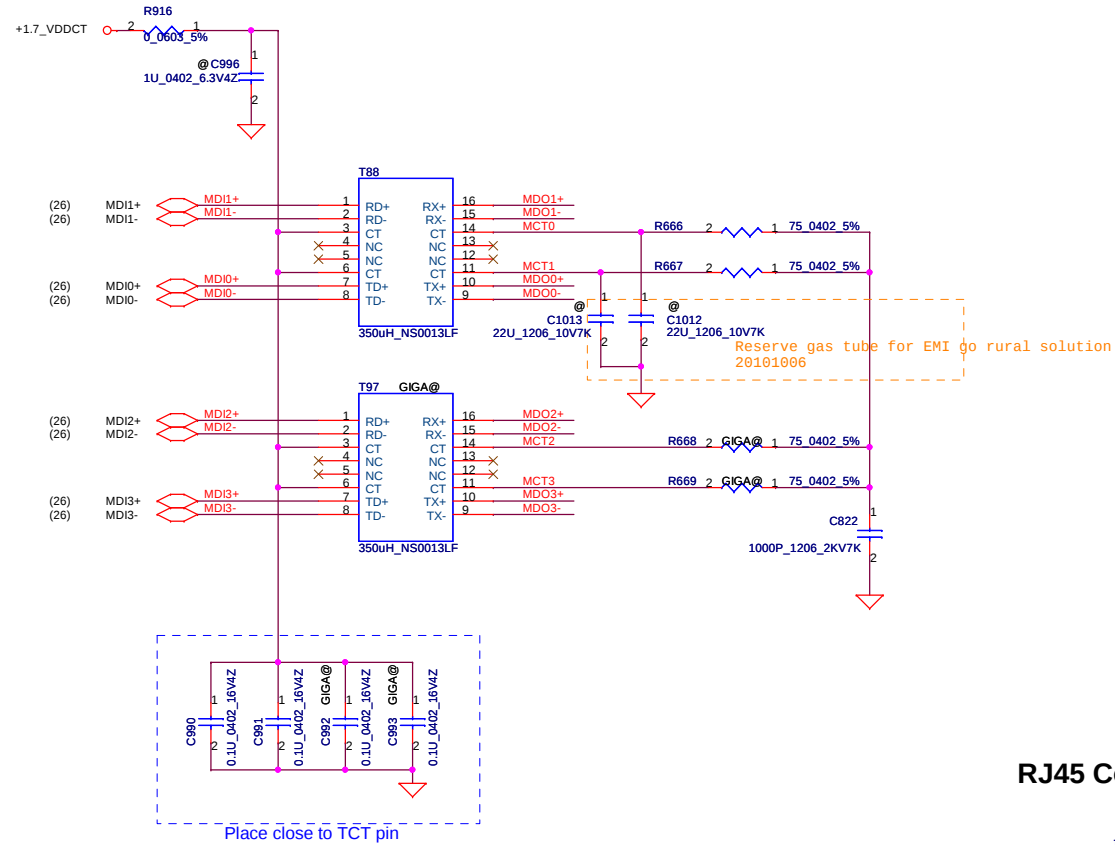
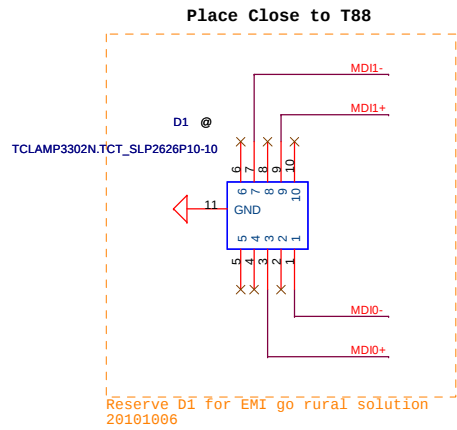


Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

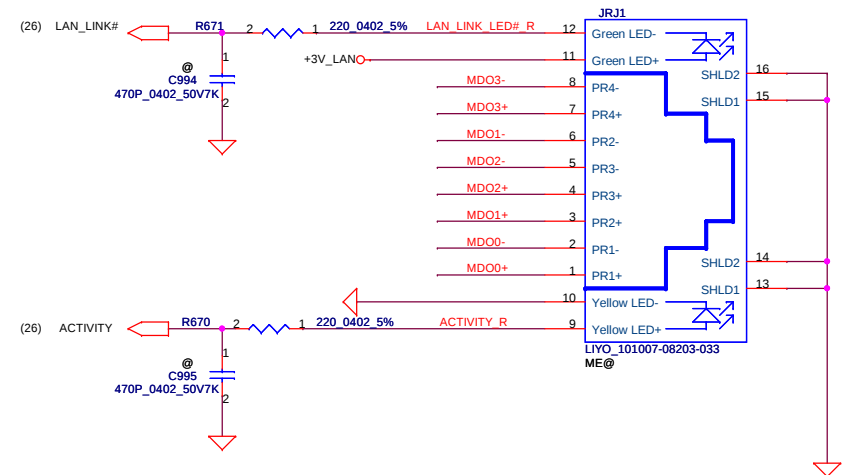


8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resister and cap

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					LA6755P/7P	1.0	
				Date:	Tuesday, November 30, 2010	Sheet	26 of 48

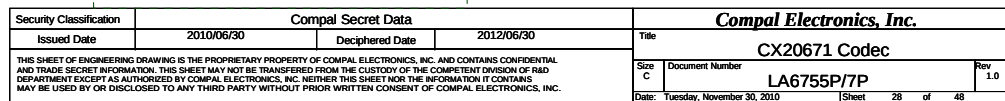


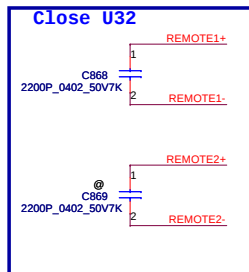
RJ45 Conn.



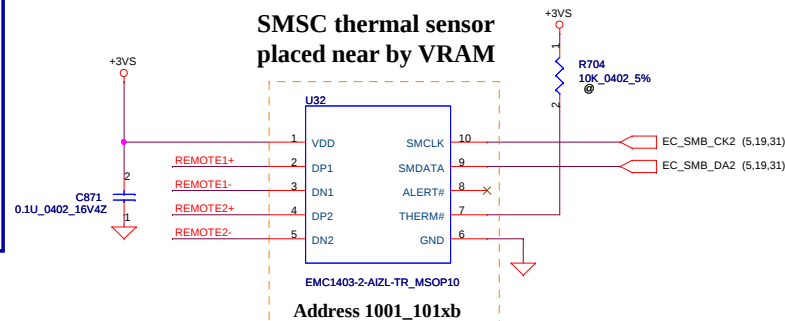
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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	
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				Custom	1.0
				Document Number	
				LA6755P/7P	
				Date:	Tuesday, November 30, 2010
				Sheet	27 of 48

An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

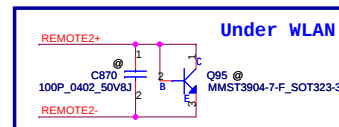
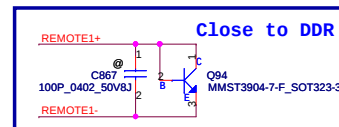




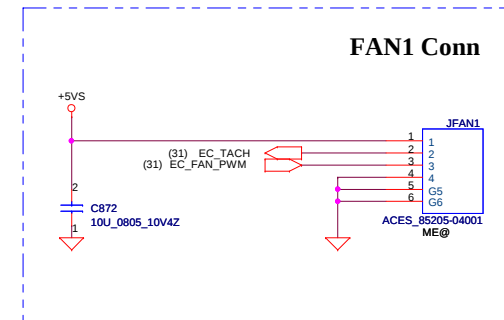
SMSC thermal sensor placed near by VRAM



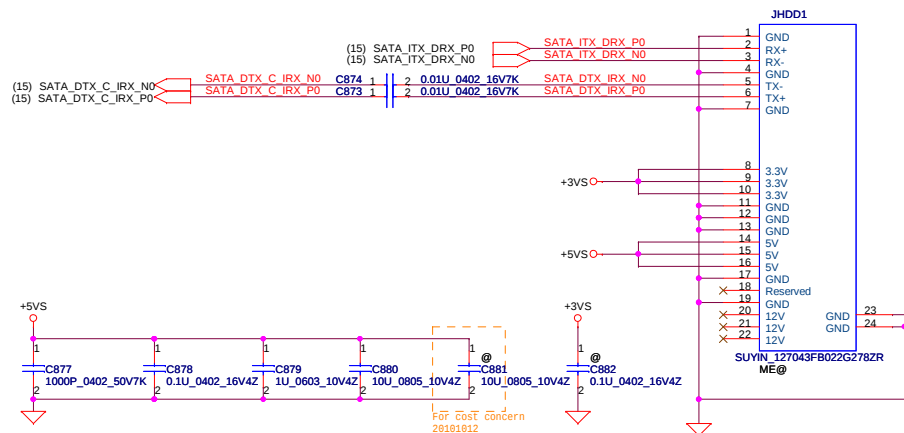
Change from SA000029210 to SA000046C00 for main source



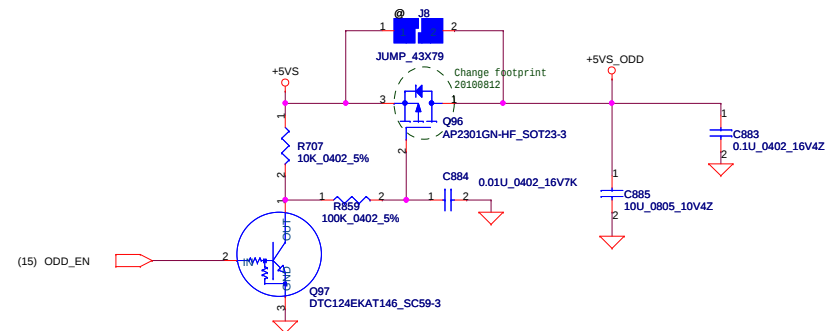
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



SATA HDD Conn.

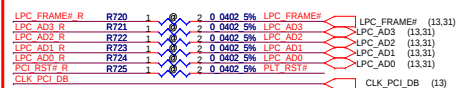


ODD Power Control

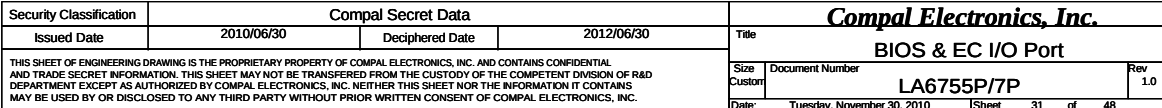


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								HDD/ODD/EMC1403/FAN	
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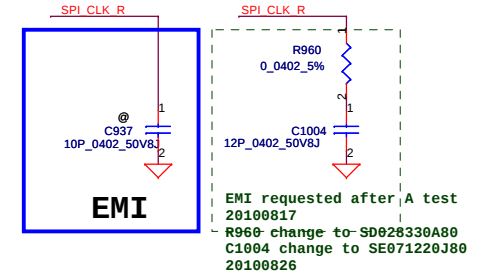
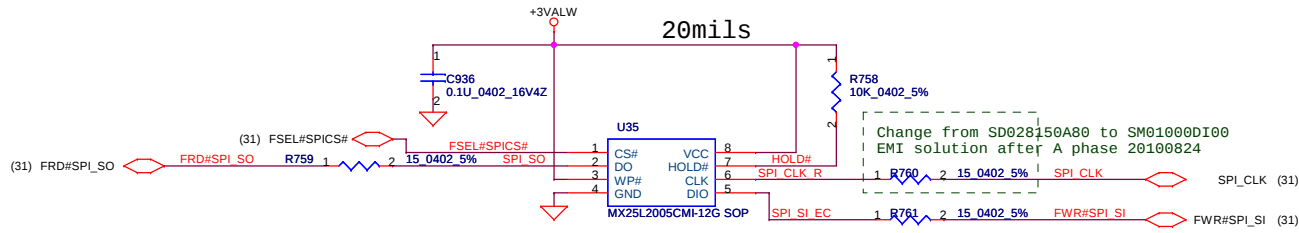
Mini-Express Card(WLAN/WiMAX)



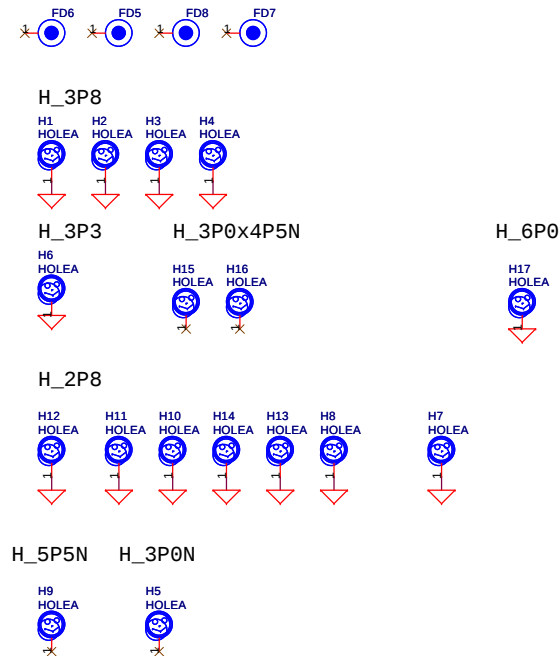
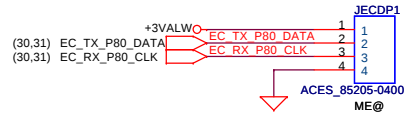
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				Mini PCIE	
				Size	Document Number
				LA6755P/7P	Rev 1
Date:				Tuesday, November 30, 2010	Sheet 30 of 48



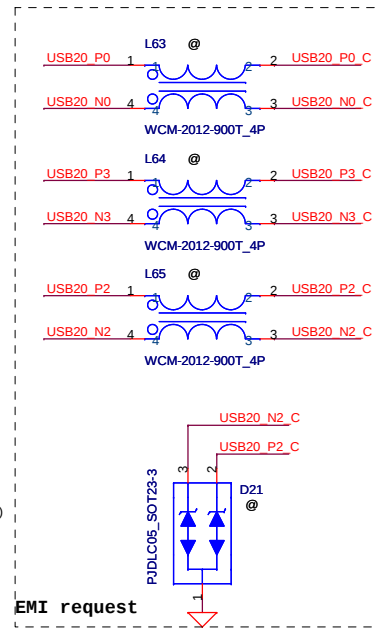
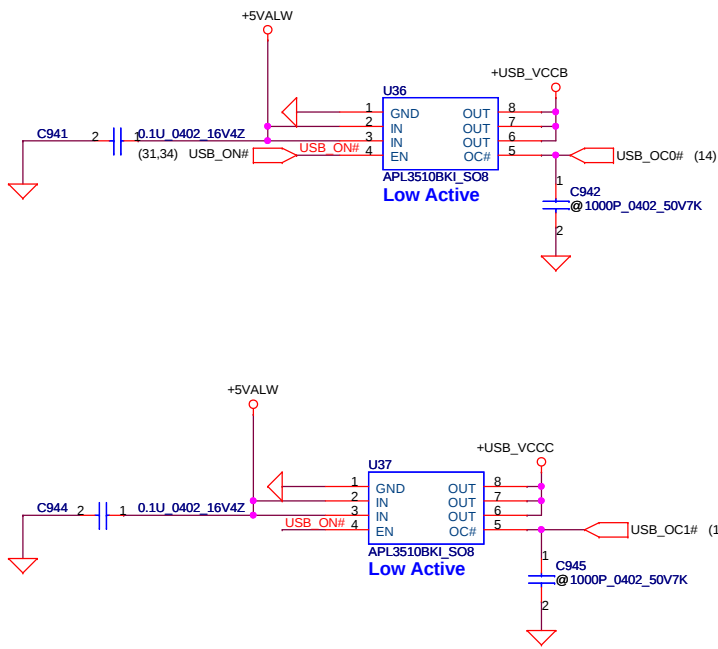
**FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00**



EC DEBUG PORT

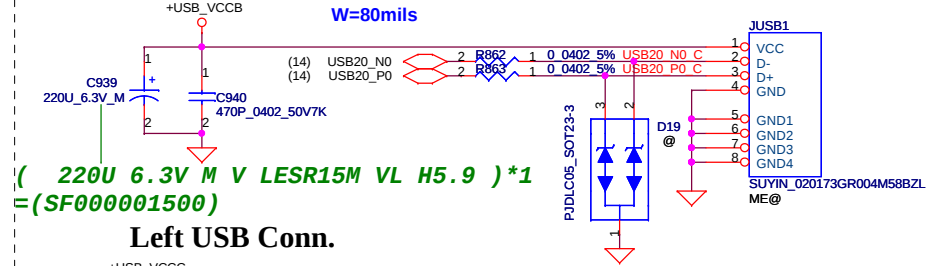


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title	EC SPI ROM/LPC Debug Conn.		
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				B	LA6755P/7P	1.0	
				Date: Tuesday, November 30, 2010			
				Sheet 32 of 48			

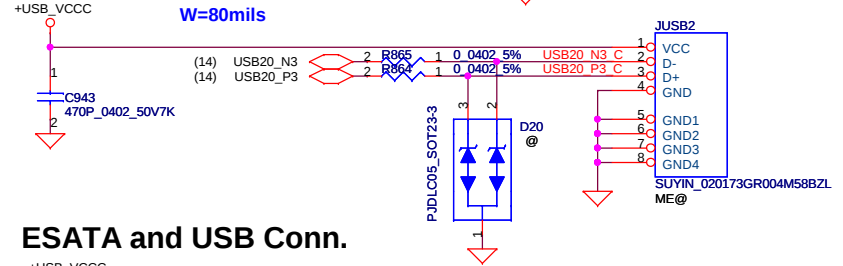


(220U 6.3V M 6.3X4.2) *1=(SF000002Y00)

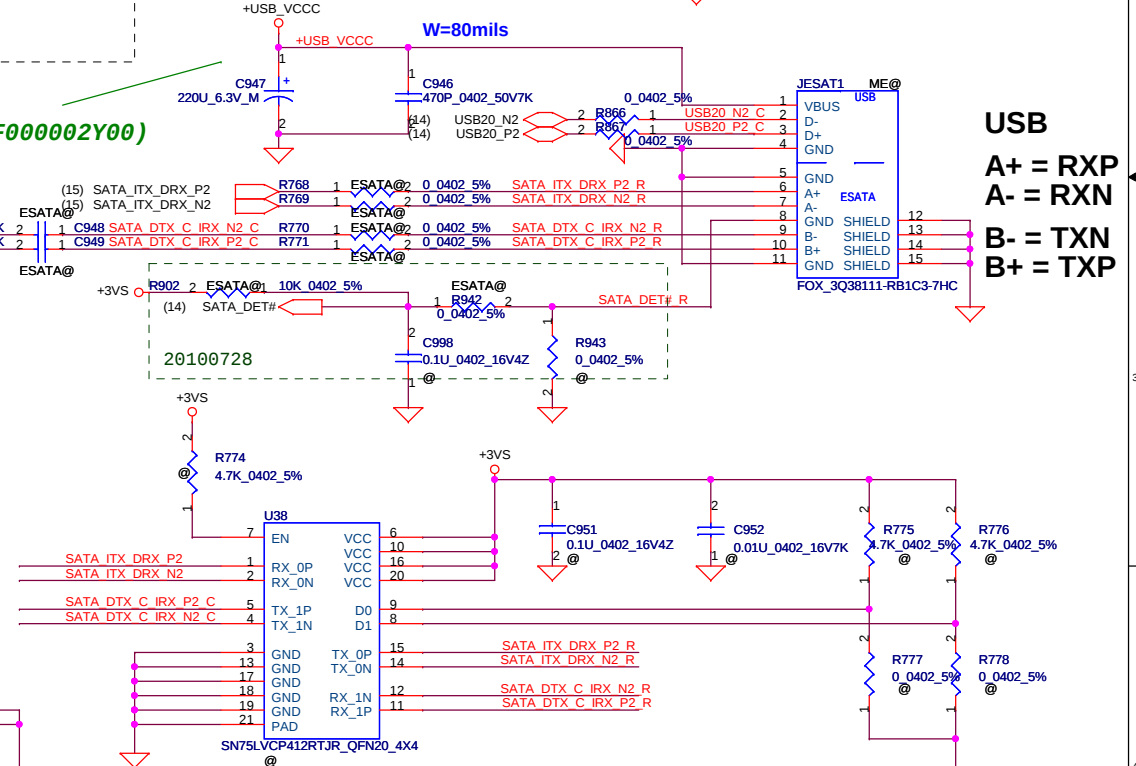
Left USB Conn.



Left USB Conn.



ESATA and USB Conn.



USB

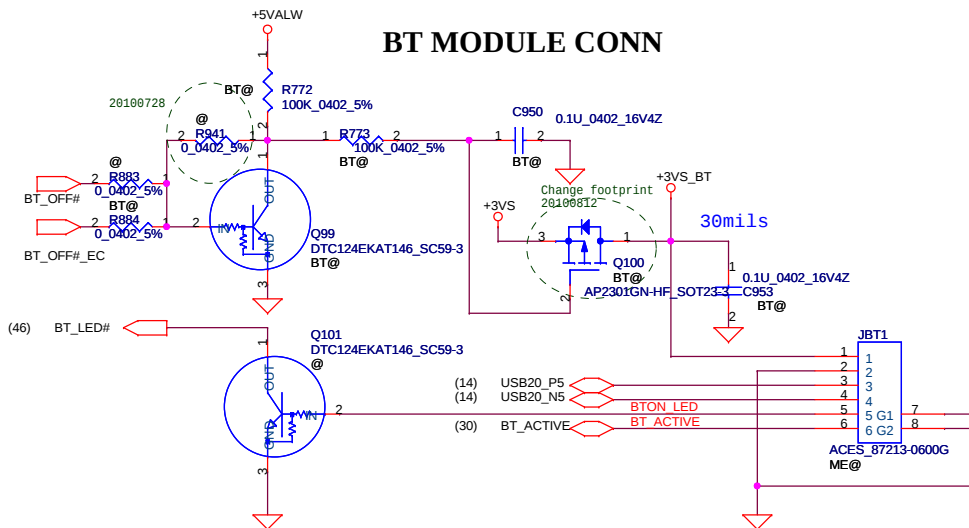
A+ = RXP

A- = RXN

B- = TXN

B+ = TXP

BT MODULE CONN



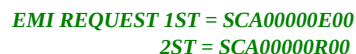
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Issued Date		2010/06/30		Deciphered Date		2012/06/30		Title			
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						Size		Document Number		Rev	
						Custom		LA6755P/7P		1.0	
						Date:		Tuesday, November 30, 2010		Sheet 33 of 48	

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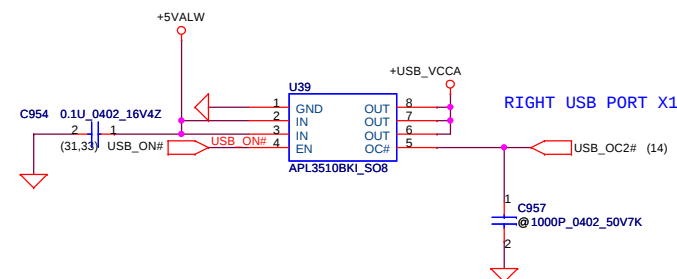
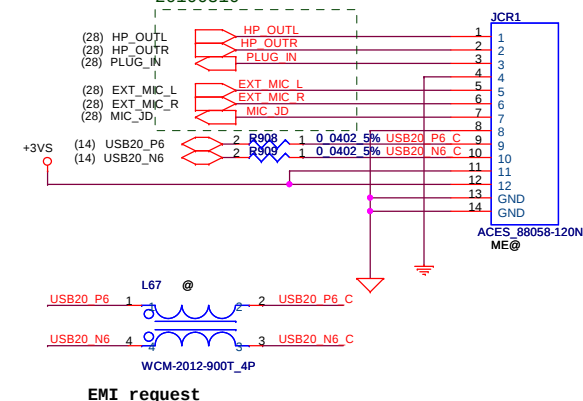
Bottom Side



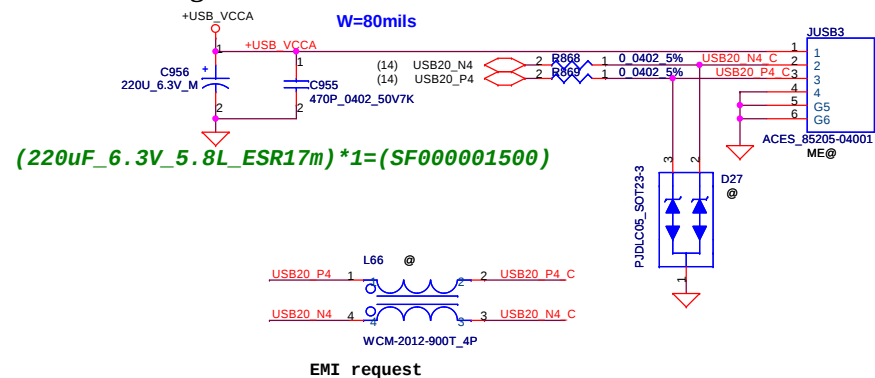
+5VALW



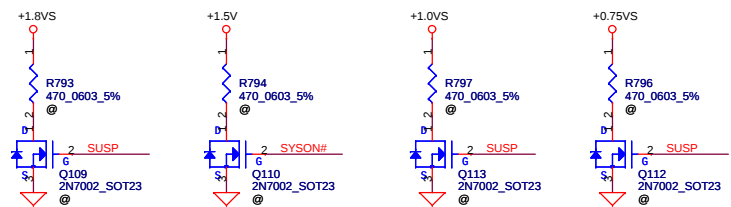
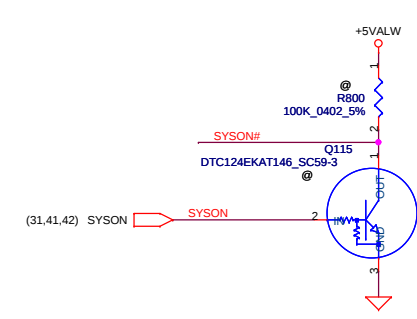
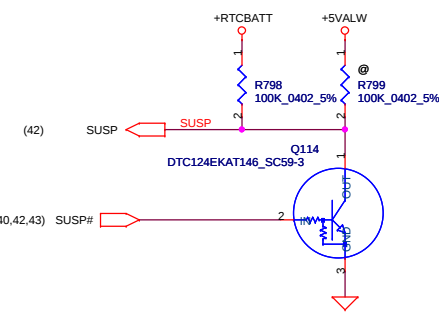
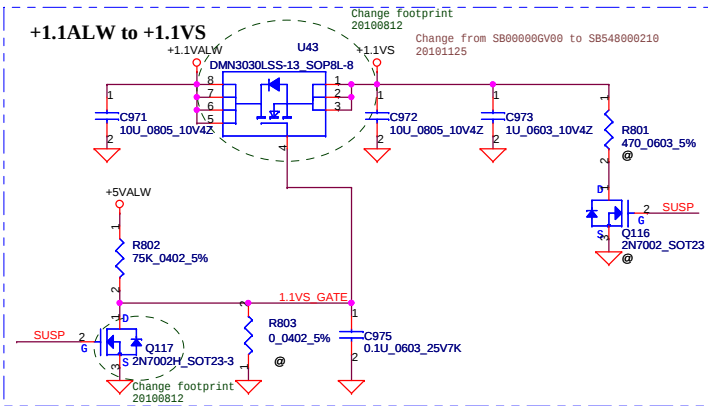
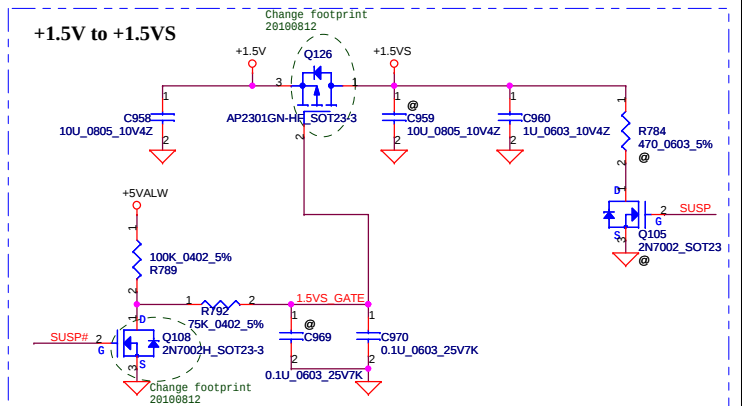
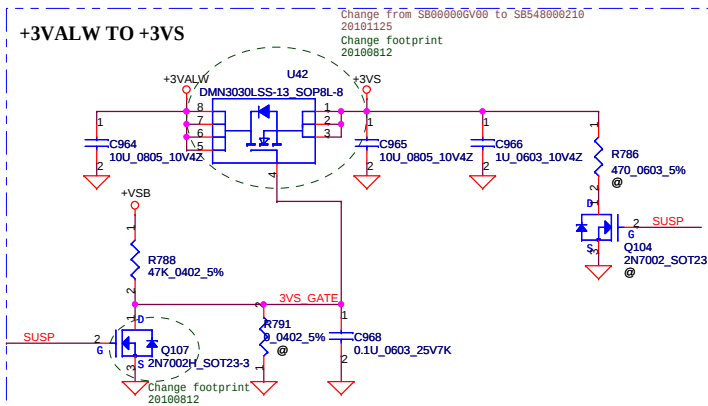
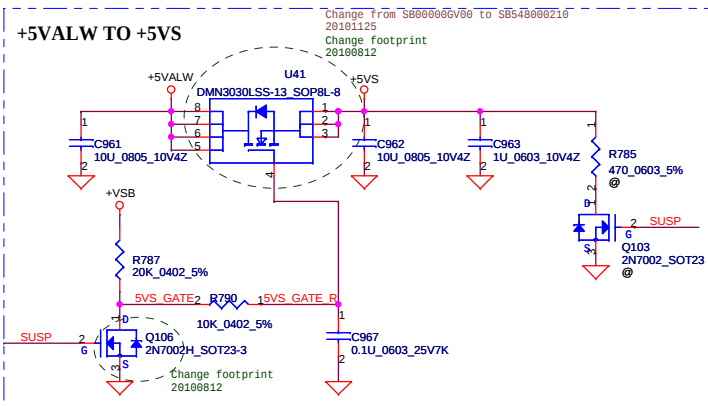
Pin swap
20100810



W=80mils

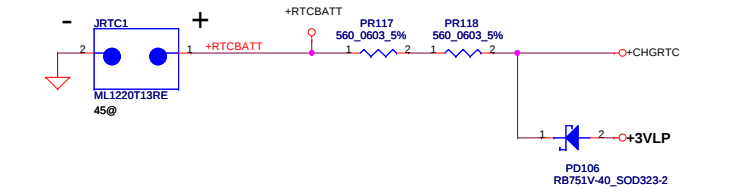
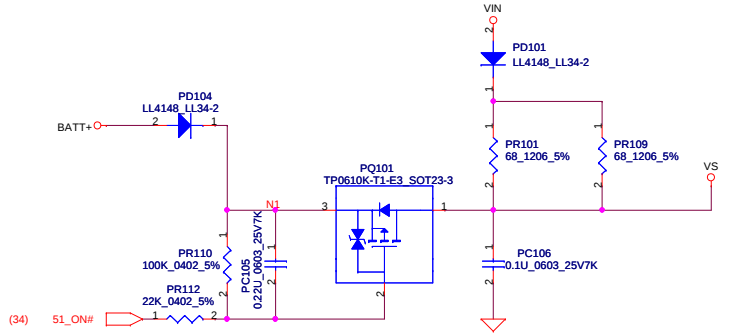
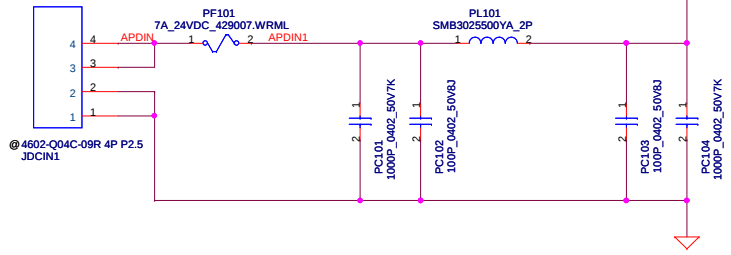


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title Other IO/USB (right)		
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				Custom	LA6755P/7P	1.0
				Date:	Tuesday, November 30, 2010	Sheet 34 of 48

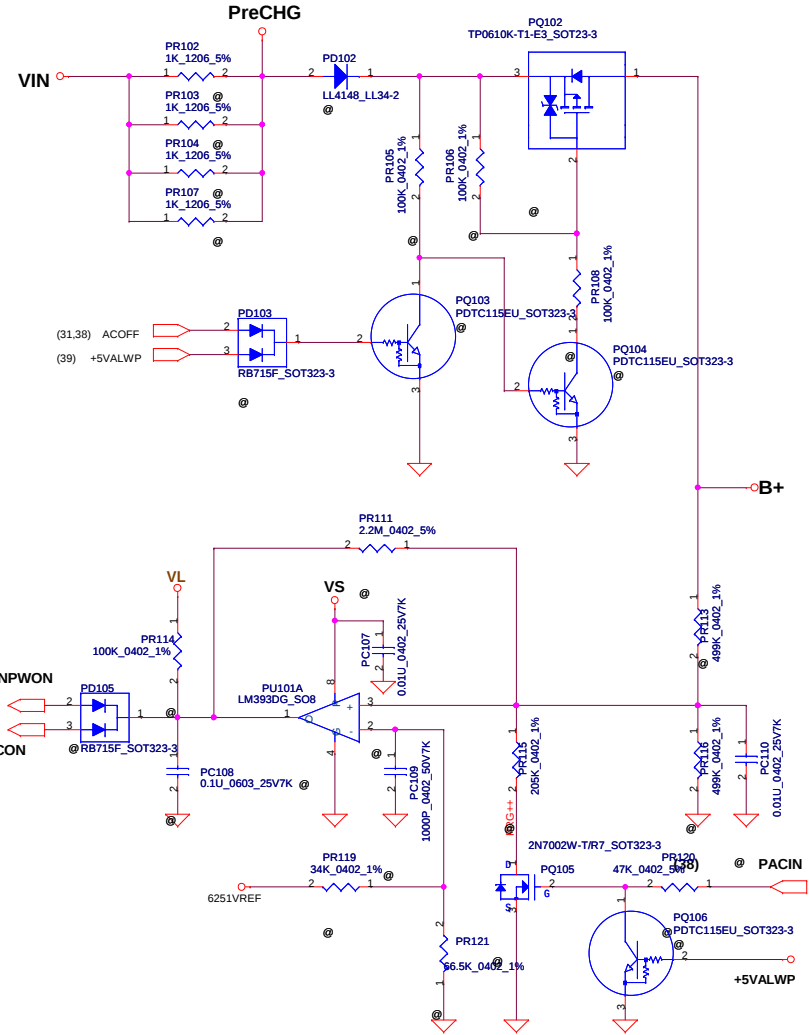


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Issued Date	2010/06/30	Deciphered Date	2012/06/30	Title		
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				Size	Document Number	Rev
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Date: Tuesday, November 30, 2010				Sheet	35	of 48

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

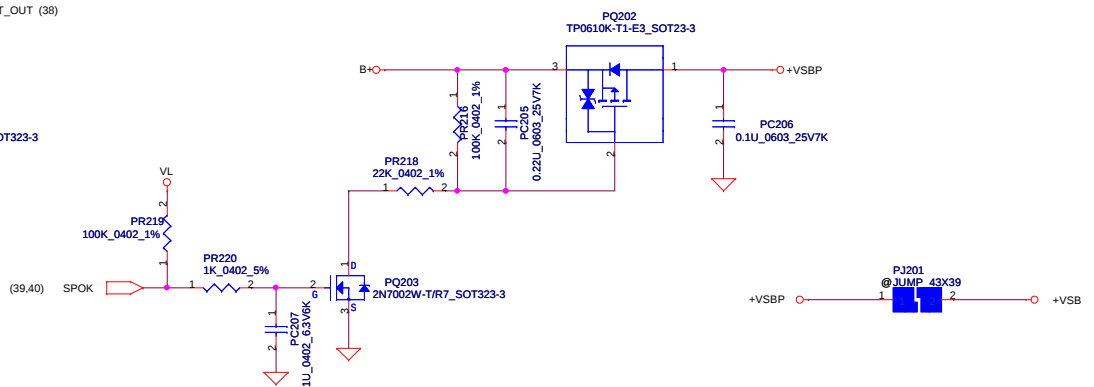
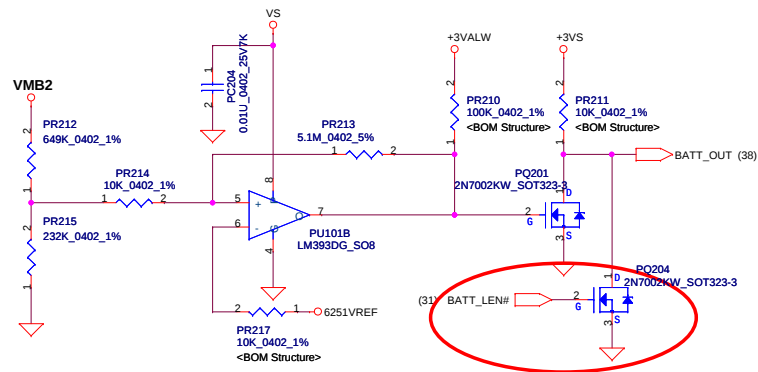
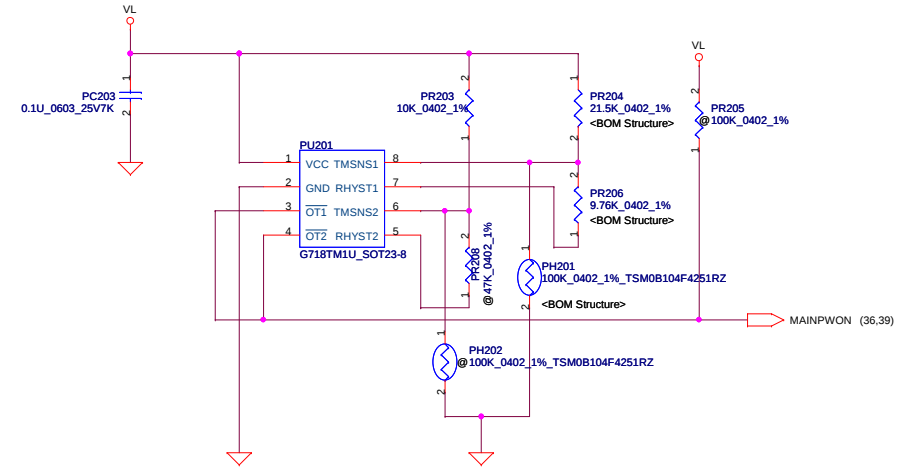
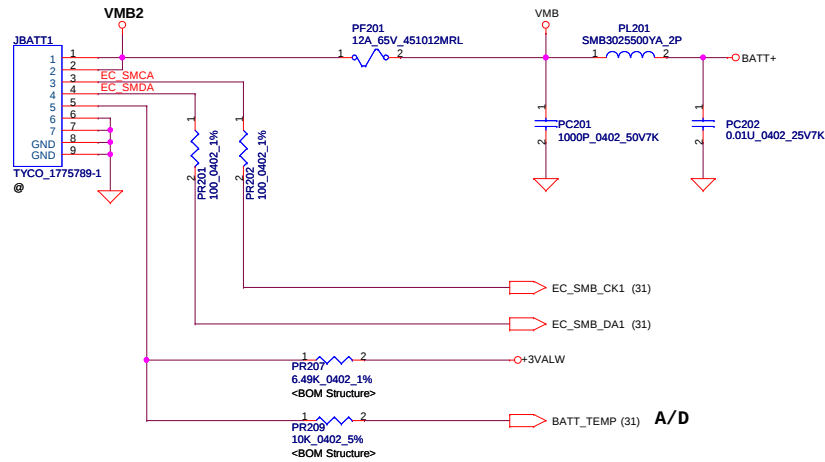
BATT ONLY

Precharge detector

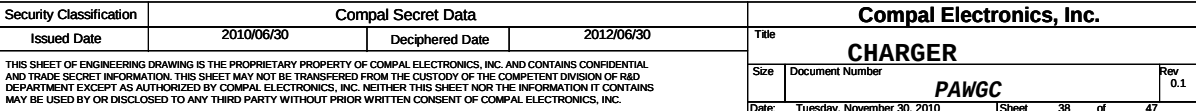
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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				Custom	PAWGC	0.1
				Date:	Tuesday, November 30, 2010	Sheet 36 of 47

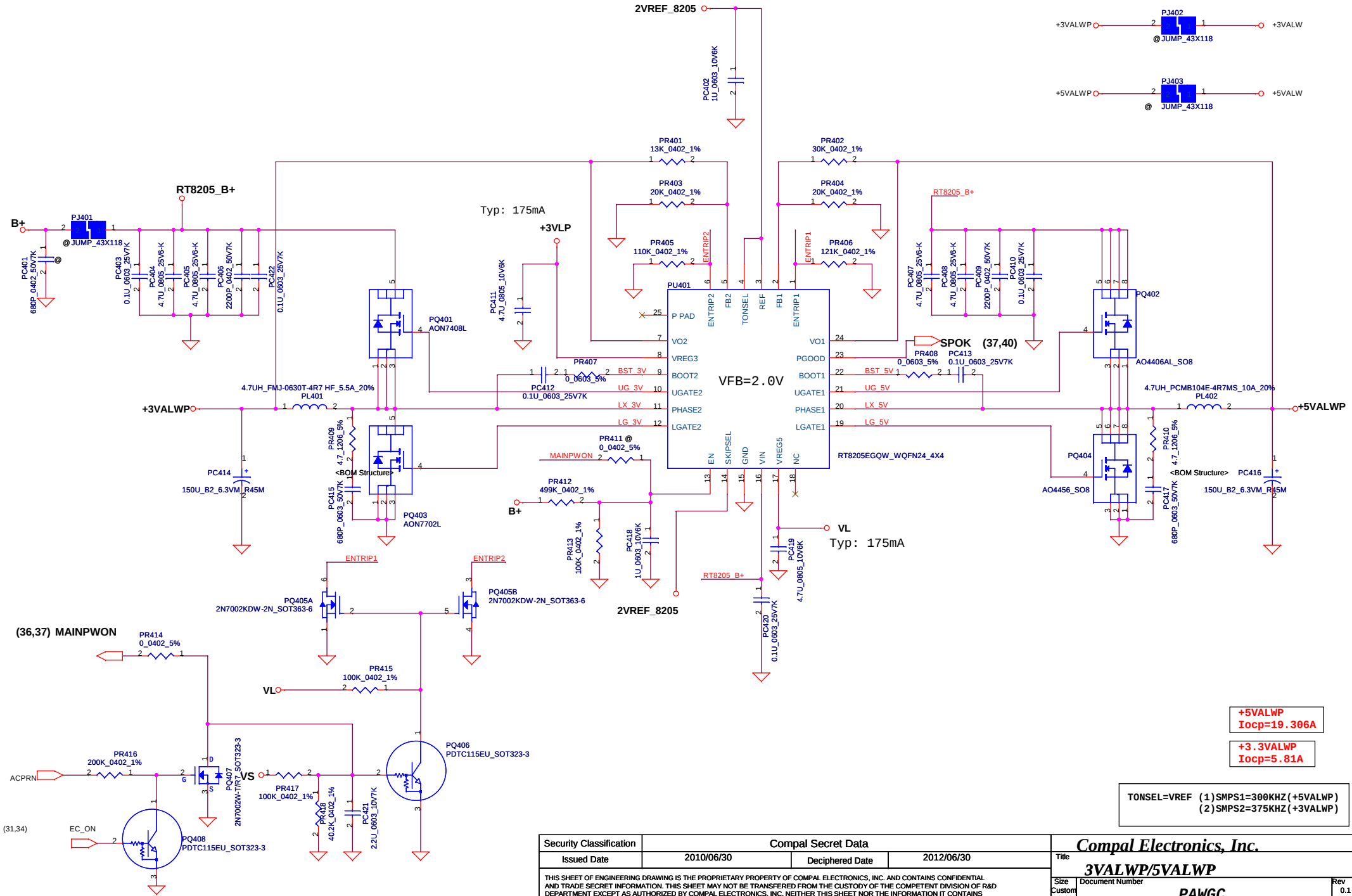
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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				BATTERY CONN/OTP					
				Size Custom		Document Number		Rev	
				Date:		Tuesday, November 30, 2010		Sheet 37 of 47	
				PAWGC		0.1			

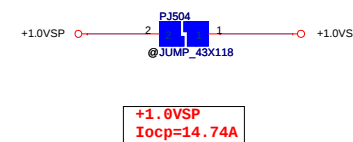
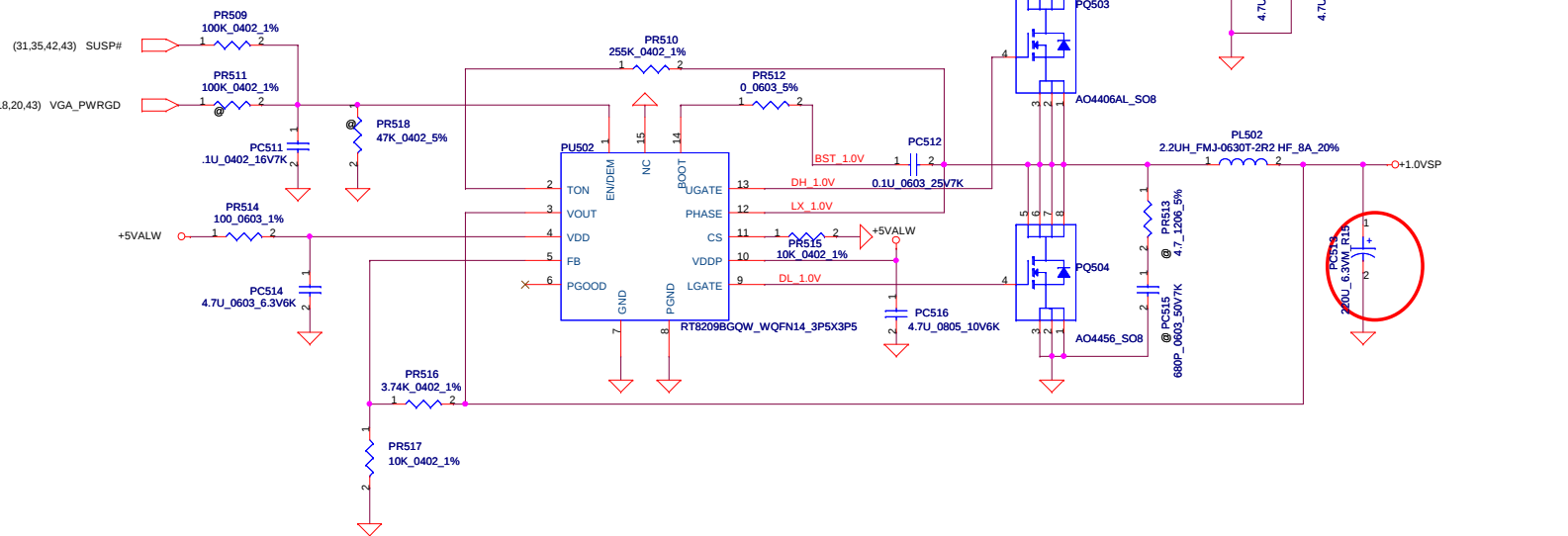
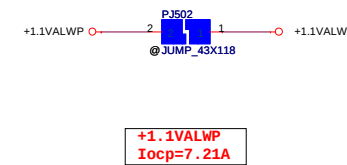
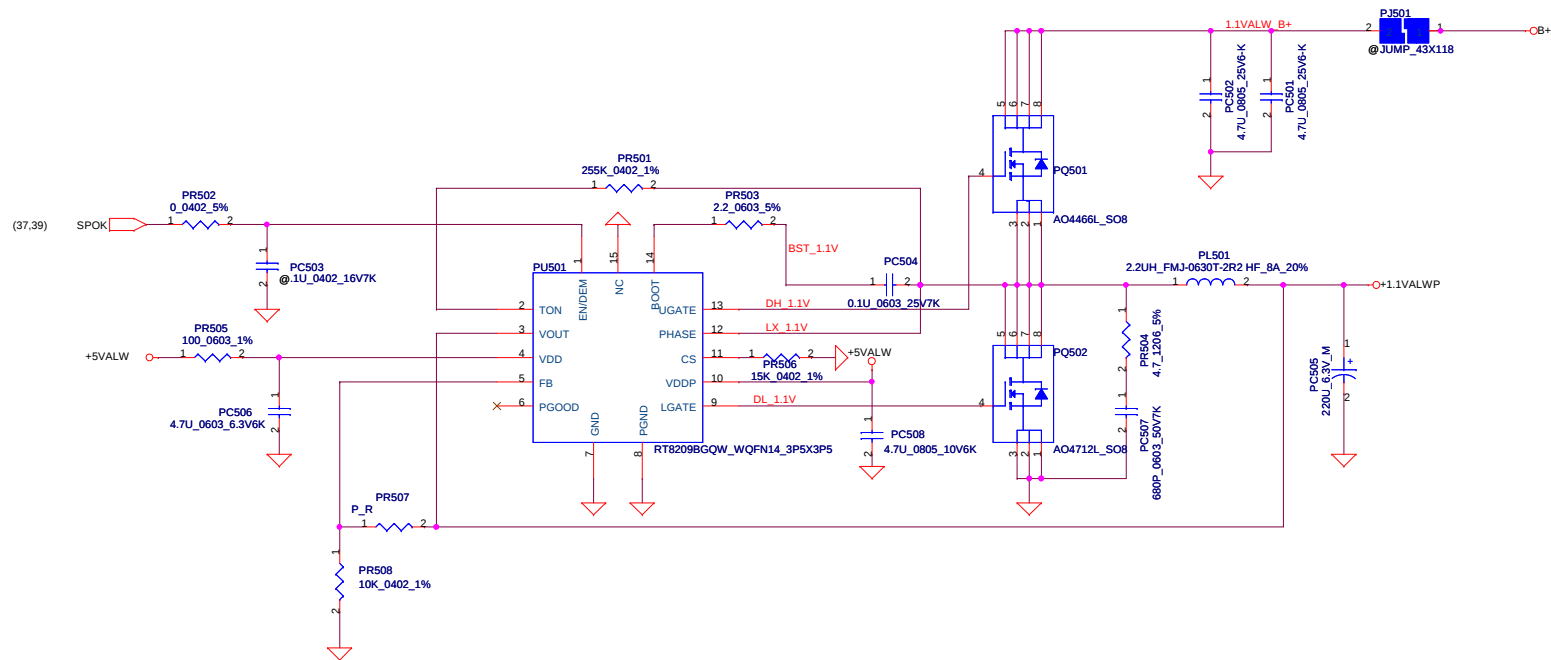


Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

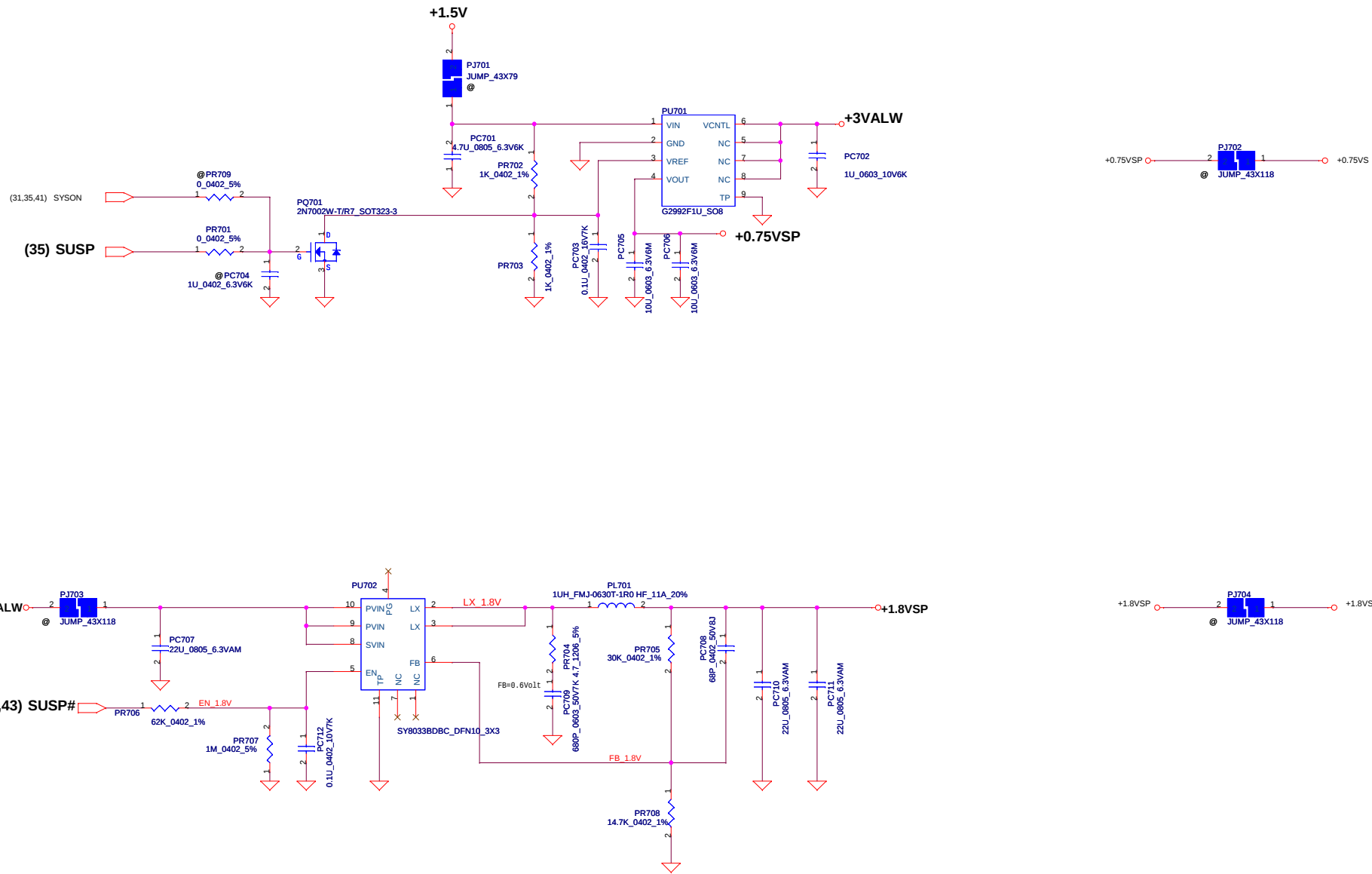


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Compal Electronics, Inc.	
Title	3VALWP/5VALWP
Size	Document Number
Custom	PAWGC
Date	Tuesday, November 30, 2010
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Rev	0.1

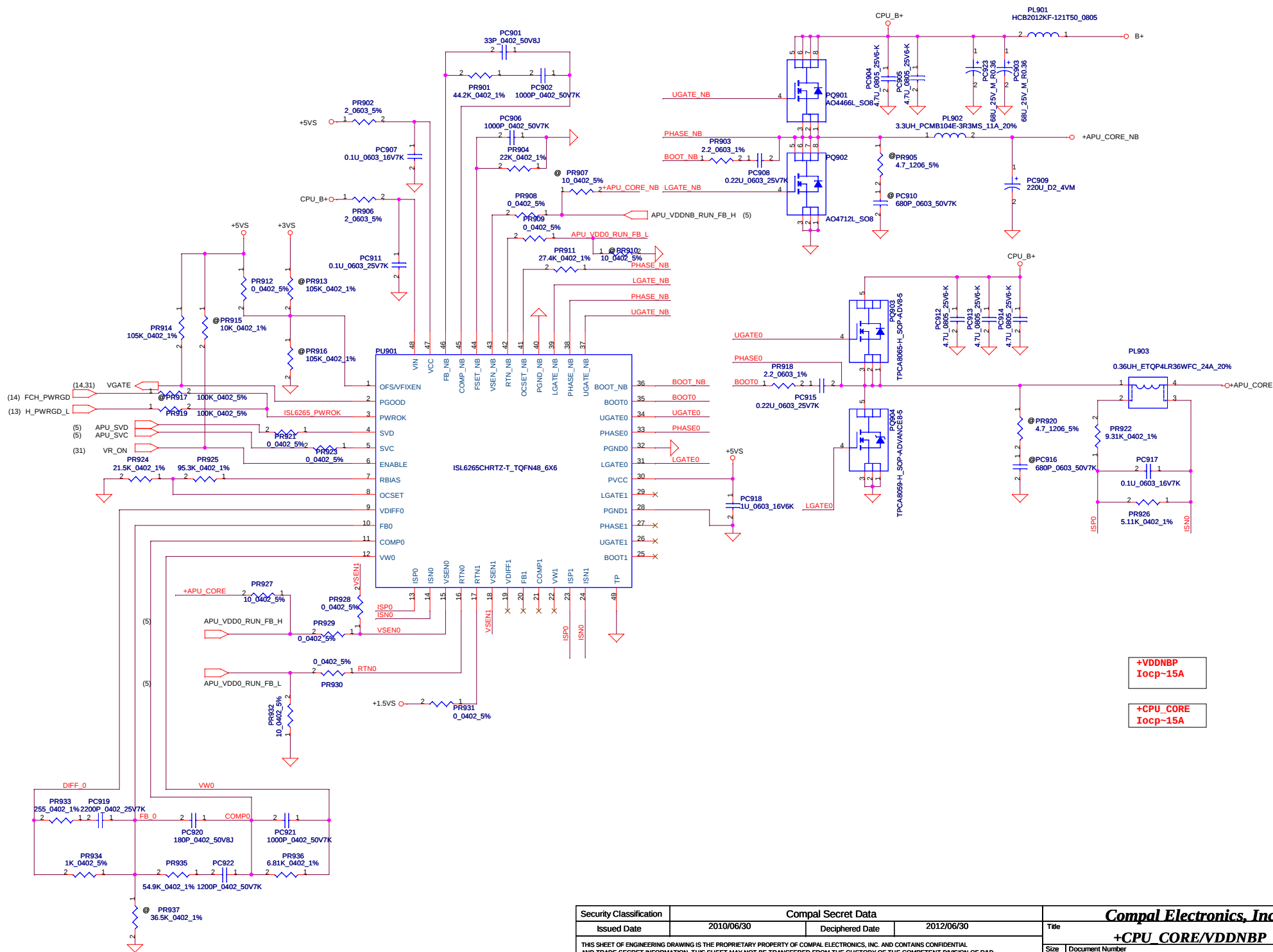


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								Size	Document Number					Rev	
								PAWGC					0.1		
								Date: Tuesday, November 30, 2010					Sheet 42 of 47		

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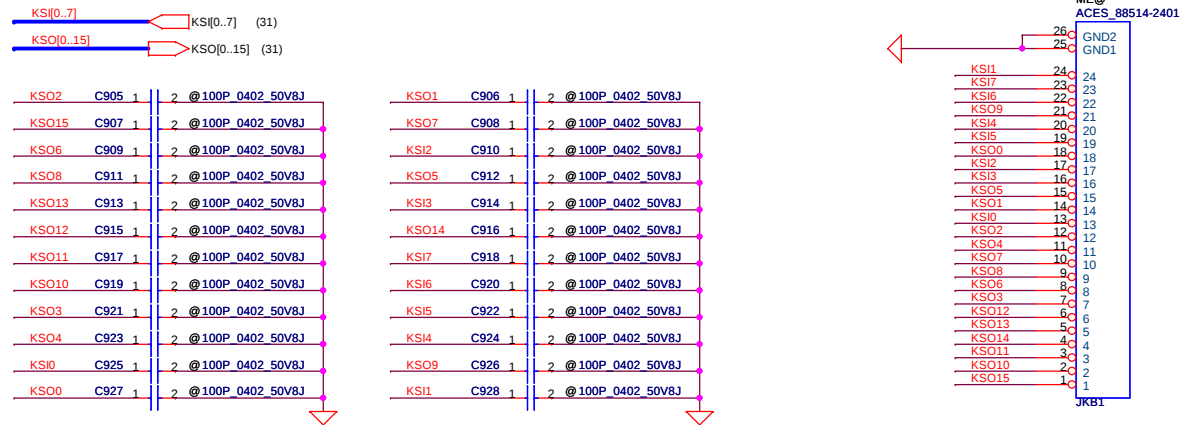


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				PAWGC Date: Tuesday, November 30, 2010	
				Rev	0.1
				Sheet	44 of 47

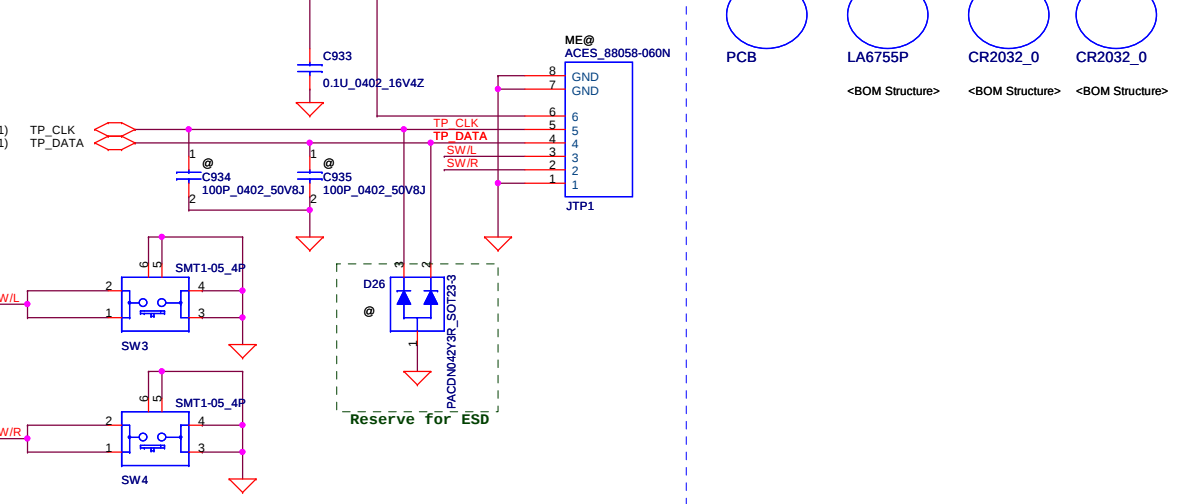
Version Change List (P. I. R. List)for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
	power sequence	2010/07/30	HW		PR701 change to 0 ohm and PC704 non mount.
	Add PU802 for AMD's request	2010/09/21	AMD		
Add PL302,PC324 and PC325 for EMC Solution.		2010/10/04	EMC		change PJ301 to PL302.
	Add PC422 for EMC Solution.	2010/10/06	EMC		
Add PQ204 for EM6.0 battery learning function.		2010/11/12	PWR		

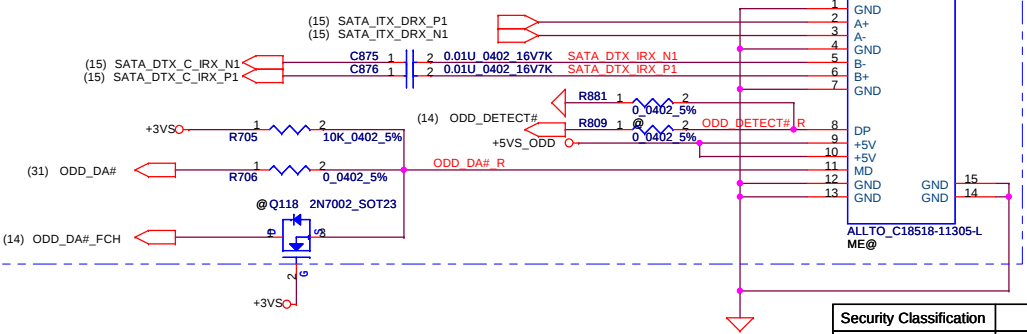
INT_KBD Conn.



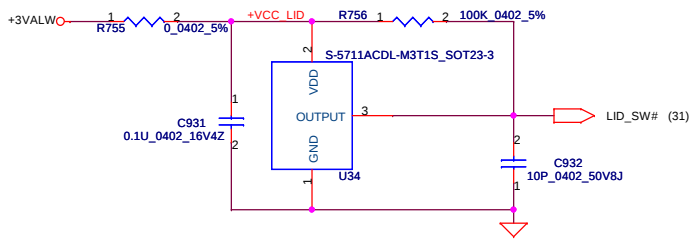
To TP/B Conn.



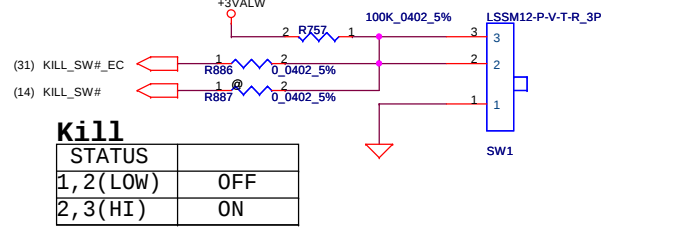
SATA ODD Conn.



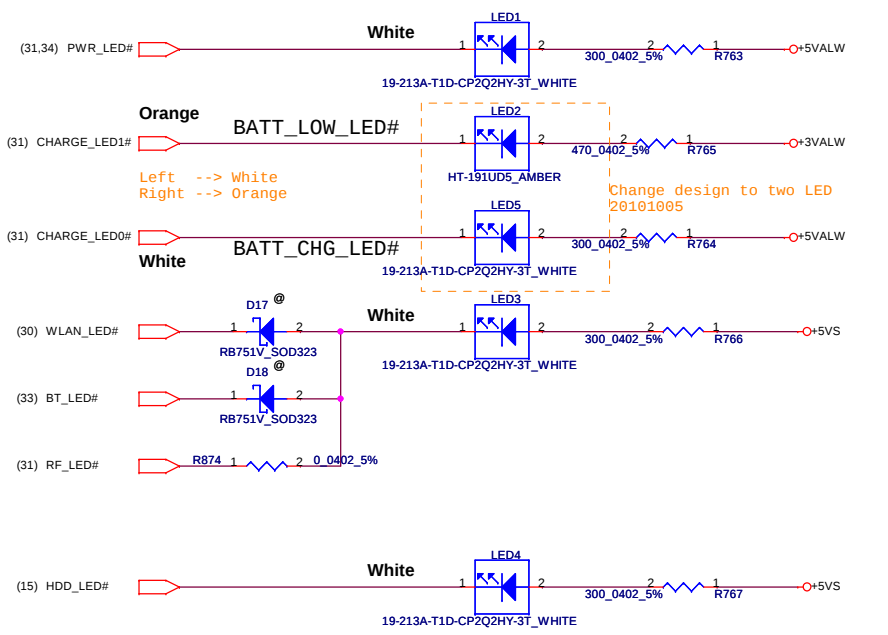
Lid Switch



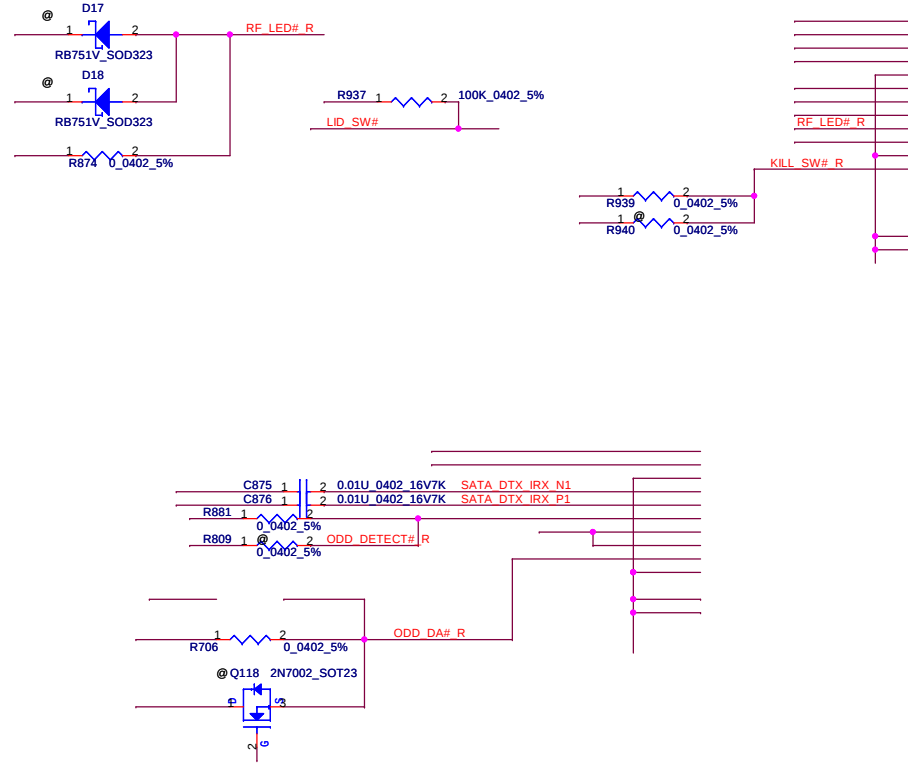
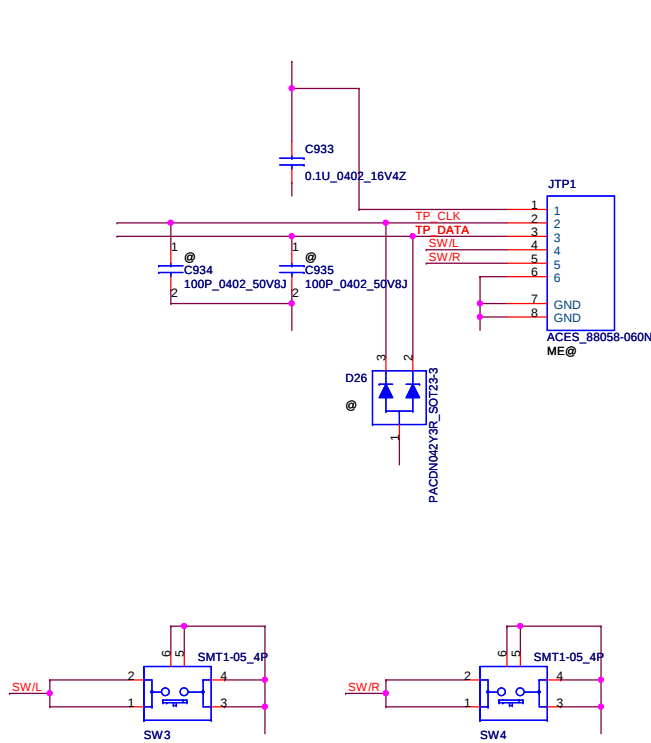
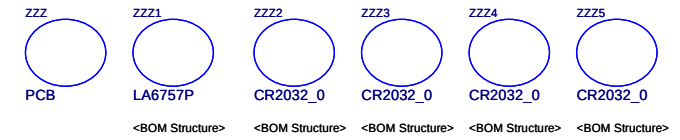
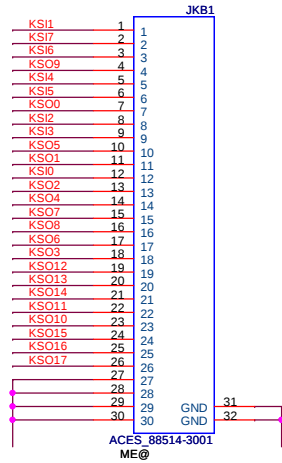
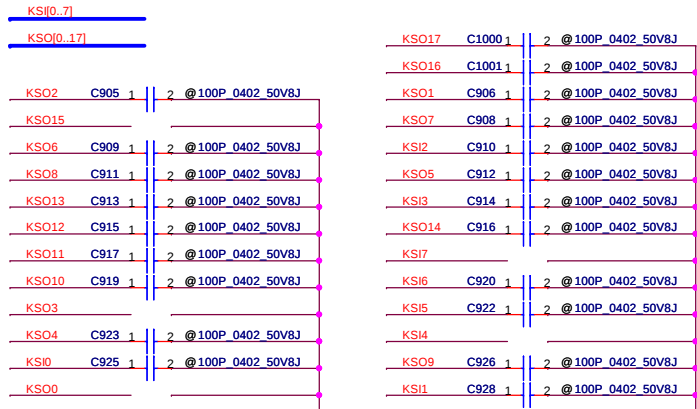
Kill Switch



LED



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Size		Document Number		Rev	
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				LA6757P	
				Date:	Tuesday, November 30, 2010
				Sheet	46 of 48
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PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
0.2	P10	Add CE_EN @ JLVDS1.16 and U33.98	For color engine function
0.2	P10	R488 pull-up to +5VALW	For C38 module design
0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCR11 change foot-print from DC060003000 to DC060004S00	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCI_DB_R and unpop R854	for EMI concern
0.2	P28	Modify PC_BEEP circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	DeI U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.IVS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13 P18	Add C1003, U48, R956, R957 Delete R556, R841, R889, D28	For PX GPU_RST# function
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and C1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
15 only part			
0.2	P46	Add C1000, C1001	For 15" 30pin KB connector

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