Compal Confidential

Z5WAE Schematics Document

AMD "Beema" Platform

AMD 25W APU With Puma+ Core and 25W DGPU with Jet

LA-B231P REV: 1.0

2014-03-27

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				Date: Thursday, March 27, 2014; Sheet 1 of 45

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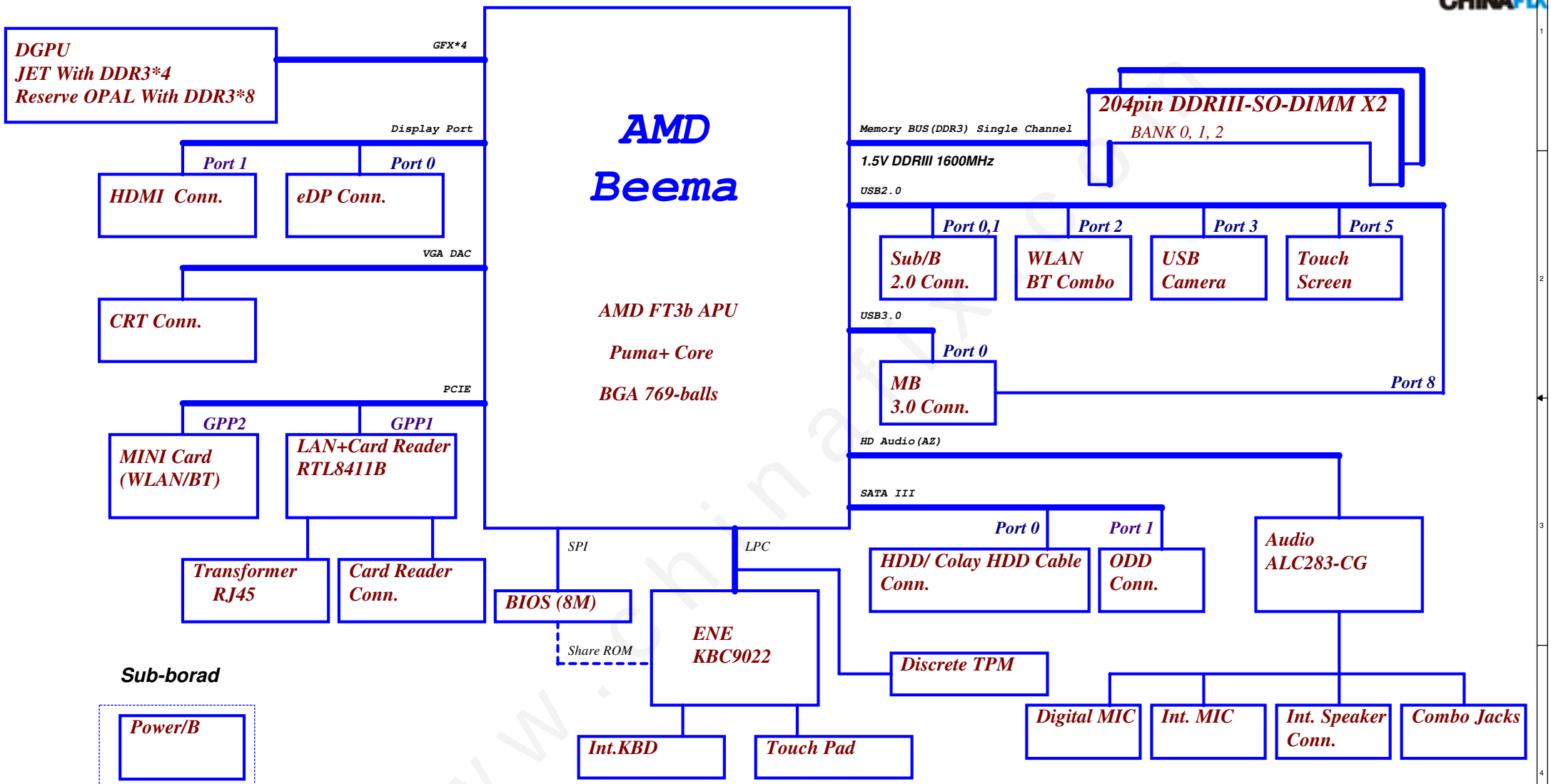
Model Name : Z5WAE



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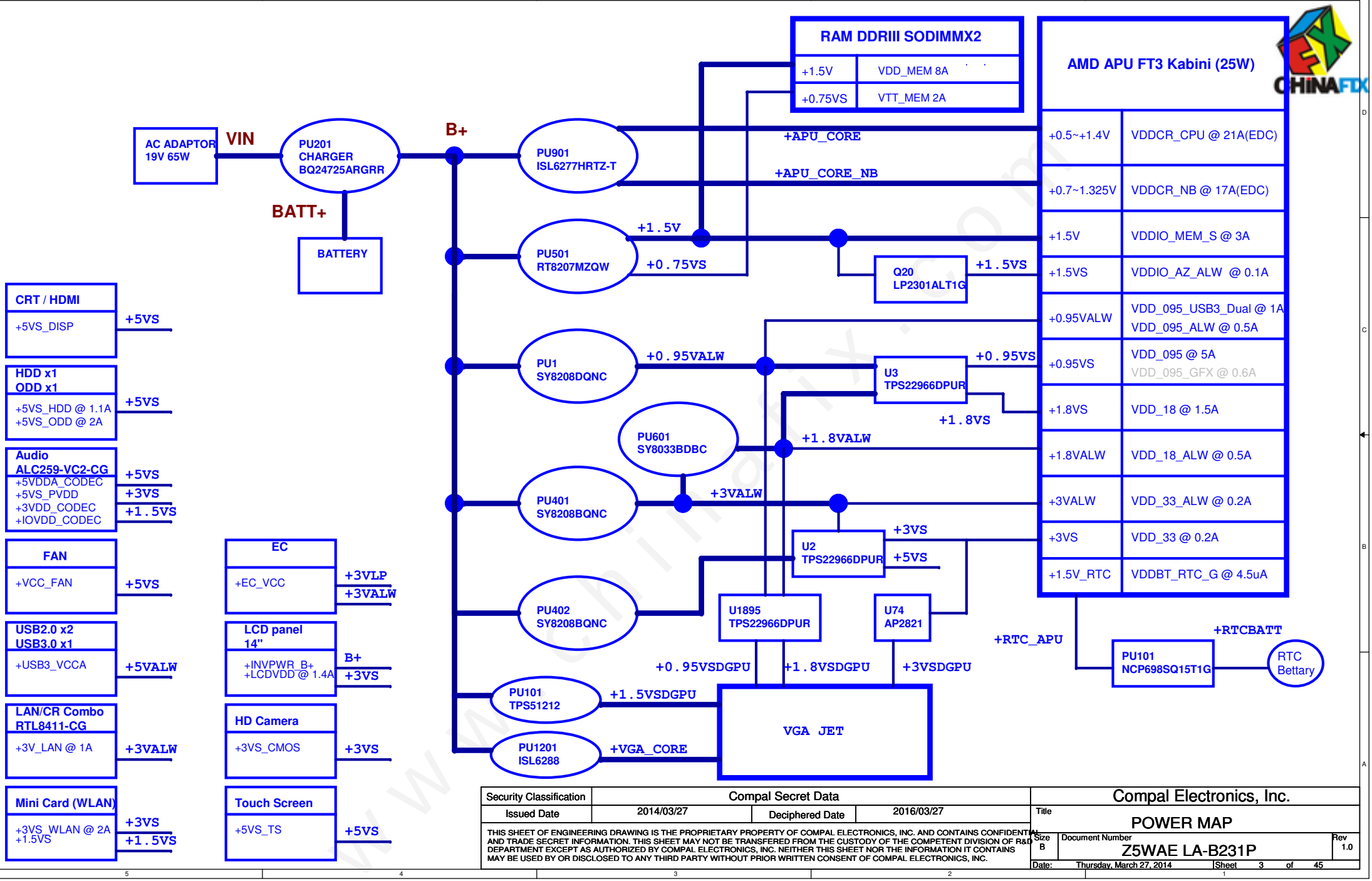
Compal Electronics, Inc.			
Title: BLOCK DIAGRAMS			
Size: B	Document Number: Z5WAE LA-B231P		Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 2 of 45		



Security Classification	Compal Secret Data		
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Title: POWER MAP

Size: B | Document Number: Z5WAE LA-B231P | Rev: 1.0

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	OFF	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+0.95VSDGPU	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

SMBus List

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H
			VGA Temp.		41H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			
Mini Card (DNI)					

ZZZ
PCB
Part Number = DA60014I000
PCB 157 LA-B231P REV0 M/B 2

ZZZ
X7681@
X76550BOL81
HYN 128M16*4

UAPU1 A6@
APU
Part Number = SA00007R900
S IC A6-6310 AM6310ITJ44JB 1.8G BGA 769P

UAPU1 E1@
APU
Part Number = SA00007RC00
S IC E1-6010 EM6010IUJ23JB 1.35G BGA769P

ZZZ
HDMI_ROYALTY
ROYALTY HDMI W/LOGO+HDCP
RO0000003HM
45@

ZZZ
X7682@
X76550BOL82
MIC 128M16*4

UAPU1 A4@
APU
Part Number = SA00007RA00
S IC A4-6210 AM6210ITJ44JB 1.8G BGA 769P

UAPU1 E2@
APU
Part Number = SA00007RB00
S IC E2-6110 EM6110ITJ44JB 1.5G BGA 769P

ZZZ
X7683@
X76550BOL83
SAM 128M16*4

U44 9022@
EC
Part Number = SA000075S20
S IC KB9022QC LQFP 128P EC CONTROLLER, A.3

U75 JET@
VGA
Part Number = SA000079010
S IC 216-0856000 A0 JET XT M2 FCBGA ABO!,

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOARD ID Table

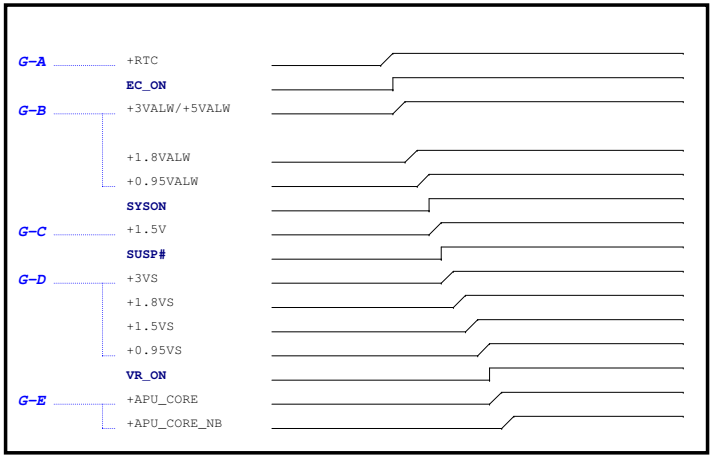
Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	
4	
5	
6	
7	

BOM Structure Table

BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
AL@	Auto Load EC ROM
RS@	R-short
JP@	Jump
TP@	Test point
SP@	Short pad for clear CMOS
1DMIC@	Use 1 DMIC
2DMIC@	Use 2 DMIC
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
A6@	Use A6 APU
E1@	Use E1 APU
BL@	Keyboard backlight
TPM@	Use discrete TPM module
TPUSB@	Use USB to I2C IC for T/P
TPSM@	Use APU SMBus for T/P
VGA@	Have discrete graphic
MARS@	Use Opal
JET@	Use Jet
128@	Dual channel VRAM,pop with MARS@
X76@	VRAM type select,control by X76XX@
X76XX@	VRAM type select, control level X76

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

APU POWER SEQUENCE



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Title: NOTES LIST

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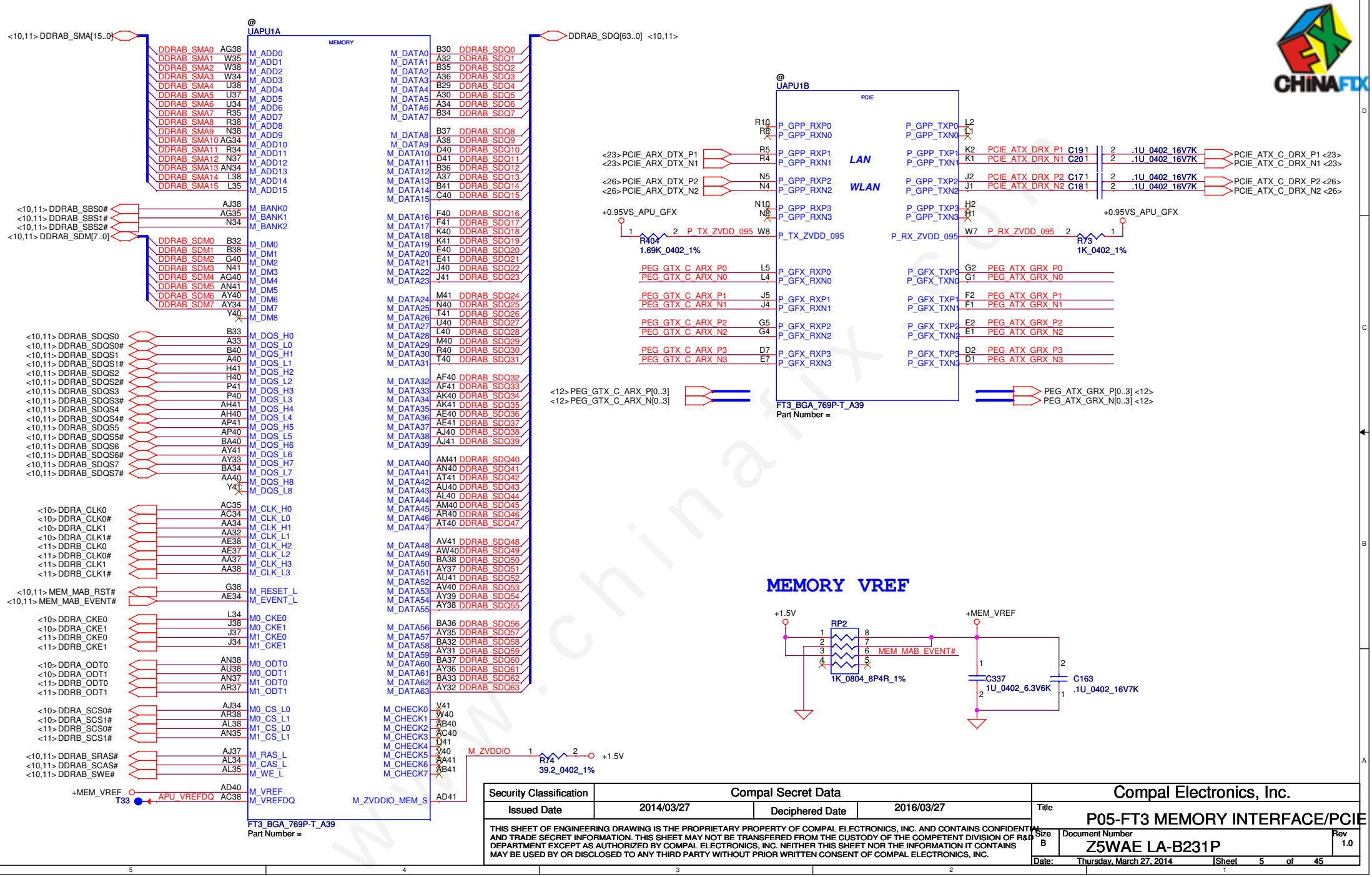

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Title: P05-FT3 MEMORY INTERFACE/PCIE

Size	Document Number	Rev
B	Z5WAE LA-B231P	1.0

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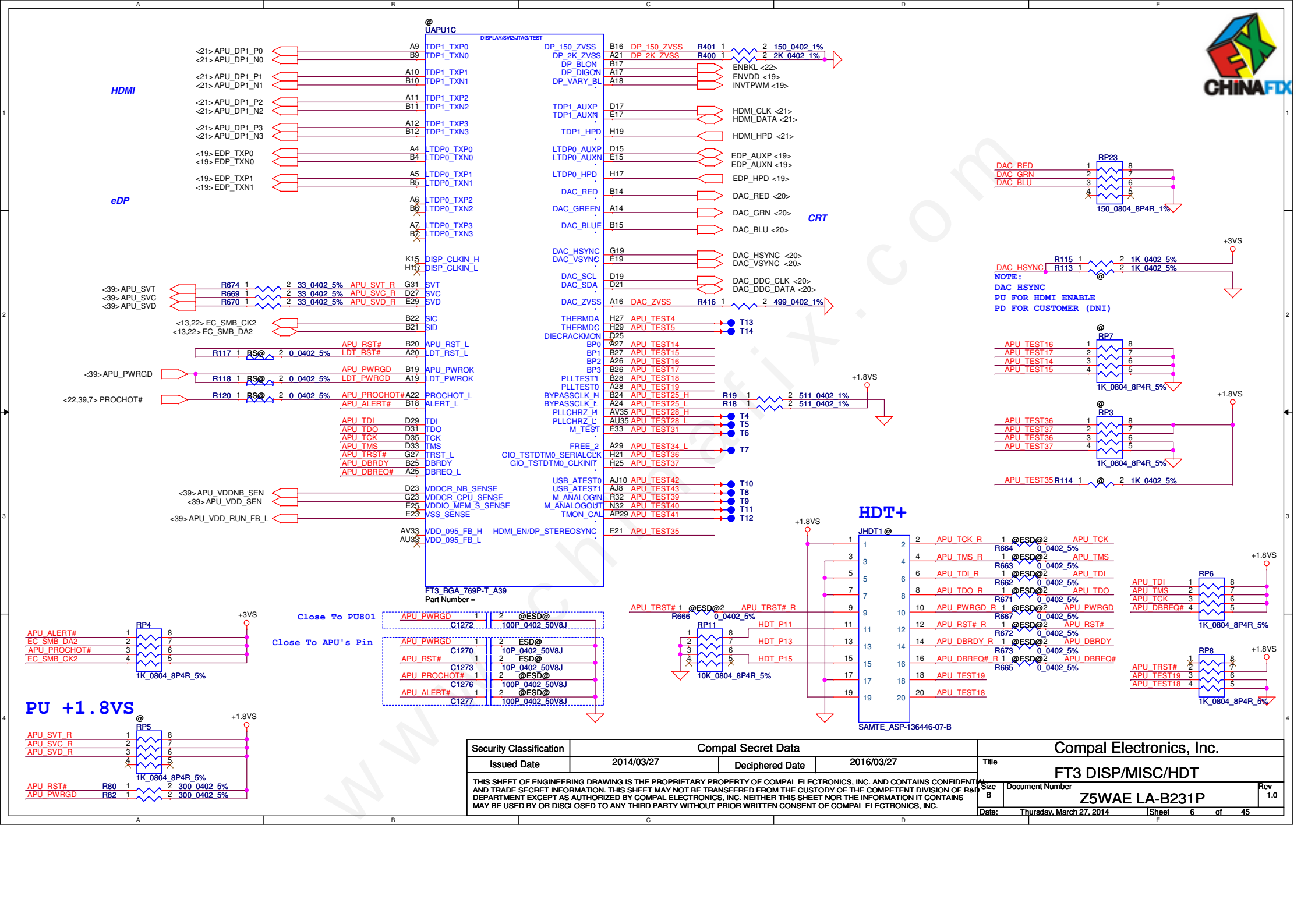

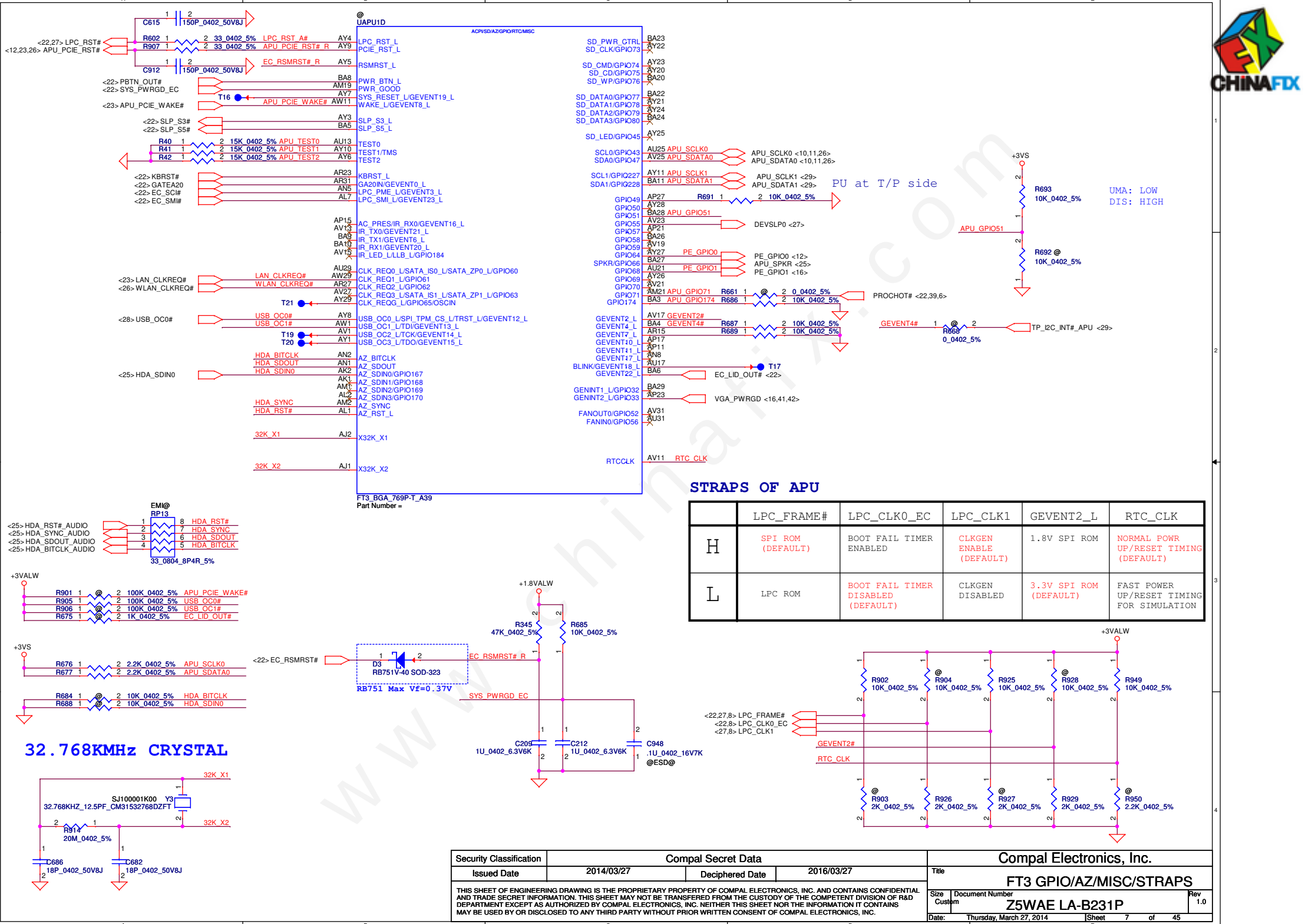

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Title: FT3 GPIO/AZ/MISC/STRAPS

Size	Document Number	Rev
Custom	Z5WAE LA-B231P	1.0

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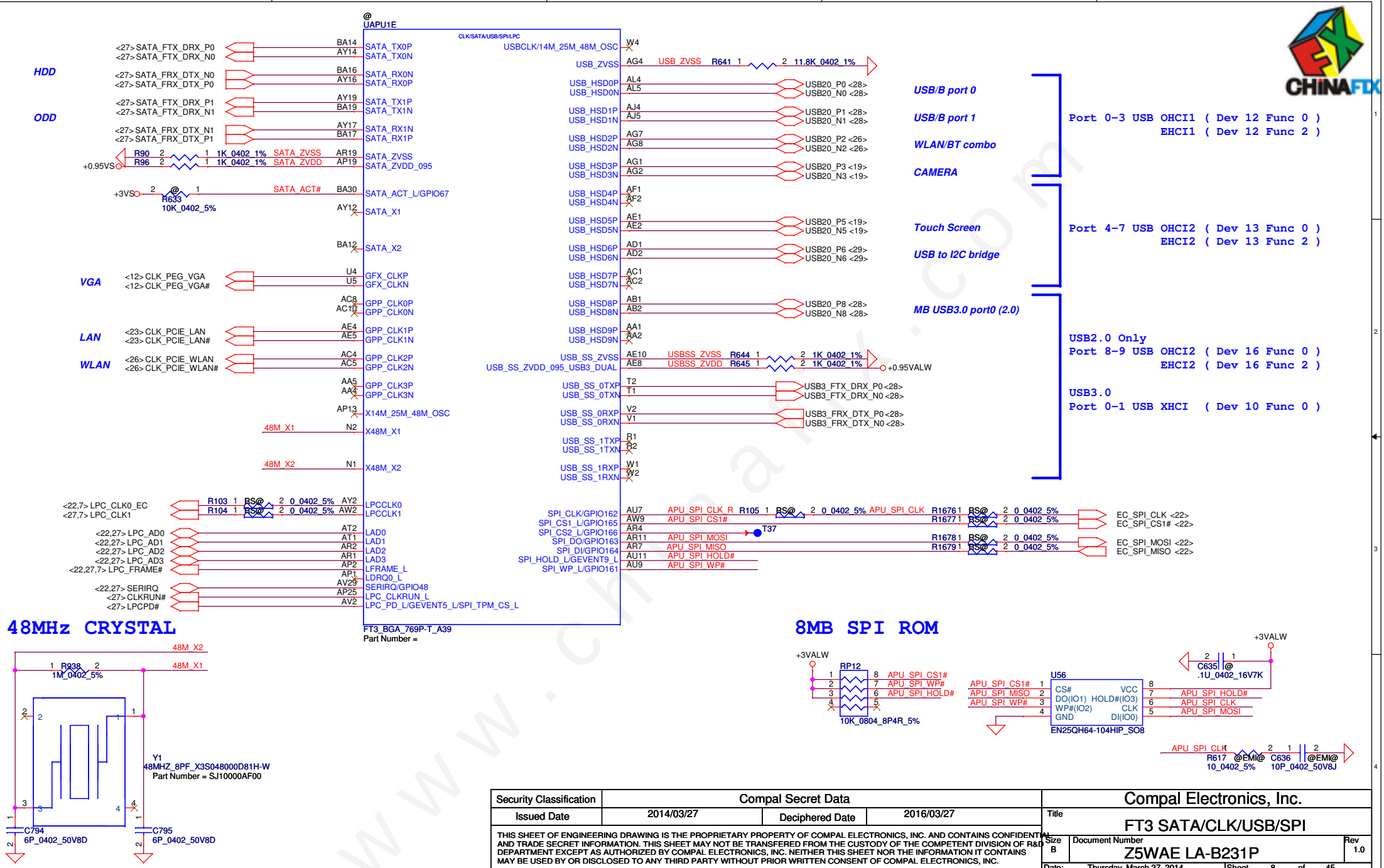

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Title: FT3 SATA/CLK/USB/SPI

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CORE POWER OF APU

+APU_CORE — VDDCR_CPU

C174 C180 C182 C183 C184 C186 C187 C188 C189 C190 1U_0402_6.3V6K; C191 180P_0402_50V8J

INTEGRATED GPU POWER OF APU

+APU_CORE_NB — VDDCR_NB

C205 C206 C207 C208 C209 C210 C211 C212 C213 1U_0402_6.3V6K; C214 180P_0402_50V8J

+3VALW/+3VS OF APU

+3VS — C262 1U_0402_6.3V6K; C263 C264 1U_0402_6.3V6K — +3VALW

VDD_33 — C257 180P_0402_50V8J — VDD_33_ALW

+1.5V/+1.5VS OF APU

VDDIO_AZ_ALW
(Could be S0 or S5 power rail)

+1.5V — VDDIO_MEM_S — PLANE SPLIT

C234 C235 C236 C237 C238 C239 C240 C241 C242 C243 C244 1U_0603_6.3V6M; C245 C246 C247 C248 C249 C250 C251 C252 C253 C254 1U_0402_1.8V7K; C255 C256 180P_0402_50V8J

+1.5VS — C258 C259 C260 4.7U_0603_6.3V6K; C261 C262 C263 1U_0402_6.3V6K

+0.95VALW/+0.95VS OF APU

+0.95VS — VDD_095 — VDD_095_GFX — +0.95VS_APU_GFX

L22 FBMA-L11-201209-121LMA50T_0805

C194 C195 C196 C197 C198 C199 C200 C201 C213 180P_0402_50V8J; C202 C203 1U_0603_6.3V6M

+0.95VALW — C204 C205 C206 C207 C208 C209 C210 C211 C212 1U_0402_6.3V6K

+0.95VALW — C214 C215 C216 C217 C218 C219 C220 C221 C222 1U_0402_6.3V6K

VDD_095_USB3_DUAL — VDD_095_ALW

+1.8VALW/+1.8VS OF APU

+1.8VS — VDD_18

C223 C224 C225 C226 C227 C228 C229 C230 C231 C232 1U_0402_6.3V6K; C946 1U_0402_16V7K @ESD@; C947 1U_0402_16V7K @ESD@

+1.8VALW — C233 1U_0603_6.3V6M

+1.8VALW — C160 4.7U_0603_6.3V6K; C234 C235 C236 C237 C238 C239 C240 C241 C242 C243 C244 C245 1U_0402_6.3V6K; C246 180P_0402_50V8J

VDD_18_ALW

3A

@ UAPU1F — POWER — FT3_BGA_769P-T_A39 Part Number =

VDDIO_MEM_S_1 … VDDIO_MEM_S_23 (J35 … AR35)

VDDCR_CPU_1 … VDDCR_CPU_26 (L21 … AE27) — +APU_CORE

R119 0_0402_5% RS@

VDDCR_NB_1 … VDDCR_NB_9 (L13 … AG21) — +APU_CORE_NB

VDDIO_AZ_ALW_1 (AL10), VDDIO_AZ_ALW_2 (AL11)

VDD_18_ALW_1 (B1), VDD_18_ALW_2 (B2)

VDD_33_ALW_1 (AL13), VDD_33_ALW_2 (AM13)

VDD_095_USB3_DUAL_1 (AR5) … VDD_095_USB3_DUAL_4 (AW5)

VDD_095_ALW_1 (AE11) … VDD_095_ALW_4 (AJ13)

VDDBT_RTC_G (AN4) — +RTC_APU_R

VDD_18_1 … VDD_18_4 (A2, A3, B3, C3) — +1.8VS

VDD_33_1 (AM15), VDD_33_2 (AM17) — +3VS

VDD_095_1 … VDD_095_9 (AG23, AG27, AJ21, AJ27, AL21, AL23, AL27, AM23, AM25) — +0.95VS

VDD_095_GFX_1 … VDD_095_GFX_3 (U10, W10, AA10) — +0.95VS_APU_GFX

@ UAPU1G — GND — FT3_BGA_769P-T_A39 Part Number =

VSS_1 … VSS_187 (A8 … AL39)

@ UAPU1H — GND — FT3_BGA_769P-T_A39 Part Number =

VSS_125 … VSS_242, VSSBG_DAC, VBURN, PSEN (W29 … AN29)

RTC OF APU

VDDBT_RTC_G

+RTC_APU_R — W=20mils — R93 10K_0402_5% — +RTC_APU

C166 0.22U_0402_10V6K

CLRP1 SP@ SHORT PADS

Need OPEN for Clear CMOS

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Title: FT3 PWR/GND

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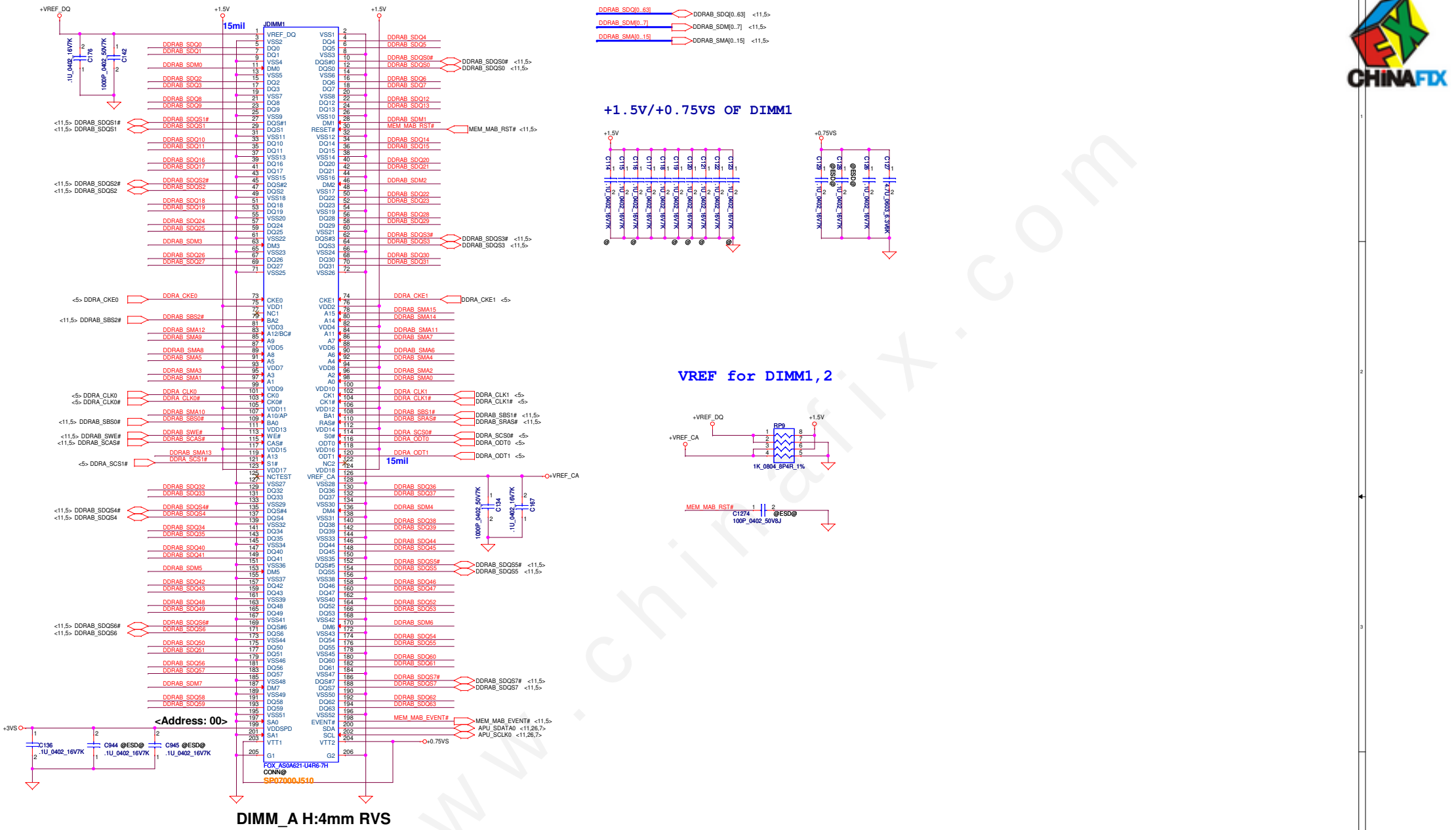

DIMM_A H:4mm RVS

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Title	DDR3 SODIMM-I Socket		
Size C	Document Number Z5WAE LA-B231P		Rev 1.0
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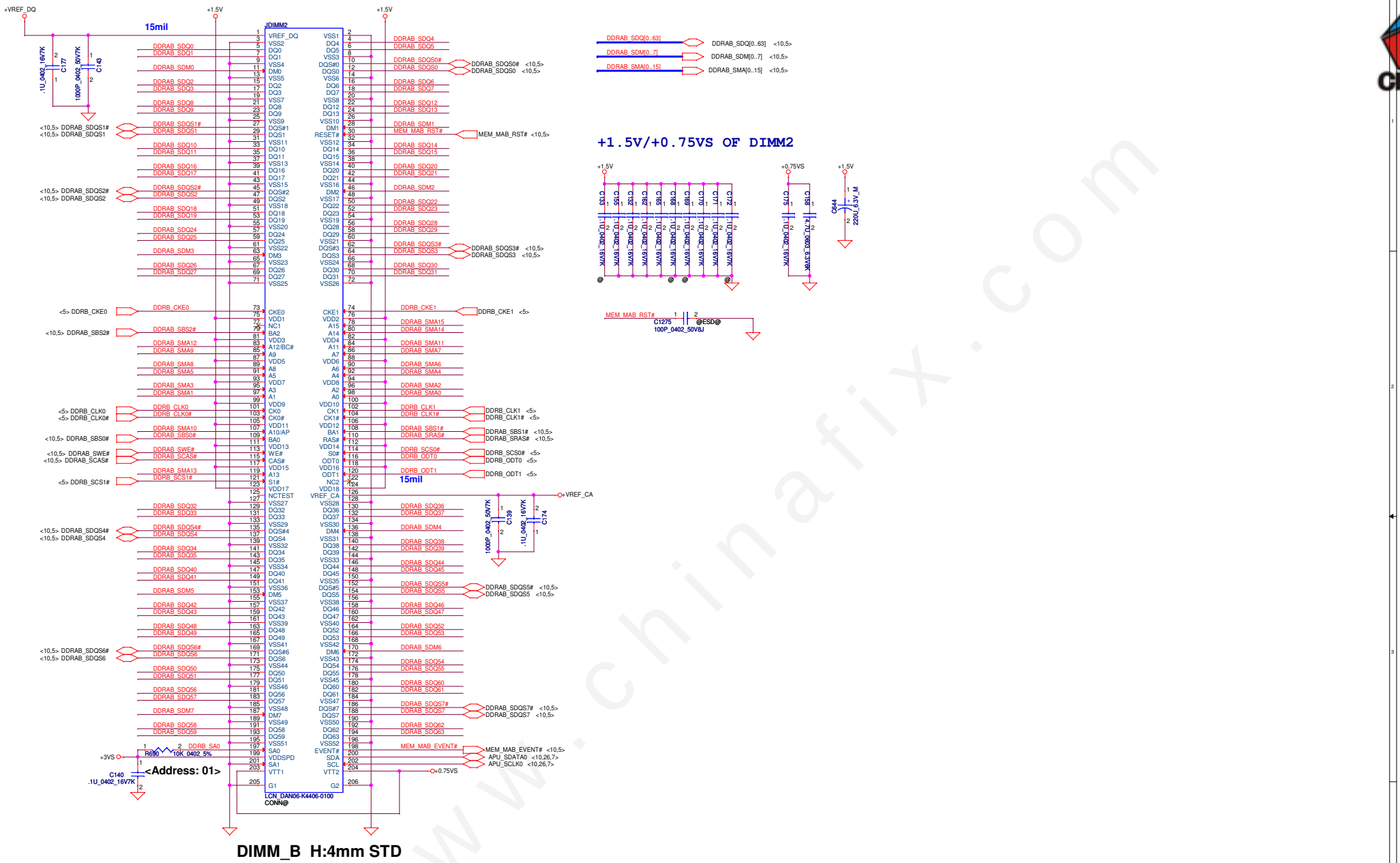

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Title	DDR3 SODIMM-II Socket		
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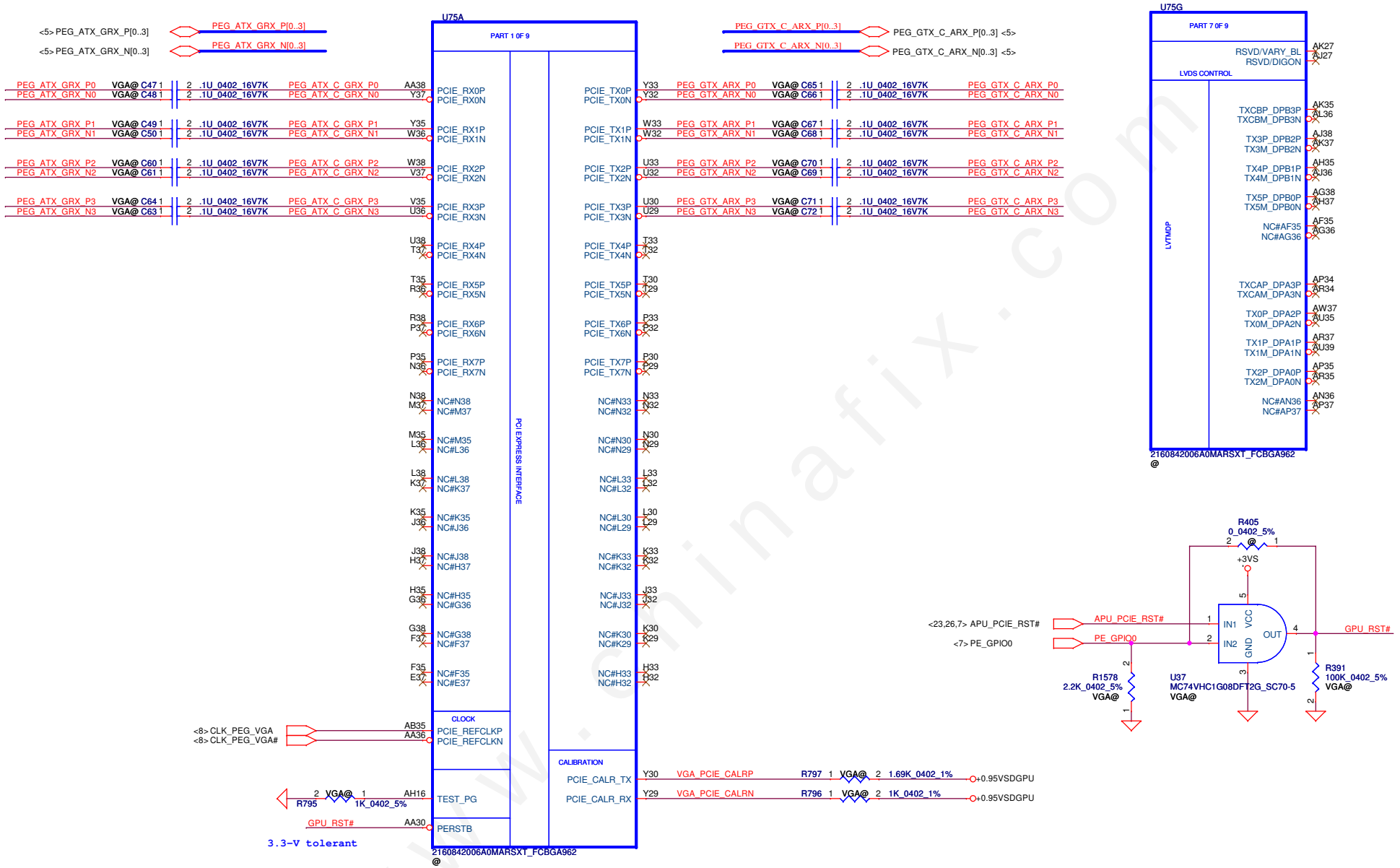
GFX PCIE LANE REVERSAL



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Title: MARS-Pro_PCIE			
Size: Custom	Document Number: Z5WAE LA-B231P		Rev: 1.0
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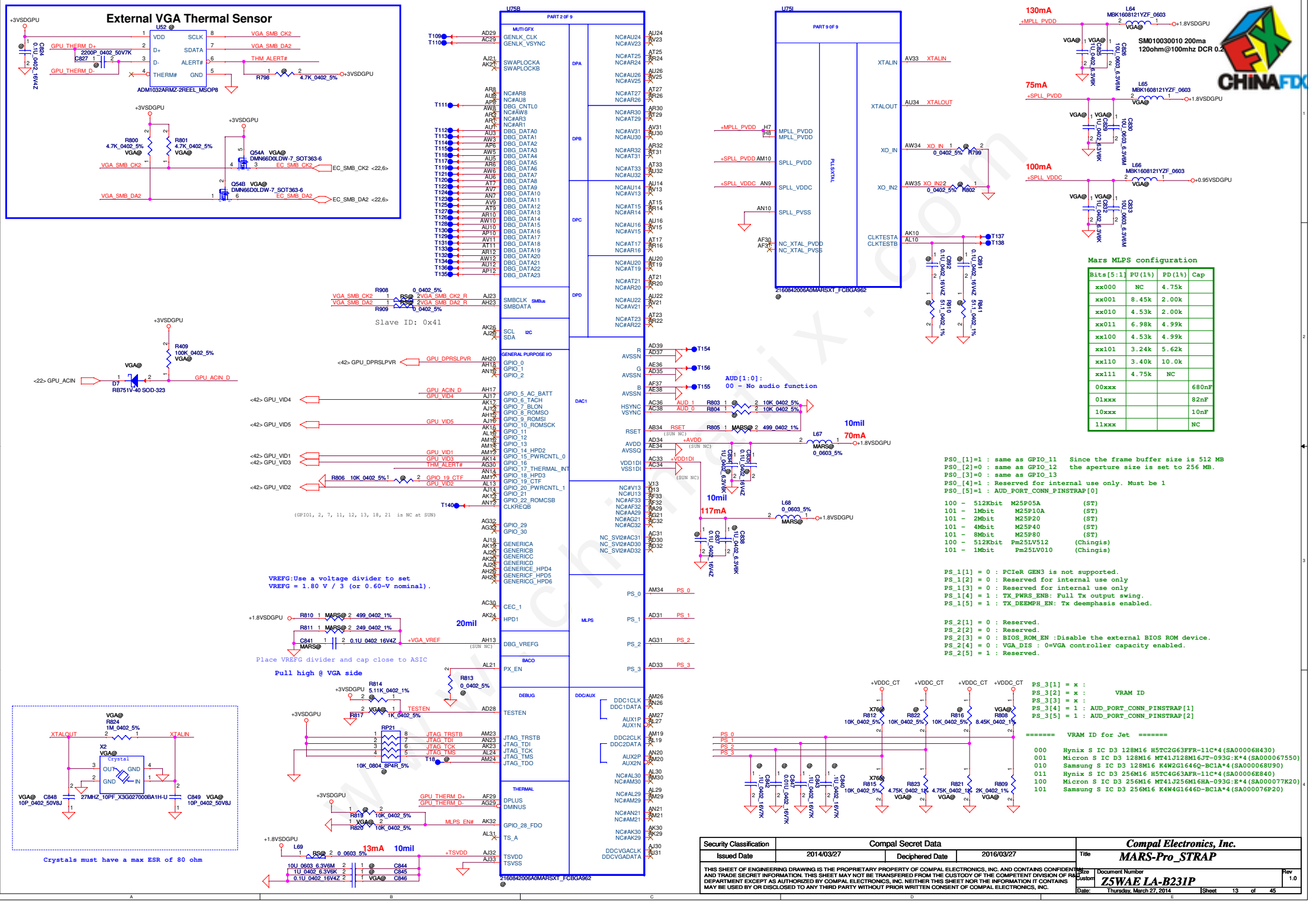
External VGA Thermal Sensor
U52 @
ADM1032ARMZ-2REEL_MSOP8
GPU_THERM_D+
GPU_THERM_D-
VGA_SMB_CK2
VGA_SMB_DA2
THM_ALERT#
Q54A VGA@ DMN66D0LDW-7_SOT363-6
Q54B VGA@ DMN66D0LDW-7_SOT363-6
EC_SMB_CK2 <22,6>
EC_SMB_DA2 <22,6>
U75B
PART 2 OF 9
MUTI GFX
SMBus
I2C
GENERAL PURPOSE I/O
DAC1
MLPS
DEBUG
THERMAL
DDC/AUX
2160842006A0MARSXT_FCBGA962
Slave ID: 0x41
GPU_DPRSLPVR
GPU_ACIN
GPU_ACIN_D
GPU_VID4
GPU_VID5
GPU_VID1
GPU_VID3
GPU_VID2
VREFG:Use a voltage divider to set
VREFG = 1.80 V / 3 (or 0.60-V nominal).
Place VREFG divider and cap close to ASIC
Pull high @ VGA side
Crystals must have a max ESR of 80 ohm
U75I
PART 9 OF 9
PLL/XTAL
2160842006A0MARSXT_FCBGA962
AUD[1:0]:
00 - No audio function
130mA
75mA
100mA
SM100030010 200ma
120ohm@100mhz DCR 0.2
Mars MLPS configuration
Bits[5:1] | PU(1%) | PD(1%) | Cap
xx000 | NC | 4.75k |
xx001 | 8.45k | 2.00k |
xx010 | 4.53k | 2.00k |
xx011 | 6.98k | 4.99k |
xx100 | 4.53k | 4.99k |
xx101 | 3.24k | 5.62k |
xx110 | 3.40k | 10.0k |
xx111 | 4.75k | NC |
00xxx | | | 680nF
01xxx | | | 82nF
10xxx | | | 10nF
11xxx | | | NC
PS0_[1]=1 : same as GPIO_11 Since the frame buffer size is 512 MB
PS0_[2]=0 : same as GPIO_12 the aperture size is set to 256 MB.
PS0_[3]=0 : same as GPIO_13
PS0_[4]=1 : Reserved for internal use only. Must be 1
PS0_[5]=1 : AUD_PORT_CONN_PINSTRAP[0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)
PS_1[1] = 0 : PCIeR GEN3 is not supported.
PS_1[2] = 0 : Reserved for internal use only
PS_1[3] = 0 : Reserved for internal use only
PS_1[4] = 1 : TX_PWRS_ENB: Full Tx output swing.
PS_1[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.
PS_2[1] = 0 : Reserved.
PS_2[2] = 0 : Reserved.
PS_2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
PS_2[4] = 0 : VGA_DIS : 0=VGA controller capacity enabled.
PS_2[5] = 1 : Reserved.
PS_3[1] = x :
PS_3[2] = x : VRAM ID
PS_3[3] = x :
PS_3[4] = 1 : AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] = 1 : AUD_PORT_CONN_PINSTRAP[2]
======= VRAM ID for Jet =======
000 Hynix S IC D3 128M16 H5TC2G63FFR-11C*4(SA00006H430)
001 Micron S IC D3 128M16 MT41J128M16JT-093G:K*4(SA000067550)
010 Samsung S IC D3 128M16 K4W2G1646Q-BC1A*4(SA000068U90)
011 Hynix S IC D3 256M16 H5TC4G63AFR-11C*4(SA00006E840)
100 Micron S IC D3 256M16 MT41J256M16HA-093G:E*4(SA000077K20)
101 Samsung S IC D3 256M16 K4W4G1646D-BC1A*4(SA000076P20)
Mars-Pro_STRAP
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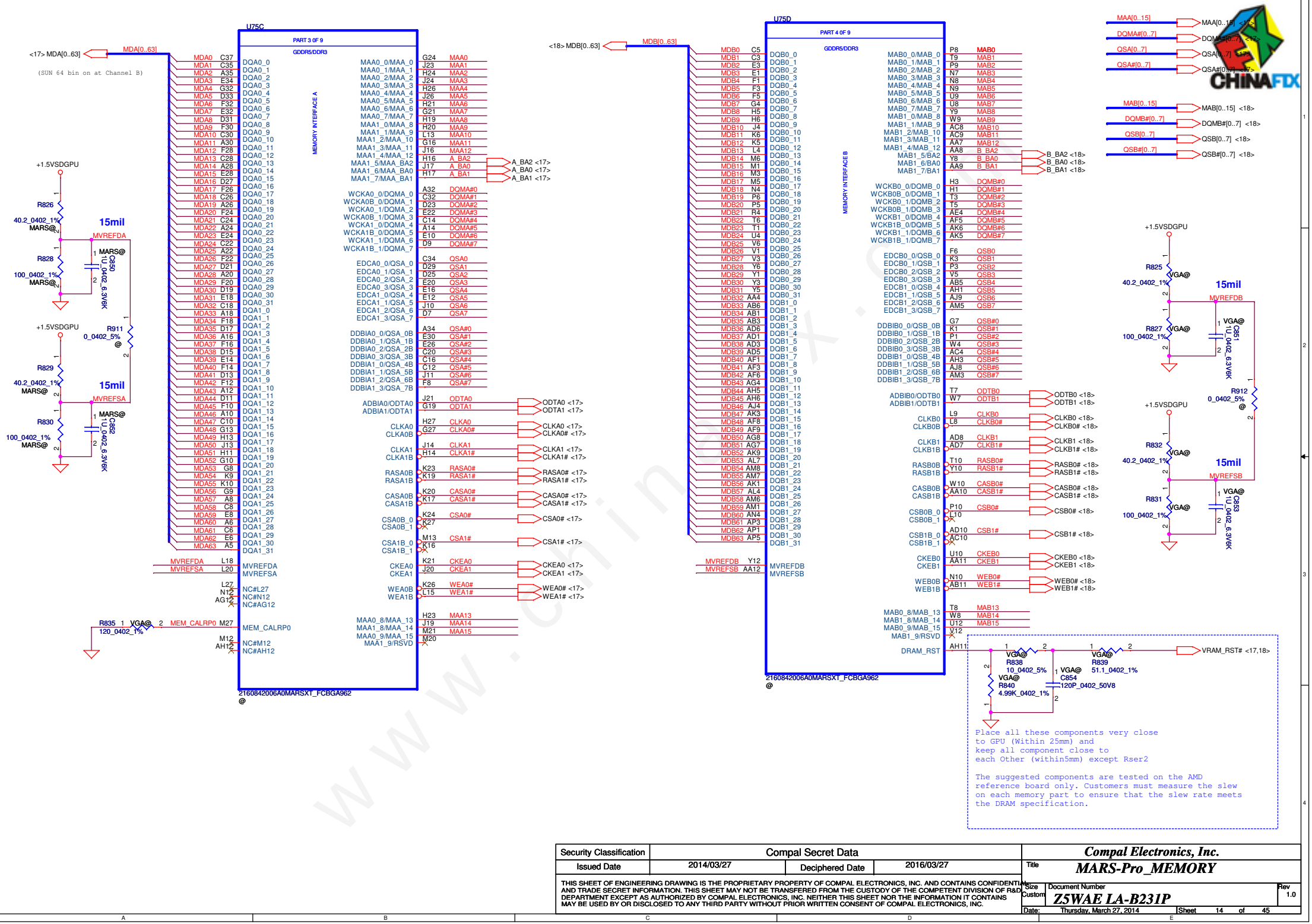

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Title: MARS-Pro_MEMORY			
Size: Custom	Document Number: Z5WAE LA-B231P		Rev: 1.0
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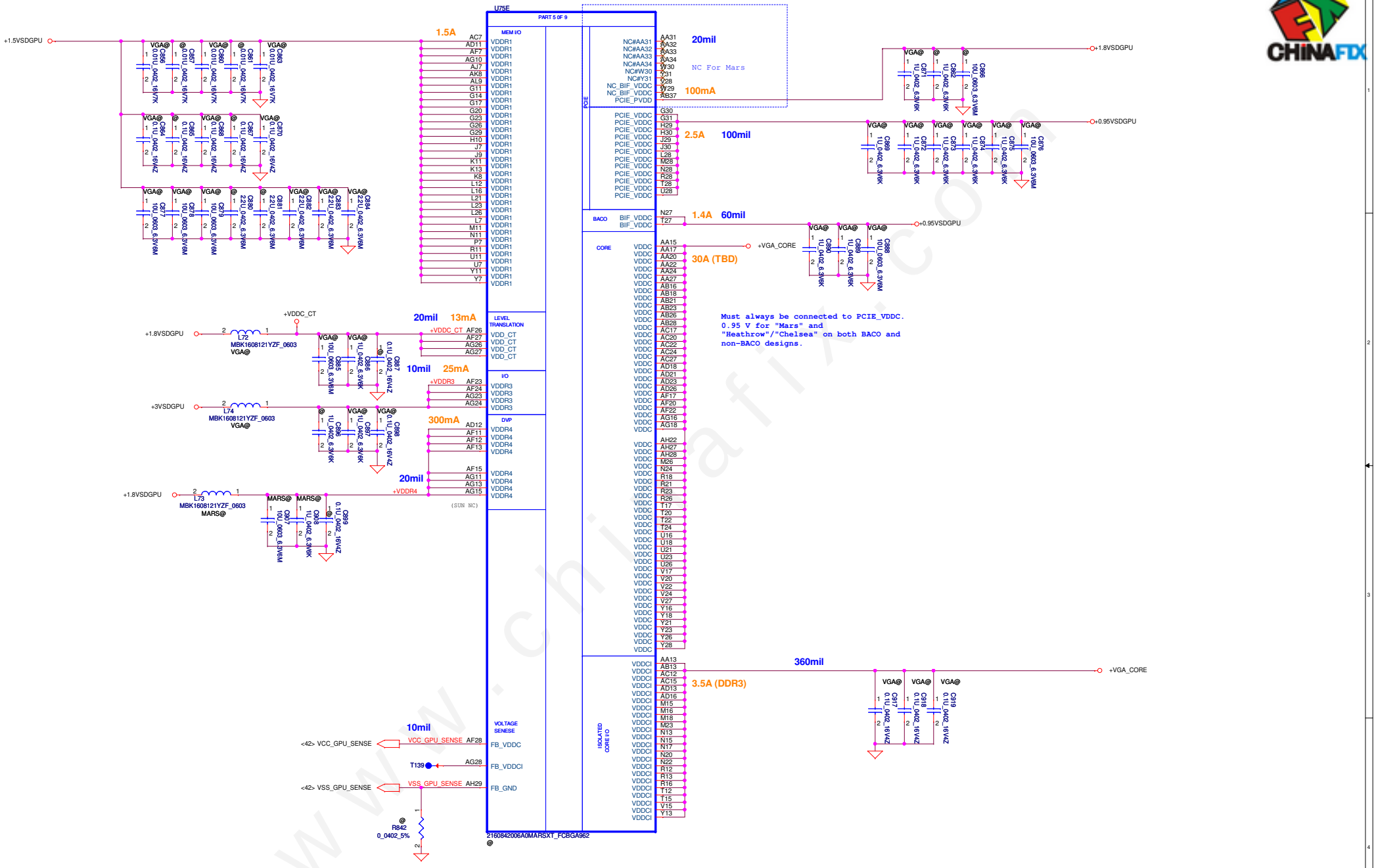
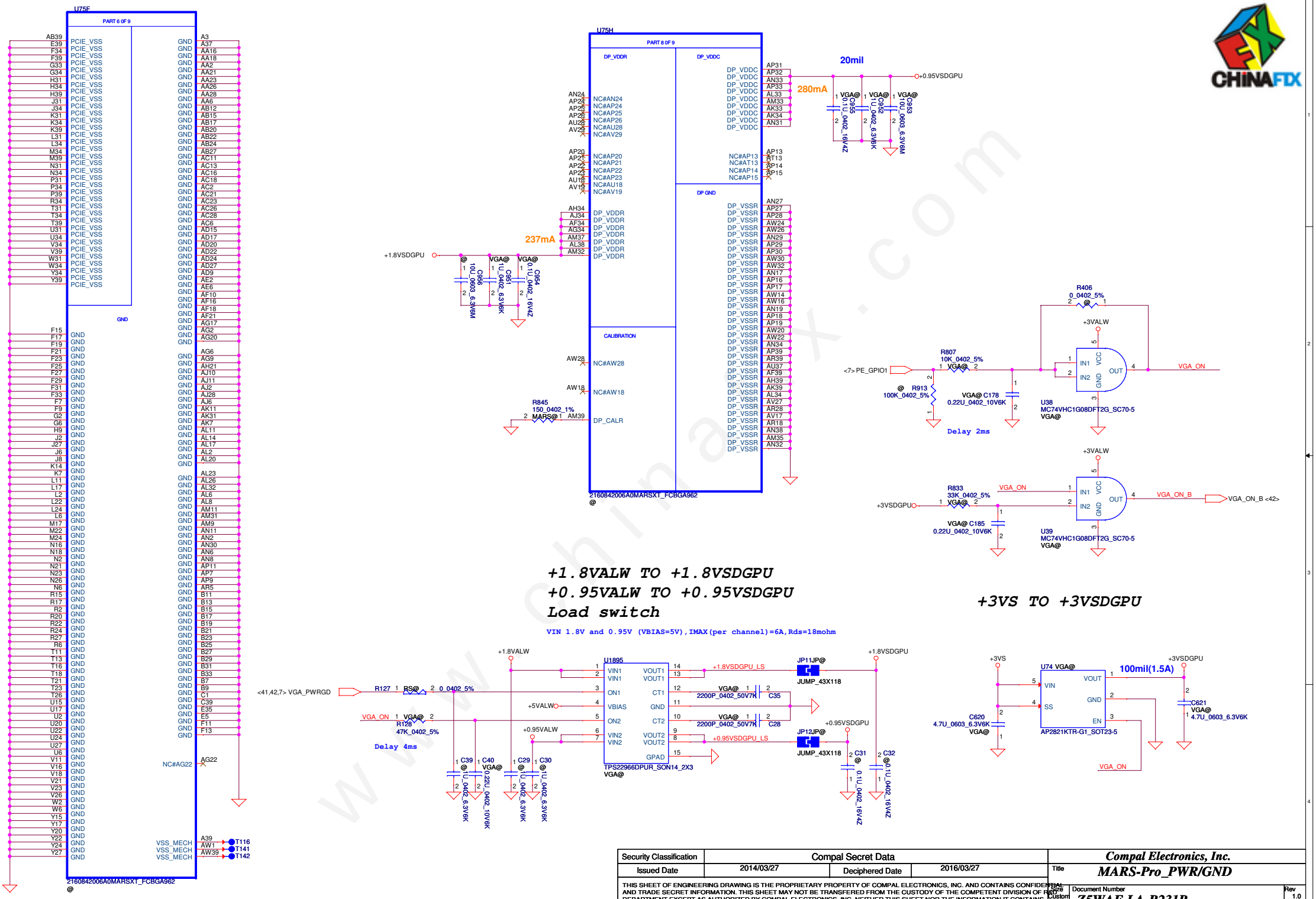


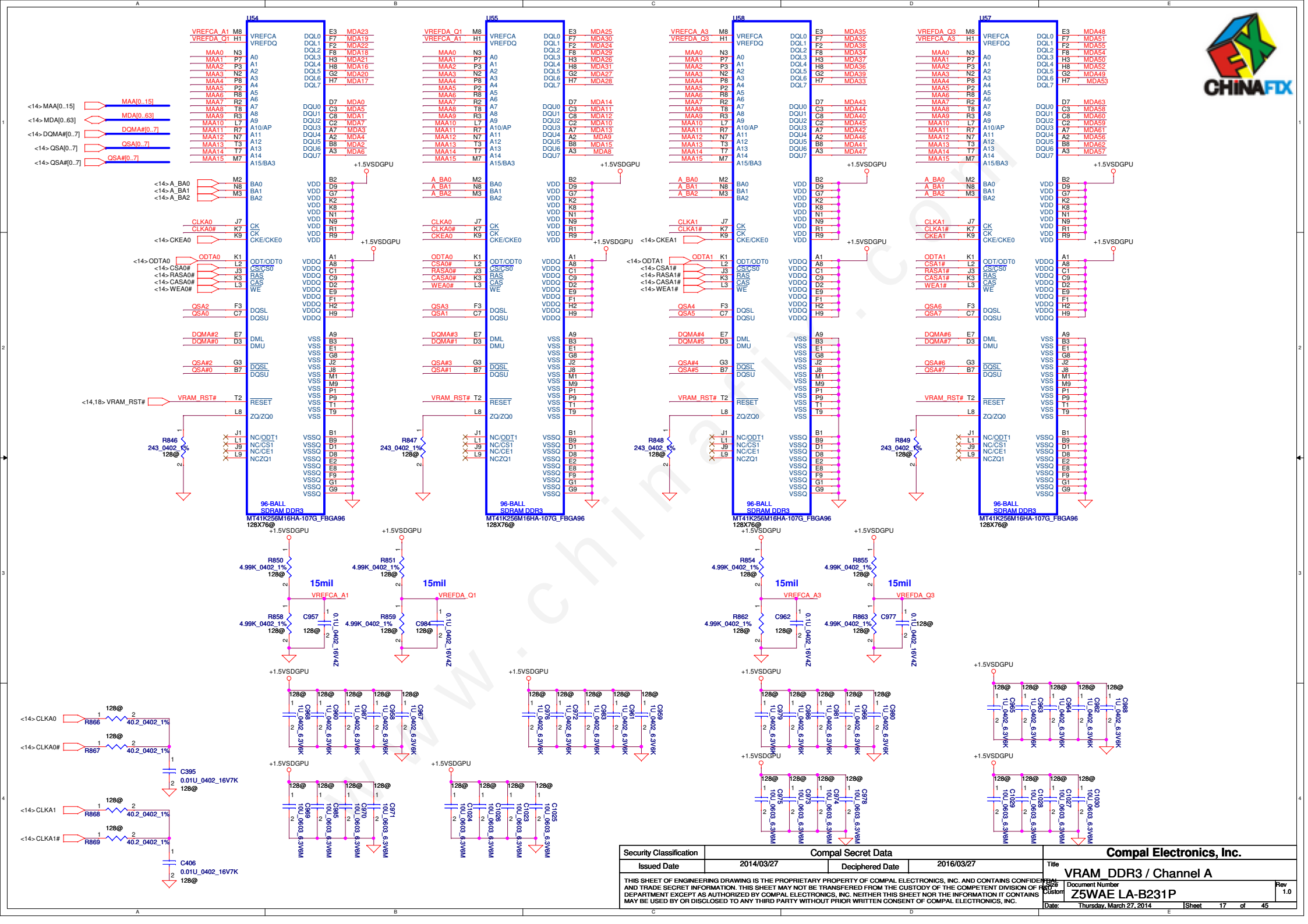
Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.			
Title: MARS-Pro_PWR/GND			
Size: Custom	Document Number: Z5WAE LA-B231P		Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 15 of 45		



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.			
Title	MARS-Pro_PWR/GND		
Size Custom	Document Number Z5WAE LA-B231P		Rev 1.0
Date: Thursday, March 27, 2014	Sheet 16 of 45		


U54
U55
U58
U57
96-BALL SDRAM DDR3
MT41K256M16HA-107G_FBGA96
128X76@
+1.5VSDGPU
<14> MAA[0..15]
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<14,18> VRAM_RST#
R846 243_0402_1% 128@
R847 243_0402_1% 128@
R848 243_0402_1% 128@
R849 243_0402_1% 128@
R850 4.99K_0402_1% 128@
R851 4.99K_0402_1% 128@
R854 4.99K_0402_1% 128@
R855 4.99K_0402_1% 128@
15mil
VREFCA_A1
VREFDA_Q1
VREFCA_A3
VREFDA_Q3
R858 4.99K_0402_1% 128@
R859 4.99K_0402_1% 128@
R862 4.99K_0402_1% 128@
R863 4.99K_0402_1% 128@
C957 0.1U_0402_16V4Z 128@
C984 0.1U_0402_16V4Z 128@
C962 0.1U_0402_16V4Z 128@
C977 0.1U_0402_16V4Z 128@
<14> CLKA0
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<14> CLKA1#
R866 40.2_0402_1%
R867 40.2_0402_1%
R868 40.2_0402_1%
R869 40.2_0402_1%
C395 0.01U_0402_16V7K 128@
C406 0.01U_0402_16V7K 128@
Security Classification
Compal Secret Data
Issued Date
2014/03/27
Deciphered Date
2016/03/27
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Compal Electronics, Inc.
Title
VRAM_DDR3 / Channel A
Size
Custom
Document Number
Z5WAE LA-B231P
Rev
1.0
Date:
Thursday, March 27, 2014
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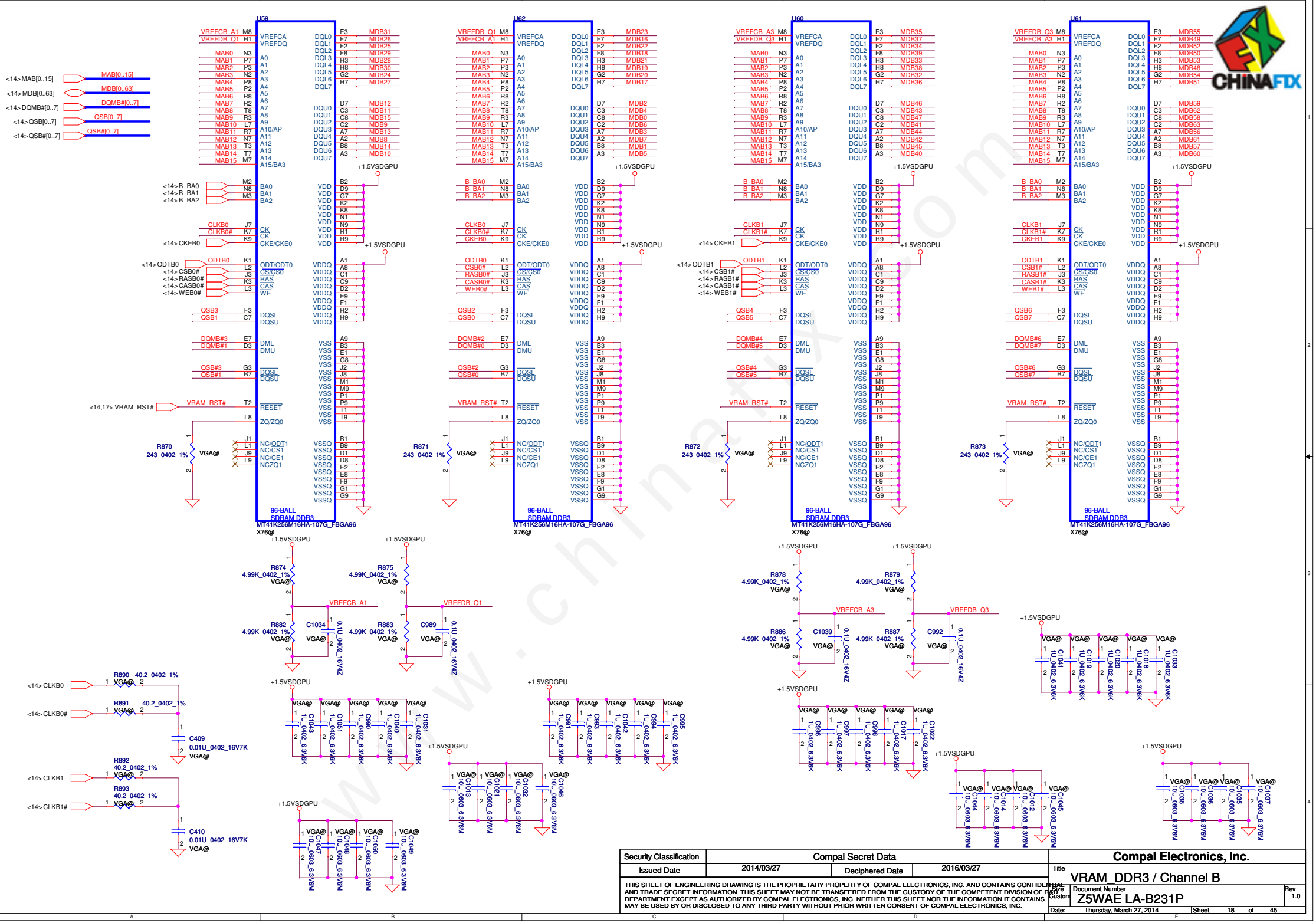
of
45



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

Size: Custom | Document Number: Z5WAE LA-B231P | Rev: 1.0

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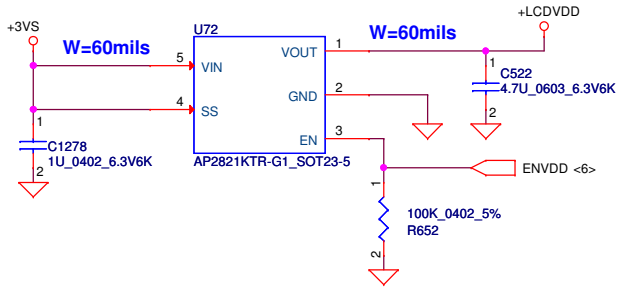
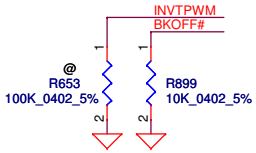
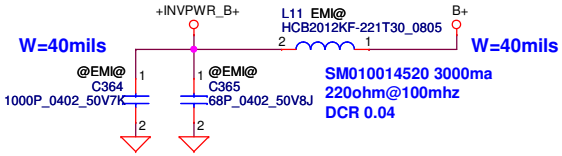
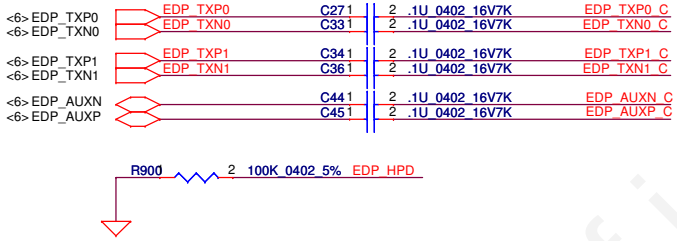
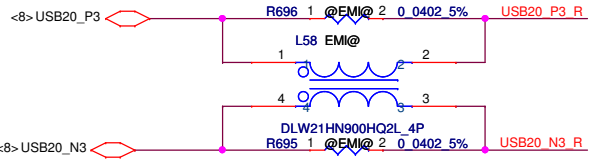
LCD POWER CIRCUIT

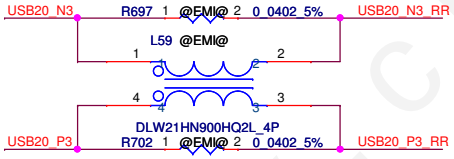






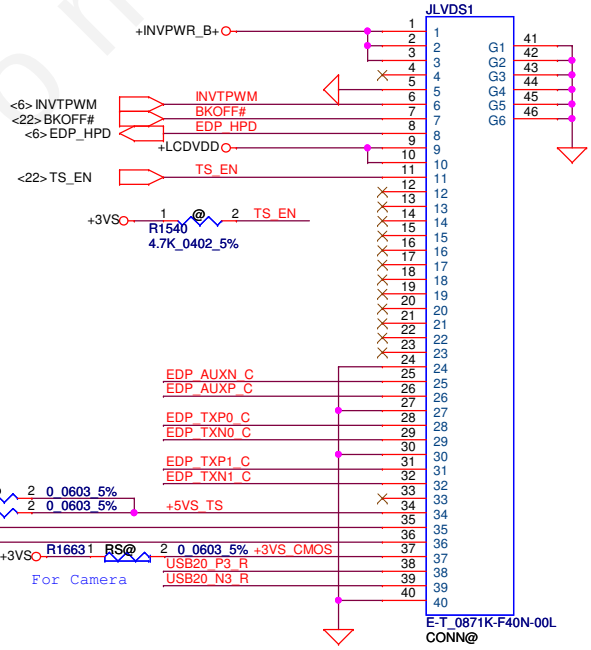


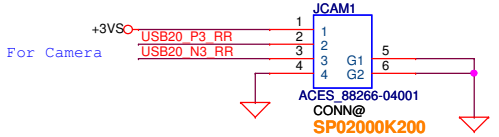




Touch Screen

eDP PANEL Conn.





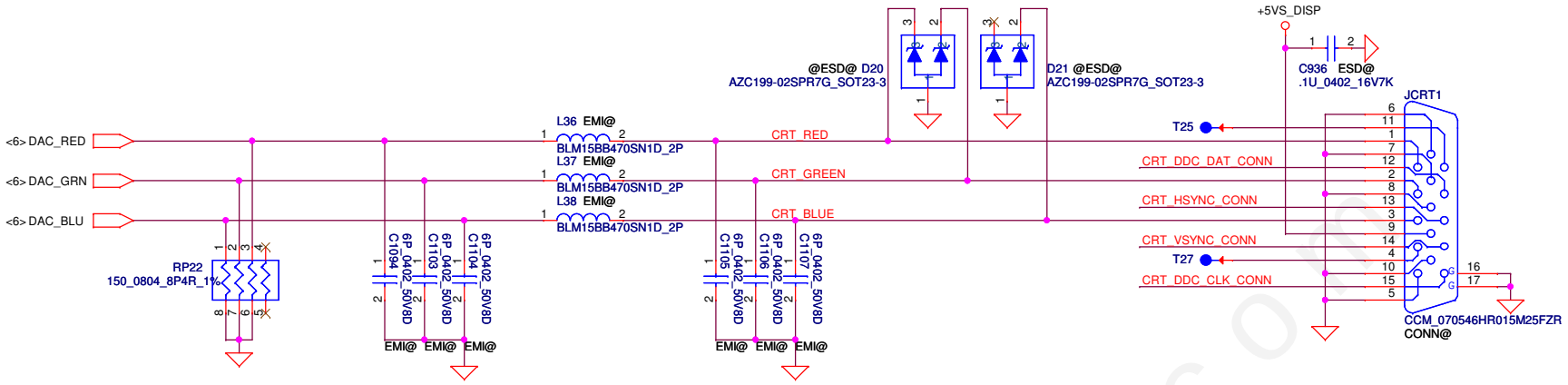
Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

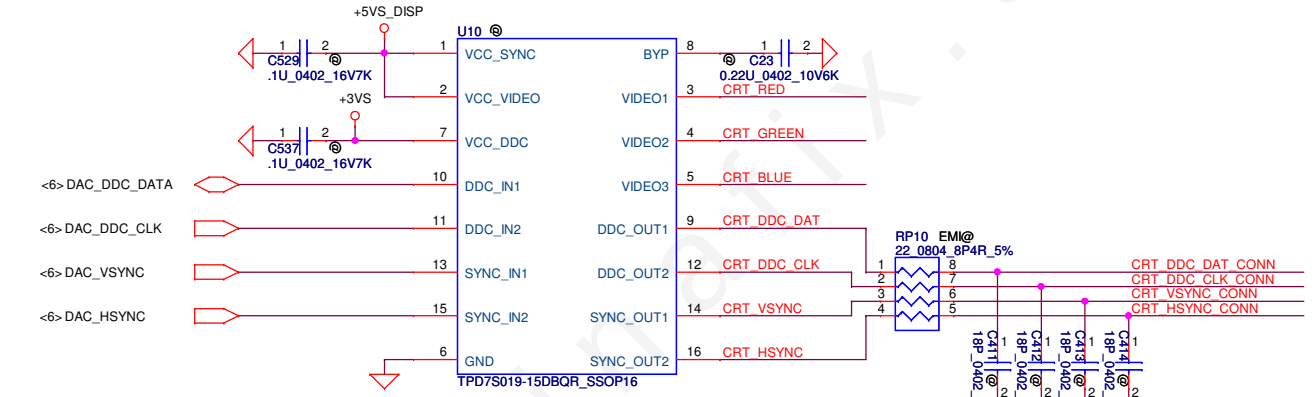
Compal Electronics, Inc.

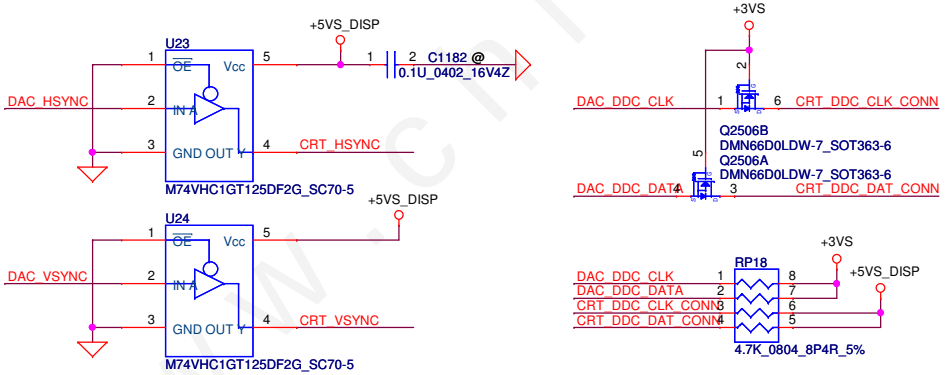
Title: eDP/Camera/TS

Size: B | Document Number: Z5WAE LA-B231P | Rev: 1.0

Date: Thursday, March 27, 2014 | Sheet 19 of 45







Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: CRT CONN

Size: B | Document Number: Z5WAE LA-B231P | Rev: 1.0

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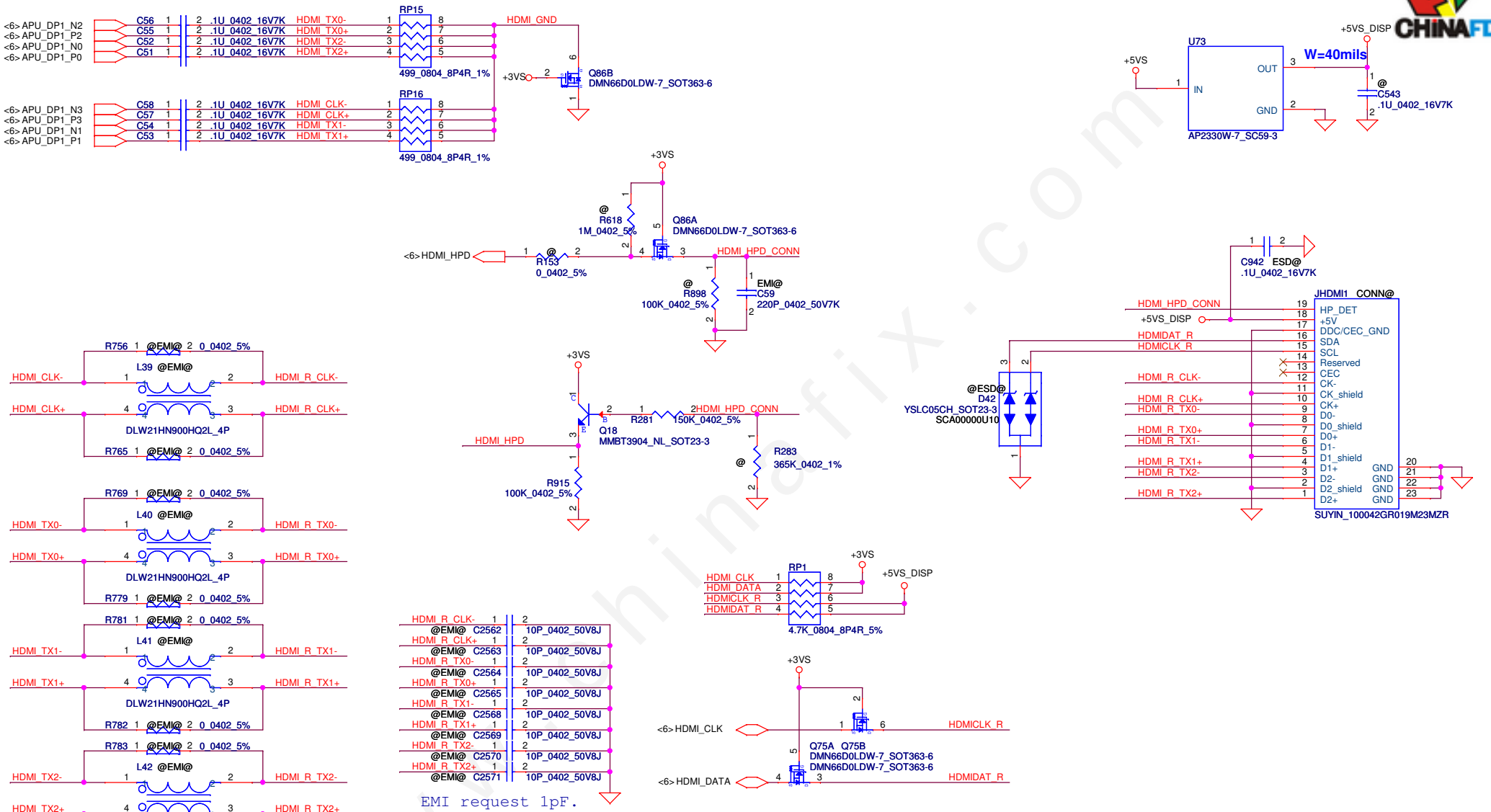

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: HDMI CONN

Size	Document Number	Rev
B	Z5WAE LA-B231P	1.0

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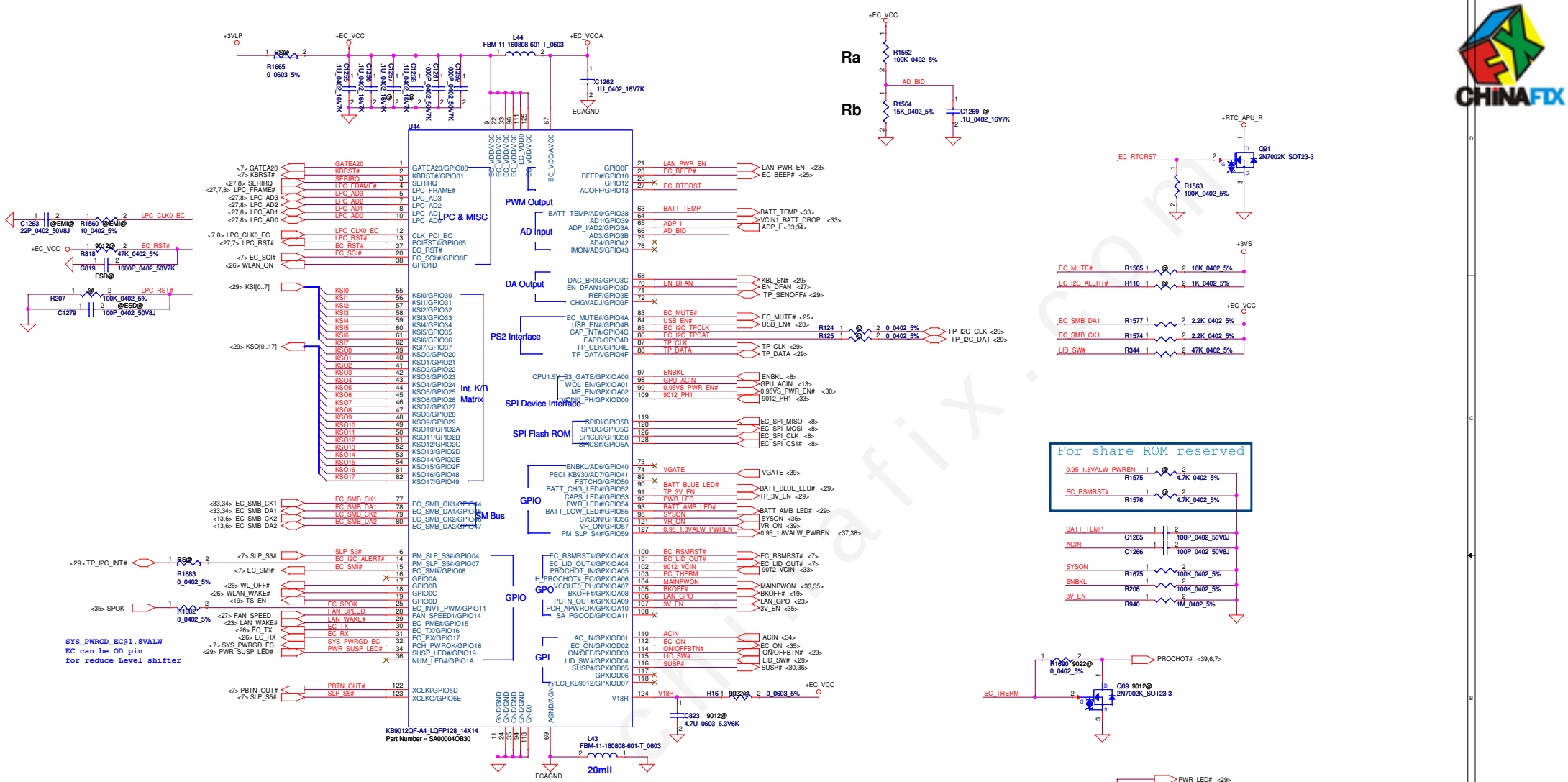
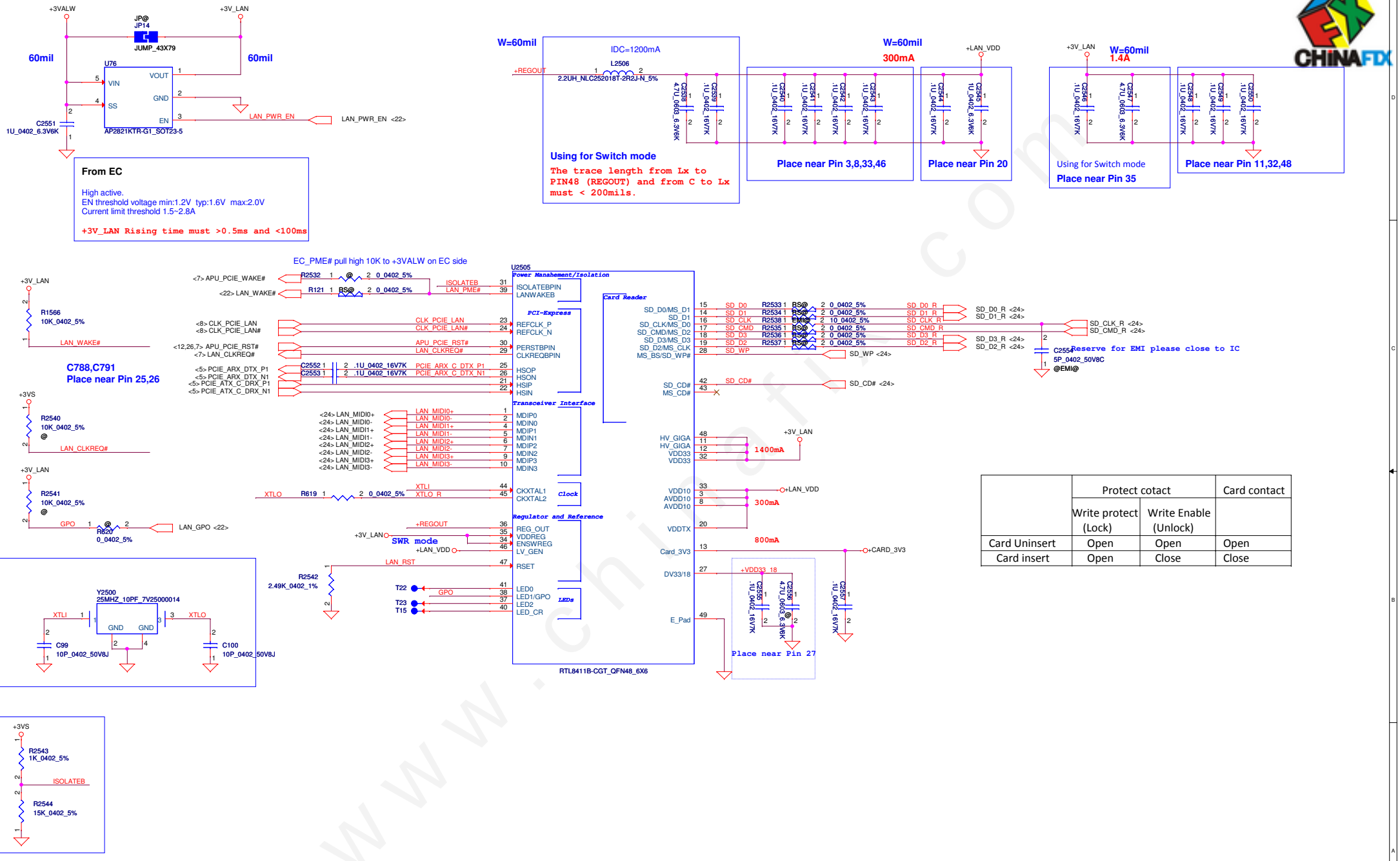


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/27	Deciphered Date	2016/03/27
Title	EC ENE-KB9012		
Size C	Document Number Z5WAE LA-B231P		Rev 1.0
Date: Thursday, March 27, 2014	Sheet 22 of 45		



	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: LAN RTL8411-CG

Size: Custom | Document Number: Z5WAE LA-B231P | Rev: 1.0

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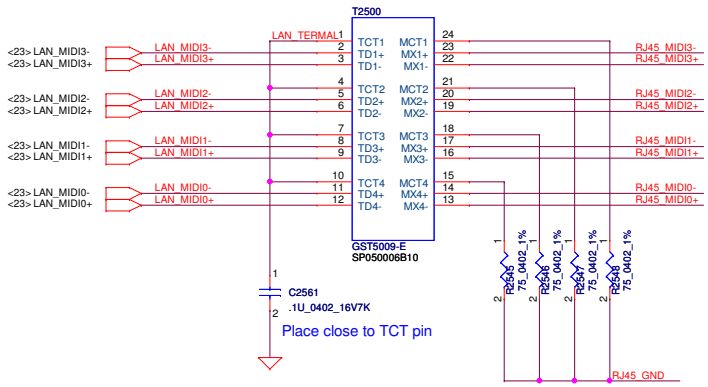
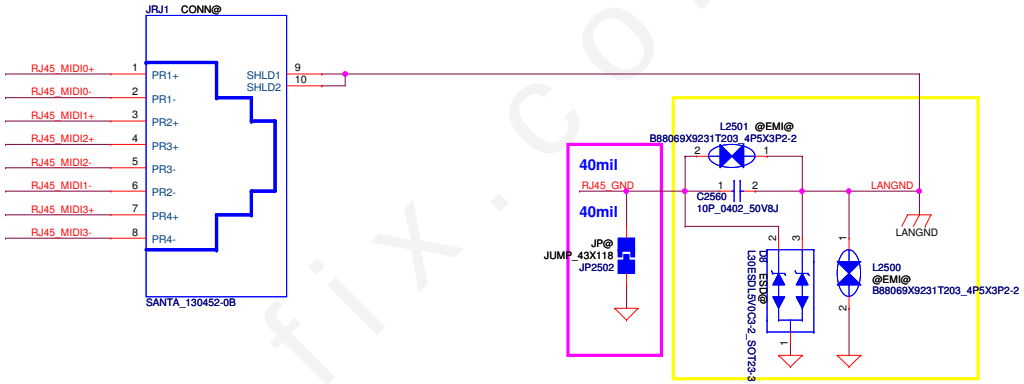
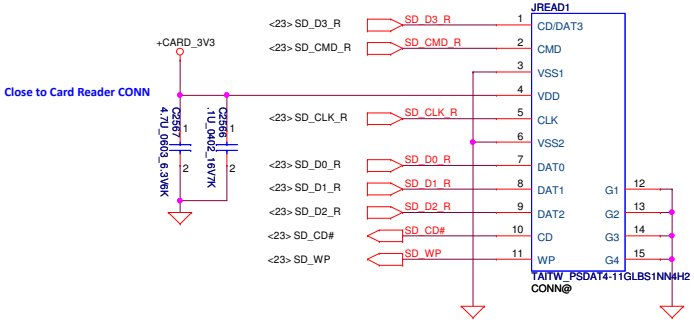
LAN Connector





Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: LAN RJ45/CR SD Connector

Size	Document Number	Rev
Custom	Z5WAE LA-B231P	1.0

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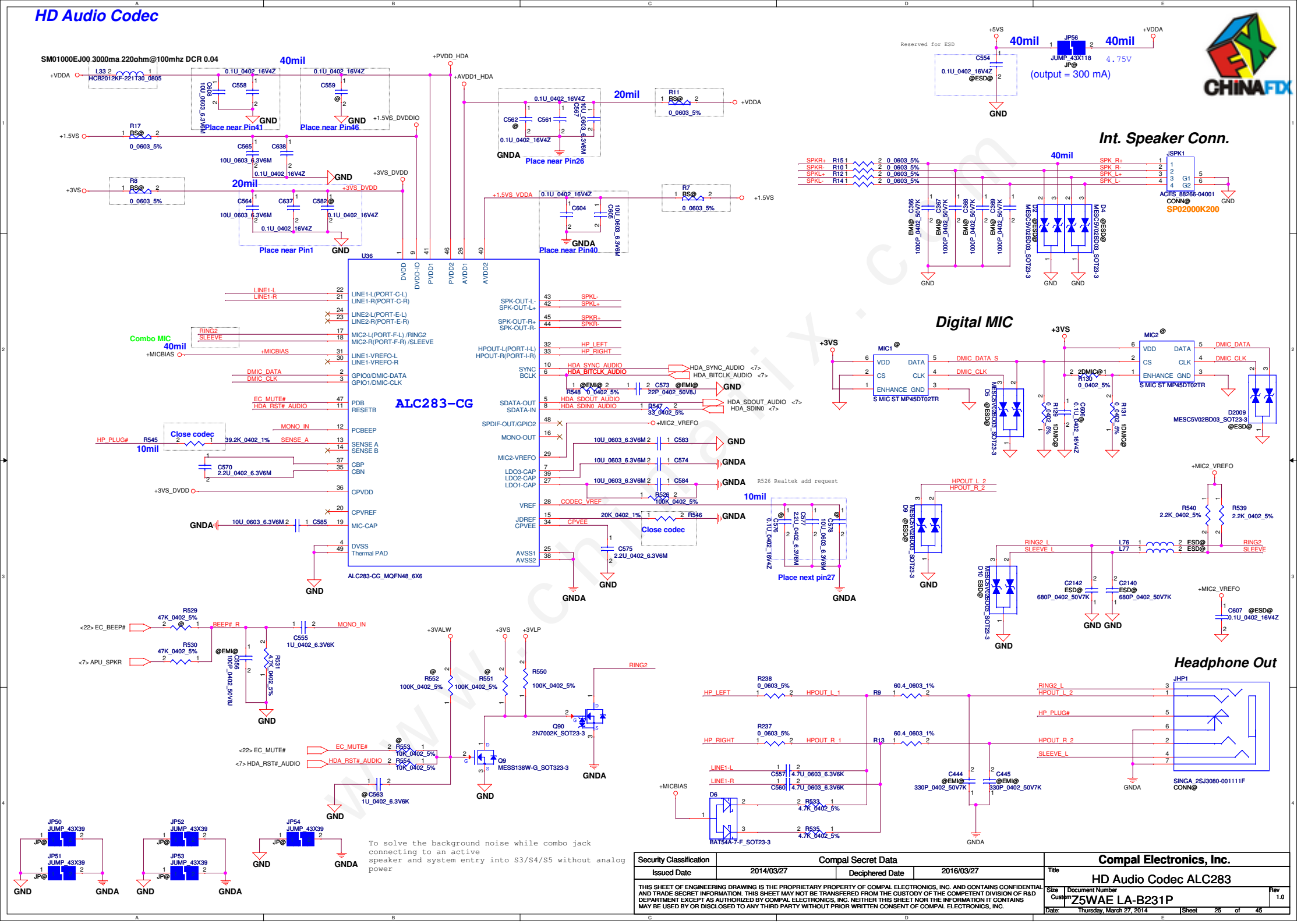
HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: HD Audio Codec ALC283

Size: Custom | Document Number: Z5WAE LA-B231P | Rev: 1.0

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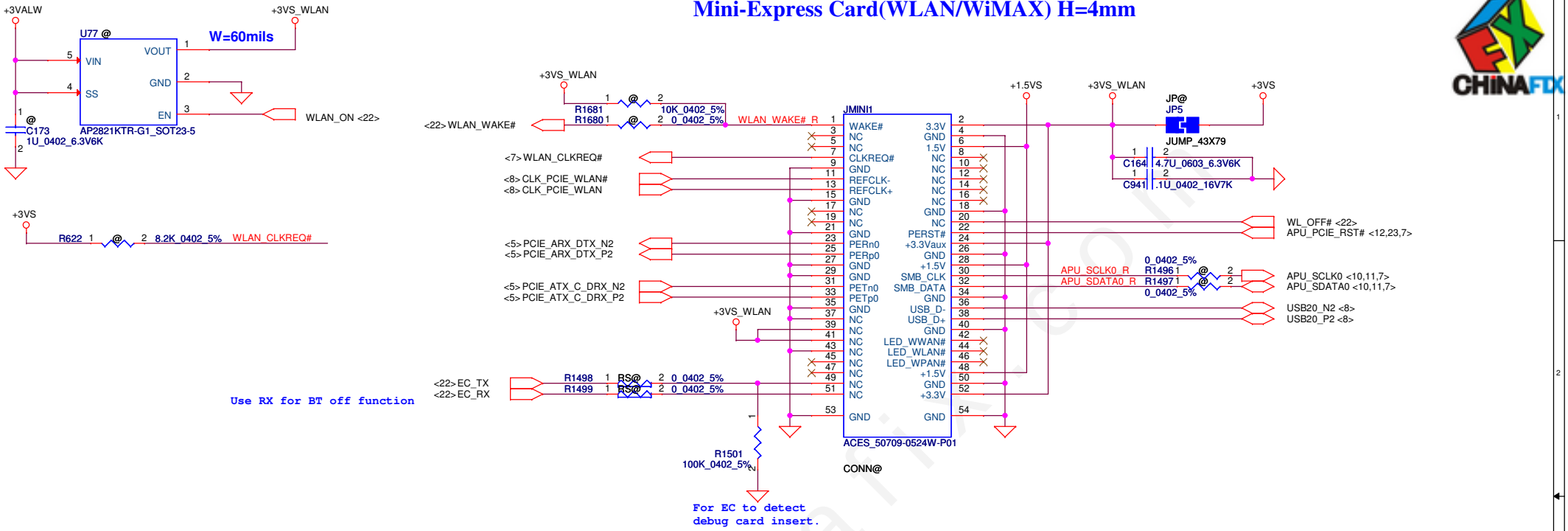
Mini-Express Card(WLAN/WiMAX) H=4mm



H3 H_3P0 H4 H_3P0 H5 H_3P0 H6 H_3P0 H9 H_3P0 H10 H_3P0 H11 H_3P0
H17 H_6P5 H21 H_3P0
H13 H_4P0 H14 H_4P0 H15 H_4P0 H16 H_4P0 H20 H_4P0
H27 H_3P7
H23 H_3P5X3P0N H25 H_3P0N

FD1 FIDUCIAL_C40M80 FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80 FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: MINI CARD (WLAN)/Screw

Size: B | Document Number: Z5WAE LA-B231P | Rev: 1.0

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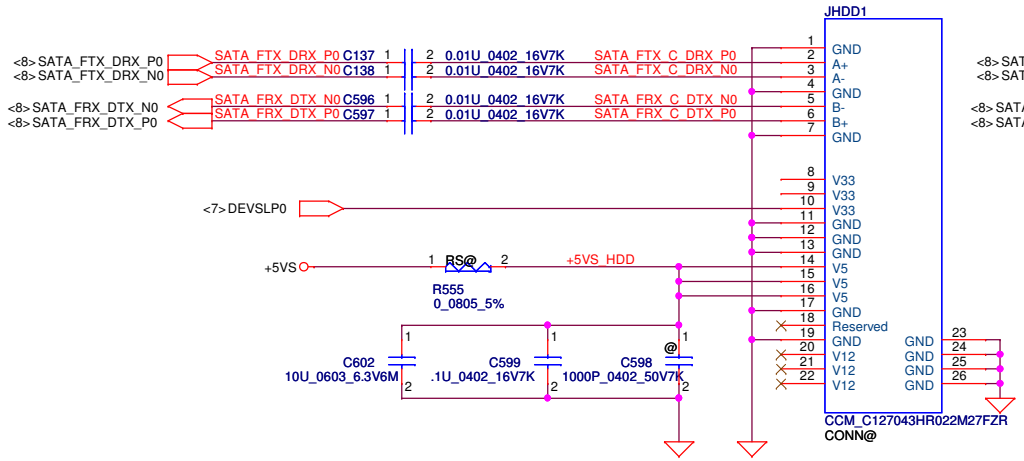
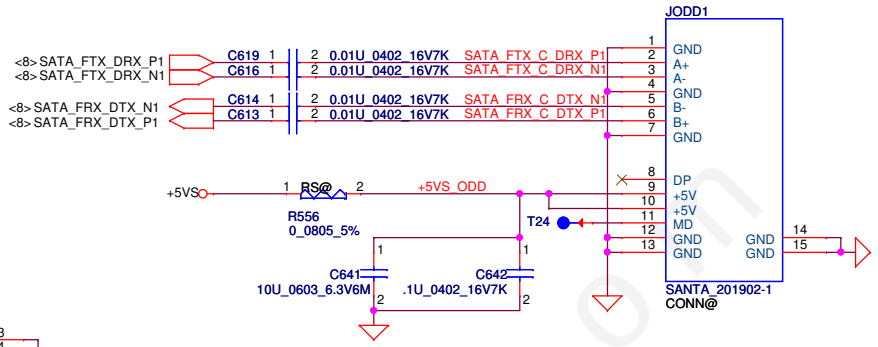
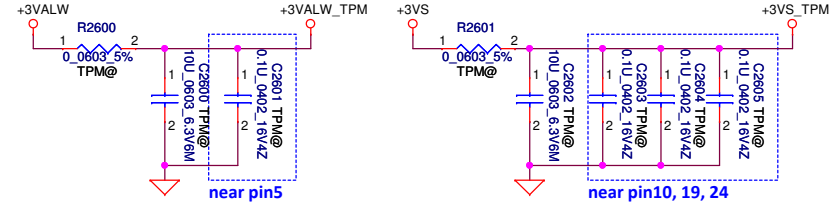
SATA HDD Conn.



SATA ODD Conn.



TPM



BADD	SELECTION
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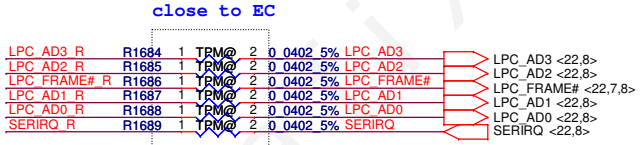
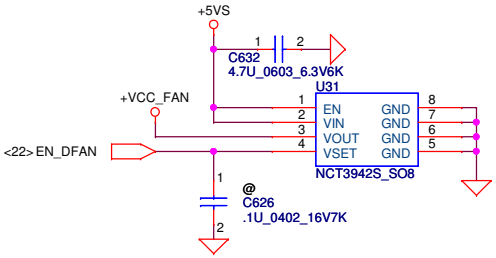
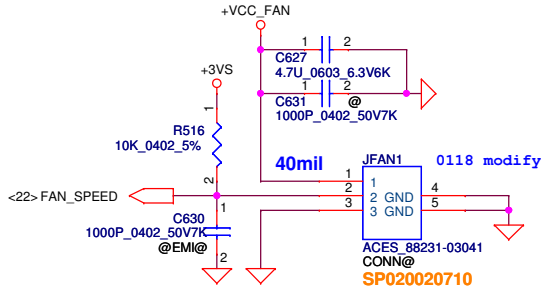
* 1	7Eh - 7Fh

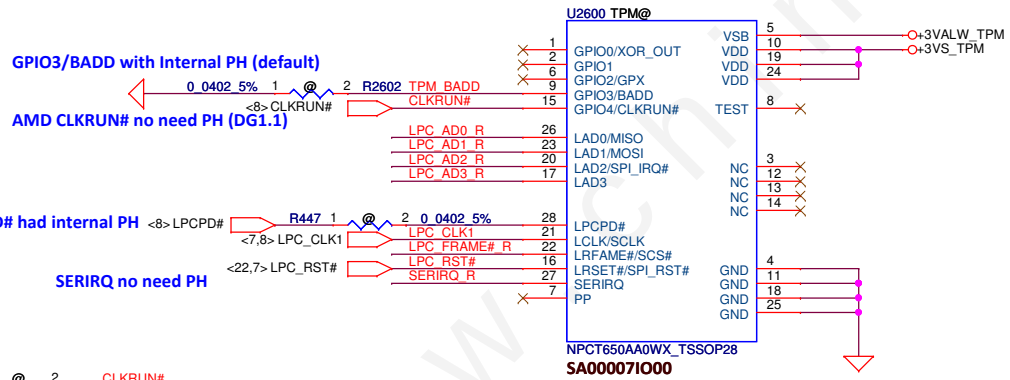
close to EC

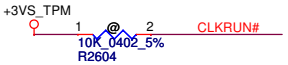


FAN Conn

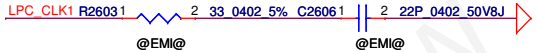








CLKRUN# PH request by TPM chip DG 1/22



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: HDD/ODD/FAN/TPM

Size: B | Document Number: Z5WAE LA-B231P | Rev: 1.0

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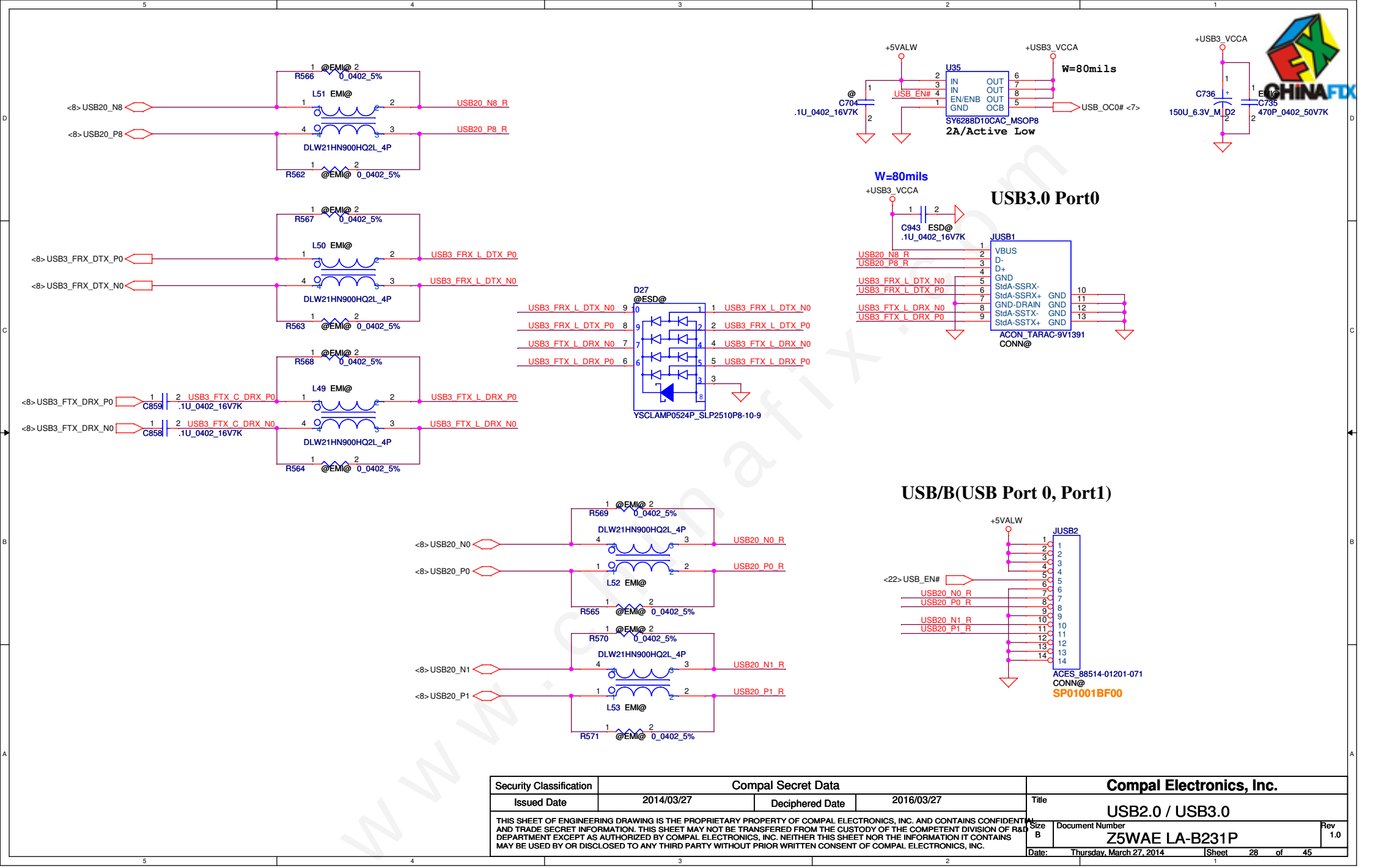

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: USB2.0 / USB3.0

Size	Document Number	Rev
B	Z5WAE LA-B231P	1.0

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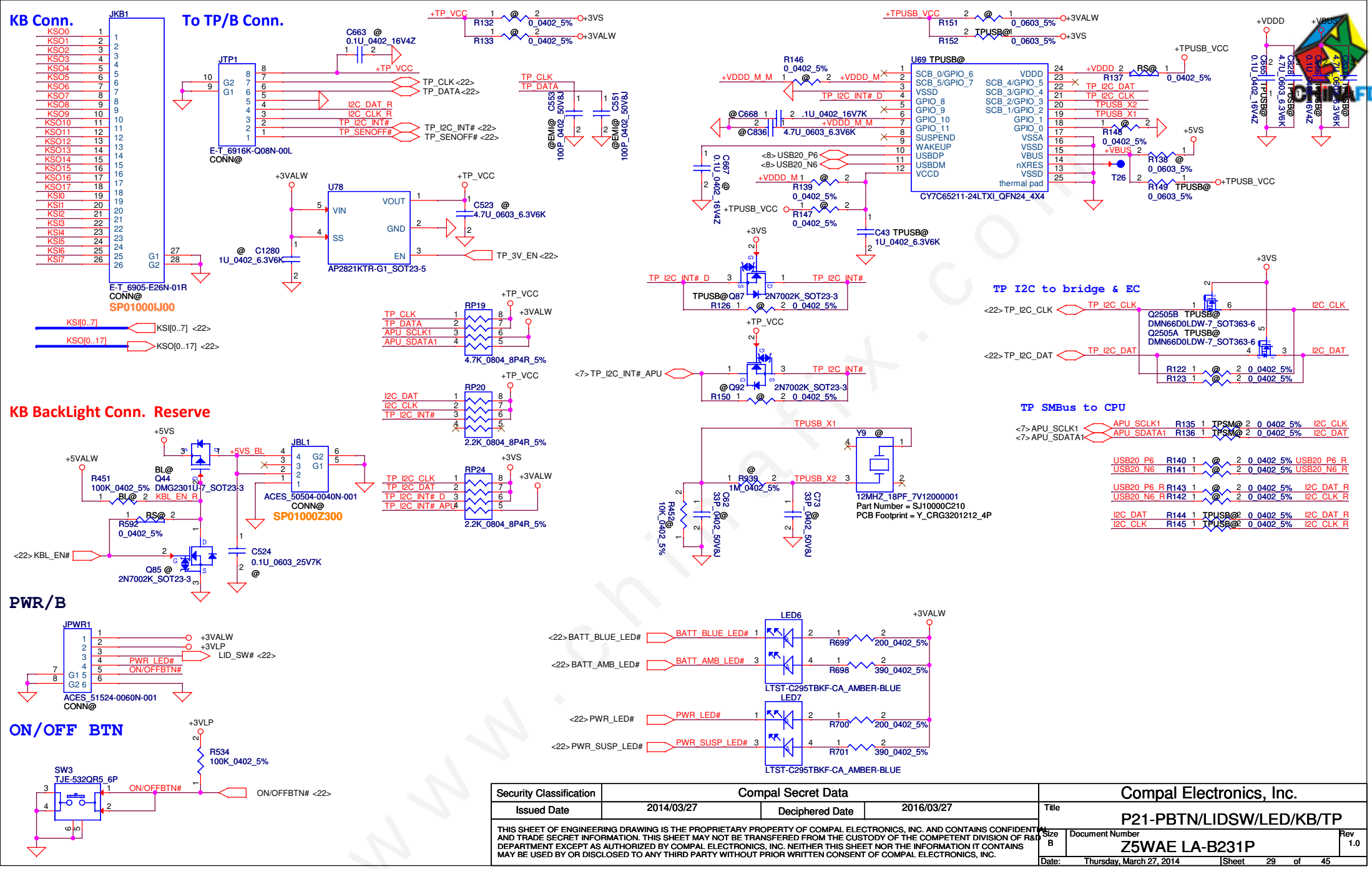

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.			
Title	P21-PBTN/LIDSW/LED/KB/TP		
Size B	Document Number Z5WAE LA-B231P		Rev 1.0
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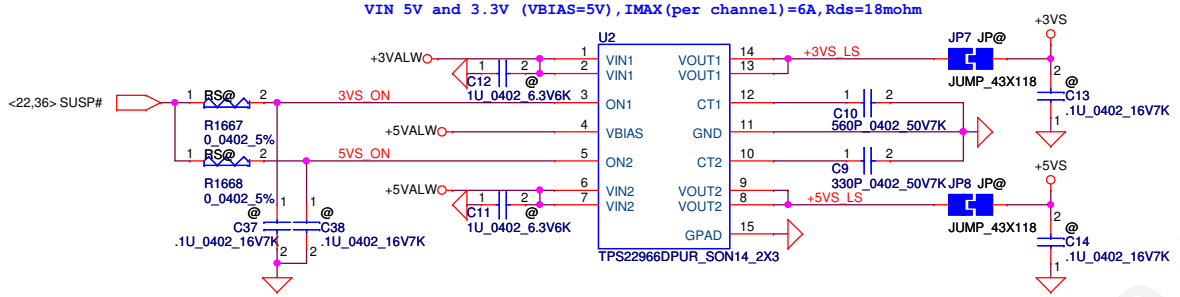
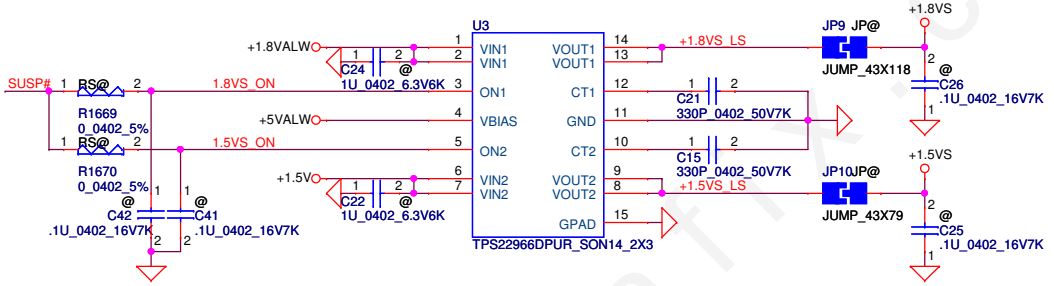
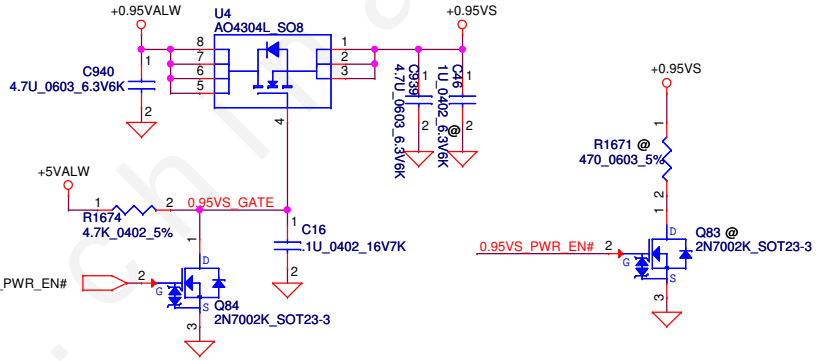
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch



+0.95VALW to +0.95VS



Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: P22-DC INTERFACE

Size	Document Number	Rev
B	Z5WAE LA-B231P	1.0

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0.2

1. Add R693 for UMA/DIS select
2. Change R756,R765,R769,R779,R781,R782,R783 and R794 to Rshort for EMI request
3. Change BID to 1 for DVT
4. Change LAN_WAKE# PU to +3V_LAN
5. Add L76,L77,C2142 and C2140 for ESD request
6. Change R238 and R237 to 59ohm
7. Add L52,L53,R565,R569,R570 and R571 for EMI request.
8. Add R140,R141,R142,R143,R144 and R145 for reserve USB TP
9. Pop Q89, unpop R1690
10. Change D10 to SCA00001B00
11. Change L11 to SM01000EJ00
12. Add U39,R833,C185,R1578 for VGA power sequence issue
13. Remove APU_ALERT#_R
14. Add C668 and C836 for vendor request

0.3

1. Change JTP1
2. Add U78 for TP +3V power plane
3. Change C849, C849 to 10p
4. Change C736 to 150u D2 type.
5. Change R699, R700 to 330ohm; R698, R701 to 560ohm
6. Change U69 +3VALW to +3VS
7. Add C366, C367, C368, C369 for EMI request
8. Add on board TPM
9. Add R619

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/27	Deciphered Date 2016/03/27	Title HW-PIR

Size C	Document Number Z5WAE LA-B231P	Rev 1.0
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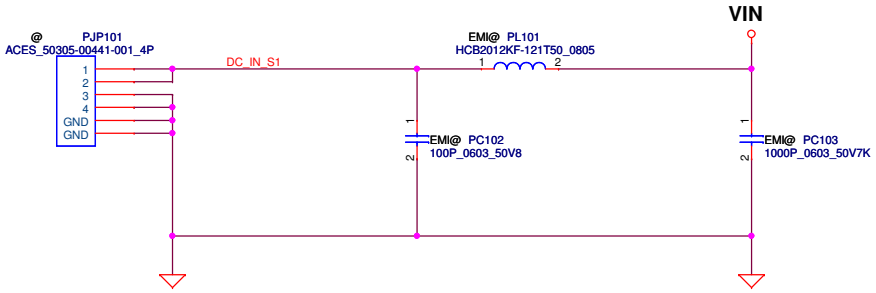

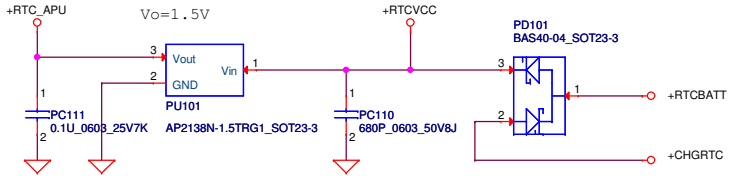

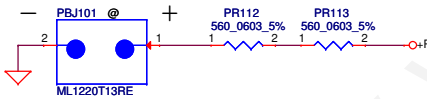

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: *DCIN*

Size	Document Number	Rev
Custom		1.0

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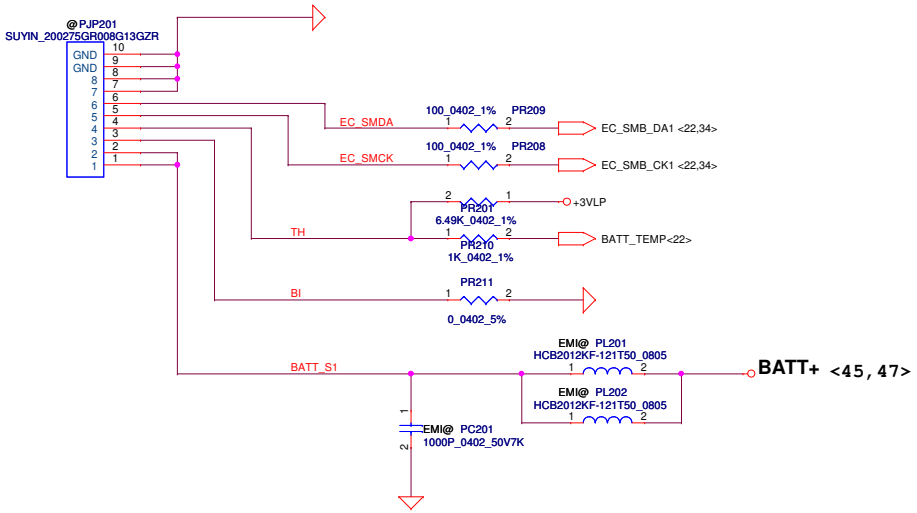
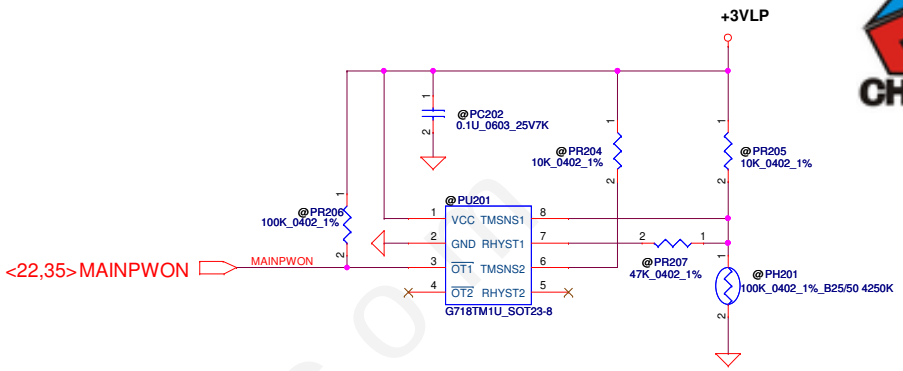





```
---Battery_pin define---      ---Battery Con_pin define---
PIN1 GND                      PIN8 GND
PIN2 GND                      PIN7 GND
PIN3 SMD                      PIN6 SMD
PIN4 SMC                      PIN5 SMC
PIN5 TS                       PIN4 TS
PIN6 B/I                      PIN3 B/I
PIN7 Batt+                    PIN2 Batt+
PIN8 Batt+                    PIN1 Batt+
```

	For KB9012 OTP	For KB9022 OTP
92℃		1.0V
56℃		2.0V
PR216		16.9K ohm

2014/01/02 update

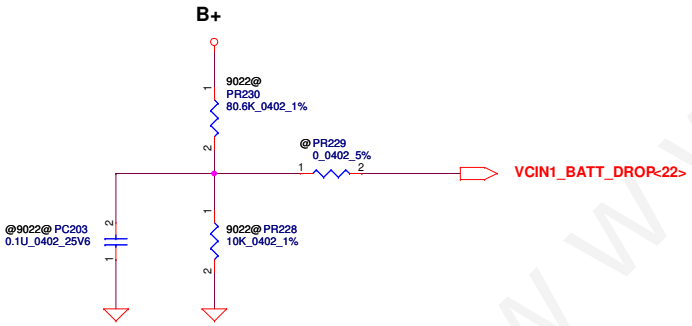
For KB9022 sense 20mΩ	Active	Recovery
65W	70W,0.73V	55.9W,0.59V

2013/10/22 Modify
PH201,PH202 change to common part.

2013/12/16 Modify
Delete PR223.(remove HW hysteresis)

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

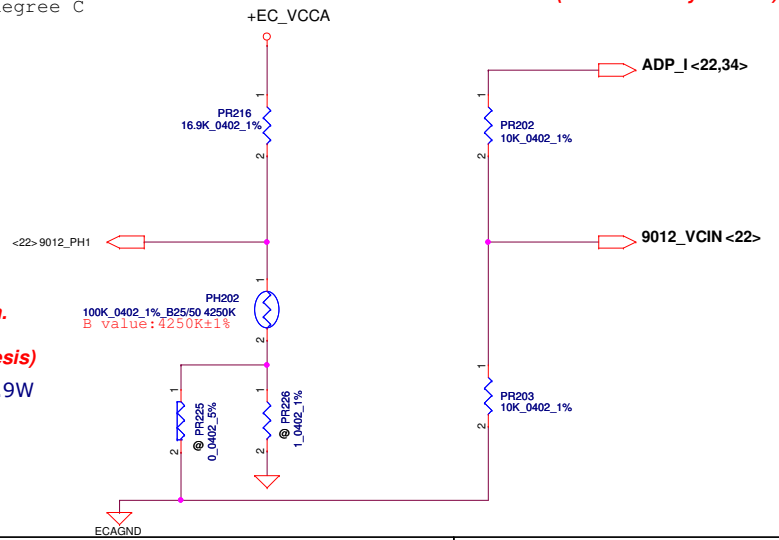
Battery is 3-cell design.
B+=9V



PH201 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

2013/10/25 Modify
PR227(9012@) change to 26.1K ohm.
2014/02/07 Modify
Delete @PR227.(remove HW hysteresis)

For 65W adapter==>action 70W , Recovery 55.9W



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Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size	Document Number	Rev
Custom		1.0

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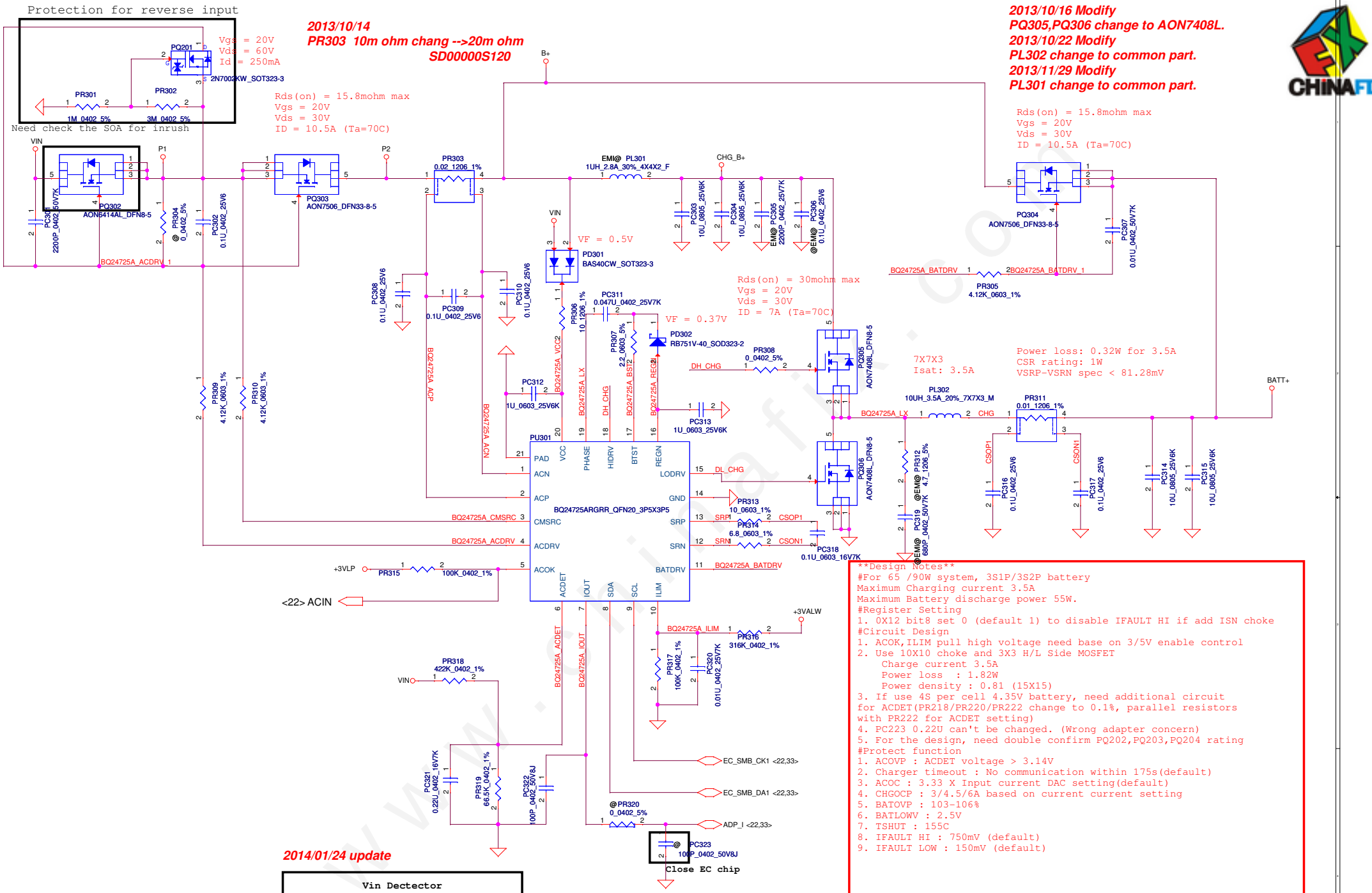


Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

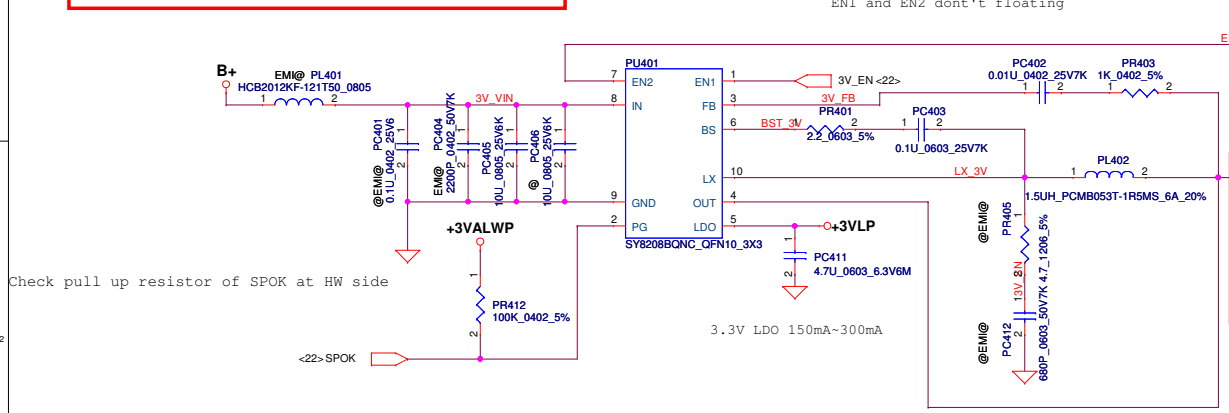
Compal Electronics, Inc.			
Title	CHARGER		
Size	Document Number		Rev 1.0
Date: Thursday, March 27, 2014		Sheet 34 of 45	

Module model information

SY8208B_V2.mdd

SY8208C_V2.mdd

EN1 and EN2 dont't floating



Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

Vout is 3.234V~3.366V

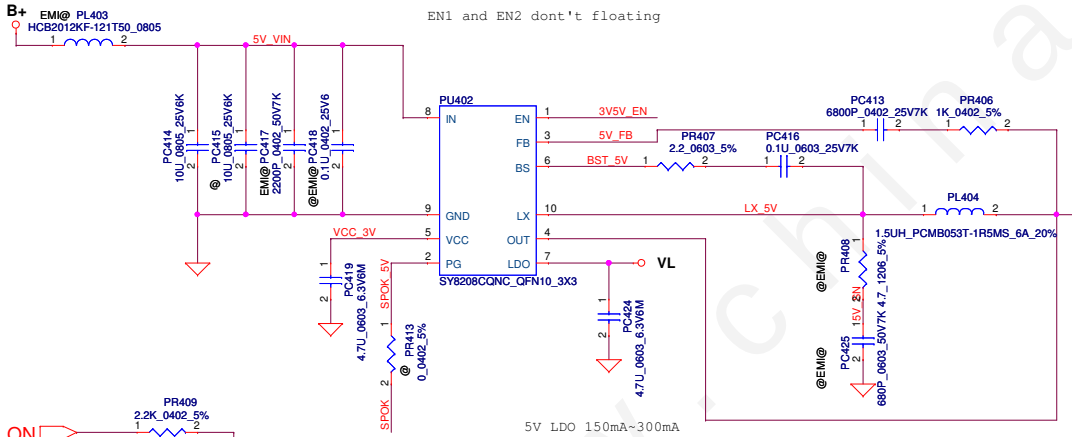
TDC=6A

22u Capacitor change to 0603 size.
2013/10/16 modify.

+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+5VALWP — @PJ402 JUMP_43X118 — +5VALW

EN1 and EN2 dont't floating



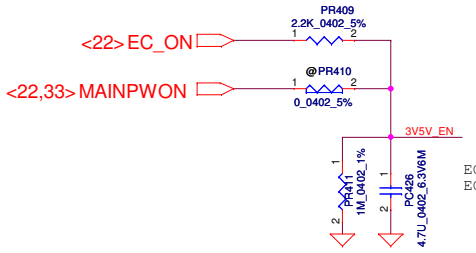
5V LDO 150mA~300mA

Vout is 4.998V~5.202V

TDC=6A

22u Capacitor change to 0603 size.
2013/10/16 modify.
reserve PC427,PC428 for IC Application.
2013/11/29 modify.

Add non-pop PR413 for Test.
2013/11/04 modify.



EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 1.0

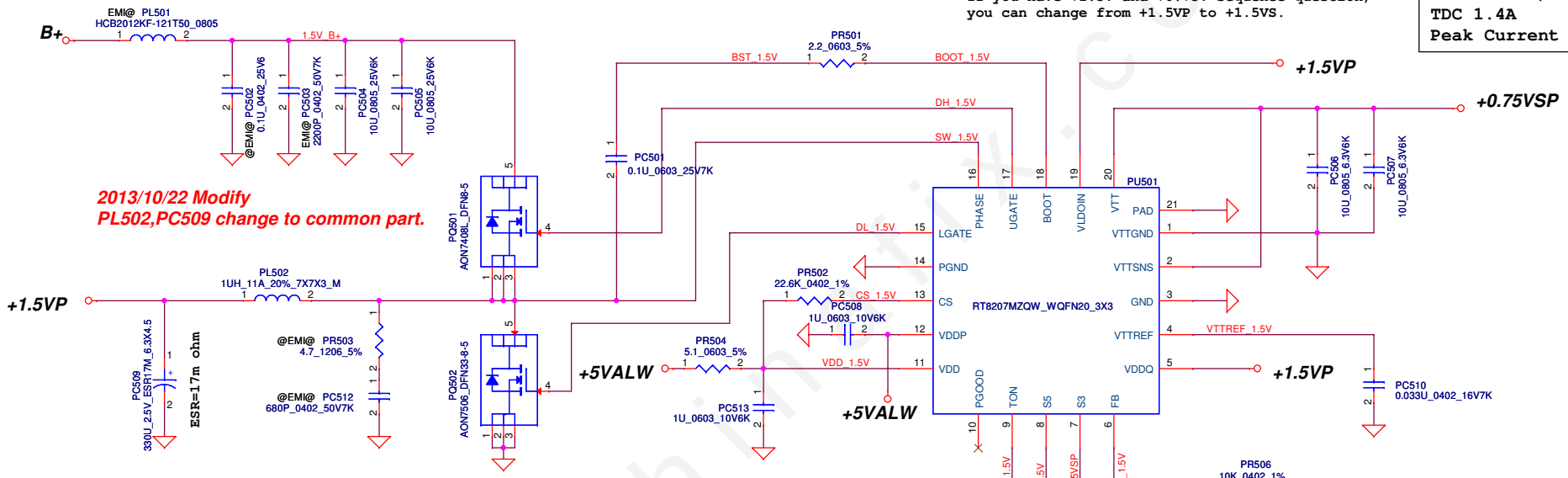
Date: Thursday, March 27, 2014 | Sheet 35 of 45

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 1.4A
Peak Current 2A



2013/10/22 Modify
PL502,PC509 change to common part.

2013/10/14 update
PQ502__AON7702A EOL chang
-->AON7506_SB000010A00

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

for this project
Switching Frequency: 285kHz
Ipeak=11A
OCP:15.939A~13.371A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: +1.5VP/+0.75VSP

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, March 27, 2014 | Sheet 36 of 45

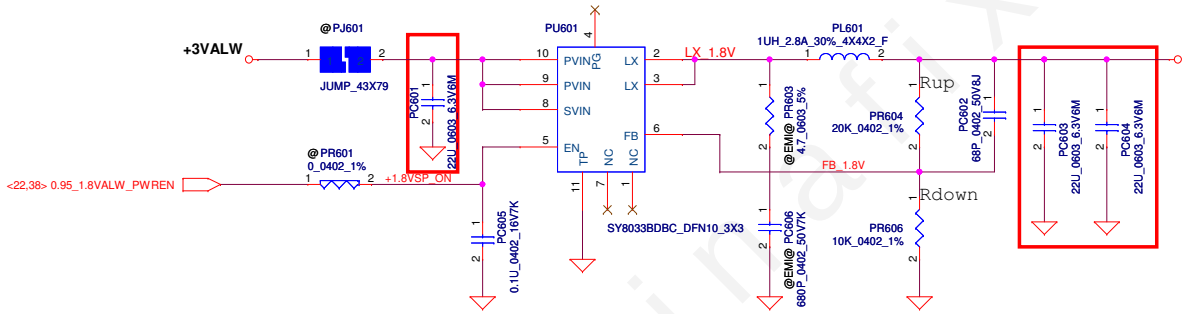
Module model information

SY8033_V1.mdd

22u Capacitor change to 0603 size.
2013/10/16 modify.

2013/10/22 Modify
PL601 change to common part.

FB=0.6V
Note:Iload(max)=3.5A

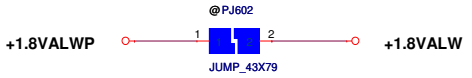


22u Capacitor change to 0603 size.
2013/10/16 modify.

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Delete PR605,because same net name have two PD resister in circuit.
2013/11/29 modify.



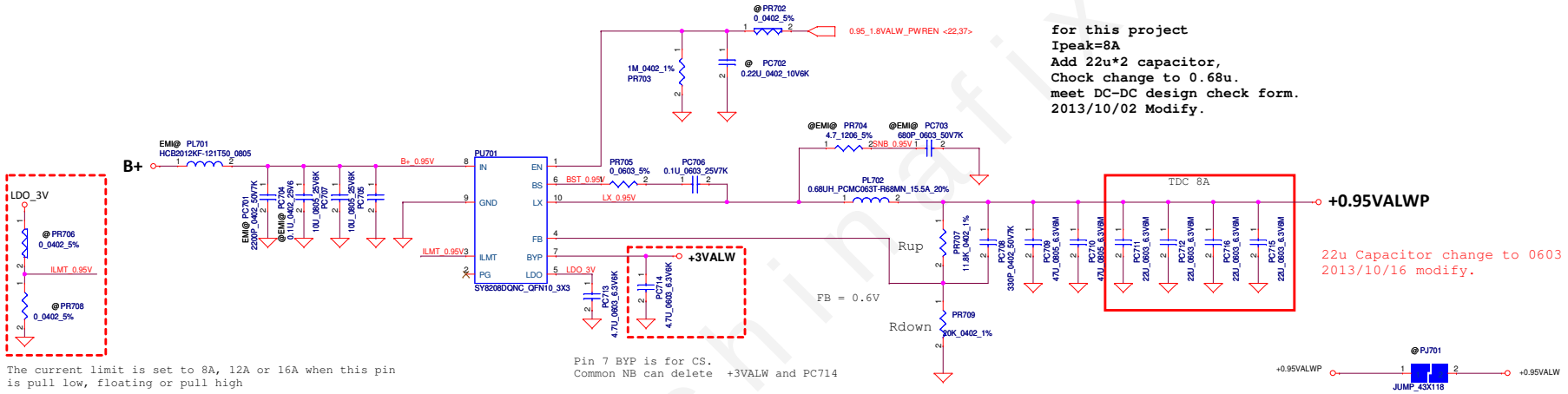
Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.		
Title: *+1.8VALWP*		
Size: Custom	Document Number	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 37 of 45	

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



for this project
Ipeak=8A
Add 22u*2 capacitor,
Chock change to 0.68u.
meet DC-DC design check form.
2013/10/02 Modify.

22u Capacitor change to 0603 size.
2013/10/16 modify.

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC714

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=0.954V

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: +0.95VALWP

Size: C | Document Number | Rev: 1.0

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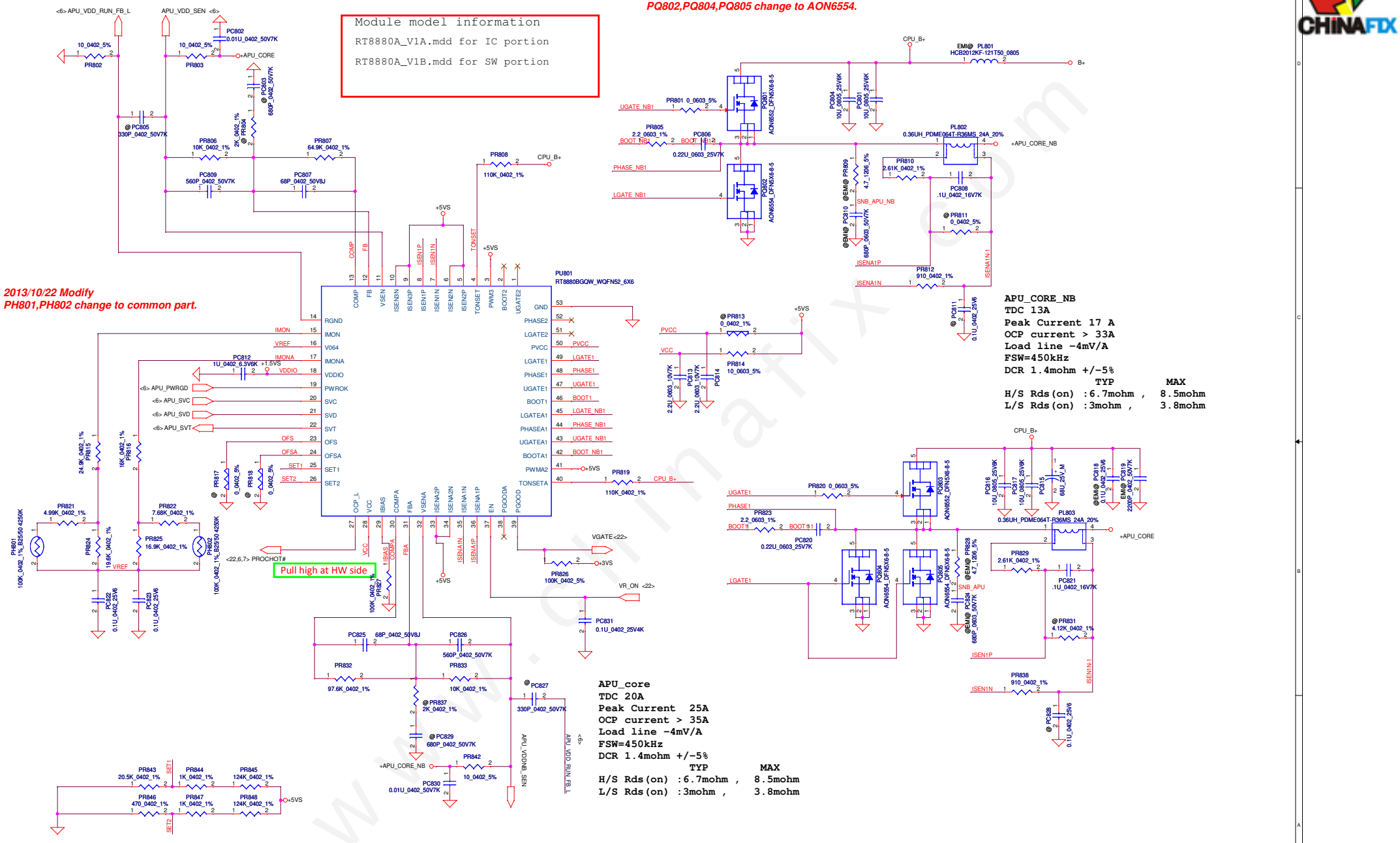

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/27	Deciphered Date 2016/03/27	Title APU_CORE/APU_CORE_NB
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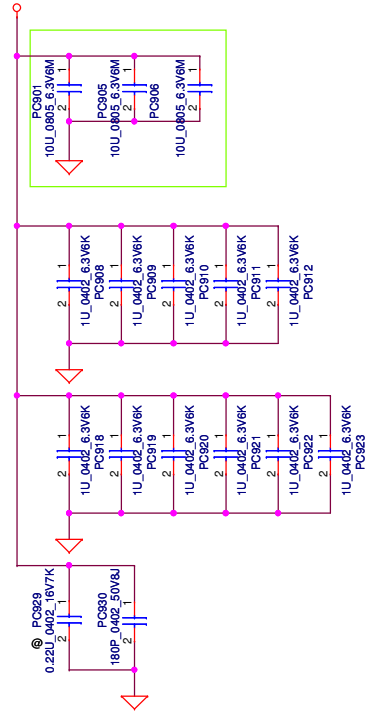
			Date: Thursday, March 27, 2014 Sheet 39 of 45

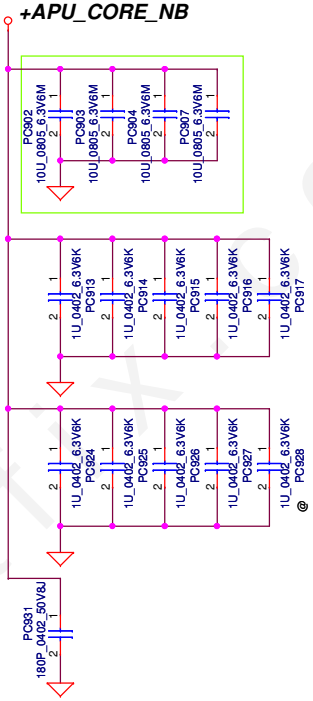
+APU_CORE (36.4)

+APU_CORE_NB (36.5)

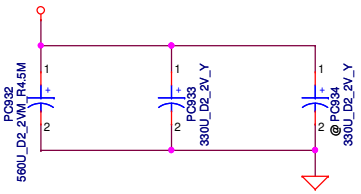
+APU_CORE



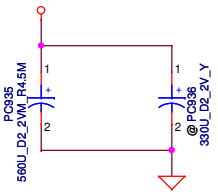
+APU_CORE_NB



+APU_CORE



+APU_CORE_NB



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *APU_CORE/APU_CORE capacitor*

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Custom		1.0

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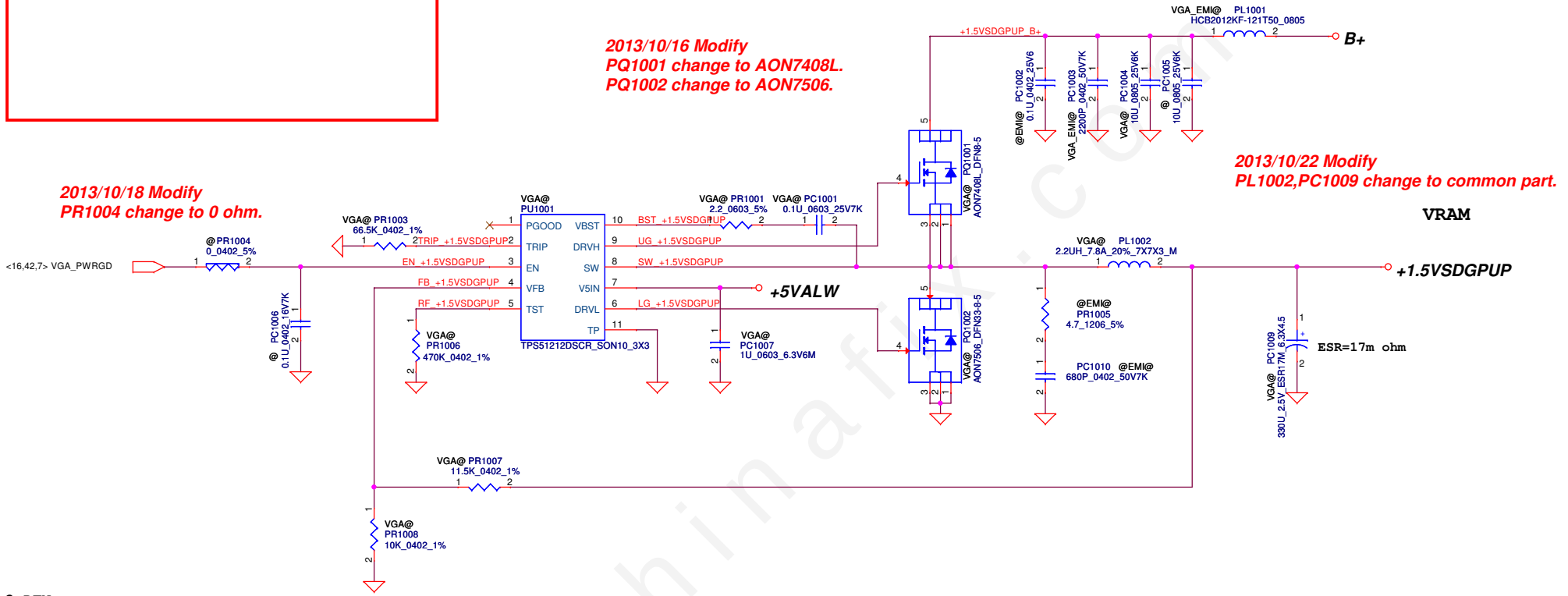
Module model information

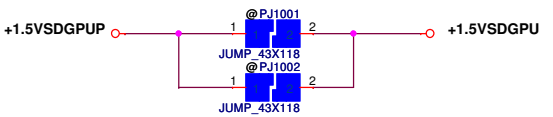
TPS51212_V1.mdd for Single layer
TPS51212_V2.mdd for Dual layer

2013/10/16 Modify
PQ1001 change to AON7408L.
PQ1002 change to AON7506.

2013/10/22 Modify
PL1002,PC1009 change to common part.

2013/10/18 Modify
PR1004 change to 0 ohm.





MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Vout	PR1007	PR1008	PR1003
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k
+1.5V	11.5K	10k	105K

+1.5V(for this project)

Switching Frequency: 290kHz
Ipeak=4.7A
OCP:6.884A~5.751A
OVP: 120%~130%
VFB=0.704V, Vout=1.514V
PR1003=66.5K Ohm

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Issued Date	2014/03/27	Deciphered Date	

Compal Electronics, Inc.

Title: 1.5VSDGPUP

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GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

"Jet Type"

Vboot(merge)

	AMD MARS series (LP: DDR3 Pro/XT/XTX: GDDR5)				AMD SUN series (UL: DDR3 Pro/XT/XTX: GDDR5)			Description
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775~1.175V	0.775~1.125V	0.775~1.050V	0.775~1.000V	0.775~1.125V	0.800~1.075V	0.800~1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	----------	----------	----------	1mohm	NA
Ri PR1248	1.13K Ohm	887 Ohm	750 Ohm	----------	----------	----------	887 Ohm	for OCP and LoadLine Setting
Rdroop PR1229	1.43K Ohm	1.13K Ohm	953 Ohm	----------	----------	----------	1.13K Ohm	for LoadLine Setting
PR1233	187K Ohm	147K Ohm	124K Ohm	----------	----------	----------	147K Ohm	for Compensation
PR1236	51.1K Ohm	51.1K Ohm	51.1K Ohm	----------	----------	----------	51.1K Ohm	for Positive offset

Remark: MARS LP/ SUN UL/ SUN PRO don't use this 2-phase solution

MOS

	TYP	MAX
H/S Rds(on)	6.7mohm	8.5mohm
L/S Rds(on)	3mohm	3.8mohm

Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

2013/10/16 Modify
PQ1201,PQ1203 change to AON6552.
PQ1202,PQ1204 change to AON6554.

Remark:

1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
   => 2 phase CPU VR config
   PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
   => 2 phase GPU VR config

2. When 2 Phase GPU config
   a. DPSLPVR (Pin39)=0 PSI# (Pin2)=0
      =>1 phase CCM operation mode
   b. DPSLPVR (Pin39)=0 PSI# (Pin2)=1
      =>2 phase CCM operation mode
   c. DPSLPVR (Pin39)=1 PSI# (Pin2)=0 or 1
      =>1 phase DE operation mode

3. Rbias=147K =>overshoot reduction function disable
   Rbias=47K =>overshoot reduction function enable

4. Thermal throttling:
   Protect: (6.98K+Rth)*60uA=1.2V
   => Rth=13.02K
   =>Tp=110C (+-3C) <13> GPU_DPRSLPVR
   Recovery:(6.98K+Rth)*56uA=1.24V
   => Rth=15.16K
   => Tr=105C (+-3C)

PR1226=6.98K	PR1226=1.5K
protect T 110C +-3	protect T 100C +-3
Recovery T 105C +-3	Recovery T 96C +-3

5. Switching frequency set :
   Rfset(kohm)=[period(us)-0.29]*2.65
   =5.9Kohm
   fsw=1/period(us)=400KHZ

2013/10/18 Modify
EN Signal change to VGA_ON.
Delay Time follow HW request.

2013/11/29 Modify
Delay Time follow HW request.
Add PD Resister(PR1250)
2013/12/16 Modify
Delay Time follow HW request.

Vboot regulation

Module model information:
ISL62883C_V1A for IC
ISL62883C_V1B for SW Choke/MOS on BTN
ISL62883C_V2B for SW Choke on BTN, MOS on TOP

2013/11/29 Modify
PL1202.PL1203 change to common part.

TDC 28A
Peak Current = 42A
OCP Current = 48.6A
Load line=mohm

PR1230 Pop:
for Loadline disable
PR1230 @:
for Loadline enable
and LL=1mohm

Transient response :
Rntcnet=(Rntcs+Rntc)*Rp/(Rntcs+Rntc+Rp)
Cn=L*(Rntcnet+Rsum/N)/[Rntcnet*DCR*(Rsum/N)]
N is the number of phases

Rdroop=Io*LL/Idroop

2013/10/22 Modify
PH1201,PH1202 change to common part.

2013/10/25 Modify
PR1229 change to 1.24K ohm.
PR1248 change to 976 ohm.

Layout Note:
PH1201 should place near phase1 H-side MOS

Layout Note:
PH1202 should place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: ISL62883C

Size: | Document Number: | Rev: 1.0

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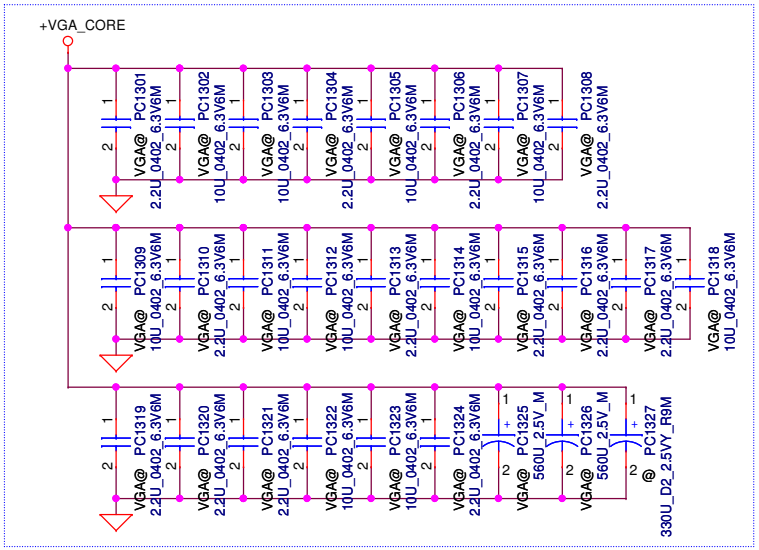
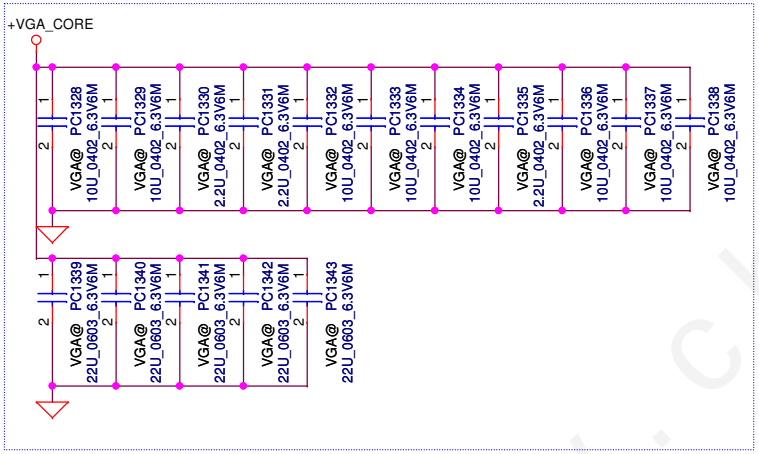


AMD MARS
GPU_CORE
560uF*2+330uF*1
10uF*8+2.2uF*16



AMD MARS
meet ripple
22uF*5+10uF*11

Security Classification	Compal Secret Data		
Issued Date	2014/03/27	Deciphered Date	2016/03/27

Compal Electronics, Inc.

Title: *VGA_CORE CAP*

Size	Document Number	Rev
Custom		1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of Diode Application.	0.2	32	Change PD101 to SCSS4004010(S SCH DIO BAS40-04 SOT23).	2013/11/29	DVT
2	Design Change.	Design Change of IC Application.	0.2	35	Add non-pop component PC427,PC428.	2013/11/29	DVT
3	Design Change.	reduce part count.	0.2	37	Delete PR605 PD resister.	2013/11/29	DVT
4	Design Change.	reduce part count.	0.2	39	Delete @PR834.@PR835.@PR836.@PR839.@PR840.@PR841.	2013/11/29	DVT
5	Design Change.	Design Change of VGA Type Application.	0.2	42	PR1205 change to non-pop. PR1211 change to pop.	2013/11/29	DVT
6	Design Change.	Design Change of common part.	0.2	34	Change PL301 to SH00000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE).	2013/11/29	DVT
7	Design Change.	Design Change of common part.	0.2	42	Change PL1202.PL1203 to SH000011H00 (S COIL .22UH +-20% 24A 7X7X4 MOLDING).	2013/11/29	DVT
8	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to non-pop.	2013/11/29	DVT
9	Design Change.	Design Change of EC Type Application.	0.2	35	Add PD401 SCS00000Z00(S SCH DIO RB751V-40 SOD-323).	2013/11/29	DVT
10	Design Change.	Design Change of Circuit Application.	0.2	42	Add PR1250 SD034100480(S RES 1/16W 1M +-1% 0402).	2013/11/29	DVT
11	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to SE071330J80(S CER CAP 33P 50V J NPO 0402)	2013/12/16	DVT
12	Design Change.	Design Change of Circuit Application.	0.2	33	Delete PR223.(remove HW hysteresis)	2013/12/16	DVT
13	Design Change.	Design Change of Circuit Application.	0.2	42	Change PR1250 to non-pop.	2013/12/16	DVT
14	Design Change.	Design Change of Circuit Application.	0.2	34	Change PQ303,PQ304 to SB000010A00(S TR AON7506 1N DFN).	2013/12/19	DVT
15	Design Change.	Design Change of Circuit Application.	0.2	33	Add PL202 SM01000C000 (S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2013/12/19	DVT

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16	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR211 to SD028000080(S RES 1/16W 0 +-5% 0402).	2013/12/25	DVT
17	Design Change.	Design Change of Circuit Application.	0.2	35	Change PC426 to pop.	2013/12/25	DVT
18	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034162280(S RES 1/16W 16.2K +1% 0402).	2013/12/25	DVT
19	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034169280(S RES 1/16W 16.9K +-1% 0402).	2014/01/02	DVT
20	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR202 to SD034100280(S RES 1/16W 10K +-1% 0402).	2014/01/02	DVT
21	Design Change.	Design Change of Circuit Application.	0.3	37.38. 39.41.	Change PR813,PR601,PR706,PR702,PR1004 to SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT
22	Design Change.	Design Change of Circuit Application.	0.3	35	Remove PD401. Add @PR410 SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT

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