Compal Confidential

P5WS5 Schematics Document

AMD Sabine

APU Llano / Hudson M3 / Vancouver Whistler_Seymour

DIS only / UMA only / PX Muxless with BACO

2011-04-20

LA-6973P REV: 1.0

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Compal Electronics, Inc.		
Title: Cover Page		
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Compal Confidential

Model Name : P5WS5

ZZZ1
PCB
Part Number = DAZ0JU00100
PCB P5WS5 LA-6973P LS-6902P/6905P/6973P

ZZZ2
46@
HDMI+HDCP LOGO
RO0000003HM

Sabine

VRAM 512M/1G/2G
64M16/128M16 x 8
page 18, 19

DDR3

ATI Vancuver Whistler/ Seymour
Mahattan Granville
uFCBGA-962
Page 13~17

GFX x 16 Gen2

Thermal Sensor
ADM1032
page 14

VGA HDMI
VGA LVDS(eDP)
VGA CRT

GFX x 4 (Group 1~4)
APU HDMI
(UMA / Muxless)
DP x1 (DP0 TXP/N0)

AMD FS1 APU
Llano
uPGA-722 Package
Page 6~10

Memory BUS(DDR3)
Dual Channel
1.5V DDRIII 800~1600MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
Page 11,12

HDMI Conn.
page 23

LVDS Conn.
Reserve eDP
page 22

LVDS
UAM eDP

Travis LVDS
Translator
page 21

DP x2
(DP0 TXP/N 0~1)

CRT Conn.
page 24

FCH CRT (VGA DAC)

P_GPP x 3
GEN2

DP x 4
(DP1 TXP/N 0~4)

UMI

FCH
Hudson-M2/M3
uFCBGA-656
Page 25~29

USB20 M/B*1
page 34

USB20/B *2
page 35

USB30/B *1
page 35

CMOS Camera
page 22

Bluetooth Conn.
page 35

Mini Card 1
page 33

Mini Card 2
page 33

USB
3.3V 48MHz

Port 0
Port 1
Port 2
Port 3
Port5
FSD0
Port 8
Port 9
Port 6
Port 7

HD Audio 3.3V 24.576MHz/48Mhz

S-ATA Gen2

3G/B *2
page 35

GPP1
MINI Card 1
WLAN
page 33

GPP0
LAN(GbE)
BCM57785
page 31

RJ45
page 32

GPP x 2
GEN2

LPC BUS

port 0
SATA HDD1
Conn.
page 30

port 1
SATA HDD2
Conn.
page

port 2
ODD
Conn.
page 30

HDA Codec
ALC271X
page 38

ENE KB930
page 36

LED
page 37

RTC CKT.
page 25

Power On/Off CKT.
page 37

Fan Control
page 30

DC/DC
Interface CKT.
page 39

Power Circuit
page 40~48

USB30
On SUB/B
page 35

USB30
On M/B
page 34

Touch Pad
page 37

Int.KBD
page 37

EC I/O Buffer

External board

LID SW - Power/B
page 37

USB20/B
-USB20 x2
page 35

USB30/B
-USB20 x1+ USB30 x1
page 35

BIOS ROM

SYS BIOS (2M)
page 27

EC BIOS (128K)
page 37

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Title: Block Diagrams

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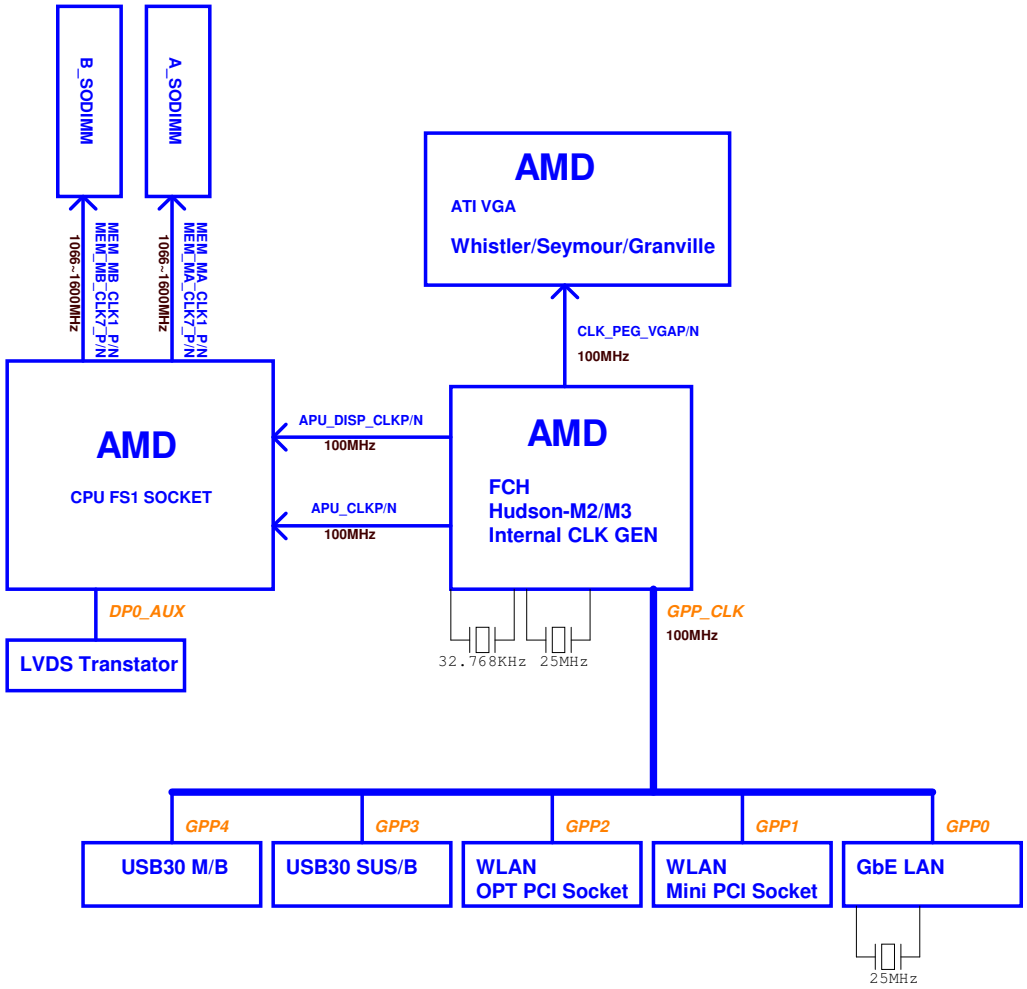
CLOCK DISTRIBUTION



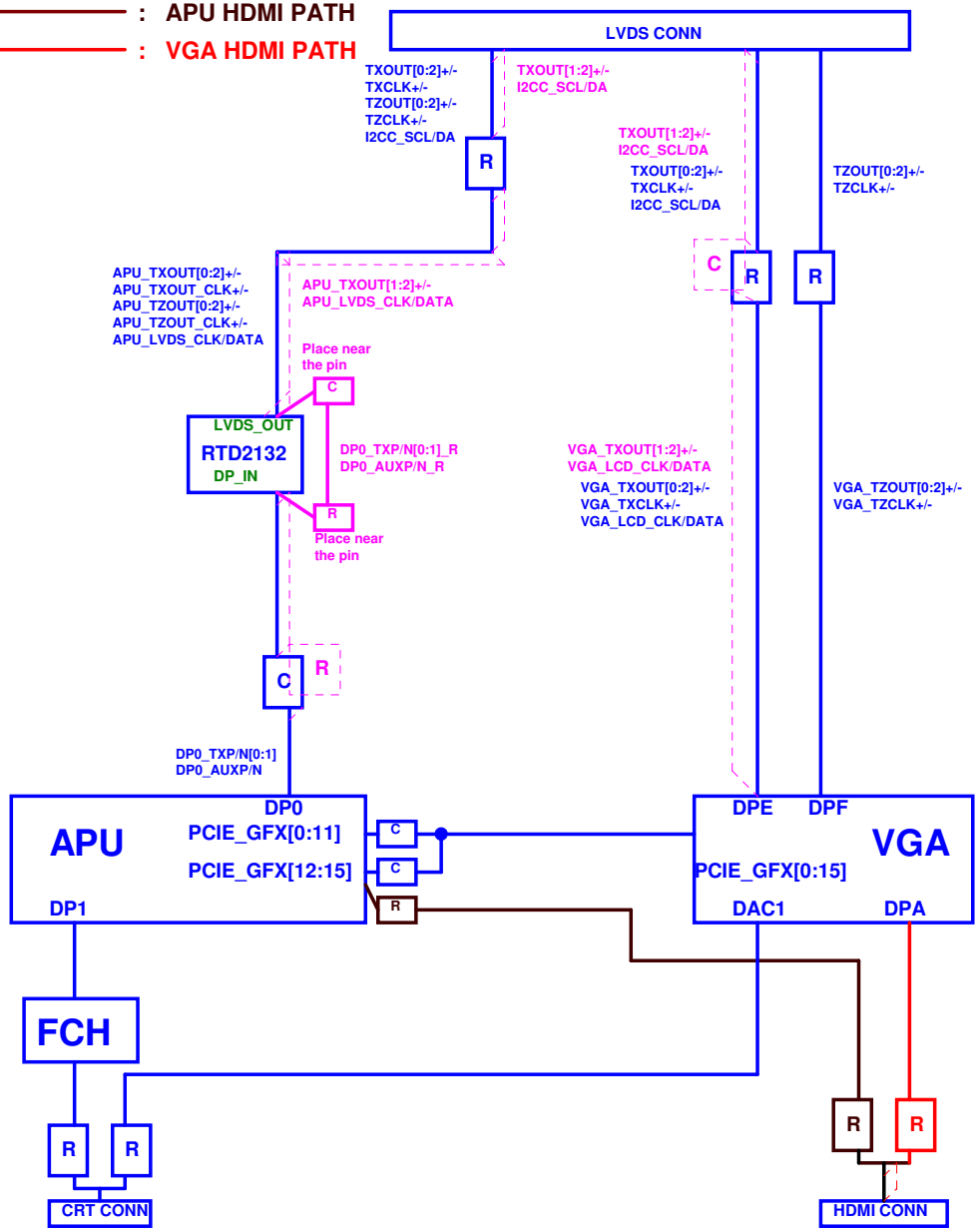
DISPLAY DISTRIBUTION

: LVDS PATH

: eDP PATH

: APU HDMI PATH

: VGA HDMI PATH



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Title	CLOCK / DISPLAY DISTRIBUTION		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	NA
1	P5WS5
2	P5WH5
3	P7YE5
4	P7YS5
5	NA
6	NA
7	NA

BTO Option Table

BOM Structure	BTO Item
UMA@	Display output from APU (UMA only or Mux)
UMAO@	UMA only
APULVDS@	APU output LVDS (UMA only or Mux)
TL@	Translator (UMA only or Mux)
APUEDP@	APU output eDP
VGA@	Use VGA (Mux or DIS only)
DISO@	Display output from VGA (DIS only)
VAN@	Use Vancouver VGA
MAN@	Use Manhattan VGA
GRAN@	Use Granville VGA
SEYM@ WHIS@	VGA P/N
PX@ WOPX@	With & Without PX function
BACO@	BACO function (Mux)
WOBACO@	Without BACO function (Mux)
VGALVDS@	VGA output LVDS (DIS only)
VGAEDP@	VGA output eDP (DIS only)
128@	Use VRAM channel A&B
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
EDP@	Use eDP display (Shared components)
USB30@	USB30 on M/B
USB20@	USB20 on M/B
3G@	With 3G function
930@	Use EC 930
9012@	Use EC 9012
ZERO@	ZERO Power ODD function
HDT@	HDT debug port

WHIS@ U8
VGA
Part Number = SA00004C720

M3@ U25
FCH M3 A13
Part Number = SA000043IB0

M2@ U25
FCH M2 A13
Part Number = SA000042C60

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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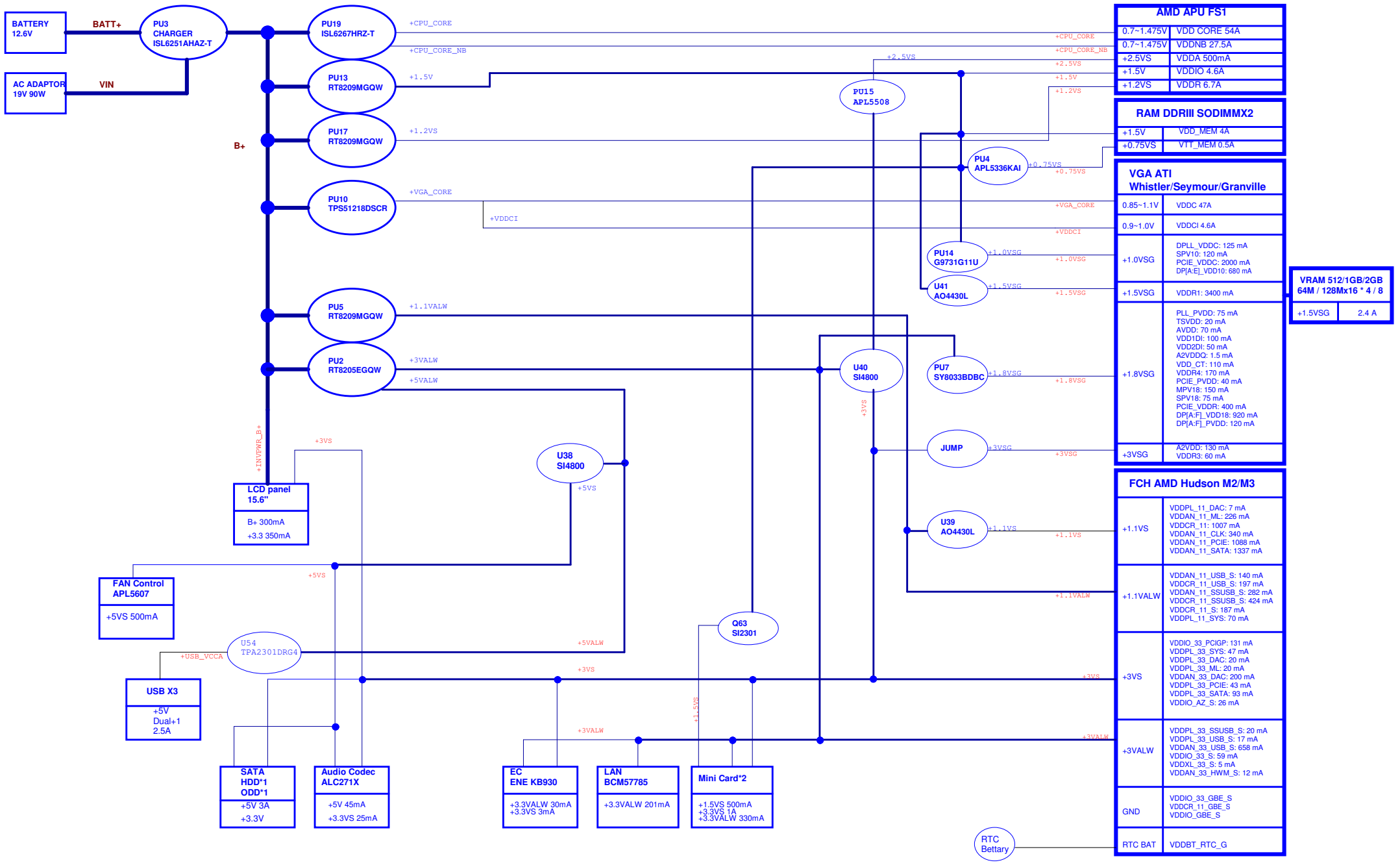

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Title: POWER DELIVERY CHART

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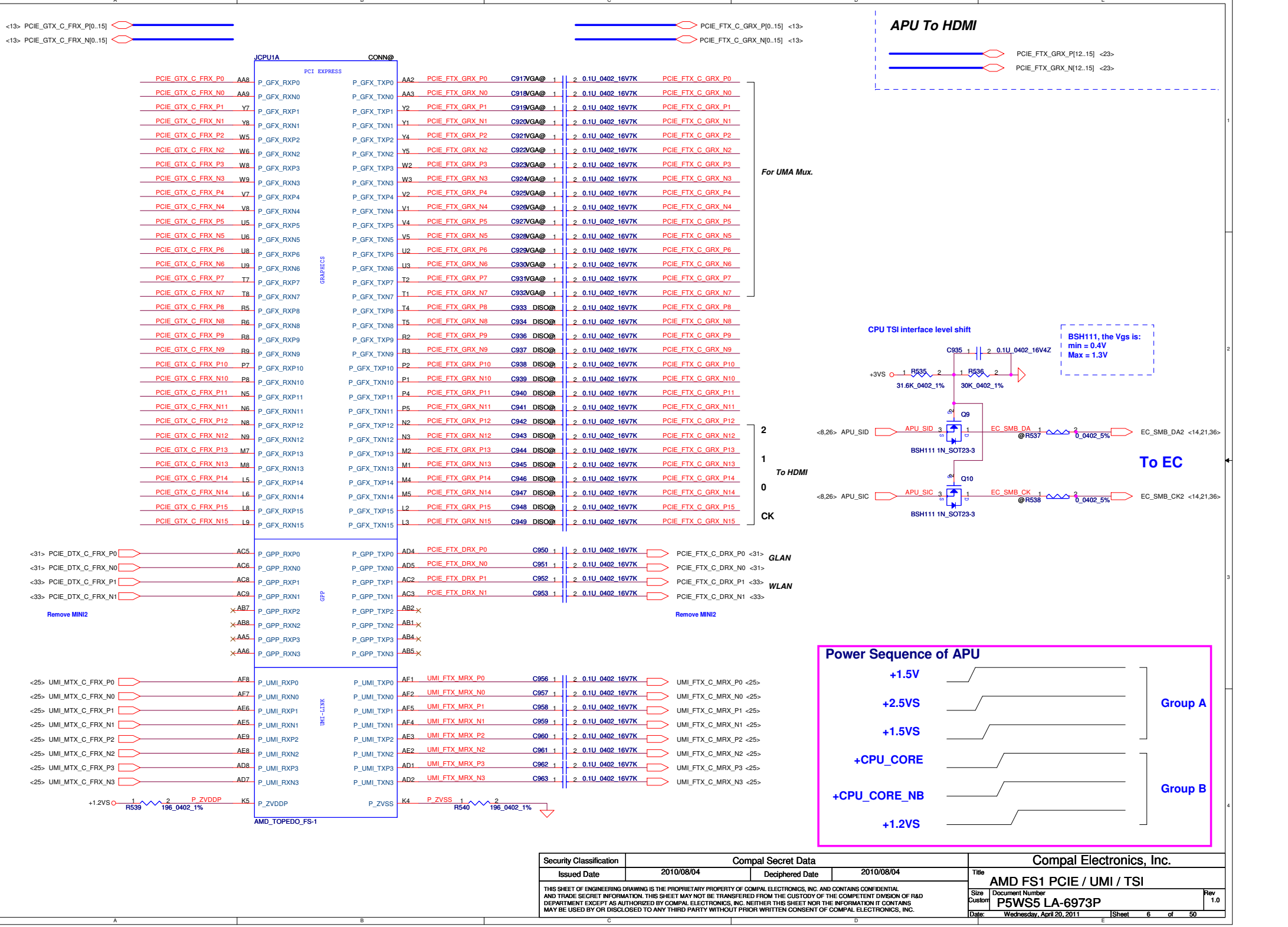

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Compal Electronics, Inc.

Title: AMD FS1 PCIE / UMI / TSI

Size	Document Number	Rev
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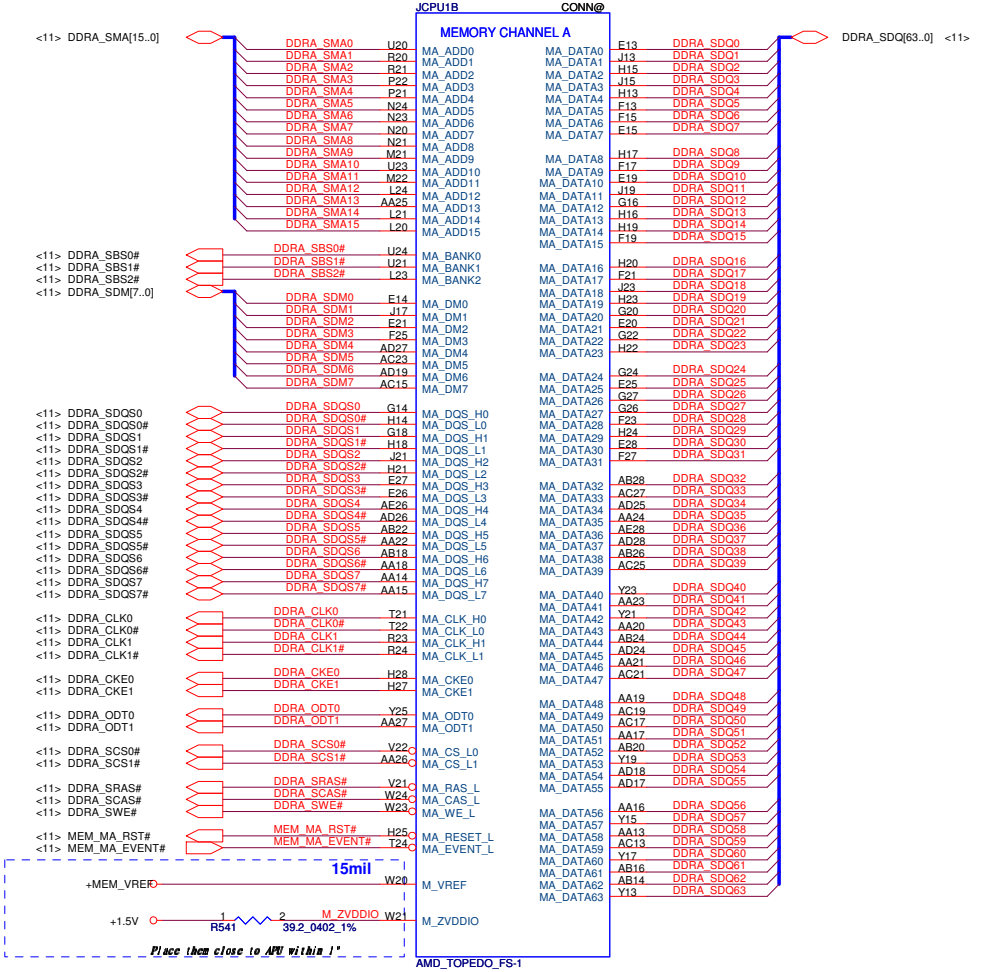
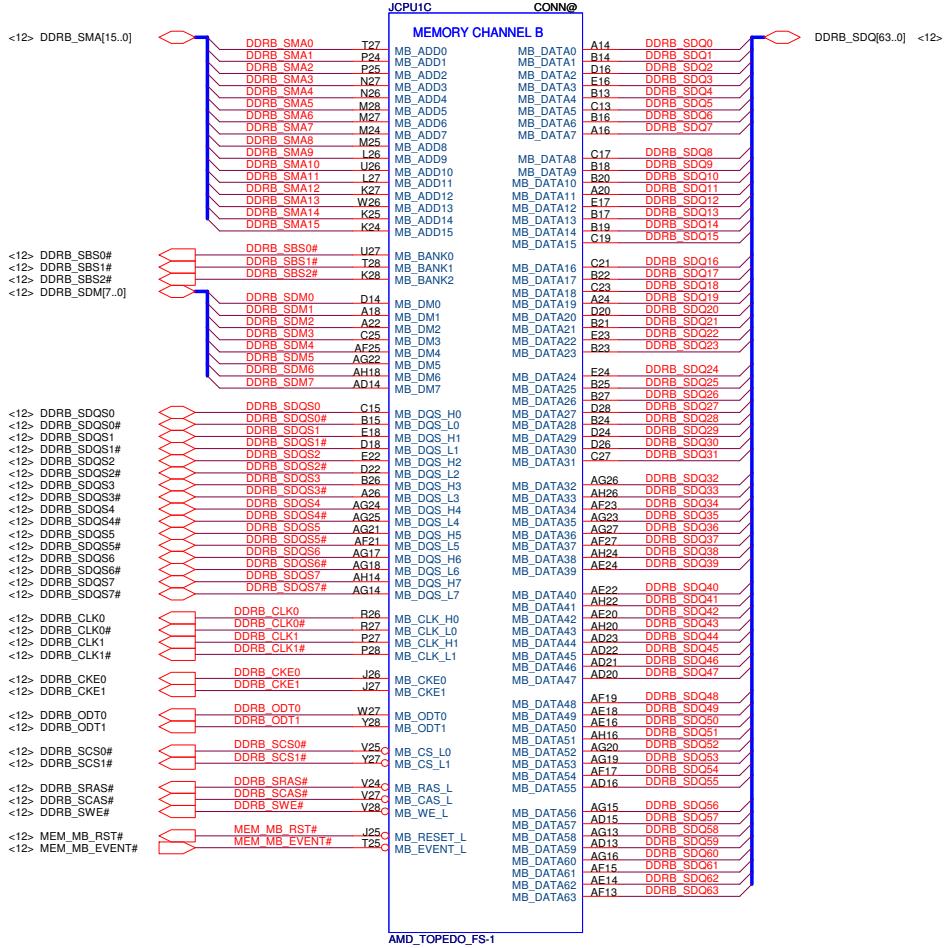
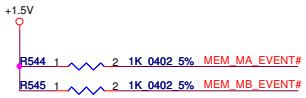
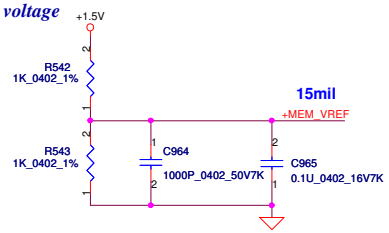




EVENT# pull high



0.75V reference voltage



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Title: AMD FS1 DDRIII I/F

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

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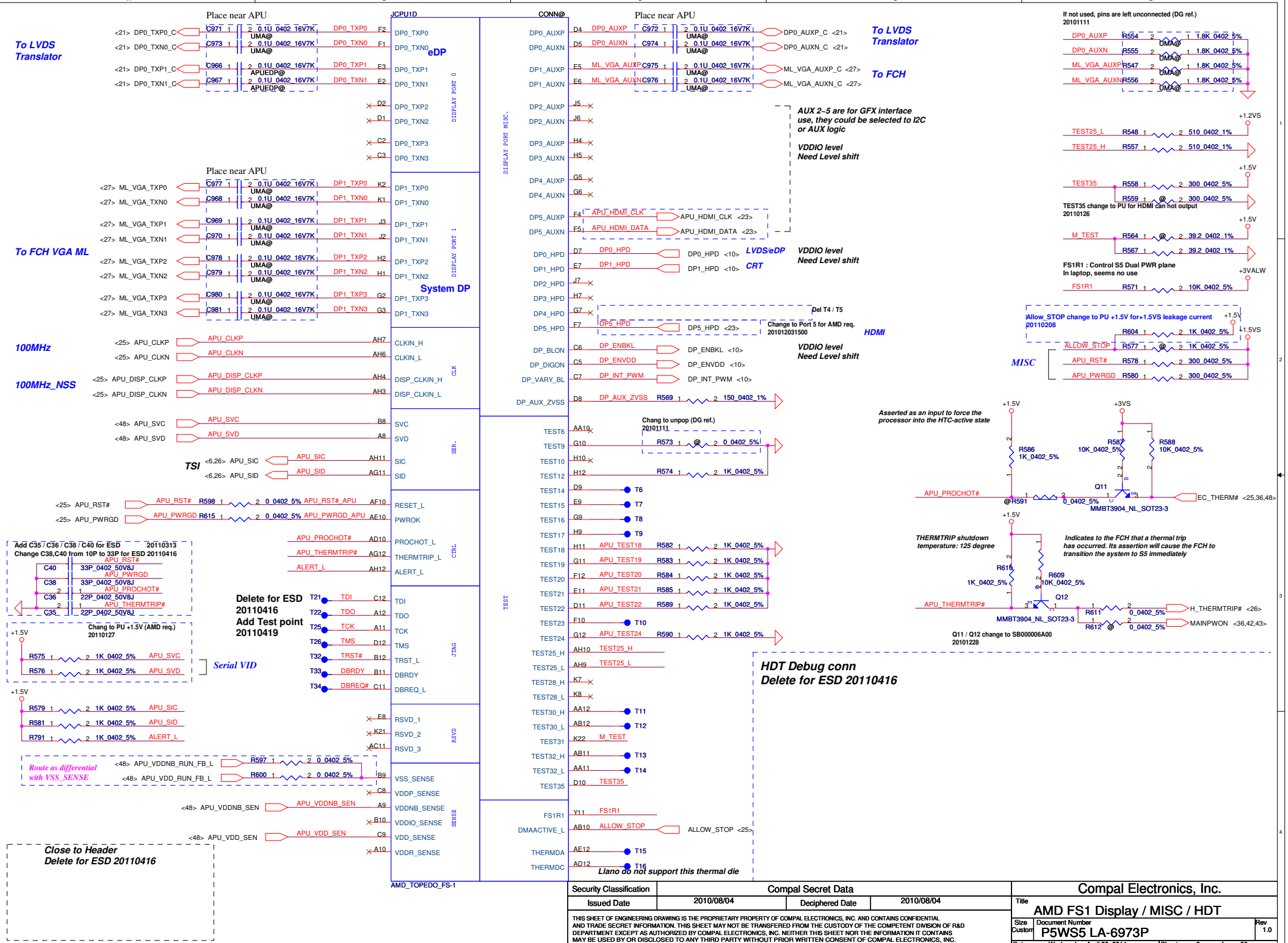

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Title: AMD FS1 Display / MISC / HDT

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Power Name	Consumption
VDD +CPU_CORE	54A
VDDNB +CPU_CORE_NB	27.5A
VDDIO +1.5V	4.6A
VDDP / VDDR +1.2VS	3A / 3.7A
VDDA +2.5VS	0.5A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

CPU BOTTOM SIDE DECOUPLING

+CPU_CORE — 22U Change to SE000000I10

C982 22U_0805_6.3V6M, C996 22U_0805_6.3V6M, C983 22U_0805_6.3V6M, C984 22U_0805_6.3V6M, C997 22U_0805_6.3V6M, C985 22U_0805_6.3V6M, C986 22U_0805_6.3V6M, C987 0.22U_0603_16V4Z, C988 0.22U_0603_16V4Z, C989 0.01U_0402_16V7K, C990 0.01U_0402_16V7K, C991 180P_0402_50V8J, C992 180P_0402_50V8J, C993 330U_D2_2VY_R7M, C994 330U_D2_2VY_R7M, C999 330U_D2_2VY_R7M, C995 330U_D2_2VY_R7M

+CPU_CORE_NB

C1000 22U_0805_6.3V6M, C1001 22U_0805_6.3V6M, C1002 22U_0805_6.3V6M, C1003 22U_0805_6.3V6M, C1004 0.22U_0603_16V4Z, C1005 0.22U_0603_16V4Z, C1006 180P_0402_50V8J, C1007 180P_0402_50V8J, C1008 180P_0402_50V8J, C1009 330U_D2_2VY_R7M, C1010 330U_D2_2VY_R7M

Delete C1011 20101101

+CPU_CORE

C29 330U_D2_2VY_R7M, C30 330U_D2_2VY_R7M @

For there phase 20101225 Delete 3 phase SKU 20110419

+1.5V

C1012 22U_0805_6.3V6M, C1013 22U_0805_6.3V6M, C14 4.7U_0603_6.3V6K, C15 4.7U_0603_6.3V6K, C16 4.7U_0603_6.3V6K, C17 4.7U_0603_6.3V6K, C1018 0.22U_0603_16V4Z, C1019 0.22U_0603_16V4Z, C1020 0.22U_0603_16V4Z, C1021 0.22U_0603_16V4Z, C1022 0.22U_0603_16V4Z, C1023 0.22U_0603_16V4Z, C1024 180P_0402_50V8J, C1025 180P_0402_50V8J, C5 330U_D2_2VY_R7M

C5 change to D2 type 201011241030

+1.5V

C1027 0.22U_0603_16V4Z, C1028 0.22U_0603_16V4Z, C1029 180P_0402_50V8J, C1030 180P_0402_50V8J

Decoupling between CPU and DIMMs across VDDIO and VSS split

JCPU1E CONN@

2160mil: +CPU_CORE — C1 D3 D6 E1 F3 F6 F8 G1 H3 H6 H8 J1 K3 K6 L1 L11 L19 M3 M6 M10 M18 N1 N11 N19 P3 P6 P10 P18 R1 R11 R19 T3 — VDD — T6 T10 T18 U1 U11 U19 V3 V6 V10 V18 W1 W11 W13 W15 W17 W19 Y3 Y6 Y10 Y12 Y14 Y16 Y18 Y20 AA1 AB3 AB6 AC1 AD3 AD6 AE1 — +CPU_CORE

1120mil: +CPU_CORE_NB — J9 J10 J11 J12 J14 J16 K9 K10 — VDDNB — K11 K12 K13 K14 K16 K17 K18 L18 — +CPU_CORE_NB

200mil: +1.5V — G28 H26 J28 K20 K23 K26 L22 L25 L28 M20 M23 M26 N22 N25 N28 P20 P23 P26 — VDDIO — R22 R25 R28 T20 T23 T26 U22 U25 U28 V20 V23 V26 W22 W25 W28 Y24 Y26 AA28 — +1.5V

120mil: +1.2VS — AG2 AG3 AG4 AG5 — VDDP_A_1 VDDP_A_2 VDDP_A_3 VDDP_A_4 — VDDP_B_1 VDDP_B_2 VDDP_B_3 VDDP_B_4 — A3 A4 B3 B4 — 120mil

160mil: +1.2VS — AG6 AG7 AG8 AG9 — VDDR — A5 A6 B5 B6 — 160mil

40mil: +2.5VS — L1 FBMA-L11-201209-221LMA30T_0805 — AE11 AF11 — VDDA

C1040 3300P_0402_50V7K, C1041 0.22U_0603_16V4Z, C18 47U_0805_4V6, C1043 180P_0402_50V8J

Del C1039 201012061900

C18 Change to 47U 20110124

AMD_TOPEDO_FS-1

Keep trace from resistor to APU within 0.6"

Keep trace from Caps to APU within 1.2"

VDDP decoupling

+1.2VS — C8 10U_0603_6.3V6M, C7 10U_0603_6.3V6M, C6 10U_0603_6.3V6M, C1034 180P_0402_50V8J, C1035 180P_0402_50V8J, C1036 180P_0402_50V8J, C1037 0.22U_0603_16V4Z, C1038 220U_6.3V_M

C1038 change to SF000002Y00 20101228

VDDR decoupling

+1.2VS — C1044 180P_0402_50V8J, C1045 180P_0402_50V8J, C1046 180P_0402_50V8J, C1047 180P_0402_50V8J, C1048 180P_0402_50V7K, C1049 1000P_0402_50V7K, C1050 1000P_0402_50V7K, C1051 1000P_0402_50V7K

C1052 0.22U_0603_16V4Z, C1053 0.22U_0603_16V4Z, C1054 0.22U_0603_16V4Z, C1055 0.22U_0603_16V4Z, C10 4.7U_0603_6.3V6K, C11 4.7U_0603_6.3V6K, C12 4.7U_0603_6.3V6K, C13 4.7U_0603_6.3V6K

JCPU1F CONN@

A7 A13 A15 A17 A19 A21 A23 A25 B7 C4 C10 C14 C16 C18 C20 C22 C24 C26 C28 D13 D15 D17 D19 D21 D23 D25 D27 E4 E10 E12 F9 F11 F14 F16 F18 F20 F22 F24 F26 F28 G4 G8 G13 G15 G17 G19 G21 G23 G25 J4 J8 J18 J20 J22 J24 K19 L4 L7 L10 M9 M11 M19 N4 N7 N10 N18 P9 P11 P19 R4 R7 R10 R18 T9 — VSS — T11 T19 U4 U7 U10 U18 V9 V11 V19 W4 W7 W10 W12 W14 W16 W18 Y9 Y22 AA4 AA7 AB9 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AB27 AC4 AC7 AC10 AC12 AC14 AC16 AC18 AC20 AC22 AC24 AC26 AC28 AD9 AD11 AE4 AE7 AE13 AE15 AE17 AE19 AE21 AE23 AE25 AE27 AF3 AF6 AF9 AF12 AF14 AF16 AF18 AF20 AF22 AF24 AF26 AF28 AG10 AH5 AH8 AH13 AH15 AH17 AH19 AH21 AH23 AH25

AMD_TOPEDO_FS-1

Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180uF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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Title: AMD FS1 PWR / GND

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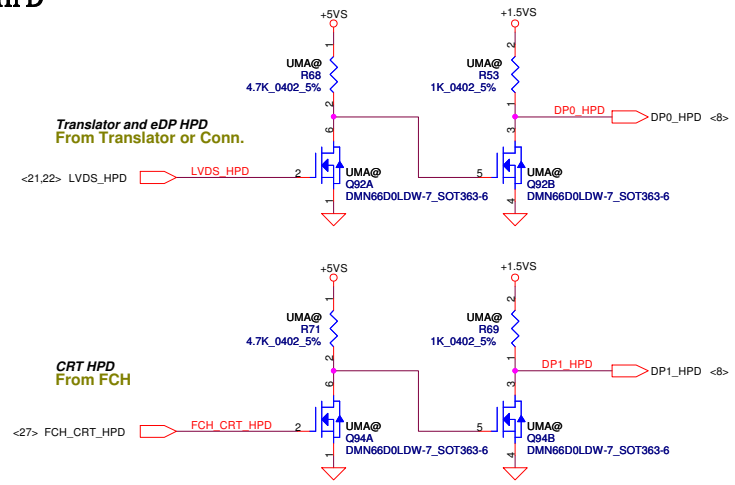
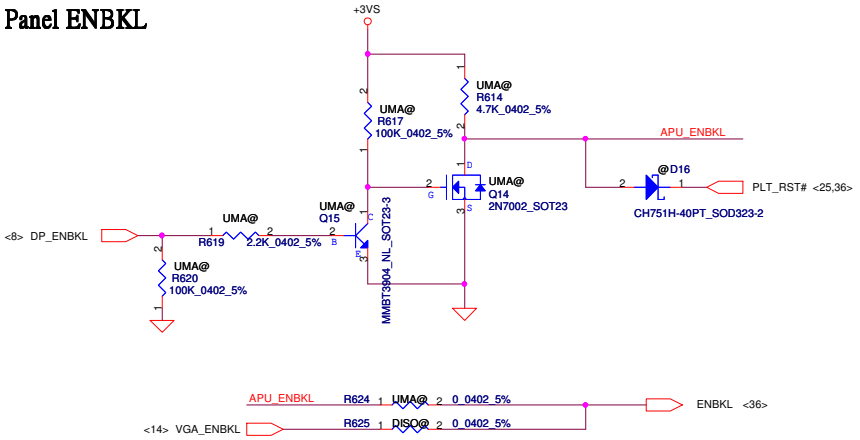
HPD

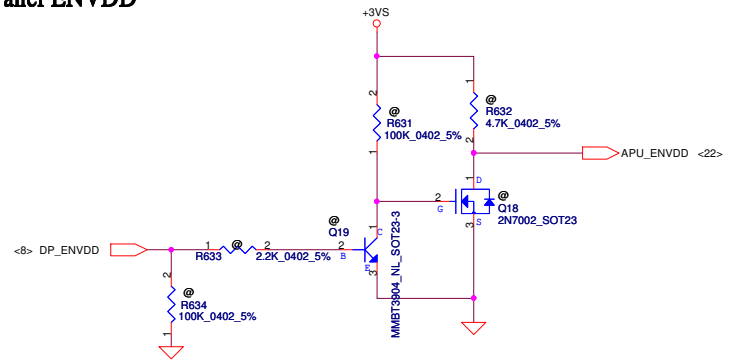


HDMI HPD
Page 23

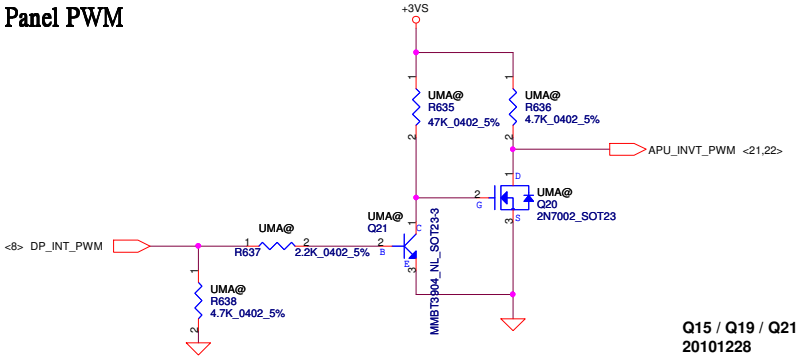
Panel ENBKL



Panel ENVDD



Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

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Title: AMD FS1 Singal Level Shifter

Size	Document Number	Rev
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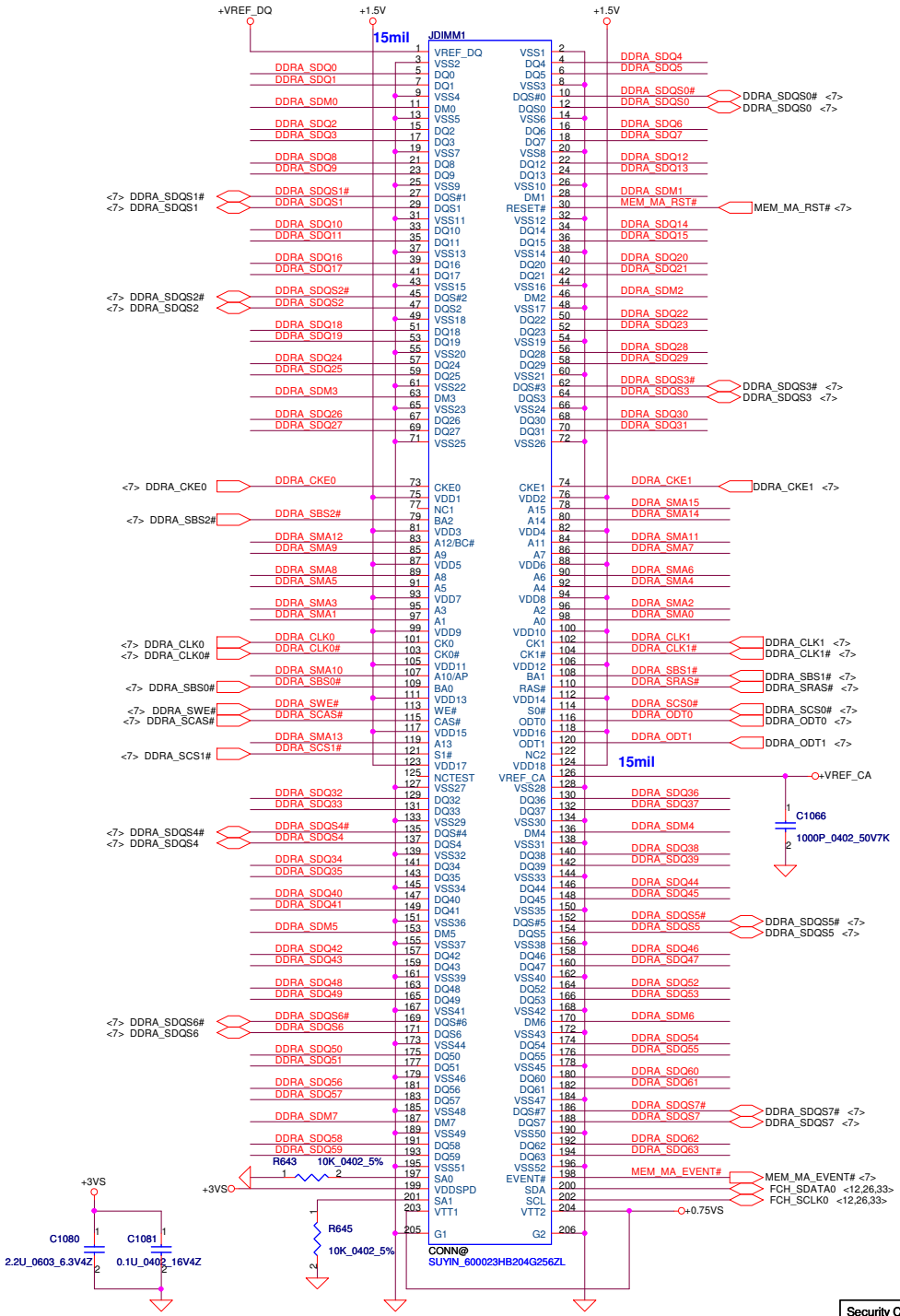
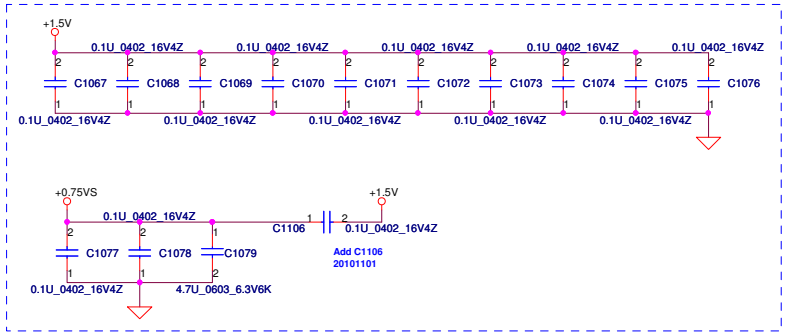
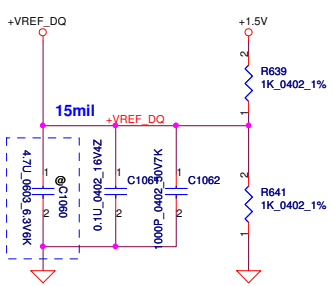
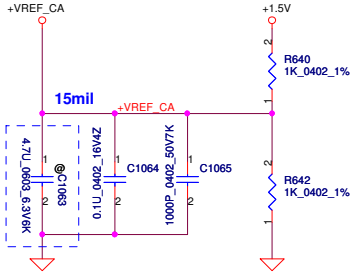


Place near DIMM1







DIMM_A STD H:8mm Change to SUYIN SP07000N500

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

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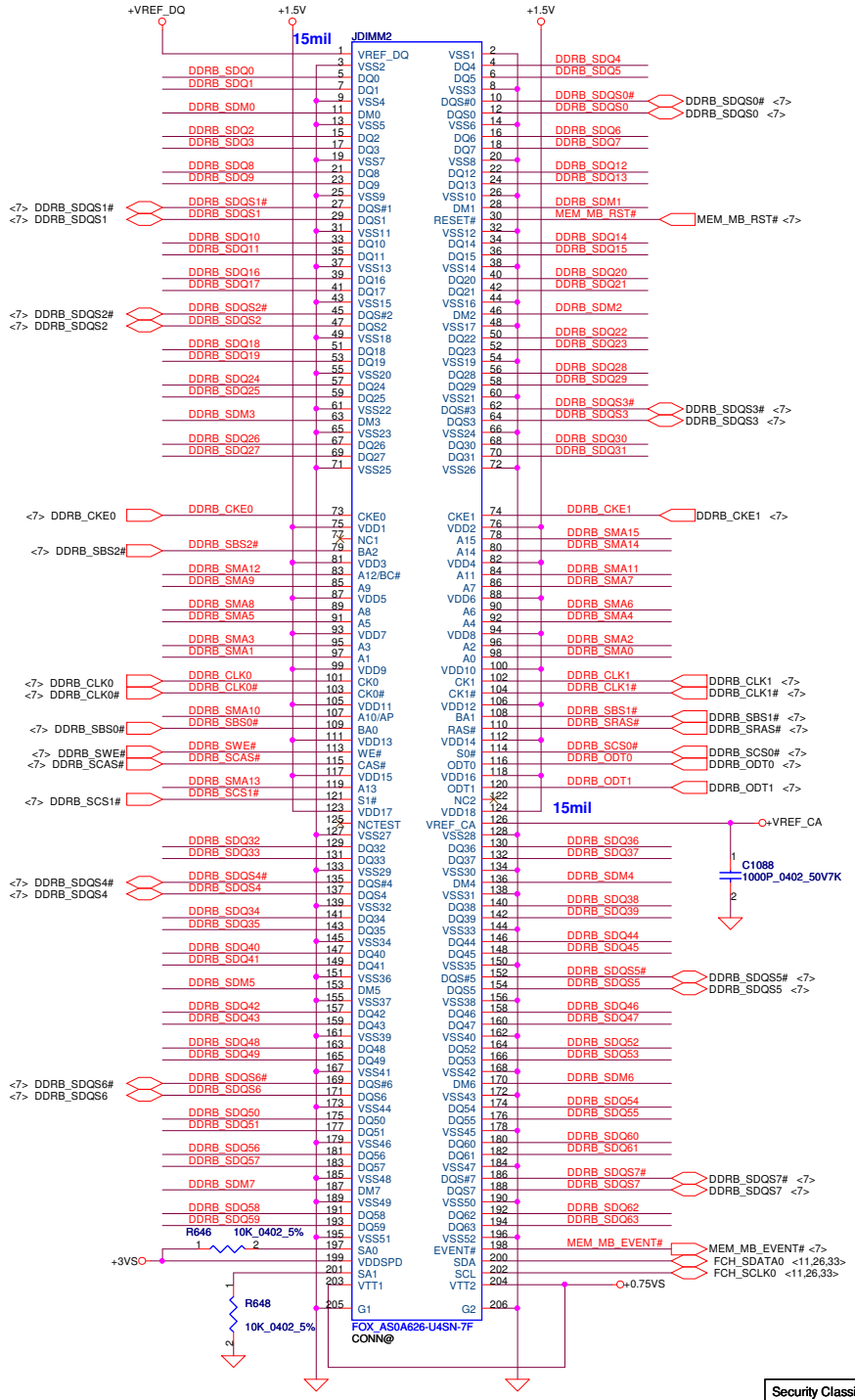
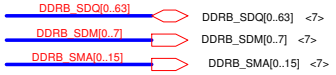
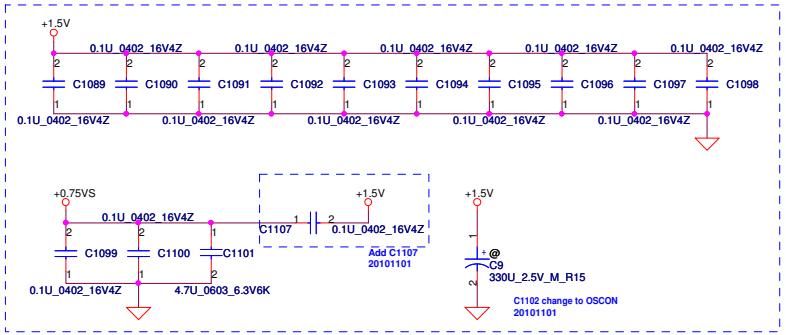
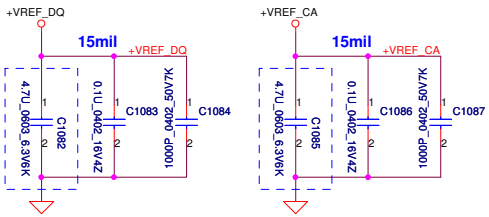




Place near DIMM2





DIMM_B STD H:4mm

<Address: 01>

P/N: SP07000H800
F/P: FOX_AS0A626-U4SN-7F_204P

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

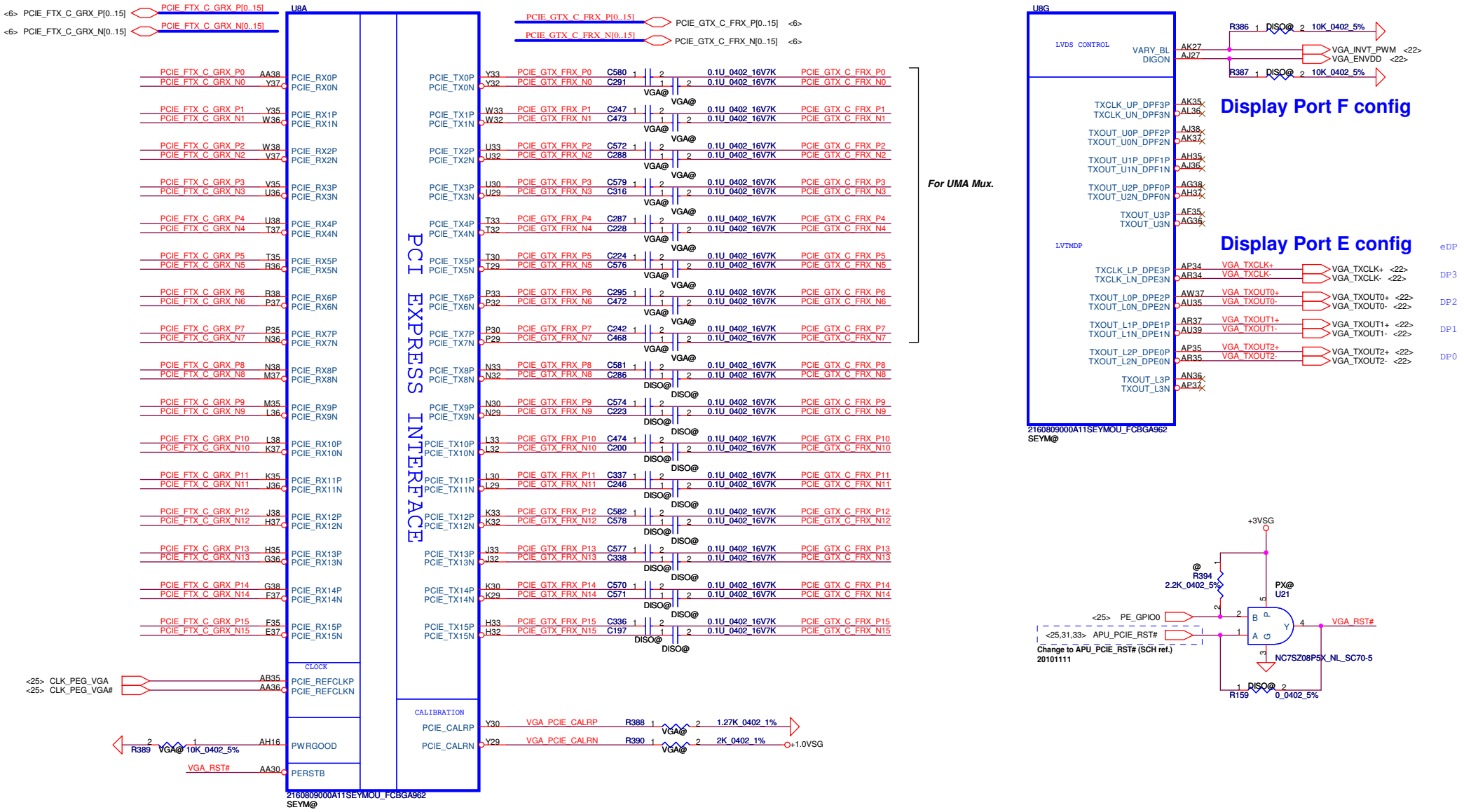
Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 12 of 50

GFX PCIE LANE REVERSAL

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need



For UMA Mux.

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 13 of 50

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

VRAM ID

VRAM_ID0 VRAM_ID1 VRAM_ID2 VRAM_ID3

GPIO5 fast-power reduction:
HW control will casue display disturb
should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

DISCRETE ONLY
PD 100K at EC side
<10> VGA_ENBKL

GPIO7 Controls backlight on/off.
Active High ,need external PD
if GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

ROM

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

Park NC pins

External 500KHz 3.3V CLK

SM010030010
200ma 120ohm@100mhz DCR 0.2

Future ASIC call MLPS.
OLD ASIC is Fan PWM

120ohm/0.3A

U8B

MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
THERMAL
PLL/CLOCK

2160809000A11SEYMOU_FCBGA962
SEYM@

NC on Park, Robson and Seymour

Not share via for other GND

NC on Whistler and Seymour

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

HDMI

LVDS

NC on Park, Robson and Seymour

CRT

NC on Park, Robson and Seymour

External VGA Thermal Sensor

ADM1032ARMZ-2REEL_MSOP8

Q8A DMN66D0LDW-7_SOT363-6
Q8B DMN66D0LDW-7_SOT363-6

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap
CRT,HDMI DDC

GPIO8 Serial-ROM output from ROM, GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

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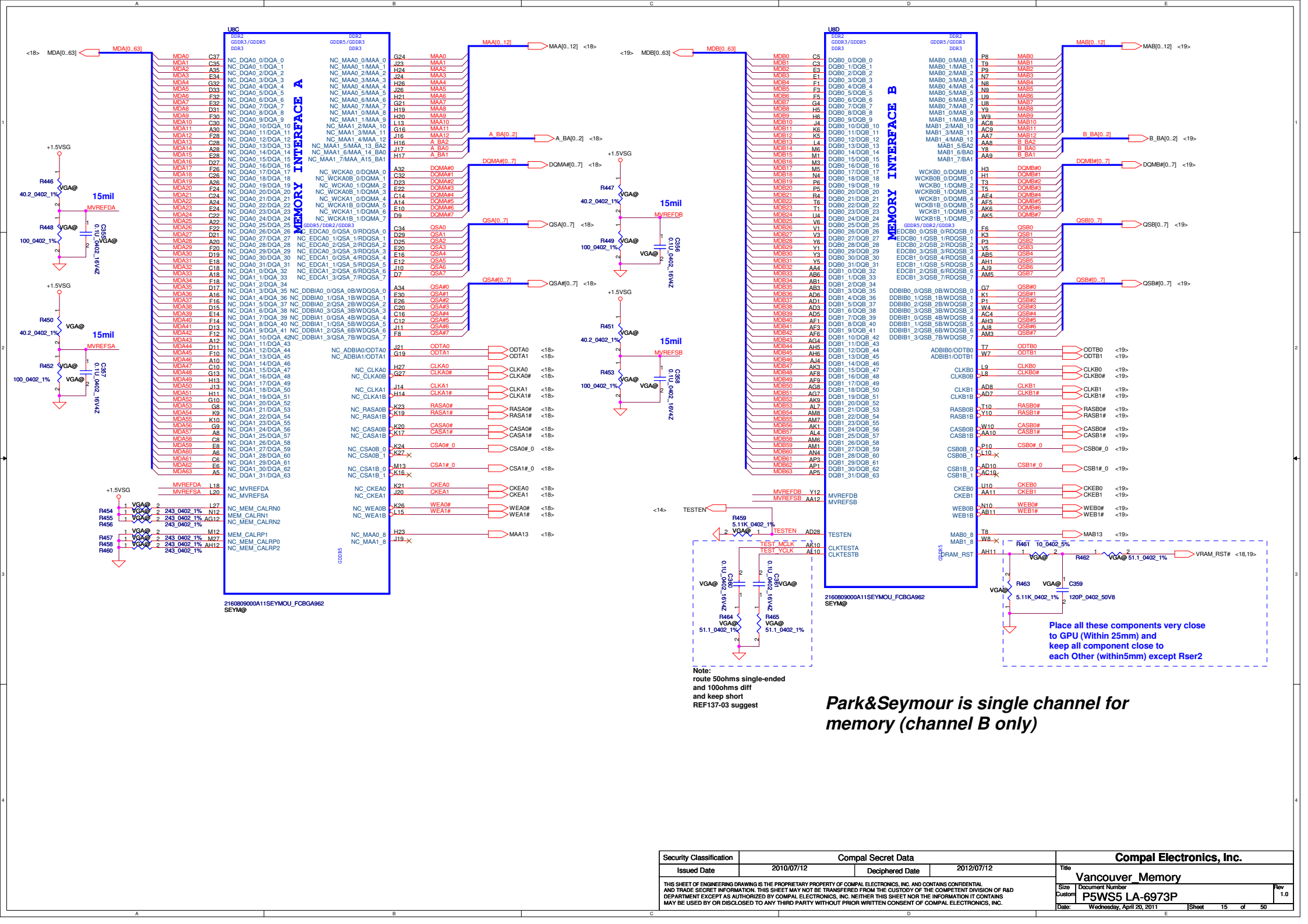


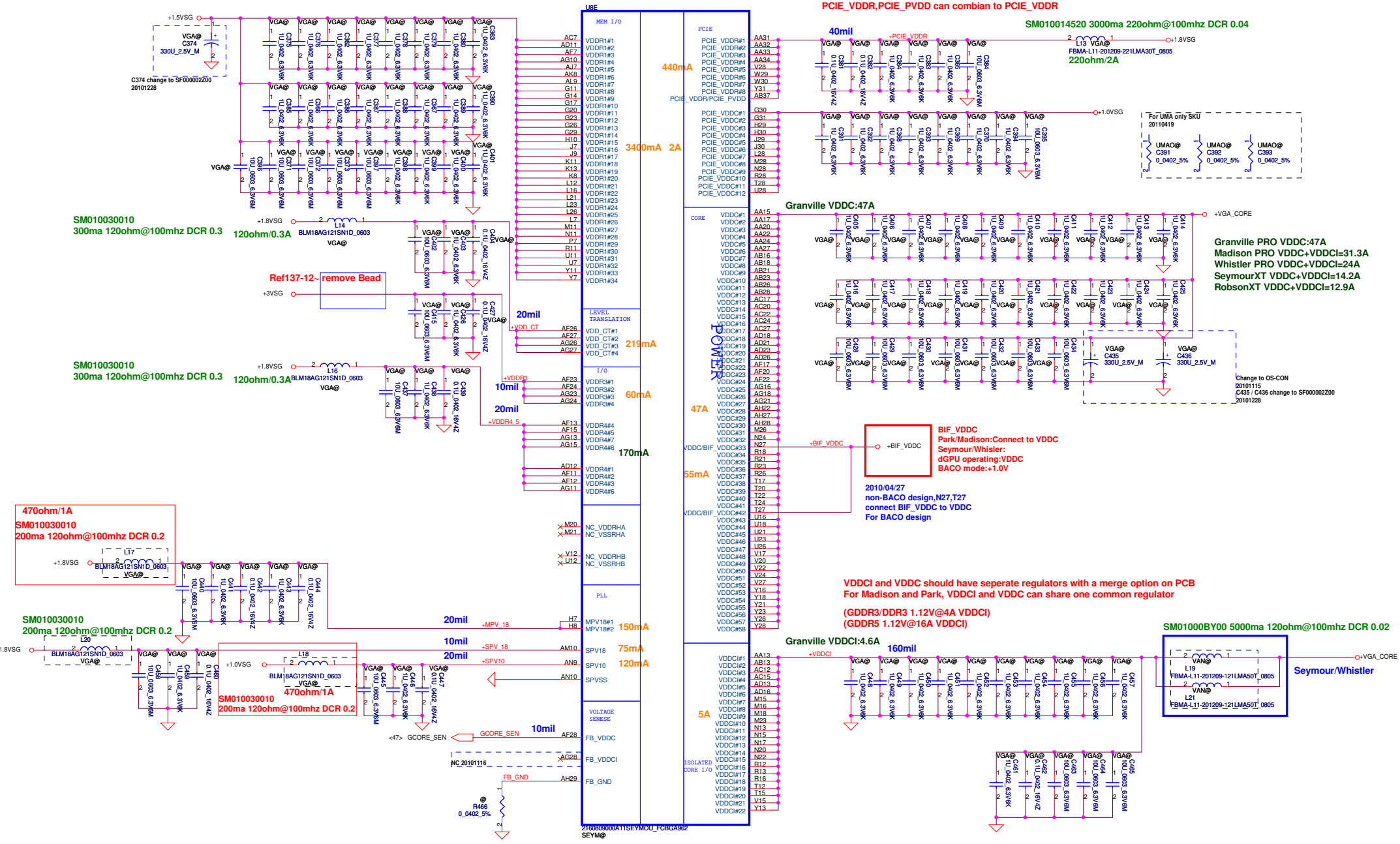
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 15 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 16 of 50

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

PCIE_VSS#1 PCIE_VSS#2 PCIE_VSS#3 PCIE_VSS#4 PCIE_VSS#5 PCIE_VSS#6 PCIE_VSS#7 PCIE_VSS#8 PCIE_VSS#9 PCIE_VSS#10 PCIE_VSS#11 PCIE_VSS#12 PCIE_VSS#13 PCIE_VSS#14 PCIE_VSS#15 PCIE_VSS#16 PCIE_VSS#17 PCIE_VSS#18 PCIE_VSS#19 PCIE_VSS#20 PCIE_VSS#21 PCIE_VSS#22 PCIE_VSS#23 PCIE_VSS#24 PCIE_VSS#25 PCIE_VSS#26 PCIE_VSS#27 PCIE_VSS#28 PCIE_VSS#29 PCIE_VSS#30 PCIE_VSS#31 PCIE_VSS#32 PCIE_VSS#33 PCIE_VSS#34 PCIE_VSS#35

GND

GND#100 GND#101 GND#102 GND#103 GND#104 GND#105 GND#106 GND#107 GND#108 GND#109 GND#110 GND#111 GND#112 GND#113 GND#114 GND#115 GND#116 GND#117 GND#118 GND#119 GND#120 GND#121 GND#122 GND#123 GND#124 GND#125 GND#126 GND#127 GND#128 GND#129 GND#130 GND#131 GND#132 GND#133 GND#134 GND#135 GND#136 GND#137 GND#138 GND#139 GND#140 GND#141 GND#142 GND#143 GND#144 GND#145 GND#146 GND#147 GND#148 GND#149 GND#150 GND#151 GND#153 GND#154 GND#155 GND#156 GND#157 GND#158 GND#159 GND#160 GND#161 GND#163 GND#164 GND#165 GND#166 GND#167 GND#168 GND#169 GND#170 GND#171 GND#172 GND#173 GND#174 GND#175 GND#152 GND#162

GND#1 GND#2 GND#3 GND#4 GND#5 GND#6 GND#7 GND#8 GND#9 GND#10 GND#11 GND#12 GND#13 GND#14 GND#15 GND#16 GND#17 GND#18 GND#19 GND#20 GND#21 GND#22 GND#23 GND#24 GND#25 GND#26 GND#27 GND#28 GND#29 GND#30 GND#31 GND#32 GND#33 GND#34 GND#35 GND#36 GND#37 GND#38 GND#39 GND#40 GND#41 GND#42 GND#43 GND#44 GND#45 GND#46 GND#47 GND#48 GND#49 GND#50 GND#51 GND#52 GND#53 GND#54 GND#55 GND#56 GND#57 GND#58 GND#59 GND#60 GND/PX_EN#61 GND#62 GND#63 GND#64 GND#65 GND#66 GND#67 GND#68 GND#69 GND#70 GND#71 GND#72 GND#73 GND#74 GND#75 GND#76 GND#77 GND#78 GND#79 GND#80 GND#81 GND#82 GND#83 GND#84 GND#85 GND#86 GND#87 GND#88 GND#89 GND#90 GND#91 GND#92 GND#93 GND#94 GND#95 GND#96 GND#97 GND#98

VSS_MECH#1 VSS_MECH#2 VSS_MECH#3

2160809000A11SEYMOU_FCBGA962
SEYM@

REF137-13 update

PX_EN <20>

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

U8H

Manhatann:300mA
Seymour:150mA

20mil +DPABCD_VDD18 AP20 AP21 DPCD/DPC_VDD18#1 DPCD/DPC_VDD18#2
20mil +DPABCD_VDD10 AP13 AT13 DPCD/DPC_VDD10#1 DPCD/DPC_VDD10#2
DP/DPC_VSSR#1 DP/DPC_VSSR#2 DP/DPC_VSSR#3 DP/DPC_VSSR#4 DP/DPC_VSSR#5
20mil +DPABCD_VDD18 AP22 AP23 DPCD/DPD_VDD18#1 DPCD/DPD_VDD18#2
20mil +DPABCD_VDD10 AP14 AP15 DPCD/DPD_VDD10#1 DPCD/DPD_VDD10#2

Manhatann:220mA
Seymour:110mA

DP/DPD_VSSR#1 DP/DPD_VSSR#2 DP/DPD_VSSR#3 DP/DPD_VSSR#4 DP/DPD_VSSR#5

R467 150_0402_1% VGA@ AW18 DPCD_CALR

DP mode:300mA
LVDS mode:440mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26 MBK1608221YZF_2P VGA@ +1.8VSG
FootPrint
VGA@ C478 10U_0603_6.3V6M VGA@ C479 1U_0402_6.3V6K VGA@ C480 0.1U_0402_16V4Z

20mil +DPEF_VDD18 AH34 AJ34 DPEF/DPE_VDD18#1 DPEF/DPE_VDD18#2
20mil +DPEF_VDD10 AL33 AM33 DPEF/DPE_VDD10#1 DPEF/DPE_VDD10#2
DP/DPE_VSSR#1 DP/DPE_VSSR#2 DP/DPE_VSSR#3 DP/DPE_VSSR#4

DP mode:220mA
LVDS mode:240mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27 MBK1608221YZF_2P VGA@ +1.0VSG
FootPrint
VGA@ C481 10U_0603_6.3V6M VGA@ C482 1U_0402_6.3V6K VGA@ C483 0.1U_0402_16V4Z

20mil +DPEF_VDD18 AF34 AG34 DPEF/DPF_VDD18#1 DPEF/DPF_VDD18#2
20mil +DPEF_VDD10 AK33 AK34 DPEF/DPF_VDD10#1 DPEF/DPF_VDD10#2
DP/DPF_VSSR#1 DP/DPF_VSSR#2 DP/DPF_VSSR#3 DP/DPF_VSSR#4 DP/DPF_VSSR#5

R470 150_0402_1% VGA@ AM39 DPEF_CALR

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

DPAB/DPA_VDD18#1 DPAB/DPA_VDD18#2
DPAB/DPA_VDD10#1 DPAB/DPA_VDD10#2
DP/DPA_VSSR#1 DP/DPA_VSSR#2 DP/DPA_VSSR#3 DP/DPA_VSSR#4 DP/DPA_VSSR#5
DPAB/DPB_VDD18#1 DPAB/DPB_VDD18#2
DPAB/DPB_VDD10#1 DPAB/DPB_VDD10#2
DP/DPB_VSSR#1 DP/DPB_VSSR#2 DP/DPB_VSSR#3 DP/DPB_VSSR#4 DP/DPB_VSSR#5
DPAB_CALR
DPAB_VDD18/DPA_PVDD DP_VSSR/DPA_PVSS
DPAB_VDD18/DPB_PVDD DP_VSSR/DPB_PVSS
DPCD_VDD18/DPC_PVDD DP_VSSR/DPC_PVSS
DPCD_VDD18/DPD_PVDD DP_VSSR/DPD_PVSS
DPEF_VDD18/DPE_PVDD DP_VSSR/DPE_PVSS
DPEF_VDD18/DPF_PVDD DP_VSSR/DPF_PVSS

20mil +DPABCD_VDD18 AN24 AP24 300mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23 MBK1608221YZF_2P VGA@ +1.8VSG
FootPrint
VGA@ C469 10U_0603_6.3V6M VGA@ C470 0.1U_0402_16V4Z VGA@ C471 1U_0402_6.3V6K

20mil +DPABCD_VDD10 AP31 AP32
AN27 AP27 AP28 AW24 AW26
20mil +DPABCD_VDD18 AP25 AP26
20mil +DPABCD_VDD10 AN33 AP33 220mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25 MBK1608221YZF_2P VGA@ +1.0VSG
FootPrint
VGA@ C475 0.1U_0402_16V4Z VGA@ C476 1U_0402_6.3V6K VGA@ C477 10U_0603_6.3V6M

AN29 AP29 AP30 AW30 AW32
R468 150_0402_1% VGA@ AW28

20mA 10mil +DPABCD_VDD18 AU28 AV27
20mA 10mil +DPABCD_VDD18 AV29 AR28
20mA 10mil +DPABCD_VDD18 AU18 AV17
20mA 10mil +DPABCD_VDD18 AV19 AR18
20mA 10mil +DPEF_VDD18 AM37 AN38
20mA 10mil +DPEF_VDD18 AL38 AM35

2160809000A11SEYMOU_FCBGA962
SEYM@

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

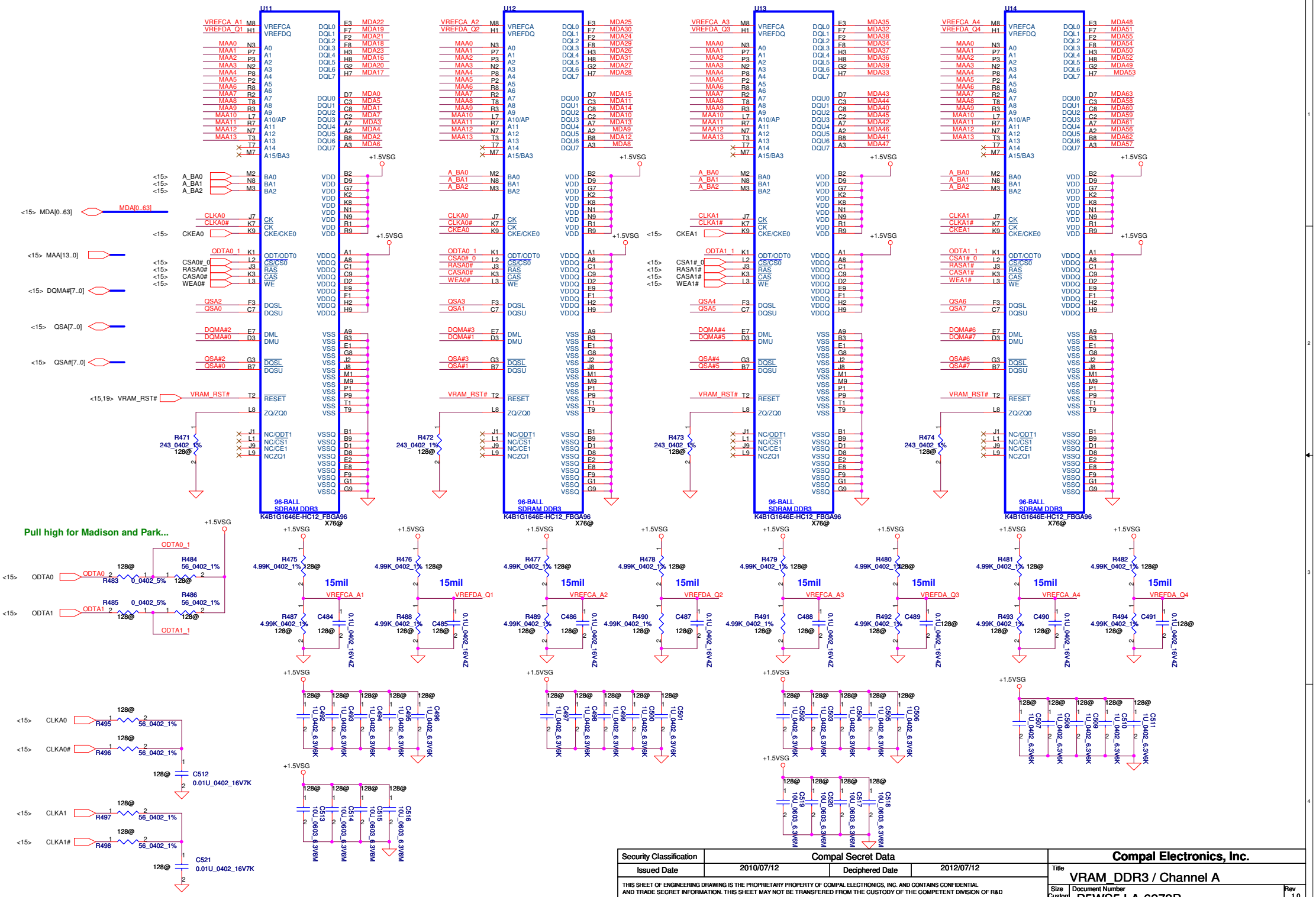
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 17 of 50



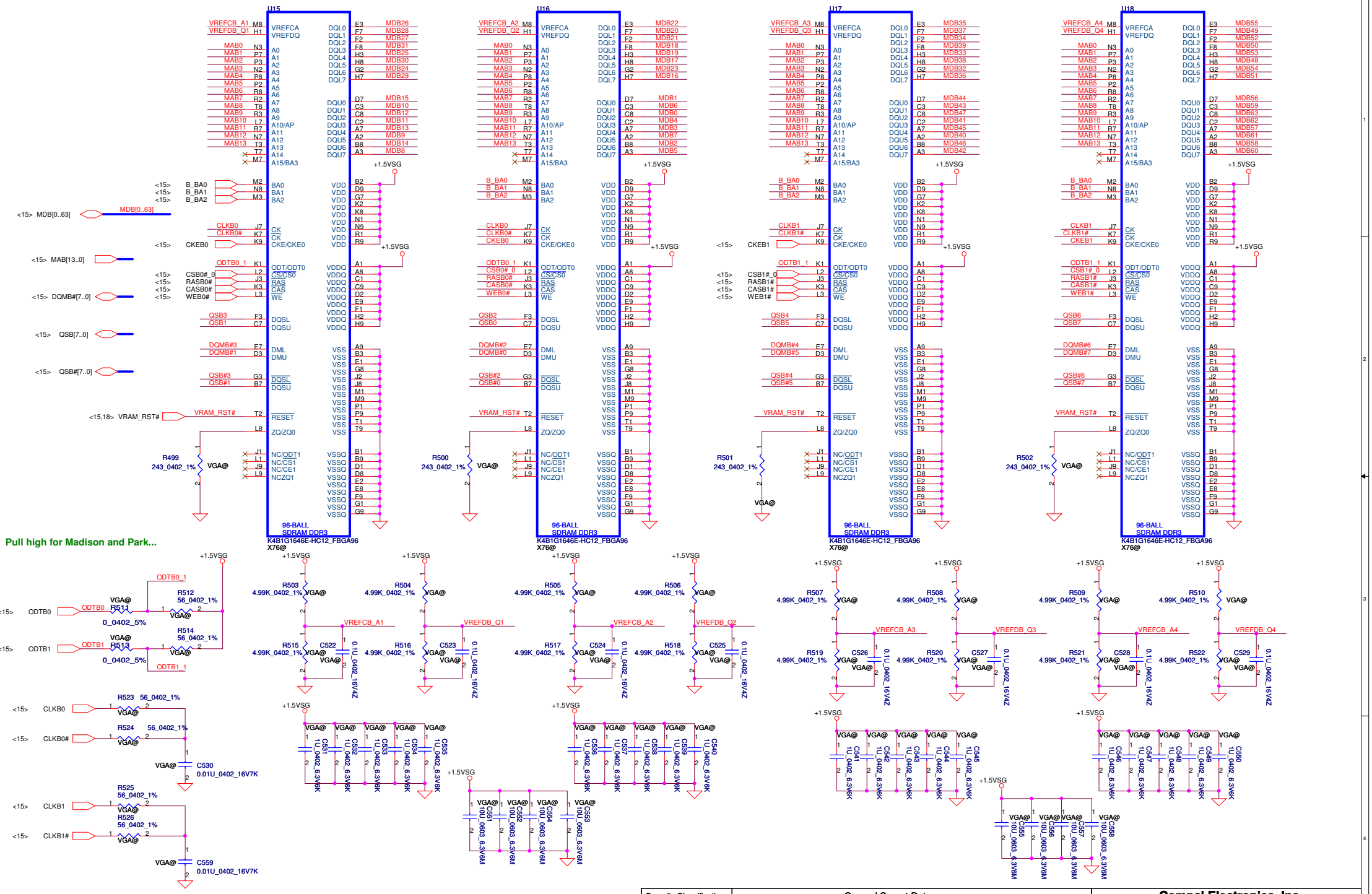
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 18 of 50



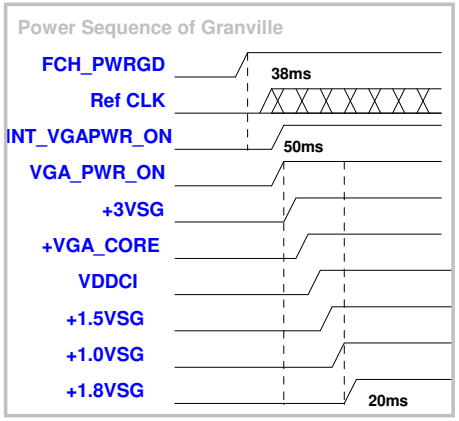
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

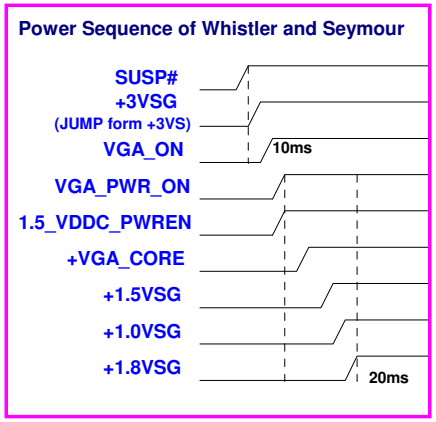
Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 19 of 50

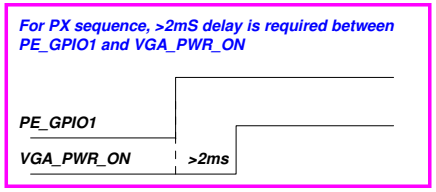


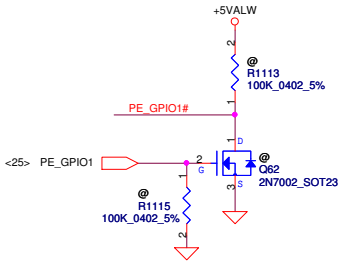


VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

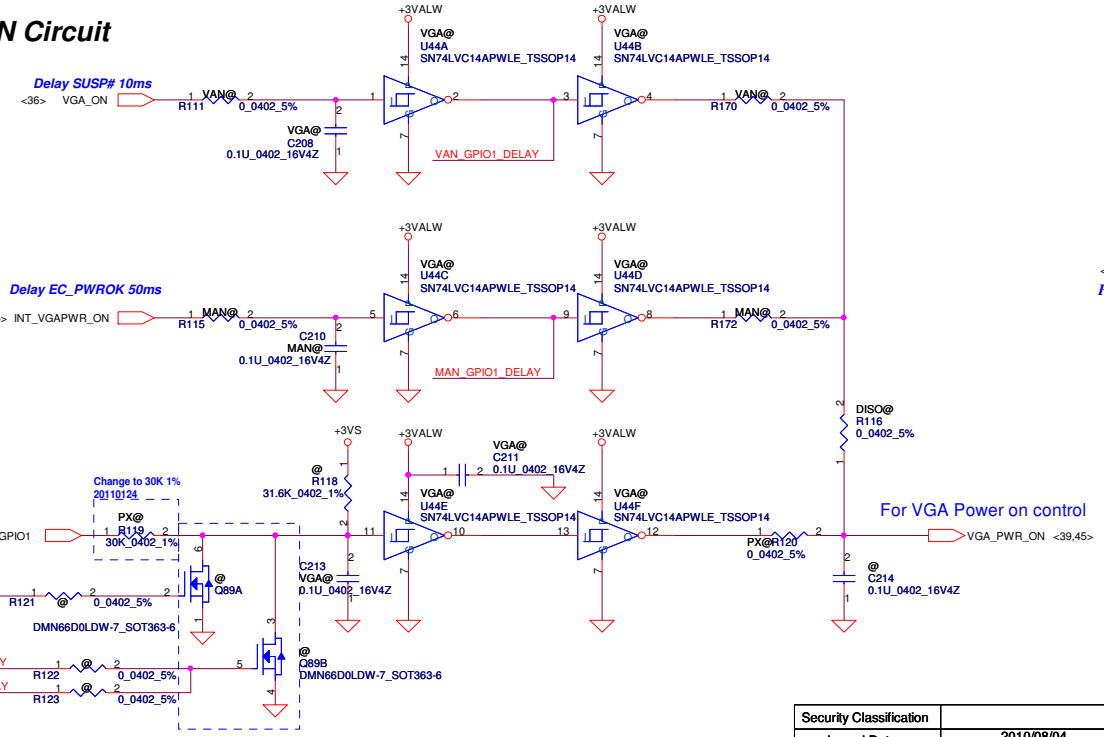
VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

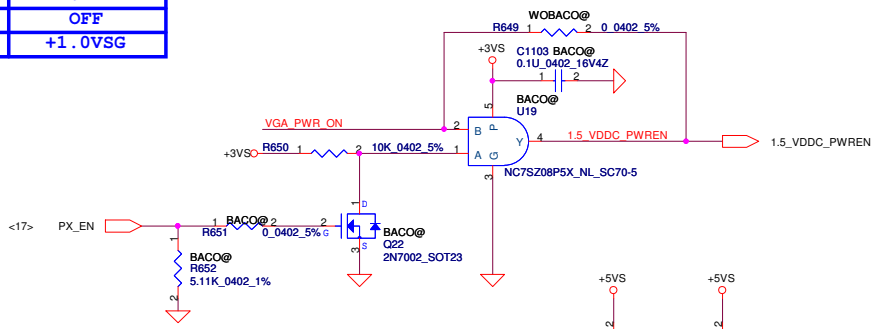
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

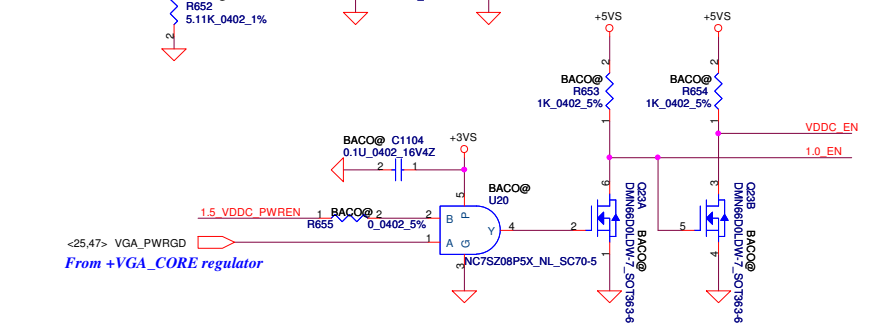


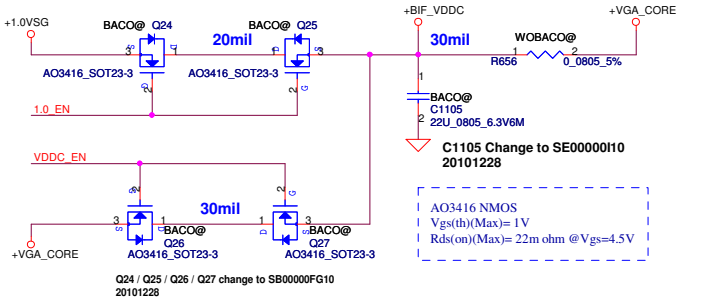


VGA Power ON Circuit









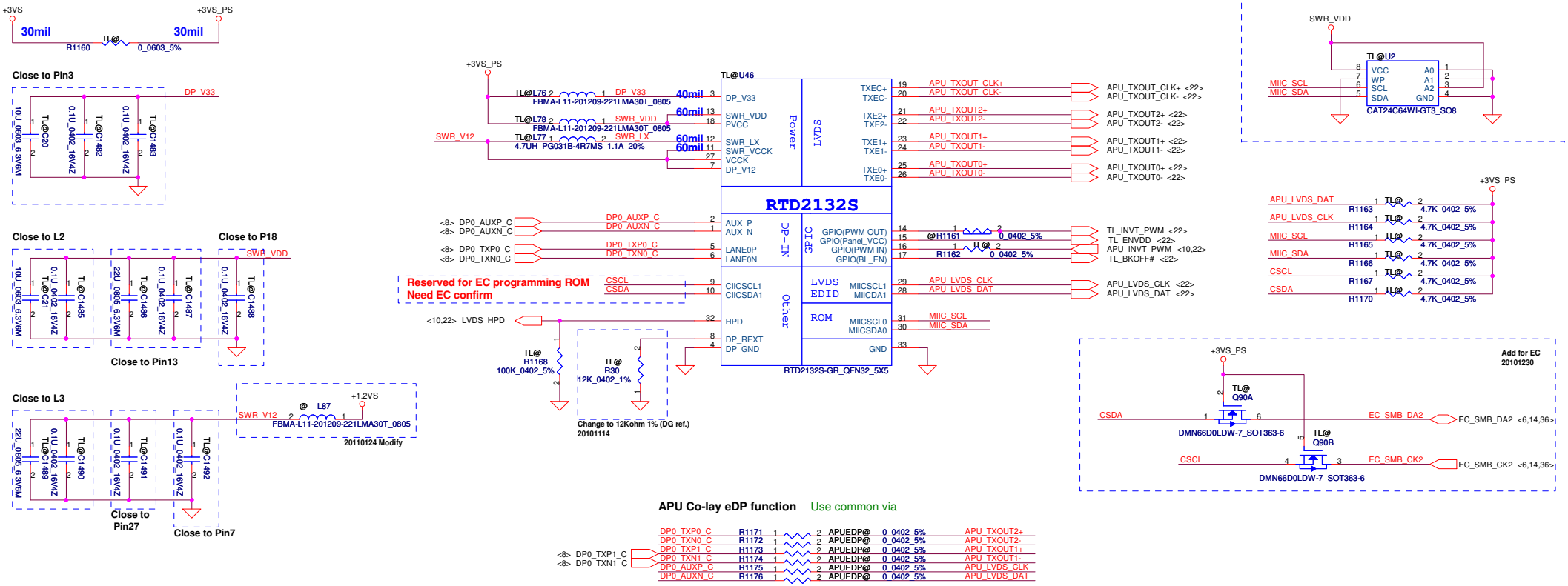
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: VGA power sequence and BACO

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 20 of 50



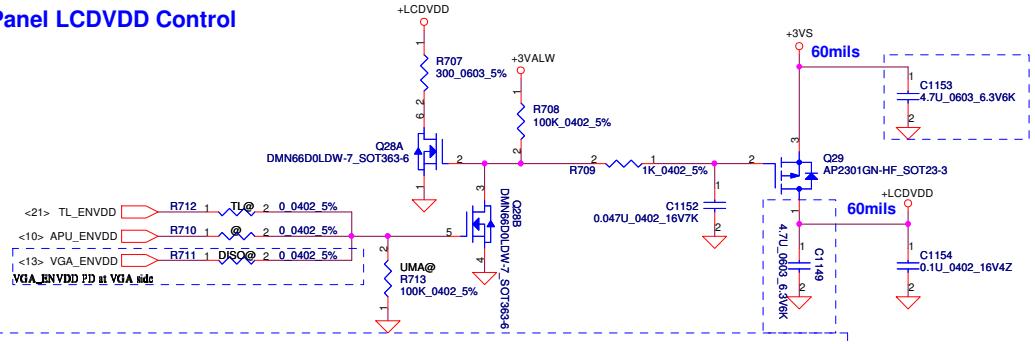
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Title: LVDS Translator - RTD2132S

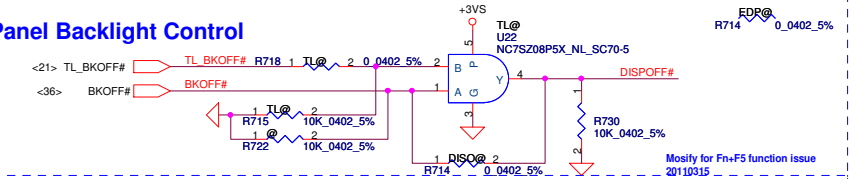
Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 21 of 50

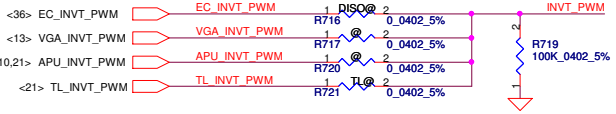
Panel LCDVDD Control



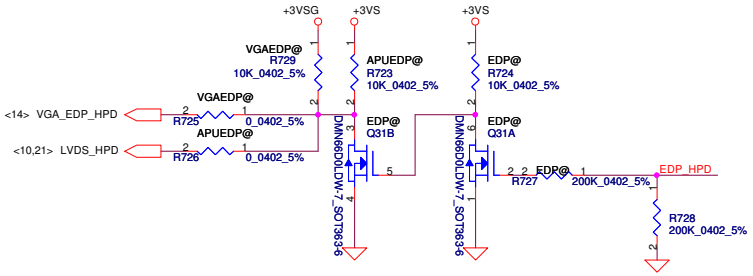
Panel Backlight Control



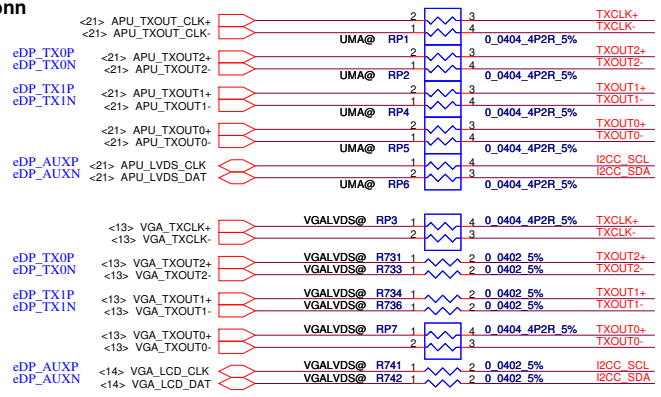
Panel PWM Control



eDP HDP for APU and VGA

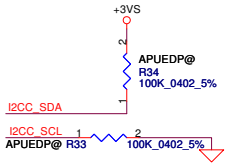


Translator LVDS Output



VGA LVDS Output

DG ref. Need close to eDP Conn.
201011251400

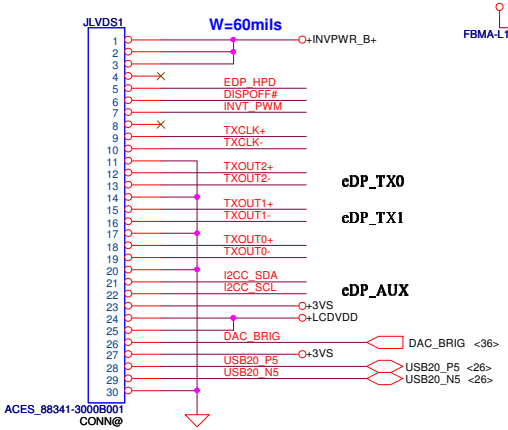


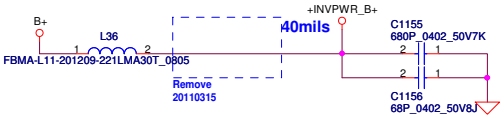
VGA Co-lay eDP function

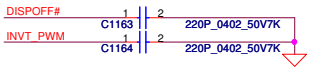
VGAEDP@ R731 0.1U_0402_16V7K
VGAEDP@ R733 0.1U_0402_16V7K
VGAEDP@ R734 0.1U_0402_16V7K
VGAEDP@ R736 0.1U_0402_16V7K
VGAEDP@ R741 0.1U_0402_16V7K
VGAEDP@ R742 0.1U_0402_16V7K

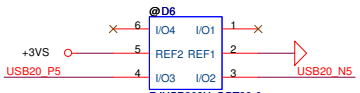
UMA/DIS LVDS/eDP Mapping table

UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
APU_TXOUT0+ APU_TXOUT0-		VGA_TXOUT0+ VGA_TXOUT0-		TXOUT0+ TXOUT0-
APU_TXOUT1+ APU_TXOUT1-	DP0_TXP1_R DP0_TXN1_R	VGA_TXOUT1+ VGA_TXOUT1-	eDP_TX1P eDP_TX1N	TXOUT1+ TXOUT1-
APU_TXOUT2+ APU_TXOUT2-	DP0_TXP0_R DP0_TXN0_R	VGA_TXOUT2+ VGA_TXOUT2-	eDP_TX0P eDP_TX0N	TXOUT2+ TXOUT2-
APU_TXOUT_CLK+ APU_TXOUT_CLK-		VGA_TXCLK+ VGA_TXCLK-		TXCLK+ TXCLK-
APU_TZOUT0+ APU_TZOUT0-		VGA_TZOUT0+ VGA_TZOUT0-		TZOUT0+ TZOUT0-
APU_TZOUT1+ APU_TZOUT1-		VGA_TZOUT1+ VGA_TZOUT1-		TZOUT1+ TZOUT1-
APU_TZOUT2+ APU_TZOUT2-		VGA_TZOUT2+ VGA_TZOUT2-		TZOUT2+ TZOUT2-
APU_TZOUT_CLK+ APU_TZOUT_CLK-		VGA_TZCLK+ VGA_TZCLK-		TZCLK+ TZCLK-
APU_LVDS_CLK APU_LVDS_DAT	DP0_AUXP_R DP0_AUXN_R	VGA_LCD_CLK VGA_LCD_DATA	eDP_AUXP eDP_AUXN	I2CC_SCL I2CC_SDA









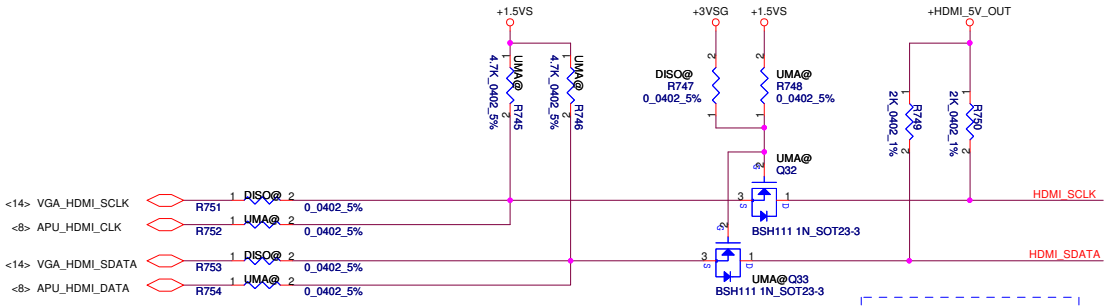
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

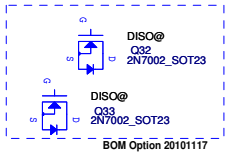
Compal Electronics, Inc.

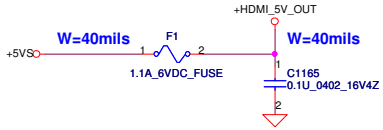
Title: LVDS/eDP Connector

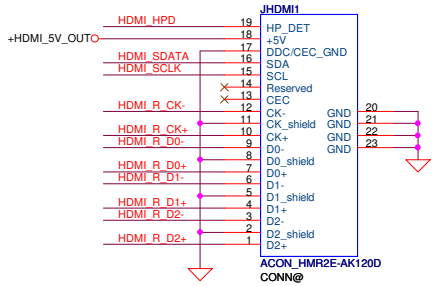
Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

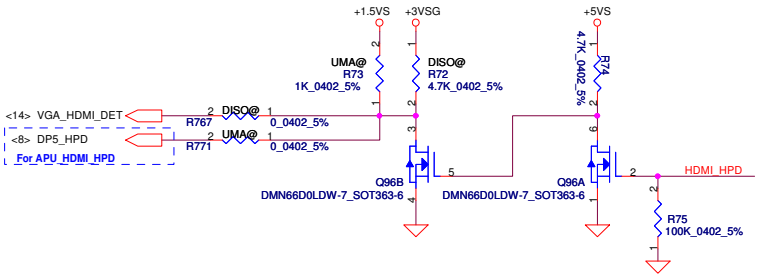
Date: Wednesday, April 20, 2011 Sheet 22 of 50





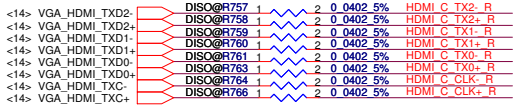






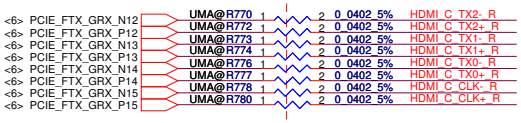
Place near C917~C924 and use common via

From VGA

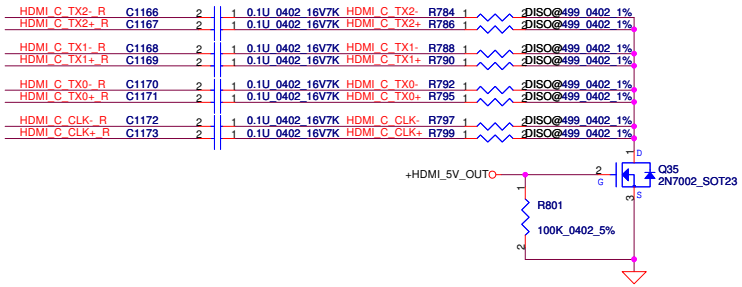


From APU

Change to 12~15 for AMD req.
201012031500



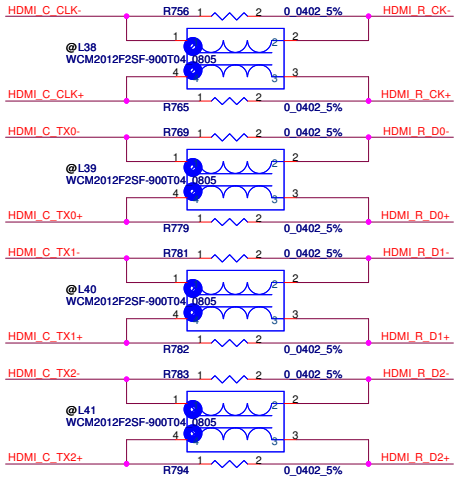
Near the connector



UMA use 604 ohm
VGA use 499 ohm

For UMA HDMI termination BOM option

R784 2 UMA@ 604_0402_1%
R786 2 UMA@ 604_0402_1%
R788 2 UMA@ 604_0402_1%
R790 2 UMA@ 604_0402_1%
R792 2 UMA@ 604_0402_1%
R795 2 UMA@ 604_0402_1%
R797 2 UMA@ 604_0402_1%
R799 2 UMA@ 604_0402_1%



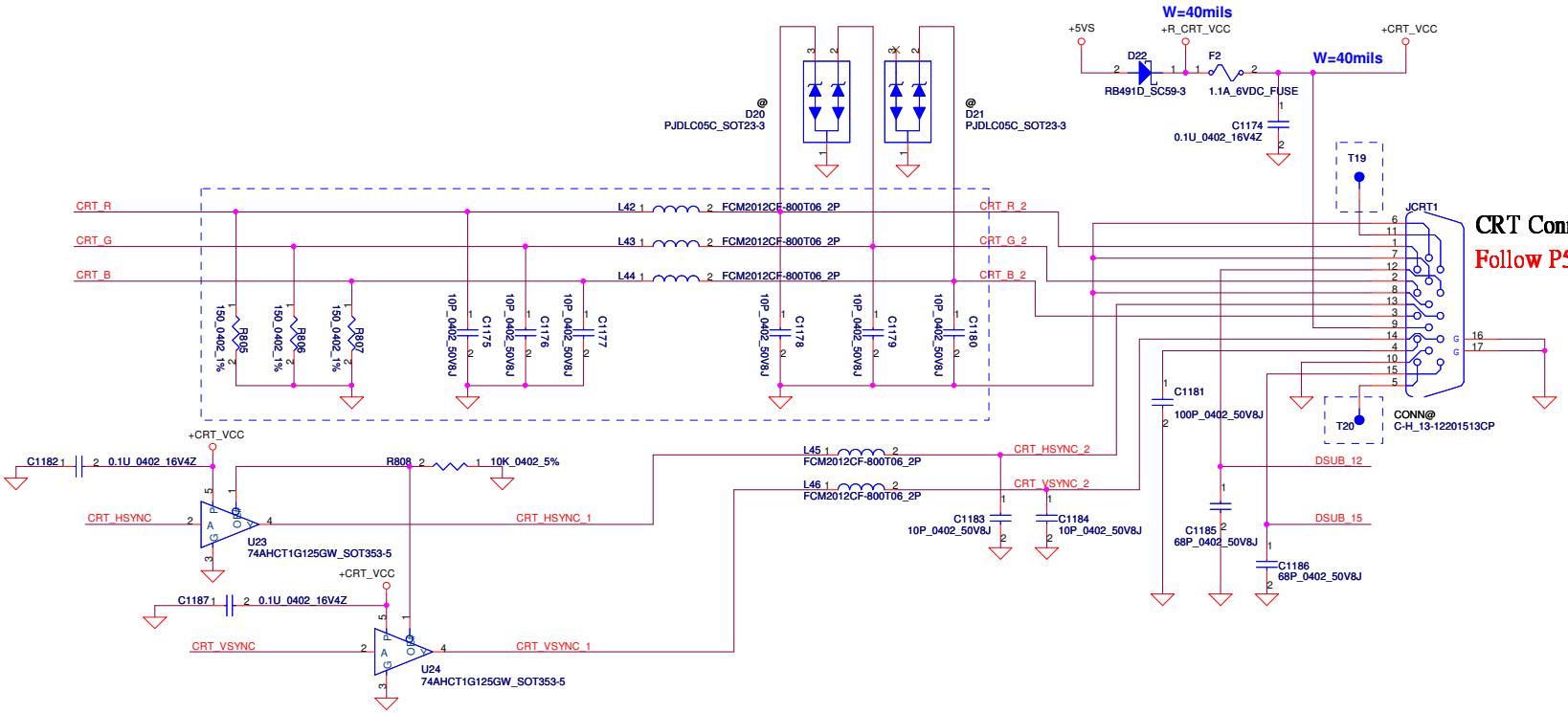
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 23 of 50



Use common via

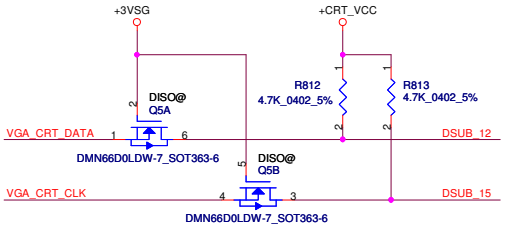
From FCH

<27> FCH_CRT_R — FCH_CRT_R — R809 2 UMA@ 1 0_0402_5% — CRT_R
<27> FCH_CRT_G — FCH_CRT_G — R810 2 UMA@ 1 0_0402_5% — CRT_G
<27> FCH_CRT_B — FCH_CRT_B — R811 2 UMA@ 1 0_0402_5% — CRT_B
<27> FCH_CRT_HSYNC — FCH_CRT_HSYNC — R814 2 UMA@ 1 0_0402_5% — CRT_HSYNC
<27> FCH_CRT_VSYNC — FCH_CRT_VSYNC — R815 2 UMA@ 1 0_0402_5% — CRT_VSYNC
<27> FCH_CRT_DDC_SDA — FCH_CRT_DDC_SDA — R816 2 UMA@ 1 0_0402_5% — DSUB_12
<27> FCH_CRT_DDC_SCL — FCH_CRT_DDC_SCL — R817 2 UMA@ 1 0_0402_5% — DSUB_15

From VGA

<14> VGA_CRT_R — VGA_CRT_R — R818 2 DISO@ 1 0_0402_5% — CRT_R
<14> VGA_CRT_G — VGA_CRT_G — R819 2 DISO@ 1 0_0402_5% — CRT_G
<14> VGA_CRT_B — VGA_CRT_B — R820 2 DISO@ 1 0_0402_5% — CRT_B
<14> VGA_CRT_HSYNC — VGA_CRT_HSYNC — R821 2 DISO@ 1 0_0402_5% — CRT_HSYNC
<14> VGA_CRT_VSYNC — VGA_CRT_VSYNC — R822 2 DISO@ 1 0_0402_5% — CRT_VSYNC
<14> VGA_CRT_DATA — VGA_CRT_DATA
<14> VGA_CRT_CLK — VGA_CRT_CLK

Close to Conn side



Change to 2N7002DW
20101111

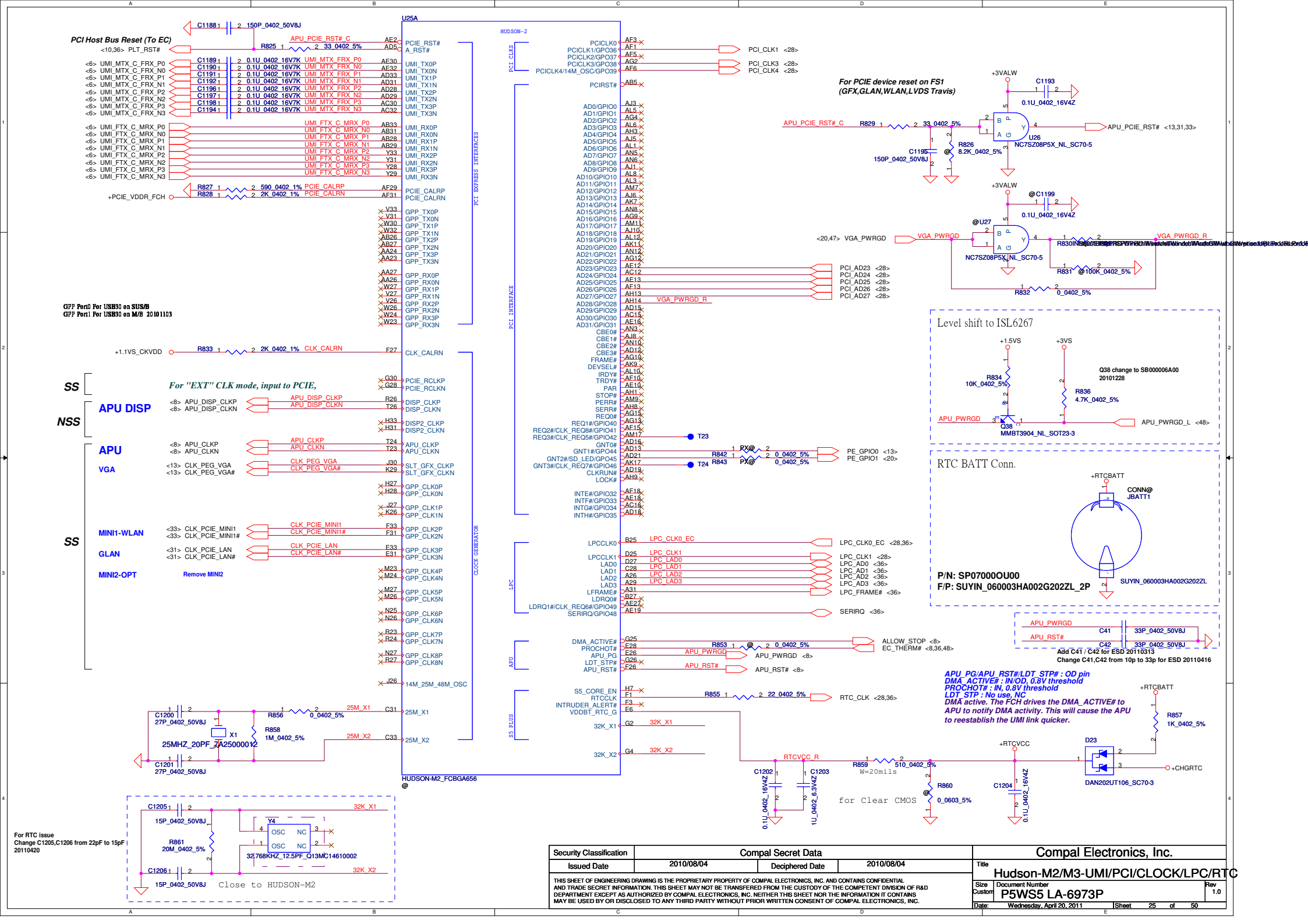
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 24 of 50



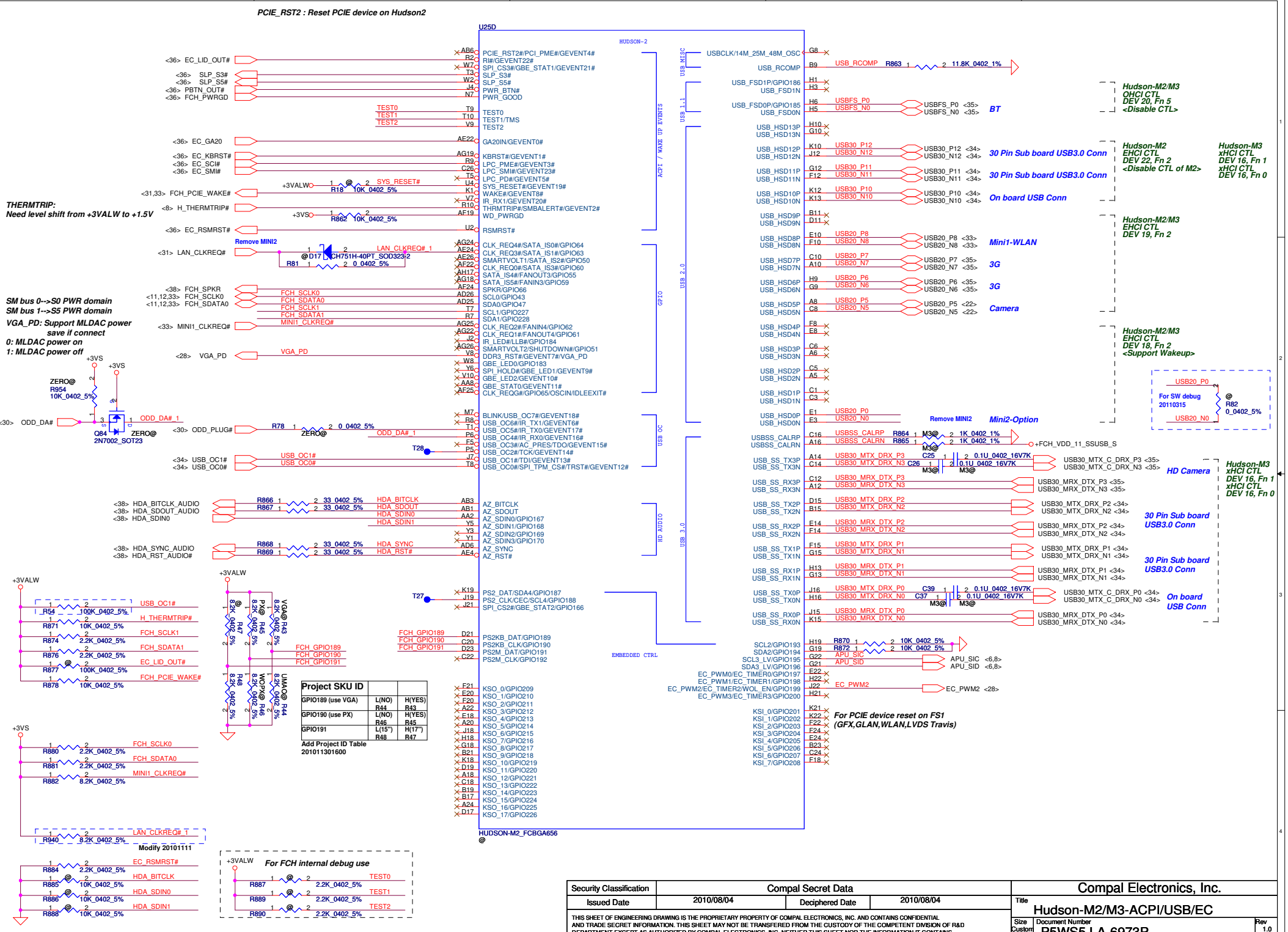
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 25 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

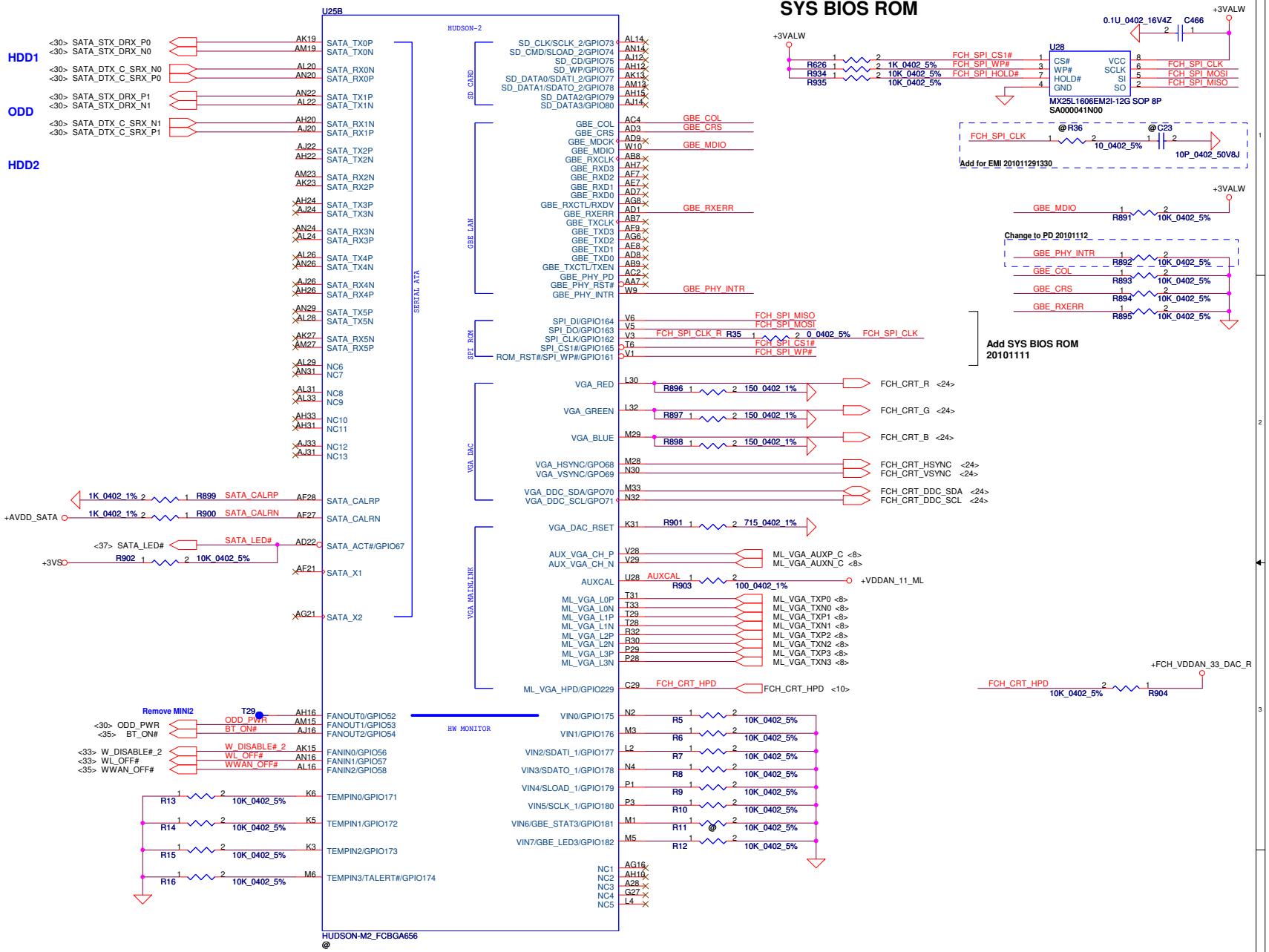
Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 26 of 50

SYS BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

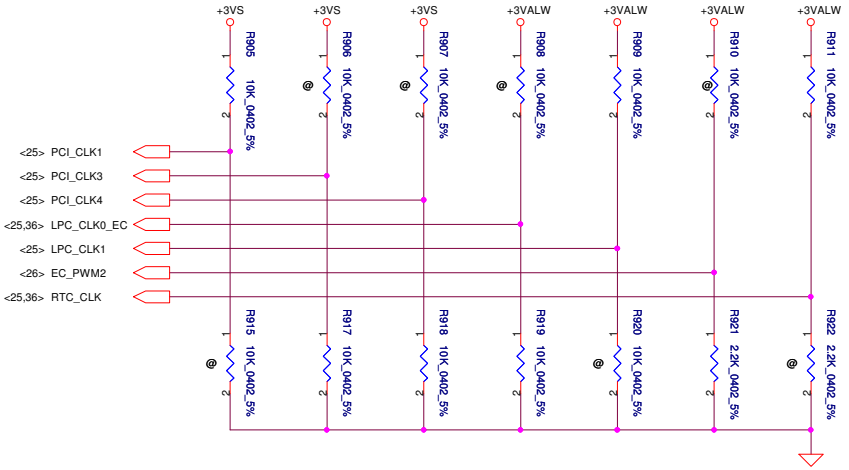
Title: Hudson-M2/M3-SATA/GBE/HWM

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 27 of 50

STRAP PINS

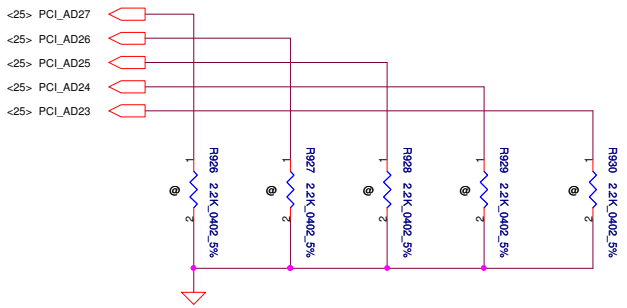
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

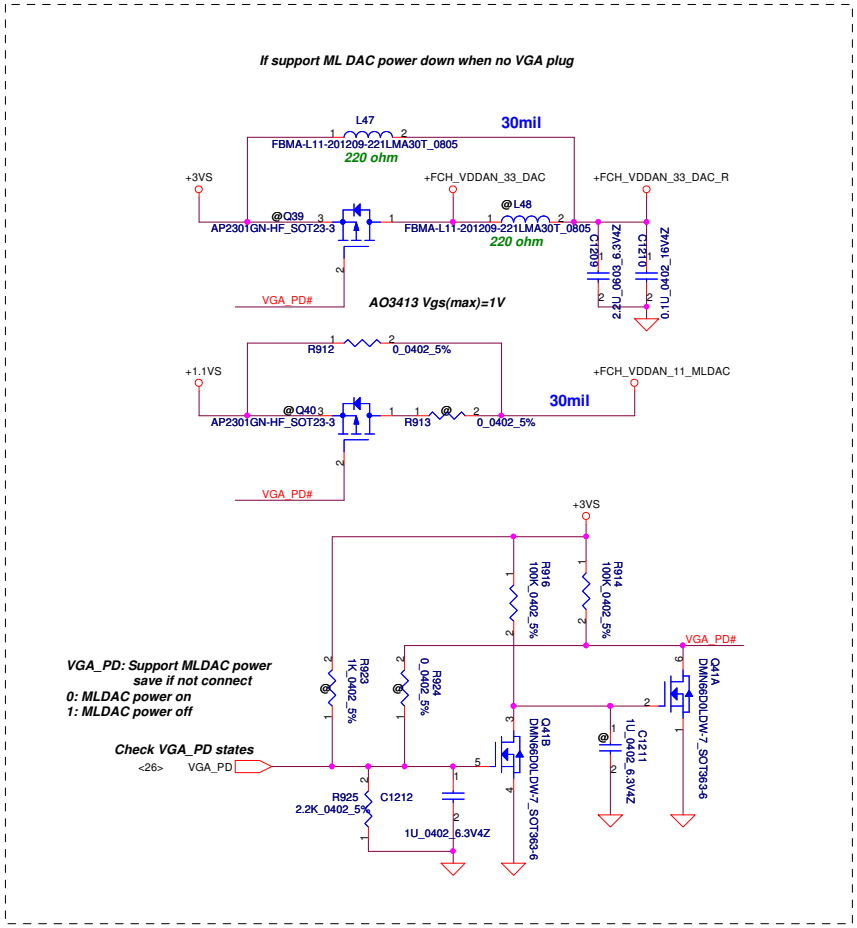


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 28 of 50

C1218 / C1219 / C1247 Change to SE00000I10
20101228

U25C

HUDSON-2

VDDIO_33_PCIGP_1 AB17
VDDIO_33_PCIGP_2 AB18
VDDIO_33_PCIGP_3 AE9
VDDIO_33_PCIGP_4 AD10
VDDIO_33_PCIGP_5 AG7
VDDIO_33_PCIGP_6 AC13
VDDIO_33_PCIGP_7 AB12
VDDIO_33_PCIGP_8 AB13
VDDIO_33_PCIGP_9 AB14
VDDIO_33_PCIGP_10 AB16

VDDCR_11_1 T14
VDDCR_11_2 T17
VDDCR_11_3 T20
VDDCR_11_4 U16
VDDCR_11_5 U18
VDDCR_11_6 V14
VDDCR_11_7 V17
VDDCR_11_8 V20
VDDCR_11_9 Y17

PCI/GPIO I/O
CORE SD

VDDIO_33_SYS H24
VDDIO_33_DAC V22
VDDIO_33_ML U22
VDDAN_33_DAC T22
VDDIO_33_SSUSB_S L18
VDDIO_33_USB_S D7
VDDIO_33_PCIE AH29
VDDIO_33_SATA AG28

VDDAN_11_CLK_1 H26
VDDAN_11_CLK_2 J25
VDDAN_11_CLK_3 K24
VDDAN_11_CLK_4 L22
VDDAN_11_CLK_5 M22
VDDAN_11_CLK_6 N21
VDDAN_11_CLK_7 N22
VDDAN_11_CLK_8 P22

CLKGEN I/O

VDDAN_11_PCIE_1 AB24
VDDAN_11_PCIE_2 Y21
VDDAN_11_PCIE_3 AE25
VDDAN_11_PCIE_4 AD24
VDDAN_11_PCIE_5 AB23
VDDAN_11_PCIE_6 AA22
VDDAN_11_PCIE_7 AF26
VDDAN_11_PCIE_8 AG27

PCI EXPRESS

LDO_CAP M31

VDDAN_11_DAC V21
VDDAN_11_ML V22
VDDAN_11_ML_1 V22
VDDAN_11_ML_2 V23
VDDAN_11_ML_3 V24
VDDAN_11_ML_4 V25

MAIN LINK

VDDAN_11_SATA_1 AA21
VDDAN_11_SATA_4 Y20
VDDAN_11_SATA_2 AB21
VDDAN_11_SATA_3 AB22
VDDAN_11_SATA_5 AC22
VDDAN_11_SATA_6 AC21
VDDAN_11_SATA_7 AA20
VDDAN_11_SATA_8 AA18
VDDAN_11_SATA_9 AB20
VDDAN_11_SATA_10 AC19

SERIAL ATA

VDDIO_33_GBE_S AB10
VDDCR_11_GBE_S_1 AB11
VDDCR_11_GBE_S_2 AA11
VDDIO_GBE_S_1 AA9
VDDIO_GBE_S_2 AA10

GBE LAN

VDDIO_33_S_1 N18
VDDIO_33_S_2 L19
VDDIO_33_S_3 M18
VDDIO_33_S_4 V12
VDDIO_33_S_5 V13
VDDIO_33_S_6 Y12
VDDIO_33_S_7 Y13
VDDIO_33_S_8 W11

3.3V_S5 I/O

VDDXL_33_S G24

VDDCR_11_S_1 N20
VDDCR_11_S_2 M20

VDDPL_11_SYS_S J24

VDDAN_33_HWM_S M8

VDDIO_AZ_S AA4

VDDAN_33_USB_S_1 G7
VDDAN_33_USB_S_2 H8
VDDAN_33_USB_S_3 J8
VDDAN_33_USB_S_4 K8
VDDAN_33_USB_S_5 K9
VDDAN_33_USB_S_6 M9
VDDAN_33_USB_S_7 M10
VDDAN_33_USB_S_8 N9
VDDAN_33_USB_S_9 N10
VDDAN_33_USB_S_10 M12
VDDAN_33_USB_S_11 N12
VDDAN_33_USB_S_12 M11

USB

VDDAN_11_USB_S_1 U12
VDDAN_11_USB_S_2 U13

VDDCR_11_USB_S_1 T12
VDDCR_11_USB_S_2 T13

VDDAN_11_SSUSB_S_1 P16
VDDAN_11_SSUSB_S_2 M14
VDDAN_11_SSUSB_S_3 N14
VDDAN_11_SSUSB_S_4 P13
VDDAN_11_SSUSB_S_5 P14

USB SS

VDDCR_11_SSUSB_S_1 N16
VDDCR_11_SSUSB_S_2 N17
VDDCR_11_SSUSB_S_3 P17
VDDCR_11_SSUSB_S_4 M17

POWER

HUDSON-M2_FCBGA656
@

U25E

HUDSON-2

VSS A3
VSS A33
VSS B7
VSS B13
VSS D9
VSS D13
VSS E5
VSS E12
VSS E16
VSS E29
VSS F7
VSS F9
VSS F11
VSS F13
VSS F16
VSS F17
VSS F19
VSS F23
VSS F25
VSS F29
VSS G6
VSS G16
VSS G32
VSS H12
VSS H15
VSS H29
VSS J6
VSS J9
VSS J10
VSS J13
VSS J28
VSS J32
VSS K7
VSS K16
VSS K27
VSS K28
VSS L6
VSS L12
VSS L13
VSS L15
VSS L16
VSS L21
VSS M13
VSS M16
VSS M21
VSS M25
VSS N6
VSS N11
VSS N13
VSS N23
VSS N24
VSS P12
VSS P18
VSS P20
VSS P21
VSS P31
VSS P33
VSS R4
VSS R11
VSS R25
VSS R28
VSS T11
VSS T16
VSS T18
VSS T25
VSS T27
VSS U6
VSS U14
VSS U17
VSS U20
VSS U21
VSS U30
VSS U32
VSS V11
VSS V16
VSS V18
VSS W4
VSS W6
VSS W25
VSS W28
VSS Y14
VSS Y16
VSS Y18
VSS AA6
VSS AA12
VSS AA13
VSS AA14
VSS AA16
VSS AA17
VSS AA25
VSS AA28
VSS AA30
VSS AA32
VSS AB25
VSS AC6
VSS AC18
VSS AC28
VSS AD27
VSS AE6
VSS AE15
VSS AE21
VSS AE28
VSS AF8
VSS AF12
VSS AF16
VSS AF33
VSS AG30
VSS AG32
VSS AH5
VSS AH11
VSS AH18
VSS AH19
VSS AH21
VSS AH23
VSS AH25
VSS AH27
VSS AJ18
VSS AJ28
VSS AJ29
VSS AK21
VSS AK25
VSS AL18
VSS AM21
VSS AM25
VSS AN1
VSS AN18
VSS AN28
VSS AN33

GROUND

VSSAN_HWM N8
VSSXL K25
VSSPL_SYS H25
VSSPL_DAC T21
VSSAN_DAC L28
VSSANQ_DAC K33
VSSIO_DAC N28
EFUSE R6

HUDSON-M2_FCBGA656
@

Connected to VSS through a dedicated via.

+3VS
L3 MBK1608221YZF_2P 220 ohm
+VDDPL_3.3V
C1222 2.2U_0603_6.3V4Z
C1223 .1U_0402_16V7K

+FCH_VDDAN_33_DAC_R
R19 0_0603_5%
+FCH_VDDPL_33_MLDAC
+3VS
@L4 MBK1608221YZF_2P 220 ohm
C1227 2.2U_0603_6.3V4Z
C1231 .1U_0402_16V7K

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI
@ C1232 2.2U_0603_6.3V4Z

+3VALW
M3@L6 MBK1608221YZF_2P 220 ohm
+FCH_VDDPL_33_SSUSB_S
C1238 2.2U_0603_6.3V4Z
M3@ C1239 .1U_0402_16V7K

+FCH_VDDAN_11_MLDAC
L24 MBK1608221YZF_2P 220 ohm/2A
R24 0_0402_5% 7mA
+VDDPL_11_DAC 10mils
+VDDAN_11_ML 20mils
R1148 0_0603_5% 226mA
C1240 4.7U_0603_6.3V6K
C1241 .1U_0402_16V7K
C1242 .1U_0402_16V7K

+VDDAN_33_USB
L7 MBK1608221YZF_2P 220 ohm
+FCH_VDDPL_33_USB_S
C1248 2.2U_0603_6.3V4Z
C1249 .1U_0402_16V7K

+3VS
L15 MBK1608221YZF_2P 220 ohm
+VDDPL_33_PCIE
C1258 2.2U_0603_6.3V4Z
C1259 .1U_0402_16V7K

+3VALW
L54 FBMA-L11-201209-221LMA30T_0805 220 ohm/2A 658mA
+VDDAN_33_USB 30mils
C1253 .1U_0402_6.3V6K
C1254 .1U_0402_6.3V6K
C1255 .1U_0402_16V7K
C1256 10U_0603_6.3V6M
C1257 .1U_0402_16V7K

+1.1VALW
L57 MBK1608221YZF_2P 220 ohm 140mA
+VDDAN_11_USB_S 10mils
C1262 2.2U_0603_6.3V4Z
C1263 .1U_0402_16V7K

+1.1VALW
L59 MBK1608221YZF_2P 220 ohm 197mA
+VDDCR_1.1V_USB 10mils
C1268 2.2U_0603_6.3V4Z
C1269 .1U_0402_16V7K
C1270 .1U_0402_16V7K

+3VS
L22 MBK1608221YZF_2P 220 ohm
+VDDPL_33_SATA
C1266 2.2U_0603_6.3V4Z
C1267 .1U_0402_16V7K

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.
M2@ C1275 0_0402_5%
M2@ C1281 0_0402_5%

+FCH_VDD_11_SSUSB_S
R1149 0_0603_5% 282mA
+VDDAN_SSUSB 20mils
C1273 .1U_0402_6.3V6K
C1274 .1U_0402_16V7K
C1275 .1U_0402_16V7K
40mils
+FCH_VDD_11_SSUSB_S
30mils

+1.1VALW
L61 M3@ FBMA-L11-201209-221LMA30T_0805 42 ohm/4A
R1150 0_0603_5% 424mA
+VDDCR_11_SSUSB
C1278 10U_0603_6.3V6M
C1279 .1U_0402_16V7K
C1280 .1U_0402_6.3V6K
C1281 .1U_0402_16V7K

+3VS
R20 0_0603_5% 131mA
+VDDIO_33_PCIGP 10mils
C1218 22U_0805_6.3V6M
C1228 .1U_0402_16V7K
C1220 .1U_0402_16V7K
C1221 .1U_0402_16V7K

+VDDPL_3.3V 47mA 10mils
+FCH_VDDPL_33_MLDAC 20mA
R22 0_0402_5% 20mA
+VDDPL_33_DAC 10mils
+VDDPL_33_ML 10mils
R23 0_0402_5% 200mA
+FCH_VDDAN_33_DAC_R
R936 M2@ 0_0402_5% 20mA
+FCH_VDDPL_33_SSUSB_S 10mils
+FCH_VDDPL_33_USB_S 17mA 10mils
+VDDPL_33_PCIE 43mA 10mils
+VDDPL_33_SATA 93mA 10mils

+VCC_FCH_R 1007mA
R937 0_0805_5% +1.1VS
50mils
C1213 1U_0402_6.3V6K
C1214 1U_0402_6.3V6K
C1215 .1U_0402_16V7K
C1216 .1U_0402_16V7K
C1217 2.2U_0603_6.3V4Z
C1219 22U_0805_6.3V6M

+1.1VS_CKVDD 340mA
R25 0_0603_5% +1.1VS
20mils
C1223 1U_0402_6.3V6K
C1224 1U_0402_6.3V6K
C1225 1U_0402_16V7K
C1226 1U_0402_16V7K
C1230 2.2U_0603_6.3V4Z

+PCIE_VDDR_FCH 1088mA
R938 0_0805_5% +1.1VS
50mils
C1233 1U_0402_6.3V6K
C1234 1U_0402_6.3V6K
C1235 1U_0402_16V7K
C1236 1U_0402_16V7K
C1237 2.2U_0603_6.3V4Z

+AVDD_SATA 1337mA
R941 0_0805_5% +1.1VS
60mils
C1243 1U_0402_6.3V6K
C1244 1U_0402_6.3V6K
C1245 1U_0402_16V7K
C1246 1U_0402_16V7K
C1247 22U_0805_6.3V6M

+VDDIO_33_S 59mA
R26 0_0402_5% +3VALW
10mils
C1250 1U_0402_16V7K
C1251
C1252 2.2U_0603_6.3V4Z

+VDDXL_3.3V 5mA
M3@ L28 MBK1608221YZF_2P +3VALW
M2@ L30 MBK1608221YZF_2P 220 ohm +3VS
10mils
C1260 1U_0402_16V7K
C1261 2.2U_0603_6.3V4Z

+VDDCR_1.1V 187mA
R1145 0_0603_5% +1.1VALW
10mils
C1264 1U_0402_6.3V6K
C1265 1U_0402_6.3V6K

SYSON <36,39,44>
@ Q13 BSH111 1N_SOT23-3

+VDDPL_1.1V 70mA
L29 MBK1608221YZF_2P +1.1VALW
@ L31 MBK1608221YZF_2P 220 ohm +1.1VS
10mils
C1271 2.2U_0603_6.3V4Z
C1272 1U_0402_16V7K

Q13 change to SB00000FG10 AOS3416
20110322

+VDDAN_33_HWM 12mA
R27 0_0402_5% +3VALW
10mils
C1472 2.2U_0603_6.3V4Z
C1473 1U_0402_16V7K

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

+VDDIO_AZ 26mA
R28 0_0402_5% +3VS
10mils
C1276 2.2U_0603_6.3V4Z
C1277 .1U_0402_16V7K

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

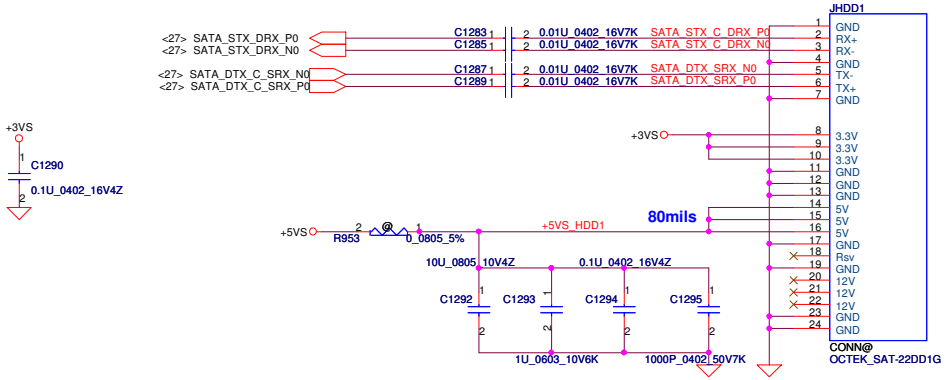
Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

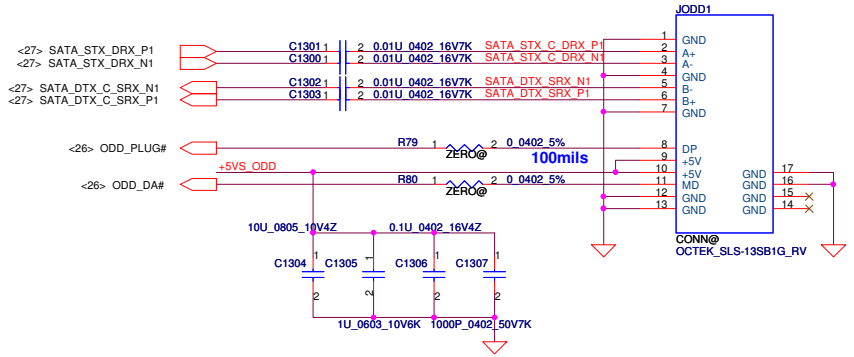
Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

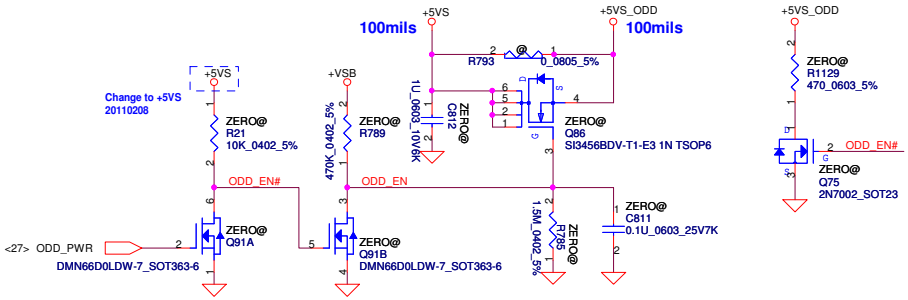
Date: Wednesday, April 20, 2011 Sheet 29 of 50

SATA HDD1 Conn. Fllow P5WE0

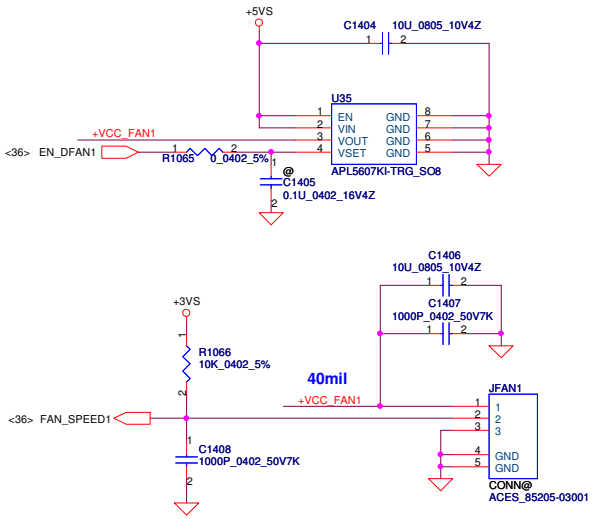


SATA ODD Conn. Fllow P5WE0

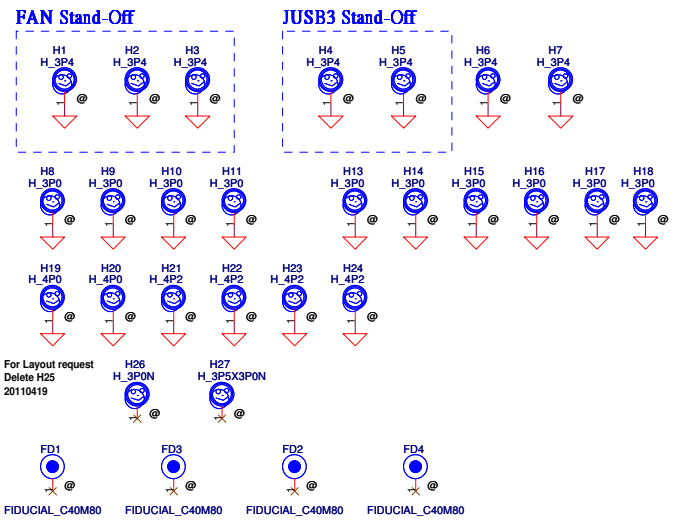




FAN



Screw Hole Fllow P5WE0



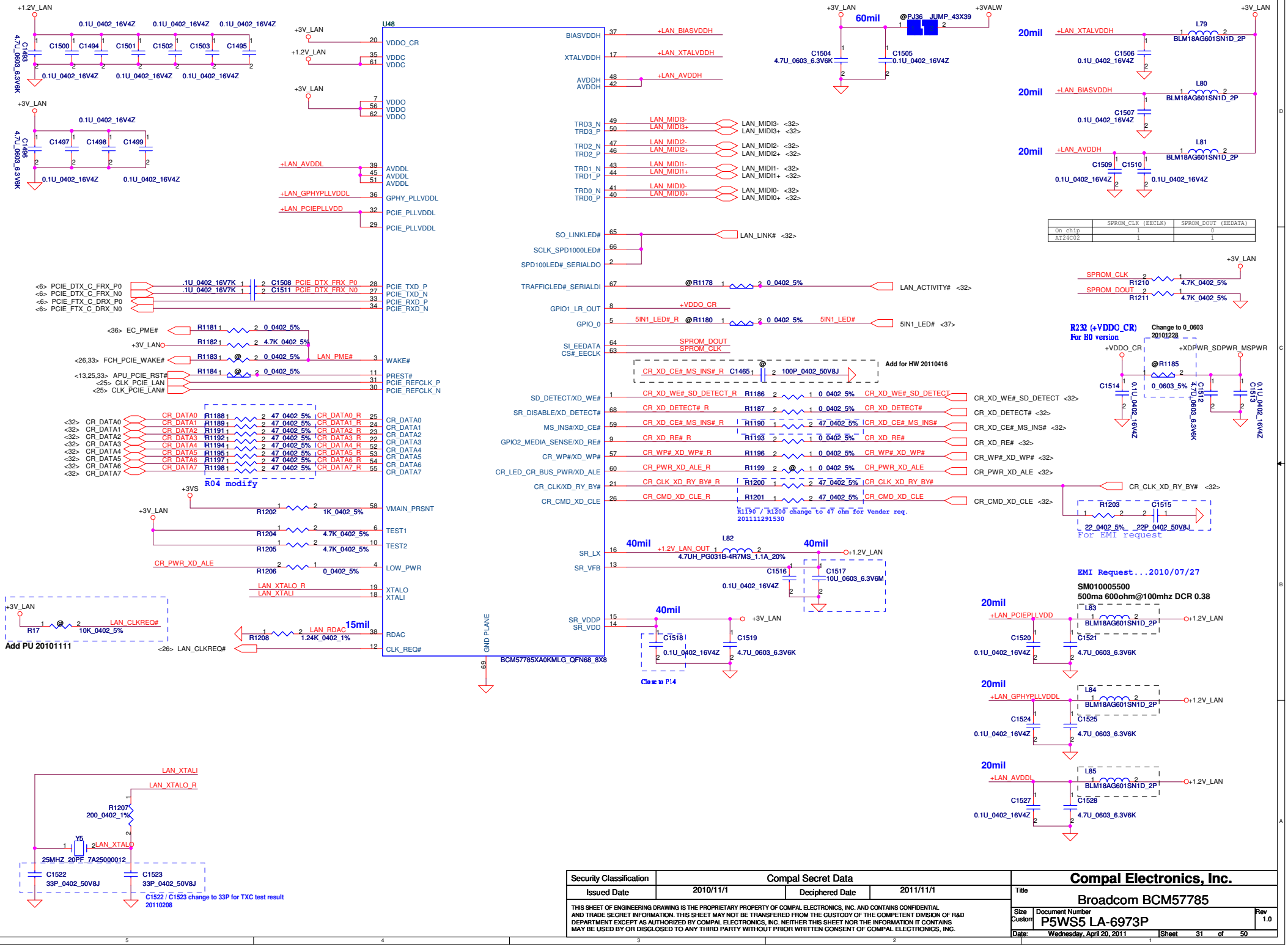
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: HDD/ODD/FAN/SCREW

Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 30 of 50


U48
BCM57785XA0KMLG_QFN68_8X8
+1.2V_LAN
+3V_LAN
+3VALW
VDDO_CR
VDDC
VDDO
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PREST#
PCIE_REFCLK_P
PCIE_REFCLK_N
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
VMAIN_PRSNT
TEST1
TEST2
LOW_PWR
XTALO
XTALI
RDAC
CLK_REQ#
BIASVDDH
XTALVDDH
AVDDH
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
SO_LINKLED#
SCLK_SPD1000LED#
SPD100LED#_SERIALDO
TRAFFICLED#_SERIALDI
GPIO1_LR_OUT
GPIO_0
SI_EEDATA
CS#_EECLK
SD_DETECT/XD_WE#
SR_DISABLE/XD_DETECT#
MS_INS#/XD_CE#
GPIO2_MEDIA_SENSE/XD_RE#
CR_WP#/XD_WP#
CR_LED_CR_BUS_PWR/XD_ALE
CR_CLK/XD_RY_BY#
CR_CMD_XD_CLE
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND PLANE
+LAN_BIASVDDH
+LAN_XTALVDDH
+LAN_AVDDH
LAN_MIDI3-
LAN_MIDI3+
LAN_MIDI2-
LAN_MIDI2+
LAN_MIDI1-
LAN_MIDI1+
LAN_MIDI0-
LAN_MIDI0+
LAN_LINK# <32>
LAN_ACTIVITY# <32>
5IN1_LED# <37>
SPROM_DOUT
SPROM_CLK
CR_XD_CE#_MS_INS#_R C1465 100P_0402_50V8J
Add for HW 20110416
CR_XD_WE#_SD_DETECT_R R1186 0_0402_5%
CR_XD_DETECT#_R R1187 0_0402_5%
CR_XD_CE#_MS_INS#_R R1190 47_0402_5%
CR_XD_RE#_R R1193 0_0402_5%
CR_WP#_XD_WP#_R R1196 0_0402_5%
CR_PWR_XD_ALE_R R1199 0_0402_5%
CR_CLK_XD_RY_BY#_R R1200 47_0402_5%
CR_CMD_XD_CLE_R R1201 47_0402_5%
R1190 / R1200 change to 47 ohm for Vender req.
20111291530
R232 (+VDDO_CR)
For B0 version
Change to 0_0603
20101228
+VDDO_CR
+XDPWR_SDPWR_MSPWR
R1185 0_0603_5%
For EMI request
EMI Request...2010/07/27
SM010005500
500ma 600ohm@100mhz DCR 0.38
L79 BLM18AG601SN1D_2P
L80 BLM18AG601SN1D_2P
L81 BLM18AG601SN1D_2P
L82 4.7UH_PG031B-4R7MS_1.1A_20%
L83 BLM18AG601SN1D_2P
L84 BLM18AG601SN1D_2P
L85 BLM18AG601SN1D_2P
+1.2V_LAN_OUT
+1.2V_LAN
+LAN_PCIEPLLVDD
+LAN_GPHYPLLVDDL
+LAN_AVDDL
SPROM_CLK R1210 4.7K_0402_5%
SPROM_DOUT R1211 4.7K_0402_5%
On chip | 1 | 0
AT24C02 | 1 | 1
LAN_XTALI
LAN_XTALO_R
R1207 200_0402_1%
Y5 25MHZ_20PF_7A25000012
C1522 33P_0402_50V8J
C1523 33P_0402_50V8J
C1522 / C1523 change to 33P for TXC test result
20110208
Add PU 20101111
R04 modify
Close to P14
Security Classification | Compal Secret Data
Issued Date | 2010/11/1 | Deciphered Date | 2011/11/1
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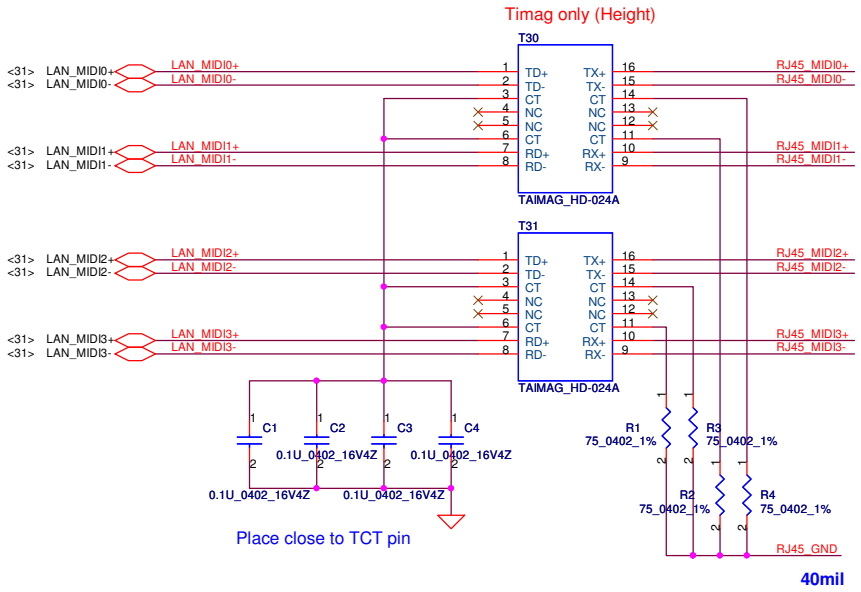
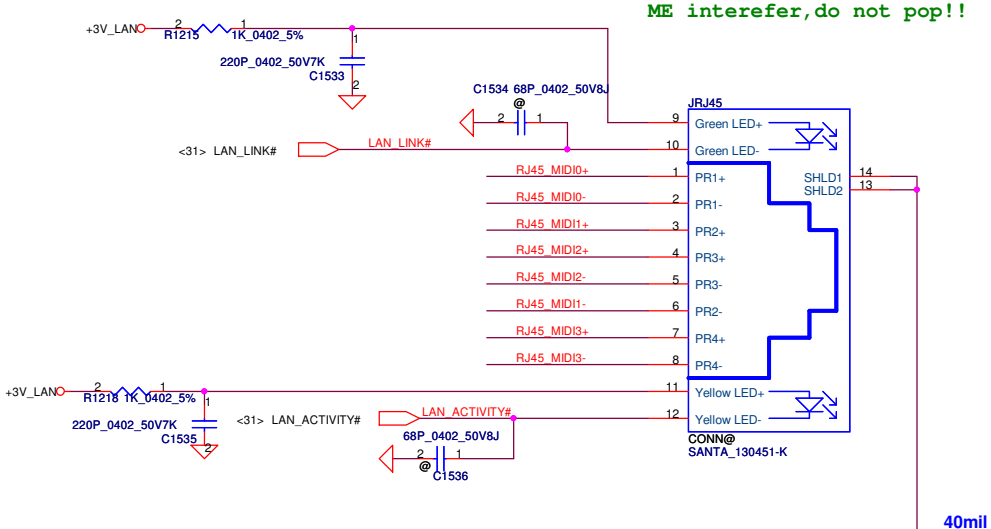
Compal Electronics, Inc.
Title: Broadcom BCM57785
Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0
Date: Wednesday, April 20, 2011 | Sheet 31 of 50



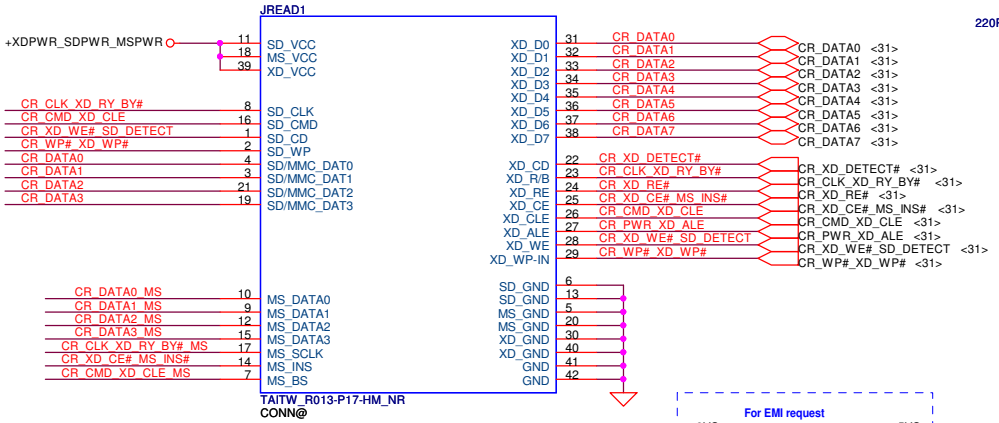
LAN Connector

R03 modify

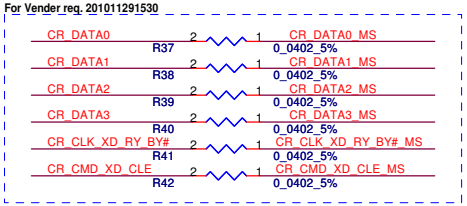
C474,C475 and D14
ME interefer,do not pop!!

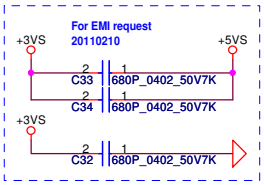


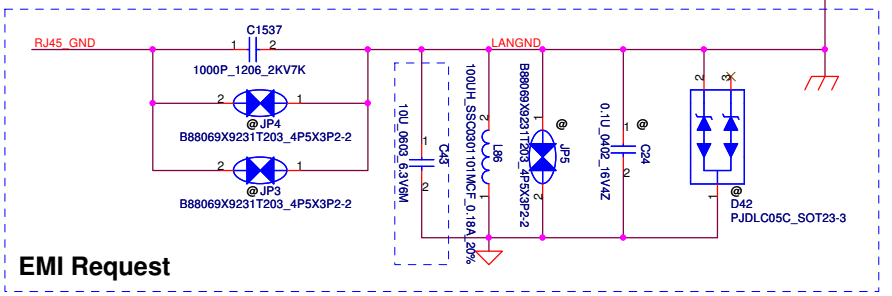
Card Reader Connector



For Vender req. 201011291530







Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

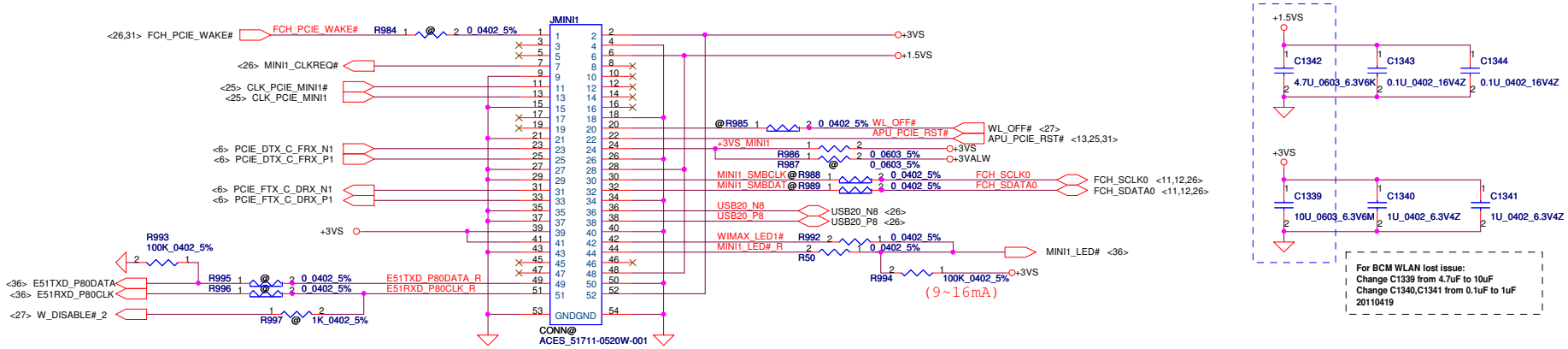
Date: Wednesday, April 20, 2011 | Sheet 32 of 50

Mini-Express Card for WLAN

Follow P5WE0

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

TOP View - Right



Remove MINI2

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

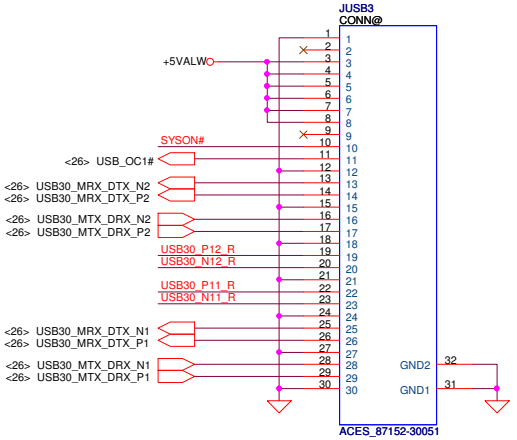
Title: MINI1 CARD (WLAN) / MINI2 CARD (Option)

Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 33 of 50

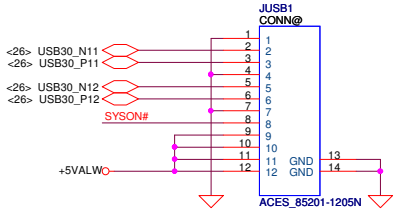
30 Pin USB30/B Conn

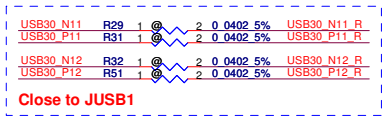
Change to Zif Conn. (SP010015Z00)
20101229

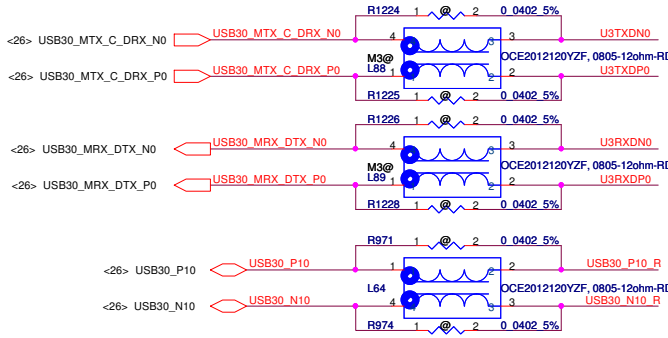


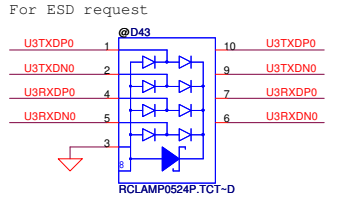
12 Pin USB20/B Conn

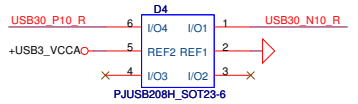
(Port 11 , 12)

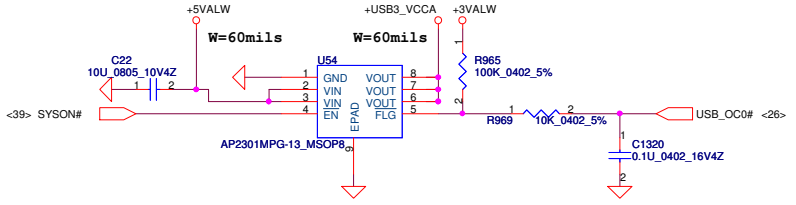


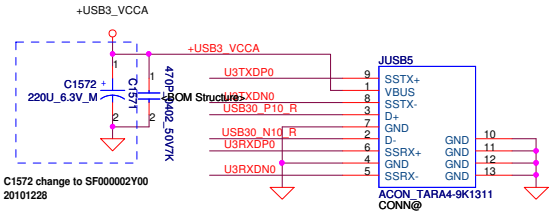












Security Classification	Compal Secret Data		
Issued Date	2010/08/27	Deciphered Date	2011/08/11

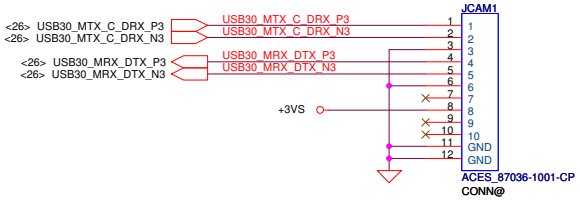
Compal Electronics, Inc.

Title: USB2.0 / USB3.0

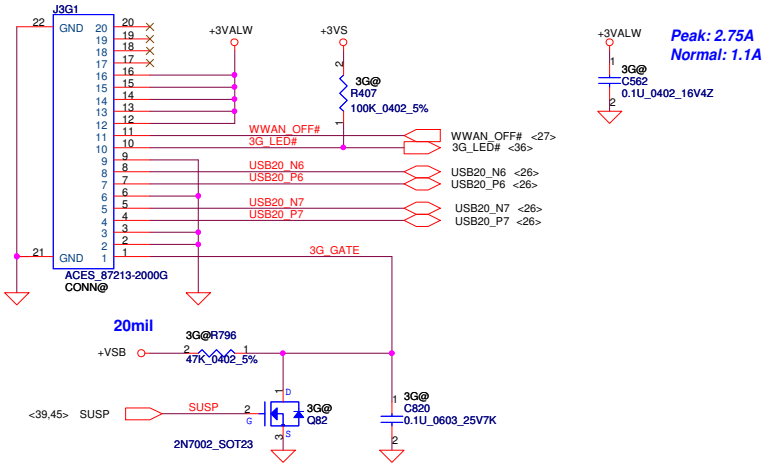
Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 34 of 50

For HD Camrea

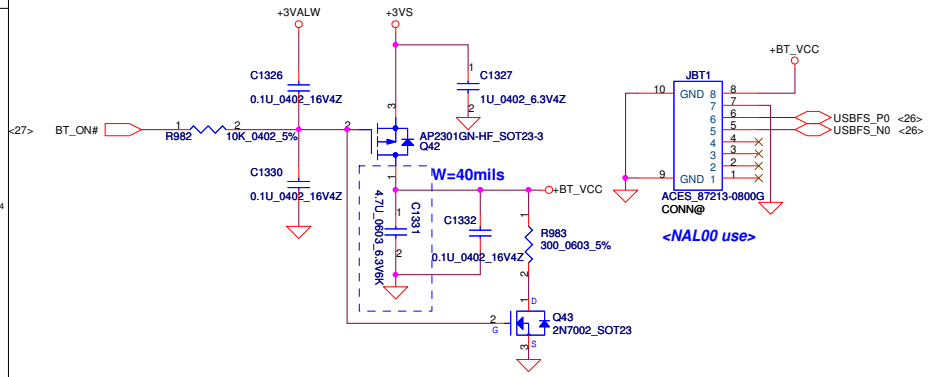


For 3G / GPS



Peak: 2.75A
Normal: 1.1A

Bluetooth Conn. Follow P5WE0



<NAL00 use>

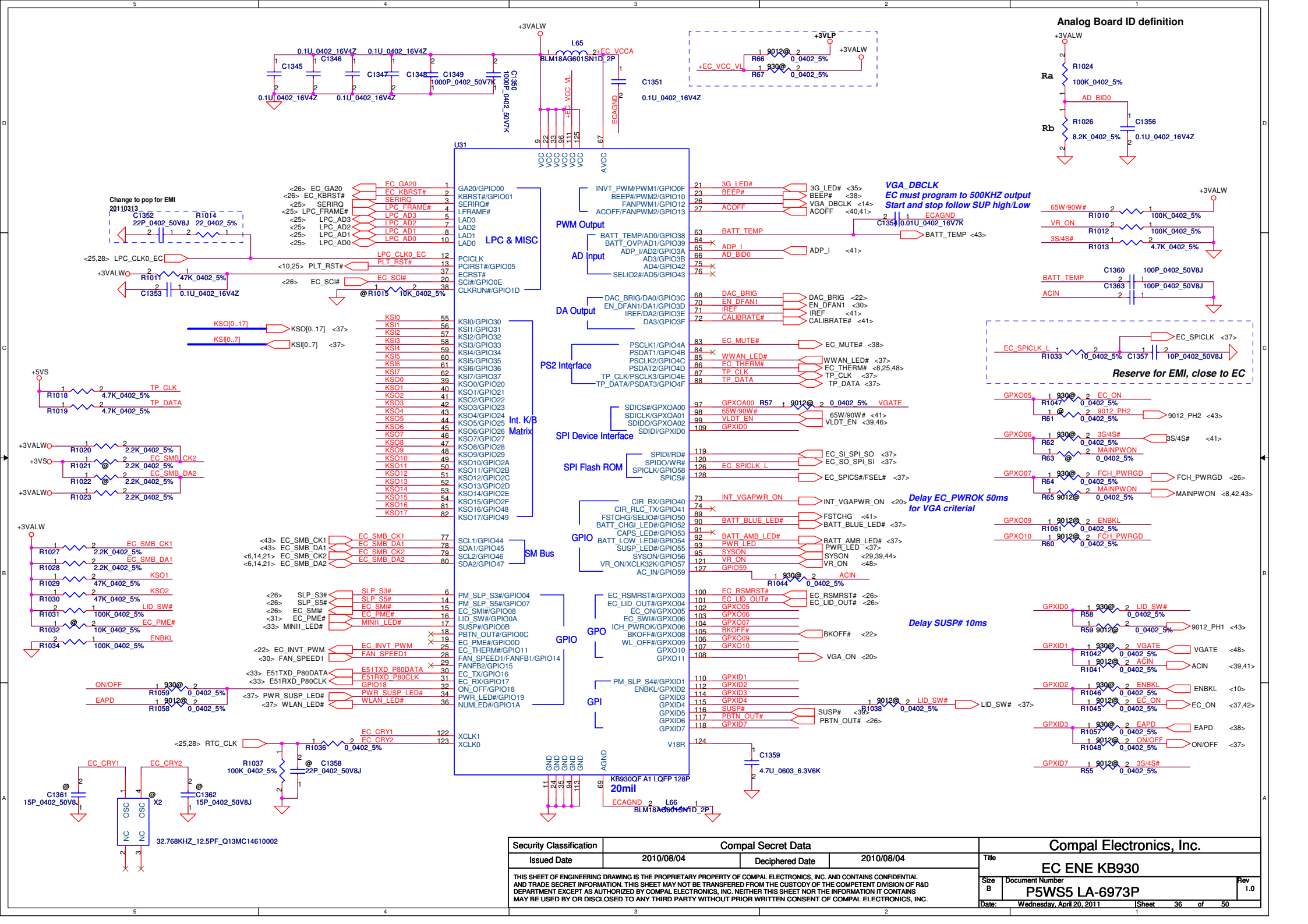
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

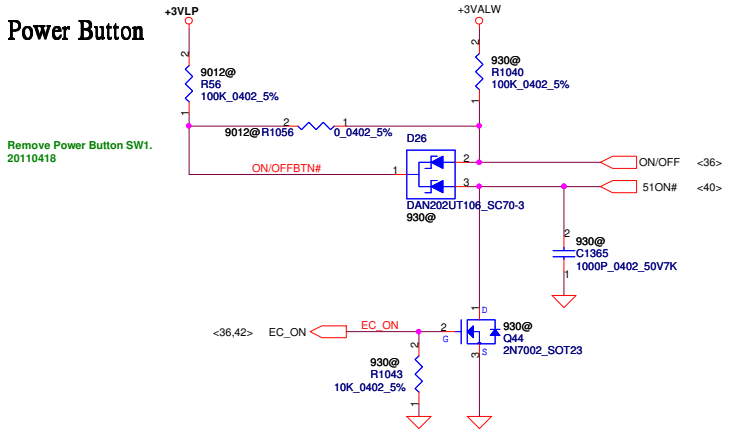
Title: USB2.0/3.0 CONN/USB/B CONN/LAN CONN

Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

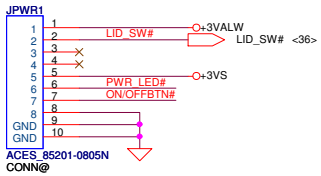
Date: Wednesday, April 20, 2011 | Sheet 35 of 50


Analog Board ID definition
Ra
Rb
R1024 100K_0402_5%
R1026 8.2K_0402_5%
AD_BID0
C1356 0.1U_0402_16V4Z
U31
KB930QF A1 LQFP 128P
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
VGA_DBCLK
EC must program to 500KHZ output
Start and stop follow SUP high/Low
Reserve for EMI, close to EC
Delay EC_PWROK 50ms for VGA criterial
Delay SUSP# 10ms
Change to pop for EMI 20110313
32.768KHZ_12.5PF_Q13MC14610002
Security Classification
Compal Secret Data
Issued Date
2010/08/04
Deciphered Date
2010/08/04
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC ENE KB930
Size B
Document Number
P5WS5 LA-6973P
Rev 1.0
Date: Wednesday, April 20, 2011
Sheet 36 of 50

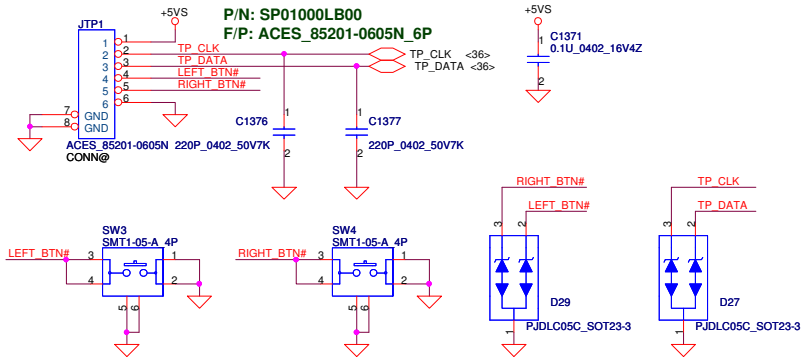
Power Button



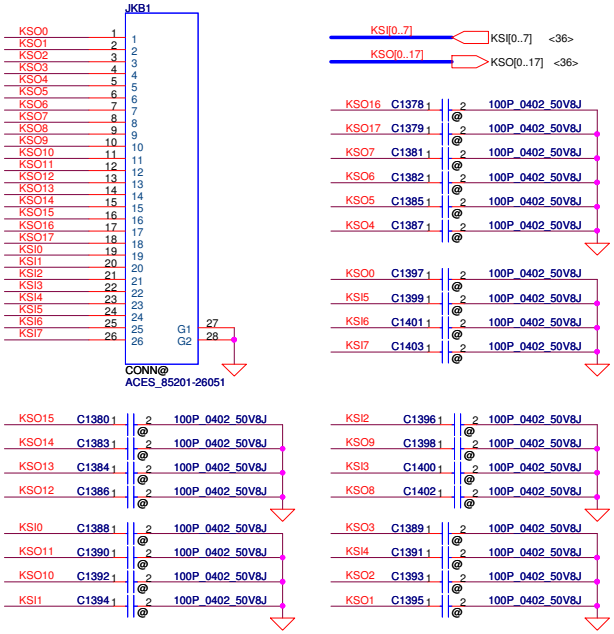
POWER/B Fllow P5WE0



TP Conn. Fllow P5WE0



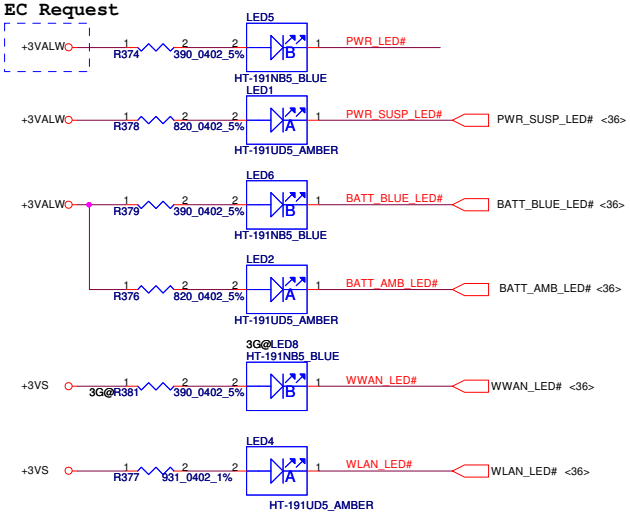
KB Conn. Fllow P5WE0

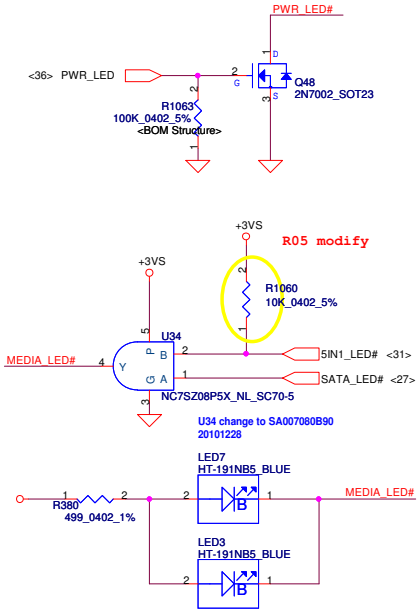


LED Fllow P5WE0

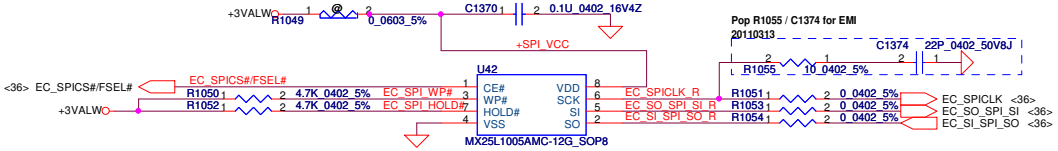
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

EC Request





EC BIOS ROM



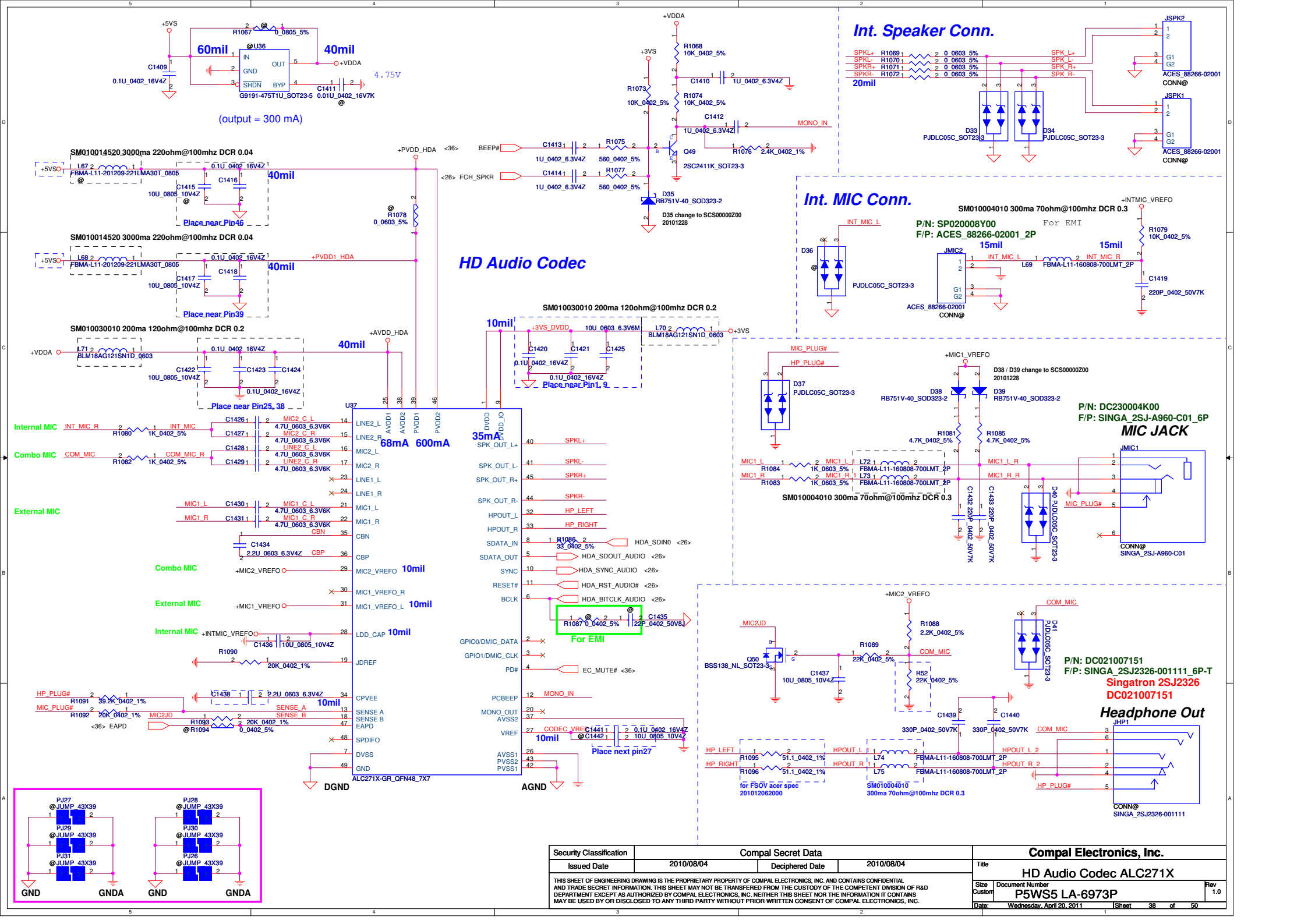
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B CONN/TP CONN/PBTN

Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 37 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

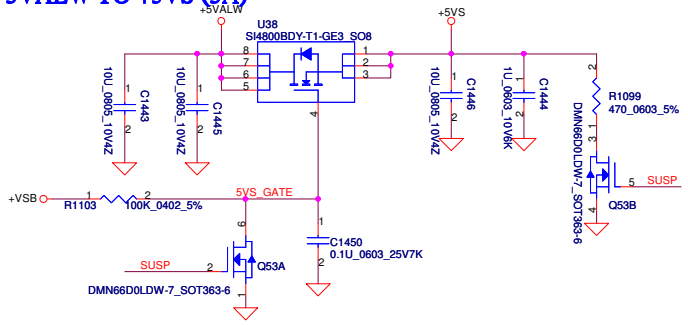
Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

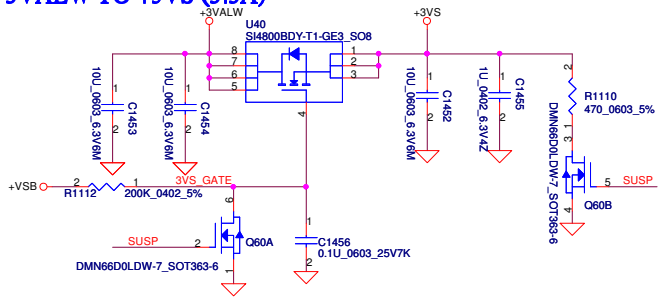
Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 | Sheet 38 of 50

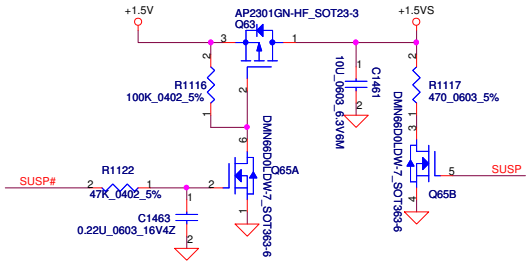
+5VALW TO +5VS (5A)

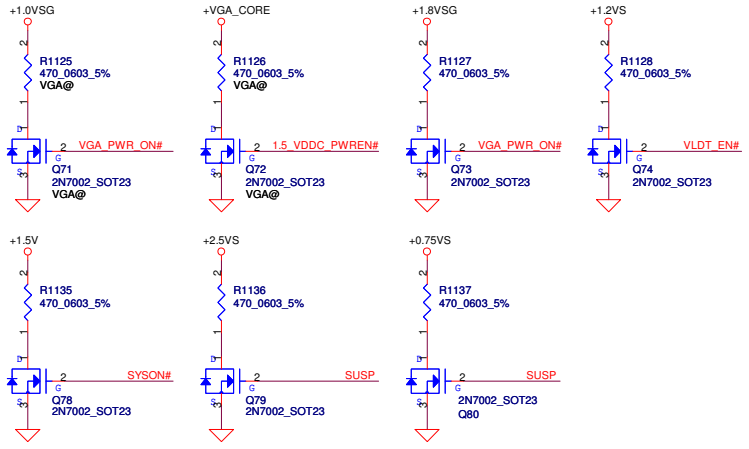


+3VALW TO +3VS (3.3A)

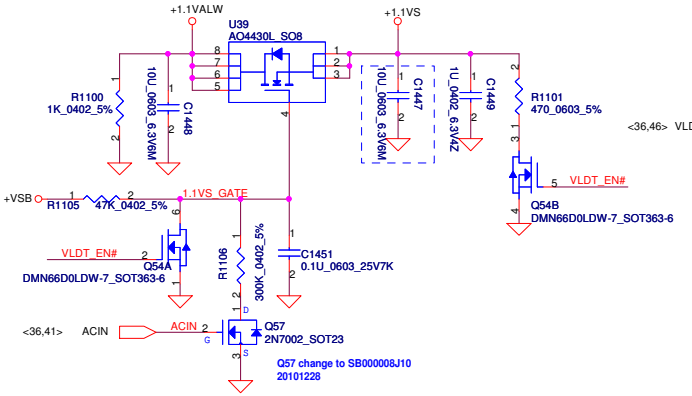


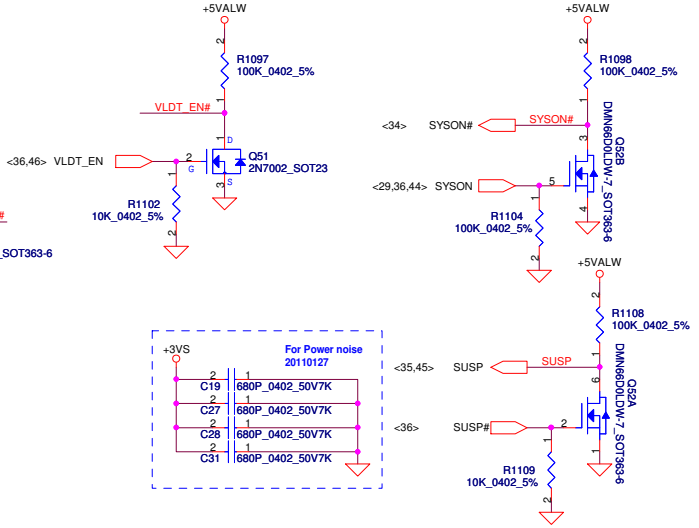
+1.5V TO +1.5VS (1.5A)





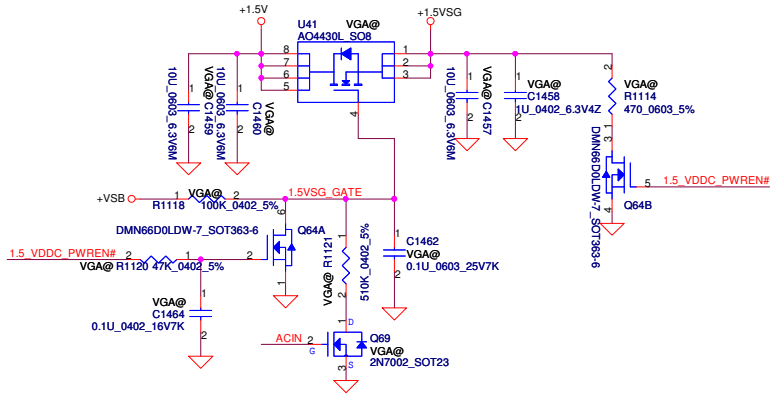
+1.1VALW TO +1.1VS (1.1A)



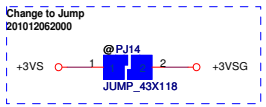


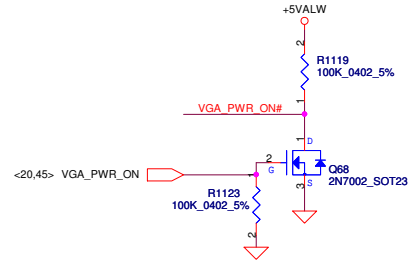
VGA Power

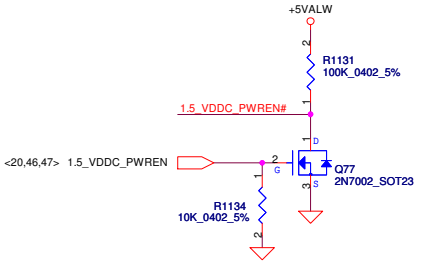
+1.5V to +1.5VSG (1.5A)



+3VS to +3VSG (3.3A)







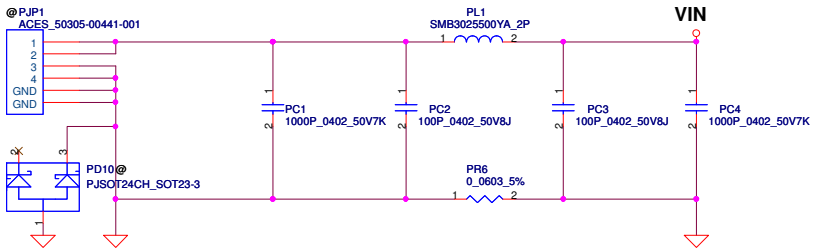
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

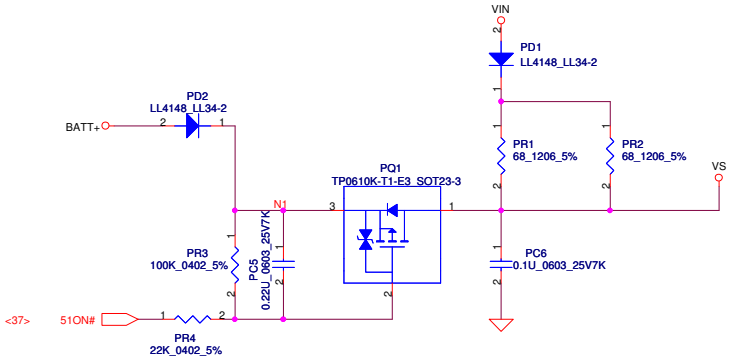
Compal Electronics, Inc.

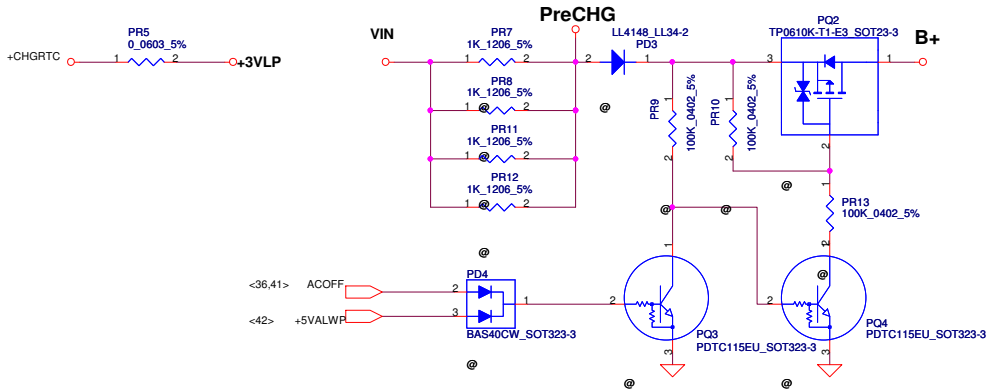
Title: DC Interface

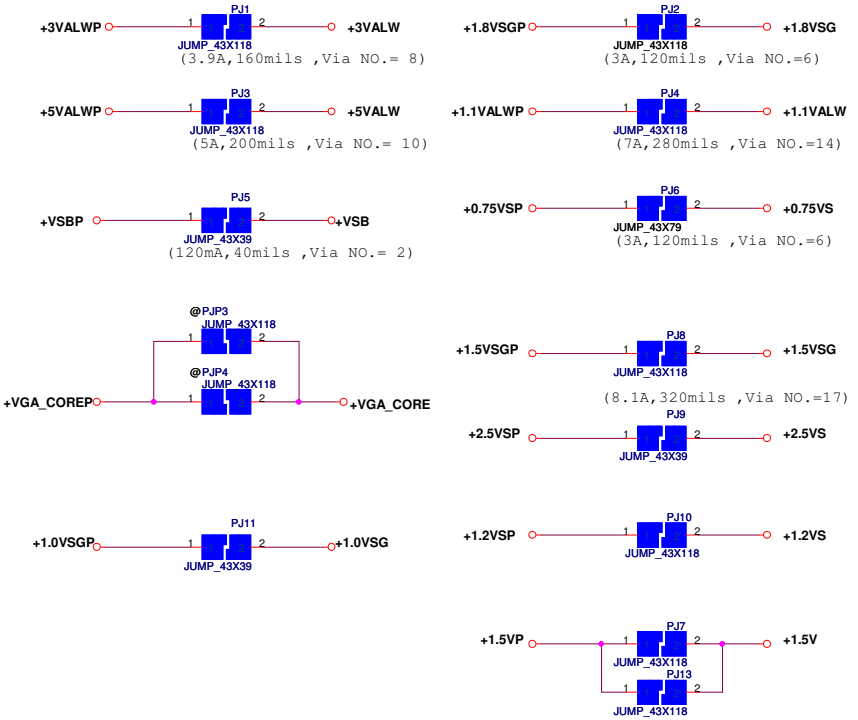
Size	Document Number	Rev
B	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 39 of 50









Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

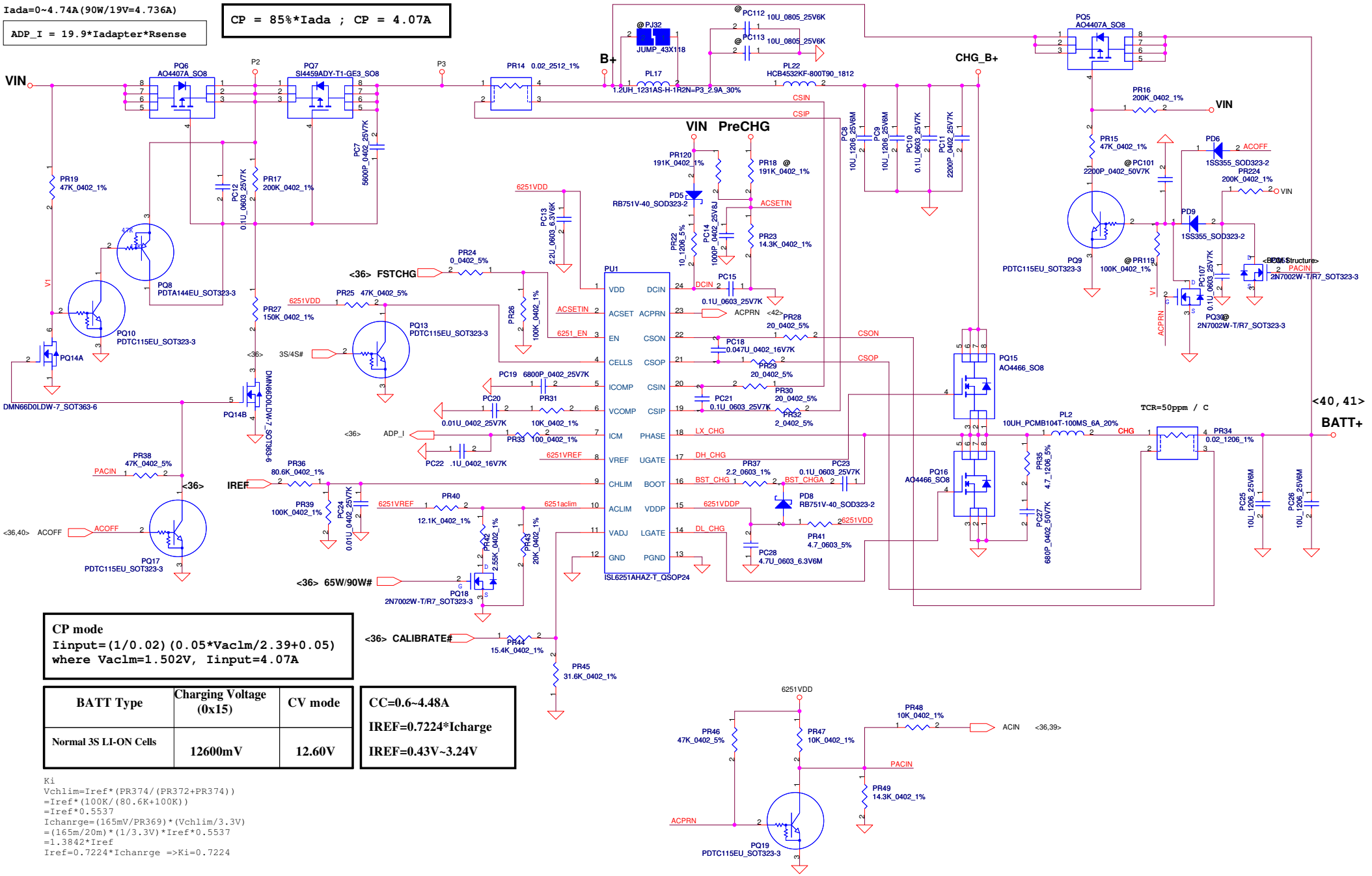
Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 40 of 50

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki

Vchlim=Iref*(PR374/(PR372+PR374))

=Iref*(100K/(80.6K+100K))

=Iref*0.5537

Ichanrge=(165mV/PR369)*(Vchlim/3.3V)

=(165m/20m)*(1/3.3V)*Iref*0.5537

=1.3842*Iref

Iref=0.7224*Ichanrge =>Ki=0.7224

Kv

Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K

R=514K//31.6K//(15.4K+3k)=11.372K

r=514K//514K//31.6K=28.14K

Vcell=0.175*Vadj+3.99v

4.2V=0.175*Vadj+3.99V =>Vadj=1.2V

Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))

1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899

1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv

A=Vref*(R/(R+514K))=0.052

Kv=9.451

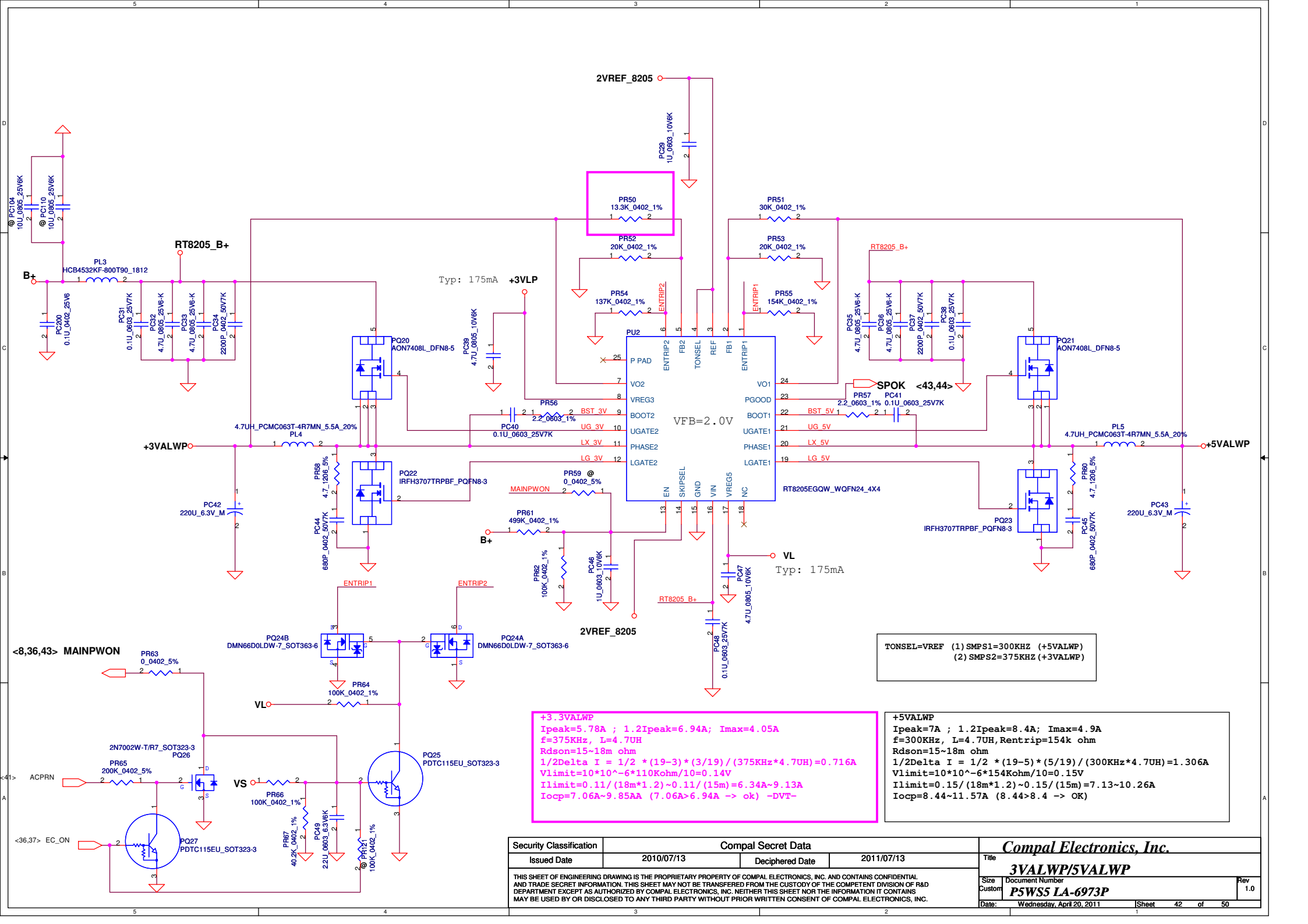
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

Date: Wednesday, April 20, 2011 | Sheet 41 of 50



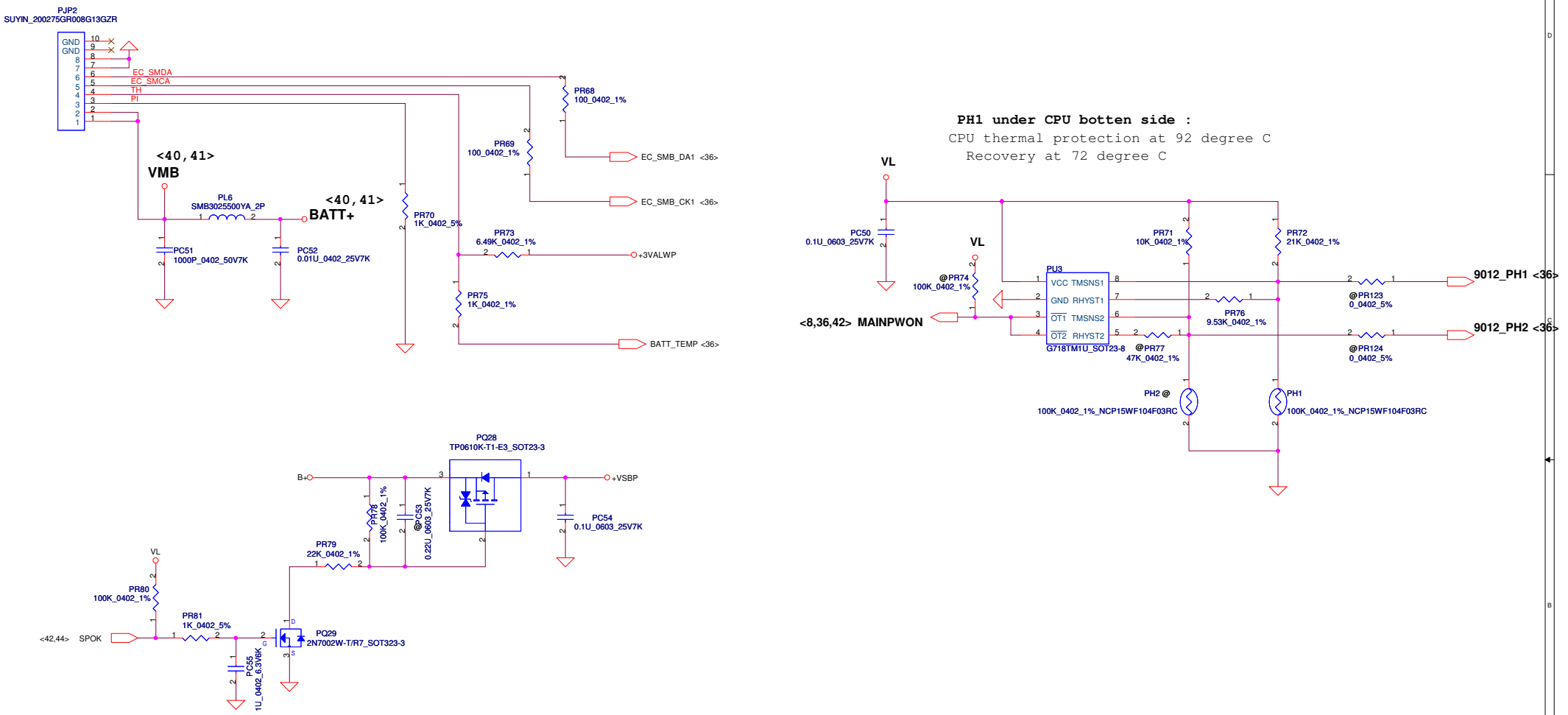
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

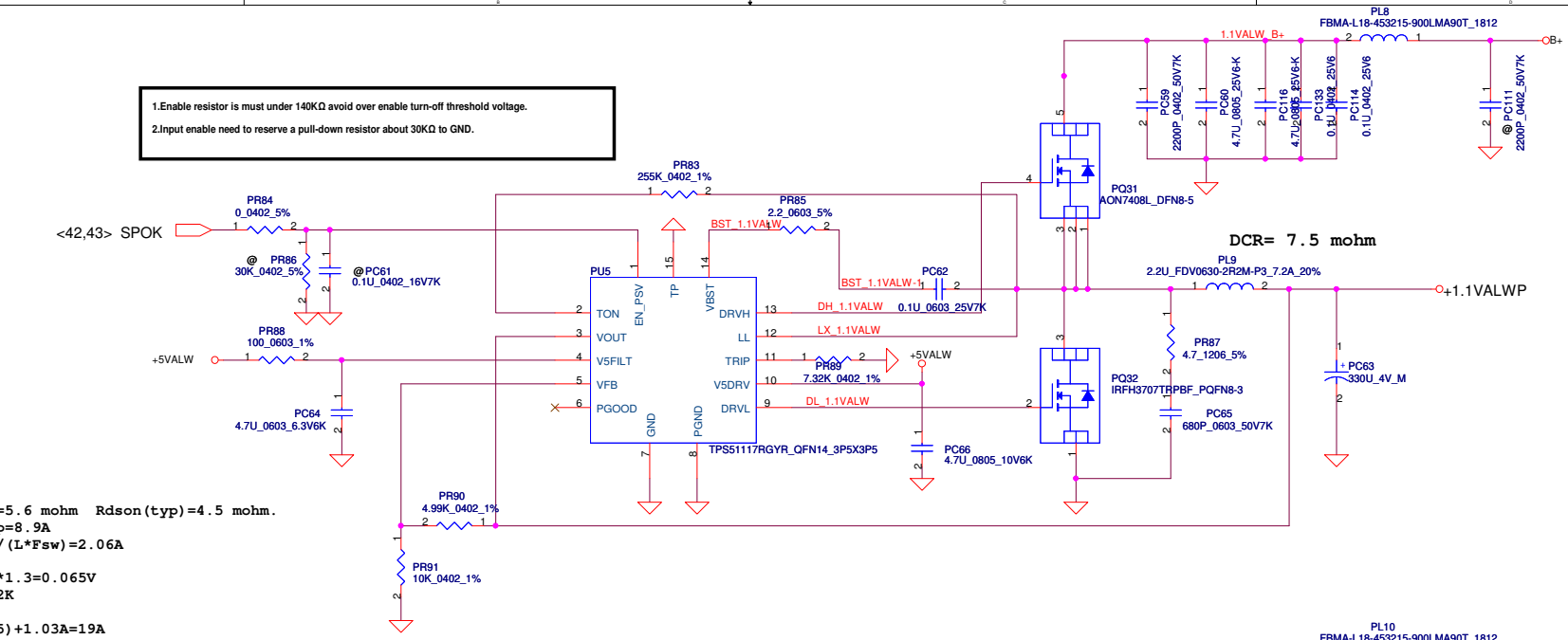
Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

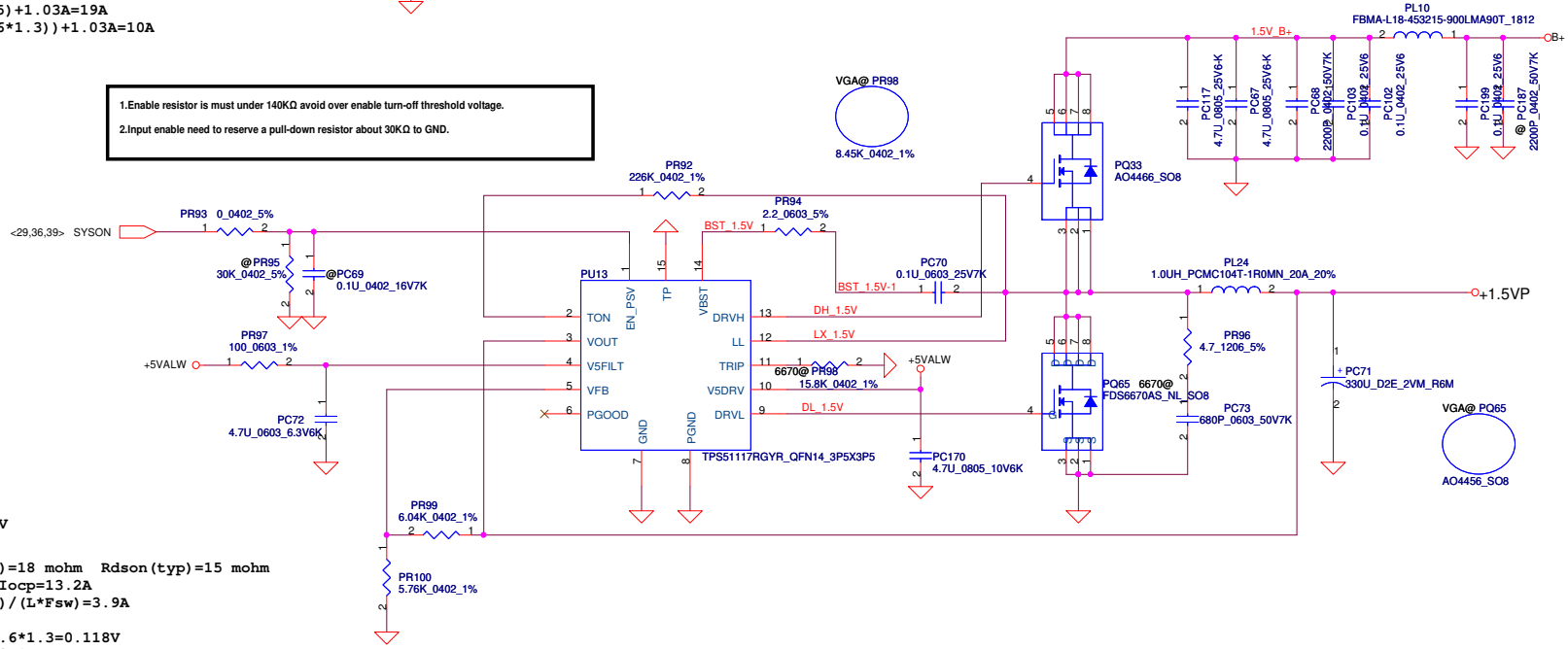
Date: Wednesday, April 20, 2011 | Sheet 42 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

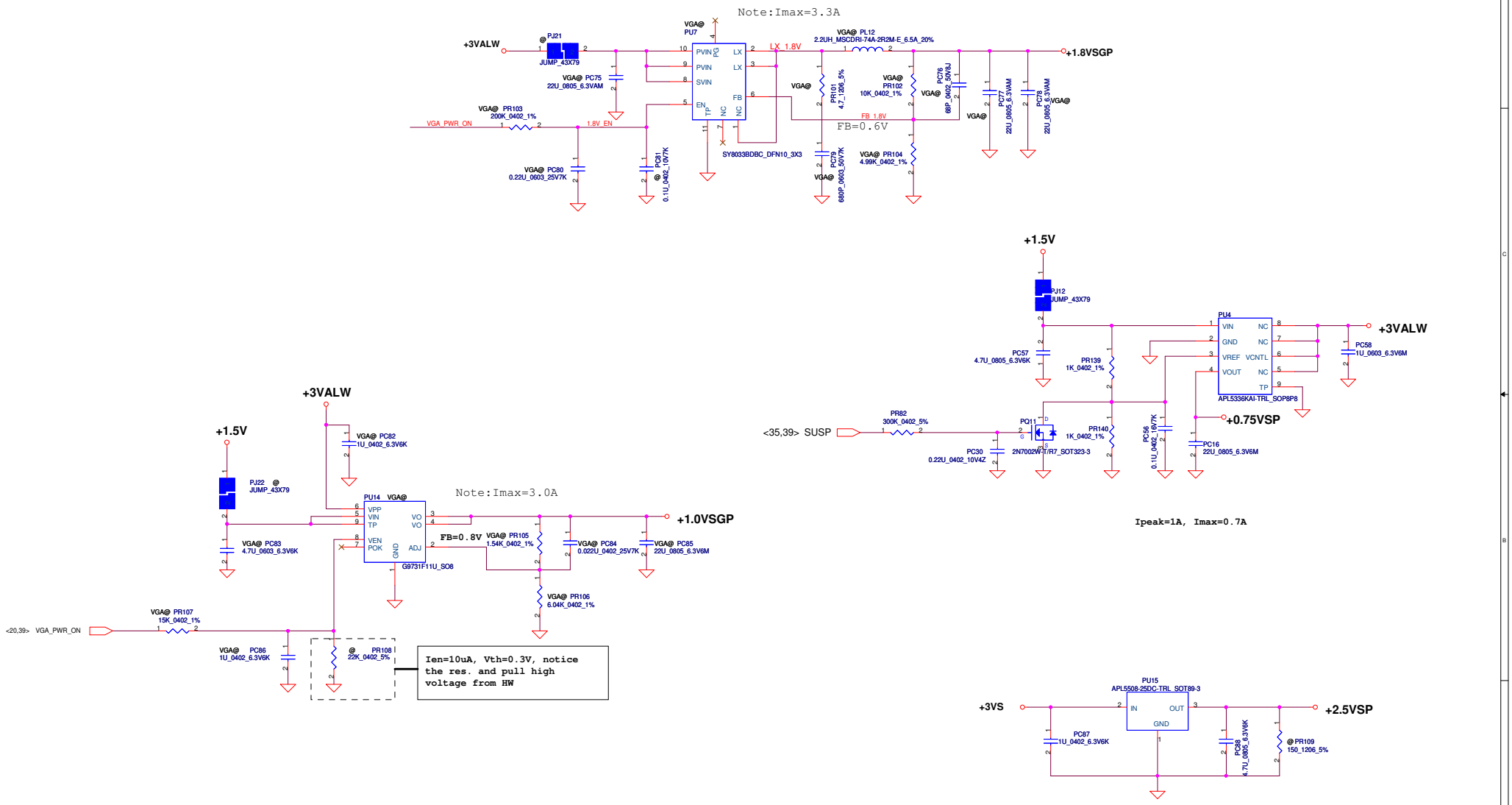
Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: P5WS5 LA-6973P		Rev: 1.0
Date: Wednesday, April 20, 2011	Sheet 43 of 50		





Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

Compal Electronics, Inc.			
Title	1.1VALWP/1.5VP		
Size	Document Number		Rev
Custom	P5WS5 LA-6973P		1.0
Date:	Wednesday, April 20, 2011	Sheet	44 of 50



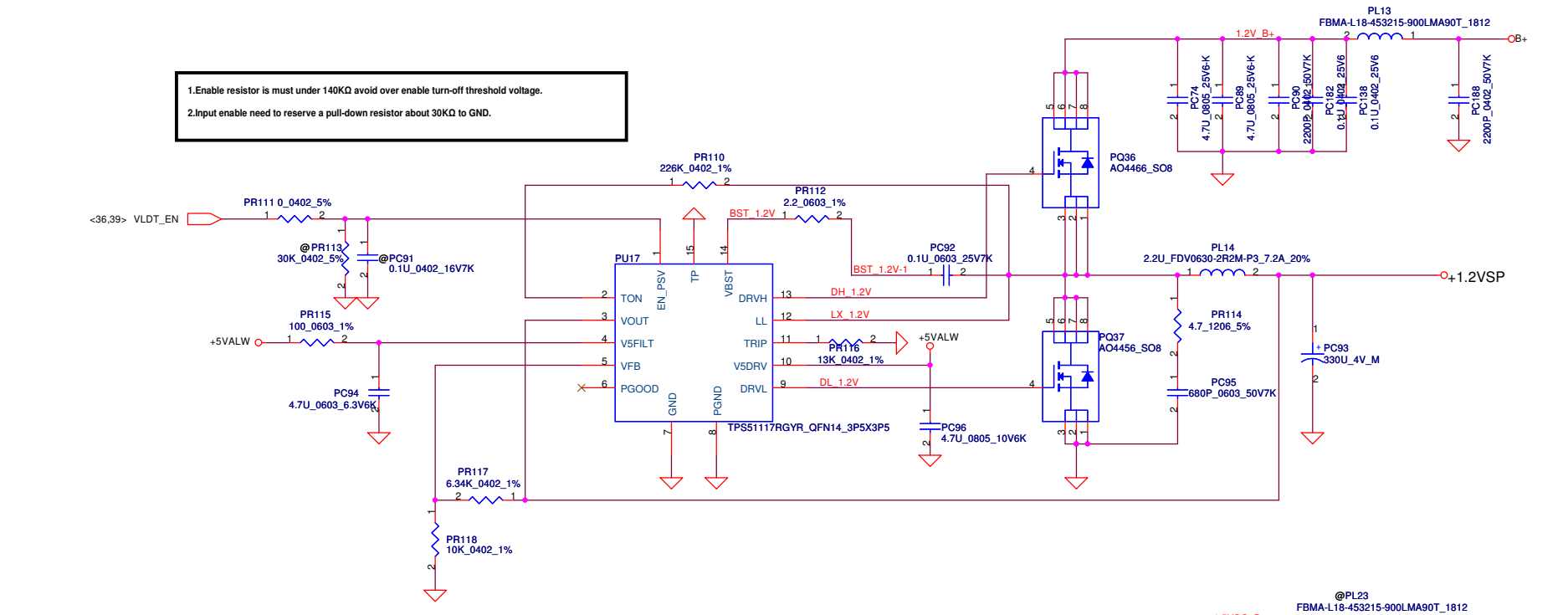
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **+1.8VSGP/+1.0VSGP/+2.5VSP/+0.75V**

Size	Document Number	Rev
C		1.0

Date: Wednesday, April 20, 2011 | Sheet 45 of 50



<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=335KHz

Cout ESR=17 mohm Rdson(max)=18 mohm Rdson(typ)=15 mohm
Ipeak=27.7A, Imax=19.39A, Iocp=13.2A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=9.94A~13.2A

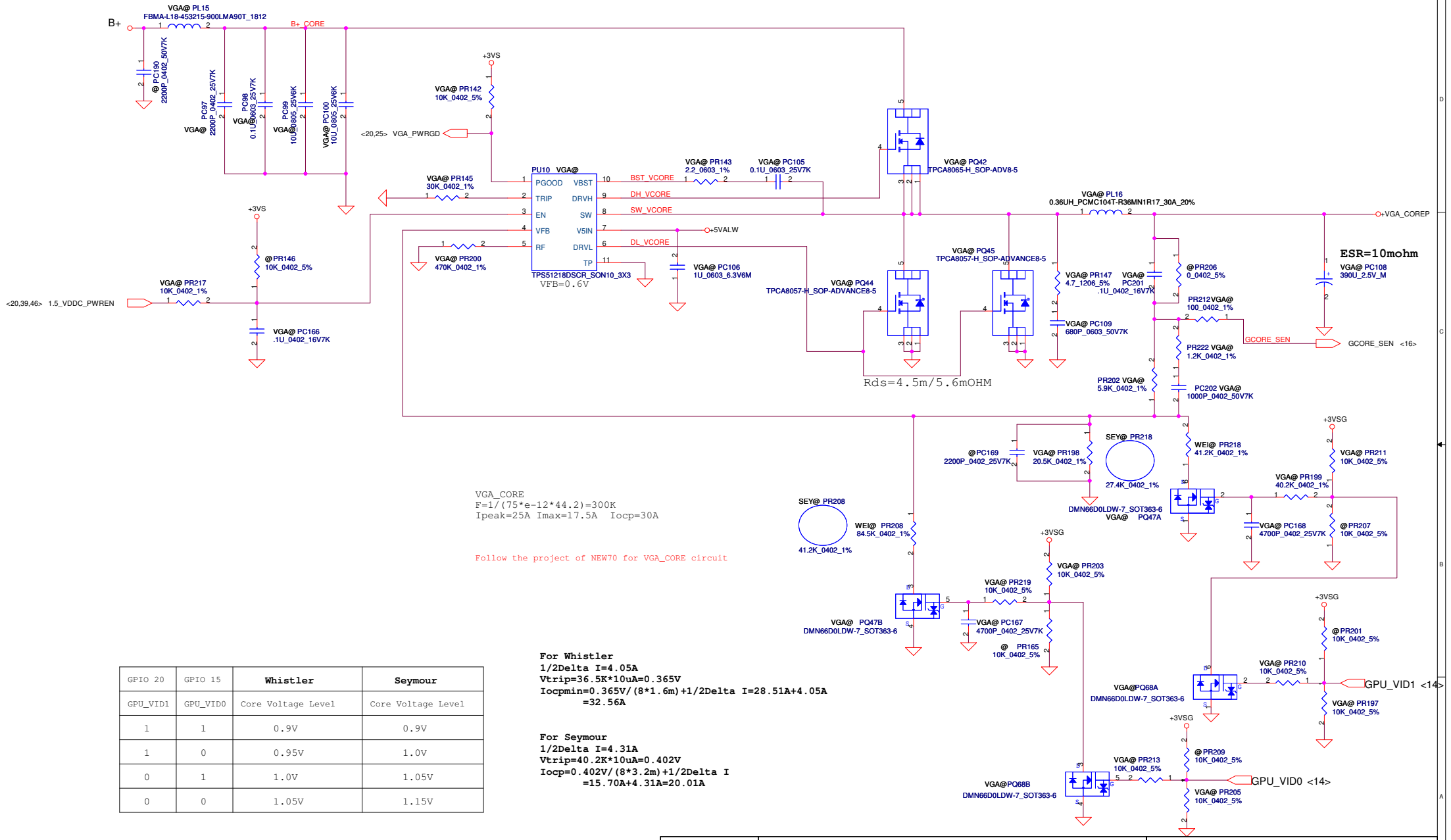
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

Compal Electronics, Inc.

Title: +1.2VSP/+1.5VSGP

Size	Document Number	Rev
Custom	P5WS5 LA-6973P	1.0

Date: Wednesday, April 20, 2011 Sheet 46 of 50



GPIO 20	GPIO 15	Whistler	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.9V	0.9V
1	0	0.95V	1.0V
0	1	1.0V	1.05V
0	0	1.05V	1.15V

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

Security Classification	Compal Secret Data		AP
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: **+VGA_COREP**

Size	Document Number	Rev
Custom	P5WE0	1.0

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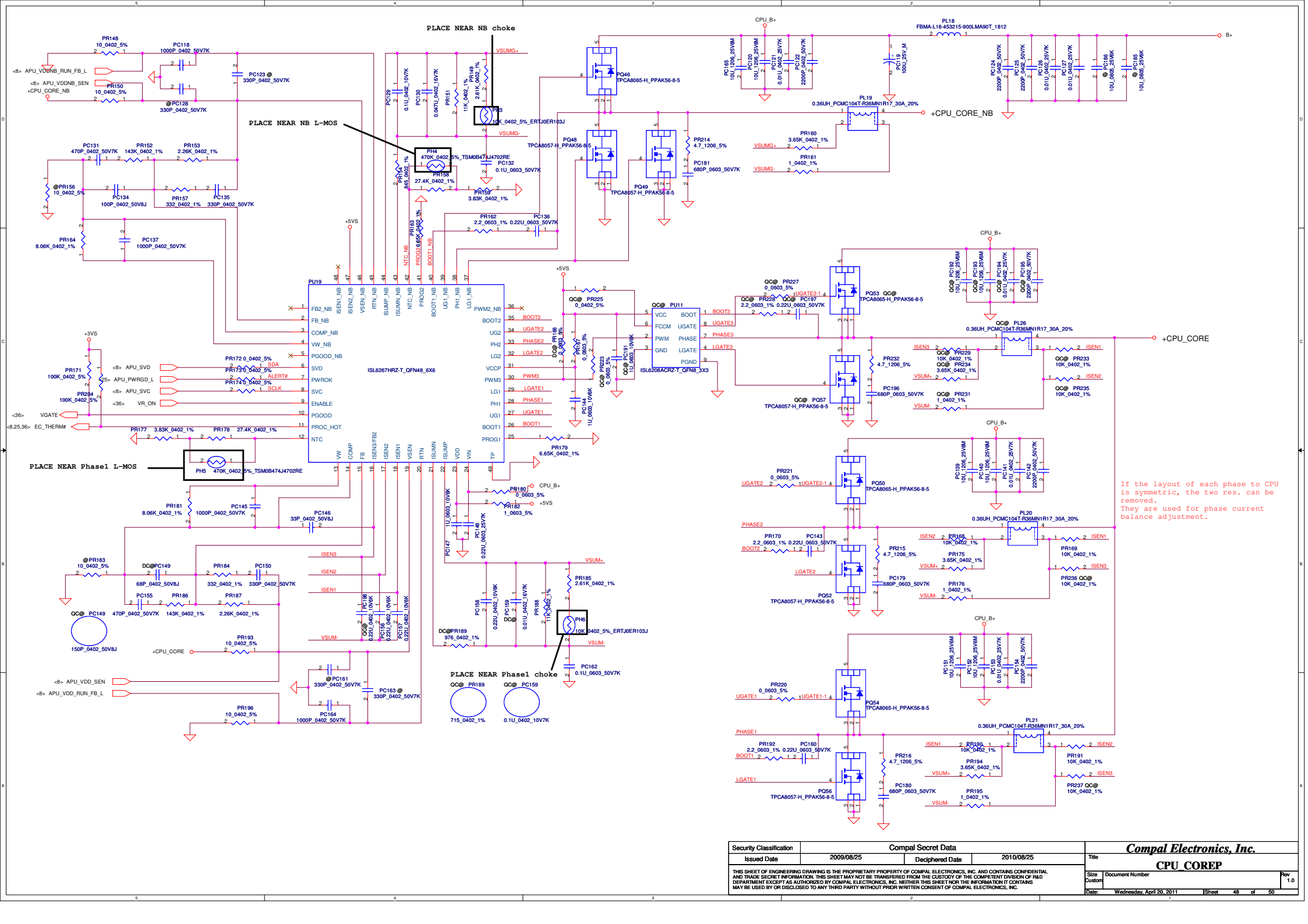

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: CPU_COREP

Size	Document Number	Rev
Custom		1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: P5WS5 LA-6973P | Rev: 1.0

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Version change list (P.I.R. List)

EVT Stage

20101124
1. C5 Change to D2 type
2. JDIMM1 Change to SUYIN
20101125
1. Del R1223 (P.34)
2. Del R1107 / R1111 / Q58 (P.39)
3. Del R1179 (P.31)
4. Update Power SCH
5. Add R33 / R34 (P.21)
20101126
1. Update Power SCH
20101129
1. Remove EC debug conn.
2. Add R35 / R36 / C23 for EMI
3. Add R37 / R38 / R39 / R40 / R41 / R42 for Vender req.
4. R1190 / R1200 change to 47 ohm ro Vender req.
20101130
1. Add Project ID R43 / R44 / R45 / R46 / R47 / R48
2. Add R50 for MINI Card option
3. Add C25 / U3 / R51 for SW req.
20101201
1. Del T4 / T5
2. Add NEC_USB30_PWR_EN FOR SW req.
20101202
1. Del D41.
20101203
1. Change APU HDMI Port to PEG12~PEG15 for AMD req.
20101206
1. Del C1039.
2. Add R52 for Vender req.
3. R1095 / R1096 change to 51.5 0402 for FSOV acer spec.
4. Del R469.
5. Add R53 for EMI req.
20101207
1. Update Power SCH.
2. Update USB30 Conn.
20101214
1. Remove R990 / R991 / R1004 / R1005
2. Remove R852
20101216
1. No any change , for gerber release .
20101221
1. Modify VGA 16X BOM structure.
20101225
1. Update Power SCH.
20101227
1. MINI2 USB port change to Port 0.
20101228
1. Del C27 / C28 / C35 / C36 and move to USB30/B.
2. Change MINI1 / MINI2 / GIGA LAN CLK ports.
3. JUSB3 change to Zif Conn.
20110106
1. Unpop SW1.
20110107
1. Update MB P/N.

DVT Stage

20110124
1. Unpop R997 / R49 for +3VS leakage current.
2. Unpop R1113 / R1115 / R122 / R123 / Q62 / Q89 for VGA power sequence.
3. R119 10K change to 22K 1% for VGA power sequence.
4. Add Q30 for FCH VDDAN_11_CLK leakage current.
5. Add R21 / Q91 for ODD Power sequence.
6. Add L87 for SWR_V12.
7. C18 22U Change to 47U.
8. TEST35 change to PU for HDMI Function.
20110127
1. Co-lay KB9012
2. Add C19 / C27 / C28 / C31 for +3VS noise.
3. D26 change to SC600000B00 for BOM.
4. Update Power SCH.
20110208
1. Pop Q30 and unpop R25 for FCH A12.
2. C1522 / C1523 change to 33p for TXC test result.
3. Pop R1167 / R1170 / Q90 for ISP function.
4. R21 change to +5VS.
5. Add R604 for +1.5VS leakage current.
20110210
1. Add C32 / C33 / C34 for EMI req.
2. Remove H12.
3. Update power SCH.
20110211
1. Add T19 / T20 for ICT&ATE test.
20110214
1. Add C1082 / C1085 / C1106 / C1107 for DDR.
2. Unpop R29 / R31 / R32 / R51 for USB spec change.
3. Unpop JMINI2 function.
4. Unpop ENBKL / ENCDD level shifter.
5. R119 change to 30K_0402 1% for VGA Power sequence.
6. Pop R1033 / C1357 for EMI req.

PVT Stage

20110301
1. Add functio field.
20110309
1. Re-name to R03
2. Un-pop C954 / C955 for MINI2 not used.
3. Un-pop C1442 for Audio noise issue.
20110324
1.Update L29(always on),Q13(@) BOM structure.
2..Add AMD VRAM table
20110310
1. R1067 change to PJ33 JUMP.
2. R793 change to PJ34 JUMP.
3. R953 change to PJ35 JUMP.
4. R1177 change to PJ36 JUMP.
20110313
1. Add C35 / C36 / C38 / C40 / C41 / C42 for EDS.
2. Pop C1376 / C1377 220pF for EMI.
3. Pop R1014 22ohm / C1352 22pF for EMI.
4. Pop R1055 10ohm / C1352 22pF for EMI.
5. Pop R1203 22ohm / C1515 22pF for EMI.
6. Add C43 10uF for EMI.
7. Unpop Q30 & Pop R25 for FCH Ver.A13
8. Del R53.
9. R1049 / R1185 / R1078 footprint change to 0603 R-SHORT.
10. R1178/ R1184 / R989 / R988 / R995 / R996 / R1108 / R537 / R538 R1094 / R985 / R591 / R1161 footprint change to 0402 R-SHORT.
11. Remove MINI2.
12. Modify HPD level shift.
20110314
1. Add RP8 / RP9 / RP10 / RP11 / R607 for ESD.
2. SWAP USB30 pin define.
3. R1067 / R793 / R953 change to 0805 R-SHORT
4. Add U22 for Fn+F5 issue.
5. Pop L77 and unpop L87 for LVDS flash issue.
6. Add R82 for SW debug<USB PORT0>.
7. C1512 / C1513 connect to +XDPWR_SDPWR_MSPWR.
20110317
1. Update Power SCH.
20110318
1. Add T29 .
2. Add L30 for FCH M2 .
20110321
1. Add L31 for FCH M2 .
2. Add Q13 for AMD req.
3. Del Q30 for FCH A13.
20110322
1. Pop D33 / D34 / D4 for ESD.
2. Pop R730.
3. Q13 change to SB00000FG10 AOS3416.
4. Unpop LED8 / R381 (3G@) for 3G.
5. Add FCH M2 A13 Part number SC000042C60.
6. SA000008J10 change to SB00000EN00.
7. Pop R728 for factory req.
20110323
1. C995 / C999 / C994 / C993 / C30 / C29 / C1010 / C1009 / C5 Change to SGA20331E10 for Power req.
20110324
1.Add AMD 128M*16 VRAM table of Whistler,Seymour
2.Update L29(pop),Q13(@) BOM Structure
20110327
1. Update Power SCH.

Pre MP Stage

20110416
1.Add C1465 100p for HW Card Reader
2.Change C38,C40,C41,C42 from 10p to 33p for ESD
3.Add APU_PWRGD 0 ohm(R615) on APU side for ESD
APU_RST# 0 ohm(R598) on APU side for ESD
4.Remove HDT connector and releated nets,pins
5.Pop COM_MIC ESD diode:D41 for ESD
20110417
1.Mask PJ32,C9 for DFX
20110418
2.Remove Power Button SW1.
20110419
1.Delete H25 for Layout request
2.Add Test point of JTAG for 測試 request
3.Unpop C29,C30 for only 2 phase sku
4.Change PCB P/N from DA60000NA00 to DAZ0JU00100
5.Change C391,C392,C393 from 1uF to 0 ohm For UMA SKU
6.For BCM WLAN lost issue:
Change C1339 from 4.7uF to 10uF
Change C1340,C1341 from 0.1uF to 1uF
20110420
1.Change C1205,C1206 from 22pF to 15pF For RTC issue
2.Add HDMI Royalty:RO0000003HM

WHISTLER-PRO

ID3-0	Vendor	Size	Freq	P/N	Description	Qualify
0000	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12	V
0001	SAM	C-die 128*16	800MHz	SA00003MQ60	K4W2G1646C-HC12	V
0010	SAM	G-die 64*16	933MHz	SA00004GS10	K4W1G1646G-BC11	
0011	SAM	C-die 128*16	933MHz	SA000047Q20	K4W2G1646C-HC11	
0100						
0101						
0110						
0111						
1000	HYN	Orion-die 64*16	800MHz	SA000032420	H5TQ1G63BFR-12C	
1001	HYN	Vega-die 128*16	800MHz	SA00003VS10	H5TQ2G63BFR-12C	V
1010	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C	V
1011	HYN	Vega-die 64*16	800MHz	SA0000324G0	H5TQ1G63DFR-12C	
1100	HYN	Vega-die 128*16	900MHz	SA00003YO20	H5TQ2G63BFR-11C	
1101						
1110						
1111	AMD	A-die 128*16	900MHz	SA00004U500	23EY4187MA11	

SEYMOUR-XT

ID3-0	Vendor	Size	Freq	P/N	Description	Qualify
0000	AMD	A-die 128*16	900MHz	SA00004U500	23EY4187MA11	
0001						
0010	SAM	C-die 128*16	933MHz	SA000047Q20	K4W2G1646C-HC11	
0011	SAM	G-die 64*16	933MHz	SA00004GS10	K4W1G1646G-BC11	
0100	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12	V
0101	SAM	C-die 128*16	800MHz	SA00003MQ60	K4W2G1646C-HC12	V
0110						
0111						
1000						
1001						
1010						
1011	HYN	Vega-die 64*16	800MHz	SA0000324G0	H5TQ1G63DFR-12C	
1100	HYN	Orion-die 64*16	800MHz	SA000032420	H5TQ1G63BFR-12C	
1101	HYN	Vega-die 128*16	800MHz	SA00003VS10	H5TQ2G63BFR-12C	V
1110	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C	V
1111	HYN	Vega-die 128*16	900MHz	SA00003YO20	H5TQ2G63BFR-11C	

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Title: HW PIR / SCREW

Size	Document Number	Rev
C	P5WS5 LA-6973P	1.0

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