

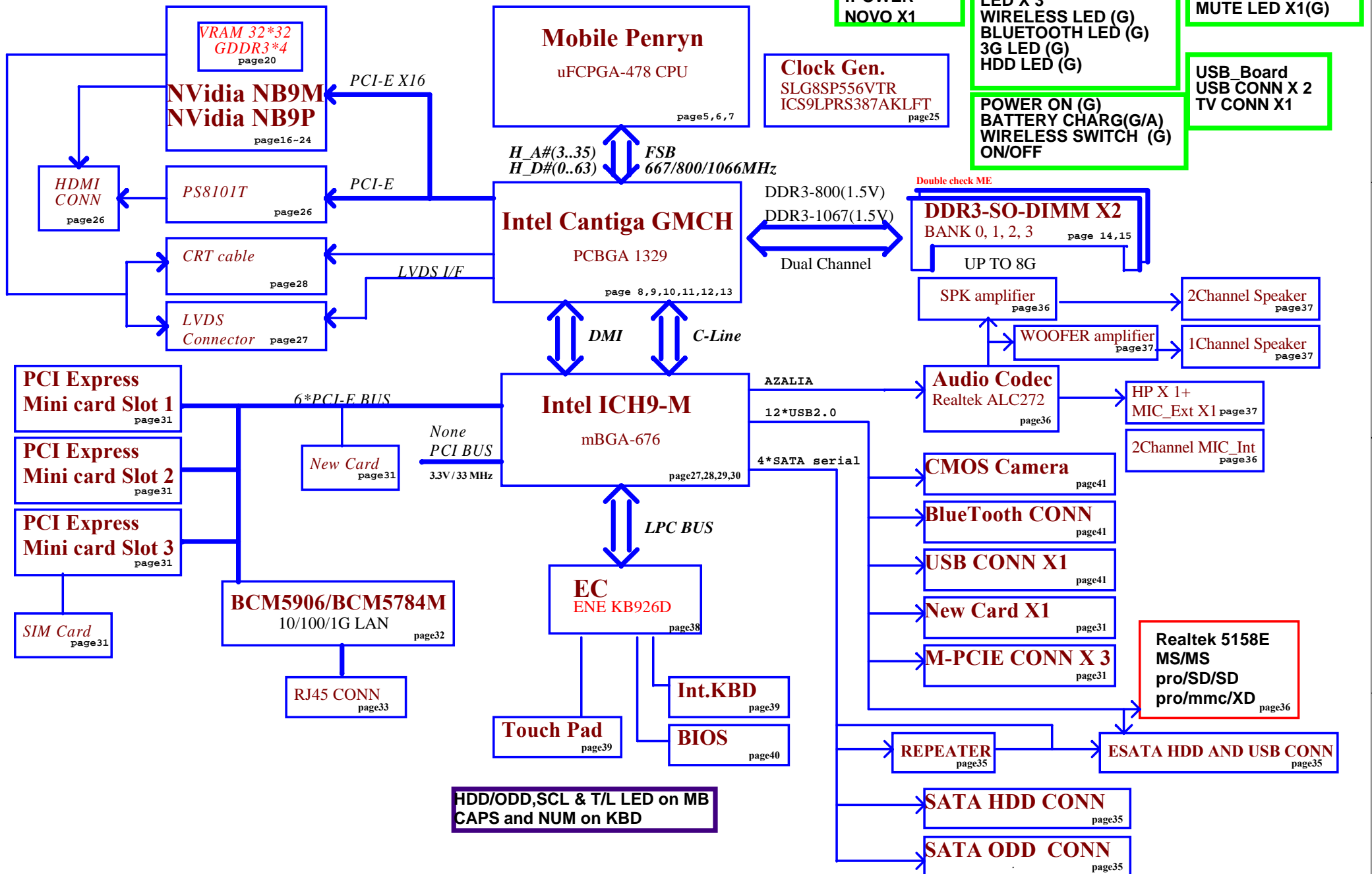
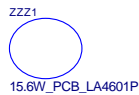
# Blue Moutain KIWB1/B2

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

REV:0.1

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# DDR3 Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
		+3VALW	+1.8V +0.75V	+3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
State				
s0	o	o	o	o
s1	o	o	o	o
s3	o	o	o	x
s5 s4/AC	o	o	x	x
s5 s4/ Battery only	o	x	x	x
s5 s4/AC & Battery don't exist	x	x	x	x

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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### VGA and DDR2 Voltage Rails (NB9M-GS)

State \ power plane			+1.8V	+3VS +VGA_CORE +1.1VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	Available
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2 or MEM VID
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	FAN control and/or Thermal Alert (PWM)
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP link E
GPIO16	IN	-	Dongle DVI Mode control for Primary Displayport
GPIO17	IN	-	Dongle HDMI Mode control for Primary Displayport
GPIO18	IN	-	Dongle DVI Mode control for Secondary Displayport
GPIO19	IN	-	Dongle HDMI Mode control for Secondary Displayport
GPIO20	IN	-	Hot plug detect for IFP link D
GPIO21	IN	-	Hot plug detect for IFP link E
GPIO22	IN	-	SLI swap ready signal
GPIO23	N/A	N/A	Available

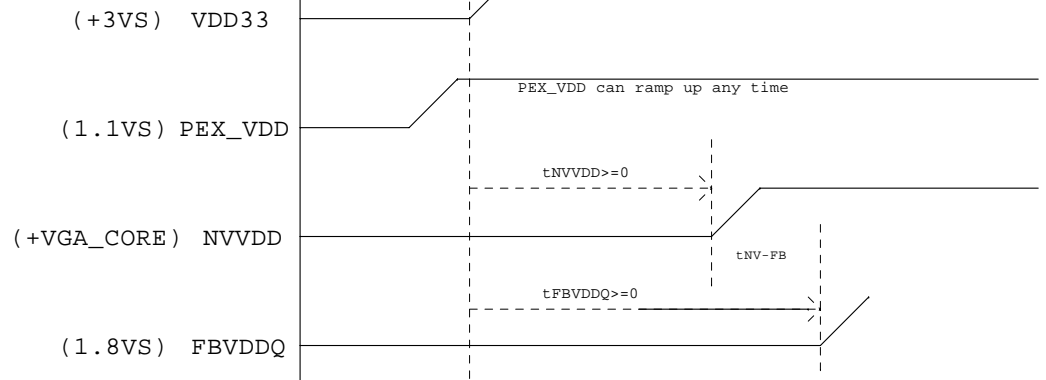
### EDP at Tj = 97C\*

VRAM POWER SEQUENCE  
GDDR3 FOR 4 UNIT = 5.4A

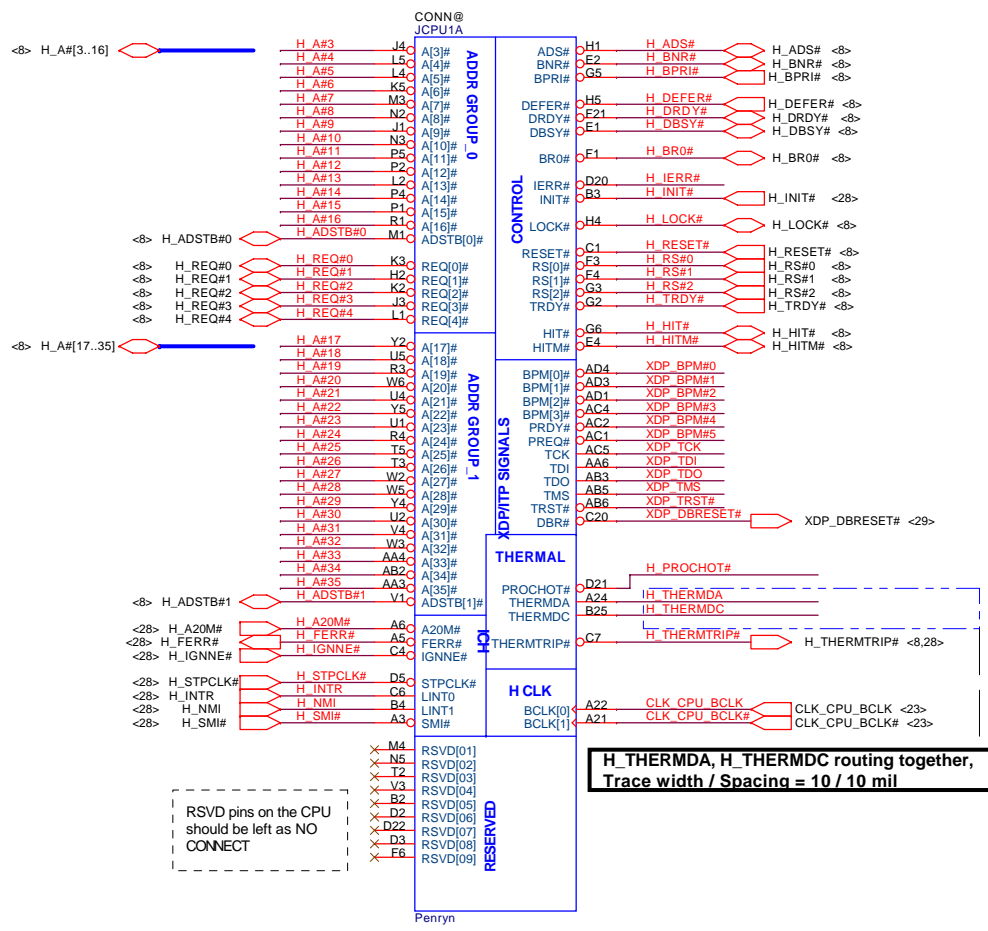
Power Supply Rail (V)	NB9P-GS		NB9P-GE2		
	GDDR3	DDR2	GDDR3	DDR2	
NVDD	20.65A	16.96A	18.47A	16.06A	
FB_DLLAVDD	1.1			10mA	
FB_PLLAVDD	1.1			10mA	
IFPC_IOVDD	1.1			80mA	
IFPD_IOVDD	1.1			80mA	
IFPE_IOVDD	1.1			160mA	
IFPF_IOVDD	1.1			160mA	
PEX_IOVDD/Q	1.1			1550mA	
PEX_PLLVDD	1.1			90mA	
PLLVDD	1.1			45mA	
SP_PLLVDD	1.1			45mA	
VID_PLLVDD	1.1			45mA	
<b>TOTAL</b>	<b>1.1</b>			<b>2.3A</b>	
FBVDD/Q	1.8	3.37A	2.02A	3.21A	2.25A
IFPA_IOVDD	1.8				95mA
IFPB_IOVDD	1.8				95mA
IFPAB_PLLVDD	1.8				70mA
IFPCD_PLLVDD	1.8				25mA
IFPEF_PLLVDD	1.8				85mA
<b>TOTAL</b>	<b>1.8</b>	<b>5.76A</b>	<b>3.69A</b>	<b>5.47A</b>	<b>3.96A</b>
DACA_VDD	3.3				110mA
DACB_VDD	3.3				120mA
DACC_VDD	3.3				110mA
MIOA_VDDQ	3.3				10mA
MIOB_VDDQ	3.3				10mA
VDD33	3.3				150mA
<b>TOTAL</b>	<b>3.3</b>				<b>0.51A</b>

### POWER SEQUENCE

The ramp time for any rail must be more than 40us



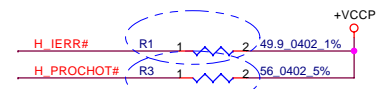
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**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

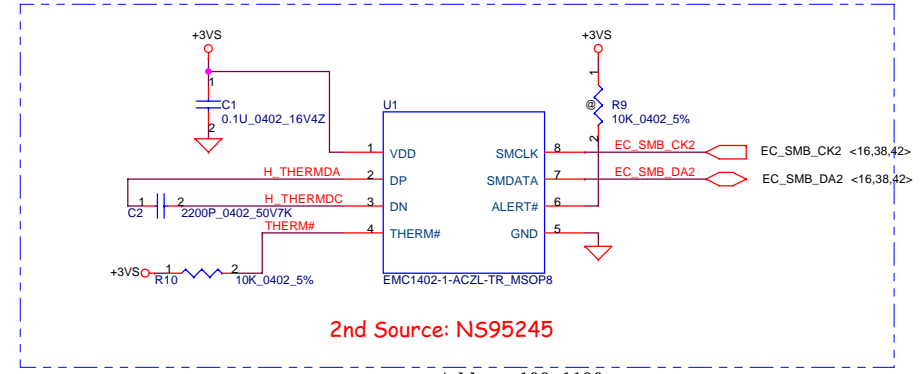
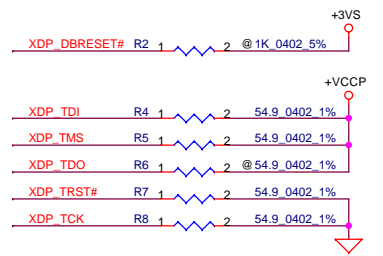
RSVD pins on the CPU should be left as NO CONNECT

USE->56Ω, NOT USE->50Ω

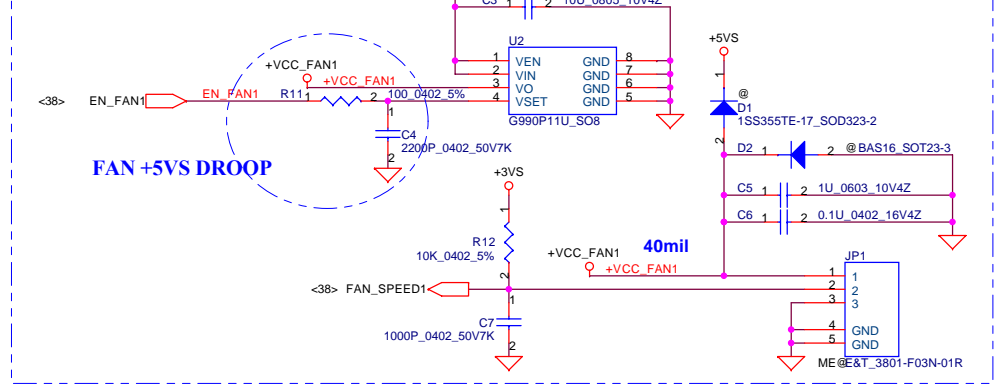


USE->68Ω, NOT USE->56Ω

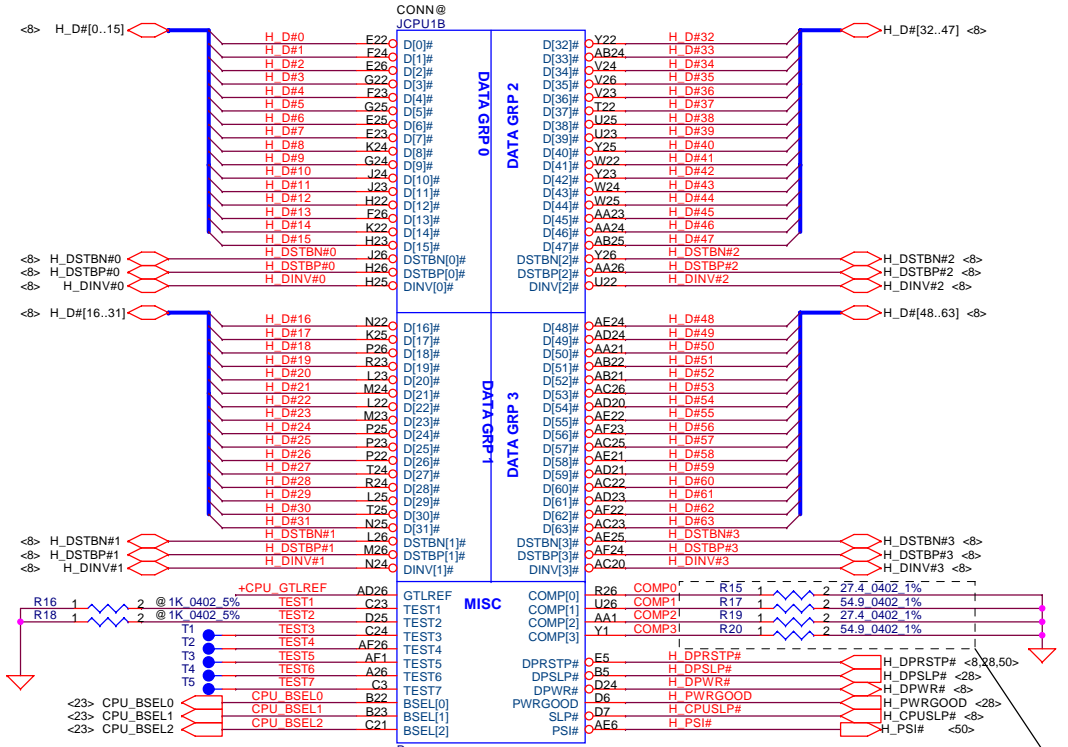
**XDP Reserve**



**FAN1 Conn**



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				<b>Penryn(1/3)</b>
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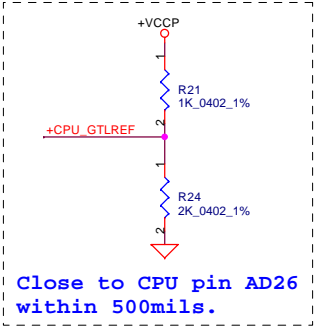
Trace Close CPU < 0.5'

Width=4 mil,  
Spacing: 15mil  
(55Ohm)

**TRACE CLOSELY CPU < 0.5'**  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

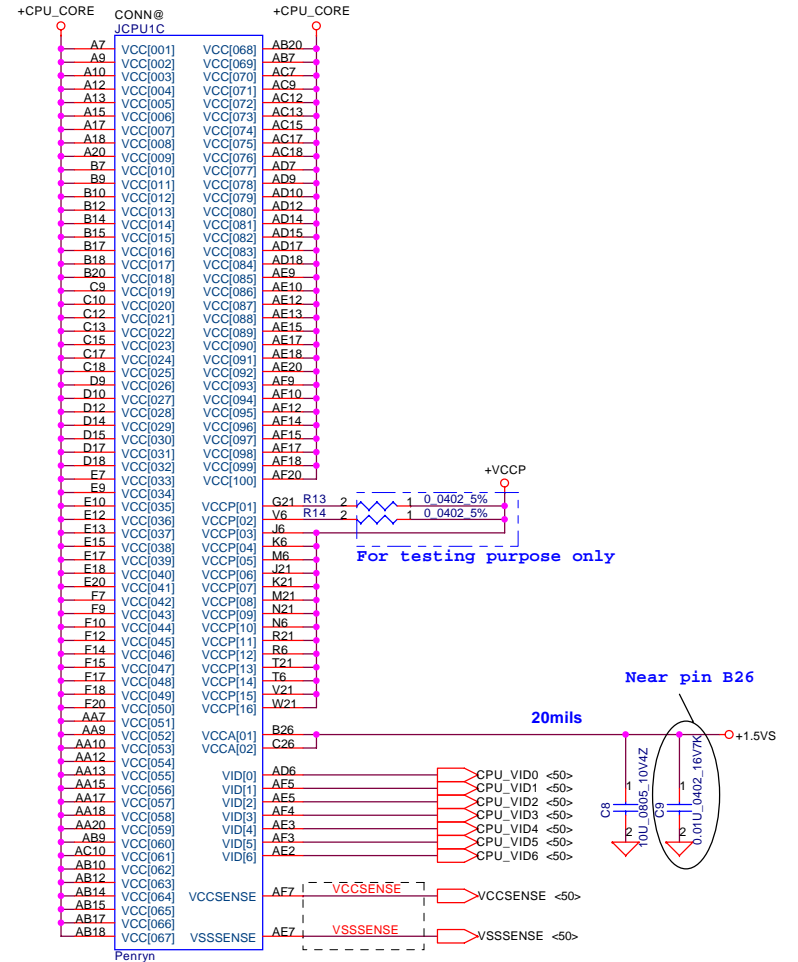
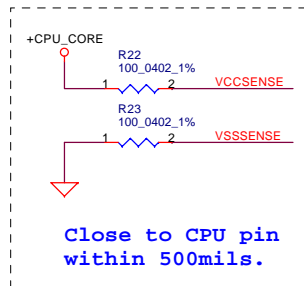
Layout note: Z0=55 ohm  
0.5" max for GTLREF.



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

length match within 25 mils.  
The trace width/space/other is 18/7/25.

Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.

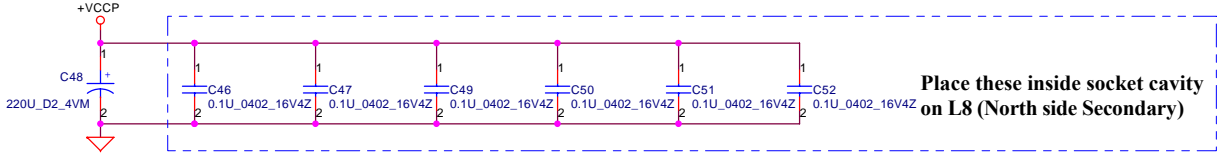
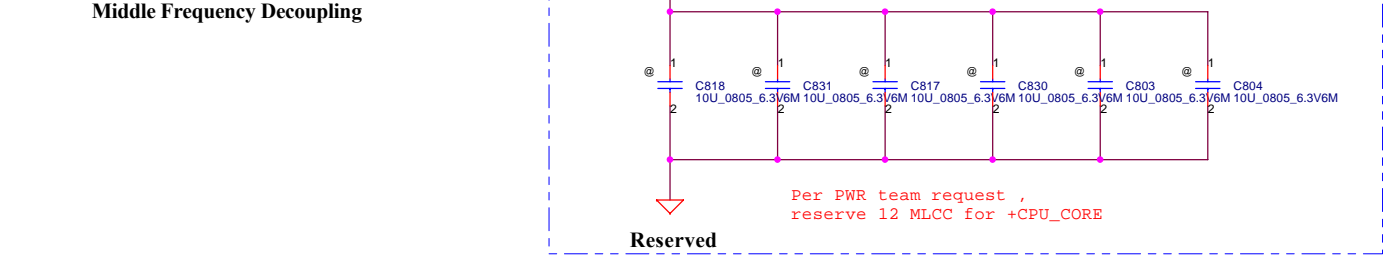
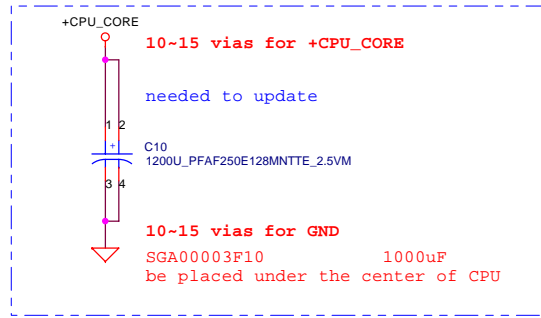


For testing purpose only

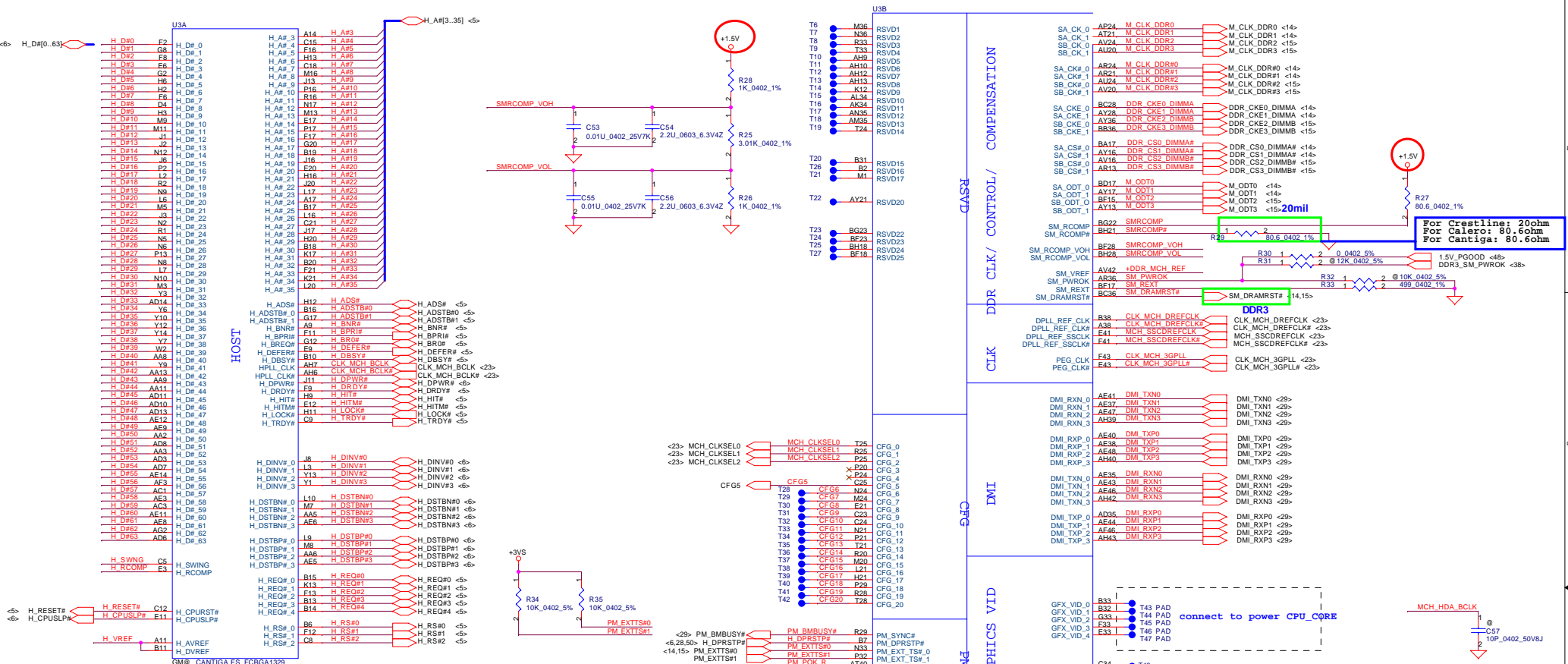
Near pin B26

20mils

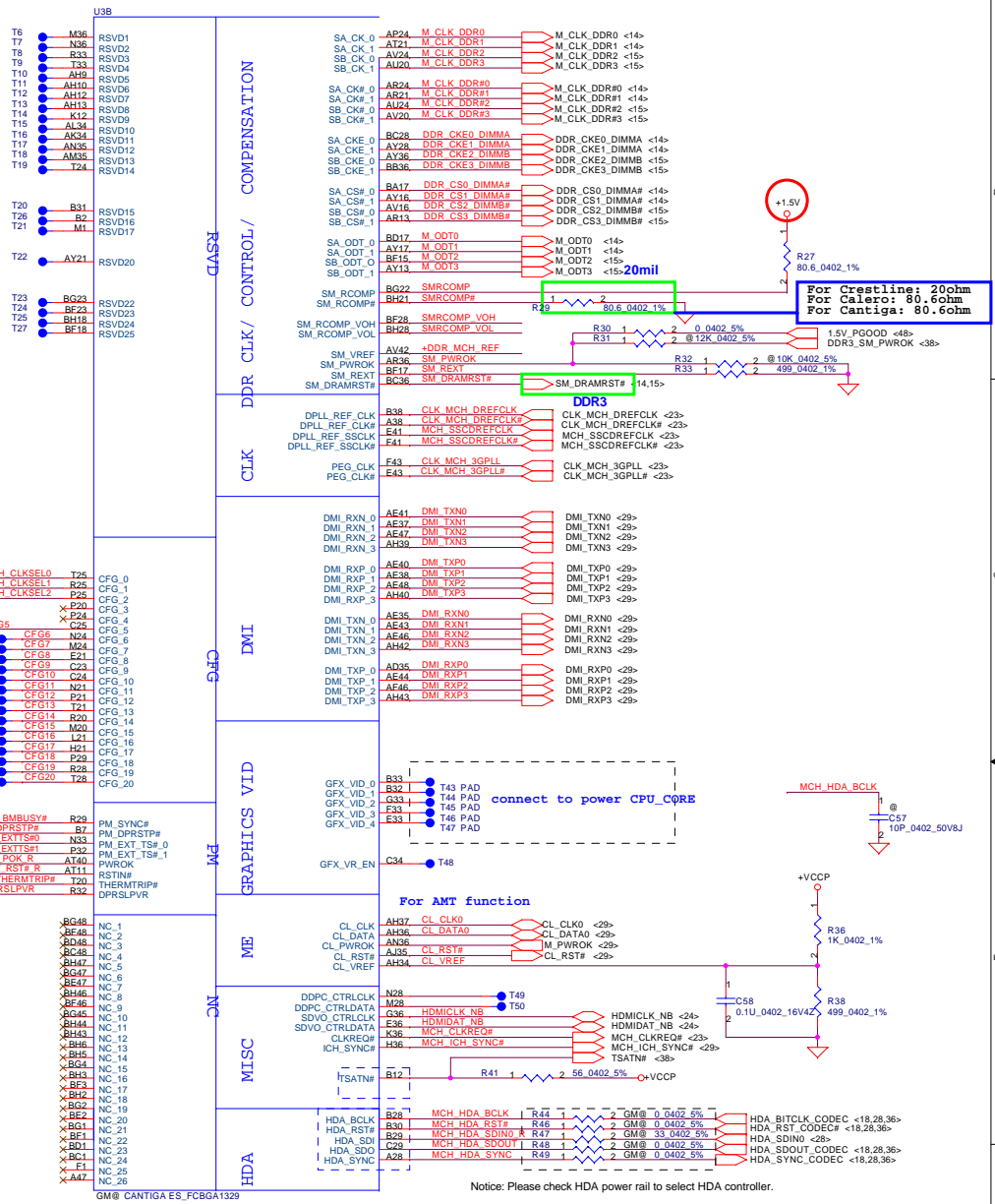
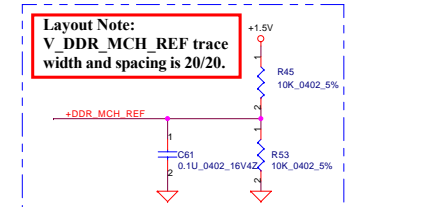
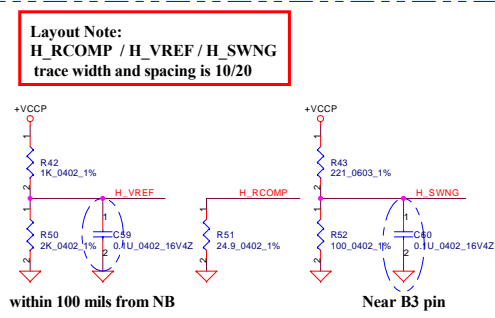
CONN@		JCPU1D	
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[003]	VSS[084]	R2
A16	VSS[004]	VSS[085]	R5
A19	VSS[005]	VSS[086]	R22
A23	VSS[006]	VSS[087]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[008]	VSS[089]	T4
B8	VSS[009]	VSS[090]	T23
B11	VSS[010]	VSS[091]	T26
B13	VSS[011]	VSS[092]	U3
B16	VSS[012]	VSS[093]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[017]	VSS[098]	V22
C11	VSS[018]	VSS[099]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E6	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC9
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
	VSS[163]		



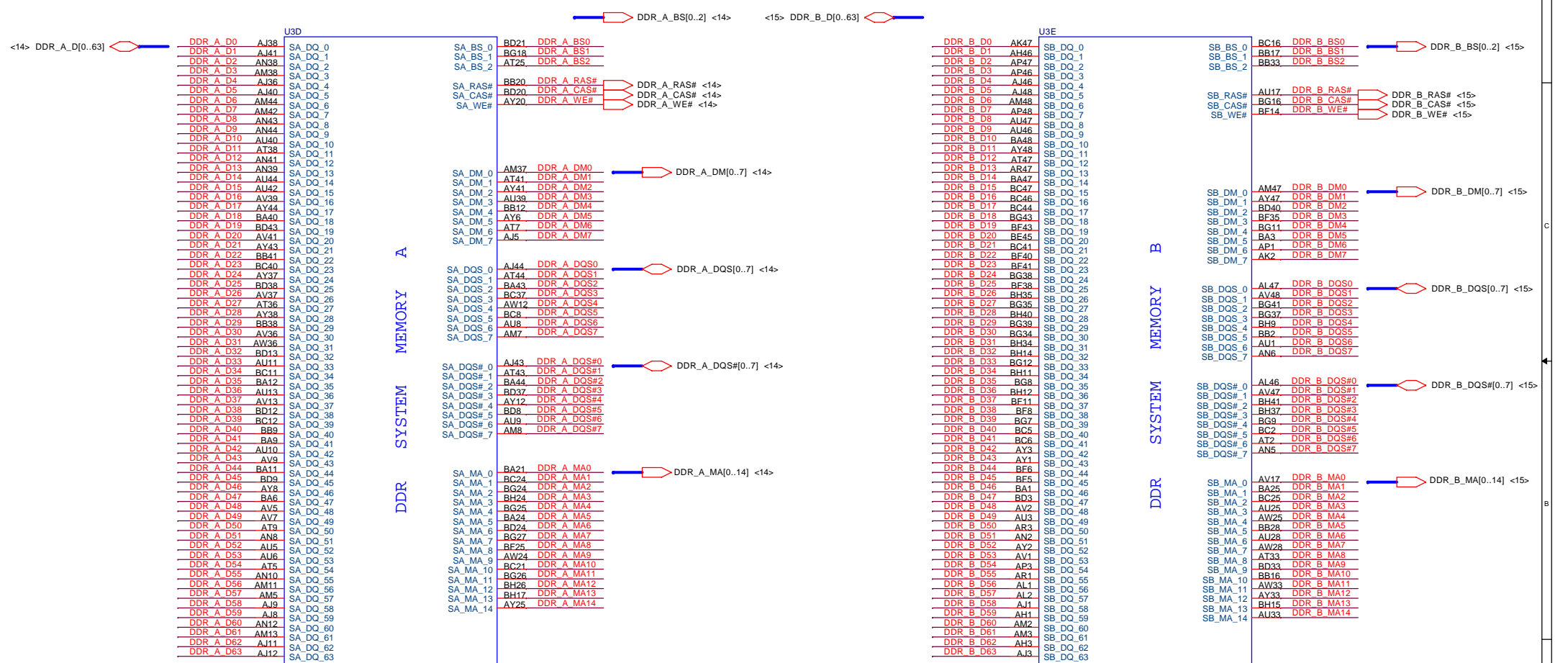
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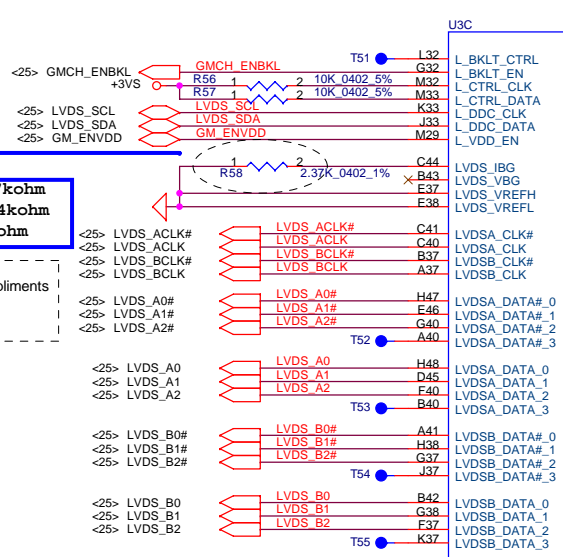
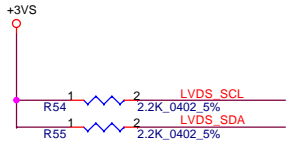
layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width spacing and impedance (55 ohm) same as FSB data traces







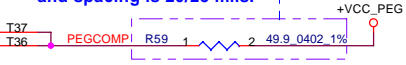
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For Cantiga: 2.37kohm  
For Crestline: 2.4kohm  
For Calero: 1.5kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

Place the resistor within 500mils (1.27mm) of the (GMCH) PEGCOMP trace width and spacing is 20/25 mils.



Please check Power source if want support IAMT

### Strap Pin Table

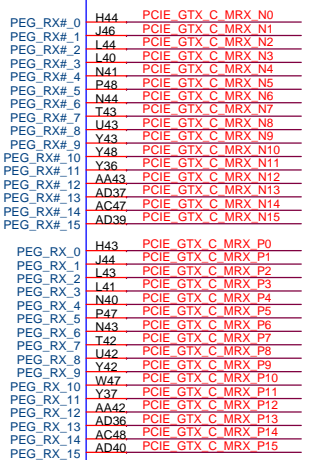
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chipset suite with no confidentiality 1 = (TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

### GRAPHICS

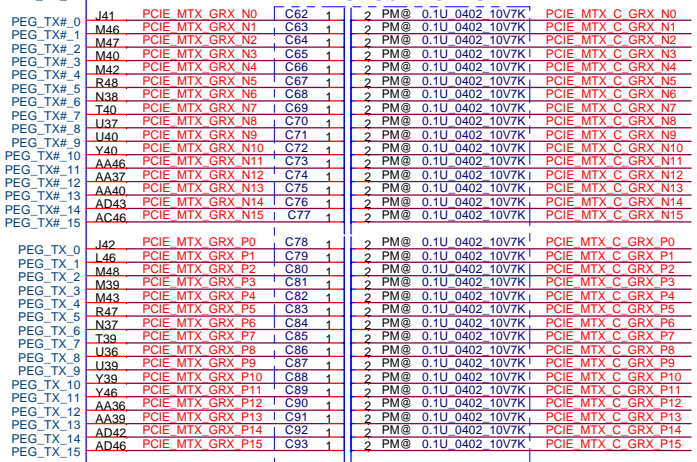
### PCI-EXPRESS

### TV

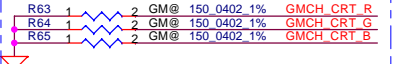
### VGA



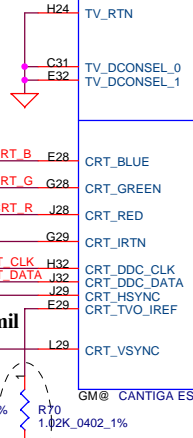
### CLOSE TO MCH



Layout Note: Place 150 Ω termination resistors close to GMCH



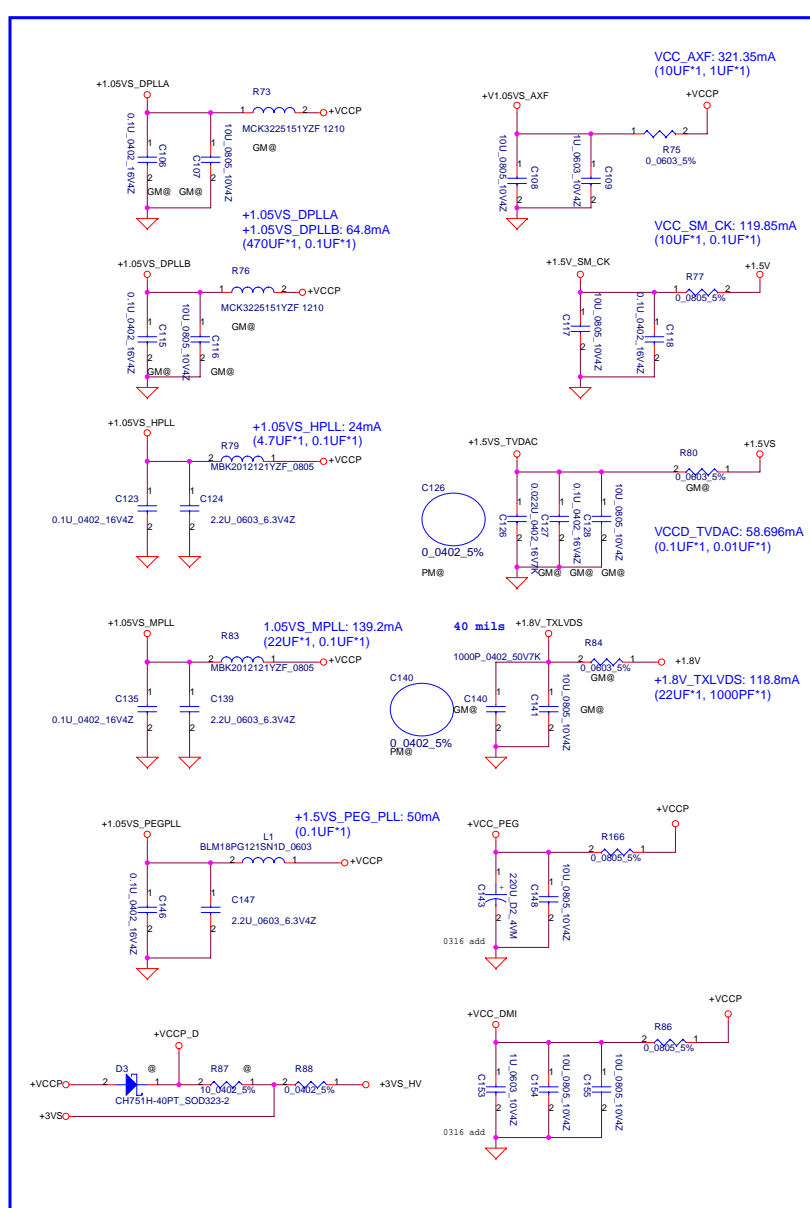
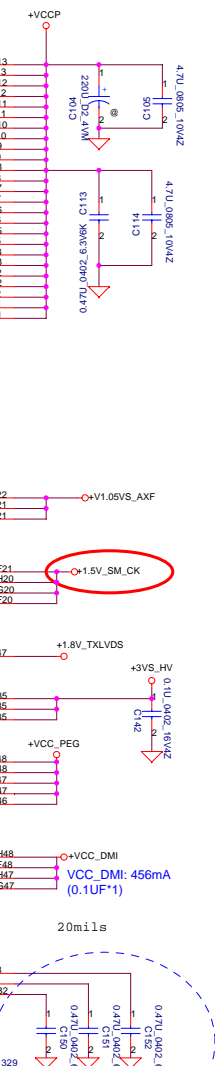
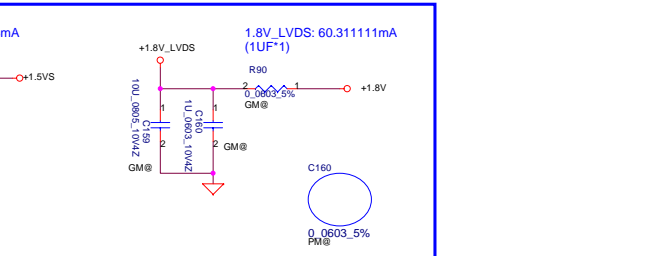
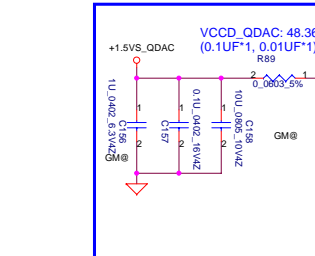
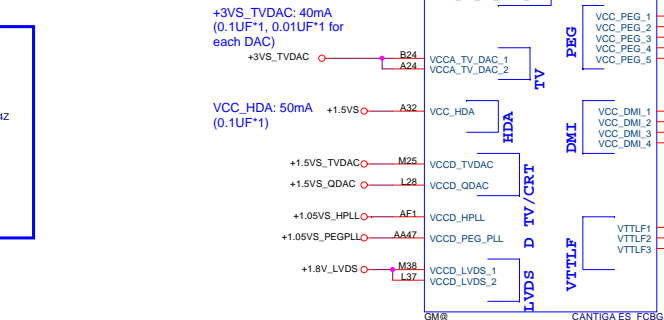
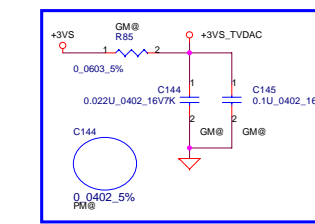
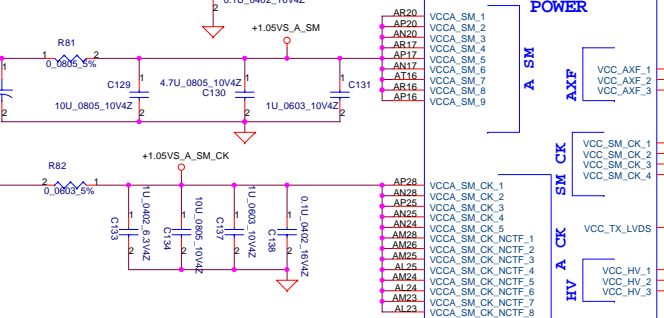
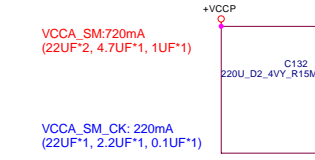
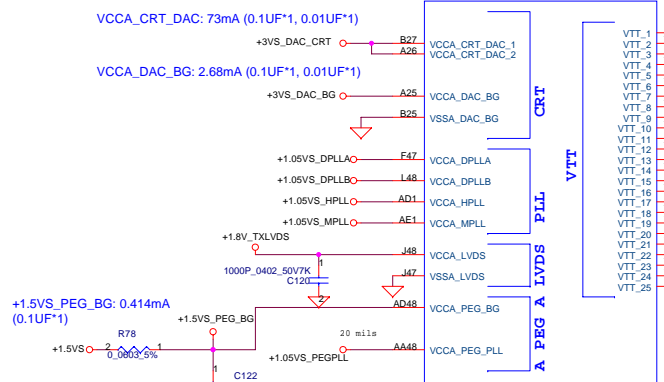
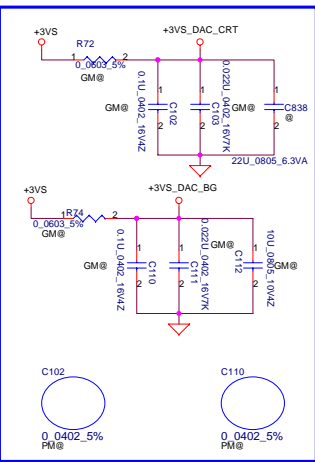
change R64,R65 from 33ohm to 30ohm by checklist2.0 & CRB1.0 05/08/08



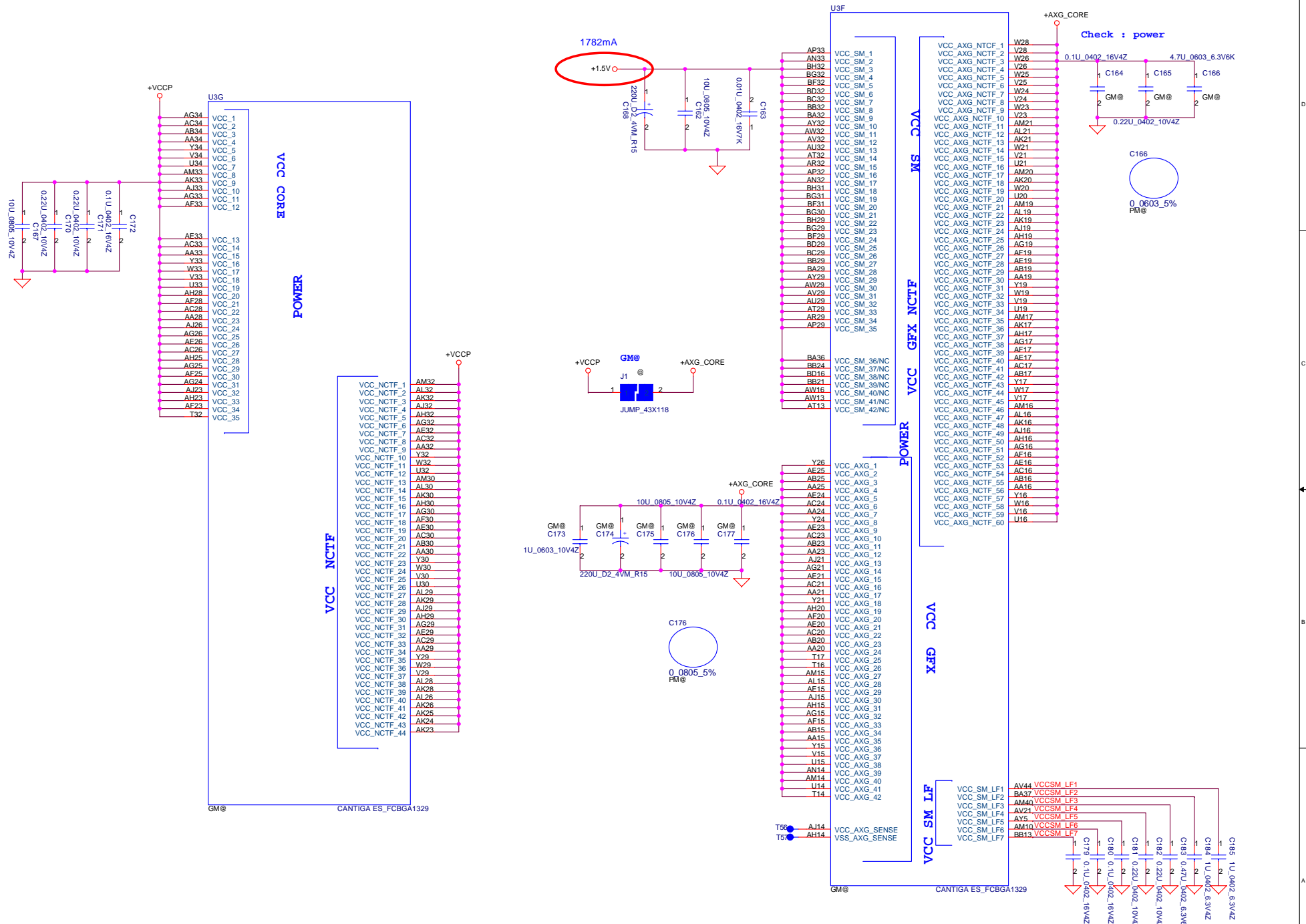
For Cantiga: 1.02kohm  
For Crestline: 1.3kohm  
For Calero: 255ohm

Security Classification		Compal Secret Data	
Issued Date	2008/03/25	Deciphered Date	2008/04/
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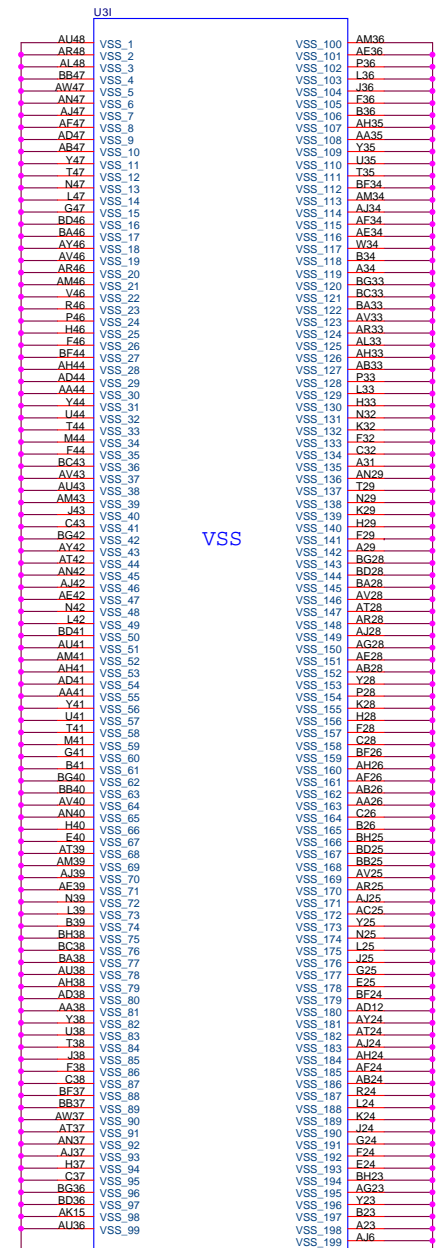
Compal Electronics, Ltd.	
Title	Cantiga(3/6)-VGA/LVDS/TV
Size	Document Number
Customer	KIWB3/B4 LA4551P
Date:	Monday, June 30, 2008
Sheet	10 of 52



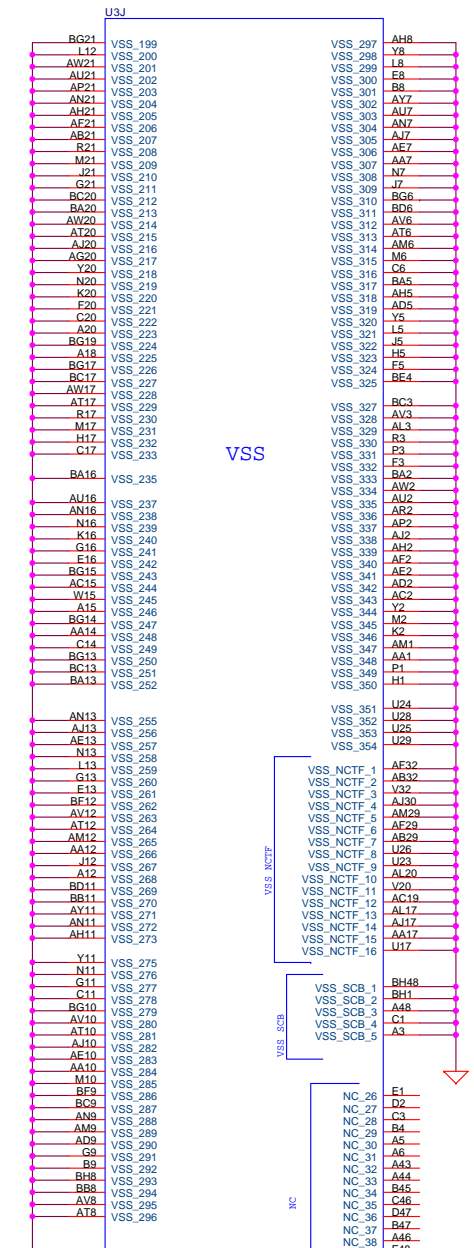
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.
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				Document Number
				Custom
				KIW63/B4_LA4551P
				Rev
				0.1
				Date:
				Thursday, June 26, 2008
				Sheet
				11 of 52



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Size	Document Number	Rev	Date	
Custom	<b>KIWB3/B4_LA4551P</b>	0.1	Thursday, June 26, 2008	
		Sheet	12	of 52



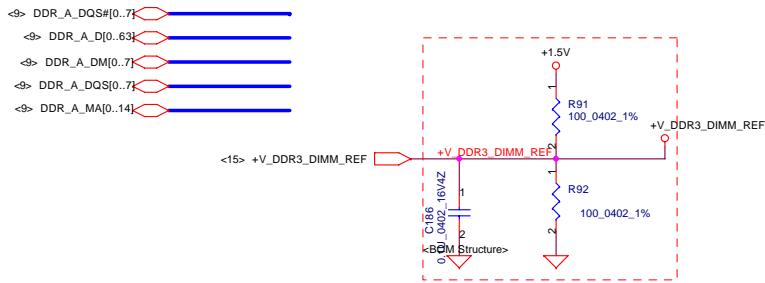
GM® CANTIGA ES\_FCBGA1329



GM® CANTIGA ES\_FCBGA1329

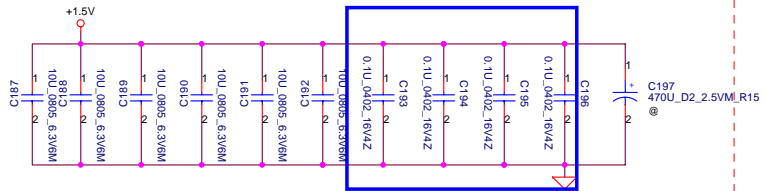
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Issued Date	2007/10/15	Deciphered Date	2008/10/15
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<b>Compal Electronics, Inc.</b>			
<b>Cantiga GMCH (6/6)-GND</b>			
Size	Document Number	Rev	
Custom	<b>KIWB3/B4_LA455IP</b>	0.1	
Date:	Thursday, June 26, 2008	Sheet	13 of 52

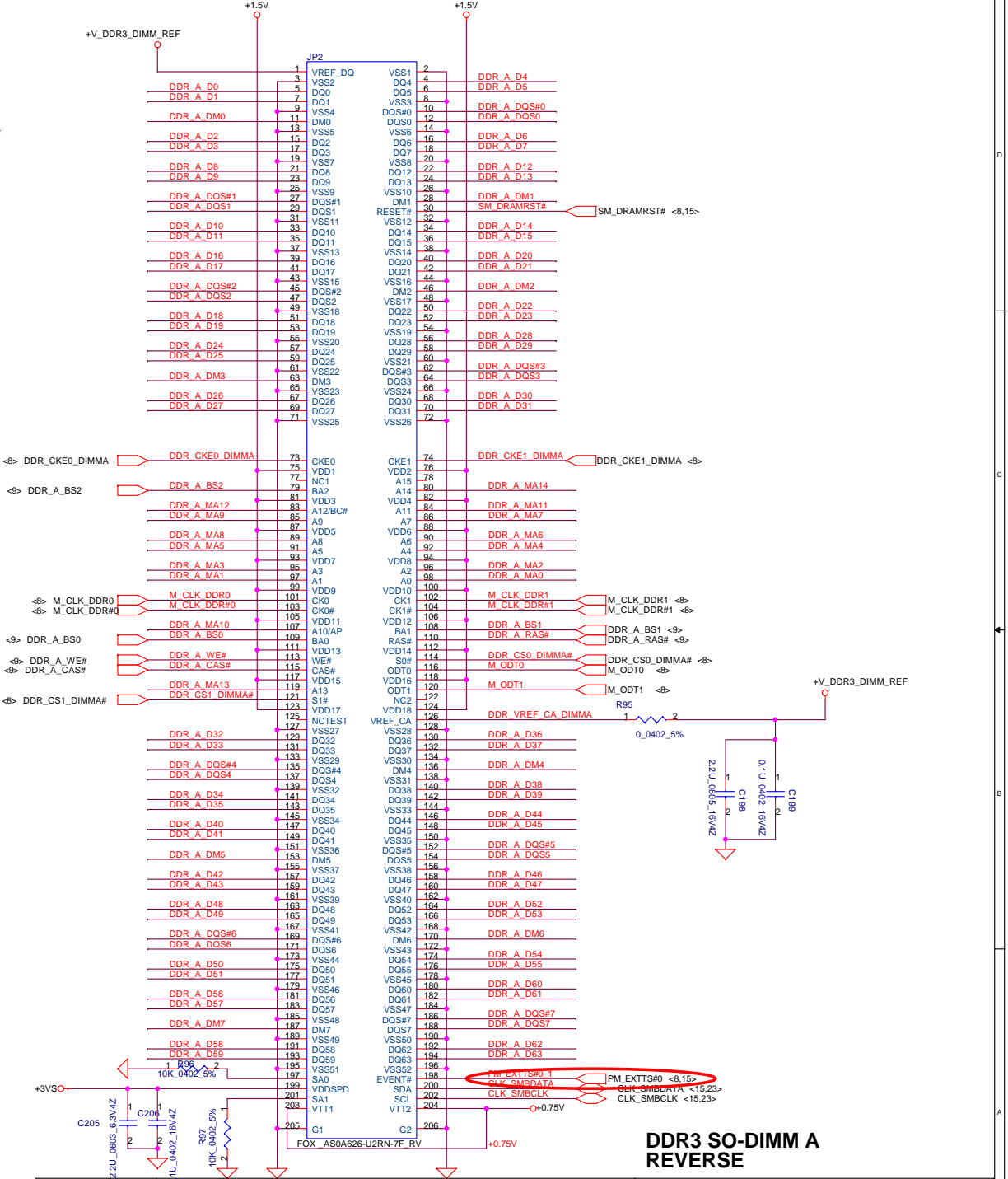
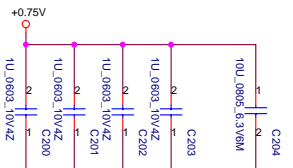


**Layout Note:**  
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMM



**Layout Note:**  
Place near JP4.203 & JP4.204

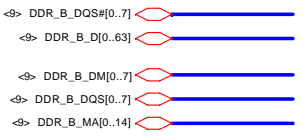


**DDR3 SO-DIMM A REVERSE**

Security Classification	Compal Secret Data
Issued Date	Deciphered Date
2007/09/29	2007/09/29

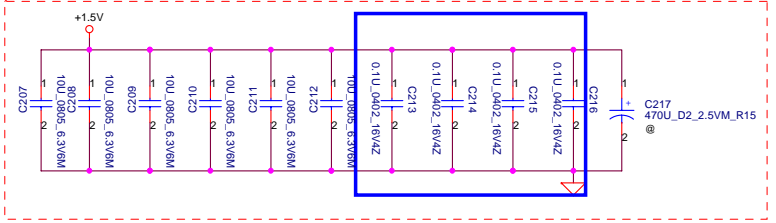
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Title			
Compal Electronics, Inc.			
DDR3-SODIMM SLOT1			
Size	Document Number	Rev	
Custom	KIWB1/B2_LA4601P	1.0	
Date:	Monday, June 30, 2008	Sheet	14 of 52

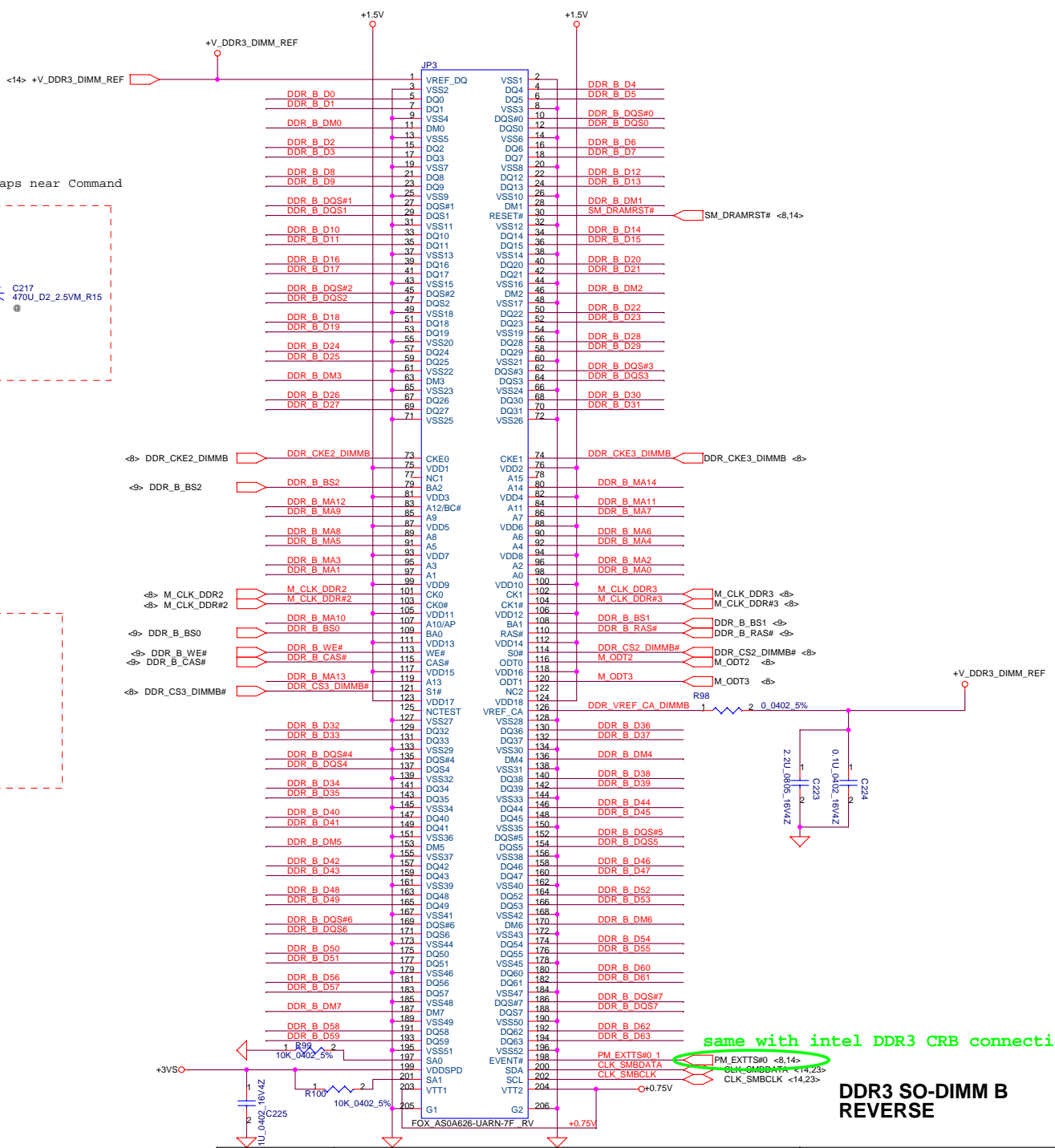
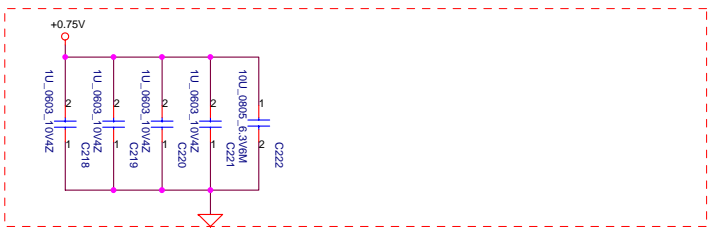


**Layout Note:**  
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



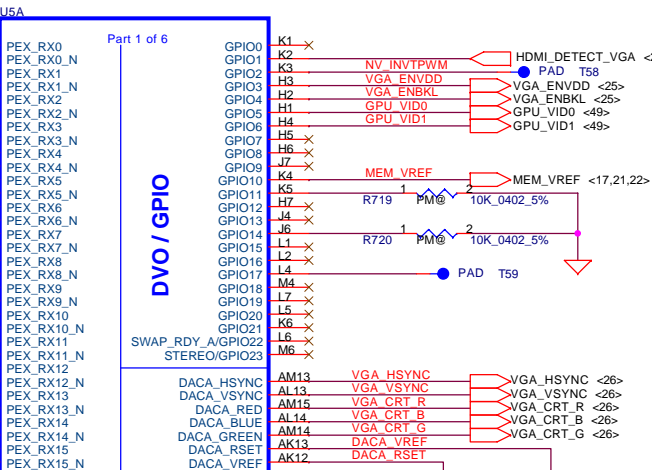
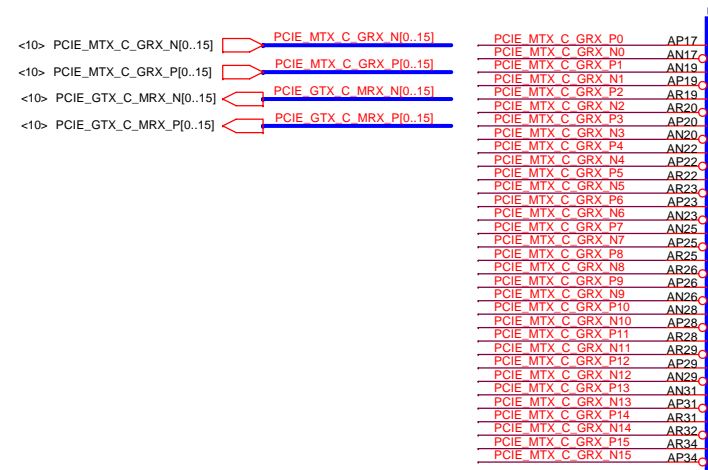
**Layout Note:**  
Place near JP5.203 & JP5.204



same with intel DDR3 CRB connection

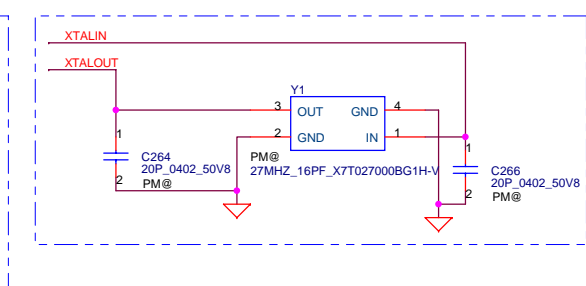
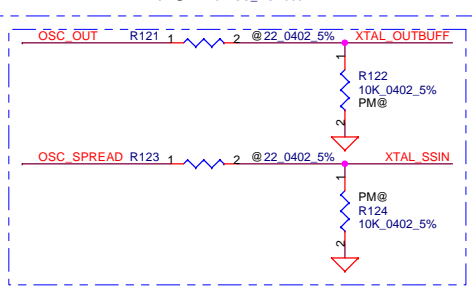
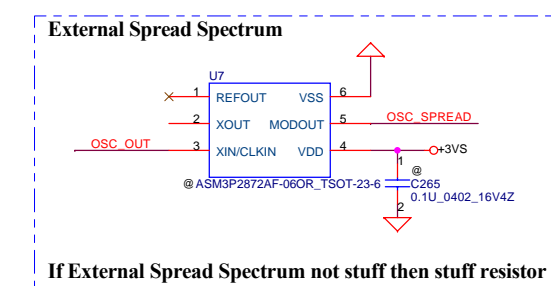
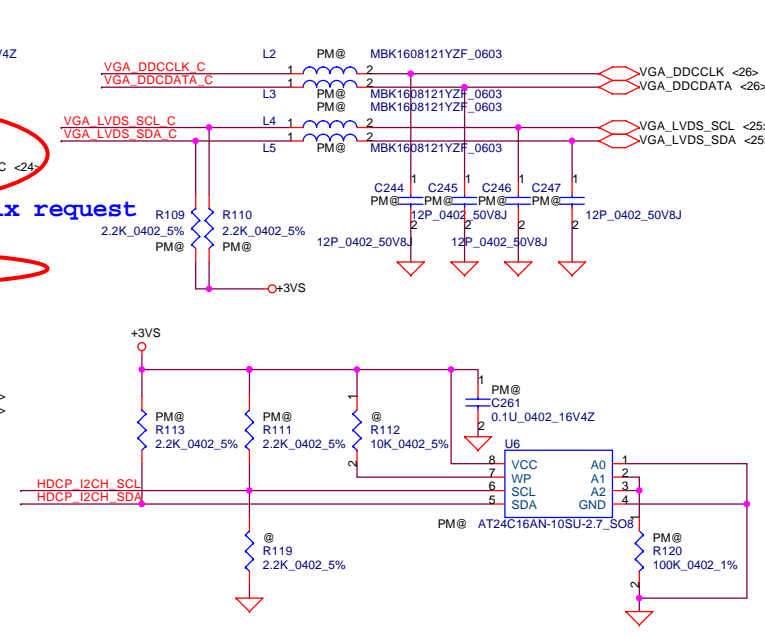
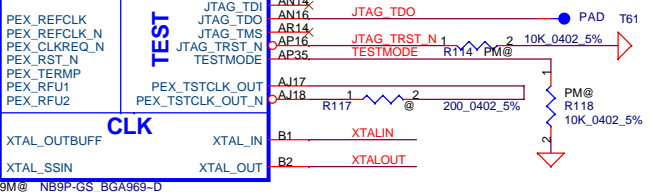
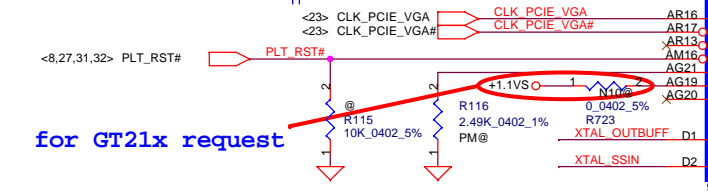
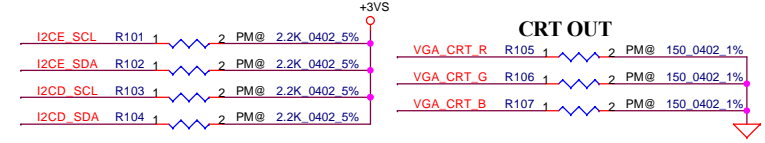
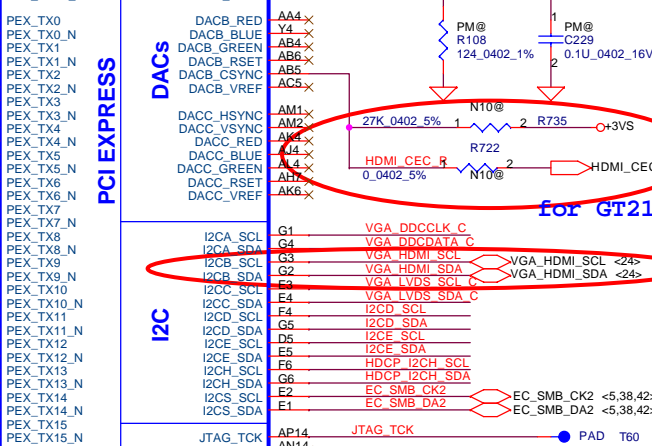
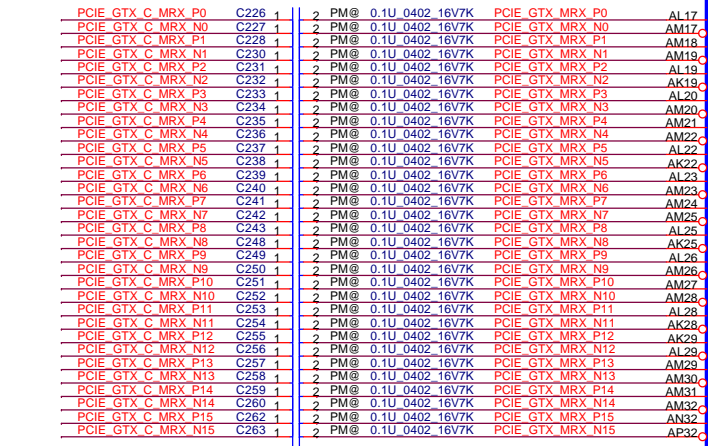
**DDR3 SO-DIMM B REVERSE**

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Size	Document Number	Rev		1.0
KIWI/B2_LA4601P				
Date:	Monday, June 30, 2008	Sheet	15	of 52



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1	1	1.17V	0
1	0	1.09V	8

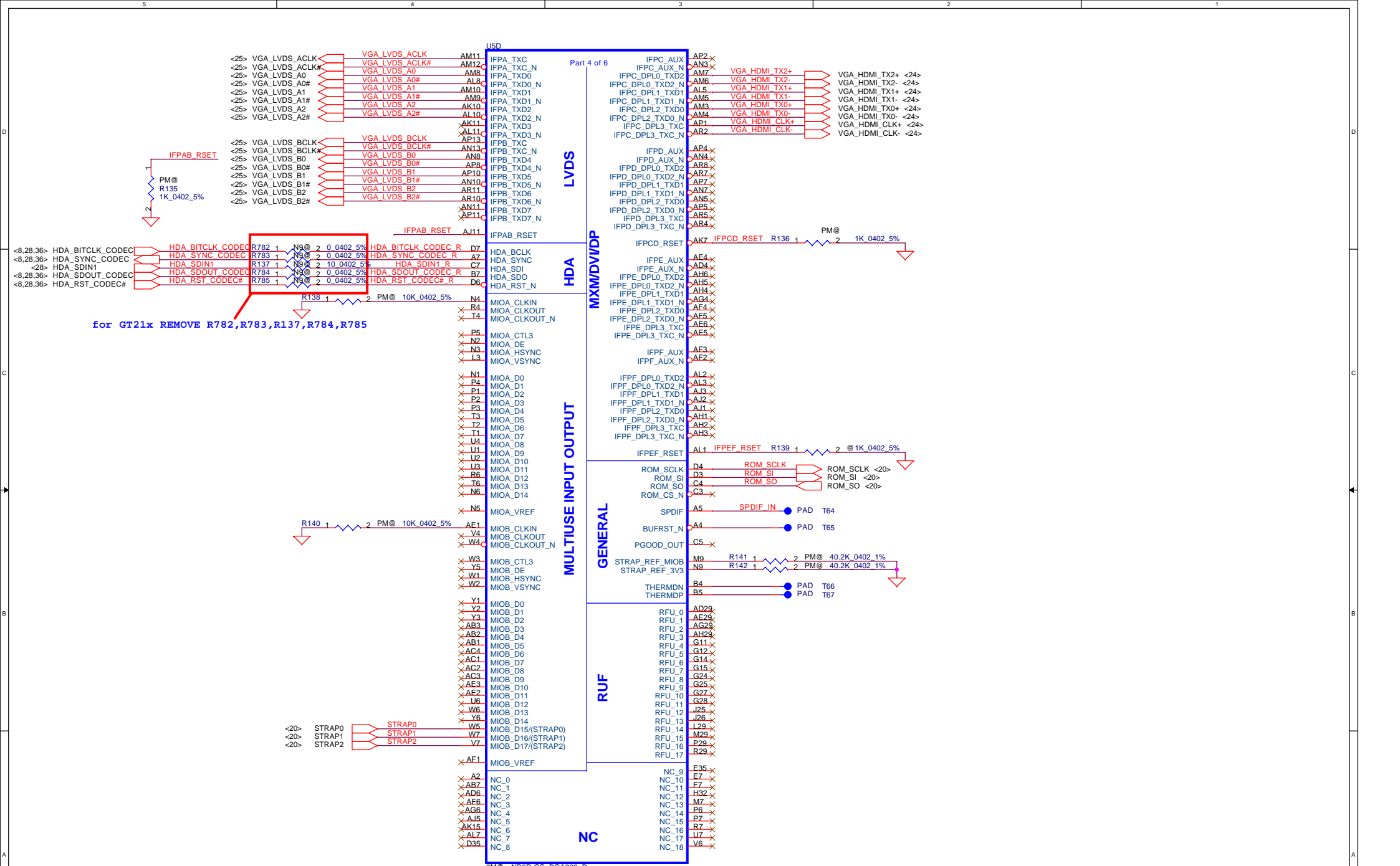
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0	1	0.9v	8,10,12



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Size	Document Number	KIWB1/B2_LA4601P		Rev	0.1
Custom	Date: Monday, June 30, 2008	Sheet	16	of	52



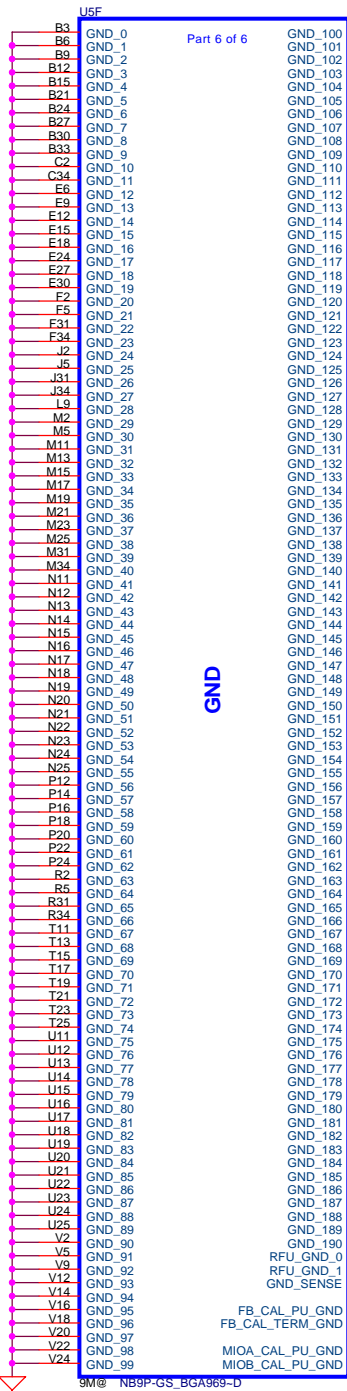




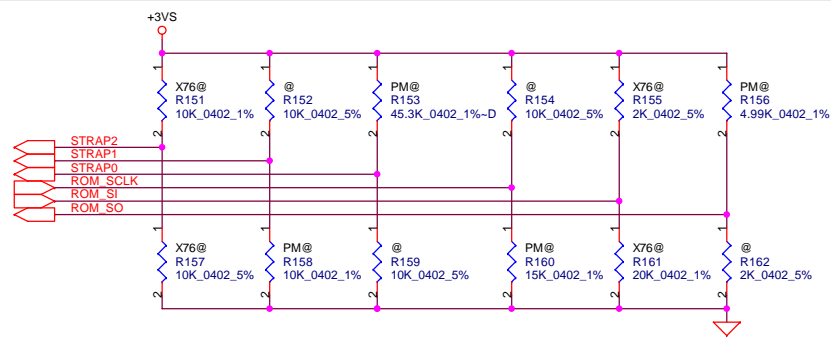
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				Custom	0.1
				Date:	Monday, June 30, 2008
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<18> STRAP2  
 <18> STRAP1  
 <18> STRAP0  
 <18> ROM\_SCLK  
 <18> ROM\_SI  
 <18> ROM\_SO



### GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS 128bit	Samsung	16Mx32	PU 5K PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
Qimonda	16Mx32	PU 5K PD 15K	PD 10K	PU 10K	PD 10K	PU 45K	
	32Mx32	PU 5K PD 15K	PD 30K	PU 10K	PD 10K	PU 45K	

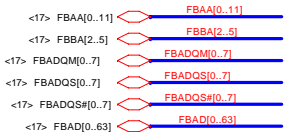
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9P-GE2 128bit	Samsung	16Mx32	PU 5K PD 15K	PD 20K	PU 5K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 45K	PU 5K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K PD 15K	PD 15K	PU 5K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 35K	PU 5K	PD 10K	PU 45K
Qimonda	16Mx32	PU 5K PD 15K	PD 10K	PU 5K	PD 10K	PU 45K	
	32Mx32	PU 5K PD 15K	PD 30K	PU 5K	PD 10K	PU 45K	

Component	Manufacturer	Compal PN	Compal X76 PN
GDDR3 VRAM (16M*32)	Hynix	X	X
	Qimonda	X	X
	Samsung	X	X
GDDR3 VRAM (32M*32)	Hynix	X	X
	Qimonda	SA000024N20	
	Samsung	SA00002R600	

Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR3	33.2ohm	44.2ohm	40.2ohm
GDDR3 BY N10			

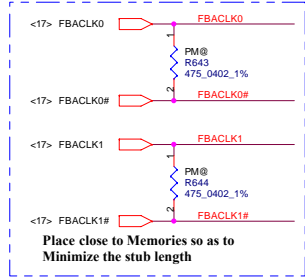
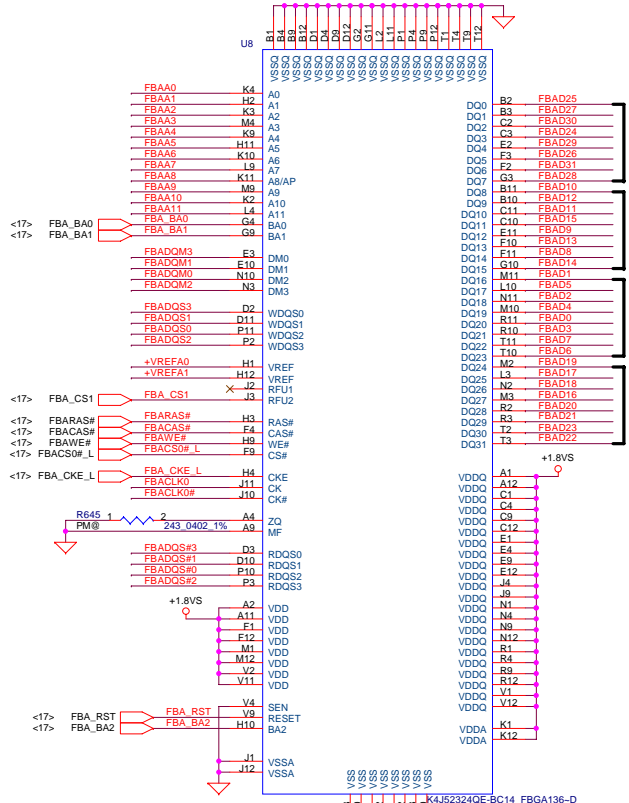
To update for NV PUN-03304-001\_V06 (2008/5/20)

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Date: Monday, June 30, 2008				Sheet	20 of 52

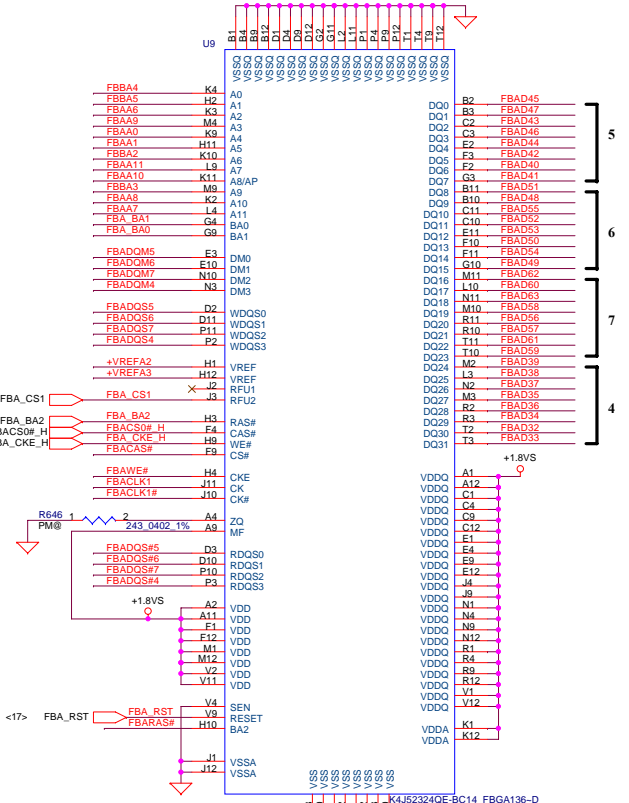


### BGA 84 ADR/CMDN MAPPING

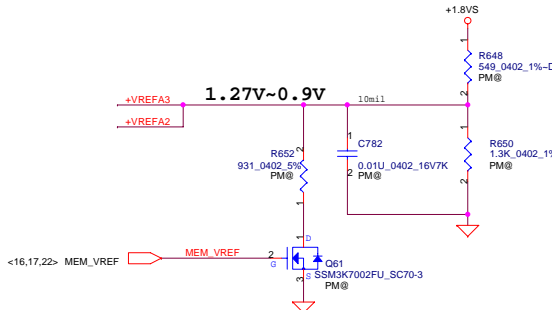
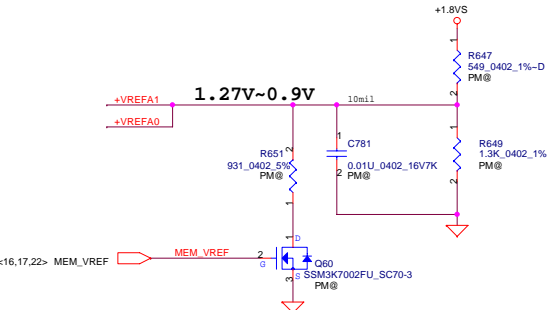
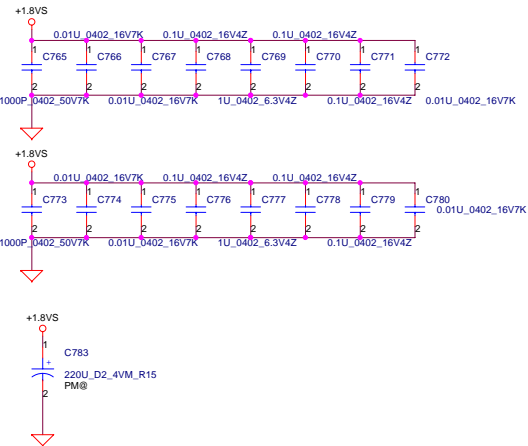
DATA Bus	
Address	0 . . 31 32 . . 63
CMD0	A4
CMD1	RAS*
CMD2	A5
CMD3	BA1
CMD4	A6
CMD5	A0
CMD6	A9
CMD7	CS1* CKE
CMD8	CS0*
CMD9	A11
CMD10	CAS*
CMD11	WE*
CMD12	BA0
CMD13	A1
CMD14	A12
CMD15	RST/ODT
CMD16	A7
CMD17	A10
CMD18	CKE
CMD19	A0
CMD20	A9
CMD21	A6
CMD22	A2
CMD23	A8
CMD24	A3
CMD25	A1
CMD26	A13
CMD27	BA2
CMD28	RFU0
CMD29	RFU1
CMD30	RFU2

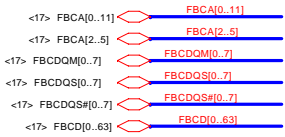


V4:Scan Enable must be to ground



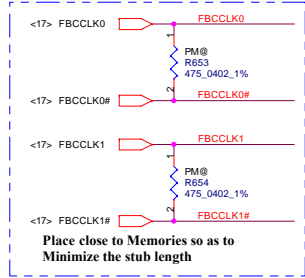
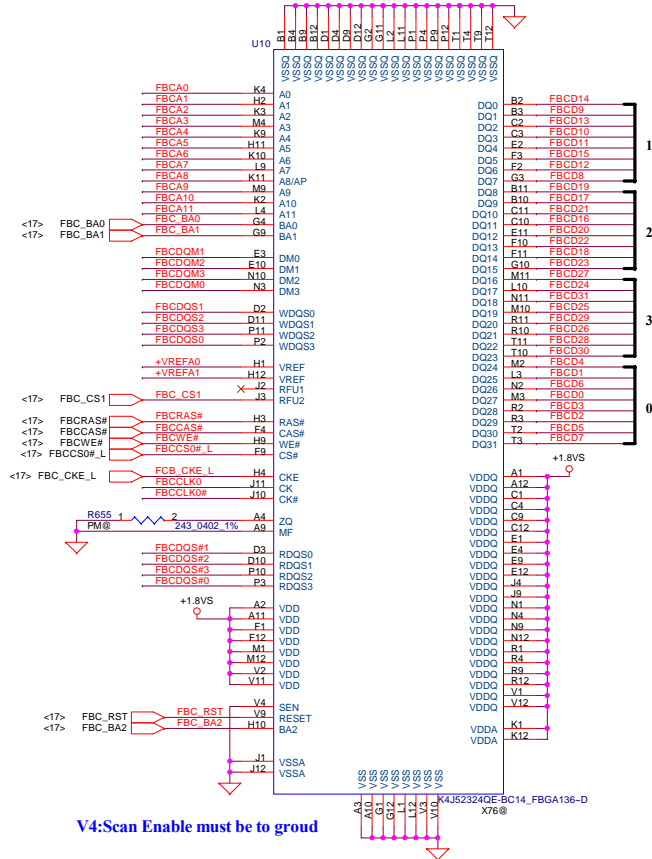
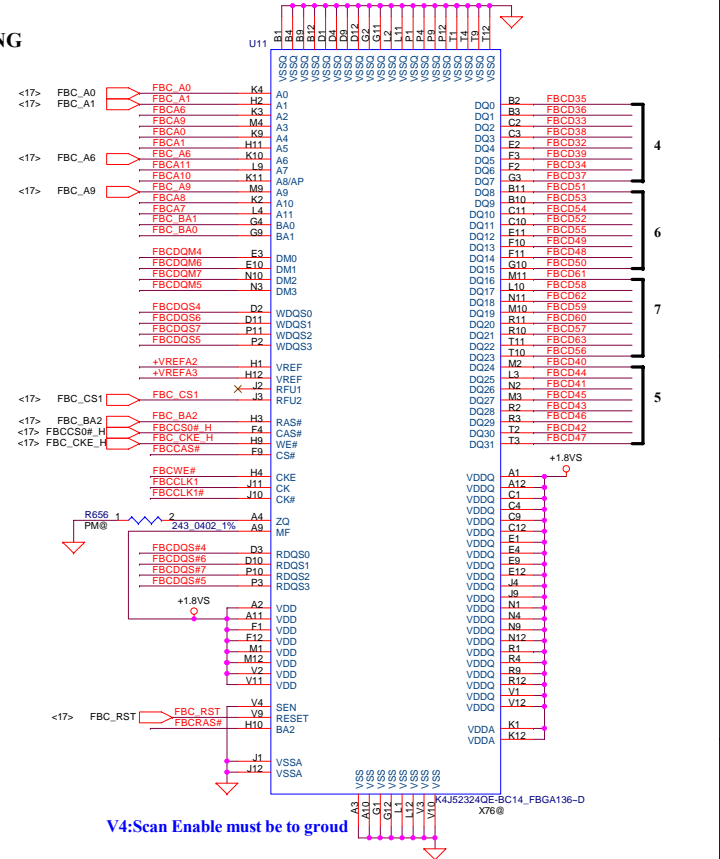
V4:Scan Enable must be to ground





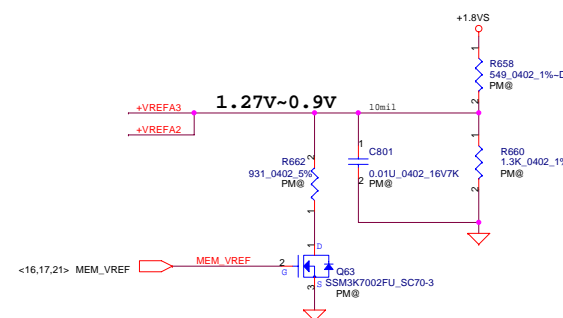
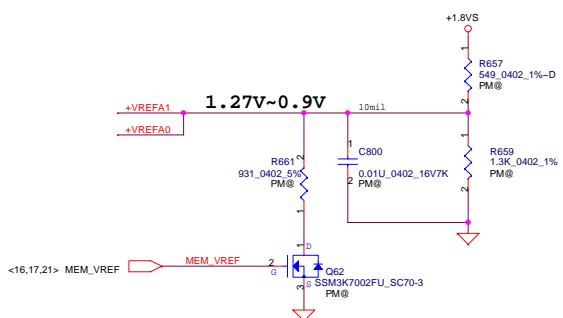
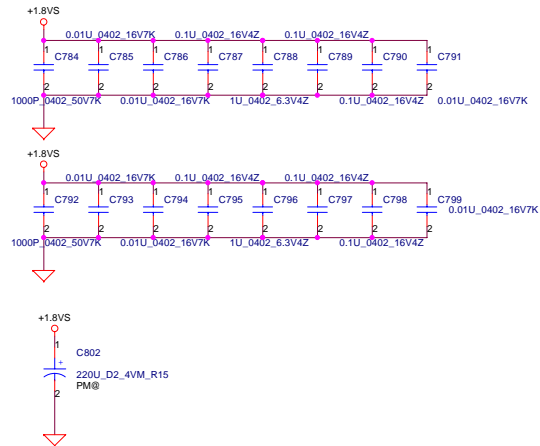
### BGA 84 ADR/CMND MAPPING

Address	DATA Bus	
CMD0	A4	32..63
CMD1	RAS*	BA2
CMD2	A5	
CMD3	BA1	BA0
CMD4		A6
CMD5		A0
CMD6	A9	
CMD7	CS1* <b>CKE</b>	CS1*
CMD8	CS0*	CAS*
CMD9	A11	A11
CMD10	CAS*	CS*
CMD11	WE*	CKE*
CMD12	BA0	BA1
CMD13		A1
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	WE#
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	RAS#
CMD28	RFU0	RFU#
CMD29	RFU1 <b>CS0*</b>	RFU1
CMD30	RFU2	RFU2

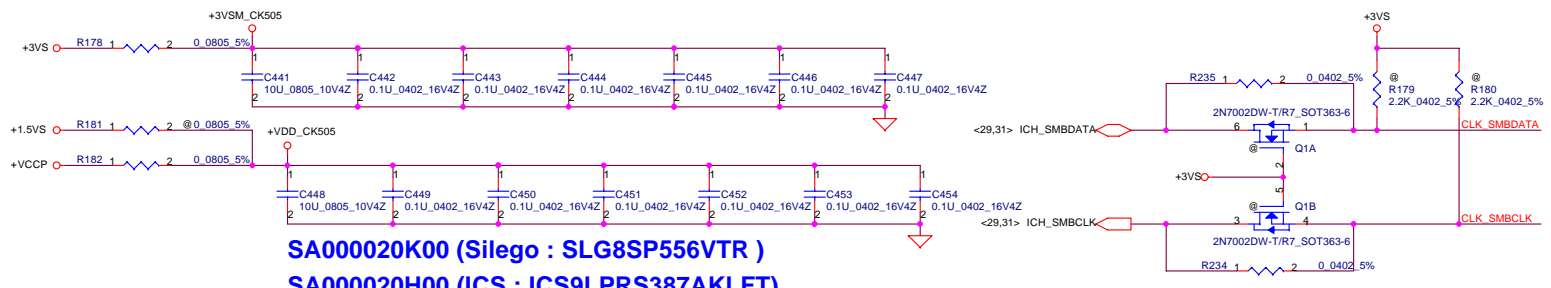


V4:Scan Enable must be to ground

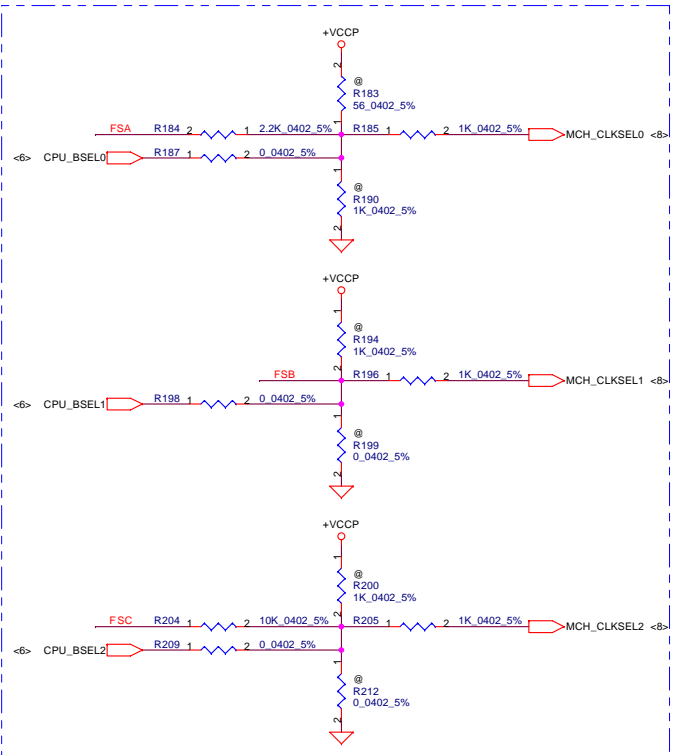
V4:Scan Enable must be to ground



FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



**SA000020K00 (Silego : SLG8SP556VTR )**  
**SA000020H00 (ICS : ICS9LPRS387AKLFT)**

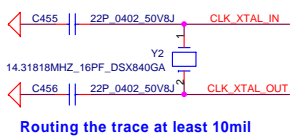
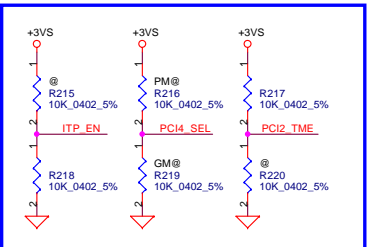


**SRC PORT LIST**

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN2
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

**REQ PORT LIST**

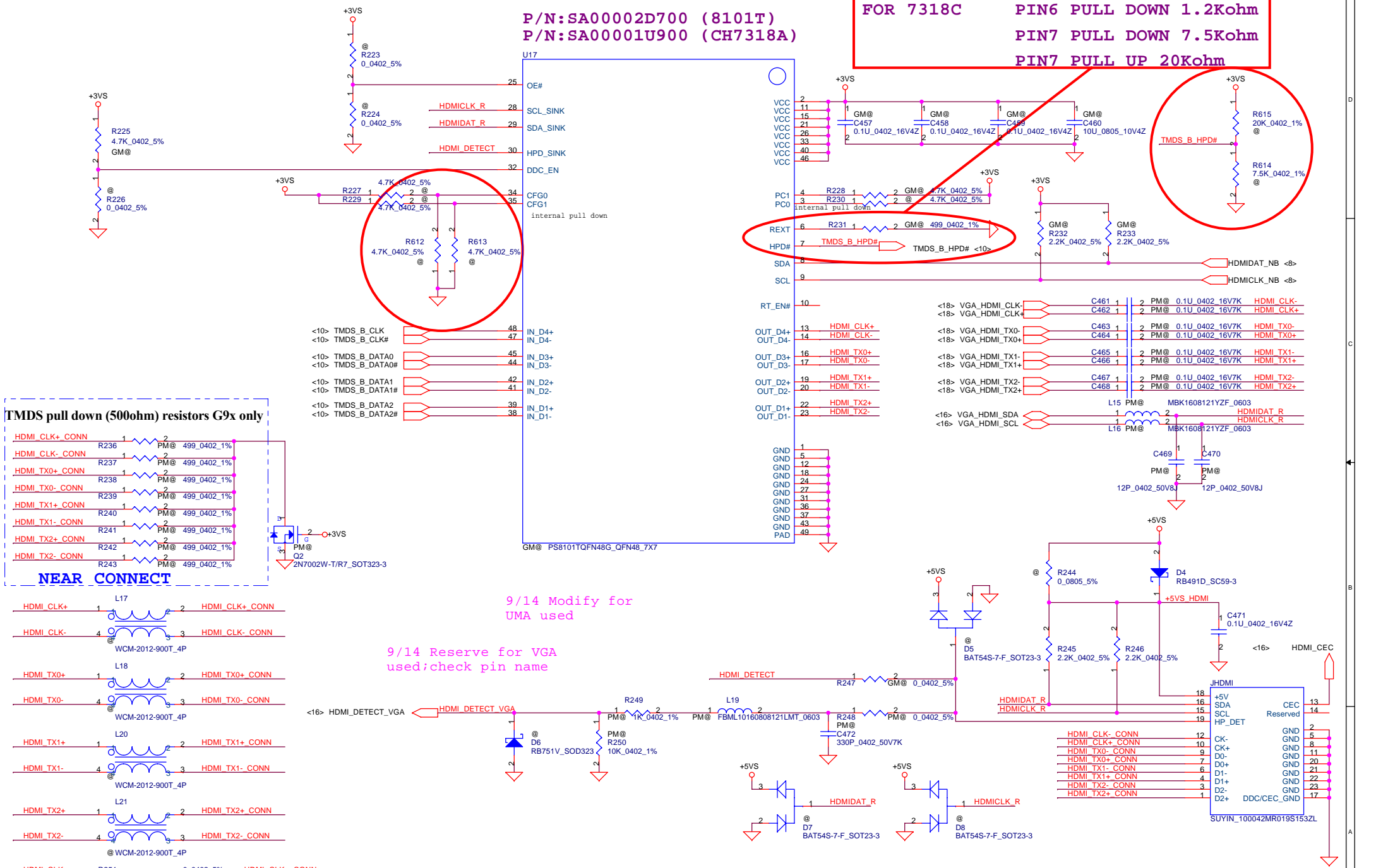
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL



For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
 Pin28/29 : LCDCLK / LCDCLK#  
 1 = Pin24/25 : SRC\_0 / SRC\_0#  
 Pin28/29 : 27M/27M\_SS

P/N:SA00002D700 (8101T)  
P/N:SA00001U900 (CH7318A)

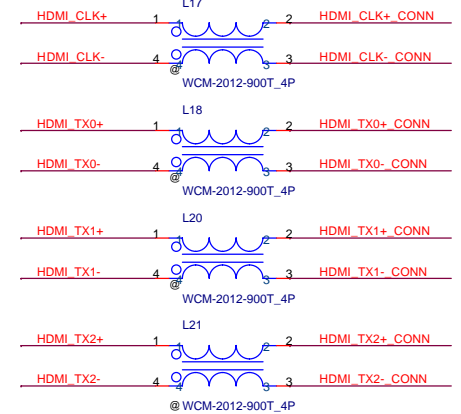
FOR 7318C  
PIN6 PULL DOWN 1.2Kohm  
PIN7 PULL DOWN 7.5Kohm  
PIN7 PULL UP 20Kohm



TMDs pull down (500ohm) resistors G9x only

- HDMI\_CLK+\_CONN R236 1 2 PM@ 499\_0402\_1%
- HDMI\_CLK-\_CONN R237 1 2 PM@ 499\_0402\_1%
- HDMI\_TX0+\_CONN R238 1 2 PM@ 499\_0402\_1%
- HDMI\_TX0-\_CONN R239 1 2 PM@ 499\_0402\_1%
- HDMI\_TX1+\_CONN R240 1 2 PM@ 499\_0402\_1%
- HDMI\_TX1-\_CONN R241 1 2 PM@ 499\_0402\_1%
- HDMI\_TX2+\_CONN R242 1 2 PM@ 499\_0402\_1%
- HDMI\_TX2-\_CONN R243 1 2 PM@ 499\_0402\_1%

NEAR CONNECT



- HDMI\_CLK+ R251 1 2 0 0402 5% HDMI\_CLK+\_CONN
- HDMI\_CLK- R252 1 2 0 0402 5% HDMI\_CLK-\_CONN
- HDMI\_TX0+ R253 1 2 0 0402 5% HDMI\_TX0+\_CONN
- HDMI\_TX0- R254 1 2 0 0402 5% HDMI\_TX0-\_CONN
- HDMI\_TX1+ R255 1 2 0 0402 5% HDMI\_TX1+\_CONN
- HDMI\_TX1- R256 1 2 0 0402 5% HDMI\_TX1-\_CONN
- HDMI\_TX2+ R257 1 2 0 0402 5% HDMI\_TX2+\_CONN
- HDMI\_TX2- R258 1 2 0 0402 5% HDMI\_TX2-\_CONN

9/14 Modify for UMA used

9/14 Reserve for VGA used; check pin name

Security Classification	Compal Secret Data	
Issued Date	2008/03/25	Deciphered Date
		2008/04/

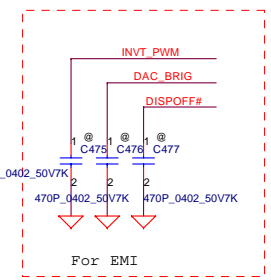
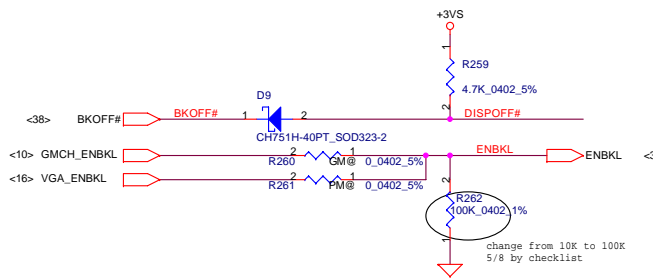
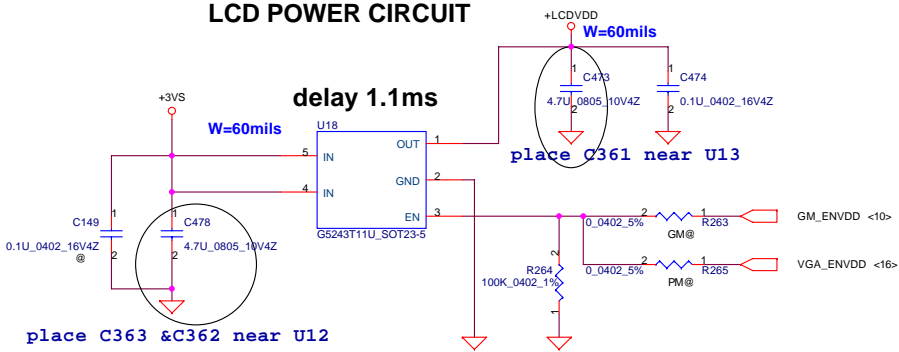
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Compal Electronics, Ltd.  
Title: Level Shifter\_PS8101T

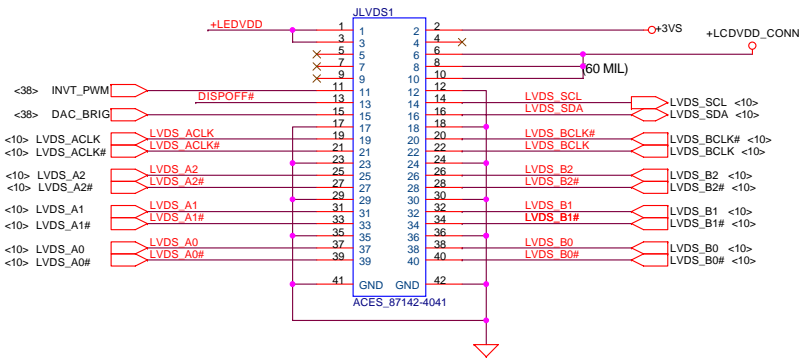
Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1
Date:	Monday, June 30, 2008	Sheet 24 of 52



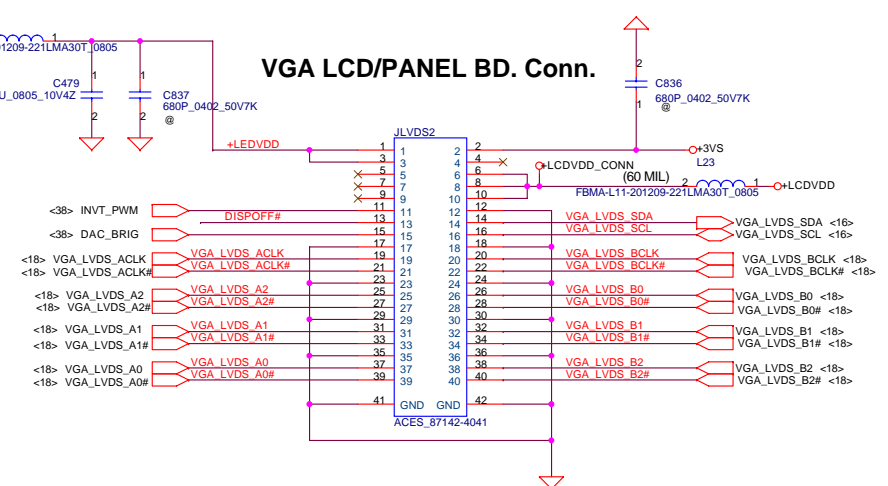
### LCD POWER CIRCUIT



### UMA LCD/PANEL BD. Conn.



### VGA LCD/PANEL BD. Conn.

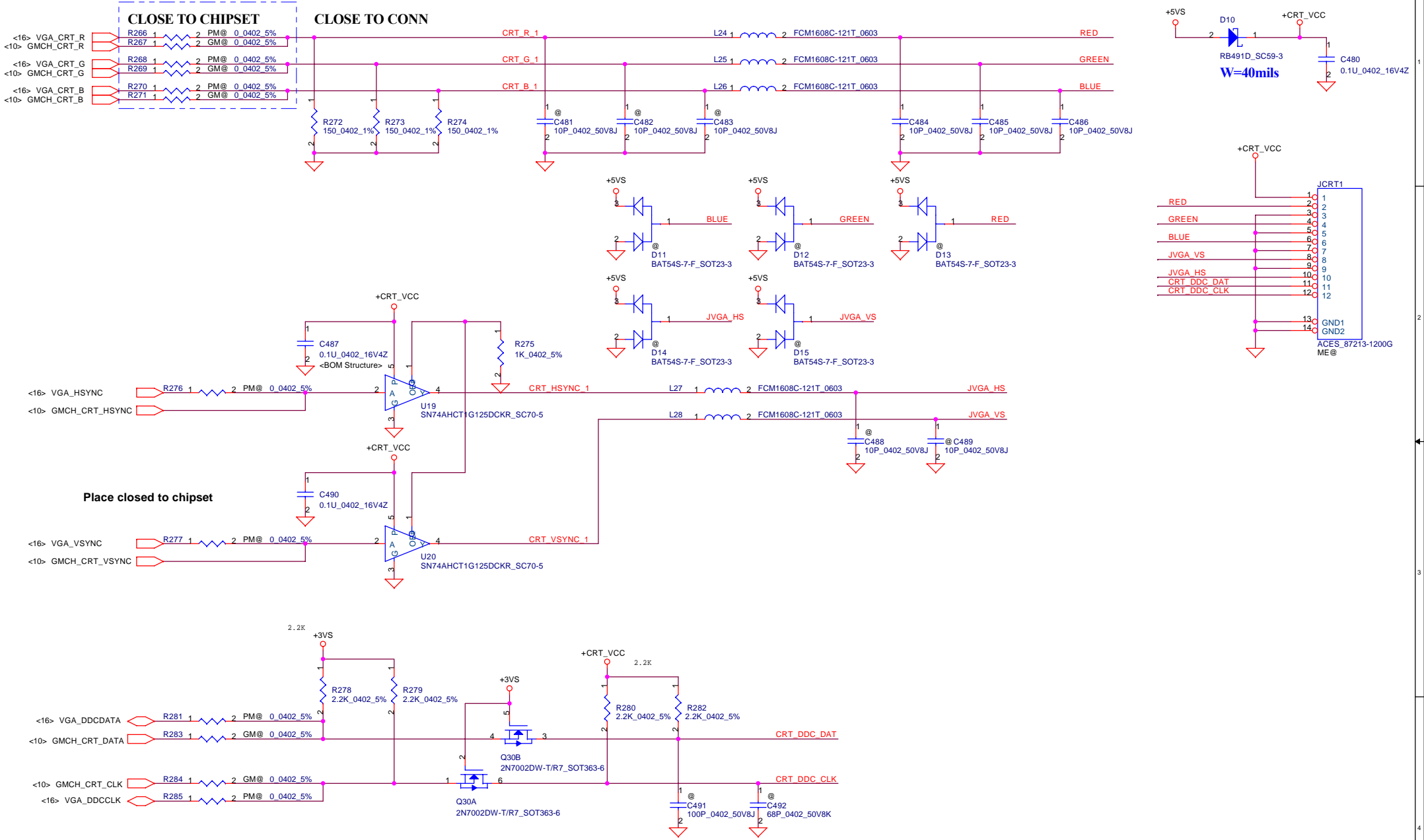


+LCDVDD

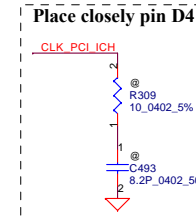
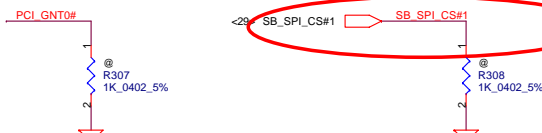
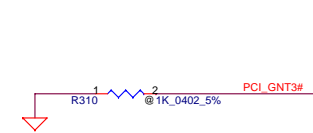
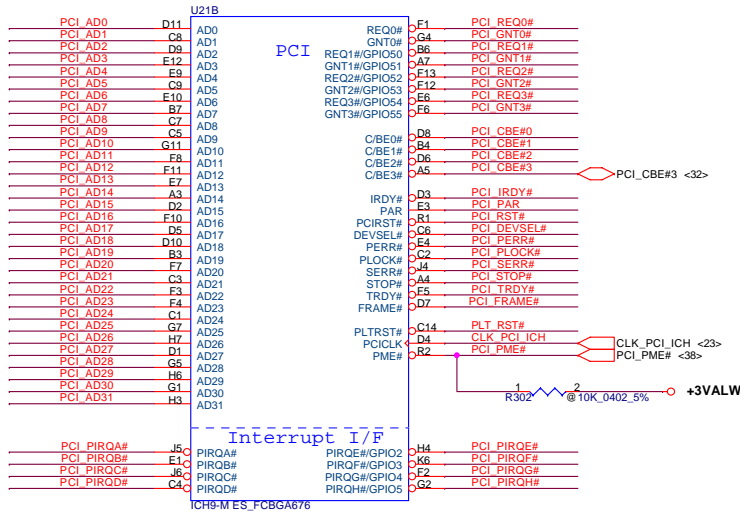
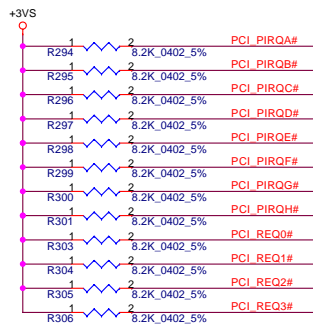
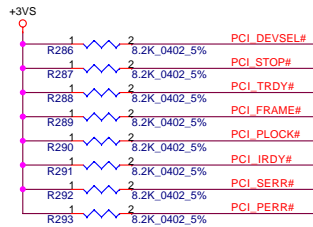
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Issued Date	2007/10/15	Deciphered Date	2008/10/15
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Title			
<b>Compal Electronics, Inc.</b>			
<b>LVDS &amp; DVI Connector</b>			
Size	Document Number	Rev	
B	<b>KIWB1/B2_LA4601P</b>	0.1	
Date:	Monday, June 30, 2008	Sheet	25 of 52

# CRT Connector

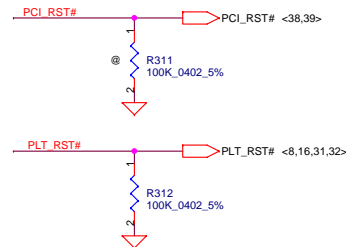


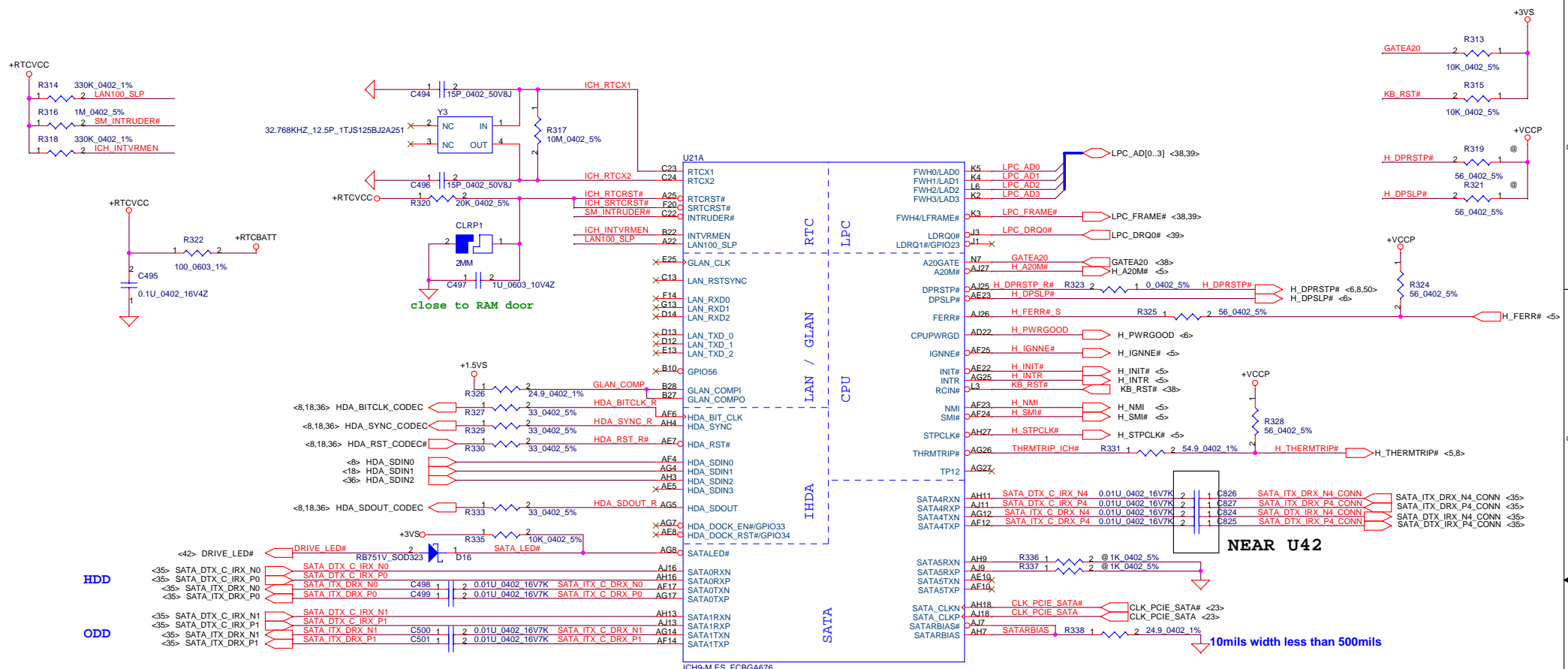
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b> <b>CRT &amp; TV-OUT Connector</b>	
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				Custom	0.1
				Document Number <b>KIWBI/B2_LA4601P</b>	
				Date:	Monday, June 30, 2008
				Sheet	26 of 52



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPL_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



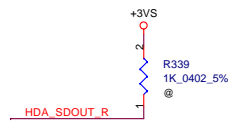


close to RAM door

NEAR U42

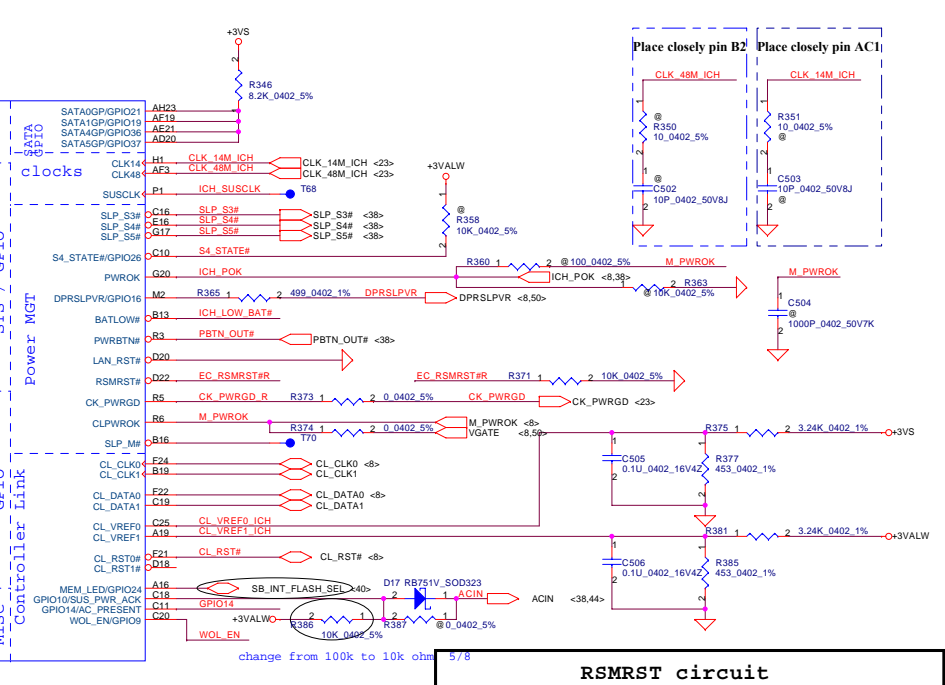
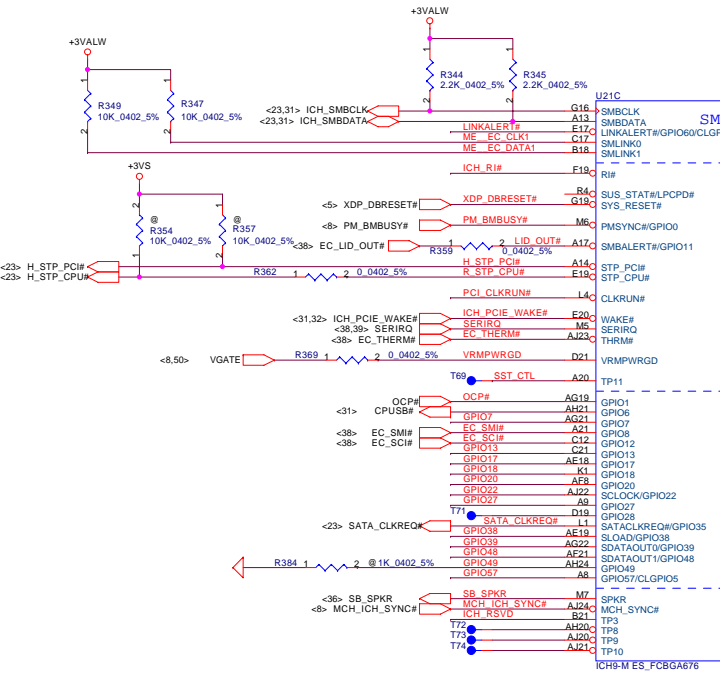
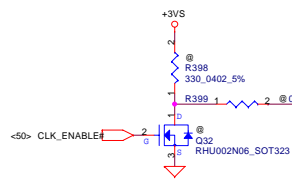
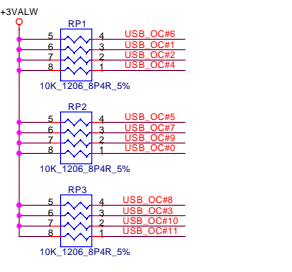
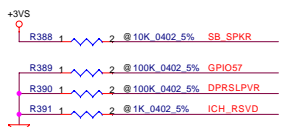
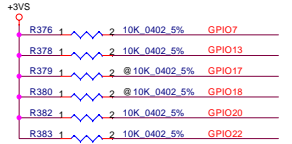
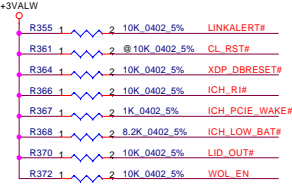
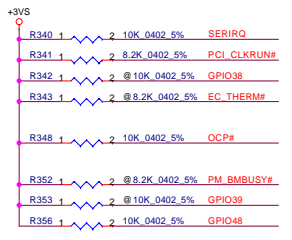
10mils width less than 500mils

Need check

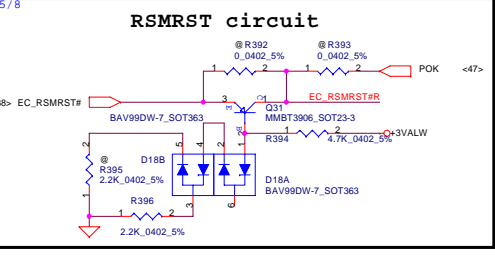
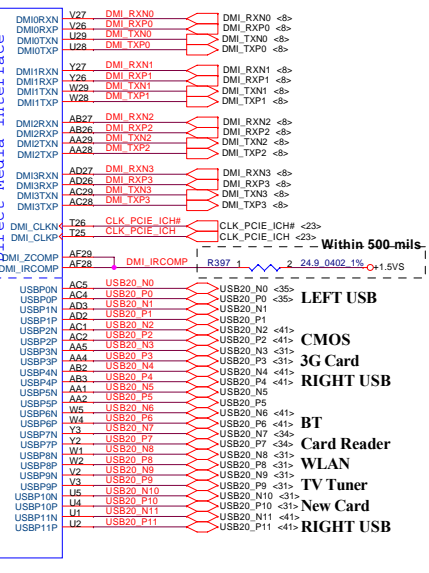
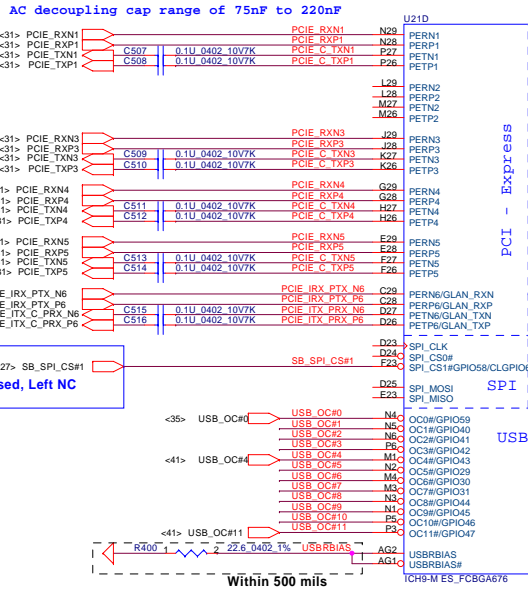


XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
2	X
3	X
4	ESATA
5	X

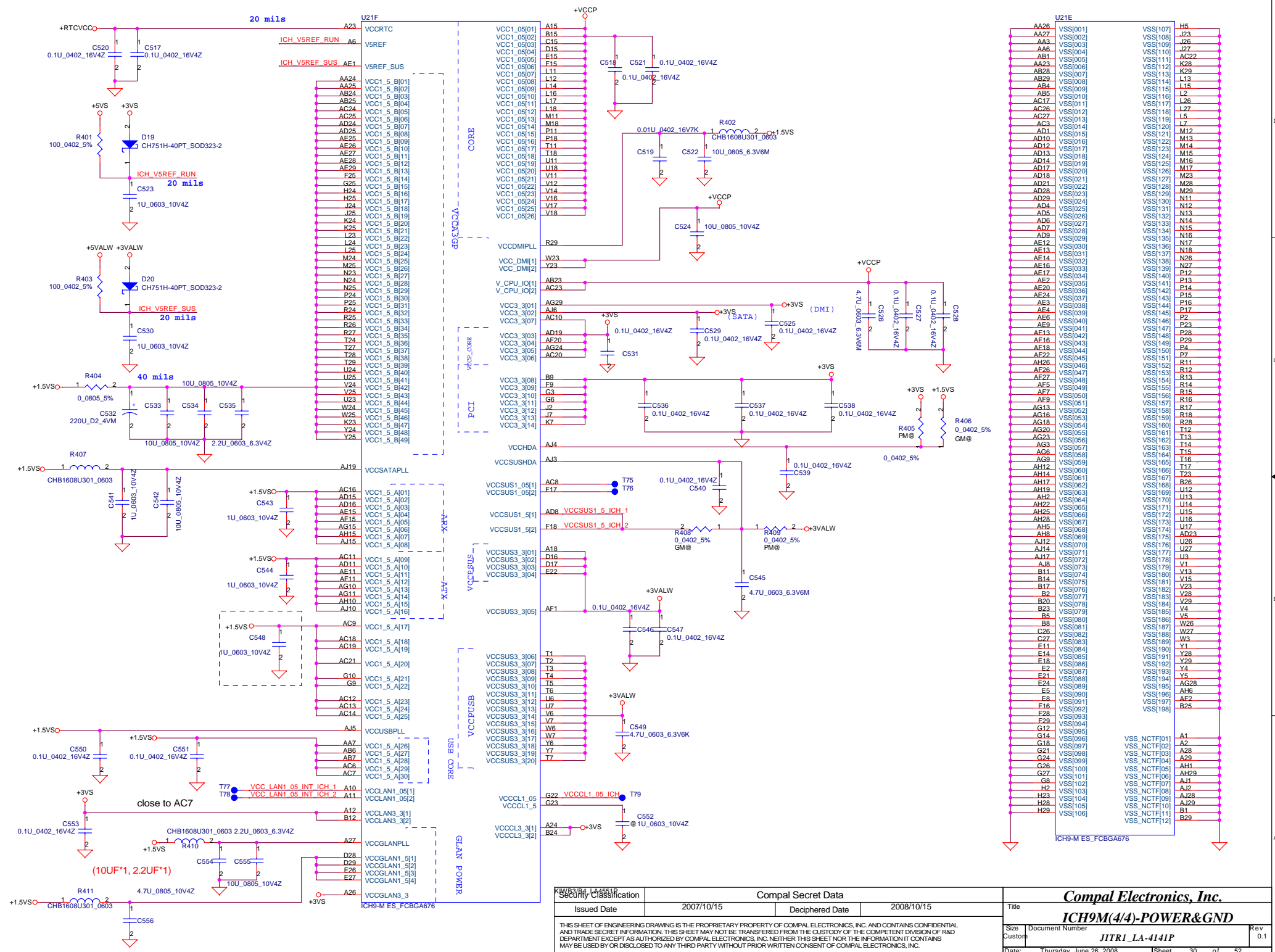


low-->default  
High -->No boot



PORT	DEVICE
1	3G
2	WLAN
3	NEW CARD
4	TV TUNNER
5	LAN

PORT	DEVICE
0	LEFT SIDE
1	CMOS
2	3G
3	RIGHT SIDE
4	BT
5	CARD READER
6	WIRELESS
7	TV TUNNER
8	NEW CARD
9	RIGHT SIDE



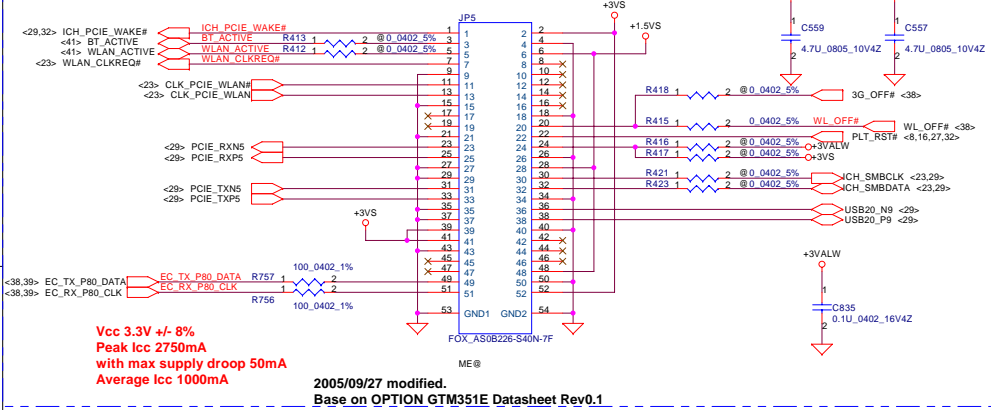
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Title		<b>Compal Electronics, Inc.</b>	
		<b>ICH9M(4/4)-POWER&amp;GND</b>	
Size	Document Number		
Custom	<b>JITRI_LA-4141P</b>		
Date:	Thursday, June 26, 2008	Sheet	30 of 52
		Rev	0.1

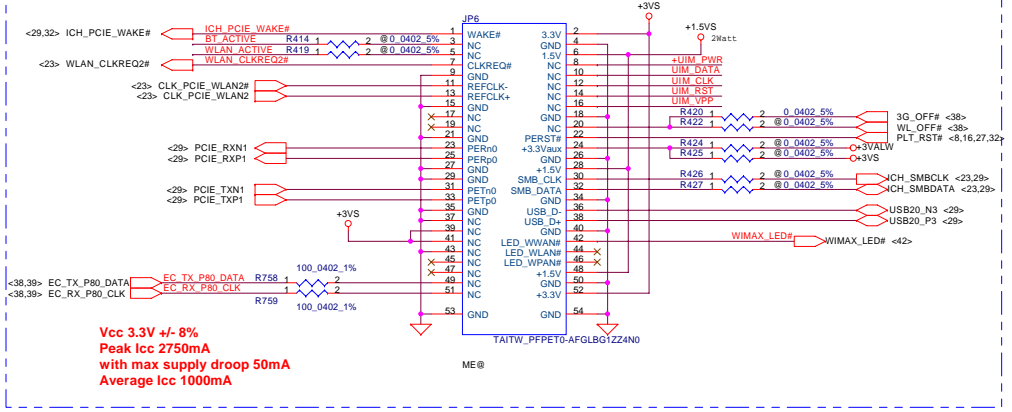
# Mini-Express Card for 3G Or TV Tuner

## Mini-Express Card for WLAN

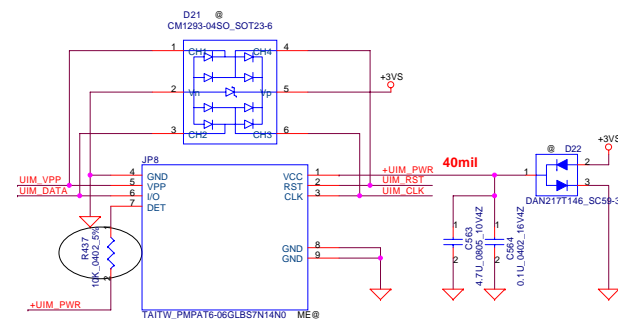
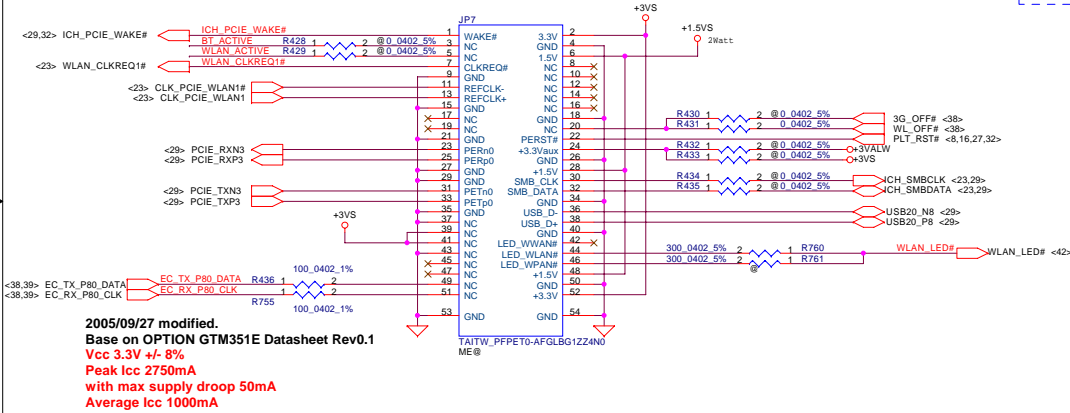
### Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high



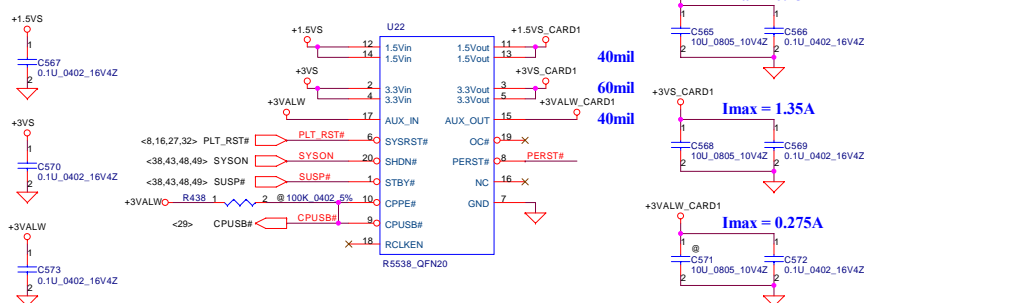
### Mini-Express Card(Slot 3-WWAN 3G) 5.6mm high



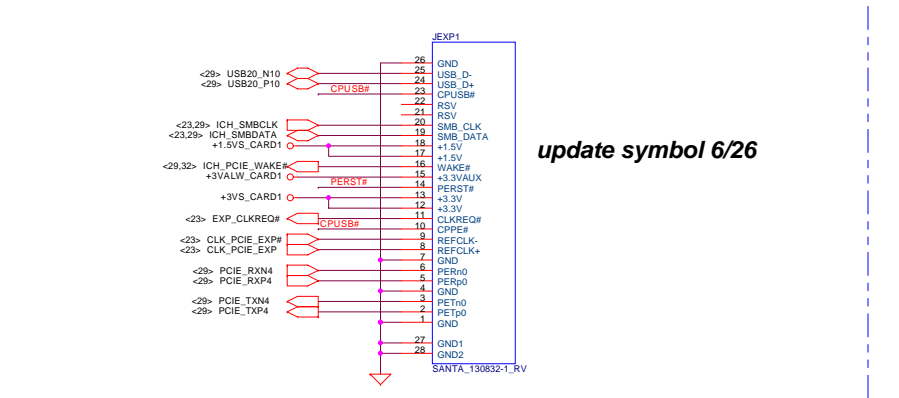
### Mini-Express Card(Slot 2-WIRELESS) 5.6mm high



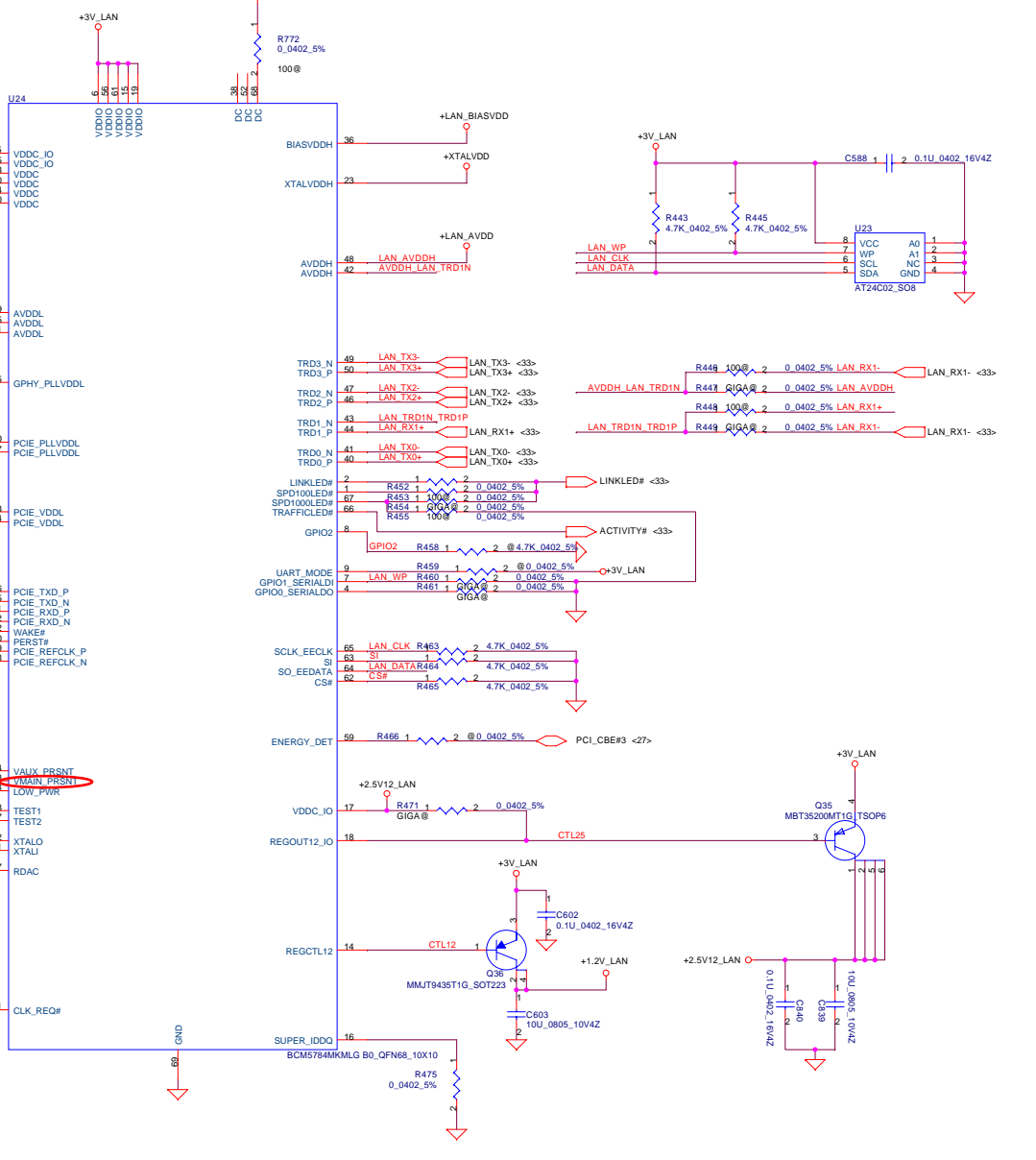
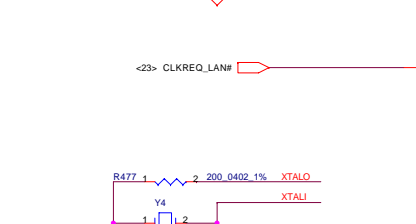
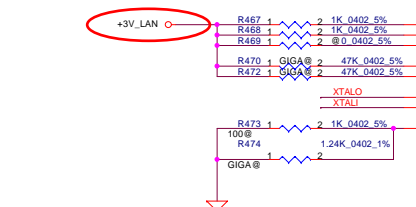
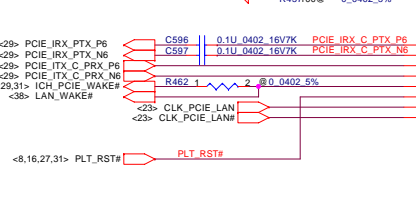
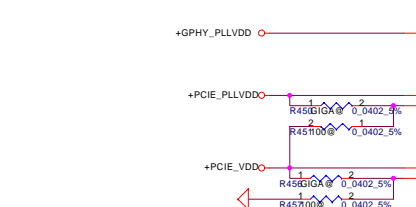
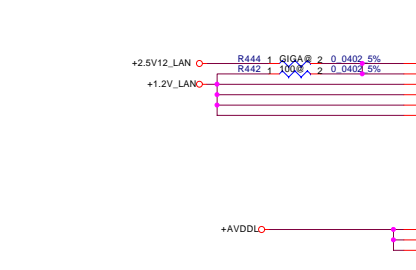
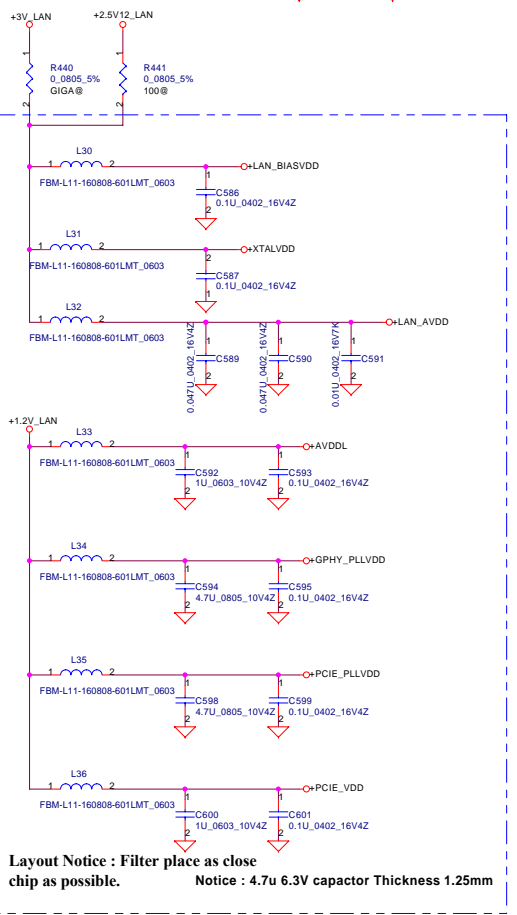
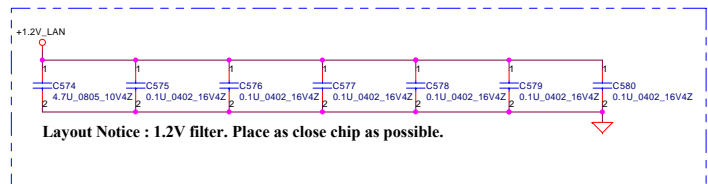
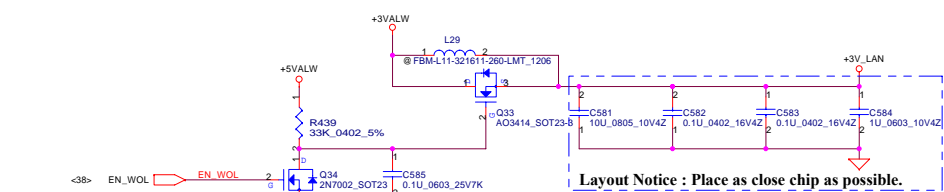
### Express Card Power Switch



### New Card 34mm Socket (Left/TOP)



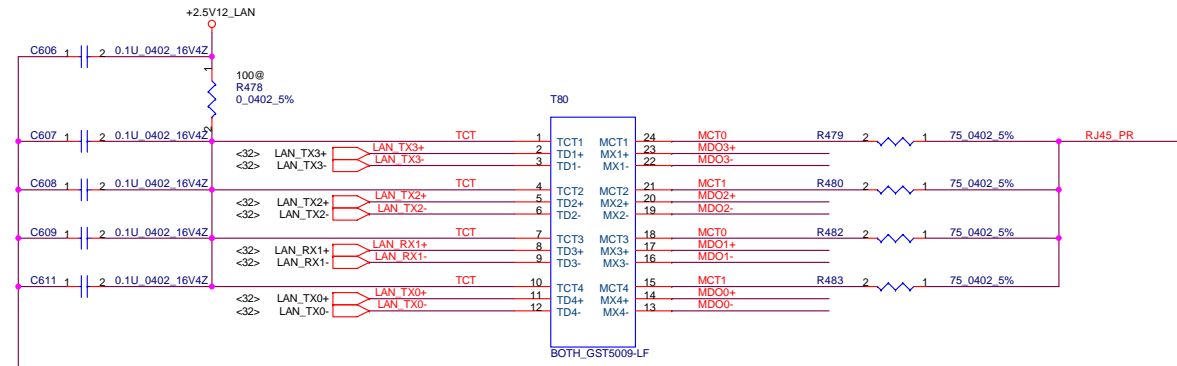
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	
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Title	Mini-Card/3G/FeliCa/BT		Size	Document Number
			J1TR1_LA-4141P	Rev 0.1
Date:	Monday, June 30, 2008	Sheet	31	of 52



Layout Notice : Filter place as close chip as possible. Notice : 4.7u 6.3V capacitor Thickness 1.25mm

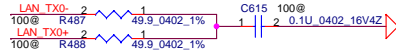
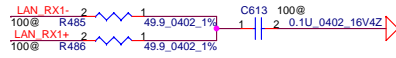
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Issued Date	2008/03/25	Deciphered Date	2008/04/
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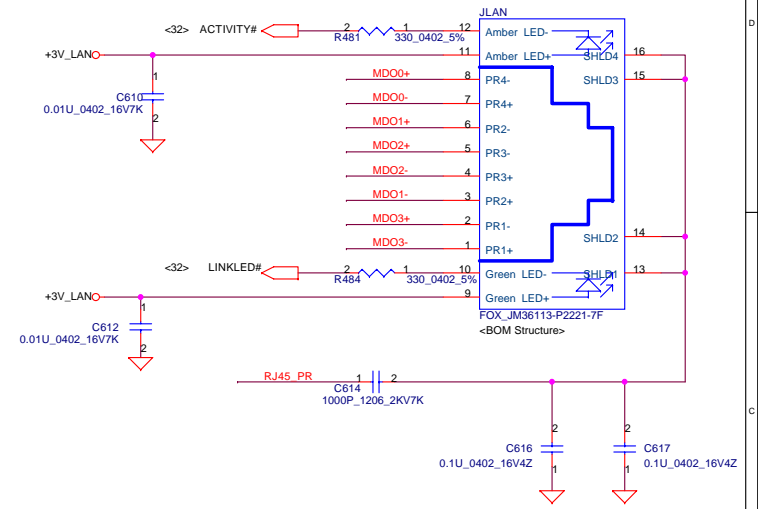


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

**near LAN controller**

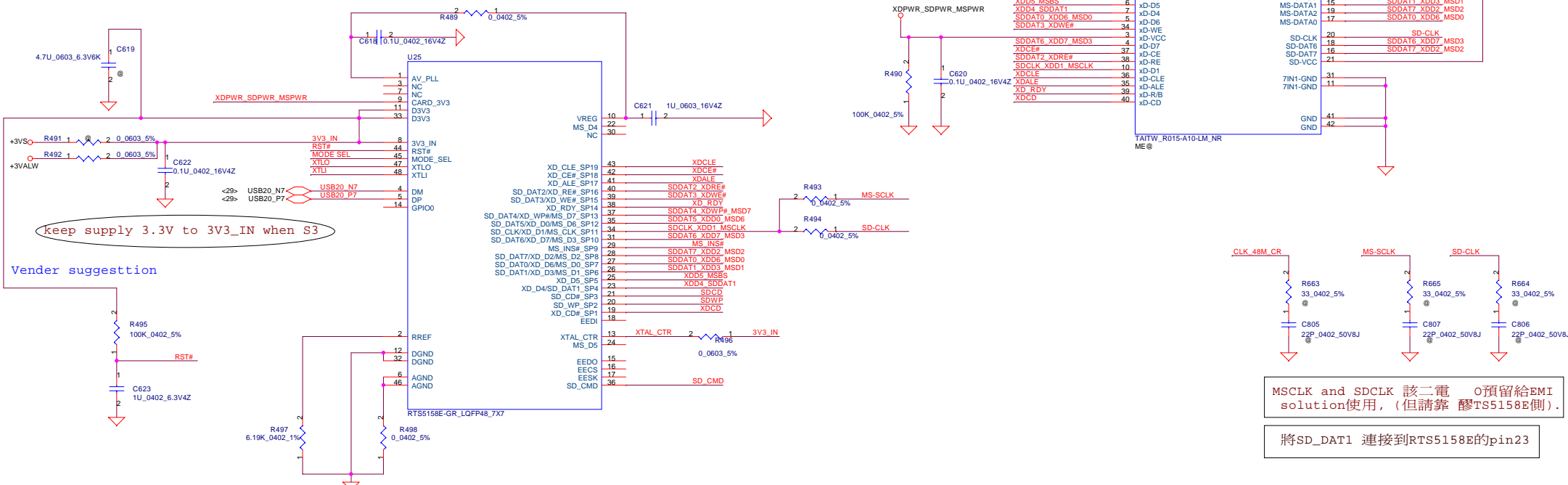


**RJ11+RJ45 CONN**

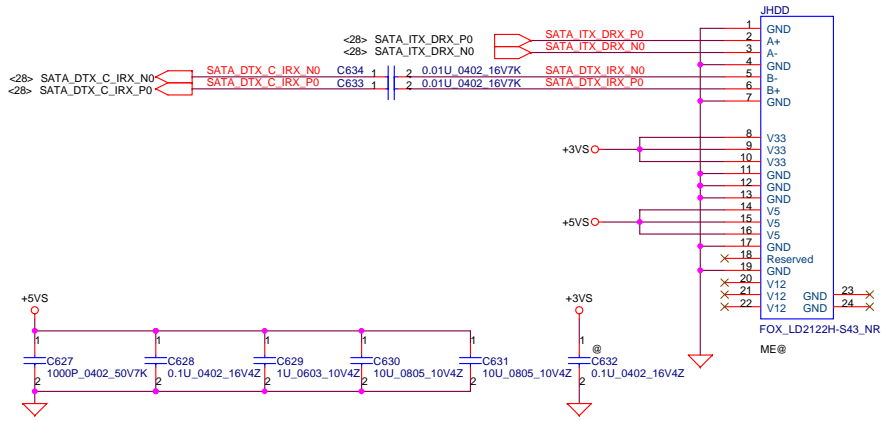


Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b> <b>LAN CONTROLLER</b>	
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				Custom	<b>KIWB1/B2_LA4601P</b> Rev 0.1
				Date:	Monday, June 30, 2008
				Sheet	33 of 52

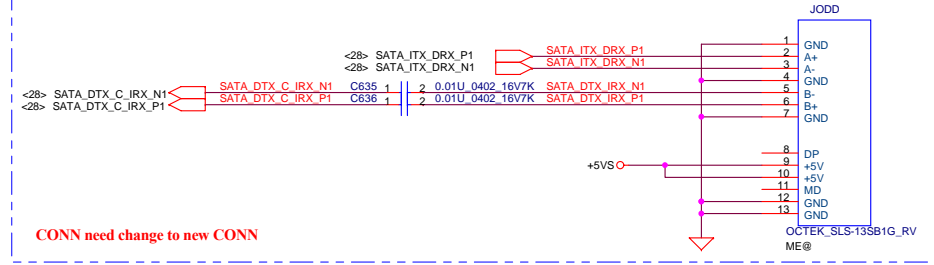
0513 : CARD\_3V3 旁路電阻 100K change to 4.7u CAP==>預留  
 0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,  
 change C526 form 1u to 4.7u



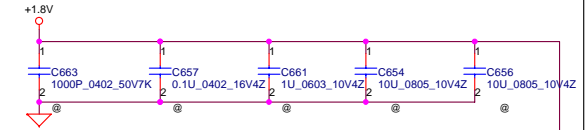
### SATA HDD Conn.



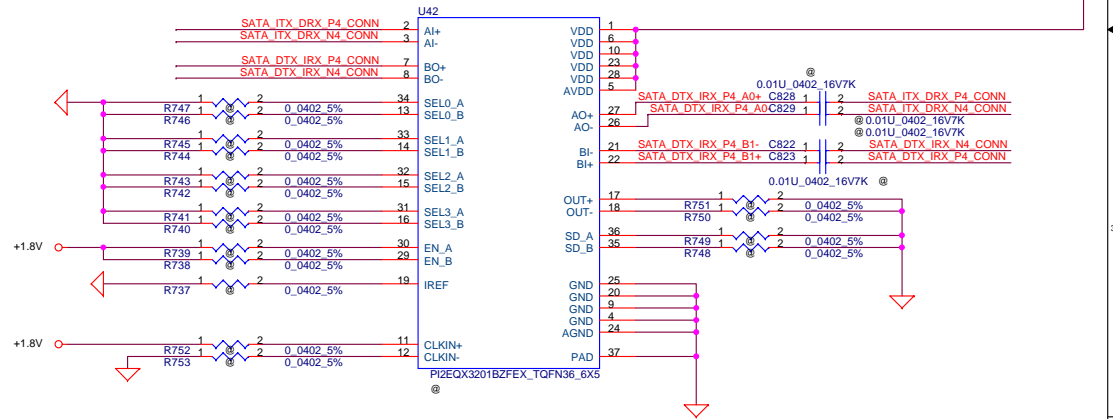
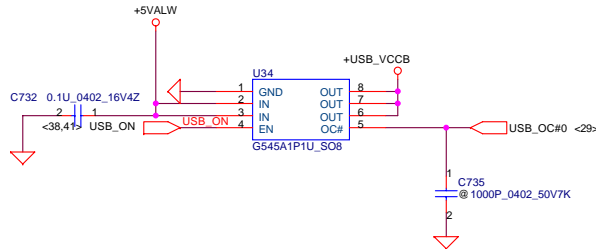
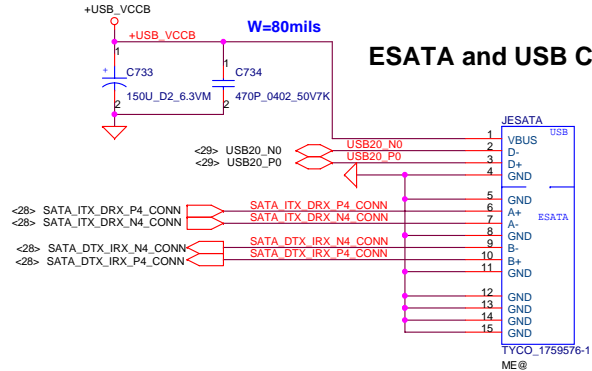
### SATA ODD Conn.



CONN need change to new CONN



### ESATA and USB Conn.



#### OUTPUT SWING CONTROL

SEL2_[A:B]	SWING
0	1X
1	1.2X

#### OUTPUT DE-EMPHASIS ADJUSTMENT

SEL3_[A:B]	DE-EMPHASIS
0	9dB
1	-3.5dB

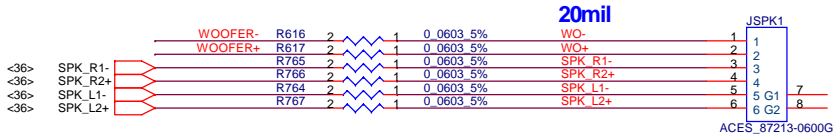
#### EQUALIZER SELECTION

SEL3_[A:B]	DE-EMPHASIS	COMPLIANCE CHANNEL
0	0	NO EQUALIZATION
1	1	[0:2.5dB]@1.6GHz
1	0	[2.5:4.5dB]@1.6GHz
1	1	[4.5:6.5dB]@1.6GHz

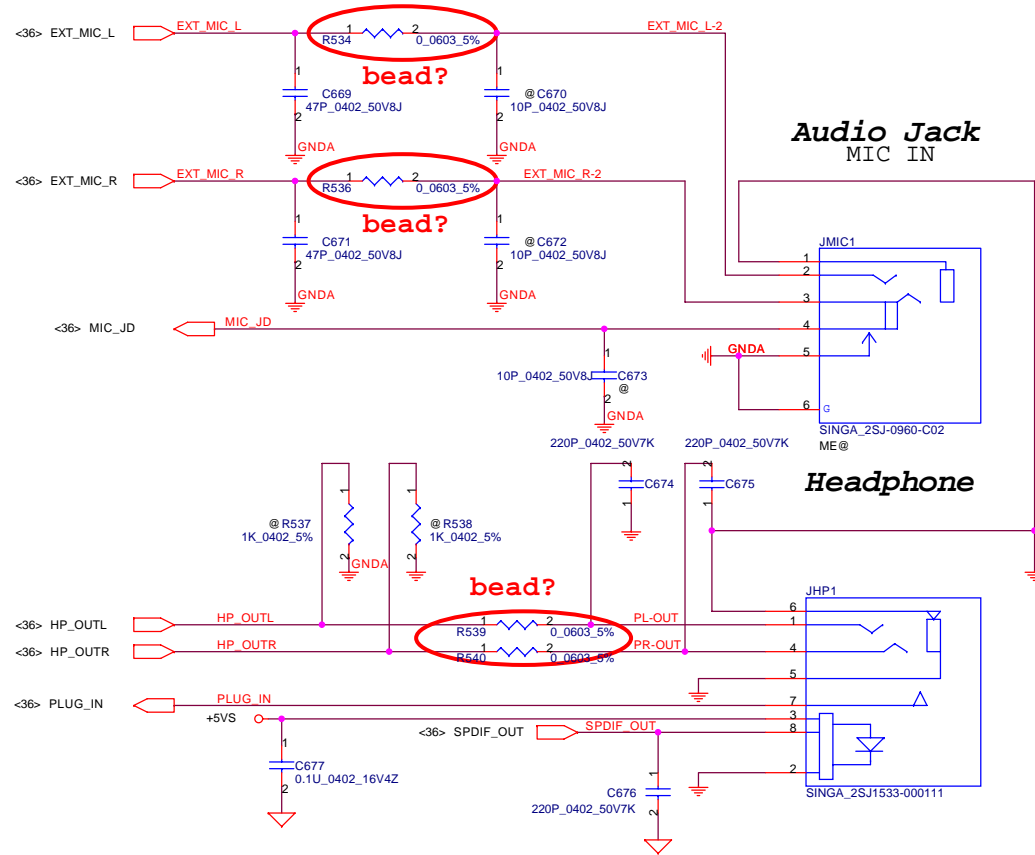
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>HDD &amp; ODD Connector</b>	
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Size B	Document Number	Rev		Date	
	<b>KIWB1/B2_LA4601P</b>	0.1		Monday, June 30, 2008	
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**SubWoofer Conn.  
Speaker Connector**

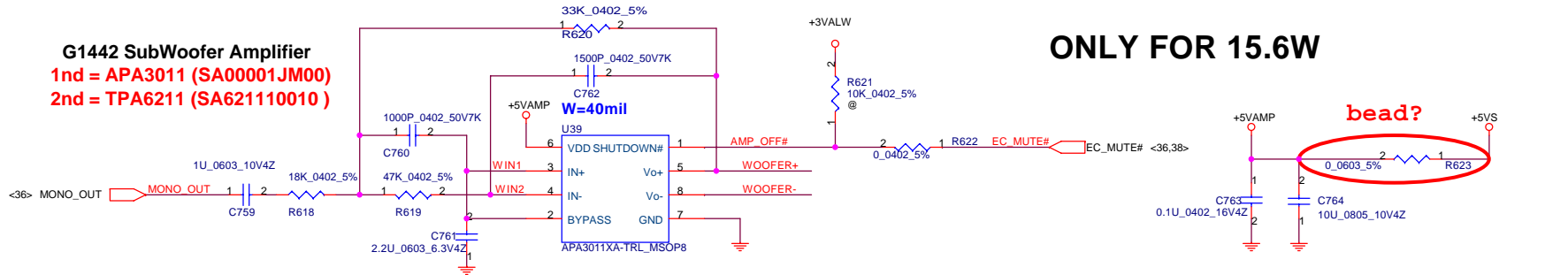


**Audio Jack**



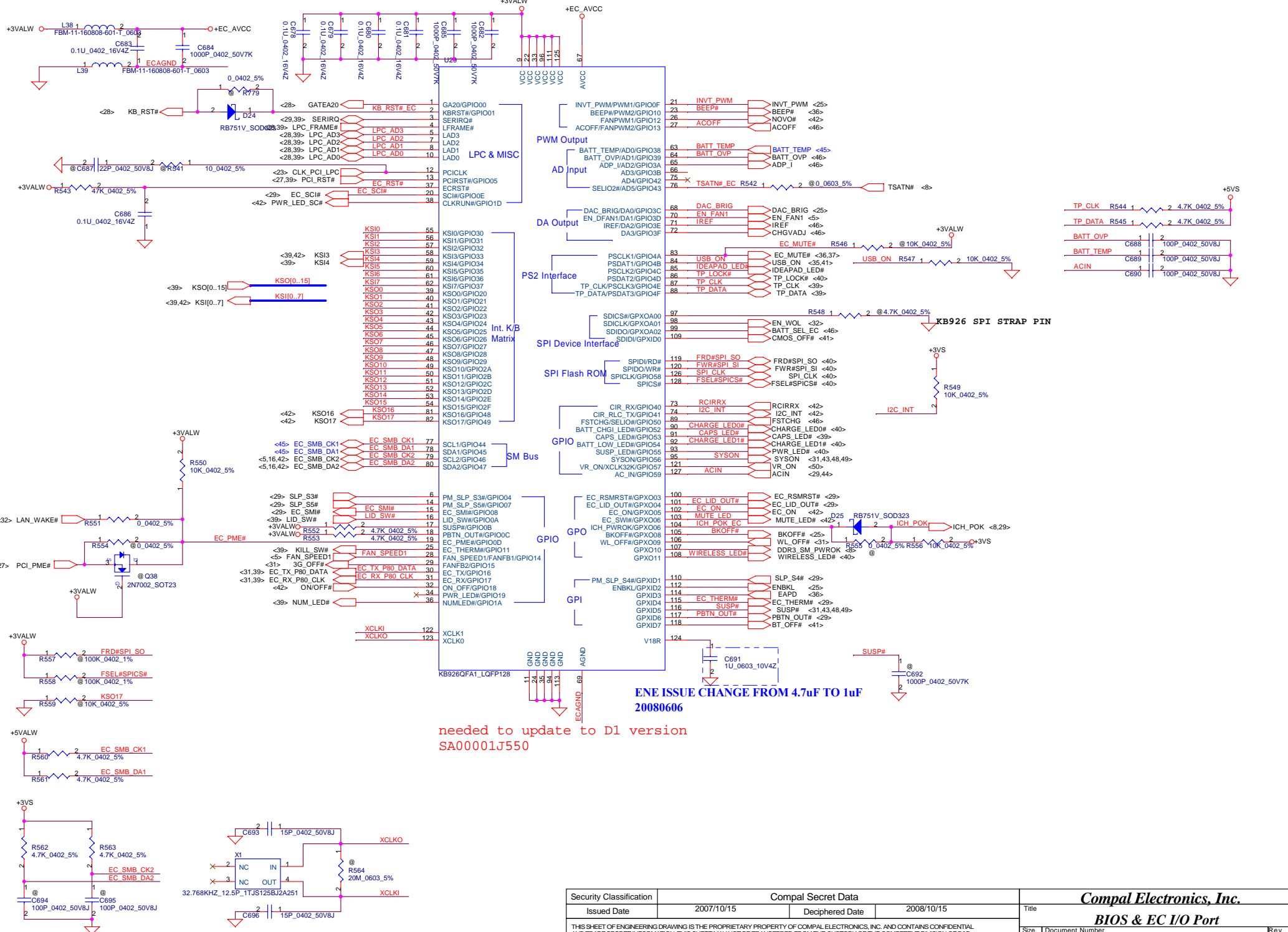
**G1442 SubWoofer Amplifier**

1nd = APA3011 (SA00001JM00)  
2nd = TPA6211 (SA621110010)



**ONLY FOR 15.6W**

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Size	Document Number			Rev	0.1
Custom	KIWB1/B2_LA4601P			Date:	Monday, June 30, 2008
				Sheet	37 of 52



ENE ISSUE CHANGE FROM 4.7uF TO 1uF  
20080606

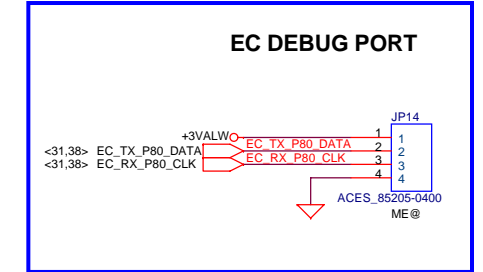
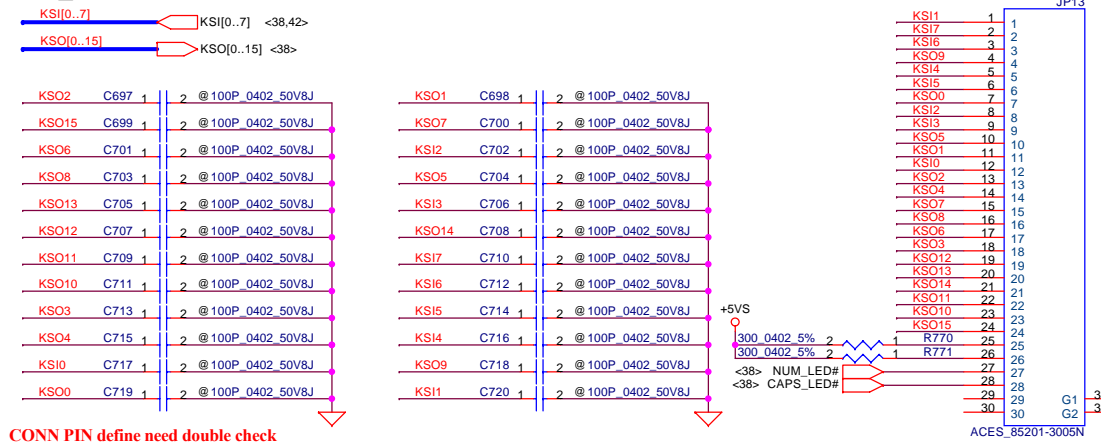
needed to update to D1 version  
SA00001J550

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>BIOS &amp; EC I/O Port</b>
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Size	Document Number	Rev		0.1
Customer	JITR1_LA-4141P			
Date	Monday, June 30, 2008	Sheet	38	of 52

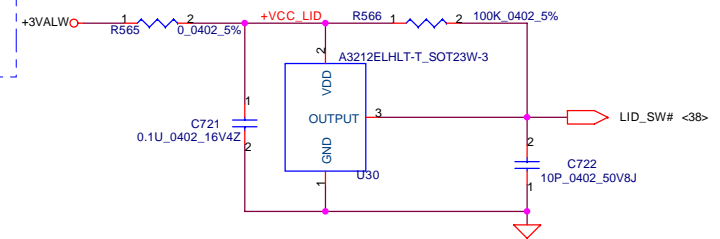
Compal Electronics, Inc.

JITR1\_LA-4141P

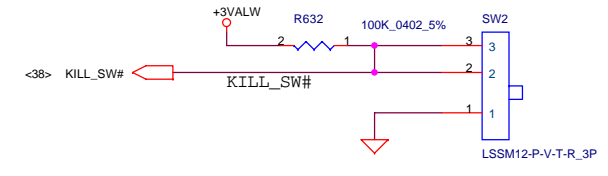
### INT\_KBD Conn.



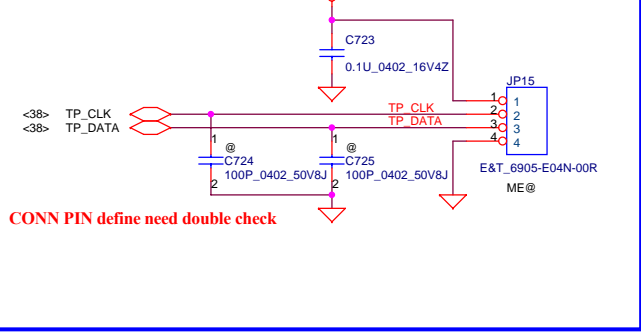
### Lid Switch



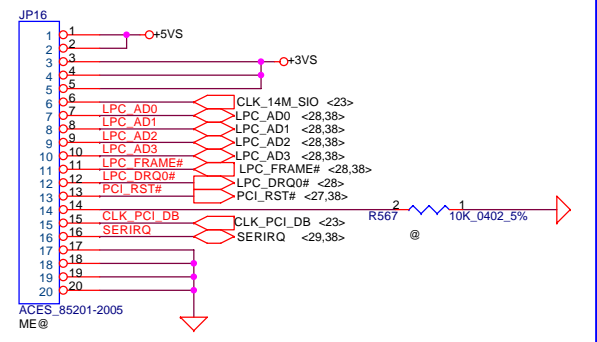
### Kill Switch



### To TP/B Conn.

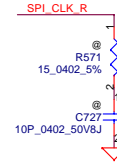
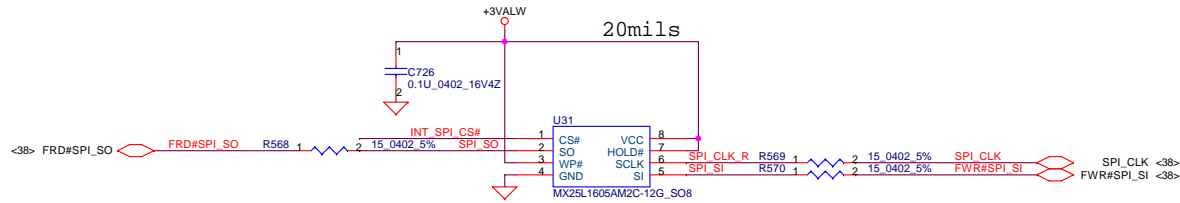


### FOR LPC SIO DEBUG PORT

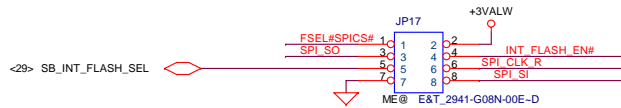
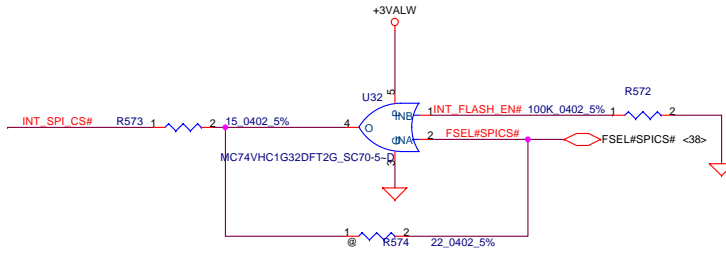


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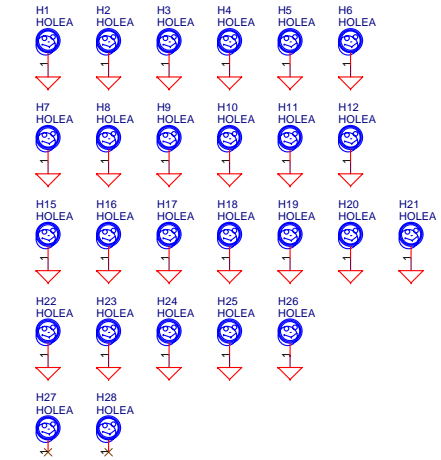
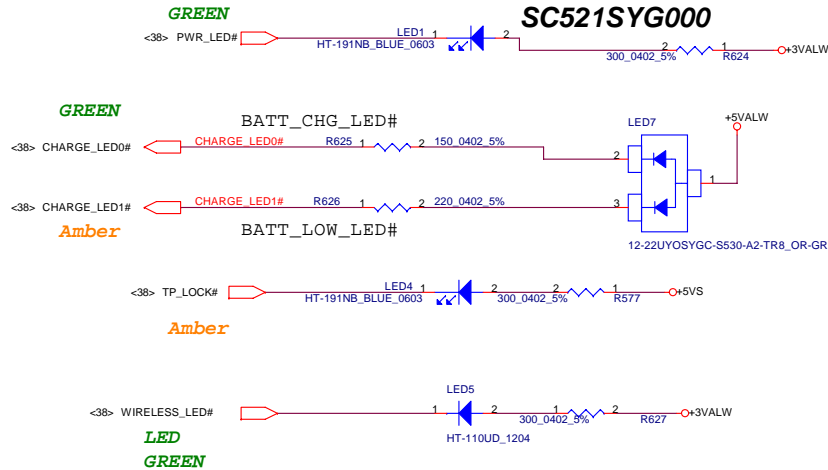
FOR EC 16M SPI ROM



INPUT		OUTPUT Y
A	B	
L	L	L
H	L	H
L	H	H
H	H	H

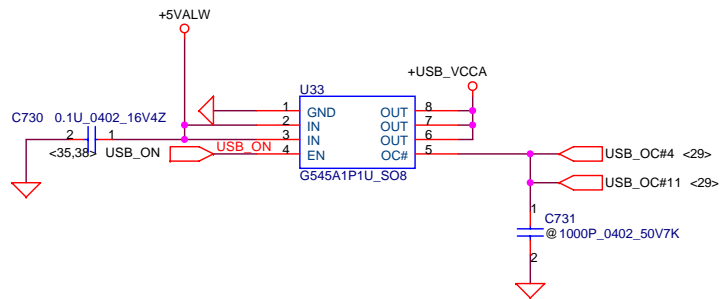


LED

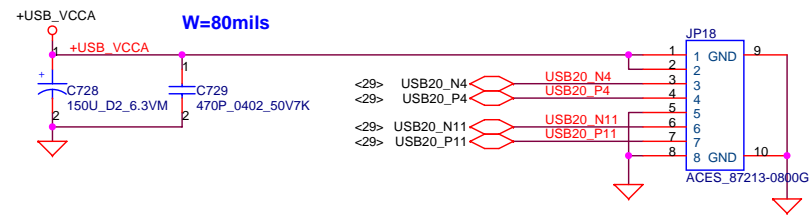


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Size	Document Number		Rev	
B	KIWB1/B2_LA4601P		0.1	
Date:	Monday, June 30, 2008	Sheet	40	of 52

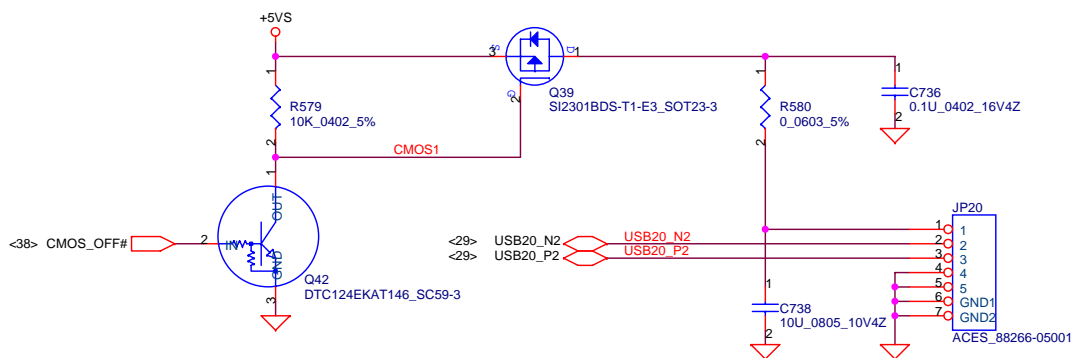




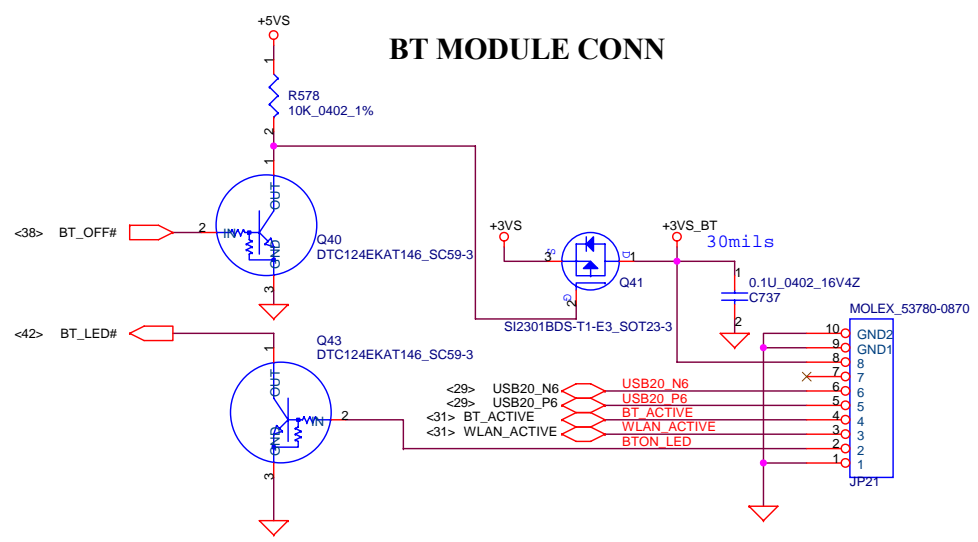
### USB Board Conn. 10 pin



### CMOS Camera Conn

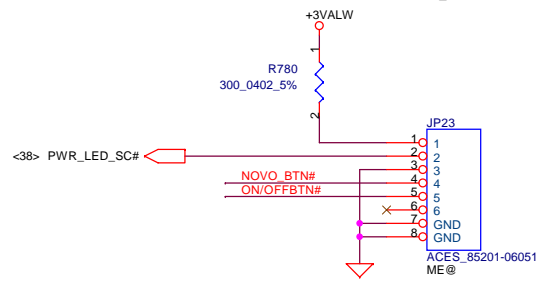


### BT MODULE CONN

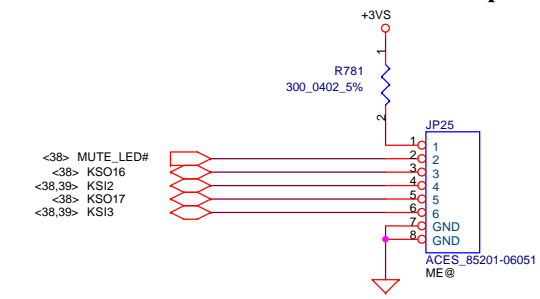


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Size	Document Number	Rev		Date	
Custom	KIWB1/B2_LA4601P	0.1		Monday, June 30, 2008	
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### Power Bottom Board Conn. 5 pin

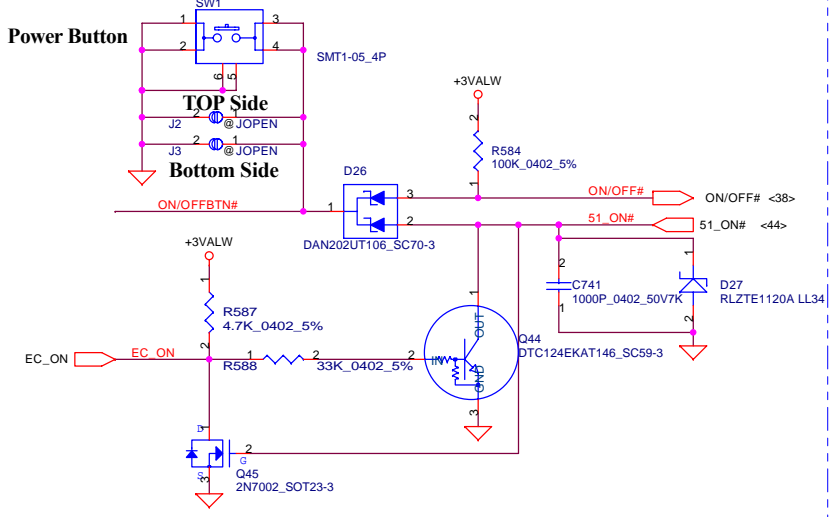


### Bottom Board Conn. 6 pin

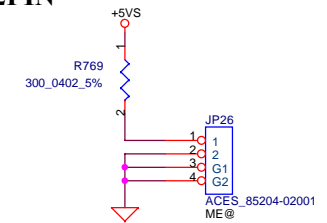


BTN FUNCTION	KEY MATRIX	
	IN	OUT
MUTE BTN	KSO17	KSI3
DOWN	KSO17	KSI2
UP	KSO16	KSI2

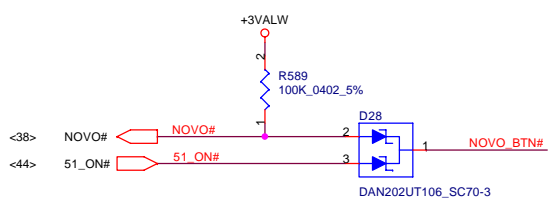
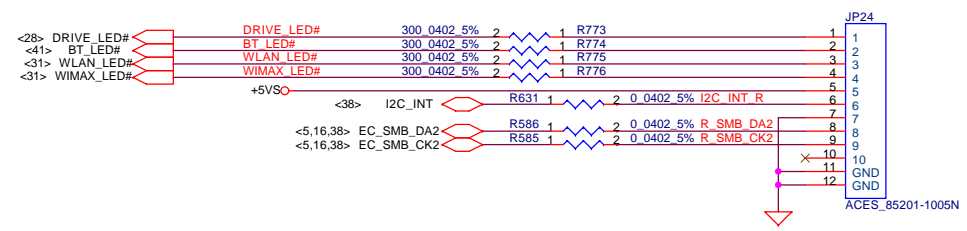
### ON/OFF switch



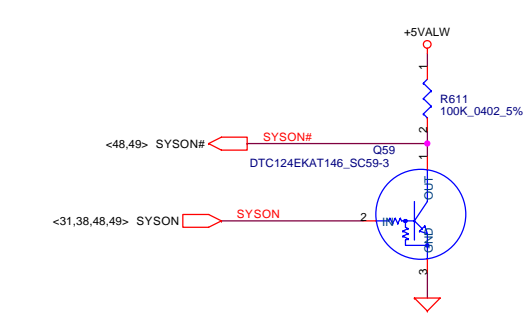
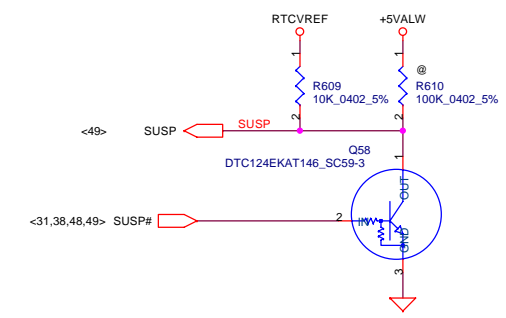
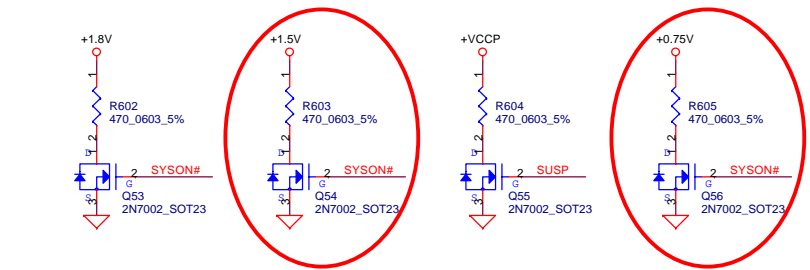
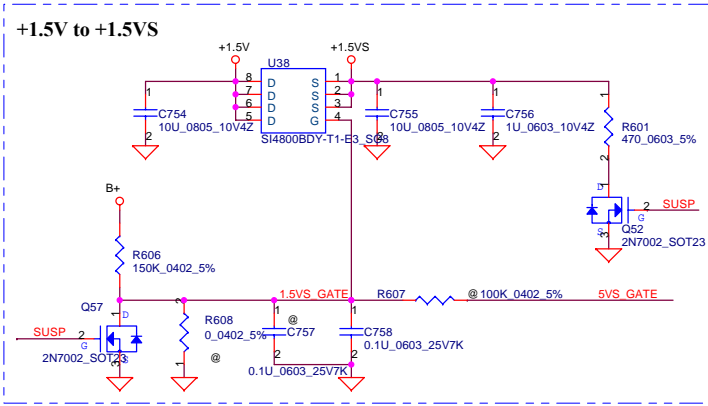
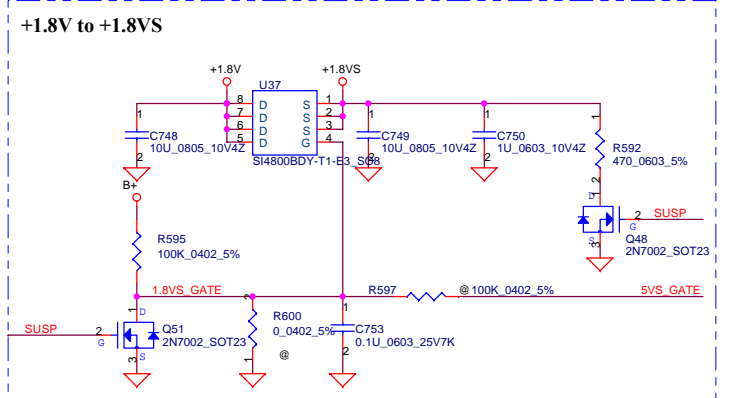
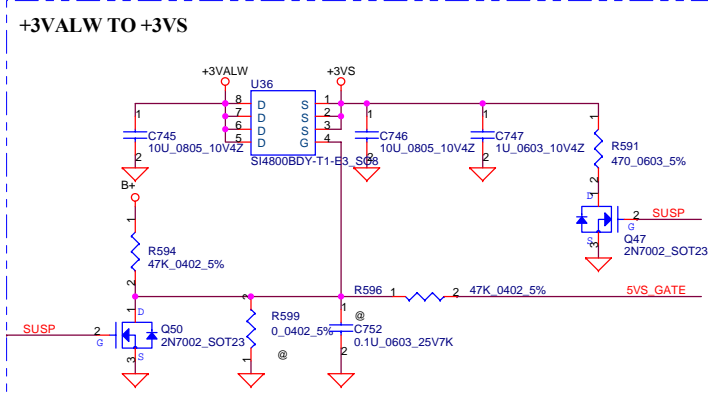
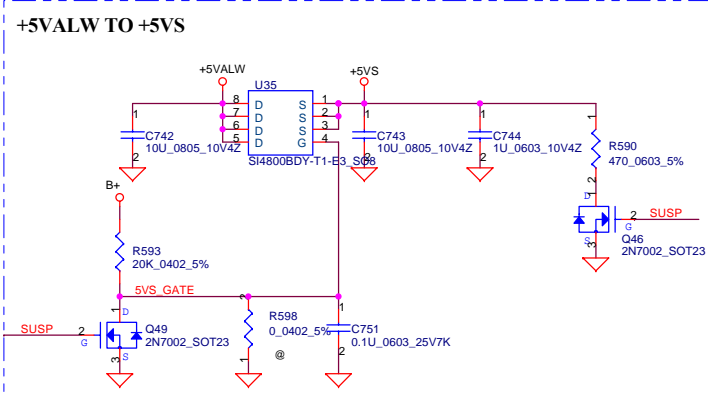
### IDEAPAD BOARD 2PIN



### Slide Board Conn. 12 pin

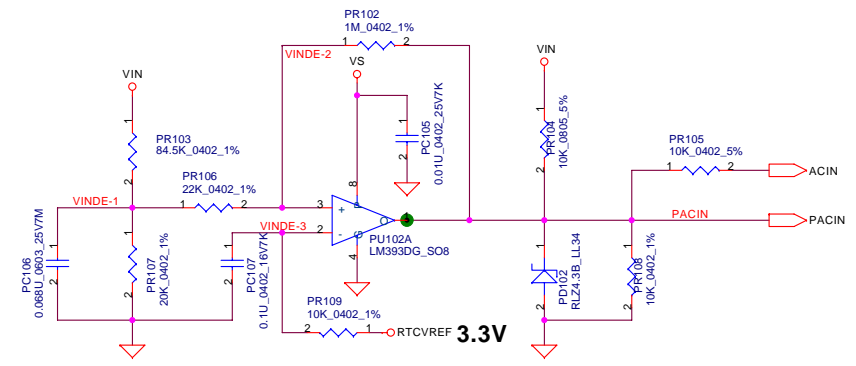
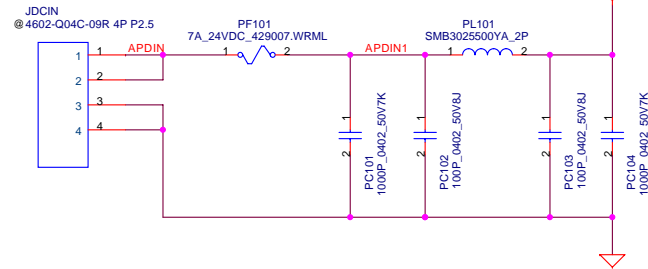


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				Size
				Custom
				KIWB1/B2_LA4601P
				0.1
Date: Monday, June 30, 2008		Sheet 42 of 52		



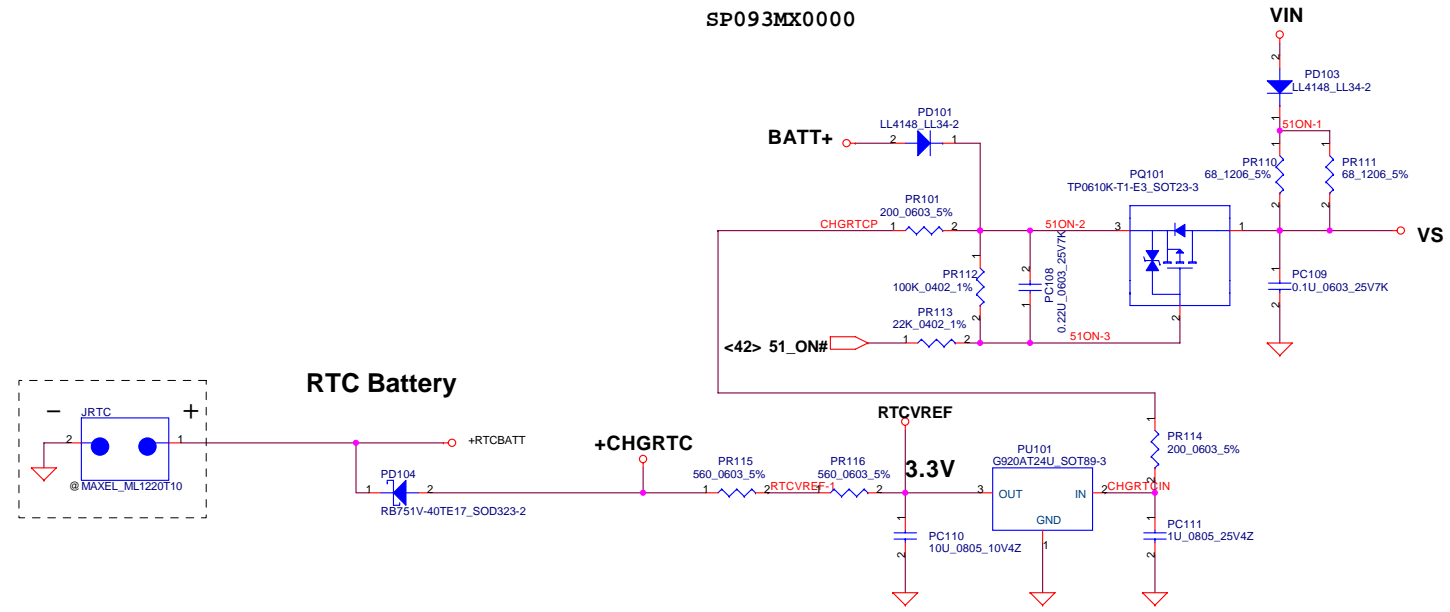
Security Classification		Compal Secret Data		Title	
Issued Date		2006/08/18	Deciphered Date	2007/8/18	DC Interface
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Size	Document Number	Date		Monday, June 30, 2008	Sheet 43 of 52
Custom	KIWB1/B2_LA4601P	Rev		0.1	

**DC030006J00**

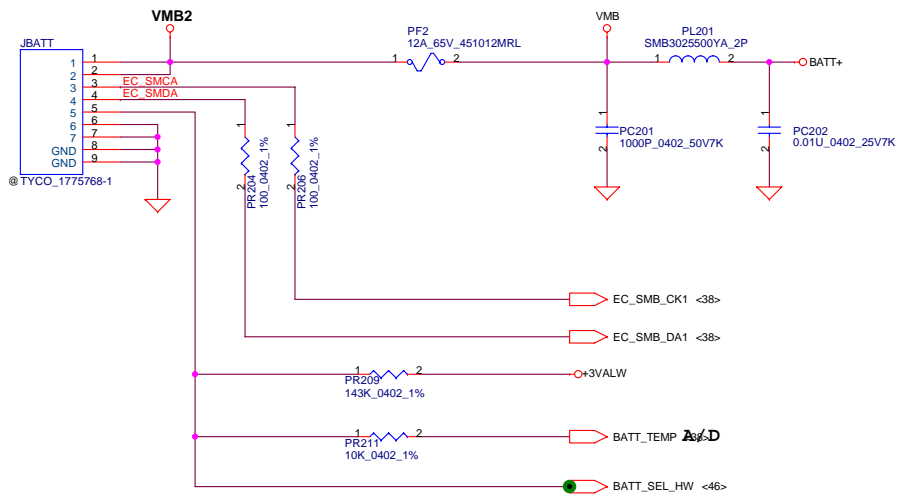


**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976

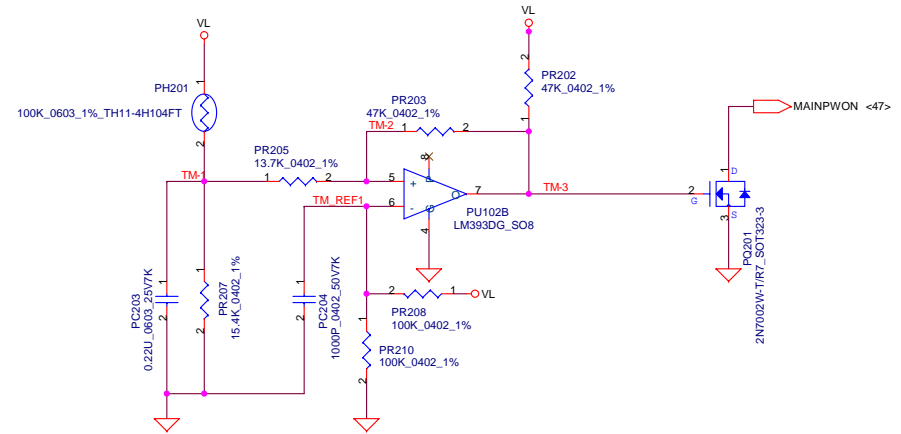
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Size	Document Number	Rev		0.1	
Custom				Date:	Monday, June 30, 2008
		Sheet	44	of	52

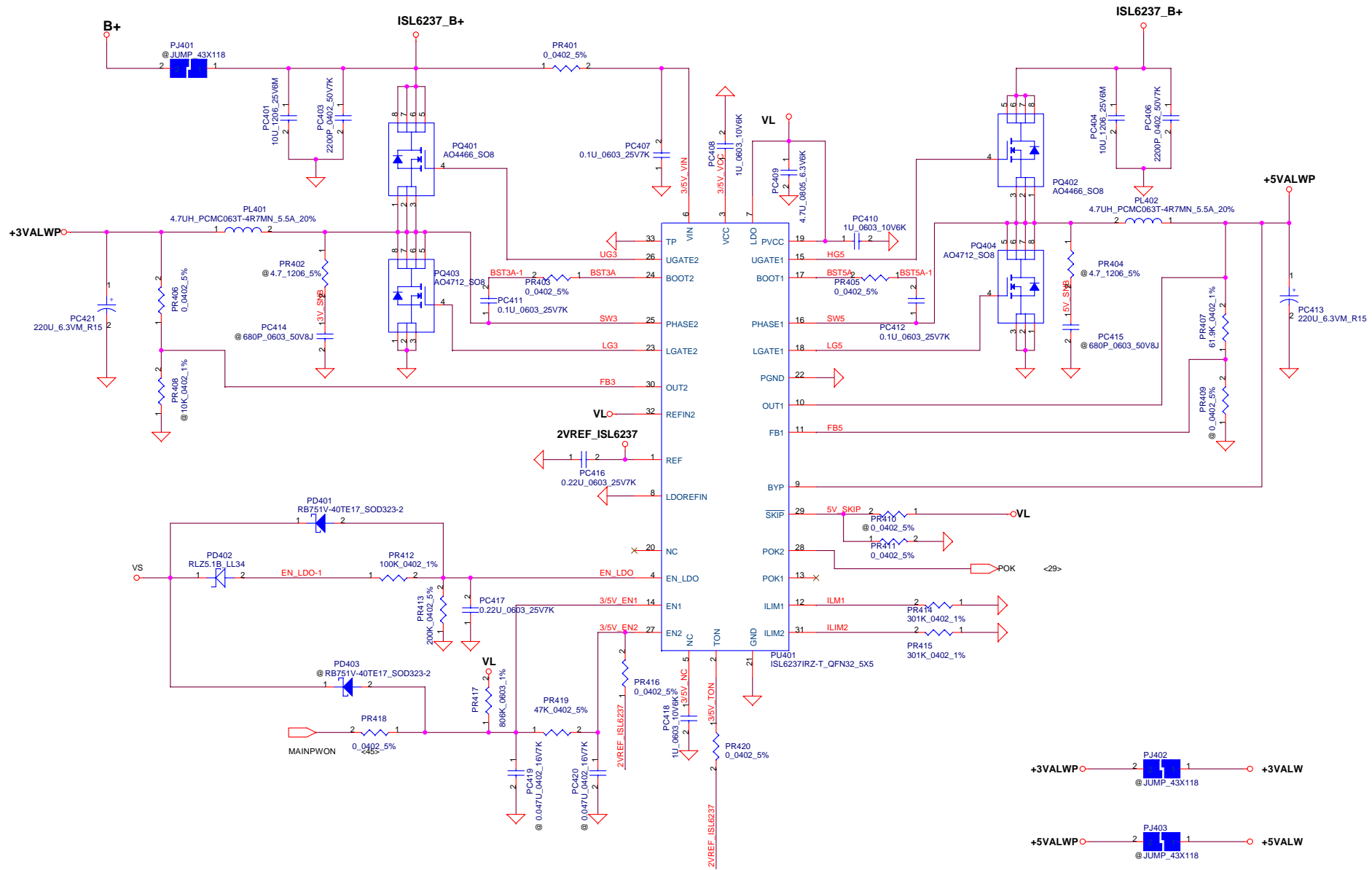


PH1 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C

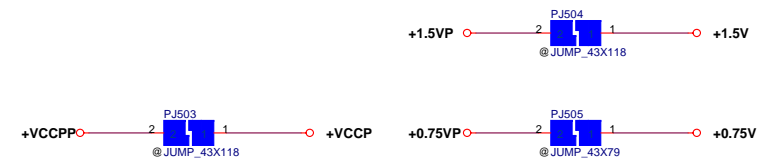
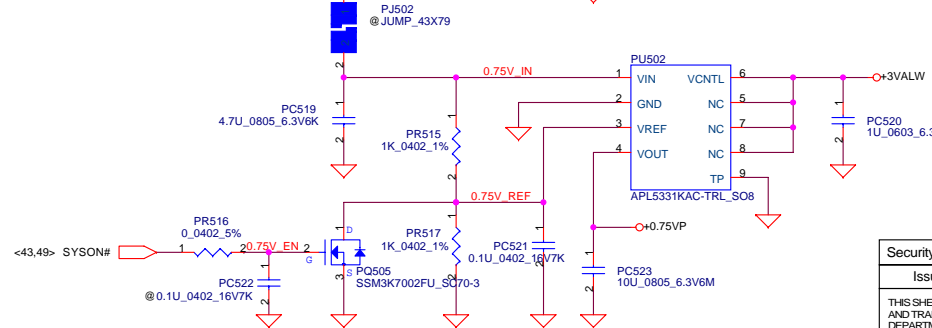
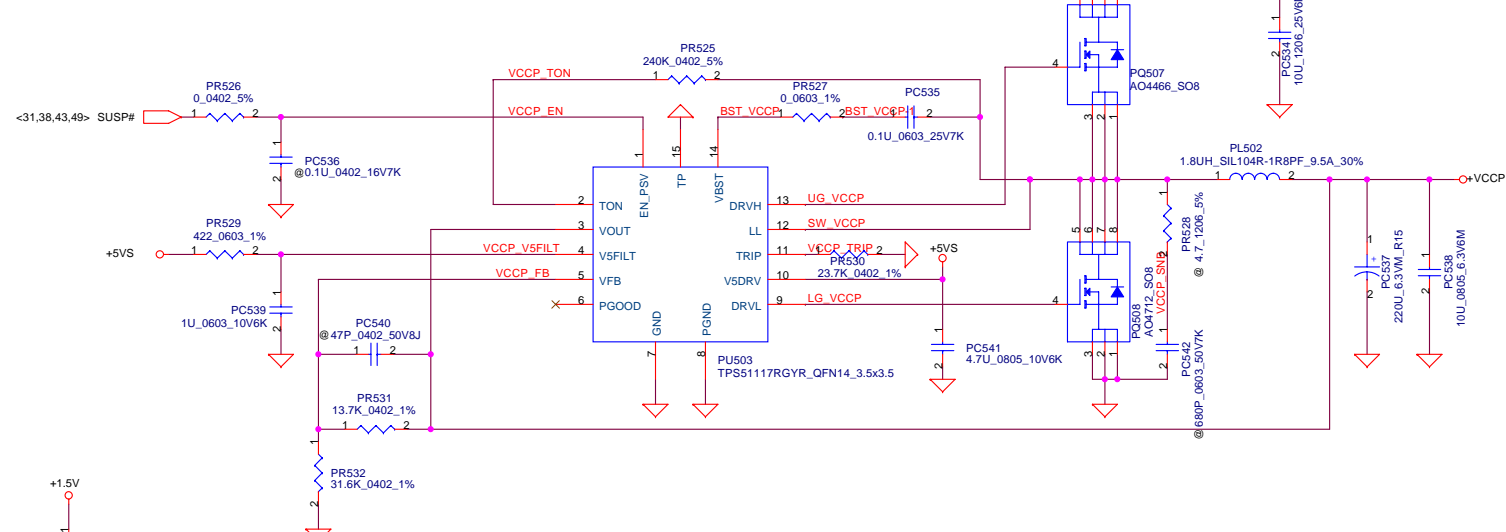
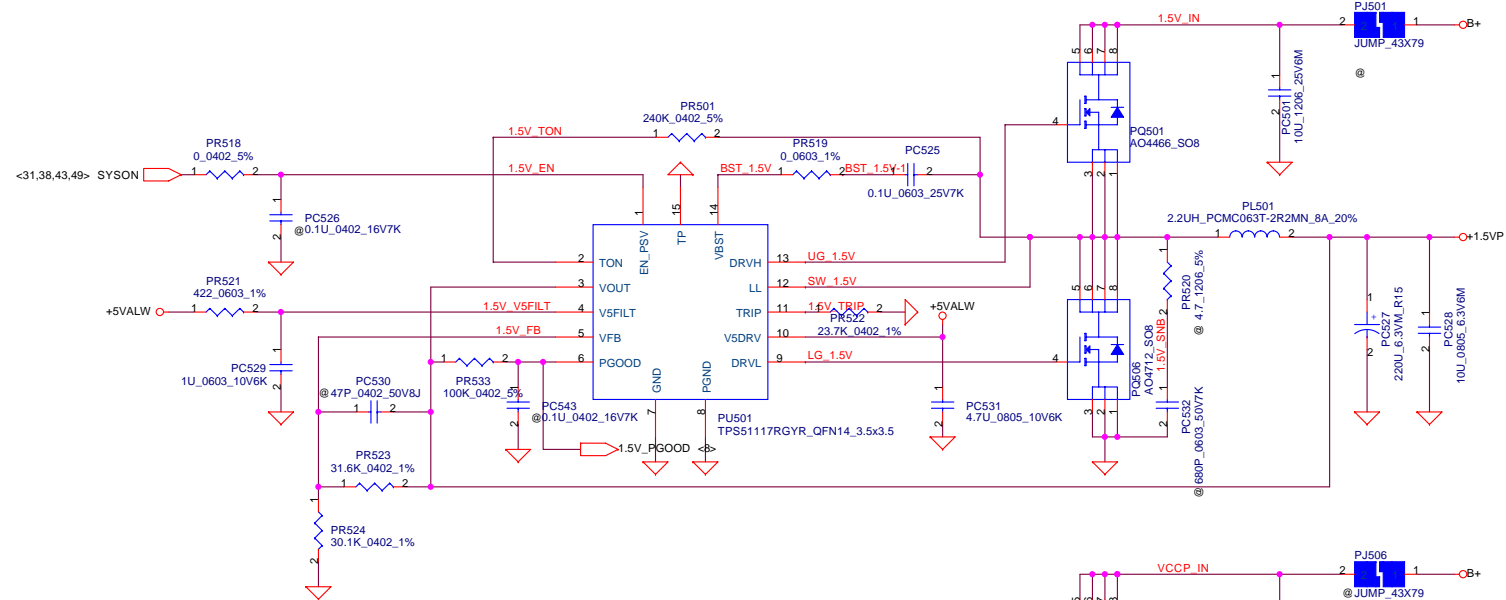


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Size	Document Number			Rev	
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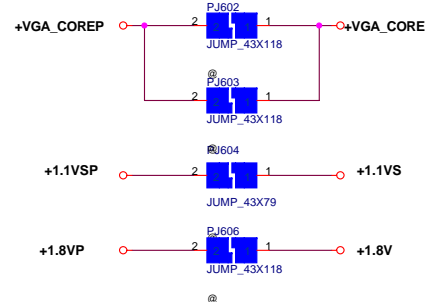
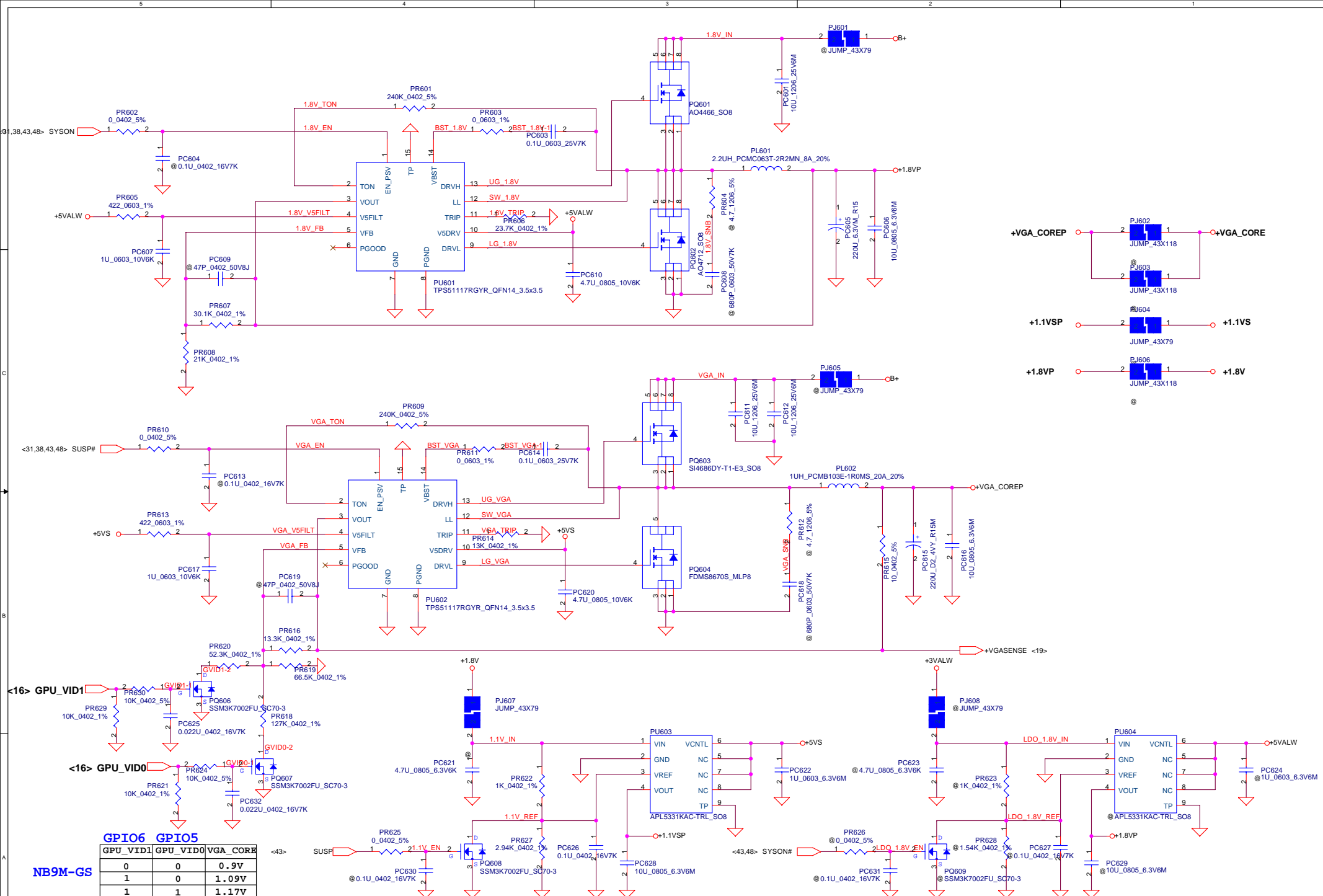


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NB9M-GS

NB9P-GE2

GPIO6	GPIO5	GPU_VID1	GPU_VID0	VGA_CORE
0	0	0	0	0.9V
1	0	0	1	1.09V
1	1	1	1	1.17V

GPIO6	GPIO5	GPU_VID1	GPU_VID0	VGA_CORE
0	1	0	0	0.9V
1	1	1	1	1.0V

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<b>VGA_CORE/1.8V/1.1V</b>		
Size	Document Number	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						20071031	EVT
2						20071115	DVT
3							
4							
5							
6							
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				Custom	0.1
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NO DATE PAGE MODIFICATION LIST PURPOSE

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Title		
<b><i>HW PIR</i></b>		
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