VCUAA

Metis 10F/10FG

LA-9161P REV 1.0 Schematic

Intel Processor (Ivy Bridge) / PCH(Panther Point)
2012-08-07 Rev 1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date	2015/04/19
Title	*Cover Page*		
Size: Custom	Document Number: VCUAA		Rev: 1.0
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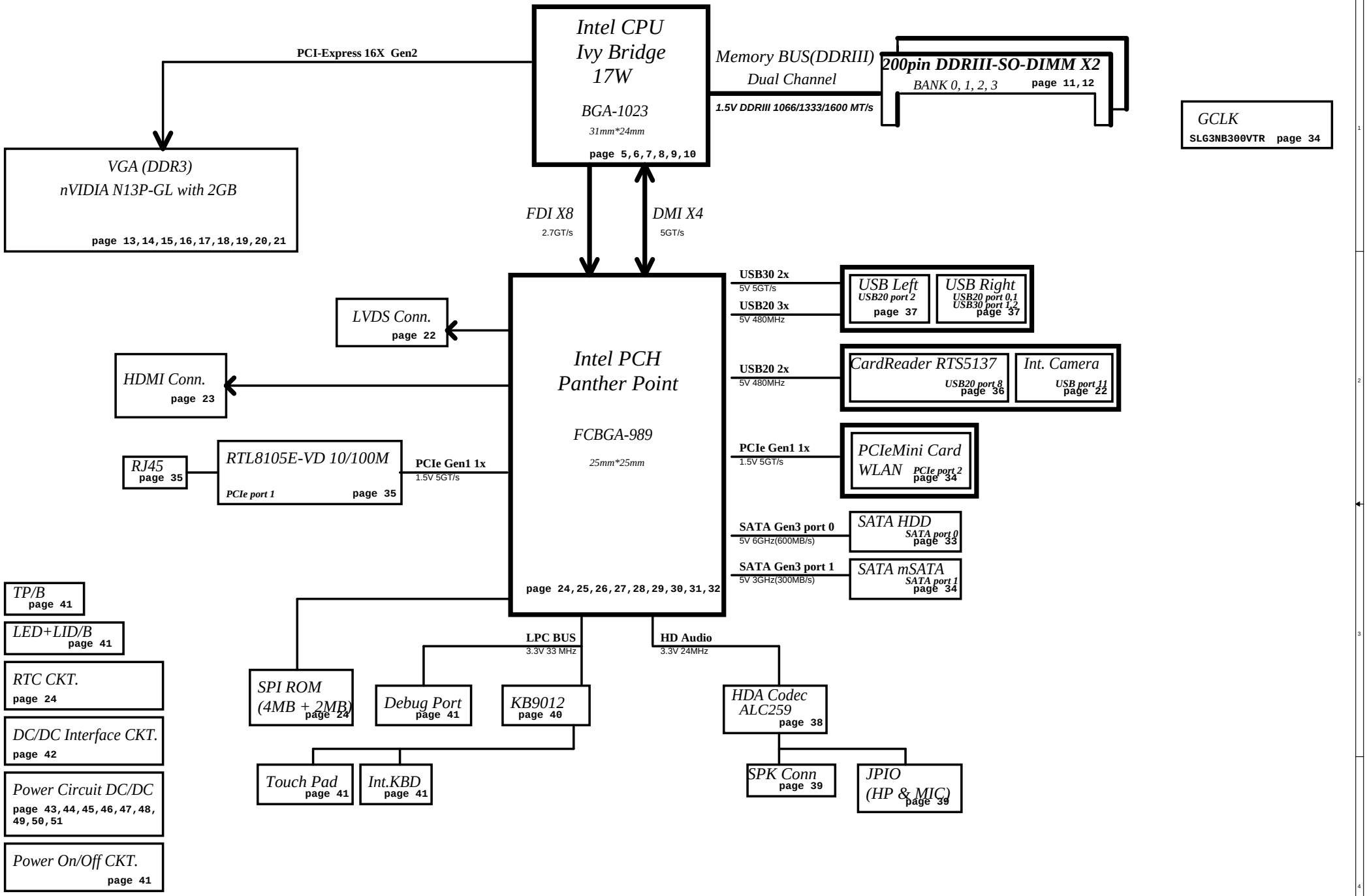
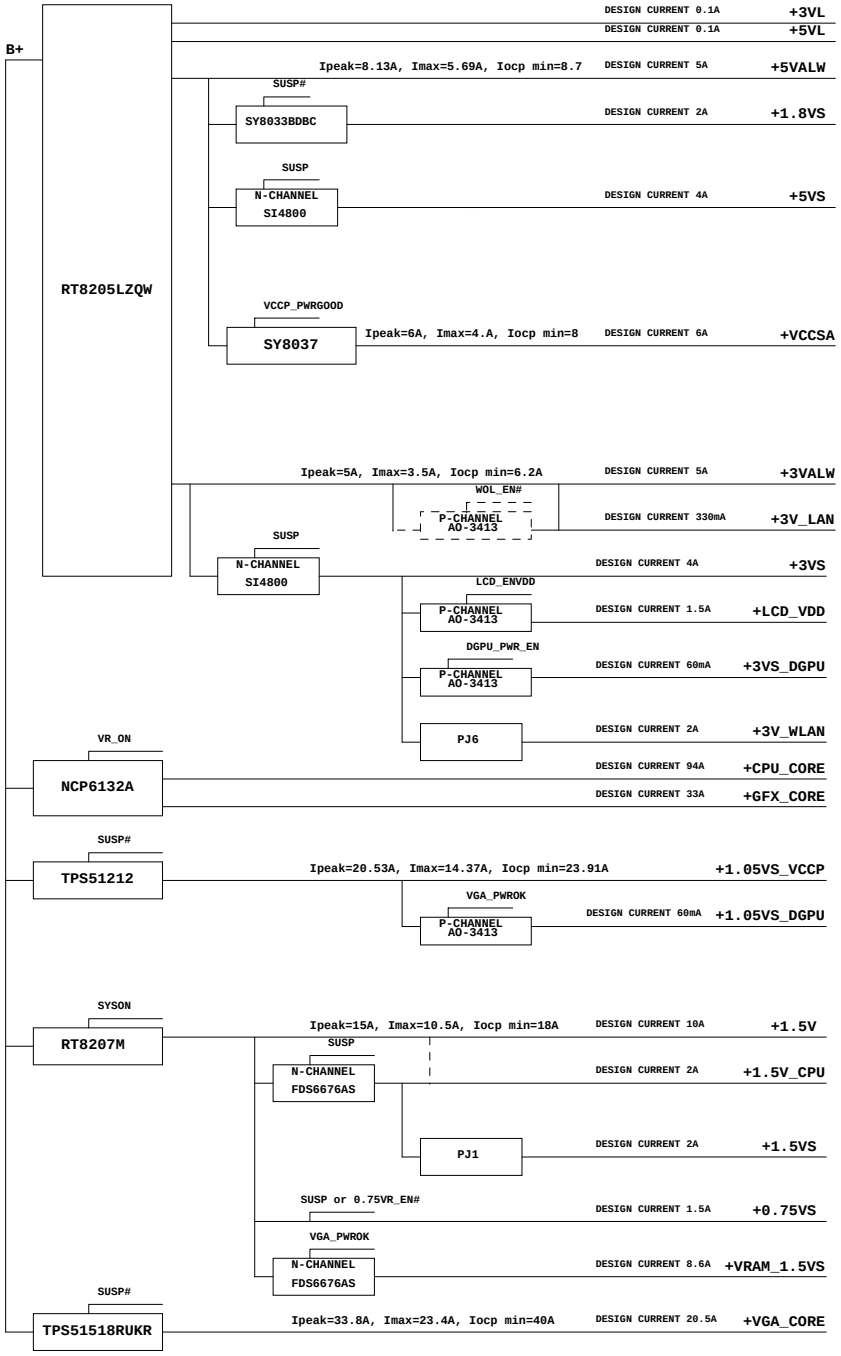


Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 2 of 53		



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Power Tree			
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
Chief River		Ivy Bridge i3 (CPUI3@) Ivy Bridge i5 (CPUI5@)	HM77C1(HM77@) HM77C1_R1(HM77R1@) HM77C1_R3(HM77R3@)	nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function			
description			
explain			
BTO			

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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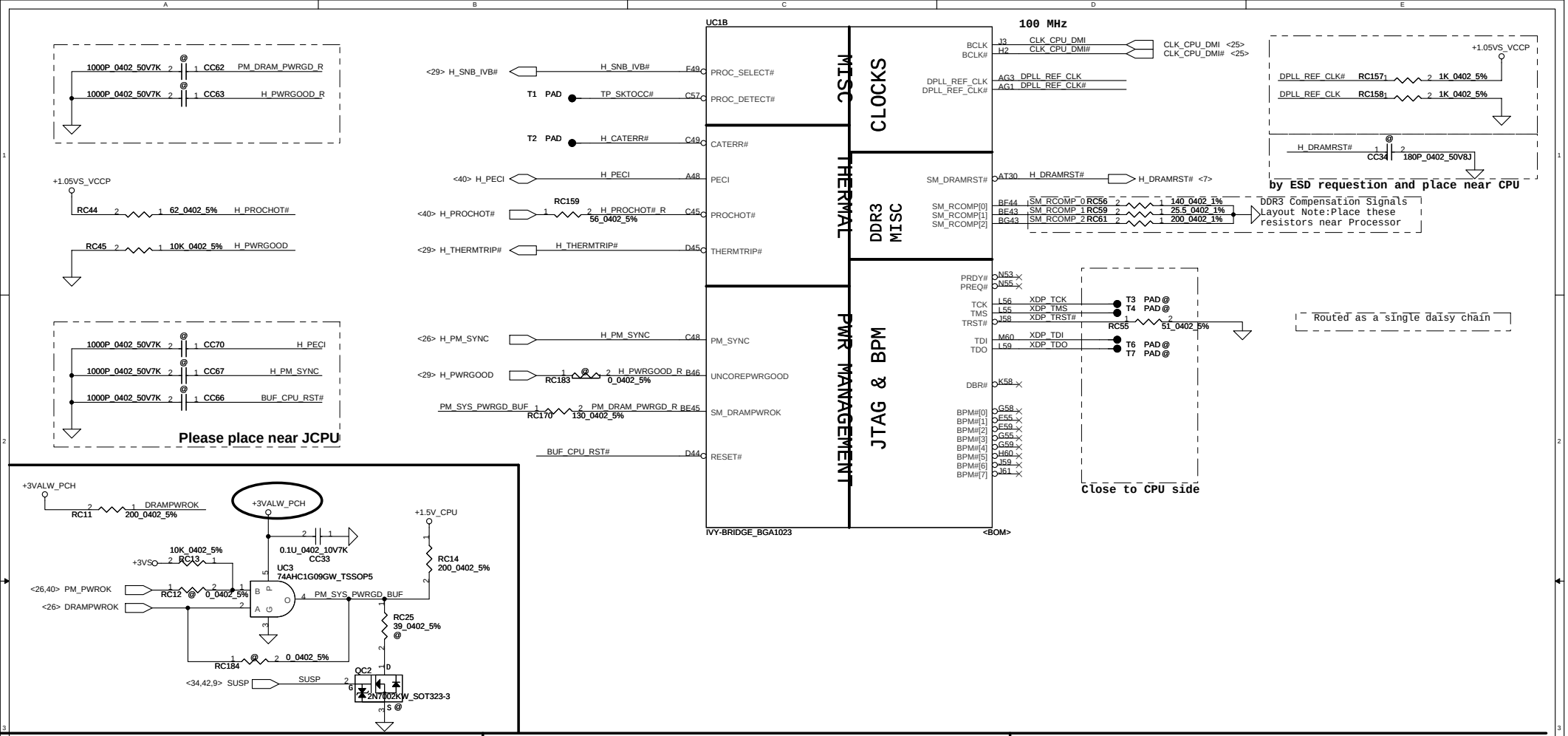
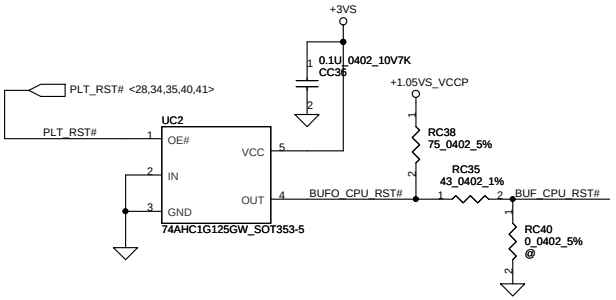
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Notes List
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 4 of 53		

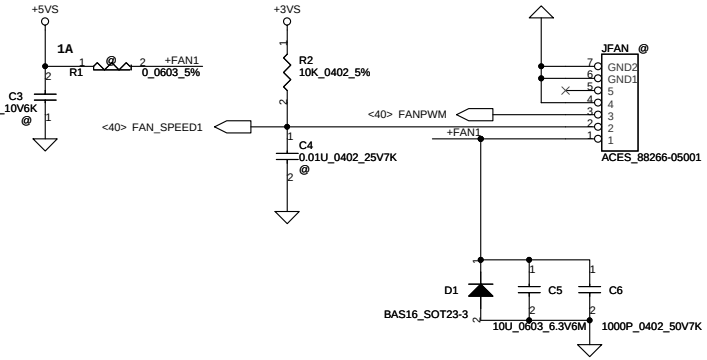


Buffered Rest to CPU



XDP Connector

FAN Control Circuit



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Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	Ivy Bridge_JTAG/XDP/FAN
Size: Custom	Document Number: VCUAA
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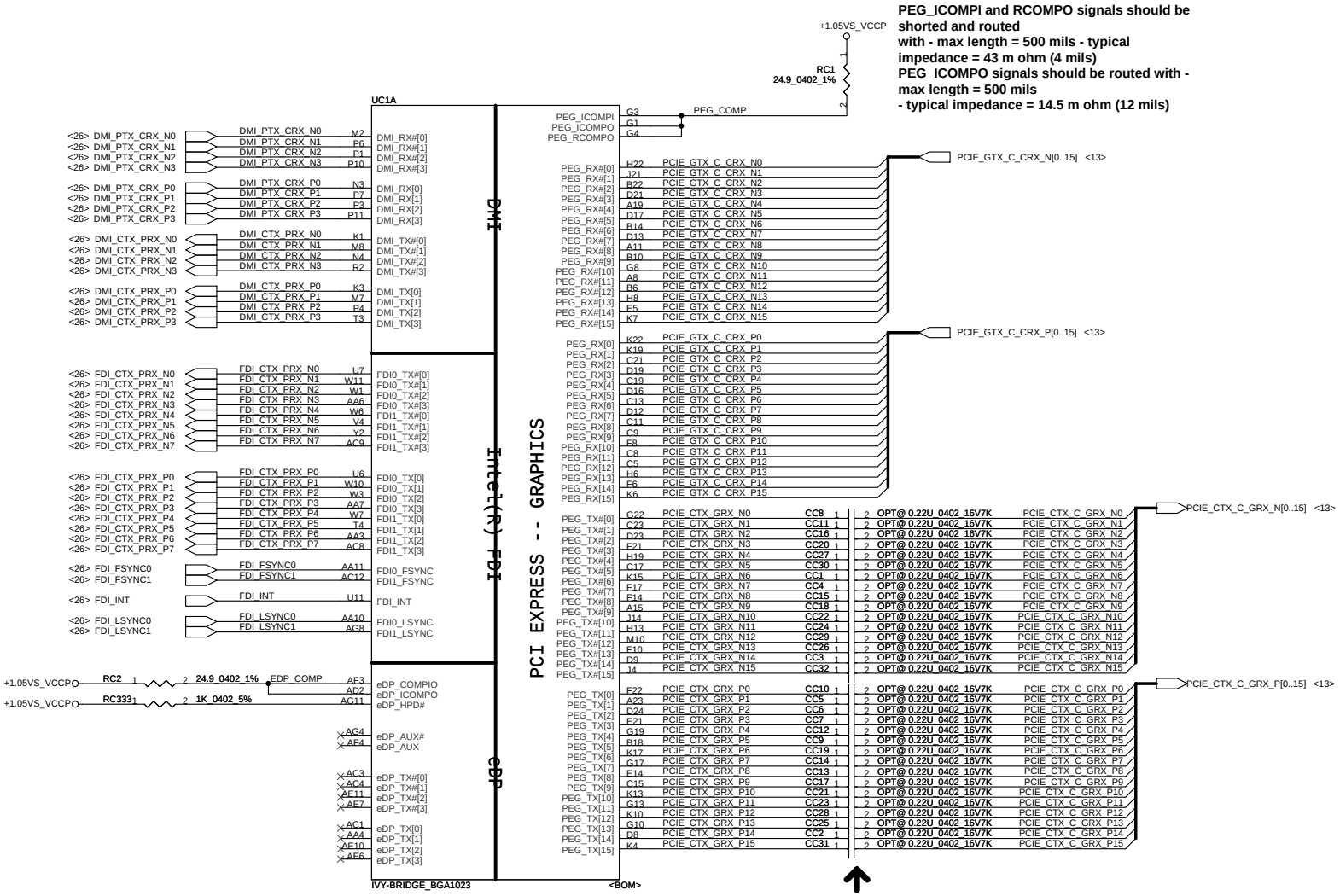
Date: Tuesday, October 16, 2012	Sheet 5 of 53



	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N13X	Gen1/2/3	Suggest 220 nF

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Title: *Ivy Bridge_DMI/PEG/FDI*

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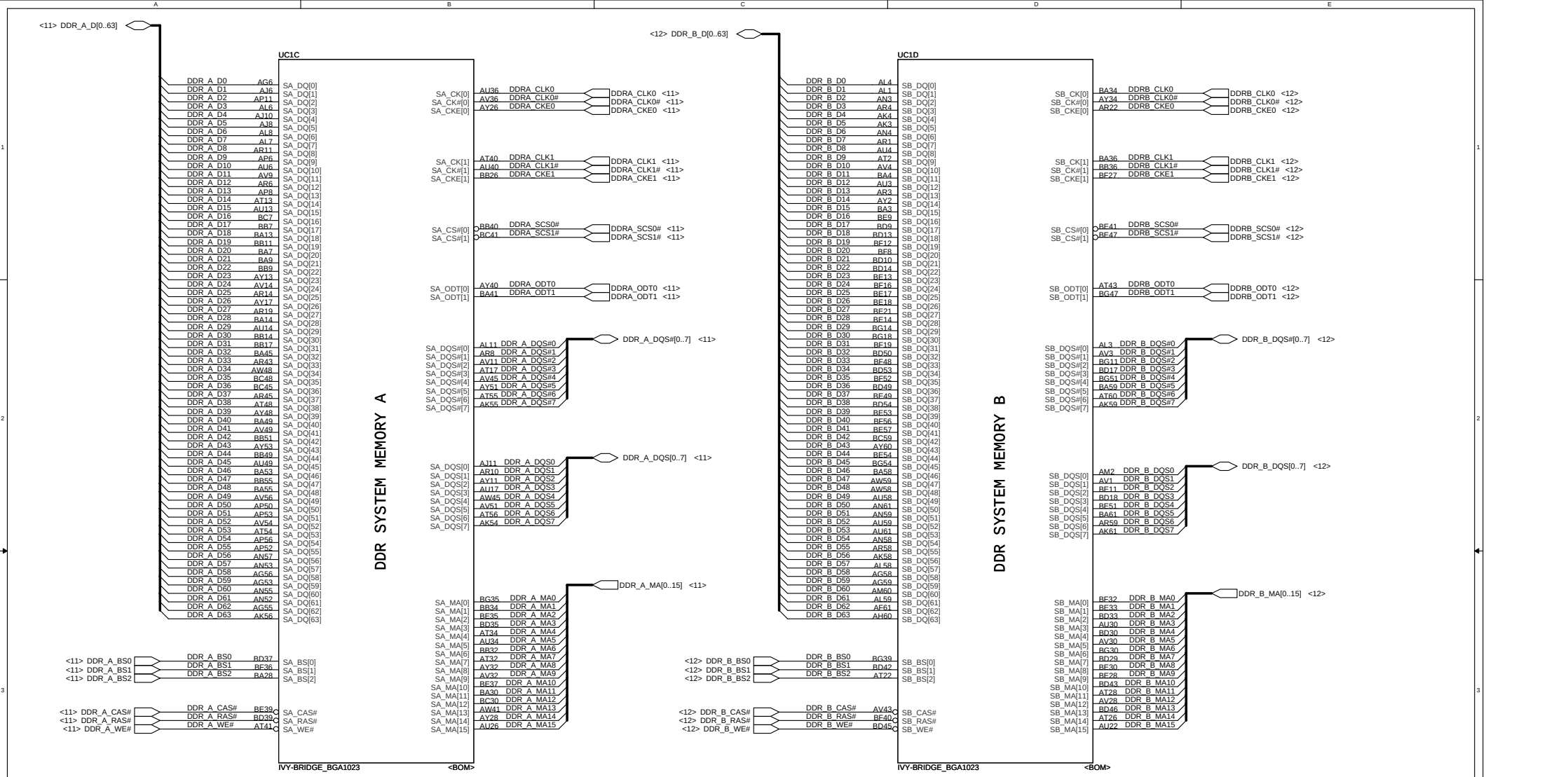

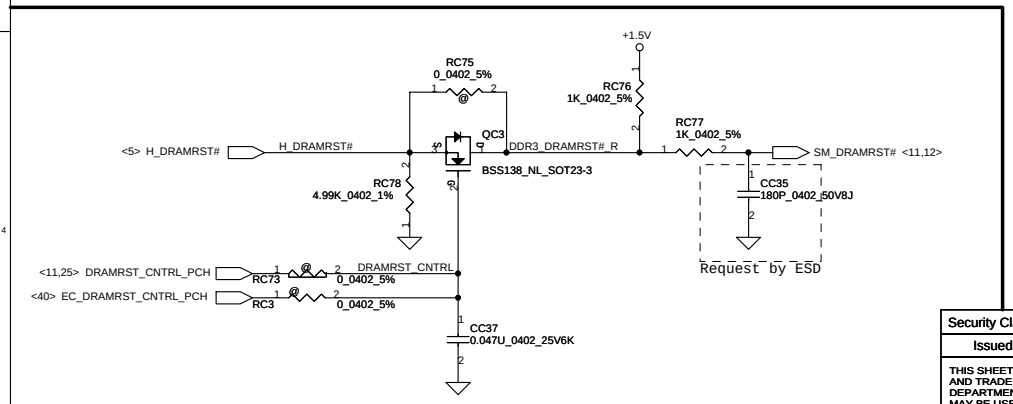

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	*Ivy Bridge_DDR3*		
Size: Custom	Document Number: VCUAA		Rev: 1.0
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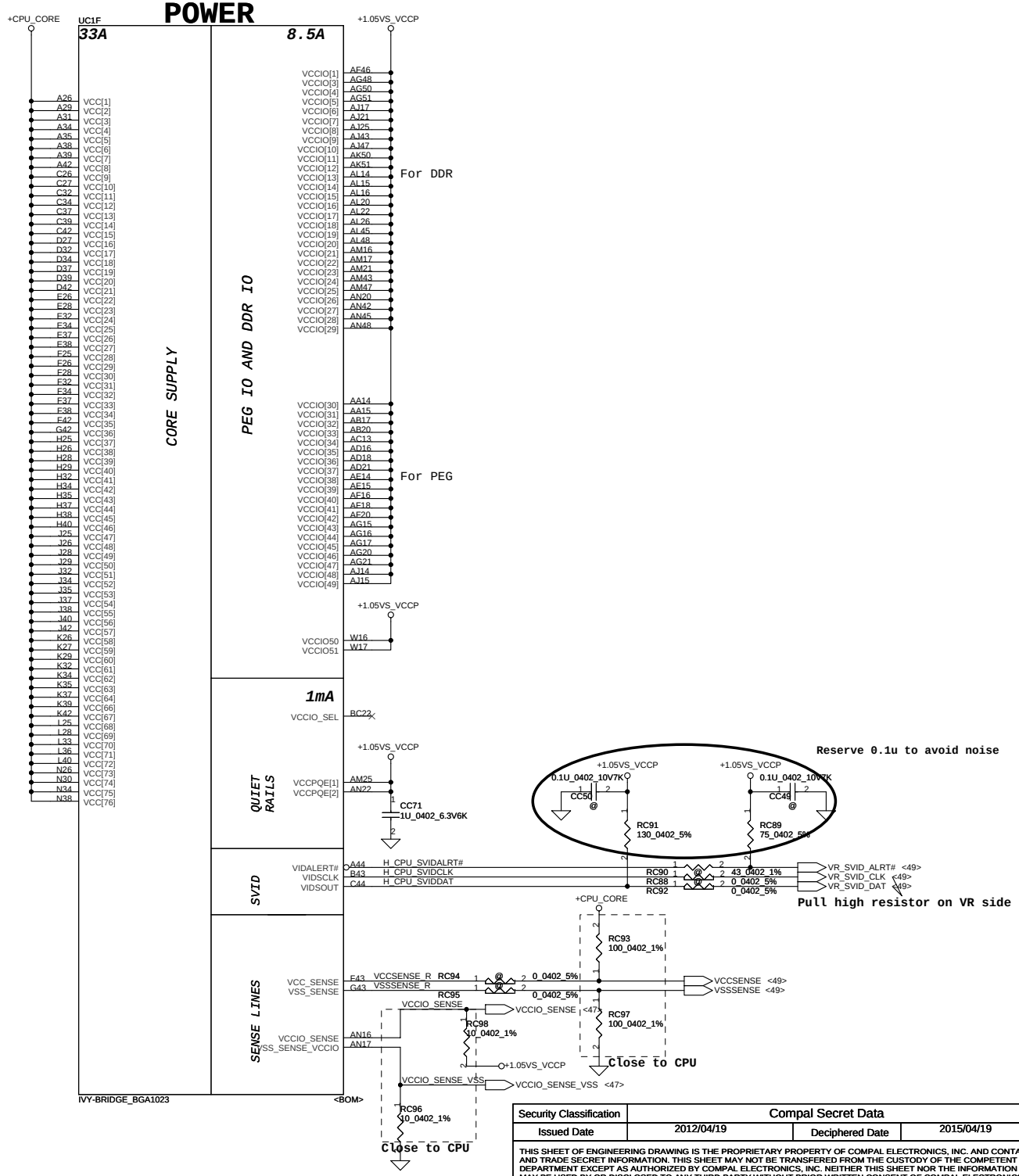
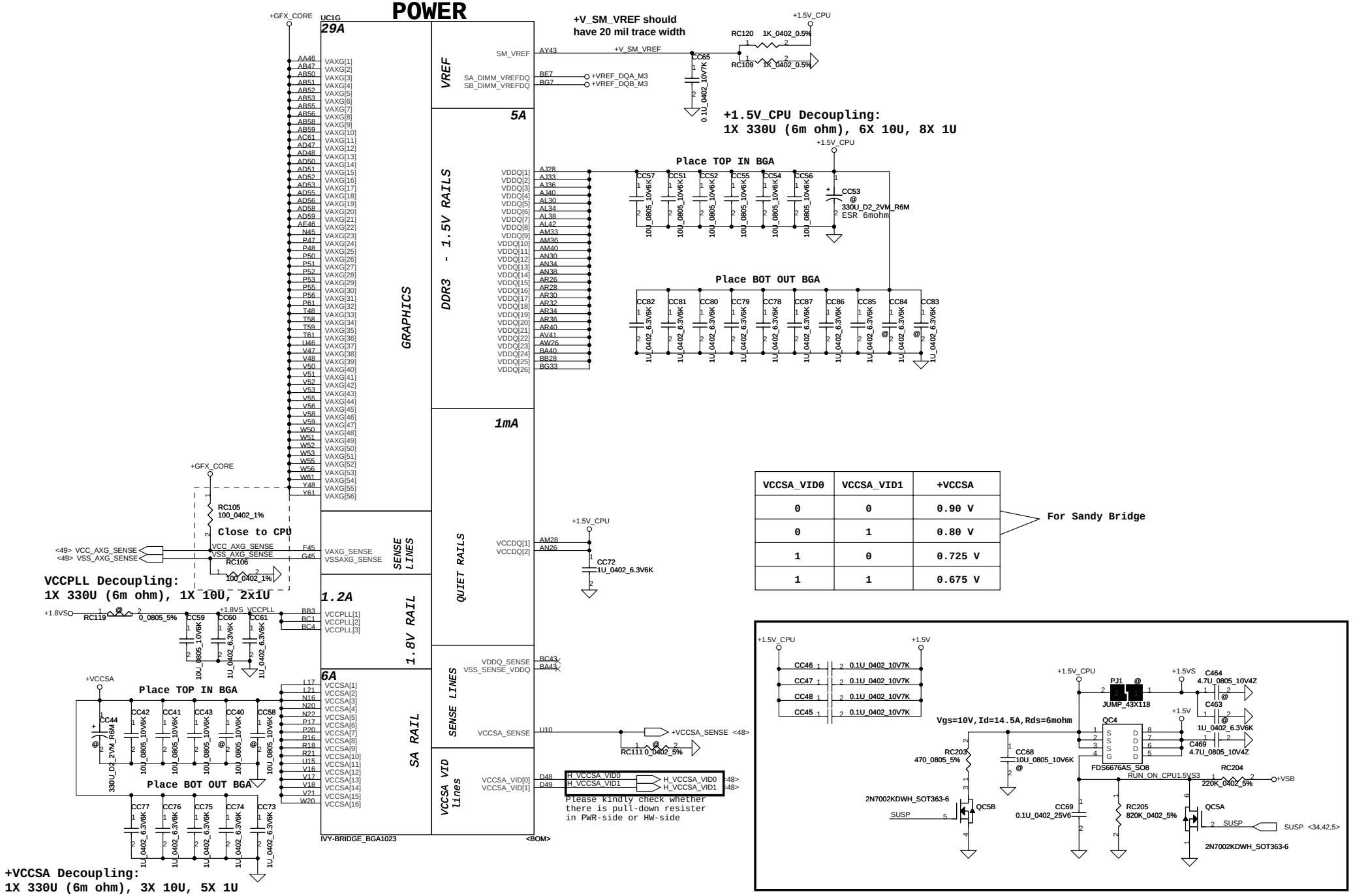
POWER



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: Ivy Bridge_POWER-1			
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 8 of 53		

POWER



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

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Compal Electronics, Inc.	
Title	Ivy Bridge_POWER-2
Size: Custom	Document Number: VCUAA
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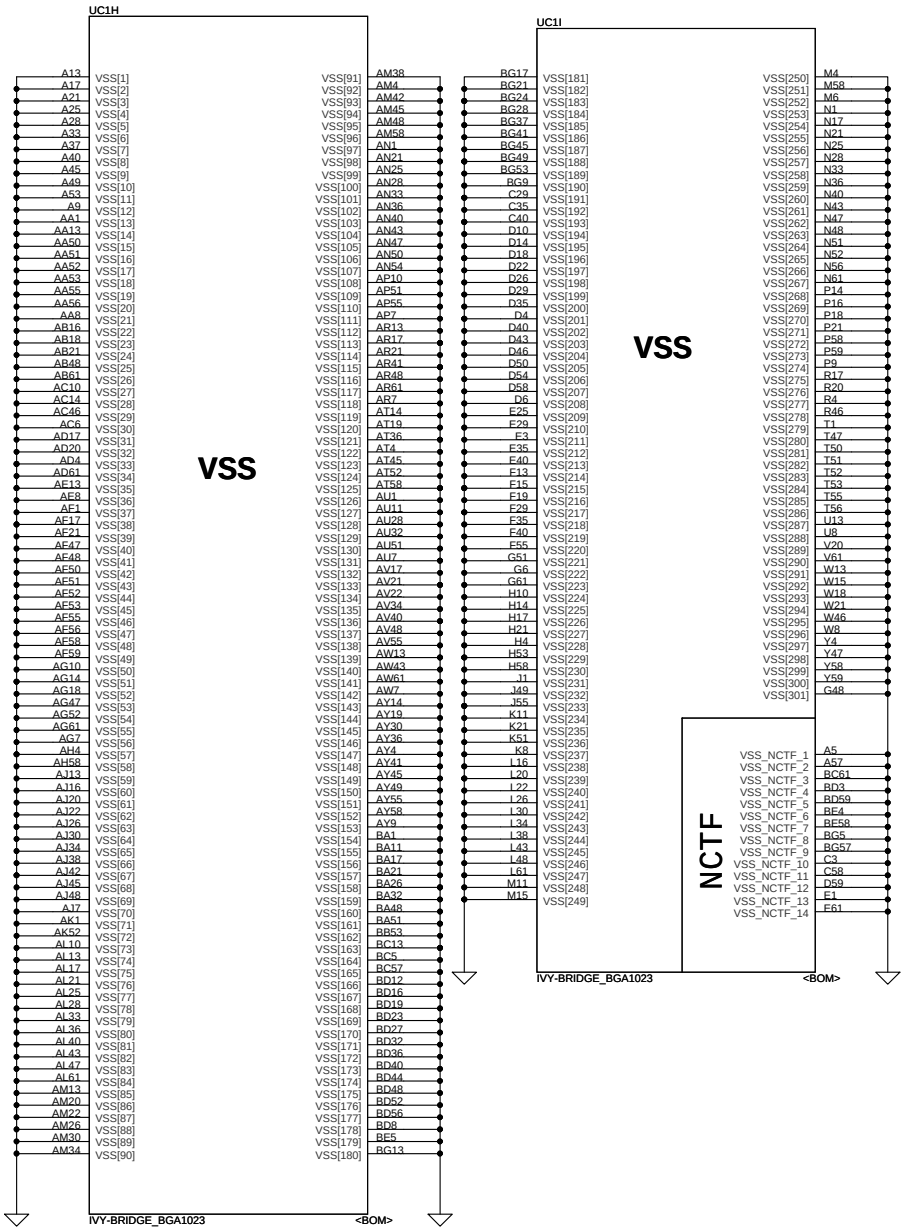

These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)

CFG2 — RC79 1K_0402_1% OPT@

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4 — RC82 1K_0402_1% @

Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — RC85 1K_0402_1% @

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG6 — RC83 1K_0402_1% @

CFG5 — RC84 1K_0402_1% @

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Ivy Bridge_GND/RSVD/CFG

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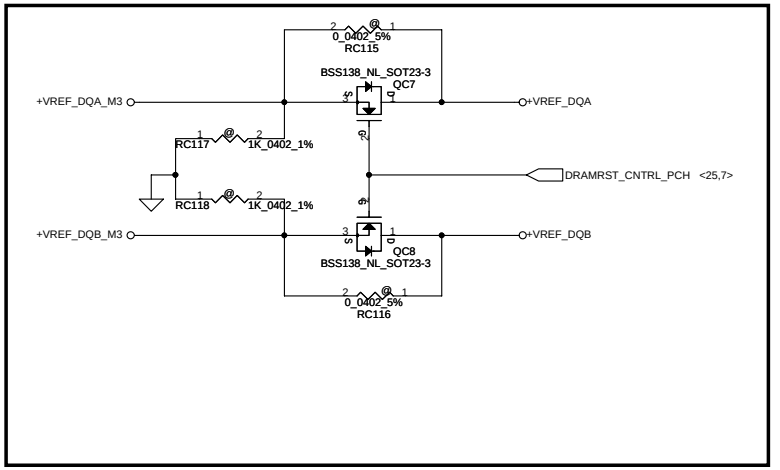
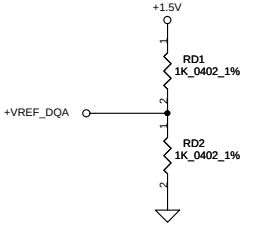
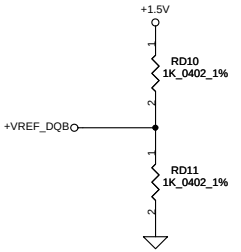
DDR3 SO-DIMM A
Reverse Type

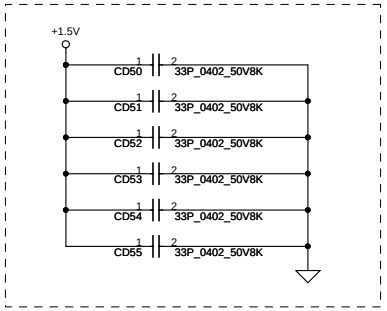
DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_MA[0..15] <7>

Intel DDR Vref M3

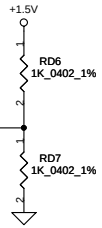


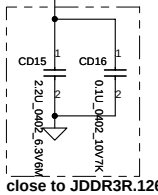






please place these caps near the reference power plane of CMD/AD

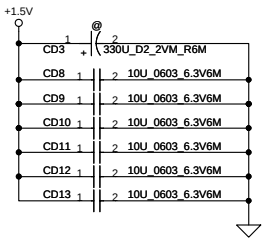




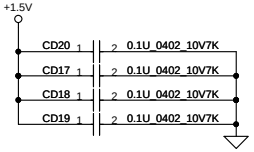
close to JDDR3R.126

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

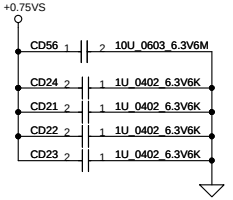
Layout Note: Place near JDDRH



Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note: Place near JDDRH.203 and 204



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Compal Electronics, Inc.	
Title	DDRIII-SODIMM0
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Standard Type
DDR3 SO-DIMM B

DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>

JDDR3S

+VREF_DQB
+1.5V
+3VSO
+0.75VS

CD28 2.2U_0402_6.3V6M
CD27 0.1U_0402_10V7K
Close to JDDR3S.1

CD46 2.2U_0402_6.3V6M
CD47 0.1U_0402_10V7K
Close to JDDR3S.126

RD12 1K_0402_1%
RD13 1K_0402_1%
+VREF_CAB

RD14 10K_0402_5%
RD15 10K_0402_5%
CD48 2.2U_0402_6.3V6M
CD49 0.1U_0402_10V7K

LCN_DAN06-K4406-0102
@

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

Layout Note: Place near JDDRL

CD31 330U_D2_2VM_R6M
CD41 10U_0603_6.3V6M
CD36 10U_0603_6.3V6M
CD37 10U_0603_6.3V6M
CD38 10U_0603_6.3V6M
CD39 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

CD33 0.1U_0402_10V7K
CD29 0.1U_0402_10V7K
CD30 0.1U_0402_10V7K
CD32 0.1U_0402_10V7K

Layout Note: Place near JDDRL.203 and 204

+0.75VS
CD57 10U_0603_6.3V6M
CD45 1U_0402_6.3V6K
CD42 1U_0402_6.3V6K
CD43 1U_0402_6.3V6K
CD44 1U_0402_6.3V6K

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM1***

Size: Custom | Document Number: **VCUAA** | Rev: 1.0

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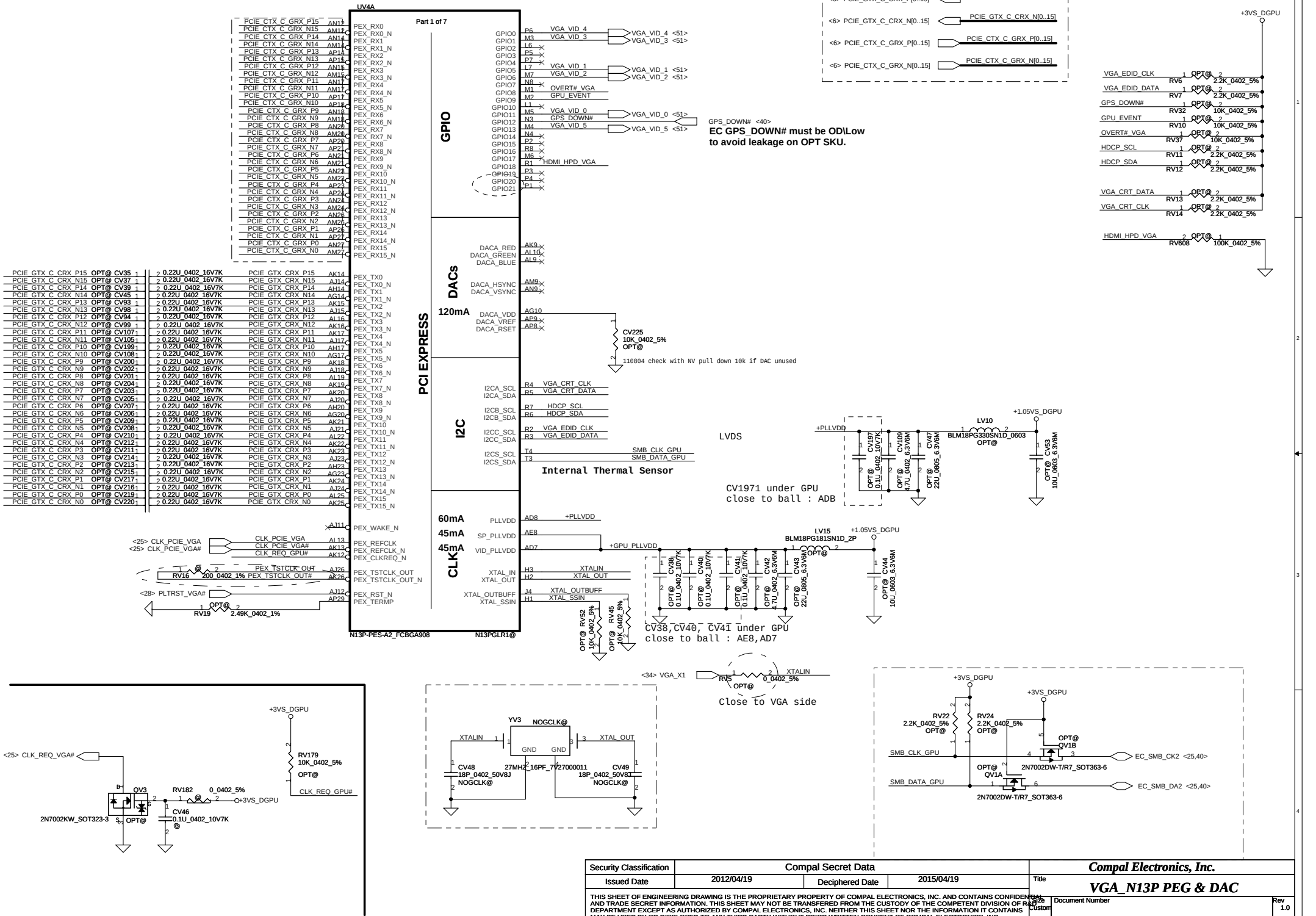

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Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: VGA_N13P PEG & DAC			
Size: Custom	Document Number		Rev: 1.0
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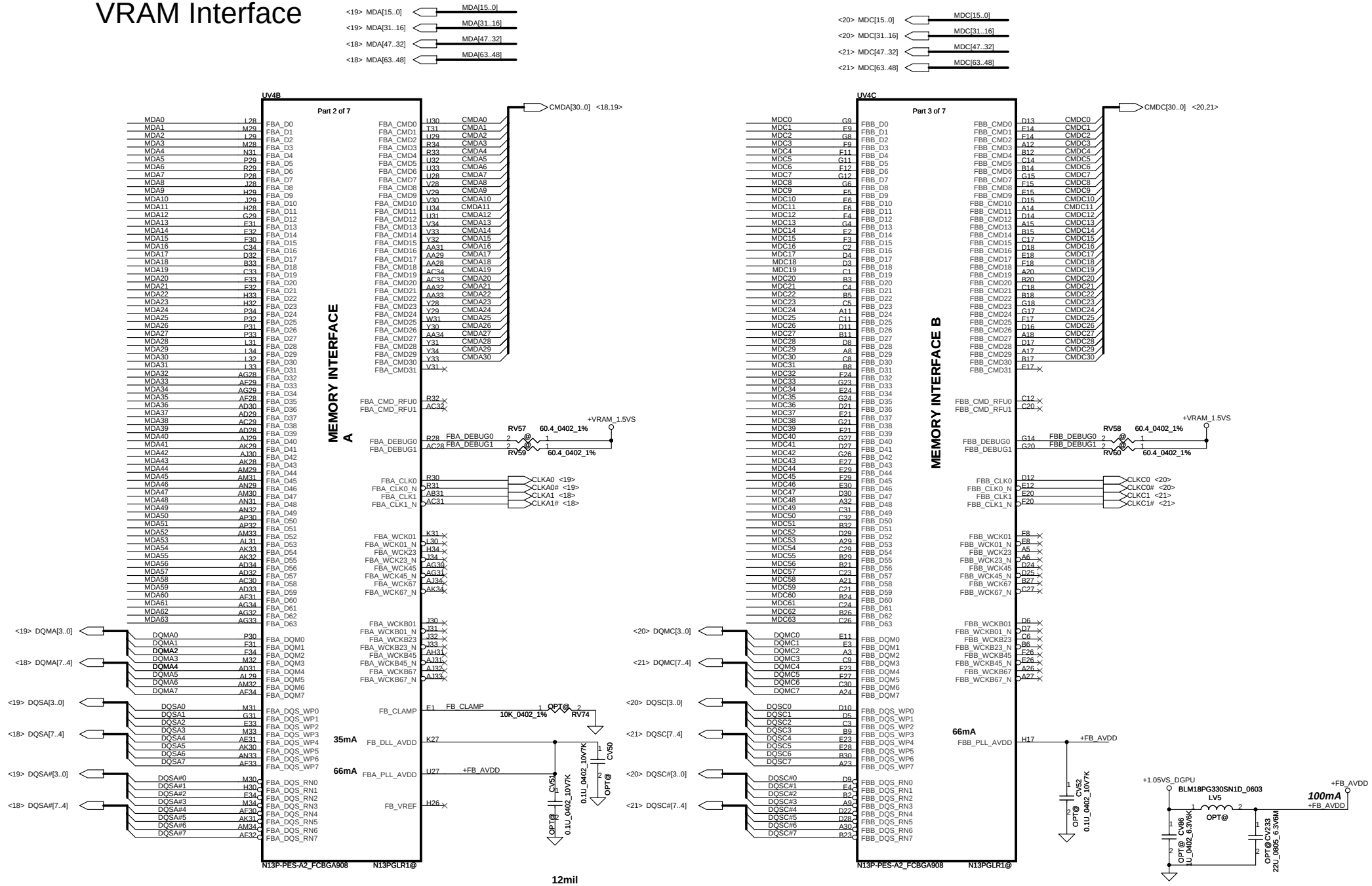
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: **N13P VRAM Interface**

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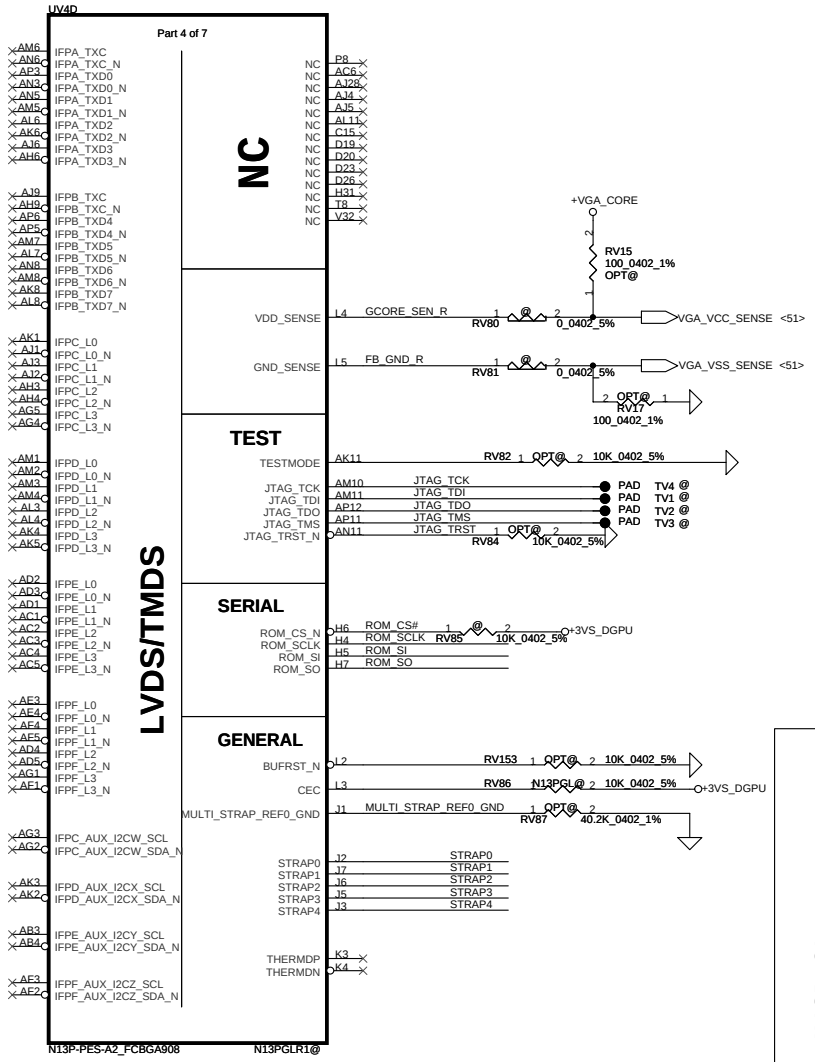
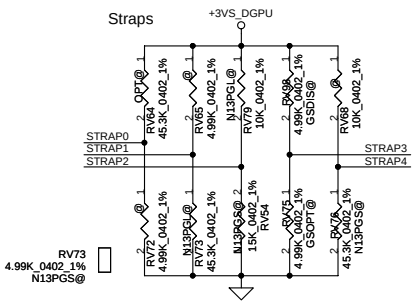
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417 for GL , FB[1]	FB_0_BAR_SIZE for GL , FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**SLOT_CLK_CFG for GL PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

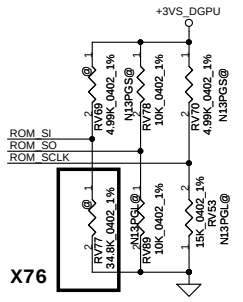
SKU	Device ID	biit5 to bit0
N13P-GL ES2	0x0DE9	101001
N13P-GS ES1	0x0FDB	011011
N13P-GS QS	0x0FD2	010010

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



MULTI LEVEL STRAPS





N13P-GL ROM_SI				
	Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	**1GB**	**0010**	**RV77 PD 15K (SD034150280)**
	Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003YO00	**2GB**	**0110**	**RV77 PD 34.8k (SD034348280)**
	Hynix (900MHZ) 128MX16 H5TQ2G63DFR-11C SA00003YO70	**2GB**	**0101**	**RV77 PD 30k (SD034300280)**
	Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS00	**1GB**	**0011**	**RV77 PD 20K (SD034200280)**
	Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	**2GB**	**0111**	**RV77 PD 45.3K (SD034453280)**
	Samsung (900MHZ) 128M16 K4W2G1646E-BC11 SA00005SH00	**2GB**	**0001**	**RV77 PD 10K (SD028100280)**

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Compal Electronics, Inc.

Title: *VGA_N13P LVDS&TMDS*

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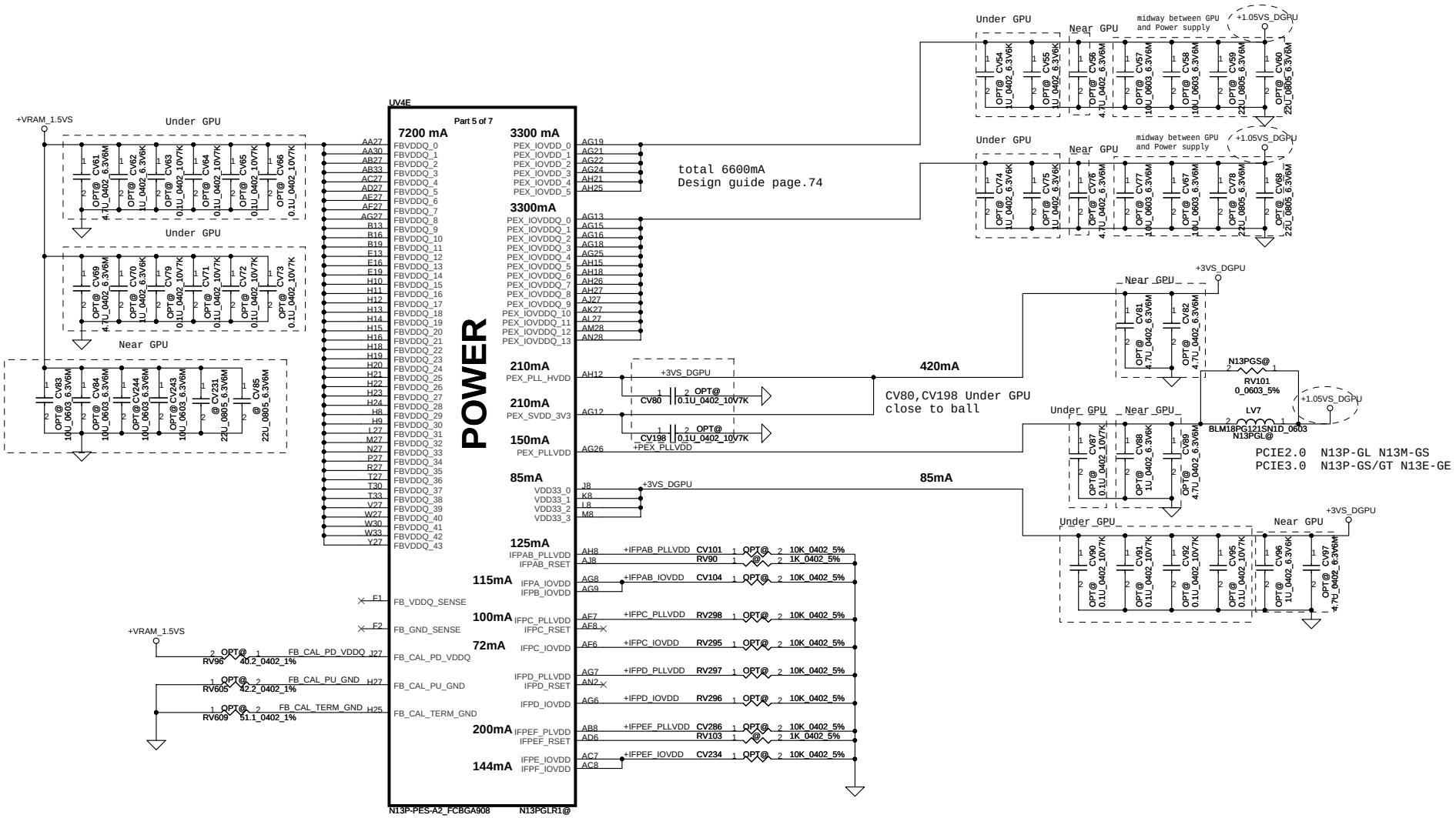

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	VGA_N13P POWER
Size: Custom	Document Number
Rev	1.0
Date:	Tuesday, October 16, 2012
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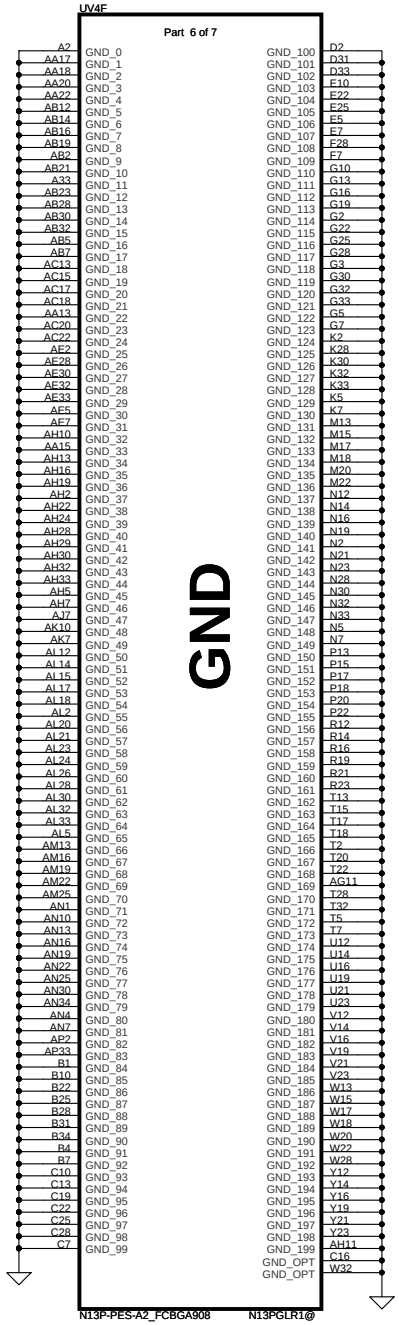

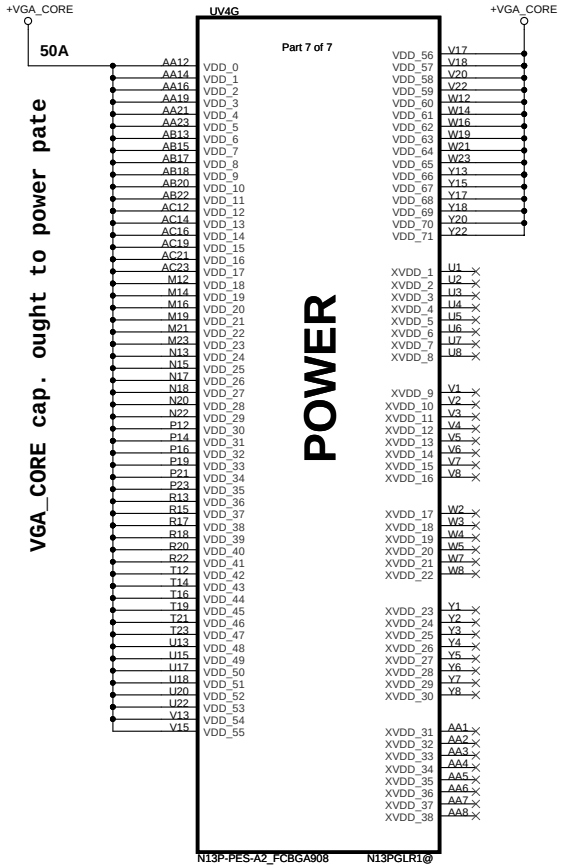

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: VGA_N13P POWER & GND		
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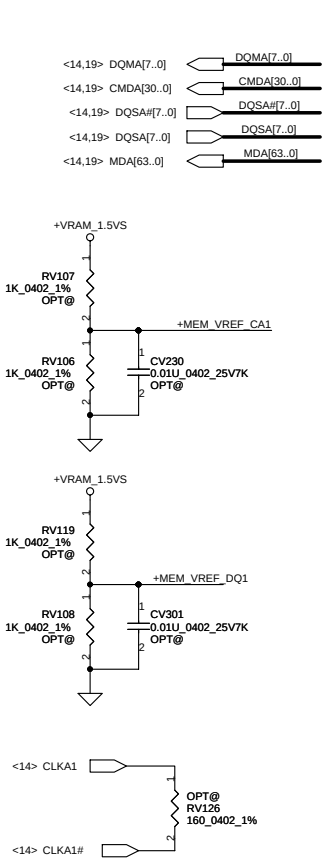
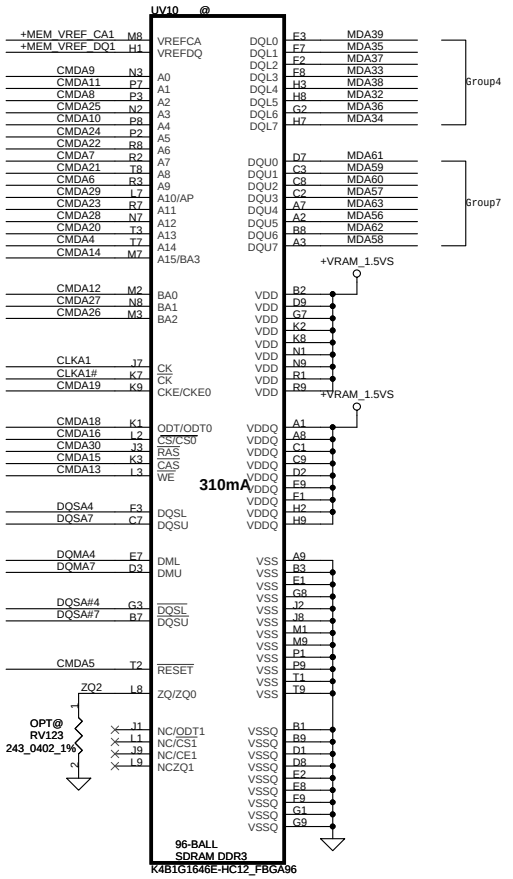
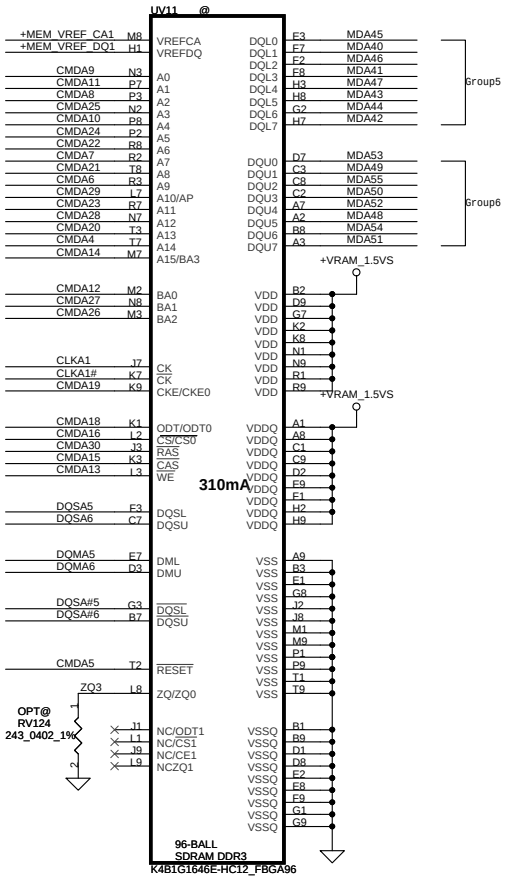
VRAM DDR3 chips (1GB)

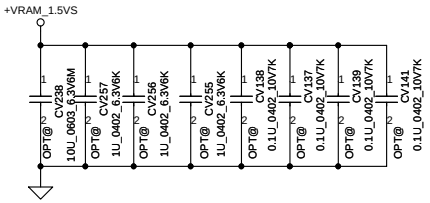
64Mx16 DDR3 *8==>1GB

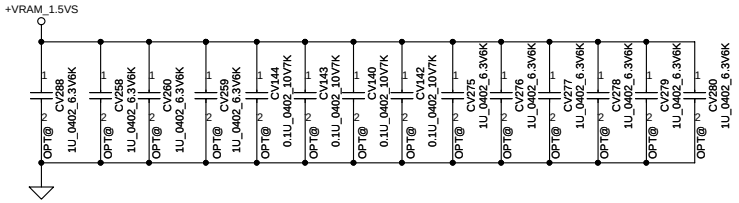






Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH



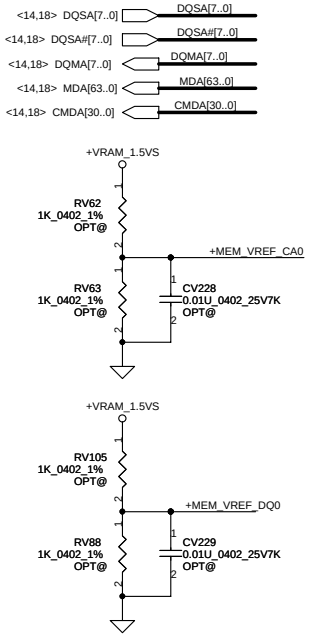


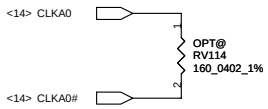
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

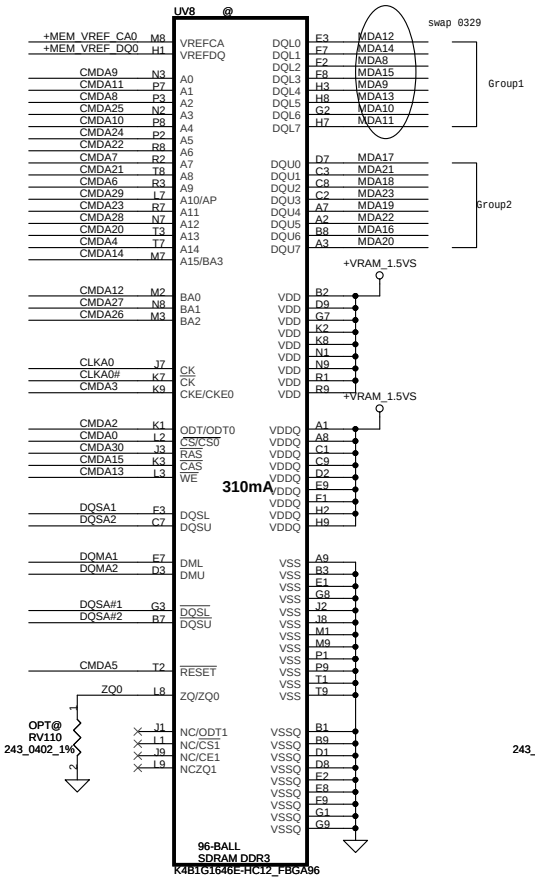
Compal Electronics, Inc.	
Title	VGA_N13P VRAM Channel AH
Size: Custom	Document Number
Rev	1.0
Date: Tuesday, October 16, 2012	Sheet 18 of 53

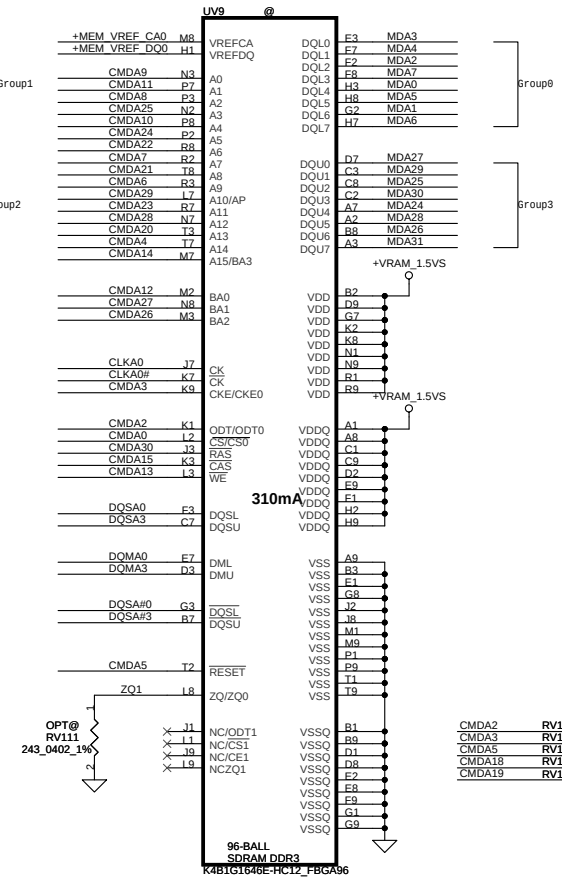
VRAM DDR3 chips (1GB)

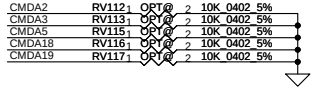
64Mx16 DDR3 *8==>1GB



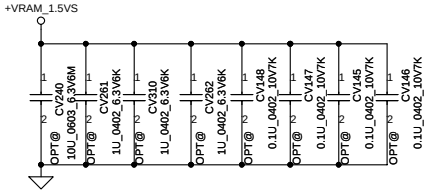


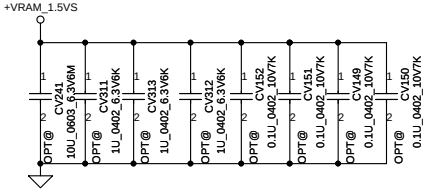






	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data	
Issued Date	2012/04/19	Deciphered Date 2015/04/19

Compal Electronics, Inc.

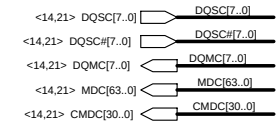
Title: VGA_N13P VRAM Channel AL

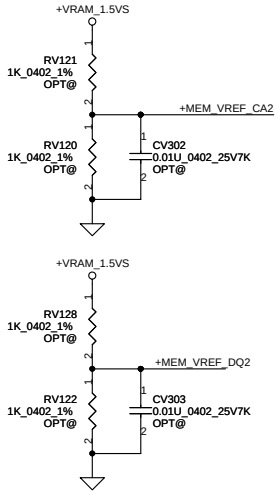
Size: Custom | Document Number | Rev 1.0

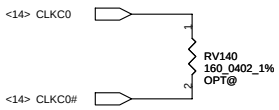
Date: Tuesday, October 16, 2012 | Sheet 19 of 53

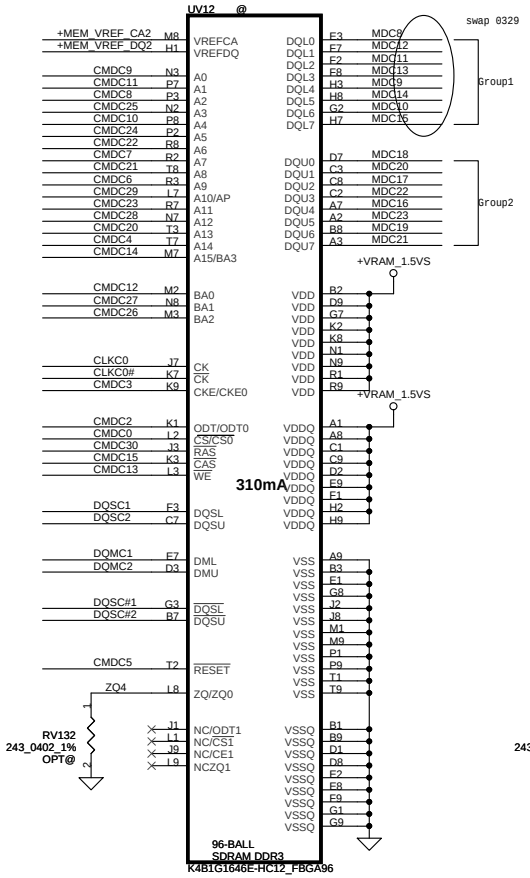
VRAM DDR3 chips (1GB)

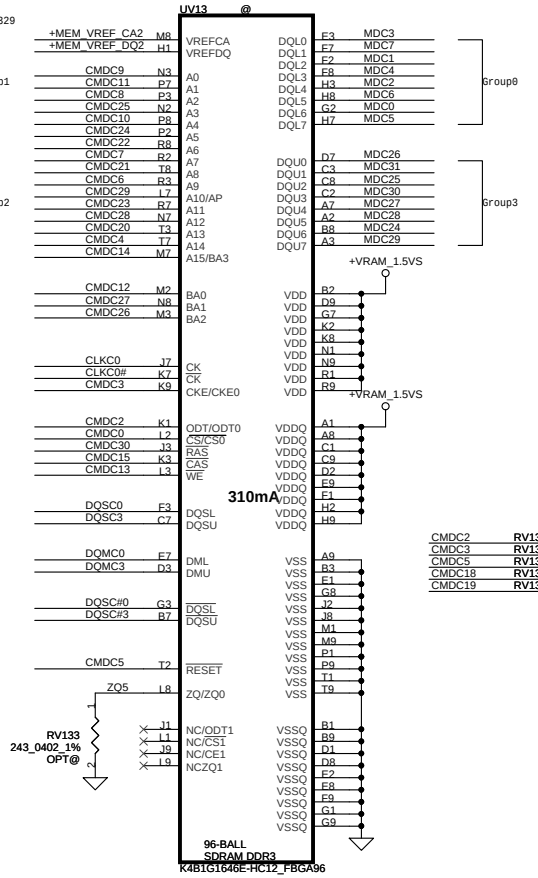
64Mx16 DDR3 *8==>1GB

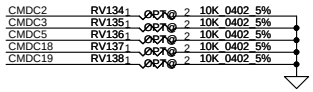






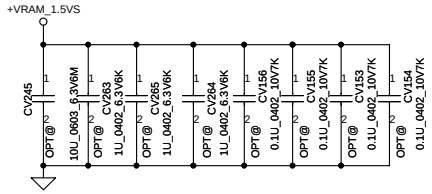


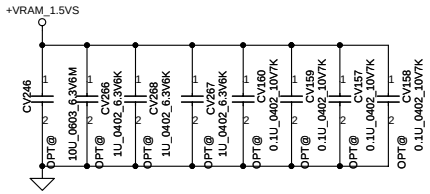


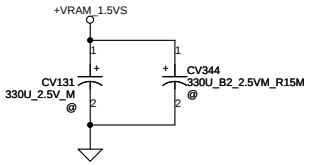


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

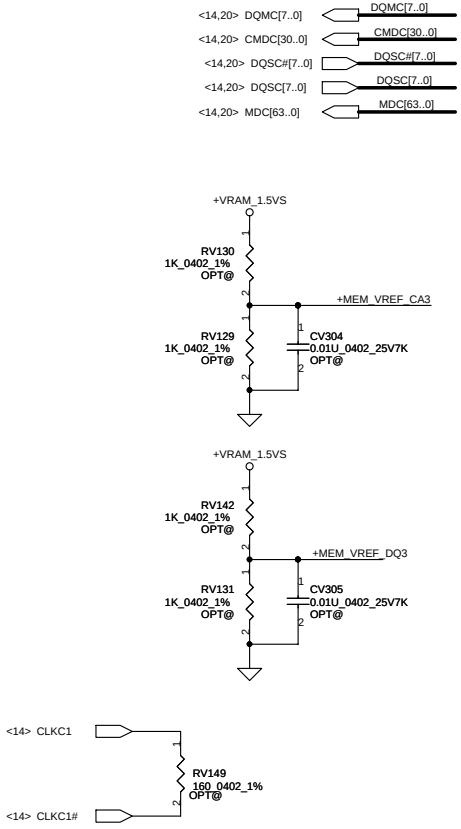
Title: VGA_N13P VRAM Channel CL

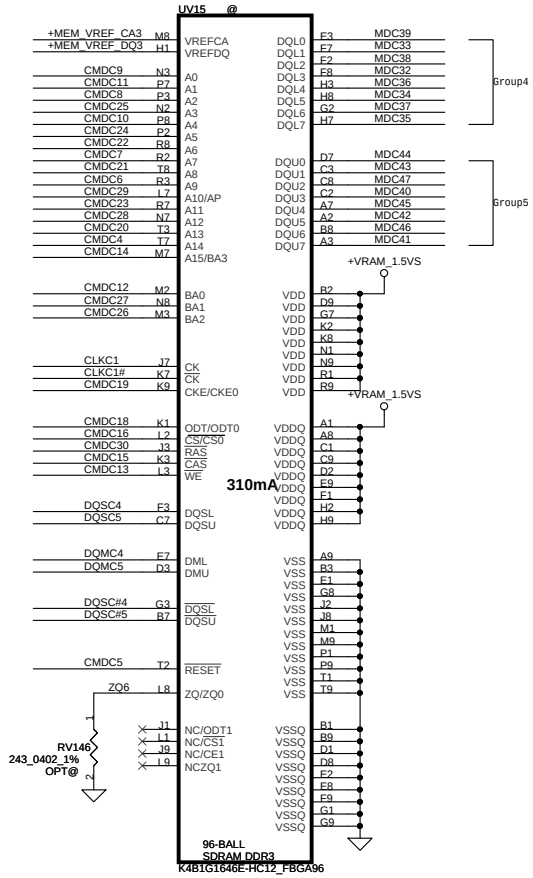
Size: Custom | Document Number | Rev: 1.0

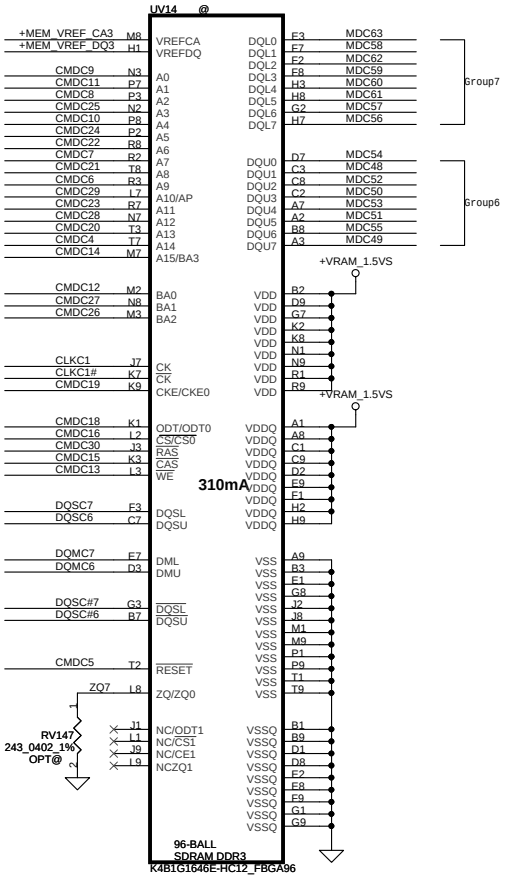
Date: Tuesday, October 16, 2012 | Sheet 20 of 53

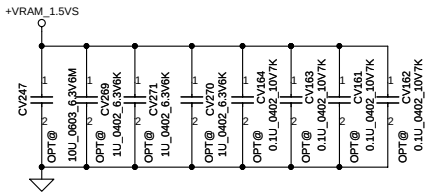
VRAM DDR3 chips (1GB)

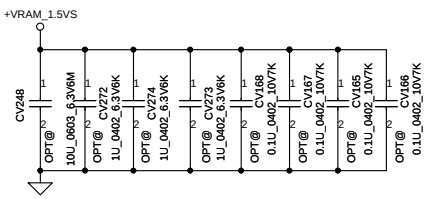
64Mx16 DDR3 *8==>1GB





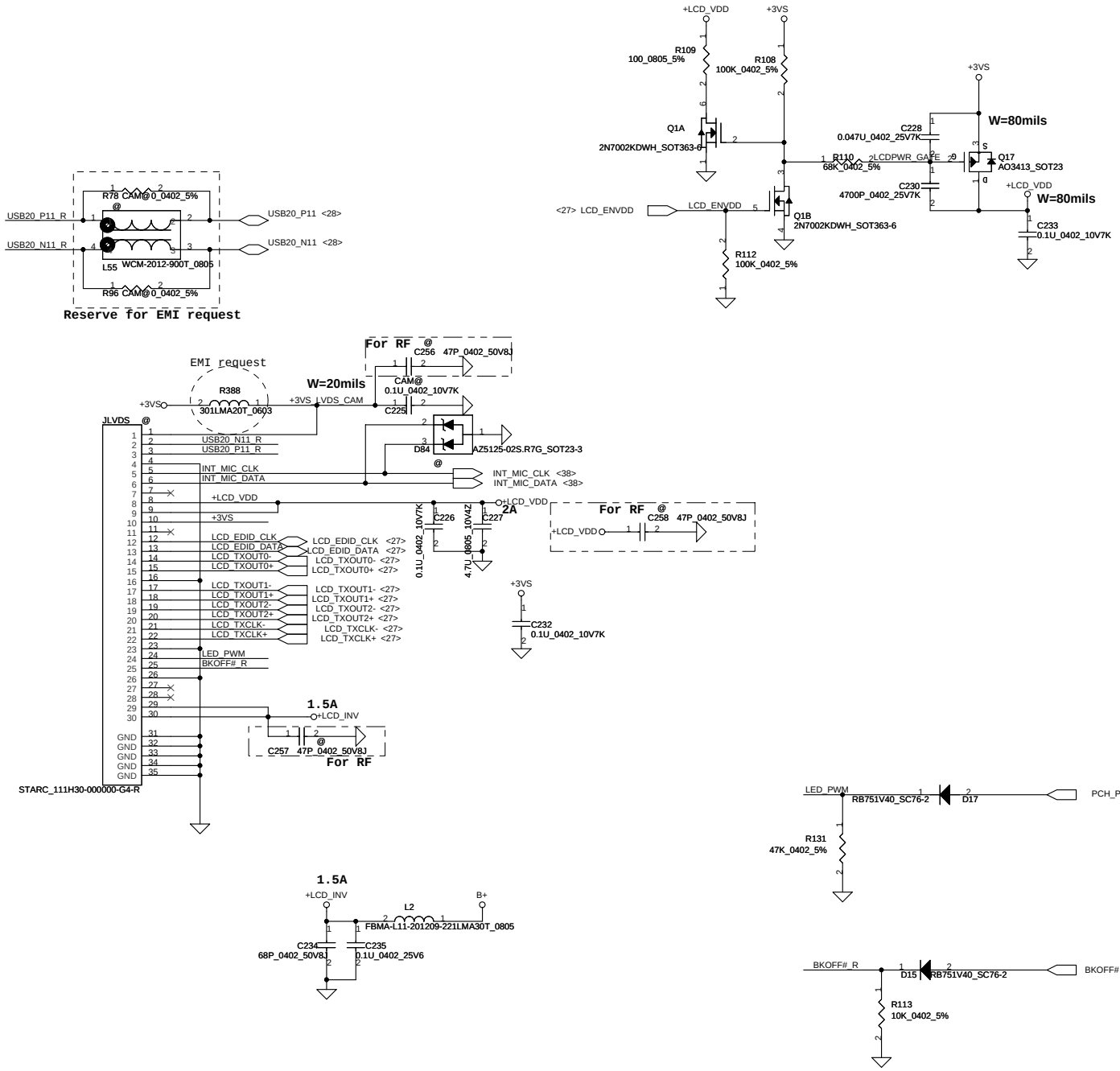






Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: VGA_N13P VRAM Channel CH
			Size: Custom; Document Number; Rev: 1.0
			Date: Tuesday, October 16, 2012; Sheet 21 of 53



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: LVDS
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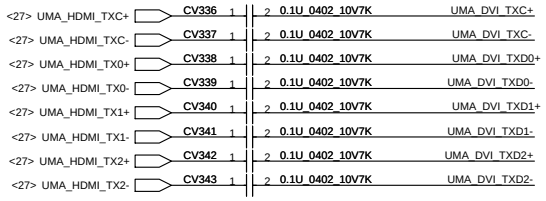
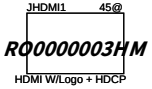
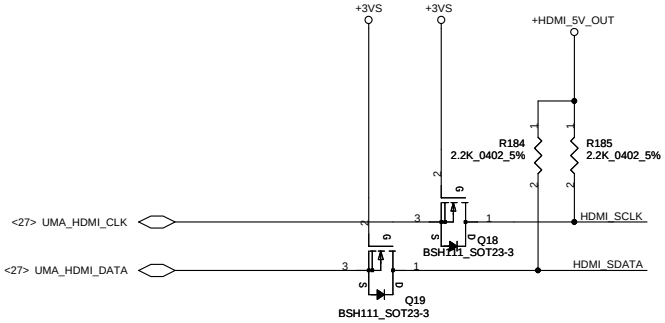
			Date: Tuesday, October 16, 2012; Sheet 22 of 53

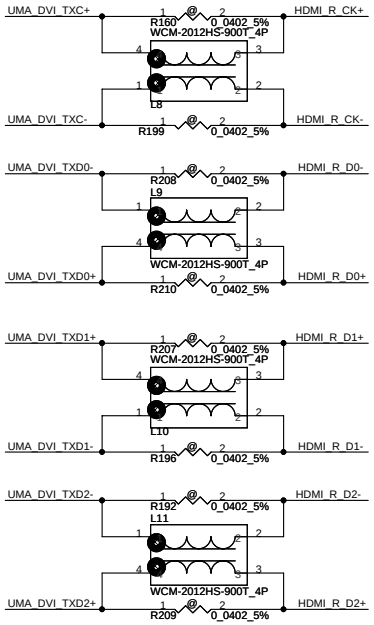


HDMI Royalty

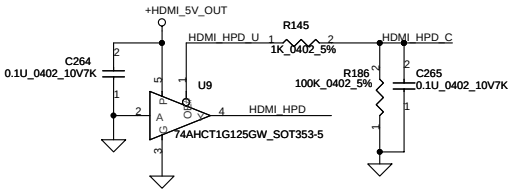


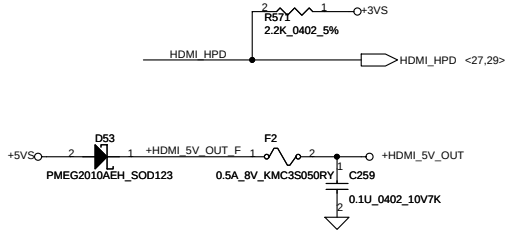
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

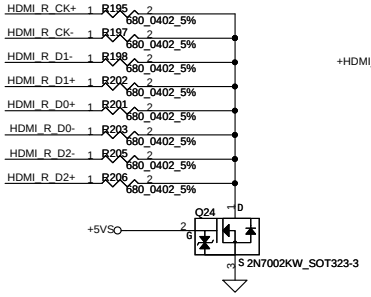




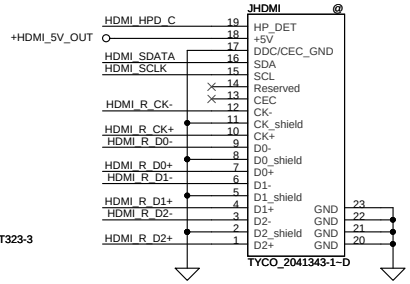
common CHOKE use 67ohm
5/30 change to 90ohm EMI request







HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	HDMI Conn.
Size	Document Number: VCUAA
Rev	1.0
Date: Tuesday, October 16, 2012	Sheet 23 of 53

CMOS Setting, near DDR Door

iME Setting.

Placement near to YH1

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

PCH_SPKR
High = Enabled "No Reboot Mode"
* Low = Disabled (Default)

Change Net name due to this function is high active

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Chief River Mobile platform

SPI ROM for BIOS & ME (4MByte)

4MB ROM P/N:
SA00003K800
SA00004LI00

SPI ROM for Win8 (2MByte)

2MB ROM P/N:
SA000041N00
SA00003FO10

Socket: SP07000F500/SP07000H900
Please place U13 & U4 close to U2 PCH,
please place RH66, RH67, RH68 near UH3
Please place RH267 near RH66, Please place RH271 near RH67,
Please place RH269 near RH68.

BOOT BIOS Strap Bit 0
If use GCLK, please delete DH1

Un-mount for reduce power consumption at S0, S3 state

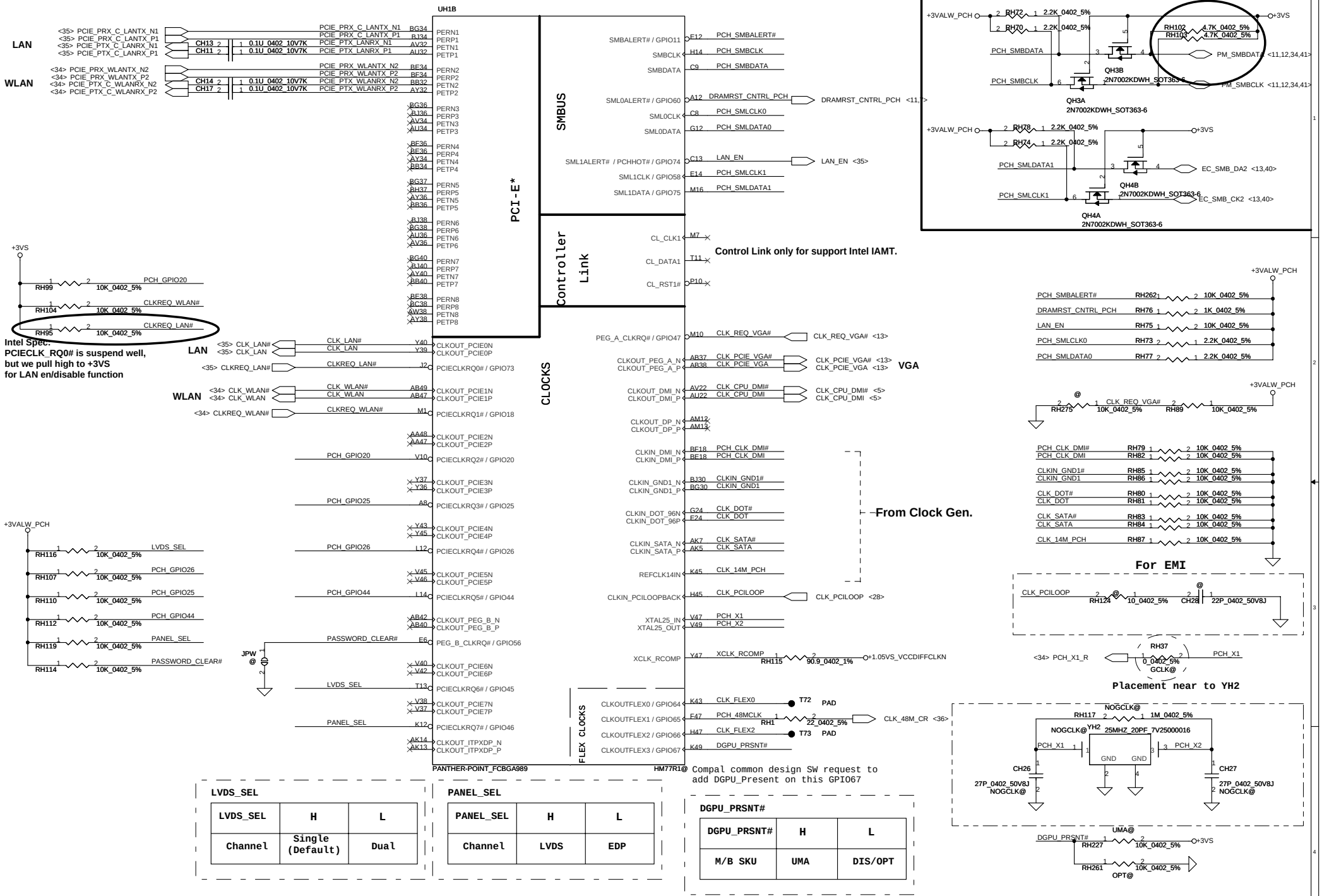
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: PCH_HDA/JTAG/SATA/SPI/LPC

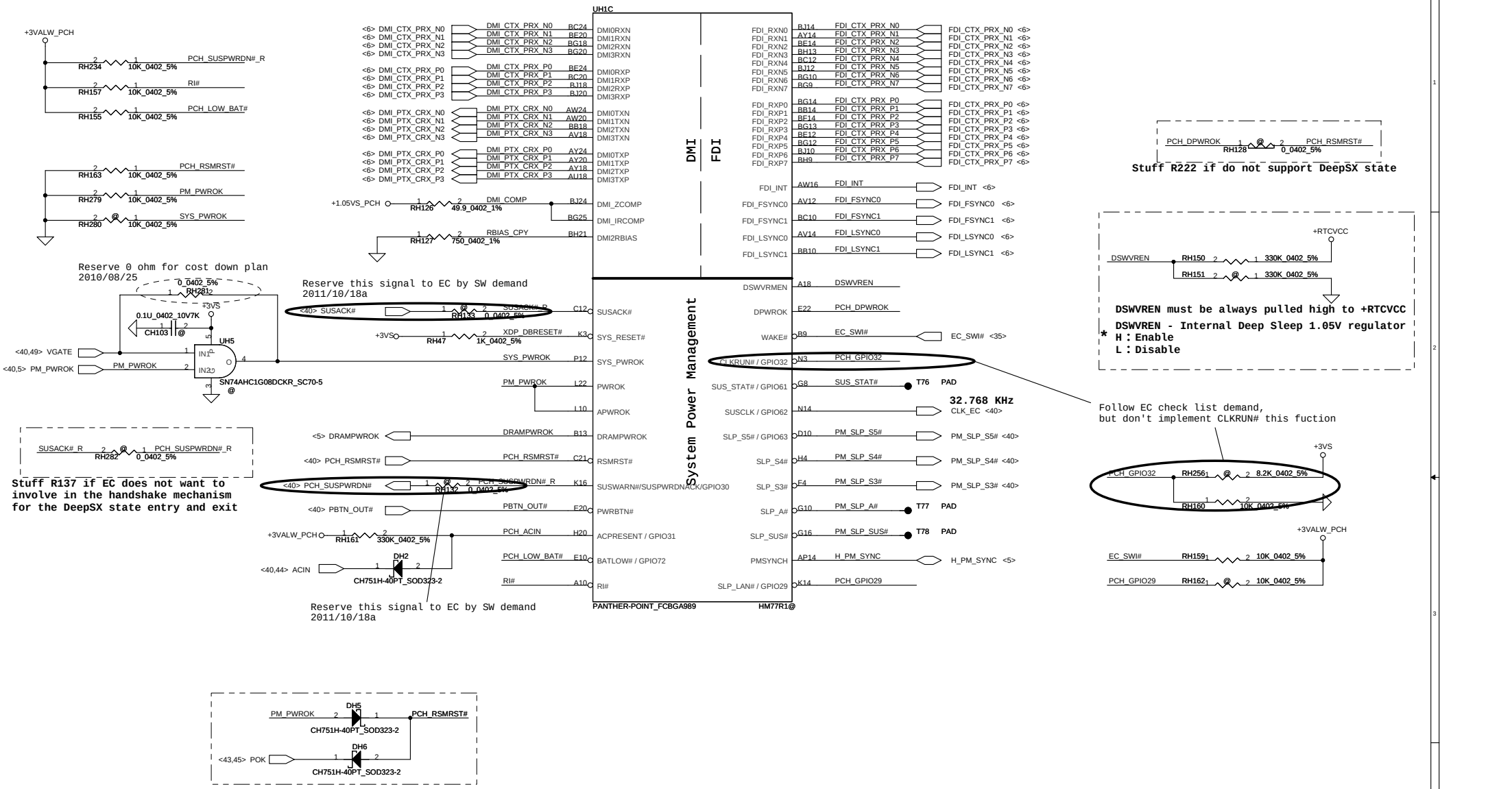
Size: Custom | Document Number: VCUAA | Rev: 1.0

Date: Tuesday, October 16, 2012 | Sheet 24 of 53



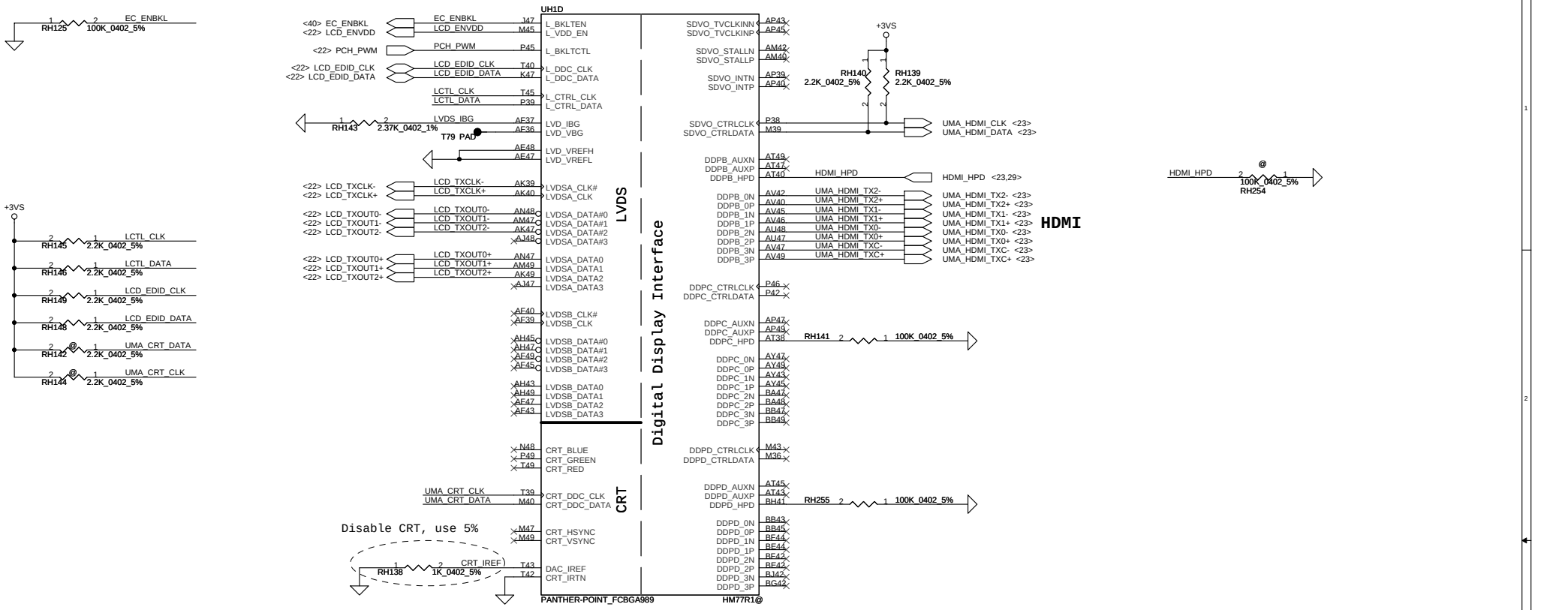
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	PCH_PCI-E/SMBUS/CLK		
Size Custom	Document Number VCUAA		Rev 1.0
Date: Tuesday, October 16, 2012	Sheet 25 of 53		



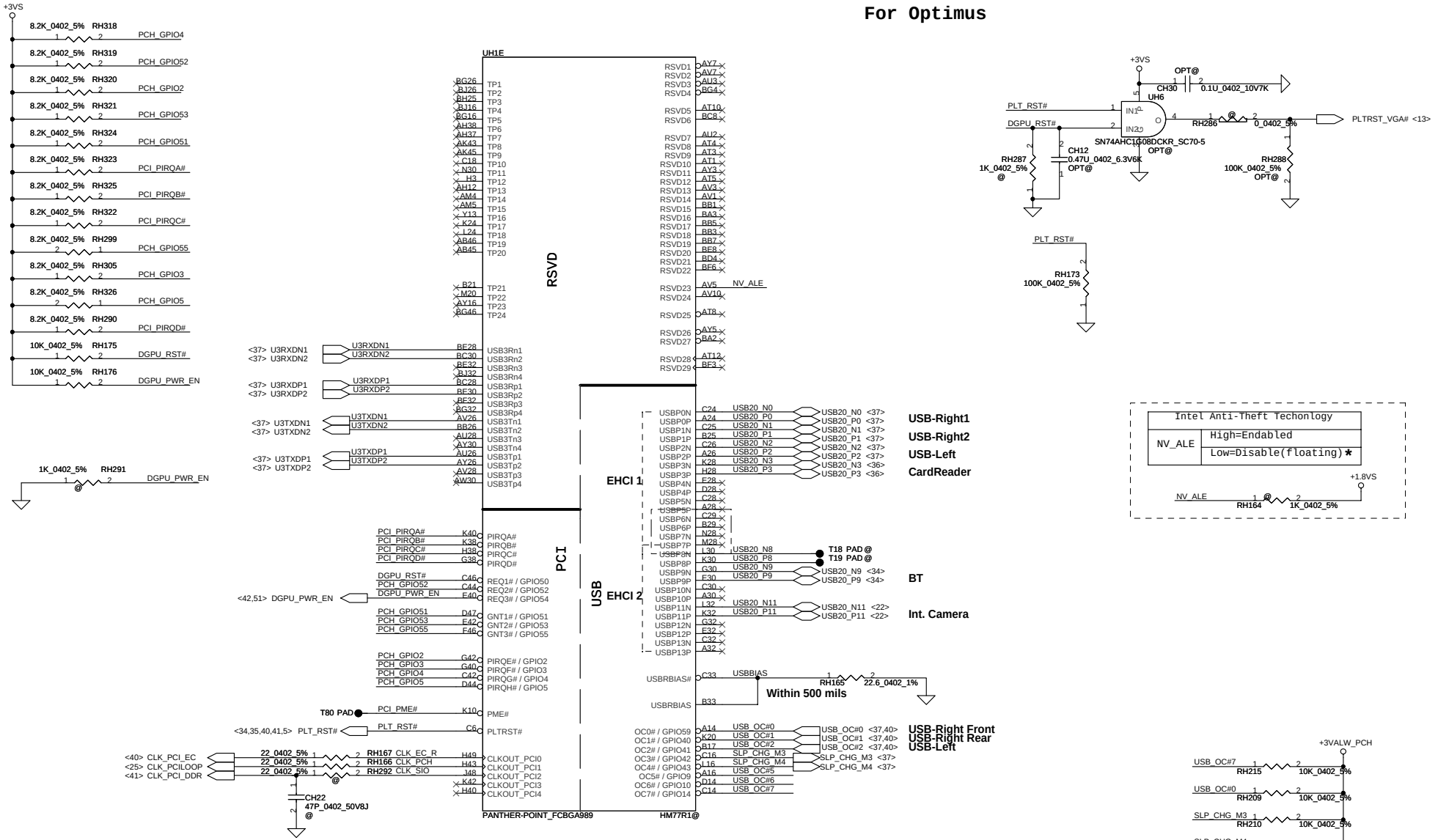
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: PCH_DMI/FDI/PM			
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 26 of 53		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_CRT/LVDS/HDMI
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 27 of 53		

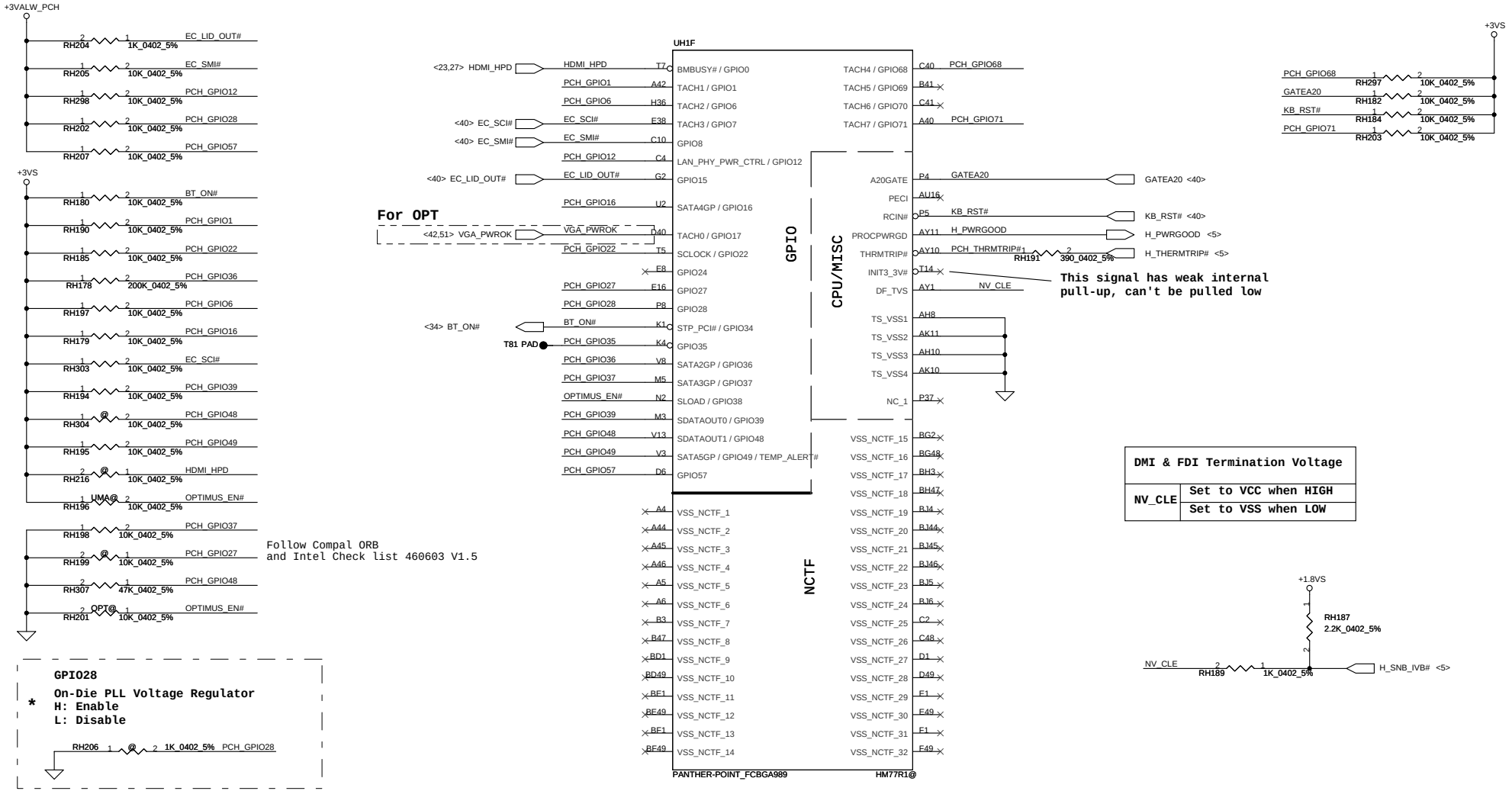
For Optimus



Boot BIOS Strap		
RF_OFF# PCH_GPIO51	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap		
WL_OFF#	*	Low= A16 swap override Enable High= A16 swap override Disable

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_PCI/USB/NAND
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 28 of 53		



DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

GPIO28

* **On-Die PLL Voltage Regulator**
H: Enable
L: Disable

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
* **L: Enable**

RH308 1 @ 2 1K_0402_5% EC_SMI#

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

PCH_GPIO57

HDD2_DET#	H	L
SKU	ONE HDD	TWO HDD

PCH_GPIO71

3D_DET#	H	L
SKU	Non3D	3D

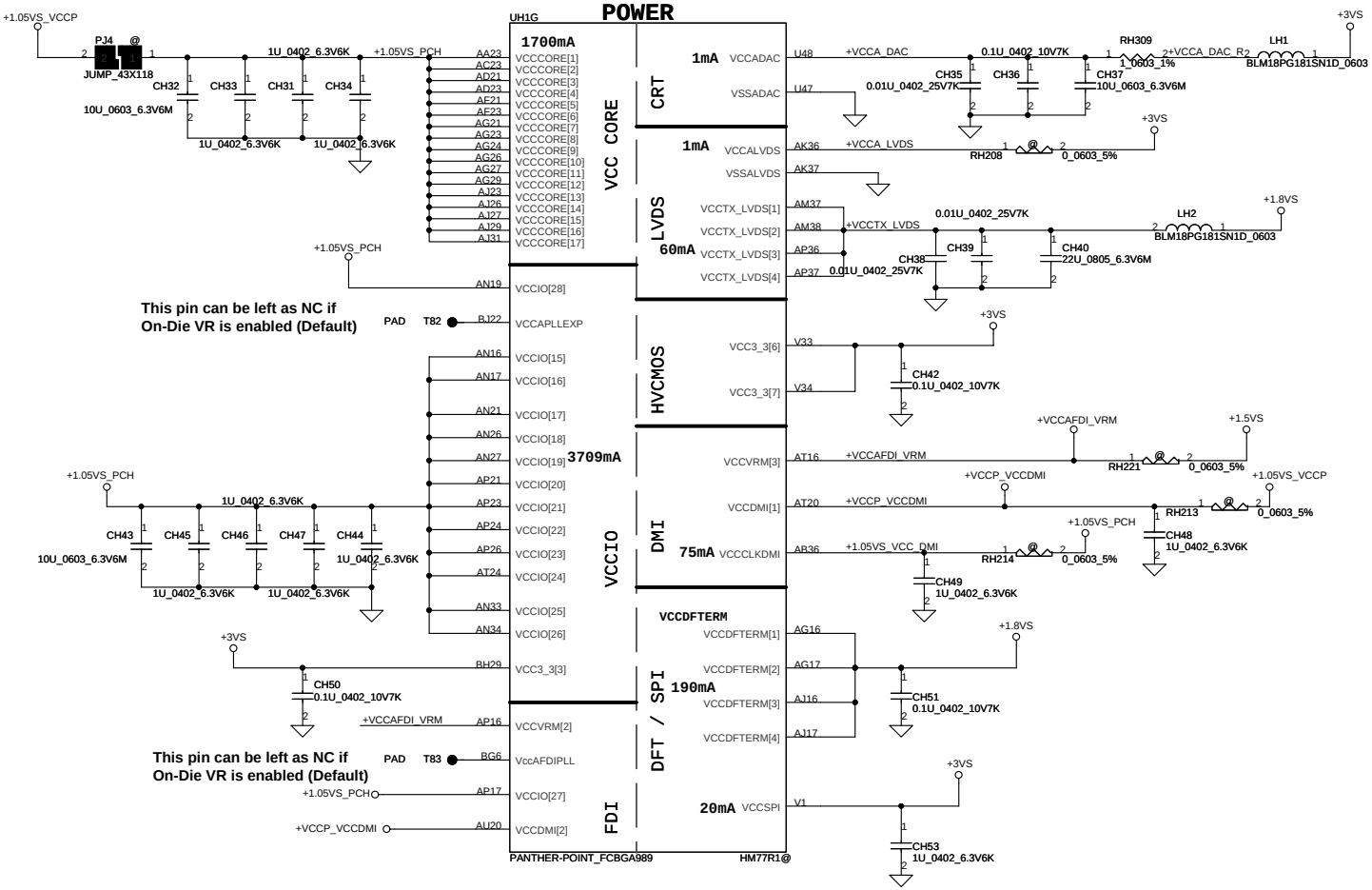
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***PCH_CPU/GPIO***

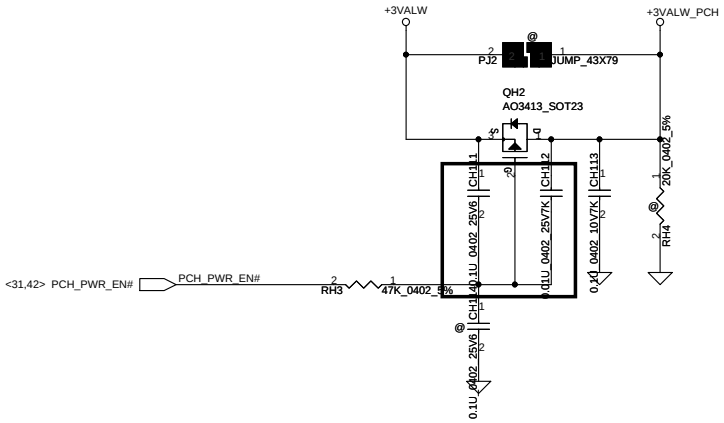
Size: Custom | Document Number: **VCUAA** | Rev: 1.0

Date: Tuesday, October 16, 2012 | Sheet 29 of 53

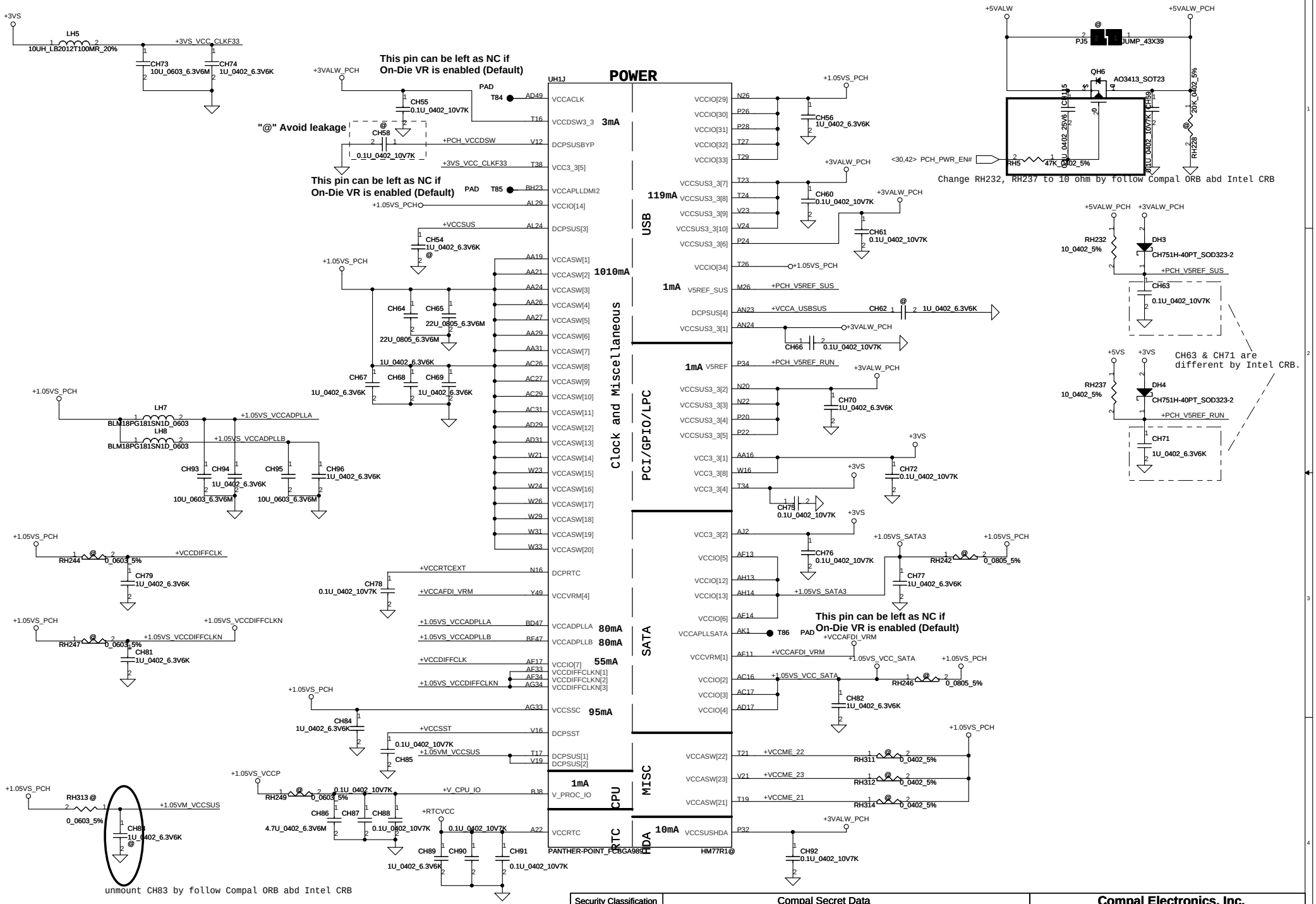


PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3V_PCH

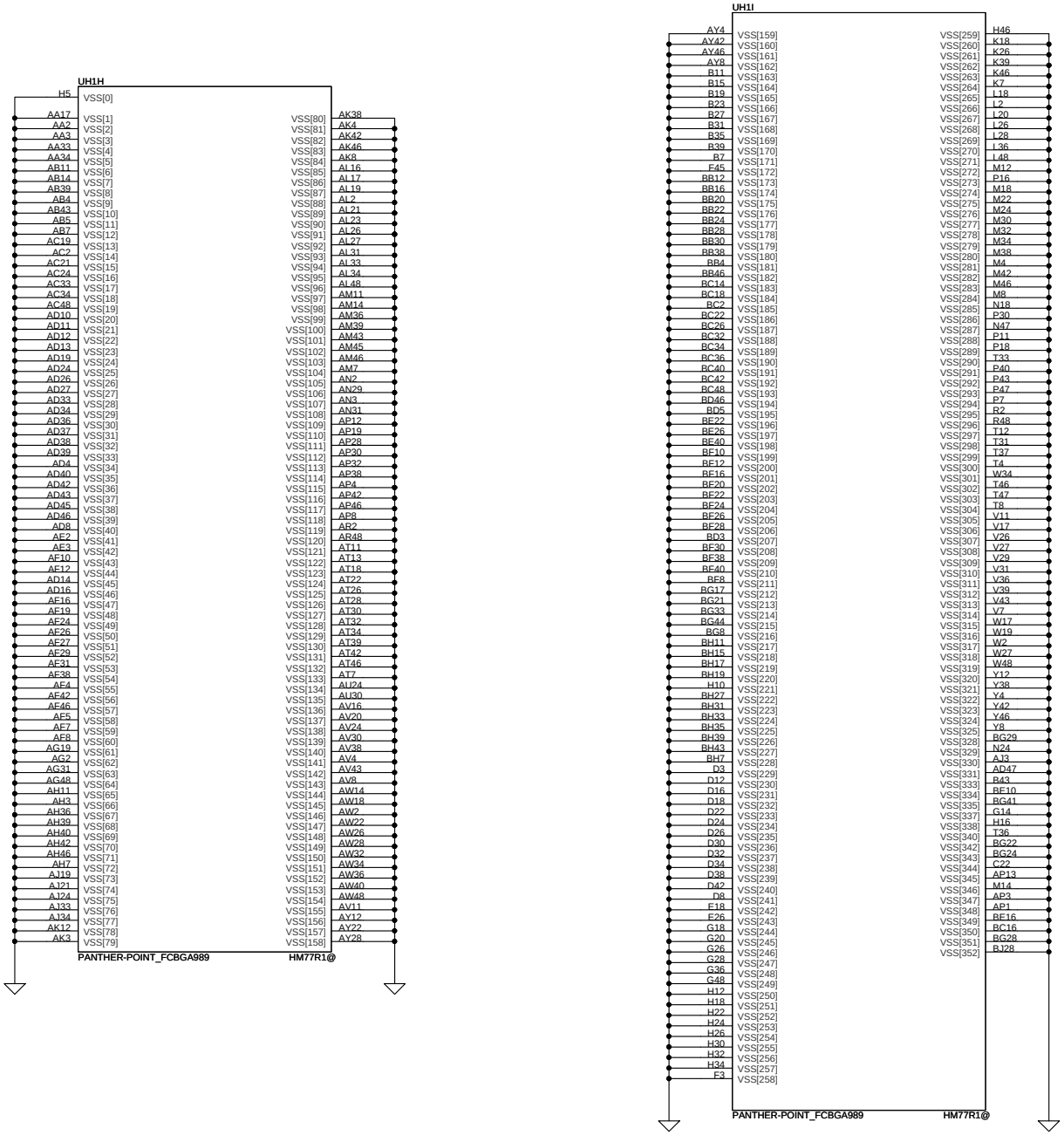


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: *PCH_POWER-1*
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 30 of 53		



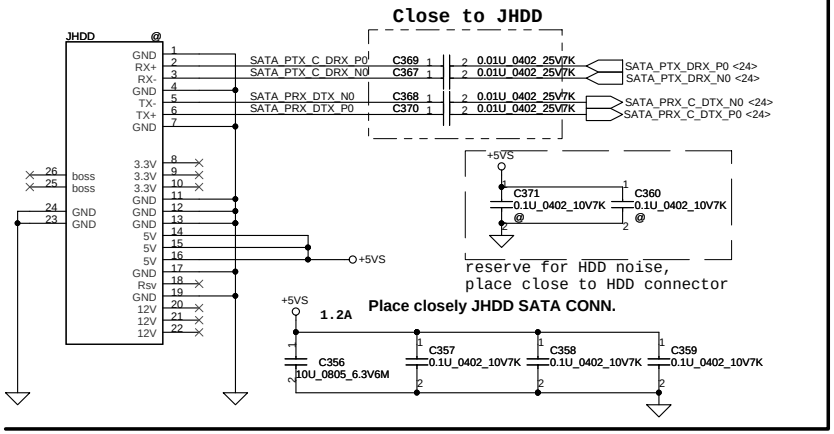
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: PCH_POWER-2			
Size: Custom	Document Number: VCUAA		Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 31 of 53		



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PCH_GND
				Size: Custom	Document Number: VCUAA
				Date: Tuesday, October 16, 2012	Sheet 32 of 53

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: **HDD**

Size | Document Number: **VCUAA** | Rev: 1.0

Date: Tuesday, October 16, 2012 | Sheet 33 of 53

Slot 1 Half PCIe Mini Card-WLAN

+3VS — PJ6 @JUMP_43X79 — +3V_WLAN

Short for WIFI

+3VALW — PJ9 @JUMP_43X79 — +3V_WLAN

reserve for BT issue

40 mils

+3V_WLAN — 0.1U_0402_10V7K — CM1 CM2 CM3 — C253 47P_0402_50V8J @ — 0.01U_0402_25V7K 4.7U_0805_10V4Z — For SED

+1.5VS — 0.1U_0402_10V7K — CM7 CM8 CM9 — C254 47P_0402_50V8J @ — 0.01U_0402_25V7K 4.7U_0805_10V4Z — For SED

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

BT_CTRL

<29> BT_ON# — 0_0402_5% R1444 — QM1A 2N7002DW-T/R7_SOT363-6 — QM1B 2N7002DW-T/R7_SOT363-6

<40> EC_BT_ON# — 0_0402_5% R1445 @

<42,5,9> SUSP

+1.5VS +3V_WLAN

JWLAN @

BT_CTRL 0_0402_5% BT_CTRL_R R1443

<25> CLKREQ_WLAN#

<25> CLK_WLAN#

<25> CLK_WLAN

<25> PCIE_PRX_WLANTX_N2

<25> PCIE_PRX_WLANTX_P2

WLAN/ WiFi

<25> PCIE_PTX_C_WLANRX_N2

<25> PCIE_PTX_C_WLANRX_P2

+3V_WLAN

<40> E51_TXD — R16 0_0402_5%

<40> E51_RXD — R17 0_0402_5% — E51_RXD_R

Debug card using

BELLW_80060-1021

+3V_WLAN — RM17 8.2K_0402_5%

BT_CTRL — R327 1K_0402_5% — E51_RXD_R

For isolate Intel Rainbow Peak and Compal Debug Card.

WLAN_OFF# — WL_OFF# <40>

PLT_RST# — PLT_RST# <28,35,40,41,5>

PM_SMBCLK <11,12,25,41>

PM_SMBDATA <11,12,25,41>

USB20_N9 <28>

USB20_P9 <28>

BT

+3V_WLAN — C266 47P_0402_50V8J @

+1.5VS — C260 47P_0402_50V8J @

Slot 2 Full PCIe Mini Card- mSATA

+3VS

JMSATA @

SATA_PRX_DTX_P1

SATA_PRX_DTX_N1

SATA_PTX_C_DRX_N1

SATA_PTX_C_DRX_P1

+3VS

BELLW_80060-1021

For RF — +3VS — 120 mils — For SED

47P_0402_50V8J — 0.1U_0402_10V7K — CM18 CM19 @ CM4 CM5 CM6 — CM20 47P_0402_50V8J @ — 680P_0402_50V7K 0.01U_0402_25V7K 4.7U_0805_10V4Z

EMI request 8/7

SATA_PRX_DTX_N1 — CM21 0.01U_0402_25V7K — SATA_PRX_C_DTX_N1 — SATA_PRX_C_DTX_N1 <24>

SATA_PRX_DTX_P1 — CM22 0.01U_0402_25V7K — SATA_PRX_C_DTX_P1 — SATA_PRX_C_DTX_P1 <24>

SATA_PTX_C_DRX_N1 — CM23 0.01U_0402_25V7K — SATA_PTX_DRX_N1 — SATA_PTX_DRX_N1 <24>

SATA_PTX_C_DRX_P1 — CM24 0.01U_0402_25V7K — SATA_PTX_DRX_P1 — SATA_PTX_DRX_P1 <24>

+3VL — CCL1 GCLK@ — 0.1U_0402_10V7K

+3V_LAN — CCL2 GCLK@ — 0.1U_0402_10V7K

+1.05VS_VCCP — CCL3 GCLK@ — 0.1U_0402_10V7K

+3VS_VDDIO — CCL6 GCLK@ — 0.1U_0402_10V7K

+3VALW — CCL8 GCLK@ — 0.1U_0402_10V7K

C16 22U_0805_6.3V6M GCLK@

CCL7 2.2U_0402_6.3V6M GCLK@

PJ8 @ — PAD-OPEN 2x2m

UCL1 G300@ — SLG3NB300VTR_TQFN16_2X3

VBAT	VDD_RTC_OUT
+V3.3A	
VDD	
	32kHz
VDDIO_27M	27MHz
VDDIO_25M_A	25MHz_A
VDDIO_25M_B	25MHz_B
XTAL_IN	
XTAL_OUT	
GND1 GND2 GND3 GND4	

+RTCBATT

+3VL

+3VALW

+3VS_DGPU

+3V_LAN

+1.05VS_VCCP

+RTCVCC_GCLK — +RTCVCC

PCH_RTCX1_R — PCH_RTCX1_R <24>

VGA_X1_R — RCL3 OPT@ 22_0402_5% — VGA_X1 <13>

LAN_X1_R_R — PCH_X1_R_R

22 ohm for NV chip

G304@ — RCL4 0_0603_5% — AO3413_SOT23 — QCL1 G300@

<42> VGA_PWROK#

CLK_X1 — CLK_X2

UCL1 SLG3NB244VTR_TQFN16_2X3 UMA@

UCL1 SLG3NB304VTR_TQFN16_2X3 G304@

PCH_X1_R_R — RCL1 GCLK@ 0_0402_5% — PCH_X1_R <25>

LAN_X1_R_R — RCL2 GCLK@ 33_0402_5% — LAN_X1_R <35>

CCL10 5P_0402_50V8C GCLK@

EMI request 11/06

LAN_X1_R_R — RCL5 @ 0_0402_5%

Reserved for Swing Level adjustment (Close GCLK side)

YCL1 GCLK@ 25MHZ 12PF X3G025000DK1H-X

CLK_X1 — CCL4 18P_0402_50V8J GCLK@

CLK_X2 — CCL5 15P_0402_50V8J GCLK@

	OPT	UMA
GCLK	300(default) SA00005RS00 304(low power)	244 SA000057I00

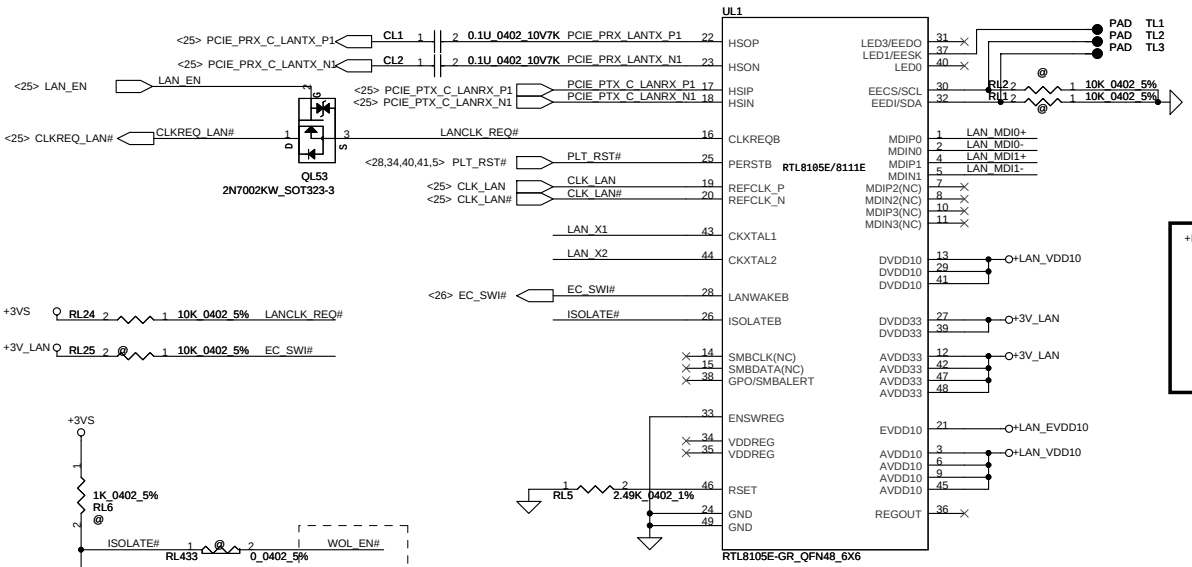
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

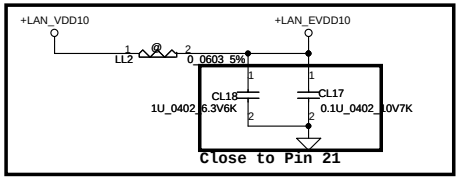
Compal Electronics, Inc.

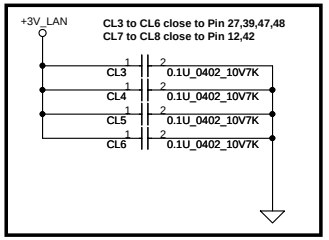
Title: PCIe-WLAN/mSATA/GCLK

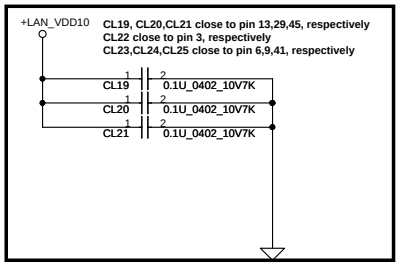
Size: — Document Number: VCUAA — Rev: 1.0

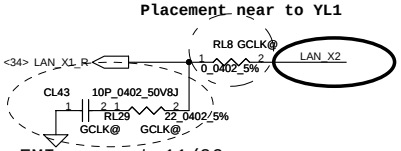
Date: Tuesday, October 16, 2012 — Sheet 34 of 53







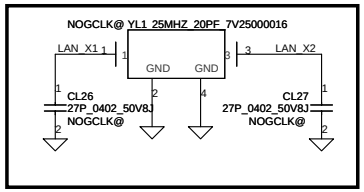




	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

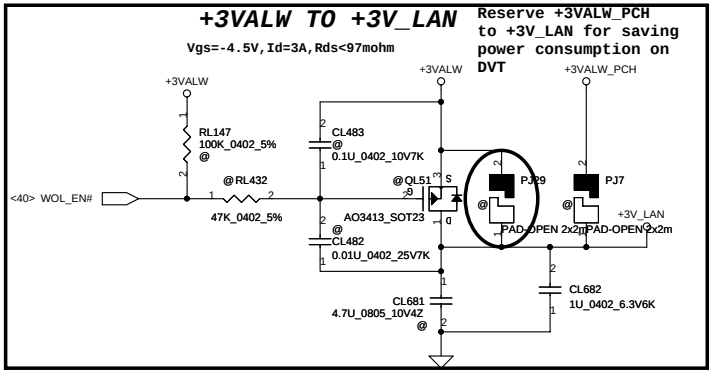
	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)



+3VALW TO +3V_LAN

Vgs=-4.5V,Id=3A,Rds<97mohm

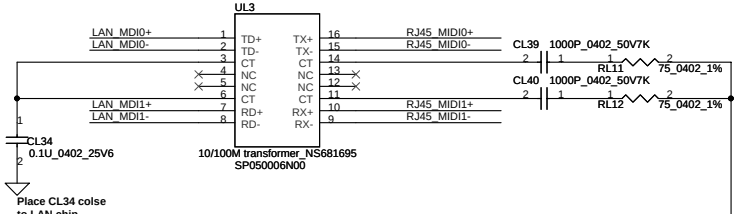
Reserve +3VALW_PCH to +3V_LAN for saving power consumption on DVT



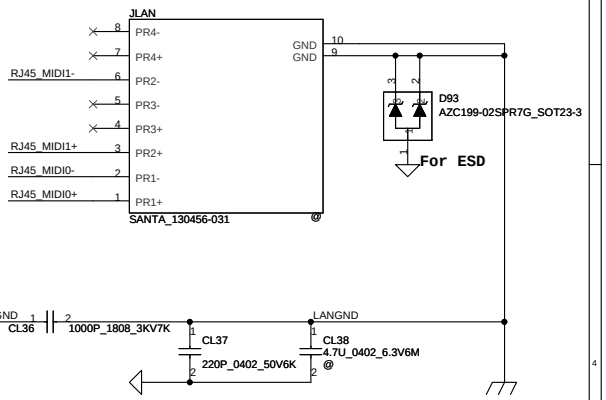
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



LAN Conn.



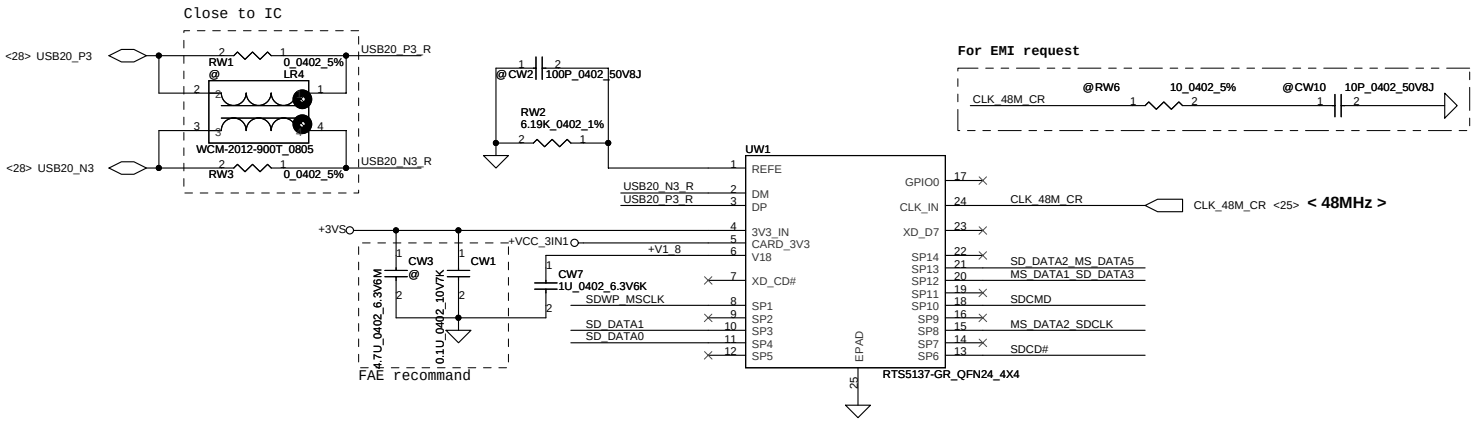
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

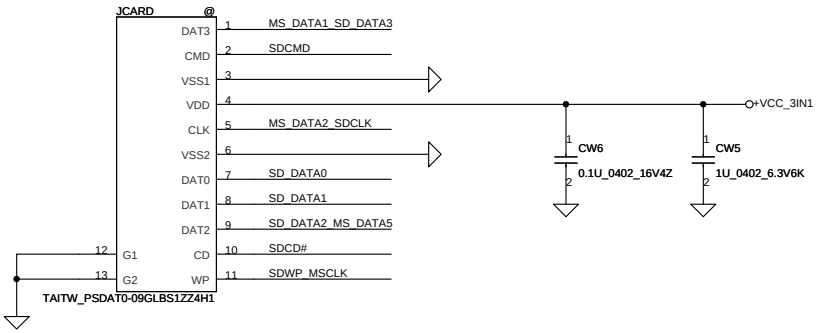
Title: PCIe-LAN-RTL8105E

Size: Custom | Document Number: VCUAA | Rev: 1.0

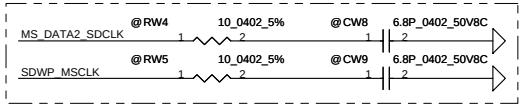
Date: Tuesday, October 16, 2012 | Sheet 35 of 53



< 2 in 1 Card Reader >



For EMI request



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

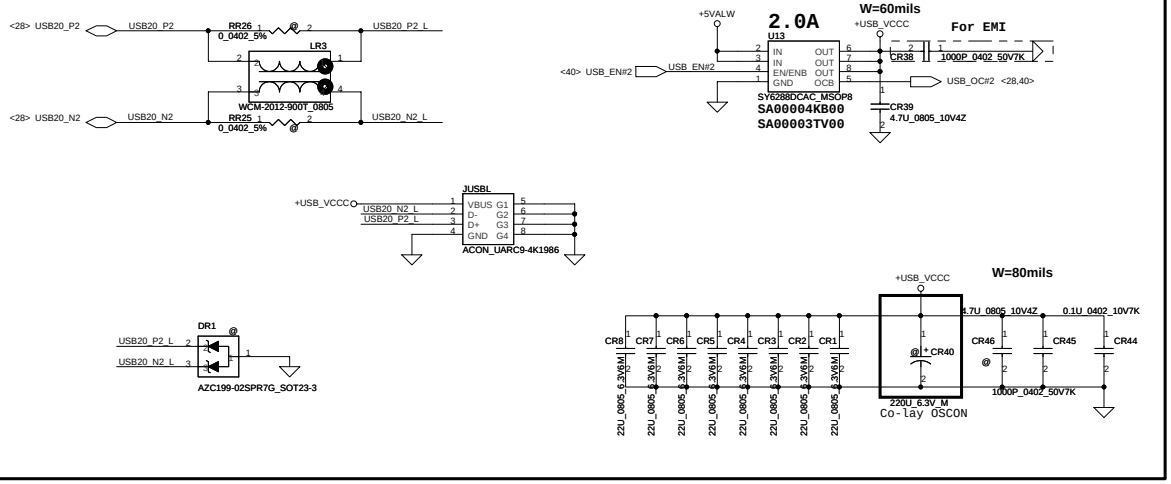
Compal Electronics, Inc.

Title: **USB-CardReader RTS5137**

Size	Document Number	Rev
Custom	VCUAA	1.0

Date: Tuesday, October 16, 2012 | Sheet 36 of 53

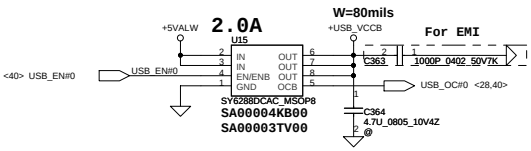
Left USB 2.0 x 1

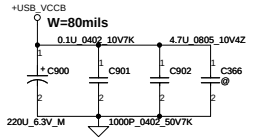


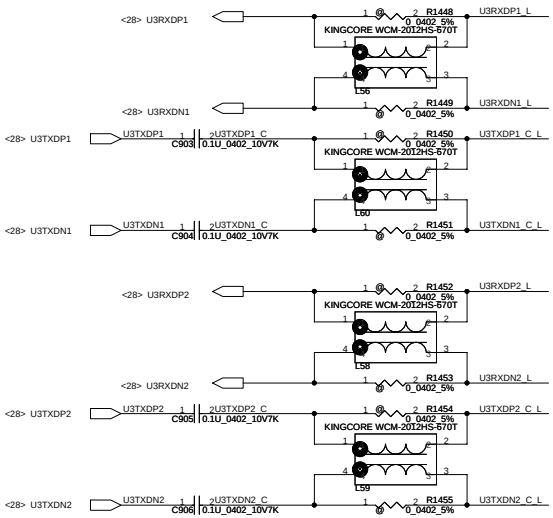
Right side USB 3.0 x 2/ Sleep&Charge

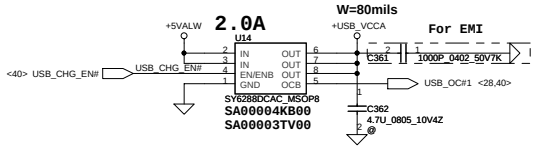
USB Sleep & Charge Auto-Mode/Mode3

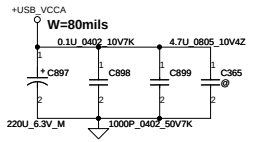
MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers

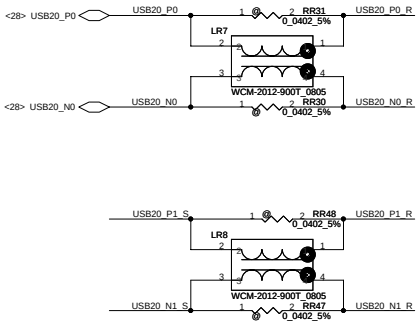


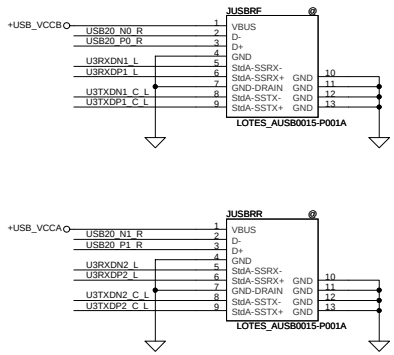


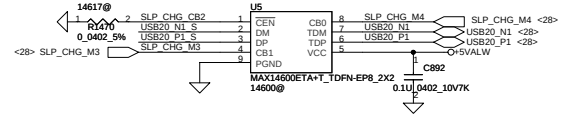


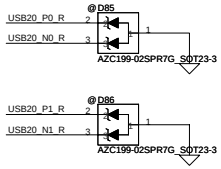


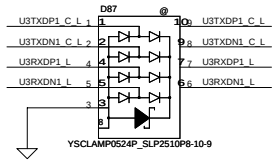


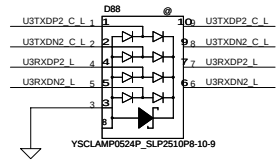












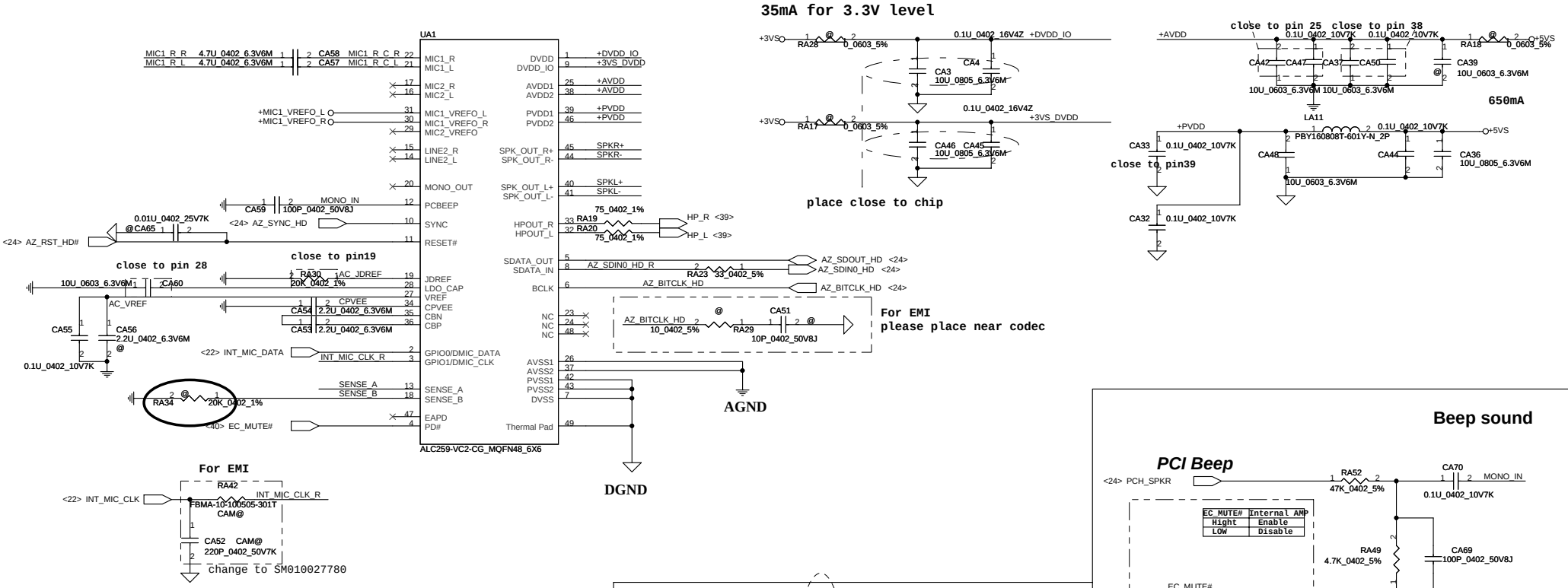
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: LUSB/RUSB/S&C

Size: Custom | Document Number: VCUAA | Rev: 1.0

Date: Tuesday, October 16, 2012 | Sheet 37 of 53

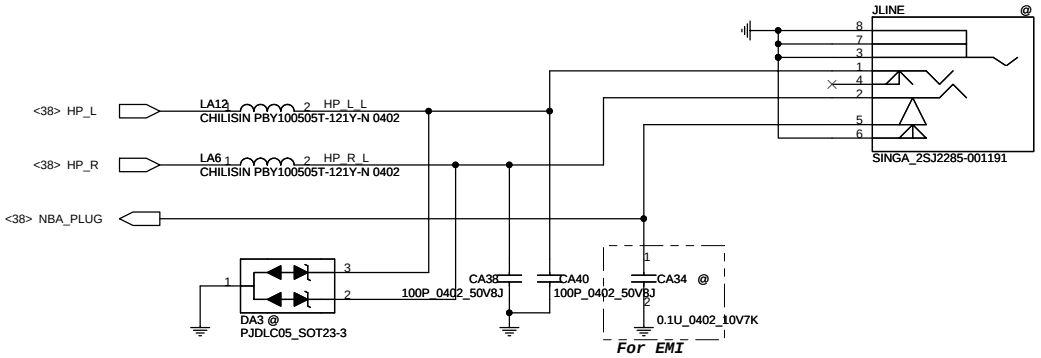


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

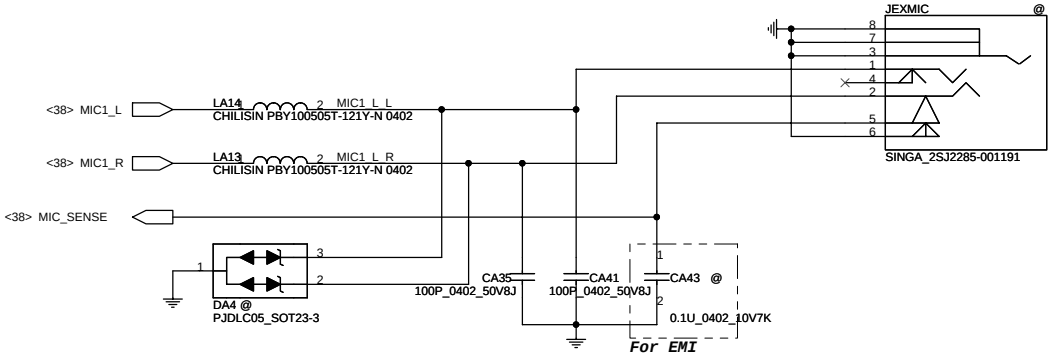
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	HDA-ALC259-VC
Size: Custom	Document Number: Rev
Date: Tuesday, October 16, 2012	Sheet 38 of 53

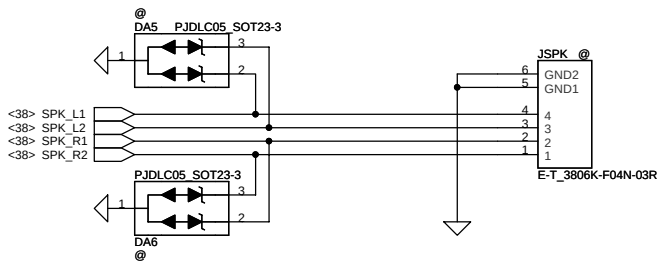
HeadPhone/LINE OUT JACK



EXT.MIC/LINE IN JACK



SPK CONN.



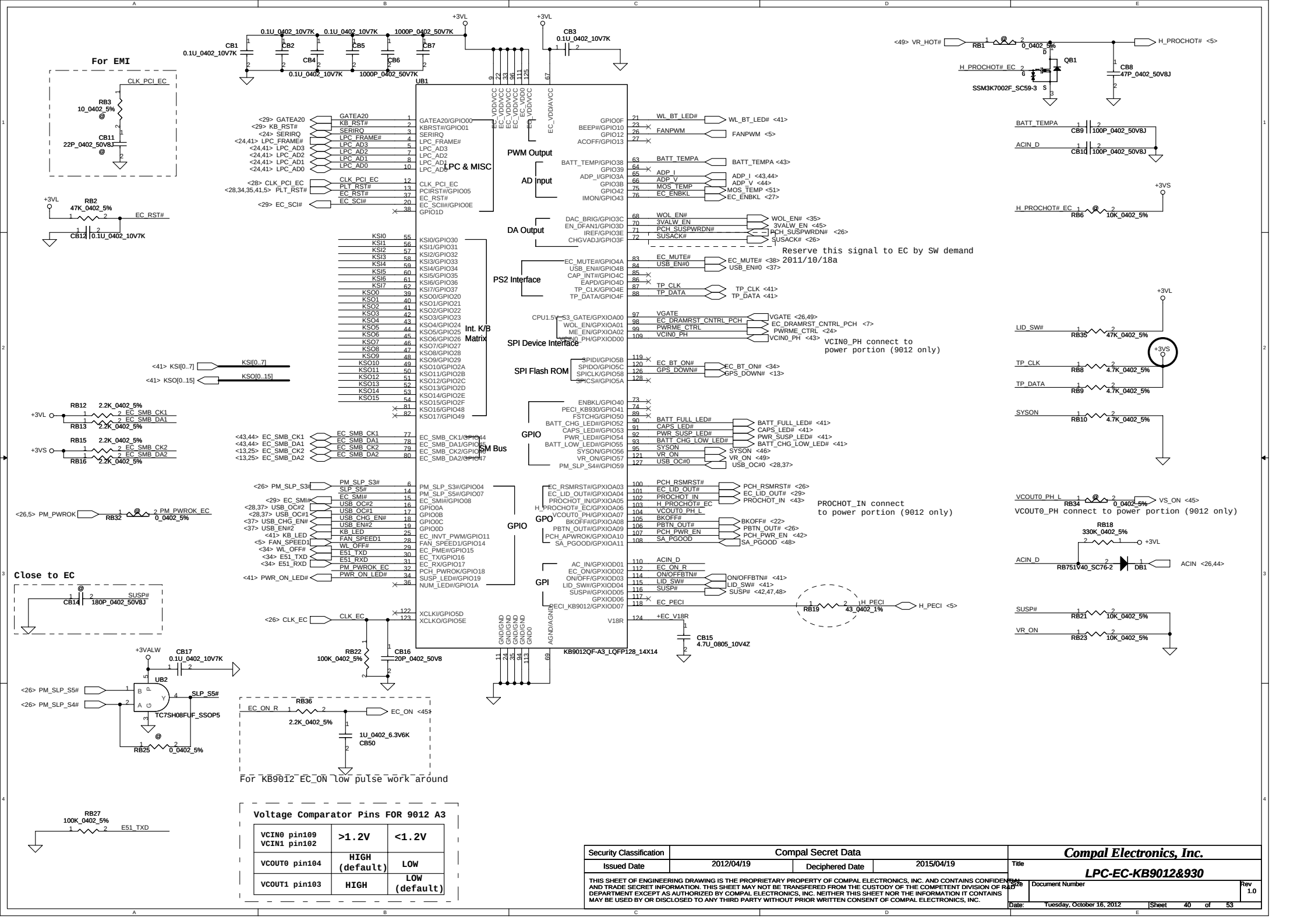
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

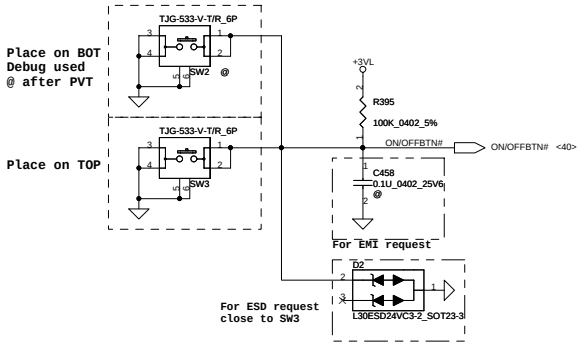
Title: AUDIO CONN

Size | Document Number | Rev 1.0

Date: Tuesday, October 16, 2012 | Sheet 39 of 53

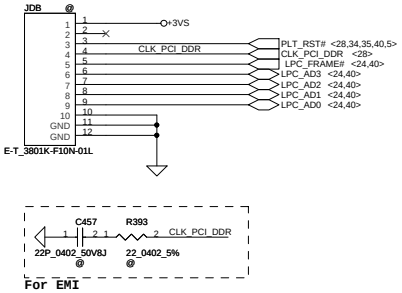

For EMI
CLK_PCI_EC
RB3 10_0402_5% @
CB11 22P_0402_50V8J @
+3VL
RB2 47K_0402_5%
EC_RST#
CB12 0.1U_0402_10V7K
CB1 0.1U_0402_10V7K
CB2
CB4
CB5
CB6
CB7 1000P_0402_50V7K
CB3 0.1U_0402_10V7K
UB1
KB9012QF-A3_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
Int. K/B Matrix
SM Bus
Reserve this signal to EC by SW demand 2011/10/18a
VCIN0_PH connect to power portion (9012 only)
PROCHOT_IN connect to power portion (9012 only)
VCOUT0_PH connect to power portion (9012 only)
QB1 SSM3K7002F_SC59-3
CB8 47P_0402_50V8J
CB9 100P_0402_50V8J
CB10 100P_0402_50V8J
RB6 10K_0402_5%
RB35 47K_0402_5%
RB8 4.7K_0402_5%
RB9 4.7K_0402_5%
RB10 4.7K_0402_5%
RB34 0_0402_5%
RB18 330K_0402_5%
DB1 RB751V40_SC76-2
RB21 10K_0402_5%
RB23 10K_0402_5%
RB19 43_0402_1%
CB15 4.7U_0805_10V4Z
RB12 2.2K_0402_5%
RB13 2.2K_0402_5%
RB15 2.2K_0402_5%
RB16 2.2K_0402_5%
RB32 0_0402_5%
Close to EC
CB14 180P_0402_50V8J
CB17 0.1U_0402_10V7K
UB2 TC7SH08FUF_SSOP5
RB25 0_0402_5%
RB22 100K_0402_5%
CB16 20P_0402_50V8
RB36 2.2K_0402_5%
CB50 1U_0402_6.3V6K
For KB9012 EC_ON low pulse work around
RB27 100K_0402_5%
Voltage Comparator Pins FOR 9012 A3
VCIN0 pin109 VCIN1 pin102 | >1.2V | <1.2V
VCOUT0 pin104 | HIGH (default) | LOW
VCOUT1 pin103 | HIGH | LOW (default)
Security Classification | Compal Secret Data
Issued Date | 2012/04/19 | Deciphered Date | 2015/04/19
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title: LPC-EC-KB9012&930
Size | Document Number | Rev 1.0
Date: Tuesday, October 16, 2012 | Sheet 40 of 53

Power Button



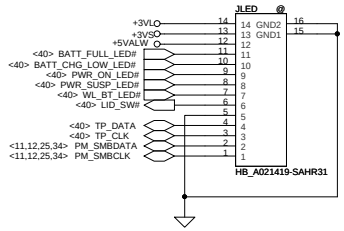
LPC Debug Port

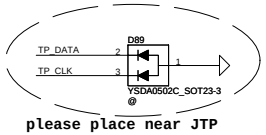
Place the PAD under DDR DIMM.



LED/LID/TP SMALL BOARD

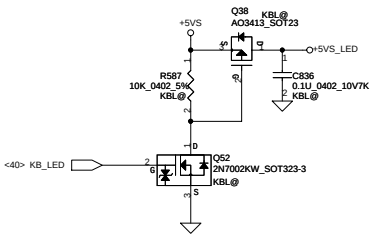
Swap pin assign to avoid DDR interference

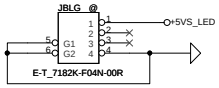




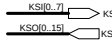
please place near JTP

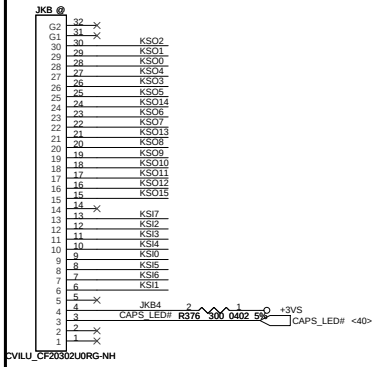
Keyboard LED

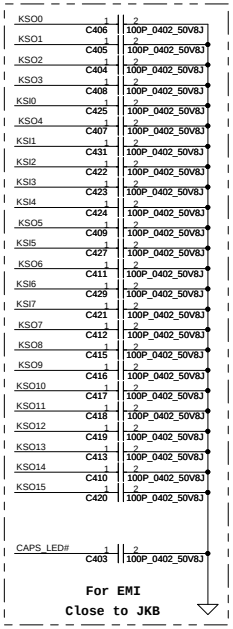




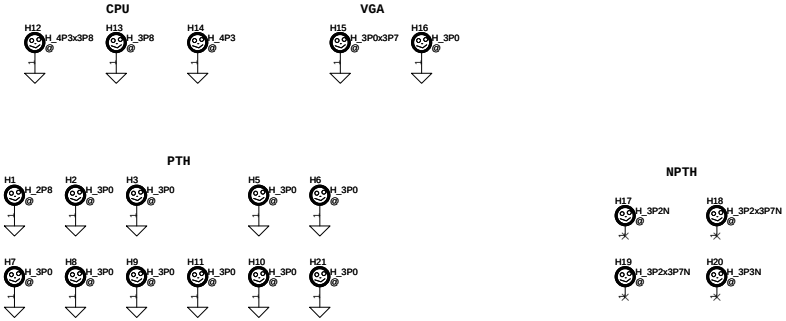
NEW KEYBOARD CONN.



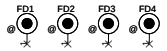




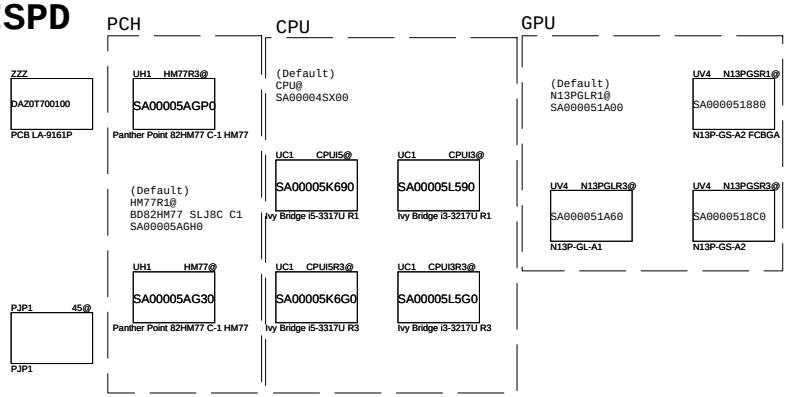
Screw Hole



PCB Fedical Mark PAD



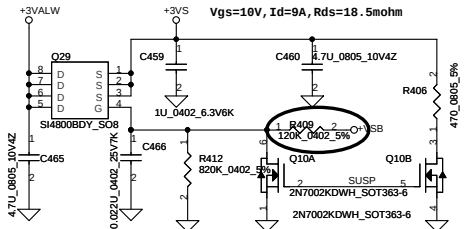
ISPD



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: TP/ISPD/KB/Screw

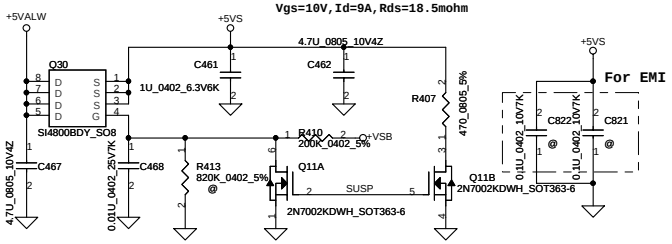
Size	Document Number VCUAA		Rev 1.0
Date: Tuesday, October 16, 2012	Sheet 41 of 53		

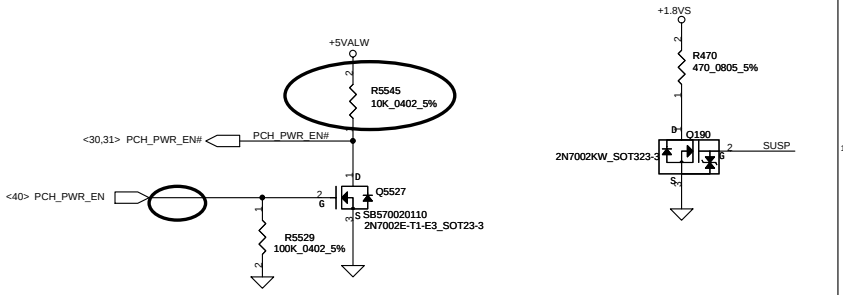
+3VALW TO +3VS



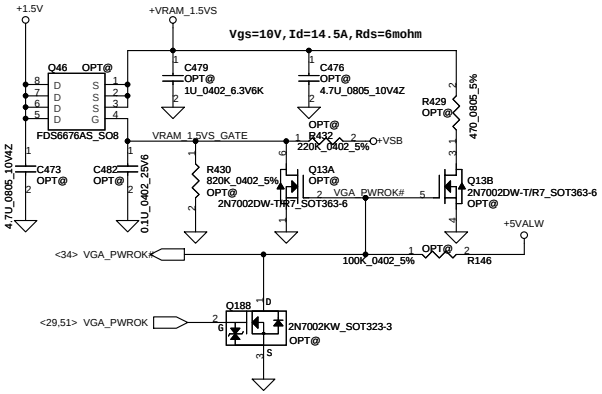
change R409 to 120k 5%

+5VALW TO +5VS

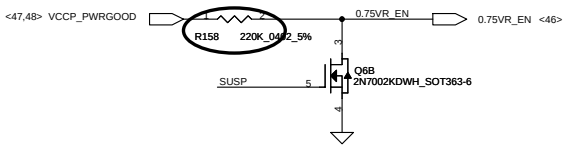


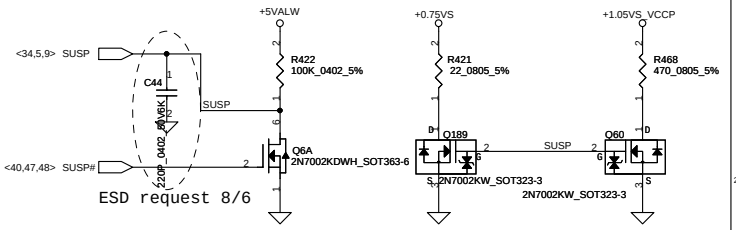


+1.5V to +VRAM_1.5VS



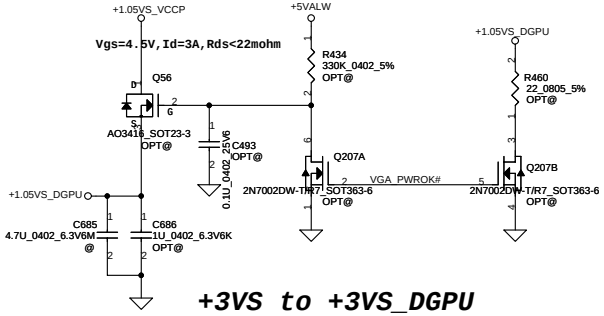
For S3 CPU Power Saving



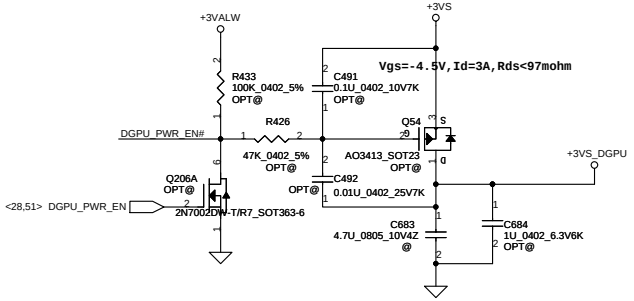


ESD request 8/6

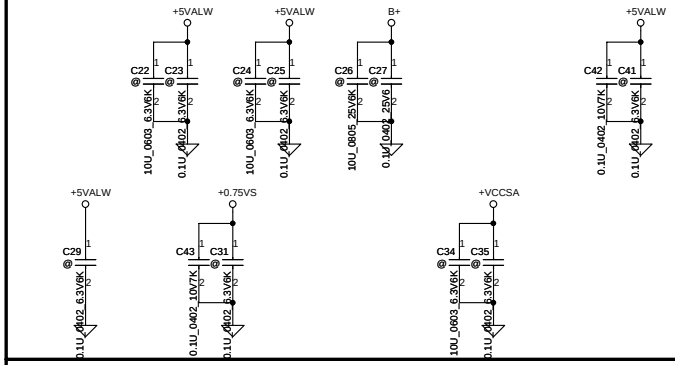
+1.05VS_VCCP to +1.05VS_DGPU

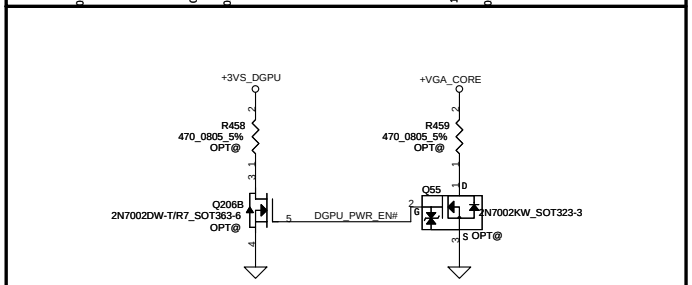


+3VS to +3VS_DGPU

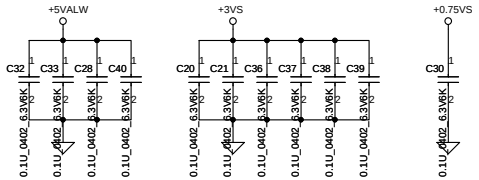


Reserve CAP to avoid Power Noise

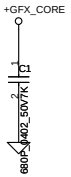




ESD Cap., please keep original location



EMI request



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	VCUAA	1.0

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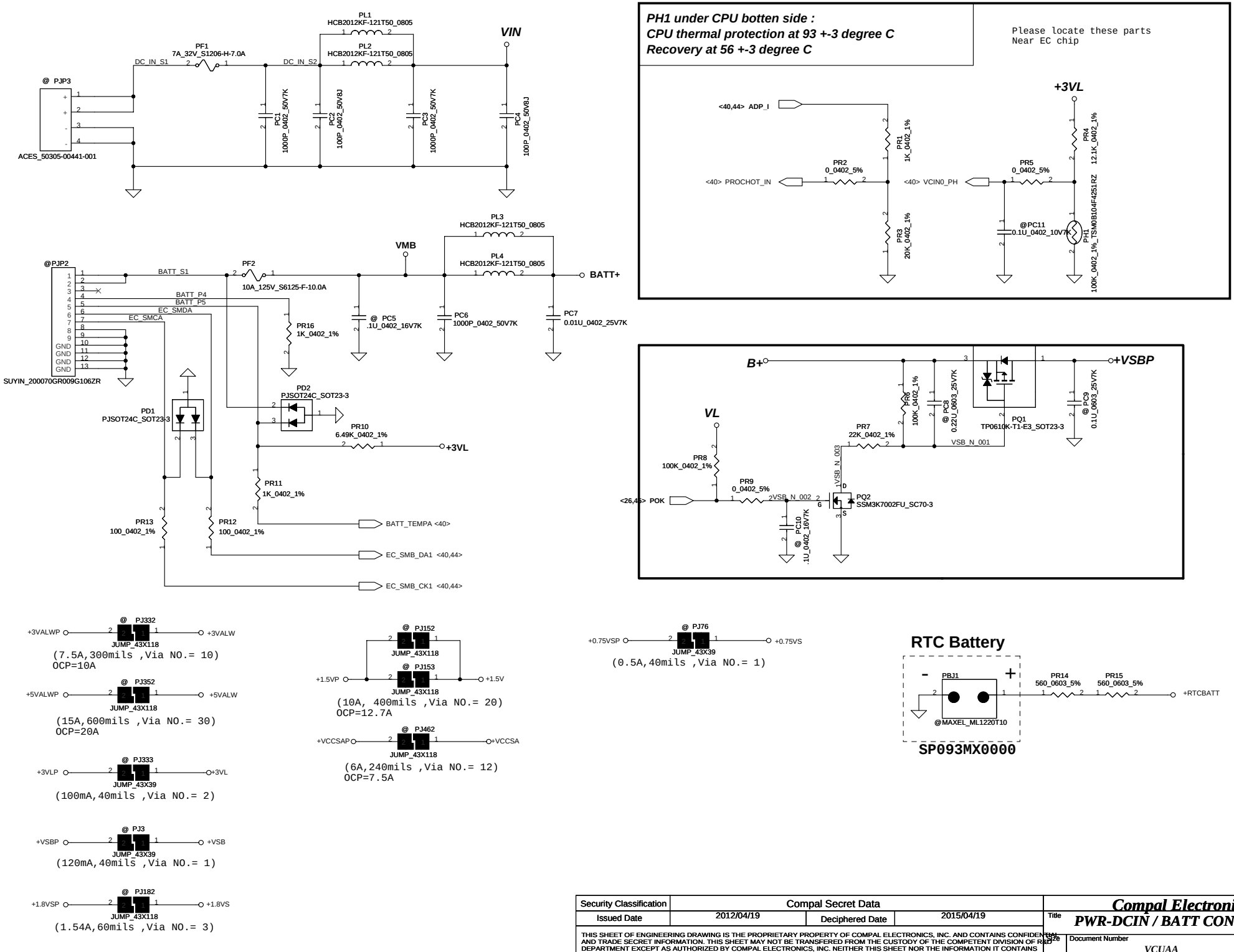


Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	PWR-DCIN / BATT CONN / OTP
Size	Document Number: VCUAA — Rev: 1.0
Date: Tuesday, October 16, 2012	Sheet 43 of 53

for reverse input protection

PQ209
SSM3K7002FU_SC70-3
PR225 1M_0402_5%
PR226 3M_0402_5%

VIN
AON6504_POWERDFN56-8-5
PQ203
P1
PR231 @ 0_0402_5%
PC230 2200P_0402_50V7K
PC231 0.1U_0402_25V6
<BOM Structure>
BQ24725_ACDRV_1

PQ205
DMG4406LSS_SO8
P2
B+
PR211 0.01_1206_1%
PL201 1UH_NRS4018T1R0NDGJ_3.2A_30%
PC211 10U_0805_25V6K
PC212 @ 10U_0805_25V6K
PC216 @ 0.1U_0402_25V6
PC213 @ 10U_0805_25V6K
PC214 10U_0805_25V6K
PC215 0.1U_0402_25V6

PC236 0.1U_0402_25V6
PC238 0.1U_0603_25V7K
PC235 0.1U_0402_25V6
PD230 BAS40CW_SOT323-3
PR228 10_1206_1%
PC237 0.047U_0402_25V7K
PR229 2.2_0603_5%
PD231 RB751V-40_SOD323-2
PC239 1U_0603_25V6K
PC205 1U_0603_25V6K

PR234 4.12K_0603_1%
PR235 4.12K_0603_1%

PU200
BQ24725RGRR_VQFN20_3P5X3P5
PAD VCC PHASE HIDRV BTST REGN
ACN LODRV
ACP GND
CMSRC SRP
ACDRV SRN
ACOK BATDRV
ACDET IOUT SDA SCL ILIM

PR236 10_0603_1%
PR237 6.8_0603_5%
PC242 0.1U_0603_16V7K

BQ24725_CMSRC
BQ24725_ACDRV
BQ24725_ACOK
BQ24725_BATDRV
BQ24725_ACP
BQ24725_ACN
BQ24725_VCC
BQ24725_LX
BQ24725_BST
BQ24725_REGN
DH_CHG
DL_CHG
CSOP1
CSON1

PQ207
DMG4406LSS_SO8
PC234 0.01U_0402_50V7K
PR232 @ 0_0402_5%
BQ24725_BATDRV
BQ24725_BATDRV_1
PR233 4.12K_0603_1%

PQ201
AON7408L
PQ202
AON7406L
PR206 4.7_1206_5%
PC206 680P_0603_50V8J

PL202 4.7UH_ETQP3W4R7WFN_5.5A_20%
PR227 0.01_1206_1%
BATT+
PC240 0.1U_0402_25V6
PC241 0.1U_0402_25V6
PC221 @ 10U_0805_25V6K
PC222 10U_0805_25V6K
PC223 10U_0805_25V6K
PC224 2200P_0402_50V7K
PC225 0.1U_0402_50V7K

+3VALW
@PR238 10K_0402_1%
+3VL
PR239 10K_0402_1%
<26,40> ACIN
PR240 10K_0402_1%
VIN
PR243 270K_0402_1%
PR244 154K_0402_1%
PC244 0.1U_0402_25V6
PR245 66.5K_0402_1%
PC245 100P_0402_50V8J
PR246 100_0402_5%
@PC246 0.1U_0402_10V7K
ADP_I <40,43>

BQ24725_ILIM
PR241 357K_0402_1%
PR242 100K_0402_1%
PC243 0.01U_0402_25V7K
EC_SMB_CK1 <40,43>
EC_SMB_DA1 <40,43>

VIN
PR247 309K_0402_1%
PR248 10K_0402_1%
ADP_V <40>
PR249 47K_0402_1%
@PC247 0.1U_0402_10V7K

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM 3.97A

Please locate the RC
Near EC chip
2011-02-22

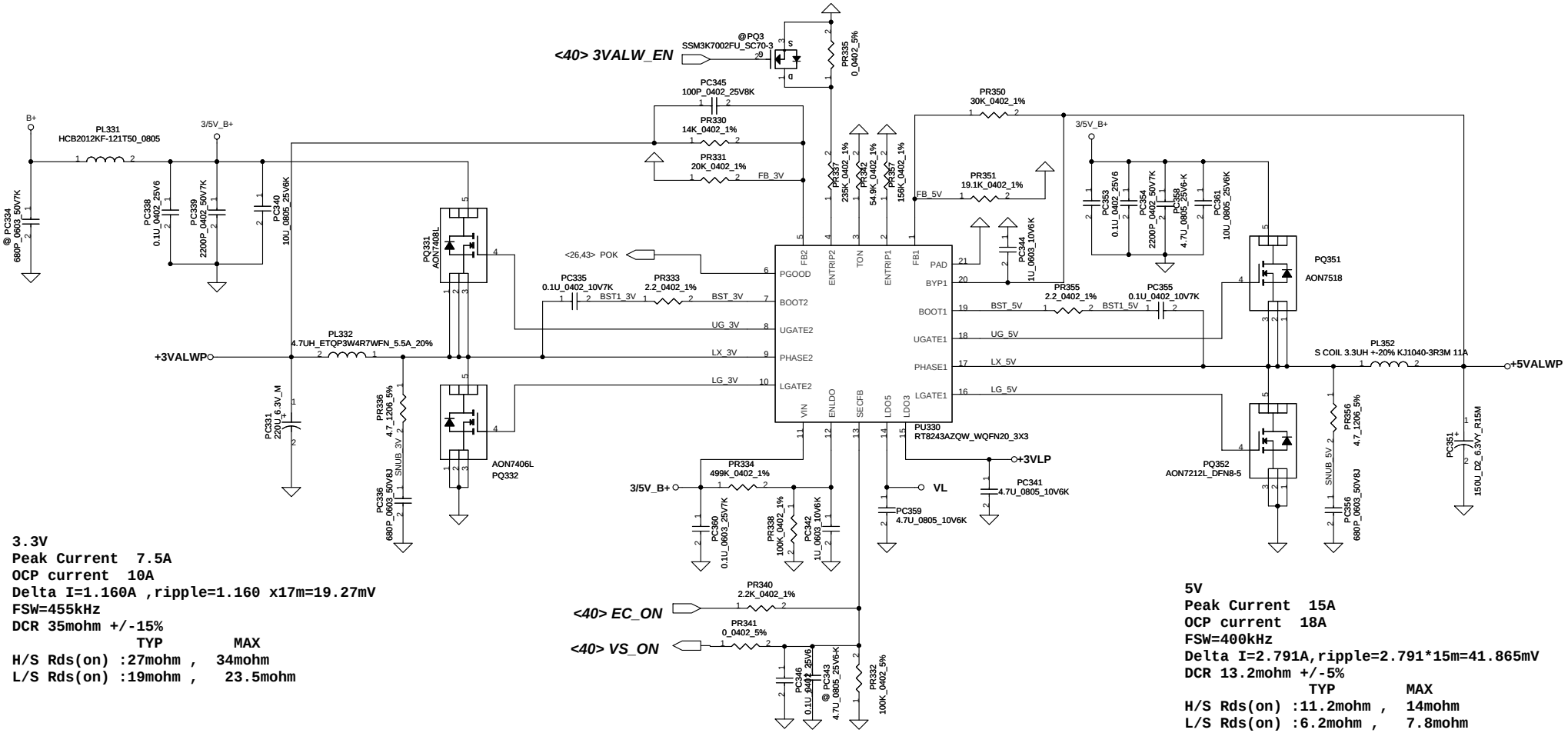
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size: | Document Number: VCUAA | Rev: 1.0

Date: Tuesday, October 16, 2012 | Sheet 44 of 53



3.3V
Peak Current 7.5A
OCP current 10A
Delta I=1.160A ,ripple=1.160 x17m=19.27mV
FSW=455kHz
DCR 35mohm +/-15%

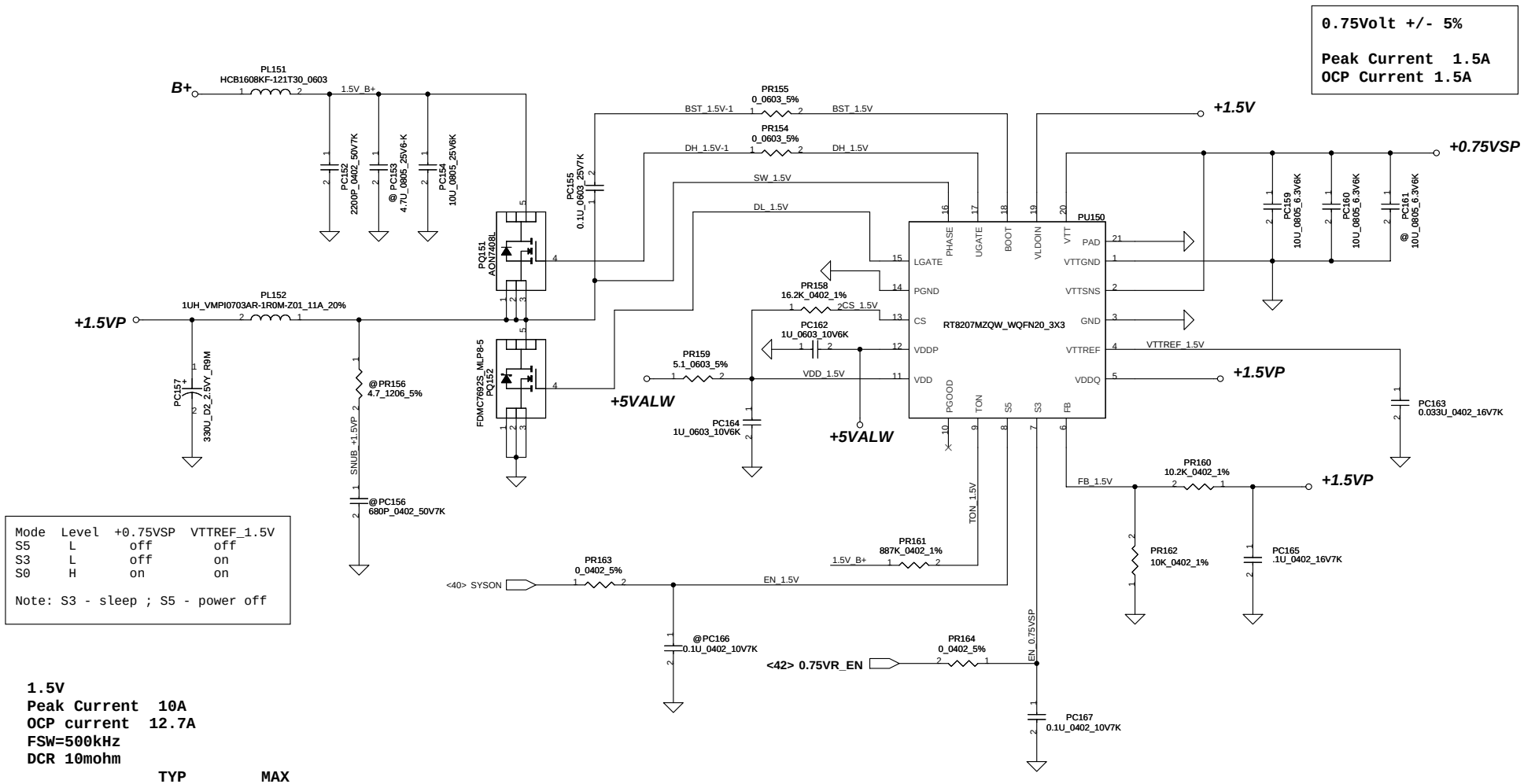
	TYP	MAX
H/S Rds(on) :	27mohm ,	34mohm
L/S Rds(on) :	19mohm ,	23.5mohm

5V
Peak Current 15A
OCP current 18A
FSW=400kHz
Delta I=2.791A,ripple=2.791*15m=41.865mV
DCR 13.2mohm +/-5%

	TYP	MAX
H/S Rds(on) :	11.2mohm ,	14mohm
L/S Rds(on) :	6.2mohm ,	7.8mohm

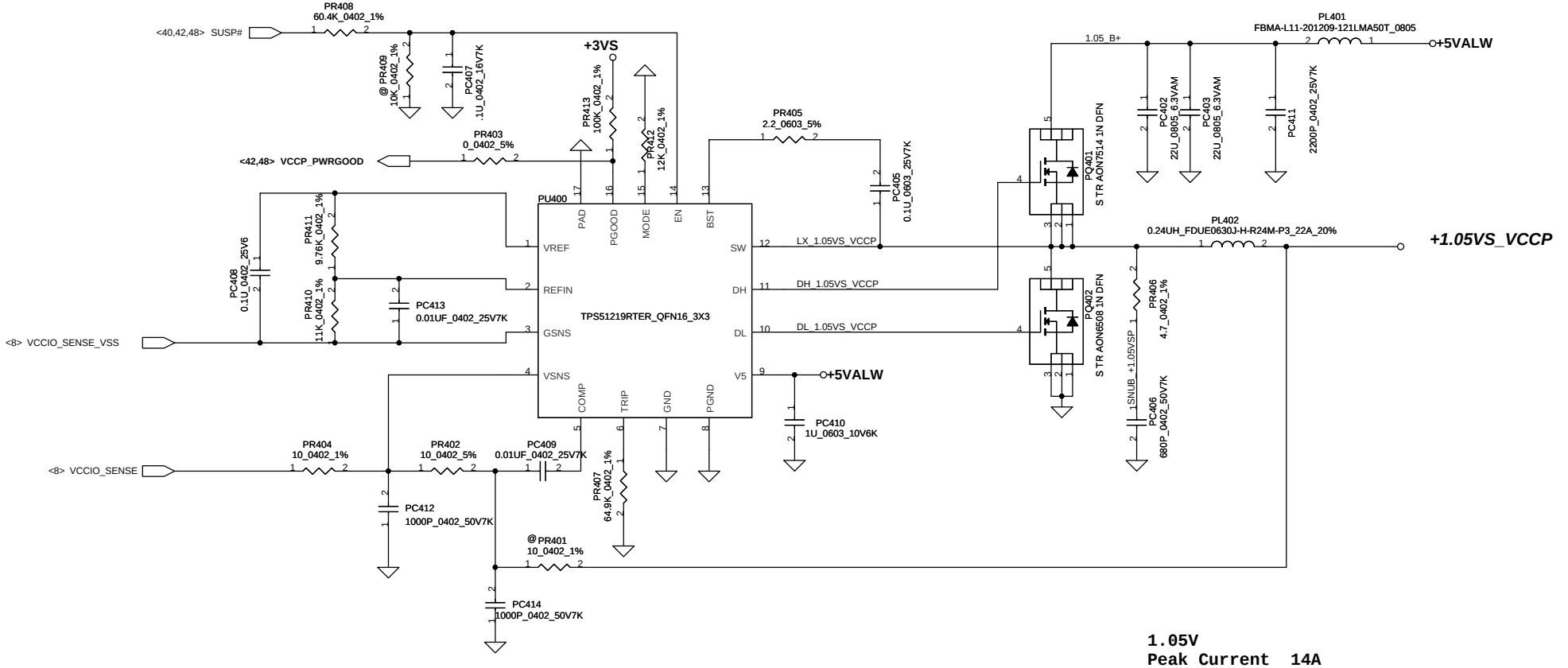
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	PWR-3.3VALWP/5VALWP
Size: Custom	Document Number: VCUAA
Rev	1.0
Date: Tuesday, October 16, 2012	Sheet 45 of 53



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	+1.5VP/+0.75VSP		
Size	Document Number		Rev
	VCUAA		1.0
Date: Tuesday, October 16, 2012	Sheet 46 of 53		



1.05V
Peak Current 14A
OCP current 15.08A
FSW=300kHz
Delta I=5.883A,Rippe=5.883x 4.5m=26.473Mv
DCR 3.7ohm +

	TYP	MAX
H/S Rds(on) :	5.6mohm ,	6.8mohm
L/S Rds(on) :	3.7mohm ,	5mohm

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***PWR-V1.05SP/16V***

Size: Custom | Document Number: VCUAA | Rev: 1.0

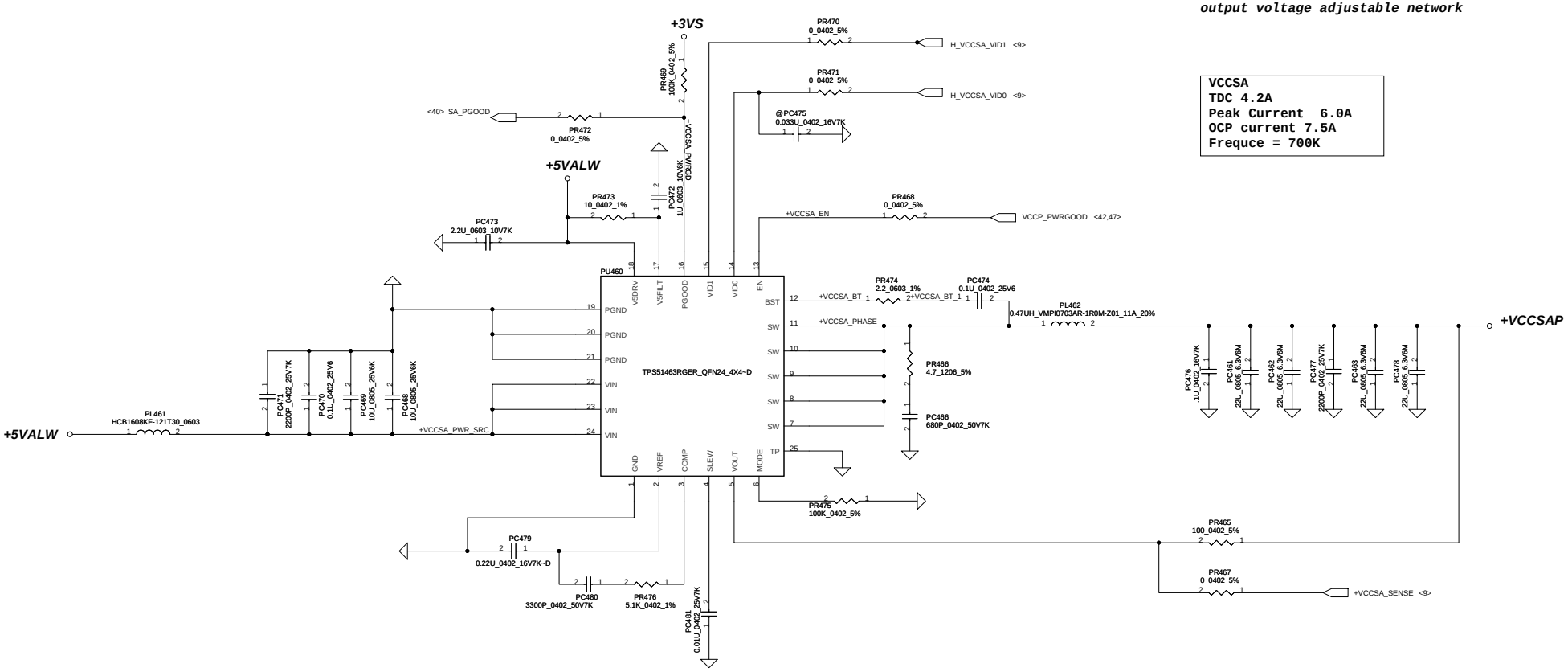
Date: Tuesday, October 16, 2012 | Sheet 47 of 53

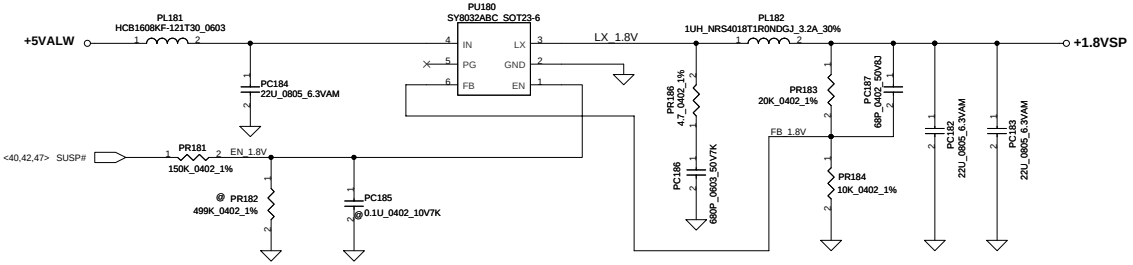
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.750V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCSA
TDC 4.2A
Peak Current 6.0A
OCP current 7.5A
Freque = 700K





VCCSA

Peak Current 1.54A
OCP current 1.078A

DELL CONFIDENTIAL/PROPRIETARY

	123	
Title	PWR-VCCSAP/1.8VSP	
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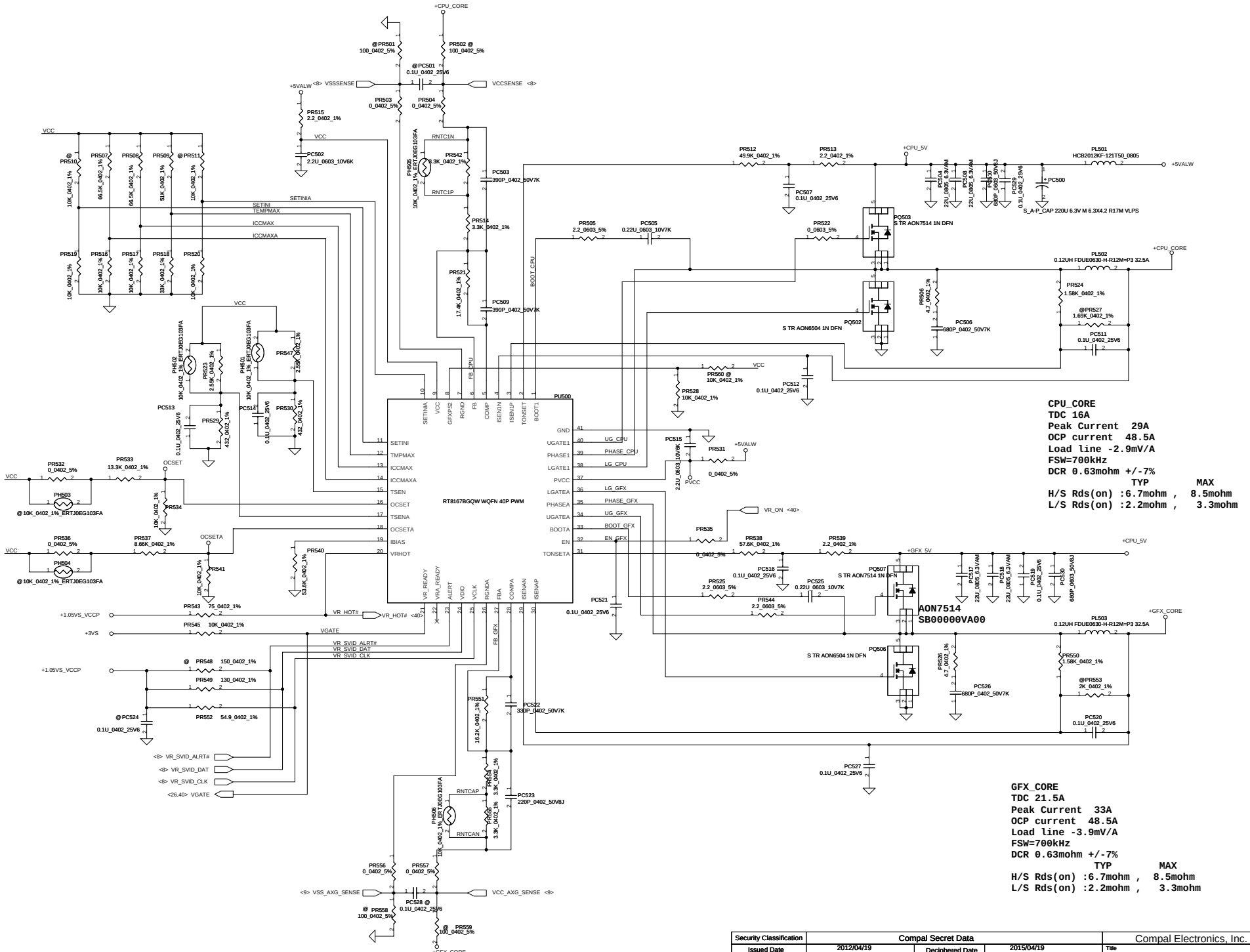

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Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PWR- CPU GFX CORE
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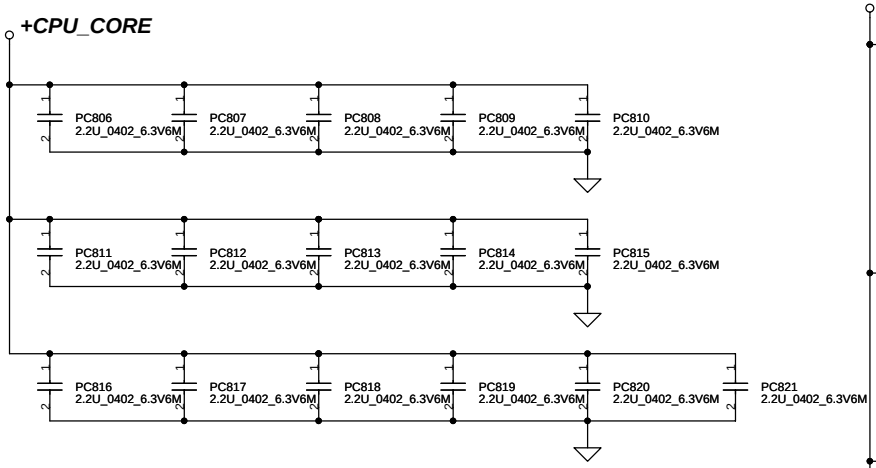
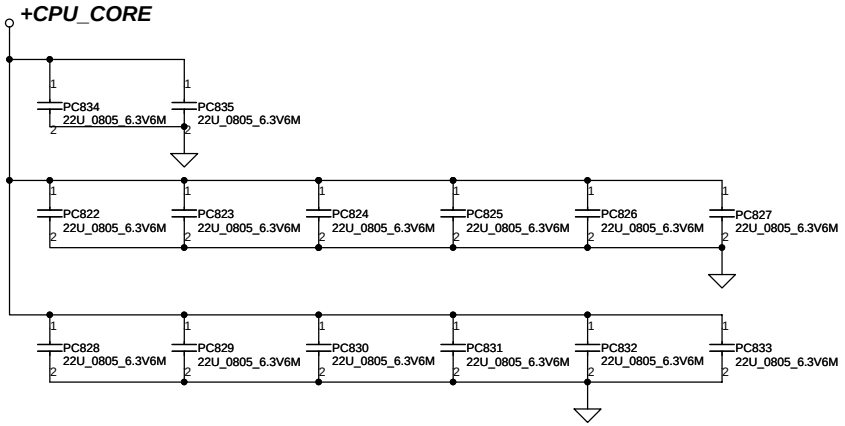
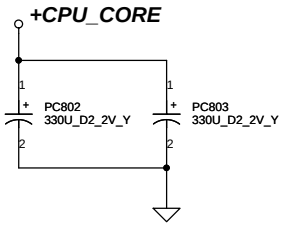
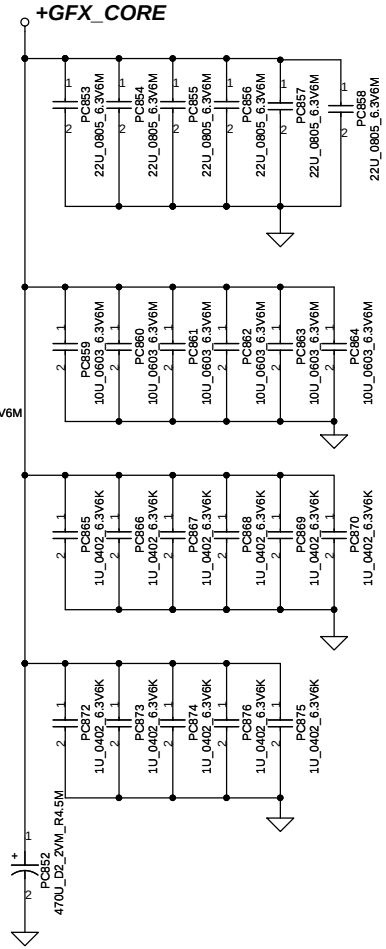
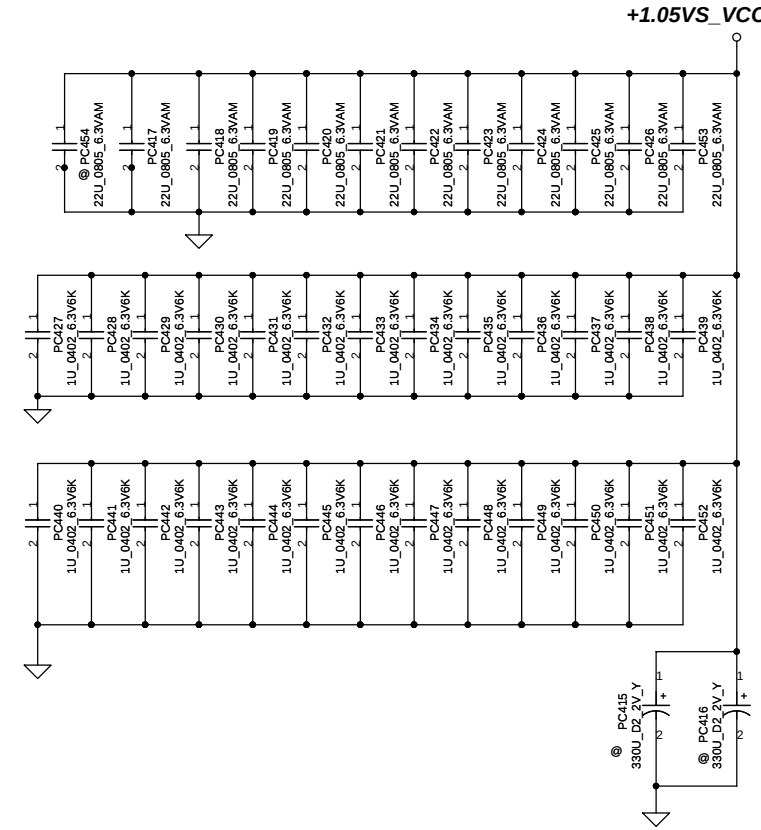
			Date: Tuesday, October 16, 2012 / Sheet 49 of 53











Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF
CPU	2	14		16	
GFX_CORE	1	6	6		11
1.05V_VCCP	2		11		26

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Title: PWR - PROCESSOR DECOUPLING

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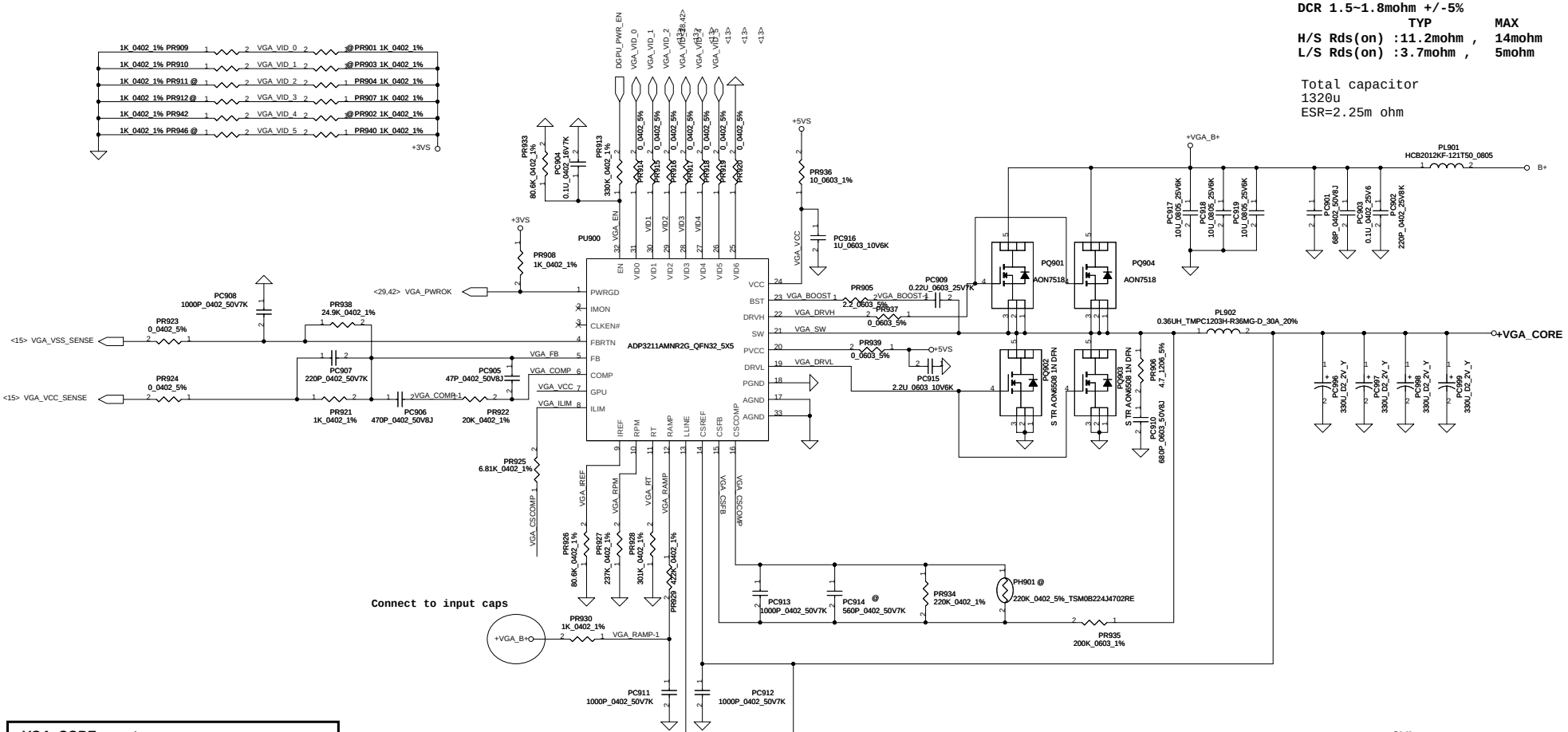
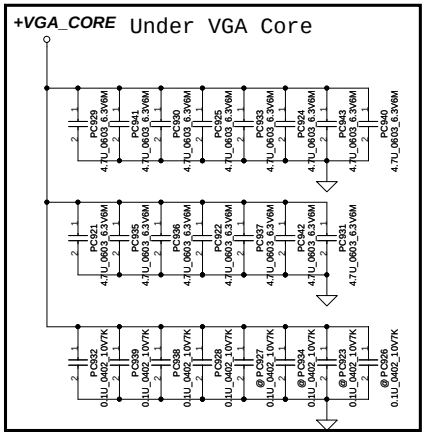
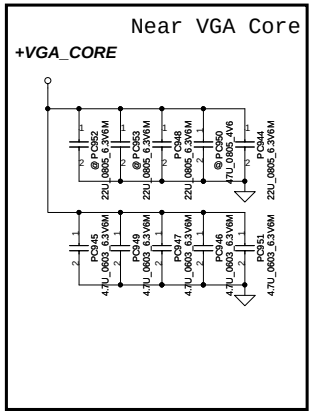
VGA_Core
TDC 35A
Peak Current 42A
OCP current 65A
Load line -
FSW=300kHz
DCR 1.5~1.8mohm +/-5%

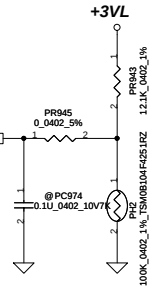
	TYP	MAX
H/S Rds(on) :	11.2mohm ,	14mohm
L/S Rds(on) :	3.7mohm ,	5mohm

Total capacitor
1320u
ESR=2.25m ohm









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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW command (Follow QFKAA)	45	change PR330 13K to 14K	2012/5/17	DVT
2	HW command (Follow QFKAA)	45	change PR351 20K to 19.1K	2012/5/17	DVT
4	fine tune 1.5V ocp =12.6A	46	change PR158 13.3K to 16.2K	2012/5/17	DVT
5	fine the 1.05V vout volatge=1.059V	47	change PR411 10.5K to 9.76K	2012/5/17	DVT
6	fine tune the CPU load line =2.7mV	49	change PR521 14.3K to 17.4K	2012/5/17	DVT
7	fine tune the GFX load line =3.7mV	49	change PR551 10.5K to 16.2K	2012/5/21	DVT
8	fine tune the GFX load line =3.7mV	49	change PC522 560P to 330P	2012/5/21	DVT
9	fine tune the GFX OCP setting	49	change PR537 13.3K to 8.66K	2012/5/21	DVT
10	purchaser command for cost down plane	48	change PU460 SY8037D to TPS51463	2012/5/22	DVT
11	for 1.05V high frequeence change to remote sense	47	add PR402 reserve PR401	2012/5/24	DVT
12	for 1.05V high frequeence	47	change PR412 100k to 12K	2012/5/24	DVT
13	change the same solution for 2nd sourcd	44	change PQ203 TPCA8057 to AON6504	2012/5/24	DVT
14	change the same solution for 2nd sourcd	44	change PR227 with the same PR211	2012/5/25	DVT
15	change the same solution for 2nd sourcd	46	change PC157 with the same PC996	2012/5/25	DVT
16	fine tune 1.05V vout volatge=1.059V	47	change PR410 12K to 11K	2012/5/25	DVT
17	fine tune the CPU DCR sense	49	change PR538 49.9K to 57.6K	2012/5/25	DVT
18	fine tune the CPU DCR sense	49	change PR550 1.13K to 1.58K	2012/5/25	DVT
19	fine tune the 5V OCP=18A	45	change PR357 120K to 133K	2012/5/25	DVT
20	fine tune 3.3V OCP =10A	45	change PR337 120K to 200K	2012/5/25	DVT
21	for 1.05V high frequeence	47	change PL402 0.47u to 0.24u	2012/5/25	DVT
22	for 1.05V high frequeence	47	Reserve the PC415 and PC416	2012/5/25	DVT
23	change the 3v/5v IC version	45	change the PU330 RT8243B to RT8243A	2012/5/25	DVT
24	change 1.5V chokethe same part number with PL462	46	change the PL152 SH00000GJ00 to SH00000KS00	2012/5/25	DVT
25	change 1.05V high frequeence OCP=16.5A	47	change the PR407 75K to 64.9K	2012/5/25	DVT
26	change charger current =3.46A	48	change the PR241 150 Kto 357K		
27	**change the PF2 for design change**	43	change the PF2 8A to 10A		

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HW PIR (Product Improve Record)

VCUAA LA-9161P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

Item	Page	Date	Request	Solution
1)	24	2012/7/23A	Change RTCBATT power rail from GCLK to original design	DH1 mount always
2)	24	2012/7/23A	remove BIOS socket	UH3 mount always
3)	41	2012/7/23A	remove debug SW	Change SW2 to @
4)	38	2012/7/26A	EMI request	CA71,CA72,CA75,CA76 mount SE025102K80/1000pF
5)	41	2012/8/3A	Update JBLG footprint	Change JBLG footprint to E-T_7182K_F04N-00R_4P
6)	41	2012/8/3A	Update H20	Change H20 from 3P8 to 3P3 size
7)	05	2012/8/6C	remove JTAG for ESD request	remove T5, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17
8)	42	2012/8/6D	ESD request	mount C20,C21,C28,C30,C32,C33,C36,C37,C38,C39,C40; add C44 on SUSP
9)		2012/8/6D	Change footprint of 0ohm to Short_pad	Change location: LL2, R1, R16, R17, R388, RA17, RA18, RA28, RB1,RB32, RB34, RC119, RC183, RC73, RC88, RC92, RC94, RC95, RH128, RH208, RH213, RH214, RH221, RH242, RH244, RH246, RH247, RH249, RH25, RH286, RH311, RH312, RH314, RL433, RV182, RV80, RV81
10)	41	2012/8/6D	Change PCB PN	Change to DAZ0T700100
11)	34	2012/8/6D	EMI request	Change CM18 from 47pF to 680pF
12)	42	2012/8/6D	EMI request	Add C1(680pF) on +GFX_CORE, place close to CPU

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