

ZZZ1
PCB
DA2@

ZZZ2
LA-4821P
MB
DA2@

ZZZ3
LS-4821P
FUNCTION_B
DA2@

ZZZ4
LS-4822P
FP_B
DA2@

ZZZ5
MDC Cable
45@

02/24 Change LA-4821P from mount to DA2@

Compal Confidential

KFT00 Schematics Document

Intel Penryn Processor with SiSM672FX + DDRII + SiS968 + SiS307ELV

2009-03-10

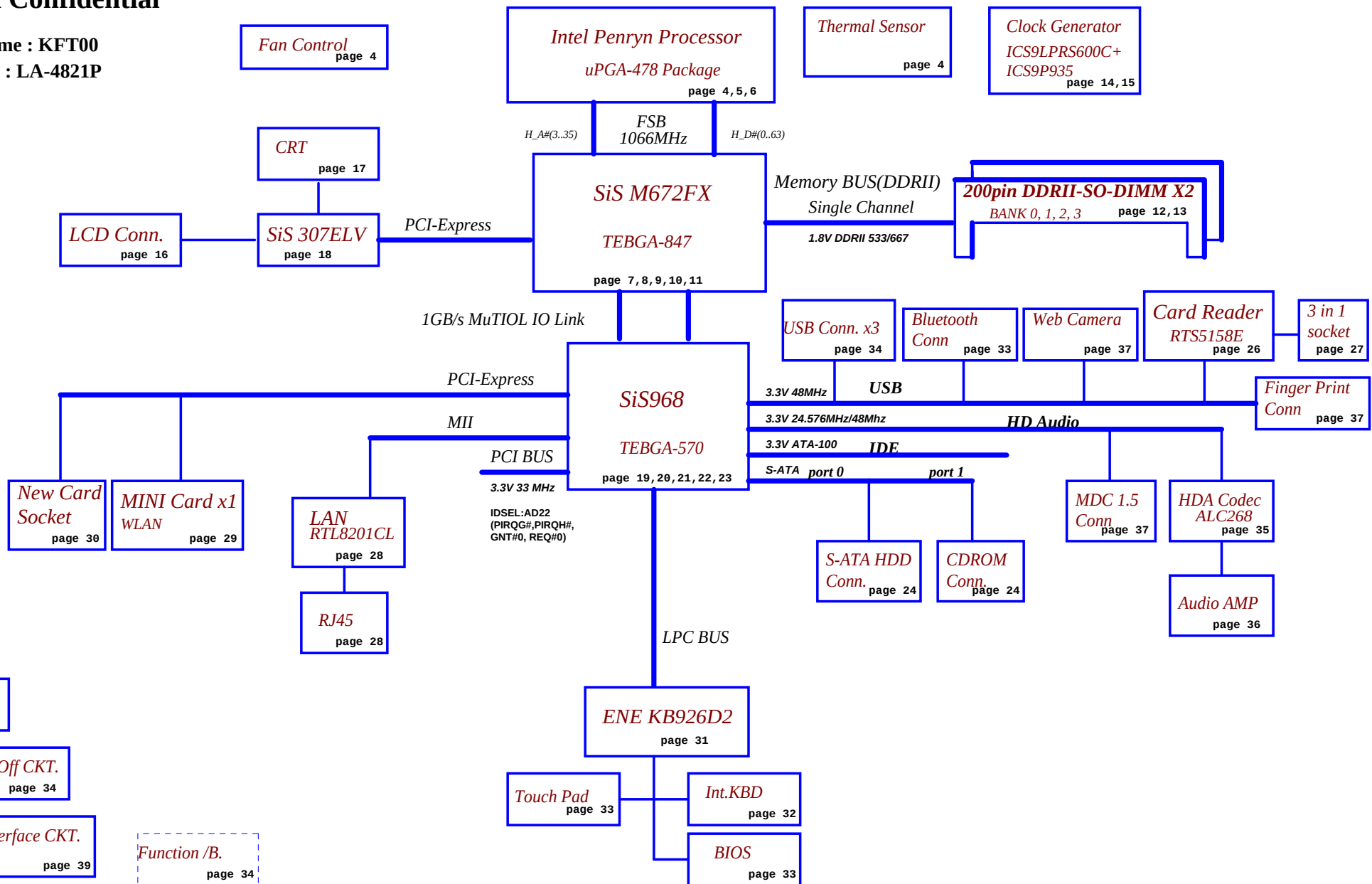
REV:1.0

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Model Name : KFT00

File Name : LA-4821P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID1 GPIO5	PROJECT_ID0 GPIO0
KFT00	0	0
KSW01	1	0
KSW91	1	1

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	SMC EMC1402-1	

EC SM Bus2 address

M672 SM Bus address

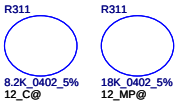
Device	Address
Clock Generator	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

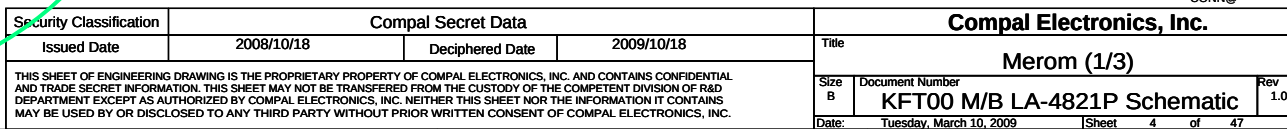
Ra~ R312

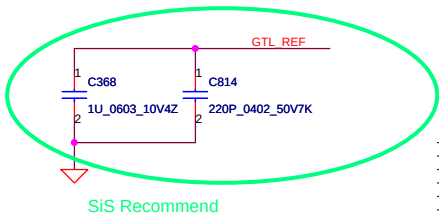
Rb~ R311



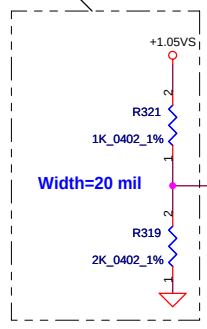
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	Rb BOM Structure
0	0	0 V	0 V	0 V	12_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	12_C@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	12_MP@

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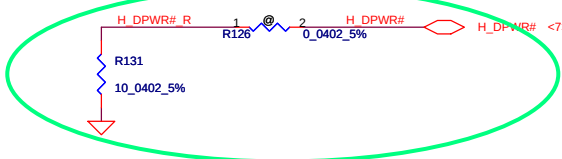
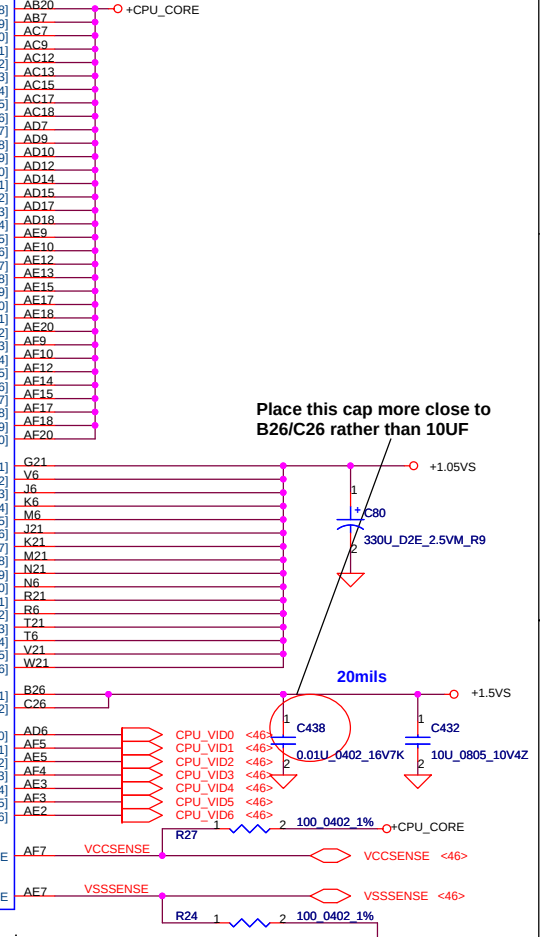
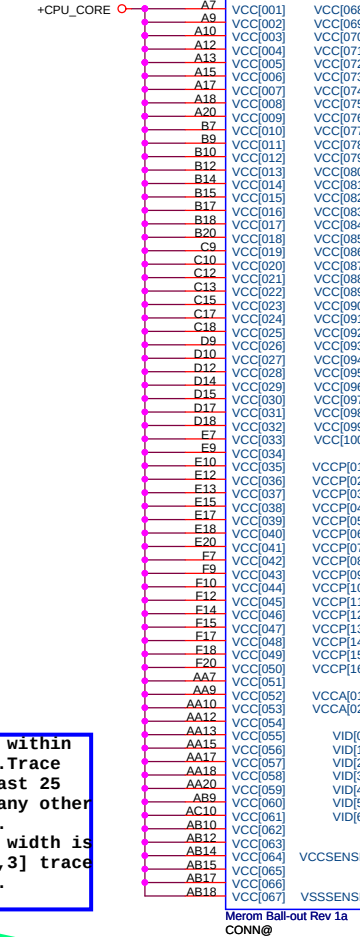
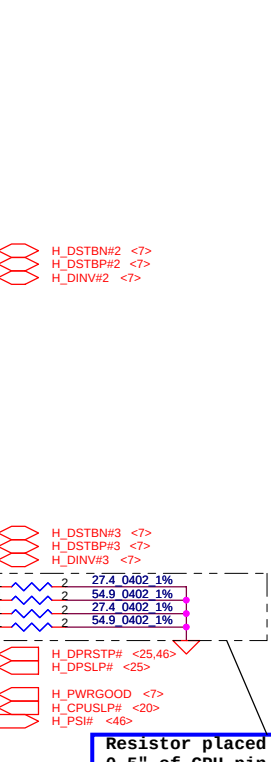
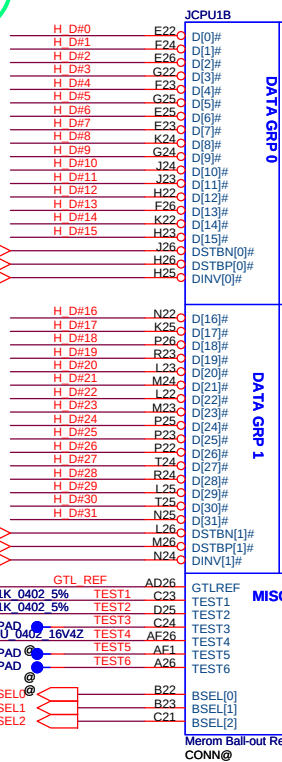
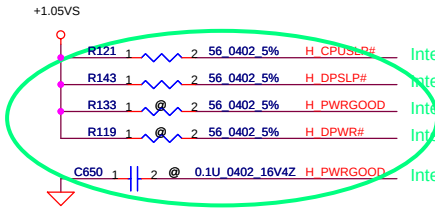


Close to CPU pin AD26 within 500mils.



Layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0



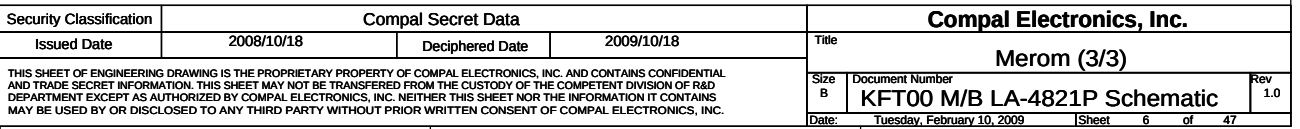
Length match within 25 mils. The trace width/space/other is 20/7/25.

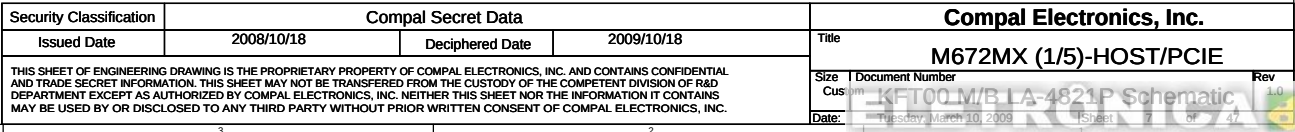
Close to CPU pin within 500mils.

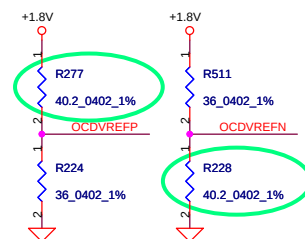
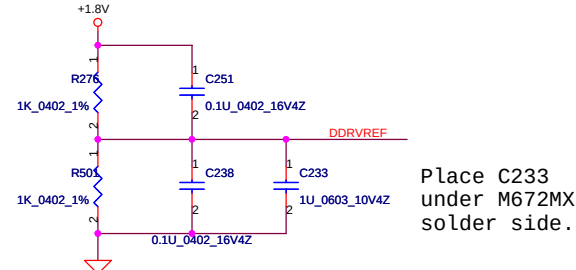
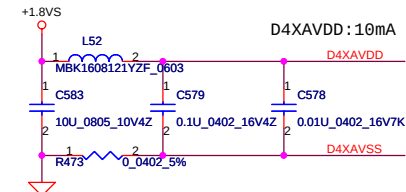
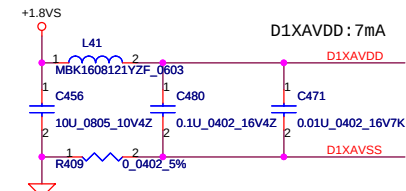
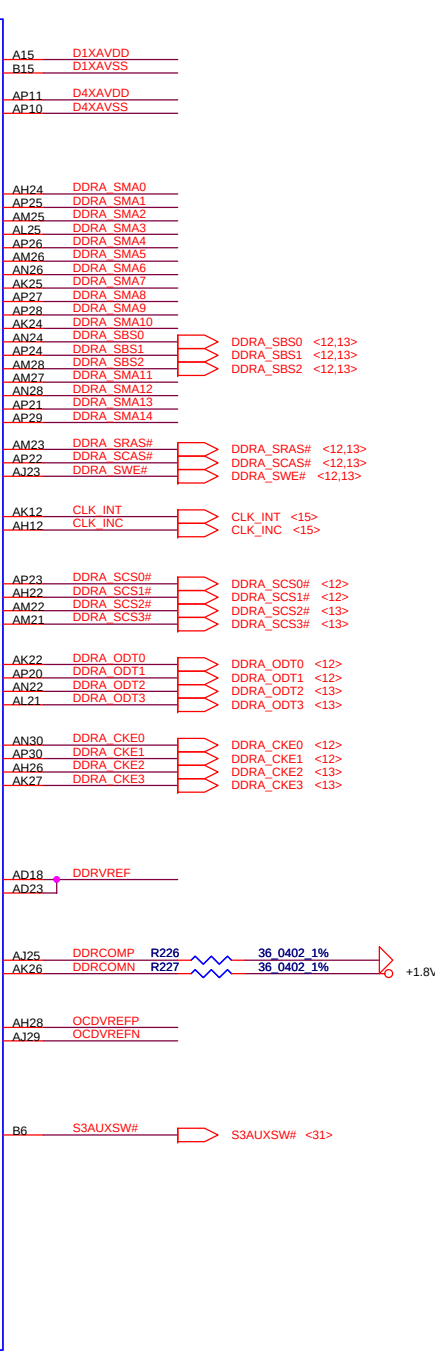
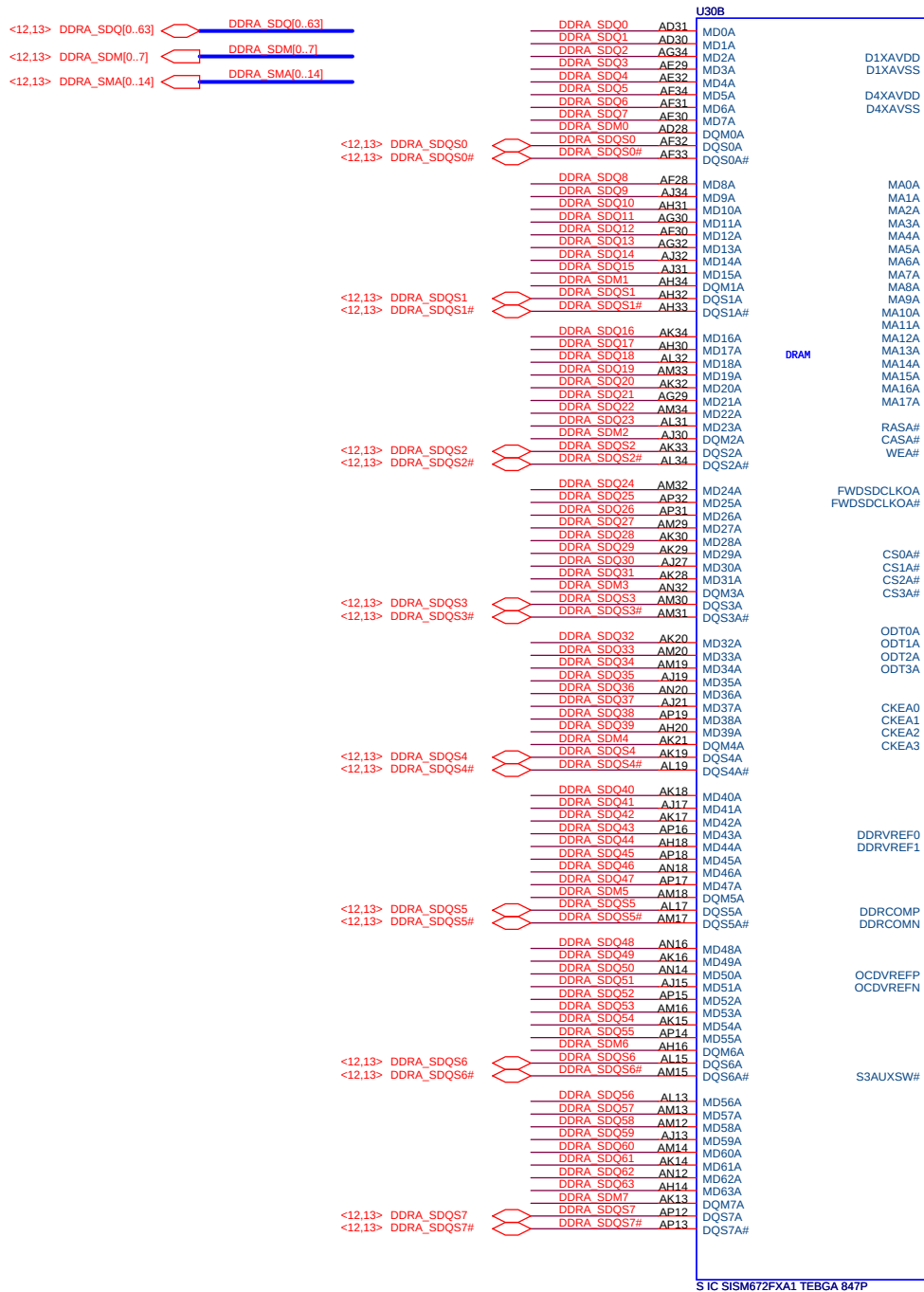
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

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Merom (2/3)			
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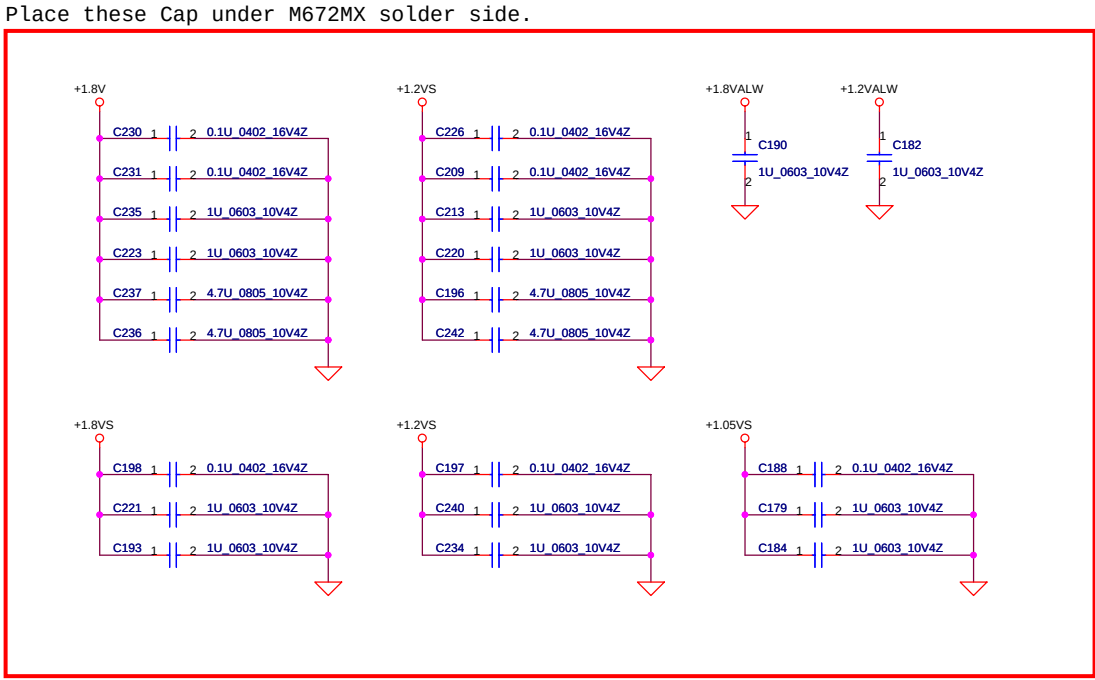




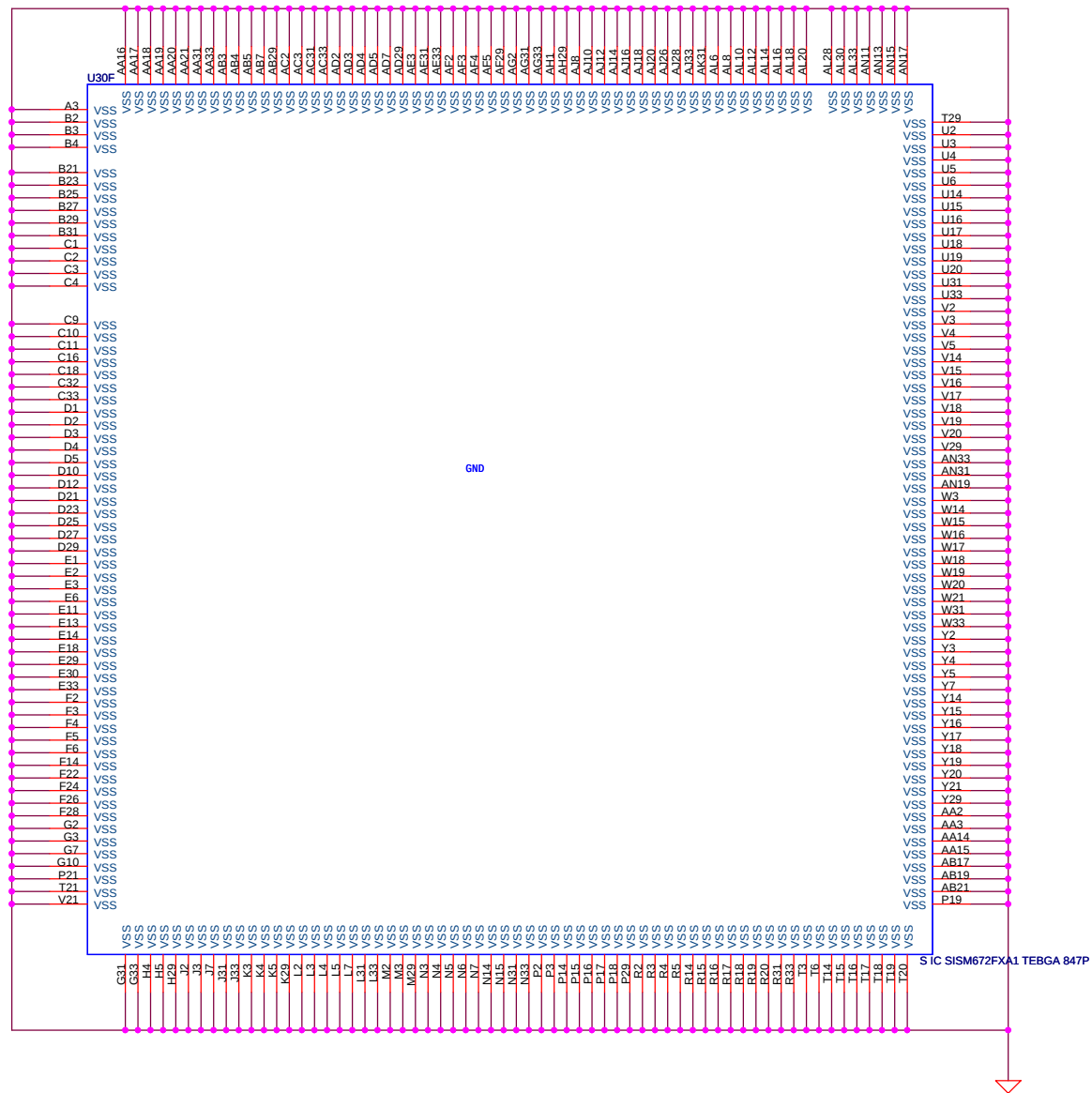


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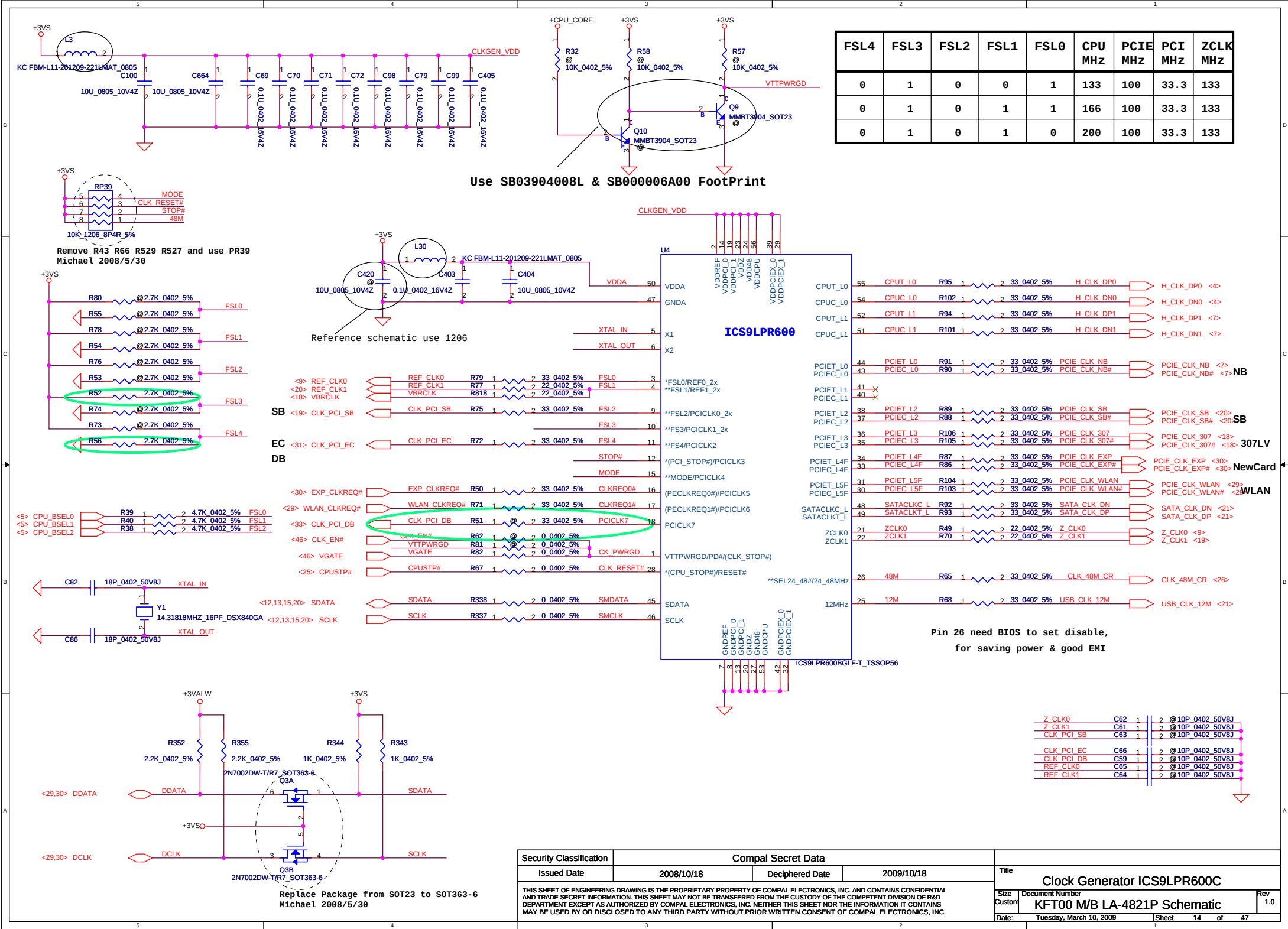




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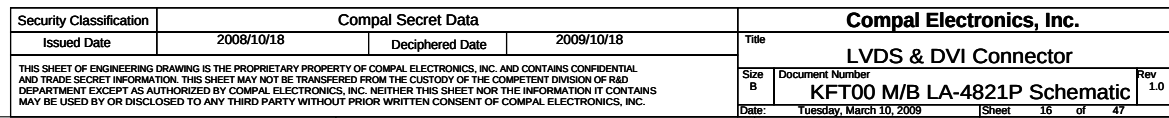
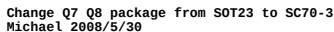
FSL4	FSL3	FSL2	FSL1	FSL0	CPU MHz	PCIE MHz	PCI MHz	ZCLK MHz
0	1	0	0	1	133	100	33.3	133
0	1	0	1	1	166	100	33.3	133
0	1	0	1	0	200	100	33.3	133

55	CPUT_L0	R95	1	2	33	0402	5%	H CLK DP0	H_CLK_DP0 <4>
54	CPUC_L0	R102	1	2	33	0402	5%	H CLK DN0	H_CLK_DN0 <4>
52	CPUT_L1	R94	1	2	33	0402	5%	H CLK DP1	H_CLK_DP1 <7>
51	CPUC_L1	R101	1	2	33	0402	5%	H CLK DN1	H_CLK_DN1 <7>
44	PCIE_T_L0	R91	1	2	33	0402	5%	PCIE_CLK_NB	PCIE_CLK_NB <7>
43	PCIE_C_L0	R90	1	2	33	0402	5%	PCIE_CLK_NB#	PCIE_CLK_NB# <7>
41	PCIE_T_L1								
40	PCIE_C_L1								
38	PCIE_T_L2	R89	1	2	33	0402	5%	PCIE_CLK_SB	PCIE_CLK_SB <20>
37	PCIE_C_L2	R88	1	2	33	0402	5%	PCIE_CLK_SB#	PCIE_CLK_SB# <20>
36	PCIE_T_L3	R106	1	2	33	0402	5%	PCIE_CLK_307	PCIE_CLK_307 <18>
35	PCIE_C_L3	R105	1	2	33	0402	5%	PCIE_CLK_307#	PCIE_CLK_307# <18>
34	PCIE_T_L4F	R87	1	2	33	0402	5%	PCIE_CLK_EXP	PCIE_CLK_EXP <30>
33	PCIE_C_L4F	R86	1	2	33	0402	5%	PCIE_CLK_EXP#	PCIE_CLK_EXP# <30>
31	PCIE_T_L5F	R104	1	2	33	0402	5%	PCIE_CLK_WLAN	PCIE_CLK_WLAN <29>
30	PCIE_C_L5F	R103	1	2	33	0402	5%	PCIE_CLK_WLAN#	PCIE_CLK_WLAN# <29>
48	SATACLKC_L	R92	1	2	33	0402	5%	SATA_CLK_DN	SATA_CLK_DN <21>
49	SATACLKT_L	R93	1	2	33	0402	5%	SATA_CLK_DP	SATA_CLK_DP <21>
21	ZCLK0	R49	1	2	22	0402	5%	Z_CLK0	Z_CLK0 <9>
22	ZCLK1	R70	1	2	22	0402	5%	Z_CLK1	Z_CLK1 <19>
26	48M	R65	1	2	33	0402	5%	CLK_48M_CR	CLK_48M_CR <26>
25	12M	R68	1	2	33	0402	5%	USB_CLK_12M	USB_CLK_12M <21>

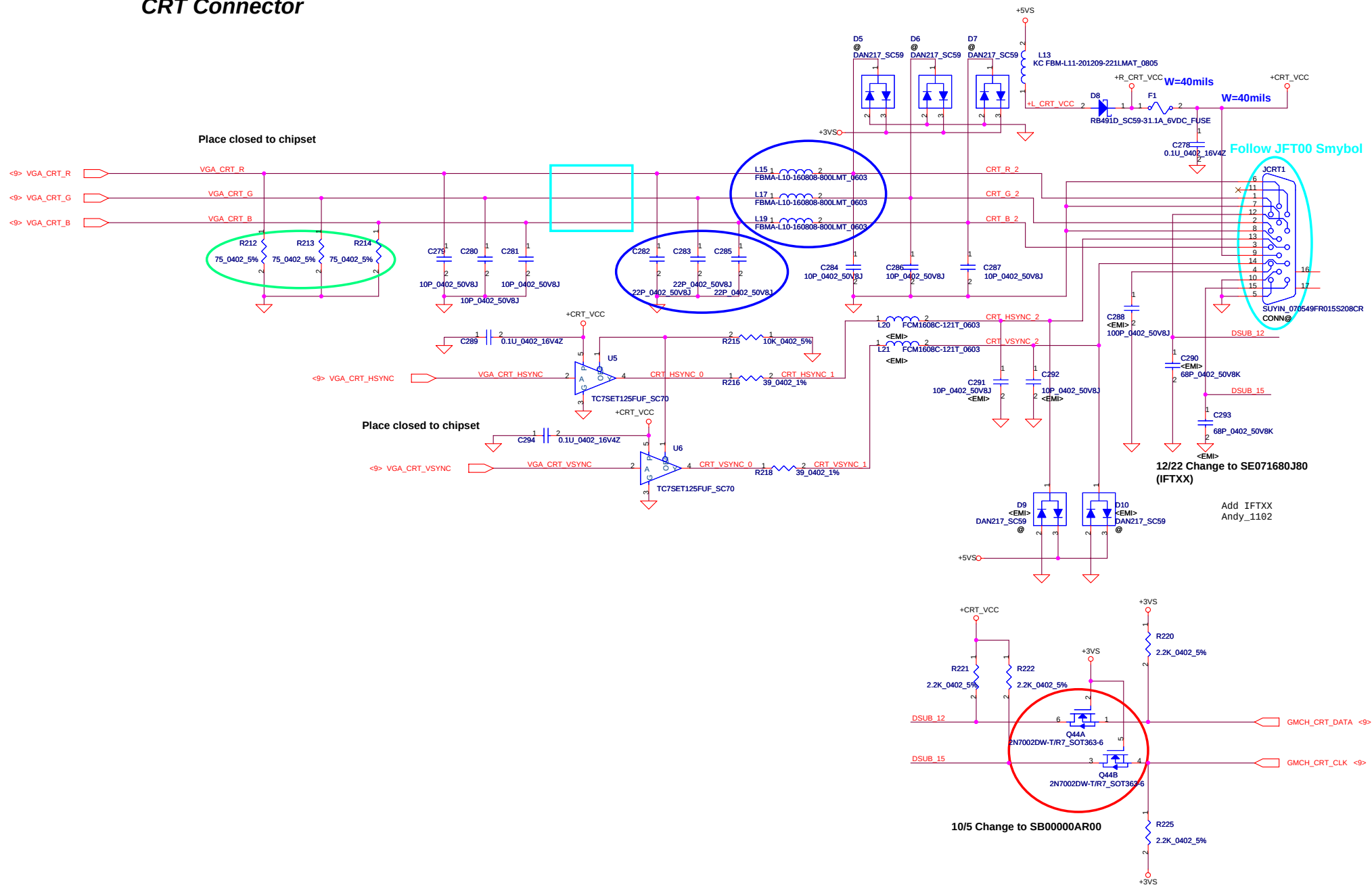
Pin 26 need BIOS to set disable,
for saving power & good EMI

Z_CLK0	C62	1	2	@10P	0402	50V8J
Z_CLK1	C61	1	2	@10P	0402	50V8J
CLK_PCI_SB	C63	1	2	@10P	0402	50V8J
CLK_PCI_EC	C66	1	2	@10P	0402	50V8J
CLK_PCI_DB	C59	1	2	@10P	0402	50V8J
REF_CLK0	C65	1	2	@10P	0402	50V8J
REF_CLK1	C64	1	2	@10P	0402	50V8J

A

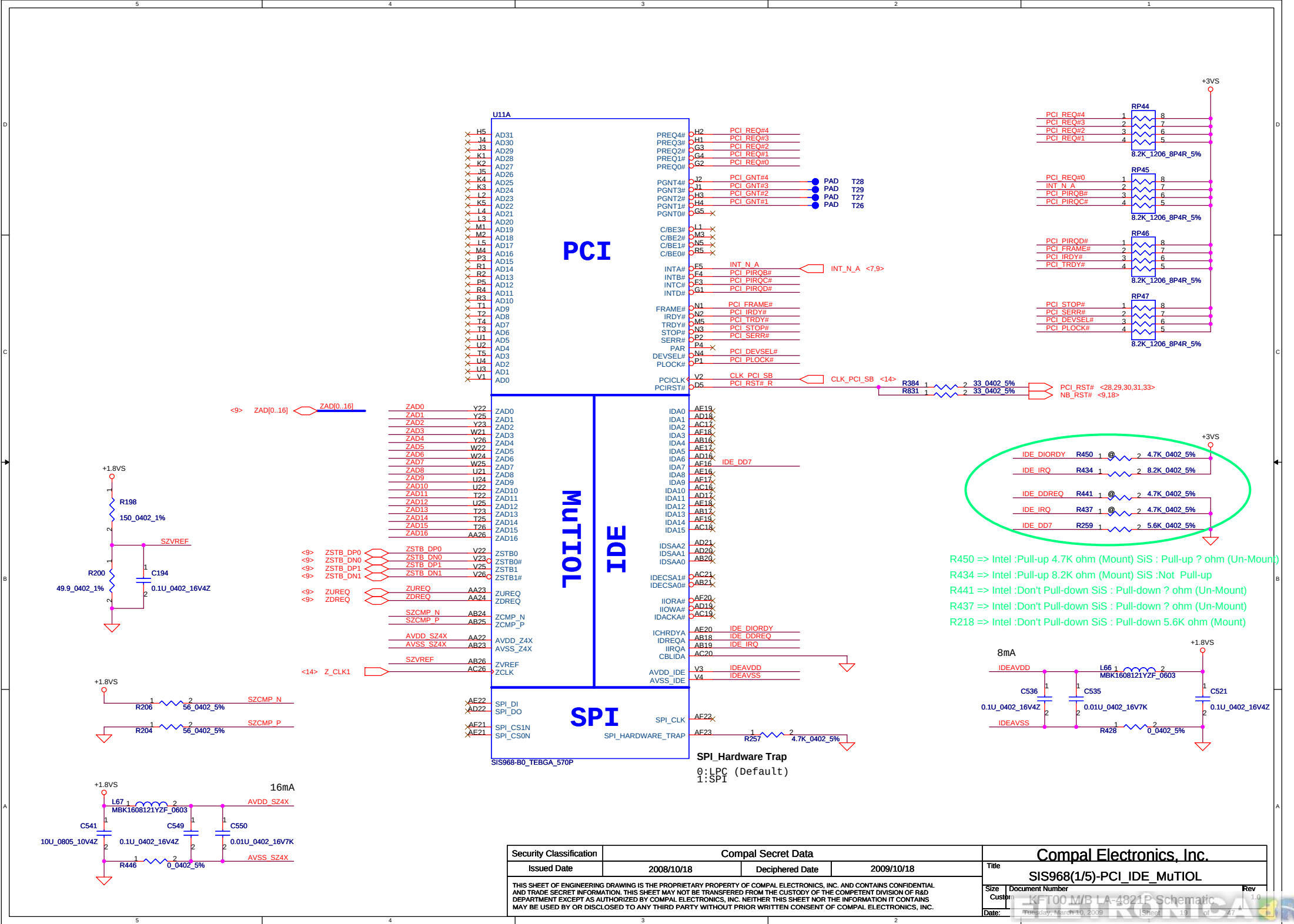


CRT Connector

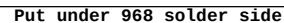
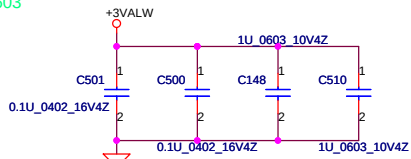


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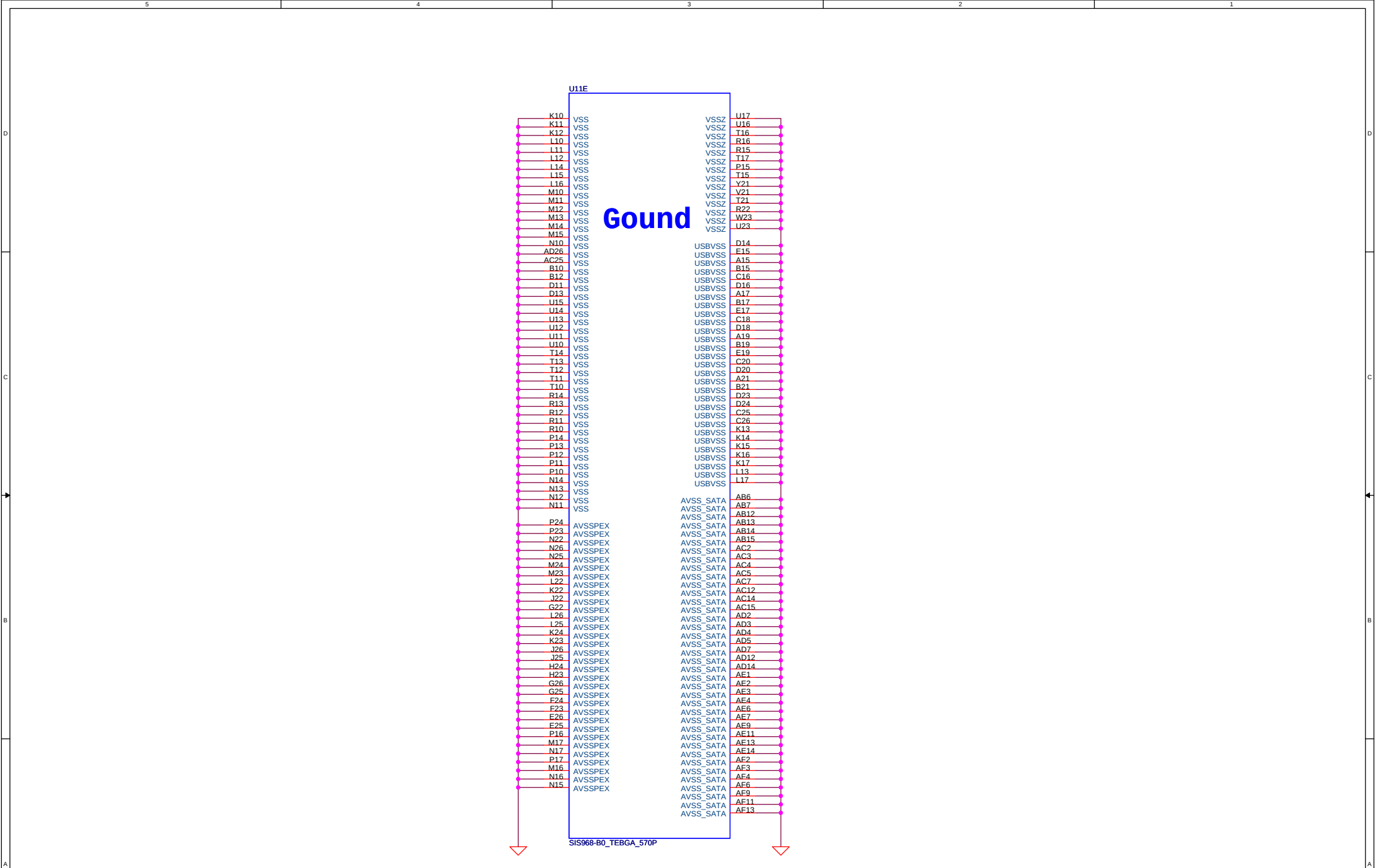




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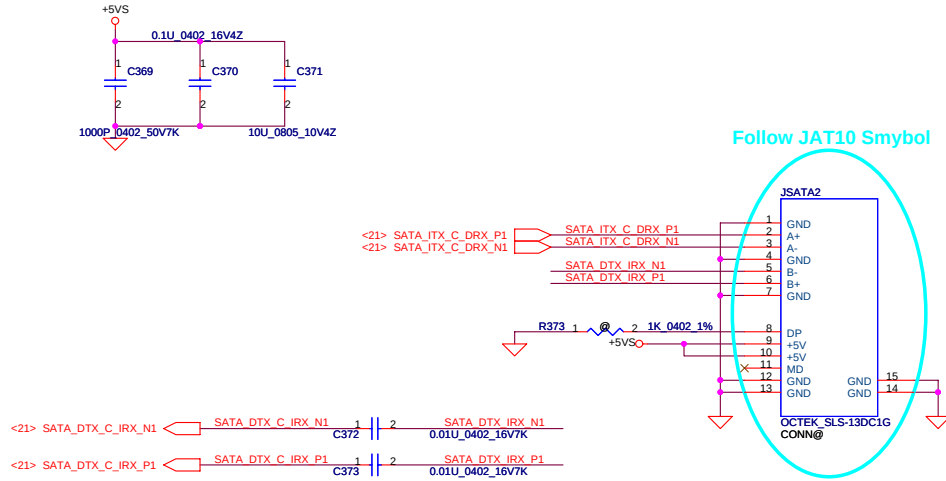


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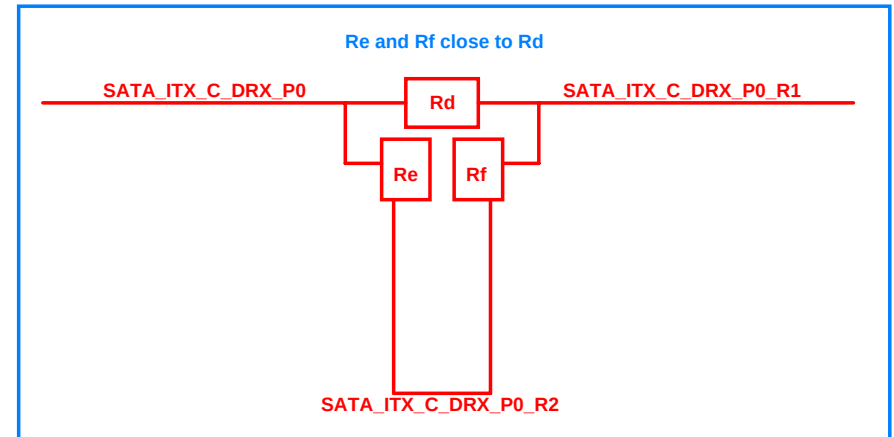
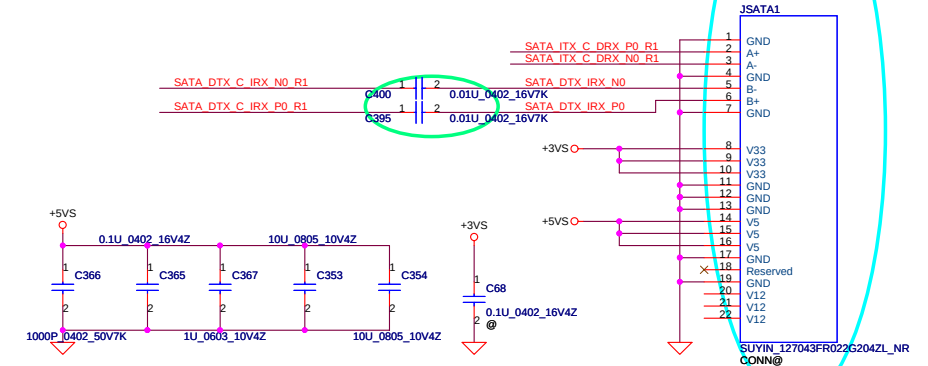
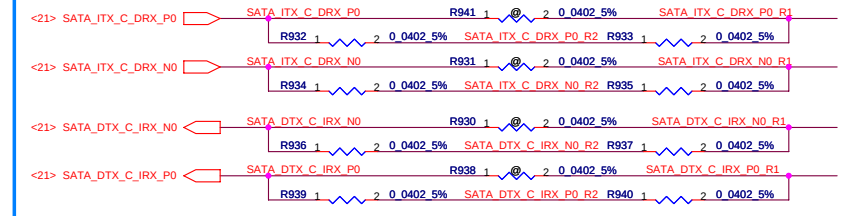
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SATA ODD Conn.

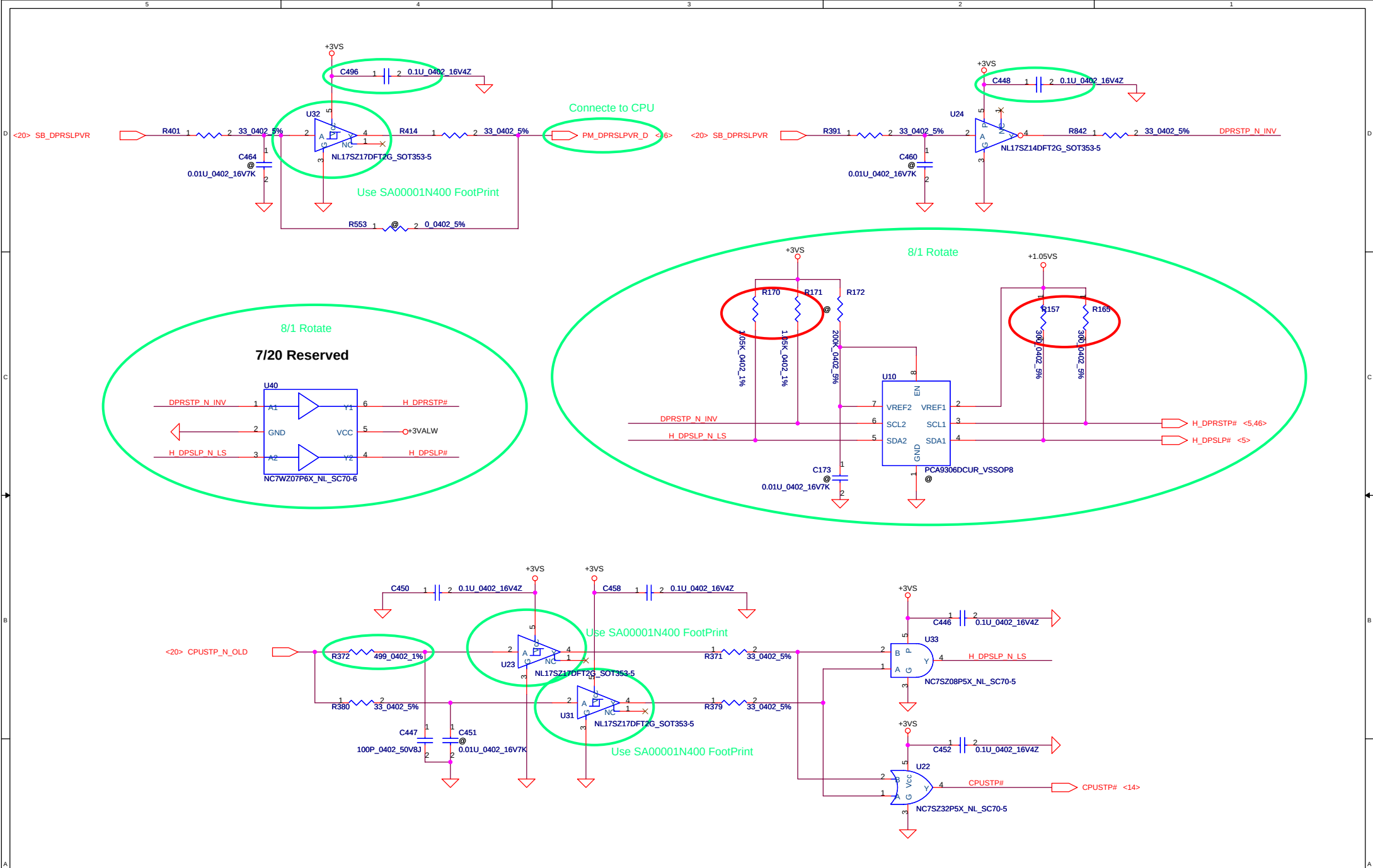


SATA HDD Conn.

12/29 SATA trace routing for layout (Length)



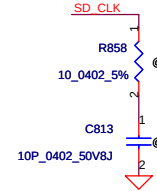
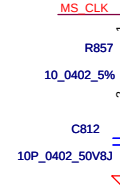
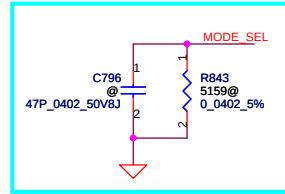
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	
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Size B		Document Number		Rev 1.0	
Date: Tuesday, March 10, 2009		Sheet 24 of 47		KFT00 M/B LA-4821P Schematic	



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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	Other
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				Customer	1.0
				Date	Wednesday, March 10, 2009
				Sheet	25 of 47

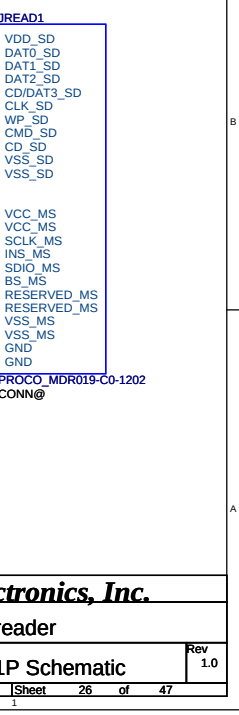
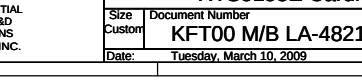
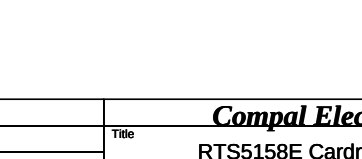
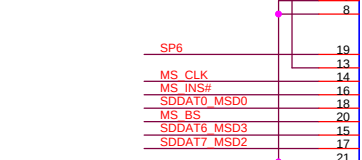
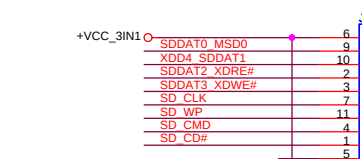
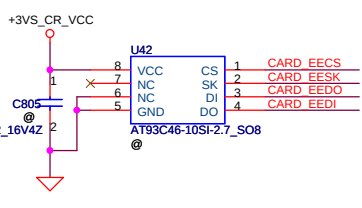
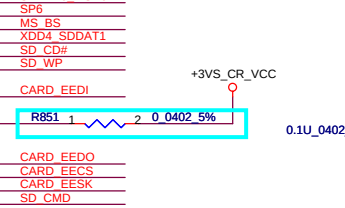
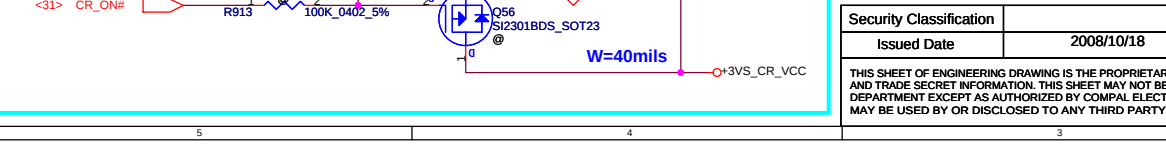
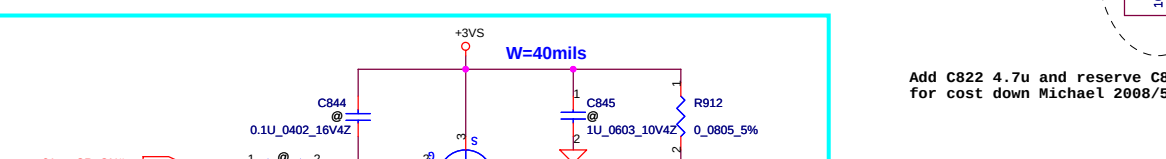
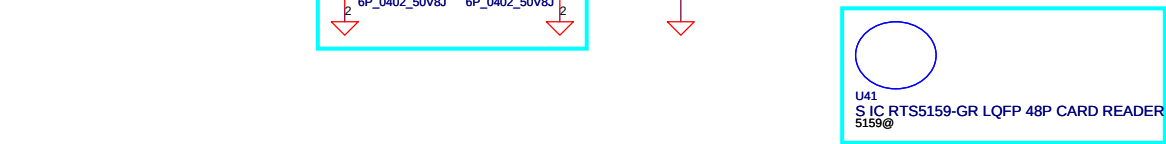
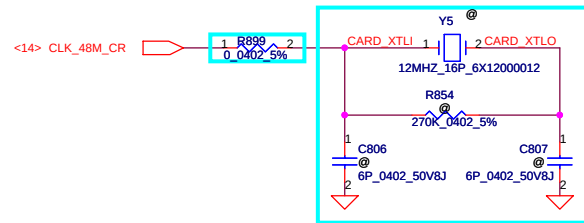
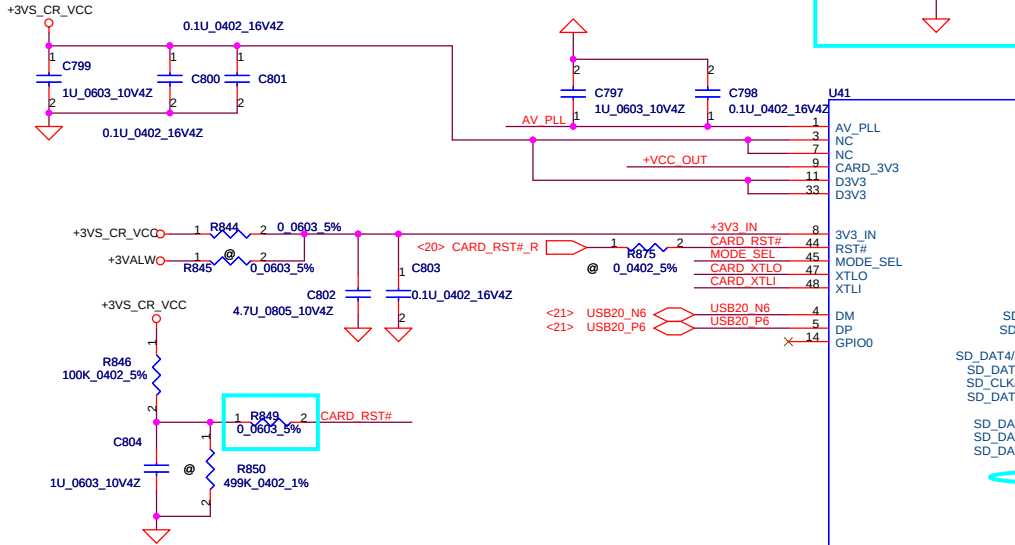
Change BOM control C796 R843 for 5158 and 5158E co-layout Michael 2008/6/18

Realtek Recommend



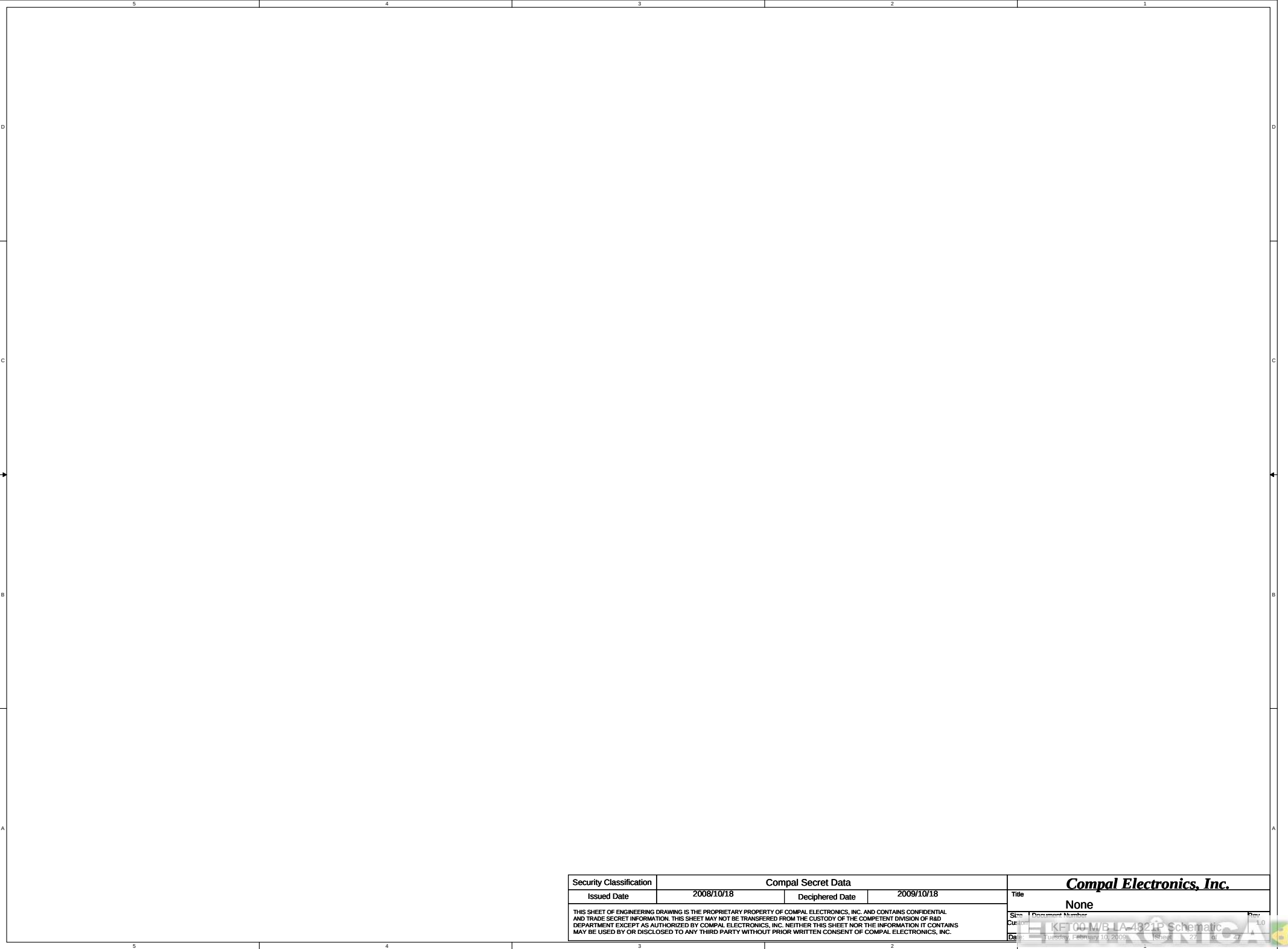
SD,MMC,MS muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			



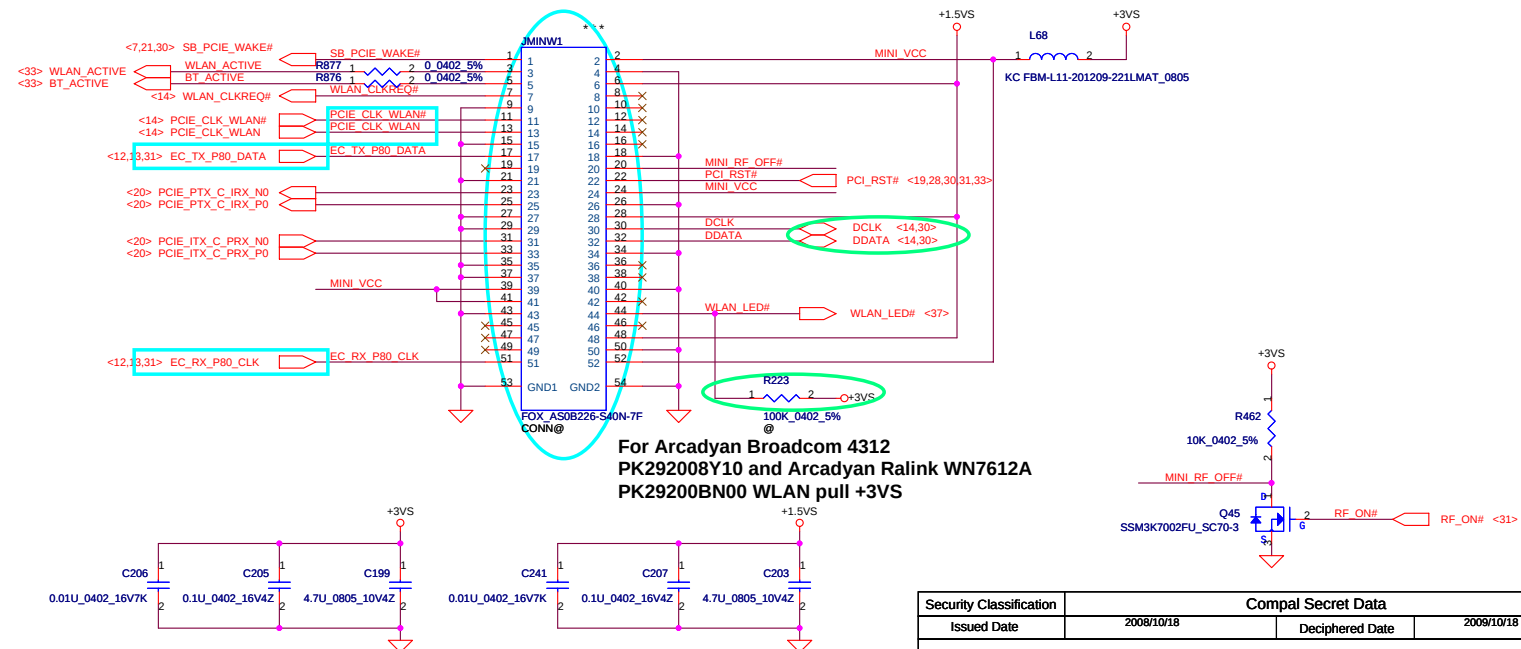
Add C822 4.7u and reserve C808 10u for cost down Michael 2008/5/30

Security Classification	Compal Secret Data			Title	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	RTS5158E Cardreader	
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				Custom	1.0
				Date:	Tuesday, March 10, 2009
				Sheet	26 of 47



Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	None	
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				Document Number	KE100.M/B.LA-4321P Schematic
				Revision	1.0
				Issue Date	Tuesday, February 10, 2009
				Issue By	27

Mini-Express Card for WLAN Follow JFT00 Smybol



Please place these caps between JMIN1 and JMIN2

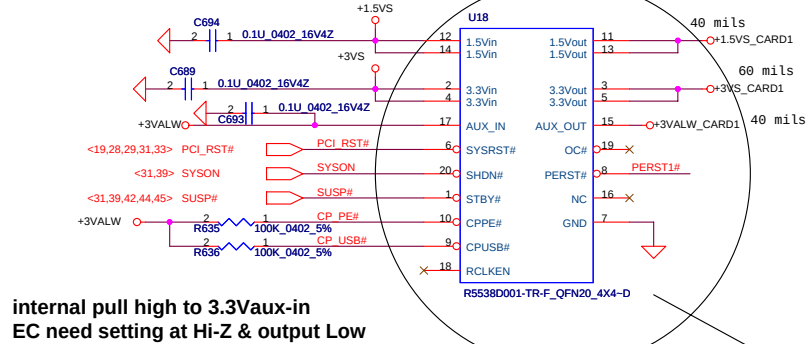


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Issued Date		2008/10/18		Deciphered Date		2009/10/18	
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Scri		Document Number		JFT00-M/B LA-4821P Schematic		Rev 1.0	
Da		Tuesday, March 10, 2009		Sheet		29 of 2	

New Card Power Switch

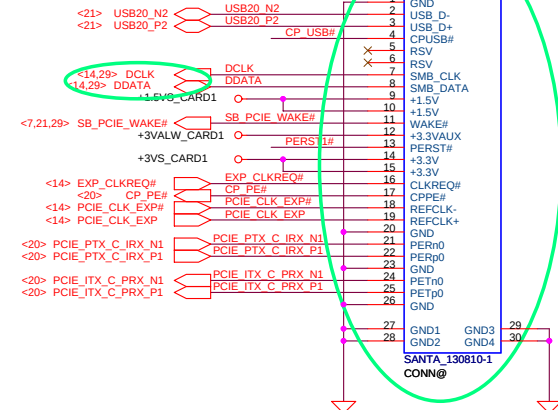
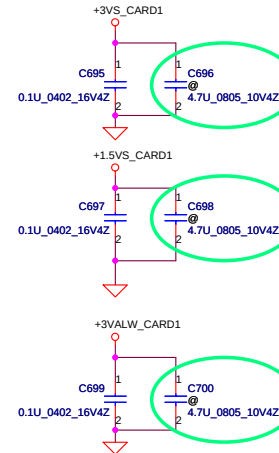
New Card

New Card Socket (Left/TOP)



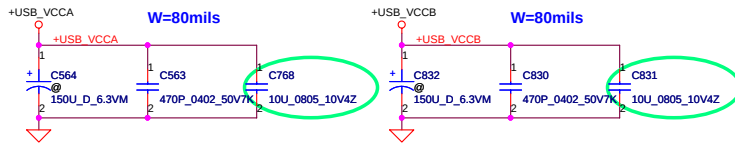
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Change to GMT PartNumber

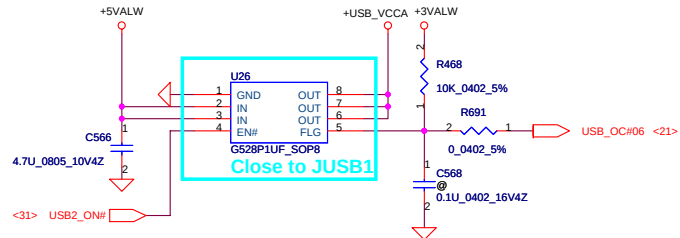


Update FootPrint from
SANTA_13181060-5_26P-T to
SANTA_130810-1_26P

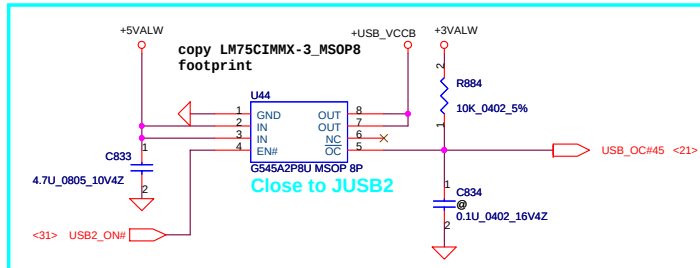
USB Connector



Change SA005280110 SOP8

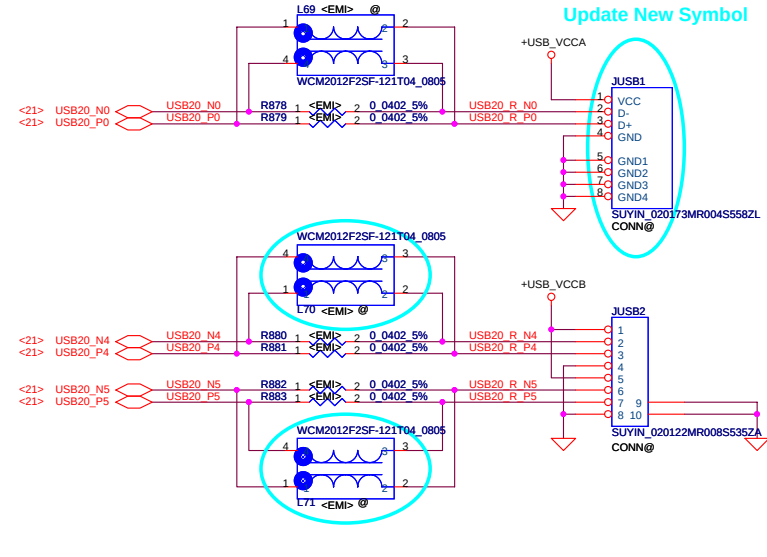


copy LM75CIMMX-3_MSOP8 footprint

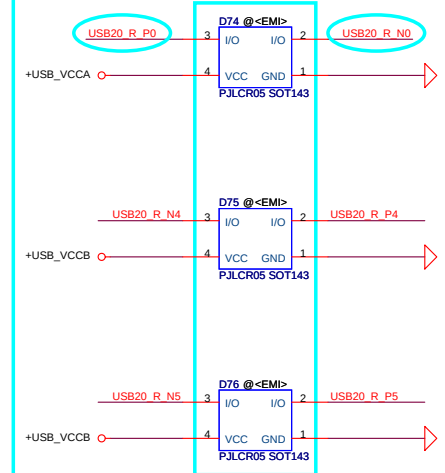
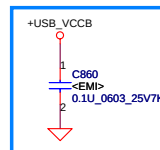


11/29 change this symbol's footprint as
AD77421ARMZ-REEL_MSOP8

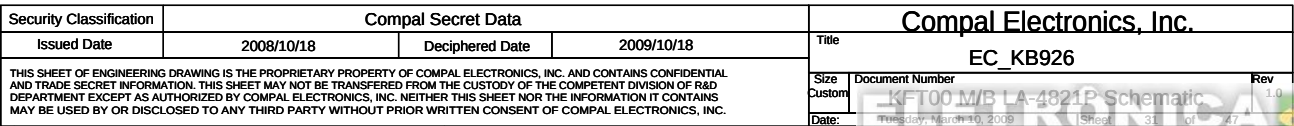
Update New Symbol



01/06 Add C860 for ESD Recommend

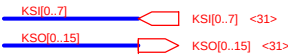
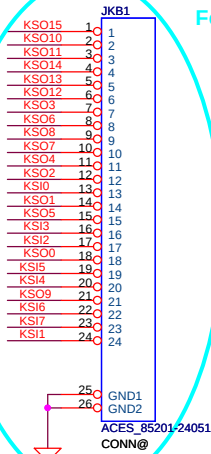


Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	New Card & USB Connector	
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				Date:	Tuesday, March 10, 2009
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				Rev	1.0

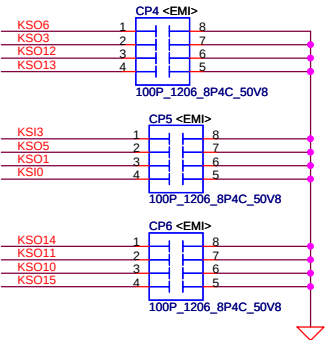
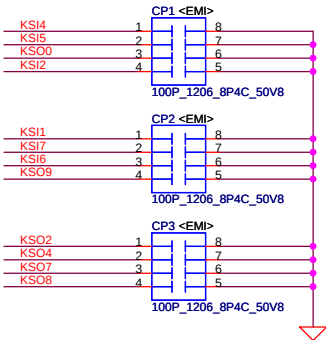


INT_KBD Conn.

Follow JFT00 Smybol

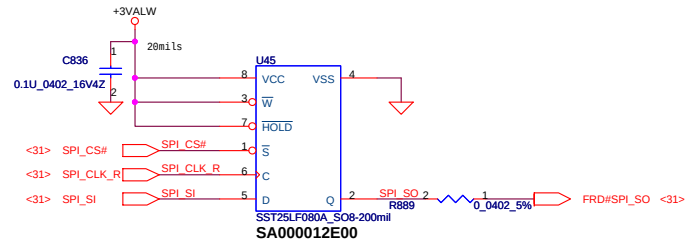


Delete C525~C548 SE071101J80 (100pF)
Add SI102101K80 (CP : 100pF)
(EMI Recommend)



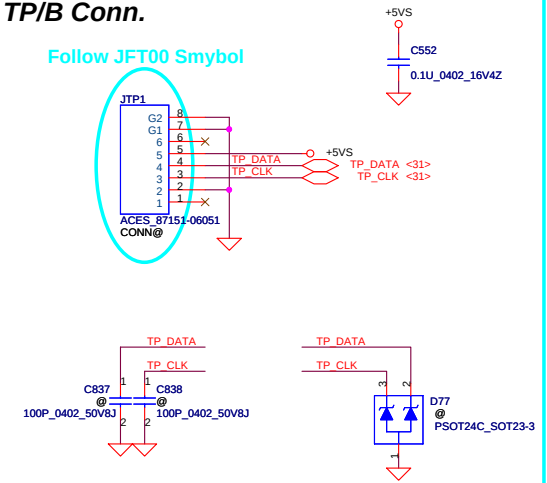
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	
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Size	Document Number	Rev		1.0	
Date:	Tuesday, March 10, 2009	Sheet	32	of	47

8M SPI ROM For EC+BIOS



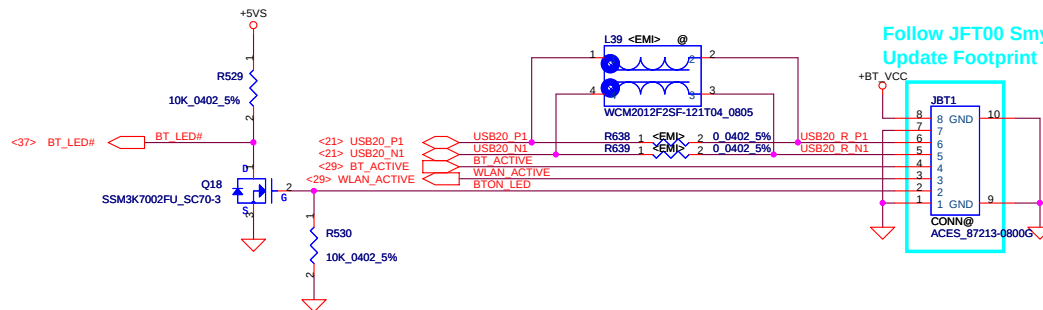
To TP/B Conn.

Follow JFT00 Smybol

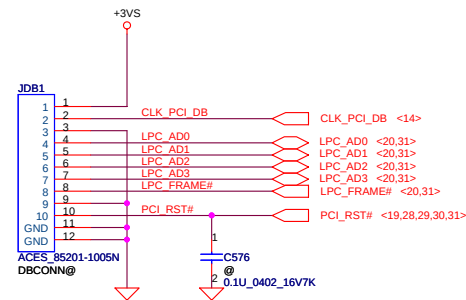
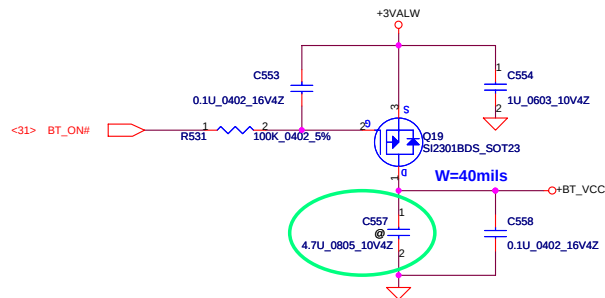


Bluetooth Conn.

Follow JFT00 Smybol
Update Footprint

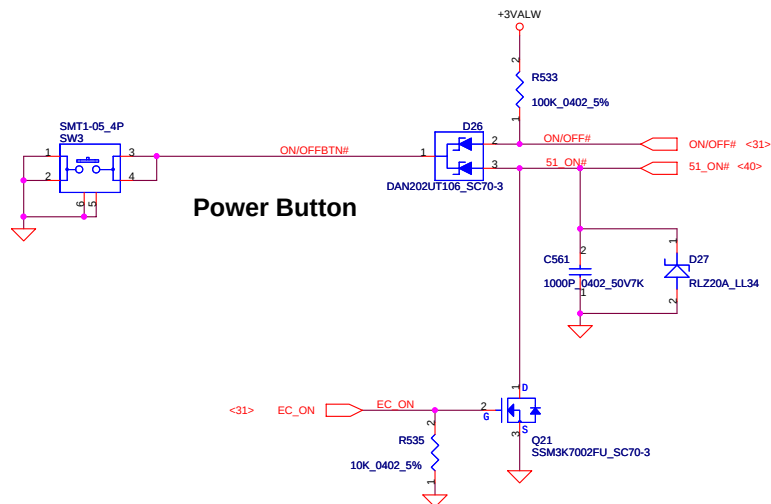


FOR LPC DEBUG PORT

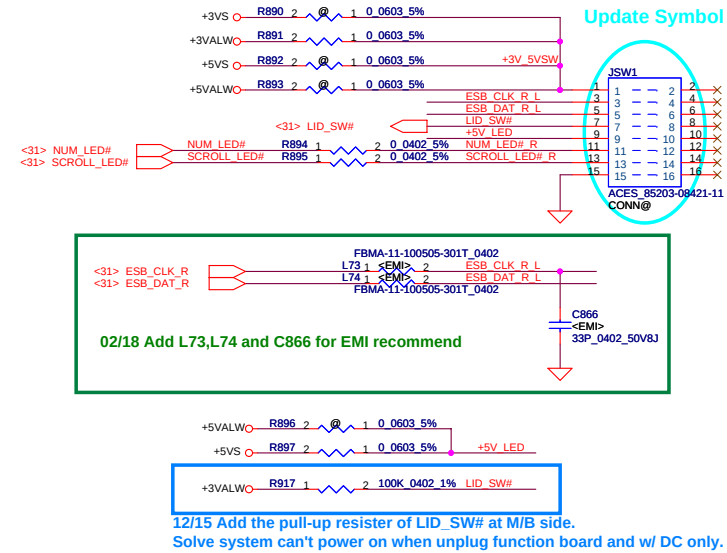


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	BIOS, I/O Port & K/B Connector
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Size	B	Date	Tuesday, March 10, 2009	Sheet	33 of 47
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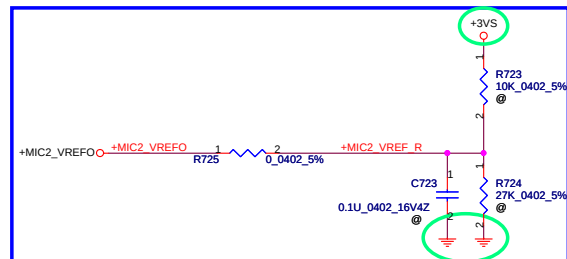
ON/OFF switch



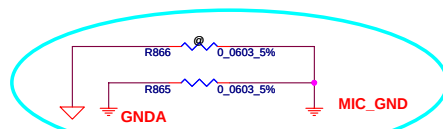
Conductive Board Conn.



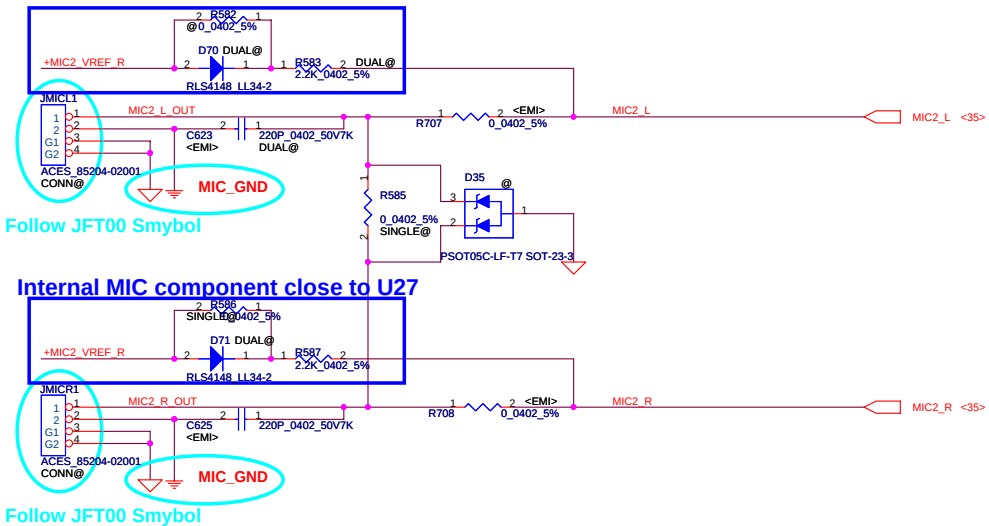
SINGLE INT MIC/DUAL INT MIC



Internal MIC component close to U27



Internal MIC component close to U27

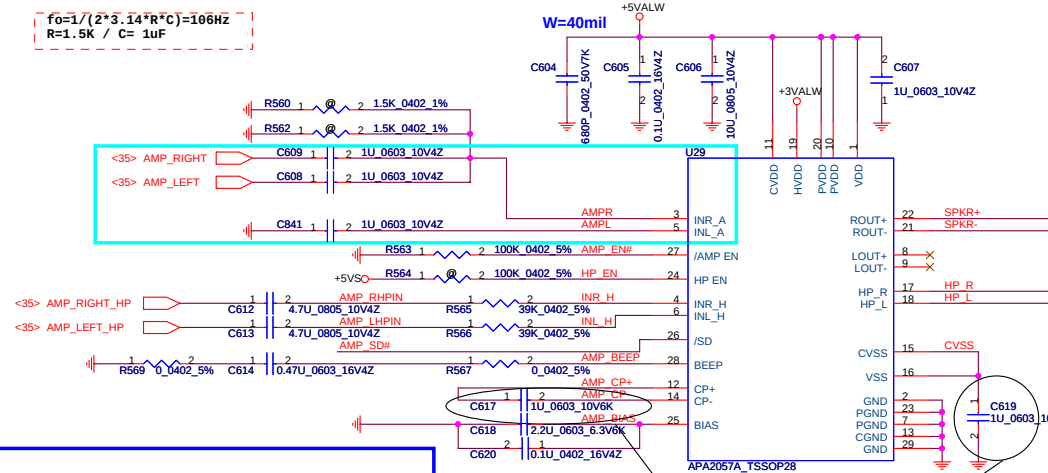


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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	PWROK/LID/Front/IO Board
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				KFT00 M/B LA-4821P Schematic	

APA2057 SPK/HP Amplifier

$$f_0 = 1 / (2 * 3.14 * R * C) = 106\text{Hz}$$

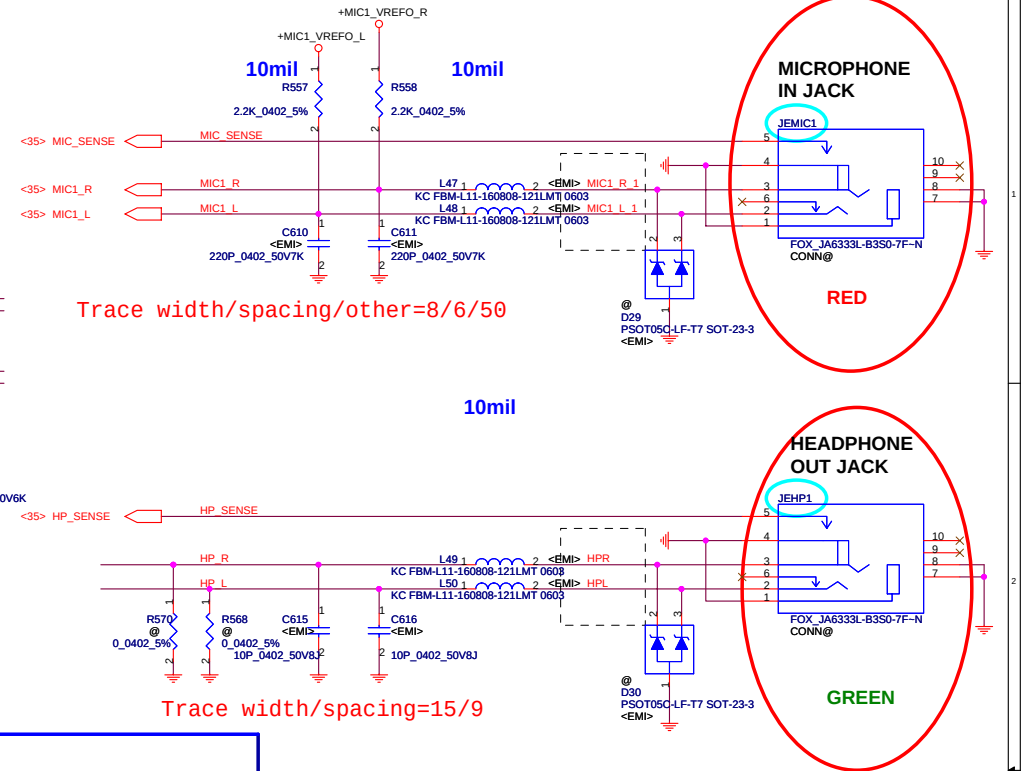
$$R = 1.5\text{K} / C = 1\mu\text{F}$$



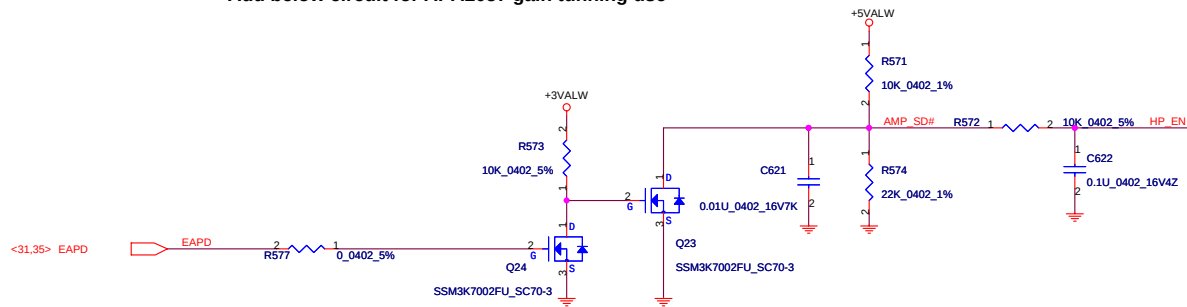
9/5 If implement AMP BEEP, Swap C641 and R524.
R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

11/28 Modified to X5R
11/28 Change to SE080105K80



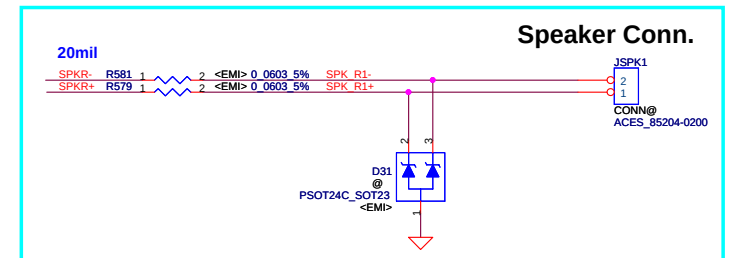
Add below circuit for APA2057 gain tuning use



Gain= 10dB

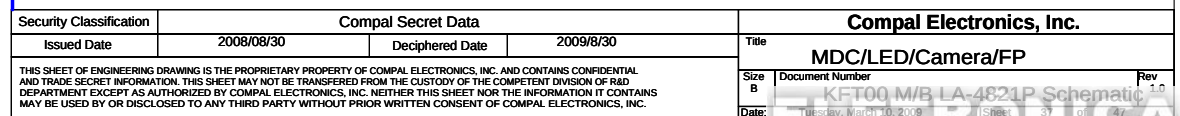
Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

+5VALW assume equal 5.1V
10 dB ----> 5.1 x 220 / 320 = 3.5

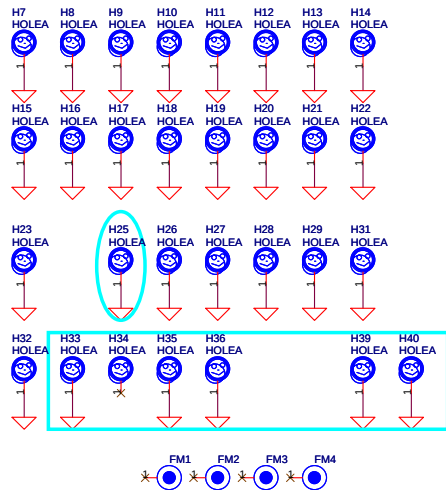


Security Classification		Compal Secret Data		Title	
Issued Date	2008/08/30	Deciphered Date	2009/8/30	AMP/VR/Audio Jack	
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Date:	Tuesday, March 10, 2008	Sheet	35 of 47	Rev	1.0

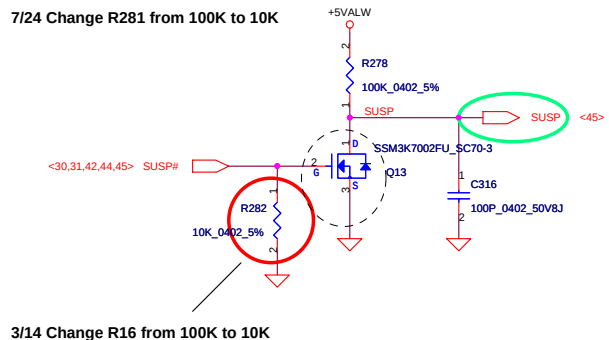
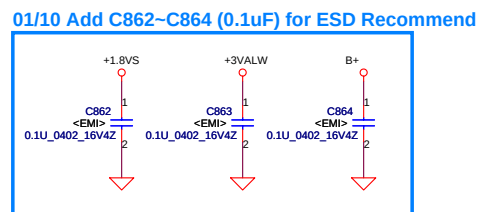
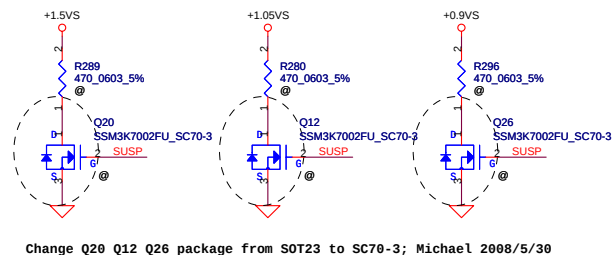
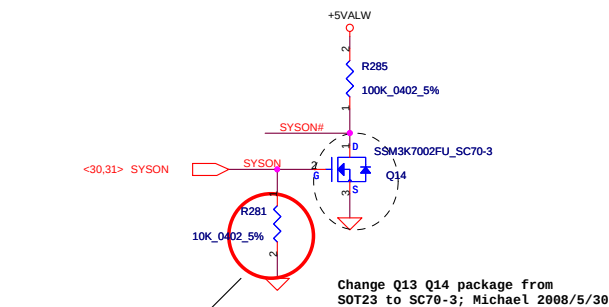
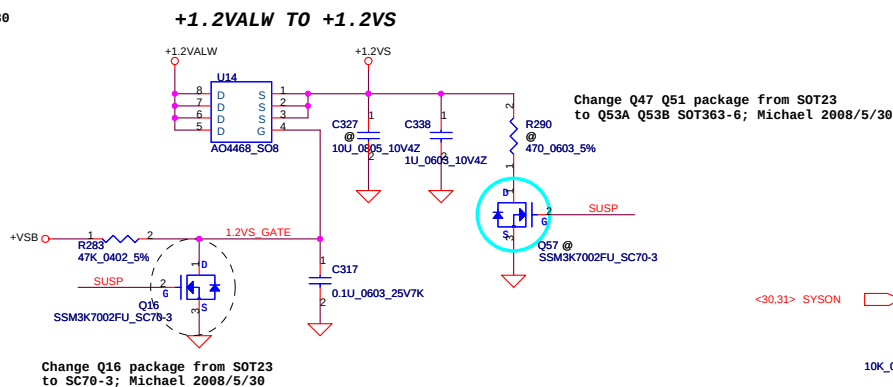
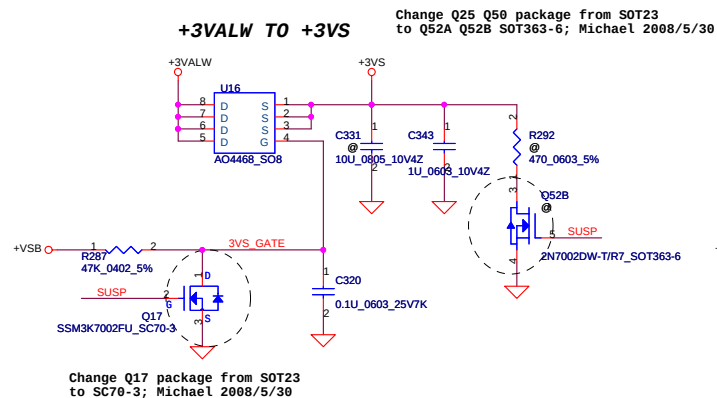
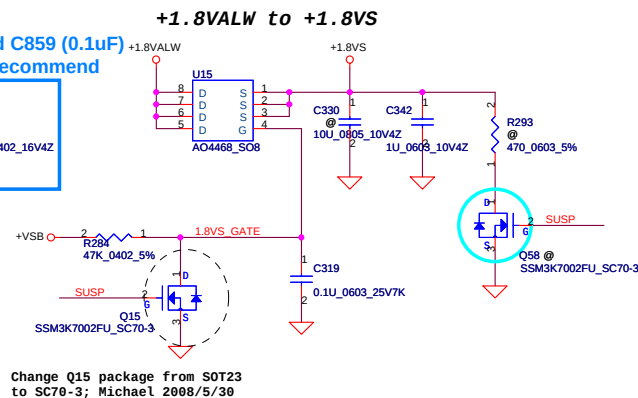
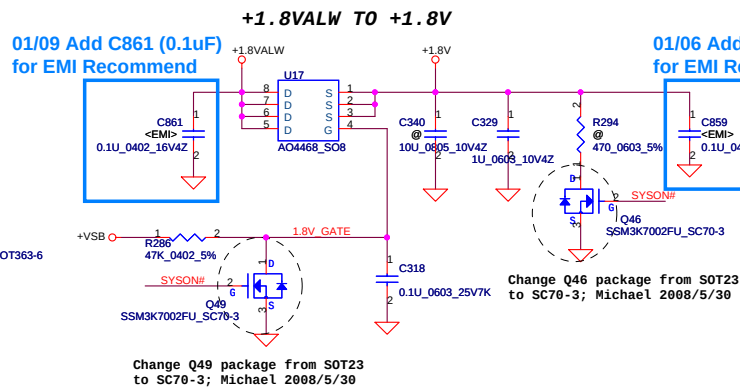
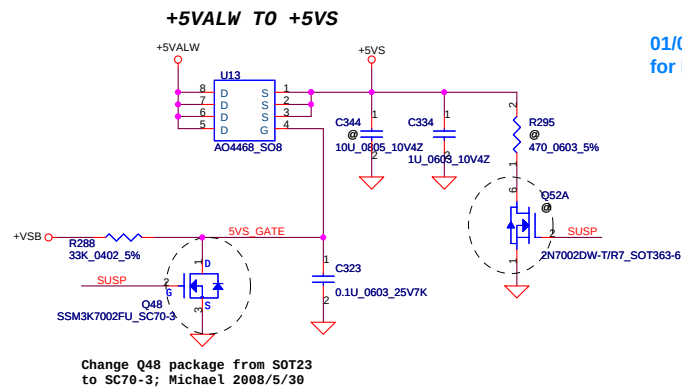
LED



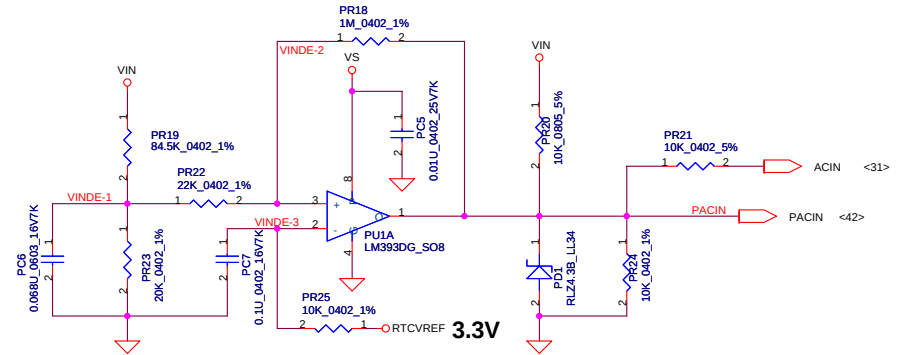
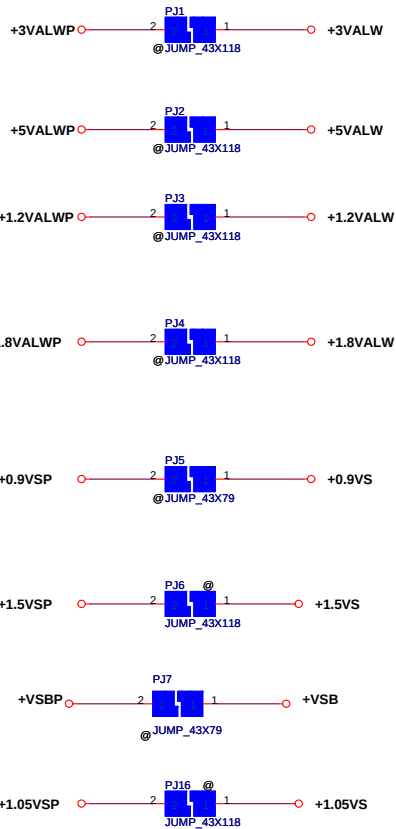
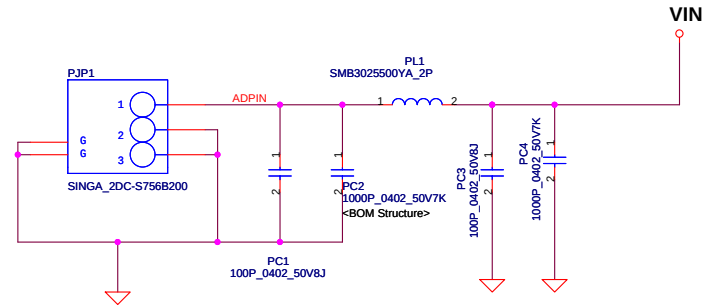
12/7 Modified LED footprint to LED_HT-297UD-CB_4P
12/15 Modified to correct LED symbol!!



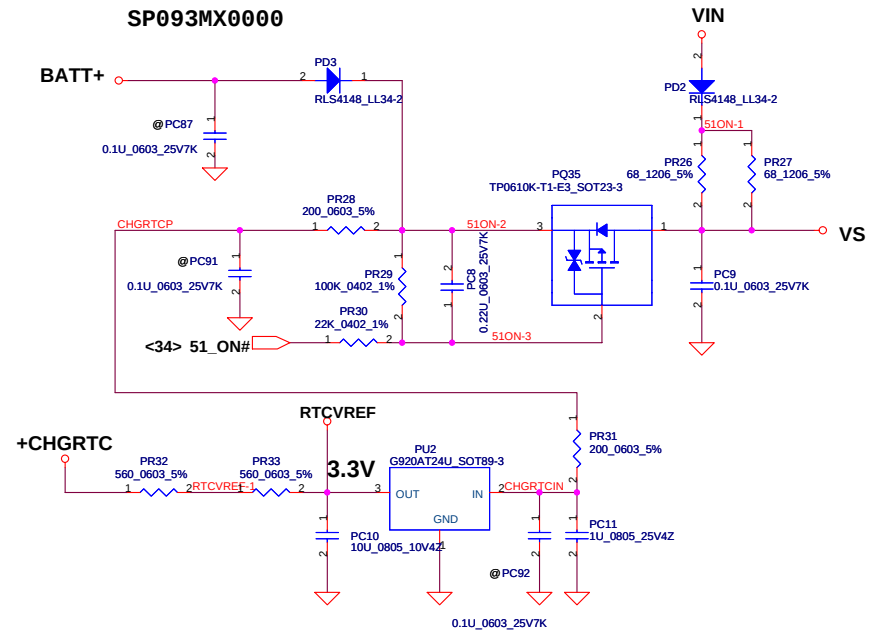
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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title		
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				Size	Document Number	Rev
				KFT00 M/B LA-4821P Schematic		
				1.0		
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				KF00 M/B LA-4321P Schematic	1.0
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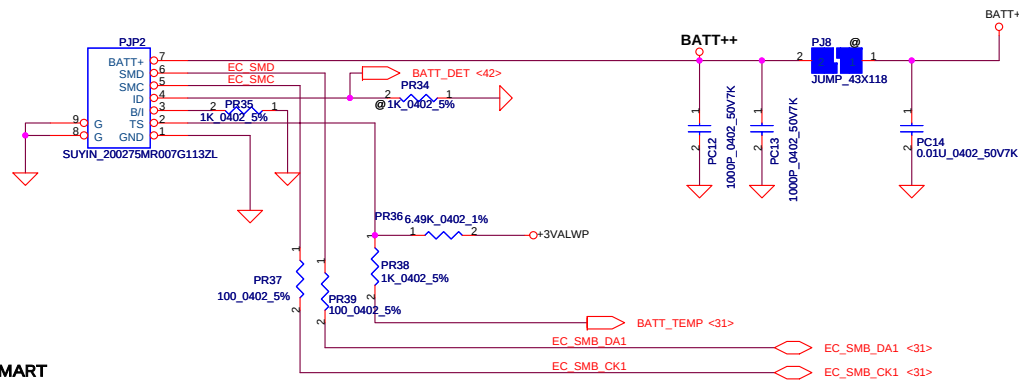


Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



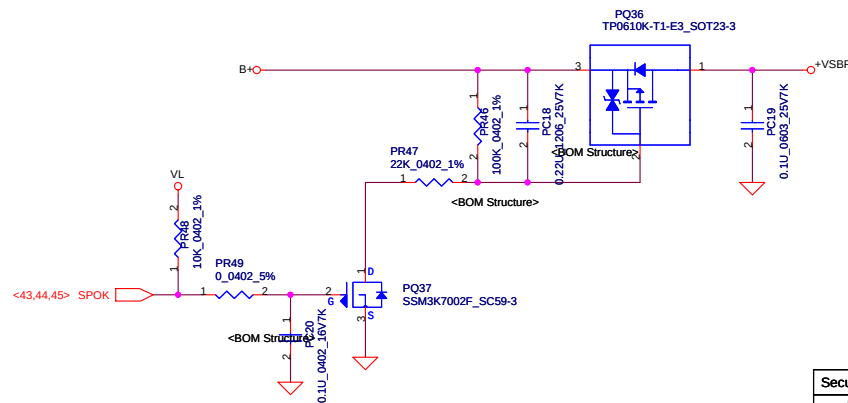
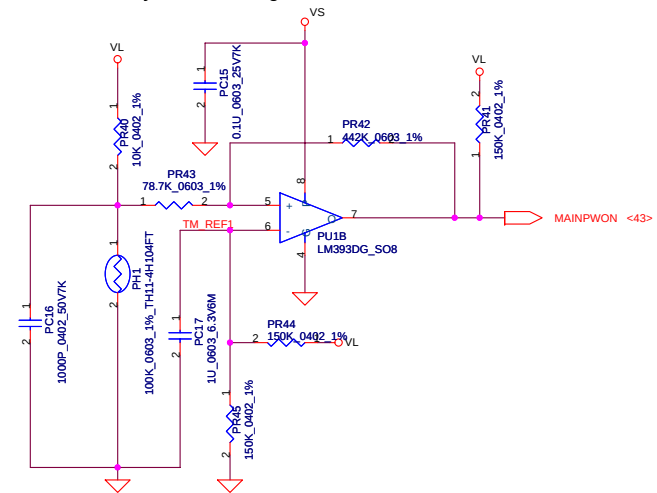
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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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Size	Document Number	KFT00 MB Schematic		Rev	
Customer				0.2	
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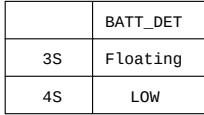
SMART
Battery:
7.BATT+
6.SMD
5.SMC
4.ID
3.B/I
2.TS
1.GND

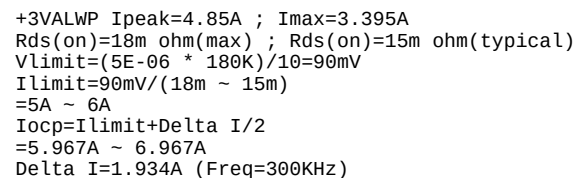


	BATT_DET
3S	Floating
4S	LOW

PH1 under CPU botten side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C

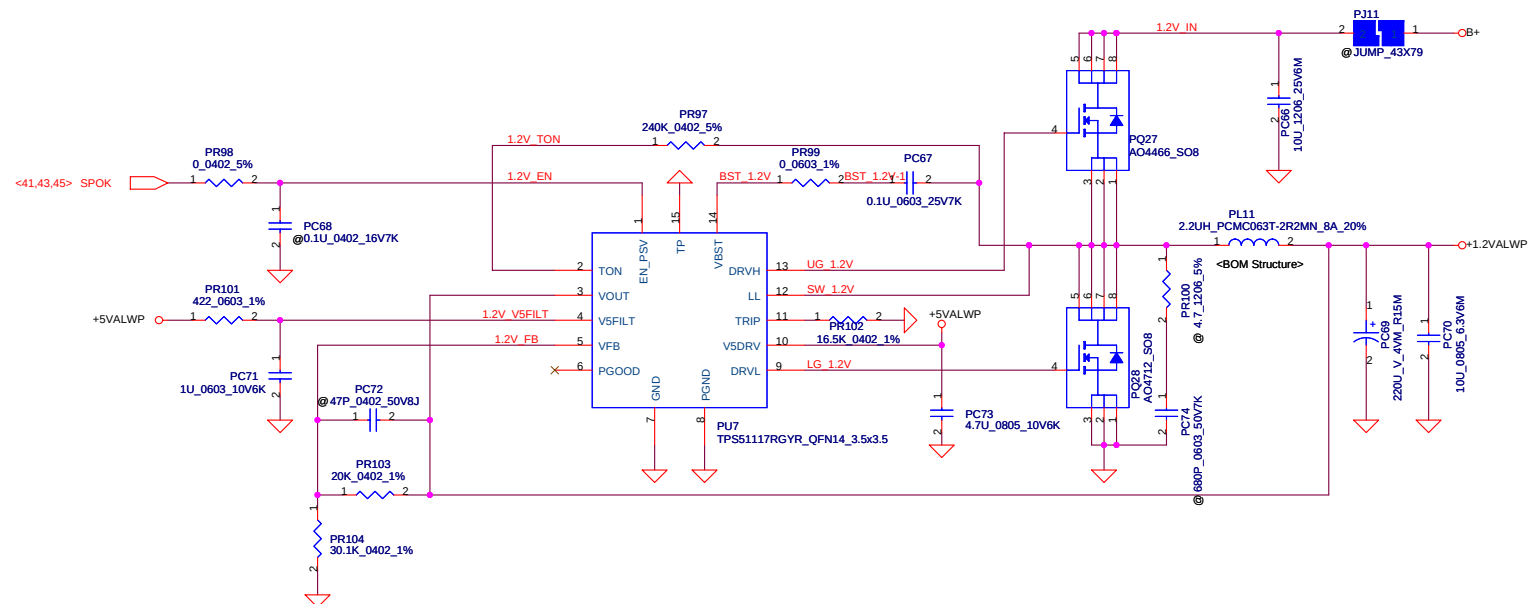




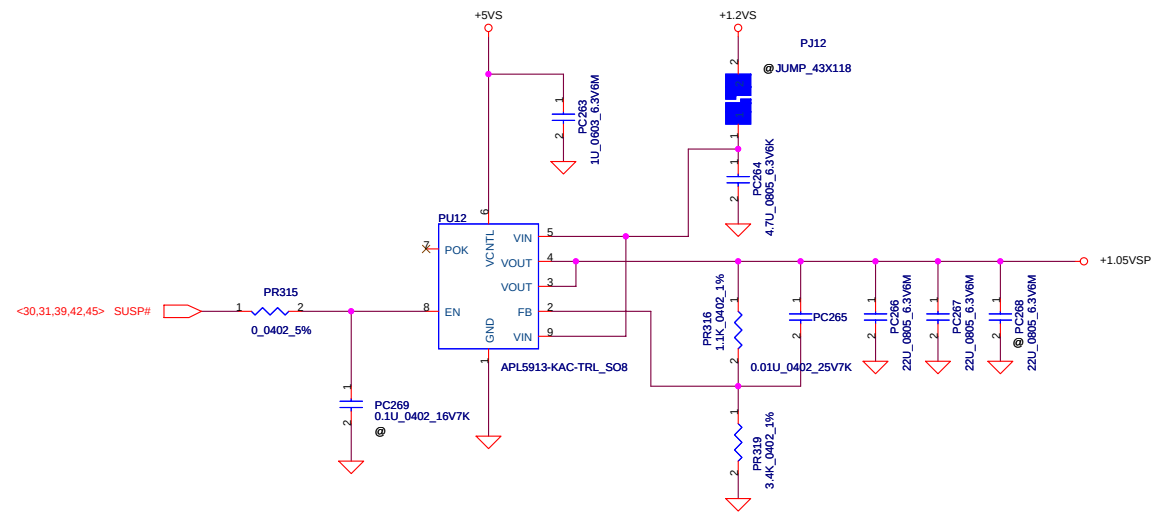


```
+5VALWP Ipeak=8.11A ; Imax=5.677A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 316K)/10=158mV
Ilimit=158mV/(18m ~ 15m)
=8.77A ~ 10.53A
Iocp=Ilimit+Delta I/2
=9.75A ~11.51 A
Delta I=1.956A (Freq=400KHz)
```

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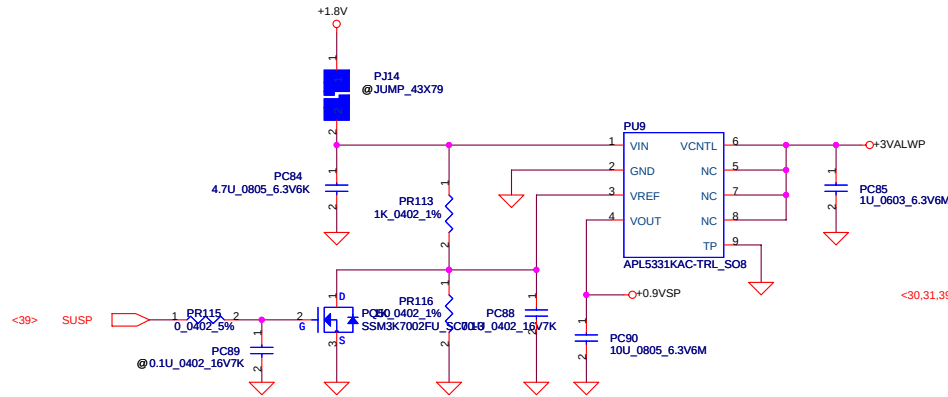
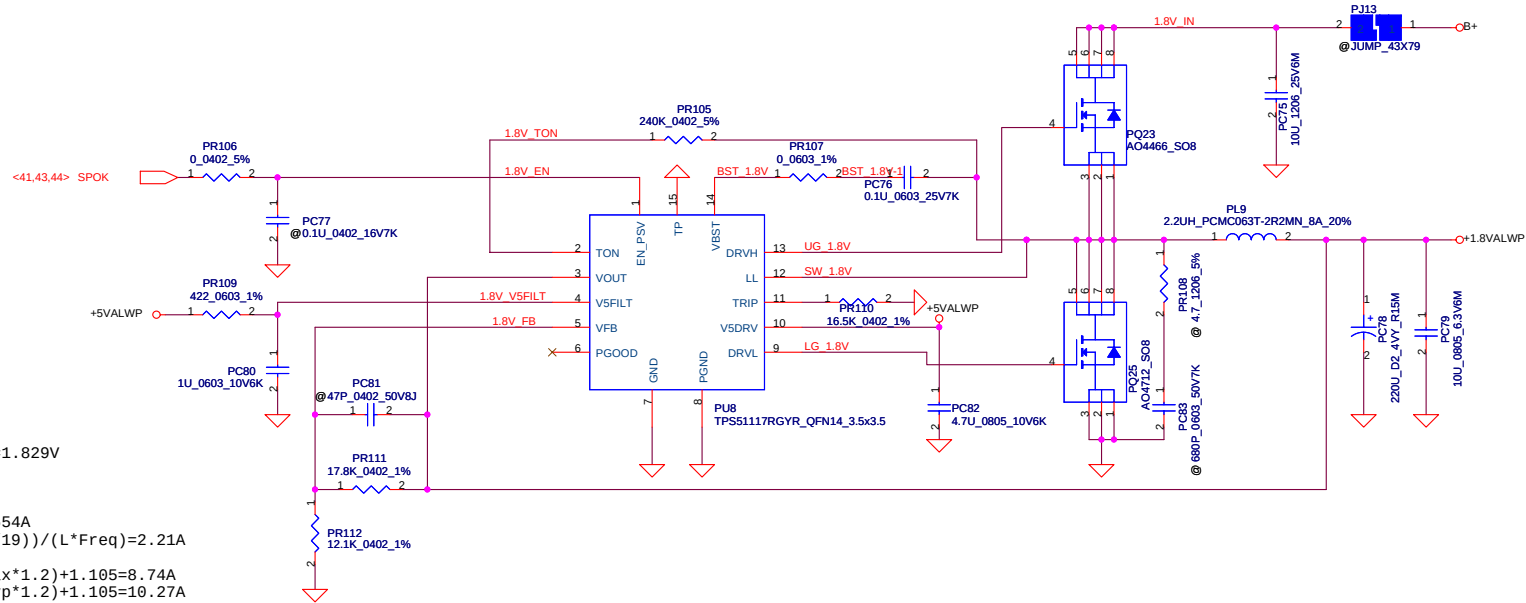
$V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR103/PR104)=1.203V$
 $Ton=187.68ns$
 $Freq=337KHz$
 $Cesr=15m\ ohm$
 $I_{peak}=7.82A\ I_{max}=5.474A$
 $\Delta I=((19-1.2) \cdot (1.2/19))/(L \cdot Freq)=1.516A$
 $V_{trip}=R_{trip} \cdot 10\mu A=165mV$
 $I_{ocp-min}=V_{trip}/(R_{ds(on)max} \cdot 1.2)+0.758=8.4A$
 $I_{ocp-max}=V_{trip}/(R_{ds(on)typ} \cdot 1.2)+0.758=9.92A$
 $I_{ocp}=8.4A \sim 9.92A$



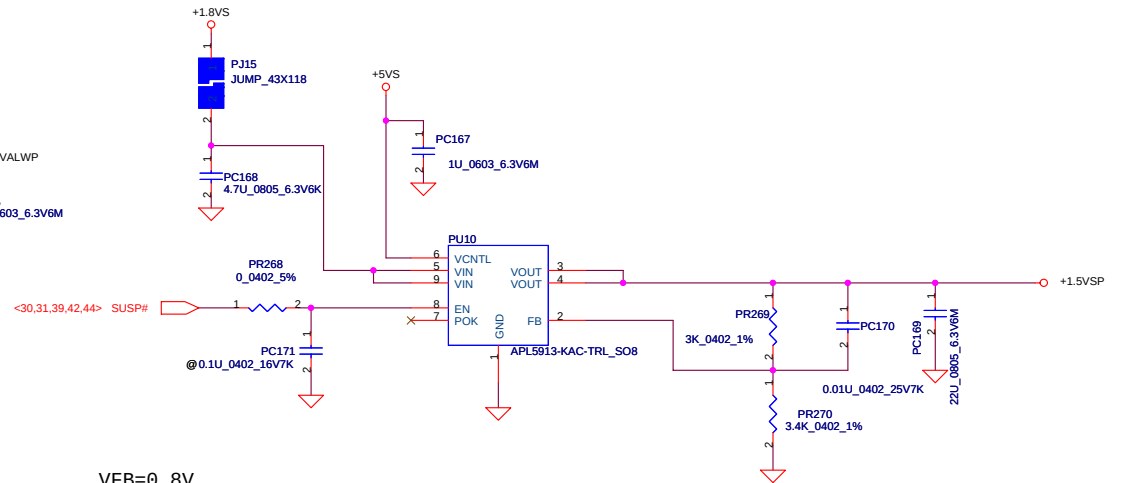
$FB=0.8V$
 $V_{out}=0.8V \cdot (1+R316/R319)$
 $I_{max}=3.22A\ I_{peak}=4.6A$

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$V_{FB}=0.75V$
 $V_o=V_{FB}*(1+PR111/PR112)=1.829V$
 $Freq=334KHz$
 $Cesr=ohm$
 $I_{peak}=12.22A$ $I_{max}=8.554A$
 $\Delta I=((19-1.8)*(1.8/19))/(L*Freq)=2.21A$
 $V_{trip}=R_{trip}*I_{max}=165mV$
 $I_{ocp-min}=V_{trip}/(R_{dsonmax}*1.2)+1.105=8.74A$
 $I_{ocp-max}=V_{trip}/(R_{dsonmax}*1.2)+1.105=10.27A$
 $I_{ocp}=8.74A-10.27A$

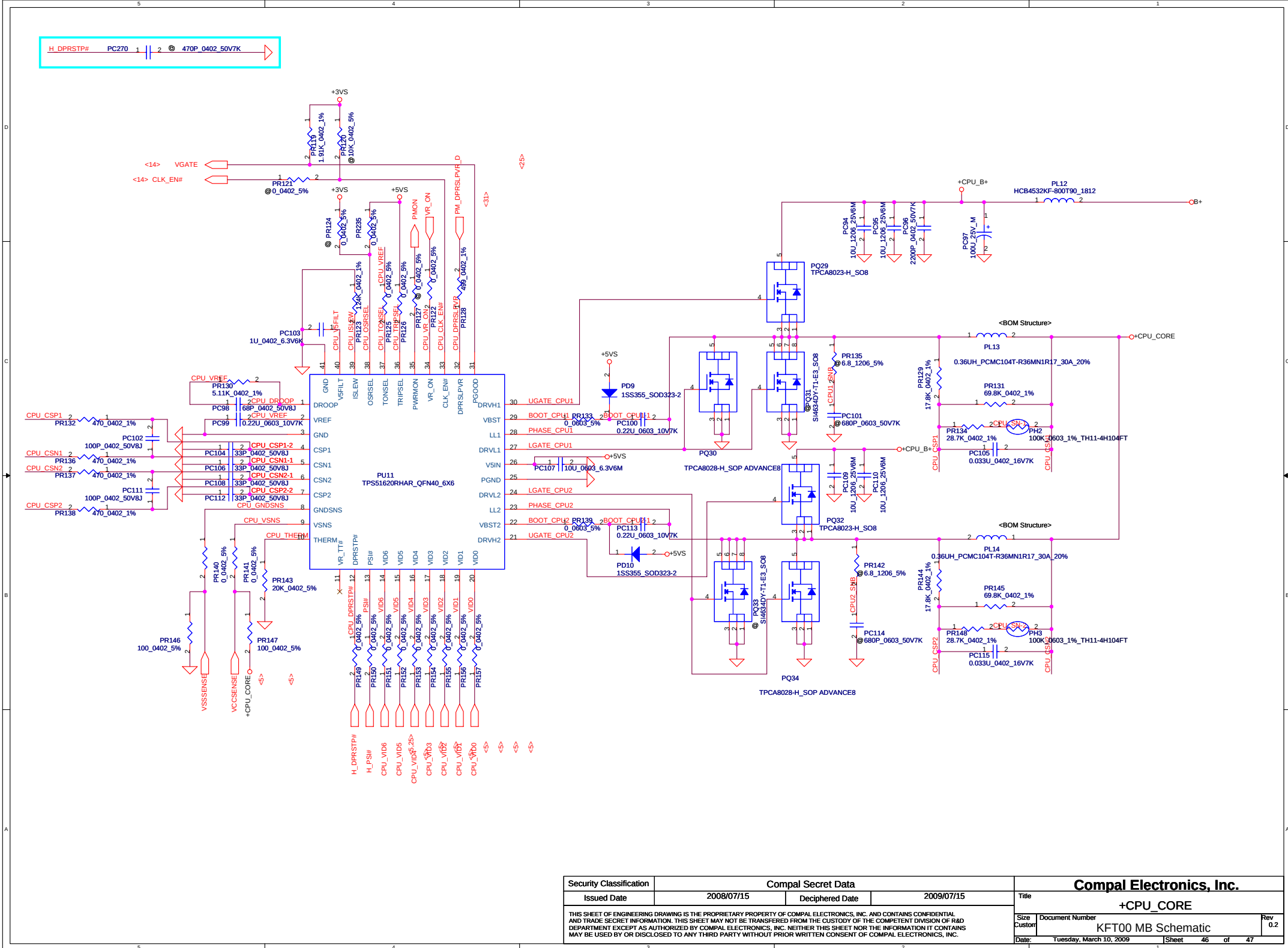


$V_{out}=V_{in}*R116/(R113+R116)=0.925$
 $I_{max}=1.4A$ $I_{peak}=2A$



$V_{FB}=0.8V$
 $I_{max}=0.966A$ $I_{peak}=1.38A$

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1		Change charge current to 3.36A at Iref=3.3V	A	3	change PR70 from 133K to 97.6K		
2		change charger current sense size and value	A	3	change PR17 from 15m to 20m ohm		
3		Set charger voltage	A	3	Delet PR64		
4		change PQ38 ,PQ39 for EOL	A	3	Change to FDS4435BZ		
5		change PR90 ,PR91 for 3V,5V ocp set	A	4	Change from 301K to 315K and 174K		
6		change PR102 for 1.2V OCP set	A	5	Change from 14.7K to 16.5K		
7		change 1.2v from 1.225V to 1.2V follow KSWXX	A	5	Change PR103 and PR104 to 18.2K and 30.1K		
8		change PR110 for 1.8V OCP set	A	6	Change from 14.7K to 16.5K		
9		change 1.8v from 1.851V to 1.829V follow KSWXX	A	6	Change PR111 and PR112 to 17.4K and 12.1K		
10		change chgvadj risister match ec parameter	A	3	Change PR66 100K to 499K		
11		change PL13,PL14 for cost	A	7	Change PL13 PL14 to Toho		
12		modify CP point to 3.13A	A	3	change PR53 from 0 to 113K ohm		
13		change charger current to 3A	C		change PR70 from 97.6K to 133K ohm		
14		change 3V OCP	C		change PR91 from 180K to 316K ohm		
15		adjust cpu load line	C		change PR130 from 4.02K to 5.49 K ohm		
16		change cpu choke footprint	C		change choke footprint from toho to cyntec		
17		change PR229 from 100k to 47k			adjust cell pin voltage		
18		adjust back to back mos turn off time			change PC27 from 0.47U to 0.1U		
19		Adjust 1.2v voltage from 1.2035V to 1.2483V for hw requet			change PR103 from 18.2k to 20k		
20		Adjust 1.8v voltage from 1.8285V to 1.8533V for hw request			change PR111 from 17.4k to 17.8k		
21		adjust cpu load line			change PR130 from 5.49k to 5.11k		
22		NP0 must use J tolerance			change PC104 PC106 PC108 PC112 from K to J tolerance		
23							

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