

COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA

PCB NO : LA-A971P

BOM P/N : 4319RJ31LXX

GPIO MAP: 3.3b

Goliad MLK 12" UMA

Broadwell U Processor

2013-12-23

REV : 0.3 (X01)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

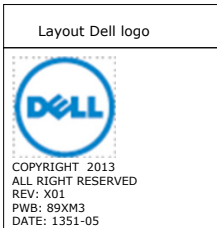
@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

VPRO@ : Vpro Component


NVPRO@ : Non-Vpro Component



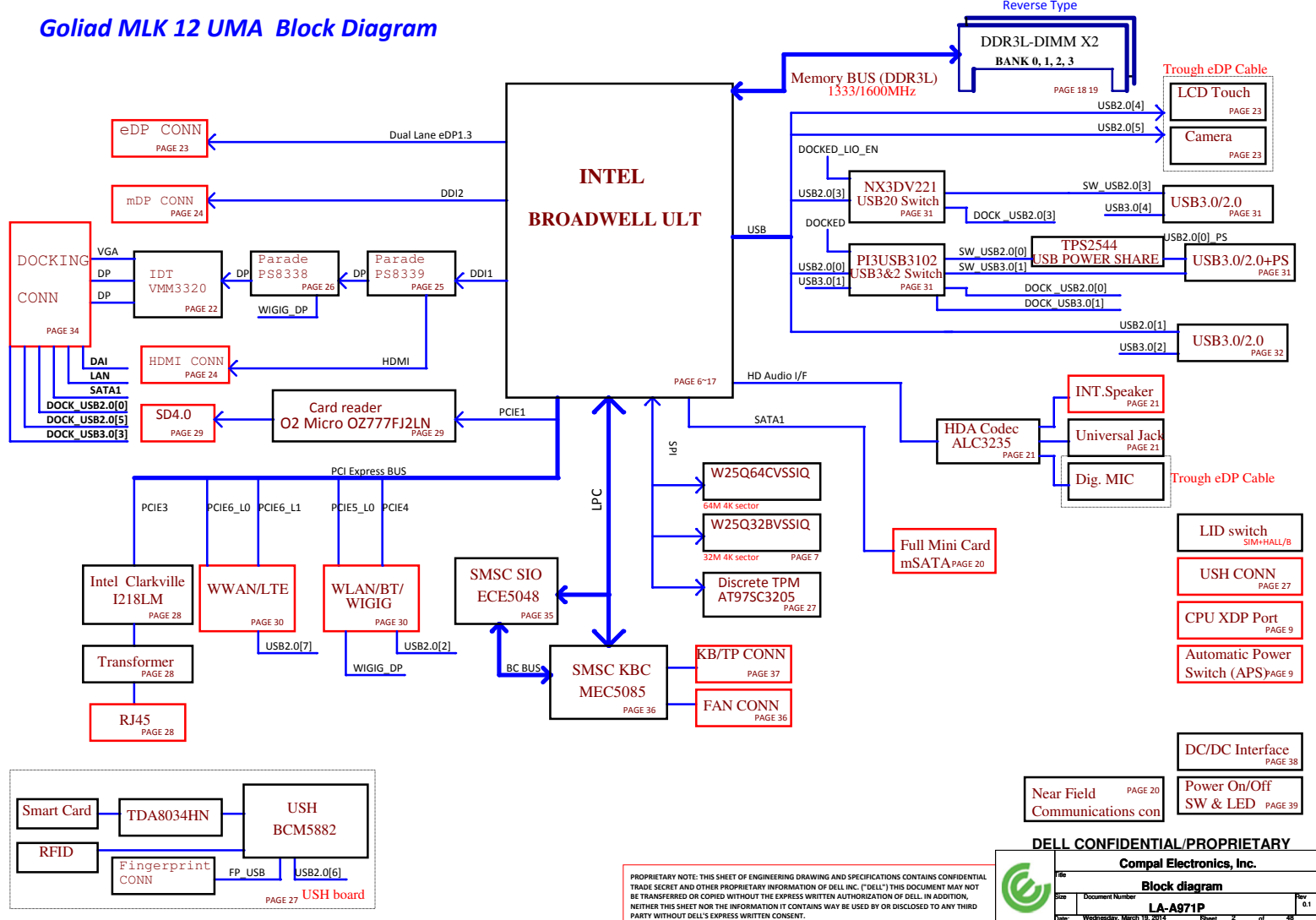
MB PCB	
Part Number	Description
DAA0083000	PCB 14A LA-A971P REV0 MB WITH DOCKING 2

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Goliad MLK 12 UMA Block Diagram



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Block diagram

LA-A871P

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	HCA & SATA Cache - JNGFF2
		SATA 2	SATA Cache - JNGFF2
		SATA 1	JMINI3
		SATA 0	JDOCK1

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

BDW ULT	USB PORT#	DESTINATION
	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
7	WWAN	

USH	0	BIO
	1	NA

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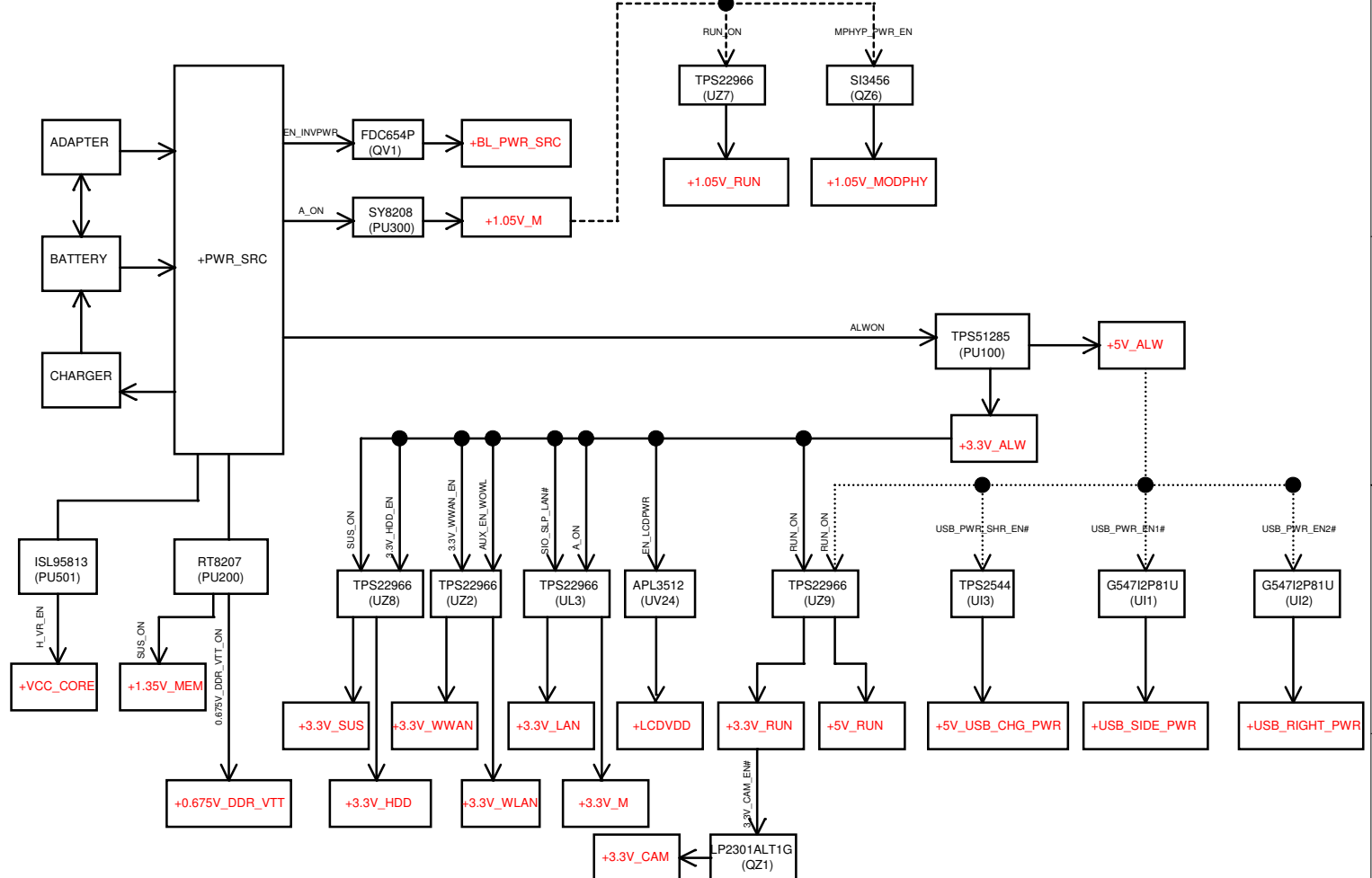
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File: **Port assignment**

Size: Document Number **LA-A971P** Rev: 0.1


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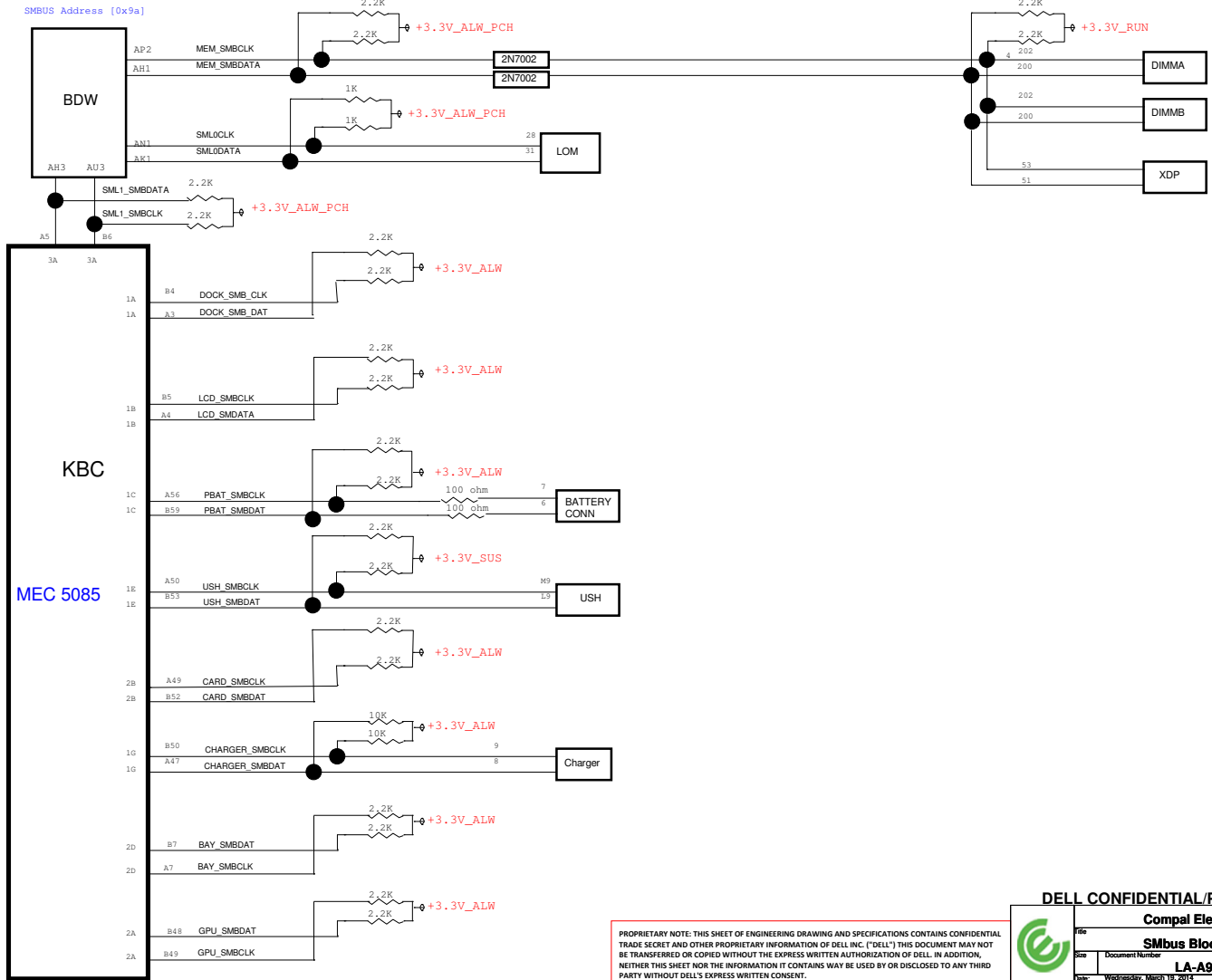
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SMBUS Address [0x9a]



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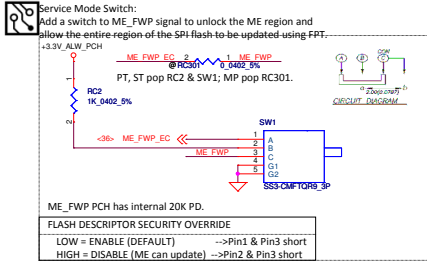
SMBus Block diagram

LA-A971P

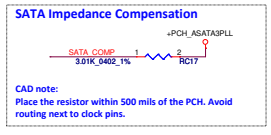
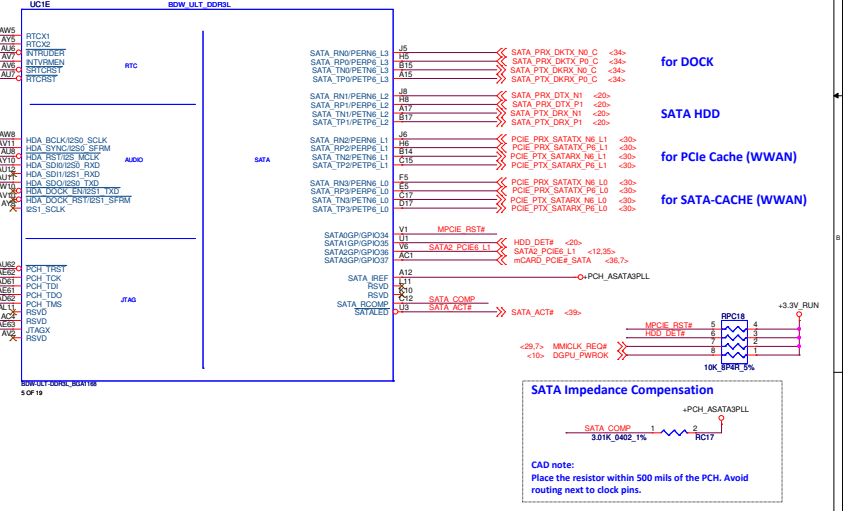
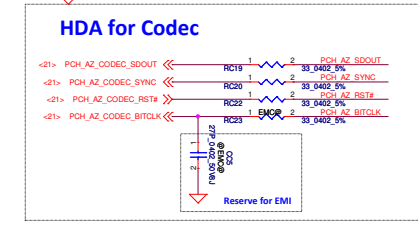
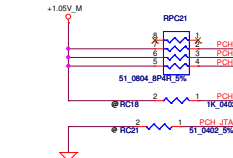
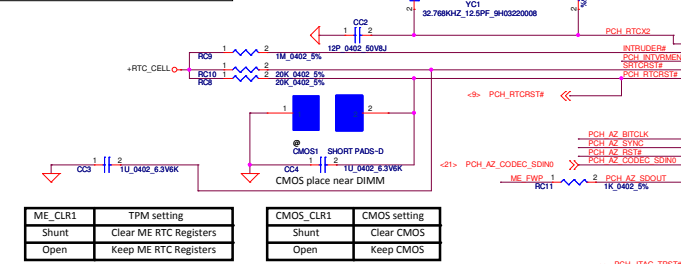
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UMA SATA port

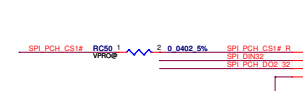
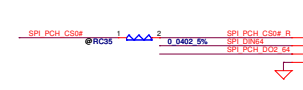
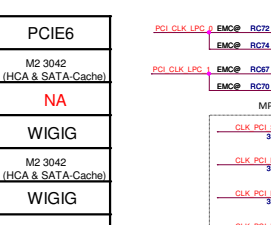
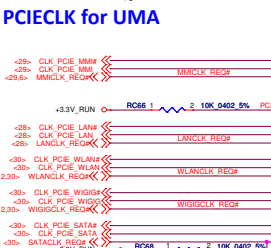
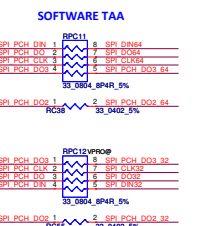
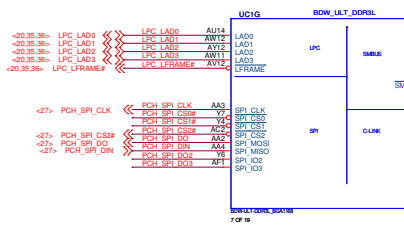
SATA0	SATA1	PCB	SATA2/PCIe6 L1	SATA3/PCIe6 L0	
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G12 Entry	NA	NA	
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIe6_L1 contact to WWAN SATA3/PCIe6 L0 contact to WLAN
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	G14U_En	NA	NA	



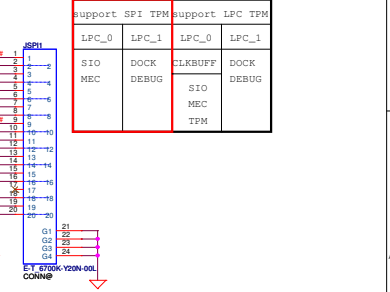
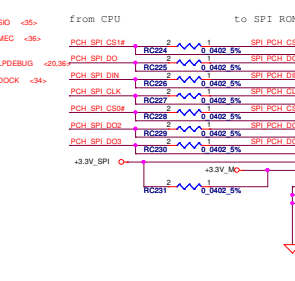
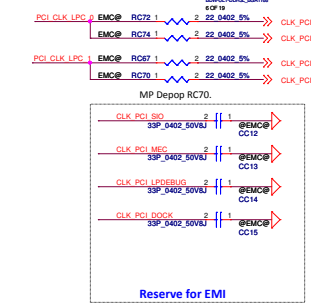
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs



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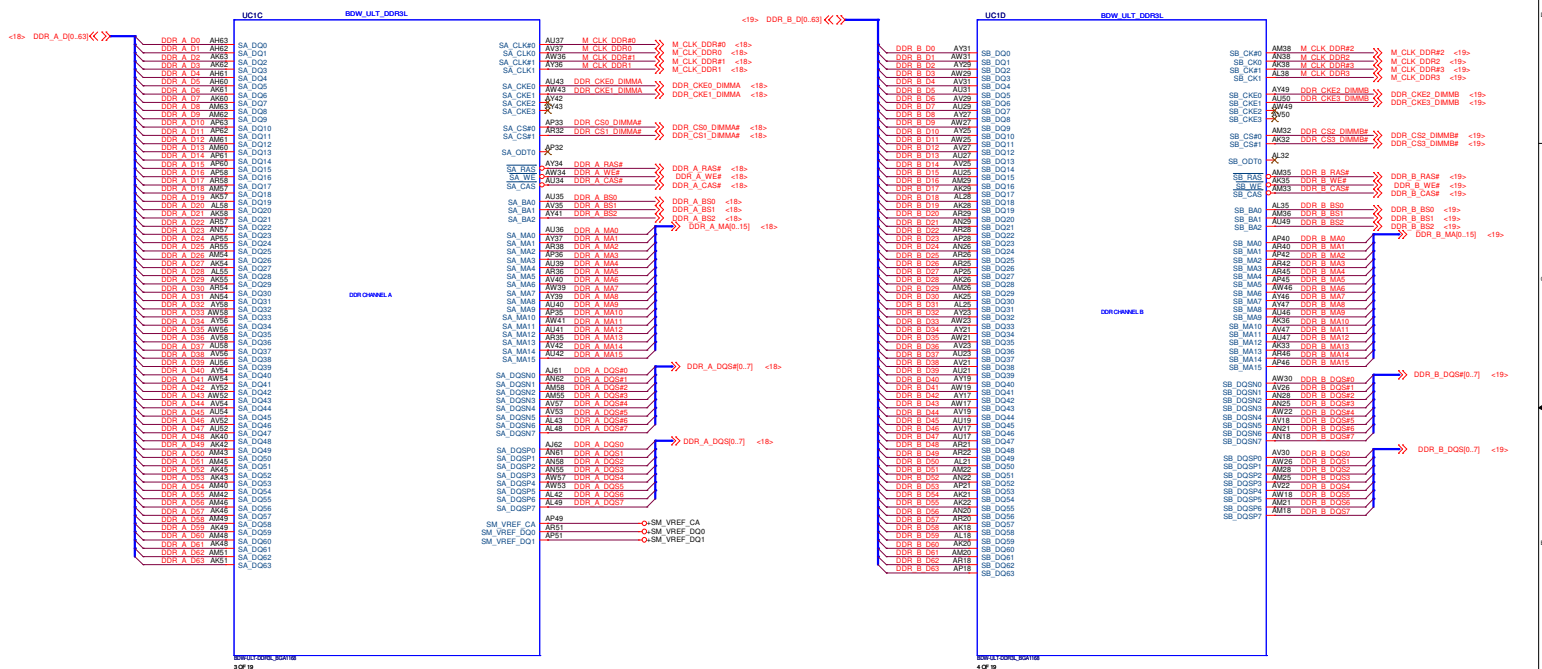
PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA



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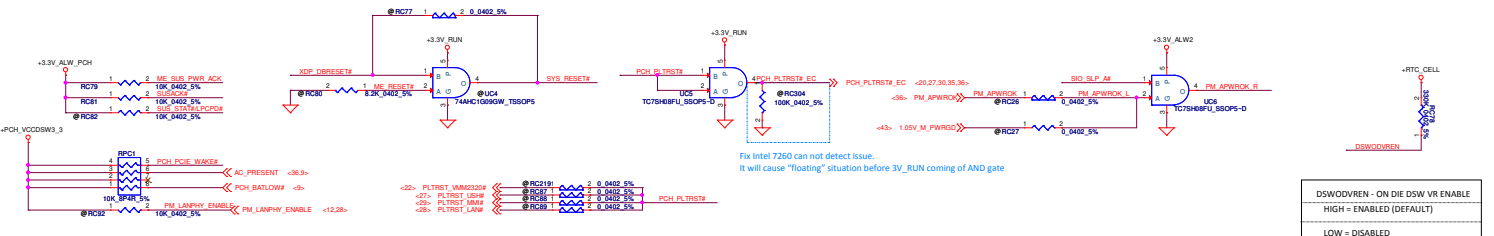
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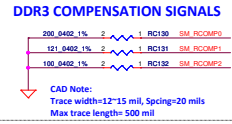
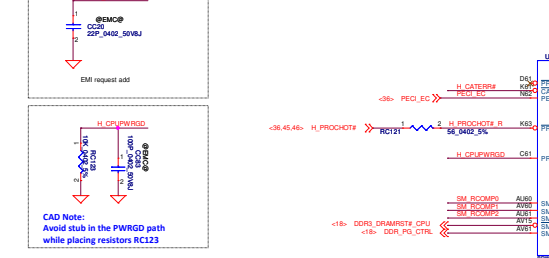
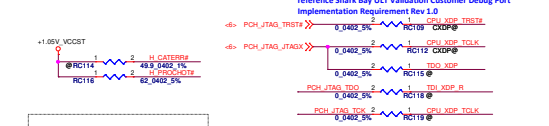
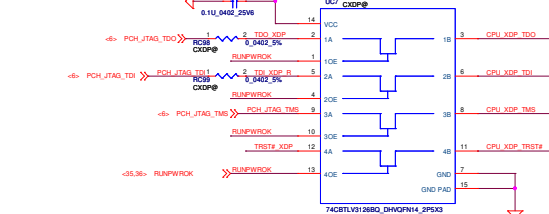
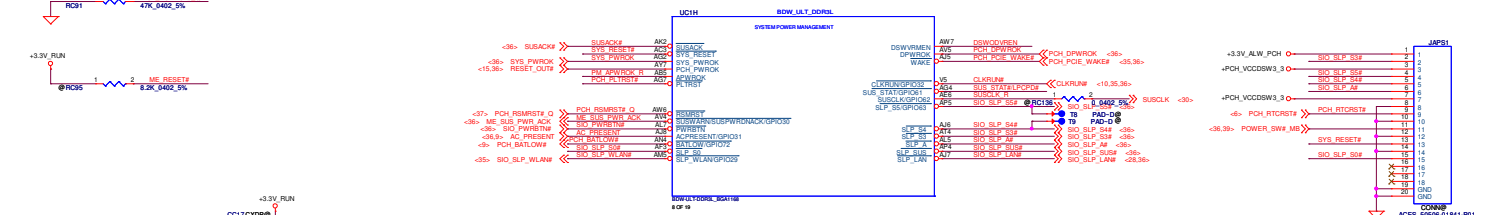
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Fix when 7250 can not detect issue. It will cause "floating" situation before 3V_RUN coming of AND gate

DSW00VREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED



DDR3 COMPENSATION SIGNALS
200 0402 1% 2 1 RC130 SM_RC0MP0
100 0402 1% 2 1 RC131 SM_RC0MP1
100 0402 1% 2 1 RC132 SM_RC0MP2

CAD Note:
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

EMI request add
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC123

CAD Note:
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

CAD Note:
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

CAD Note:
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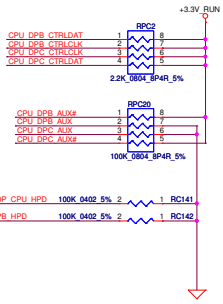
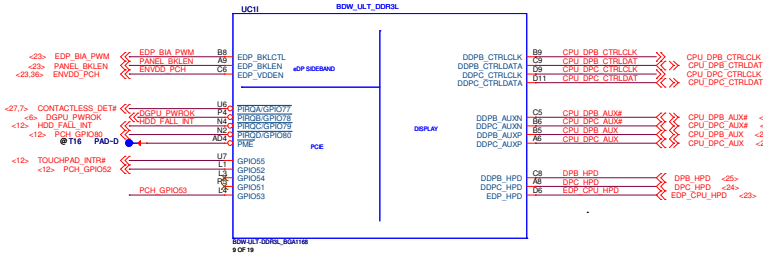
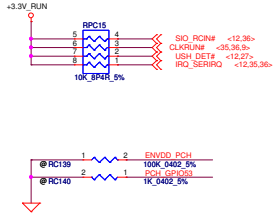
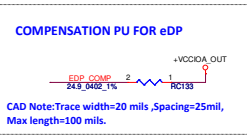
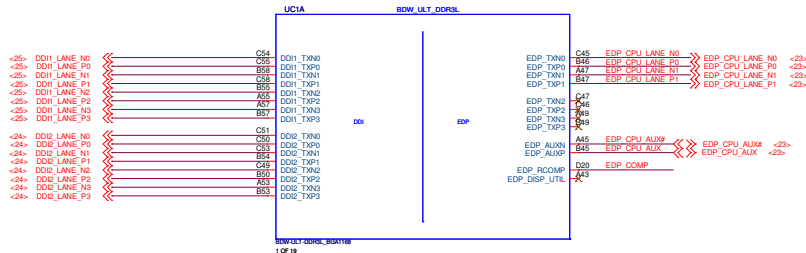
CAD Note:
Trace width=12-15 mil, Spacing=20 mils
Max trace length= 500 mil

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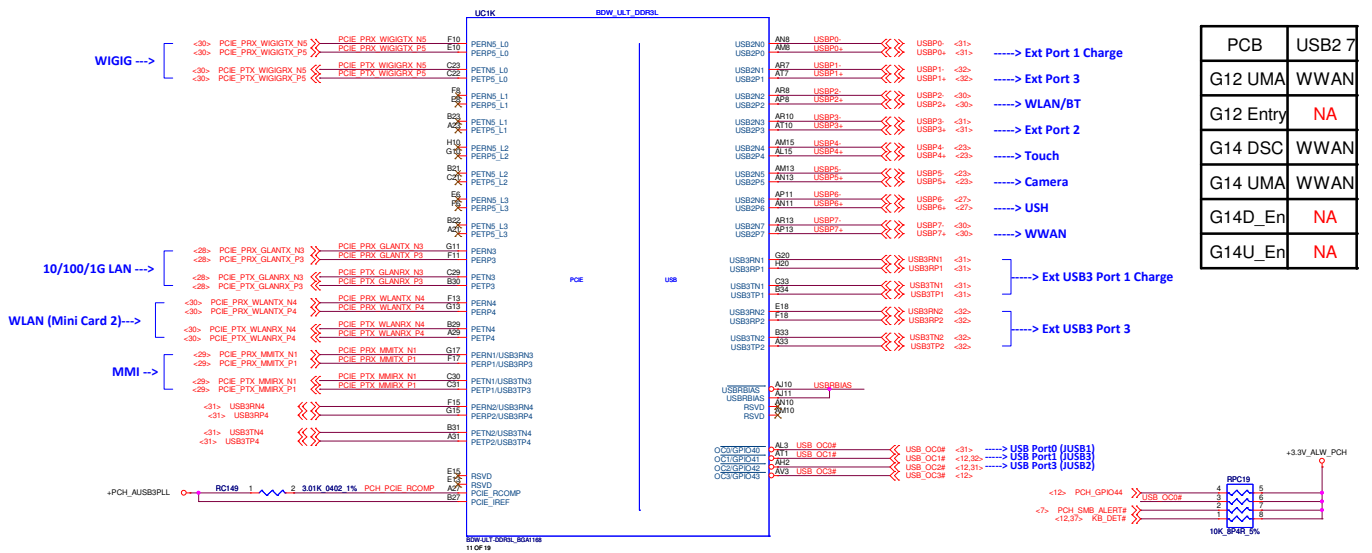
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CPU (5/12)

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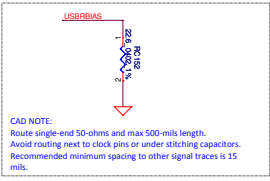
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PCIe for UMA



PCB	USB2 7
G12 UMA	WWAN
G12 Entry	NA
G14 DSC	WWAN
G14 UMA	WWAN
G14D_En	NA
G14U_En	NA

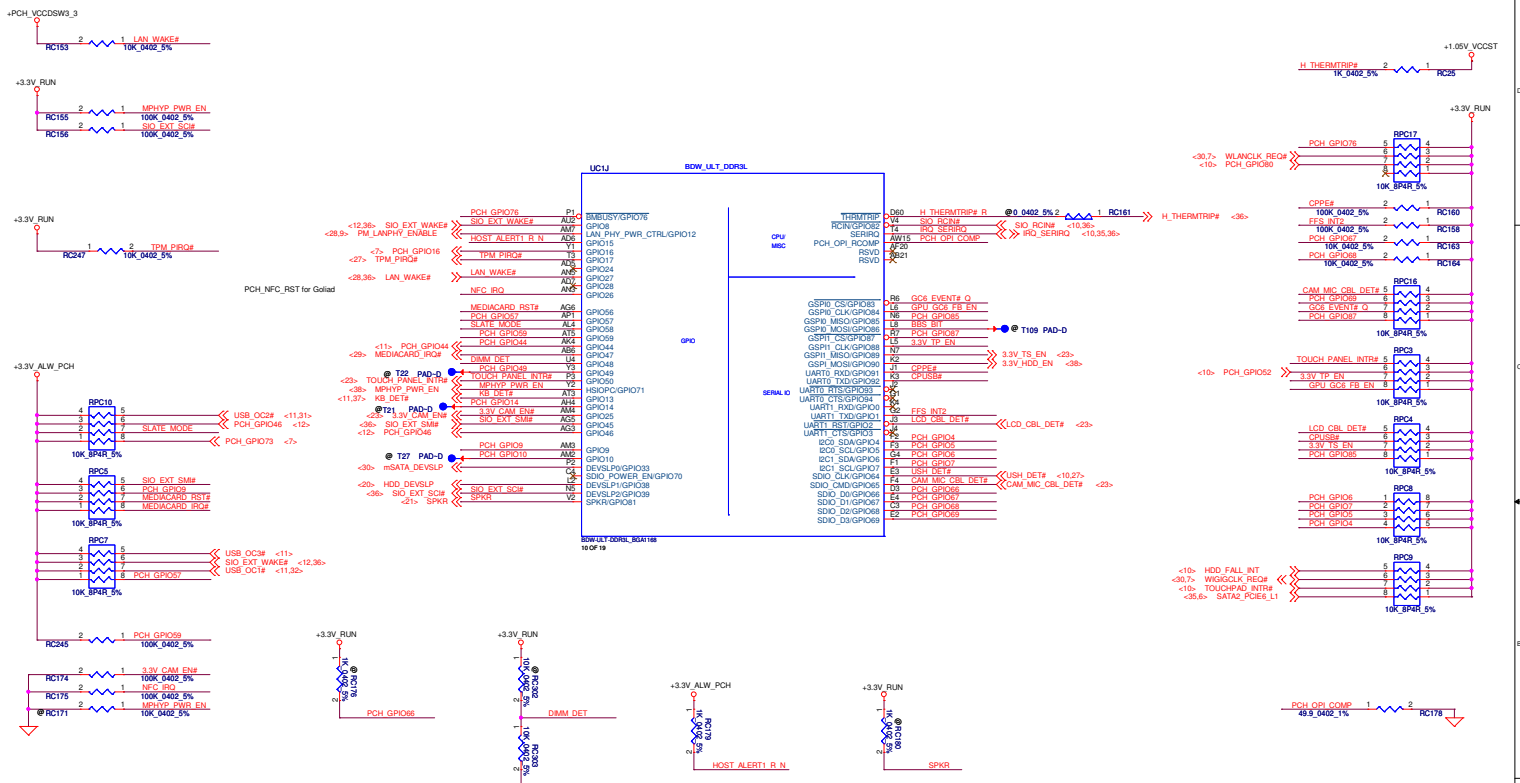
PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
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G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
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G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA



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TOP-BOARD SWAP OVERRIDE		DIMM Detect		TLS CONFIDENTIALITY		No Reboot on TCO Timer expiration	
HIGH	ENABLE	HIGH	1 DIMM	HIGH	ENABLE	HIGH	ENABLE
LOW(DEFAULT)	DISABLE	LOW	2 DIMM	LOW(DEFAULT)	DISABLE	LOW(DEFAULT)	DISABLE

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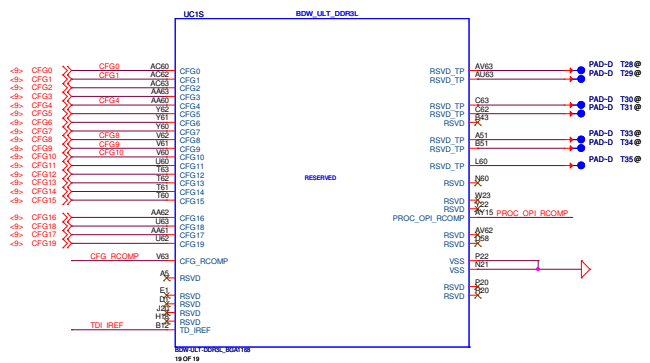
CPU (712)

LA-A971P

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CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked 0:Disable Noa will be available pegrardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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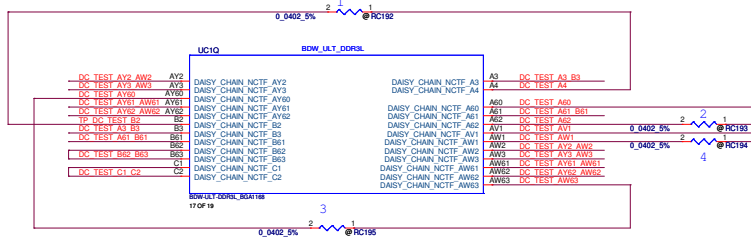
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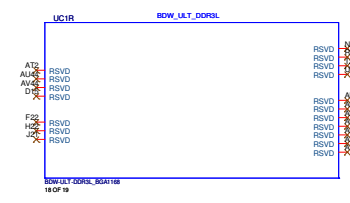
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- Package Daisy Chain:**
1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
 2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
 3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
 4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

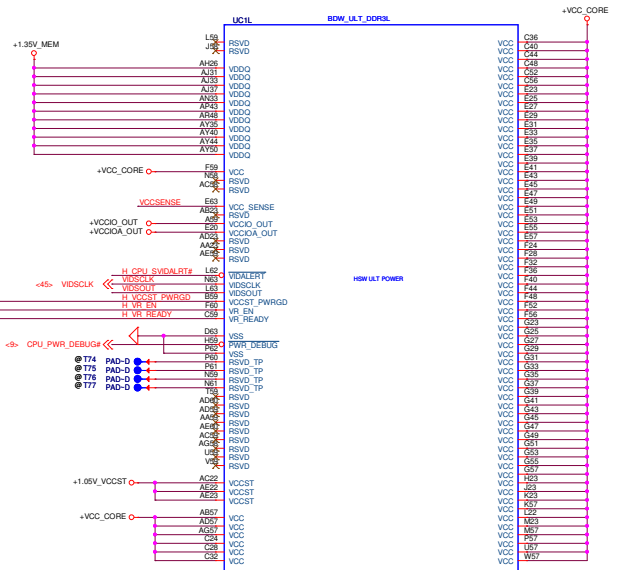
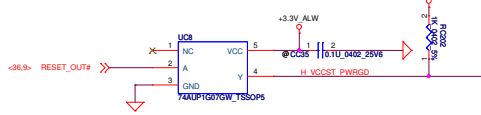
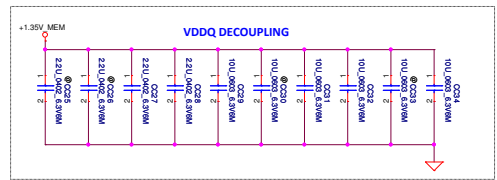
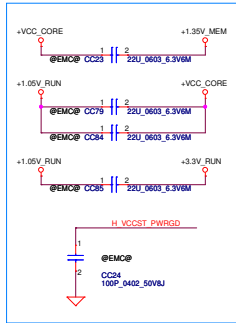
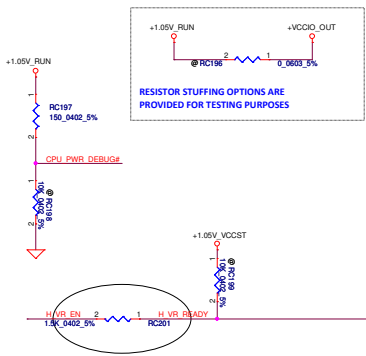


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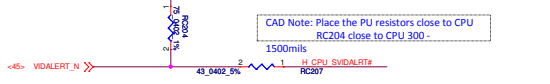
Compal Electronics, Inc.

File	CPU (9/12)		Rev	0.1
Size	Document Number	LA-A971P		
Date	Wednesday, March 19, 2014	Sheet	14	of 48

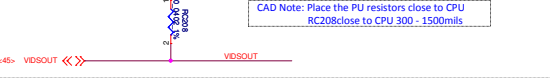
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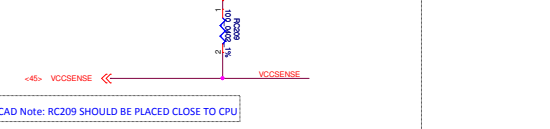
SVID ALERT



SVID DATA



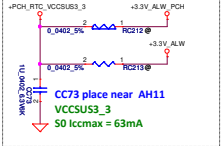
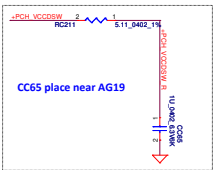
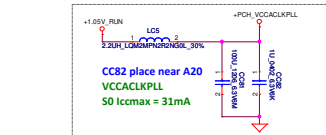
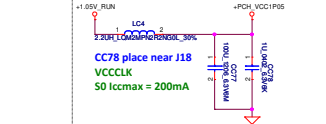
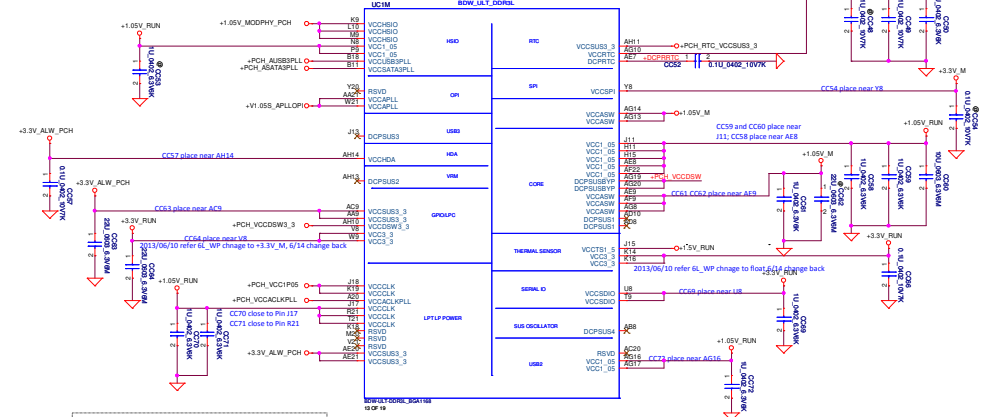
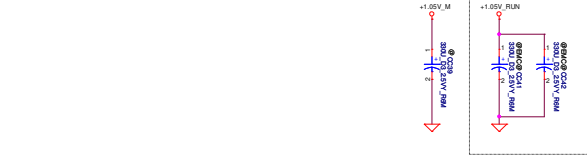
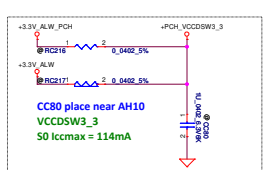
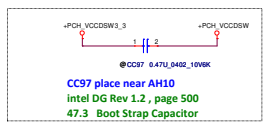
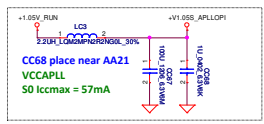
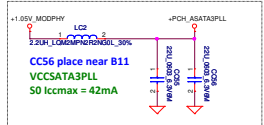
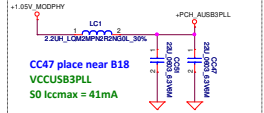
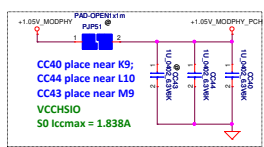
VCC_SENSE



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Voltage Rail	Voltage (V)	S0 Iccmax Current (A)	Sx Iccmax Current (A)	Deep-Sx Iccmax (A)	G3
VCCIO5 (Internal Suspend VR mode using HTVMMEN)	1.05	1.741	0	0	0
VCCIO3 (Internal Suspend VR mode using HTVMMEN)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCSIO	1.05	1.838	0	0	0
VCCSUS3_3	1.5	0.003	0	0	0
VCC1_3	3.3	0.041	0	0	0
VCCSIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSP	3.3	0.058	0	0	0
VCCBDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using HTVMMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using HTVMMEN)	3.3	0.062	0.005	0	0
DcpSus1*	1.05	0.109	0.014	0	0
DcpSus2*	1.05	0.025	0.001	0	0
DcpSus3*	1.05	0.010	0.001	0	0
DcpSus4*	1.05	0.001	0.001	0	0
VCCDSW2_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	8 μ A See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interface (power rail isolation required)	PCH Pins sharing power rail
V1.05v	Core	J11, H11, H15, A81, AF22
	DIE	RA21, W21
	HSD	K9, L10, M1, P9, B18, B11, M9
	USB2	AG16, AG17
	CLK(A)	A20
V3.3v	CLK(A)	B21, Y21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3v	LPD	ACE, A85, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3v	GPD	W8, W9
	USD	U8, T9
	Thermal Sensor	K14, K15

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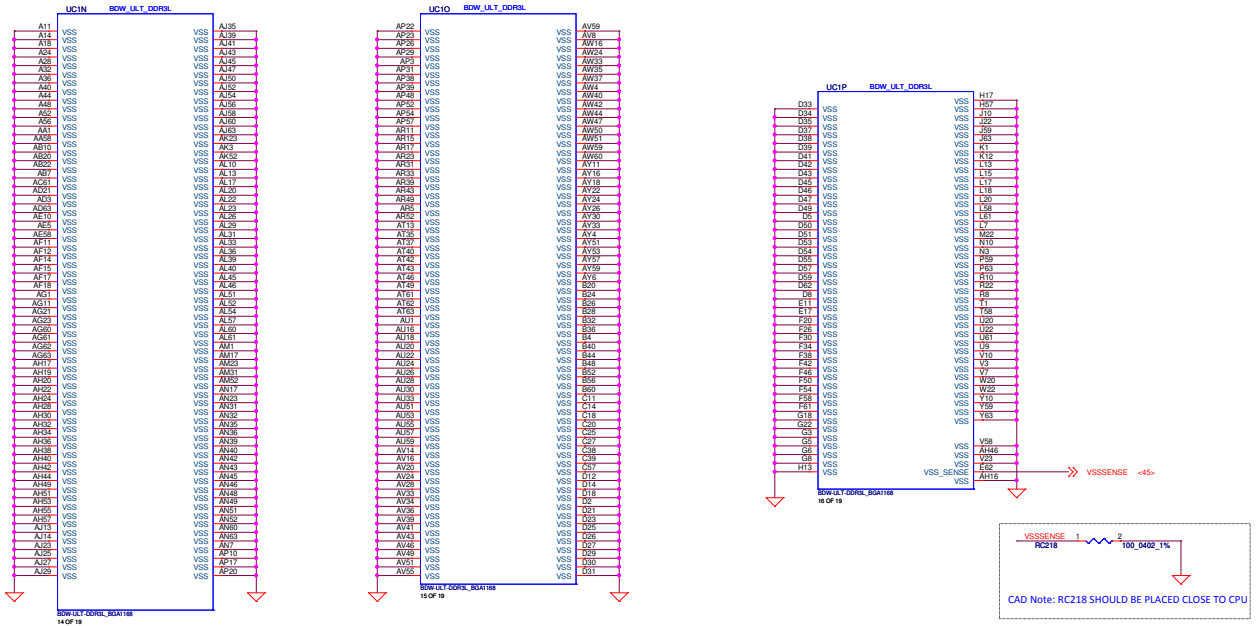
Compal Electronics, Inc.

File: **CPU (11/12)**

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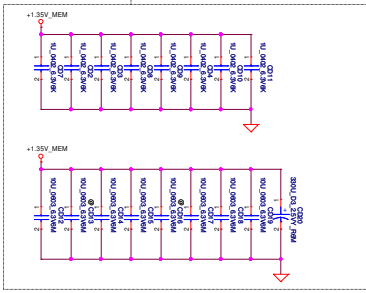
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Compal Electronics, Inc.	
CPU (12/12)	
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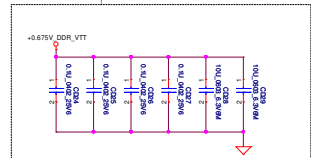
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- DDR_A_DQS[0-7]
- DDR_A_DS[0-63]
- DDR_A_DQS[0-7]
- DDR_A_M[0-15]

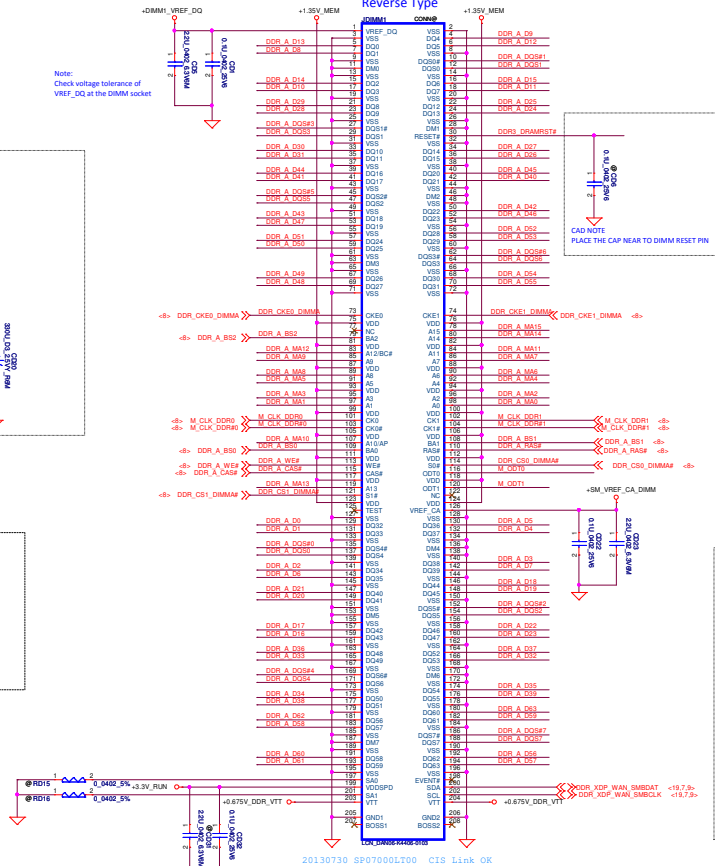
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203_204



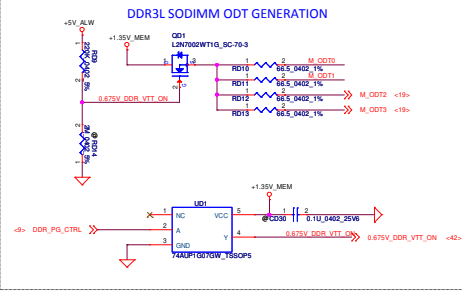
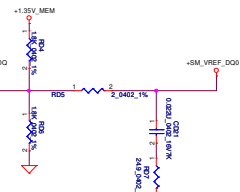
H=4mm Reverse Type



Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAI NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3_DRAMRST# CPU



20130730 SP07000LTD0 CIS Link OK

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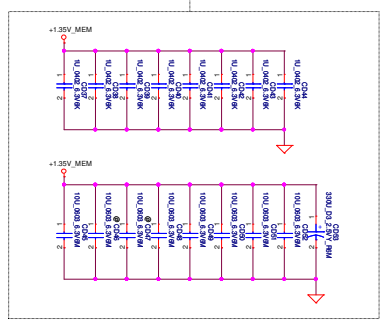
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Compaq Electronics, Inc.
LA-A971P
Doc: W0020557, M00315, 0114 Sheet 18 of 48

H=4mm
Reverse Type

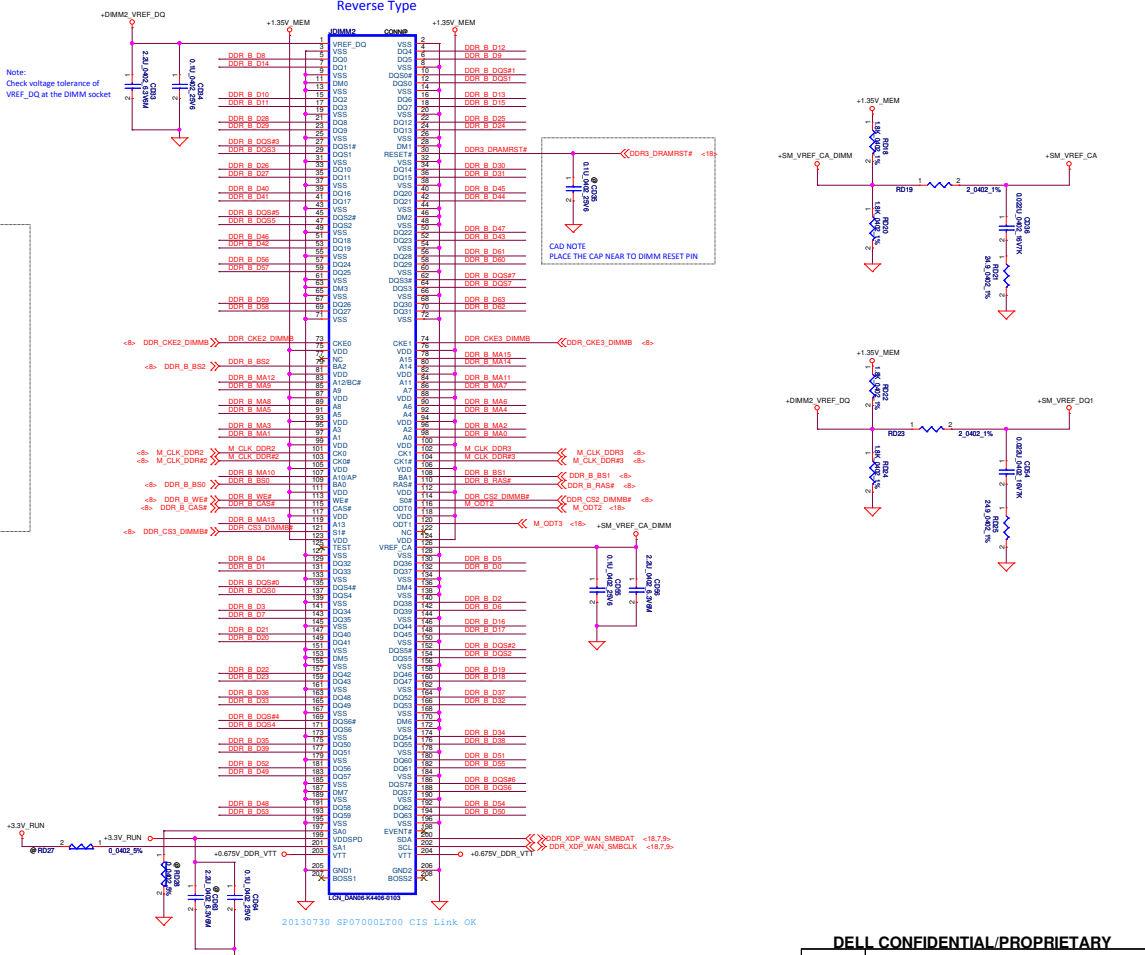
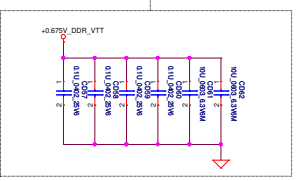
- <-> DDR_B_D0S4E-7
- <-> DDR_B_D0E-7
- <-> DDR_B_D0S0-7
- <-> DDR_B_MAP-1E

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



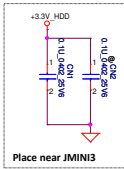
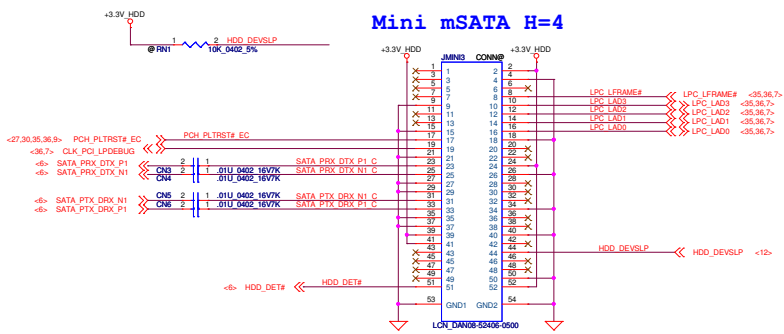
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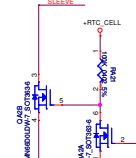
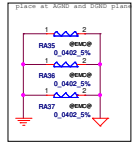
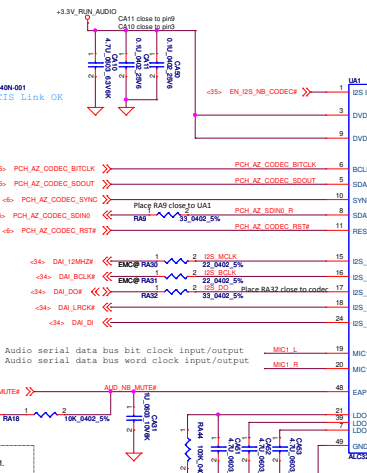
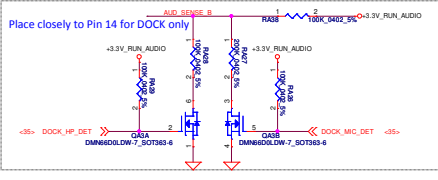
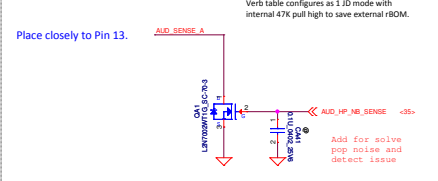
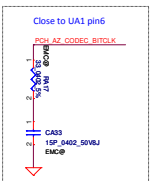
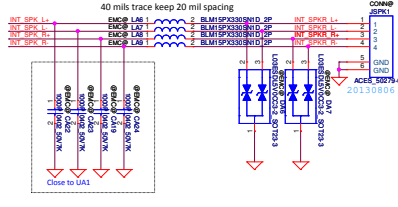
Compal Electronics, Inc.



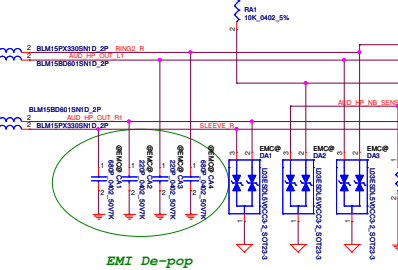
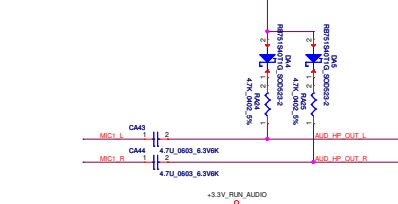
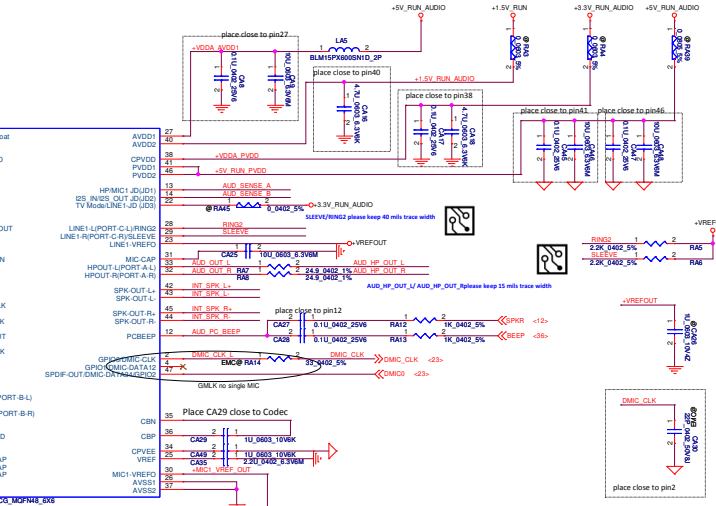
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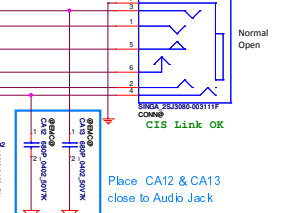
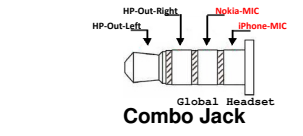
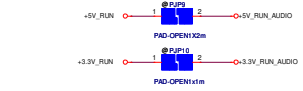
Internal Speakers Header



Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 / S5



EMI De-pop



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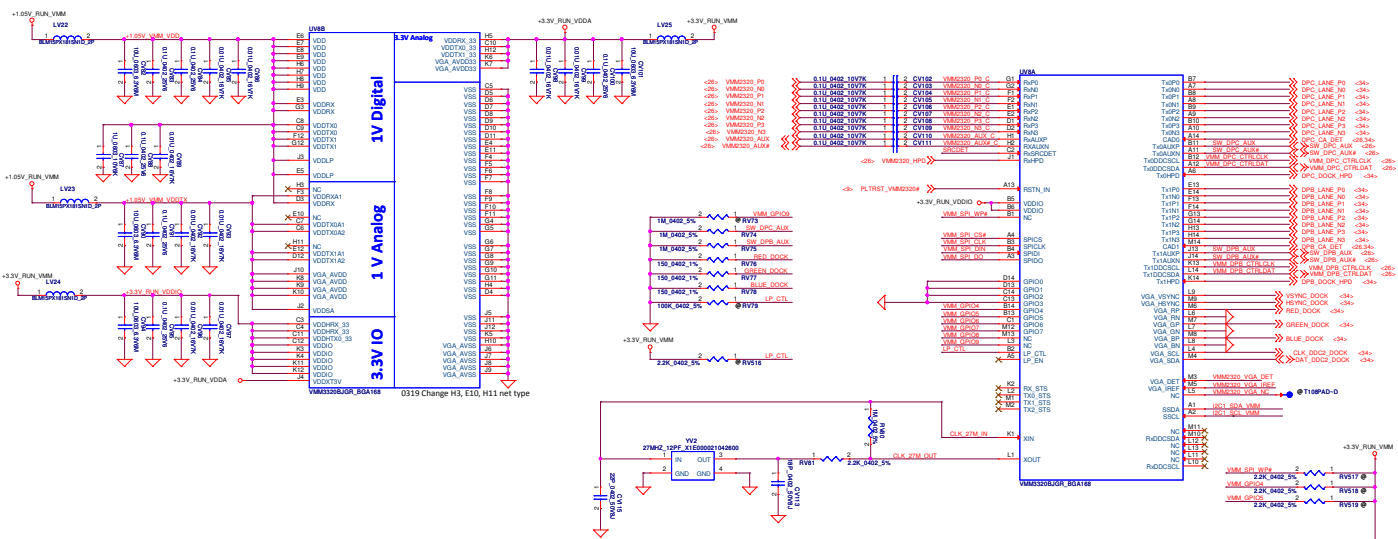
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Doc# LA-A971P

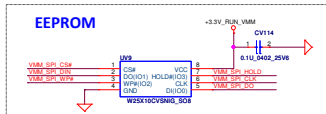
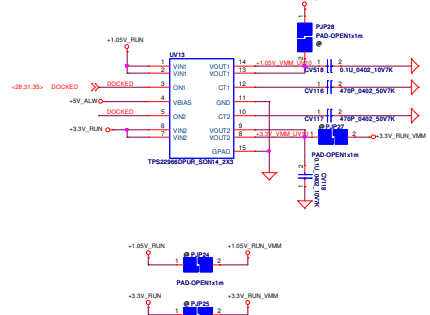
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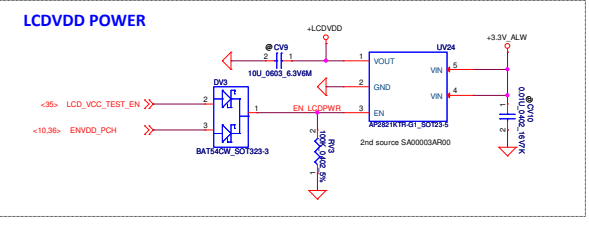
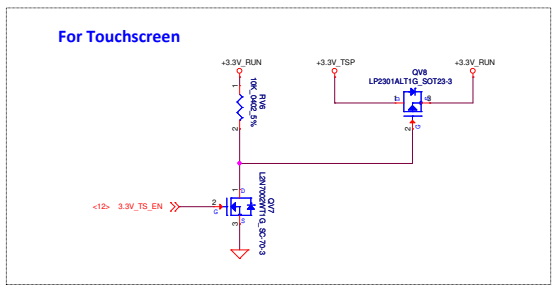
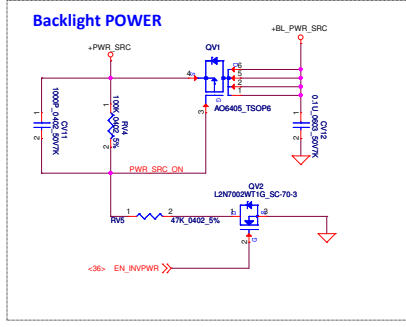
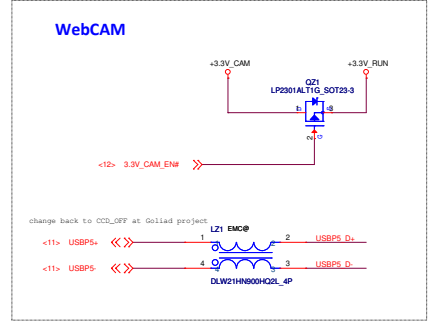
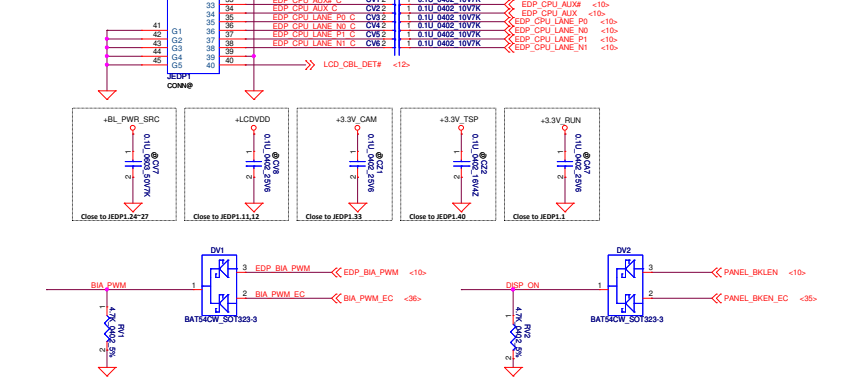
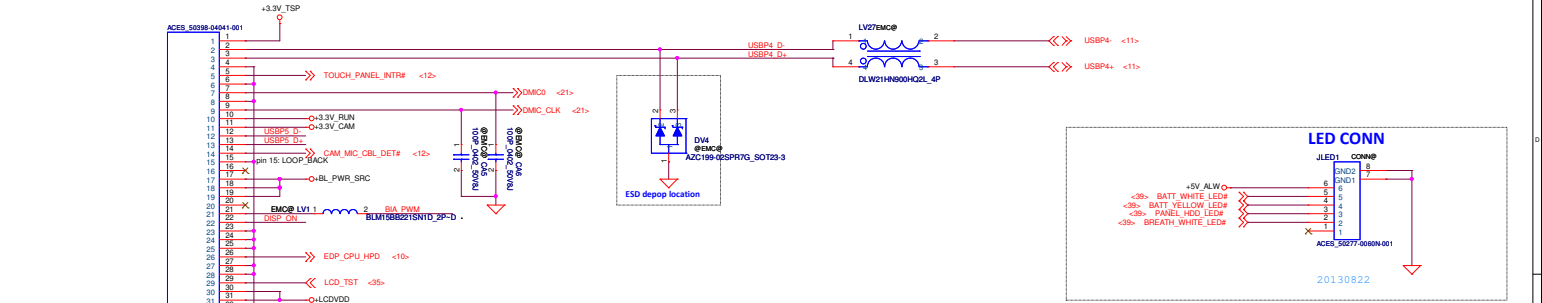
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**Goliad MLK should use DOCKED to control TPS22966
Huston 14"/15" use jumper**

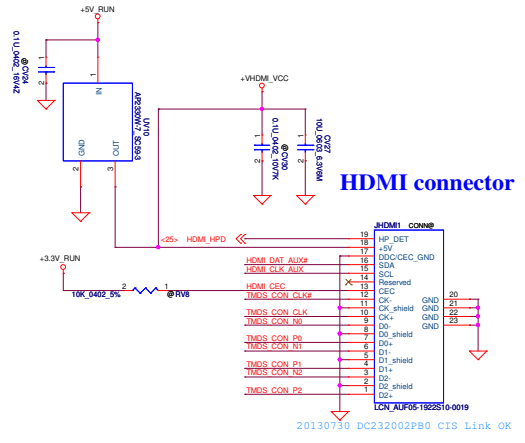
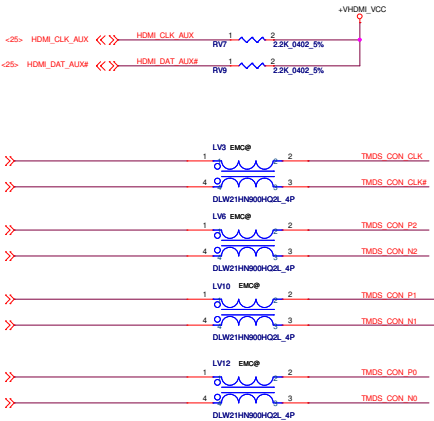


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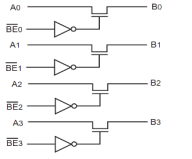


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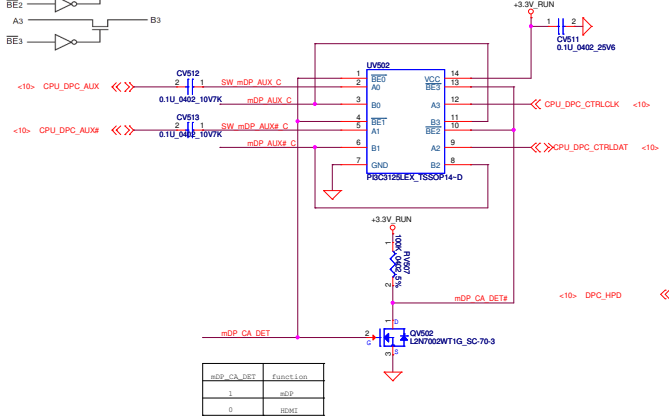
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Compal Electronics, Inc.
eDP CONN & Touch screen
LA-A971P
 Wednesday, March 19, 2014 Sheet 23 of 48



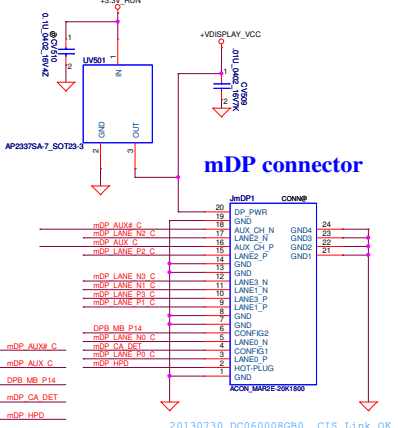
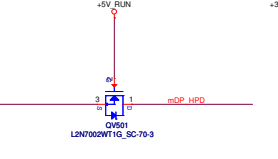
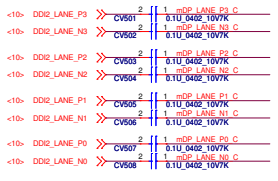
20130730 DC232002P80 CIS Link OK
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AUX/DDC SW for DDI2 to Mini DP



mDP_CA_DET	Function
1	mDP
0	BIOS



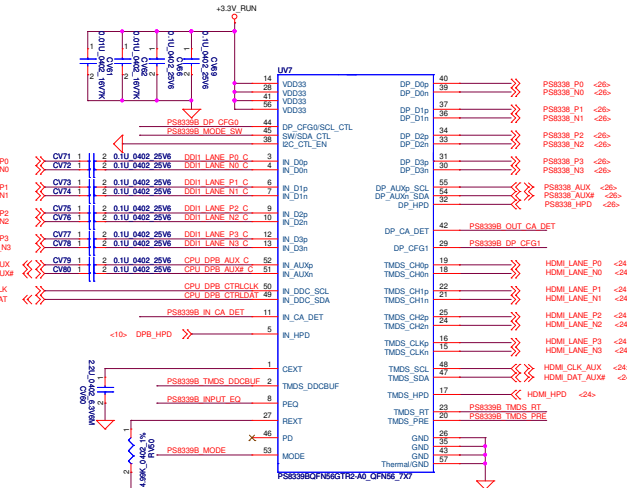
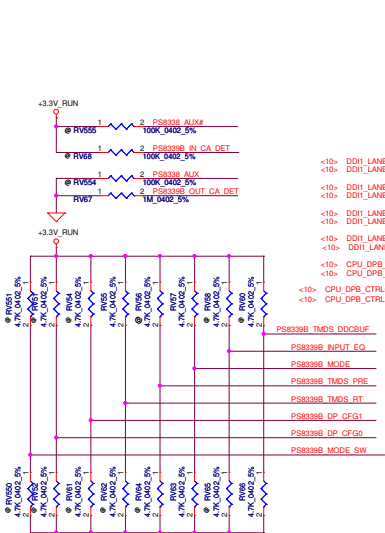
20130730 DC060008G80 CIS Link OK

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		Compal Electronics, Inc.	
HDMI CONN		LA-A971P	
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PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



DP_Dn0	40	PS8338_P0	<26>
DP_Dn1	39	PS8338_N0	<26>
DP_Dp0	38	PS8338_P1	<26>
DP_Dp1	37	PS8338_N1	<26>
DP_Dn2	36	PS8338_P2	<26>
DP_Dn3	35	PS8338_N2	<26>
DP_Dp2	34	PS8338_P3	<26>
DP_Dp3	33	PS8338_N3	<26>
DP_AUX0_SDA	55	PS8338_AUX0	<26>
DP_AUX1_SDA	54	PS8338_AUX1	<26>
DP_HP0	32	PS8338_HP0	<26>
DP_CA_DET	42	PS8339_OUT_CA_DET	
DP_CFG1	29	PS8339_DP_CFG1	
TMDS_Ch0p	19	HDMI_LANE_P0	<24>
TMDS_Ch0n	18	HDMI_LANE_N0	<24>
TMDS_Ch1p	21	HDMI_LANE_P1	<24>
TMDS_Ch1n	20	HDMI_LANE_N1	<24>
TMDS_Ch2p	23	HDMI_LANE_P2	<24>
TMDS_Ch2n	22	HDMI_LANE_N2	<24>
TMDS_Ch3p	16	HDMI_LANE_P3	<24>
TMDS_Ch3n	15	HDMI_LANE_N3	<24>
TMDS_SCL	48	HDMI_CLK_AUX	<24>
TMDS_SDA	27	HDMI_DAT_AUX0	<24>
TMDS_HPD	17	HDMI_HPD	<24>
TMDS_RT	23	PS8339_TMDS_RT	
TMDS_PRE	20	PS8339_TMDS_PRE	
GND	26		
GND	35		
GND	41		
GND	57		

MODE = L: Control Switching Mode, HDMI ID disable
 = H: Automatic Switching Mode, HDMI ID disable
 = M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
 = H: 1.5dB pre-emphasis
 = M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
 = H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
 = H: DDC active buffer
 = M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 = H: HEQ, compensate channel loss up to 15dB @ HBR2
 = M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
 = H: auto test enable & input offset cancellation enable
 = M: auto test disable & input offset cancellation disable

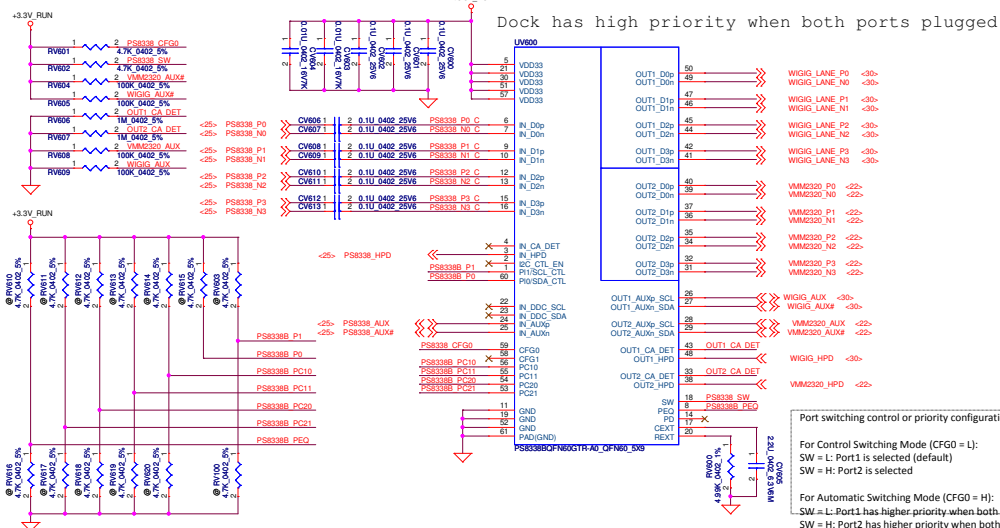
DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
 = H: automatic EQ disable & AUX interception enable
 = M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

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Compal Electronics, Inc.	
DP SW	
Doc Number	LA-A971P
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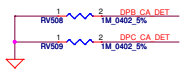
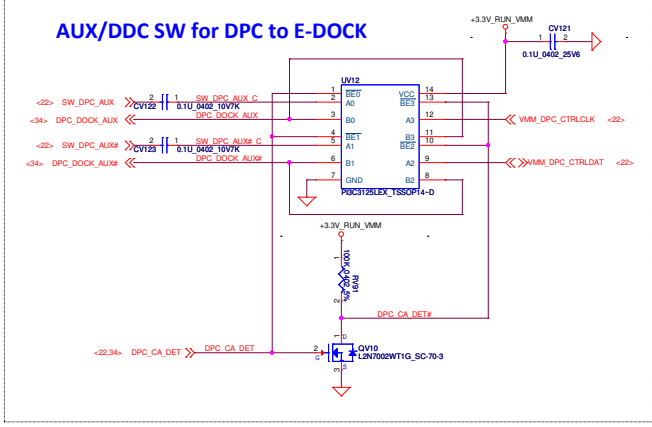
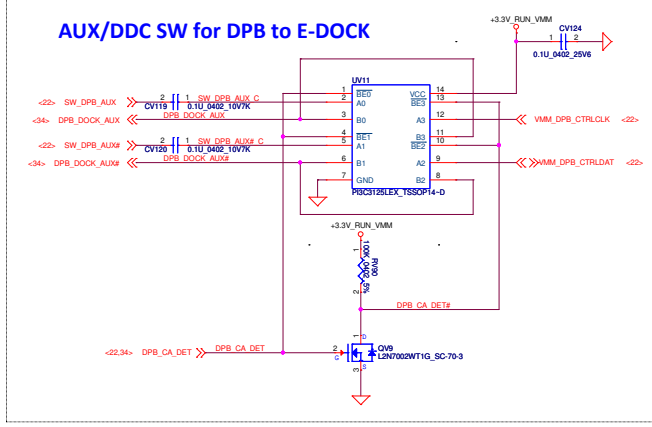
PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



Port switching control or priority configuration. Internal pull down ~150kΩ, 3.3V I/O

For Control Switching Mode (CFG0 = L):
 SW = L: Port1 is selected (default)
 SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H):
 SW = L: Port1 has higher priority when both ports are plugged (default)
 SW = H: Port2 has higher priority when both ports are plugged



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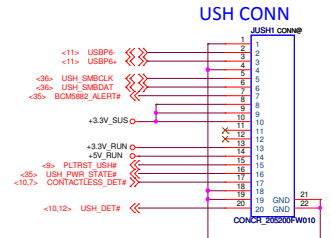
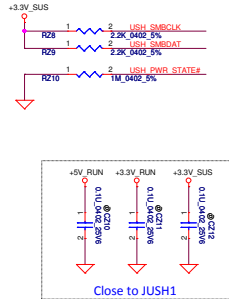
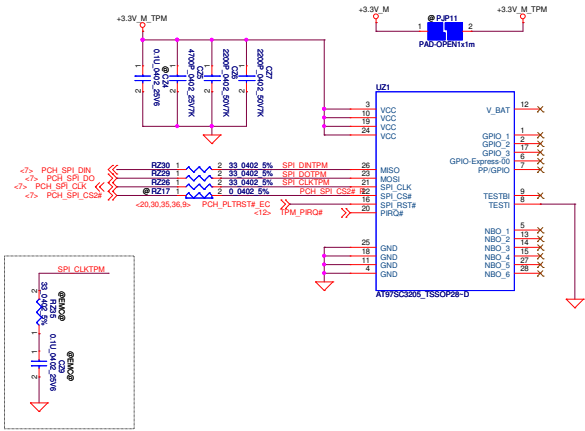
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Compal Electronics, Inc.

DP SW

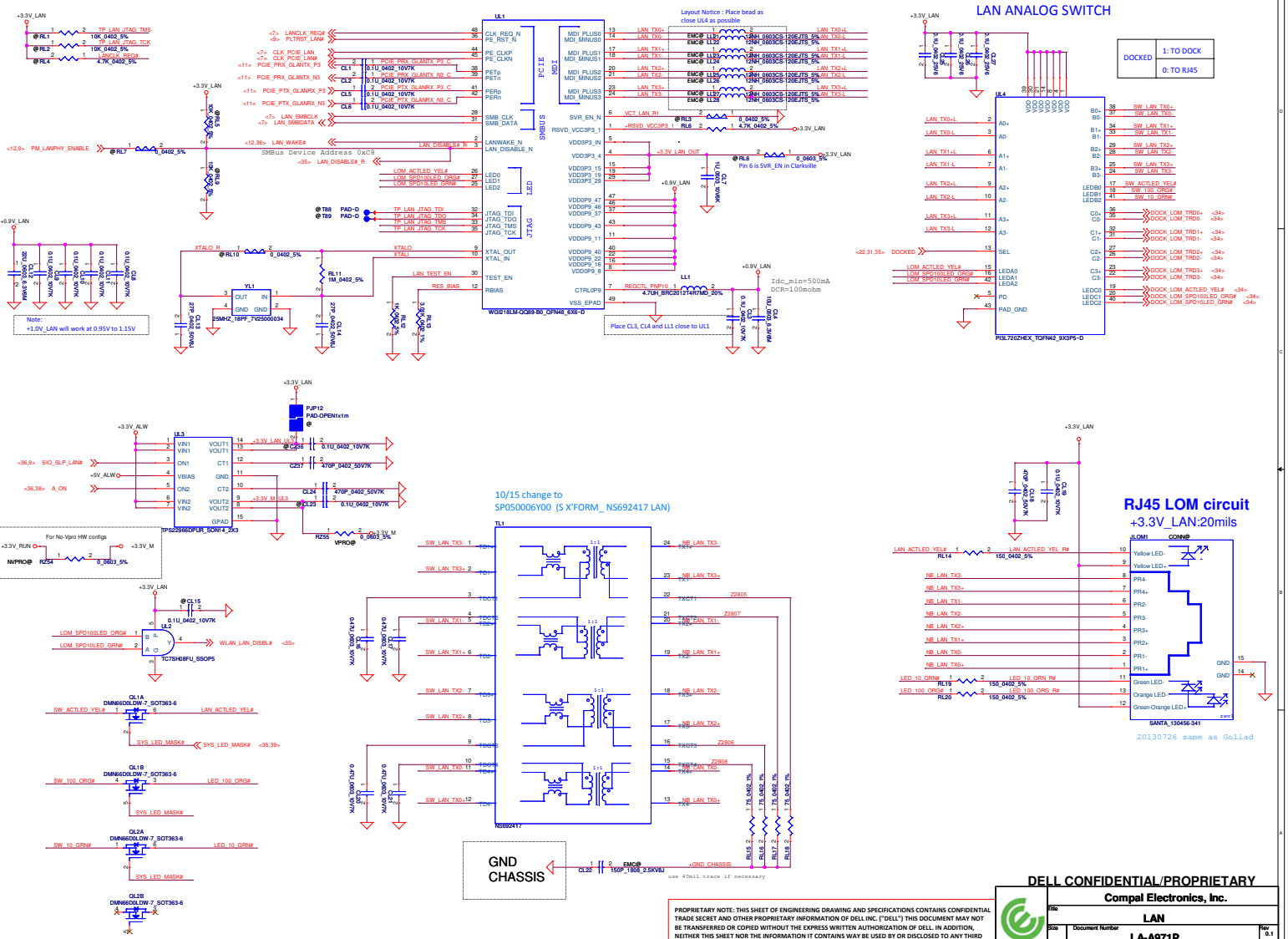
LA-A971P

File: DP SW
 Size: Document Number
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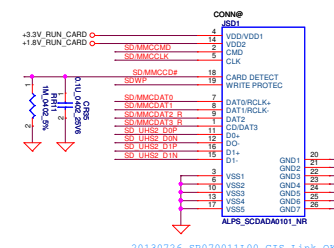
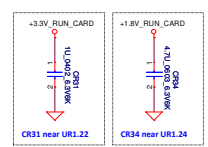
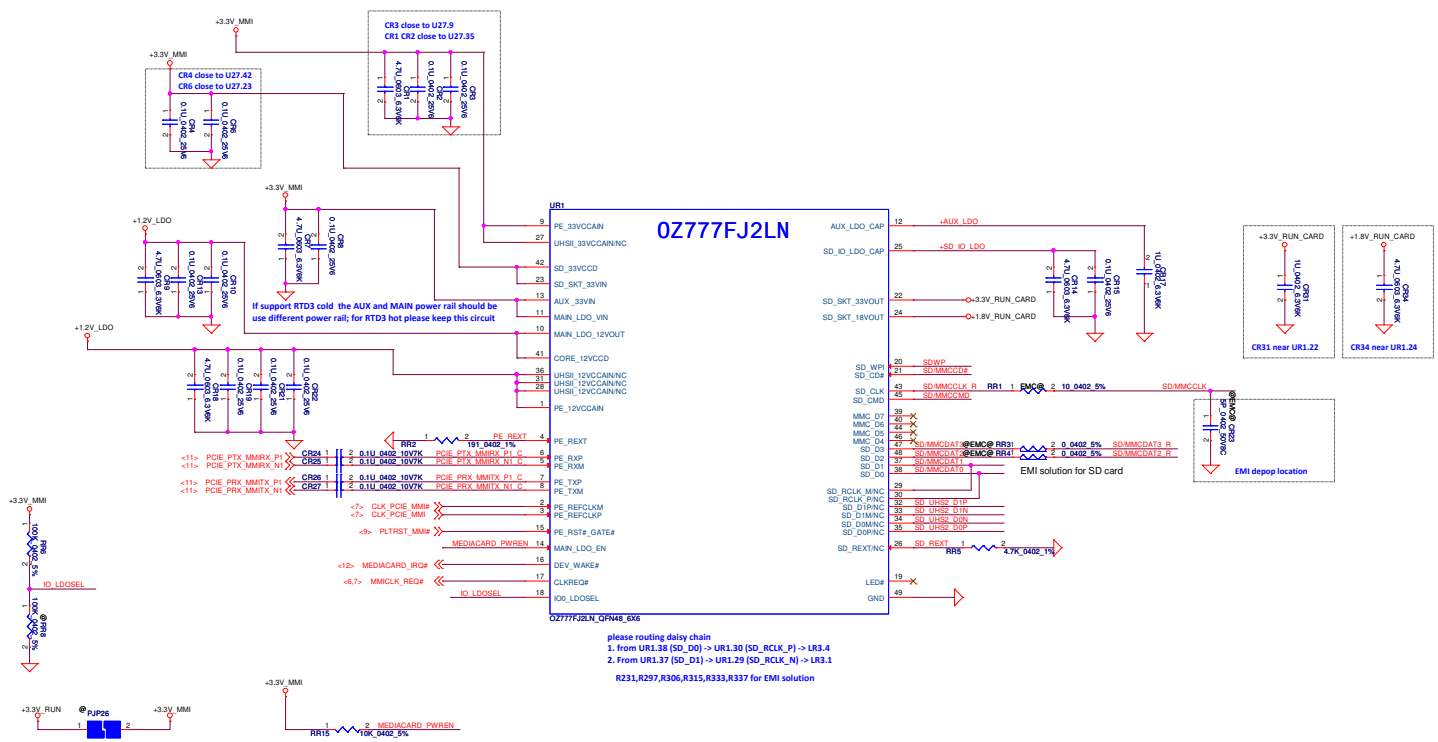


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USH & TPM
LA-A971P
 Date: Wednesday, March 19, 2014 Sheet 27 of 48 Rev 0.1



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Part	LA-A971P	Sheet	38 of 45



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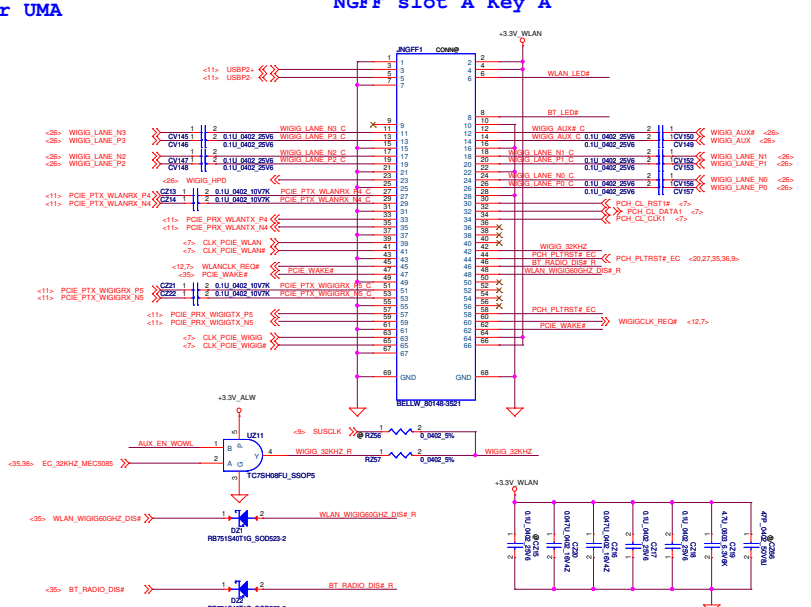
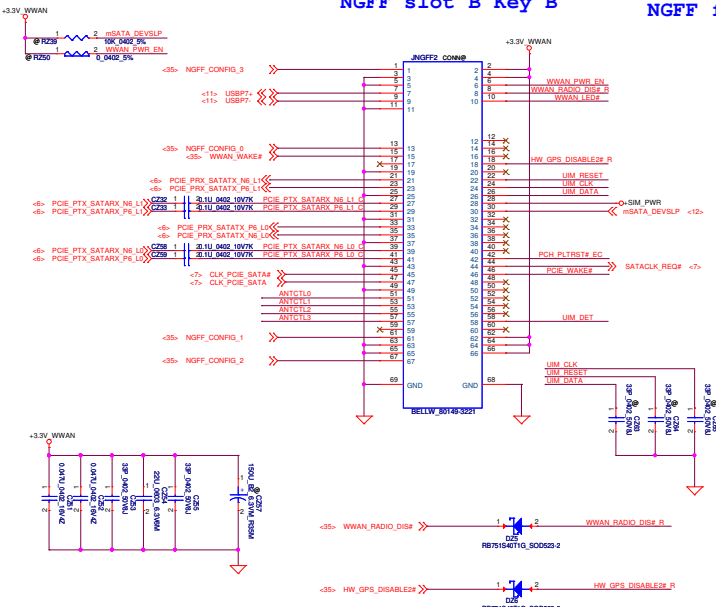
Compal Electronics, Inc.	
File	Card Reader
Size	Document Number
Date	LA-A971P
Rev	0.1
Date	Wednesday, March 13, 2014
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NGFF slot B Key B

NGFF for UMA

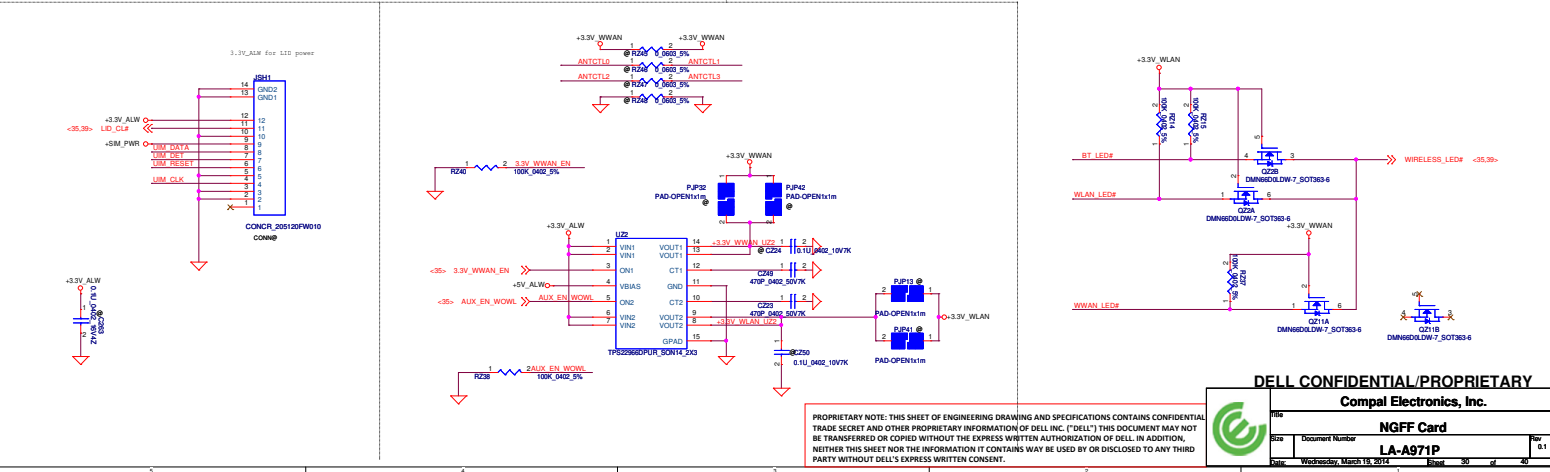
NGFF slot A Key A



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

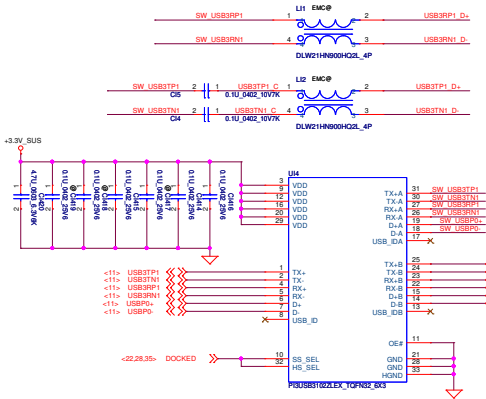
PWR Rail	Voltage Tolerance	Primary Power	Aux Power
+3.3V		Peak	Normal

LED control circuit



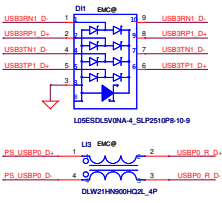
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 Compaq Electronics, Inc.
NGFF Card
LA-A971P
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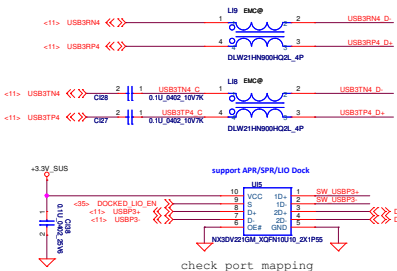
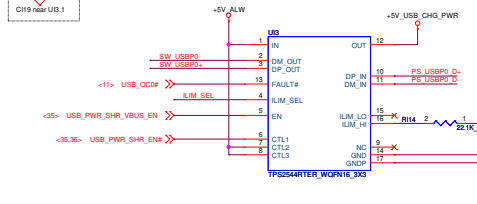
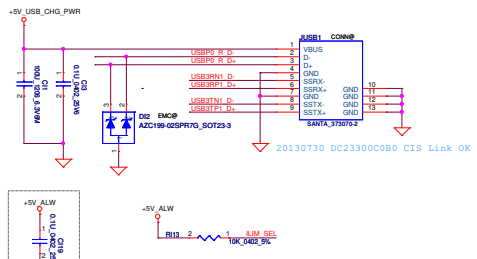


check port mapping

DOCKED	function
1	Dock
0	N/A

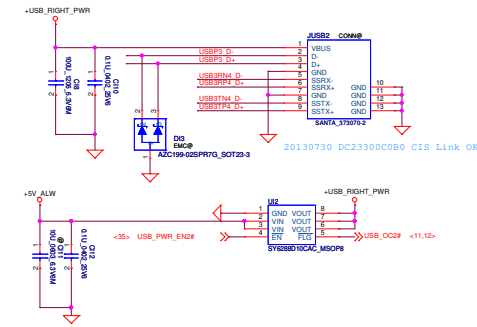
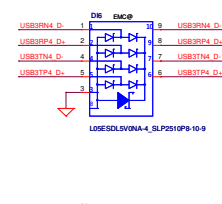


PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA



check port mapping

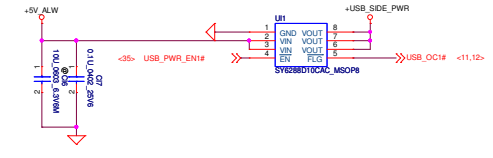
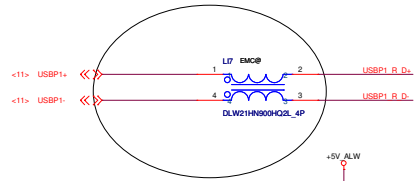
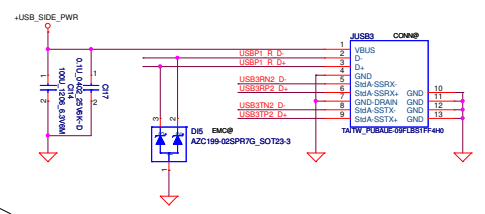
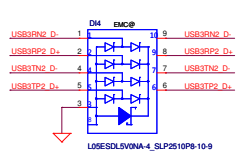
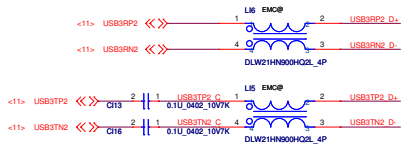
DOCKED	function
1	Dock
0	N/A



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USB3.0		Rev 01	
Size	Document Number	LA-A971P	
Rev	Microcode	March 18, 2014	Page 31 of 42




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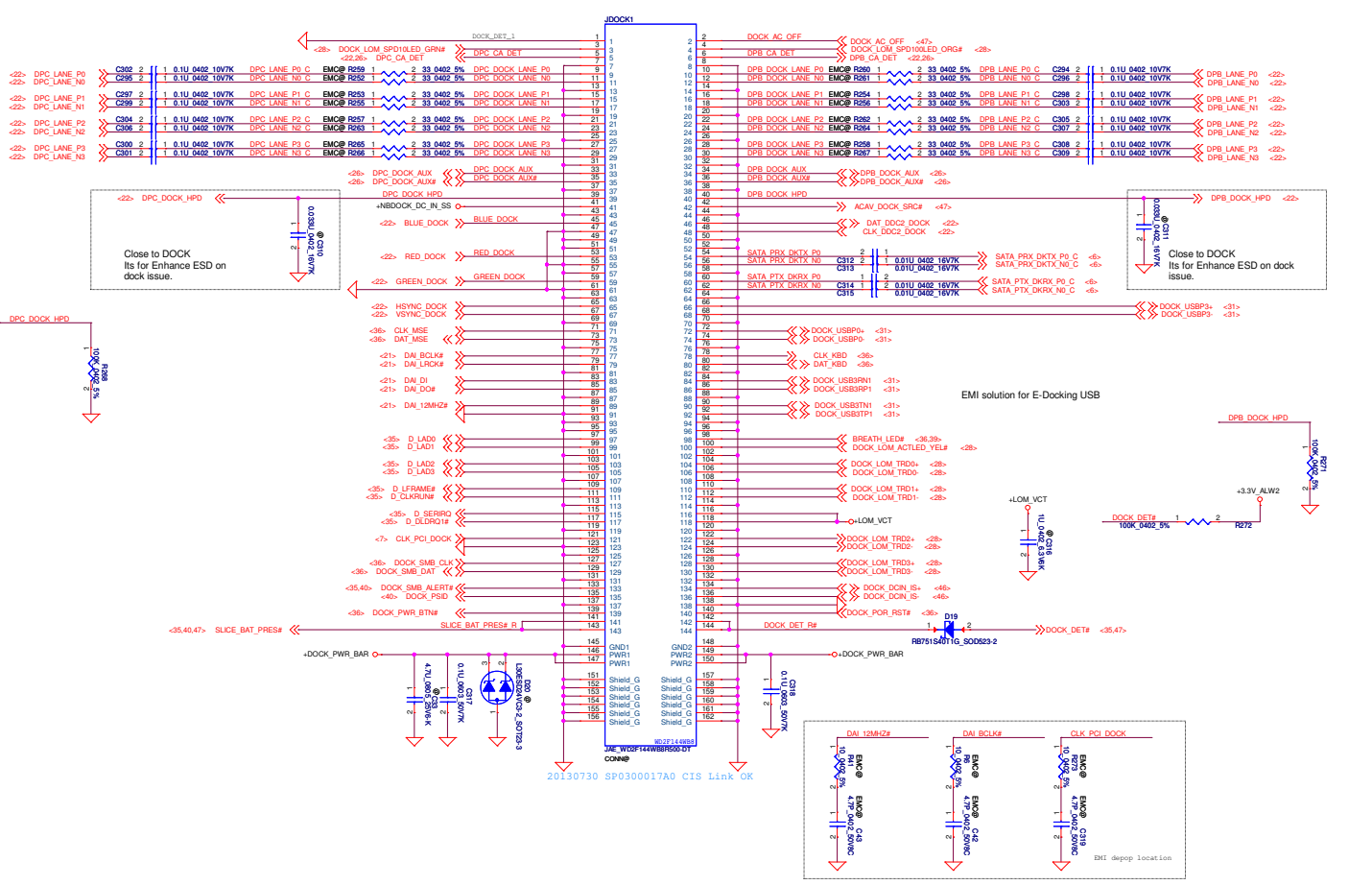
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		Compal Electronics, Inc.	
		USB SW	Rev 0.1
Size	Document Number	LA-A971P	Date: Wednesday, March 19, 2014
Sheet	of	48	

NFC on USH/B

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	File	
	Document Number	NFC
	Date	LA-A971P
	Wednesday, March 19, 2014	Sheet 33 of 48

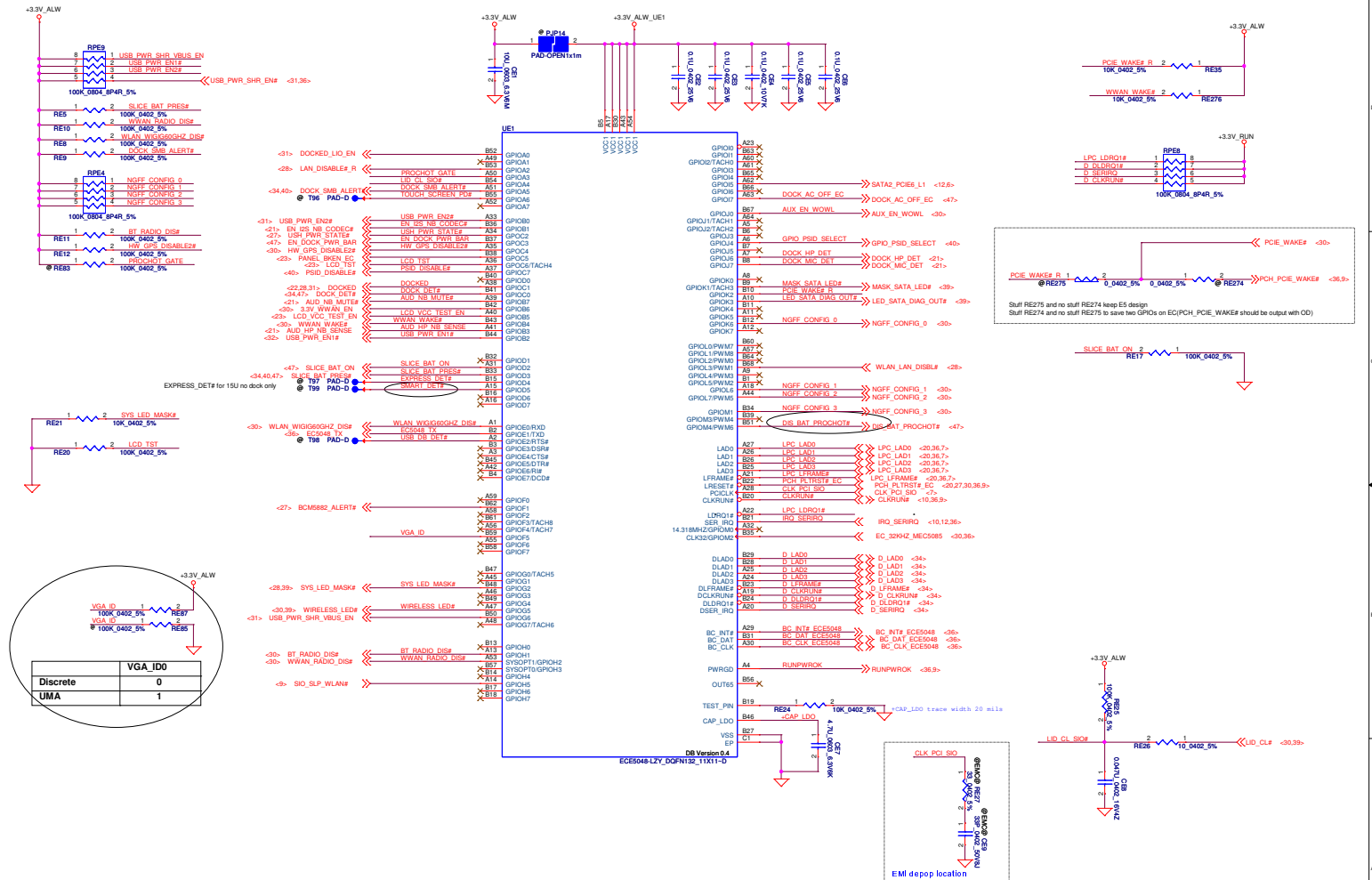


20130730 SP0300017A0 CIS Link OK

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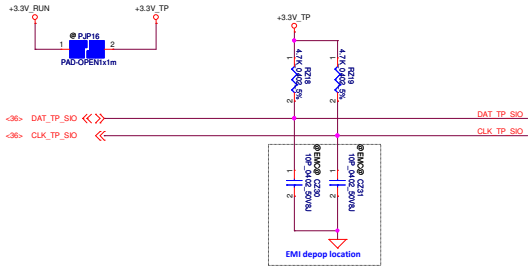
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Doc Number		LA-A971P	
Date	Wednesday, March 19, 2014	Sheet	34 of 48



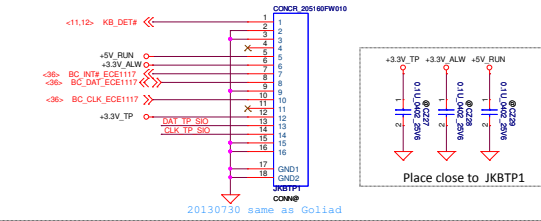
DELL CONFIDENTIAL/PROPRIETARY
 Compal Electronics, Inc.
 File: ECE5048
 Size: Document Number
 Date: Wednesday, March 13, 2014 Sheet 35 of 48
 LA-A971P Rev 0.1

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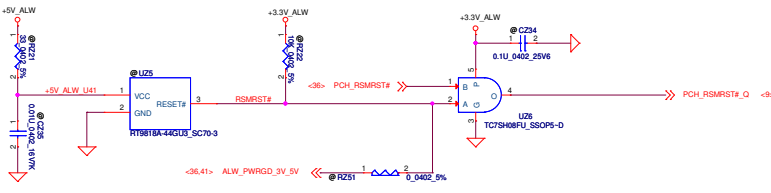
Touch Pad



Keyboard



RSMRST circuit



Part Number	Description
DA30505020	FPC 0VW LP-9591P MEVO H/8-10/B
DC02C004900	R-COMN SET 0VW MB-LD+LED-CAM-TS
DC02C004700	R-COMN SET 0VW MB-LD+LED-CAM
DC02C004800	R-COMN SET 0VW MB-HBD
DC30100M000	CONN SET 0VW DC3ACR-MB 22M1003-038110F
DC30100M000	CONN SET 0VW DC3ACR-MB 22M1003-038110F
DC28A000800	FAN SET DAQ25 DC5V AB74058B-MB3 A20A

Part Number	Description
NBK0001C0W00	FPC 6P G P0.5 PAD0.3 50MM MB-MEDIA/B 0/H
NBK0001C2000	FPC 15P G P.5 PAD.3 85MM MB-SPC M200 0/H
NBK0001C2000	FPC 15P G P.5 PAD.3 85MM MB-SPC M200 0/H
NBK0001C2000	FPC 15P G P.5 PAD.3 85MM MB-SPC M200 0/H
NBK0001D1000	FPC 6P G P0.5 PAD0.3 75MM USB/B-PP 0VW
PK230003Q0L	SPK PACK 2.5X 2.0X 4 08M PD

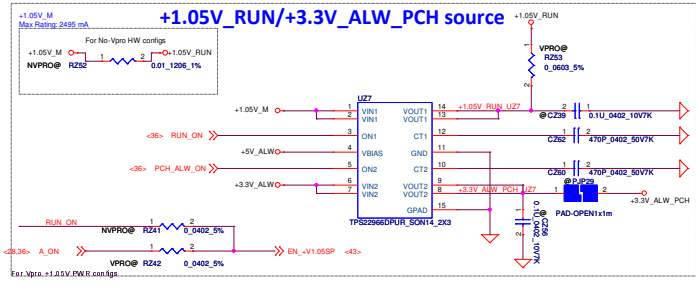
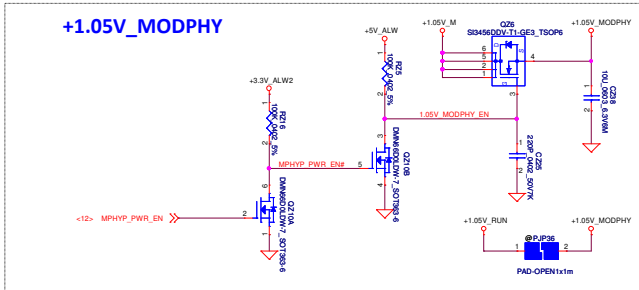
Part Number	Description
TC93H08FU_SSC0P5-D	

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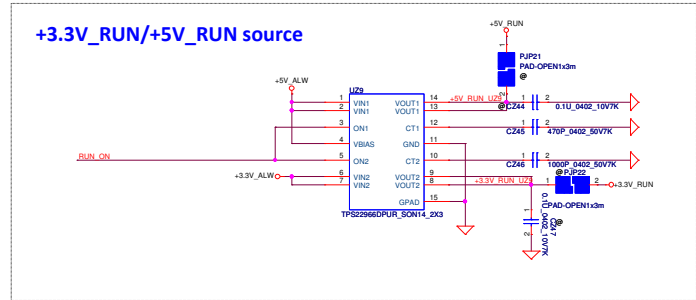
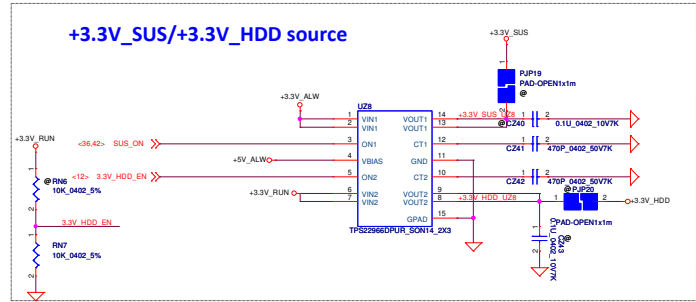
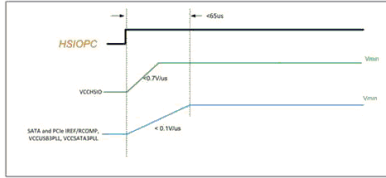
Compal Electronics, Inc.

File	Keyboard
Size	Document Number
LA-A971P	
Date	Wednesday, March 19, 2014
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if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



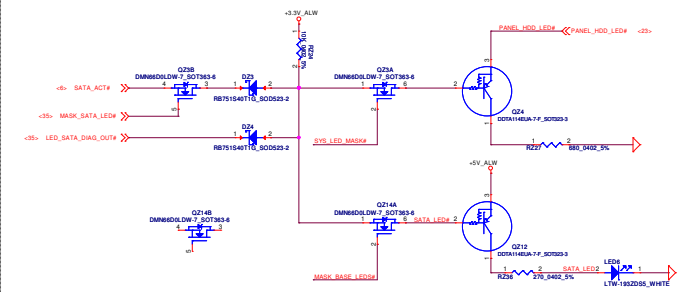
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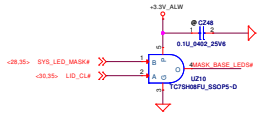
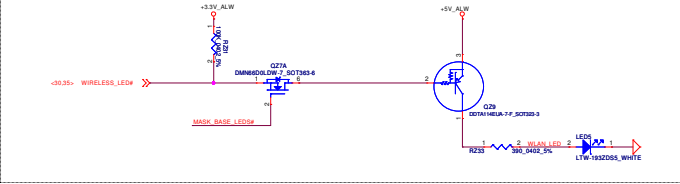
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File		Power control	
Size	Document Number	LA-A971P	
Date	Wednesday, March 18, 2015	Sheet	38 of 48

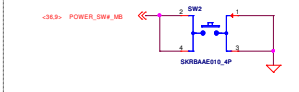
HDD LED solution for White LED



WLAN LED solution for White LED



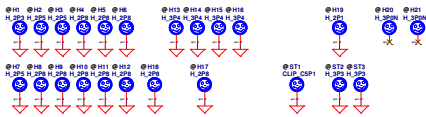
POWER & INSTANT ON SWITCH



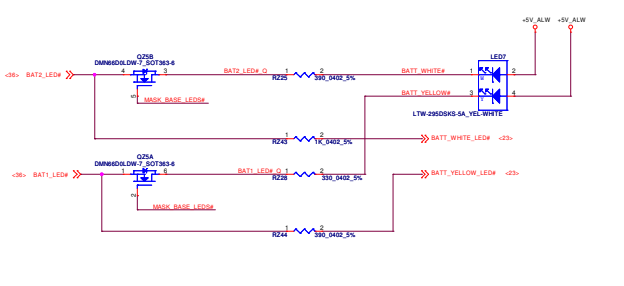
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

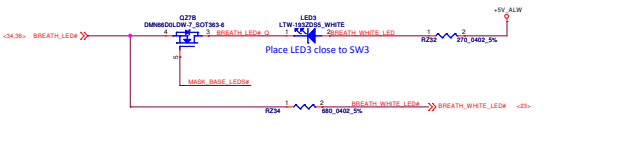
- Fiducial Mark**
- ⊙ F01
 - ✕ F02
 - F03
 - ✕ F04
- FIDUCIAL MARK-O
- FIDUCIAL MARK-X
- FIDUCIAL MARK-O
- FIDUCIAL MARK-X
- FIDUCIAL MARK-O
- FIDUCIAL MARK-X



Battery LED



Breath LED



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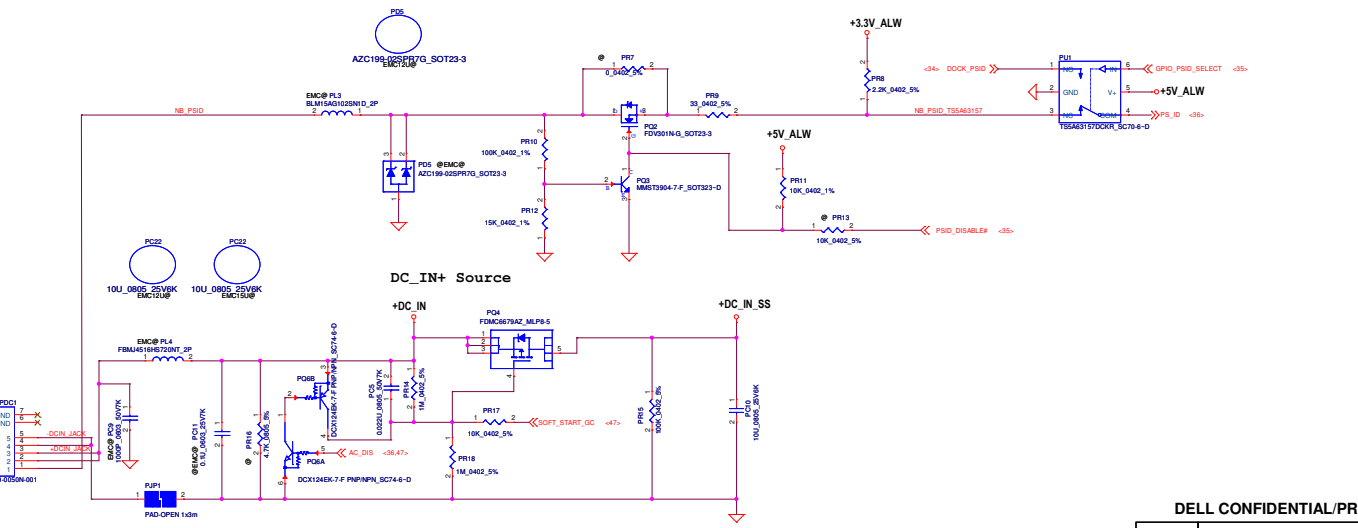
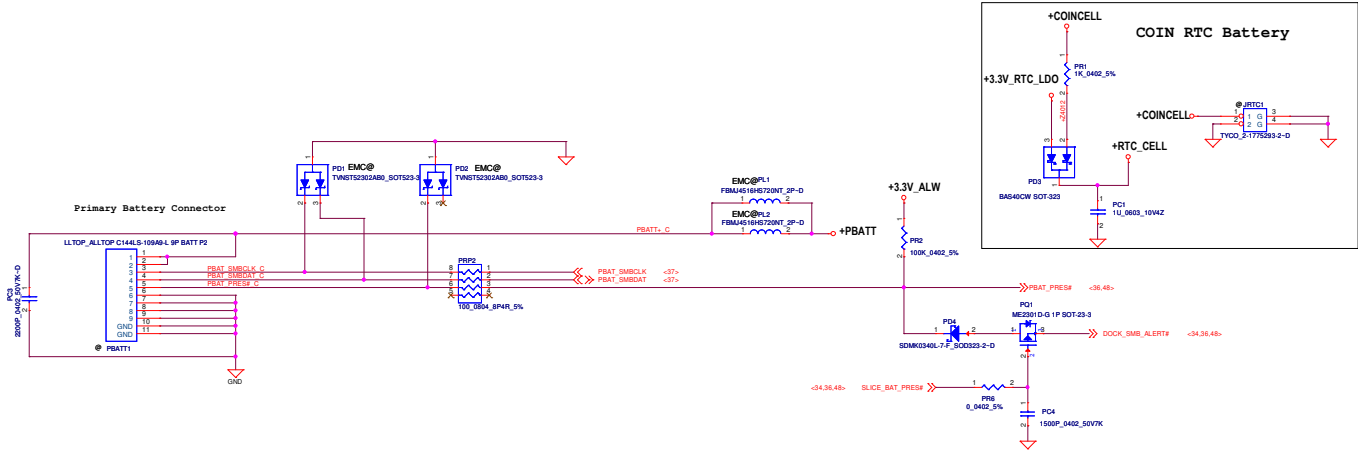
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PAD_LED

Doc# Document Number: **LA-A971P**

Date: Wednesday, March 19, 2014

Rev: 0.1



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LA-A901P

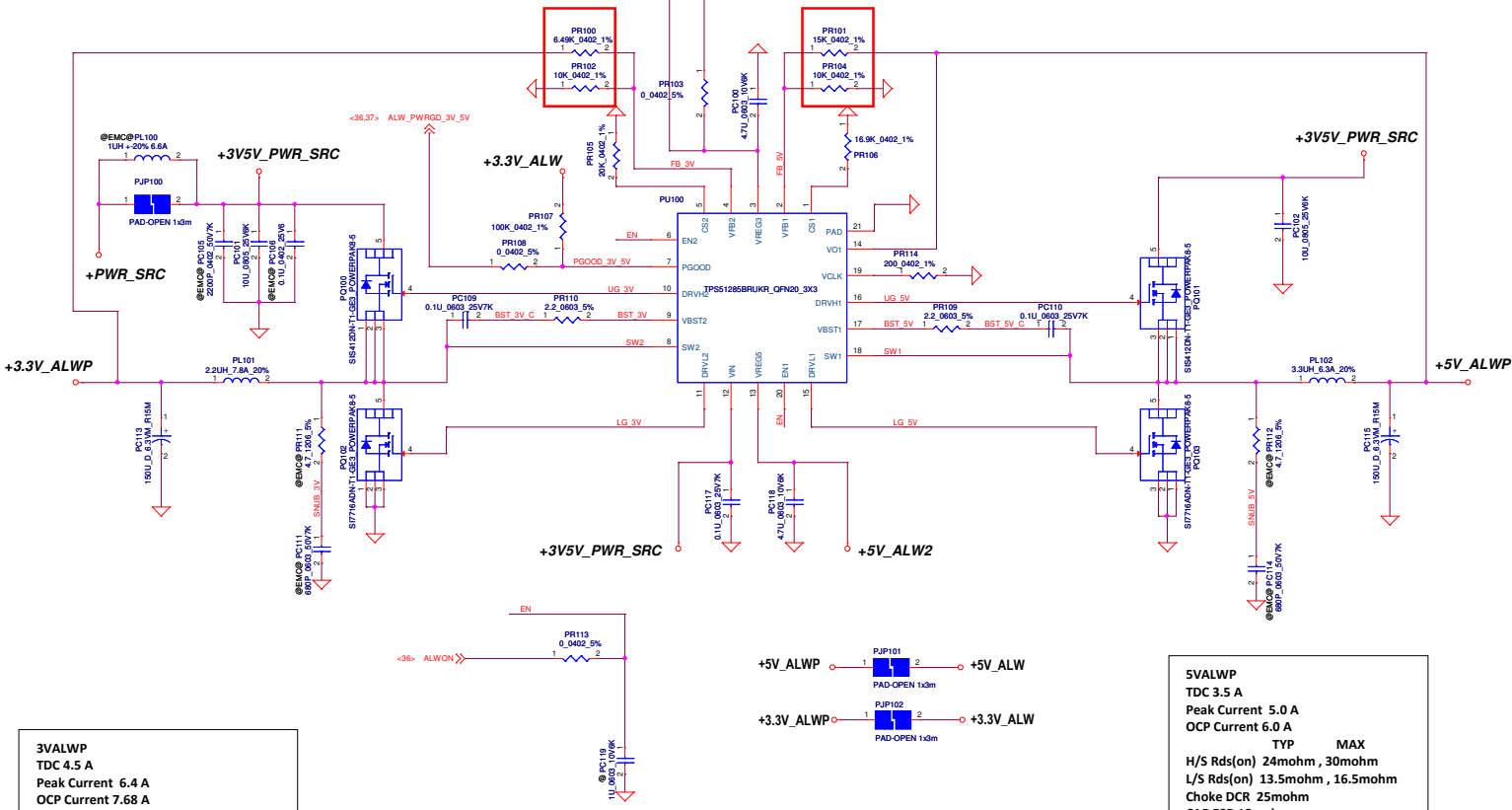
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+DCIN	
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PC105
2200P 0402 50V7K
EMC12Uwh#D@

PC108
0.1U 0402 25V6
EMC12Uwh#D@

+3.3V_ALW2 +3.3V_RTC_LDO



3VALWP
TDC 4.5 A
Peak Current 6.4 A
OCP Current 7.68 A

TYP	MAX
H/S Rds(on)	24mohm , 30mohm
L/S Rds(on)	13.5mohm , 16.5mohm
Choke DCR	15.5mohm
CAP ESR	18mohm

5VALWP
TDC 3.5 A
Peak Current 5.0 A
OCP Current 6.0 A

TYP	MAX
H/S Rds(on)	24mohm , 30mohm
L/S Rds(on)	13.5mohm , 16.5mohm
Choke DCR	25mohm
CAP ESR	18mohm

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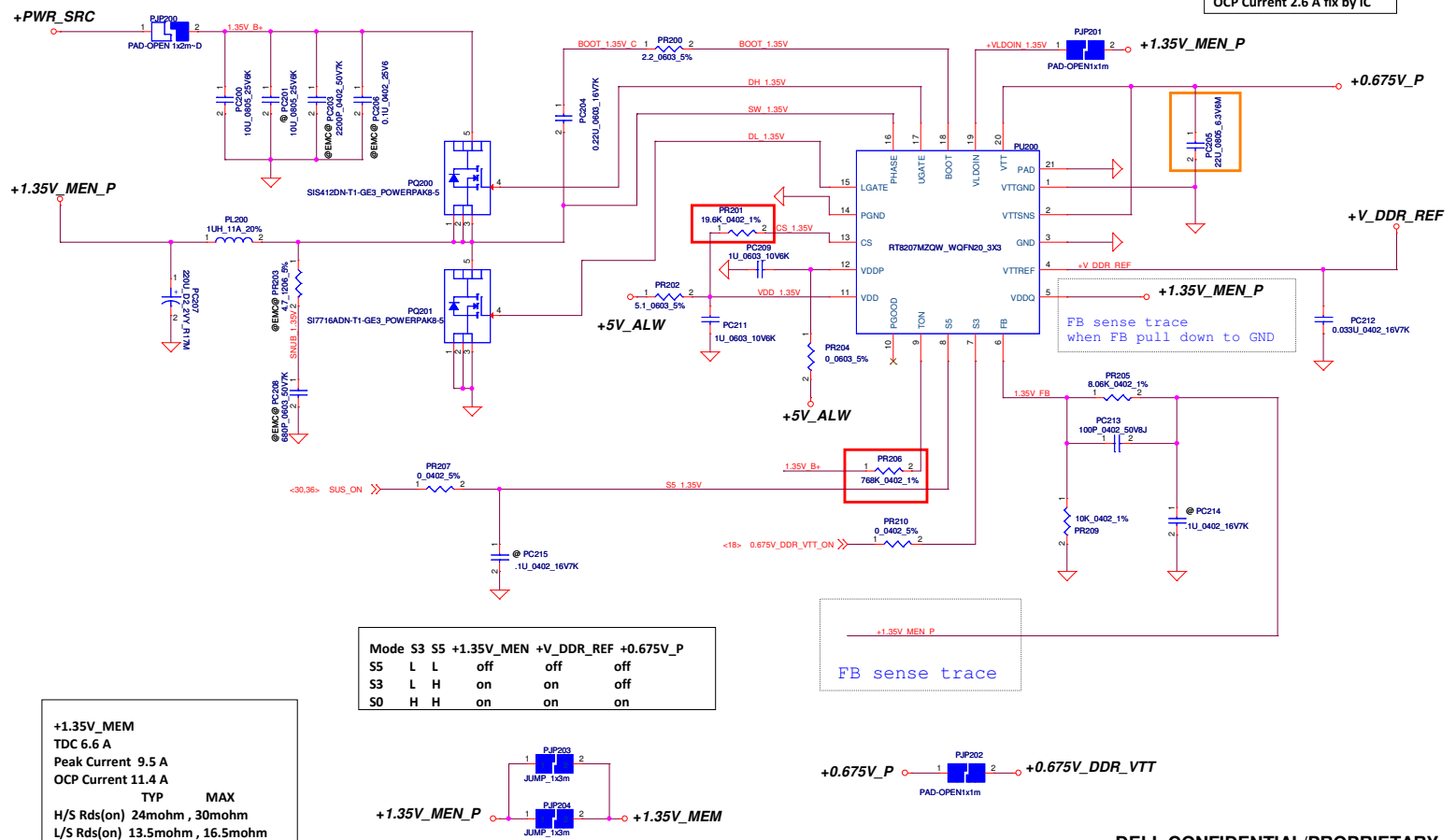
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Title	+5V_ALW/3.3V_ALW	
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PC203
2200P_0402_50V7K
EMC12LWIND@

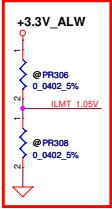
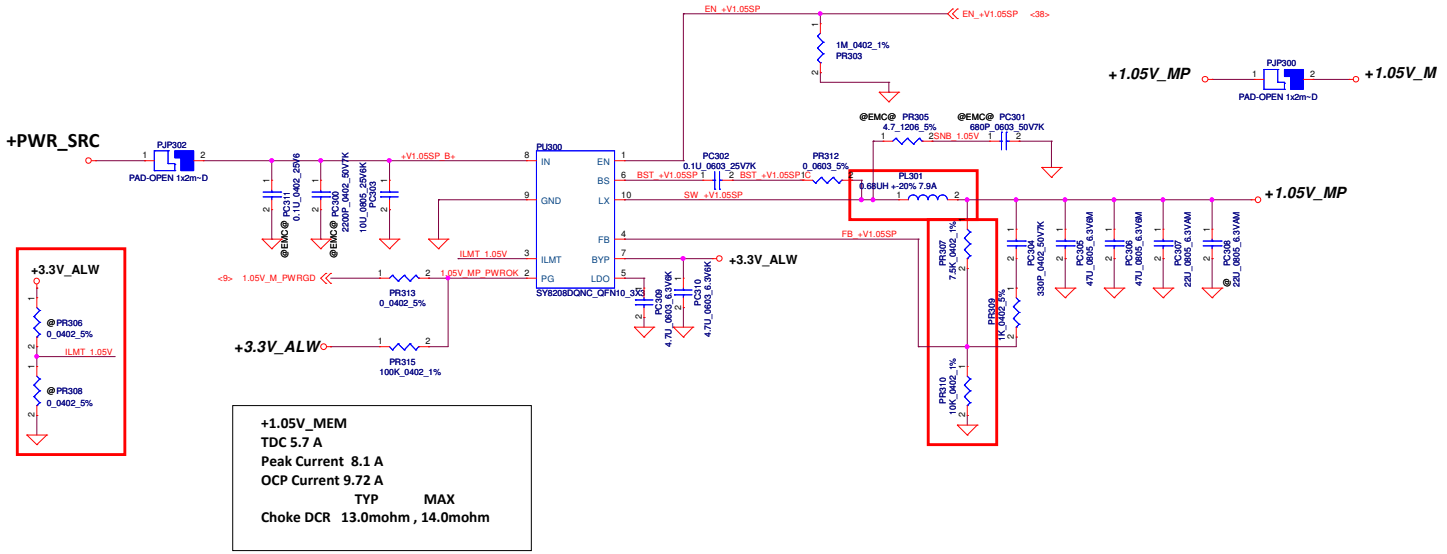
0.675Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC



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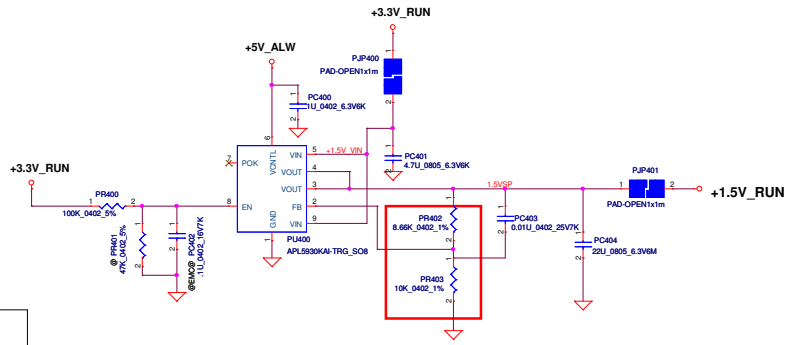


+1.05V_MEM
 TDC 5.7 A
 Peak Current 8.1 A
 OCP Current 9.72 A
 TYP MAX
 Choke DCR 13.0mohm, 14.0mohm

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File	+1.05V_M	
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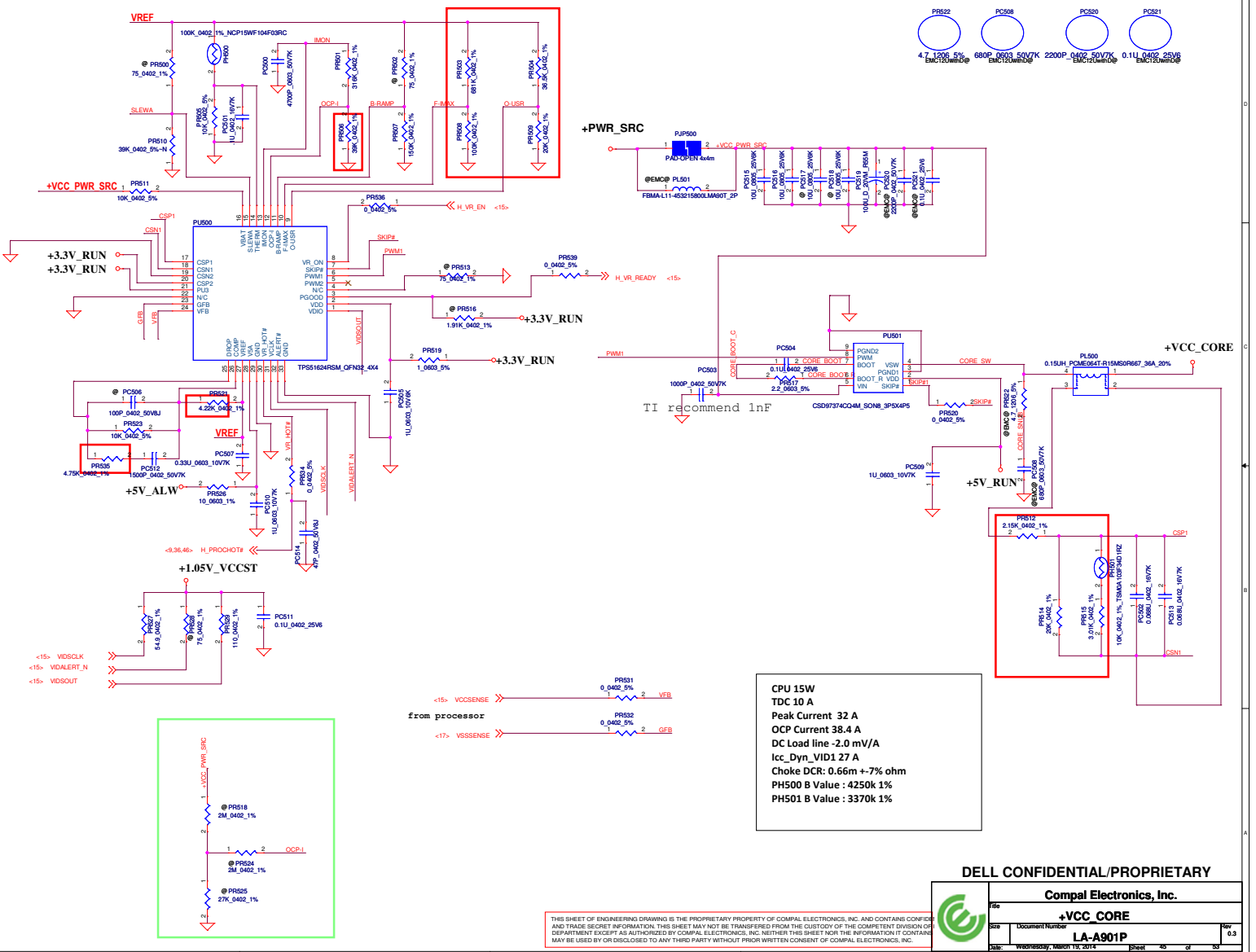


+1.5V_RUN
 TDC 0.47 A
 Peak Current 0.67 A

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				Compal Electronics, Inc.	
				+1.5V_RUN	
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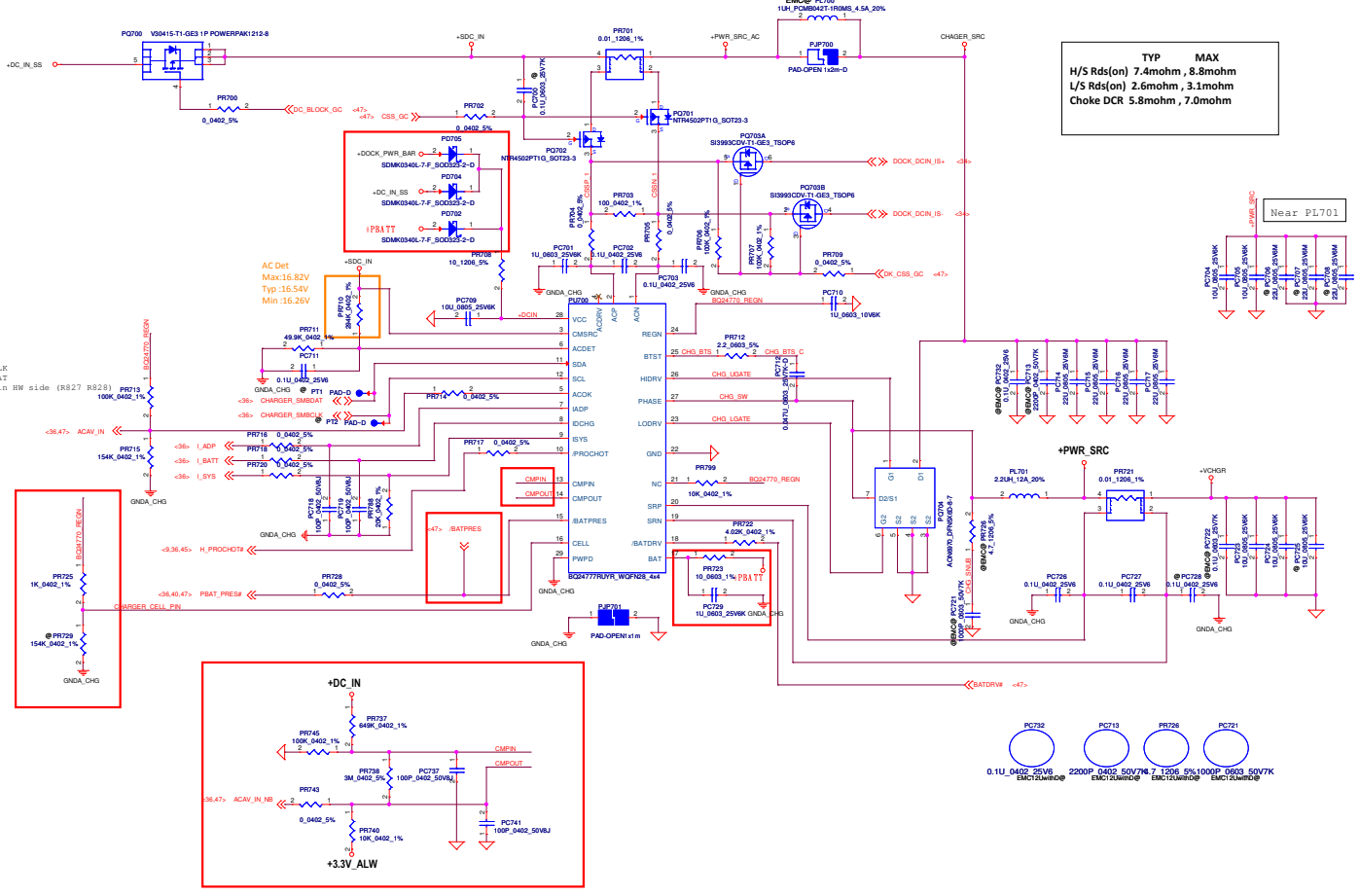


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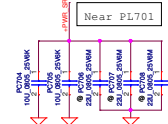
		Compal Electronics, Inc.	
		+VCC CORE	
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CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in RW side (R827 R828)



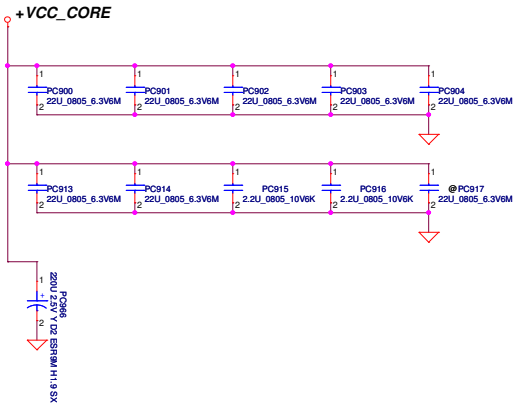
TYP MAX
H/s Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm



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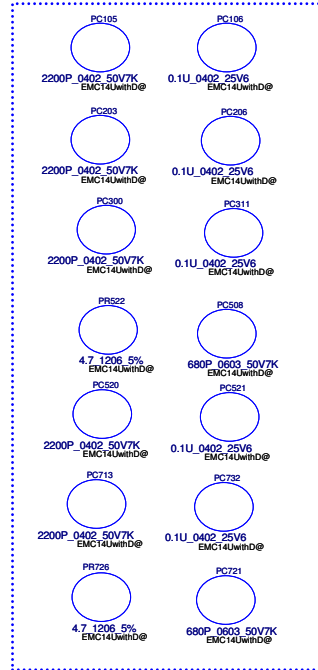
		Cmpal Electronics, Inc.	
		Charger	
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Based on _RF Cheng. Hill
鄭智仁 (11257) for PT 20131107



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 (0.1uF)	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111, PC111, PR112, PC114, PR203, PC208, PR305, PC301, PR522, PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01

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PWR P.I.R (1/1)	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4, reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. UV8 pin B5, B6 change to +3.3V_RUN_VMM 7. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 8. Depop RV73	0.2 (X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2 (X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_MURATA DLW21HN900HQ2L)	0.2 (X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2 (X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
9	24	HW	2013/10/9	COMPAL	SATA circuit issue	Swap mSATA P & N	0.2 (X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDL0C5C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NPRO option.	0.2 (X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)

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EE P.I.R (1/3)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2 (X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 -- RUN_ON_EC	0.2 (X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4? to replace PCH_GPIO48 , Reserve RC302 & RC303	0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 & CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detect issue.	Add RZ50, 100k pull up for WWAN_PWR_EN	0.2 (X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop Q26, Q210, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDF_WAN_SMBDAT/SMBCLK	0.2 (X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
39	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3 (X01)
40	22	HW	2013/12/17	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 & RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 & RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 & RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 & RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.3 (X01)

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EE P.I.R (2/3)

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