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DA6000YE000
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S1



FRAME
ECOMV000200

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Compal Confidential

Schematics Document

VSJEV

MT8317

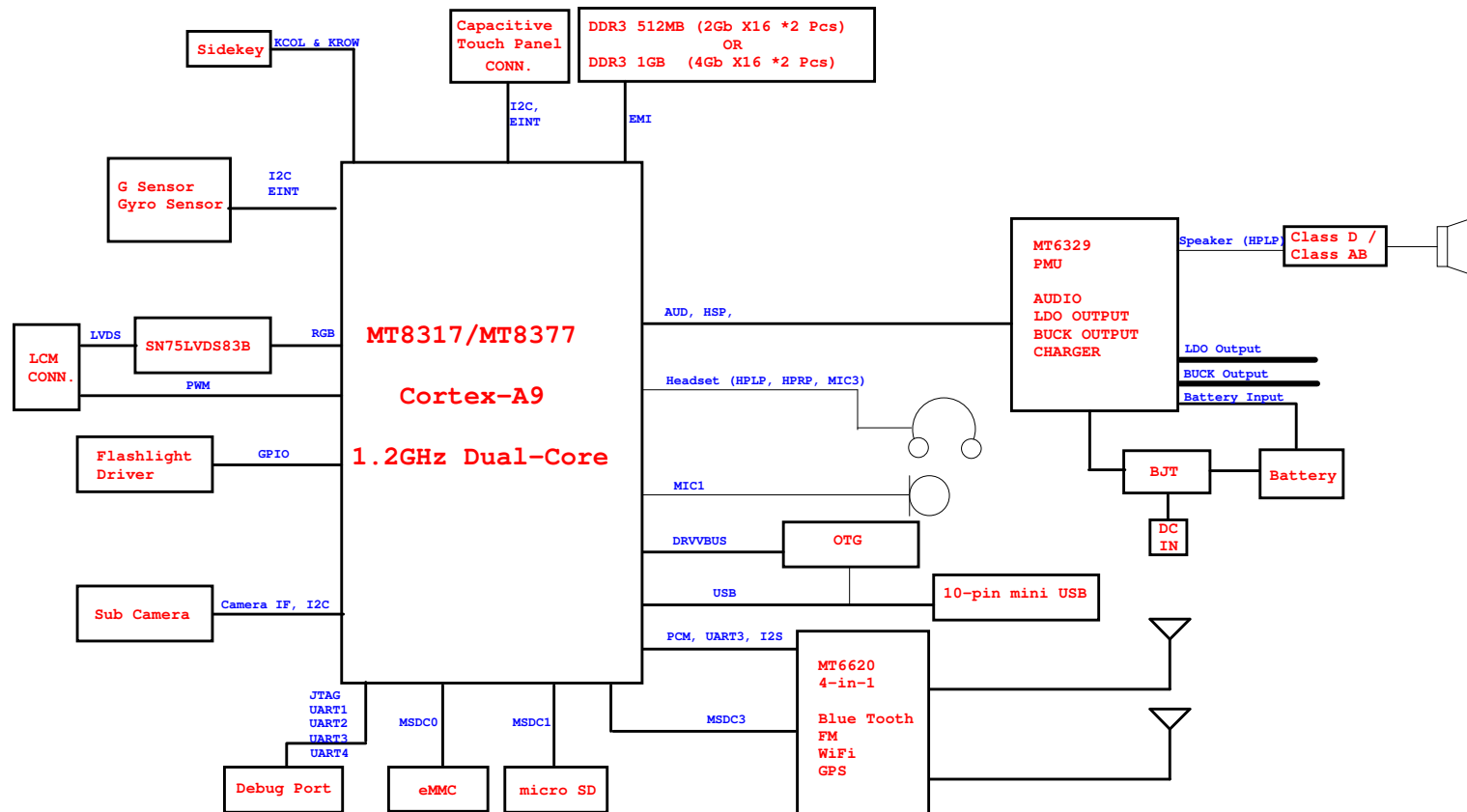
LA-A031P

2013-01-02

REV: 1B

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				Date Wednesday, January 02, 2013	Sheet 1 of 23

VSJEV system block diagram



Voltage Rails

MT6329 Power Plane	Function	Power Level	IDLE	Sleep mode
VCORE_PMU	VCORE switching output	0.75 ~ 1.3	ON	Low voltage
VAPROC_PMU	VPROC switching output	0.75 ~ 1.3	ON	Low voltage
VCXO_PMU	LDO output for TCXO	2.8V	ON	OFF
VCAMA_PMU	LDO output for camaera analog	2.8V	ON	Gating by SW
VDD12_INT_PMU	LDO output used for 1.2V SRAM	1.2V	ON	Low voltage
VIO28_IC	LDO output used for 2.8V IO	2.8V	ON	Gating by SW
VCAM_IO	VCAM_IOPMU	1.8V	ON	Gating by SW
VMC_PMU	SD card I/O and eMMC power	3.3V	ON	Gating by SW
VMCH	SD card power	3.3V	ON	Gating by SW
VGP	Reserve for LCM 3.3V	3.3V	ON	Gating by SW
VGP2	Touch panel GT927 power	2.8V	ON	Gating by SW

I2C address

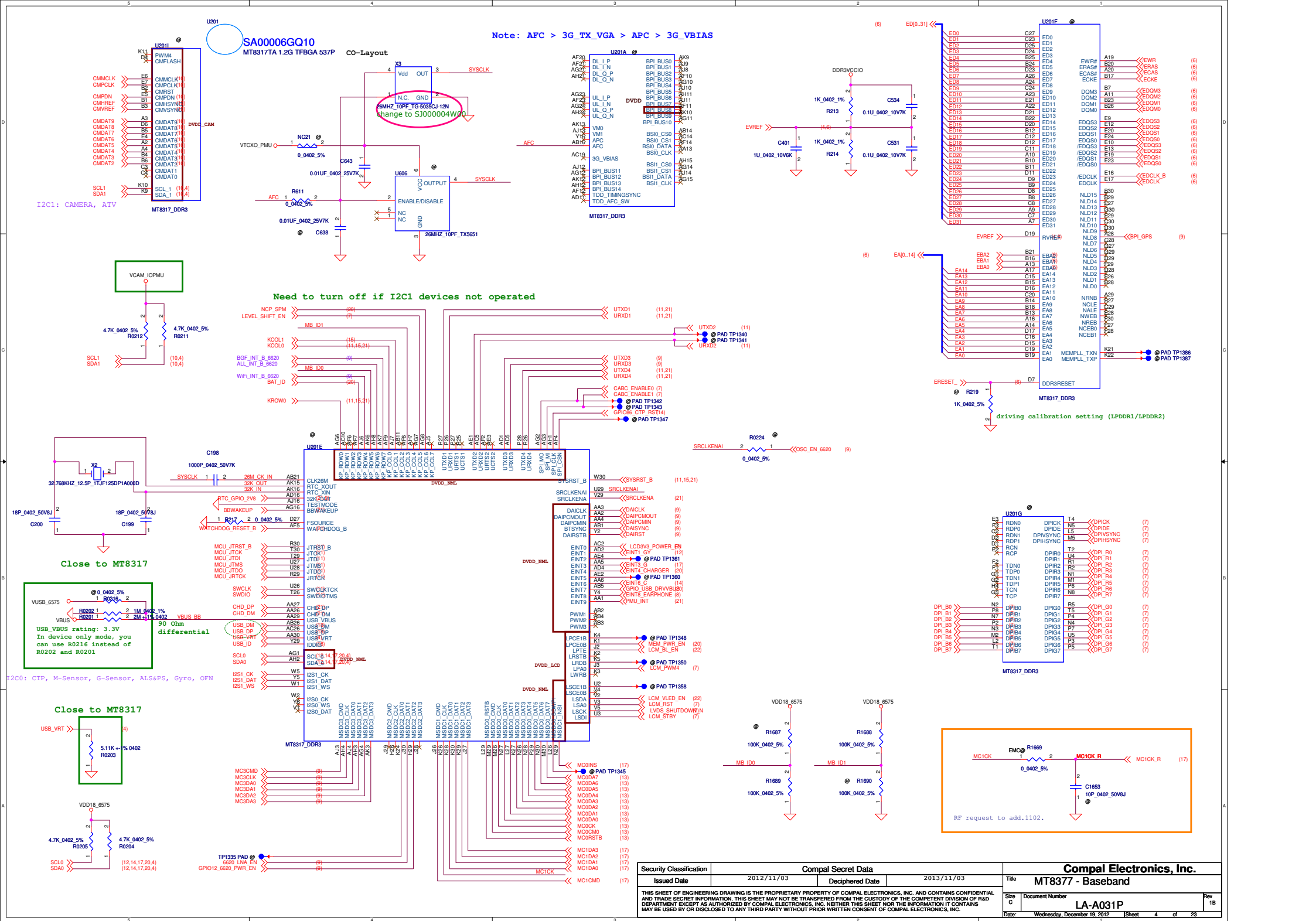
Device	Address(7 bit)	Address(8bit)	
		Write	Read
Gyro (MPU-3050)	0x68	0xD0	0xD1
G-sensor (MC3210)	0x4C	0x98	0x99
Touch screen (GT927)	0x5D	0xBA	0xBB
Camera (OV7675)	0x21	0x42	0x43
Charge (NCP1851)	0x36	0x6C	0x6D
PMU(MT6329)			
Codec			

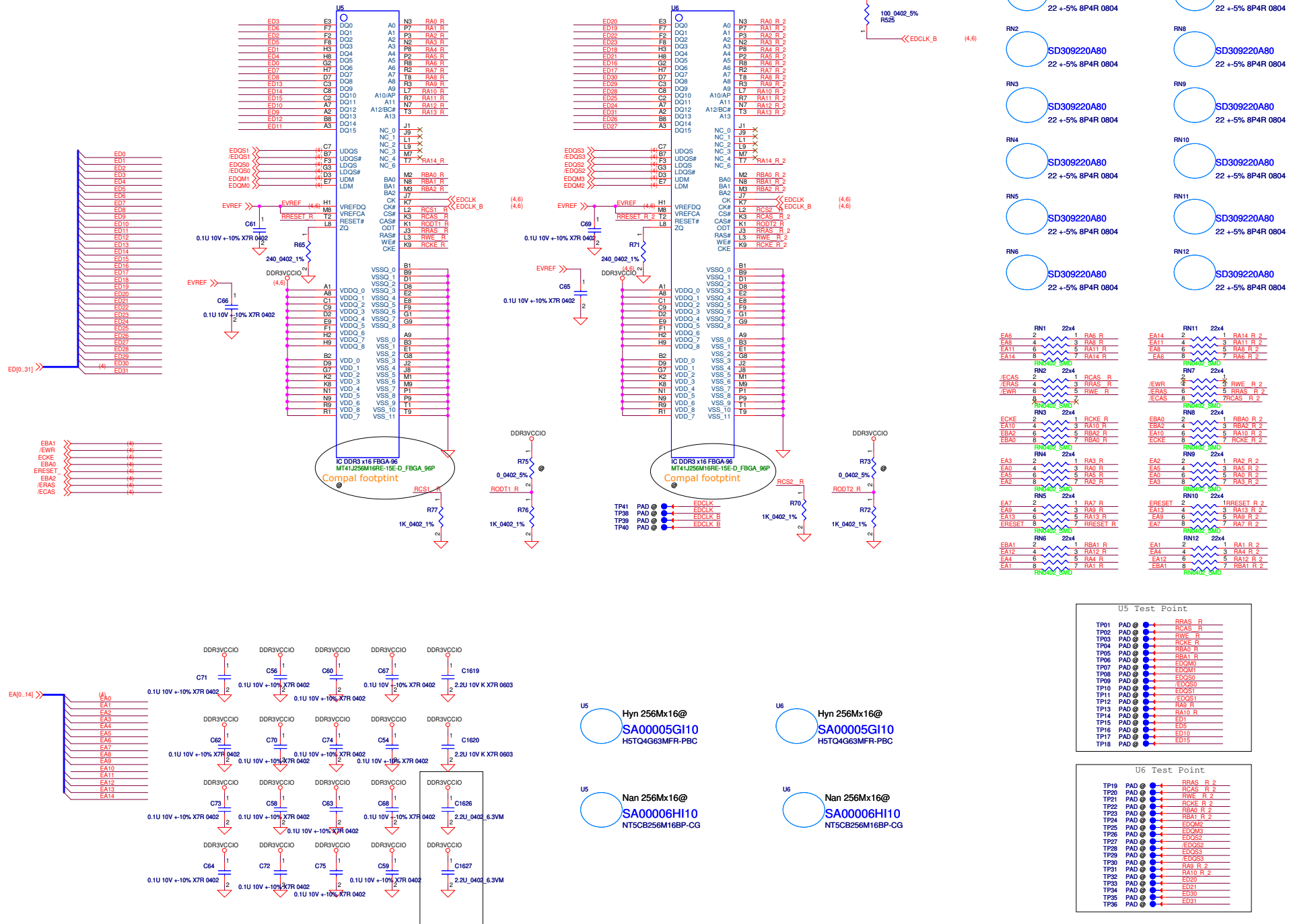
Main board ID

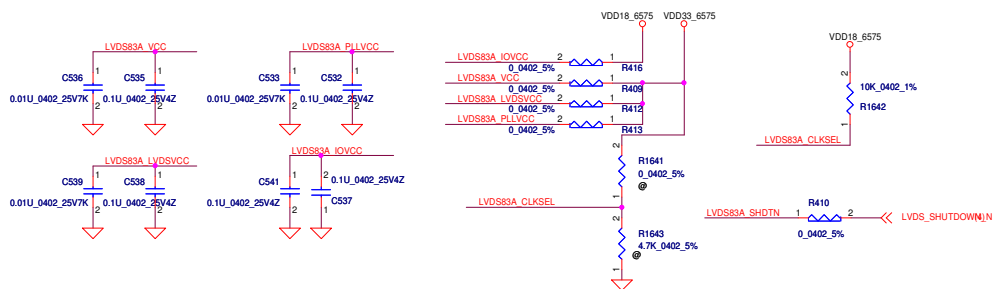
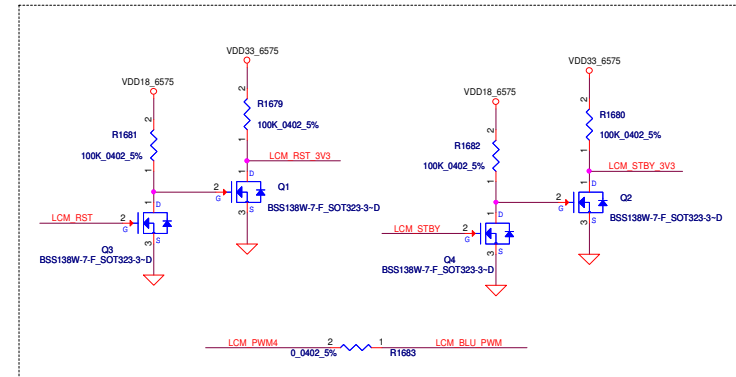
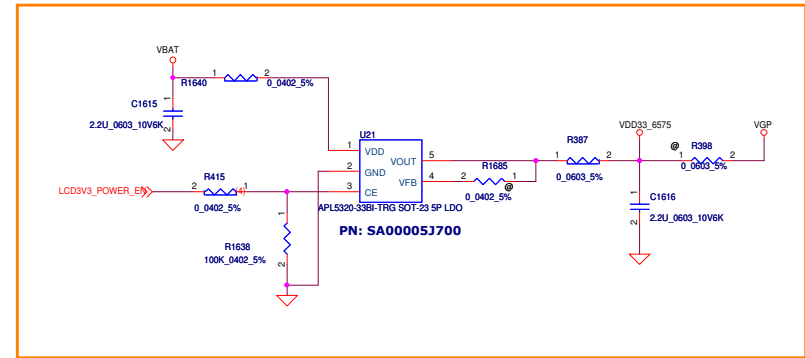
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0	1	PCB2.0+mCube
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1	1	PCB2.0+KXTIK

Battery ID

BAT_ID	
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0	Sanyo

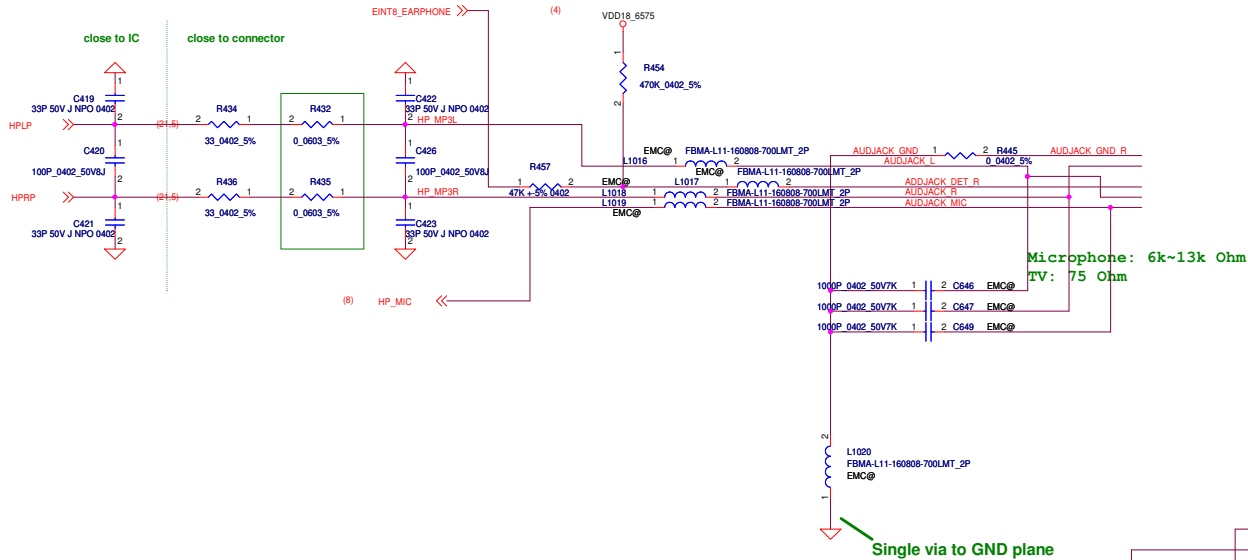




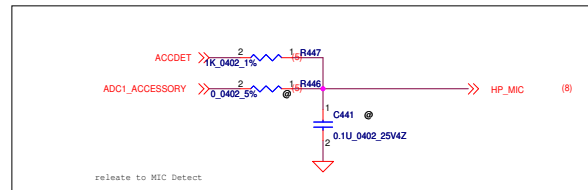
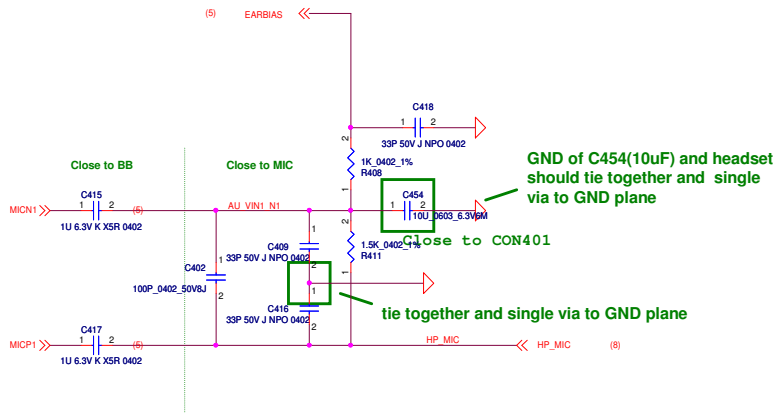


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										LA-A031P		1B	
								Date:		Tuesday, December 18, 2012		Sheet 7 of 23	

Earphone RECEIVER

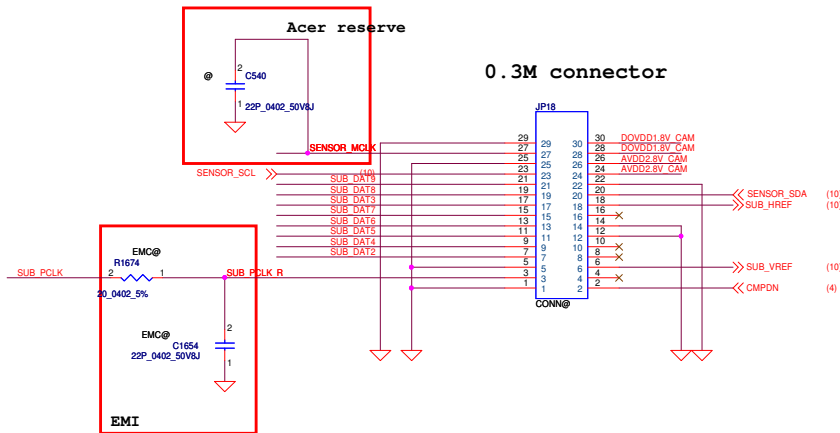
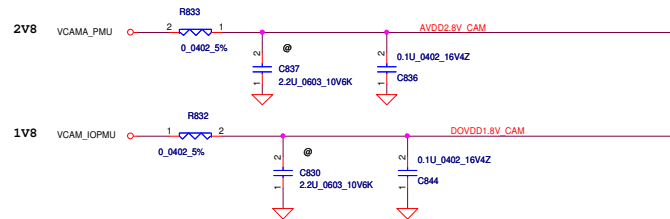
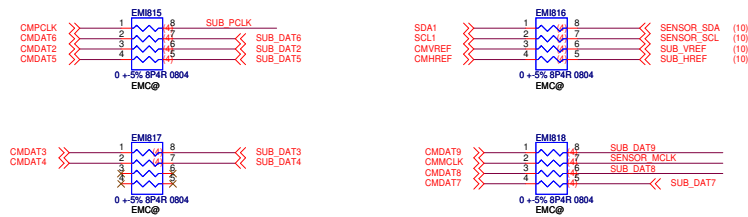


Earphone MICROPHONE



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Sub Camera

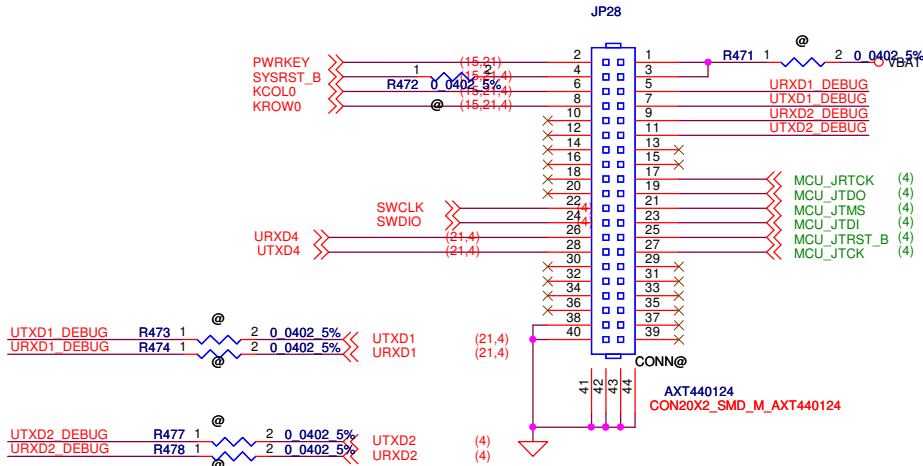


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				Document Number LA-A031P
				Rev 18
				Date: Wednesday, November 28, 2012 Sheet 10 of 23

SD CARD
MSDC1

USB OTG Power

Common Debug

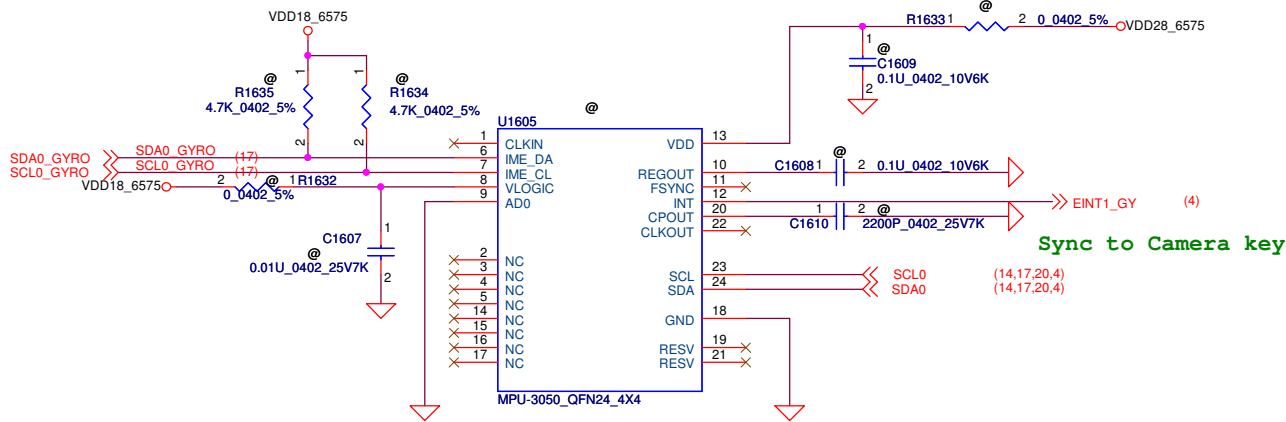


USB HS IF

If mini-A connector insert => CID < 0V => Low
If mini-B connector insert => CID > 1.2V => High
IDPULLUP pin is replaced by 1.2V power source.

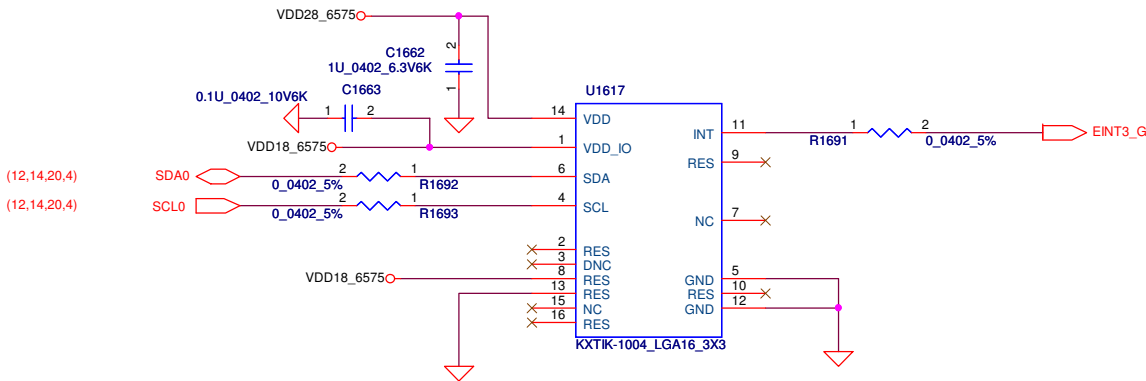
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				Date:	Wednesday, November 28, 2012
				Sheet	11 of 23

Gyro Sensor



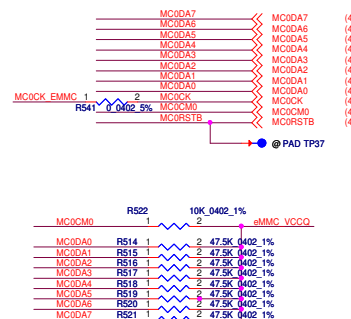
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G Sensor



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				LA-A031P	
				Date:	Monday, January 07, 2013
				Sheet	12 of 23
				Rev	1B

Close to Memory



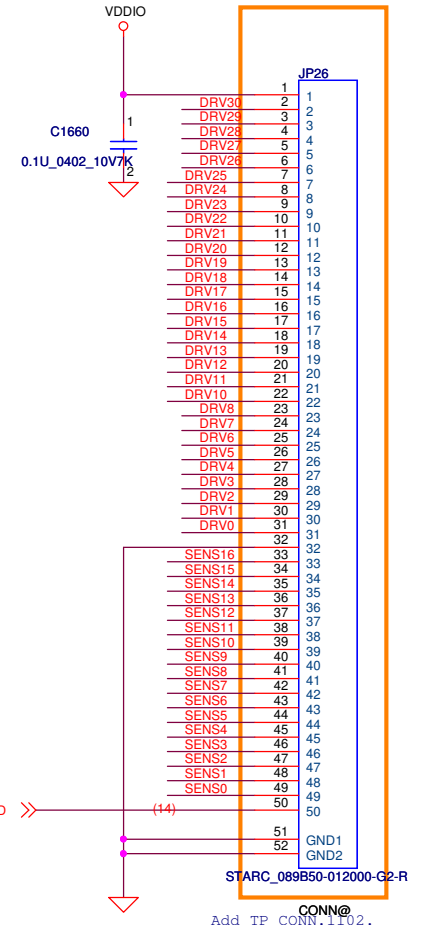
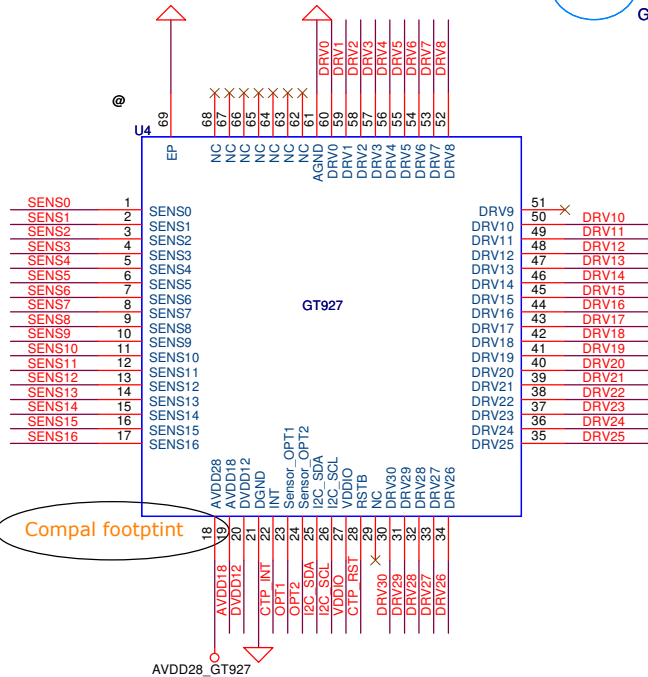
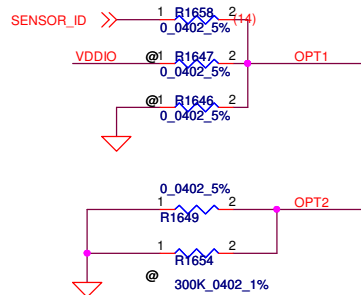
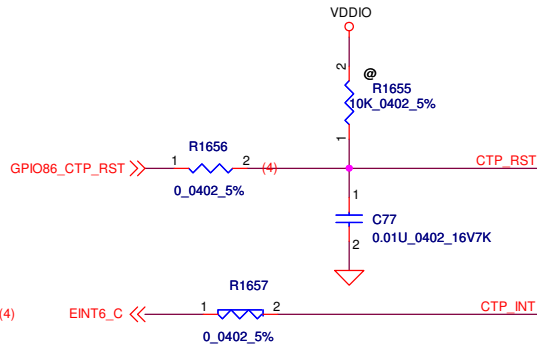
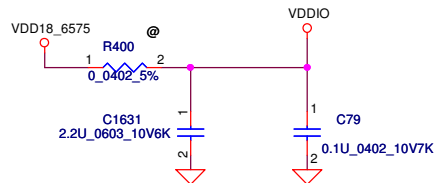
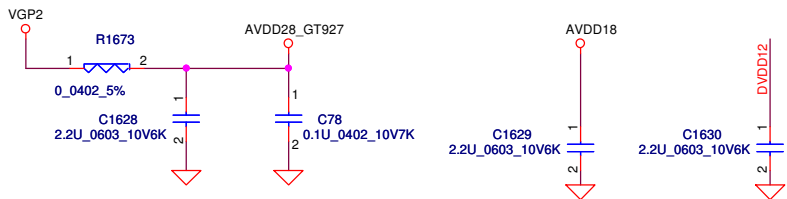
Left Panel: Genetic Screen Strategy

- H1-H5 HOEA:** Five blue circles with faces, labeled H1 HOEA, H2 HOEA, H3 HOEA, H4 HOEA, and H5 HOEA. Red arrows point down from each.
- FD1-FD4:** Four orange stars, labeled FD1, FD2, FD3, and FD4. Red arrows point down from each.
- H6 H1PSN:** A blue circle with a face, labeled H6 H1PSN. Red arrow points down.
- H7 H2P1X1PSN:** A blue circle with a face, labeled H7 H2P1X1PSN. Red arrow points down.

Right Panel: Identification of CLIP and TP

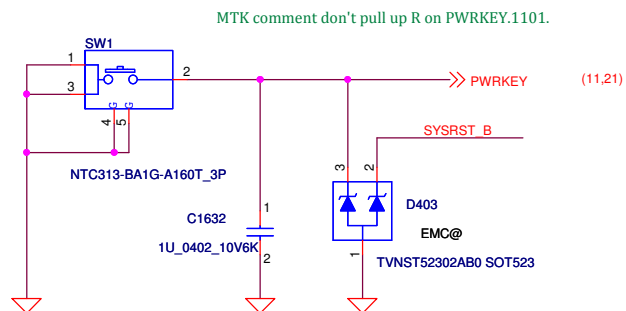
- CLIP1-CLIP8:** Eight blue circles with faces, labeled CLIP1, CLIP2, CLIP3, CLIP4, CLIP5, CLIP6, CLIP7, and CLIP8. Red arrows point down from each.
- S2-S4 TP:** Three blue rectangles with faces, labeled S2 TP, S3 TP, and S4 TP. Red arrows point down from each.

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					LA-A031P	1B
				Date:	Wednesday, November 28, 2012	Sheet 13 of 23



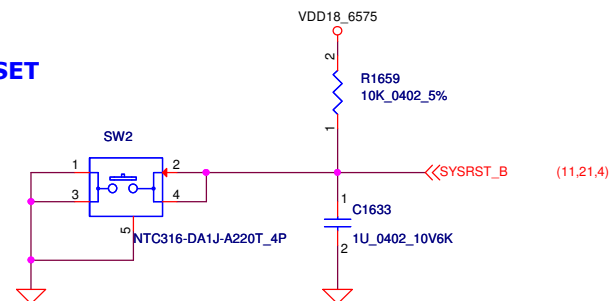
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				LA-A031P	1B
				Date: Wednesday, November 28, 2012	Sheet 14 of 23

Power-on Button

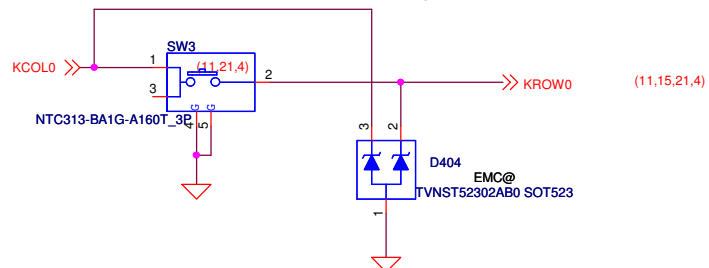


Compal GND MTK GND

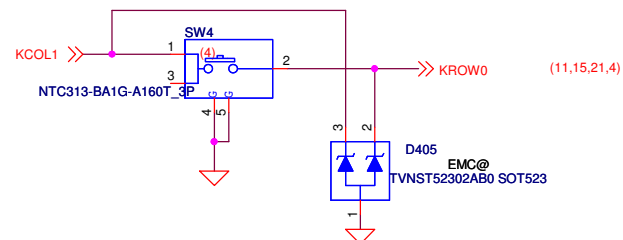
RESET



Volume Up (Download Key)

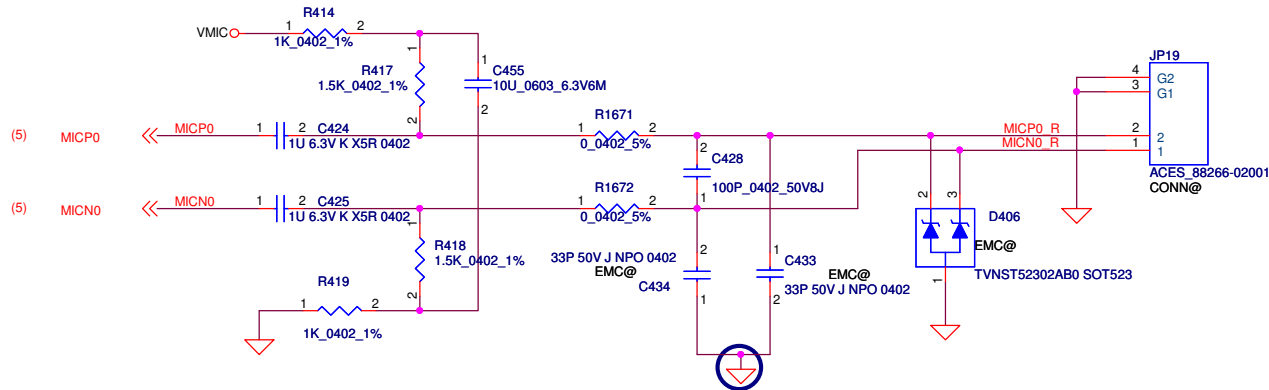


Volume Down



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				B	1B
				Date:	Wednesday, November 28, 2012
				Sheet	15 of 23

MIC

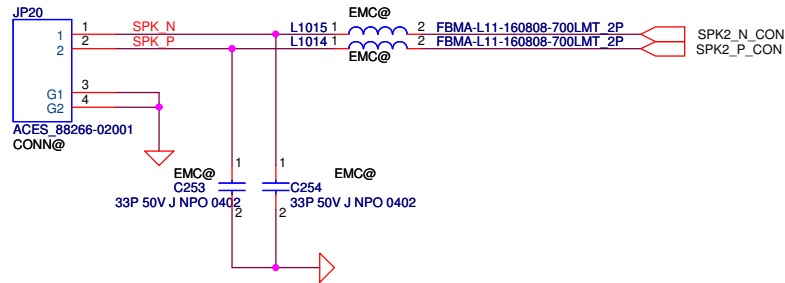


Modify MIC CONN SCH.1102.

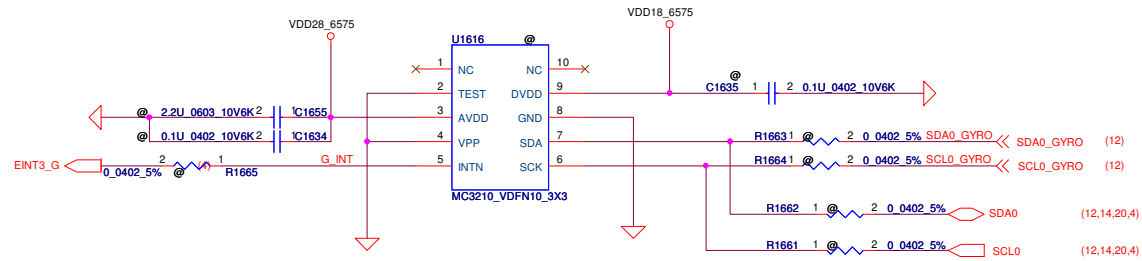
Compal GND MTK GND

SPAKER

Confirm L17/L18 add or not?.1101.



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Size B	Document Number	LA-A031P		Rev 1B
Date:	Wednesday, November 28, 2012	Sheet	16	of 23



D card

The schematic diagram illustrates the electrical connections for the D card, which is a 10-pin SD card. The card is shown in a red box, with its pins labeled 1 through 10. The connections are as follows:

- Pin 1 (EMC@):** Connected to the MC1CK_R signal.
- Pin 2 (EMC@):** Connected to the SD CLK signal.
- Pin 3 (EMC@):** Connected to the SD CLK signal.
- Pin 4 (EMC@):** Connected to the SD CLK signal.
- Pin 5 (EMC@):** Connected to the SD CLK signal.
- Pin 6 (EMC@):** Connected to the SD CLK signal.
- Pin 7 (EMC@):** Connected to the SD CLK signal.
- Pin 8 (EMC@):** Connected to the SD CLK signal.
- Pin 9 (EMC@):** Connected to the SD CLK signal.
- Pin 10 (EMC@):** Connected to the SD CLK signal.

The diagram also shows the power supply connections for the card:

- VMCH:** Connected to the VDD pin (pin 1).
- VSD:** Connected to the VDD pin (pin 1).
- C1636:** A 2.2uF capacitor connected between the VDD pin (pin 1) and ground.
- C1637:** A 10pF capacitor connected between the EMC@ pin (pin 2) and ground.
- JP22:** A 10-pin connector connected to the card pins 1 through 10.

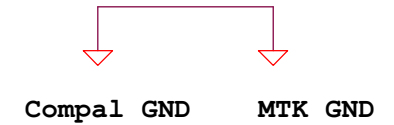
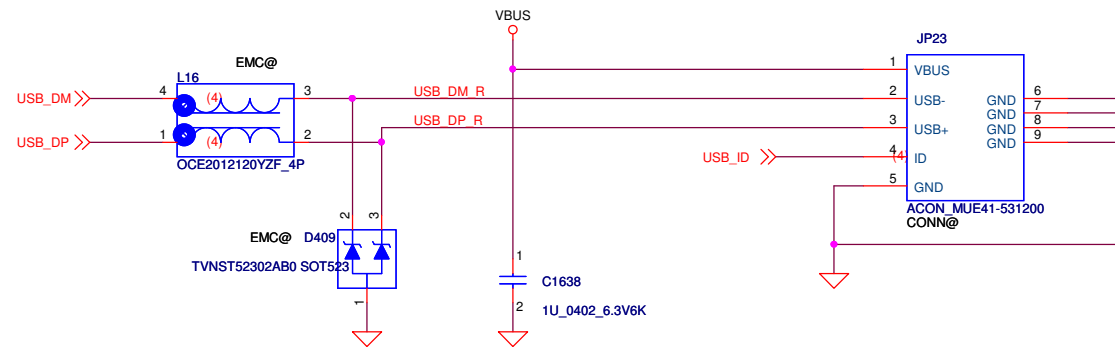
The diagram includes a legend for the SW and L signals:

- SW:** Card remove
- L:** Card insert

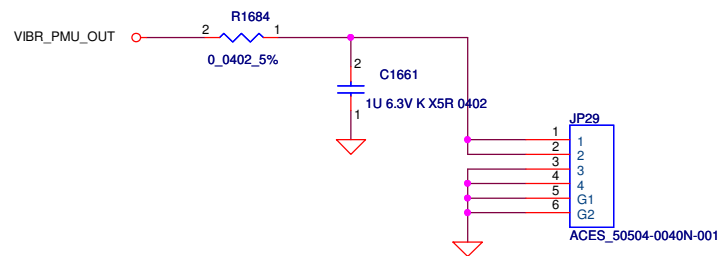
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				1229	LA-A031P	1B
				Date:	Friday, December 28, 2012	Sheet 17 of 23

Micro-USB

If mini-A connector insert => CID < 0V => Low
If mini-B connector insert => CID > 1.2V => High
IDPULLUP pin is replaced by 1.2V power source.



Vibrator



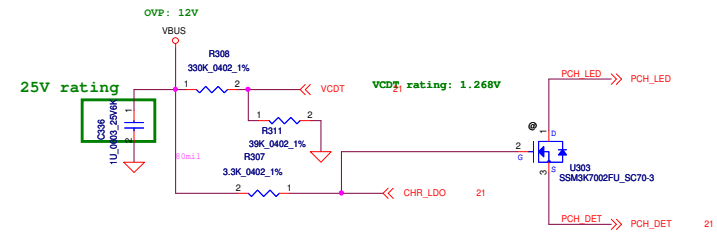
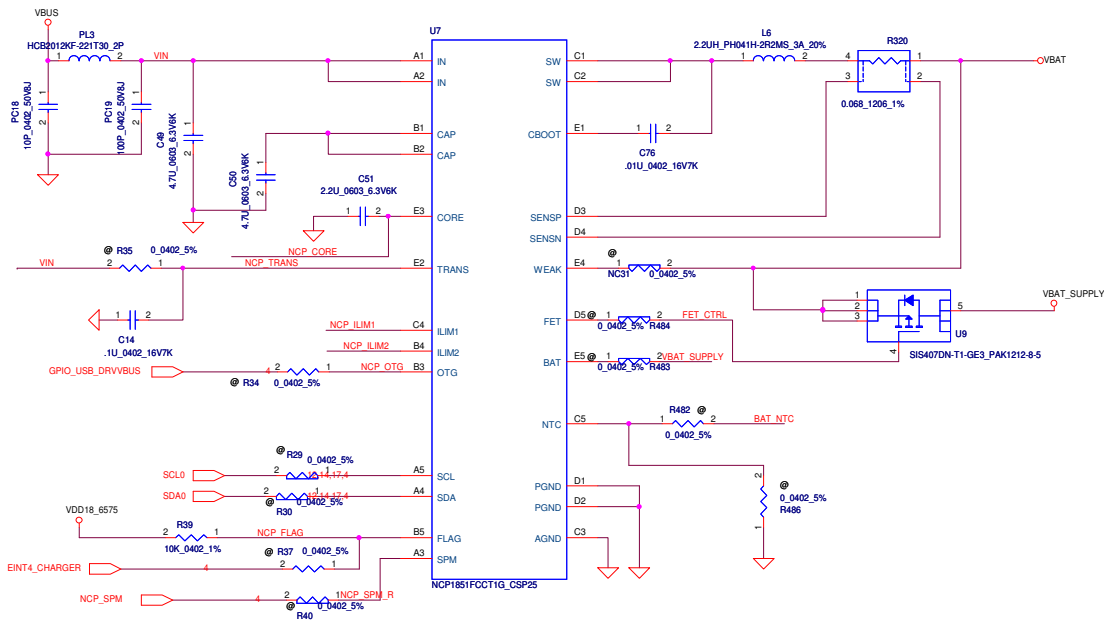
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				B	LA-A031P	1B
				Date:	Wednesday, November 28, 2012	Sheet 18 of 23

RF Antenna change to use MTK

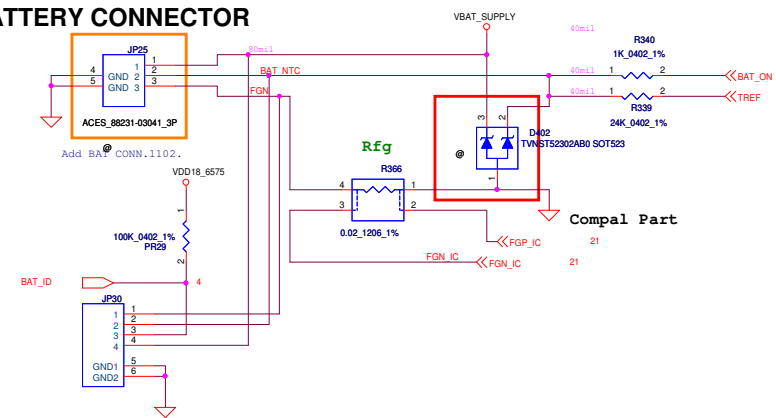


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Date: Wednesday, January 02, 2013				Sheet 19 of 23	

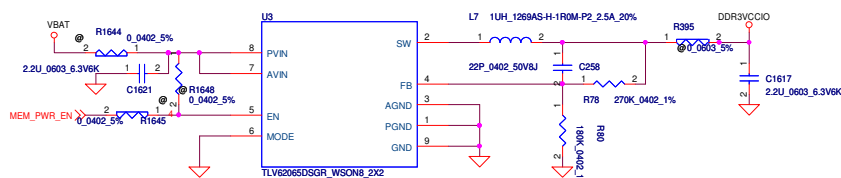
Charger



BATTERY CONNECTOR



DDR3



ILIM1	ILIM2	INPUT CURRENT LIMIT
0	0	100 mA
0	1	Automatic Charge Current
1	0	500 mA
1	1	900 mA

The diagram illustrates the internal architecture and external connections of the MT6329BA PMIC. Key functional blocks include:

- Buck Converter:** Regulates the main system voltage (VOUT) from a 1.2V input. It includes a feedback network (FB) and a control signal (VREF).
- LDOs (Linear Voltage Regulators):** Provide regulated outputs for various PMIC blocks (e.g., VAPROC, VCORE, VDD1V8, VRF18, VTCXO, VCAMA, VCAM_AF, VMC, VMCH, VGP, VGP2, VIBR, VRTC).
- Charger:** Manages battery charging, including detection (PCH_DET), current (KROW0), and voltage (KCOL0) monitoring.
- Control Signal:** Interfaces with the system controller for functions like reset (SRCLKENA, RESETB), test mode (PMU_TESTMODE), and status (SYSRSTB, FSOURCE).
- Gas Gauge:** Monitors battery level and provides status signals (CHG_DP, CHG_DM).
- MP Test Point:** A set of test points (TP1327 to TP1338) for manufacturing and field testing.

Table 1: Buck Converter Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Buck	VPA	0.9 ~ 3.4 (100mV/step)	800	PA_SEL[2:0]
	VPROC	0.75 ~ 1.3 (25mV/step)	1800	SRCLKENA, DVS[2:1]
	VRF18	1.8	250	SRCLKENA
	VCORE	0.75 ~ 1.3 (25mV/step)	1300	SRCLKENA

Table 2: Analog LDO Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Analog LDO	VIO18	1.8	1000	N/A
	VRF	2.85	200	SRCLKENA
	VTCXO	2.8	10	SRCLKENA
	VCAMA	1.5/1.8/2.5/2.8	200	N/A

Table 3: Digital LDO Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Digital LDO	VM12_1	1.2	300	
	VM12_2	1.2	300	
	VM12_INT	1.2	100	
	VRF28	2.85	200	
	VIO28	2.8	100	
	VSIM1	1.8/3.0	100	
	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VUSB	3.3	100	
	VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	300	
	VCAM_IO	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	

Table 4: Vibrator and RTC Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Vibrator	VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	
	VRTC	2.8	2	

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The diagram illustrates the internal architecture and external connections of the MT6329BA PMIC. Key functional blocks include:

- Buck Converter:** Regulates the main system voltage (VOUT) from a 1.2V input. It includes a feedback network (FB) and a control signal (VREF).
- LDOs (Linear Voltage Regulators):** Provide regulated outputs for various PMIC blocks (e.g., VAPROC, VCORE, VDD1V8, VRF18, VTCXO, VCAMA, VCAM_AF, VMC, VMCH, VGP, VGP2, VIBR, VRTC).
- Charger:** Manages battery charging, including detection (PCH_DET), current (KROW0), and voltage (KCOL0) monitoring.
- Control Signal:** Interfaces with the system controller for functions like reset (SRCLKENA, RESETB), test mode (PMU_TESTMODE), and status (SYSRSTB, FSOURCE).
- Gas Gauge:** Monitors battery level and provides status signals (CHG_DP, CHG_DM).
- MP Test Point:** A set of test points (TP1327 to TP1338) for manufacturing and field testing.

Table 1: Buck Converter Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Buck	VPA	0.9 ~ 3.4 (100mV/step)	800	PA_SEL[2:0]
	VPROC	0.75 ~ 1.3 (25mV/step)	1800	SRCLKENA, DVS[2:1]
	VRF18	1.8	250	SRCLKENA
	VCORE	0.75 ~ 1.3 (25mV/step)	1300	SRCLKENA

Table 2: Analog LDO Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Analog LDO	VIO18	1.8	1000	N/A
	VRF	2.85	200	SRCLKENA
	VTCXO	2.8	10	SRCLKENA
	VCAMA	1.5/1.8/2.5/2.8	200	N/A

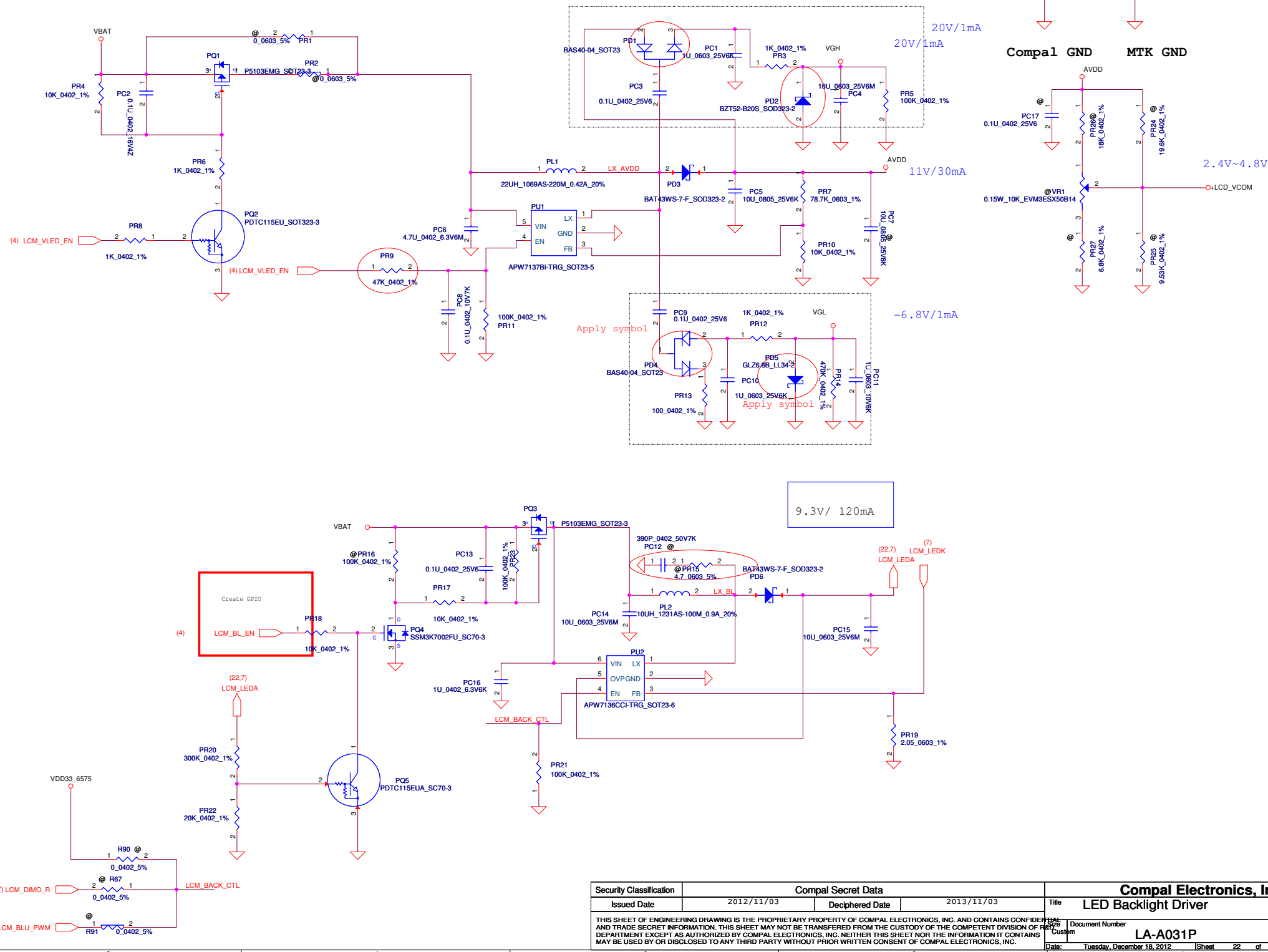
Table 3: Digital LDO Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Digital LDO	VM12_1	1.2	300	
	VM12_2	1.2	300	
	VM12_INT	1.2	100	
	VRF28	2.85	200	
	VIO28	2.8	100	
	VSIM1	1.8/3.0	100	
	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VUSB	3.3	100	
	VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	300	
	VCAM_AF	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	

Table 4: Vibrator and RTC Specifications

Function	Symbol	Vout (V)	Iout (mA)	External HW Control
Vibrator	VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	
	VRTC	2.8	2	

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				LA-A031P	1B
				Date: Tuesday, December 18, 2012	Sheet 22 of 23

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