

QCLA4 / QCLA5

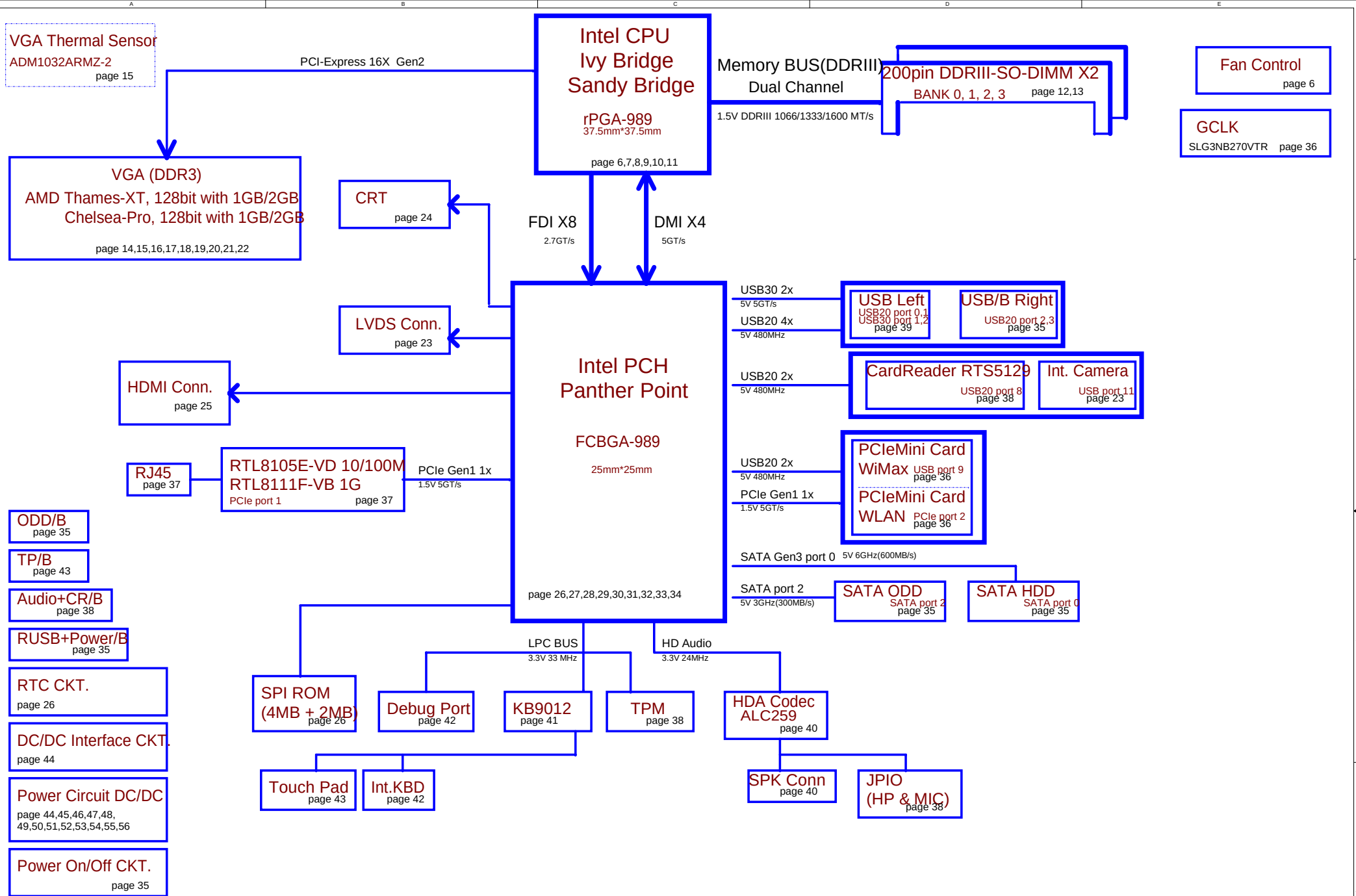
Eureka 10FG

LA-8861P REV 0.2 Schematic

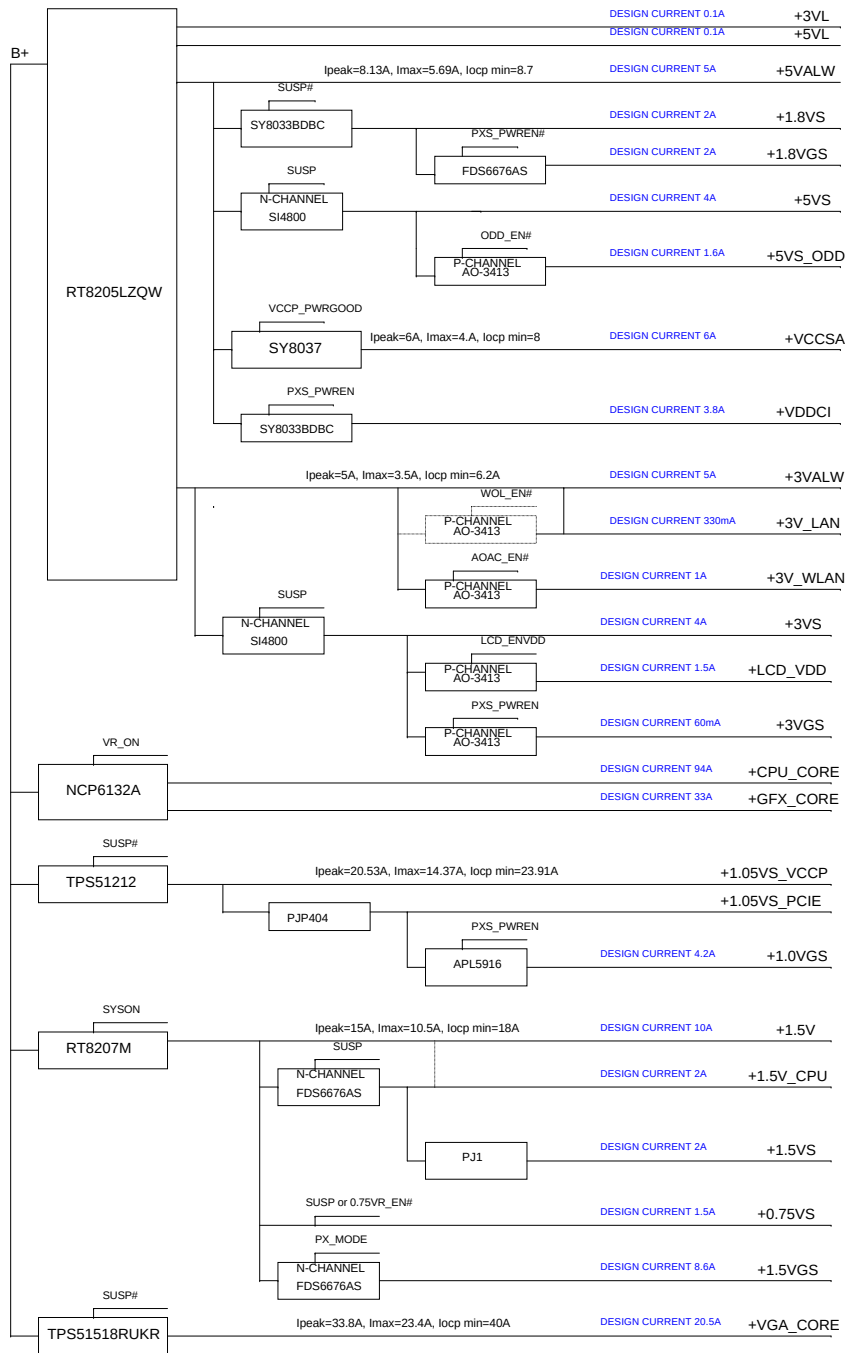
Intel Processor (Ivy Bridge) / PCH(Panther Point)
2012-02-09 Rev 0.2

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Voltage Rails (O MEANS ON X MEANS OFF)						
power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address			
Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address				EC SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
				+3VS	ATI GPU	82 H	1000 0010 b
Power	Device	HEX	Address				

Platform	SKU	CPU	PCH	VGA
Chief River		Clarksfield	HM76ES2/HM70C0 (PCHB0@/HM70C0@)	Themes/Chlsea (TH@/CH@)

BTO Option Table

Function	SKU	MIC		LAN		TPM			
description	SKU	MIC		LAN		TPM			
explain	PX4(reserve)	Dig Mic	Analog Mic	10/100M	Giga	9635	9655		
BTO	PX4@	CAM@	AMIC@	8105ELDO@	8111FVB@	TPM9635@	TPM9655@		

Function							
description							
explain							
BTO							

Function							
description							
explain							
BTO							

Function		
description		
explain		
BTO		

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

All the ASIC supplies, except for VDDR3, must full nominal voltages within 20 ms of the start of the r shorter ramp-up duration is preferred. There is no ramp up of VDDR3 relative to other power rails.

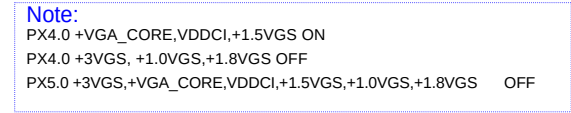
The external pull-up resistors on the DDC/AUX sign ramp up before or after both VDDC and VDD_CT have r VDDC and VDD_CT should not ramp up simultaneously. should reach 90% before VDD_CT starts to ramp up (o For power down, reversing the ramp-up sequence is

reach their respective ramp-up sequence, though a timing requirement on the

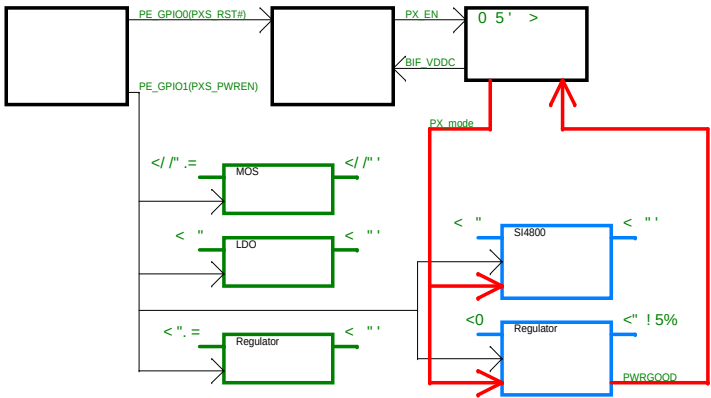
als (if applicable) should be ramped up.

For example, VDDC (or vice versa).

recommended.

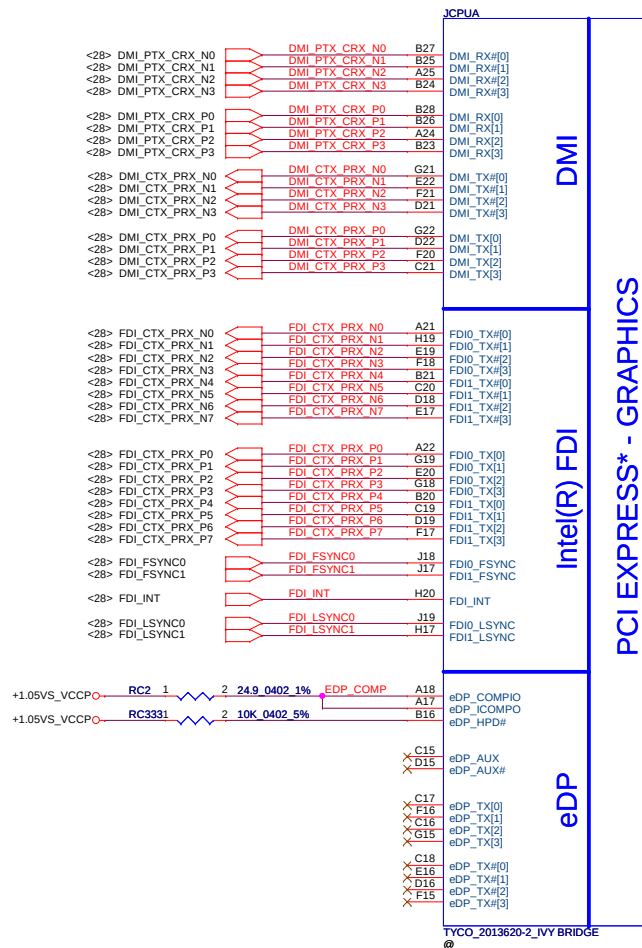


Timing diagram showing the sequence of power-up signals for the A64 core. The signals are +3VGS, +VGA_CORE, +VDDCI, +1.5VGS, +1.0VGS, and +1.8VGS. The diagram shows a staggered sequence where each signal transitions from low to high at a different time, with a total delay of less than 20ms indicated for the +1.8VGS signal.

[illegible]

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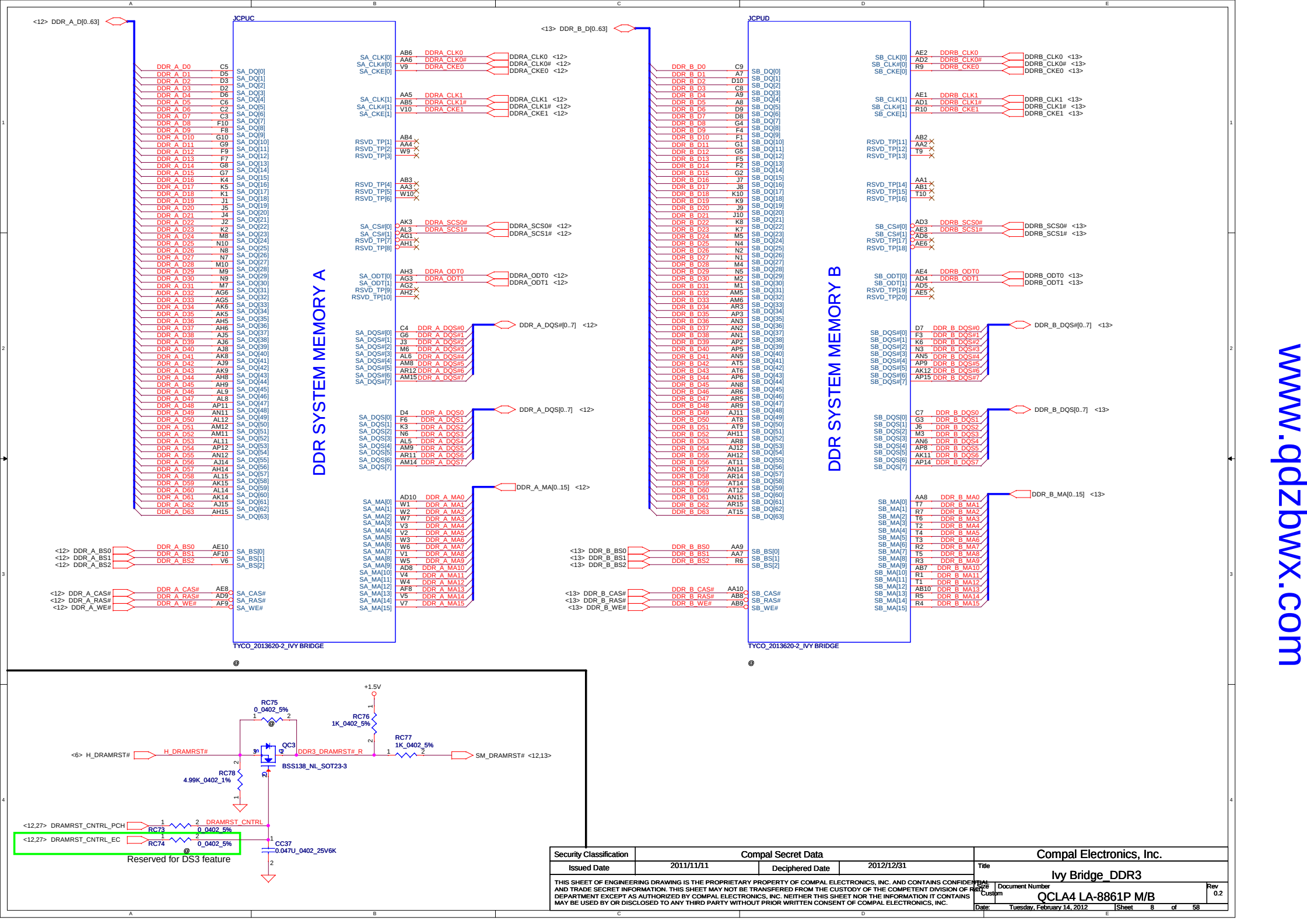
PCI EXPRESS* - GRAPHICS

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

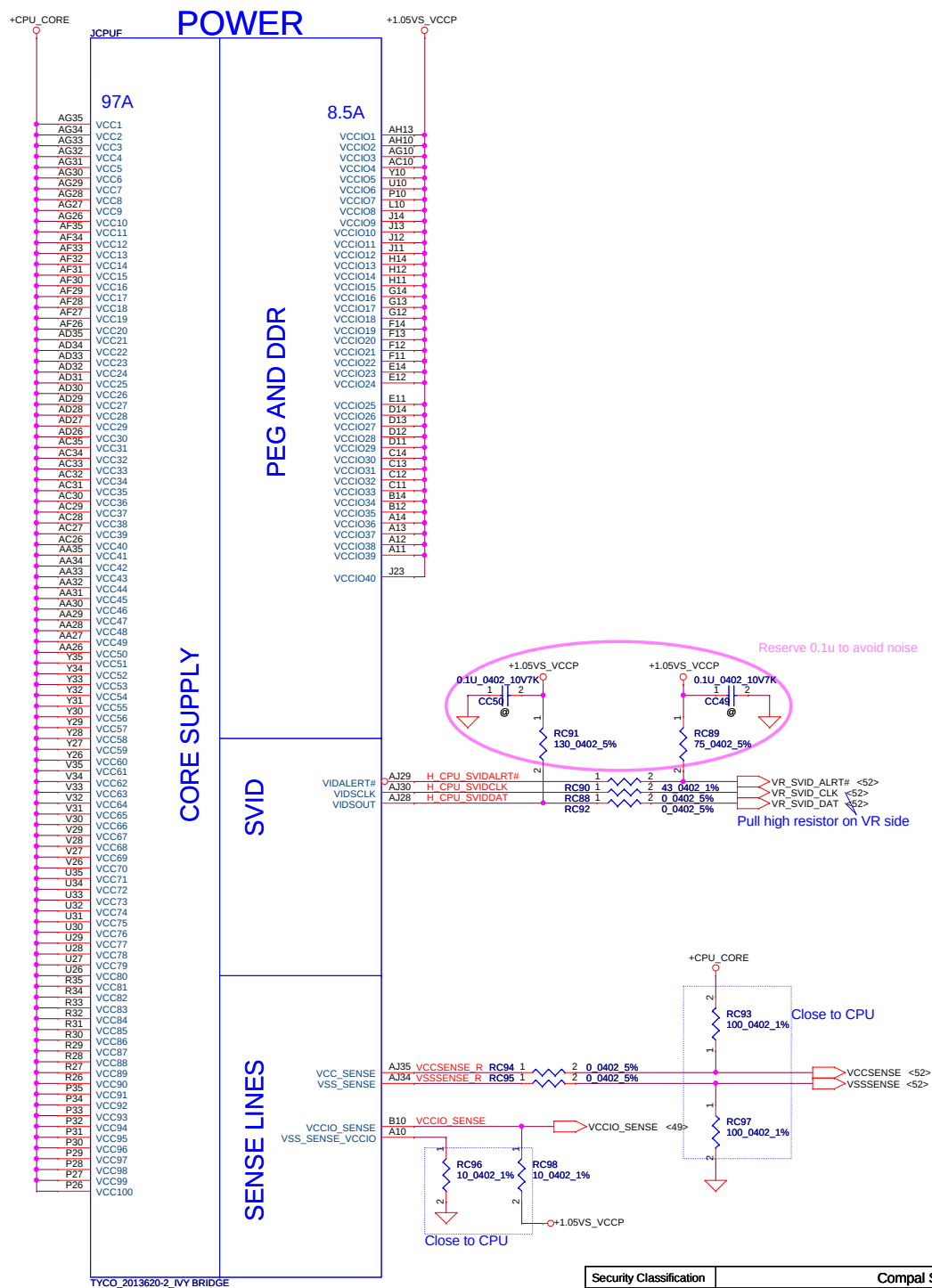
	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	100 nF~220 nF

AMD GPU (Themes & Chlsea) only support up to Gen2

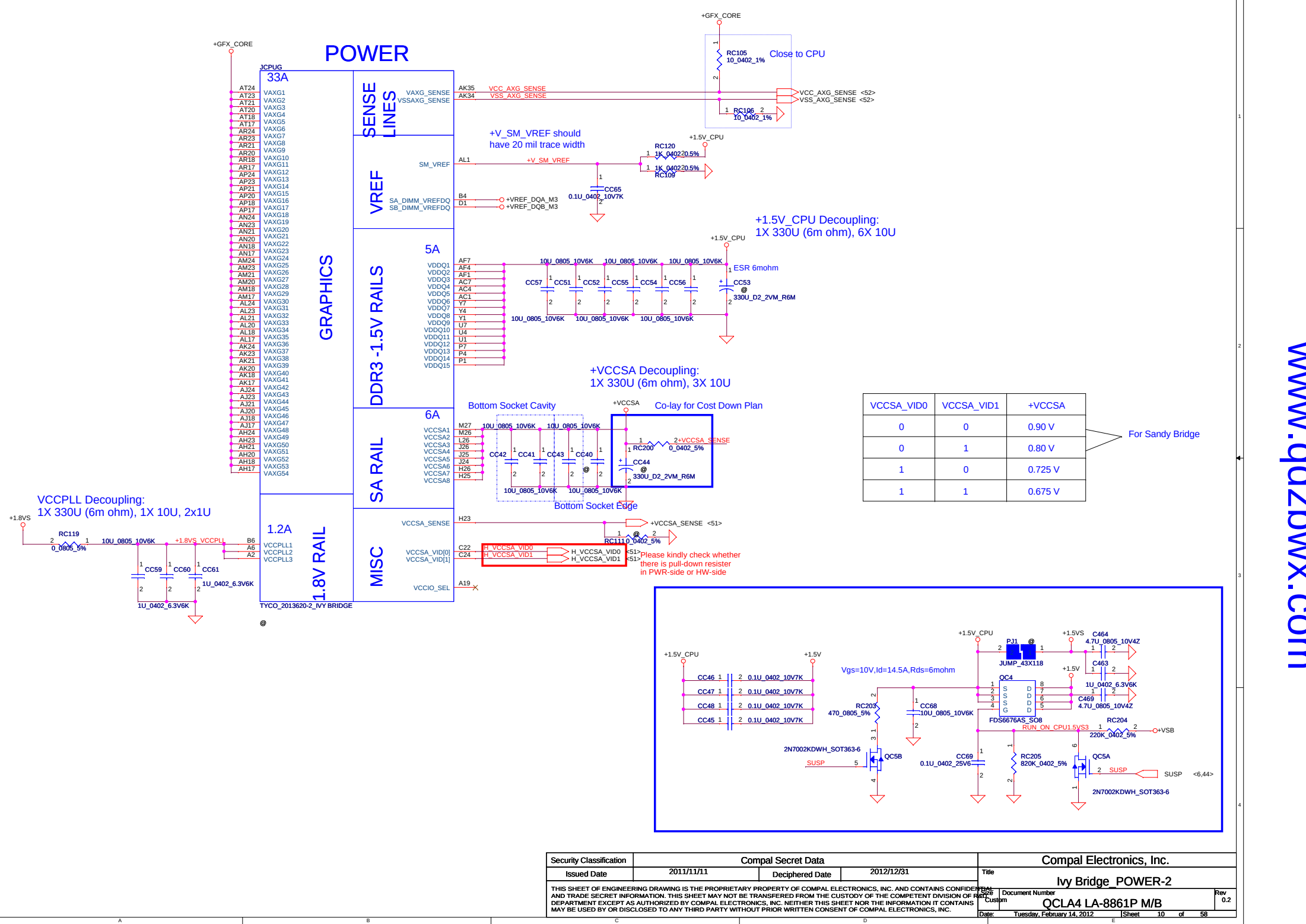
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								Ivy Bridge_DMI/PEG/FDI		
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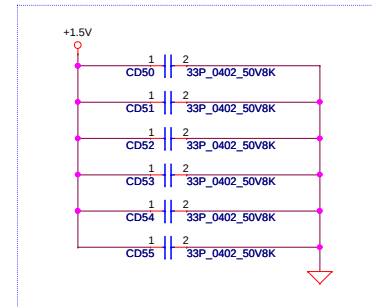
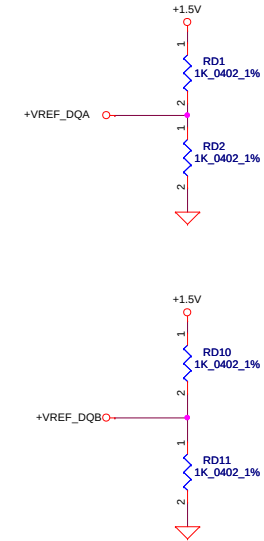
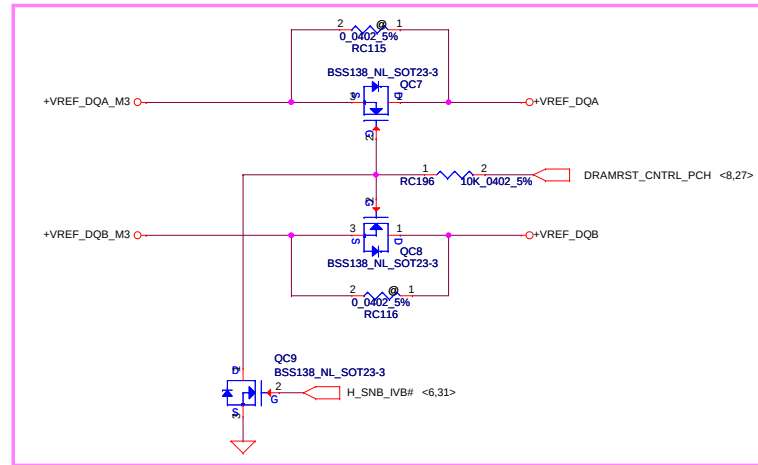
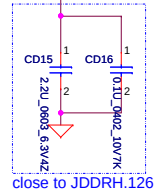
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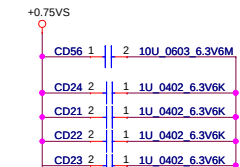
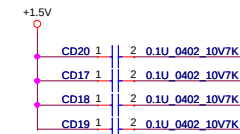
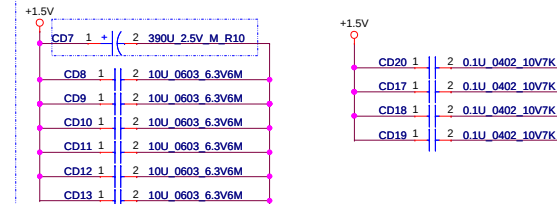
DDR3 SO-DIMM A
Reverse Type

Intel DDR Vref M3

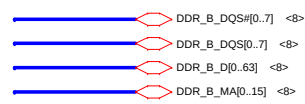
DDR_A_DQS[0..7] <8>
DDR_A_DQS#[0..7] <8>
DDR_A_D[0..63] <8>
DDR_A_MA[0..15] <8>

please place these caps near the
reference power plane of CMD/AD

close to JDDRH.126

Layout Note:
Place near JDDRHLayout Note: Place these 4 Caps near
Command and Control signals of DIMMALayout Note:
Place near JDDRH.203 and 204Swap DIMMA to DDR3H
(for layout concern)

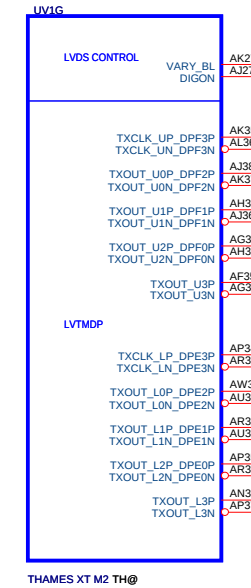
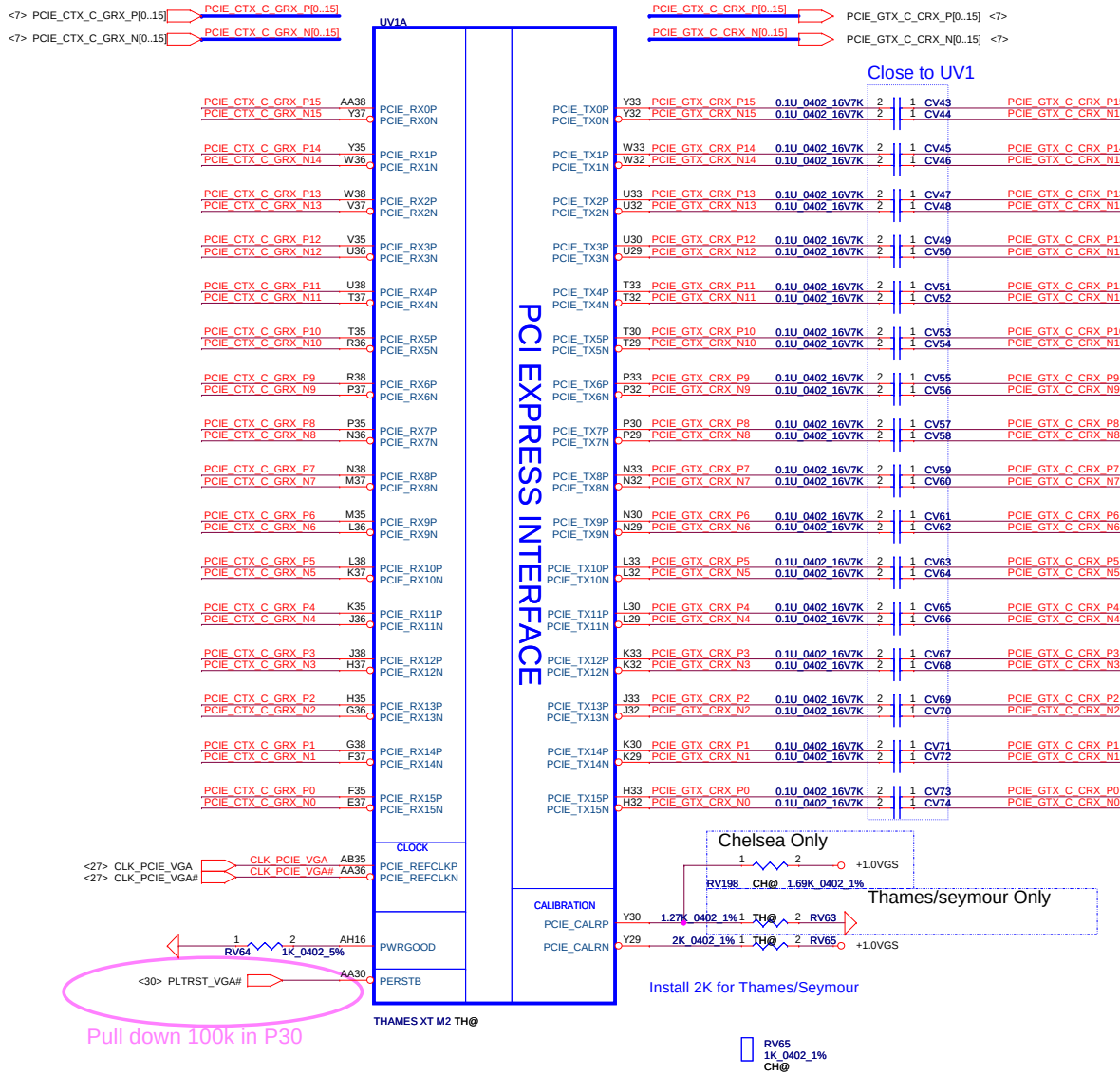
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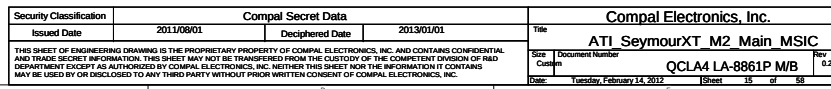
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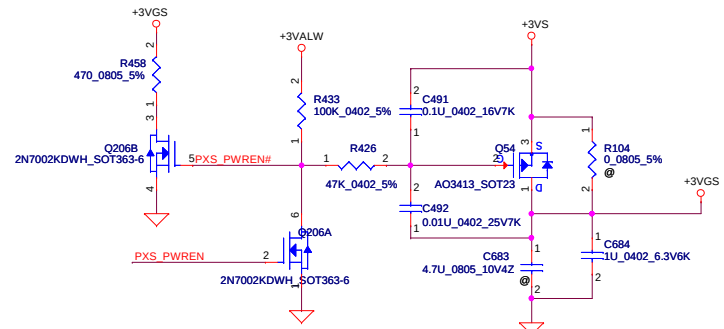
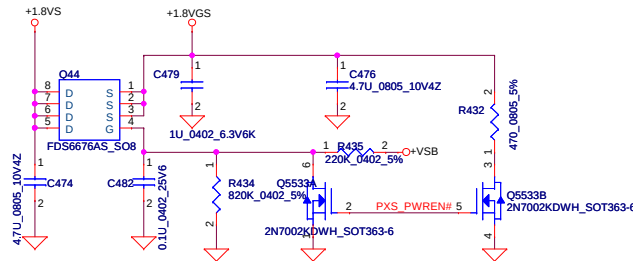
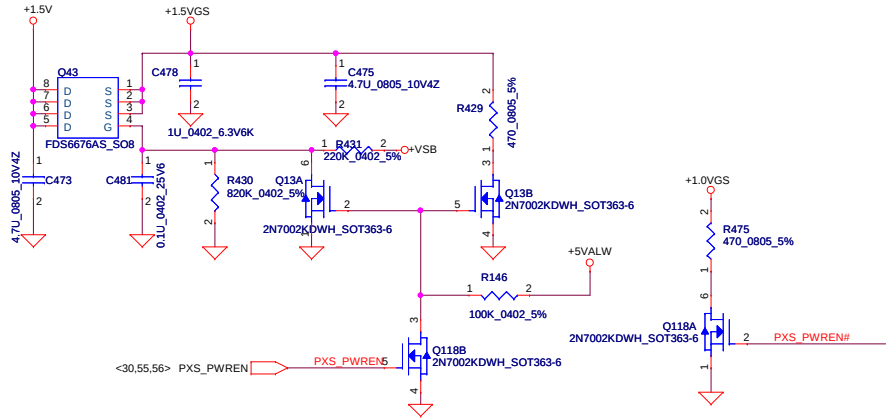
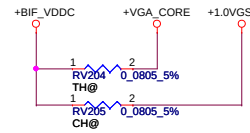
GFX PCIE LANE REVERSAL

LVDS Interface



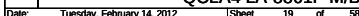
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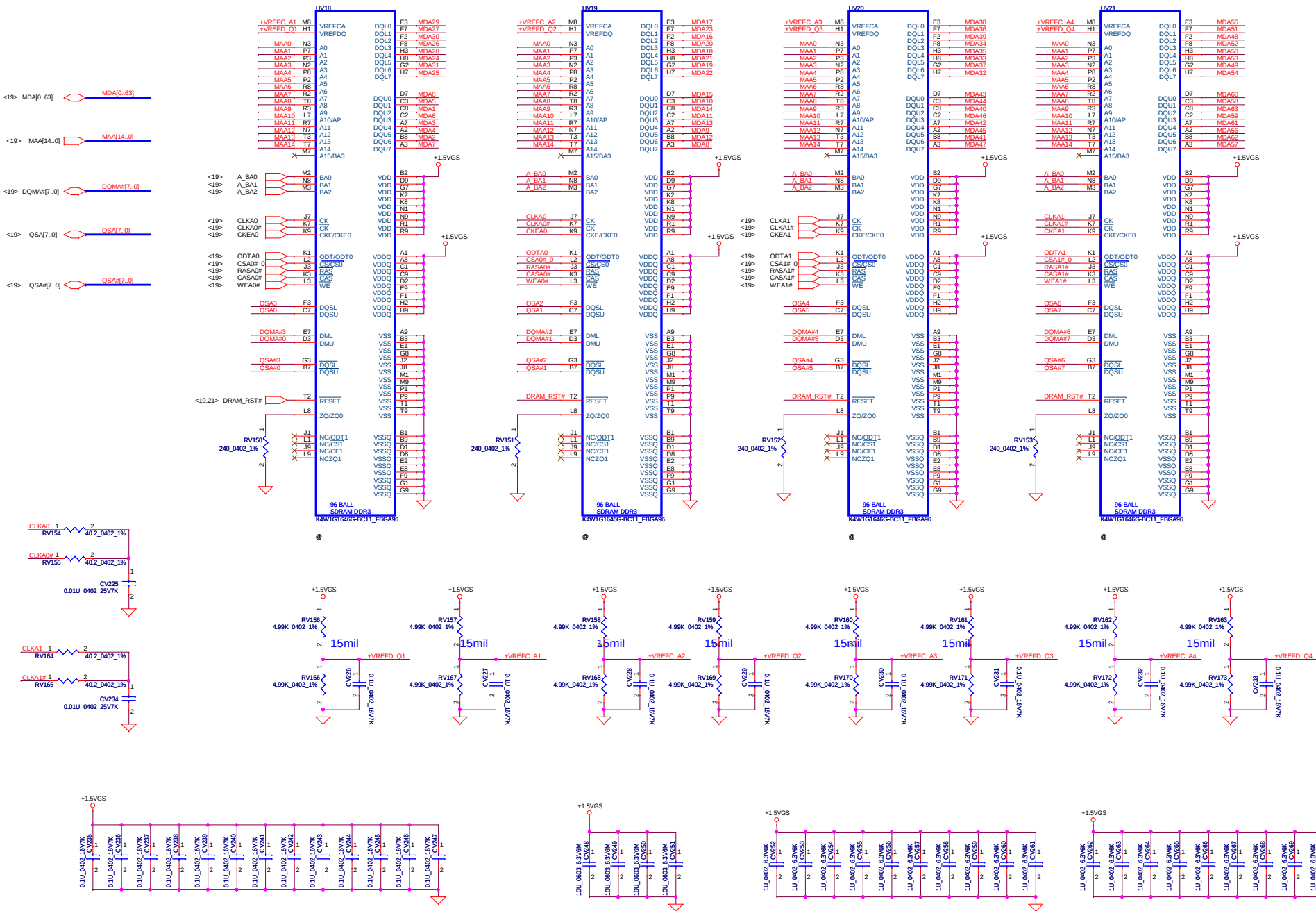


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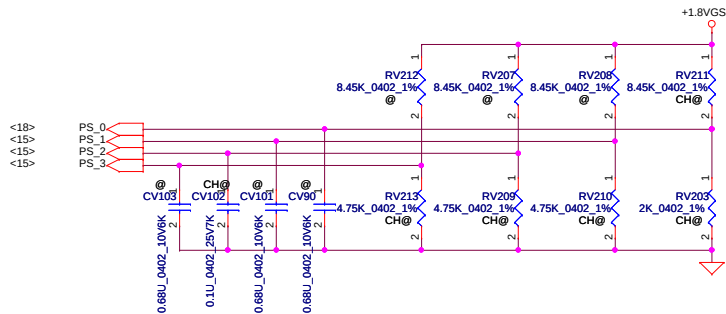
CHANNEL A: 256MB/512MB DDR3



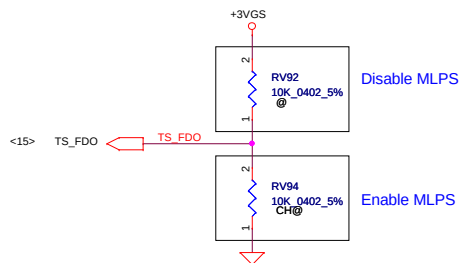
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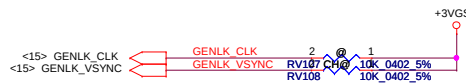


	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45k	2k
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75k
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75k
PS_3[5:1]	1 1	0 0 0	NC	NC	4.75k

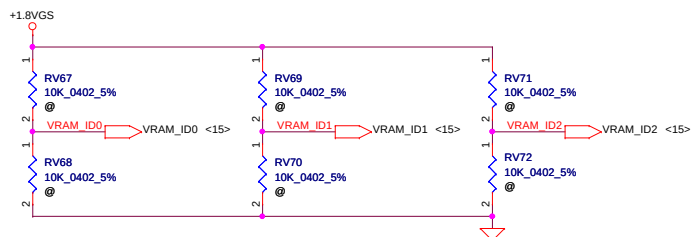


VRAM Straps

	!	"#\$%	"#\$%	"#\$%
64MX16 (1G)	H5TQ1G63DFR-11C			
64MX16 (1G)	K4W1G1646G-BC11	0	0	1
* 128M16 (2G)	H5TQ2G63BFR-11C	1	0	1
* 128M16 (2G)	K4W2G1646C-HC11	0	1	1
		1	1	1



Modify VRAM Straps different from AMD platform
(Because BIOS team want to Common VBIOS,
Seperate VRAM Straps could be easily control VRAM
if AMD & Intel have different VRAM turning setting)



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE
GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

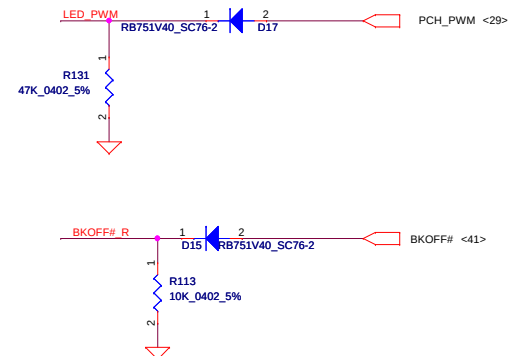
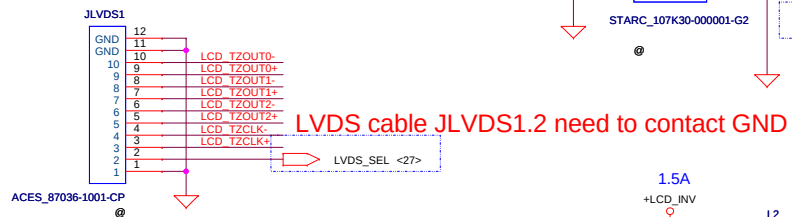
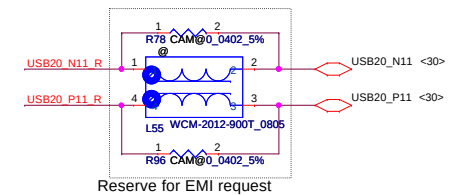
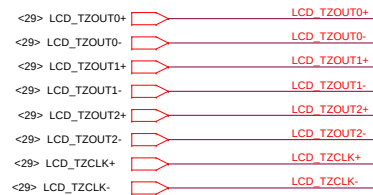
MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsa PRO)	1
PS_1[1]	STRAP_BIF GEN3_EN_A	GPIO2	PCIe Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF CLK_PM_EN	GPIO8	PCIe clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsa PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIe full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN _PINSTRAP[0] AUD_PORT_CONN _PINSTRAP[1] AUD_PORT_CONN _PINSTRAP[2]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
AUD[1] AUD[0]	HSYNC VSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT I NSTALL
RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP " LOW" AND
NOT CONFLICT DURING RESET

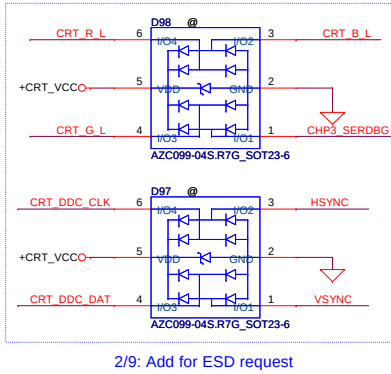
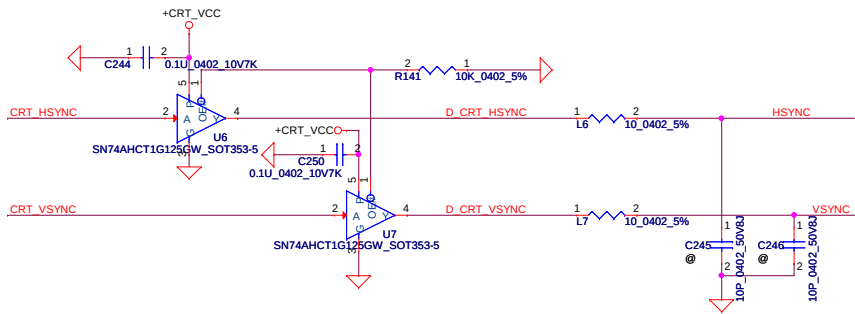
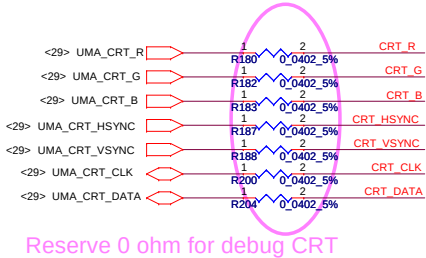
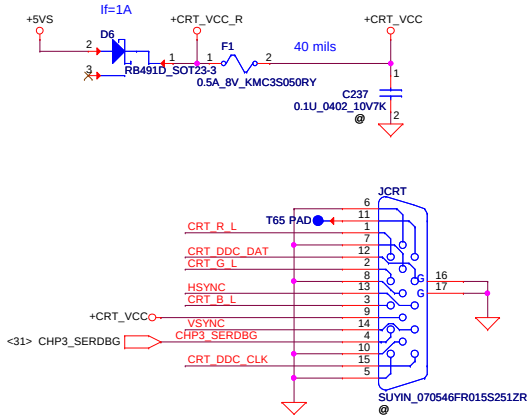
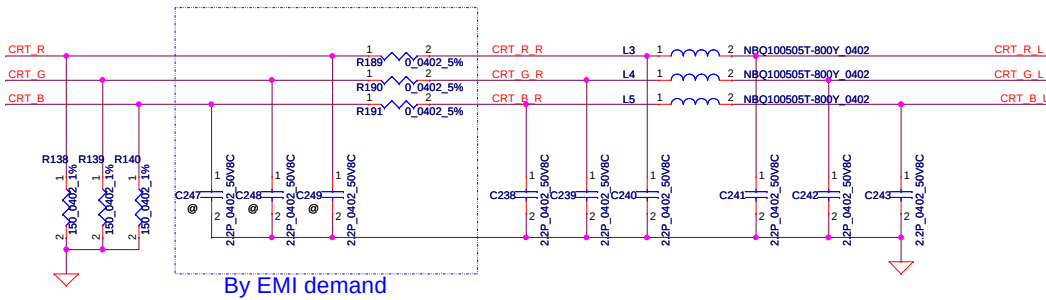
GPIO21 H2SYNC GENERICC GPIO2 GPIO8

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				Date:	Tuesday, February 14, 2012	Sheet 22 of 58

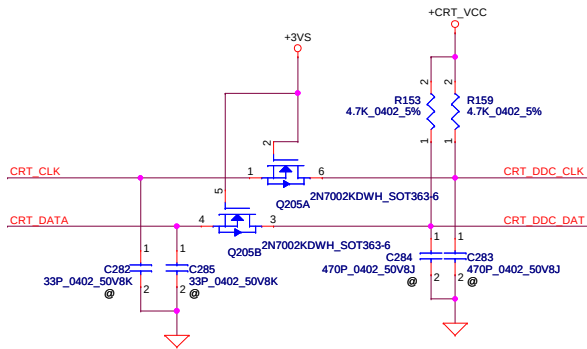
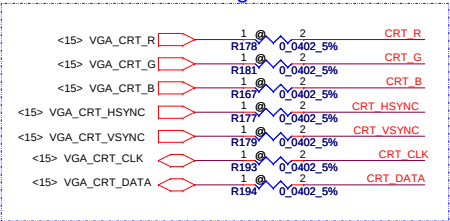


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				Custom	0.2	
				Date:	Tuesday, February 14, 2012	Sheet 23 of 58

CRT CONNECTOR

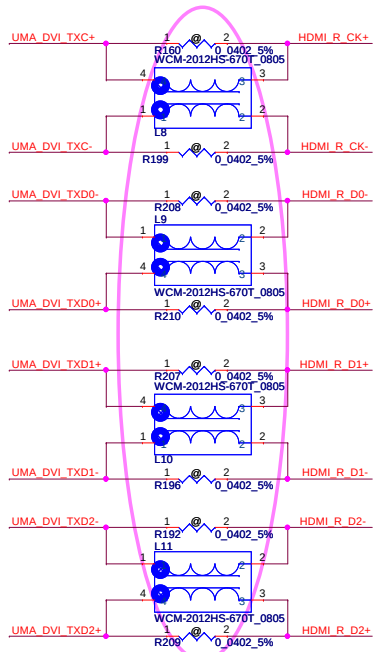


From VGA for debug CRT

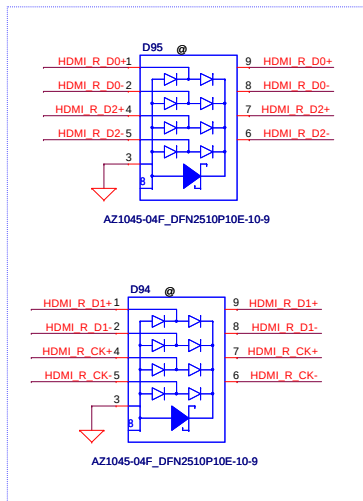


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				Document Number	Rev
				QCLA4 LA-8861P M/B	0.2
				Date	Sheet
				Tuesday, February 14, 2012	24 of 58

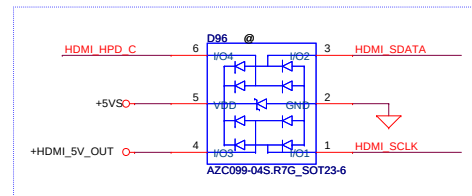
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 <29> UMA_HDMI_TXC- CV337 1 2 0.1U_0402_10V7K UMA_DVI_TXC-
 <29> UMA_HDMI_TX0+ CV338 1 2 0.1U_0402_10V7K UMA_DVI_TXD0+
 <29> UMA_HDMI_TX0- CV339 1 2 0.1U_0402_10V7K UMA_DVI_TXD0-
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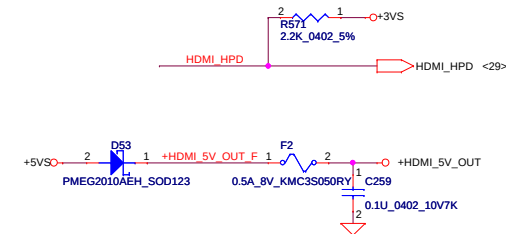
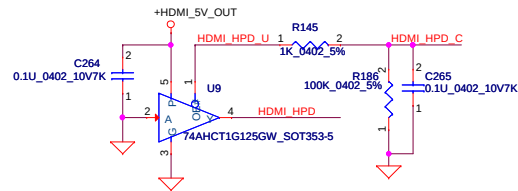
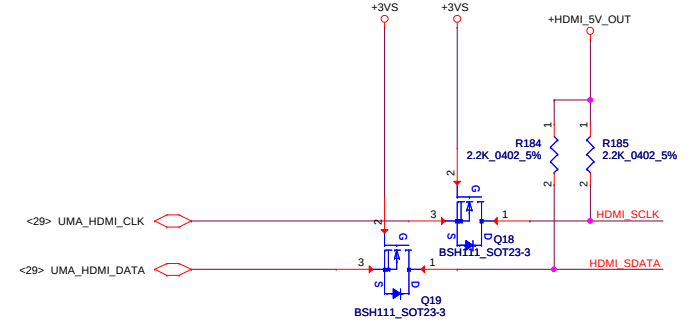
change to 67ohm



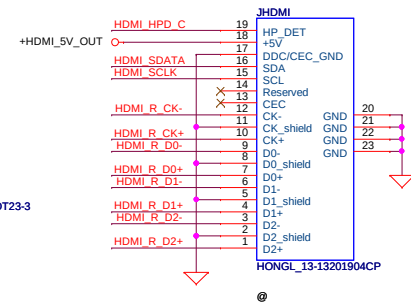
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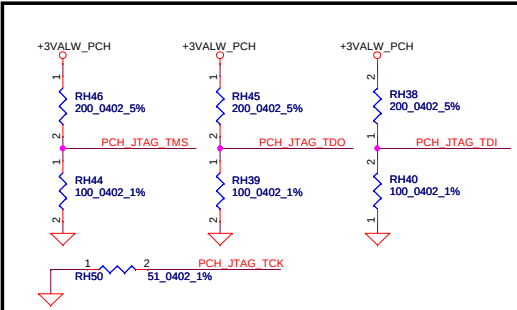
2/9: Add for ESD request



HDMI Connector

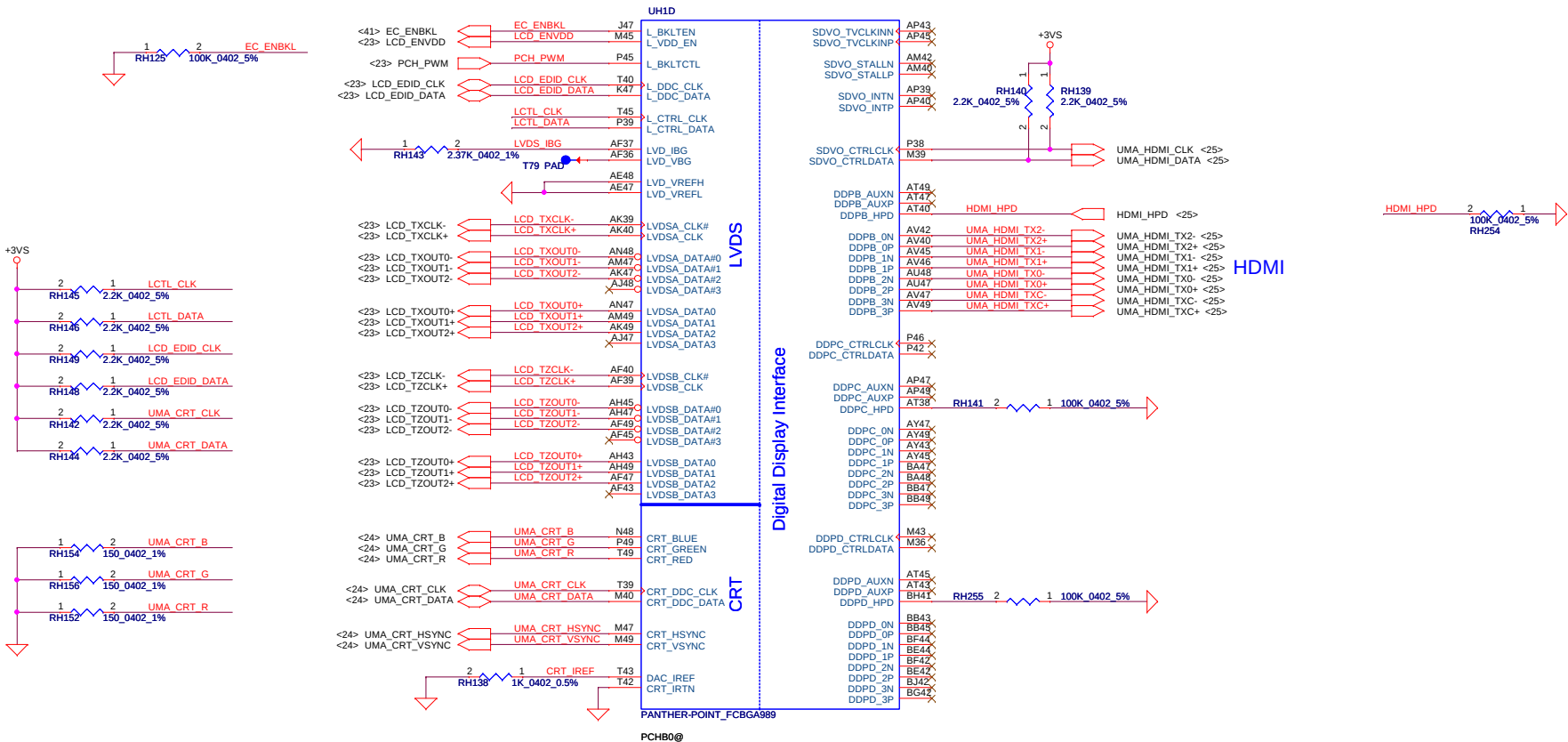


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2011/11/11				2012/12/31				Title			
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				QCLA4 LA-8861P M/B				Date			
				Tuesday, February 14, 2012				Sheet			
				25				of			
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				0.2							

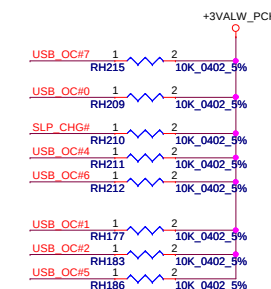
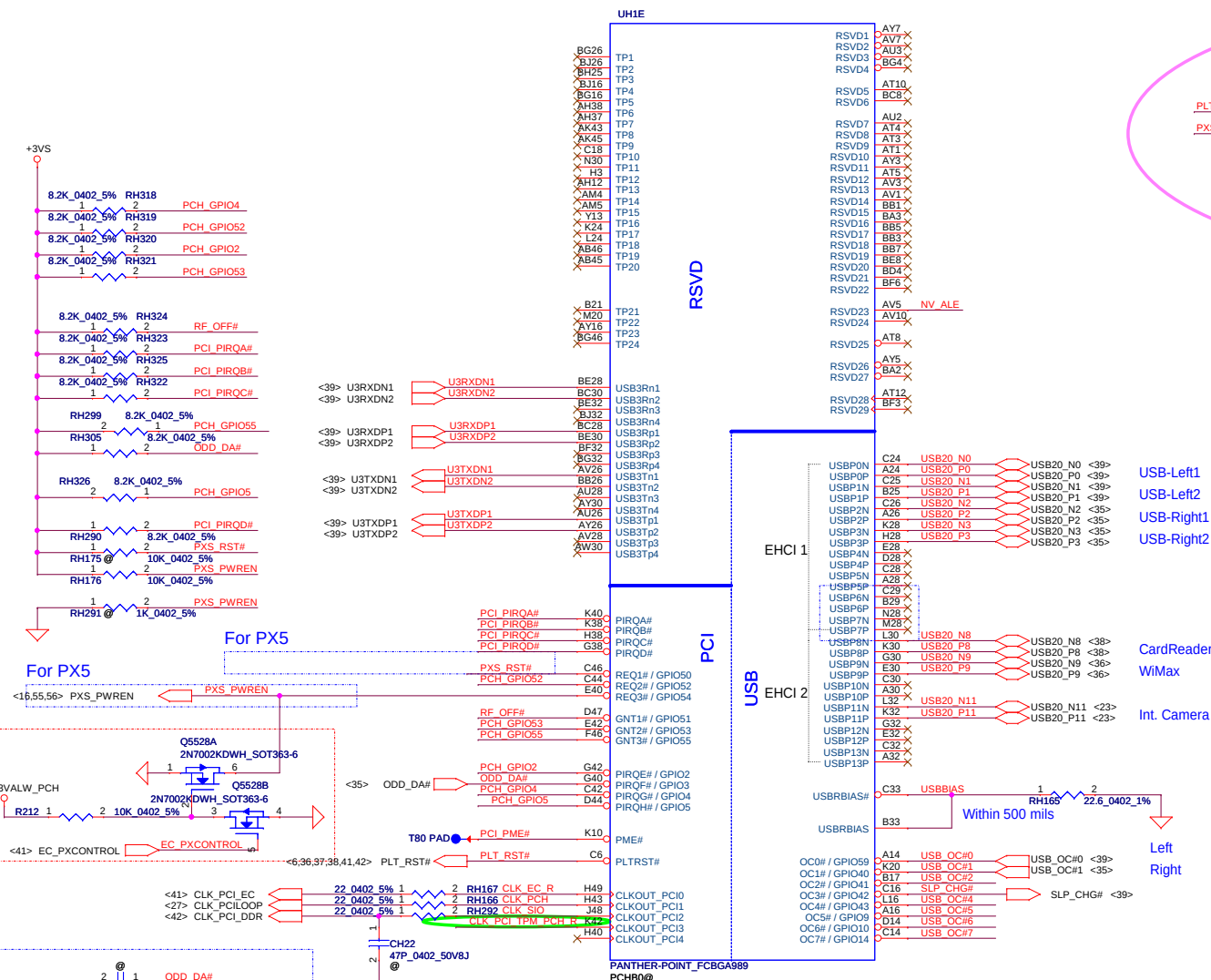
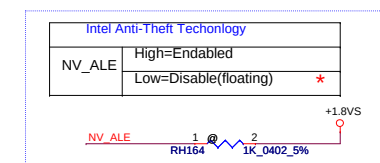
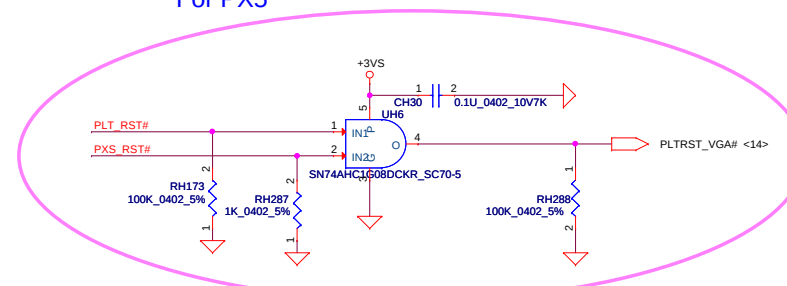


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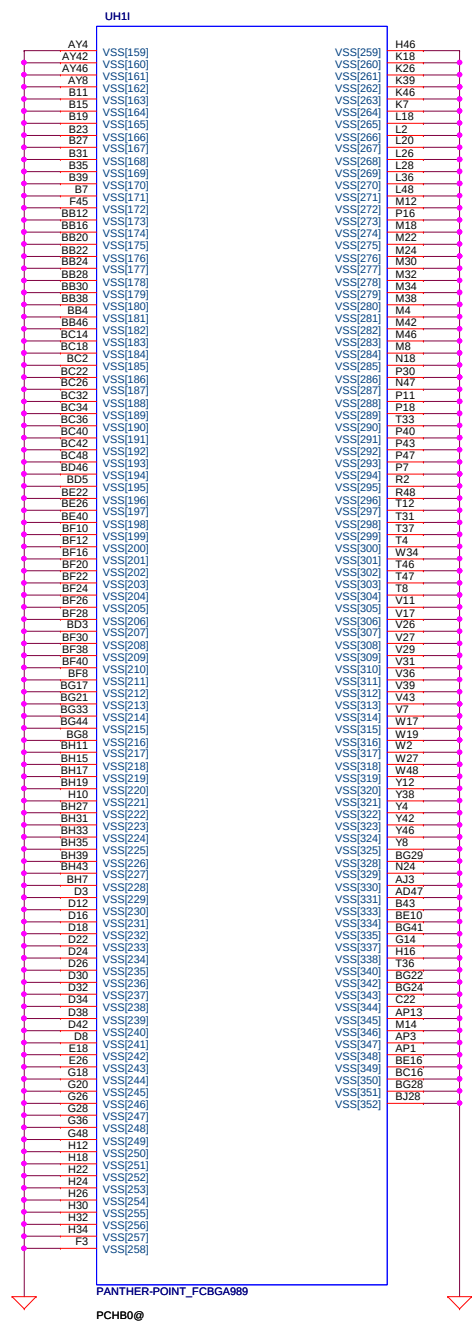
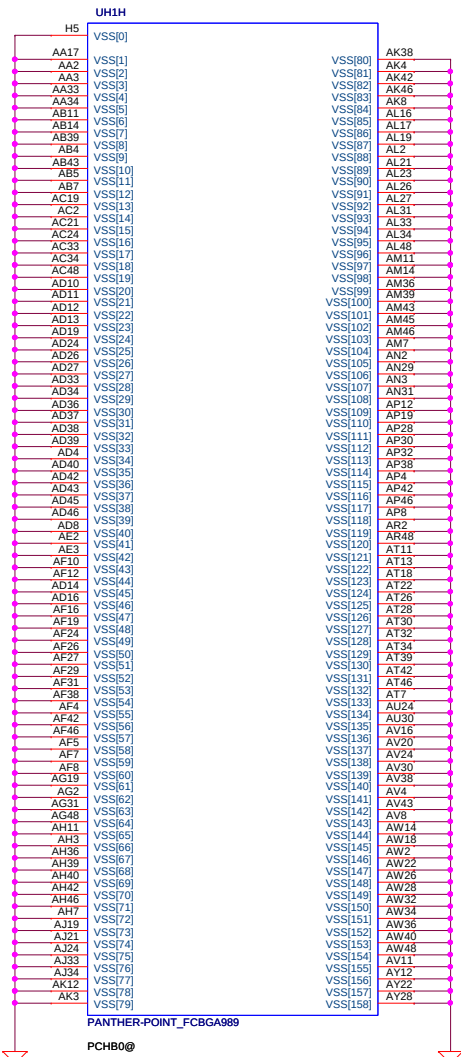
Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	★ Low= A16 swap override Enable High= A16 swap override Disable

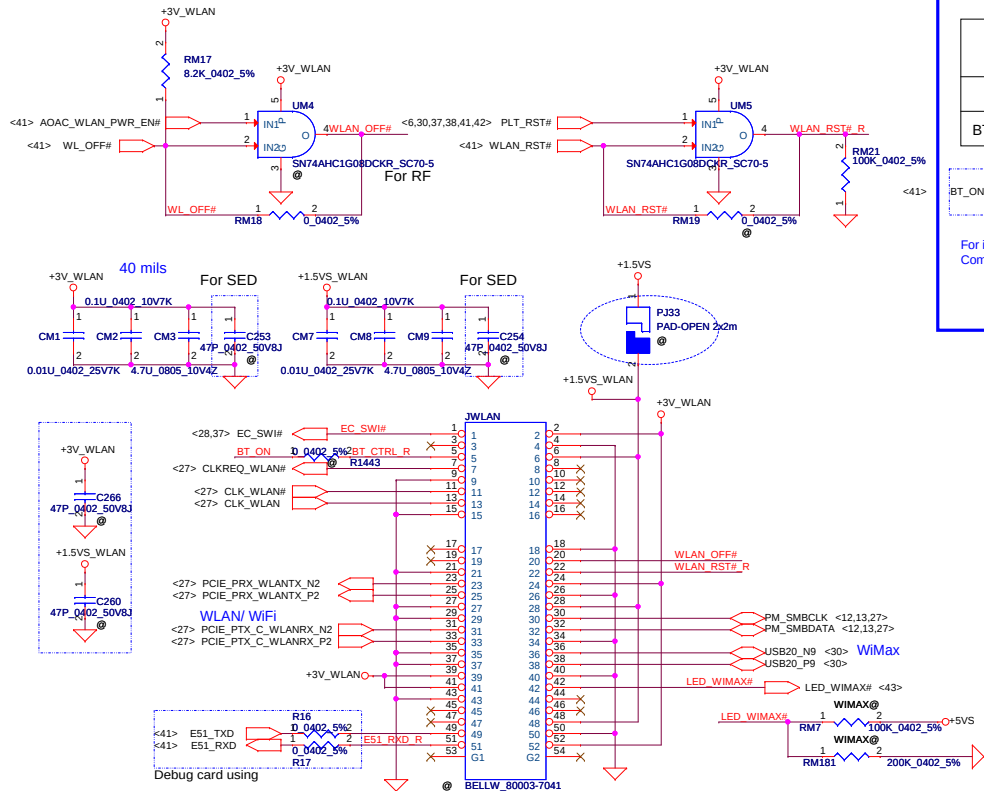
<38> CLK_PCI_TPM_PCH 

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						Doc Number	QCLA4 LA-8861P M/B			Rev	0
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax



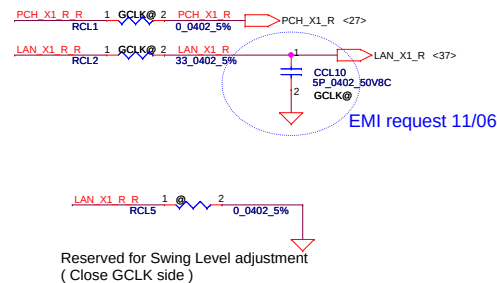
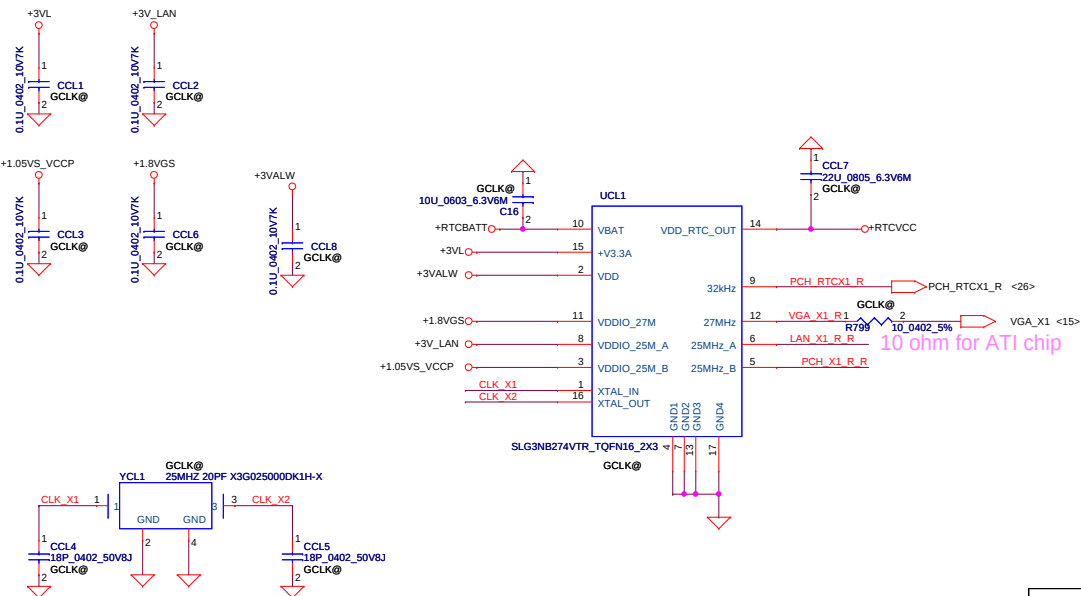
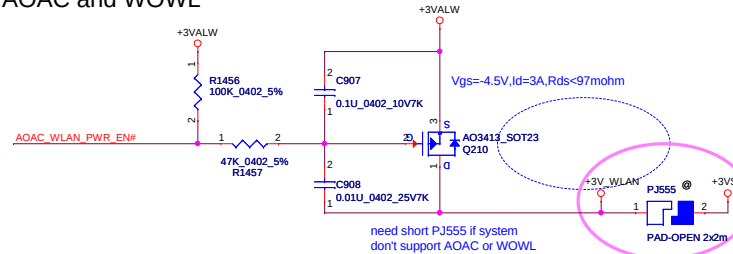
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON#	H	L

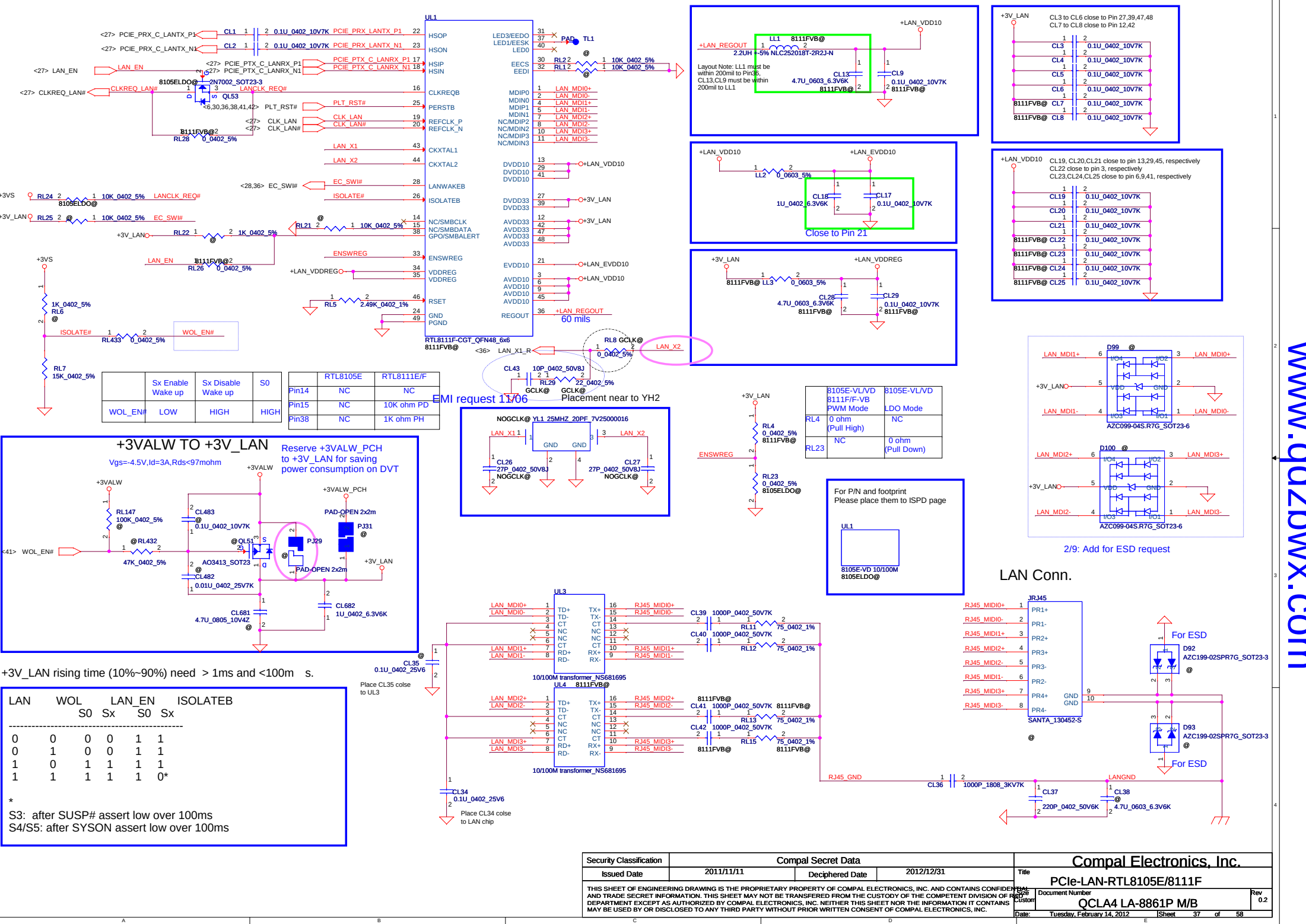
BT_ON# BT_ON 1 R327 1K 0402_5% 2 E51 RXD R

For isolate Intel Rainbow Peak and Compal Debug Card.

+3VALW TO +3V_WLAN for AOAC and WOWL

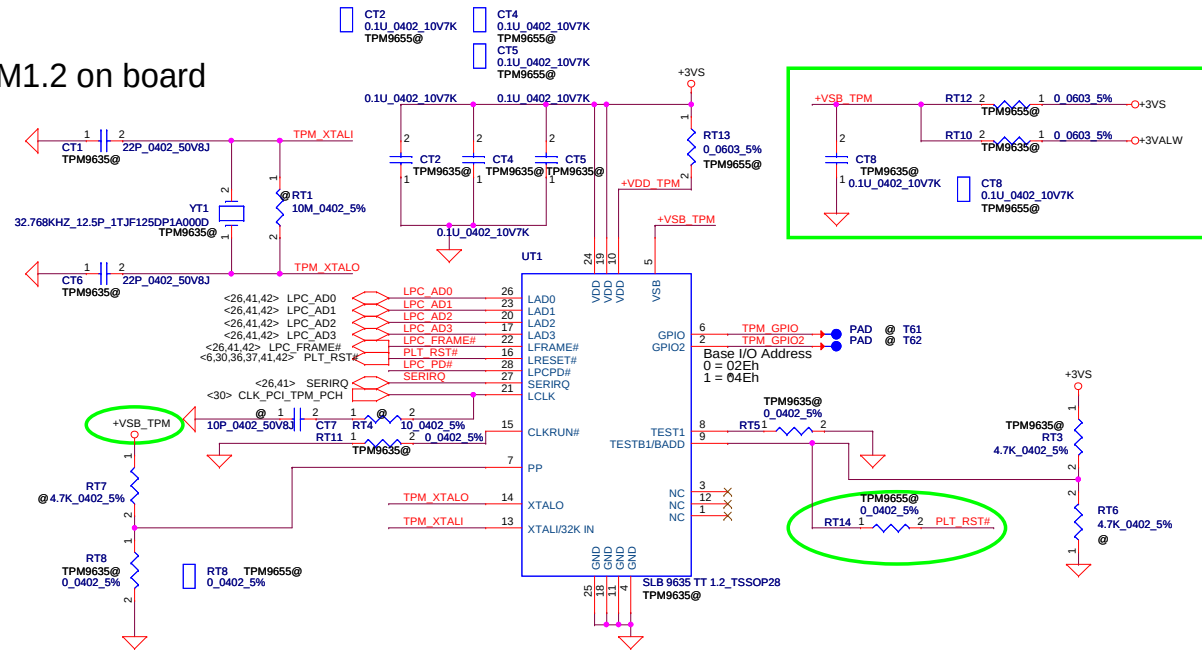
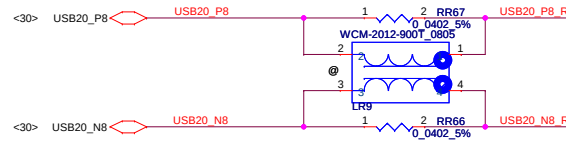
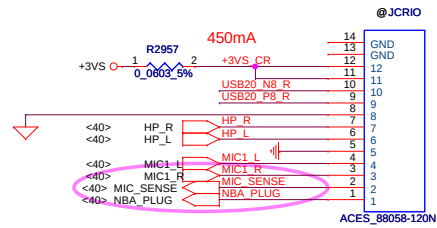


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				Size Document Number
				QCLA4 LA-8861P M/B
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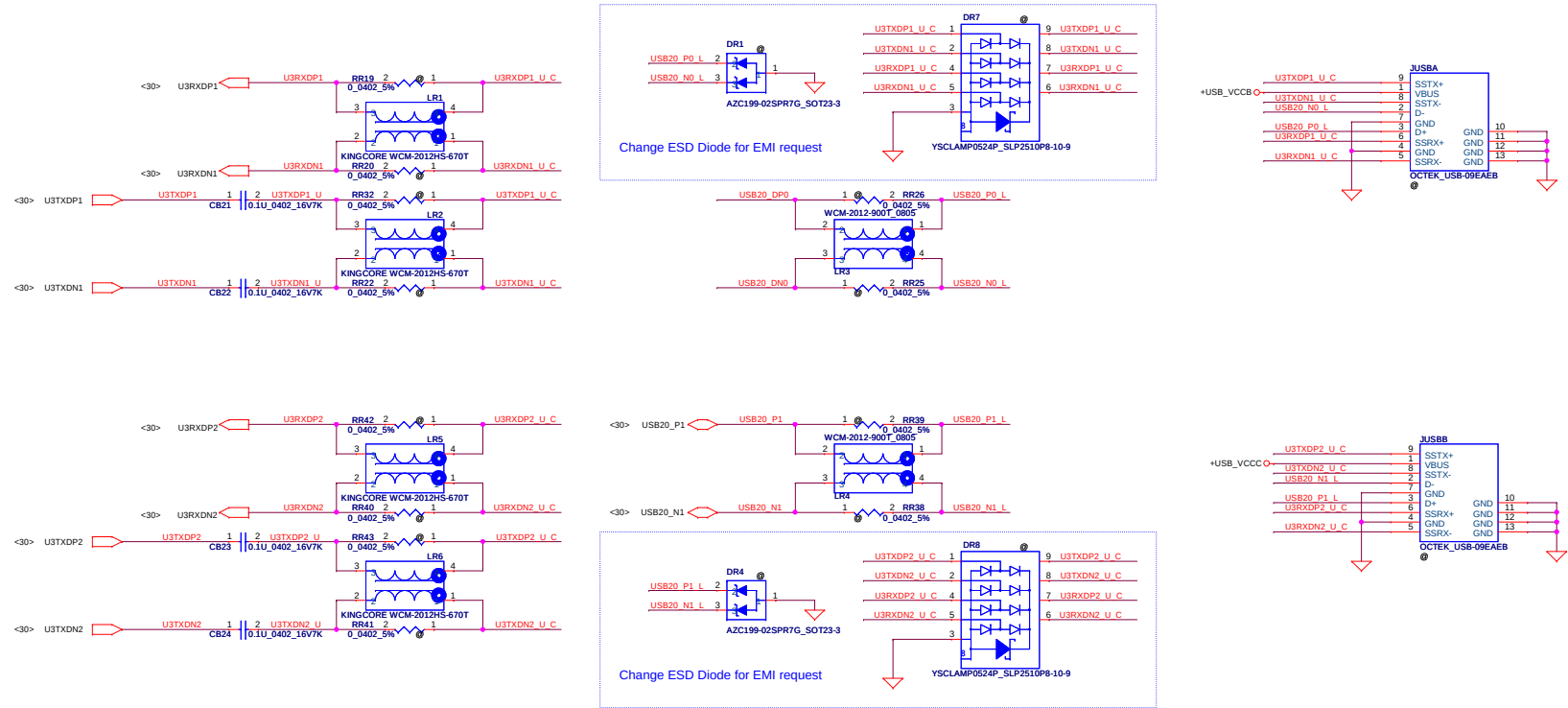
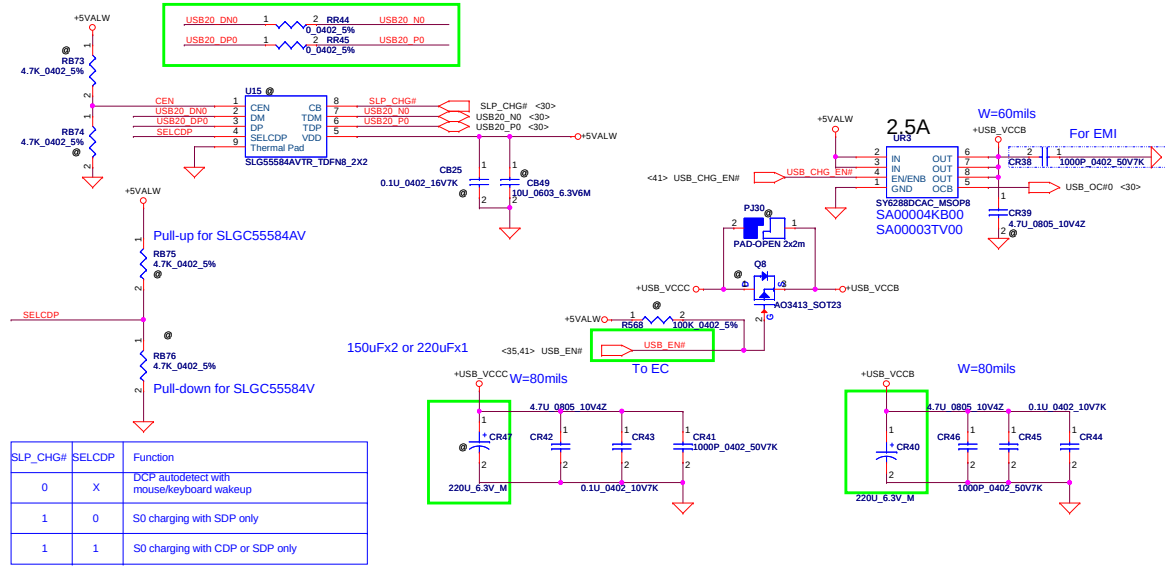
TPM1.2 on board



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				Date:	Tuesday, February 14, 2012	Sheet 38 of 58

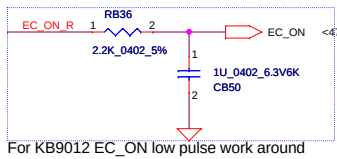
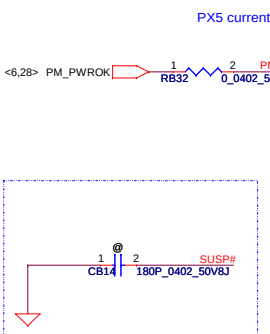
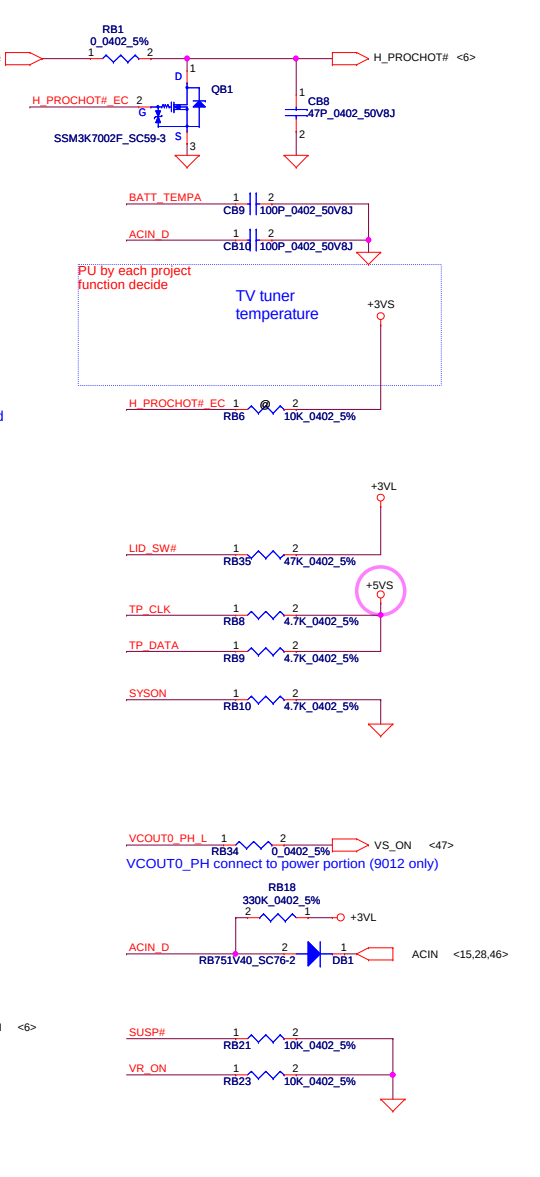
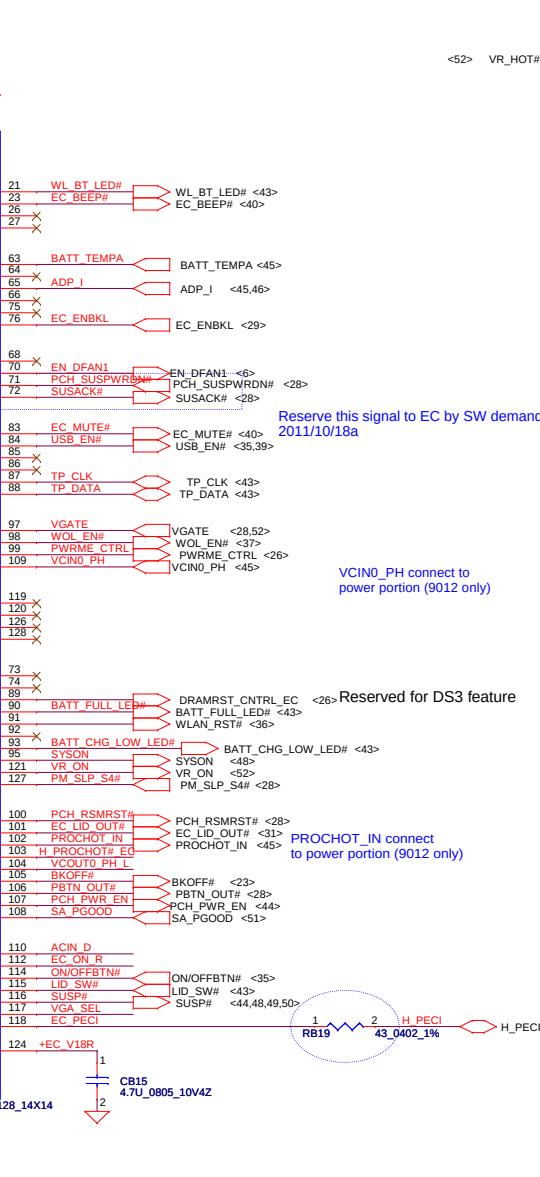
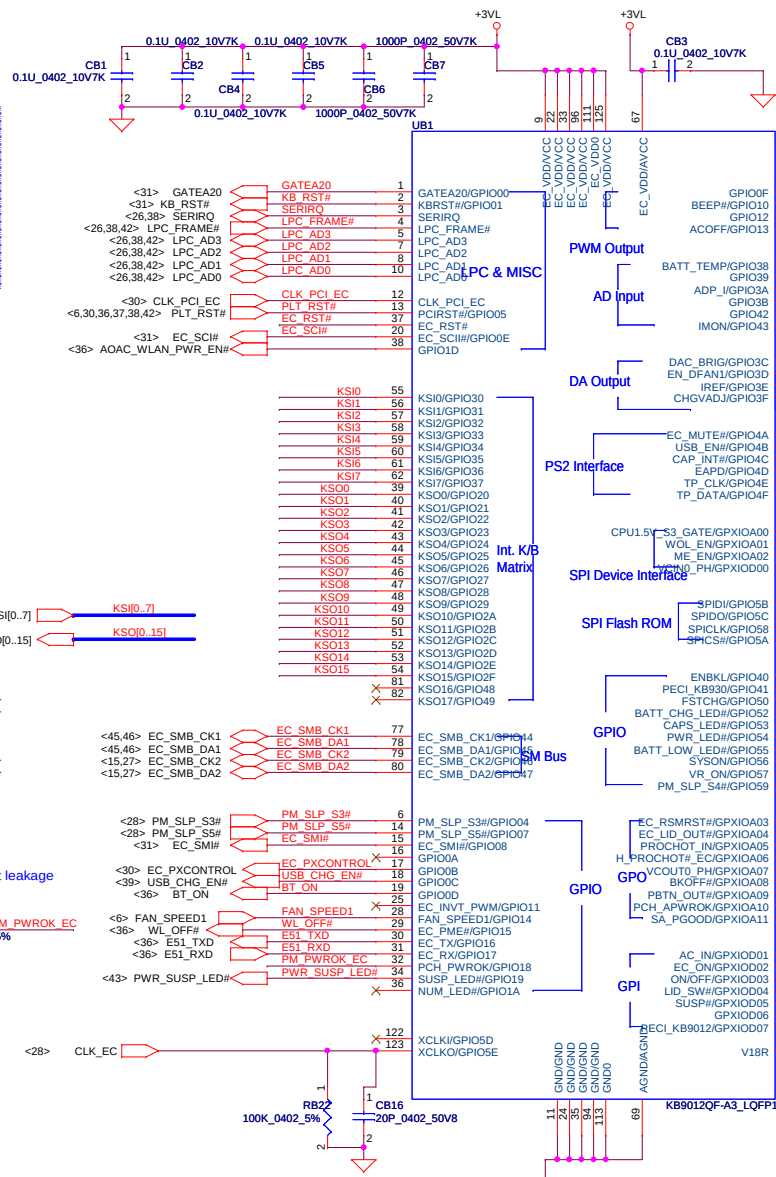
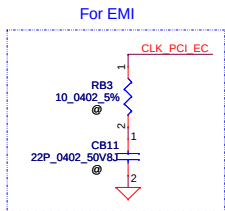
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Sleep & Charge Function



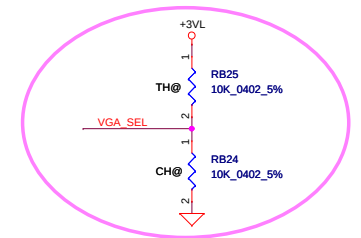


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				Size	Custom	
				Date:	Tuesday, February 14, 2012	Sheet 40 of 58

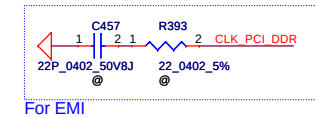
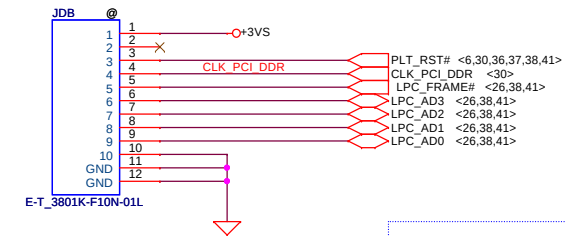


Voltage Comparator Pins FOR 9012 A3

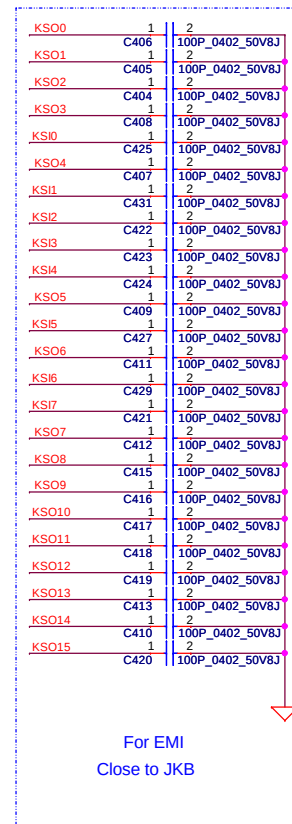
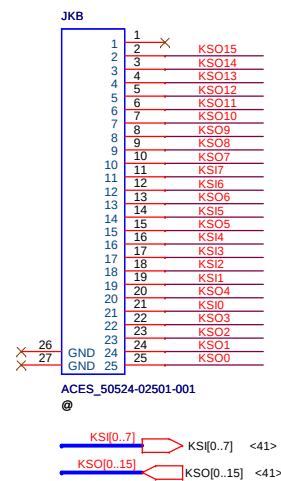
VIN0 pin109	>1.2V	<1.2V
VIN1 pin102	HIGH	LOW
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



VGA_SEL (for thermal sensor)	High	Low
Pin117	Thames	Chelsea
Address	82h	9Ah

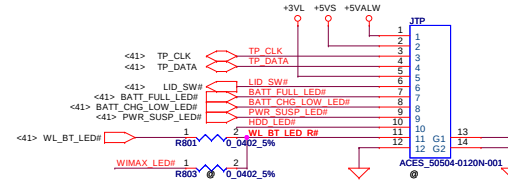


KEYBOARD CONN.

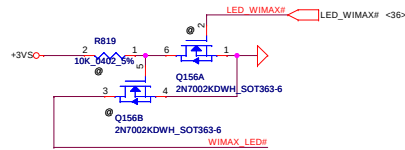


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Size		Document Number			Rev
		QCLA4 LA-8861P M/B			0.2
Date:		Tuesday, February 14, 2012		Sheet	42 of 58

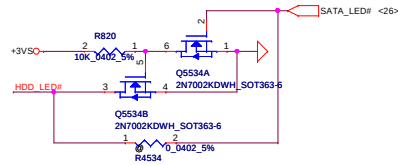
Touchpad Connector



WiMAX LED



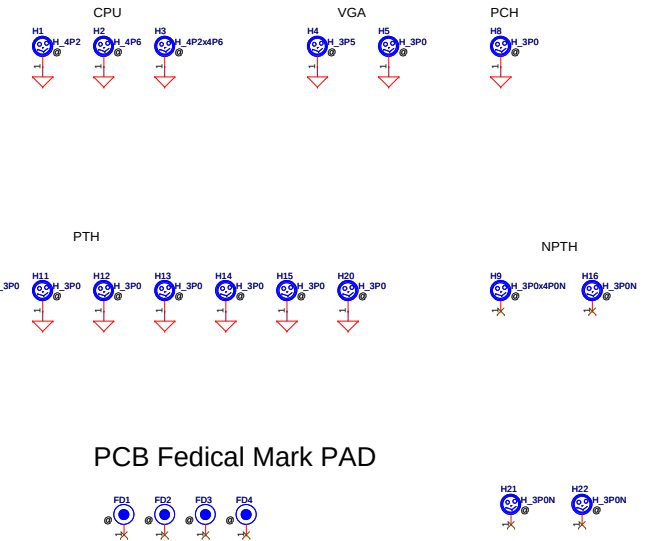
SATA LED



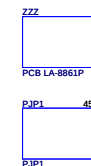
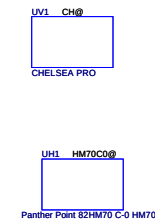
ESD solution

EMI solution

Screw Hole



ISPD



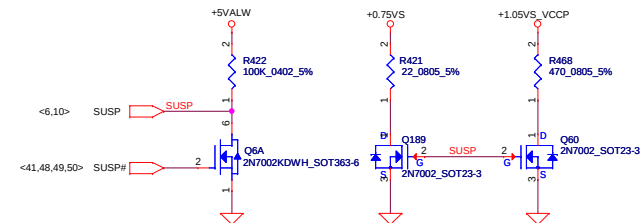
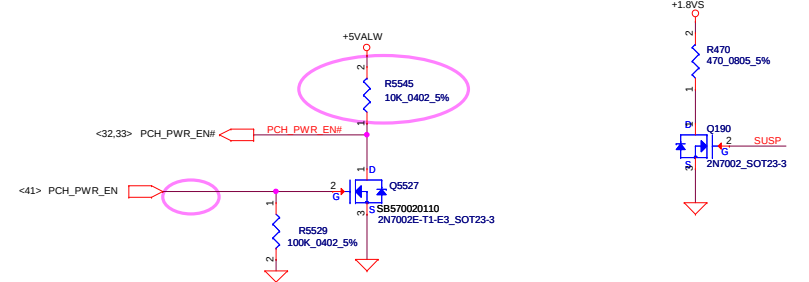
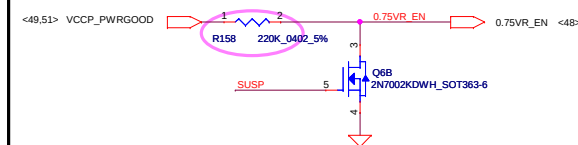
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Issued Date	2011/11/11	Deciphered Date	2012/12/31	Title	PWR/TP/LED/LP/LS/Screw
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				Rev	0.2

[illegible]

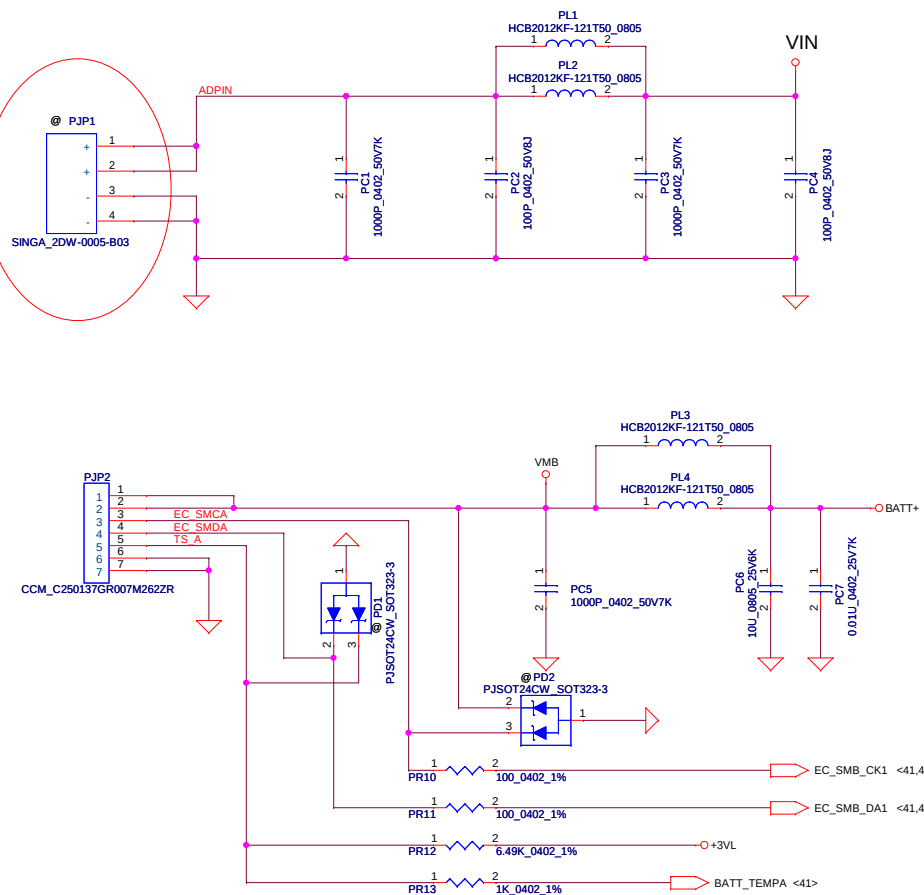
change R409 to 120k 5%

[illegible]

For S3 CPU Power Saving

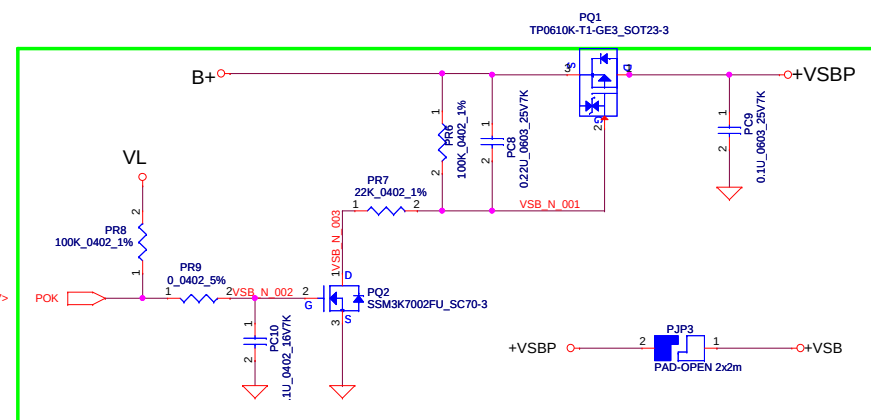
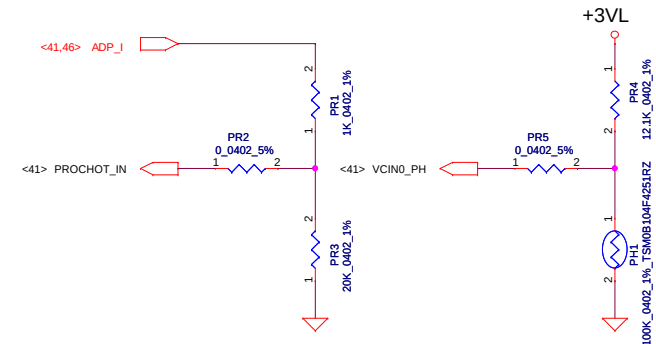
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/11	Deciphered Date	2012/12/31	Title	DC-DC INTERFACE
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				Date	QCLA4 LA-8861P M/B
				Date	Tuesday, February 14, 2012
				Sheet	44 of 58
				Rev	0.2

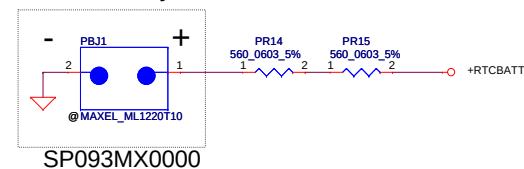


PH1 near CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

Please locate these parts
Near EC chip



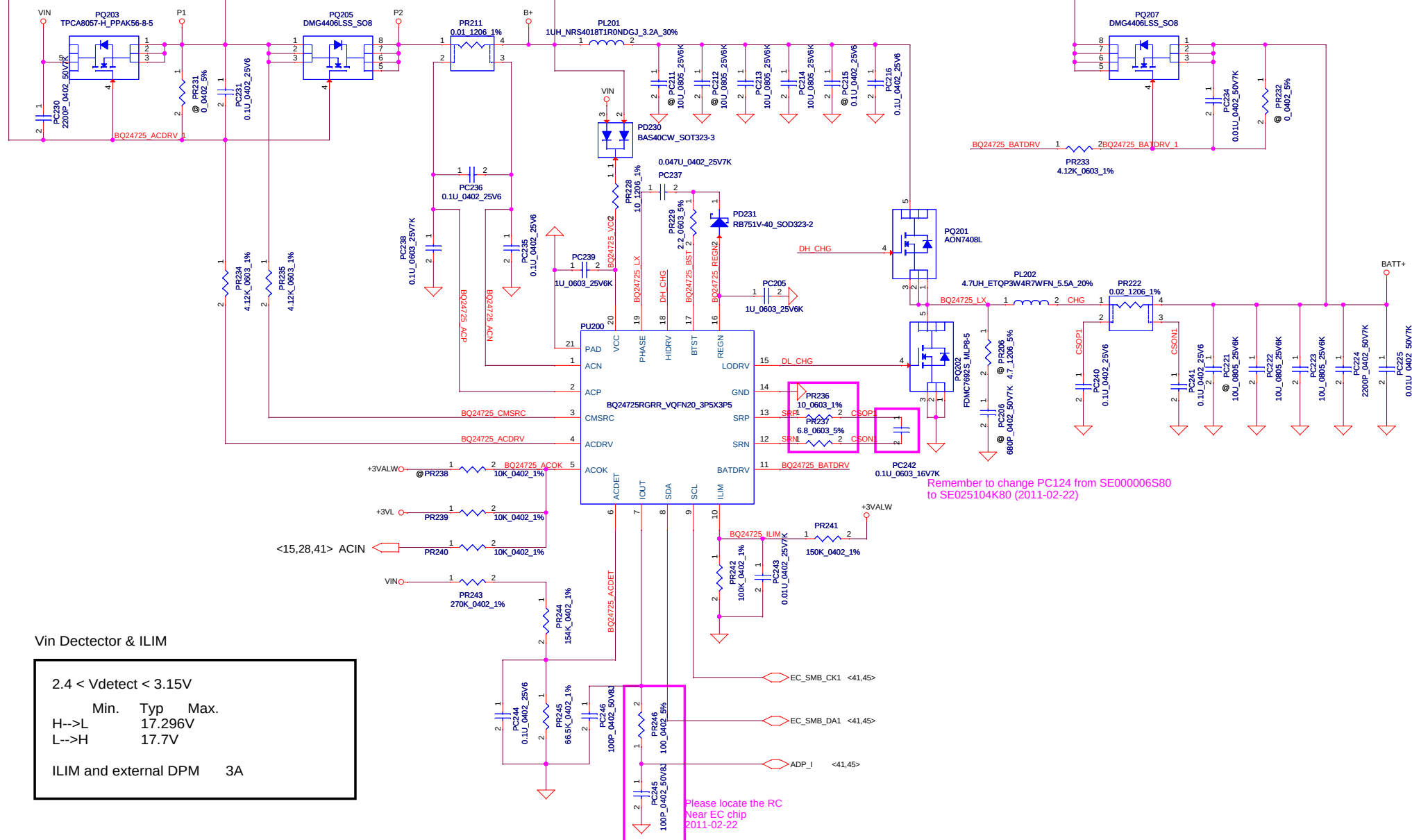
RTC Battery



SP093MX0000

Security Classification		Compal Secret Data				Compal Electronics, Inc.								
Issued Date		2009/01/23		Deciphered Date		2010/01/23		Title		PWR-DCIN / BATT CONN / OTP				
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										Date:		Tuesday, February 14, 2012		Sheet

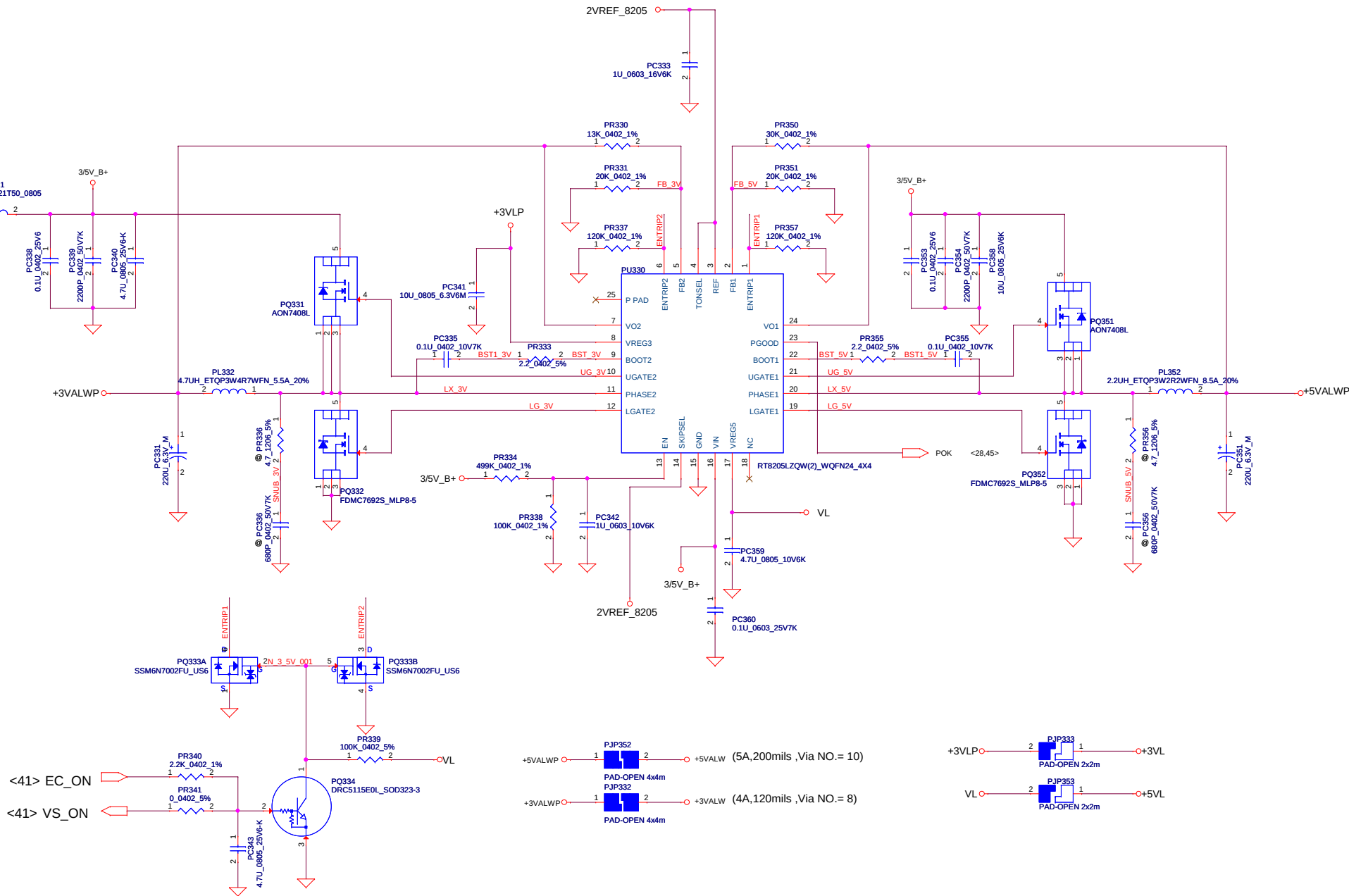
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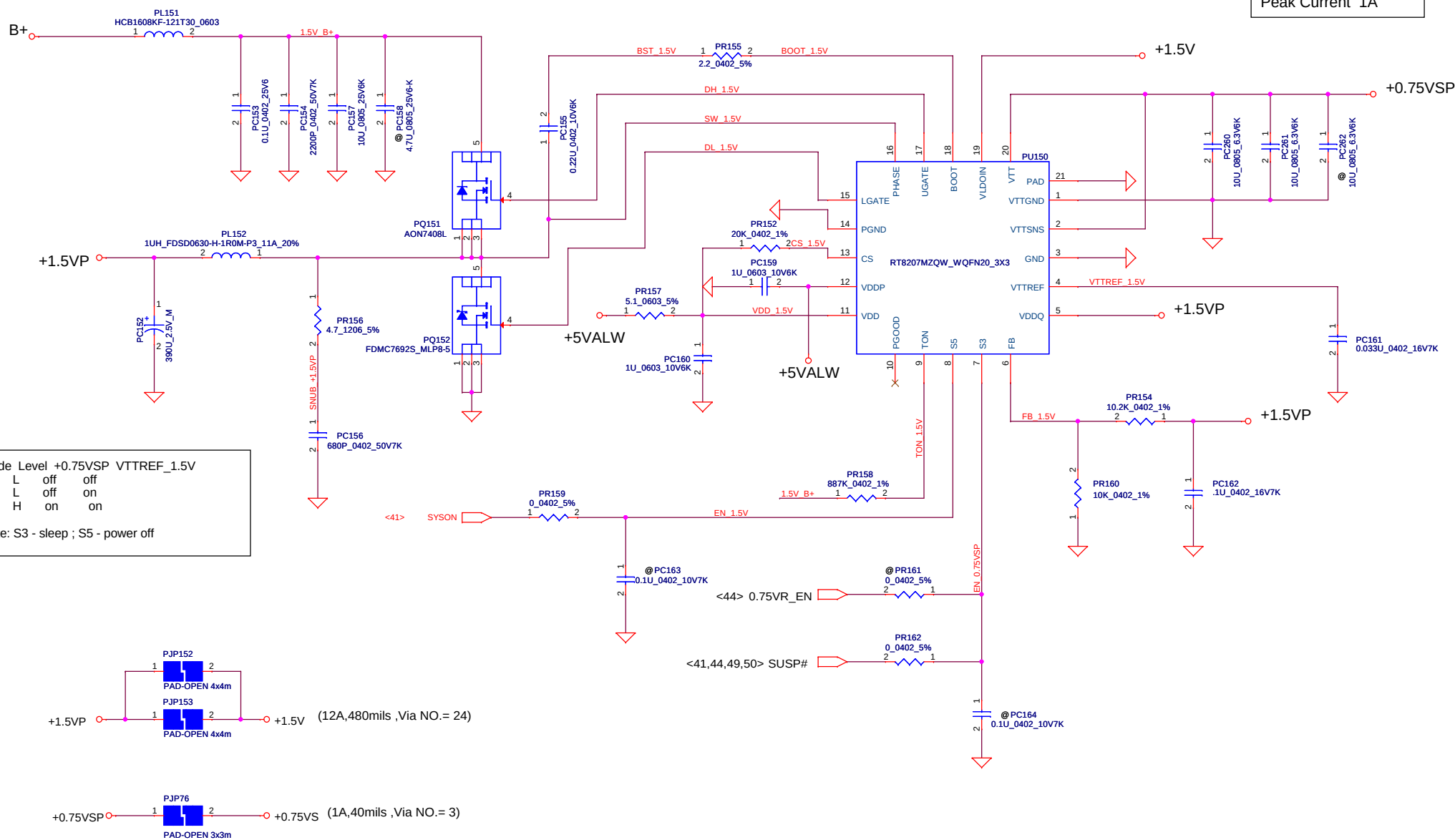
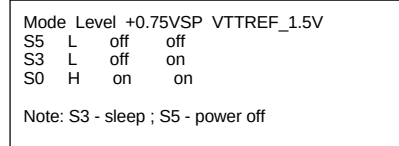
2.4 < Vdetect < 3.15V		
Min.	Typ	Max.
H-->L	17.296V	
L-->H	17.7V	
ILIM and external DPM		3A

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title PWR-CHARGER		
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					SAMSUNG	0.2
				Date:	Tuesday, February 14, 2012	Sheet 46 of 58

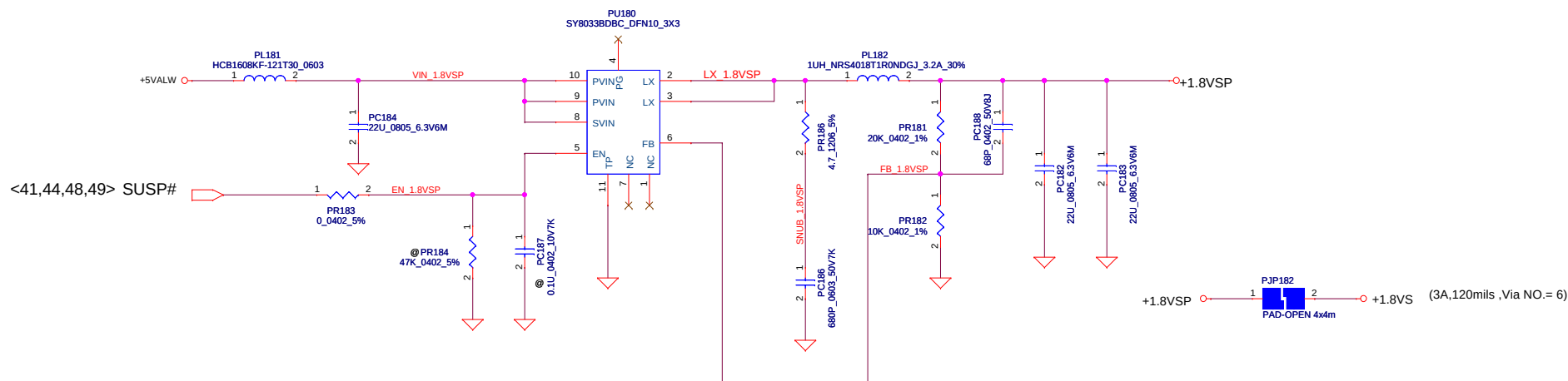
www.qdzbxw.com



Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	PWR-3.3VALWP/5VALWP	
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				QCLA4 LA-8861P M/B	0.2
				Date: Tuesday, February 14, 2012	Sheet 47 of 58



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	PWR-1.5VP / +0.75VSP
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				Custom	0.2
				SAMSUNG	
Date:	Tuesday, February 14, 2012	Sheet	48	of	58



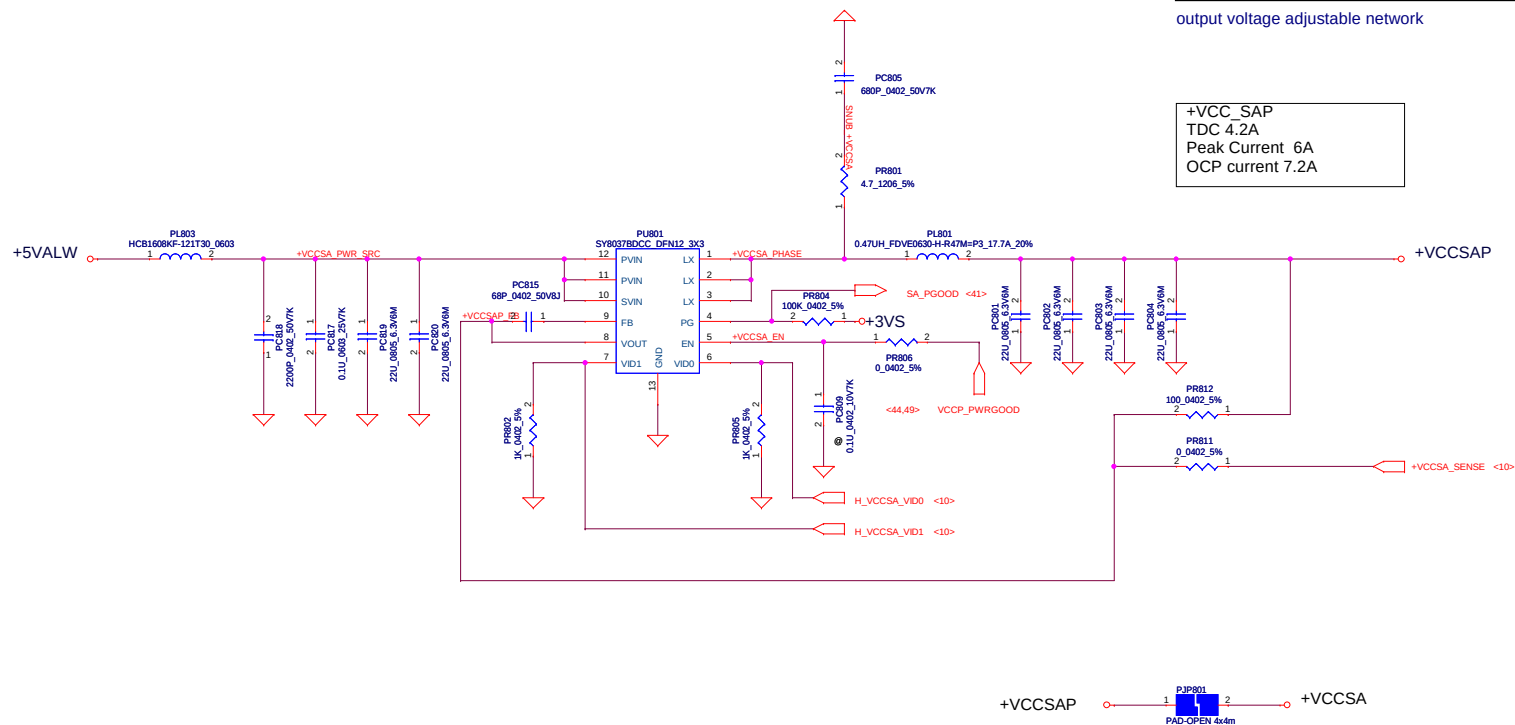
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-1.8VSP	
Size	Document Number	SAMSUNG			Rev
					0.2
Date:	Tuesday, February 14, 2012	Sheet	50	of	58

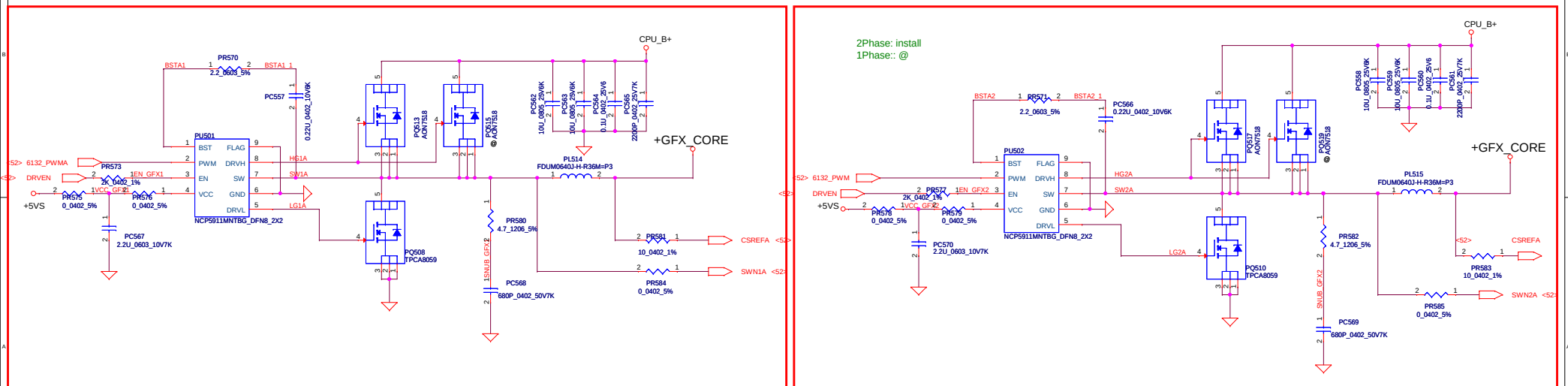
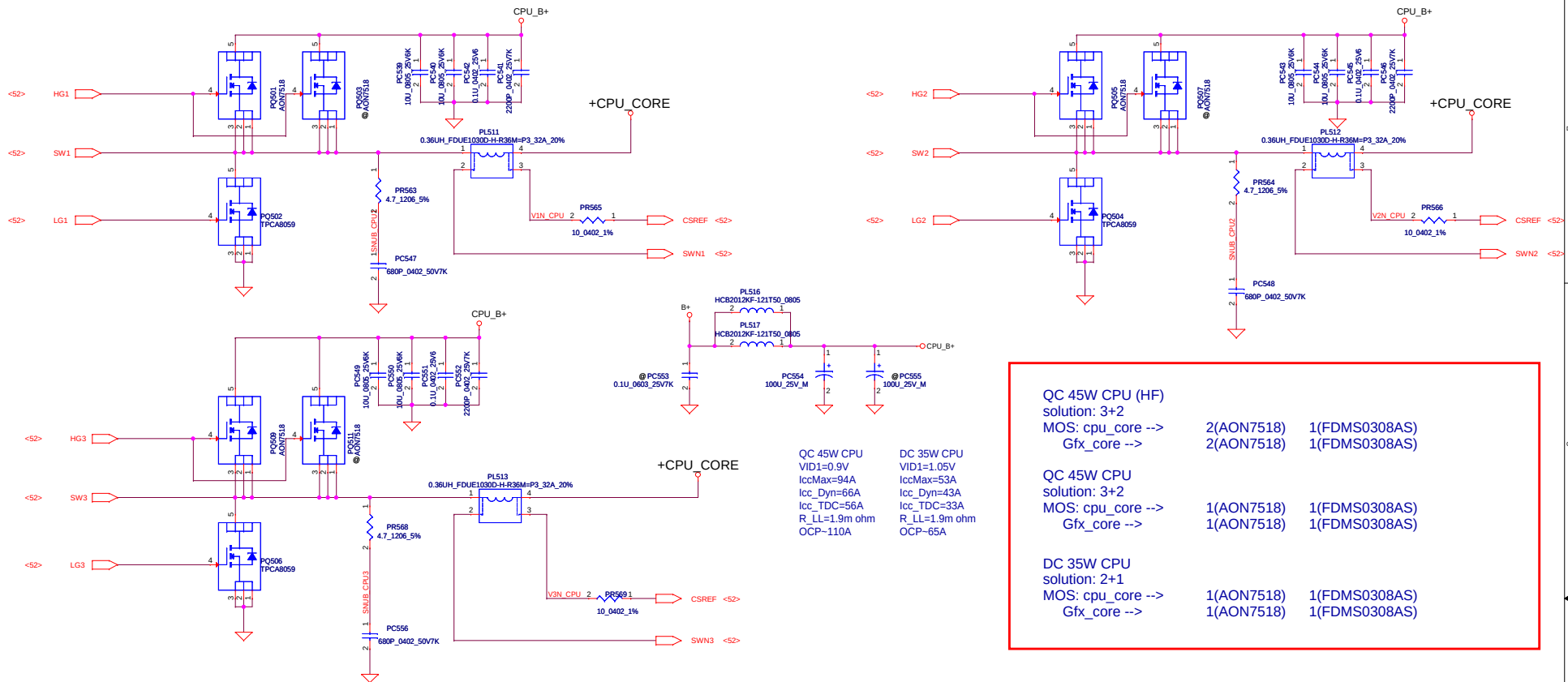
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCF current 7.2A

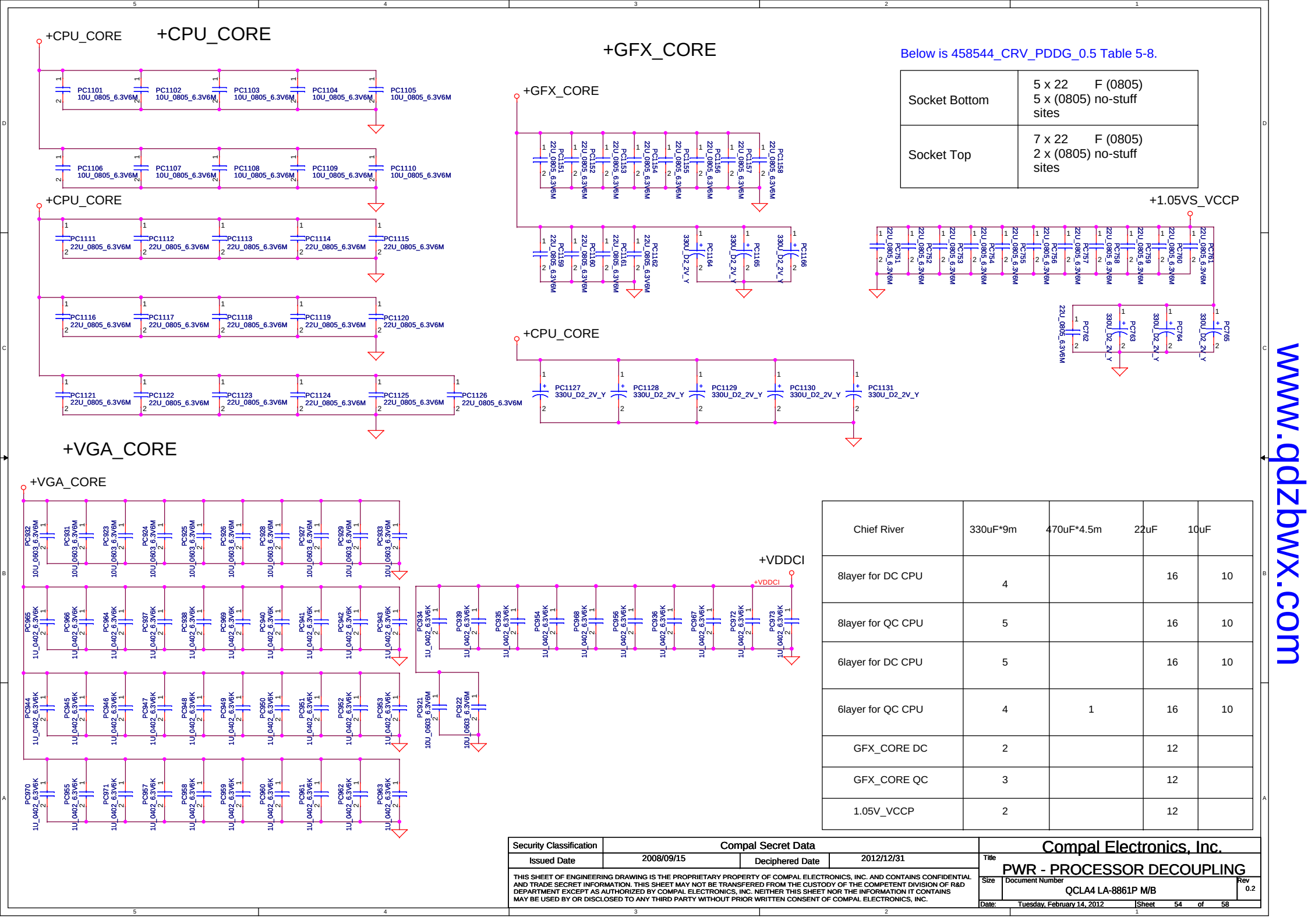




QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP=55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP=40A

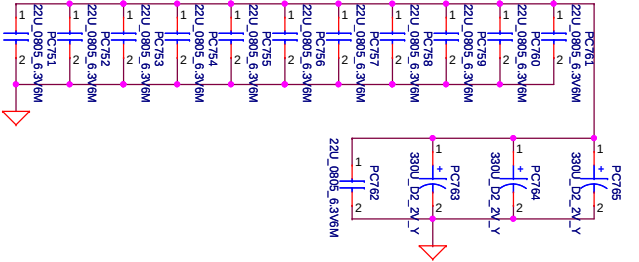
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title
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Size	Document Number	QCL70		Rev 0.2
Date:	Tuesday, February 14, 2012	Sheet	53	of 58



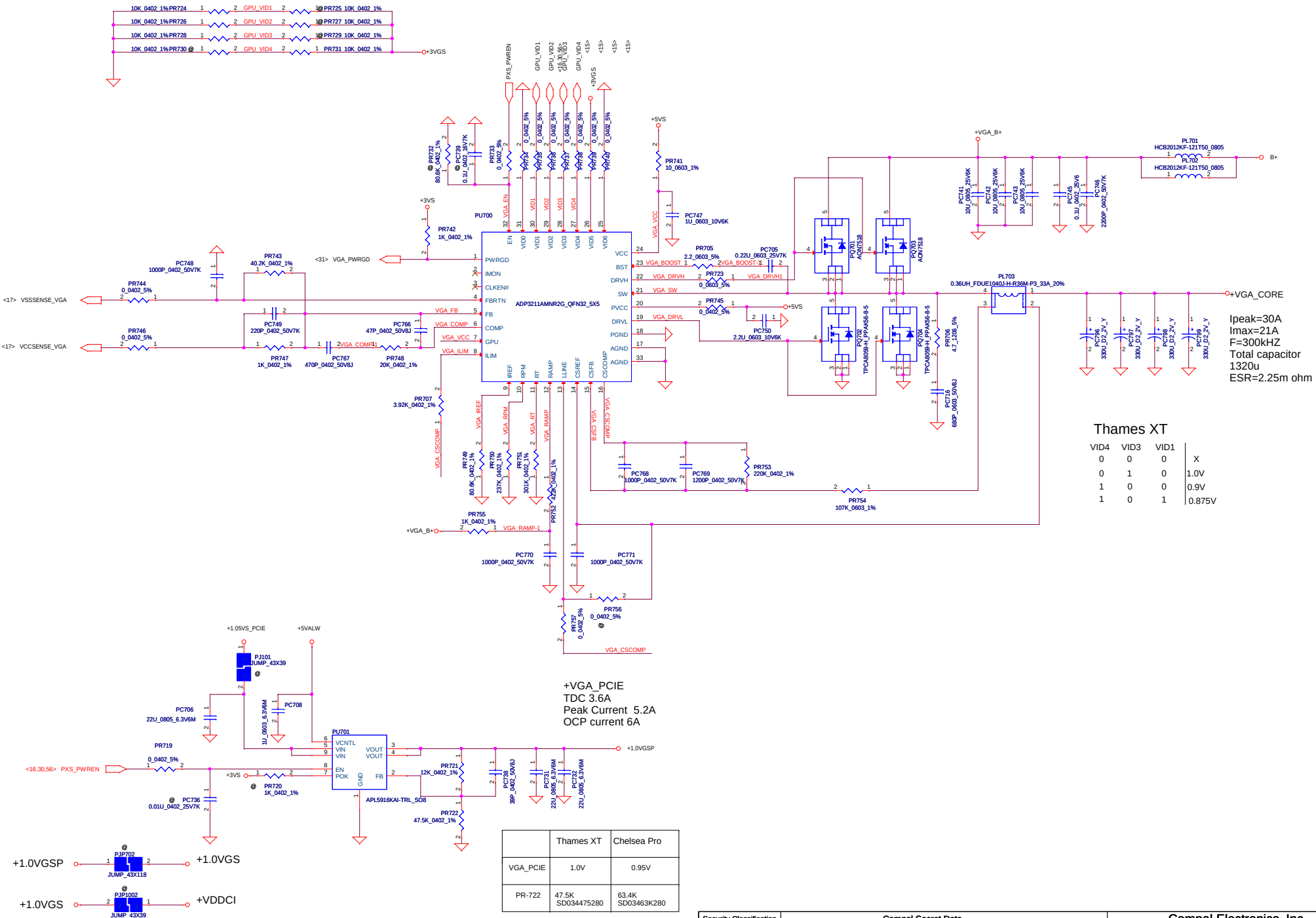
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 F (0805) 2 x (0805) no-stuff sites

+1.05VS_VCCP



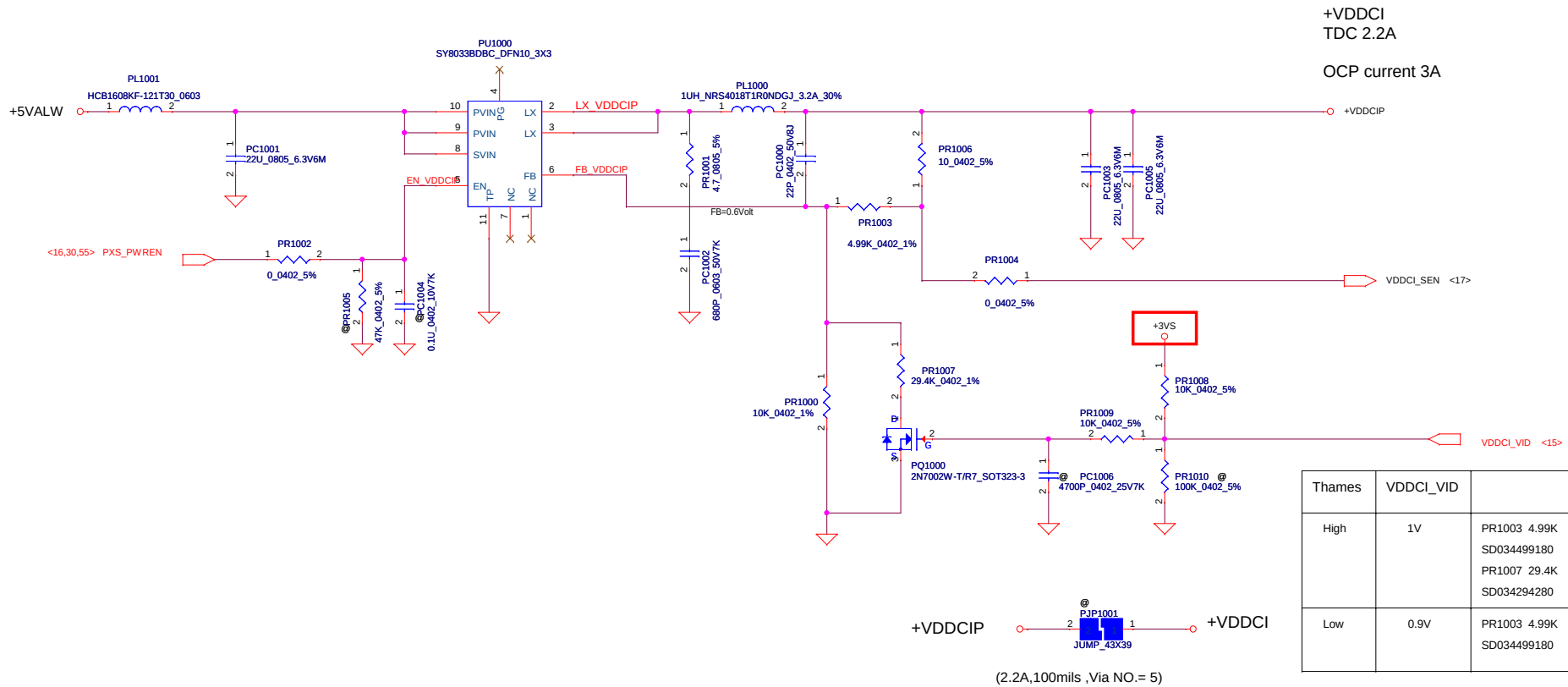
Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	



Thames XT

VID4	VID3	VID1	
0	0	0	X
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

$I_{peak}=30A$
 $I_{max}=21A$
 $F=300kHz$
 Total capacitor
 1320u
 $ESR=2.25m\ ohm$



1. 2011/09/29

P51-PWR_+3VALWP/+5VALWP

2. 2011/09/29

P53-PWR_+1.05VS_VCCP/+16V

SP

3. 2011/09/29

P54-PWR_+VCCSAP/1.8VSP

4. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

5. 2011/09/29

P53-PWR_+1.05VS_VCCP/+16V

SP

6. 2011/09/29

P49-PWR_BATTERY CONN / OTP

7. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

8. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

10. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

11. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

12. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

13. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

14. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

15. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

16. 2011/09/29

P57-PWR +CPU_CORE DECOUPLI

NG

17. 2011/09/29

P49-PWR_BATTERY CONN / OTP

18. 2011/09/29

P58-PWR_VGA_CORE

19. 2011/09/29

P51-PWR_+3VALWP/+5VALWP

20. 2011/09/29

P58-PWR_VGA_CORE

21. 2011/09/29

P49-PWR_BATTERY CONN / OTP

22. 2011/09/29

P51-PWR_+3VALWP/+5VALWP
- Change PU330 to RT8205L

Change PU400 to RT8237C

Change PU450 to SY8037B

Change HMOS to MDV1525

Change HMOS to MDV1525

Change PD5,PD6 to SCA00001G00

Change PR589 from 348 to 8.06k

Change PR590 from 3.65k to 806

Change PC574 from 680P to 0.033u

Change PC577 from 4700P to 0.033u

Change PR548 from 1.21k to 8.06k

Change PR550 from 10.7k to 806

Change PC547 from 680P to 0.033u

Change PC551 from 4700P to 0.033u

Add snubber and boost resistor

Add PR22 120k,PR27 100k, PR32 0 Ohm

Remove PC803, PC804 add PC806 47u

Change PC360 to SE000006R80

Change PC702 to SE00000H180

Add PR17 14k, PR33 0 Ohm

Add PR373 0 Ohm
- Change source

Change source

Change source

Change source

Change source

ESD team request

FAE suggestion

FAE suggestion

FAE suggestion

FAE suggestion

FAE suggestion

FAE suggestion

FAE suggestion

FAE suggestion

For 3x3 H-MOS solution

For 120W adapter protect(9012)

For Nvidia suggestion

Change source

Change source

For CPU temperature protect(9012)

For 3/5 V always power on(9012)

HW PIR (Product Improve Record)

QCLA4 LA-8861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO DATE PAGE			MODIFICATION LIST	PURPOSE
1.	02/01	16	Remove PX_MODE and BACO components	No support PX4.0 by K99's request
2.	02/01	18	Remove PX_EN and RV125	No support PX4.0 by K99's request
3.	02/01	12	Change RD9.2 to GND	Correct the DDR SPD address
4.	02/01	13	Change RD15.1 to +3VS	Correct the DDR SPD address
5.	02/01	26	Stuff BIOS 2M ROM:UH4,RH267,RH269,	For win8 common design
6.	02/01	27	Change JTP footprint to ACES_50504	Follow connector list
7.	02/01	40	Add JMIC ACES_50271-0020N-001_2P	From K99's request to change AMIC
8.	02/01	36	Change JWLAN footprint to ACES_889	Follow connector list
9.	02/01	38	Remove INT_MIC from JCRI0.1	From K99's request to change AMIC
10.	02/01	37	Reserve PJ31 from +3VALW_PCH to +3	To save power consumption
11.	02/06	38	Swap LR9	For layout smoothly
12.	02/06	36	Add UM5,RM21;Reserve RM19,PJ33,Lin	For WLAN ON/OFF feature
13.	02/06	43	Connect AOAC_WLAN_PWR_EN# to EC pin38; Connect WLAN_RST# to EC pin91	For WLAN ON/OFF feature
14.	02/06	38	Change JCRI0.1 netname to NBA_PLUG	Remove AMic solution on sub/B
15.	02/06	40	Remove CA64 and add RA32,RA33 to I	Remove AMic solution on sub/B
16.	02/09	37	Add TL1 on UL1.37	Reserved from vendor's suggestion
17.	02/09	31	Change UH1.T7 from HDMI_HPD to CHP	For Serial POST debugger feature
18.	02/09	24	Delete T66 and link CHP3_SERDBG to JCRT.4	For Serial POST debugger feature
19.	02/09	10	Remove CC58	To prevent from short with thermal
19.	02/09	25	Add D94,D95,D96 on HDMI signal	For ESD request
20.	02/09	24	DEL D3~D5 and add D97,D98 on CRT s	For ESD request
21.	02/09	37	Add D99,D100 on LAN signal	For ESD request
22.	02/09	35	Add R1000~R1003 between JODD and J	Reserve for reducing SATA signal refle
23.	02/09	08	Reserve DRAMRST_CNTRL_EC to QC3	Reserved for DS3 feature
24.	02/09	41	Reserve DRAMRST_CNTRL_EC to EC pin	Reserved for DS3 feature