

Compal Confidential

Couger-Brazos

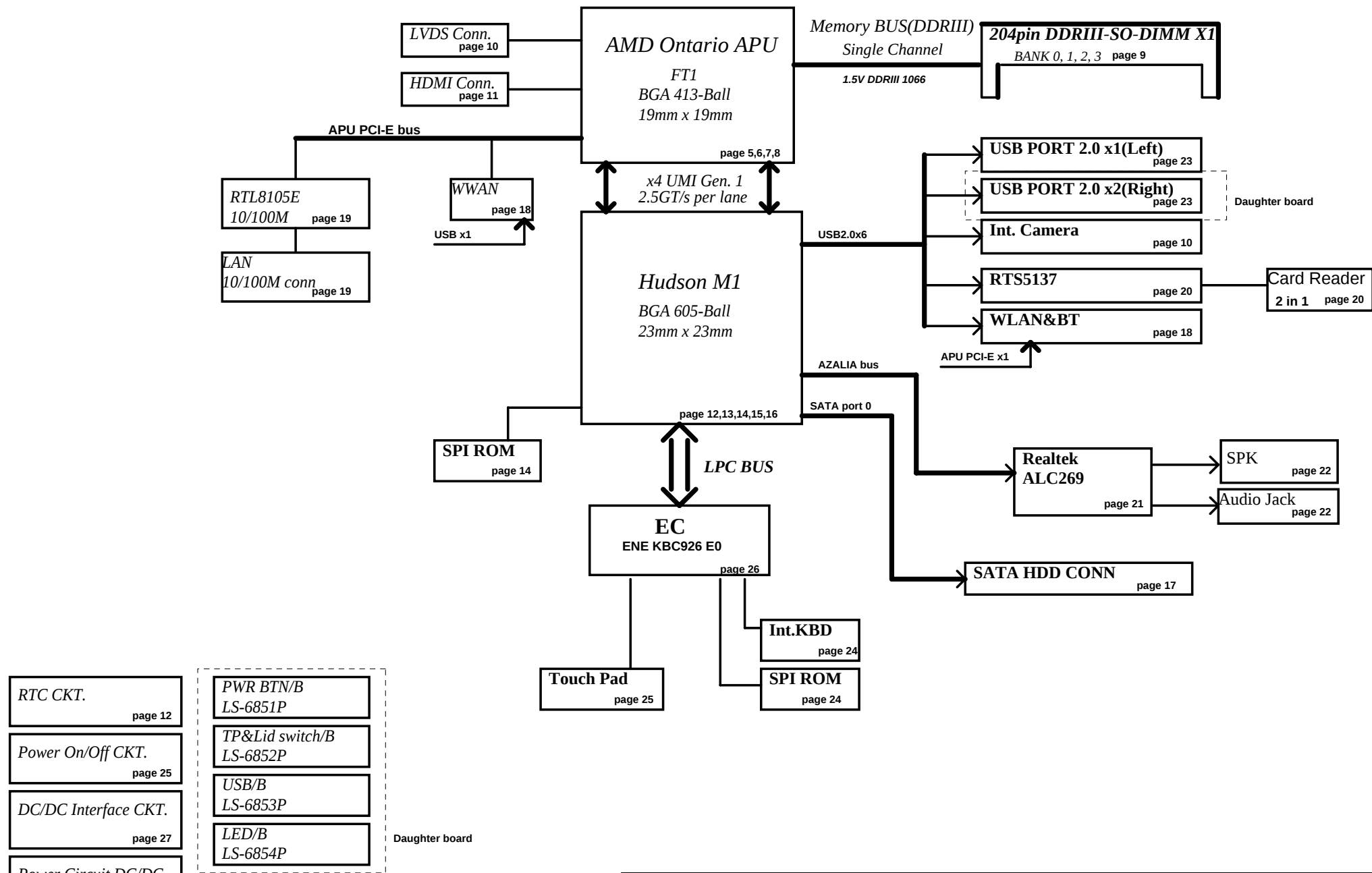
PBU01 LA-6852P Schematics Document

AMD APU Ontario-FT1 + FCH Hudson-M1

2012-2-20

REV:1.A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	SCHEMTIC A6852
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Voltage Rails

0 MEANS ON X MEANS OFF

power plane State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +1.0VS +0.75VS +APU_CORE +APU_VDDNB
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DAZ P/N

ZZZ1



LA-6852P

1.2G APU P/N

U1

1.2G APU R3
1G2R3@

1.2G APU P/N

U1

1.2G APU R1
1G2R1@

1G APU P/N

U1

1G APU R1
1GR1@

BTO (Build-To-Order) Option Table

Function	Sleep&Charger		Sleep&Music			
Description	Support	No Support	Support	No Support		
BTO	CHG@	non-CHG@	ALC269@	ALC259@		

FCH SM Bus0 Address

FCH SM Bus1 Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b

Power	Device	HEX	Address

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b

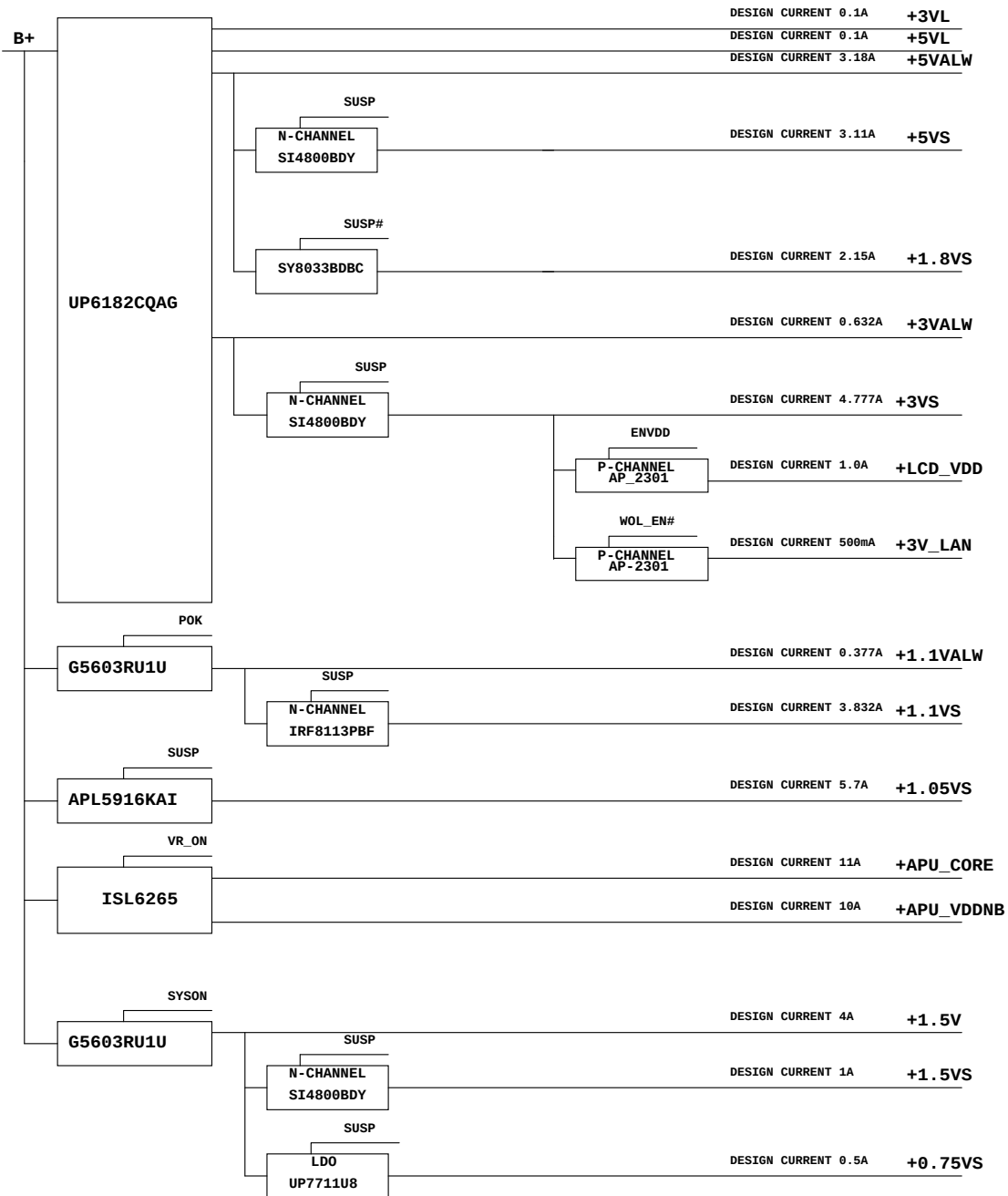
Power	Device	HEX	Address

SMBUS Control Table

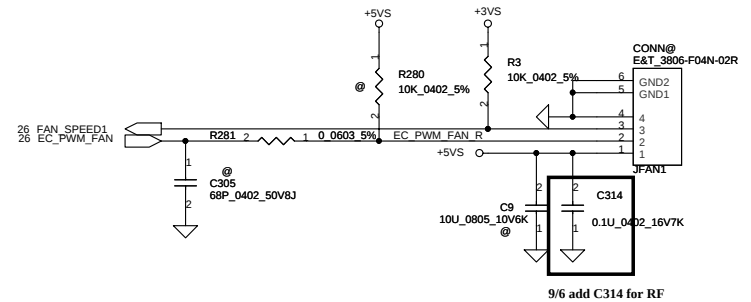
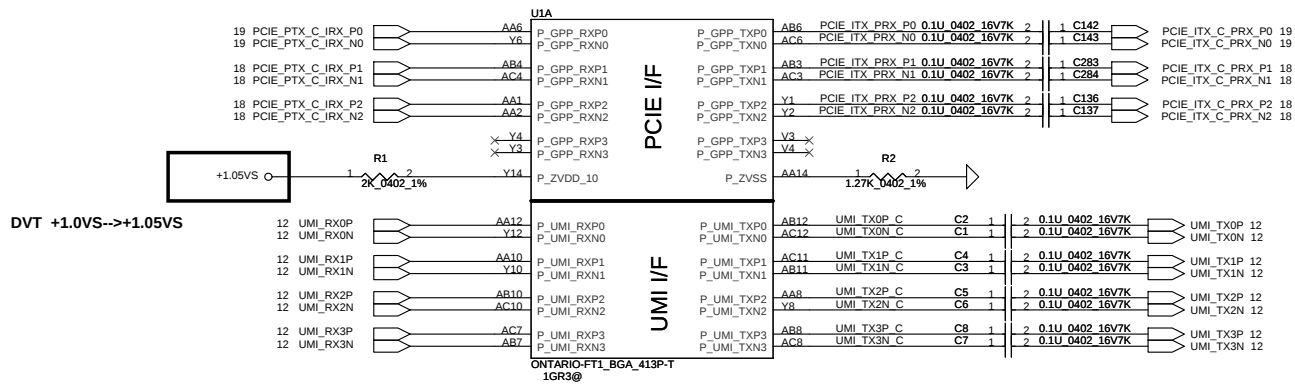
	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0	CLK GEN	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB926	V							
EC_SMB_CK2 EC_SMB_DA2	KB926								V
LCD_EDID_CLK LCD_EDID_DATA	APU FT1						V		
HDMICLK HDMIDAT	APU FT1							V	
FCH_SMCLK0 FCH_SMDAT0	FCH M1			V					
FCH_SMCLK1 FCH_SMDAT1	FCH M1					V			

08/05 update pin define

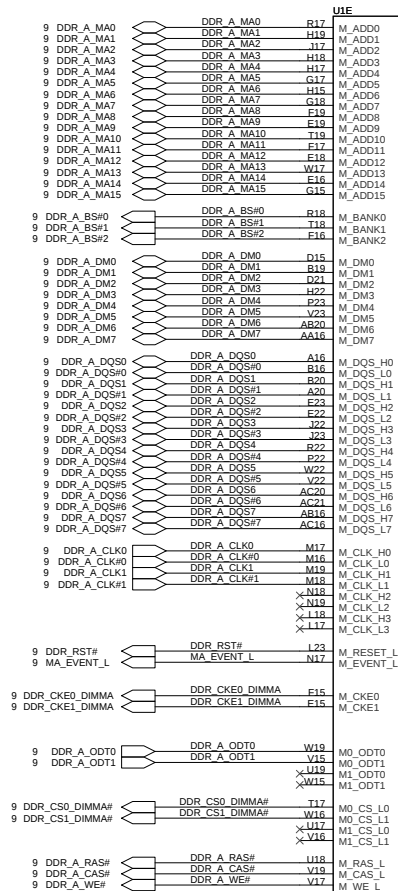
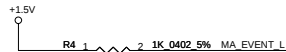
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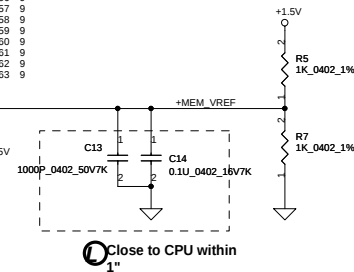
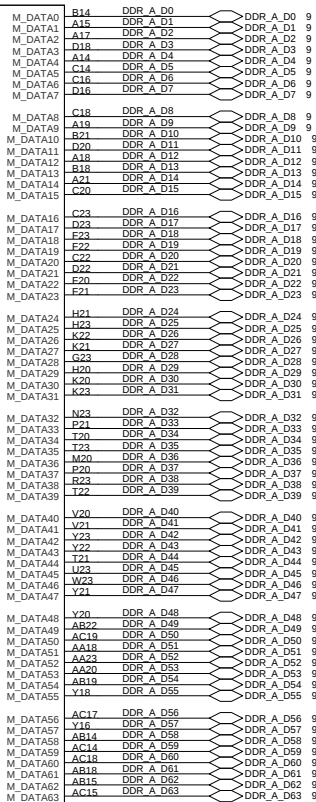
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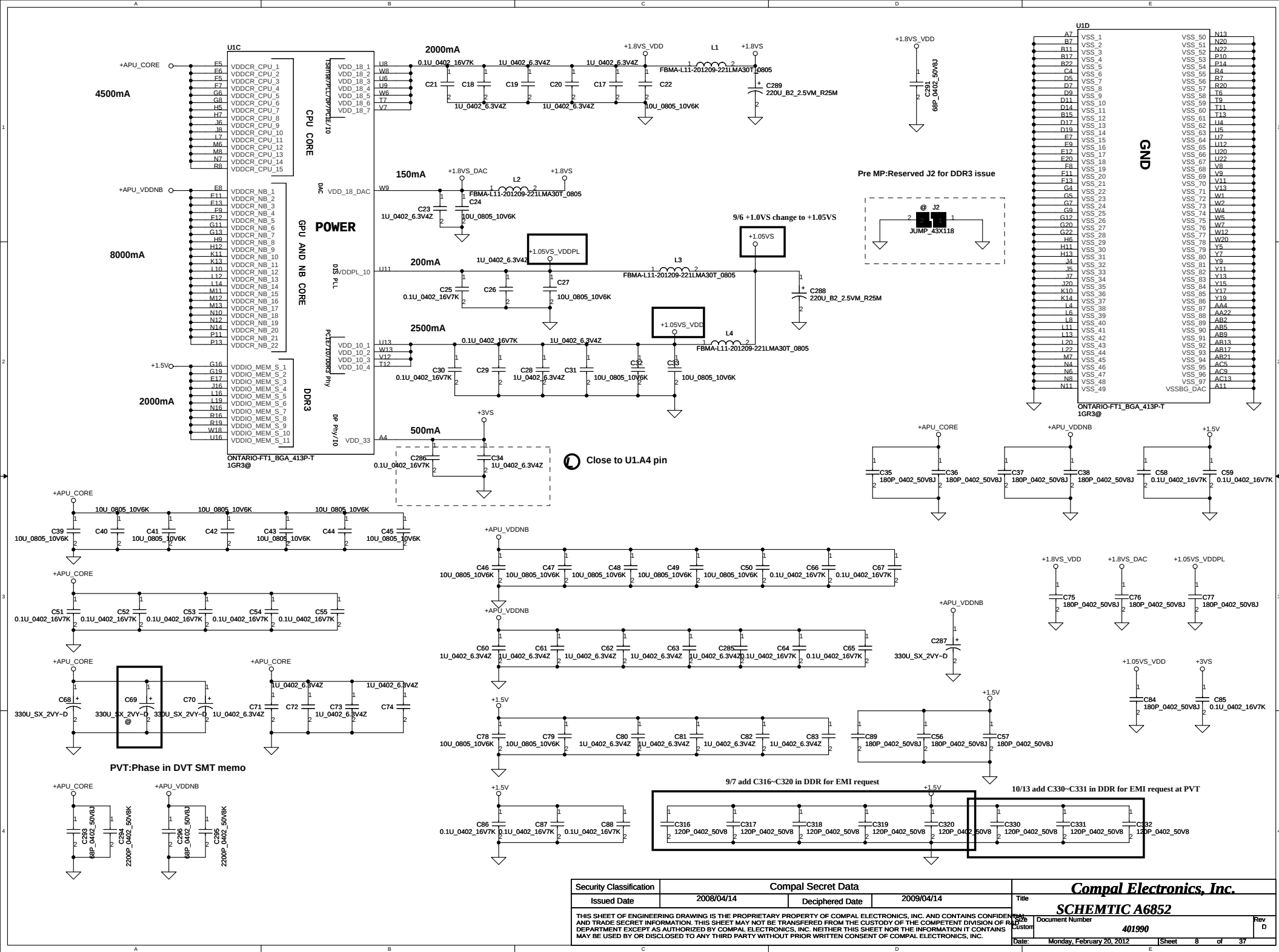
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DDR SYSTEM MEMORY



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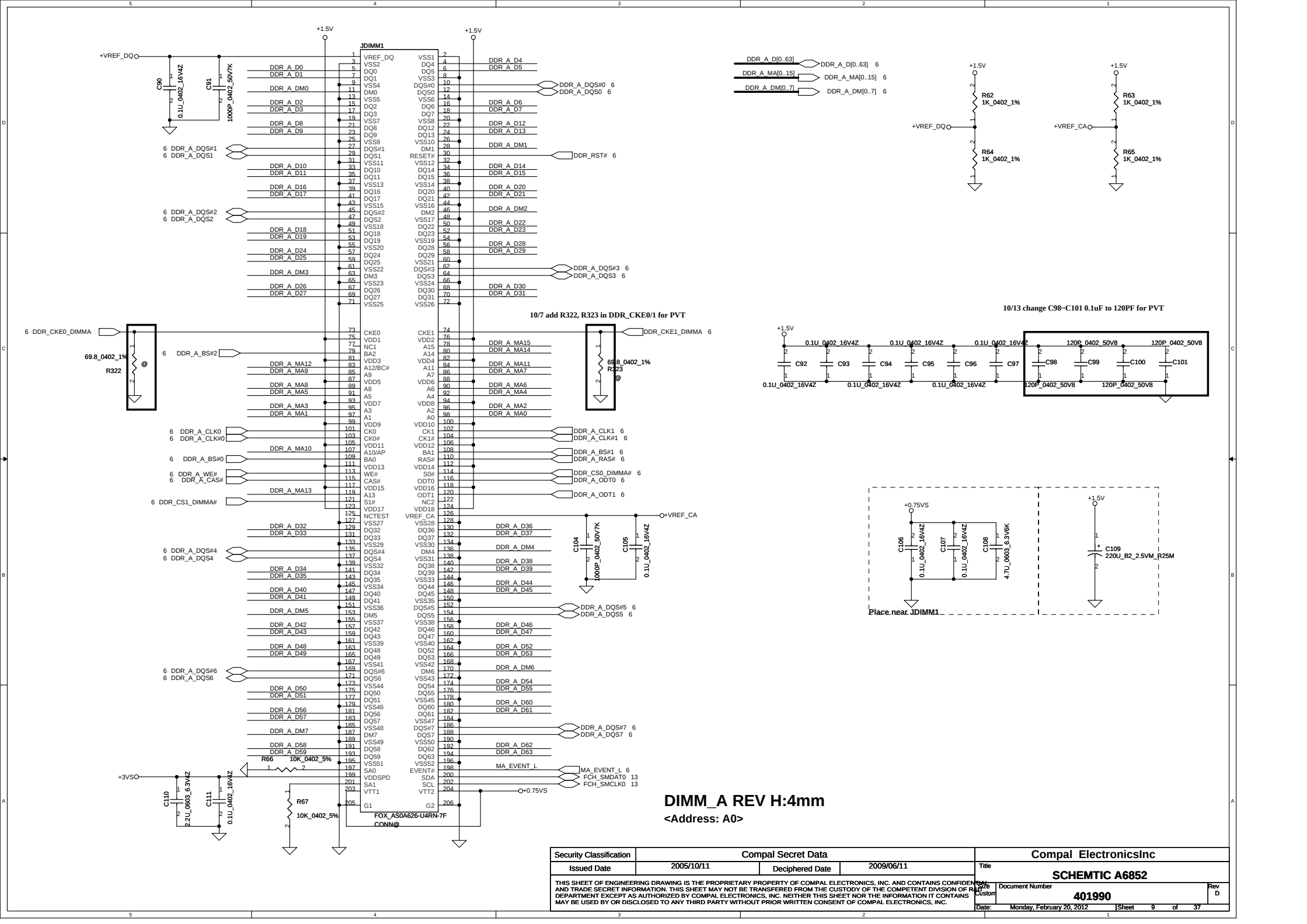


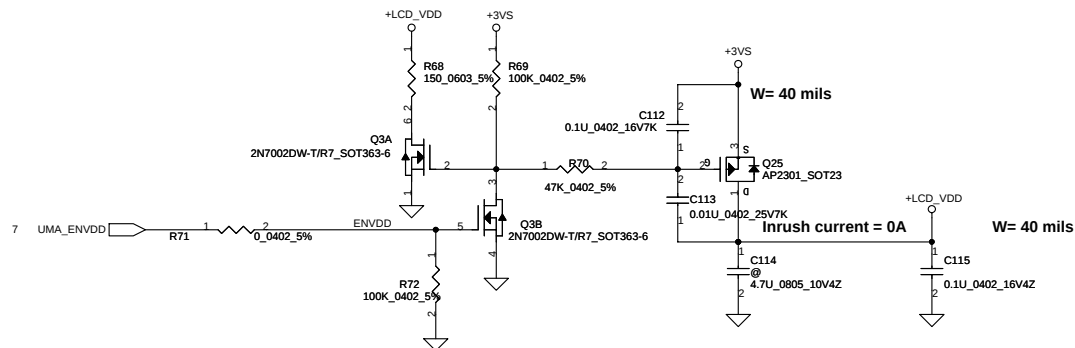
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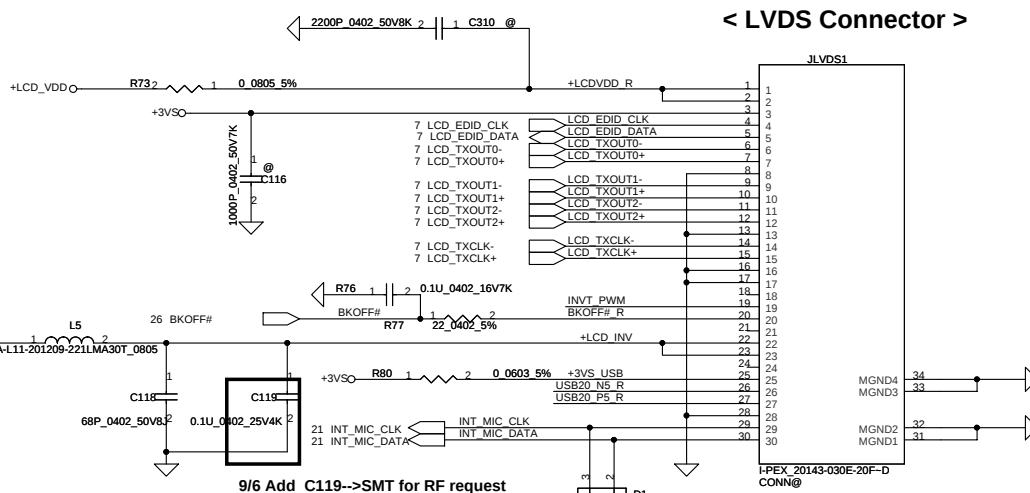
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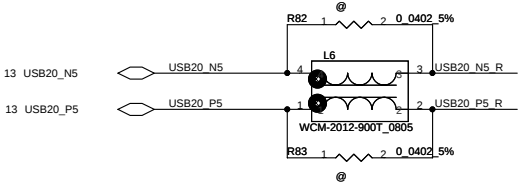




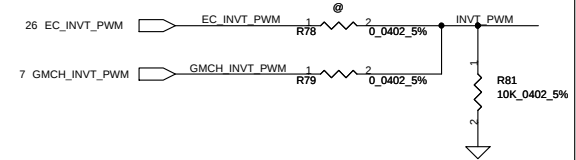
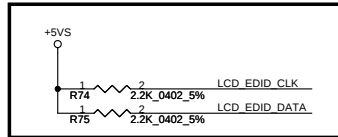
< LVDS Connector >



9/6 Add C119-->SMT for RF request

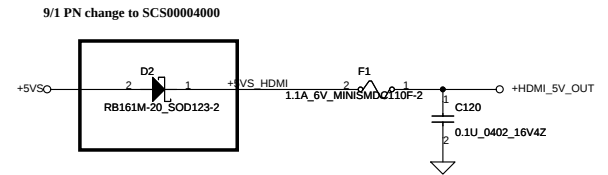
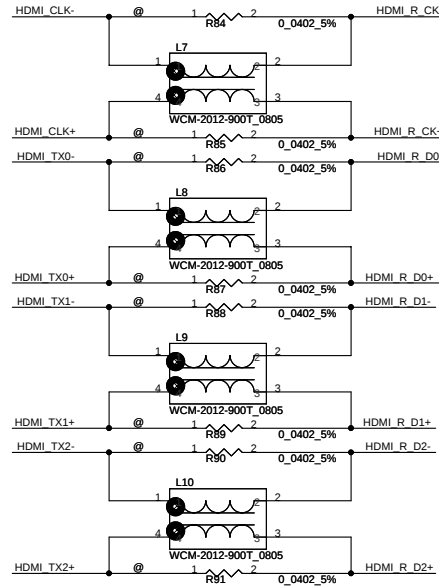
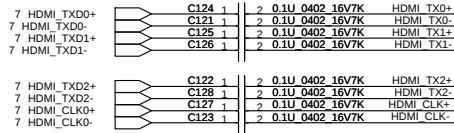


R74, R75 change to 2.2K-->for PVT
+3VS change to +5VS

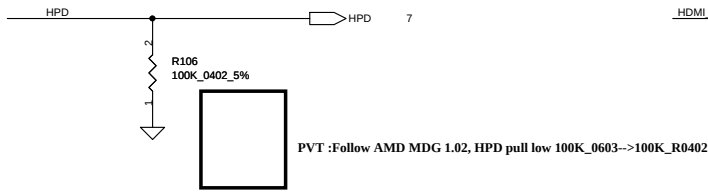
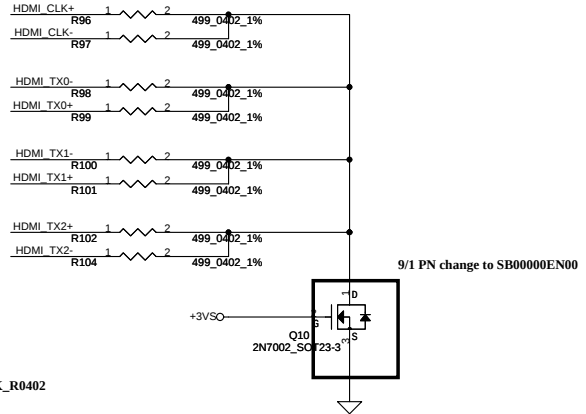
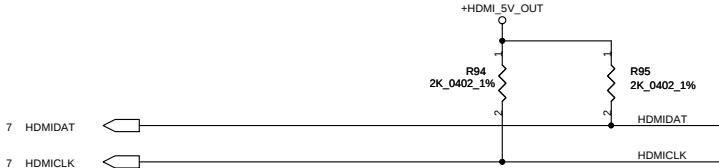
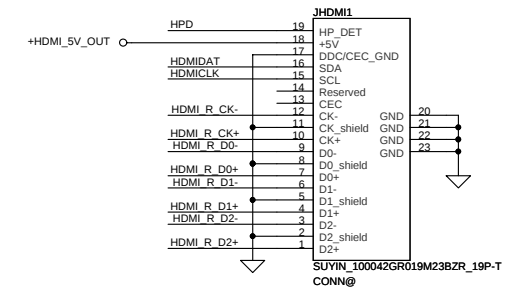


10/12 add C322--C329 for PVT RF request

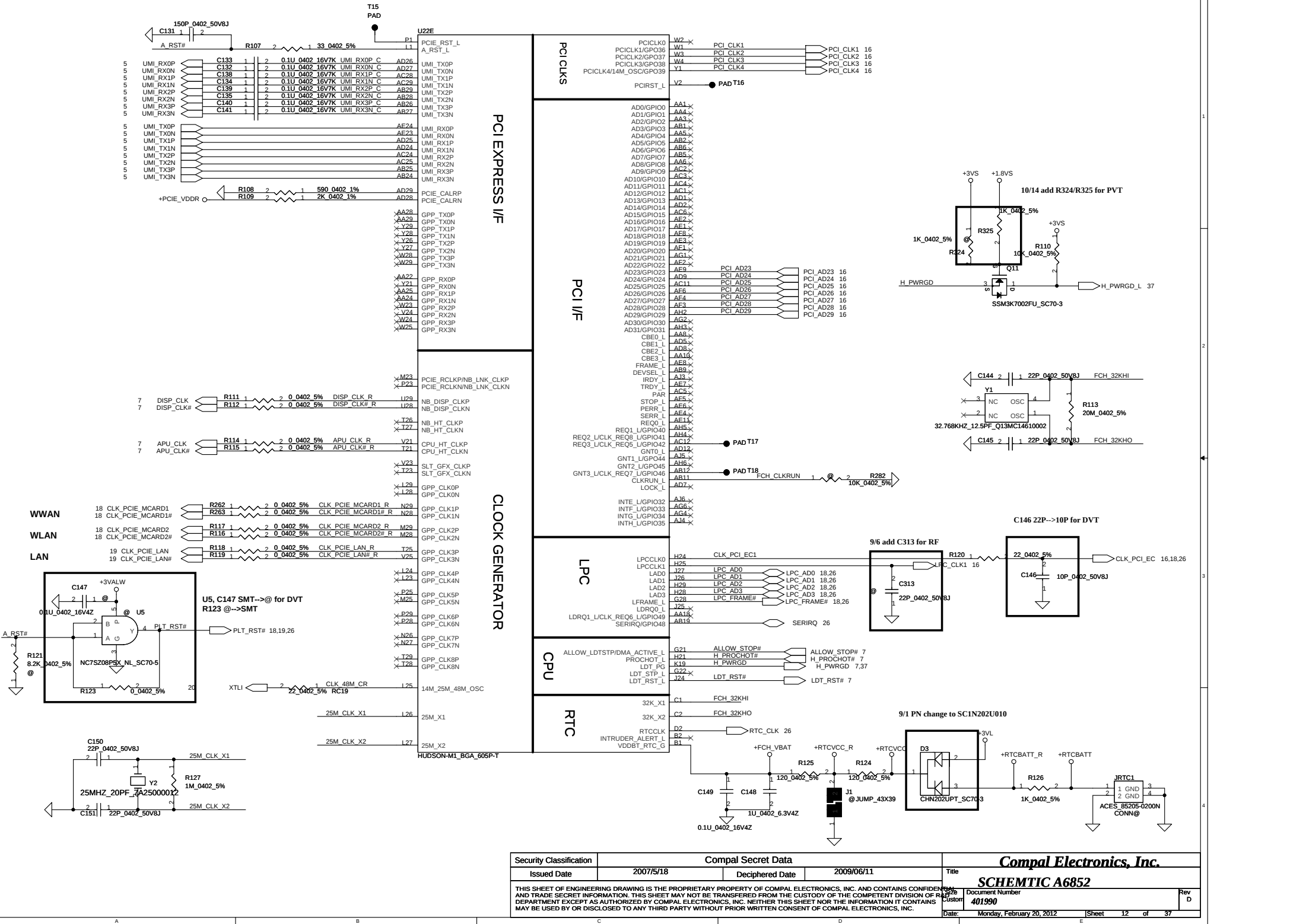
LCD_TXOUT0-	C322	1	2	18P_0402_50V8J
LCD_TXOUT0+	C323	1	2	18P_0402_50V8J
LCD_TXOUT1-	C324	1	2	18P_0402_50V8J
LCD_TXOUT1+	C325	1	2	18P_0402_50V8J
LCD_TXOUT2-	C326	1	2	18P_0402_50V8J
LCD_TXOUT2+	C327	1	2	18P_0402_50V8J
LCD_TXCLK-	C328	1	2	18P_0402_50V8J
LCD_TXCLK+	C329	1	2	18P_0402_50V8J



< HDMI Connector >



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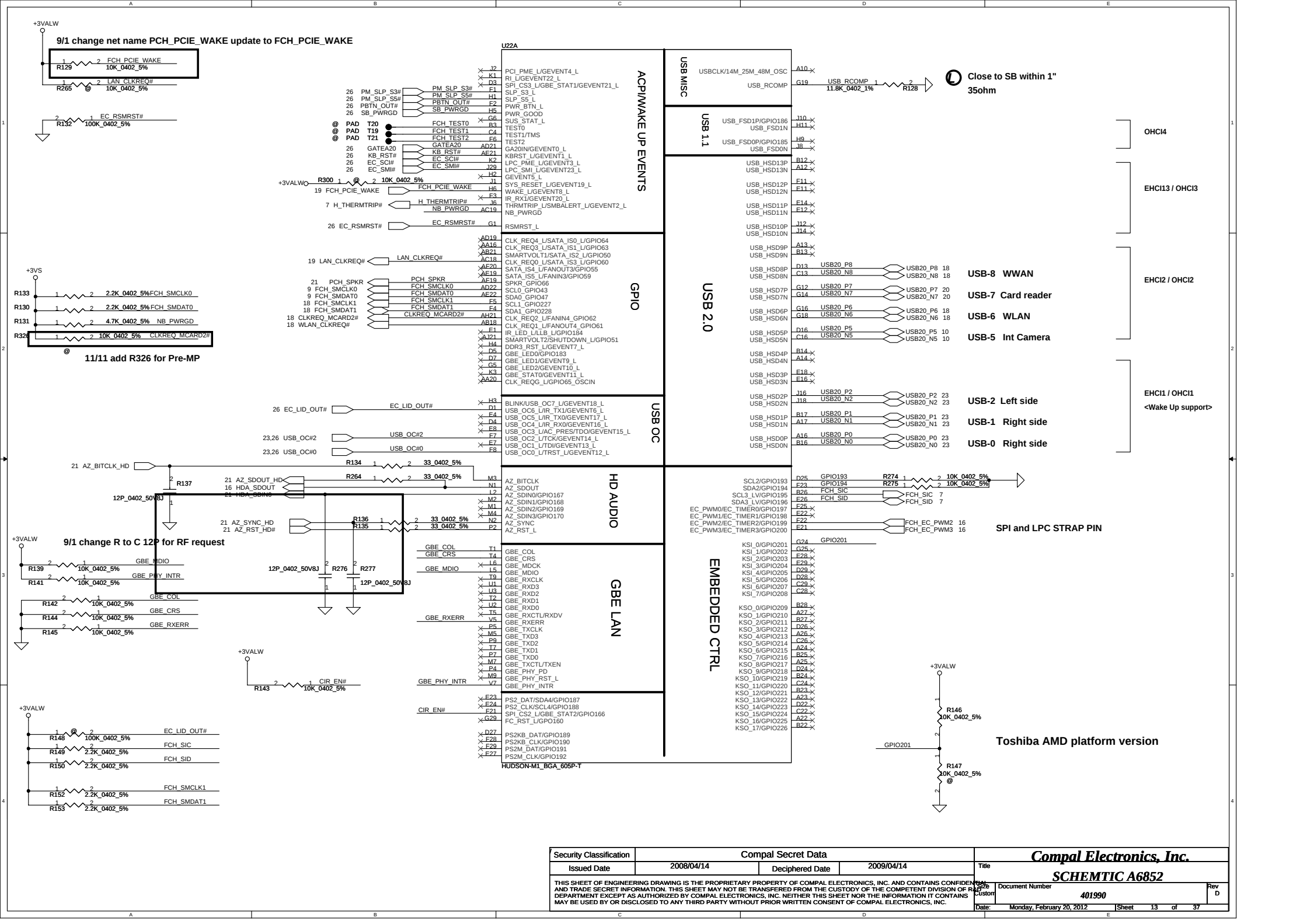
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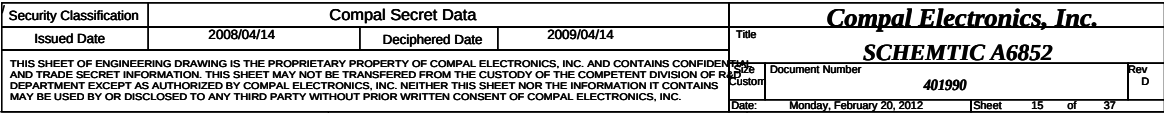
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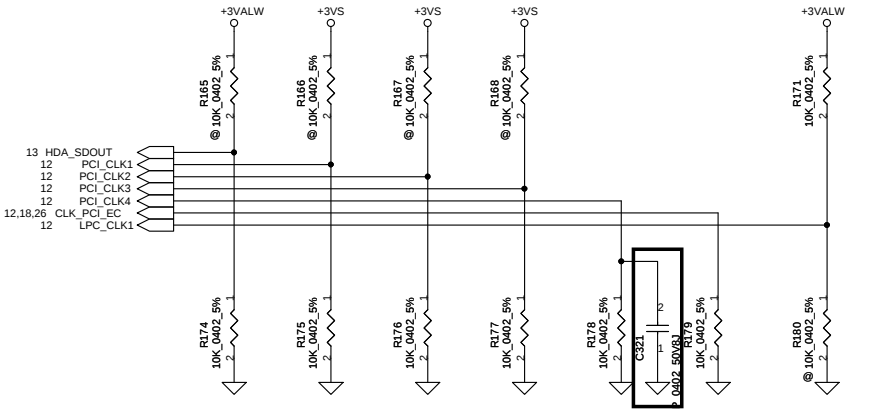
REQUIRED STRAPS

Check Internal PU/PD

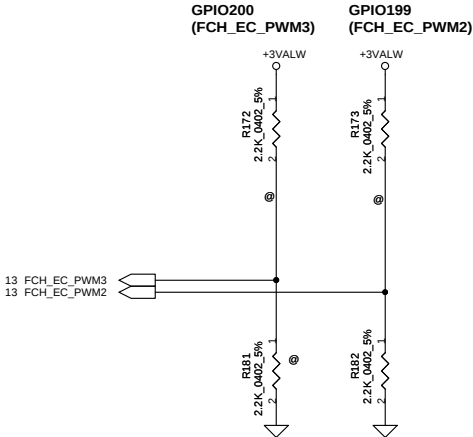
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Disable	EC ENABLE	CLOCKGEN ENABLE	
							*	DEFAULT
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Enable	EC DISABLE	CLOCKGEN DISABLE	
	*	*	*	*	*	*		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		

	GPIO200 (FCH_EC_PWM3)	GPIO199 (FCH_EC_PWM2)
Reserved	2.2k pull down	2.2k pull down
* SPI	Not contact	2.2k pull down
LPC	2.2k pull down	Not contact
Reserved	Not contact	Not contact

DEFAULT
07/21 Follow AMD 47791_SCL



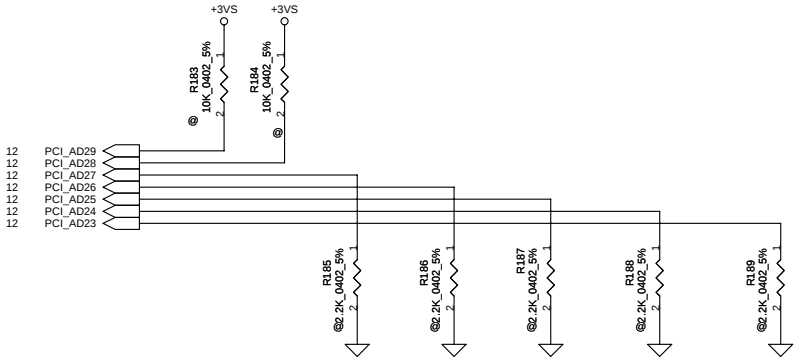
9/7 add C321 for RF request
11/18 C321 @-->SMT for RF request

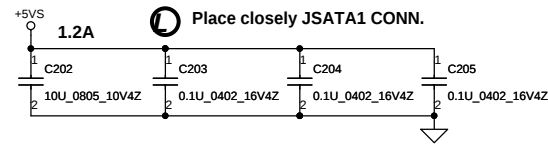


DEBUG STRAPS

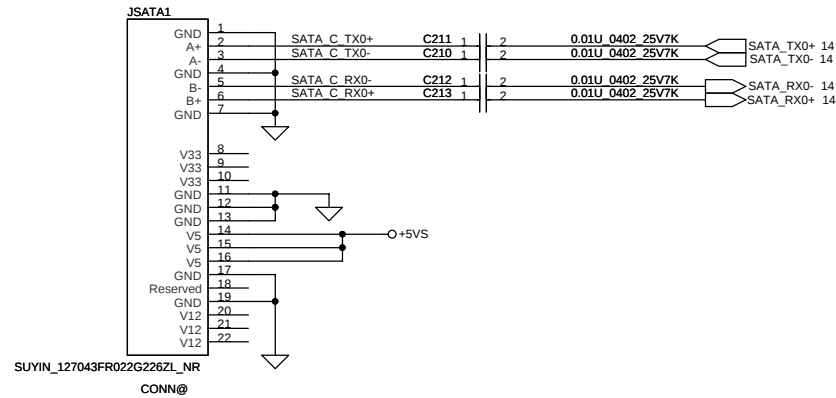
M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





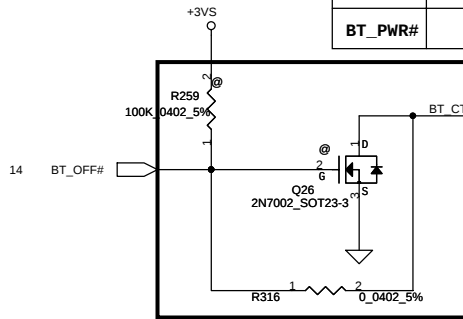
< SATA Connector >



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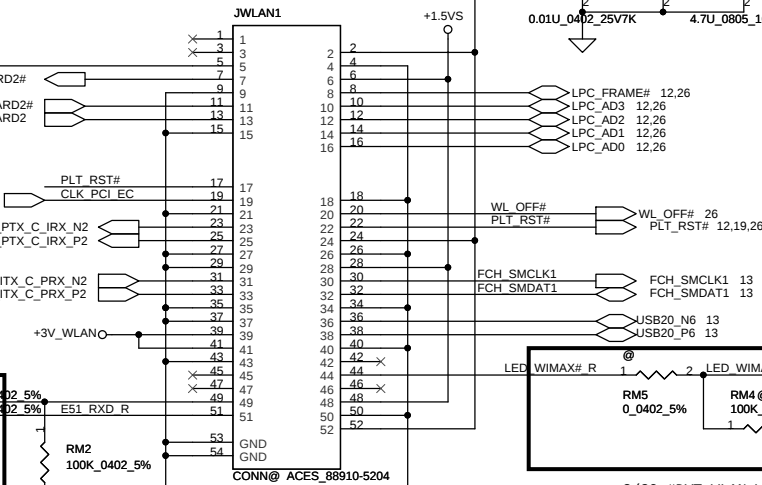
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

The image contains two circuit diagrams for the JUMP_43X79 component. Both diagrams show a three-pin component with pins 1, 2, and 3. The left diagram is connected to a +1.5VS supply, and the right diagram is connected to a +3V_WLAN supply. Both diagrams include capacitors CM1, CM2, CM3, CM4, CM5, and CM6, and resistors 0.01U_0402_25V7K and 4.7U_0805_10V4Z.



Timing diagram showing signals E51_TXD, E51_RXD, and BT_CTRL. The diagram includes a 1K resistor and a 5% tolerance for the BT_CTRL signal. The signals are labeled R320, R321, and R319.

402 5% E51
P319



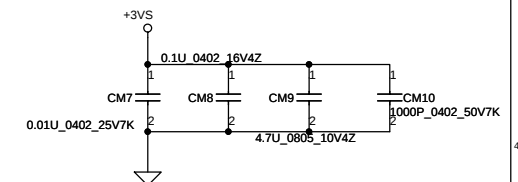
Pinout diagram for the BELLY 80019-1021_52P connector. The diagram shows 56 pins with their corresponding functions. Pins 1-16 are connected to WLAN and PCIe signals. Pins 17-27 are connected to PCIe signals. Pins 28-37 are connected to FCH and USB signals. Pins 38-44 are connected to LED_WIMAX#_R. Pins 45-56 are connected to various signals including WLAN_CLKREQ#, CLK_PCIE_MCARD1#, PCIE_PTX_C_IRX_N1, PCIE_ITX_C_PRX_N1, +3VS, and COMMON. The diagram also shows the connection to the BELLY 80019-1021_52P connector and the COMMON R260 pin.

Pin	Function
1	WLAN_CLKREQ#
2	CLK_PCIE_MCARD1#
3	CLK_PCIE_MCARD1#
4	PCIE_PTX_C_IRX_N1
5	PCIE_PTX_C_IRX_P1
6	PCIE_ITX_C_PRX_N1
7	PCIE_ITX_C_PRX_P1
8	WLAN_CLKREQ#
9	CLK_PCIE_MCARD1#
10	CLK_PCIE_MCARD1#
11	PCIE_PTX_C_IRX_N1
12	PCIE_PTX_C_IRX_P1
13	PCIE_ITX_C_PRX_N1
14	PCIE_ITX_C_PRX_P1
15	WLAN_CLKREQ#
16	CLK_PCIE_MCARD1#
17	PCIE_PTX_C_IRX_N1
18	PCIE_PTX_C_IRX_P1
19	PCIE_ITX_C_PRX_N1
20	PCIE_ITX_C_PRX_P1
21	WLAN_CLKREQ#
22	CLK_PCIE_MCARD1#
23	CLK_PCIE_MCARD1#
24	PCIE_PTX_C_IRX_N1
25	PCIE_PTX_C_IRX_P1
26	PCIE_ITX_C_PRX_N1
27	PCIE_ITX_C_PRX_P1
28	WLAN_CLKREQ#
29	CLK_PCIE_MCARD1#
30	CLK_PCIE_MCARD1#
31	PCIE_PTX_C_IRX_N1
32	PCIE_PTX_C_IRX_P1
33	PCIE_ITX_C_PRX_N1
34	PCIE_ITX_C_PRX_P1
35	WLAN_CLKREQ#
36	CLK_PCIE_MCARD1#
37	CLK_PCIE_MCARD1#
38	PCIE_PTX_C_IRX_N1
39	PCIE_PTX_C_IRX_P1
40	PCIE_ITX_C_PRX_N1
41	PCIE_ITX_C_PRX_P1
42	WLAN_CLKREQ#
43	CLK_PCIE_MCARD1#
44	CLK_PCIE_MCARD1#
45	PCIE_PTX_C_IRX_N1
46	PCIE_PTX_C_IRX_P1
47	PCIE_ITX_C_PRX_N1
48	PCIE_ITX_C_PRX_P1
49	WLAN_CLKREQ#
50	CLK_PCIE_MCARD1#
51	CLK_PCIE_MCARD1#
52	PCIE_PTX_C_IRX_N1
53	PCIE_PTX_C_IRX_P1
54	PCIE_ITX_C_PRX_N1
55	PCIE_ITX_C_PRX_P1
56	WLAN_CLKREQ#

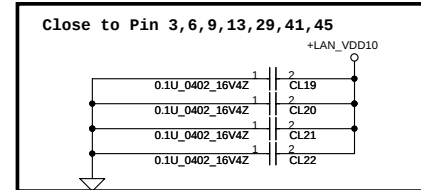
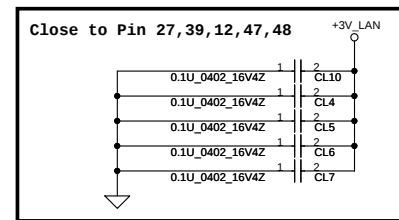
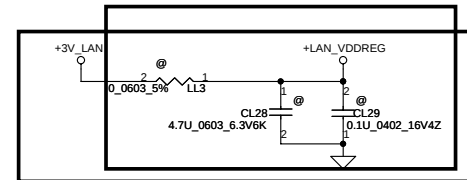
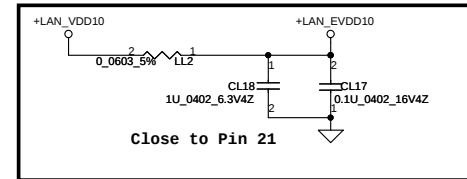
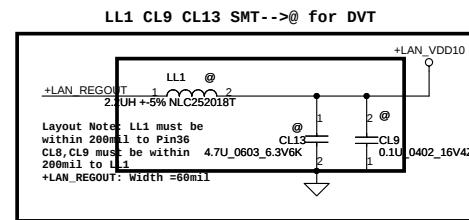
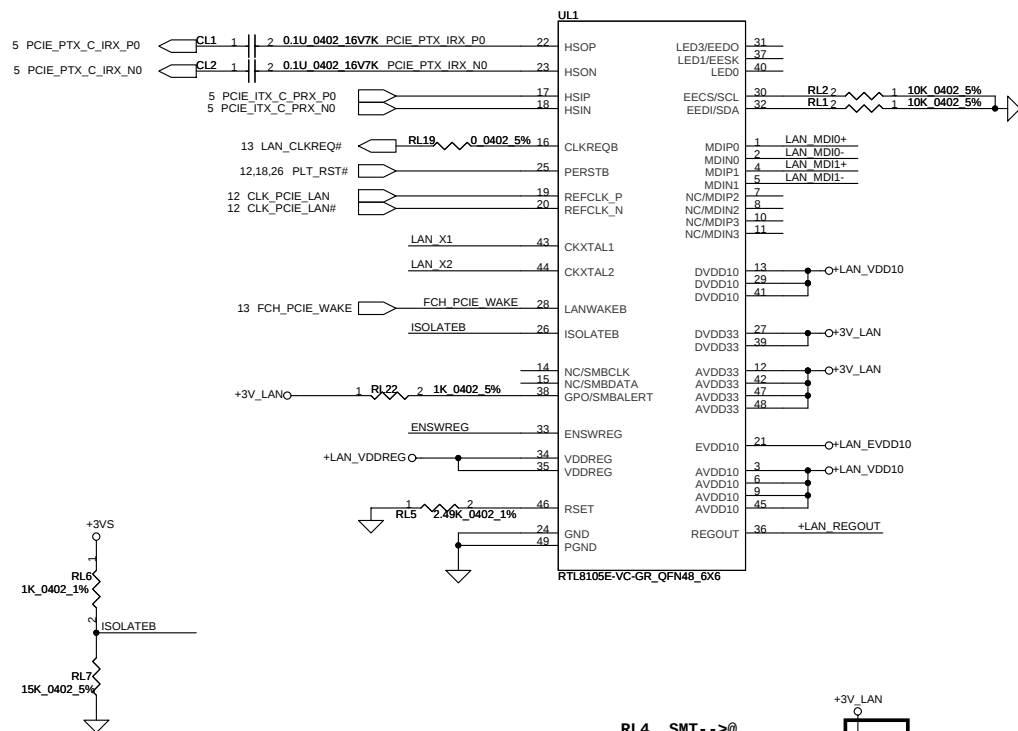
COMMON R260 1 2 0 0402 5%UIM VPP

COMMON R260 1 ^ ^ 2 0 0402 5%UIM VPP

The schematic diagram illustrates the internal structure of the WCM-2012-900T_0805 component. It features a central inductor labeled L28, which is represented by a rectangle containing two horizontal coils. The top coil is connected to terminal 1 on the left and terminal 2 on the right. The bottom coil is connected to terminal 4 on the left and terminal 3 on the right. Two resistors, R284 and R285, are connected in series with the inductor. Resistor R284 is connected between terminal 1 and the top coil. Resistor R285 is connected between terminal 4 and the bottom coil. The component is labeled WCM-2012-900T_0805.

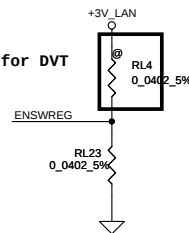


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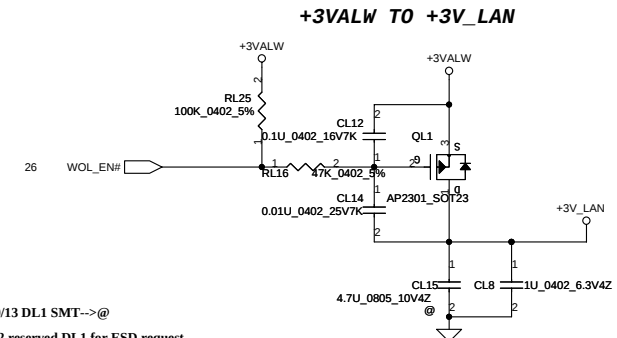
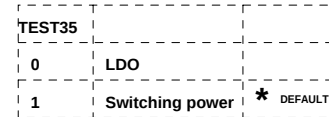


RL4 SMT-->@

RL23 @-->SMT for DVT

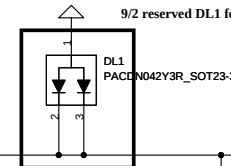


ENSWREG for LDO and switching power

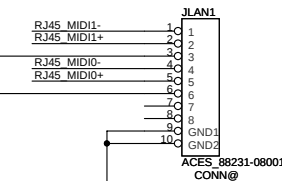


10/13 DL1 SMT-->@

9/2 reserved DL1 for ESD request

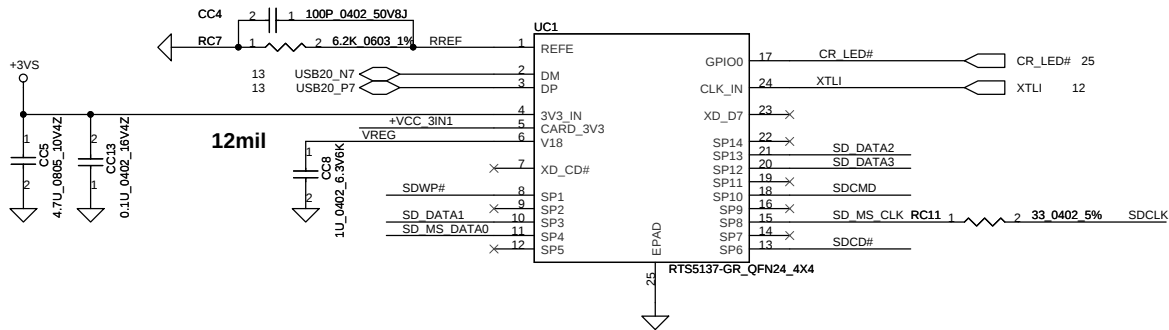


< LAN Connector >

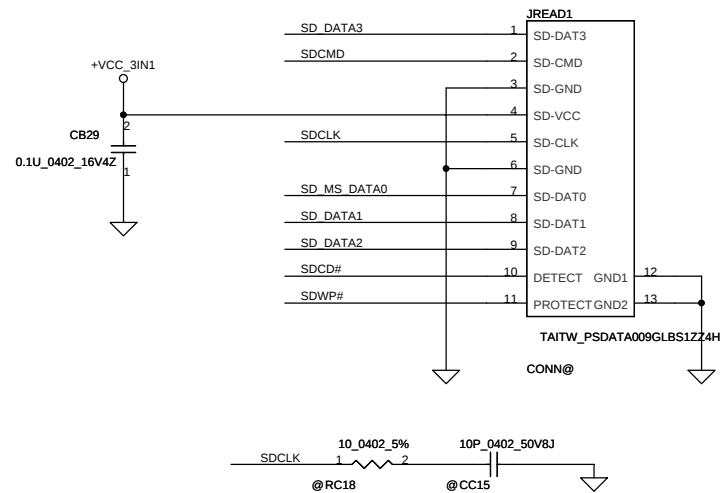


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	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CEF	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



< 2 in 1 Card Reader >



11/16 +5V_Codec change to +5VALW for pre-MP

place close to chip

place close to chip

place close to chip

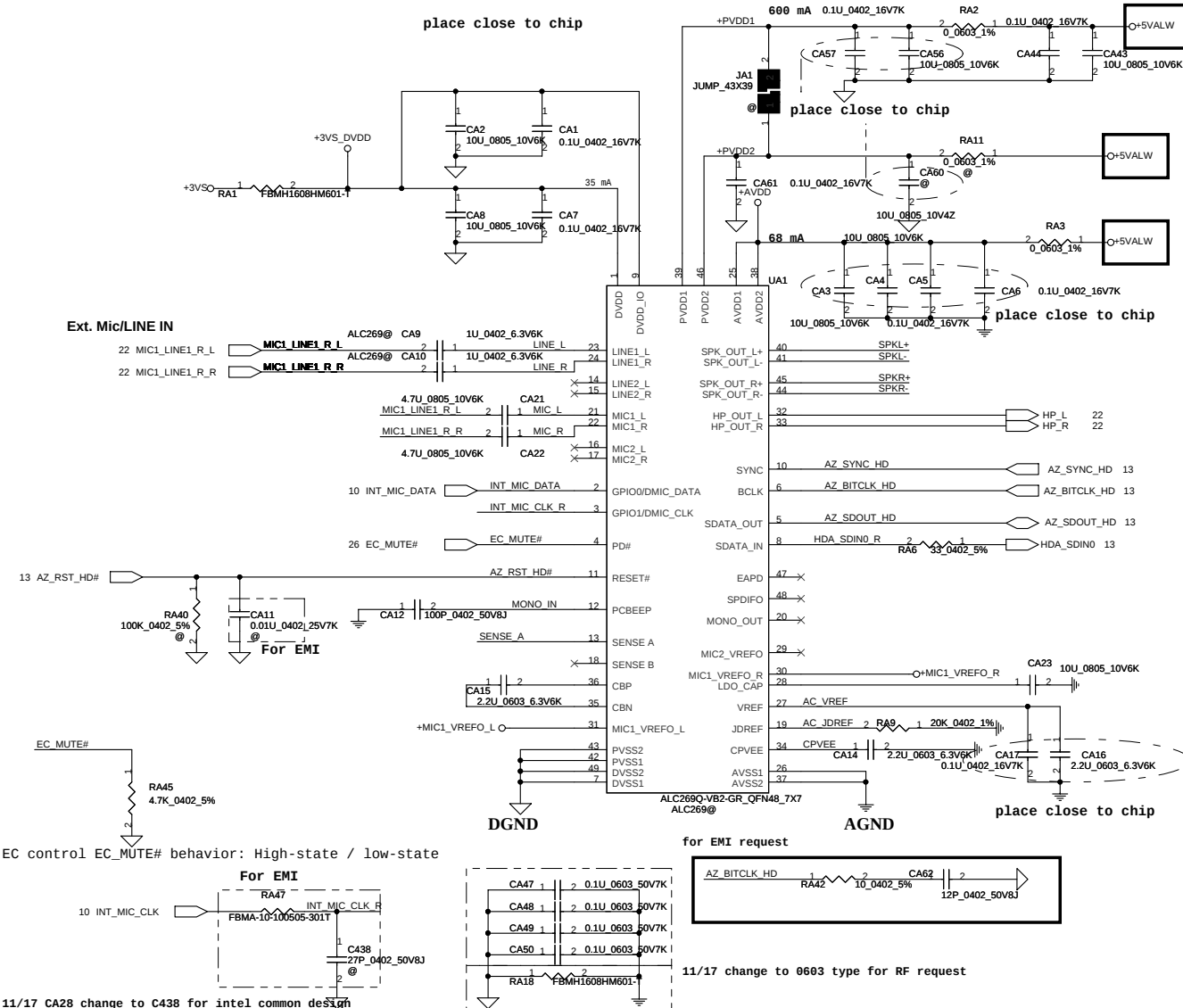
place close to chip

for EMI request

11/17 change to 0603 type for RF request

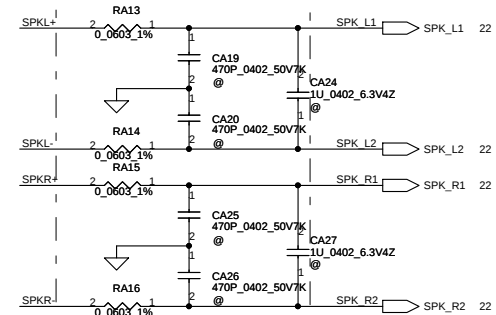
place close to chip

Ext. Mic/LINE IN



Speaker Connector

placement near Audio Codec

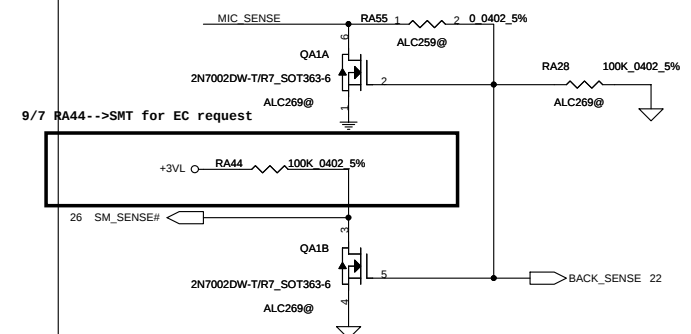


EC Beep

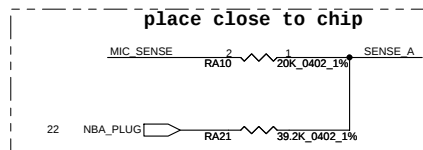
Beep sound

PCI Beep

RA12 10K-->4.7K (SD028470180) for DVT
CA18 0.1u-->100P (SE071101J80)

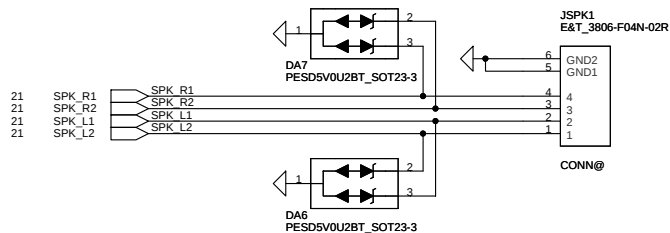


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

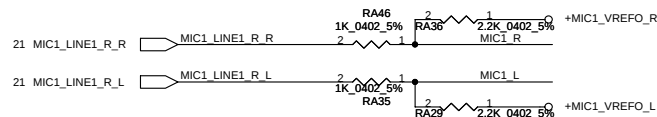


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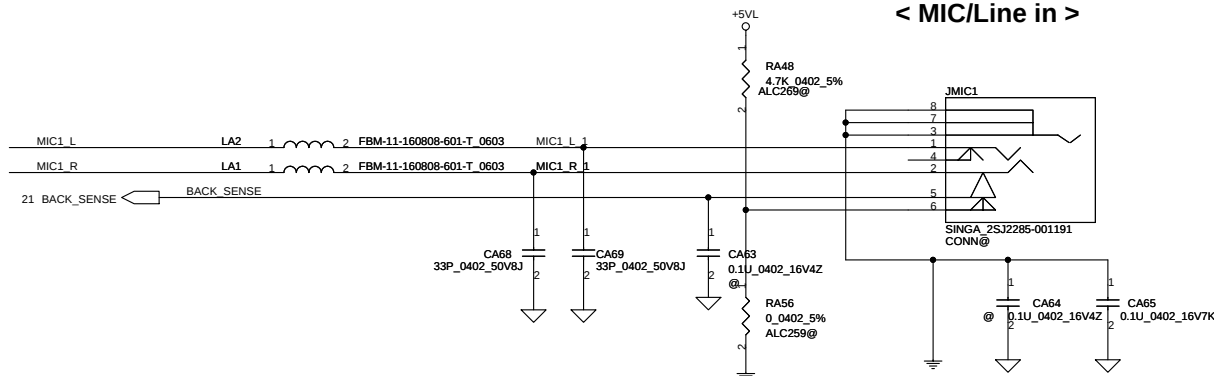
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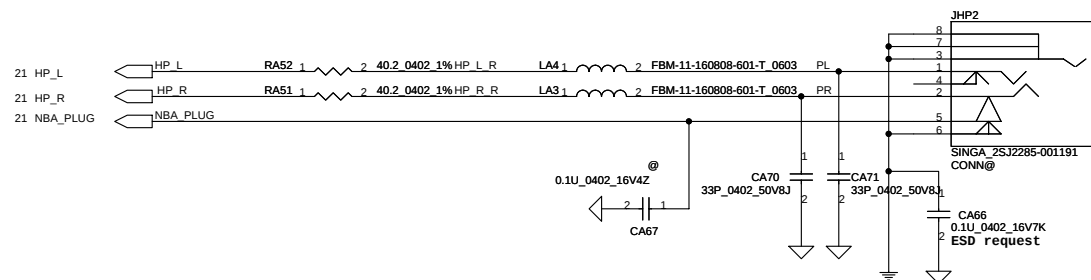
Ext.MIC/LINE IN JACK



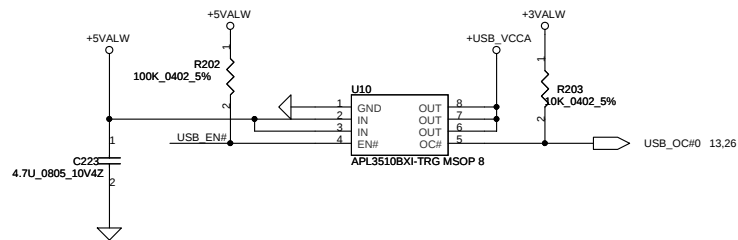
< MIC/Line in >



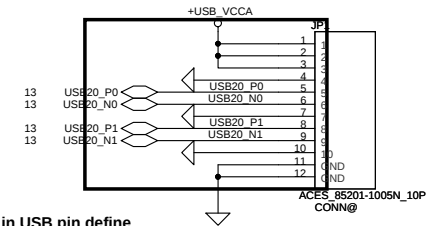
< Head phone >



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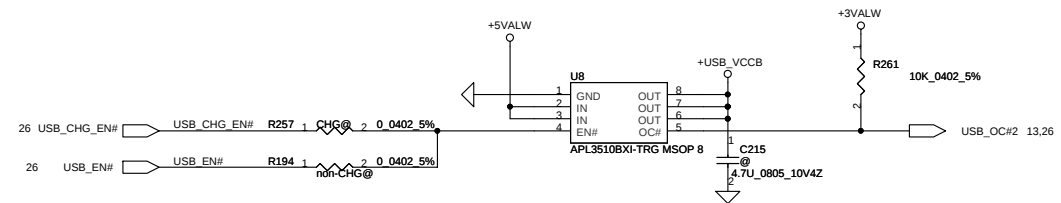
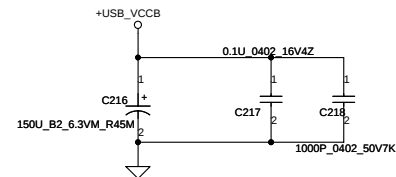
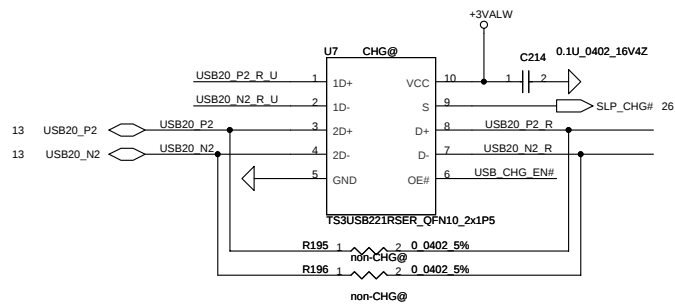


< USB connector >

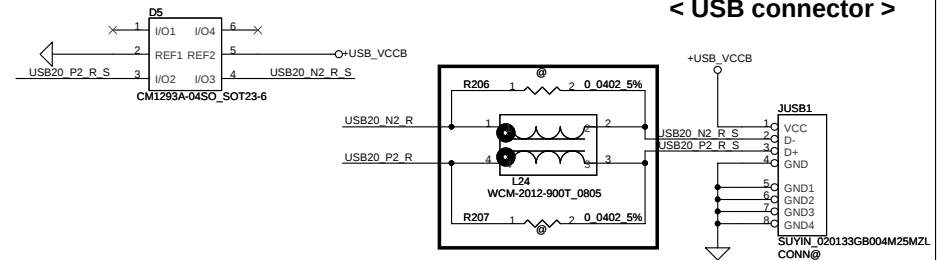
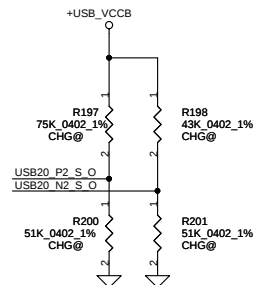
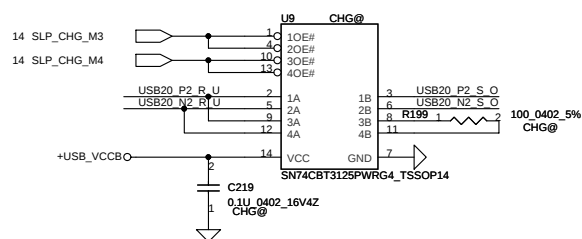


8/27 add GND pin in USB pin define

USB Sleep and charge



< USB connector >



10/13 R206/R207 SMT-->@ L24 @-->SMT

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

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Option 1:SPI Flash (2MB*1) for EC

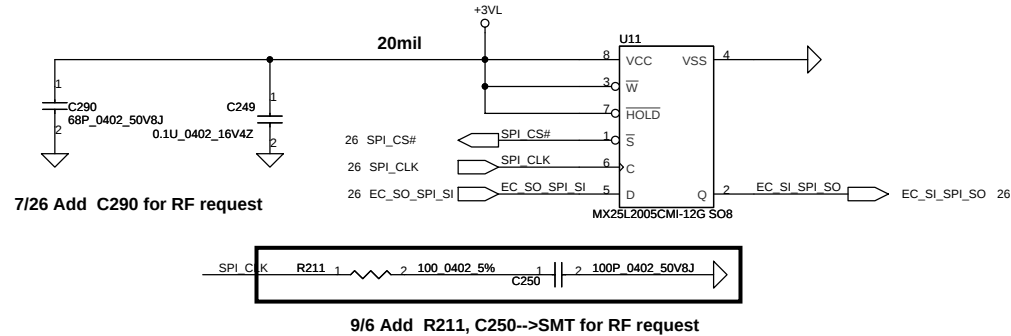
Option 2:SPI Flash (256KB*1) for EC

SPI Flash (2MB*1) for SB (set up strap pin)

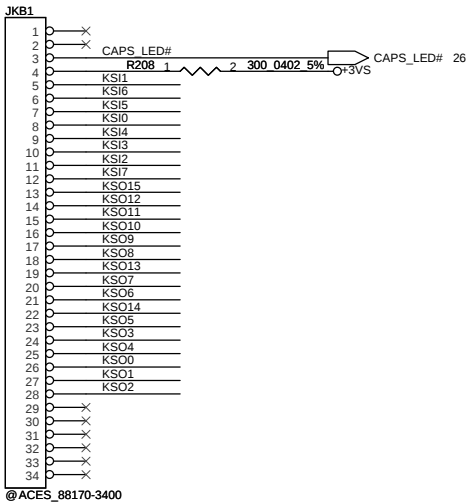
SPI Socket: SP07000F500 & SP07000H900

2MB P/N:Winbond SA00003FO00 S IC FL 16M W25Q16BVSSIG SOIC 8P

256KB P/N:MXIC SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P

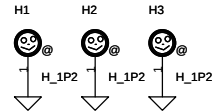


< Key board connector >

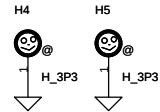


KSI0	C224	1	2	100P_0402_50V8J
KSI1	C225	1	2	100P_0402_50V8J
KSI2	C226	1	2	100P_0402_50V8J
KSI3	C227	1	2	100P_0402_50V8J
KSI4	C228	1	2	100P_0402_50V8J
KSI5	C229	1	2	100P_0402_50V8J
KSI6	C230	1	2	100P_0402_50V8J
KSI7	C231	1	2	100P_0402_50V8J
KSO0	C232	1	2	100P_0402_50V8J
KSO1	C233	1	2	100P_0402_50V8J
KSO2	C234	1	2	100P_0402_50V8J
KSO3	C235	1	2	100P_0402_50V8J
KSO4	C236	1	2	100P_0402_50V8J
KSO5	C237	1	2	100P_0402_50V8J
KSO6	C238	1	2	100P_0402_50V8J
KSO7	C239	1	2	100P_0402_50V8J
KSO8	C240	1	2	100P_0402_50V8J
KSO9	C241	1	2	100P_0402_50V8J
KSO10	C242	1	2	100P_0402_50V8J
KSO11	C243	1	2	100P_0402_50V8J
KSO12	C244	1	2	100P_0402_50V8J
KSO13	C245	1	2	100P_0402_50V8J
KSO14	C246	1	2	100P_0402_50V8J
KSO15	C247	1	2	100P_0402_50V8J
CAPS_LED#	C248	1	2	100P_0402_50V8J

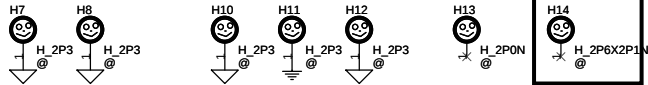
CPU Screw hole



Stand off

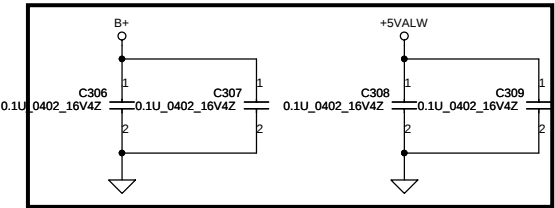


Screw hole

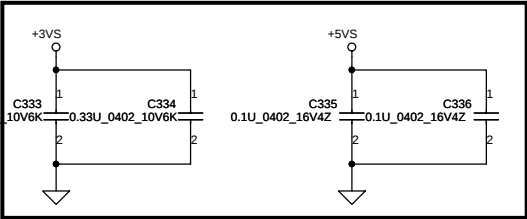


10/07 remove H9, add H14 for PVT

EMI request cap



11/12 add C306~C309 @-->SMT for RF at Pre-MP phase

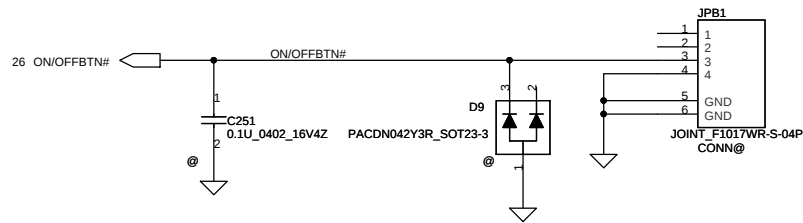


10/14 add C333~C336 for EMI at PVT phase

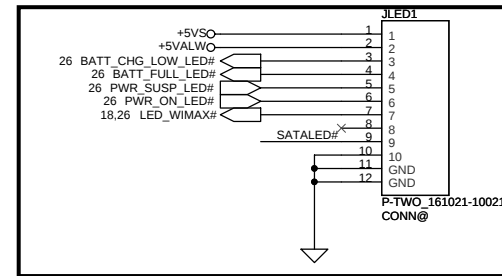
11/17 C333/C334 0.1uF change to 0.33uF for Pre-MP

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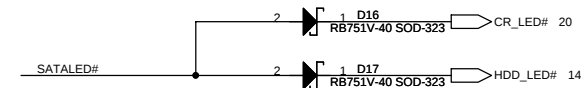
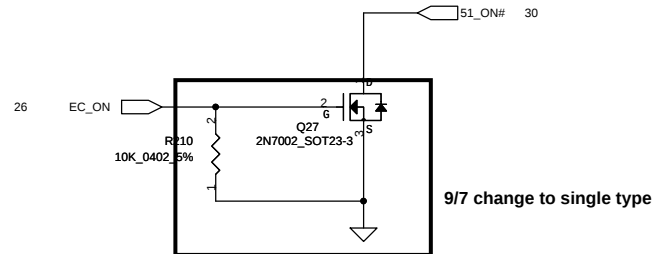
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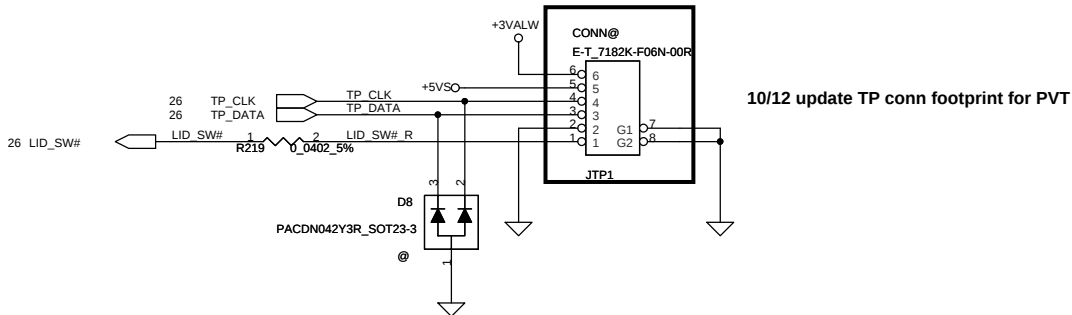
<LED connector >



10/13 update LEDconn footprint for PVT

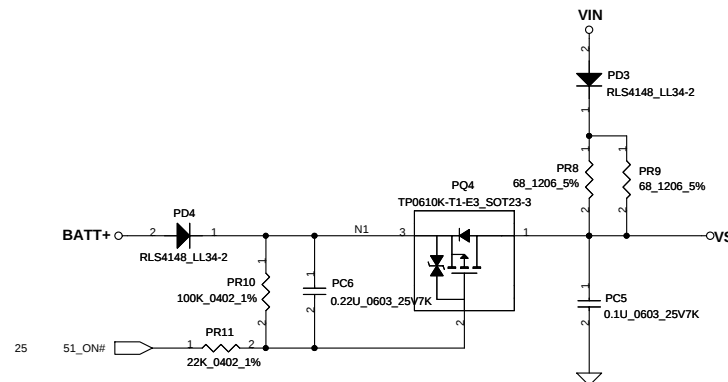
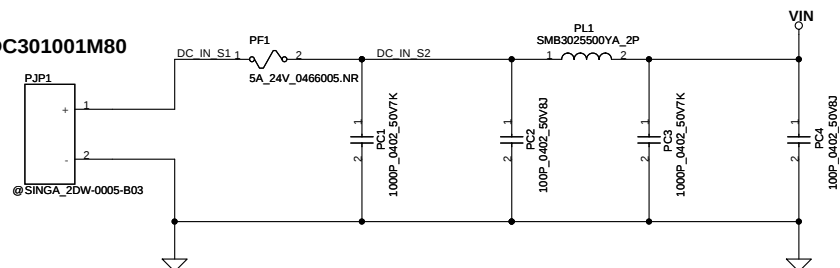


< T/P and Lid connector >



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DC301001M80



@ PJ332
JUMP_43X118
(5A, 200mils, Via NO.= 10)
OCP=8.6A

@ PJ2
JUMP_43X39
(120mA, 20mils, Via NO.= 1)

@ PJ112
JUMP_43X118
(10A, 600mils, Via NO.= 10)
OCP=A

@ PJ352
JUMP_43X118
(5A, 200mils, Via NO.= 10)
OCP=7.9A

@ PJ182
JUMP_43X118
(2.15A, 100mils, Via NO.= 5)
OCP=A

@ PJ102
JUMP_43X118
(5.7A, 240mils, Via NO.= 12)
OCP=A

@ PJ3
JUMP_43X39
(100mA, 20mils, Via NO.= 1)

@ PJ152
JUMP_43X118
(5A, 200mils, Via NO.= 10)
OCP=A

@ PJ76
JUMP_43X79
(0.5A, 20mils, Via NO.= 1)

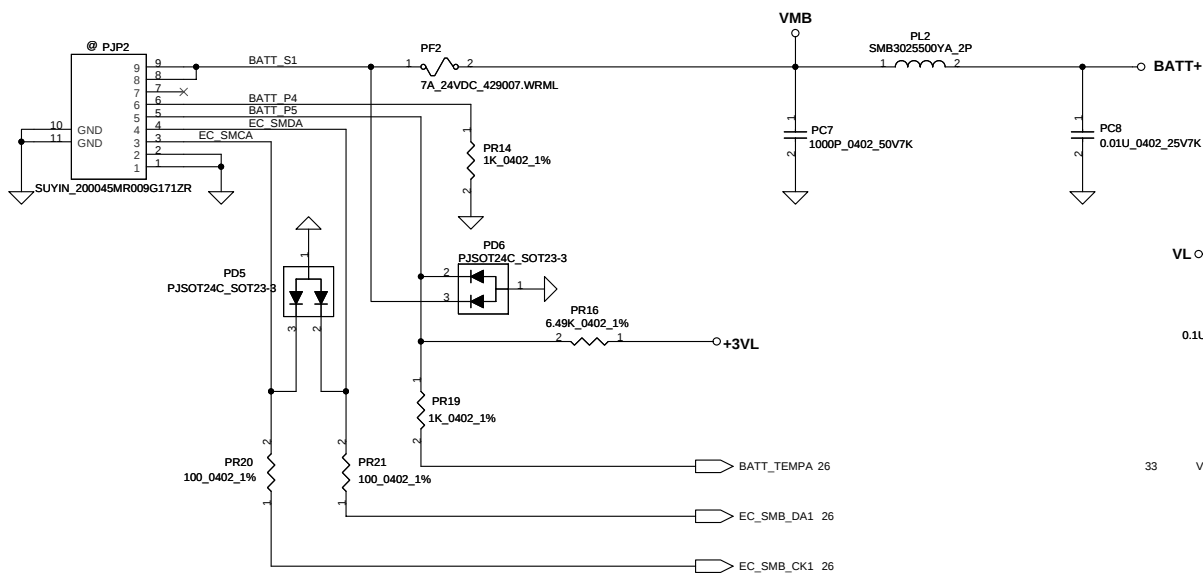
@ PJ4
JUMP_43X39
(100mA, 20mils, Via NO.= 1)

@ PJ5
JUMP_43X118
(10A, 400mils, Via NO.= 20)
OCP=A

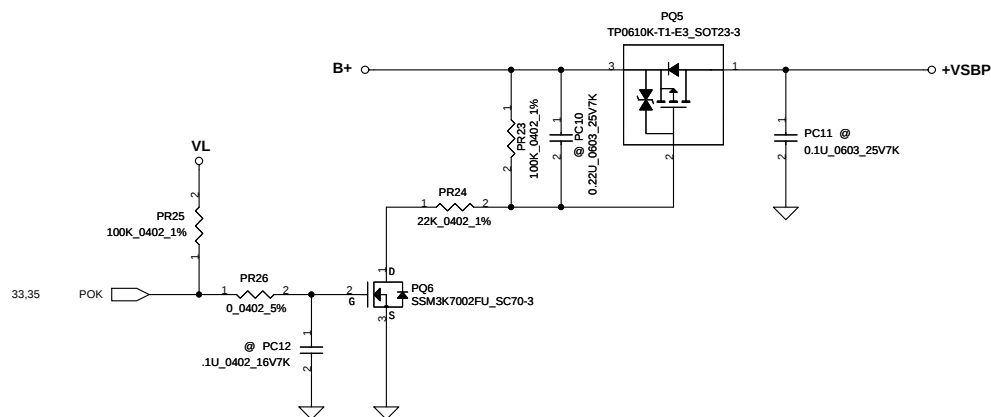
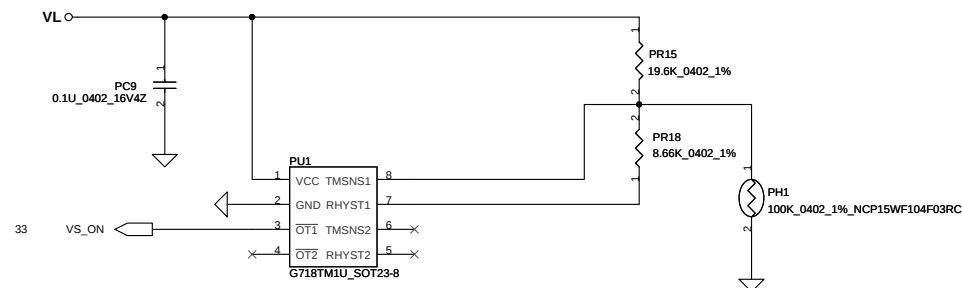
ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

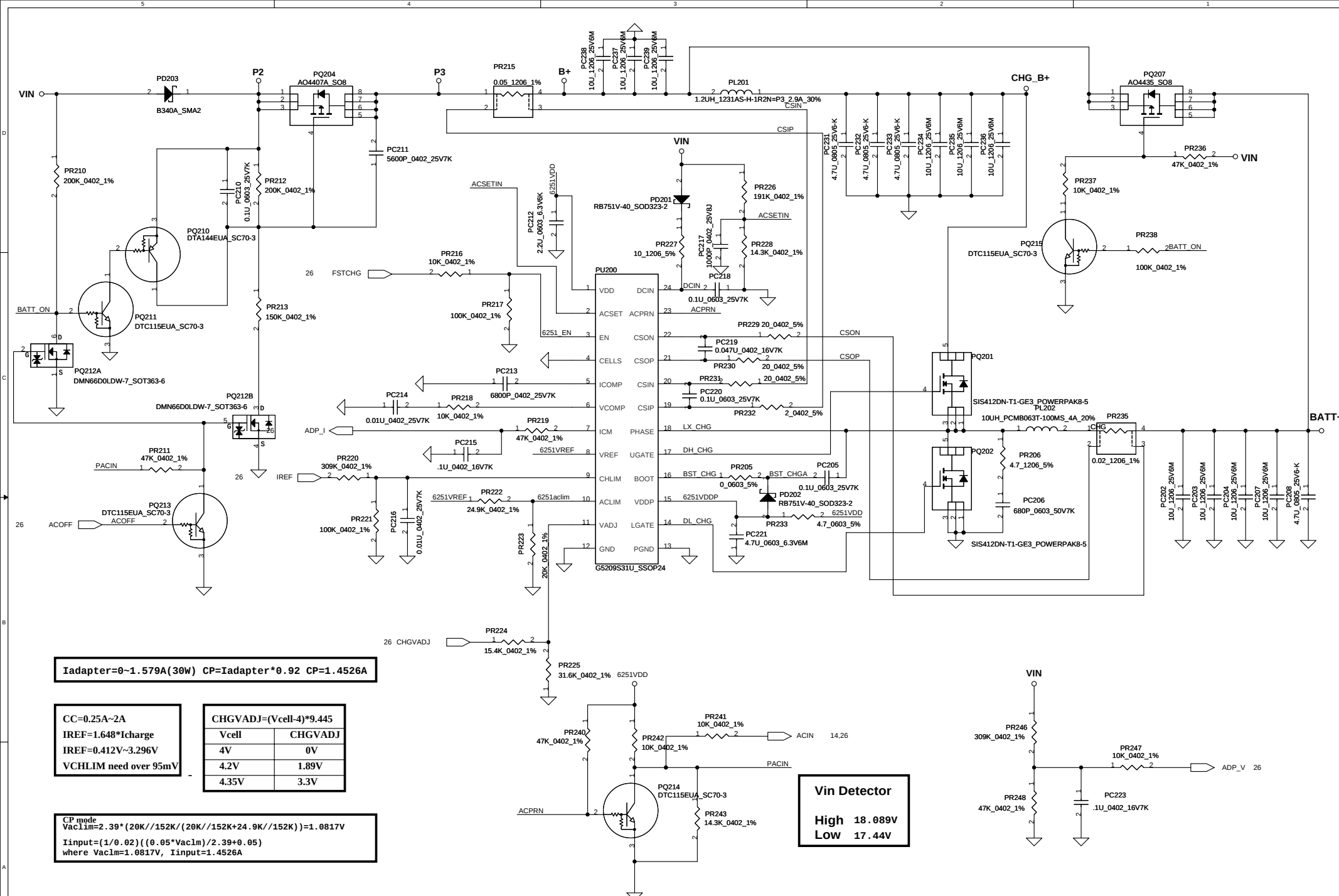
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PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



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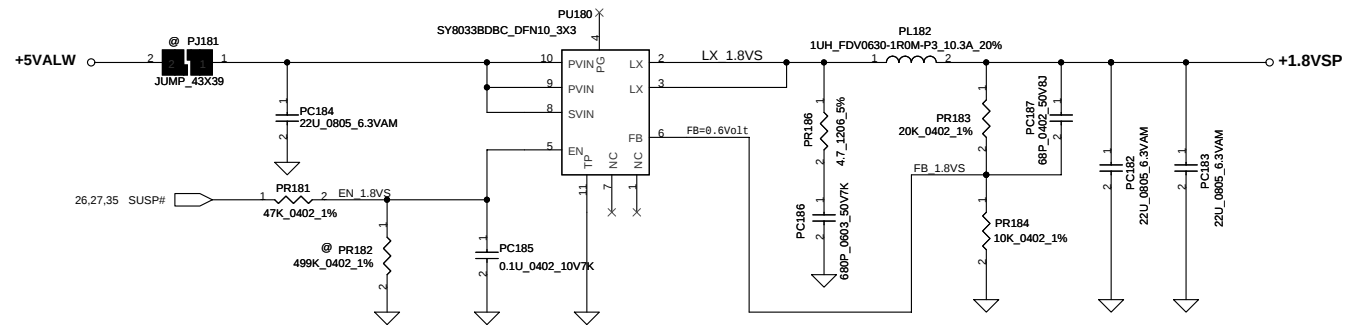
Iadapter=0~1.579A(30W) CP=Iadapter*0.92 CP=1.4526A

CC=0.25A~2A
IREF=1.648*Icharge
IREF=0.412V~3.296V
VCHLIM need over 95mV

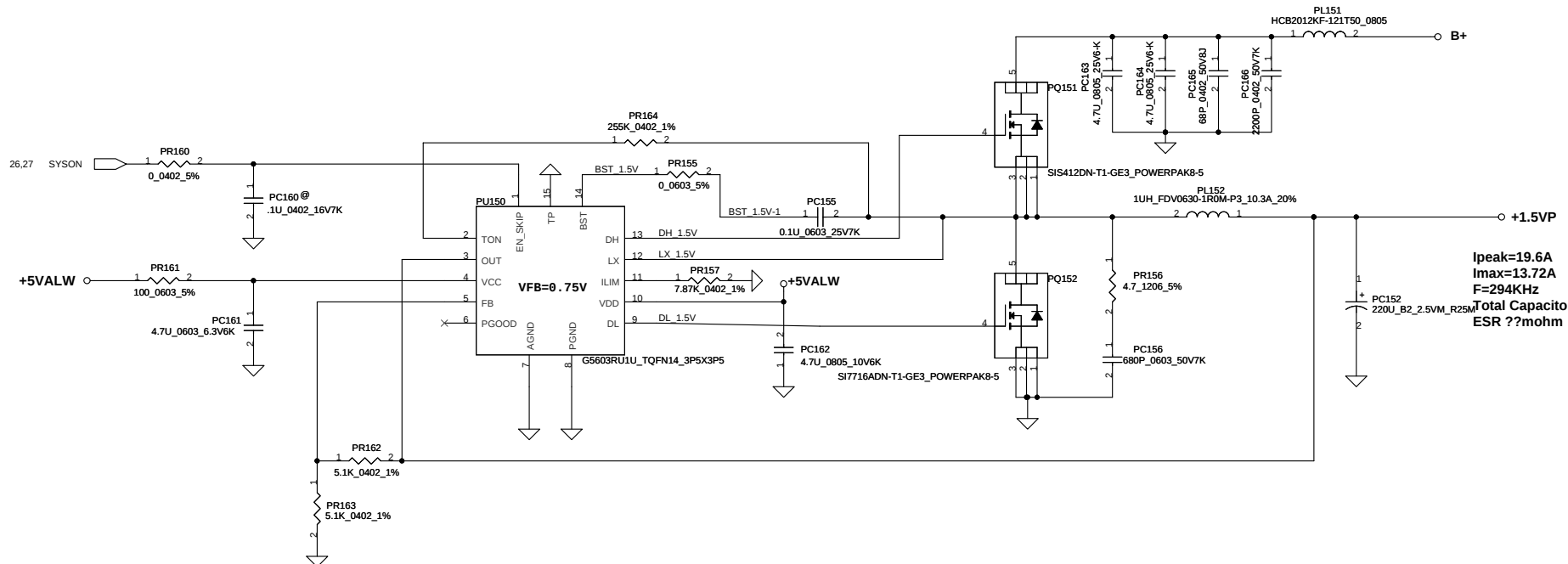
CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.89V
4.35V	3.3V

CP mode
VacLim=2.39*(20K/(152K/(20K/(152K+24.9K/(152K))=1.0817V
Iinput=(1/0.02)*((0.05*VacLim)/2.39+0.05)
where VacLim=1.0817V, Iinput=1.4526A

Vin Detector
High 18.089V
Low 17.44V

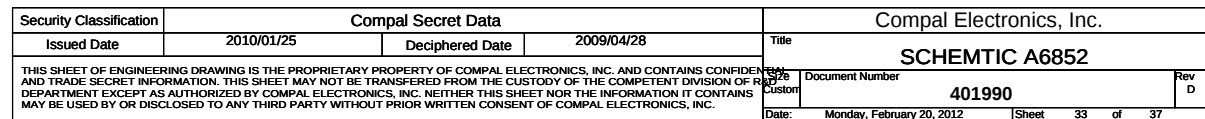
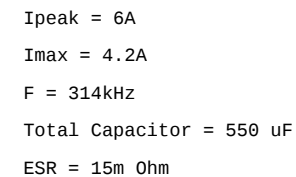


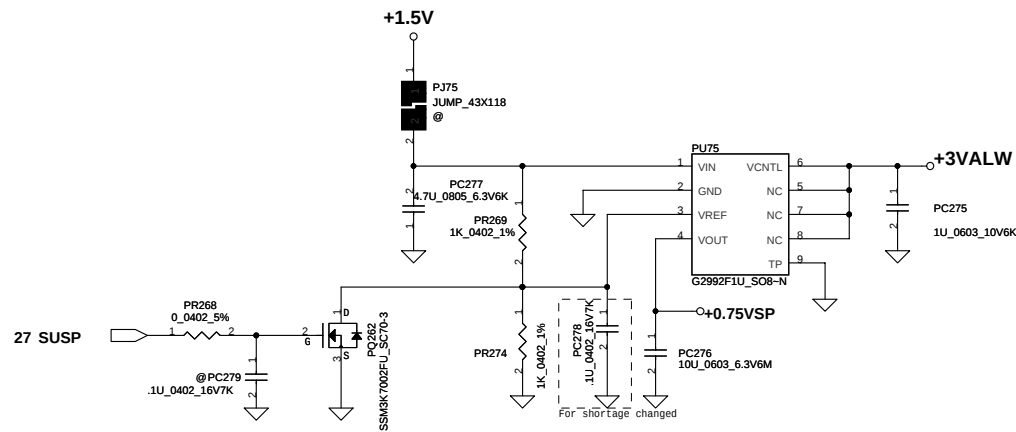
Ipeak=1.308A
ILIM = 4A
F=1MHz
Total Capacitor ??uF,
ESR ??mohm



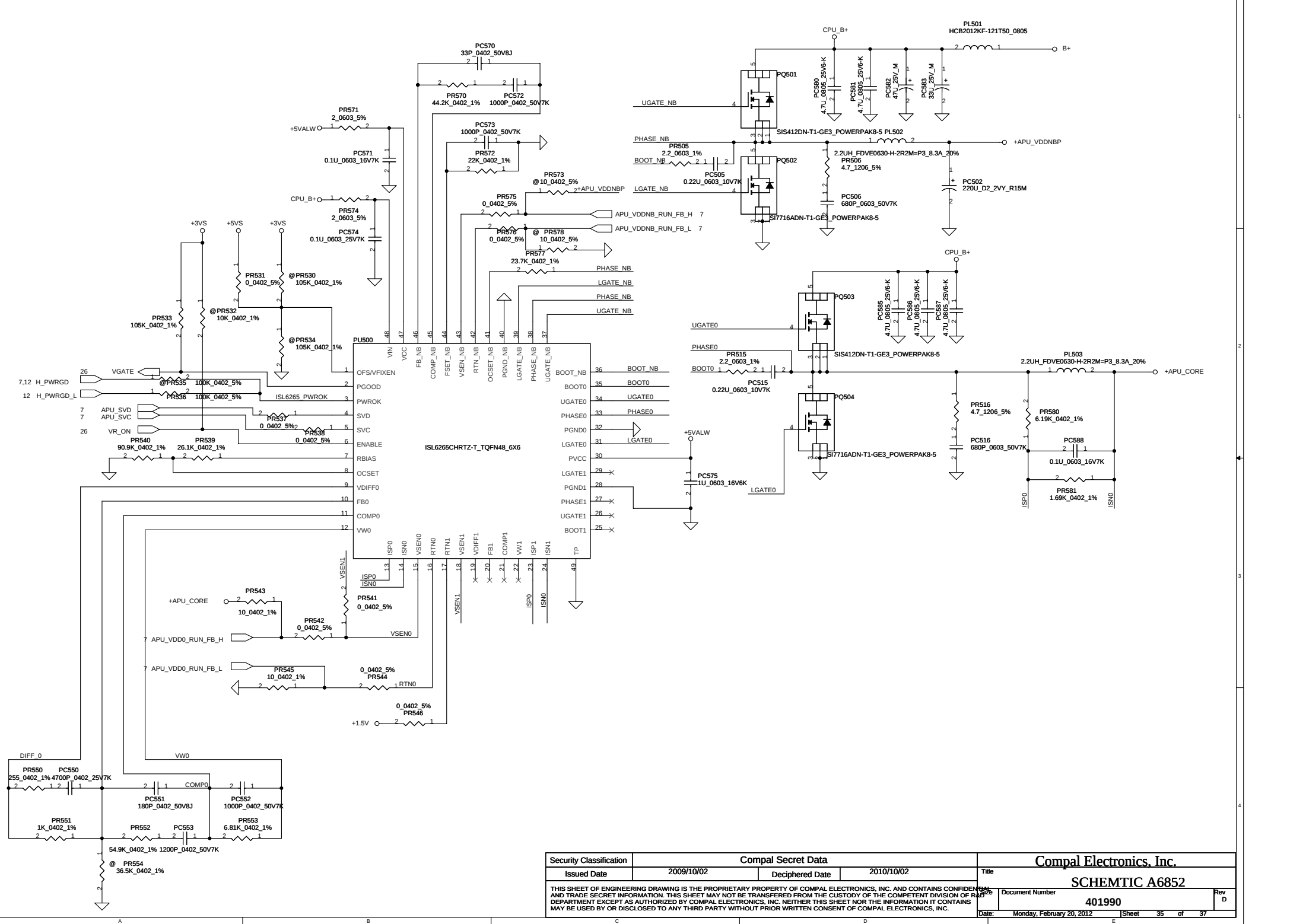
Ipeak=19.6A
Imax=13.72A
F=294KHz
Total Capacitor ??uF,
ESR ??mohm

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Issued Date		2009/10/02	Deciphered Date	2010/10/02	Document Number
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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2010/08/01	POWER		Release
P31	BATTERY CONN / OTP	2010/09/02	POWER	Add PD5,PD6 (For ESD)	DVT
P32	CHARGER	2010/09/02	POWER	Add PR246,PR247,PR248,PC223 (ADP_V)	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR337,PR357 change to 121k	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR365 change to 19.6k	DVT
P34	1.8VSP/1.5VP	2010/09/02	POWER	PR181 change to 150k, PC185 0.1uF	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PR91 change to 316k(For 1.05VSP)	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PC90 change to 39pF(1.05VSP)	DVT
P37	ACPU_CORE	2010/09/02	POWER	Add PR578 10_0402_5% , PR573 unpop.	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR577 change to 23.7k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR539 change to 26.1k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR540 change to 90.9k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PC551 change to 100pF	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR546 change to 0_0402_5%	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR580 change to 6.98k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR581 change to 1.87k	DVT
P32	CHARGER	2010/09/06	POWER	Add PC207,PC239 10uF (EMI)	DVT

Item	Reason for change	PG#	Modify List	Date	Phase
1	Update JLVDS1 footprint	P10	ME request	2009/12	EVT->DVT
2					EVT->DVT
3					EVT->DVT
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