

Compal Confidential

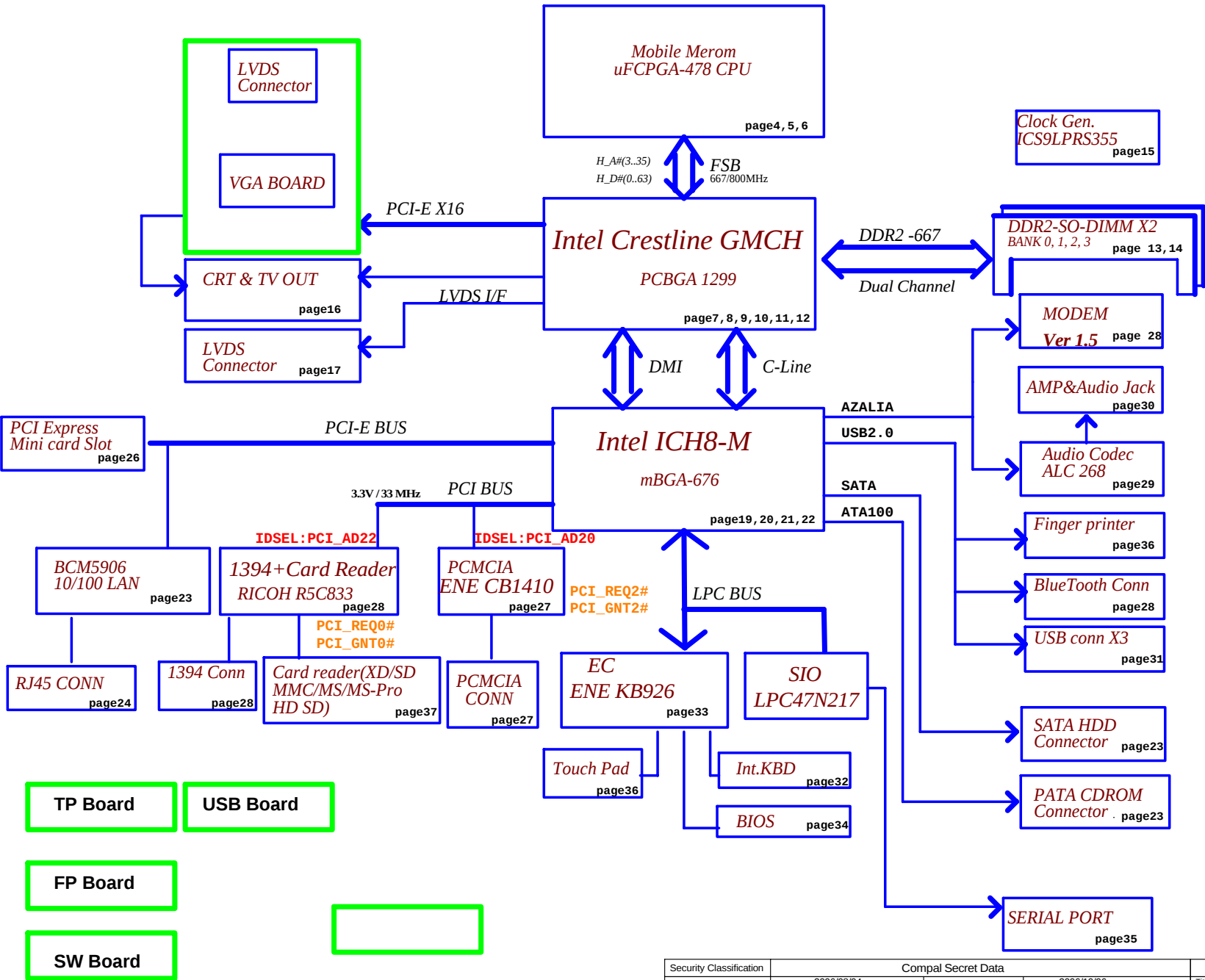
Tuesday, March 06, 2007

IGT10/11 Schematics Document

Mobile Merom uFCPGA with Intel
Crestline_GM/PM+ICH8-M core logic

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REV:0.2



Voltage Rails 0 MEANS ON X MEANS OFF

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	CLOCK
S0	0	0	0	0	0
S3	0	0	0	X	0
S5 S4/AC	0	0	X	X	0
S5 S4/ Battery only	0	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
* 1	IEL10	
2	IDL11	IDL01
3	HDL10	HDL00
4		HDL20
5	IDL12	HDL30
6		
7		

MB ID	
H	15"
L	14"

BOM Structure

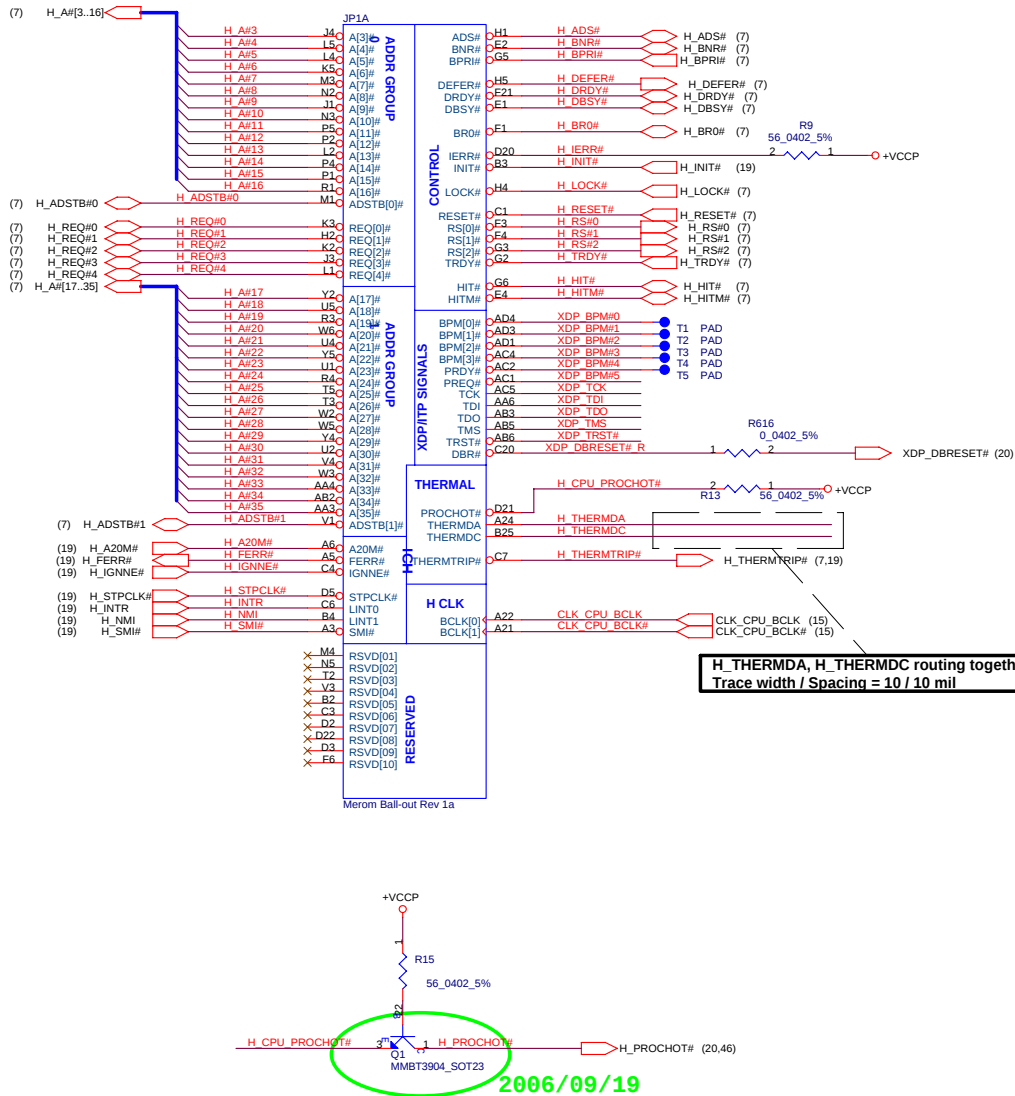
MARK	FUNCTION
@	NC FOR ALL
GIGA@	BCM5787
100@	BCM5906
UMA@	Internal 965GM
VGA@	965PM + Ext VGA

Address

USB PORT LIST

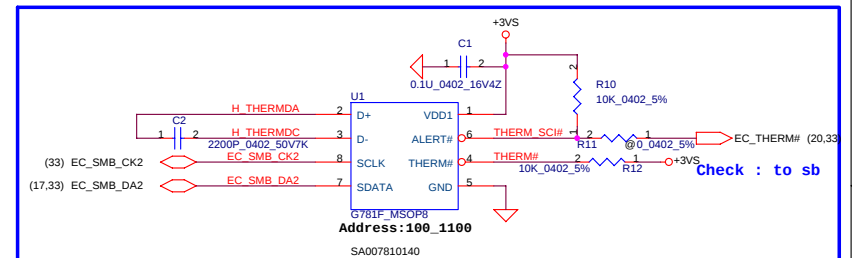
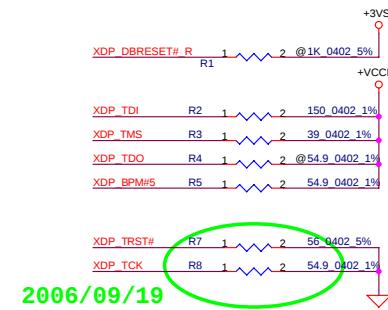
PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	RIGHT SIDE
7	BT(HDL20)
8	FINGER PRINTER
9	TV TUNER

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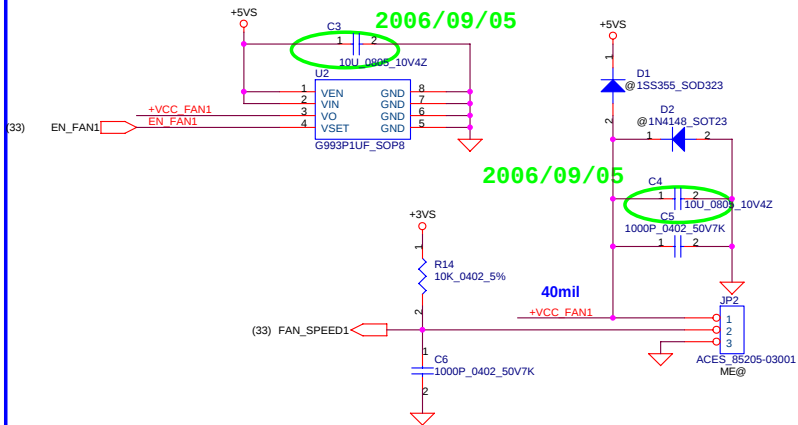


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

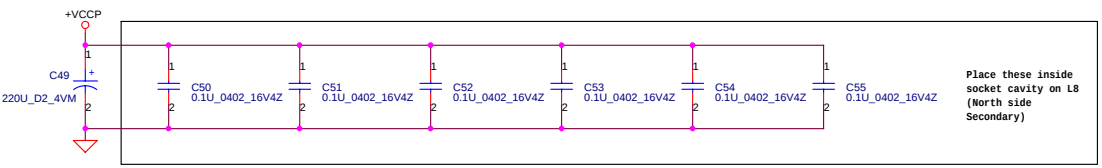
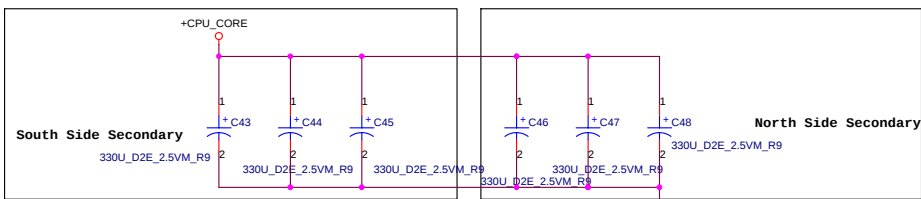
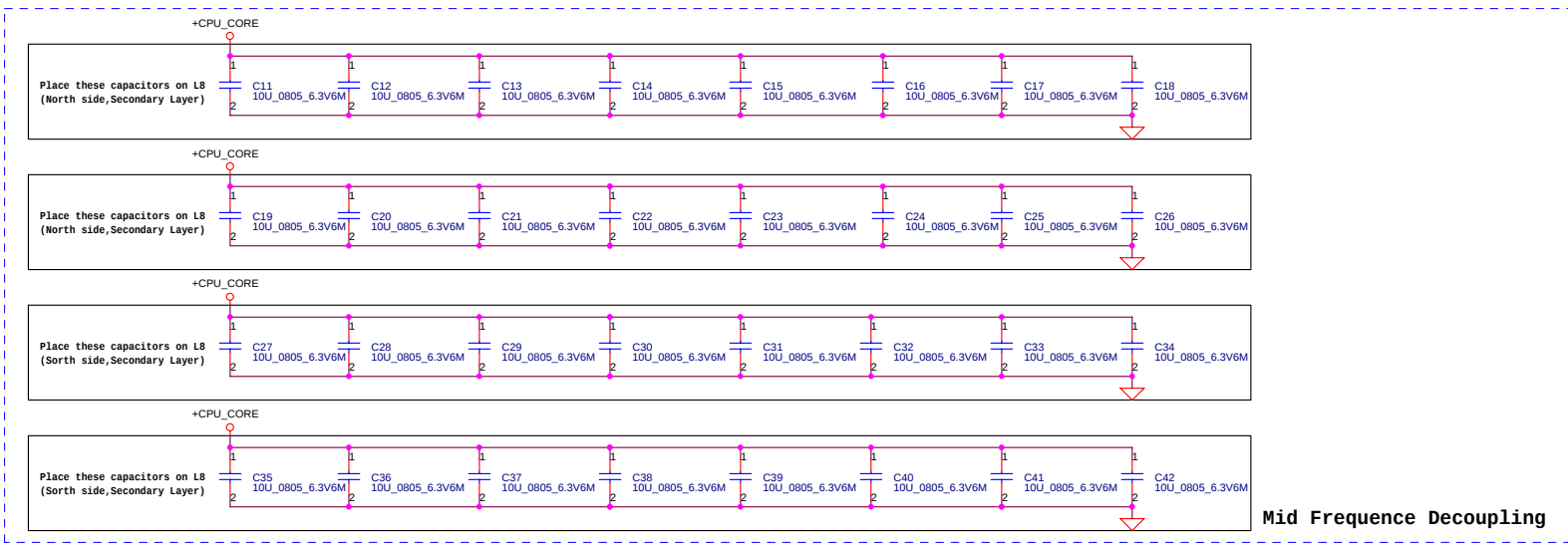
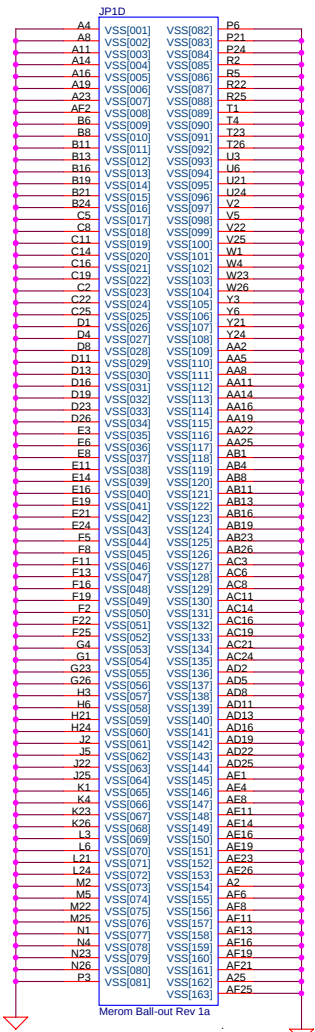
XDP Reserve

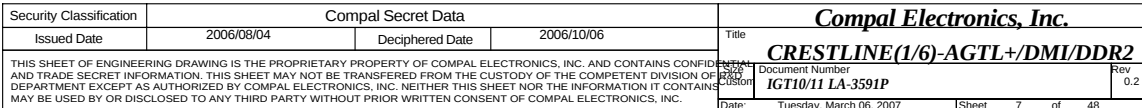


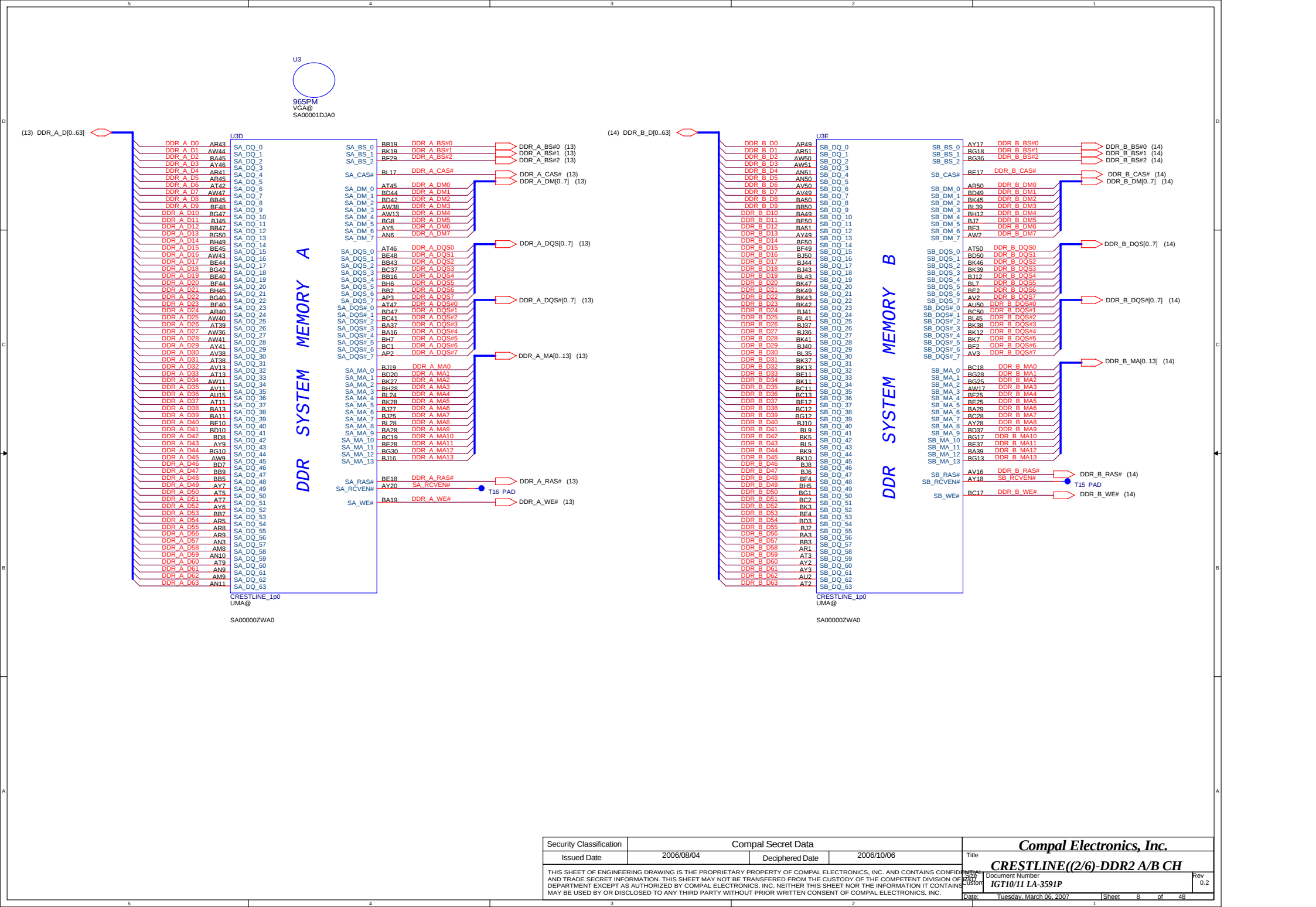
FAN1 Conn



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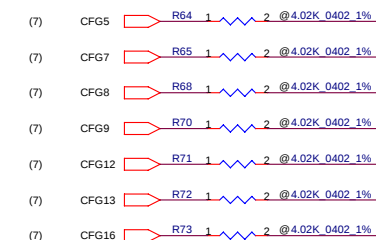




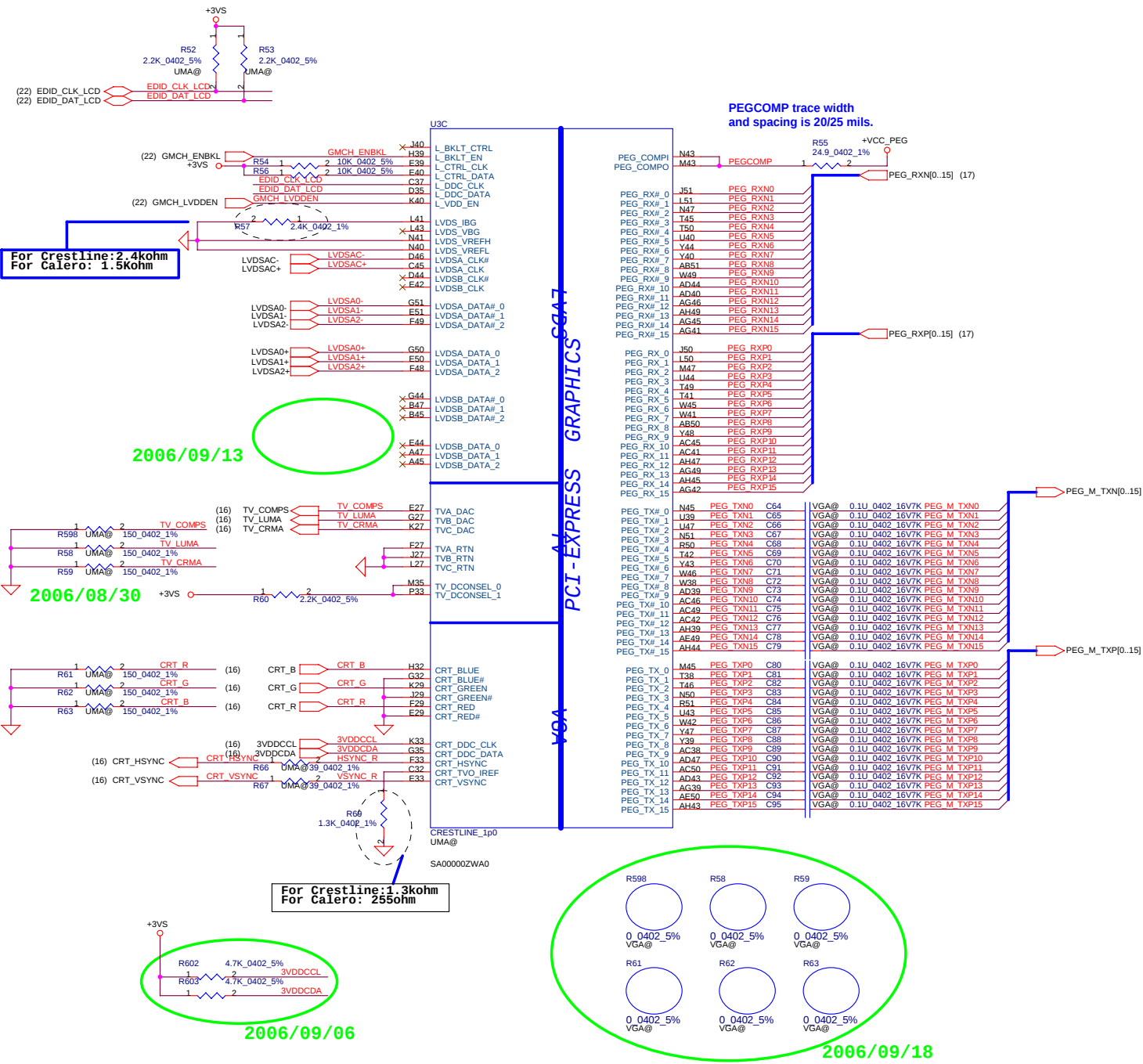


Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu. *



CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

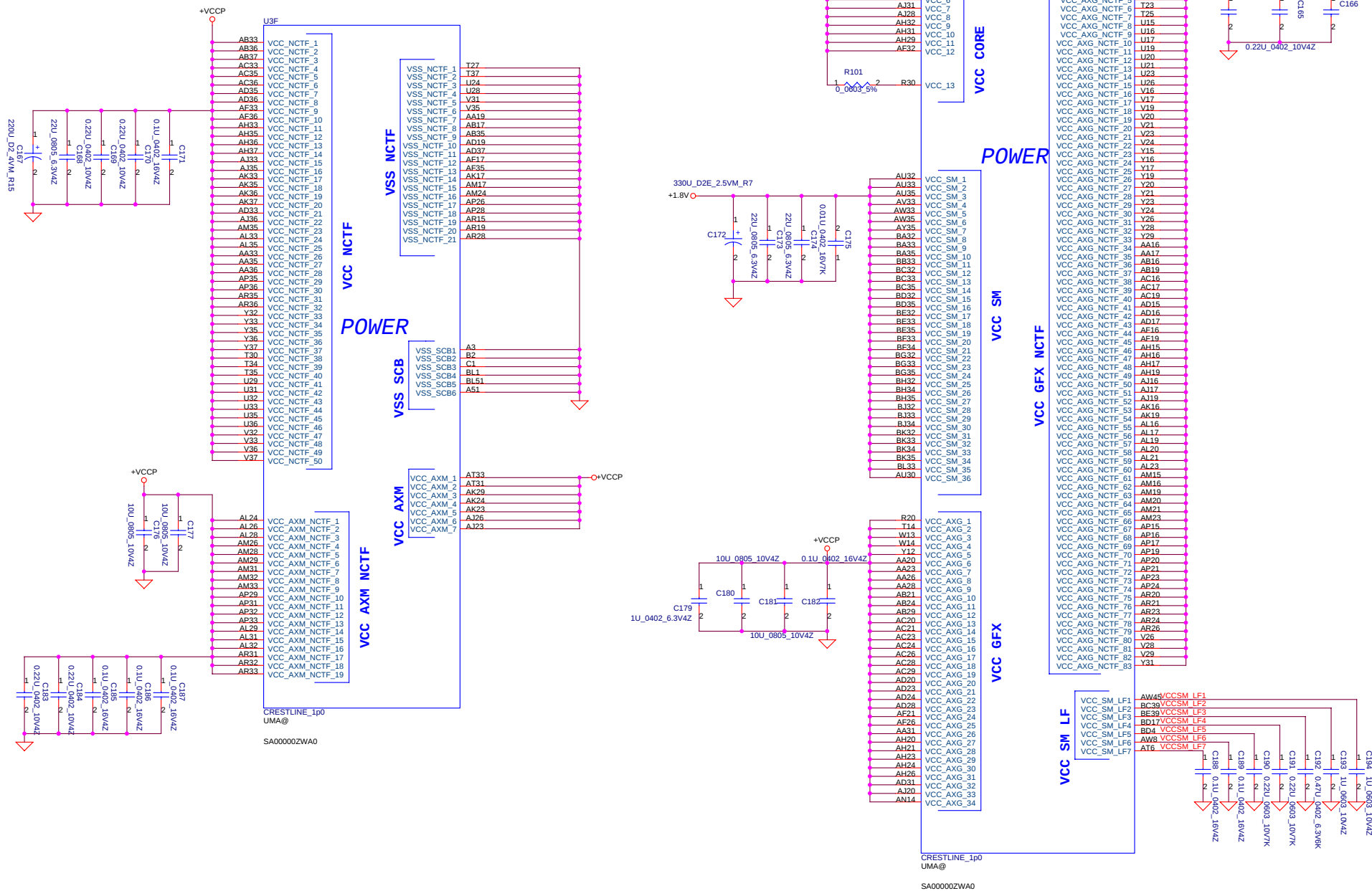


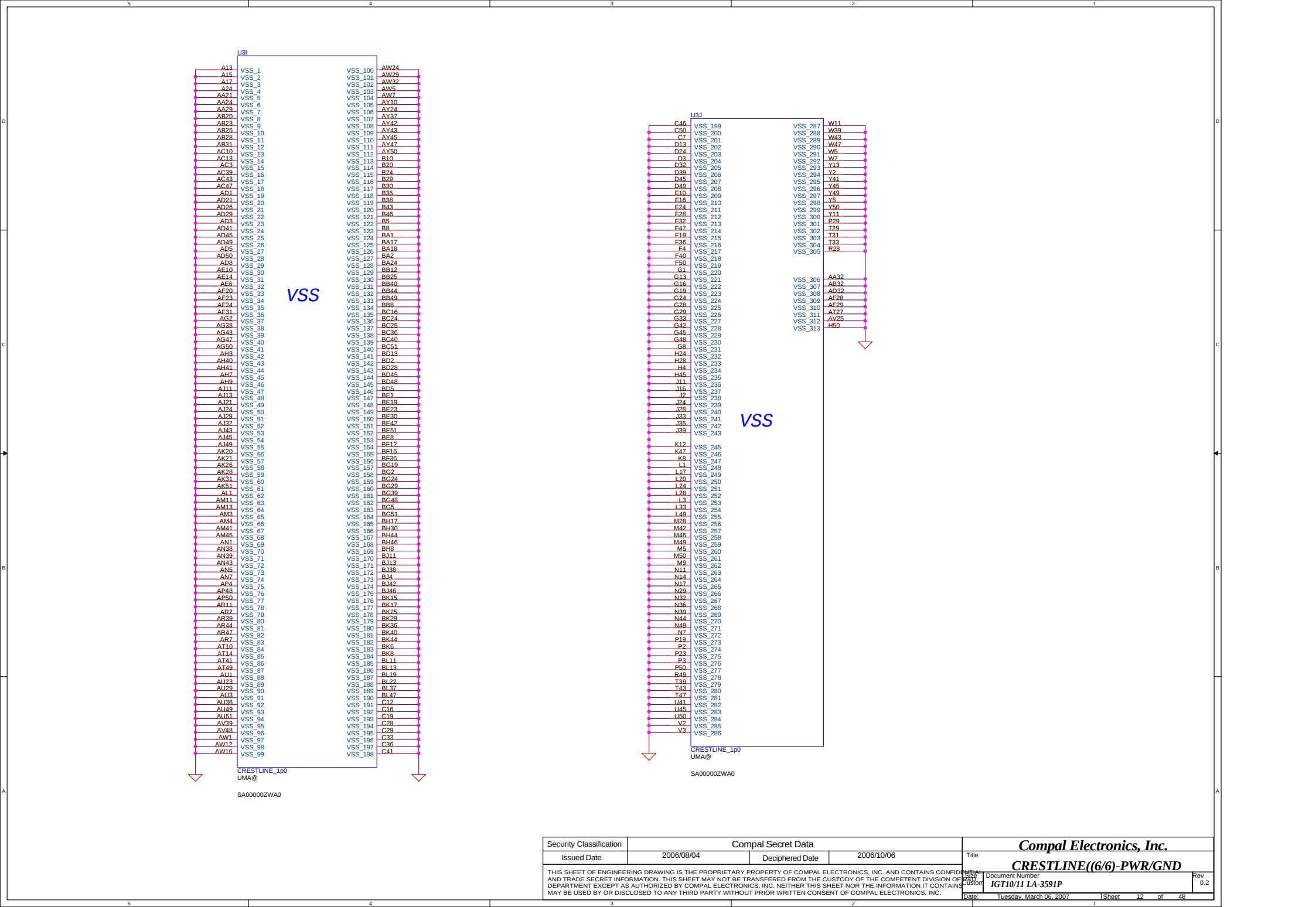
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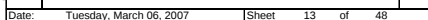
CRESTLINE (3/6)-VGA/LVDS/TV

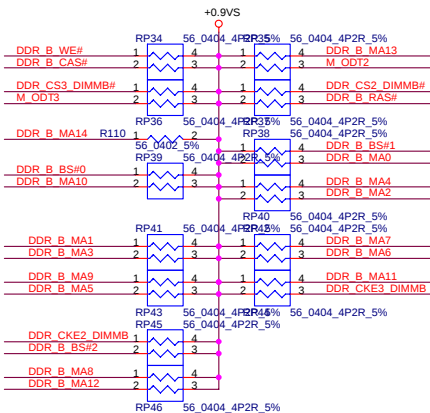
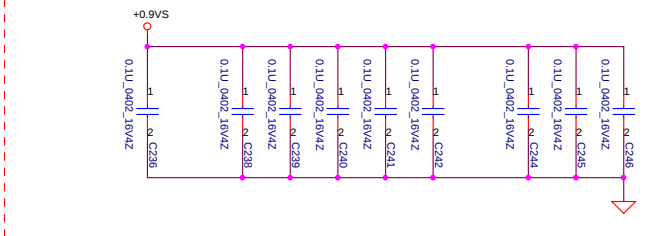
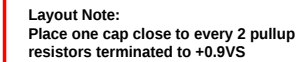
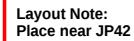
IGTI011 LA-3591P



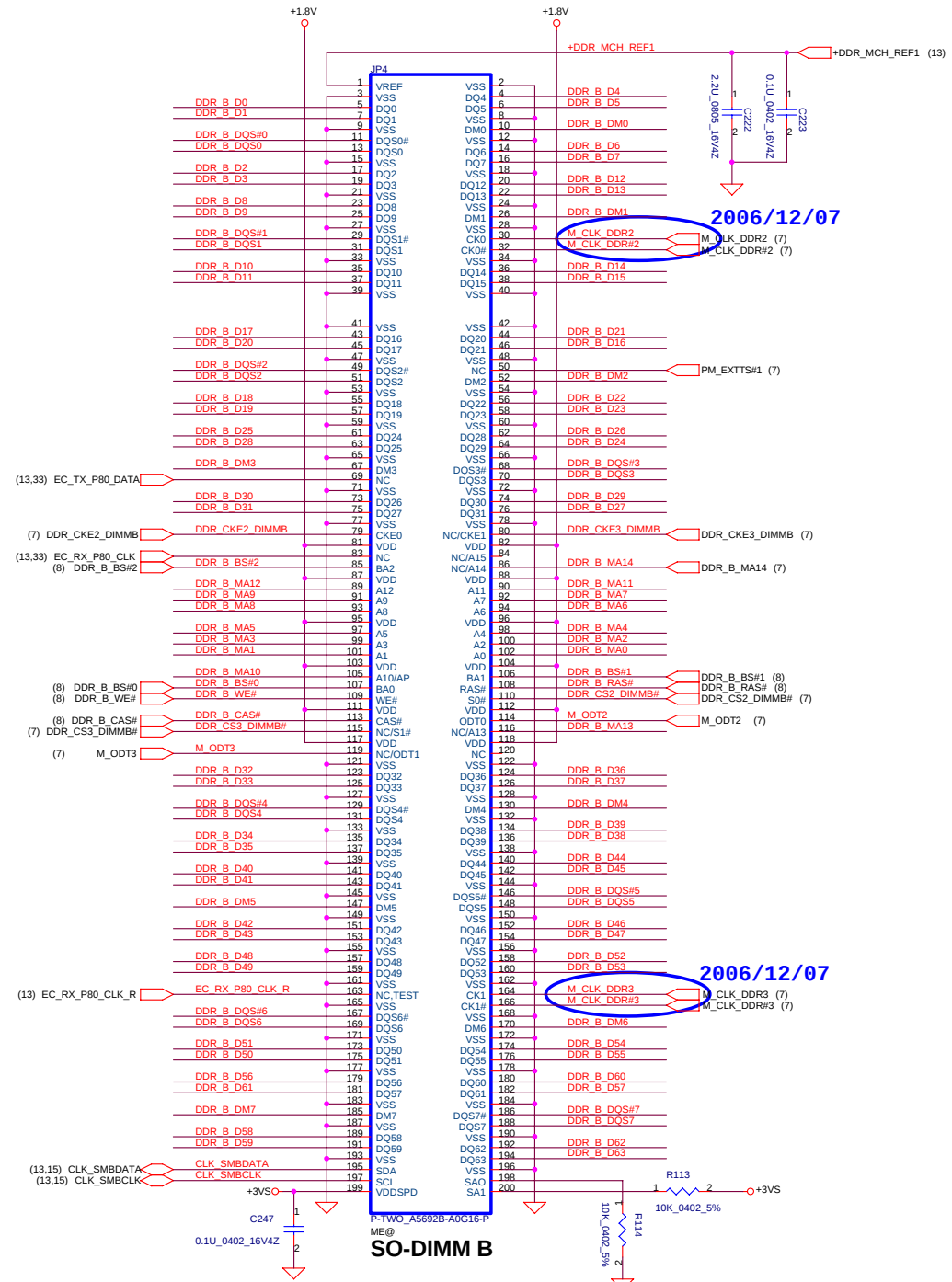


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Layout Note:
Place these resistor
closely JP4,all
trace length Max=1.5"

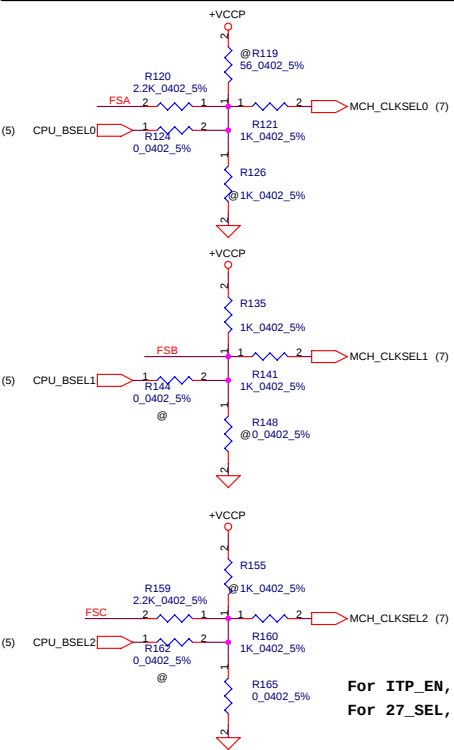


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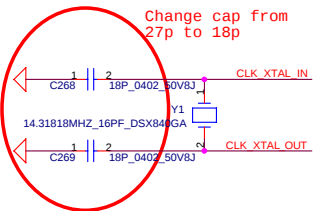
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

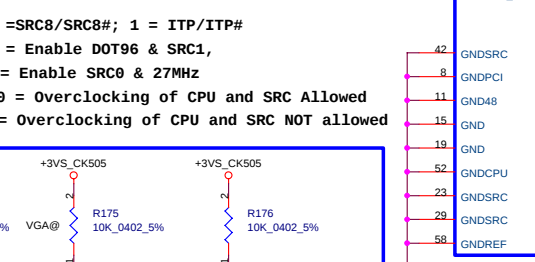
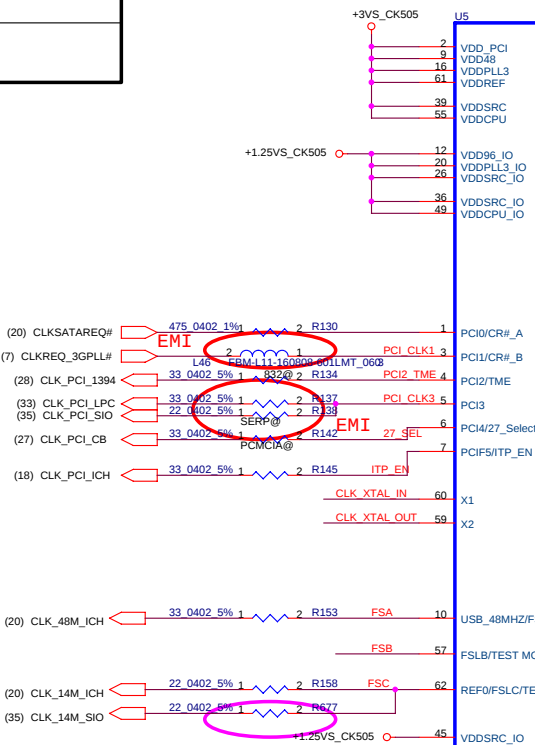
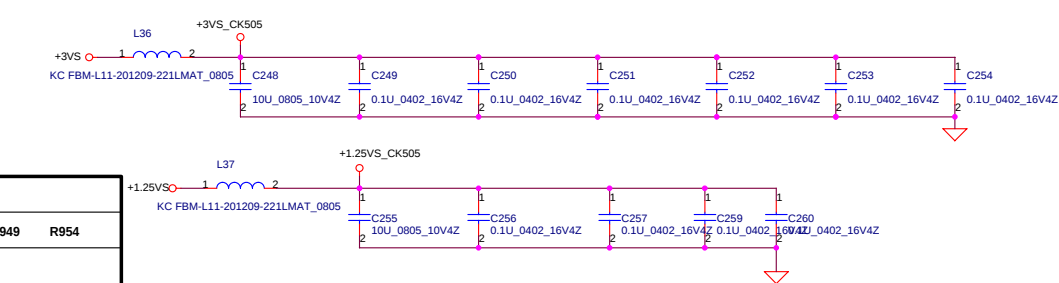
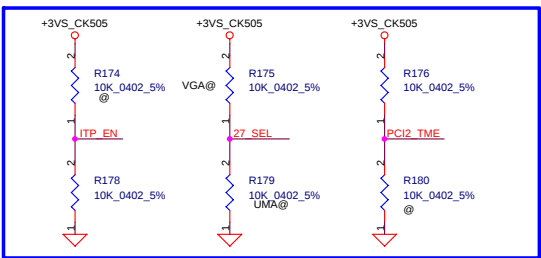
CPU Driven	Stuff	R919	R940	R956
*(Default)	No Stuff	R914	R921	R930
	Stuff	R959	R930	R914
667MHz	No Stuff	R919	R940	R956
	Stuff	R949	R943	R921
800MHz	No Stuff	R919	R940	R956
	Stuff	R949	R943	R914



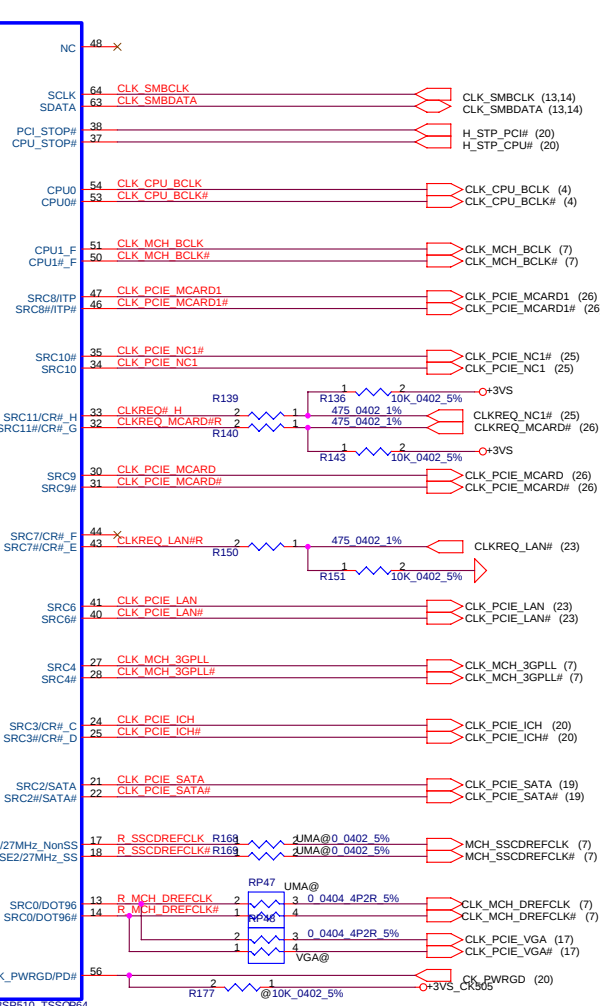
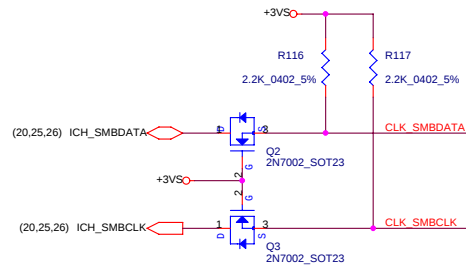
For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil



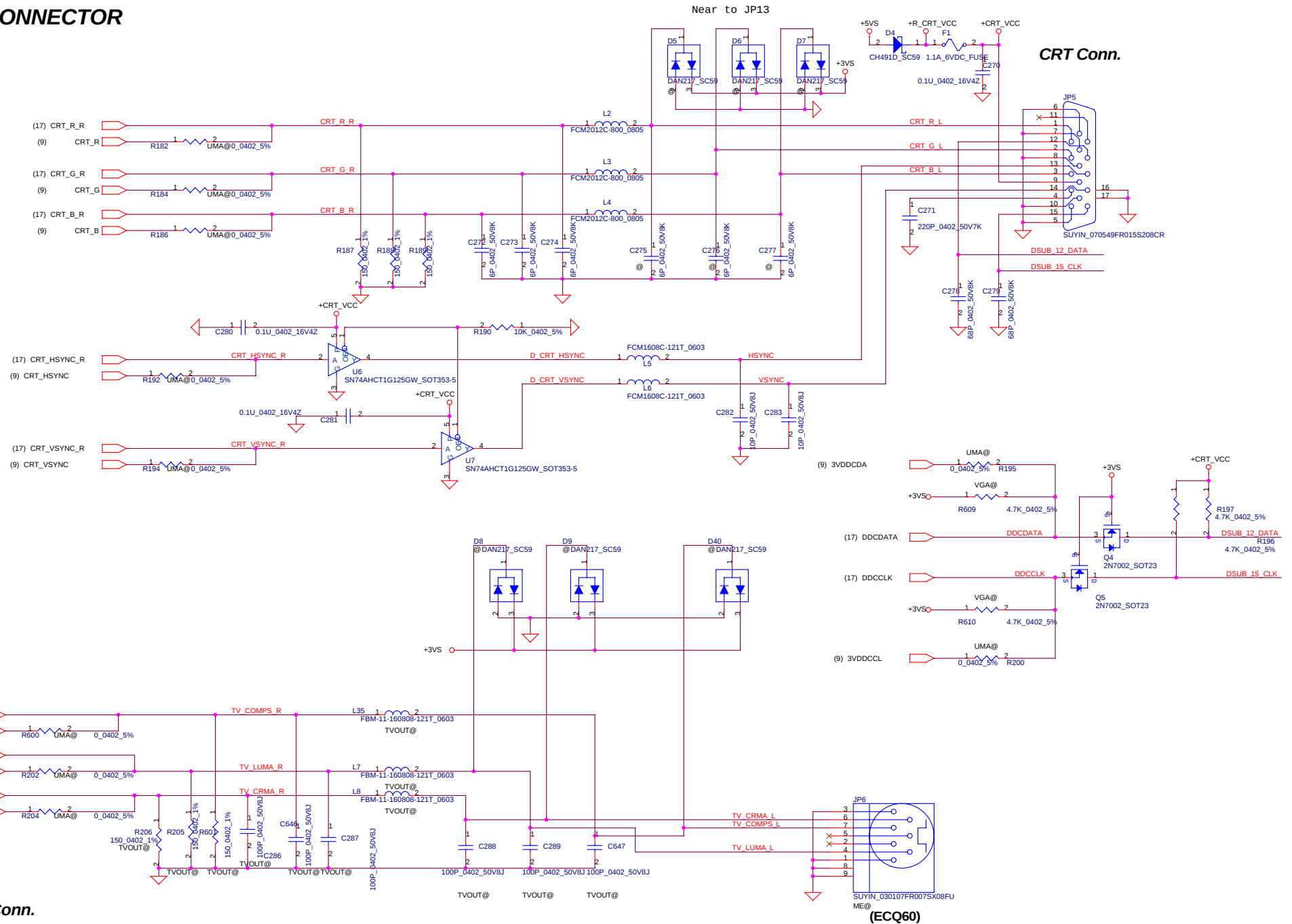
* Internal Pull-Up Resistor
** Internal Pull-Down Resistor



Place close to U41

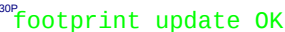
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CRT CONNECTOR

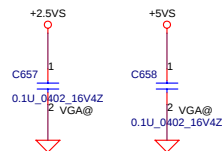
**TV-OUT Conn.**

1. Y ground
2. C ground
3. Y (luminance+sync)
4. C (chrominance)

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2006/09/13



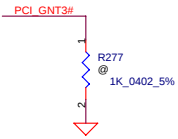
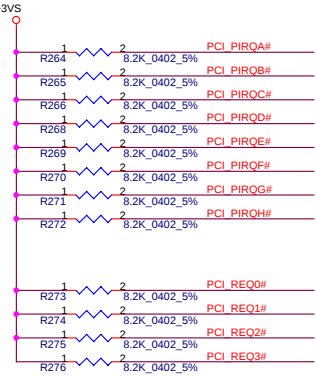
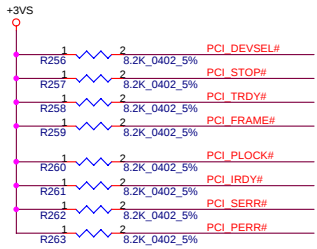
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MXM CONN

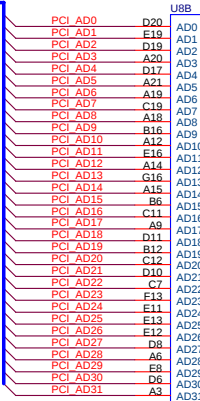
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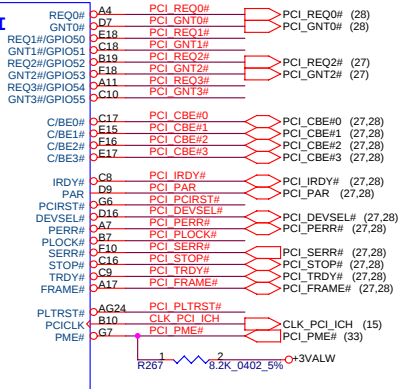
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(27,28) PCI_AD[0..31]



PCI



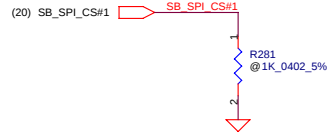
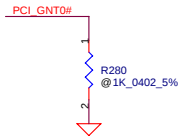
Interrupt I/F



ICH8M REV 1.0
SA000013U30

Boot BIOS Strap

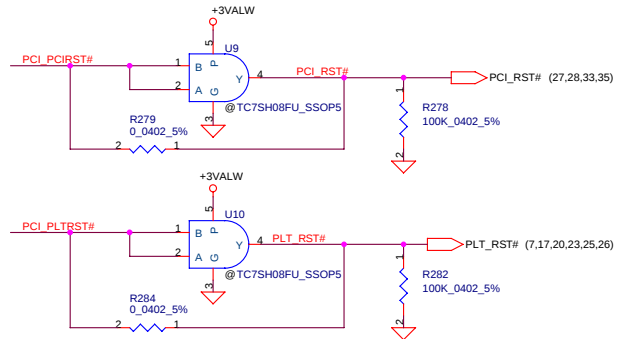
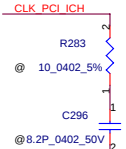
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



A16 swap override Strap

Low= A16 swap override Enble
High= Default *

Place closely pin B10



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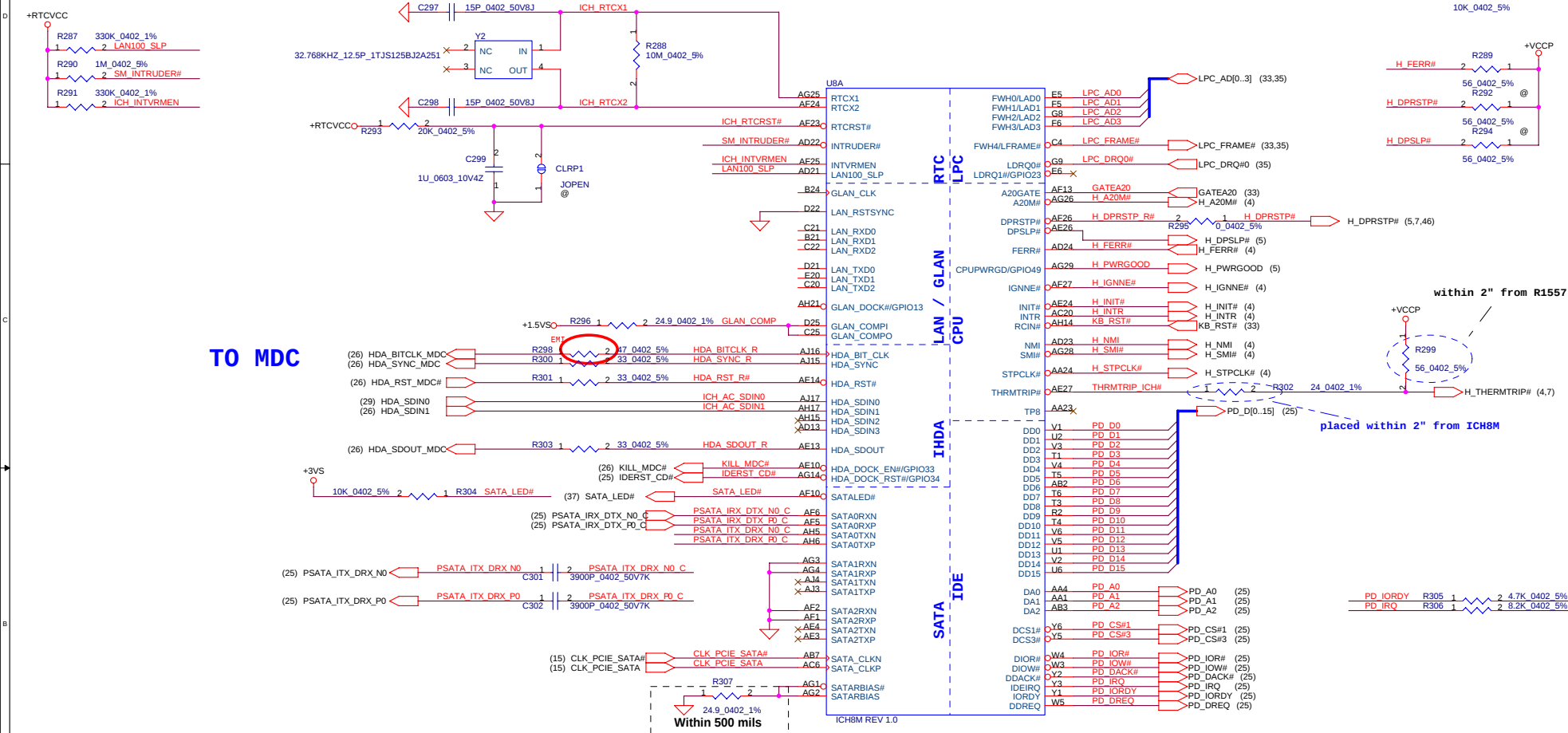
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ICH8(1/4)-PCI/INT

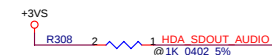
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ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

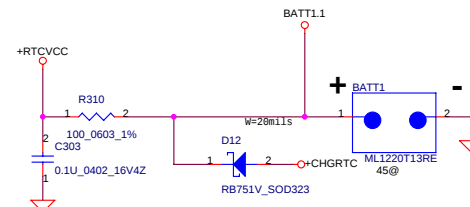
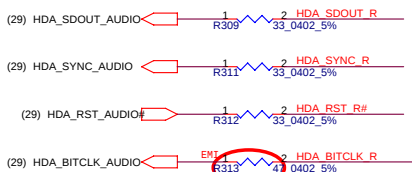
LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_INTVRMEN	



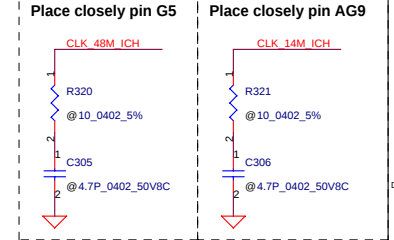
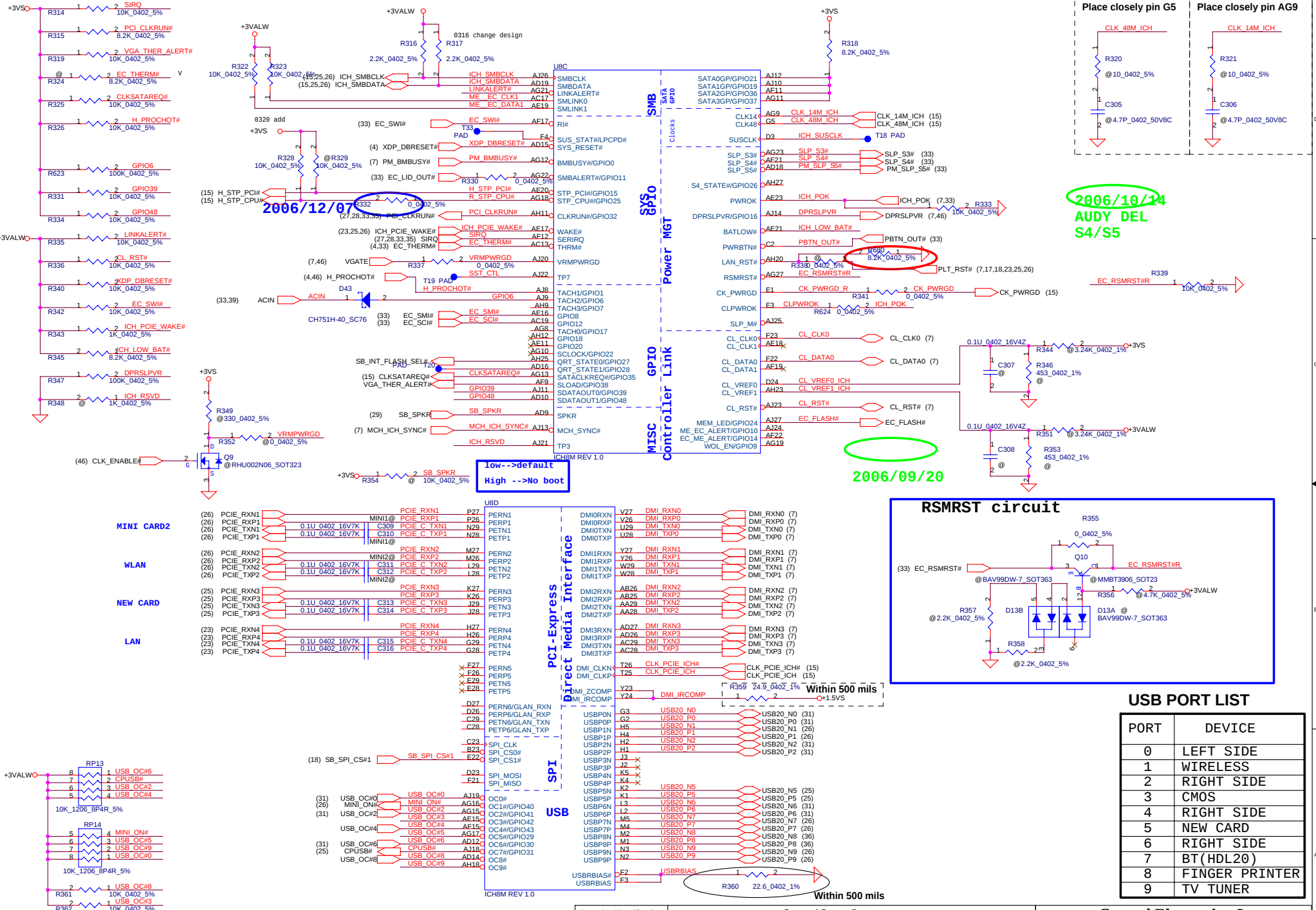
XOR CHAIN ENTRANCE STRAP:RSVD



TO CODEC Close to ICH

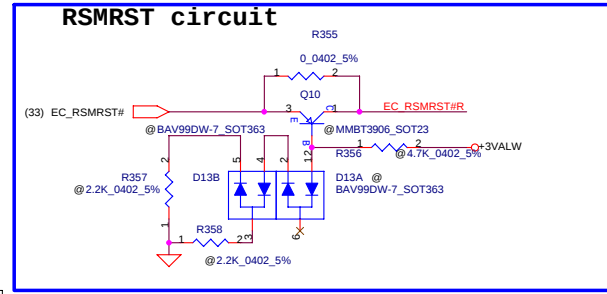


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Date:	Tuesday, March 06, 2007	Sheet	19	of 48



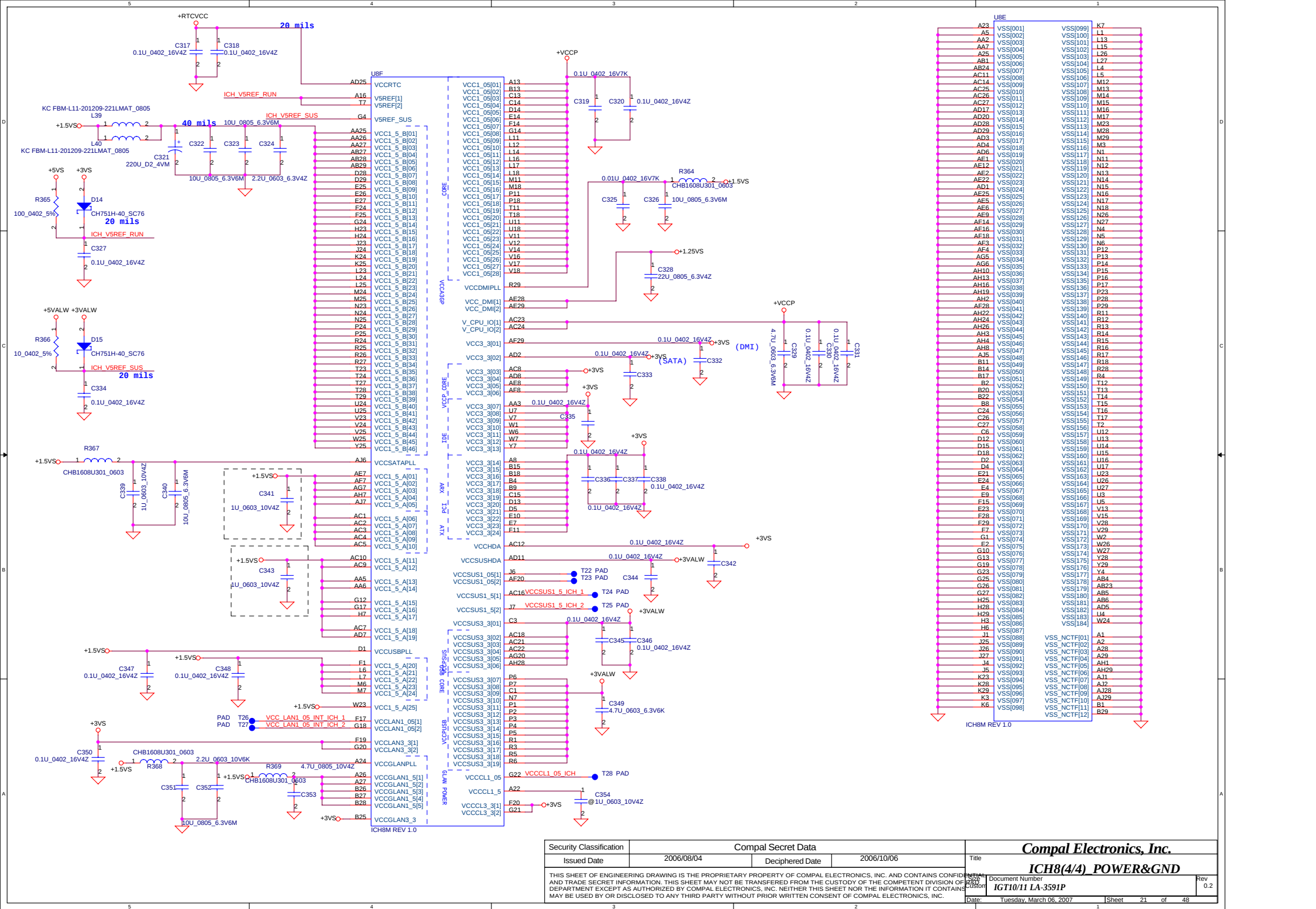
2006/10/24
AUDY DEL
S4/S5

2006/09/20

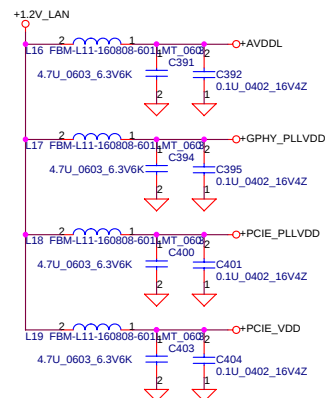
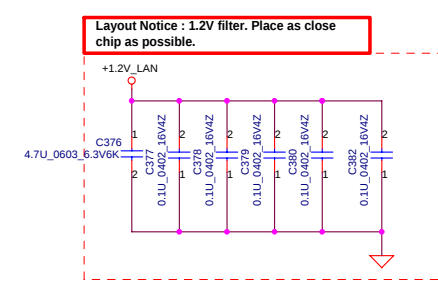
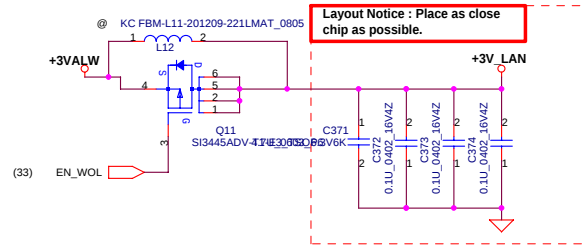
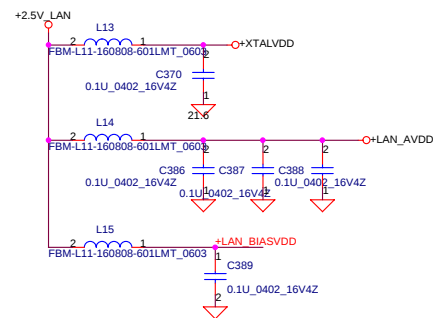


USB PORT LIST

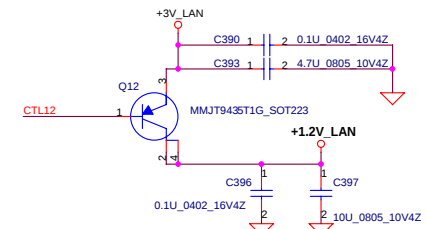
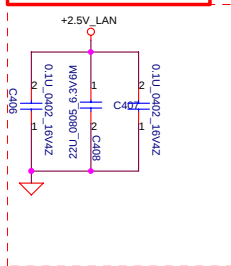
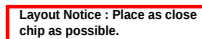
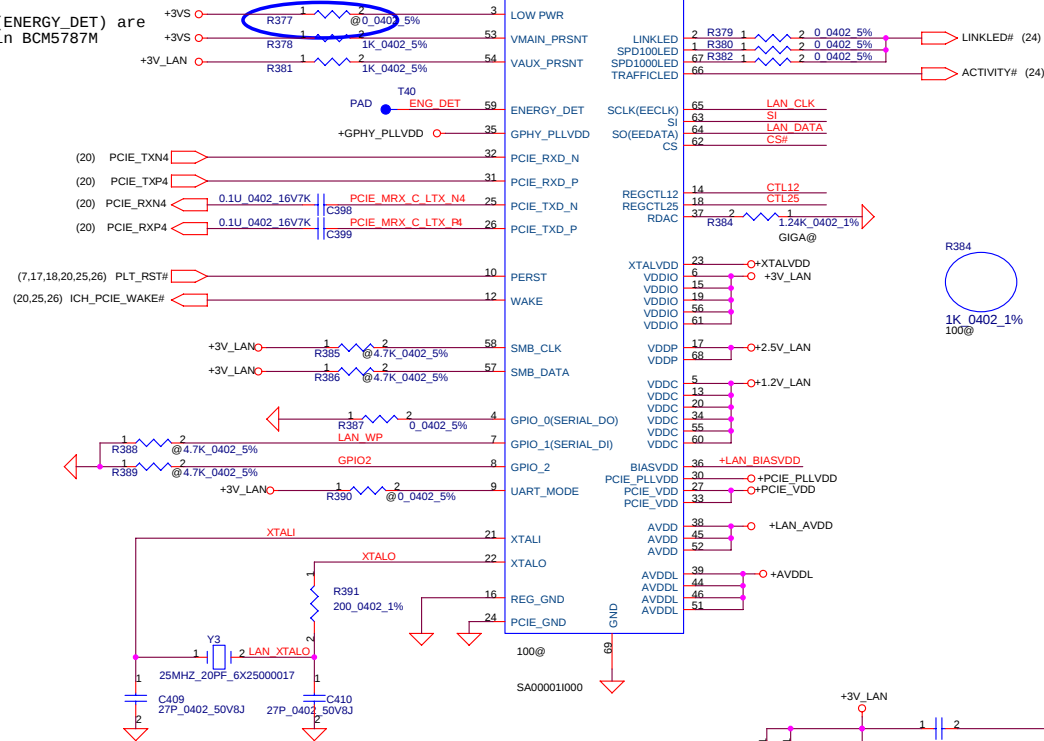
PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	RIGHT SIDE
7	BT(HDL20)
8	FINGER PRINTER
9	TV TUNER



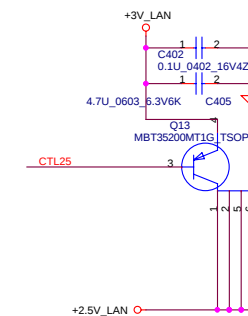
Layout Notice : Filter place as close chip as possible.



(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

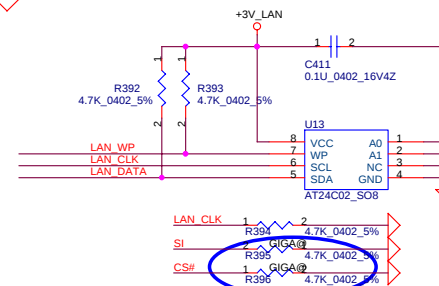


2006/12/26



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.



2006/12/27

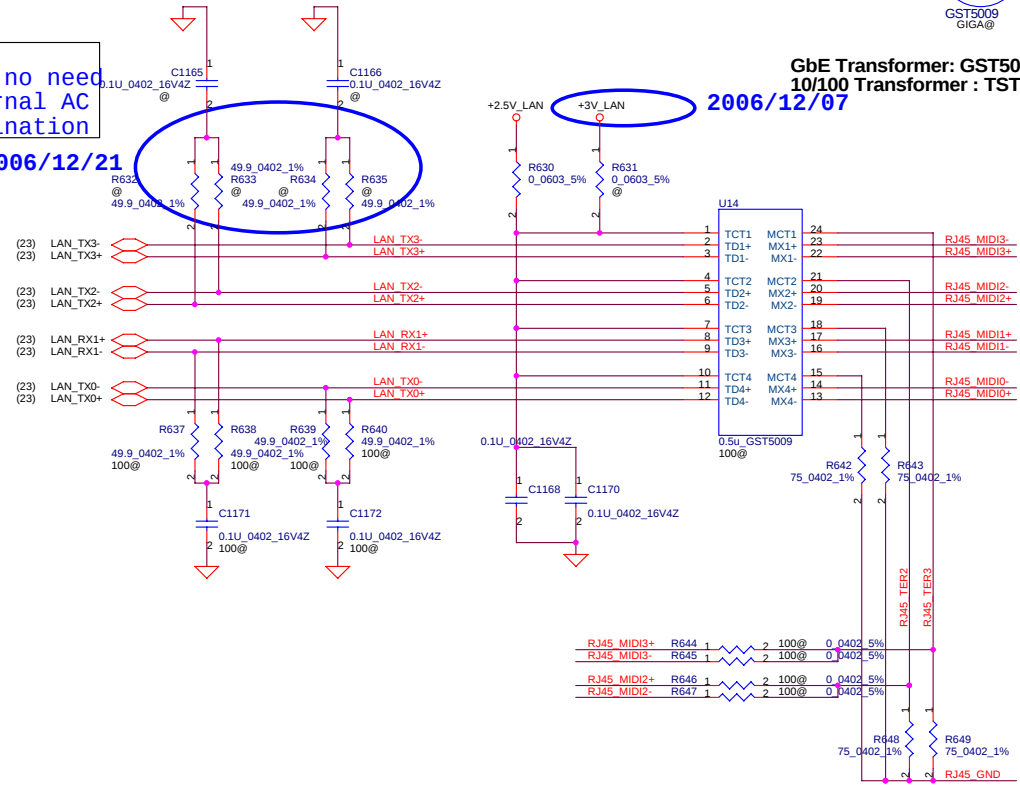
Security Classification	Compal Secret Data			2006/12/07	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	BCM5787MKML
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Date	Tuesday, March 06, 2007	Sheet	23	of	48

5787 no need
external AC
termination

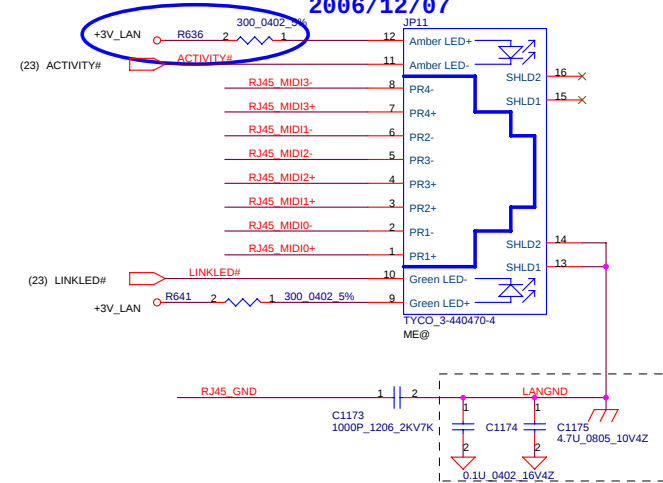
2006/12/21

2006/12/07

GbE Transformer: GST5009 (SP050005610)
10/100 Transformer : TST1284-LF (SP050001X10)



2006/12/07



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					IGT10/11 LA-3591P		0.2	
					Date: Tuesday, March 06, 2007		Sheet 24 of 48	

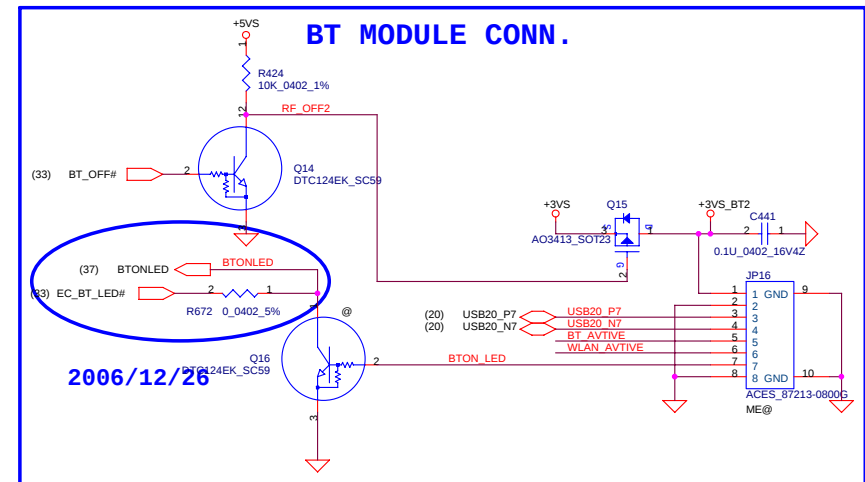
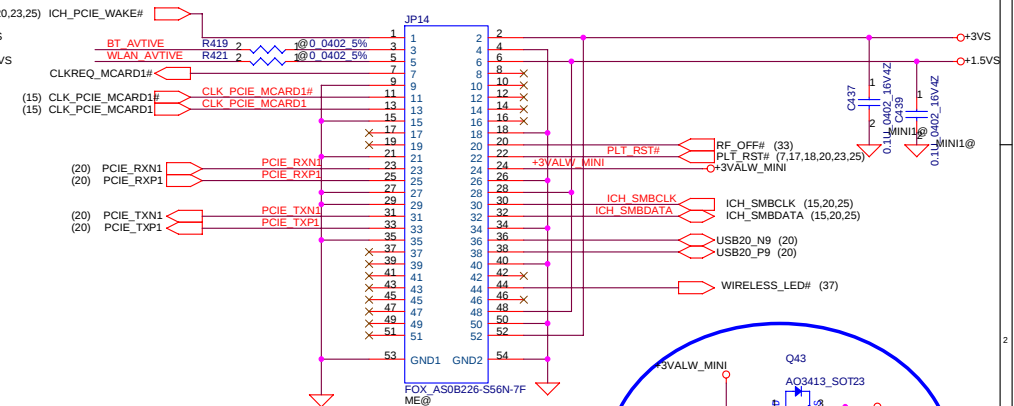


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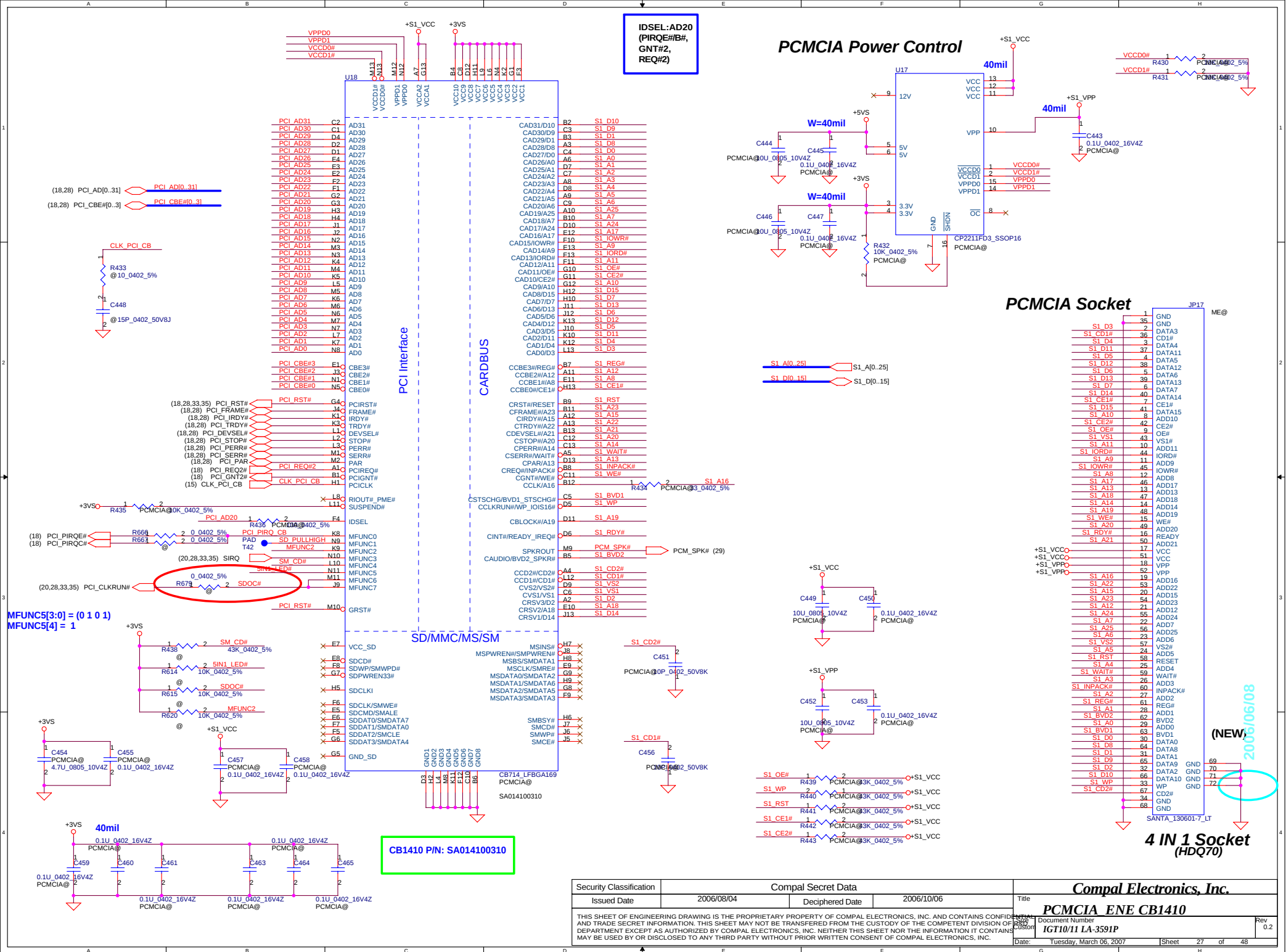


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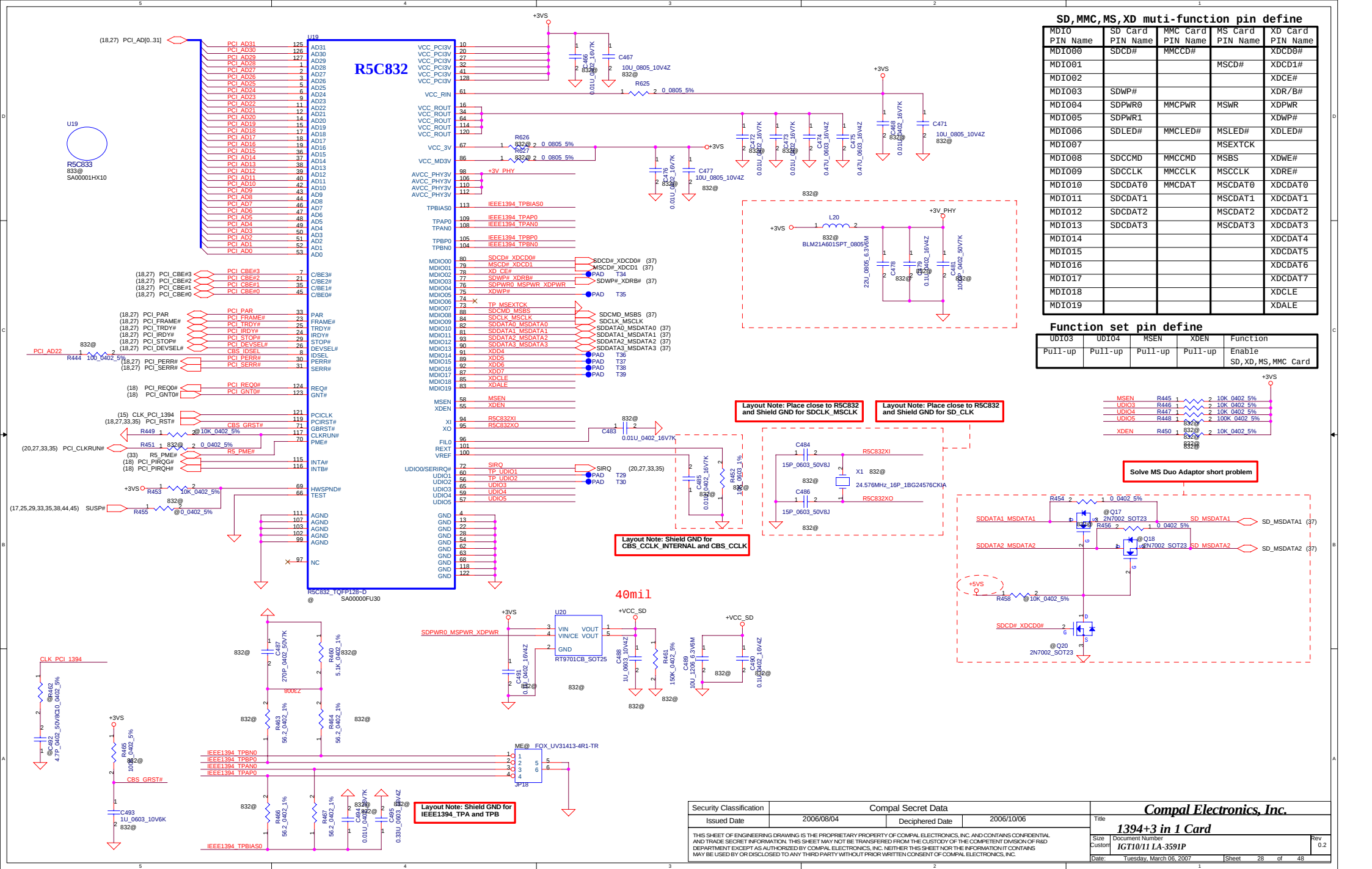
Mini-Express Card(Slot 2-TV-Tuner)

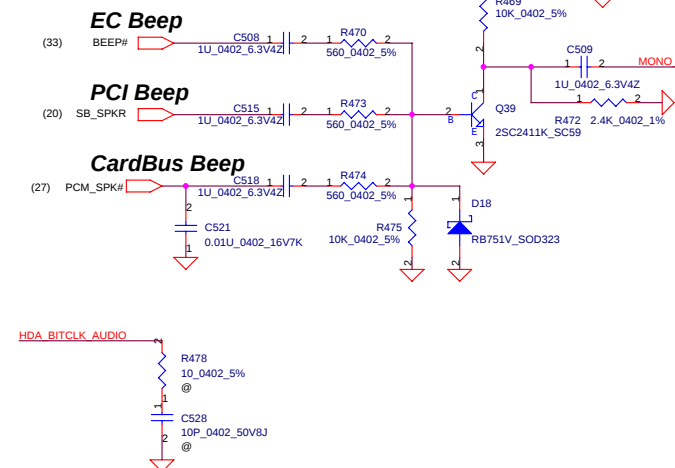
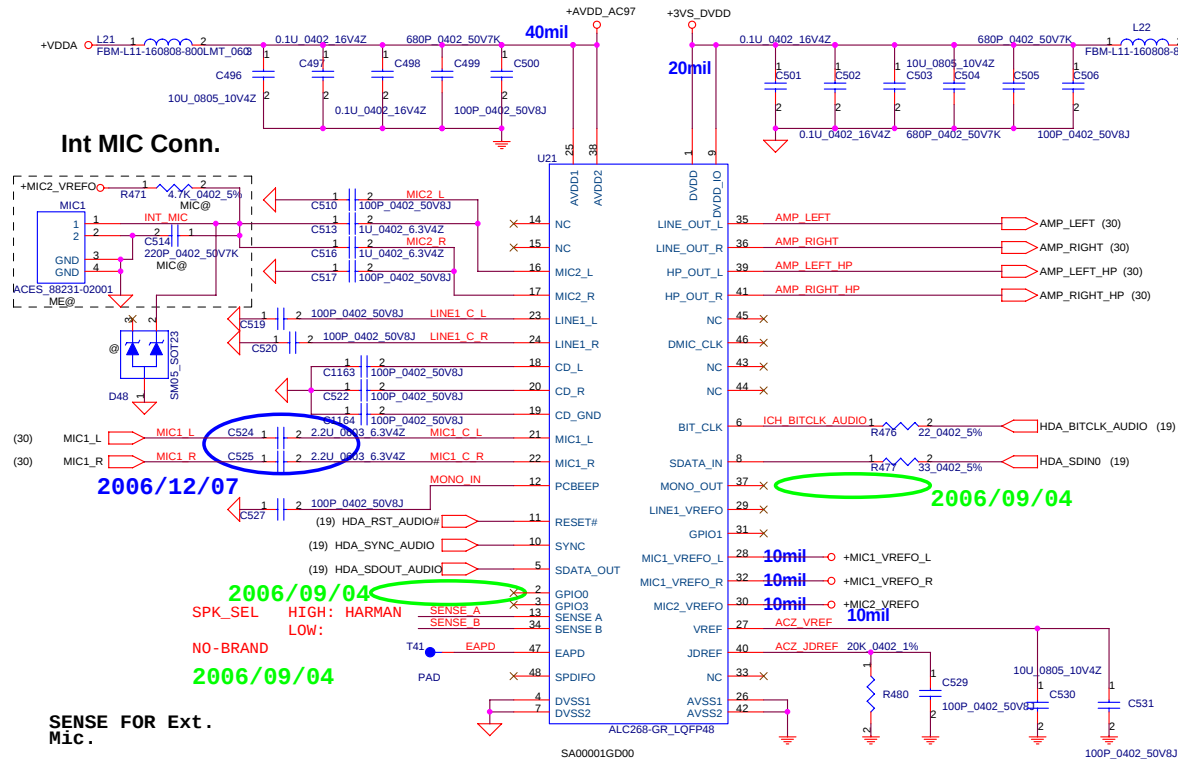


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	Mini Card / MDC CONN		
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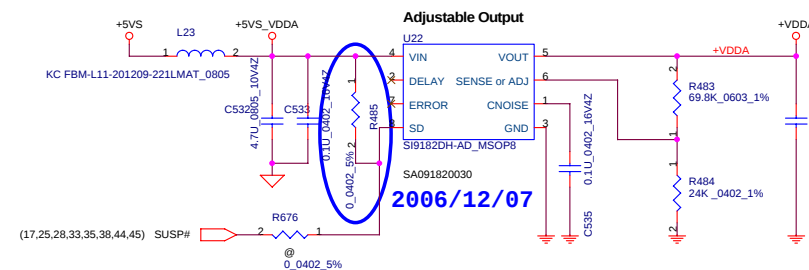
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title
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			PCMCIA ENE CB1410	0.2
			IGT10/11 LA-3591P	
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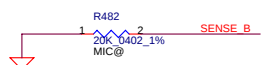


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

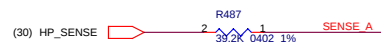
Regulator for CODEC



SENSE FOR Int. Mic.



SENSE FOR HP

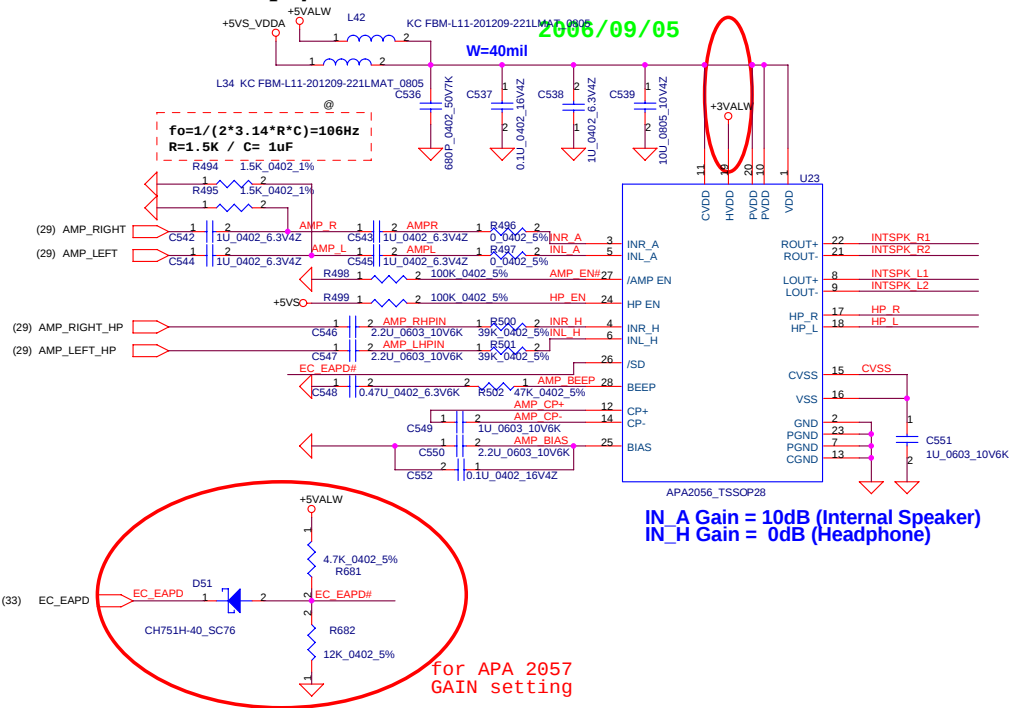


2006/09/04

2006/10/20

Security Classification	Compal Secret Data			Compal Electronics, Inc. ALC861 VD Codec Document Number IGT10/11 LA-3591P Rev 0.2		
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APA2056 SPK/HP Amplifier

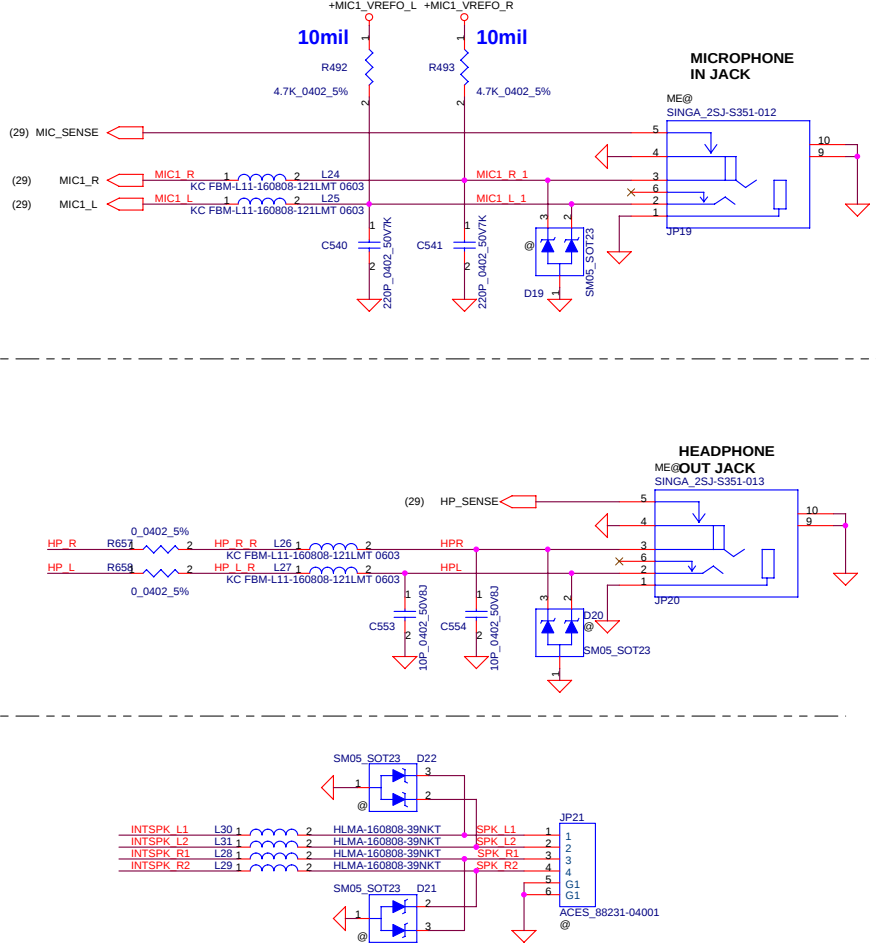


IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

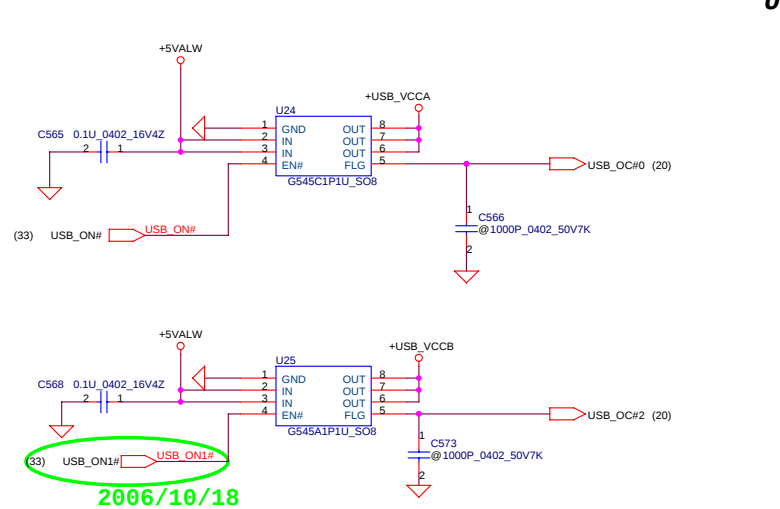
APA2057 gain setting table

gain	V	V(low)	V(high)
8		3.21	3.27
9		3.33	3.39
10		3.45	3.51

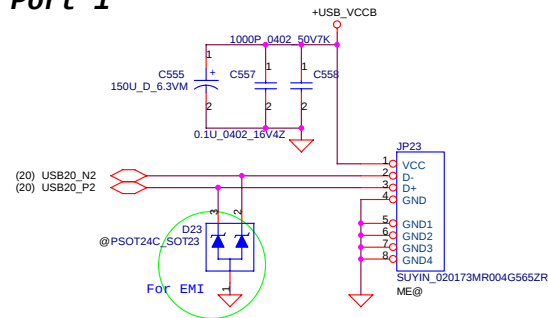
← current setting(3.48V)



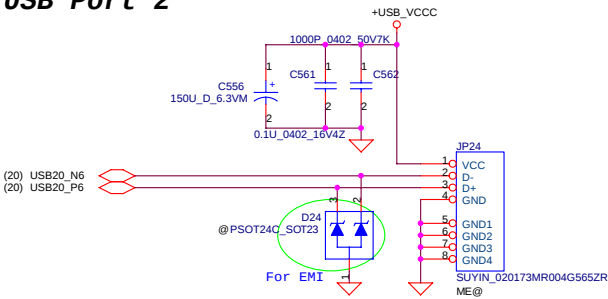
USB Port



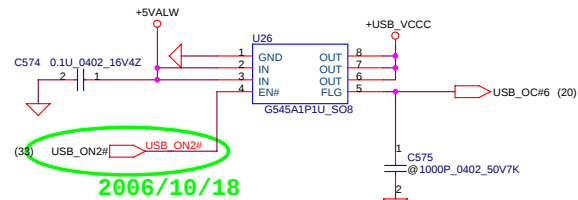
USB Port 1



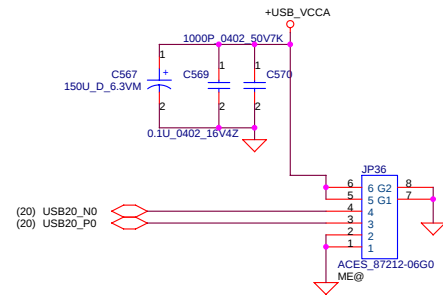
USB Port 2



USB Port 3

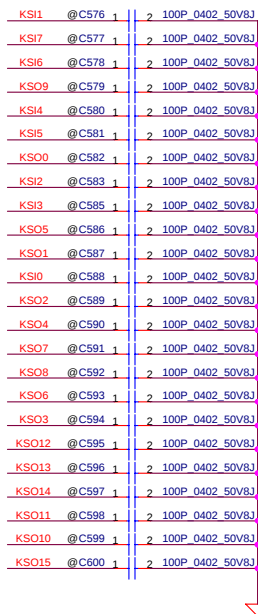
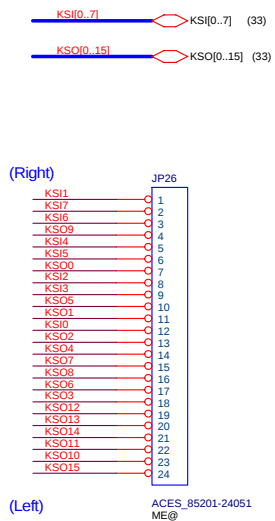


USB board

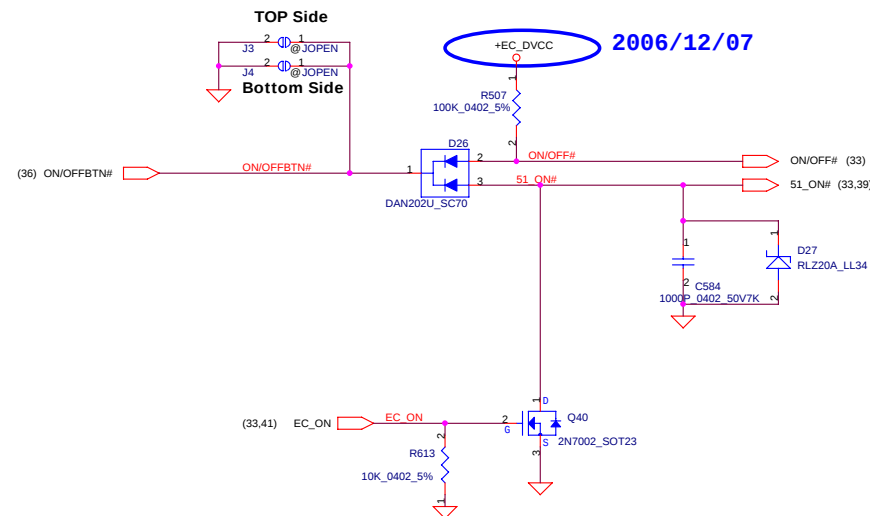


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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	Bluetooth & USB CONN.
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INT_KBD CONN



Power BTN



Security Classification	Compal Secret Data		Title	
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				Date: Tuesday, March 06, 2007
				Sheet 32 of 48

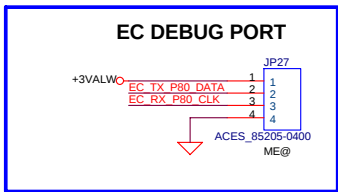
Compal Electronics, Inc.

KBD.ON/OFF,T/P,LED/B,DEBUG

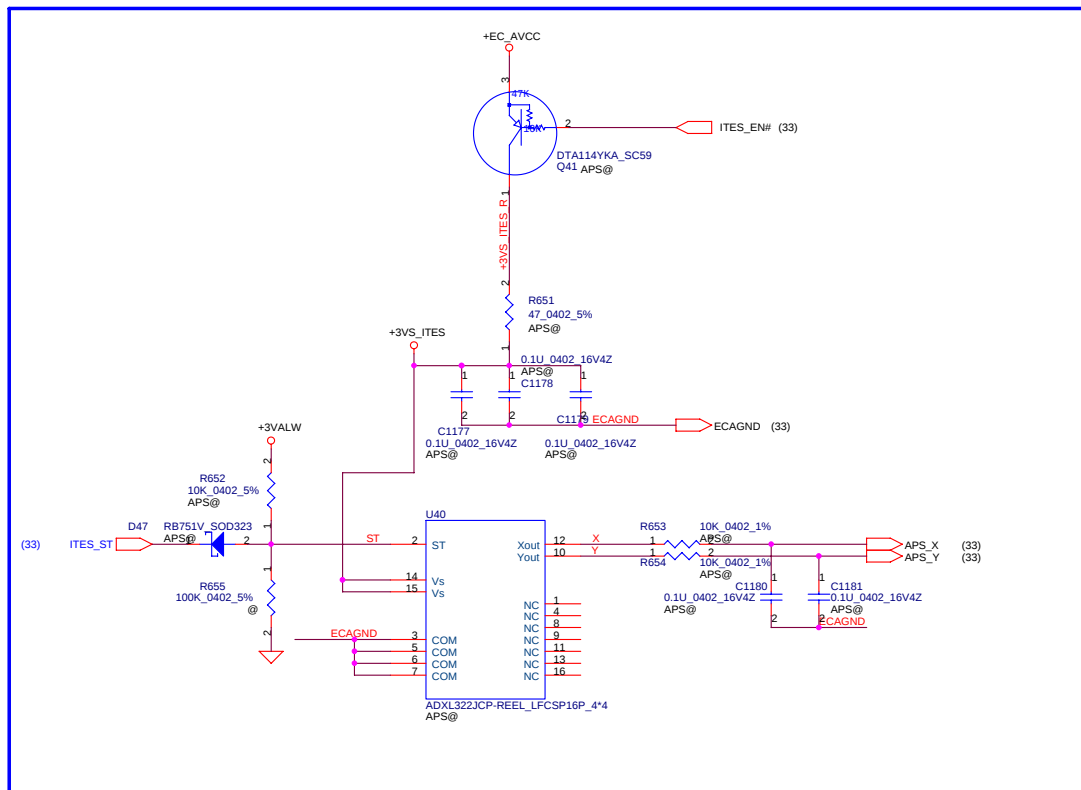
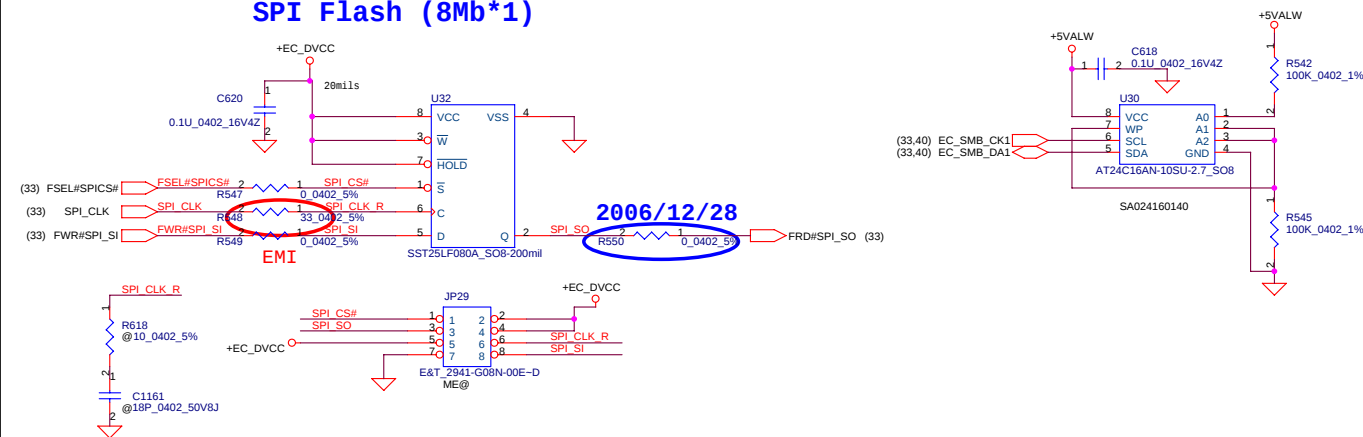
IGT10/11 LA-3591P

Date: Tuesday, March 06, 2007

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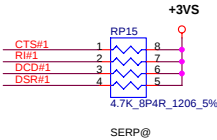
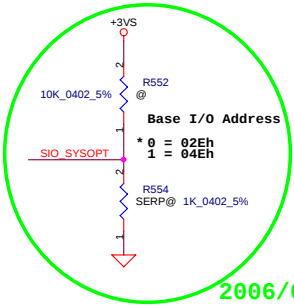
SPI Flash (8Mb*1)



2006/10/14
DEL ISA
BIOS

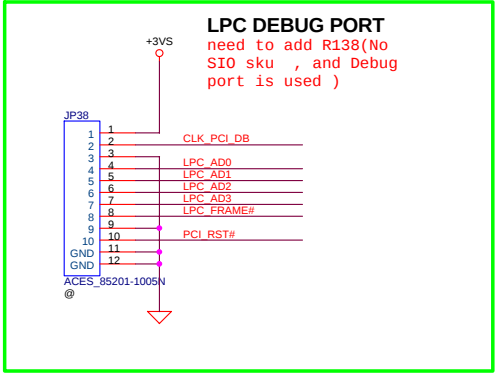
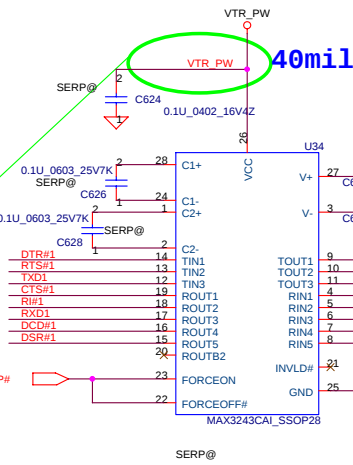
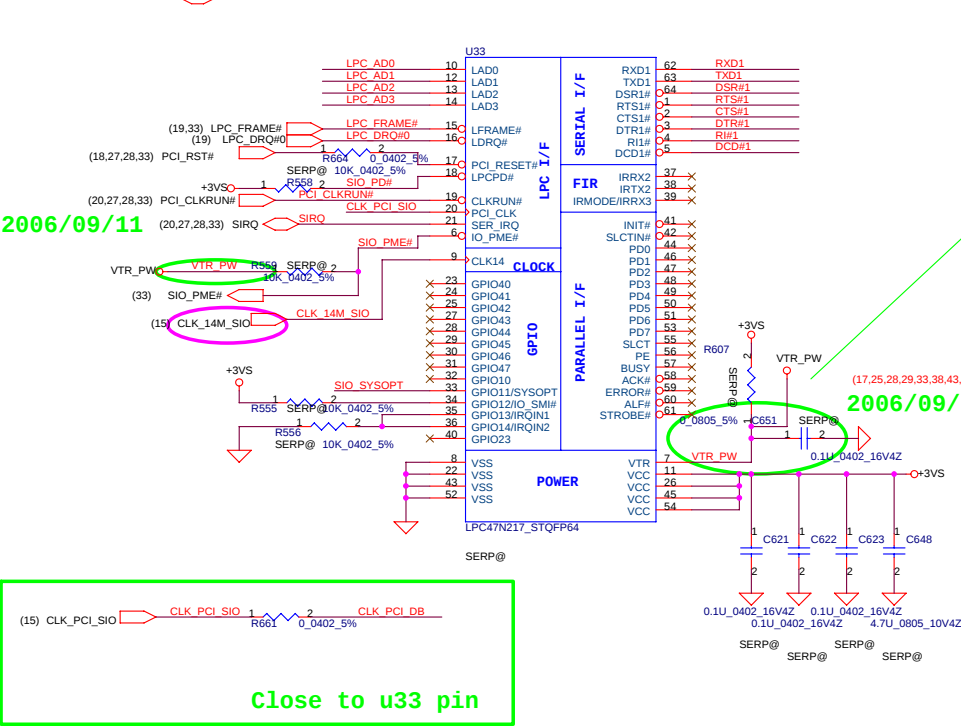
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	BIOS & APS	
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				Date: Tuesday, March 06, 2007	Sheet 34 of 48

SUPER I/O SMC LPC47N217



(19,33) LPC_AD[0..3] LPC_AD[0..3]

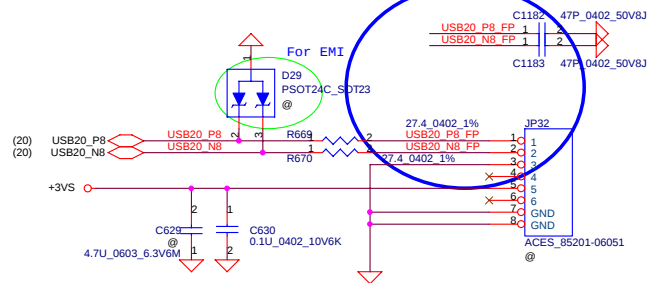
2006/09/11



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	RS232 Serial Port
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				Date	Tuesday, March 06, 2007
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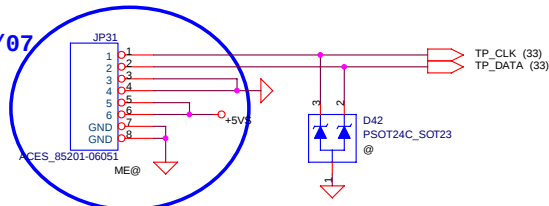
Finger Print

2006/12/22

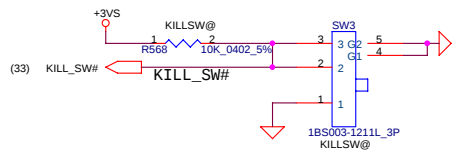


T/P Board

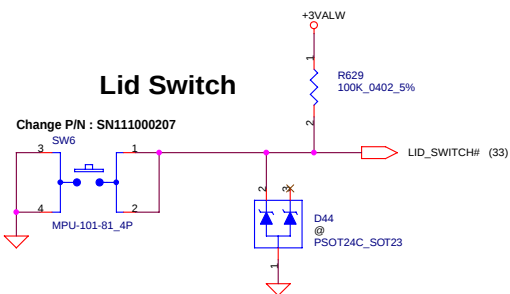
2006/12/07



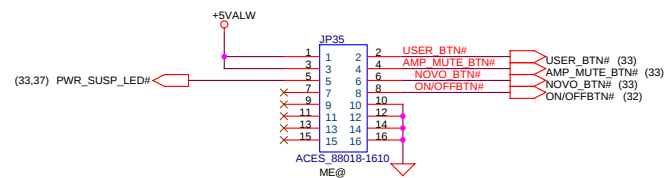
Kill Switch



LID Switch



SW Board



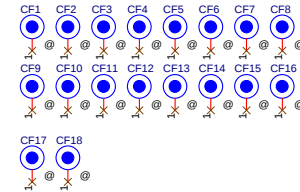
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Document Number
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Compal Electronics, Inc.

FP/SW/TP

IGT10/11 LA-3591P

+VCC_SD



Front LEDs

(26) WIRELESS_LED#

(26) BTONLED

(33) CHARGE_LED0#

(33) CHARGE_LED1#

(3,36) PWR_SUSP_LED#

R576 300_0402_5%

R577 300_0402_5%

R581 300_0402_5%

R582 300_0402_5%

R650 300_0402_5%

D33 HT-191UD_AMBER_0603

D41 HT-191NB_BLUE_0603

D45 HT-191UD_AMBER_0603

D46 HT-191NB_BLUE_0603

+5V5

+5VALW

SWAP BY EC

(33) NUM_LED# 1 2 R575 300_0402_5% D32 HT-191NB_BLUE_0603

(33) CAPS_LED# 1 2 R578 300_0402_5% D35 HT-191NB_BLUE_0603

(33) SCROLL_LED# 1 2 R579 300_0402_5% D36 HT-191NB_BLUE_0603

+5VS

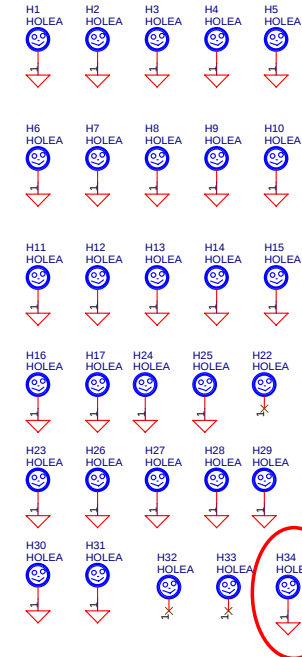
(25) ODD_LED# 1 ODD_LED# 1 U36 4 DRIVE_LED# 1 D39 HT-191NB_BLUE_0603

(19) SATA_LED# 2 SATA_LED# 2 U36 4 DRIVE_LED# 2

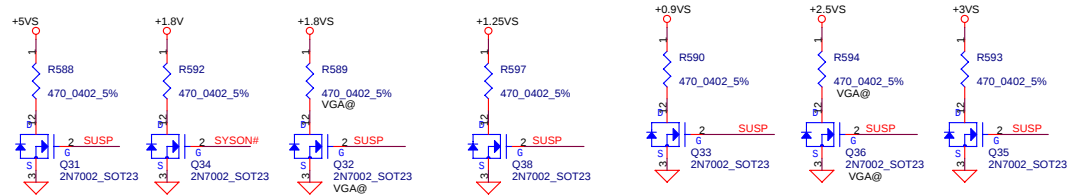
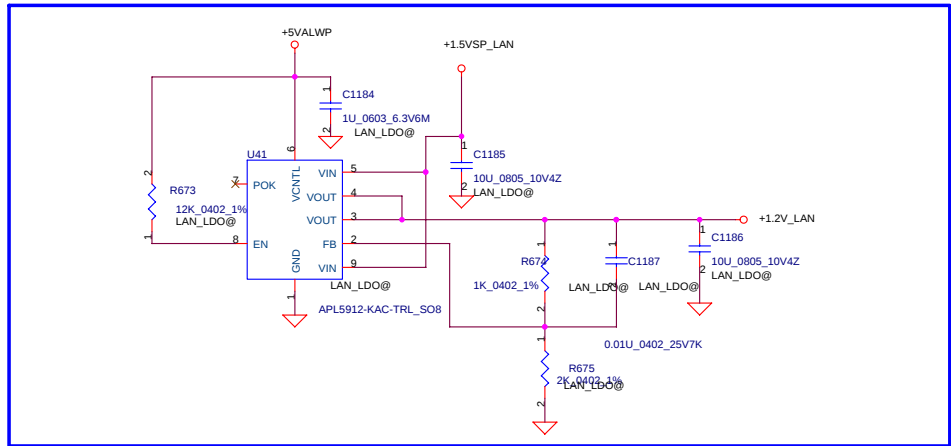
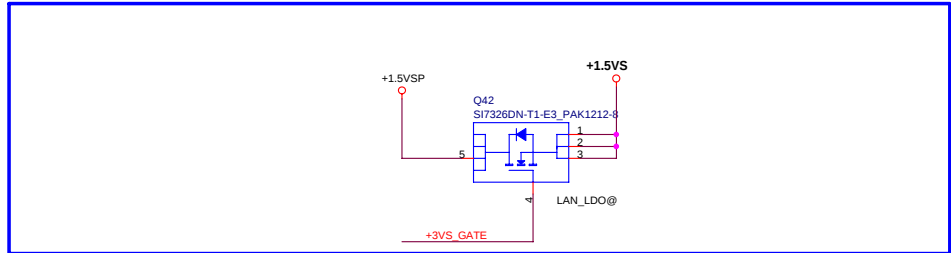
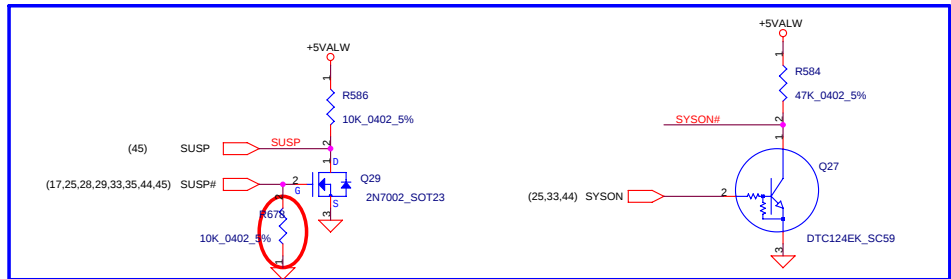
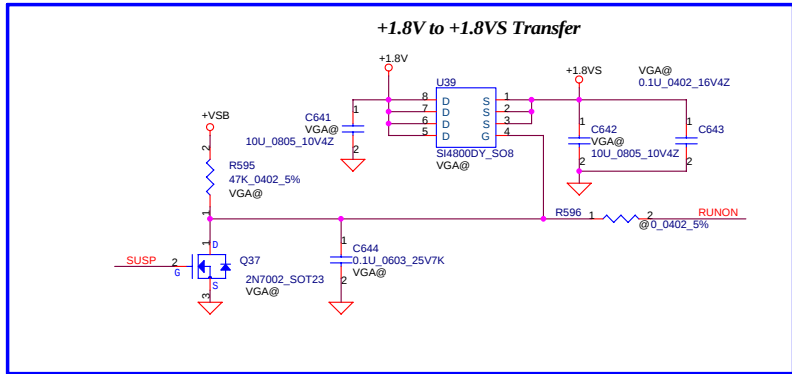
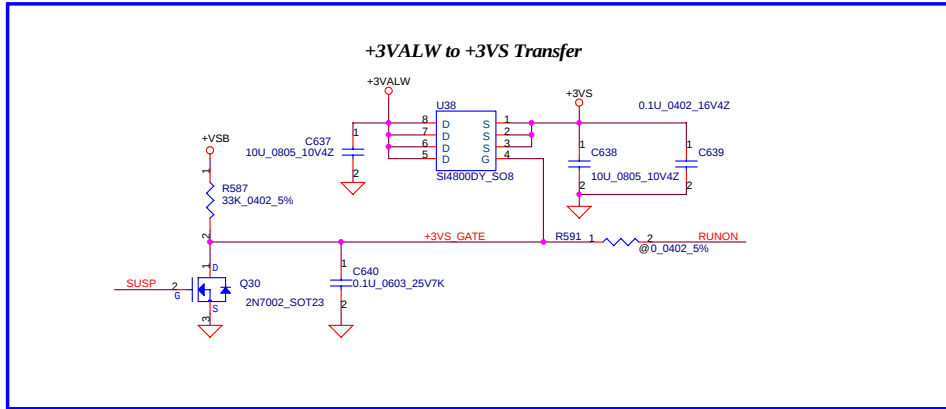
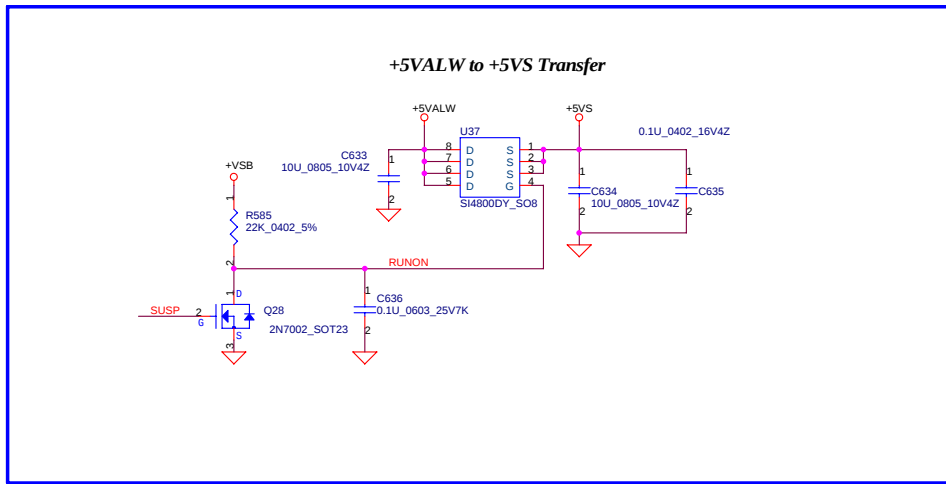
+5VS

R583 300_0402_5%

U36 TC7SH08FUF_SSOP5

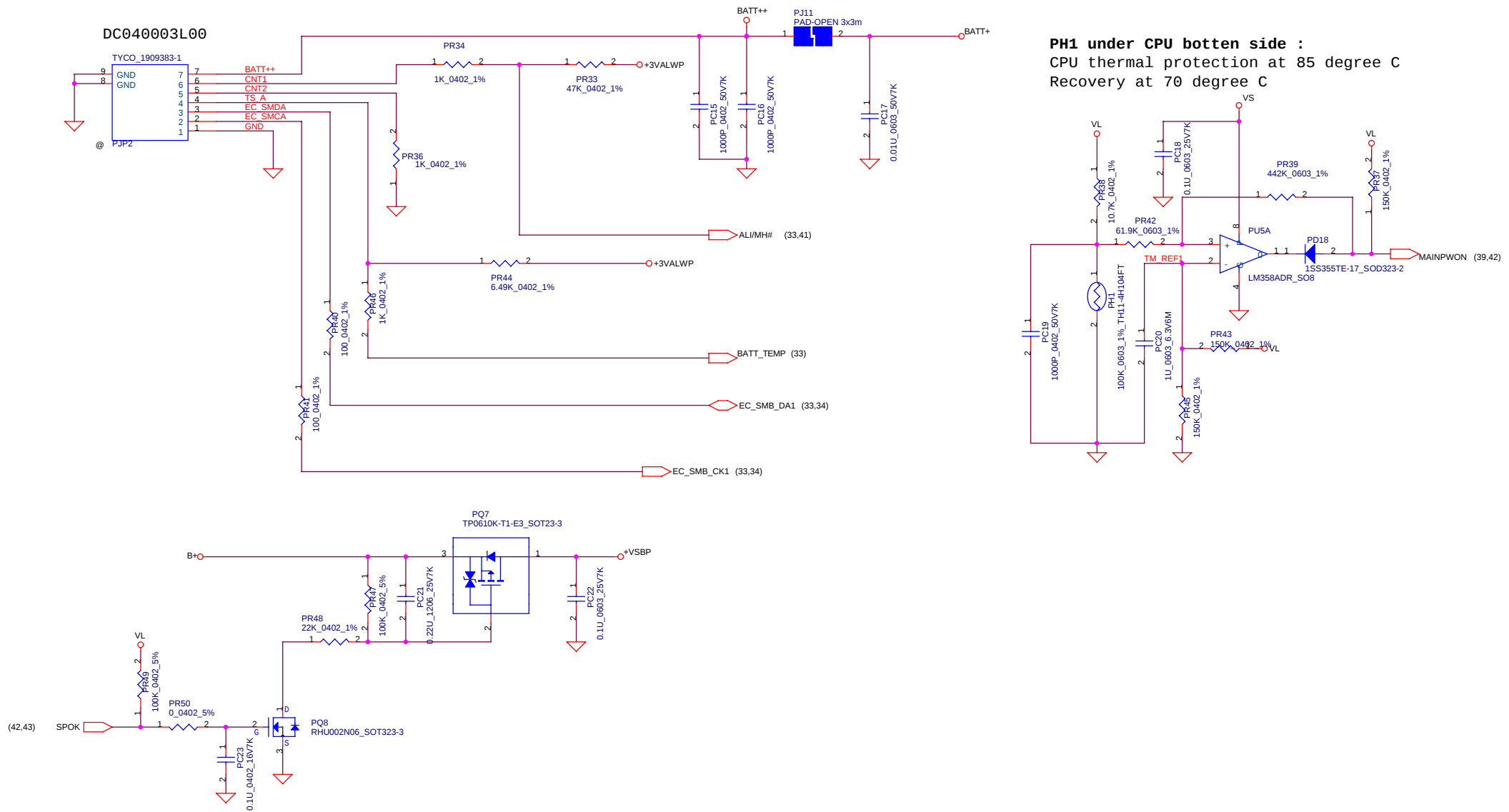


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				Document Number	
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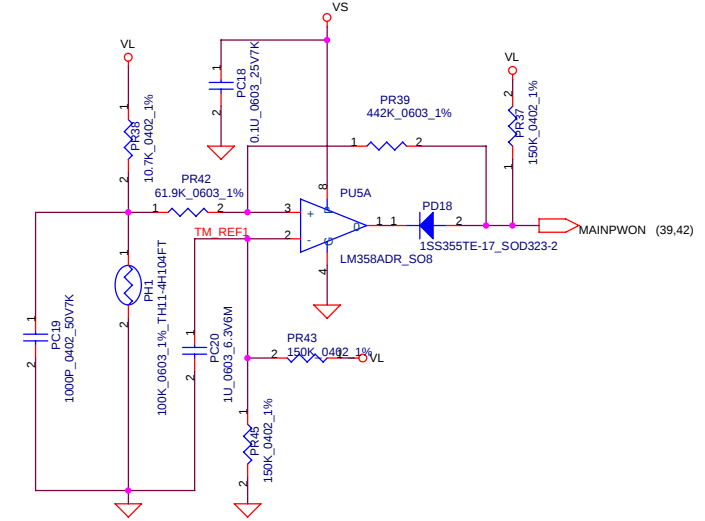


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OCP==>8A
Vripple=



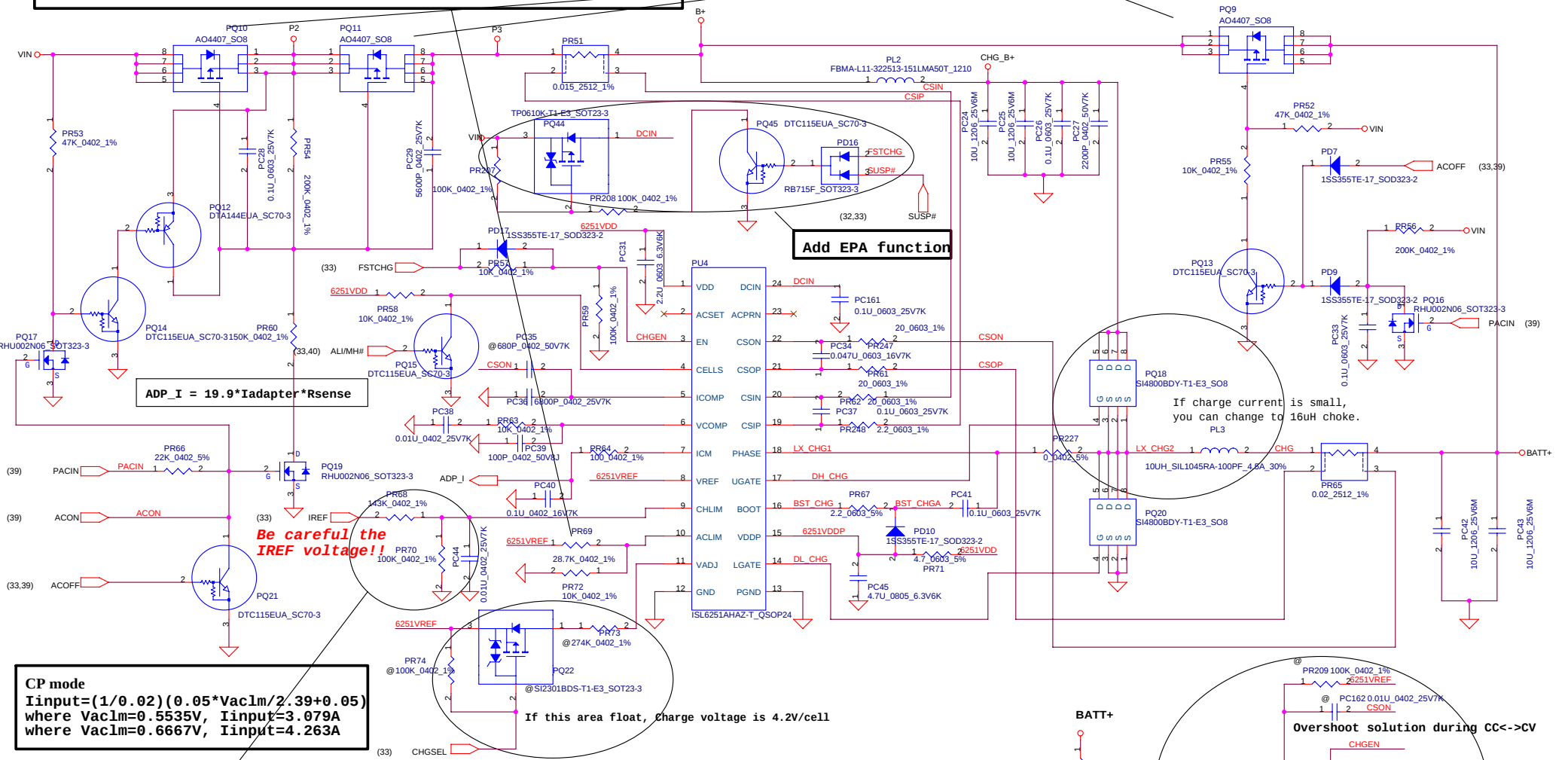
PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

65W PQ10, PQ11, PQ9->FDS4435



ADP_I = 19.9*Iadapter*Rsense

CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

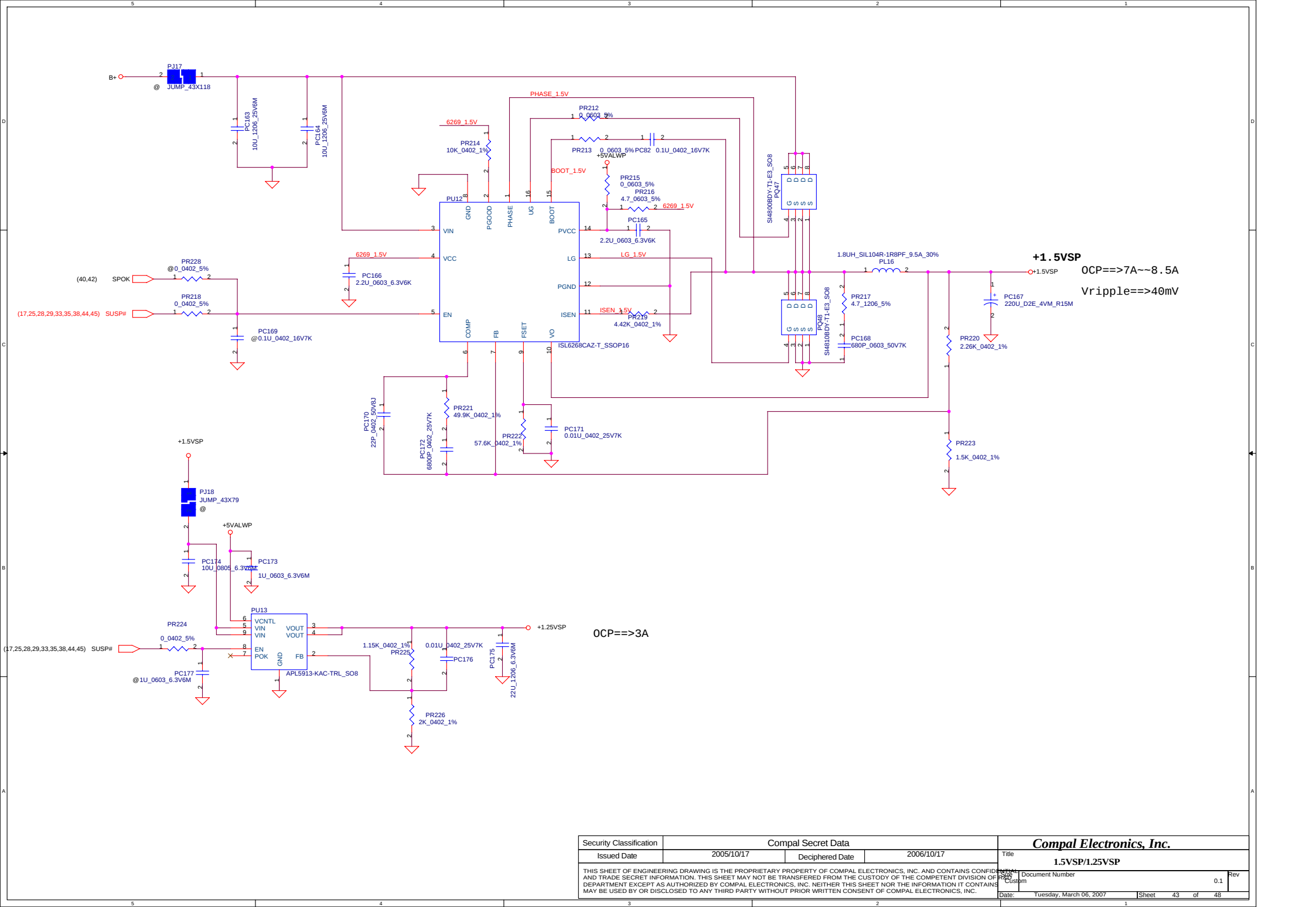
CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 * I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

Charge Voltage
 3S CC-CV MODE : 12.6V (CELLS=GND , ALI/MH#=3.3V)
 4S CC-CV MODE : 16.8V (CELLS=VDD , ALI/MH#=0V)

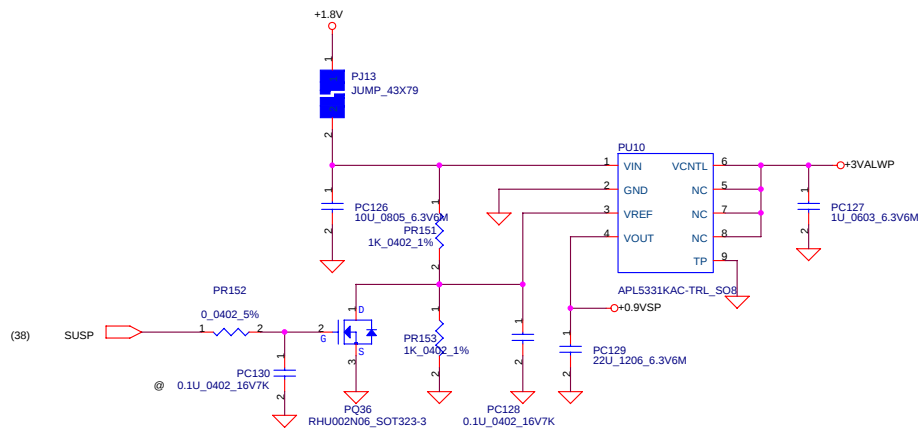
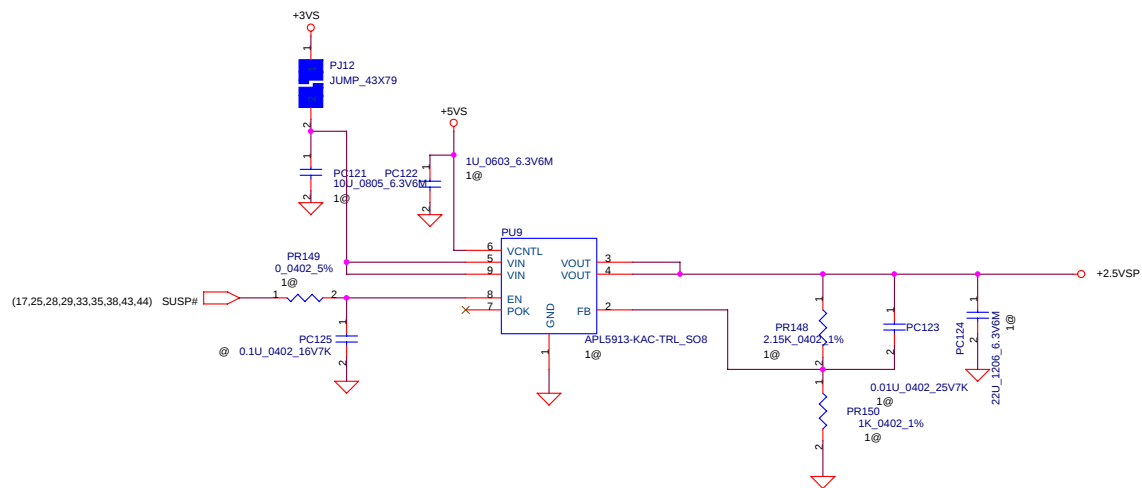
BATT Type	Charging Voltage (0x15)	ALI/MH#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+

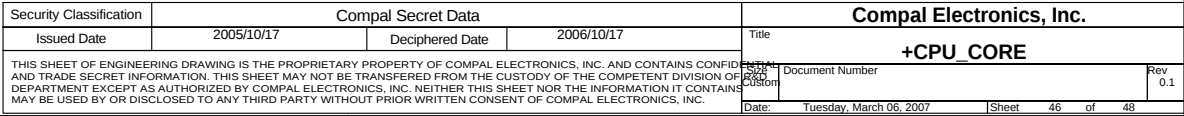
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				1.5VSP/1.25VSP	
				Document Number	
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	5	4	3	2	1
	page	Reason for change	Modify list		
EVT	P39,P42,P43,P44,P46	Shortage issue : needs to change another source	SM010018210 Replace		
	P46	Shortage issue : needs to change another source	Change SB578400080 to SB000008L80		
DVT	P39	1.Inrush decrease 2.Change to Standard part	1.Change PC1/PC4 from 0.01U to 1000P 2. PR1/PD1 no function,Change PD5 from RB751V to RL4148;Add PC6		
	P40	1.LM358A replace of LM393 2.Add Diode to anti reverse voltage 3.Modify component size	1.PU5A replace of PU3A 2.Add PD18 close to PU5A 3.Change PC15/PC16 from 0603 to 0402		
	P41	1.Add BATT-OVP function 2.Overshoot solution during CC->CV 3.Change torlance 4.Change to Standard part 5. Add PR227 to anti reverse voltage 6. 65W change to Standard part 7.Add EPA Function	1.Change PR78 value from 150K to 105K 2-1.Add PR209 ,PC162 ,PR210 ,PQ44 ,PC161 ,PQ45 ;Del PQ46/PC30 2-2.Del PD8 ; Add PD17 3. Cange torlance from 0 ohm 5% to 10Kohm 1% at PR57 4. PD10: Change CH751H to 1SS355TE ; original PU5B to PU5A; Del PC46;Change PQ20 from SI4810 to SI4800 5. PR227 : currently use 0ohm. (In the future use 2.2ohm) 6. Change PQ9/P10/PQ11 to FDS4435; Change PR69 to 39.2K 7.Add PD16/PR57/PR208/PR207/PC161		
	P42	1.Change 5V/3.3V in SKIP mode 2.Change to Standard part 3.For EPA function	1.Add PR211 (@ PR94) 2-1.Change PC62/PC63 from SGA20151360 to SF22001M300 2-2. Change PC49/PC50 from 0603_25V7K to 0402_16V7K 2-3. Change PL5/PL6 from 4.7UH to 10UH 3.Change PR95 from 6.81K to 6.49K		
	P43	Update 1.5VSP/1.25VSP to Standard part	1-1.Reduce capacitor value from 22u_1206_6.3V6M to 10u_0805_6.3VM at PC174 1-2.Change from dual PWM IC to single PWM IC for 1.5VSP (PU12), Del PU7,PC69,PC71,PC72,,PC74,PC75,PC76,PC77,PC78,PC79,PC80,PC81,PC82,PC83,PC84, PC85,PC86,PC87,PC88,PC90,PC91, PC93,PC94,PD12,PD13,PL7,PL8,PL9,PQ27,PQ28,PQ29,PQ30, PR100,PR102,PR103,PR104,PR105,PR106,PR107,PR108,PR109,PR110,PR111,PR112,PR113,PR114 ,PR115,PR116,PR117,PR118,PR119,PR120,PR121,PR122,PR123 Add Part:PC82,PC163,PC164,PC165,PC166,PC167,PC168,PC169PC170,PC171,PC172,PC173,PC174, PC175,PC176,PC177,PJ17,PJ18,PL16,PQ47,PQ48,PR212,PR213,PR214,PR215,PR216,PR217,PR218, PR219,PR220,PR221PR222,PR223,PR224,PR225,PR226,PR228 1-3.APL5913(PU13) replace of APL5912		
	P44	Update 1.05VSP/1.8VP to Standard part	1-1.Change PC107/PC110/PC100 size from 0603 to 0402 1-2.Change PD14/PD15 from RB751 to 1SS355TE 1-3.Change PC158 size from R9M to R15M;Change PC98 from NEC to Panasonic 1-4.Add PC113		
	P45	Update 2.5VSP/0.9VSP to Standard part	1-1.Change PC121 capacitor from 22u_1206_6.3V6M to (@ 10U_0805_6.3VM) 1-2. APL5913 replace of APL5912 at PU9 1-3.Change PC126 capacitor from 22u_1206_6.3V6M to 10U_0805_6.3VM 1-4. Add PR149 1-5.UMA part : Del total 2.5VSP circuit->PU9/PC122/PC121/PR148/PR150/PC123/PC124/PR149		
	P46	Update +CPU_CORE to Standard part	1-1.Change PC132/PC133/PC134/PC150/PC151/PC152 size from 10u_1206_25VAK to 10u_1206_25V6M 1-2.Change PQ38/PQ39/PQ41/PQ42 from 8113 to SI4856 1-3.Change PR158/PR194 from 0ohm to 2.2ohm 1-4.Change PC137 to 3000hrs		

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<Title>			
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Custom	<Doc>		<RevCode>
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B-TEST

page	Reason for change	Modify list
P22	DFX ISSUE	ADD RP49- RP52
P26	LED control by EC	ADD R672
P30	Reduce "bo" sound when enter sleep mode	ADD L42
P35	DFX ISSUE	Del SIO debug port
P36	F/P DFX	ADD C1182 C1183 R669 R670

C-TEST

page	Reason for change	Modify list
P10	fixed tv out ripple	ADD L43 C1190
P35	fixed COM PORT function	re connect 14M & mirror jp30 connection
P38	fixed 1st ac plug in then led flash	SUSP# pull low 10k (add r678)