

Compal Confidential

QIWY4 M/B Schematics Document

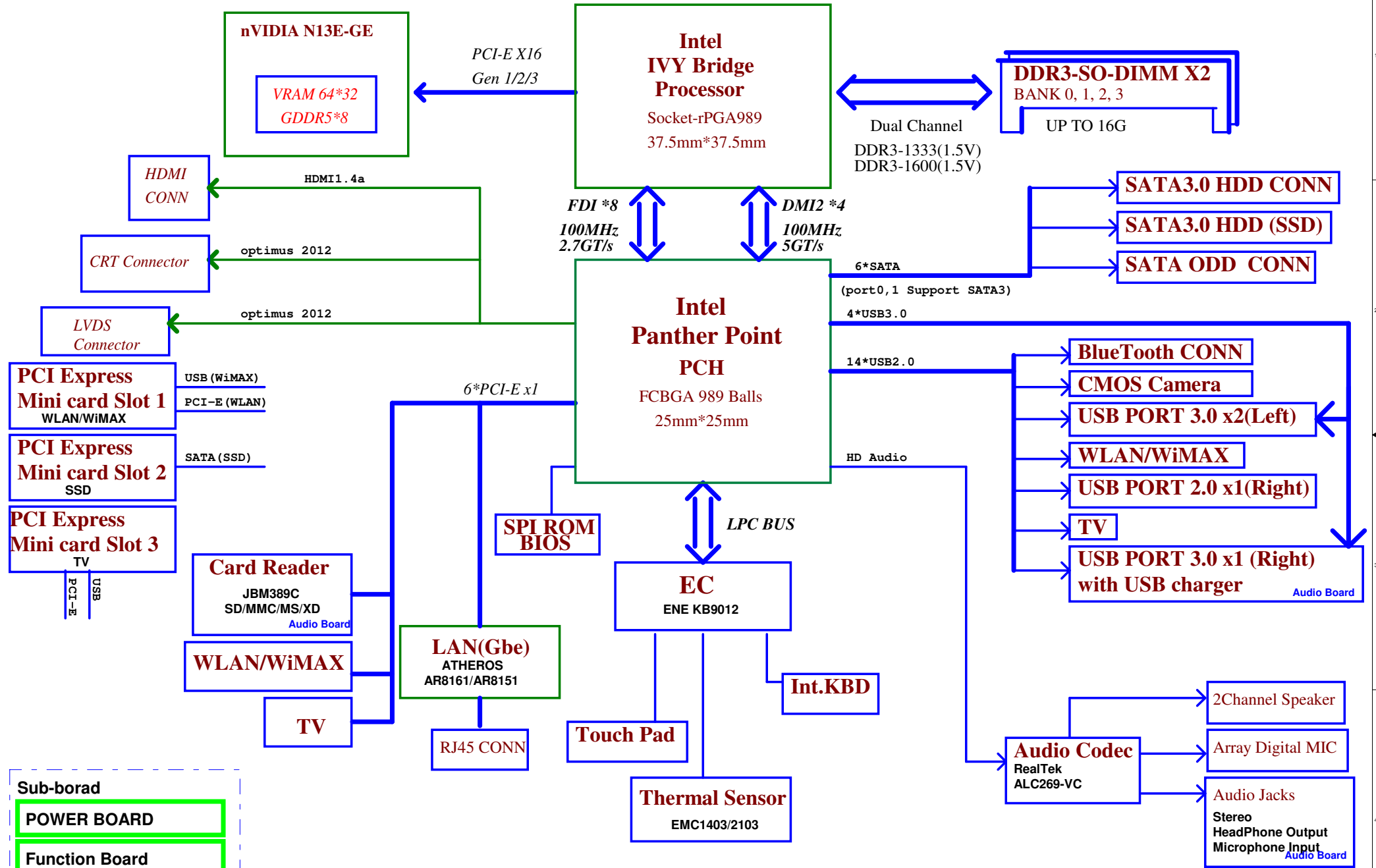
Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13X

2011-12-23

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Cover Page		
				Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0	Sheet 1 of 64			

Chief River



Sub-board

- POWER BOARD
- Function Board
- Audio Board

Security Classification	Compal Secret Data			Title		
Issued Date	2010/11/30	Deciphered Date	2011/12	Compal Electronics, Inc.		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				MB Block Diagram		
Size	Document Number	Rev	Date: Monday, January 16, 2012 Sheet 2 of 64			
Custom		1.0				

Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+VCCSA
S0	○	○	○	+V1.5S_VCCP
				+CPU_CORE
S3	○	○	○	+VGA_CORE
				+GFX_CORE
S5 S4/AC	○	○	X	+1.8VS
				+1.05VS
S5 S4/ Battery only	○	X	X	+0.75VS
				+3.3VS_VGA
S5 S4/AC & Battery don't exist	X	X	X	+1.5VS_VGA
				+1.05VS_VGA

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Board ID	Vcc	Ra/Rc/Re	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Project	EVT
0	3.3V +/- 5%	10K +/- 5%	0	0 V	0 V	0 V	QIWI3	EVT
1	8.2K +/- 5%			0.216 V	0.250 V	0.289 V	QIWI3	DVT
2	18K +/- 5%			0.436 V	0.503 V	0.538 V	QIWI3	PVT
3	33K +/- 5%			0.712 V	0.819 V	0.875 V	QIWI3	MP
4	56K +/- 5%			1.036 V	1.185 V	1.264 V	QIWI4	EVT
5	100K +/- 5%			1.453 V	1.650 V	1.759 V	QIWI4	DVT
6	200K +/- 5%			1.935 V	2.200 V	2.341 V	QIWI4	PVT
7	NC			2.500 V	3.300 V	3.300 V	QIWI4	MP

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
	KHCI	1	0 USB Port (Right Side)
		2	1
EHCI1		3	2 USB Port (Left Side)
		4	3 USB Port (Left Side)
		4	
		5	Camera
		6	
		7	
		8	
EHCI2		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	Mini Card(TV)
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
HDMI@	HDMI part
TV@	TV module part
CHG@	USB charger part
NOCHG@	No USB charger part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
S1G@	X76 P/N for Samsun VRAM 1G
S2G@	X76 P/N for Samsun VRAM 2G
H1G@	X76 P/N for Hynix VRAM 1G
H2G@	X76 P/N for Hynix VRAM 2G
GL@	N13P-GL part
GT@	N13P-GT part
GE@	N13E-GE part
GTGE@	N13P-GT&N13E-GE common part
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
1403@	EMC1403 thermal part
2103@	EMC2103 thermal part
KBL@	K/B Light part
ME@	ME part
@	Unpop

PCI-E PORT LIST

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

EC SM Bus address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

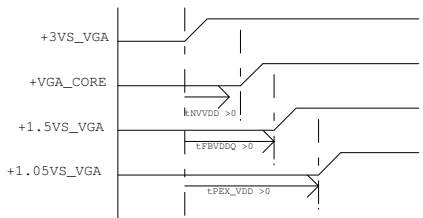
PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

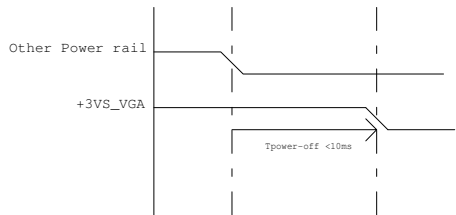


VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GC6 event
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB
N13E-GE (28nm)	0x0FDB
N13P-GL1 (40nm)	0x0DE9

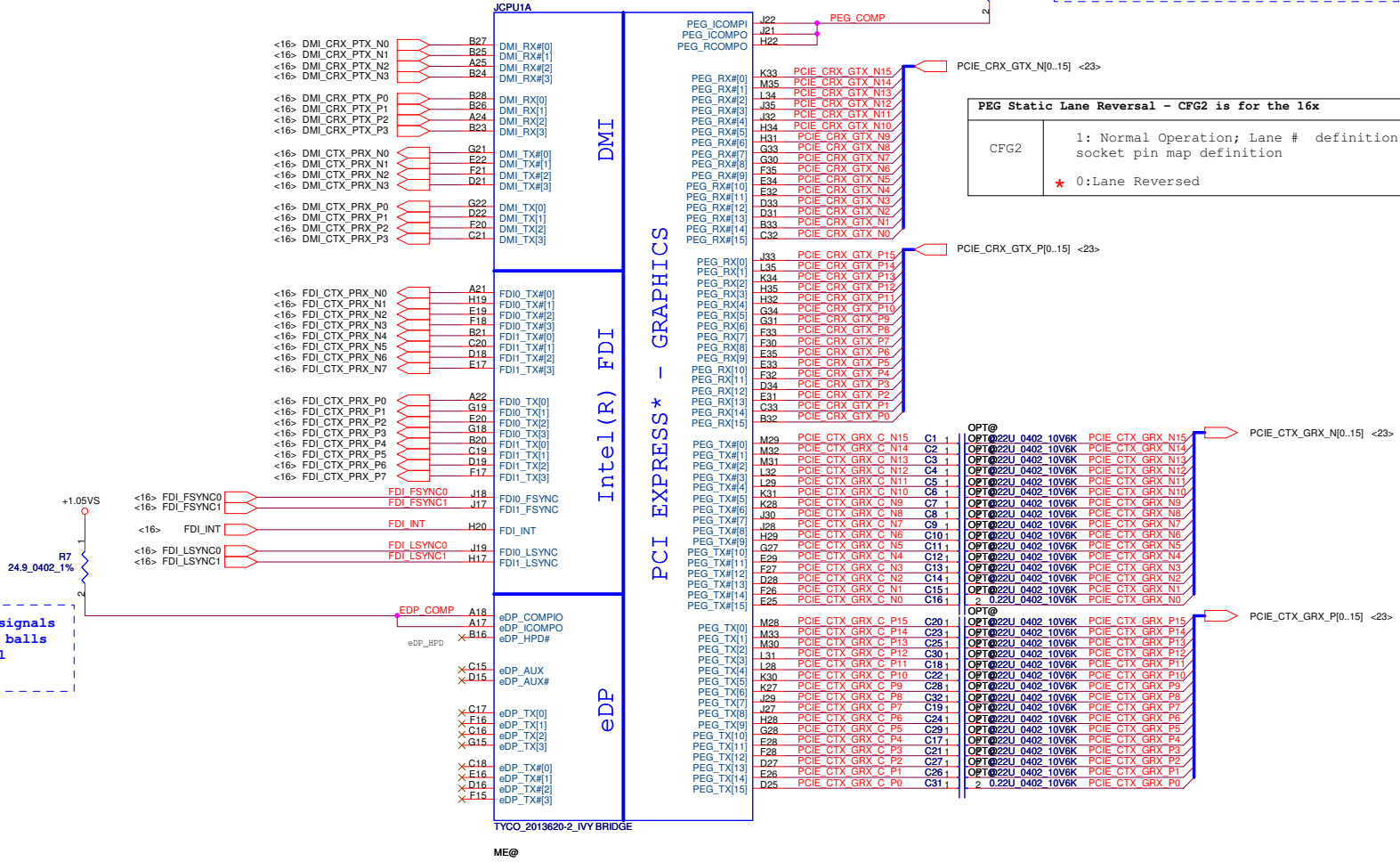
GPU	ROM_SO	ROM_SCLK	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
N13P-GT	PU 10K	PU 5K	PD 45K	PD 5K	PD 10K	PD 35K	PU 45K
N13E-GE	PU 10K	PU 5K	PD 45K	PD 5K	PD 25K	PD 35K	PU 45K
N13P-GL	PD 10K	PD 15K	NC	NC	PU 10K	PD 45K	PU 45K

GPU	N13P-GT	N13E-GE	N13P-GL
FB Memory (GDDR5)	ROM_SI	ROM_SI	ROM_SI
Samsung 2500MHz	K4G10325FG-HC04		
	32Mx32	PD 45K	PD 45K
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	PD 35K
Samsung 2500MHz	K4G20325FG-HC04		
	64Mx32	PD 30K	PD 30K
Hynix 2500MHz	H5GQ2H24MFR-T2C		
	64Mx32	PD 25K	PD 25K

Security Classification	Compal Secret Data		Title Compal Electronics, Inc. VGA Notes List
Issued Date	2011/07/21	Deciphered Date	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Document Number QIWY4 LA-8002P Rev 1.0
Date:	Monday, January 16, 2012	Sheet	4 of 64

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



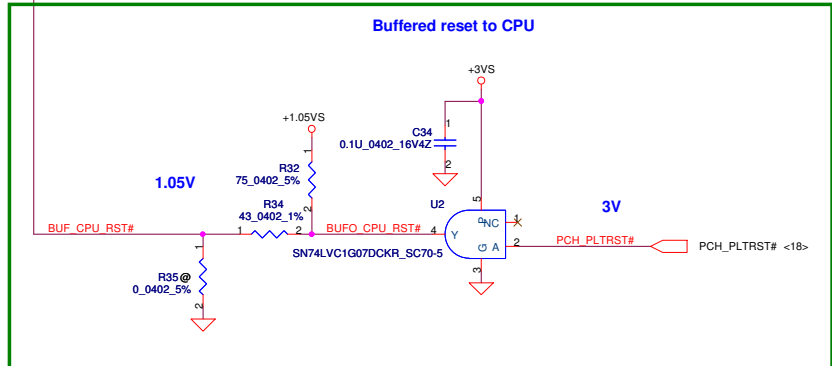
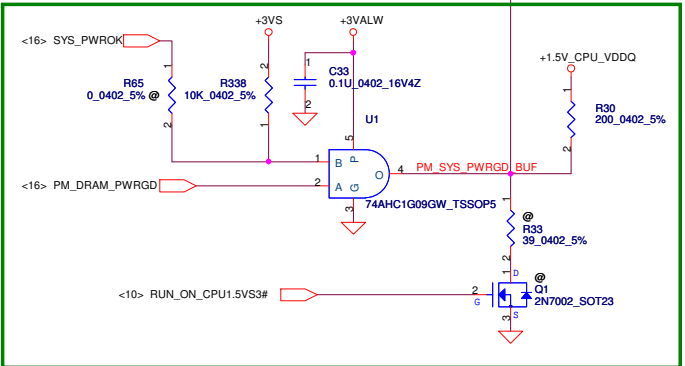
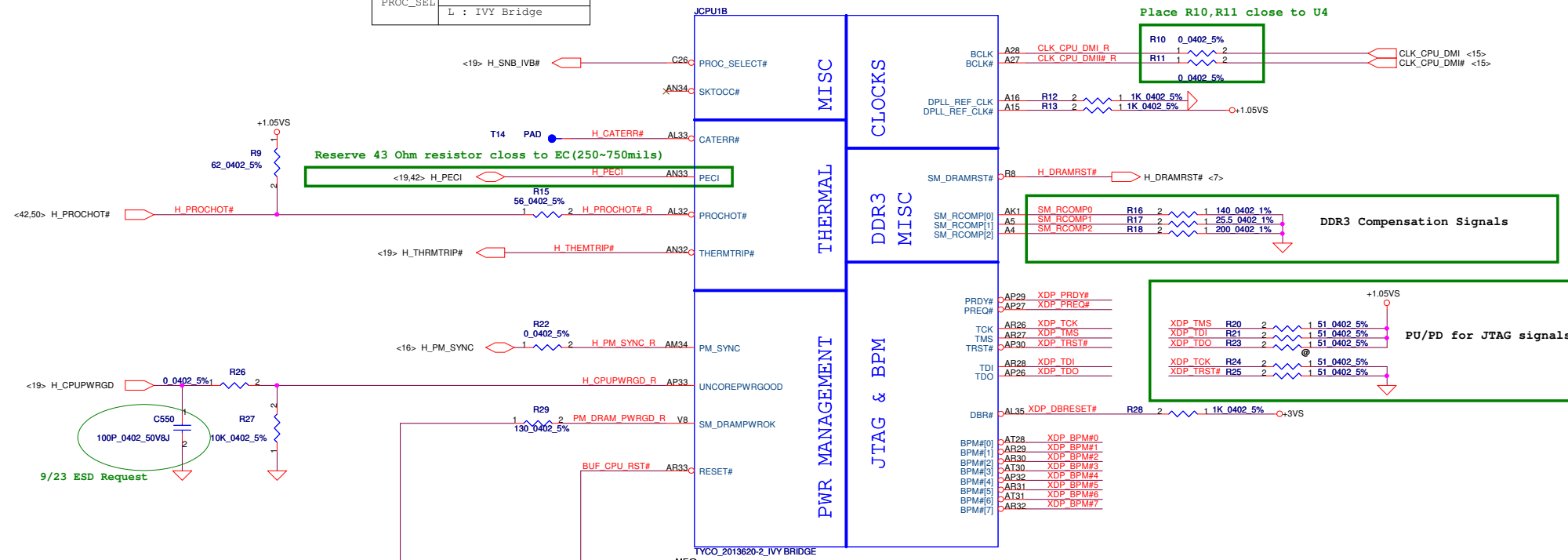
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	Definition
1	Normal Operation; Lane # definition matches socket pin map definition
* 0	Lane Reversed

Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date
		2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

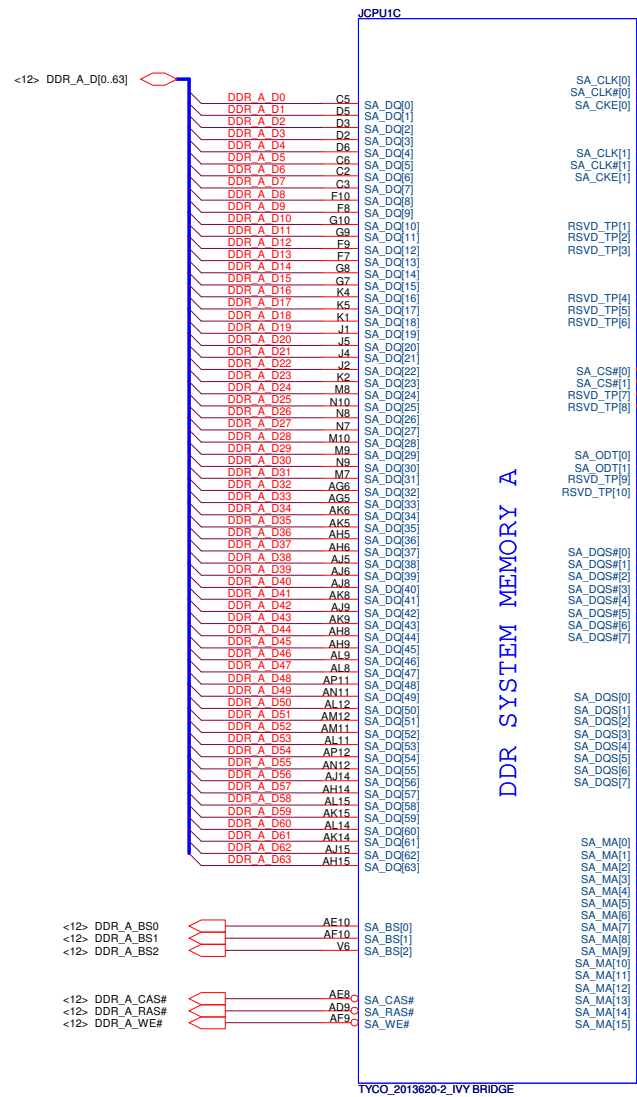
Compal Electronics, Inc.		
Title PROCESSOR(I7) DMI,FDI,PEG		
Size	Document Number	Rev
Custom	QIYW4 LA-8002P	1.0
Date:	Monday, January 16, 2012	Sheet 5 of 64

PROC_SEL	H : Sandy Bridge
	L : IVY Bridge

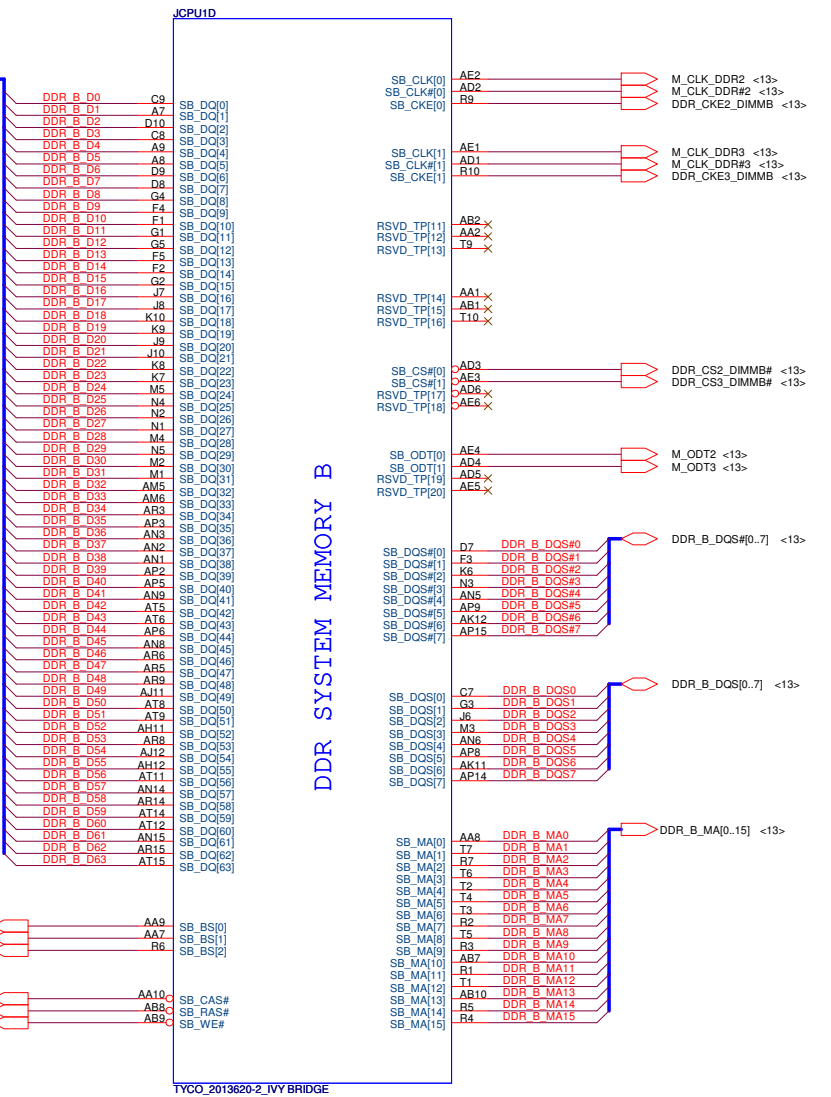


Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date
		2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

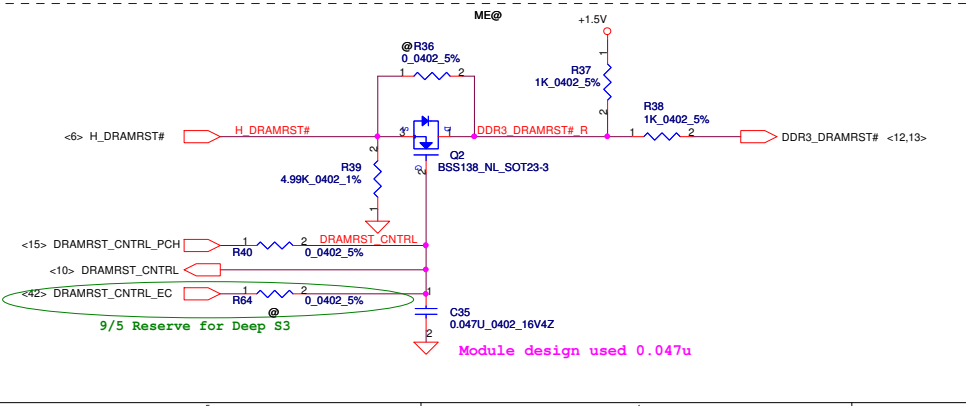
Compal Electronics, Inc.		
PROCESSOR(2/7) PM,XDP,CLK		
Size	Document Number	Rev
Custom	QIWy4 LA-8002P	1.0
Date:	Monday, January 16, 2012	Sheet 6 of 64



DDR SYSTEM MEMORY A



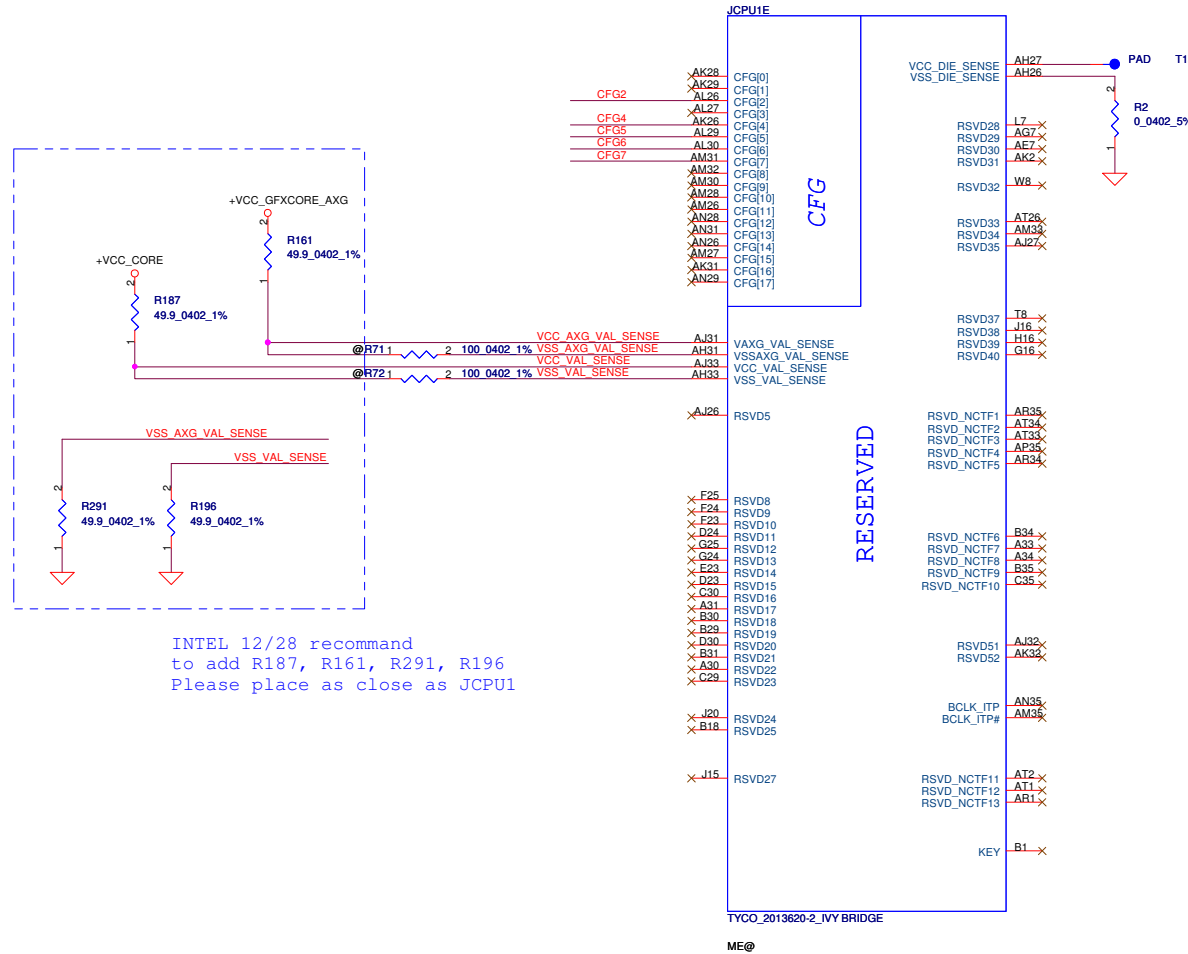
DDR SYSTEM MEMORY B



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	PROCESSOR(3/7) DDRIII
Customer		Customer		Size	Document Number
					QIYW4 LA-8002P
Date:	Monday, January 16, 2012	Sheet	7	Rev	1.0
					of 64

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

CFG Straps for Processor

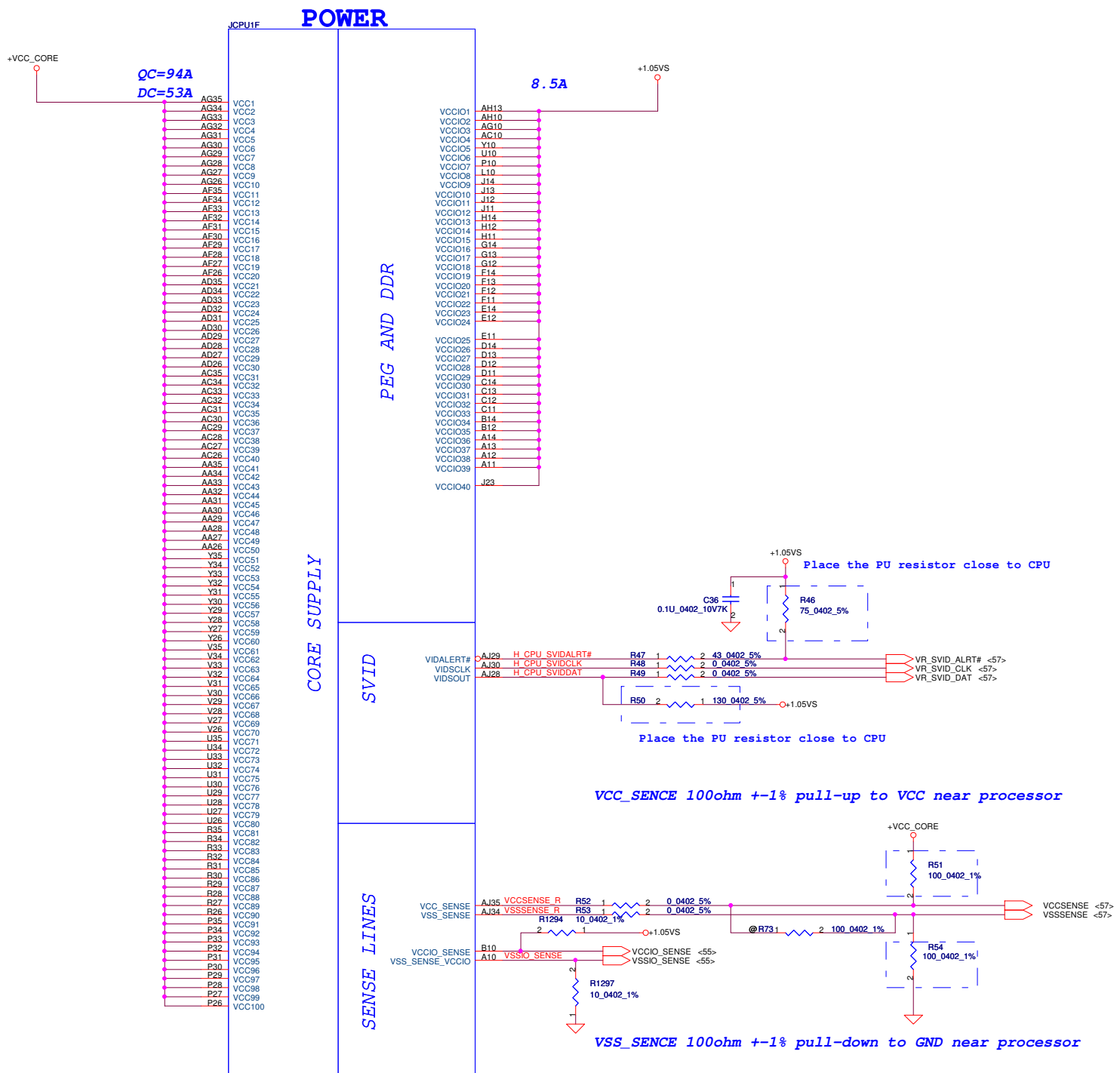


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

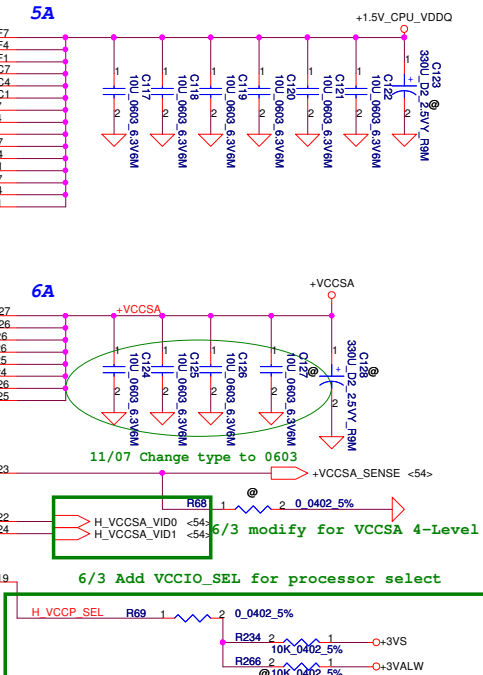
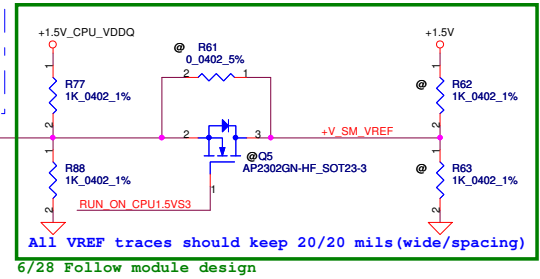
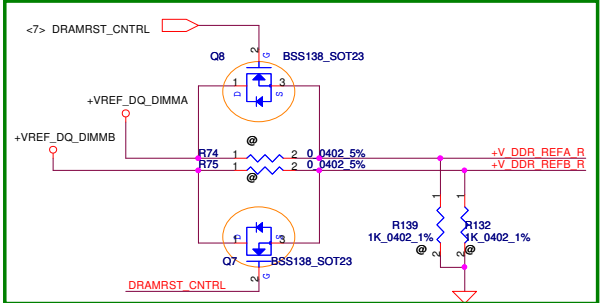
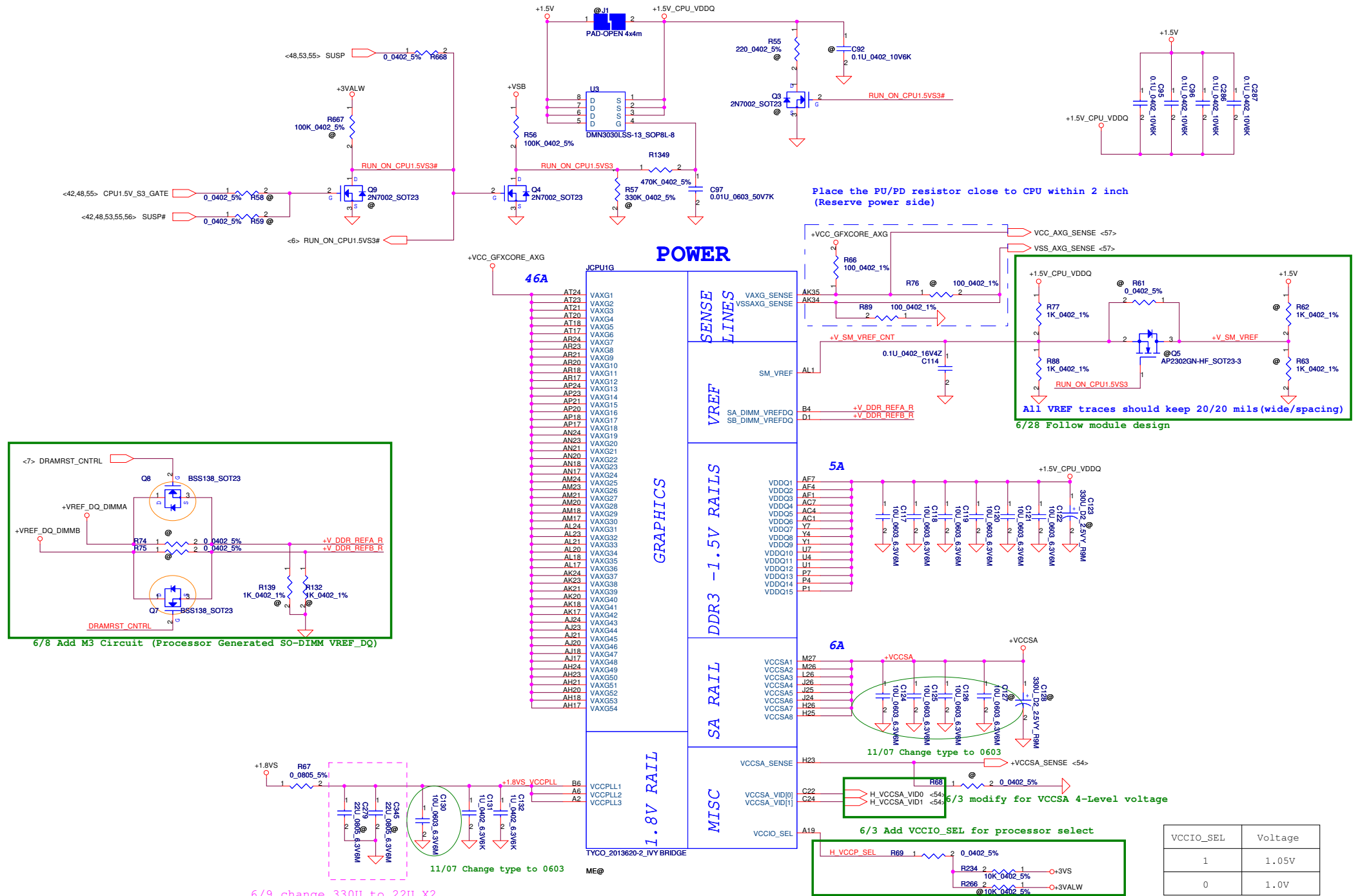
PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

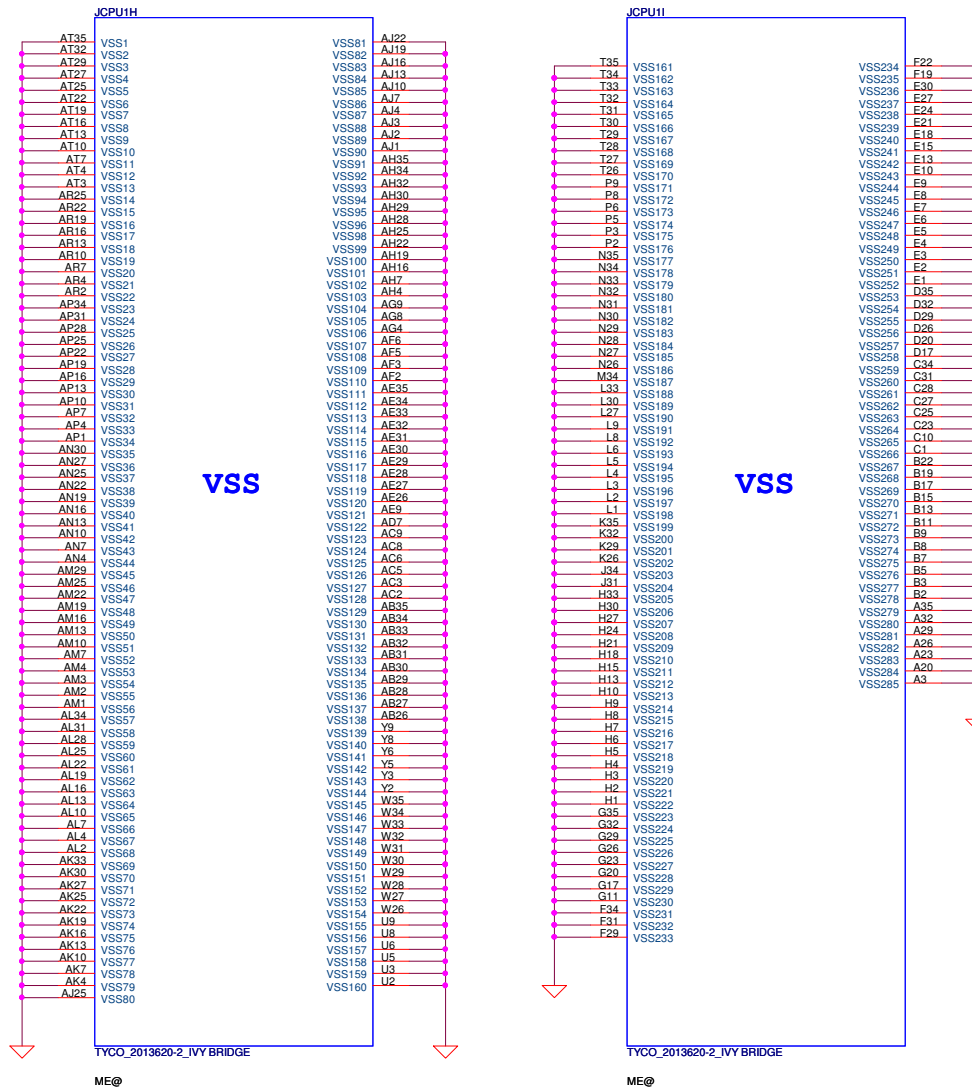


TYCO_2013620-2_VX BRIDGE	Security Classification	Compal Secret Data		Compal Electronics, Inc.	
ME@	Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title
					PROCESSOR(5/7) PWR,BYPASS
					Size: Custom
					Document Number: QIWIY4 LA-8002P
					Rev: 1.0
					Date: Monday, January 16, 2012 Sheet 9 of 64

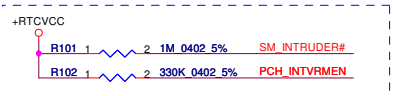
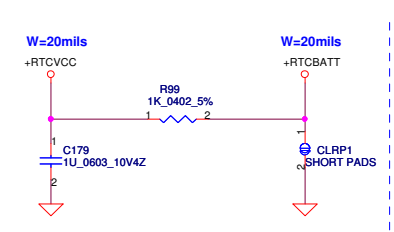
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



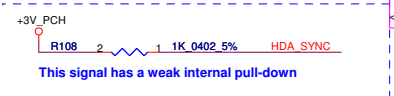
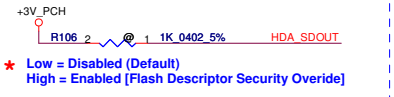
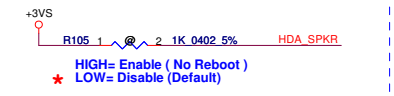
VCCIO_SEL	Voltage
1	1.05V
0	1.0V



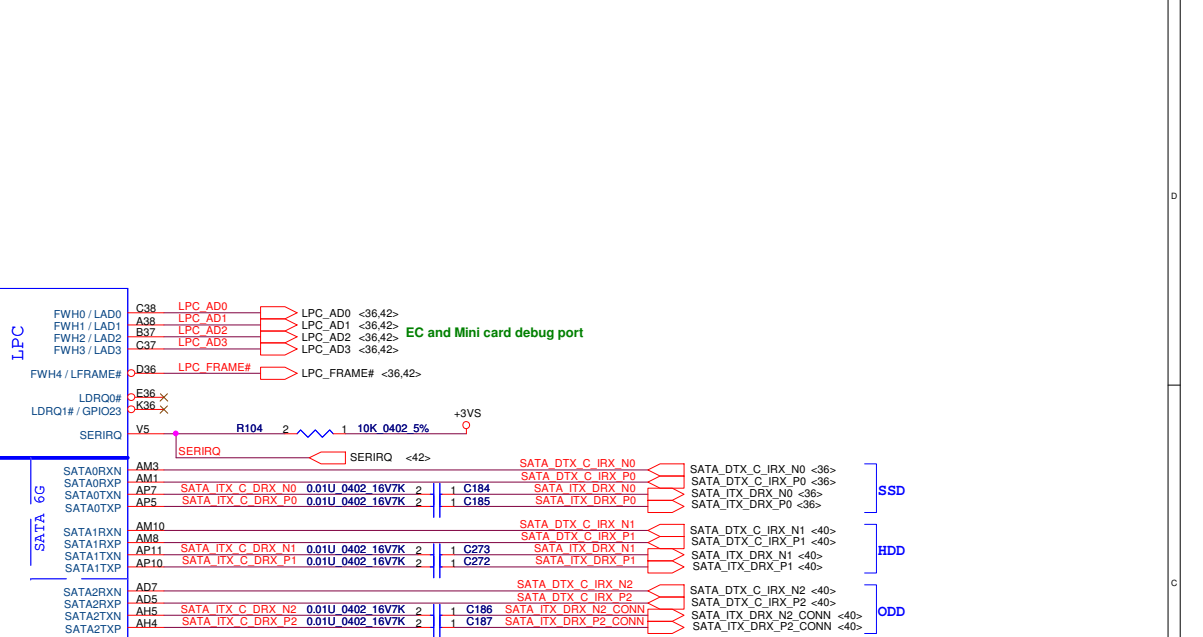
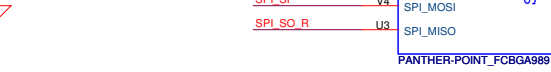
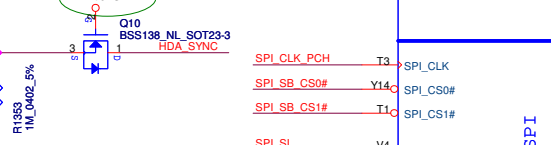
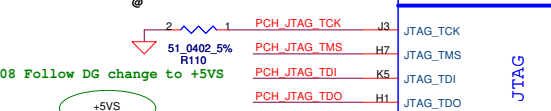
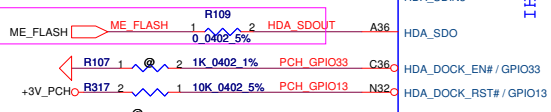
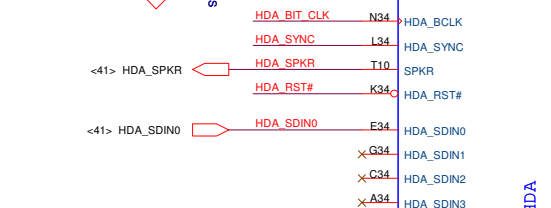
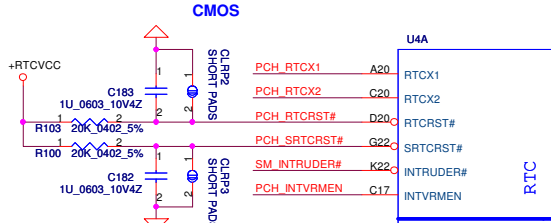
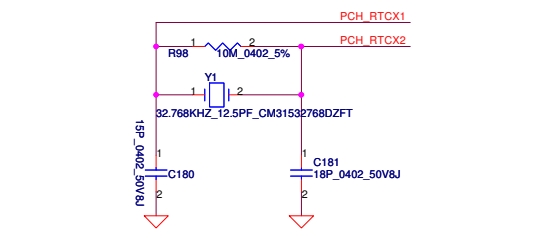
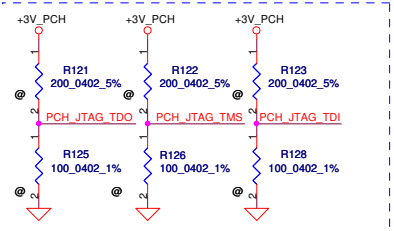
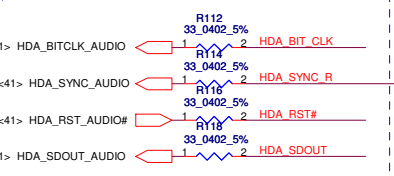
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETITION DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				PROCESSOR(7/7) VSS
				Size Custom
Date: Monday, January 16, 2012				Sheet 11 of 64

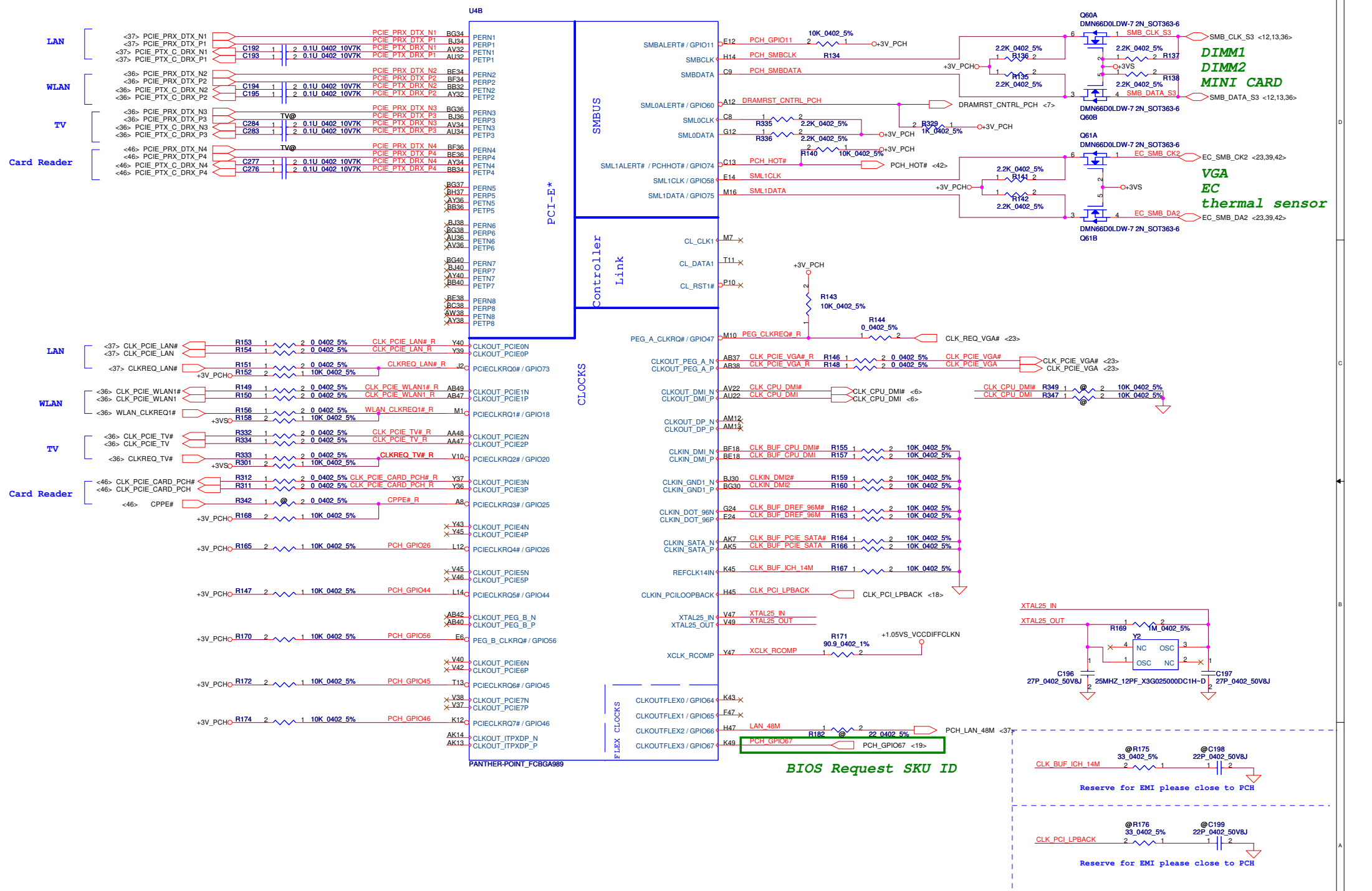


INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



On Die PLL VR Select is supplied by 1.5V when sampled high 1.8V when sampled low Needs to be pulled High for Chief River platform



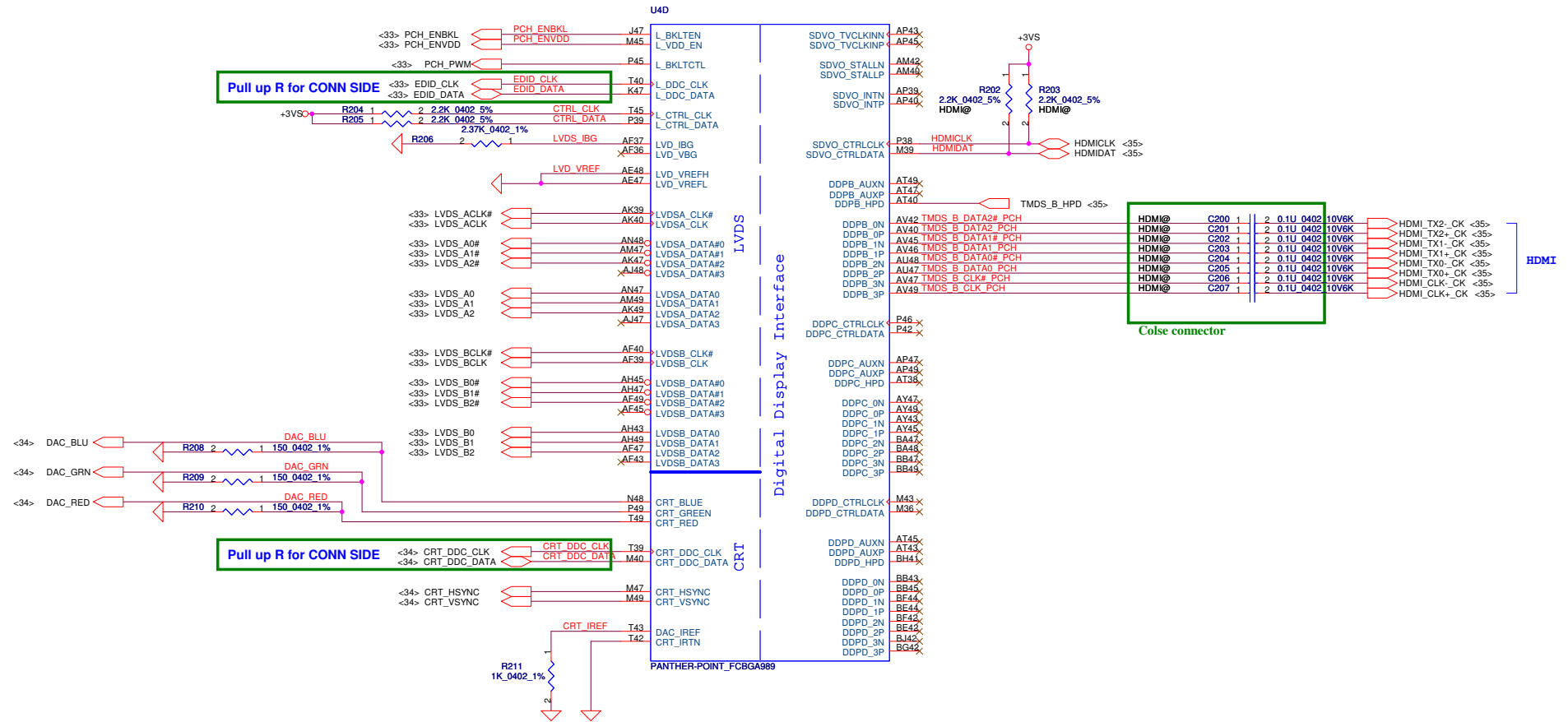


**DIMM1
DIMM2
MINI CARD**

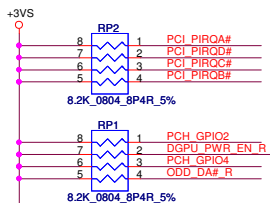
**VGA
EC
thermal sensor**

BIOS Request SKU ID

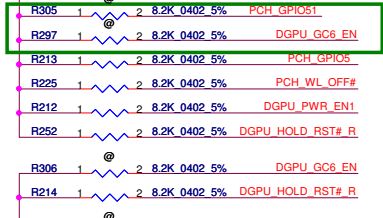
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	PCH (2/8) PCIE, SMBUS, CLK	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	QIYW4 LA-8002P
				Date:	Monday, January 16, 2012
				Sheet	15 of 64
				Rev	1.0



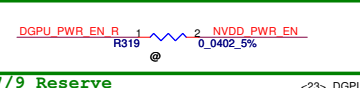
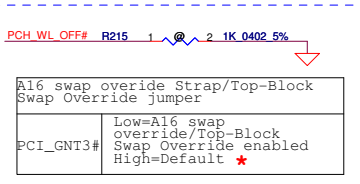
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH (4/9) LVDS,CRT,DP,HDMI	
Size	Customer	Date: Monday, January 16, 2012		Rev	1.0
				Sheet	17 of 64



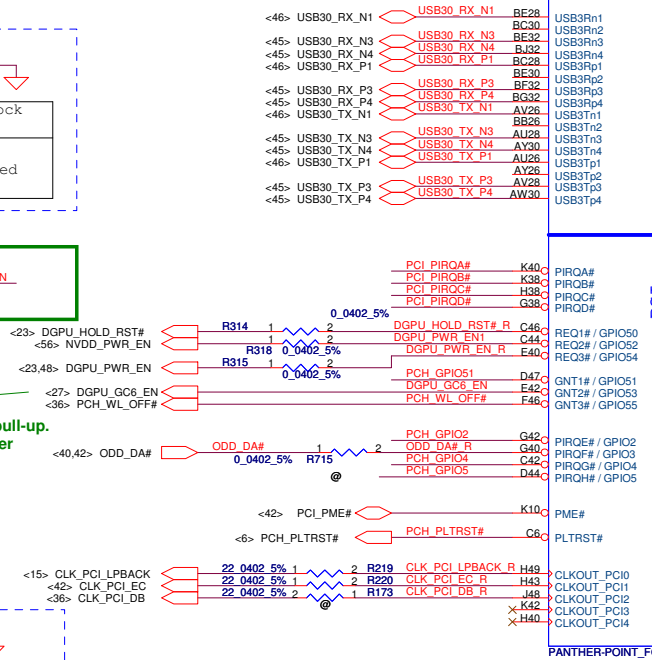
PPT EDS DOC#474146



PORT	USB30
PORT1	RIGHT USB (SUB/B)
PORT2	
PORT3	LEFT USB
PORT4	LEFT USB

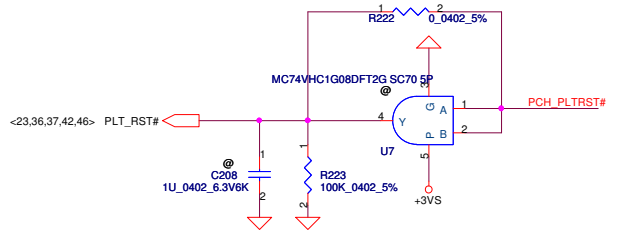
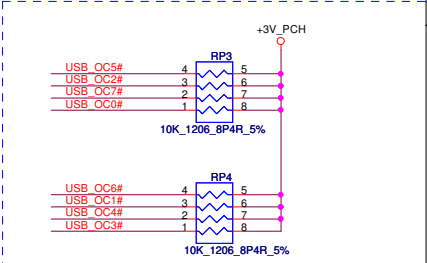


GPIO53=This signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



PCH_GPIO51 R221 1 2 1K 0402 5%

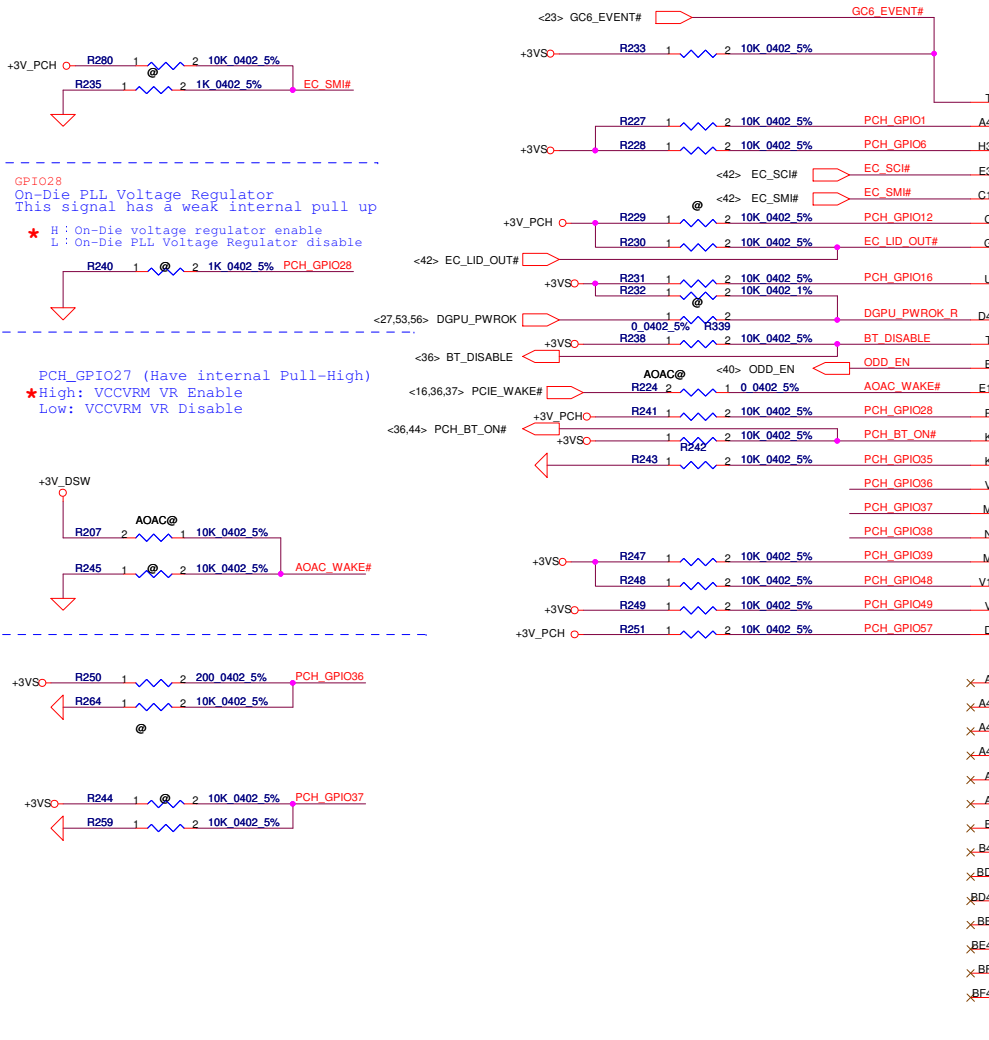
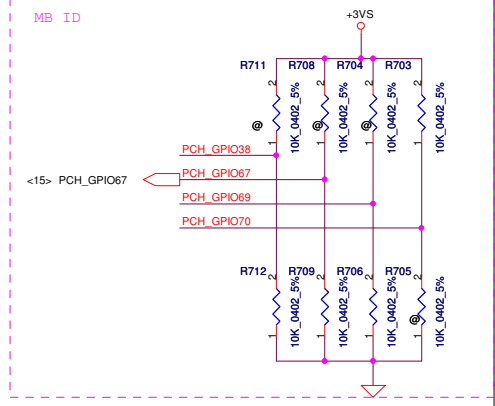
Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	* SPI (Default)
0	0	LPC



Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date 2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		

Compal Electronics, Inc.		
PCH (5/9) PCI, USB		
Title	Document Number	Rev
	QIYW4 LA-8002P	1.0
Date: Monday, January 16, 2012	Sheet	18 of 64

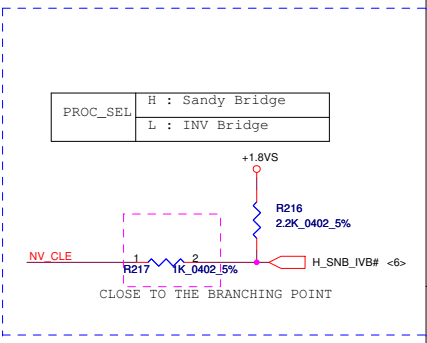
Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70	PCH_GPIO69
SG	0	0	X	X
Reserve	0	1	X	X
DIS	1	0	X	X
UMA	1	1	X	X
14"	X	X	0	0
14"L	X	X	0	1
15"	X	X	1	0
Reserve	X	X	1	1



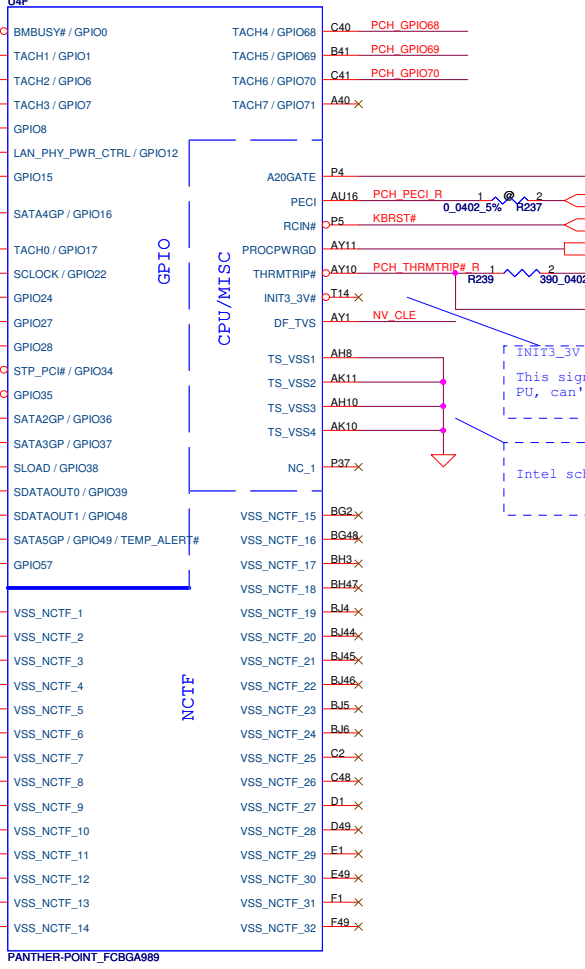
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable

INITS_3V
This signal has weak internal PU, can't pull low
Intel schematic review recommend.



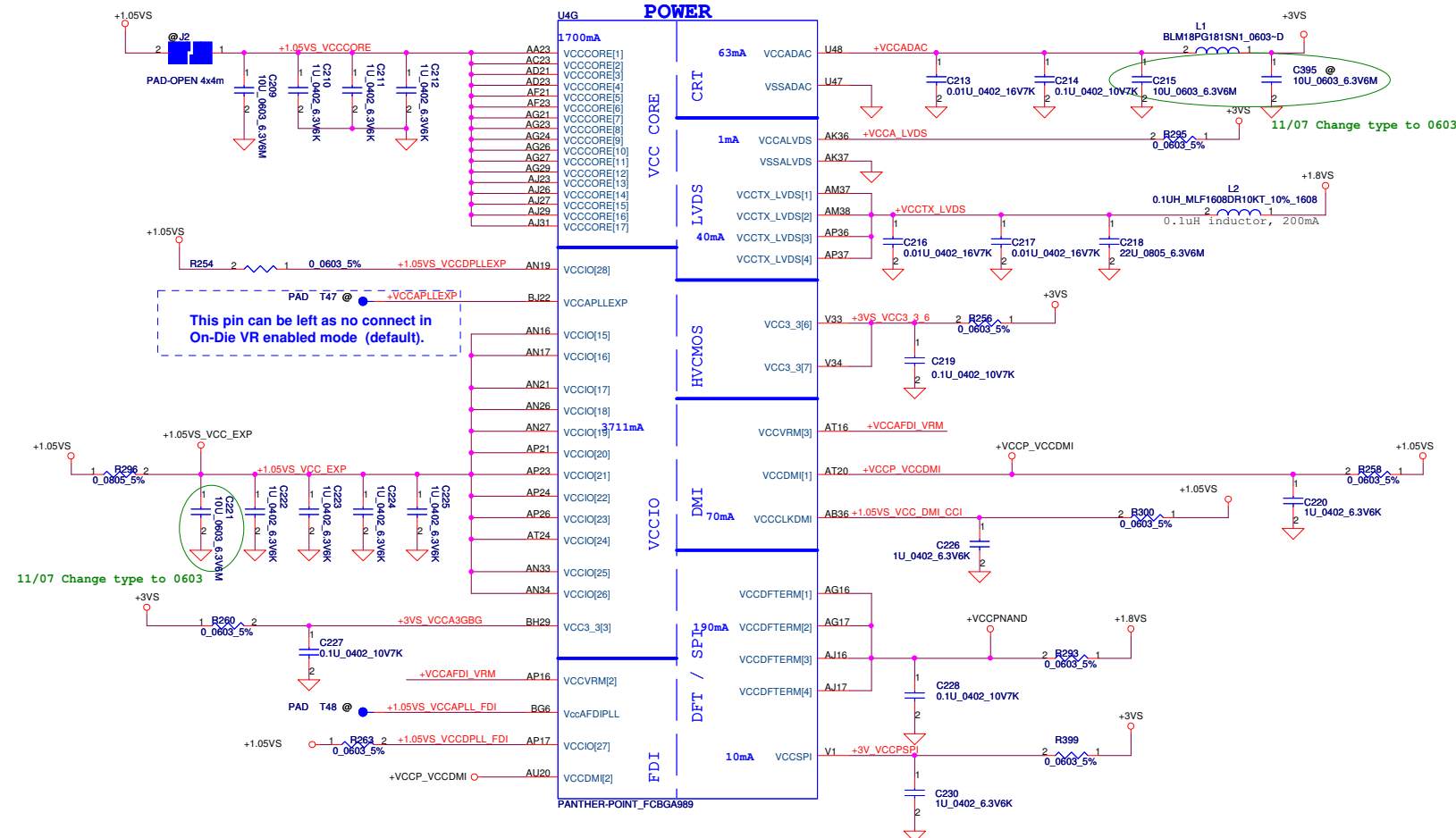
PROC_SEL	H : Sandy Bridge
	L : INV Bridge



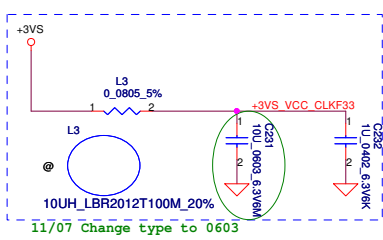
Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date
		2012/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

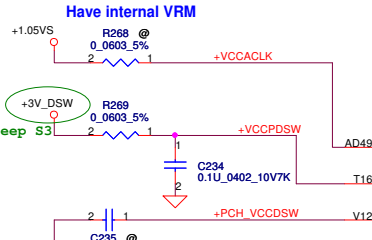
Compal Electronics, Inc.		
PCH (6/9) GPIO, CPU, MISC		
Size	Document Number	Rev
Custom	QIWIY4 LA-8002P	1.0
Date:	Monday, January 16, 2012	Sheet 19 of 64



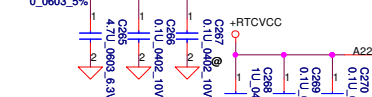
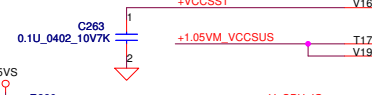
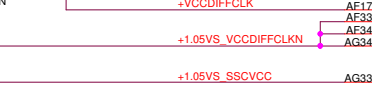
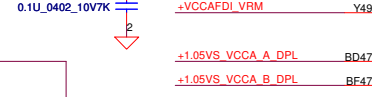
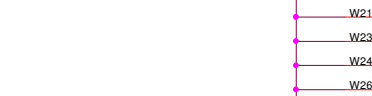
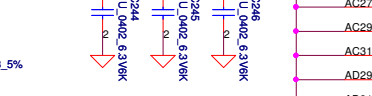
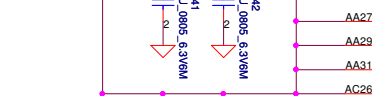
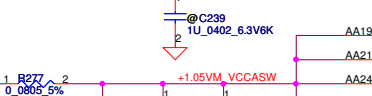
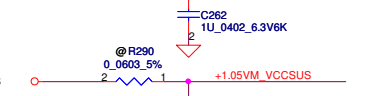
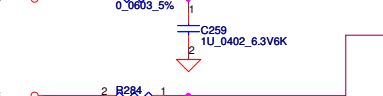
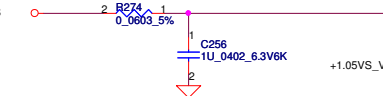
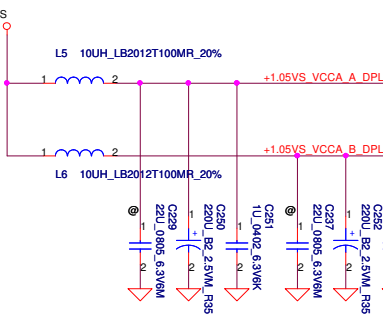
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2, VCCAPLLSATA



For Deep S3
+VCCACLK
+VCCPDSW
+PCH_VCCDSW
+3VS_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCDPLL_CPY



POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

IC

U4J

VCCACLK

VCCDSW3_3 1mA

VCCSUS3_3[7] 228mA

VCCSUS3_3[8] 1mA

VCCSUS3_3[9] 903mA

VCCSUS3_3[6] 1mA

VCCSUS3_3[2] 1mA

VCCSUS3_3[3] 1mA

VCCSUS3_3[4] 1mA

VCCSUS3_3[5] 1mA

VCCSUS3_3[1] 1mA

VCCSUS3_3[10] 1mA

VCCSUS3_3[11] 1mA

VCCSUS3_3[12] 1mA

VCCSUS3_3[13] 1mA

VCCSUS3_3[14] 1mA

VCCSUS3_3[15] 1mA

VCCSUS3_3[16] 1mA

VCCSUS3_3[17] 1mA

VCCSUS3_3[18] 1mA

VCCSUS3_3[19] 1mA

VCCSUS3_3[20] 1mA

VCCSUS3_3[21] 1mA

VCCSUS3_3[22] 1mA

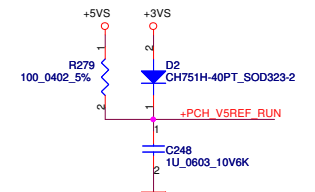
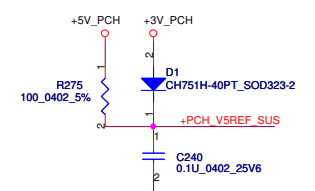
VCCSUS3_3[23] 1mA

VCCSUS3_3[24] 1mA

VCCSUS3_3[25] 1mA

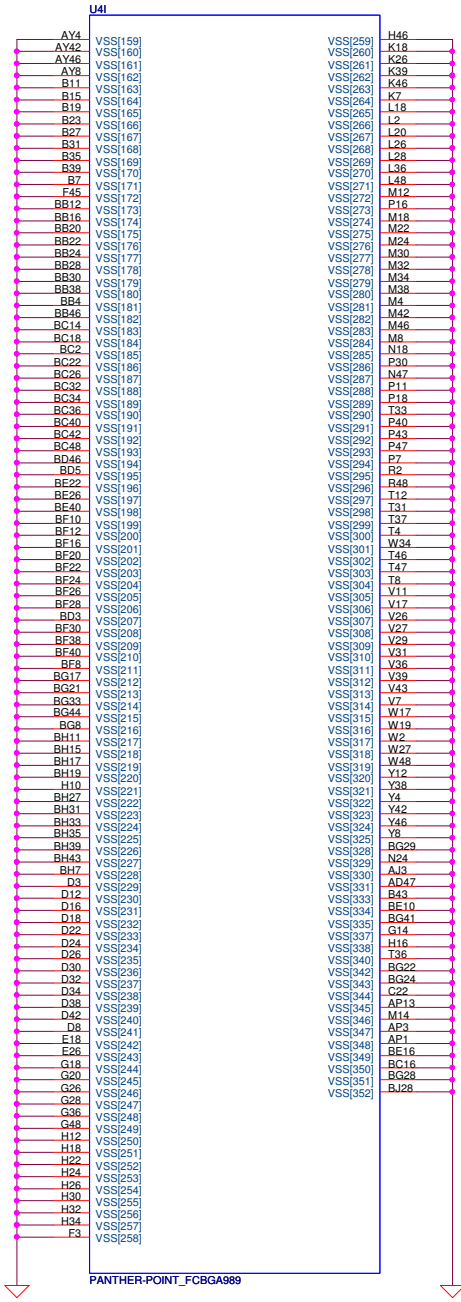
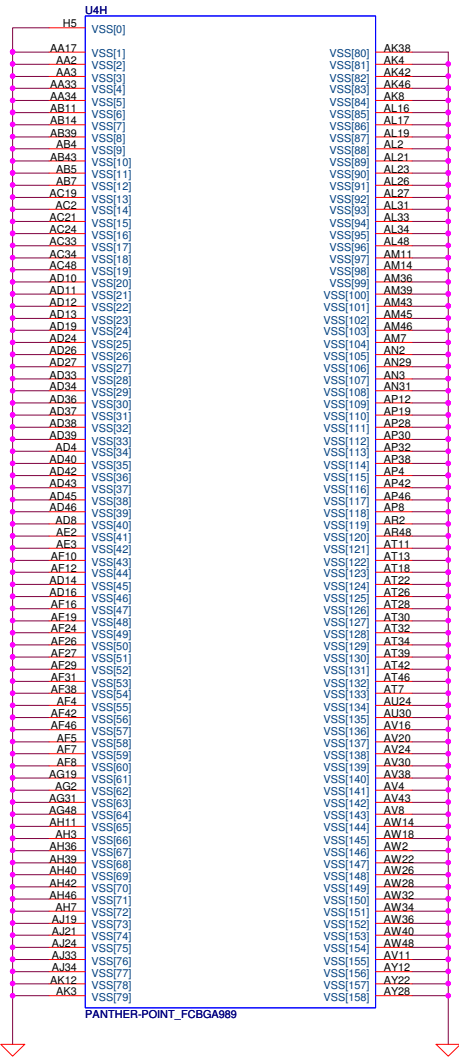
VCCSUS3_3[26] 1mA

VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

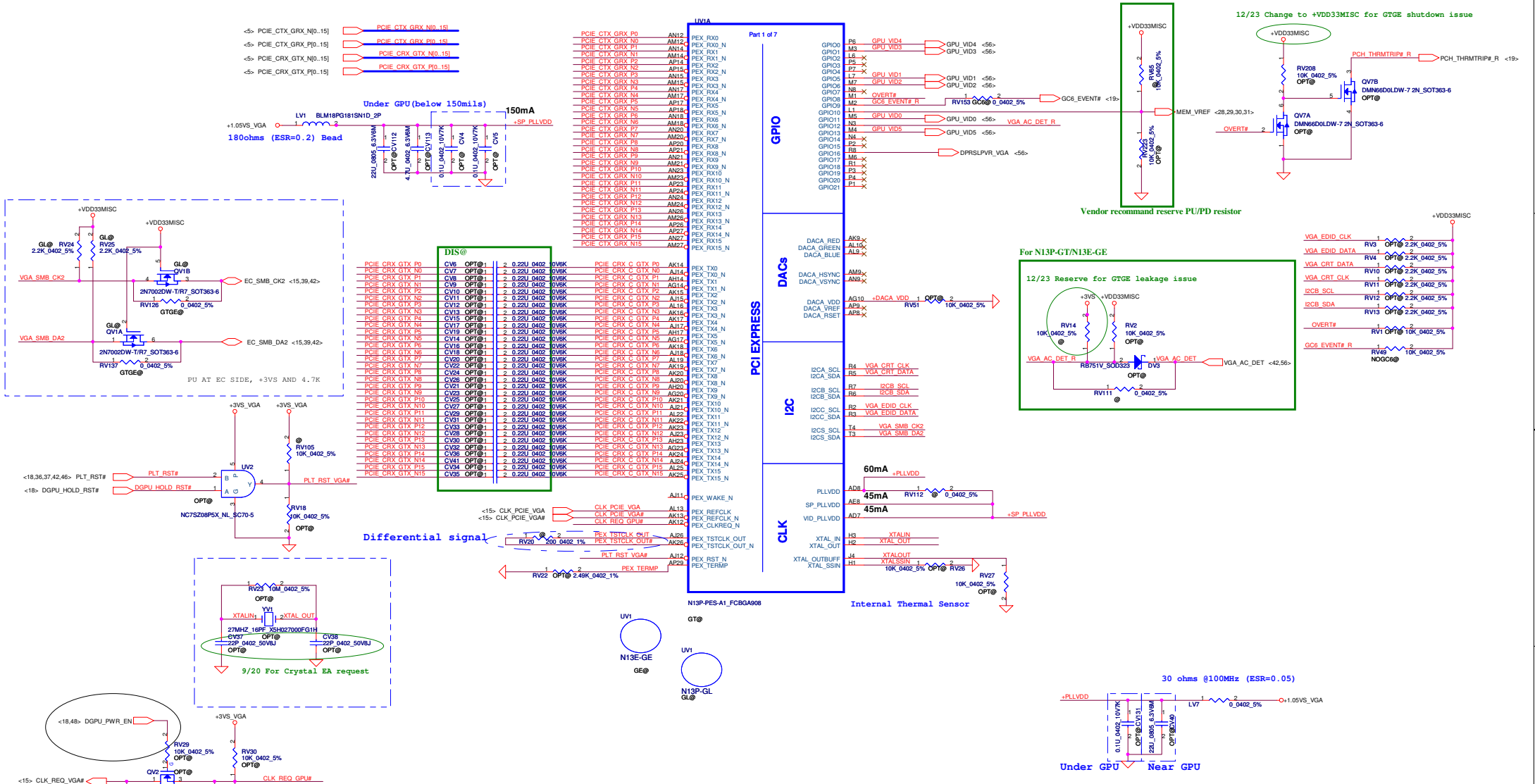


On-Die PLL Voltage Regulator
 H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLEXP, VCCAPLLDMI2, VCCAPLLSATA

Security Classification	Compal Secret Data			Title Compal Electronics, Inc. PCH (8/9) PWR
Issued Date	2011/07/21	Deciphered Date	2012/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Customer
				Document Number QIWIY4 LA-8002P
				Rev 1.0
				Date: Monday, January 16, 2012
				Sheet 21 of 64



Security Classification	Compal Secret Data			Compal Electronics, Inc. PCH (9/9) VSS			
Issued Date	2011/07/21	Deciphered Date	2012/12/31				
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Title PCH (9/9) VSS	Size Custom	Document Number QIWIY4 LA-8002P	Rev 1.0
				Date: Monday, January 16, 2012	Sheet 22	of 64	

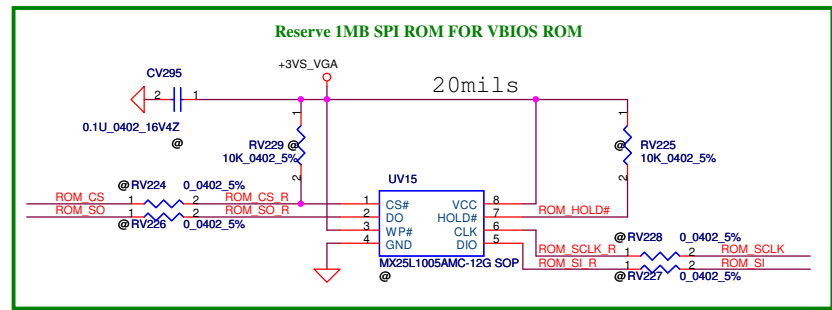
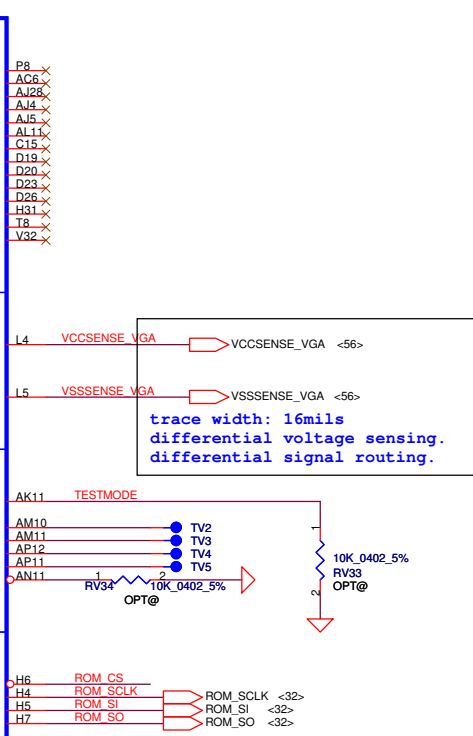
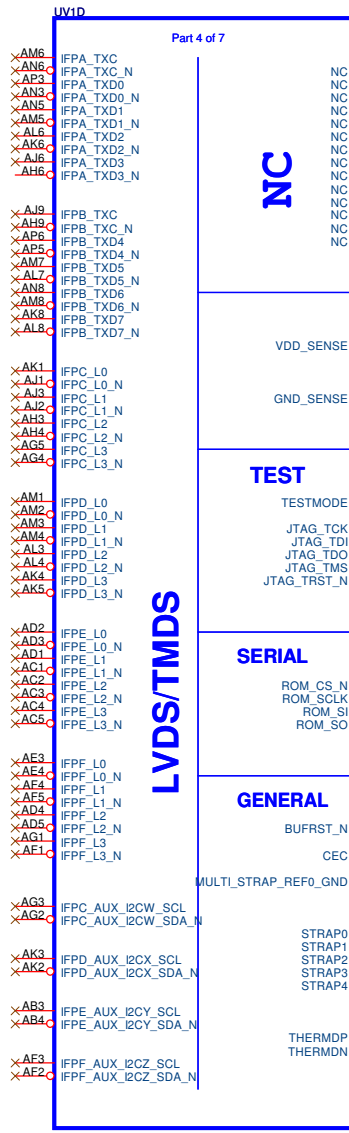


Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Document Number QIY4 LA-8002P Rev 1.0
Date	Monday, January 18, 2012	Sheet	23	of 84

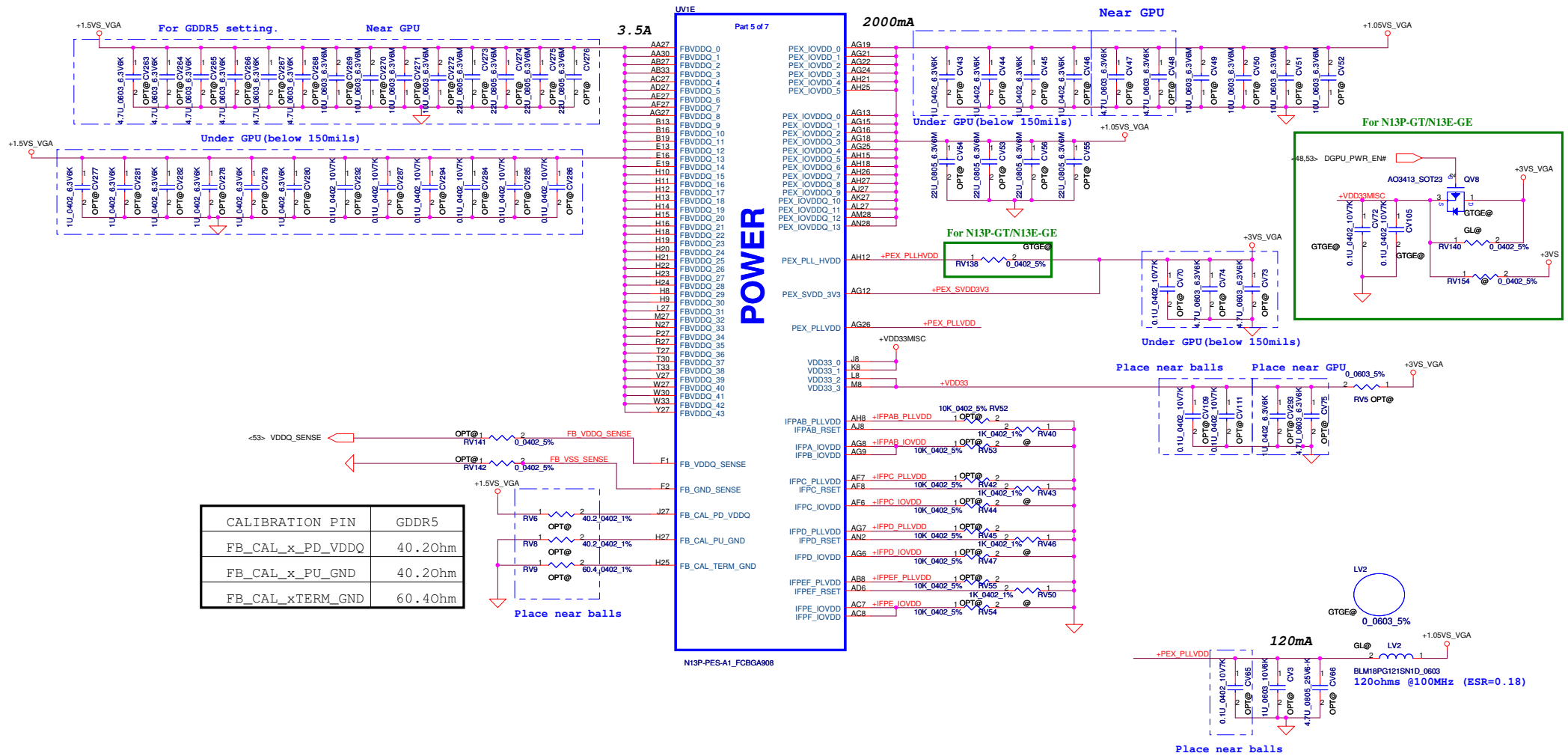
Compal Electronics, Inc.
N13P-PCIe/DAC/GPIO

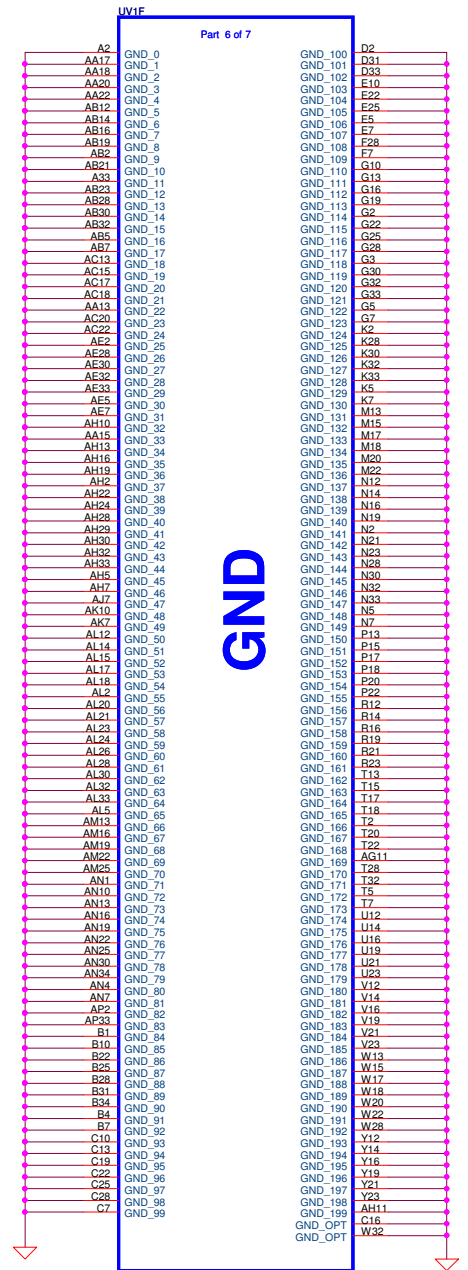
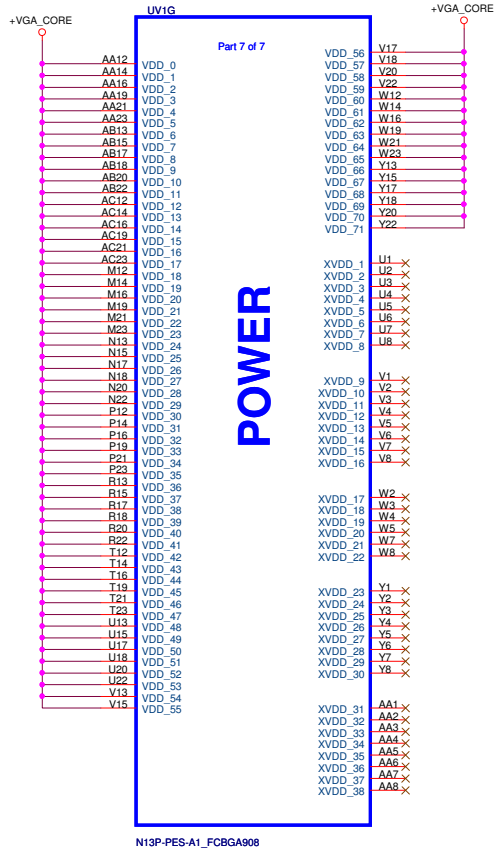
QIY4 LA-8002P

Monday, January 18, 2012 Sheet 23 of 84



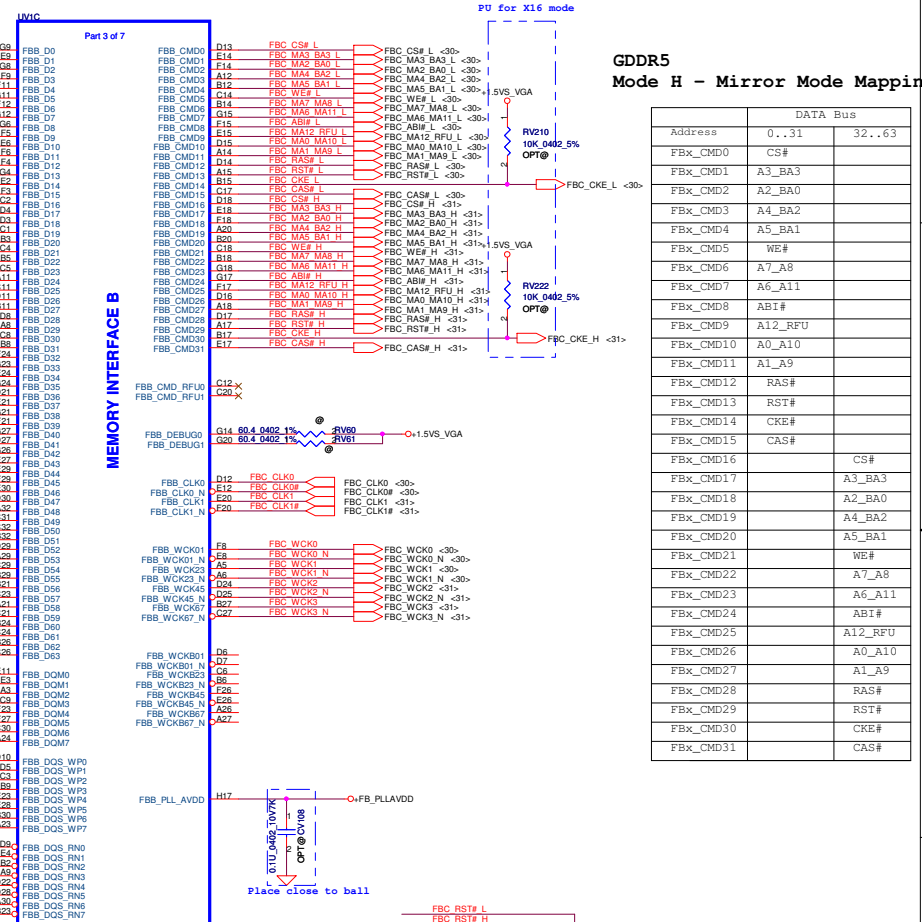
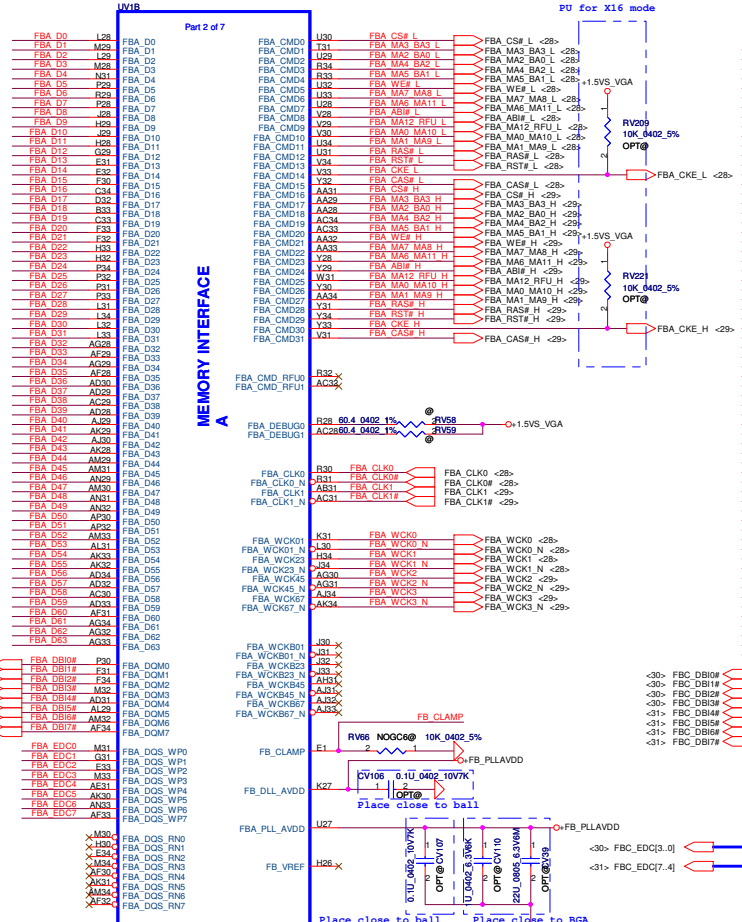
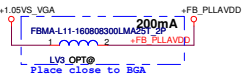
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				N13P-LVDS/HDMI/DP/THM	
Size	Document Number			Rev	1.0
Date: Monday, January 16, 2012				Sheet	24 of 64





Security Classification		Compal Secret Data		N13P-PES-A1_FCBGA908		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				N13P-VGA CORE, GND			
Size	Document Number	Date		Monday, January 16, 2012		Rev	1.0
				QIYW4 LA-8002P		Sheet	26 of 64

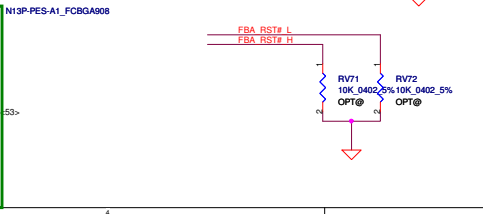
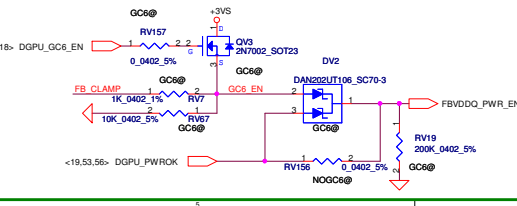
30ohms (ESR=0.01) Bead
P/N: SM010007W00



**GD8R5
Mode H - Mirror Mode Mapping**

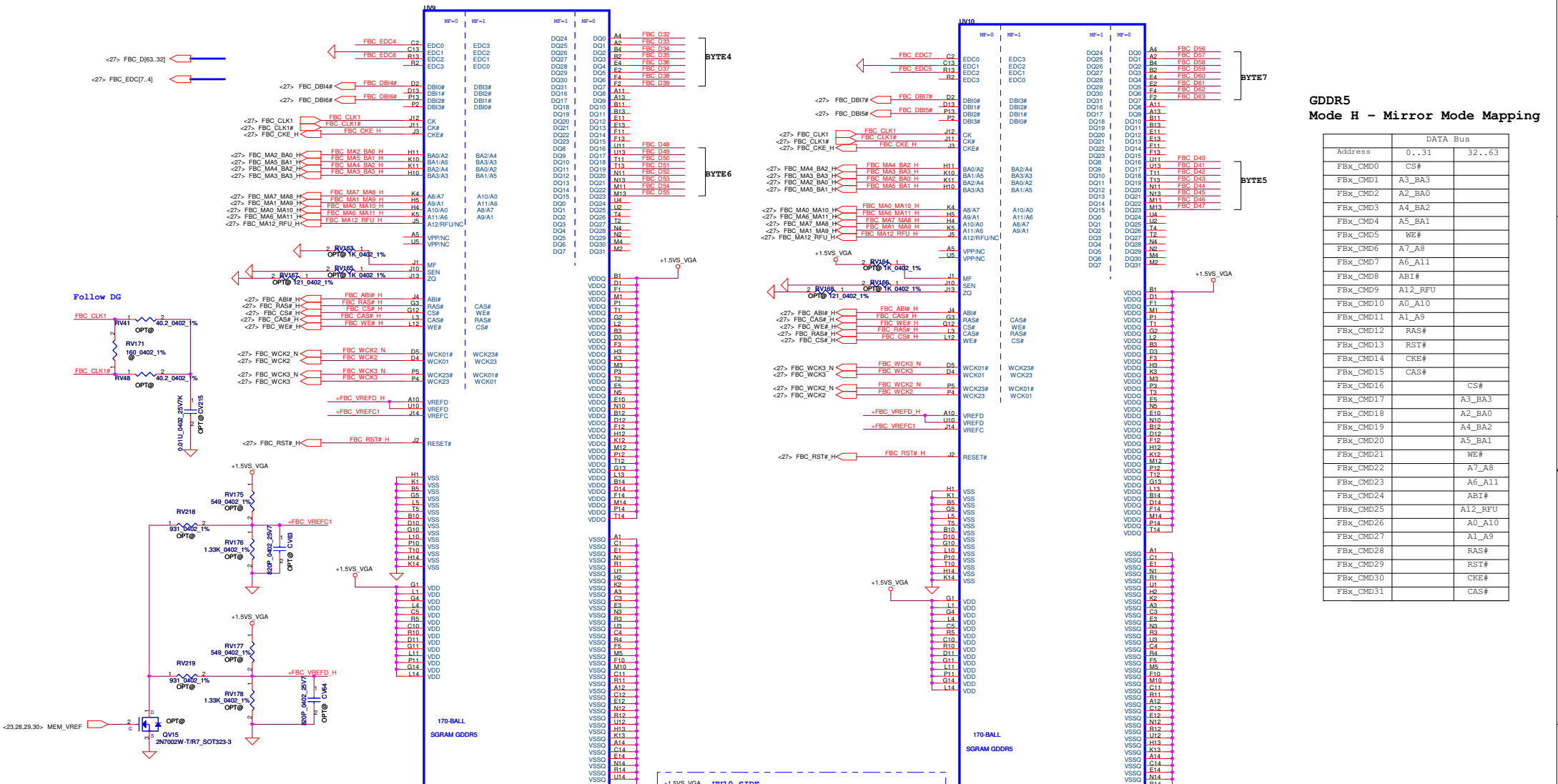
Address	DATA Bus
FBB_CMD0	0..31
FBB_CMD1	A3_BA3
FBB_CMD2	A2_BA0
FBB_CMD3	A4_BA2
FBB_CMD4	A5_BA1
FBB_CMD5	WE#
FBB_CMD6	A7_A8
FBB_CMD7	A6_A11
FBB_CMD8	ABT#
FBB_CMD9	A12_RFU
FBB_CMD10	A0_A10
FBB_CMD11	A1_A9
FBB_CMD12	RAS#
FBB_CMD13	RST#
FBB_CMD14	CKE#
FBB_CMD15	CAS#
FBB_CMD16	CS#
FBB_CMD17	A3_BA3
FBB_CMD18	A2_BA0
FBB_CMD19	A4_BA2
FBB_CMD20	A5_BA1
FBB_CMD21	WE#
FBB_CMD22	A7_A8
FBB_CMD23	A6_A11
FBB_CMD24	ABT#
FBB_CMD25	A12_RFU
FBB_CMD26	A0_A10
FBB_CMD27	A1_A9
FBB_CMD28	RAS#
FBB_CMD29	RST#
FBB_CMD30	CKE#
FBB_CMD31	CAS#

For N13P-GT/N13E-GE GC6 support



Security Classification	Compal Secret Data		<p align="center">Compal Electronics, Inc.</p> <p align="center">N13P-MEM Interface</p> <p align="center">QIYW4 LA-8002P</p>
Issued Date	2011/07/21	Deciphered Date	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPLETED DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			Title: N13P-MEM Interface Size: Document Number Date: Monday, January 18, 2012 Sheet: 27 of 84

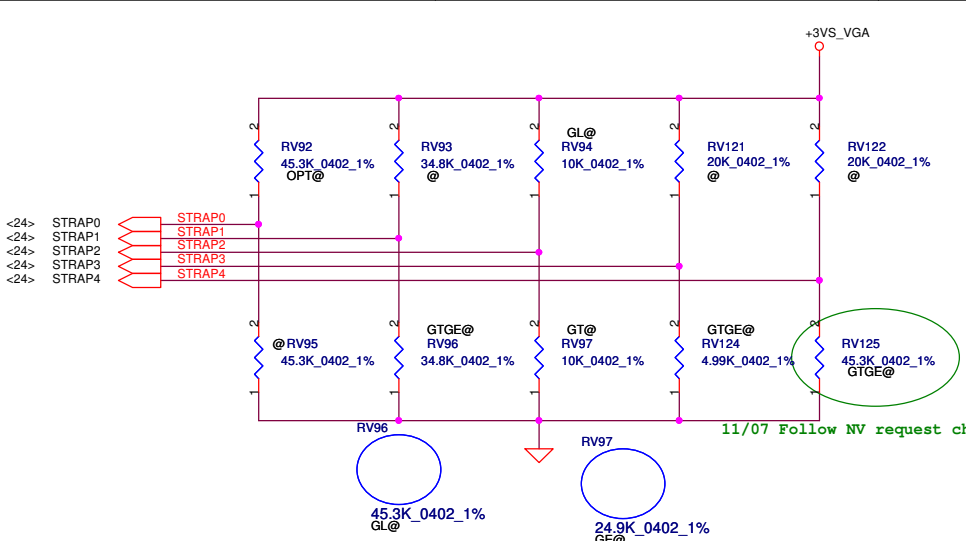
Memory Partition C - Upper 32 bits



GDDR5 Mode H - Mirror Mode Mapping

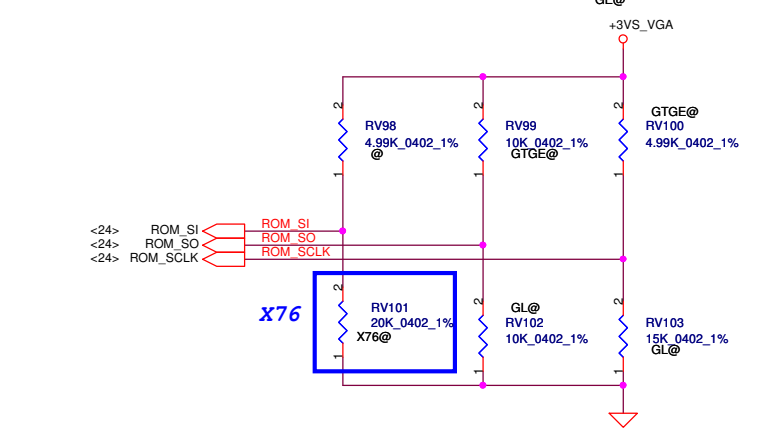
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RA5#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RA5#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2011/07/21	Deciphered Date	2012/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom
Date: Monday, January 16, 2012				Document Number QIWW4 1A-8002P
				Rev 1.0
				Sheet 31 of 84



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



3GIO_PADCFG		XCLK_417	
3GIO_PADCFG[3:0]		0	277MHz (Default)
0110	Notebook Default	1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

USER Straps	
User [3:0]	
1000-1100	Customer defined

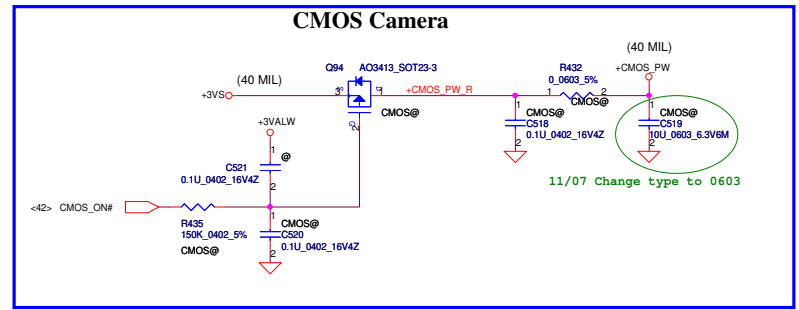
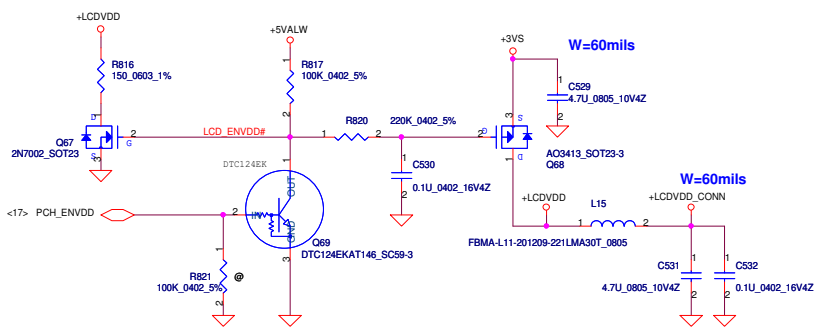
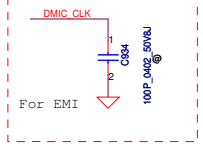
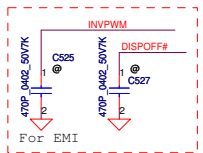
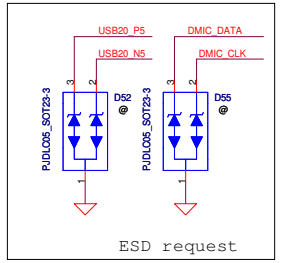
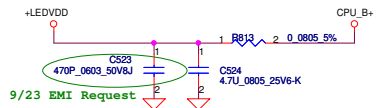
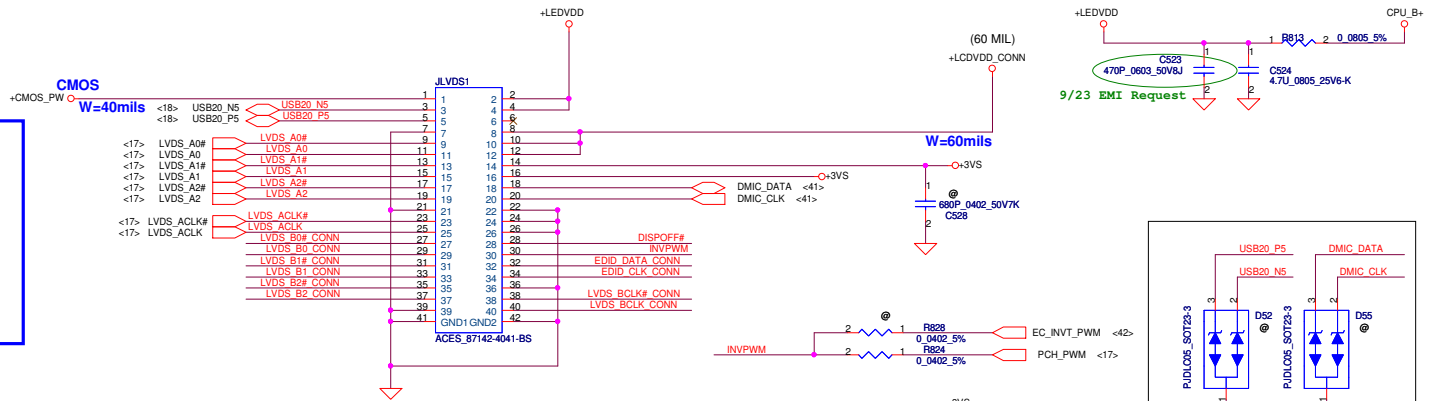
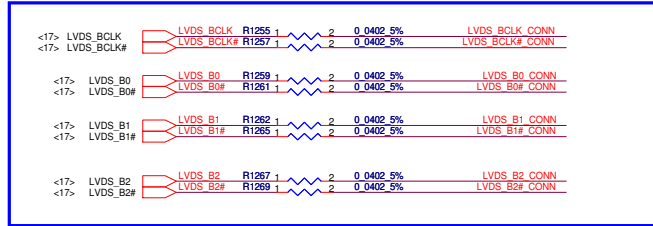
FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

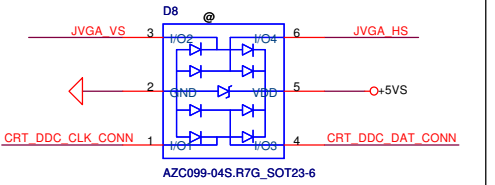
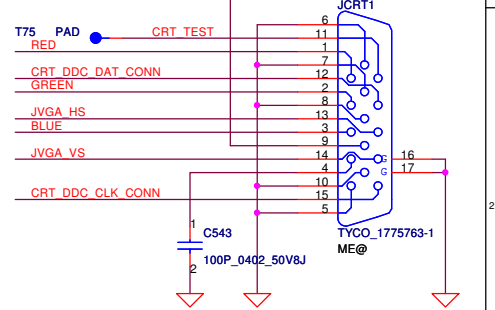
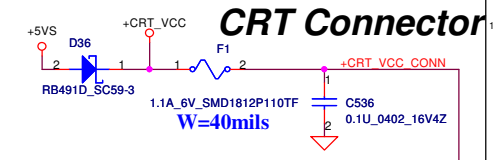
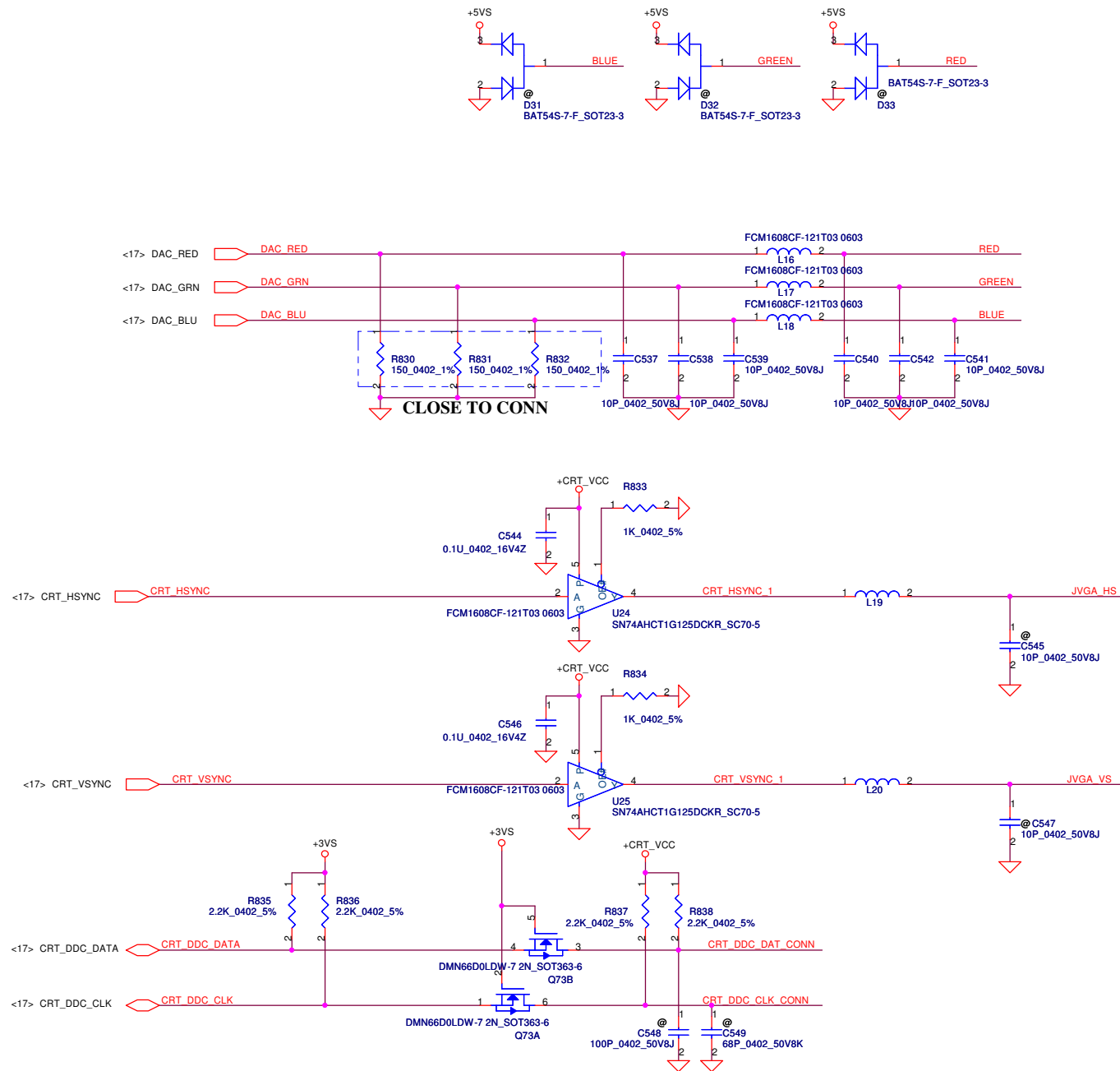
PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification	Compal Secret Data		Compal Electronics, Inc. N13P MISC QIYW4 LA-8002P	
Issued Date	2011/07/21	Deciphered Date		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title Size Custom Document Number Date: Monday, January 16, 2012
				Sheet 32 of 64 Rev 1.0

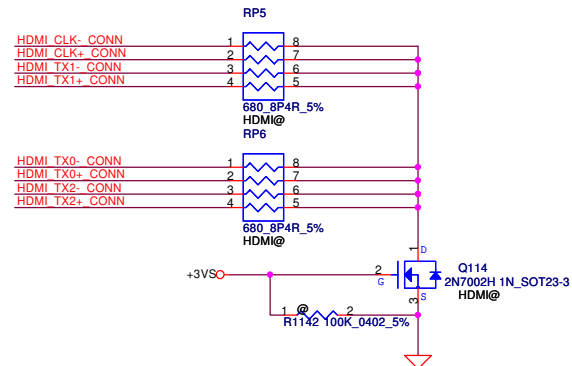
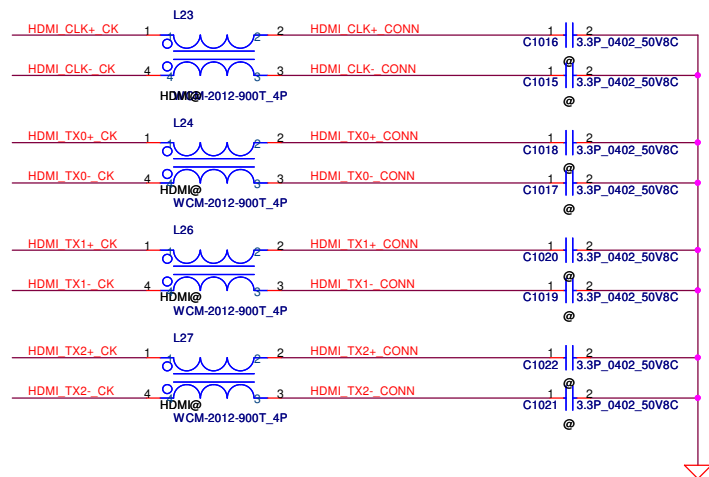
For 15" DUAL-CHANNEL reserve



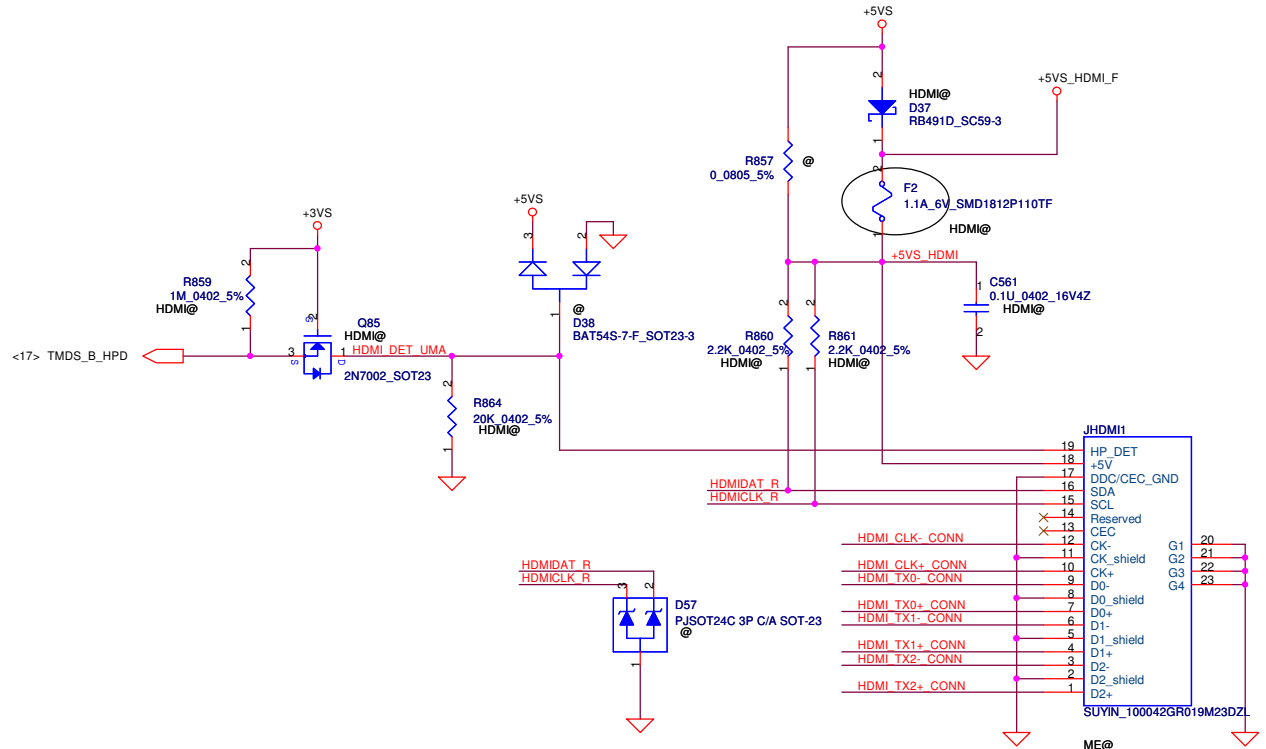
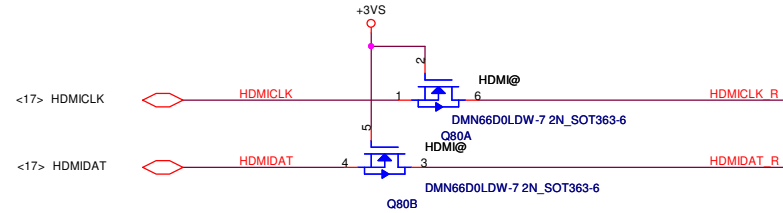
Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev
Soc				1.0
Cus				QIWIYA LA-8002P
Date				Monday, January 16, 2012
Sheet				33 of 64



Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CRT Connector	
Size	Document Number	Rev		1.0	
Custom	QIYWY4 LA-8002P	Date:		Monday, January 16, 2012	
				Sheet	34 of 64



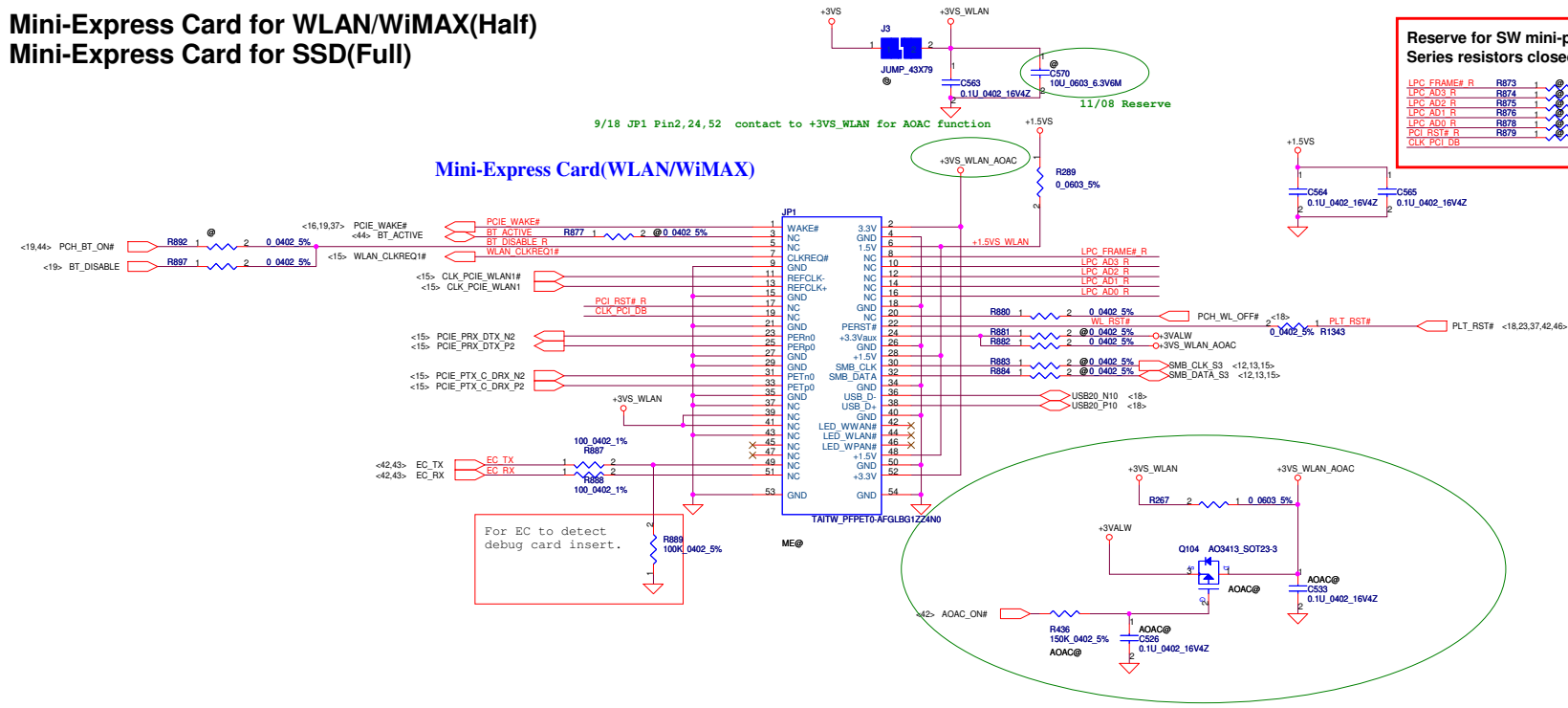
<17> HDMI_CLK+_CK	HDMI_CLK+_CK	R865	1	@	2	0.0402	5%	HDMI_CLK+_CONN
<17> HDMI_CLK-_CK	HDMI_CLK-_CK	R866	1	@	2	0.0402	5%	HDMI_CLK-_CONN
<17> HDMI_TX0+_CK	HDMI_TX0+_CK	R867	1	@	2	0.0402	5%	HDMI_TX0+_CONN
<17> HDMI_TX0-_CK	HDMI_TX0-_CK	R868	1	@	2	0.0402	5%	HDMI_TX0-_CONN
<17> HDMI_TX1+_CK	HDMI_TX1+_CK	R869	1	@	2	0.0402	5%	HDMI_TX1+_CONN
<17> HDMI_TX1-_CK	HDMI_TX1-_CK	R870	1	@	2	0.0402	5%	HDMI_TX1-_CONN
<17> HDMI_TX2+_CK	HDMI_TX2+_CK	R871	1	@	2	0.0402	5%	HDMI_TX2+_CONN
<17> HDMI_TX2-_CK	HDMI_TX2-_CK	R872	1	@	2	0.0402	5%	HDMI_TX2-_CONN



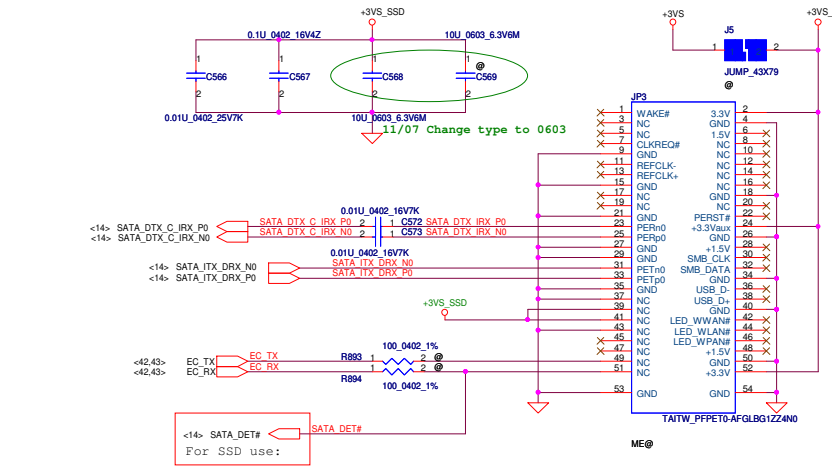
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	HDMI CONN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size Custom	Document Number	Date		Rev	1.0
	QIWY4 LA-8002P	Monday, January 16, 2012		Sheet	35 of 64

Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

Mini-Express Card(WLAN/WiMAX)

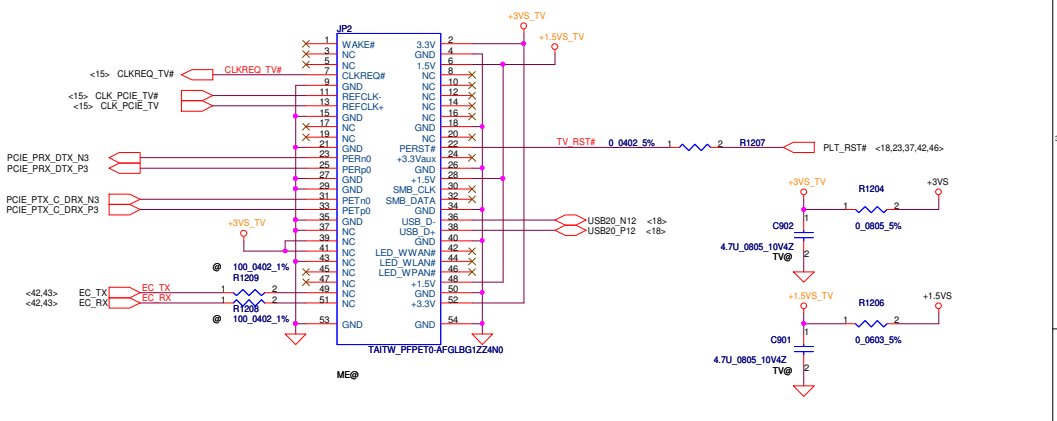


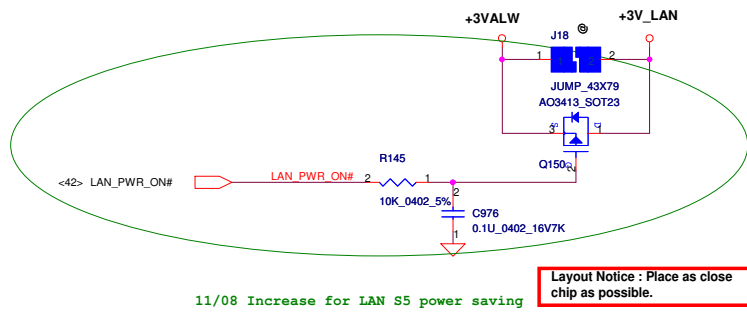
Mini-Express Card(SSD)



SSD Active:4.5W(1.5A)

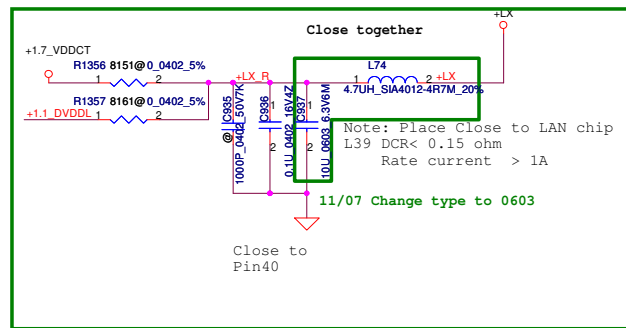
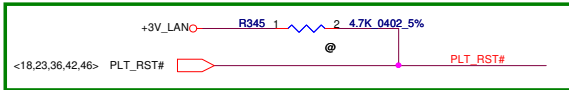
Mini-Express Card(TV)



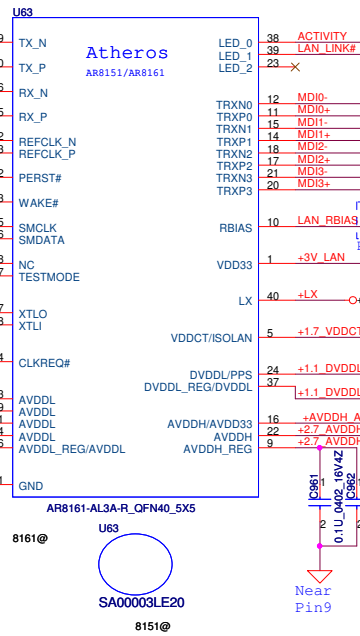
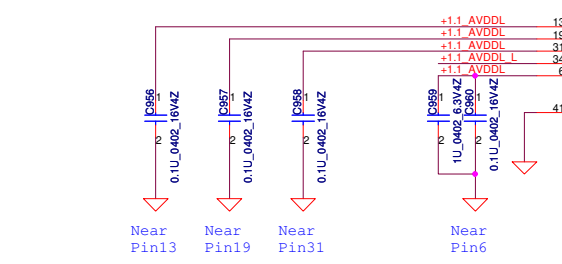
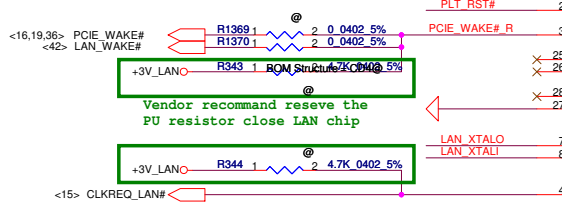
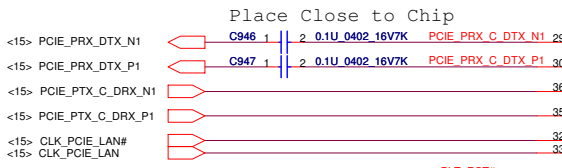
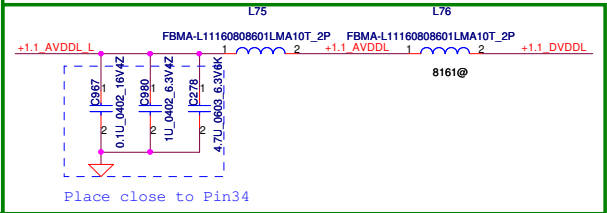


Layout Notice : Place as close chip as possible.

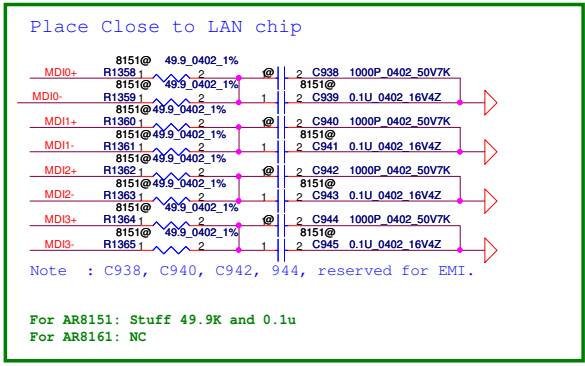
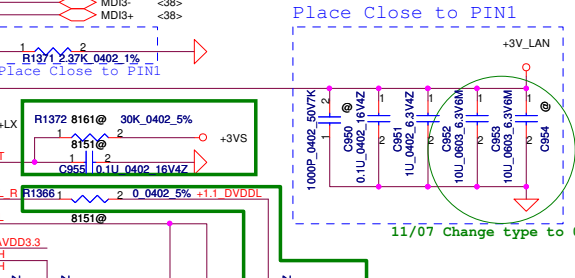
Vendor recommend reserve the PU resistor close LAN chip



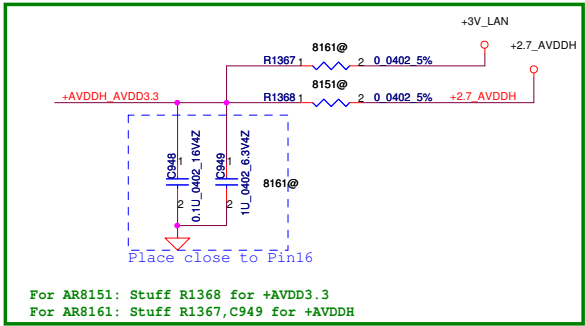
	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76



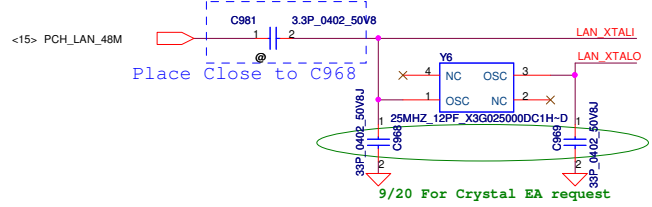
H ---> Overclocking mode
L ---> Not overclocking mode



Note : C938, C940, C942, 944, reserved for EM1.
For AR8151: Stuff 49.9K and 0.1u
For AR8161: NC



For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367, C949 for +AVDDH

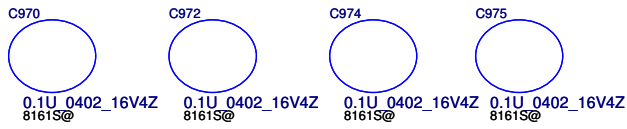


9/20 For Crystal EA request

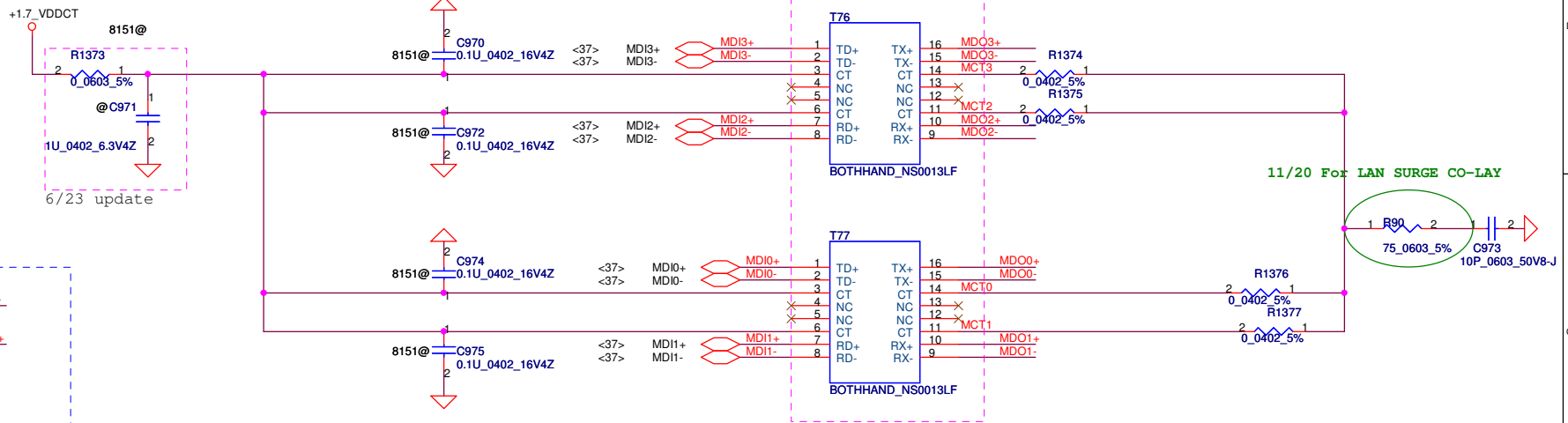
Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date
		2012/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

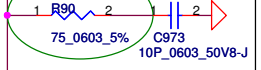
Compal Electronics, Inc.		
Title	LAN-AR8151/8161	
Size Custom	Document Number	Rev
	QIYW4 LA-8002P	1.0
Date:	Monday, January 16, 2012	Sheet 37 of 64



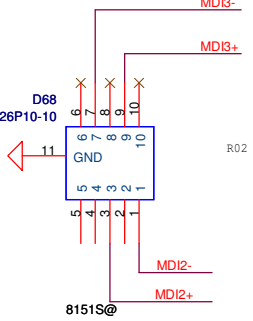
8/23 Change T1,T2 P/N to SP050007K00



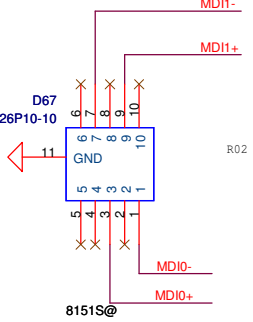
11/20 For LAN SURGE CO-LAY



Place Close to T76

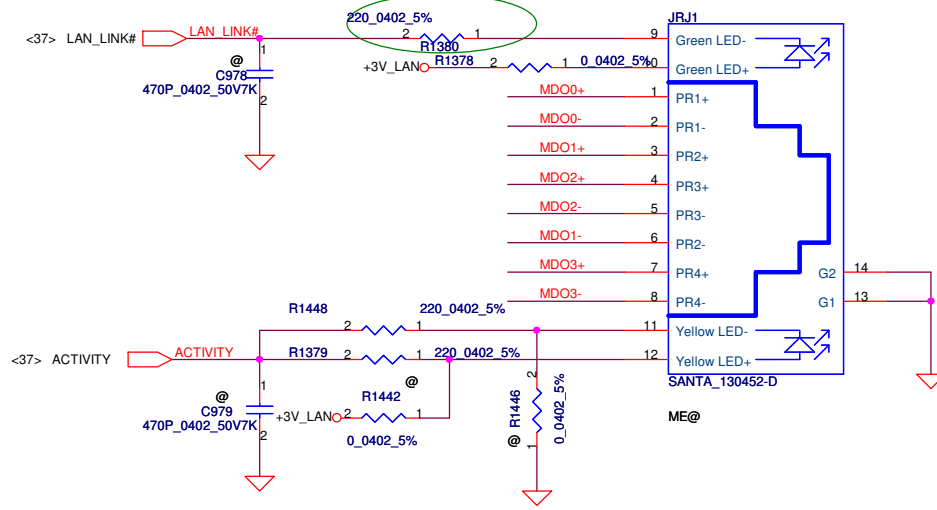


Place Close to T77

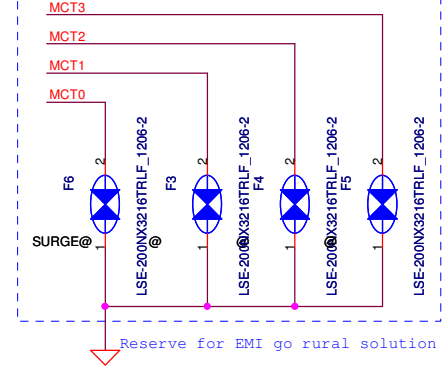


Reserve D67,D68 for EMI go rural solution

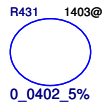
11/20 Atheros request



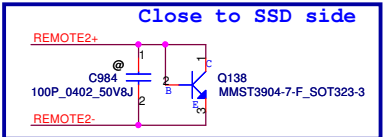
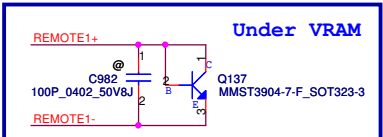
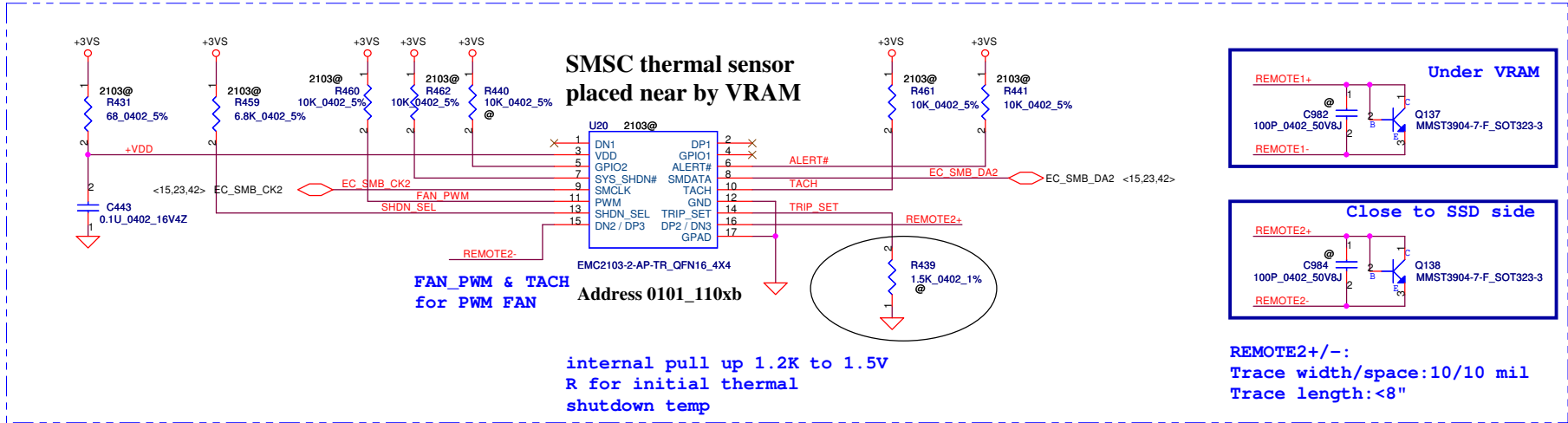
Place Close to T76, T77



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LAN_Transformer	
Size	Document Number			Rev	
	QIWY4 LA-8002P			1.0	
Date:	Monday, January 16, 2012		Sheet	38 of 64	

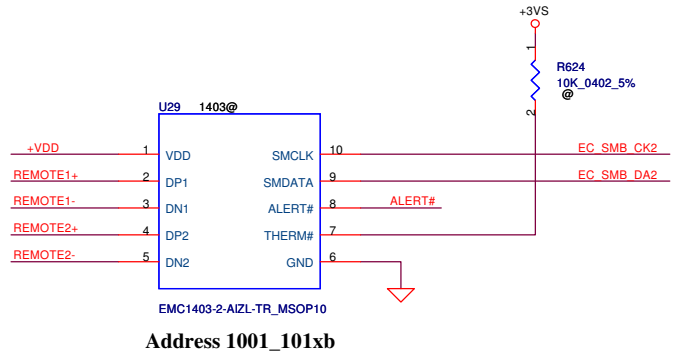
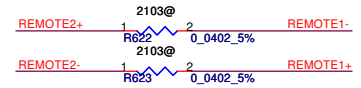
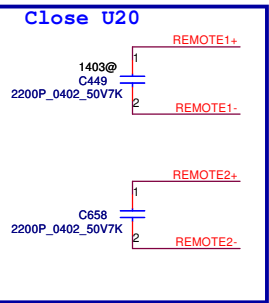


1403:
@C982/@C984=100p

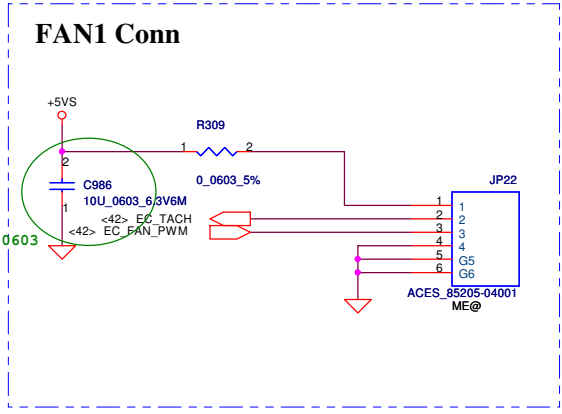


REMOTE2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp



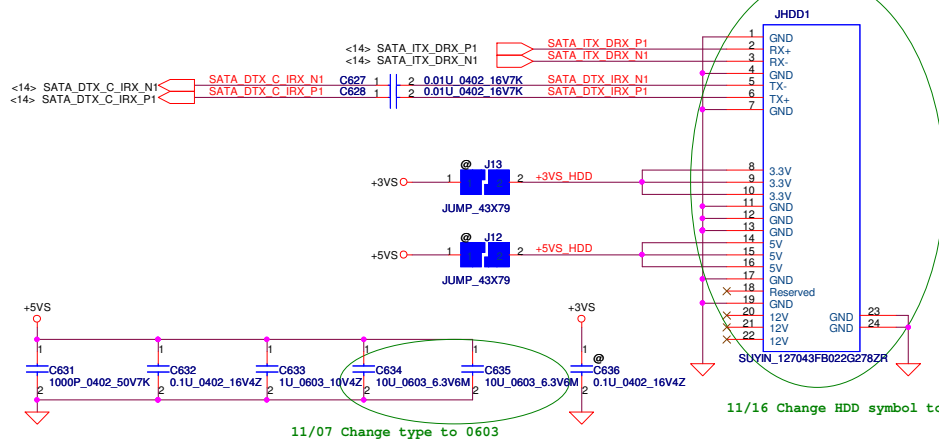
Shutdown Temp	TRIP_SET R1387 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm



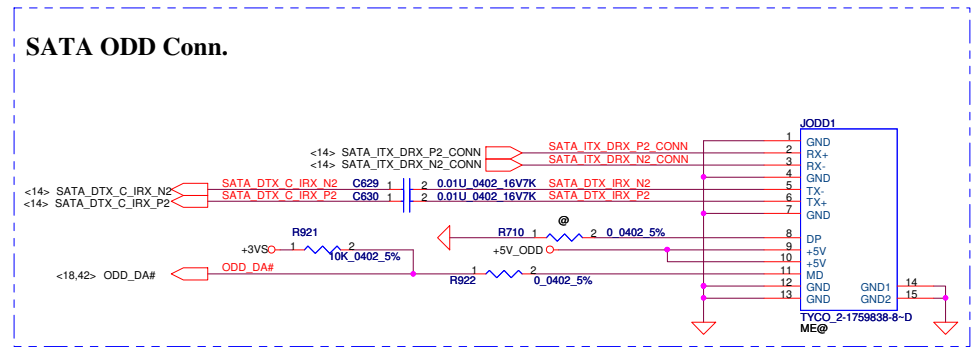
11/07 Change type to 0603

Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				EMC1403/2103 Thermal sensor/FAN	
Size	Document Number	Date		Rev	1.0
Custom	QIWIY4 LA-8002P	Monday, January 16, 2012		Sheet	39 of 64

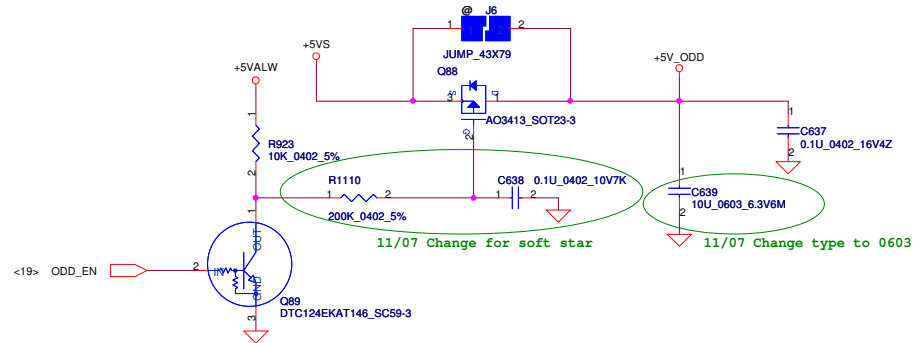
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



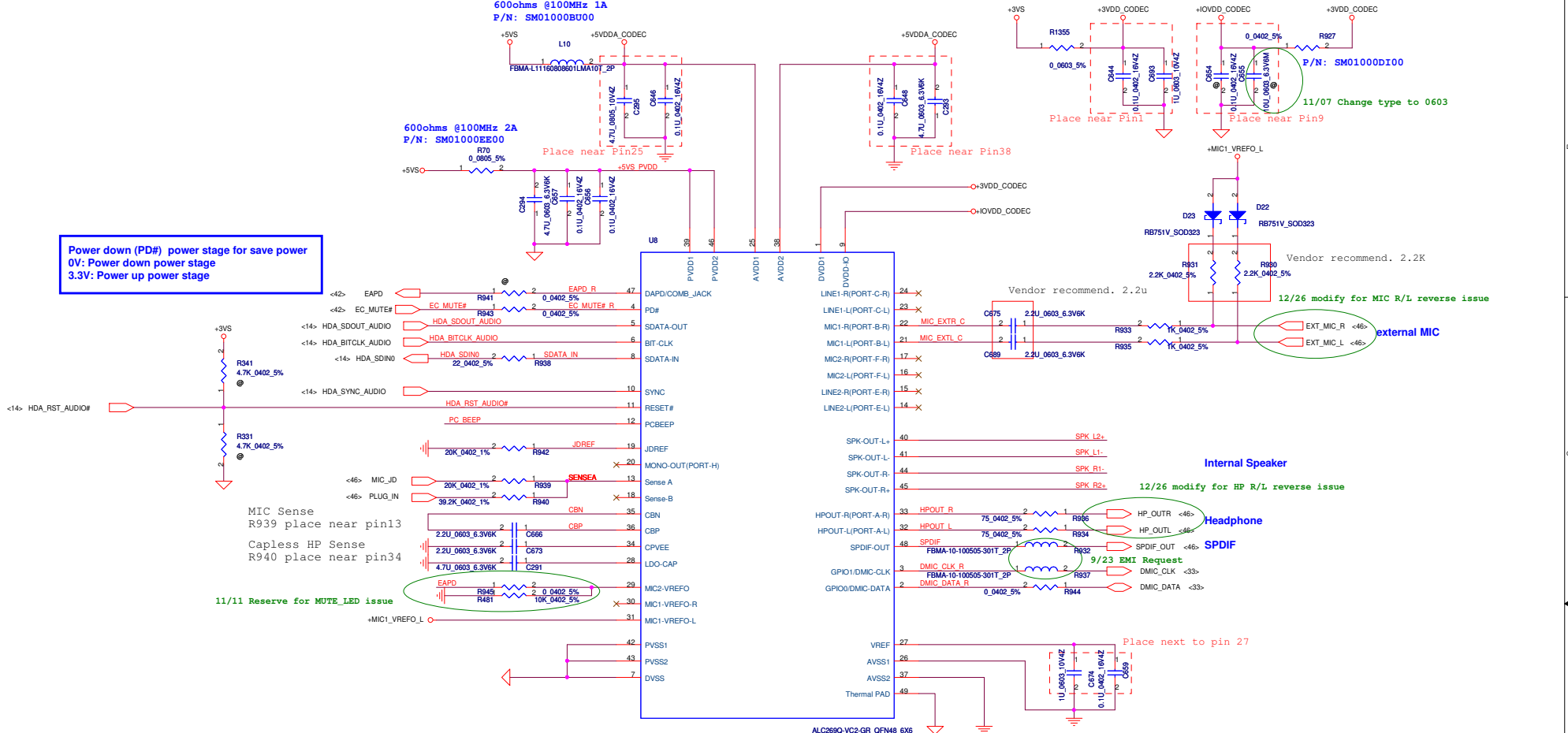
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Compal Electronics, Inc. HDD/ODD Connector	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B	Document Number
				QIWI4 LA-8002P Date: Monday, January 16, 2012 Sheet 40 of 64	
				Rev	1.0

600ohms @100MHz 1A
P/N: SM01000BU00

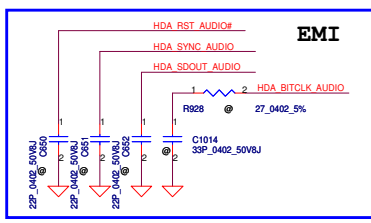
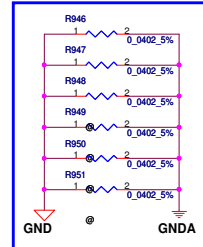
600ohms @100MHz 2A
P/N: SM01000EE00

P/N: SM01000DI00

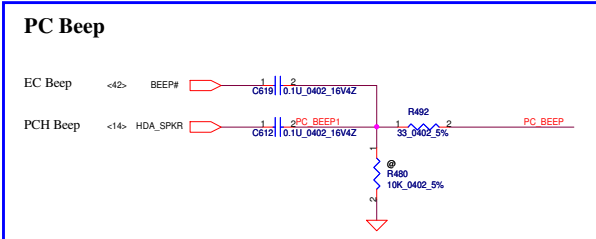
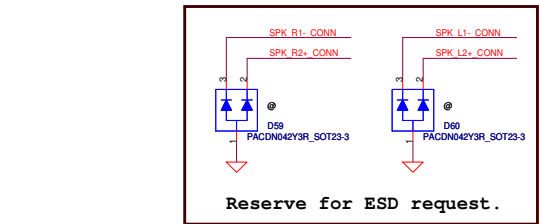
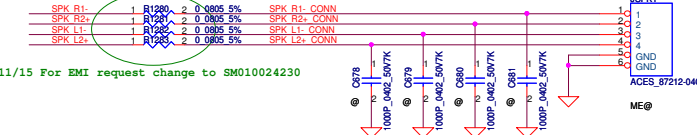
Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

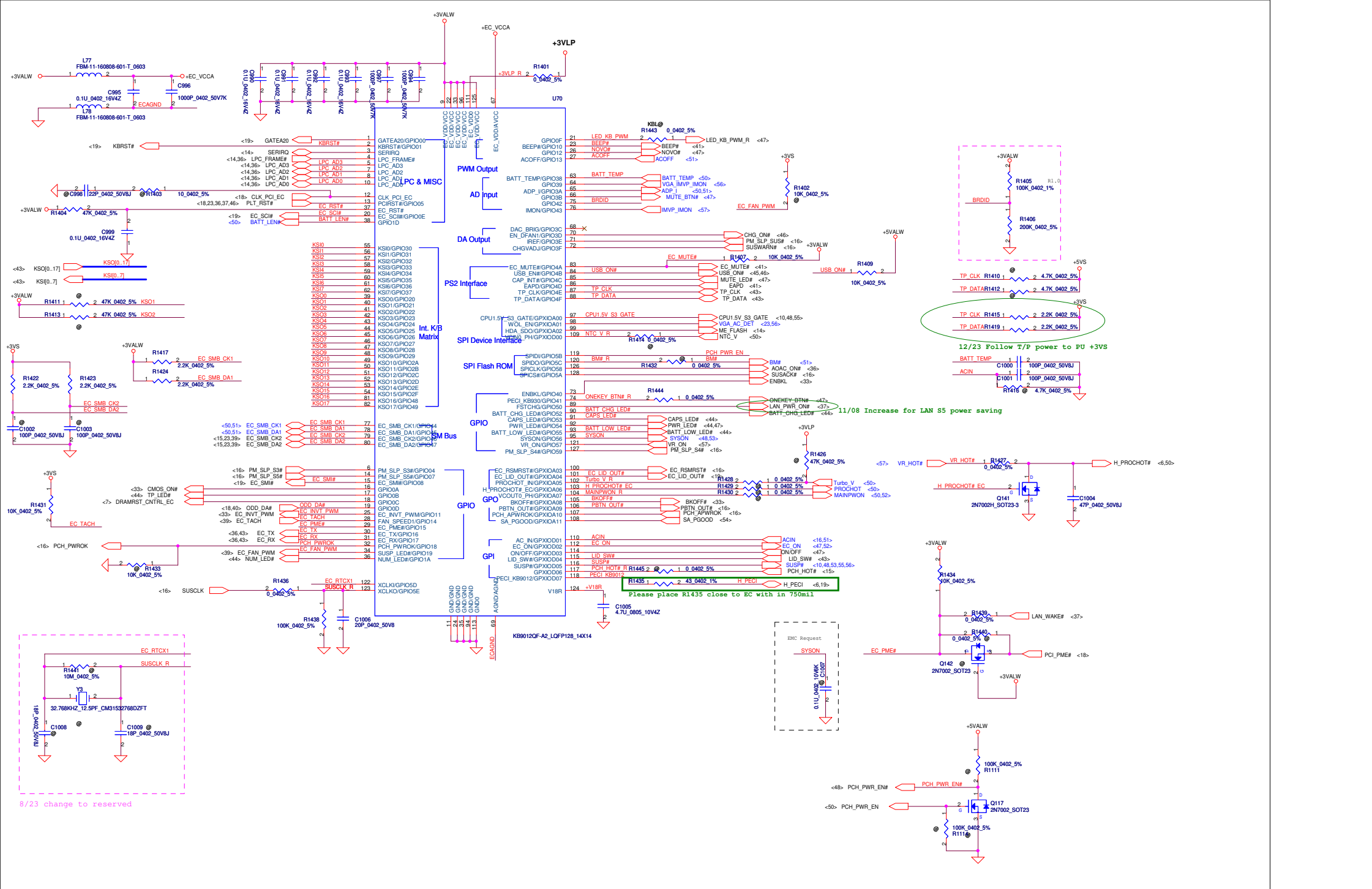


Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in



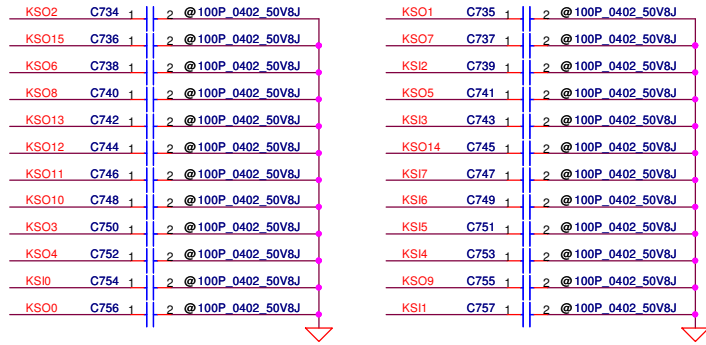
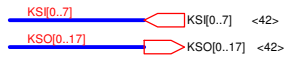
wide 25MIL



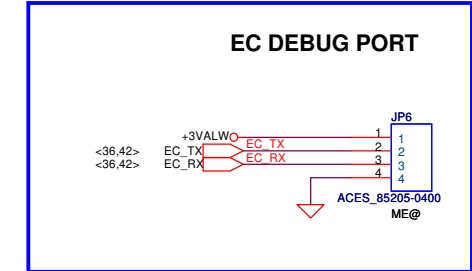
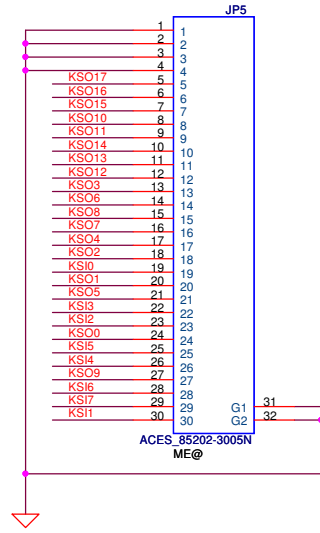


Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	BIOS & EC I/O Port	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HEAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				QIYW4 LA-8002P	Rev 1.0
Date:	Monday, January 16, 2012	ISheet	42	of 64	

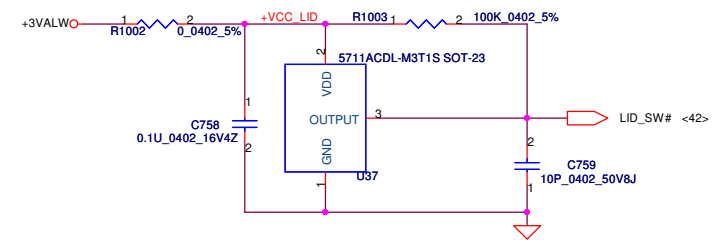
INT_KBD Conn.



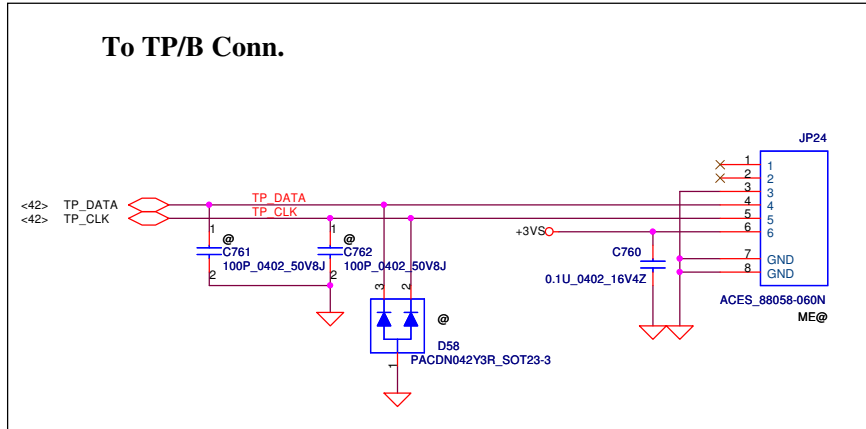
CONN PIN define need double check



Lid Switch

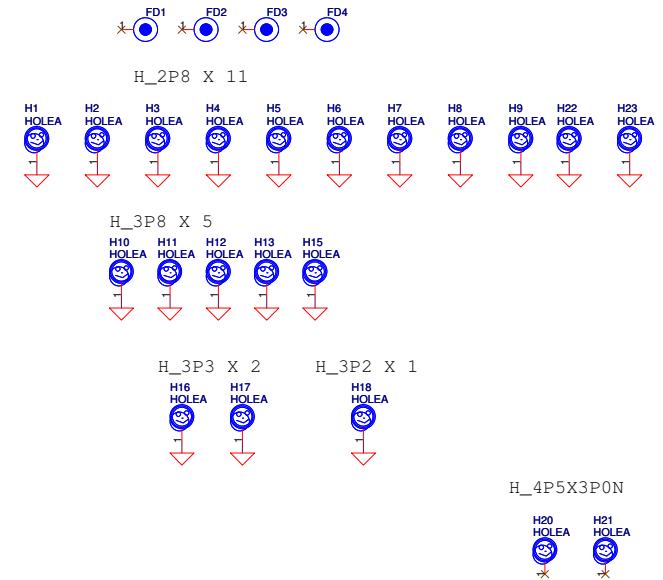
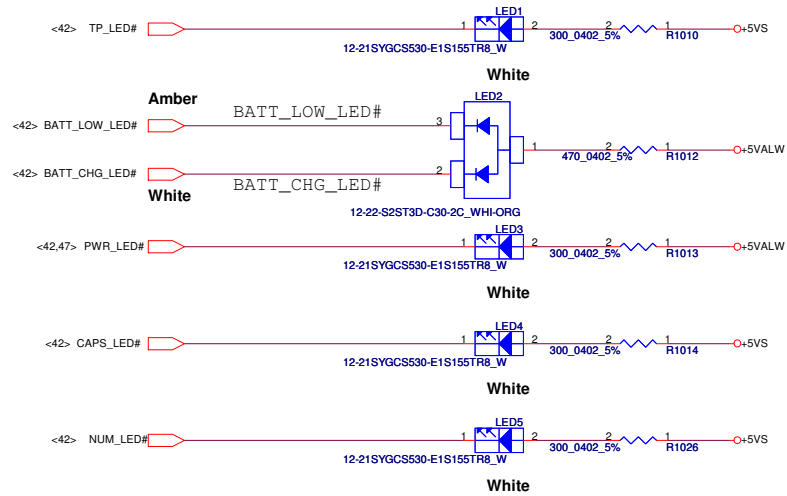


To TP/B Conn.

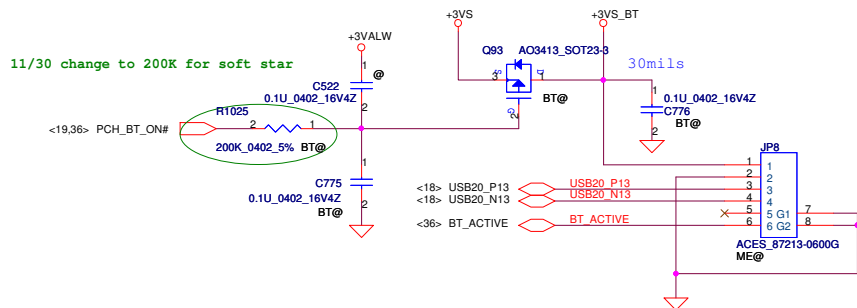


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				KB /SW /LPC Debug Conn.	
Size	Document Number			Rev	
B	QIWIY4 LA-8002P			1.0	
Date:	Monday, January 16, 2012	Sheet	43	of	64

LED



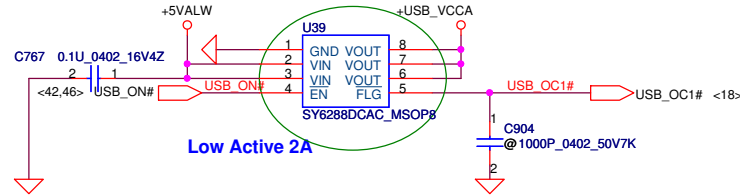
BT MODULE CONN



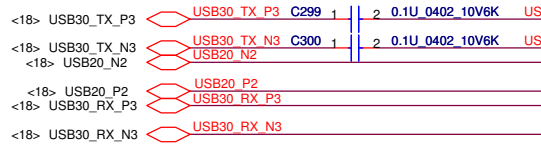
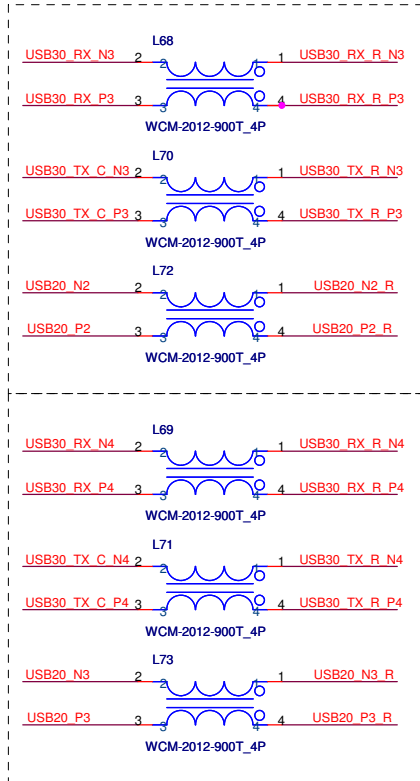
Security Classification		Compal Secret Data		Compal Electronics, Inc. LED/EC SPI ROM/BT	
Issued Date	2011/07/21	Deciphered Date	2012/12/31		
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Rev
				B	1.0
				Date:	Monday, January 16, 2012
				Sheet	44 of 64
				Document Number	QIWIY4 LA-8002P

LEFT SIDE USB3.0 PORT X2

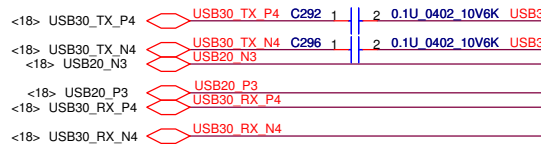
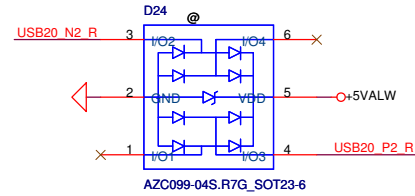
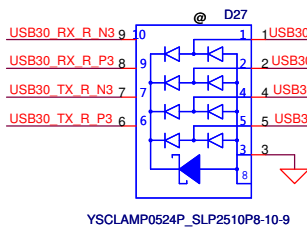
11/07 Change source to SA00004KB00



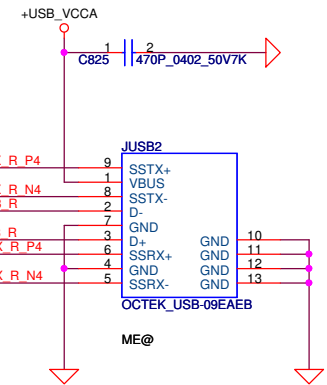
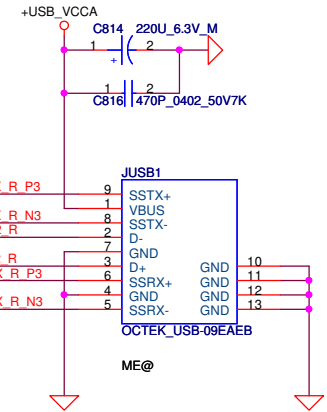
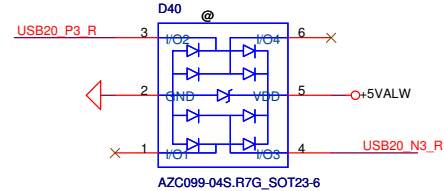
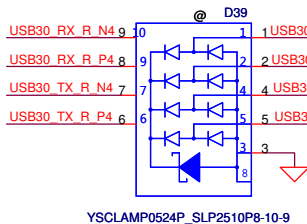
For EMI request
 USB2.0 choke --> SM070000I00
 USB3.0 Choke --> SM070001U00



For ESD request

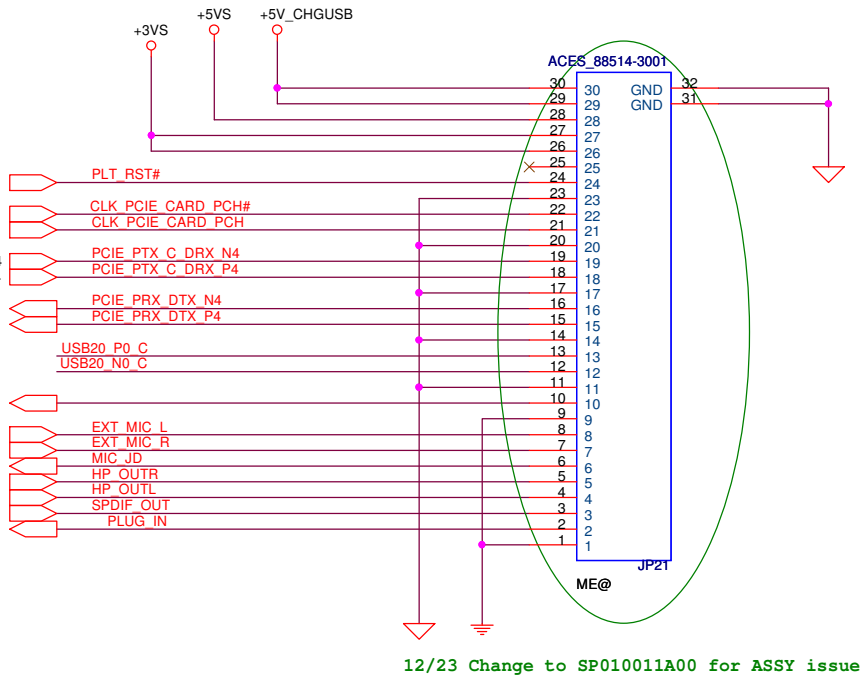
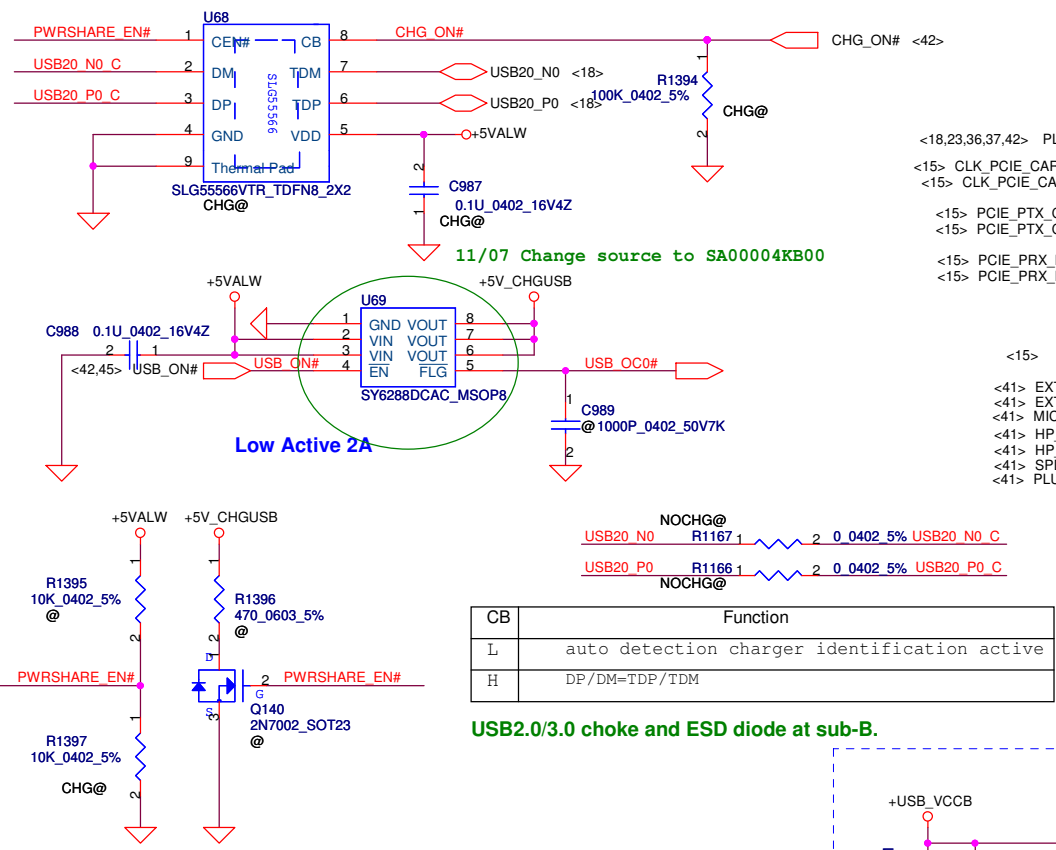


For ESD request

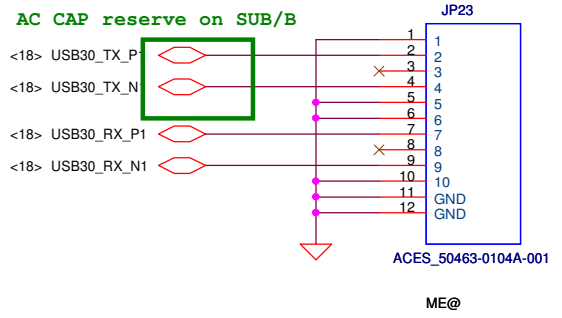


Security Classification		Compal Secret Data For EMI request		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB3.0 ports	
Size	Document Number	Rev		1.0	
Custom	QIWIY4 LA-8002P	Date:		Monday, January 16, 2012	
		Sheet		45 of 64	

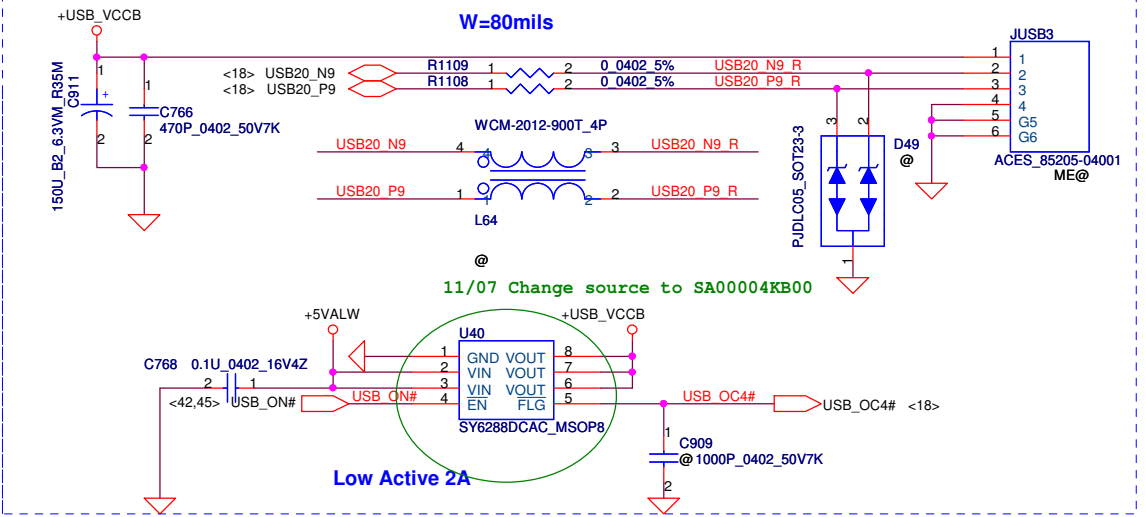
Right side USB Charger



Right side USB3.0 port (Option)

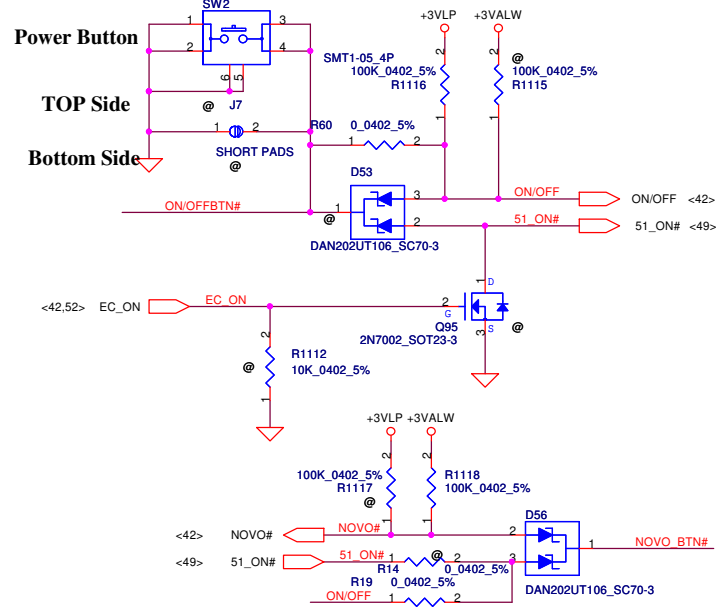


Right USB Conn.(Cable)

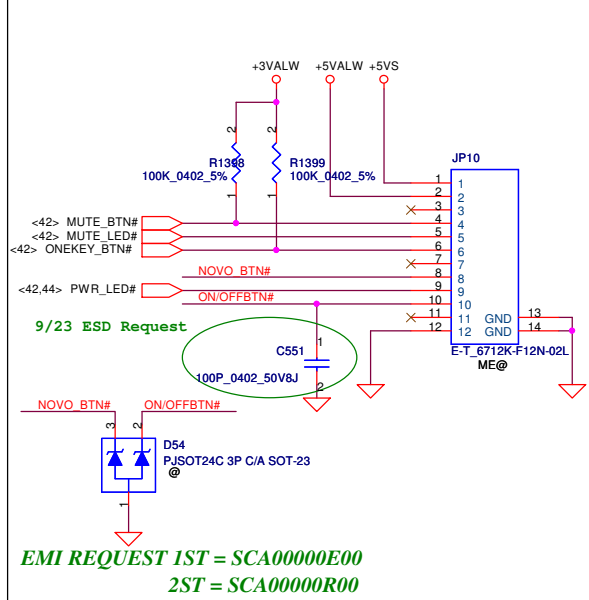


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Audio B Conn/USB charger Document Number QIYW4 LA-8002P Rev 1.0
Date:	Monday, January 16, 2012	Sheet	46 of 64	

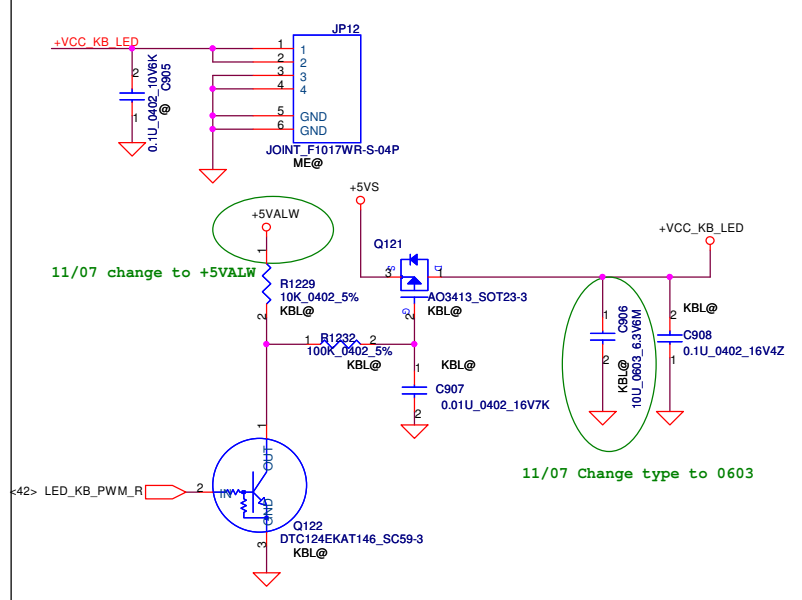
ON/OFF switch



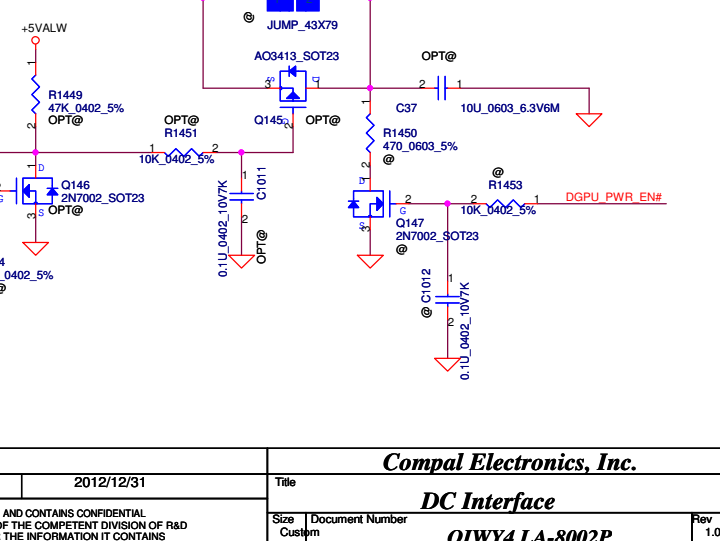
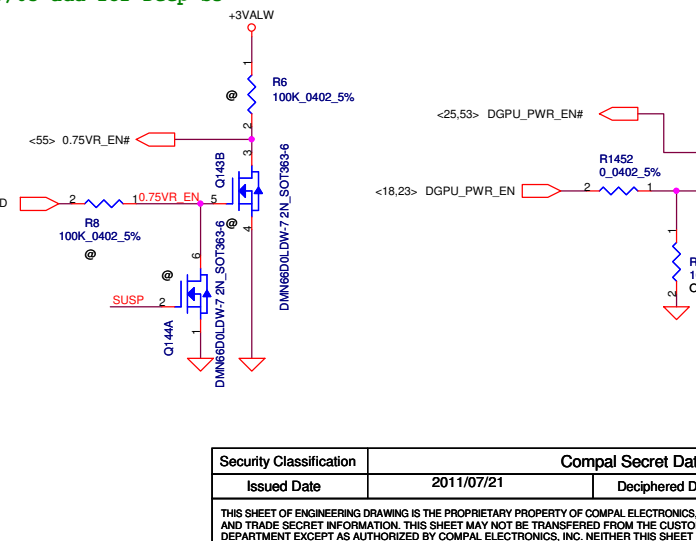
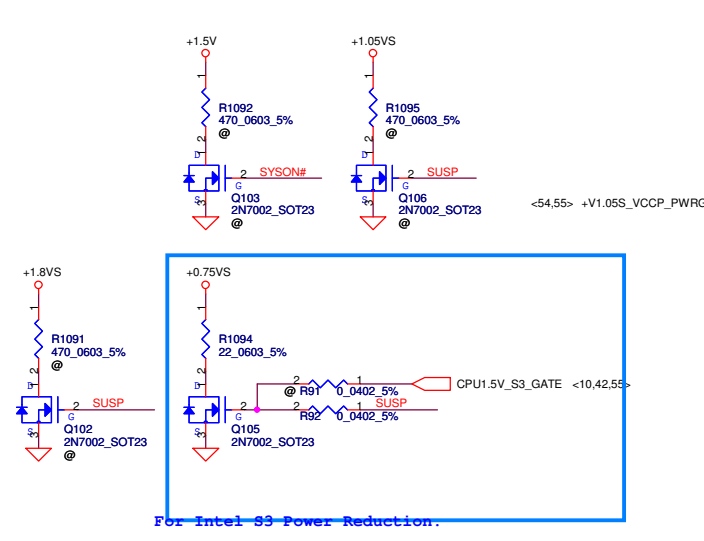
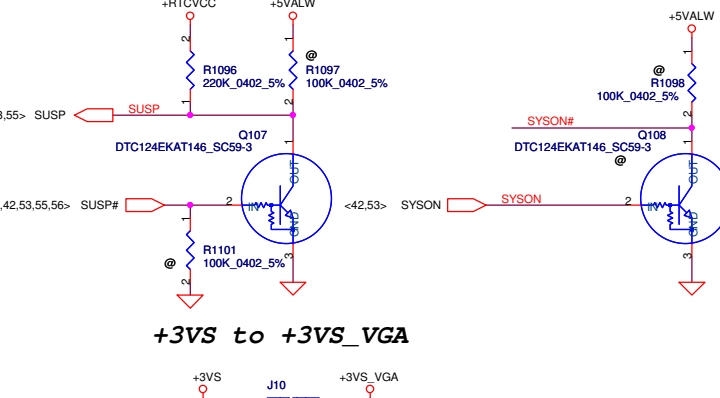
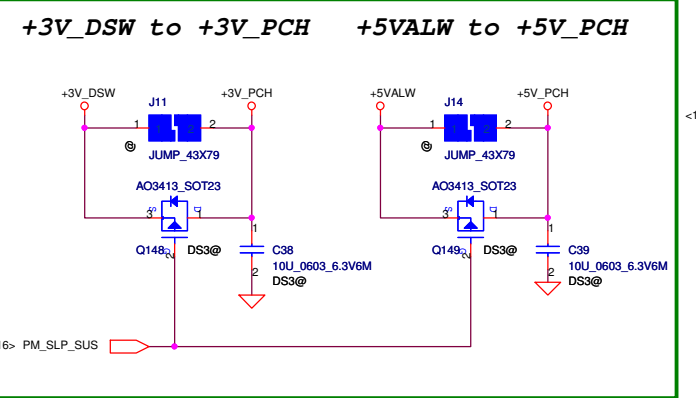
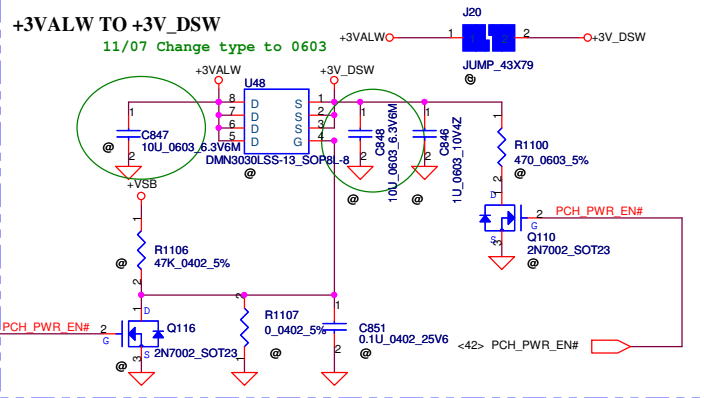
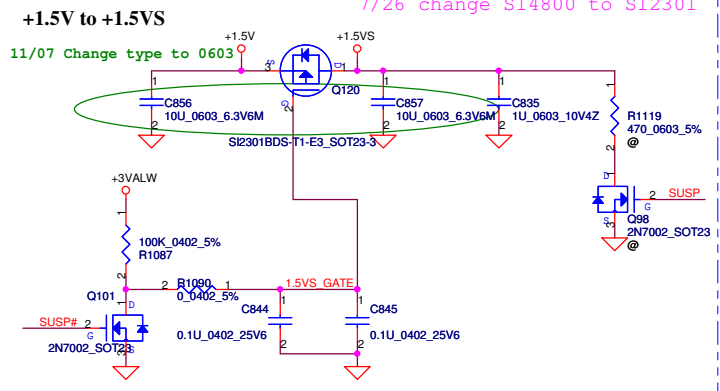
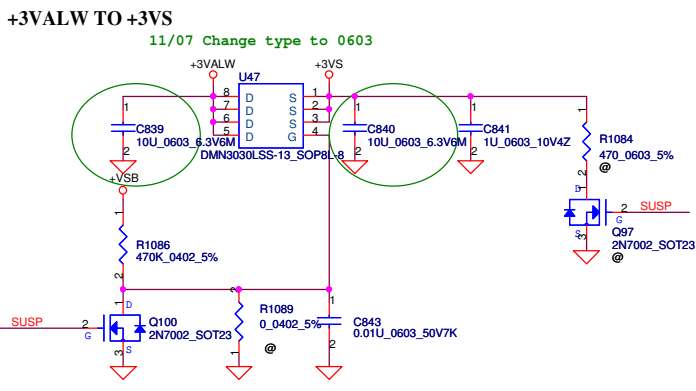
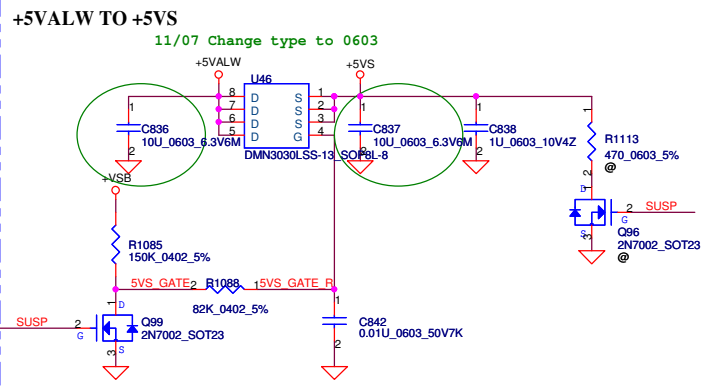
Power Button/B link to Function/B Conn. 10pin



KB Lighting CONN.4pin



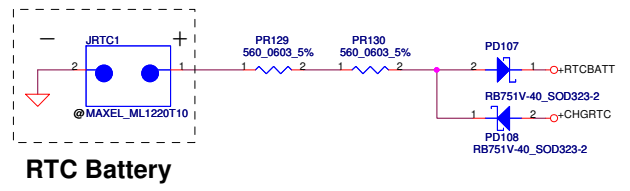
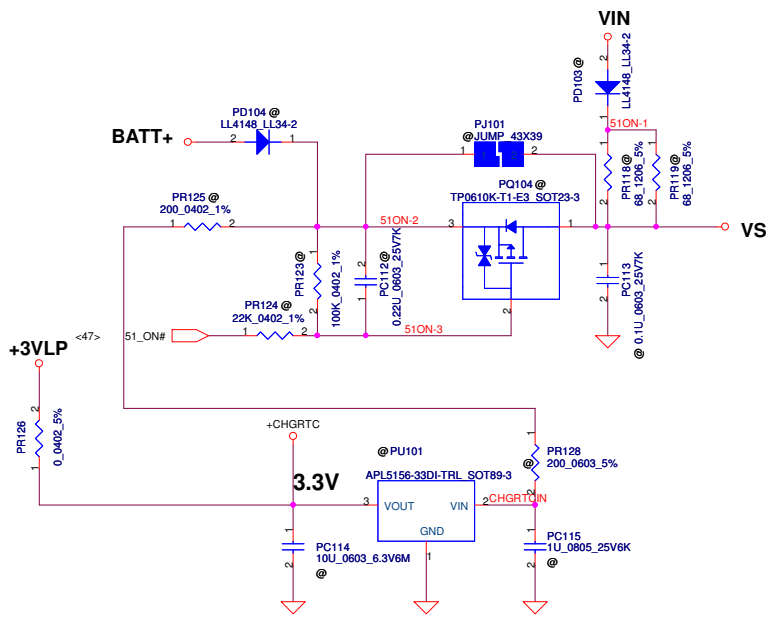
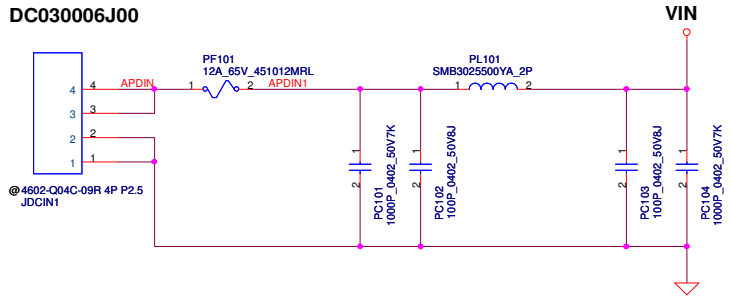
Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Compal Electronics, Ltd.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				other IO connector
				Size Custom
Date: Monday, January 16, 2012		Sheet 47 of 64		



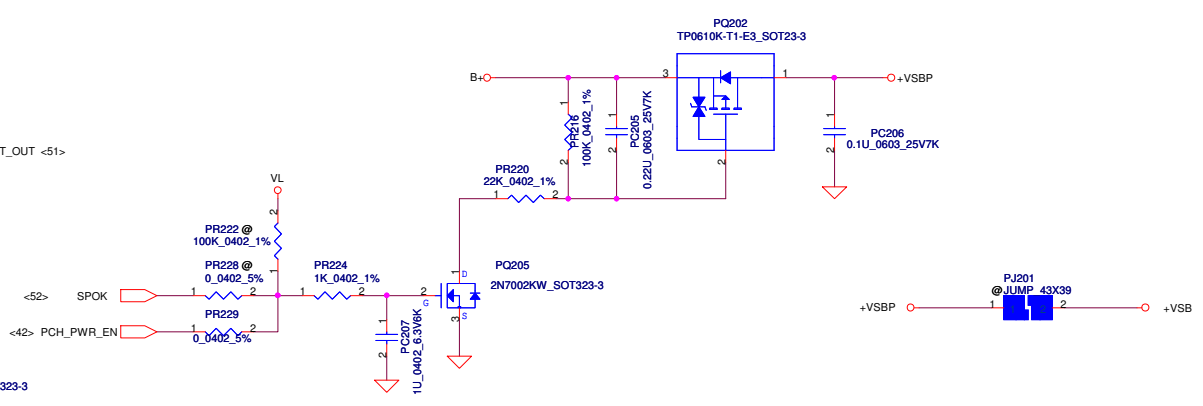
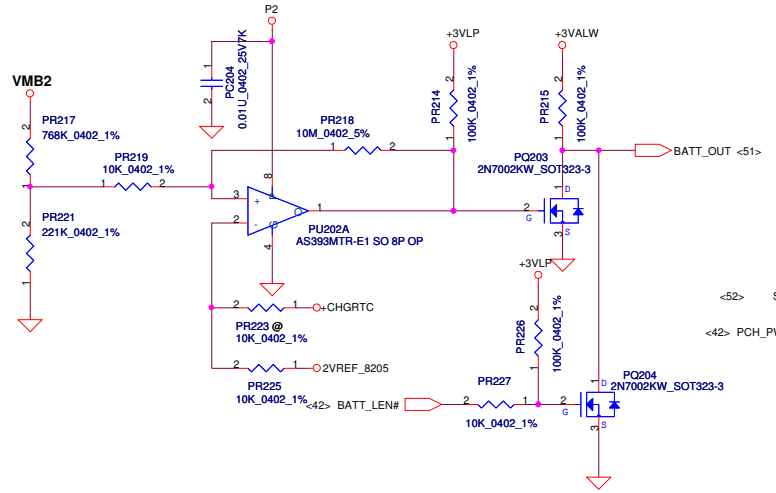
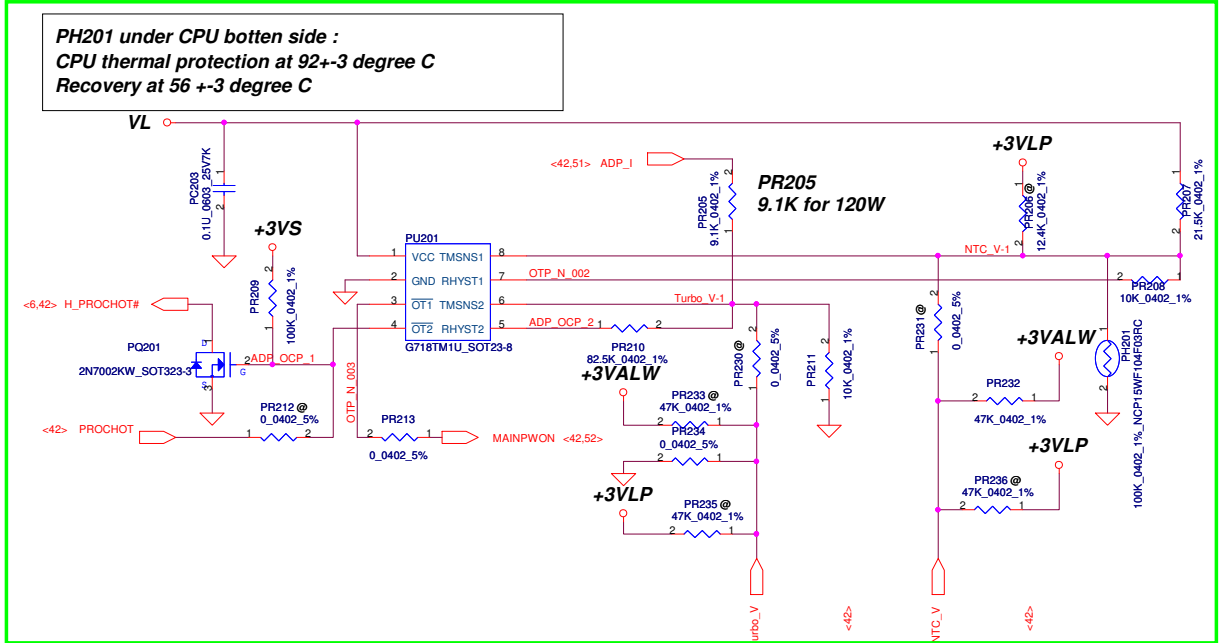
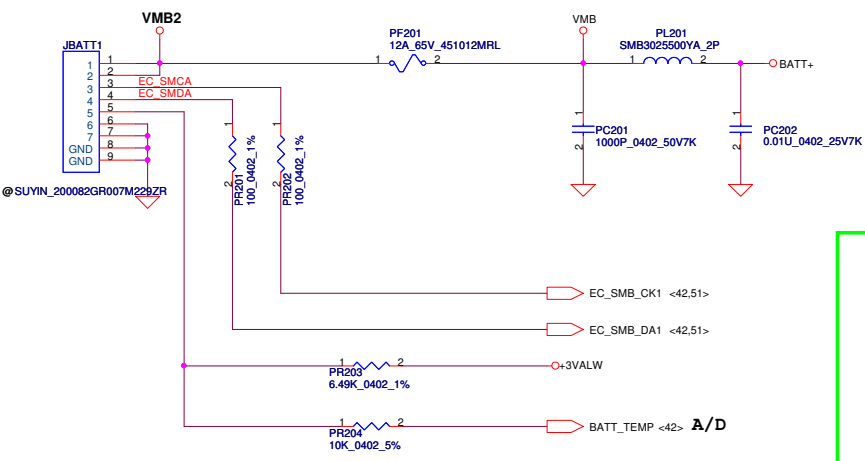
Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Customer
				QIYW4 LA-8002P
Date: Monday, January 16, 2012				Rev 1.0
Sheet 48 of 64				

For Intel® 93 Power Reduction.

DC030006J00



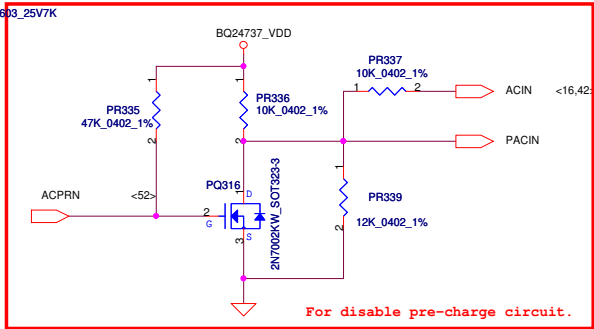
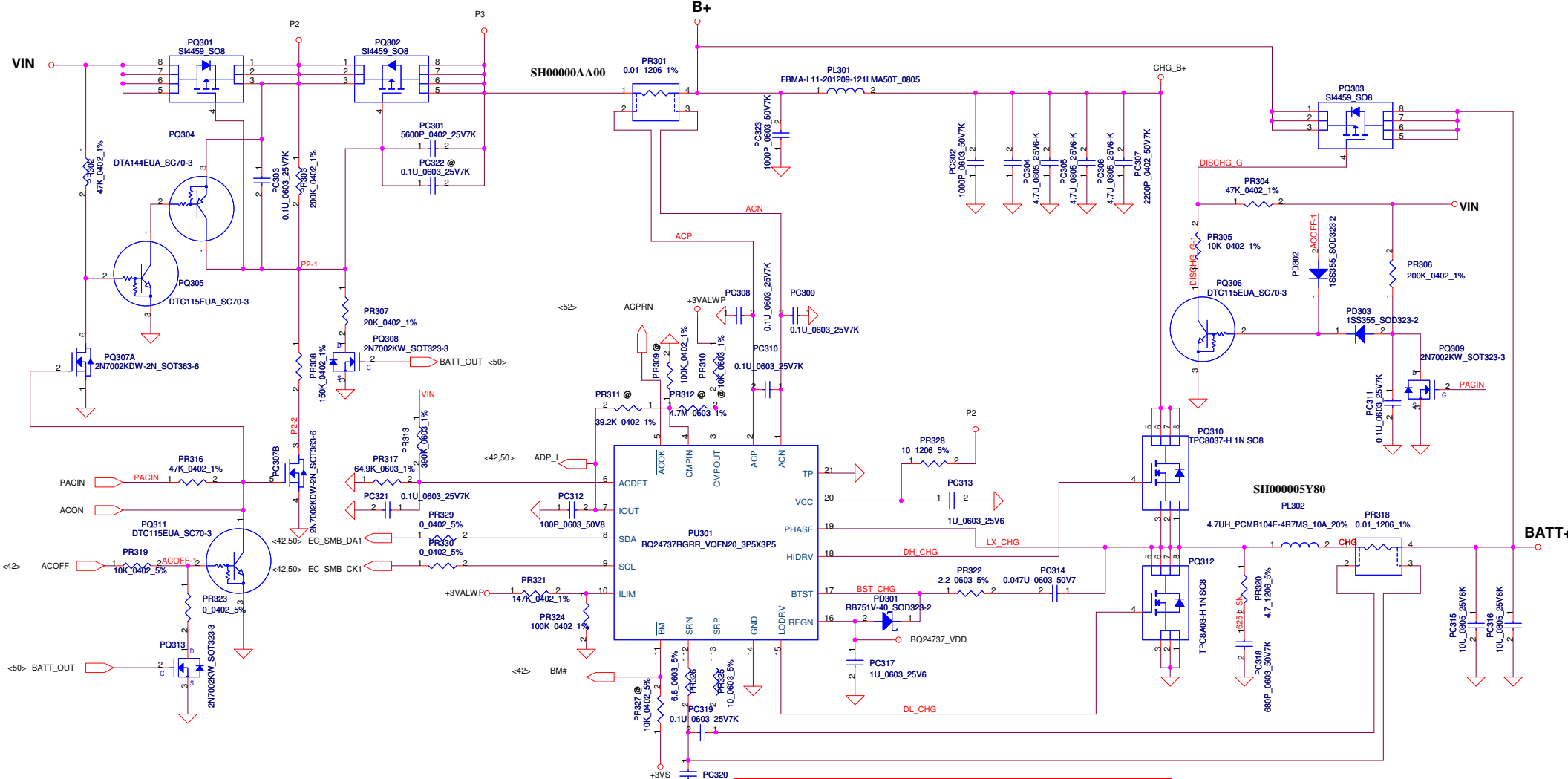
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom Document Number QIWIY4 Rev 1.0
Date: Monday, January 16, 2012				Sheet 49 of 64



Security Classification	Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date
		2012/12/31

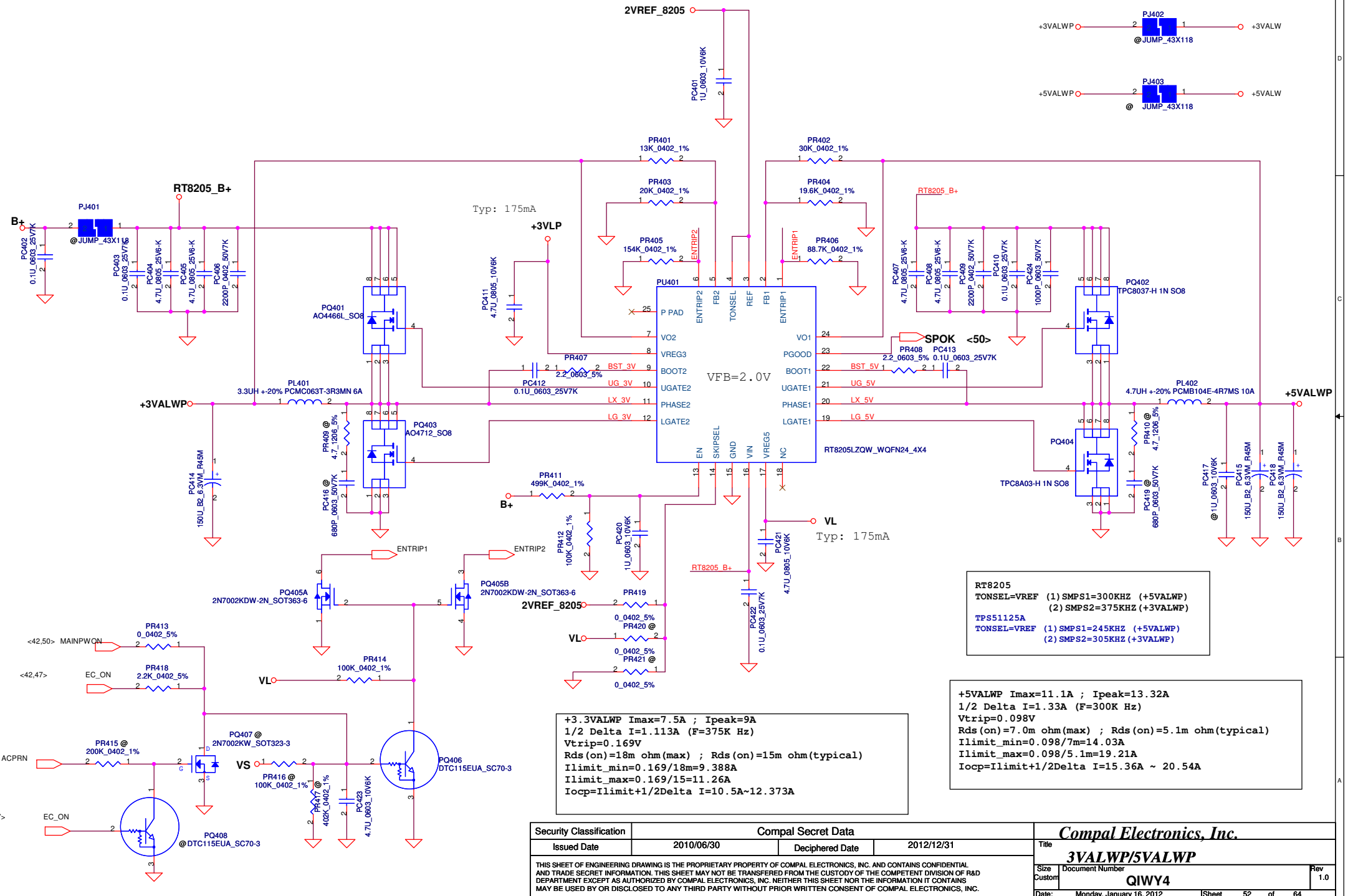
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc. BATTERY CONNIOPT		
Title		
Size	Document Number	Rev
Custom	QIWIY4	1.0
Date:	Monday, January 16, 2012	Sheet 50 of 64



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CHARGER QIYW4
Size	Document Number	Date	Monday, January 16, 2012	Rev 1.0
		Sheet	51 of	64

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)
TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)

+3.3VALWP $I_{max}=7.5A$; $I_{peak}=9A$
 $1/2 \Delta I=1.113A$ ($F=375KHz$)
 $V_{trip}=0.169V$
 $R_{ds(on)}=18m \text{ ohm(max)}$; $R_{ds(on)}=15m \text{ ohm(typical)}$
 $I_{limit_min}=0.169/18m=9.388A$
 $I_{limit_max}=0.169/15m=11.26A$
 $I_{ocp}=I_{limit}+1/2\Delta I=10.5A\sim 12.373A$

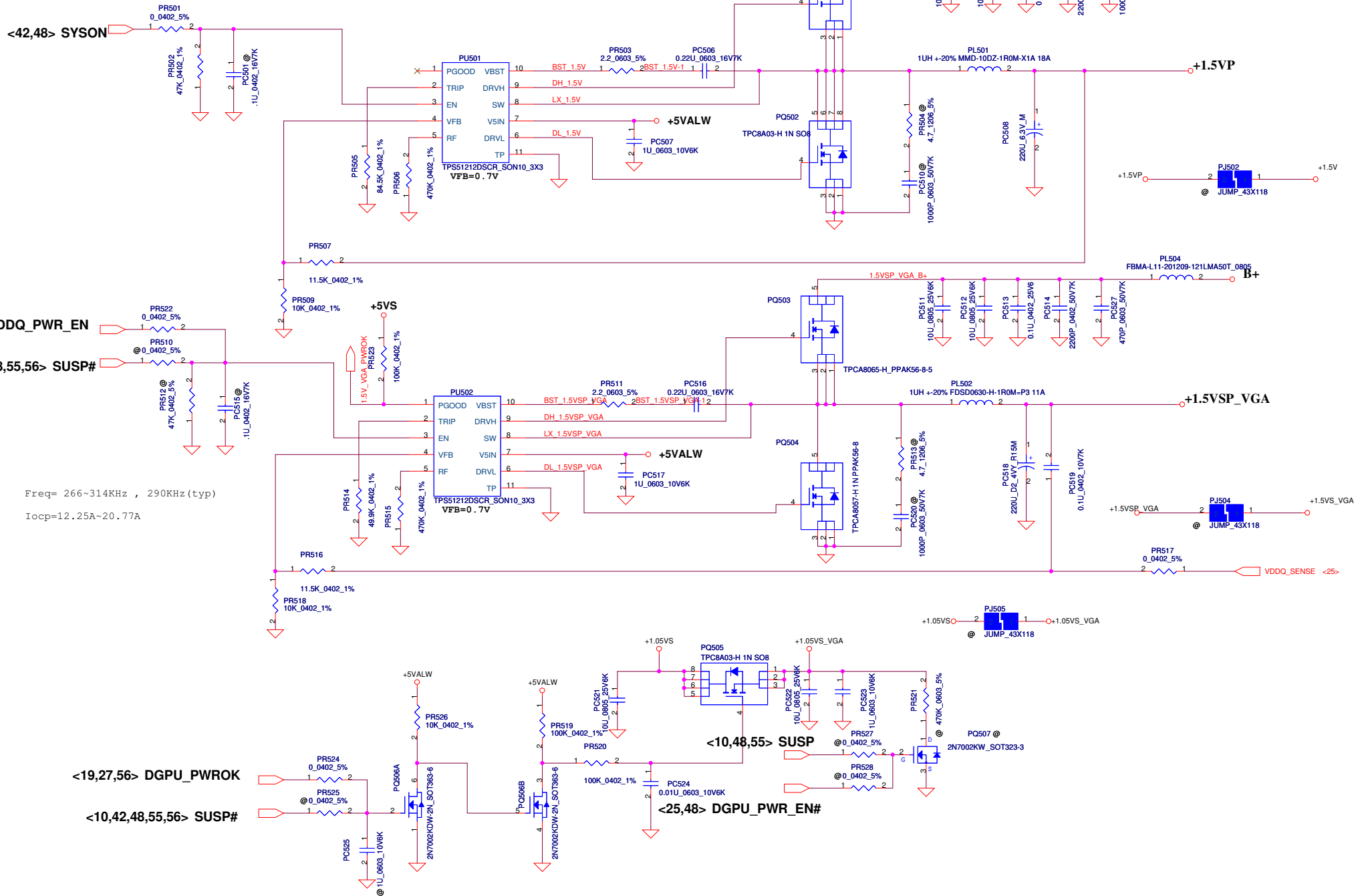
+5VALWP $I_{max}=11.1A$; $I_{peak}=13.32A$
 $1/2 \Delta I=1.33A$ ($F=300KHz$)
 $V_{trip}=0.098V$
 $R_{ds(on)}=7.0m \text{ ohm(max)}$; $R_{ds(on)}=5.1m \text{ ohm(typical)}$
 $I_{limit_min}=0.098/7m=14.03A$
 $I_{limit_max}=0.098/5.1m=19.21A$
 $I_{ocp}=I_{limit}+1/2\Delta I=15.36A \sim 20.54A$

Security Classification		Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date	2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.		
Title	3VALWP/5VALWP	
Size	Document Number	Rev
Custom	QIYW4	1.0
Date:	Monday, January 16, 2012	Sheet 52 of 64

Freq= 266~314KHz , 290KHz(typ)

Iocp=13.58A~23.10A

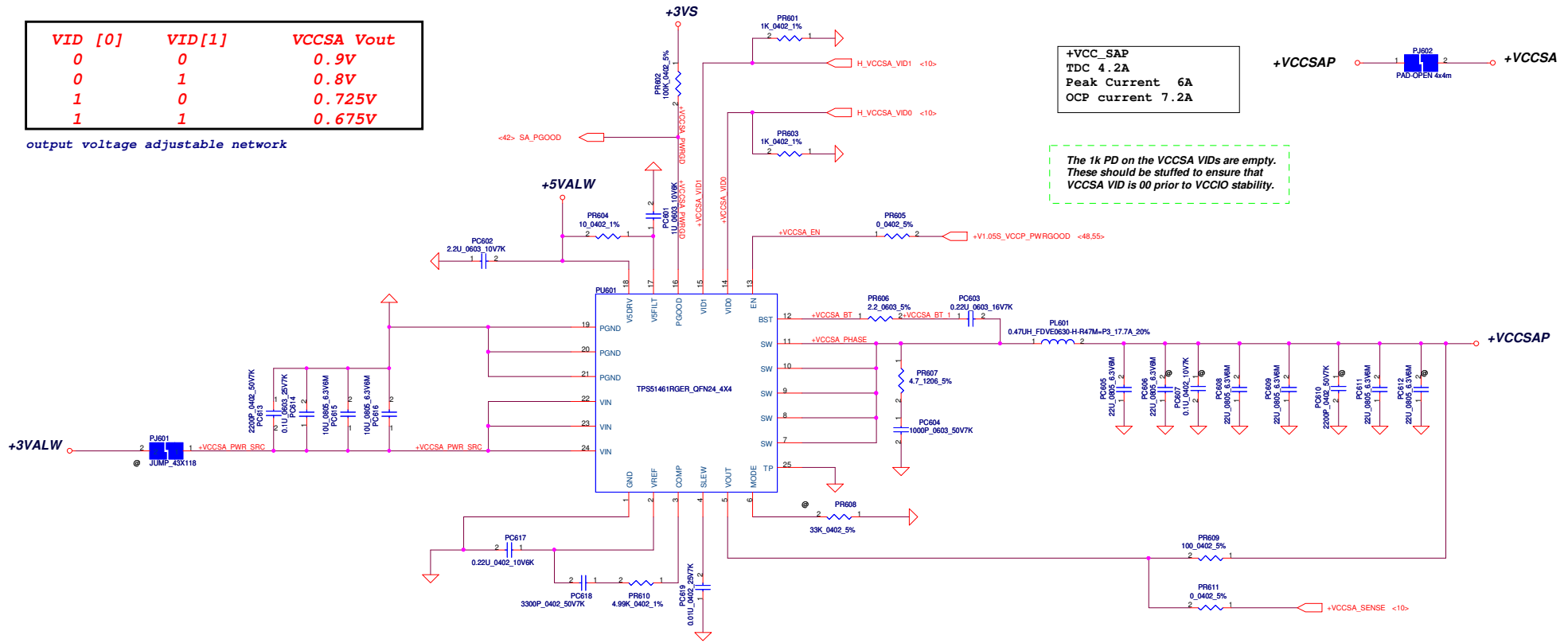


Security Classification		Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date	2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.		
Title 1.5VP/1.5VSP_VGA/1.05VSP_VGA		
Size	Document Number	Rev
Custom	QIWY4	1.0
Date:	Monday, January 16, 2012	Sheet 53 of 64

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

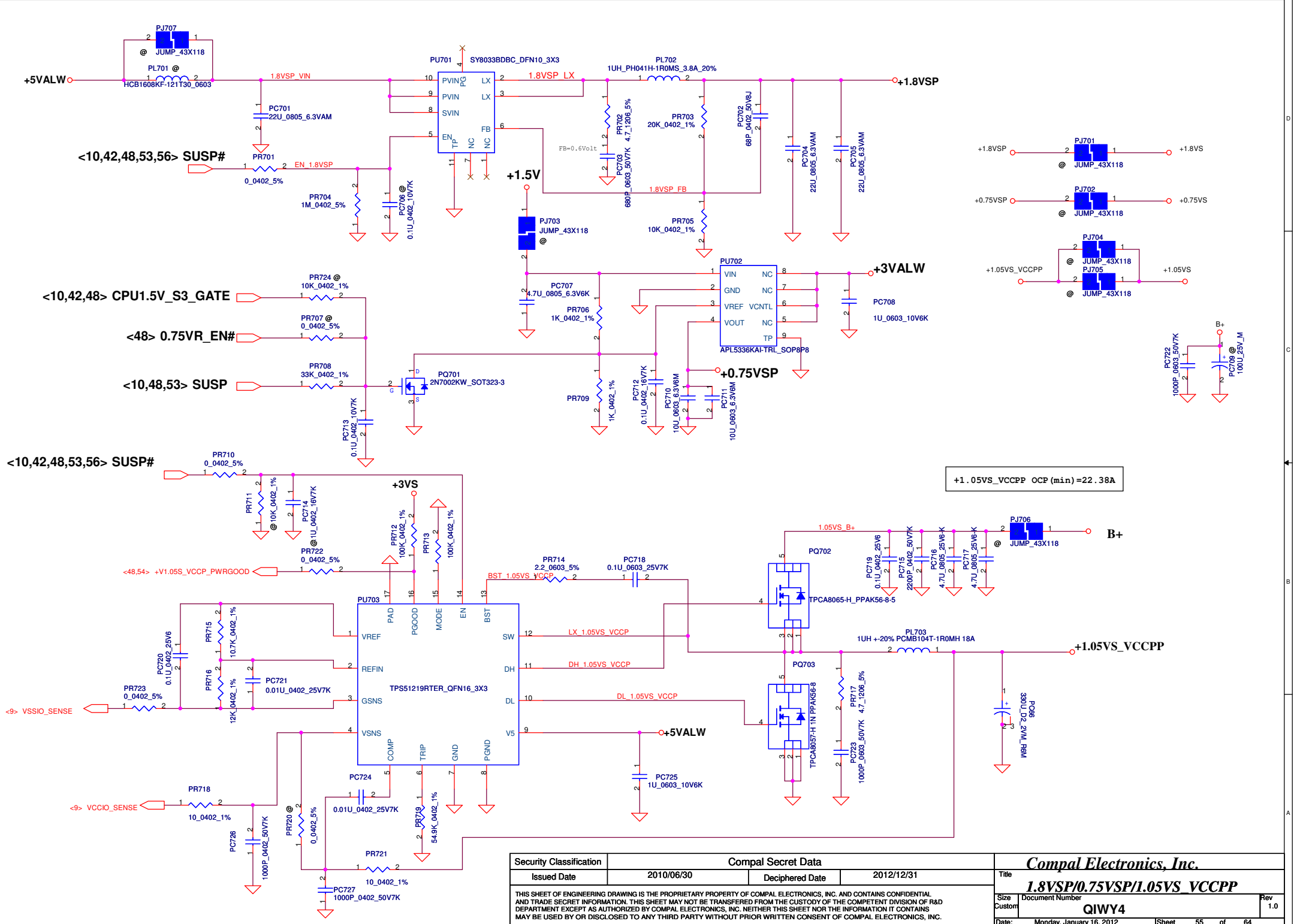
output voltage adjustable network



+VCCSAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

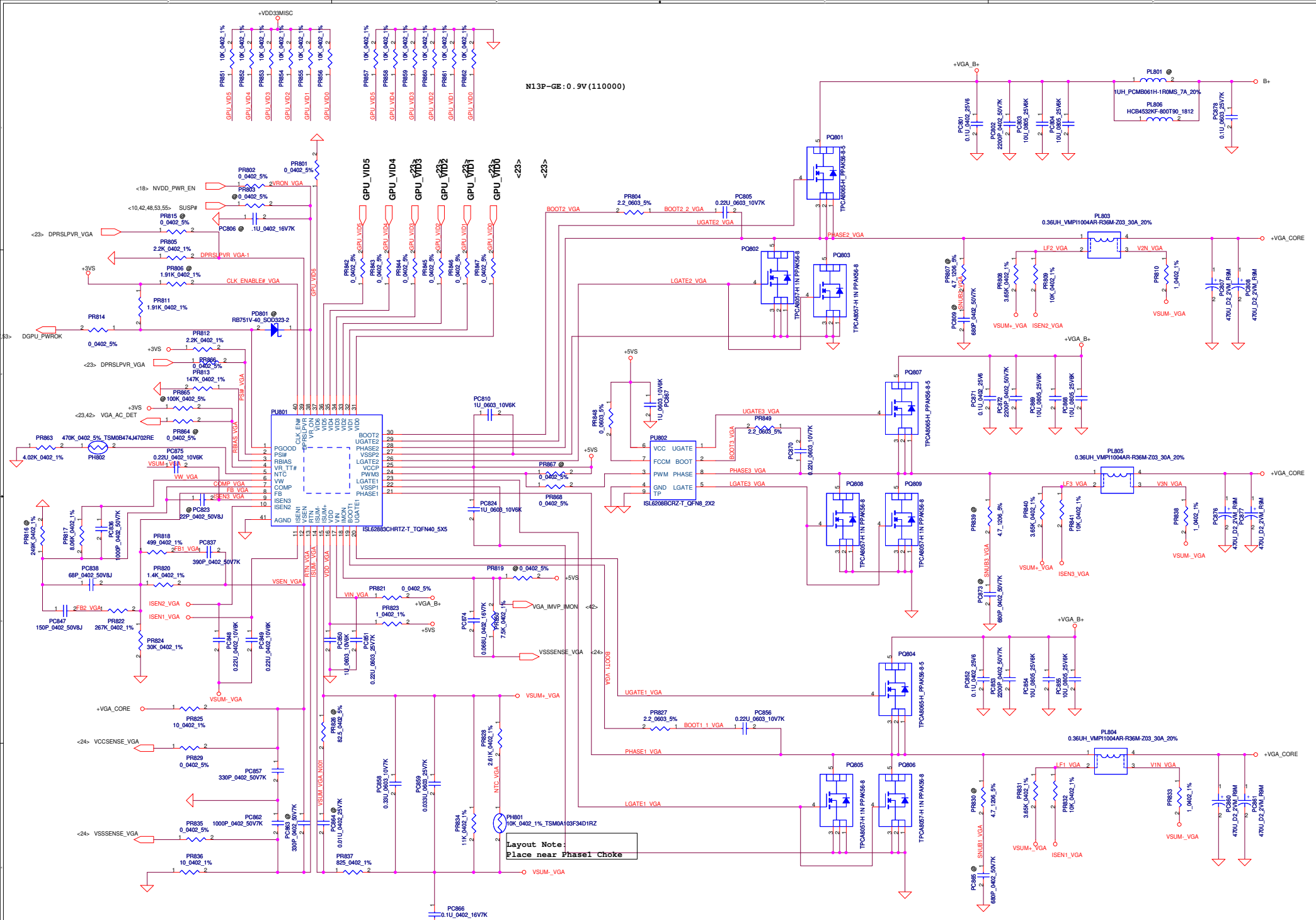


The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Security Classification		Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date	2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

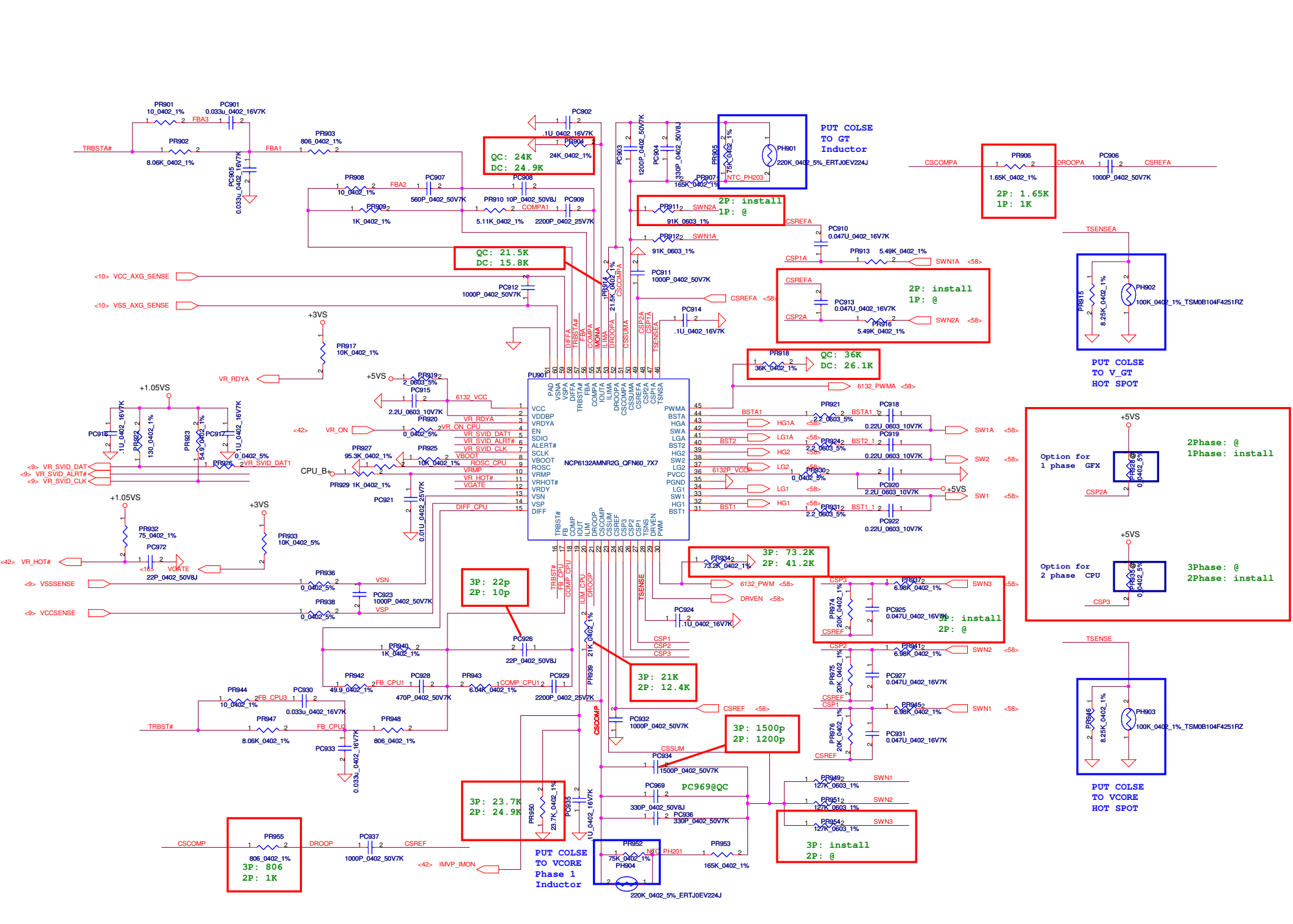
Compal Electronics, Inc. 1.8VSP/0.75VSP/1.05VS_VCCPP		
Title	Document Number	Rev
	QIYW4	1.0
Date:	Monday, January 16, 2012	Sheet 55 of 64



N13P-GE:0.9V (110000)

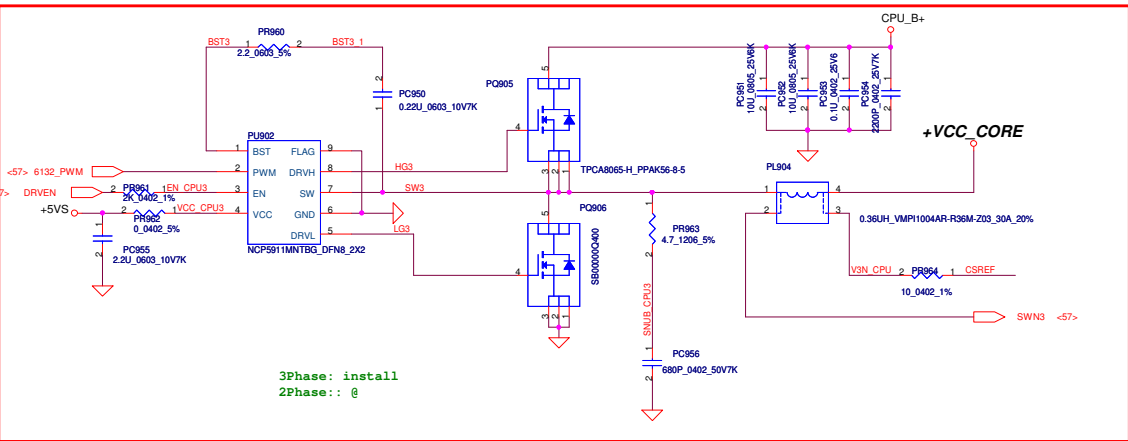
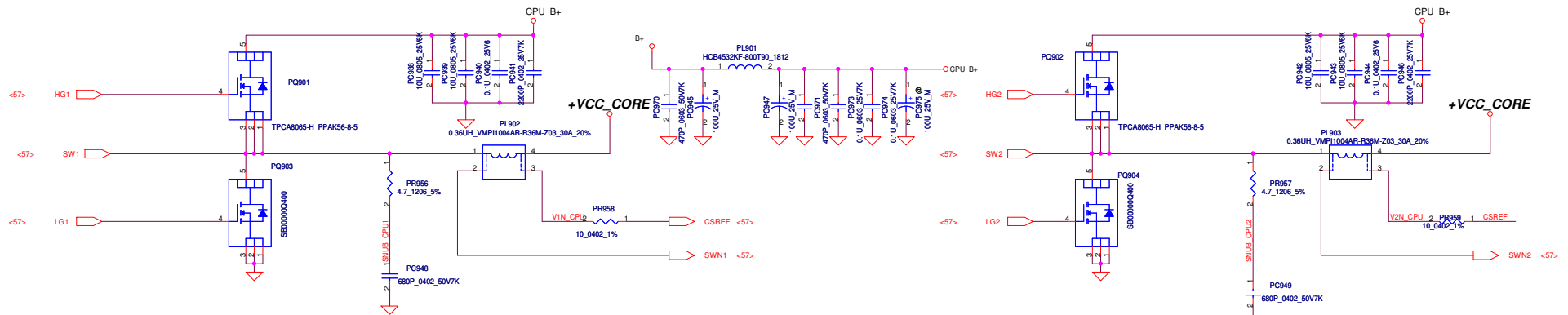
Layout Note:
Place near Phasel Choke

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	VGA_COREP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF SA&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Q1W74 LA-8002P	Rev 1.0
				Date: Monday, January 16, 2012	Sheet 56 of 64



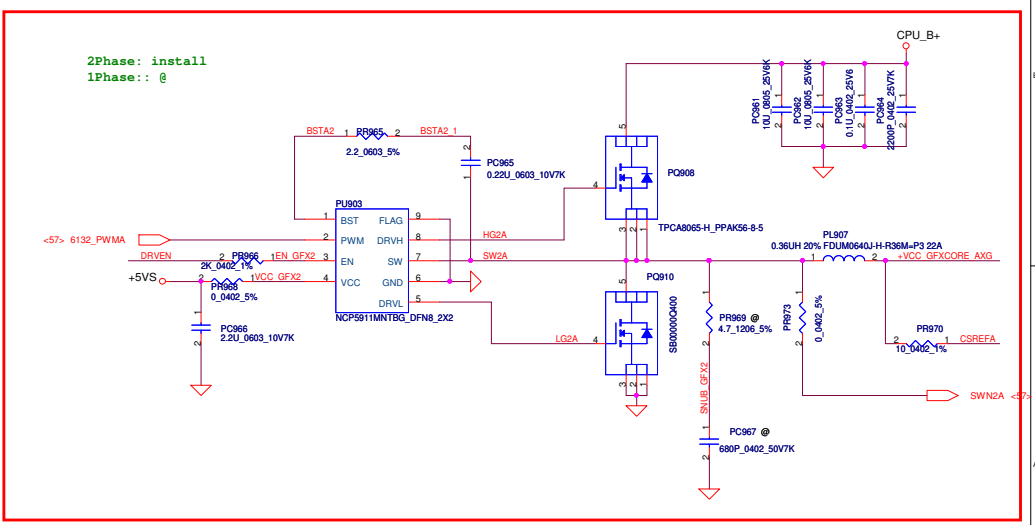
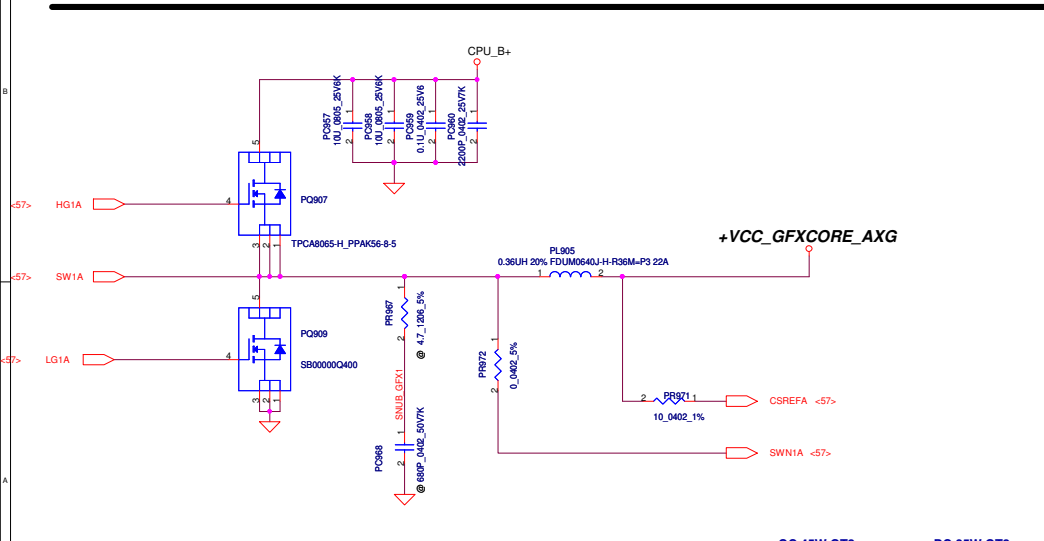
Security Classification		Compal Secret Data	
Issued Date	2011/06/30	Deciphered Date	2012/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

Compal Electronics, Inc.		
Title CPU CORE		
Size Custom	Document Number QIYW4	Rev 1.0
Date	Monday, January 16, 2012	Sheet 57 of 64



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

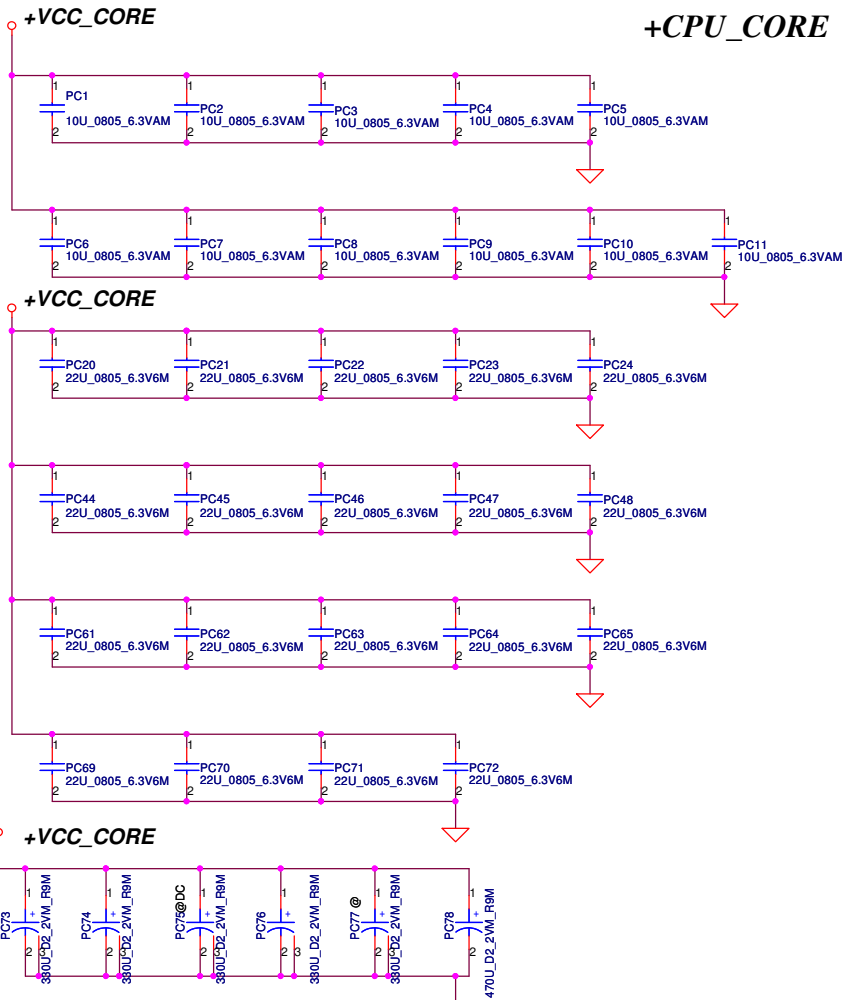
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

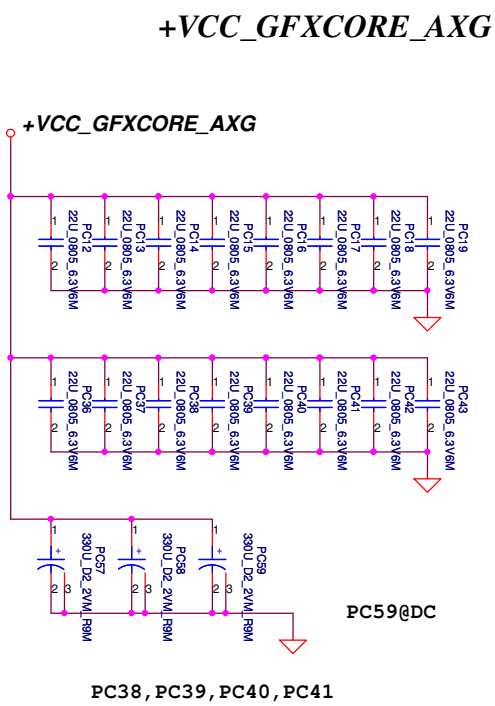
Security Classification	Compal Secret Data		2012/12/31	
Issued Date	2011/06/30	Deciphered Date		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Compal Electronics, Inc. CPU CORE			Title	
Size	Document Number	Rev		
C	QIYW4	1.0		
Date:	Monday, January 16, 2012	Sheet	58	of 64



PC8, PC21, PC22, PC63

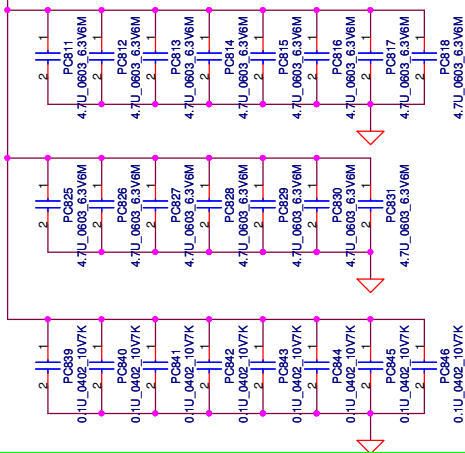
DC: PC73, PC74, PC76 (330uF/9m) + PC78 (330uF/6m)
 QC: PC73, PC74, PC75, PC76 (330uF/9m) + PC78 (470uF/9m)

PC818
 PC825, PC827, PC828, PC829
 PC839, PC841, PC844, PC845



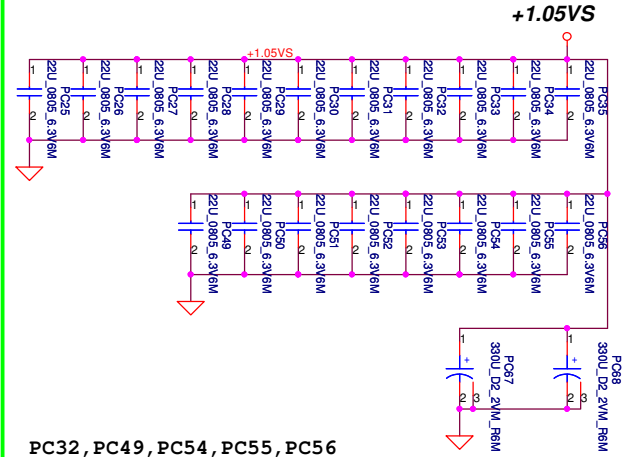
PC38, PC39, PC40, PC41

+VGA_CORE Under VGA Core



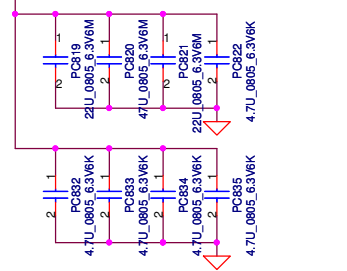
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



PC32, PC49, PC54, PC55, PC56

+VGA_CORE Near VGA Core



Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	2011/09/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470pF)	2011/09/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	2011/09/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	2011/09/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	2011/09/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	2011/09/27	B test
7	for CPU_CORE load line adjust	57	add PC969	2011/09/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	2011/09/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC778	2011/09/27	B test
10	for VGA_CORE Current Balance	56	pop PC875	2011/09/27	B test
11	for debug	51	add PR329,PR330	2011/11/30	C test
12	for VCCIO remote sense	55	add PR723	2011/11/30	C test
13	RC filter to reduce noise	55	add PR721,PC727	2011/11/30	C test
14	VGA_CORE 2 phase or 3 phase option	56	add PR867,PR868	2011/11/30	C test
15	G718 for adapter and OTP	50	pop PC203,PQ201,PR209,PU201,PR213 unpop PR206	2011/11/30	C test
16	for CPU transient	58	change PR911,PR912 to 91K	2011/11/30	C test
17	for EMI Request		add PL301,PC503,PL504,PL801 add PC302,PC323,PC424,PC526,PC722,PC970,PC974	2011/11/30	C test
18	HW request	50 55	reserve connect PCH_PWR_EN for power sequence reserve connect CPU1.5V_S3_GATE for power sequence	2011/11/30	C test
19	for thermal request to reduce temperature	53	change PQ503,PQ504	2011/11/30	C test
20	adjust 1.5VSP_VGA OCP	53	change PR514 to 49.9K	2011/11/30	C test

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)	
Size	Document Number	Rev		1.0	
Custom	QIWW4				
Date:	Monday, January 16, 2012	Sheet	60	of	64

QIWI4 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- EVT TO DVT				
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457, R1455, R1447	Reserve SUSACK#, SUSWARN#, SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118, R1120, R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8, Q104, C533, C526, R436	Reserve for AOAC function
7		P36	Change JP1 pin2, 24, 52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18, 71, 72, 126, 128)	For DeepS3/AOAC function
9		P48	Reserve J11, J14, Q148, Q149, C38, C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For DfX issue
11		P46	change U40, U69 symbol (without GND pad)	For DfX issue
12		P47	change JP10 type to SP01001B800	For DfX issue
13		P43	change JP24 type to SP010010T00	For DfX issue
14		P19	Reserve R207, R224 to contact WLAN wake even	Reserve for AOAC function
15		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
16		P23	Change CV37, CV38 to 22P	For Crystal EA request
17		P37	Change C968, C969 to 33P	For Crystal EA request

----- DVT TO PVT				
1		P14	Change power source to +5VS (Q10 pin 2)	Follow intel Design Guide
2		P16	Reserve R257 PU 10K to +3V_DSW	For Deep S3 function
3		P40	Change R1110 to 200K, C638 to 0.1u	For ODD soft star
4		P10	Change C124, C125, C126, C127, C130 to 0603 type	For common design
5		P20	Change C215, C221, C395 to 0603 type	For common design
6		P21	Change C231 to 0603 type	For common design
7		P33	Change C519 to 0603 type	For common design
8		P36	Change C568, C569 to 0603 type	For common design
9		P37	Change C937, C954, C953 to 0603 type	For common design
10		P39	Change C986 to 0603 type	For common design
11		P40	Change C634, C635, C639 to 0603 type	For common design
12		P41	Change C655 to 0603 type	For common design
13		P48	Change C836, C837, C839, C840, C847 C848, C856, C857 to 0603 type	For common design
14		P47	Change C906 to 0603 type	For common design
15		P47	Modify gate powr rail of MOS to +5VALW	Avoid leakage issue.
16		P45	Change U39 source to SA00004KB00	For main source issue
17		P46	Change U40, U69 source to SA00004KB00	For main source issue
18		P37	Add Q150, R145, C976	For LAN power control
19		P42	Reserve LAN_PWR_ON# net on EC pin 89	For LAN power control
20		P41	Stuff R945, R481 for EAPD contact U8 pin29	For MUTE_LED issue
21		P38	Add R90	For LAN SURGE CO-LAY
22		P38	Add R1380	Atheros request

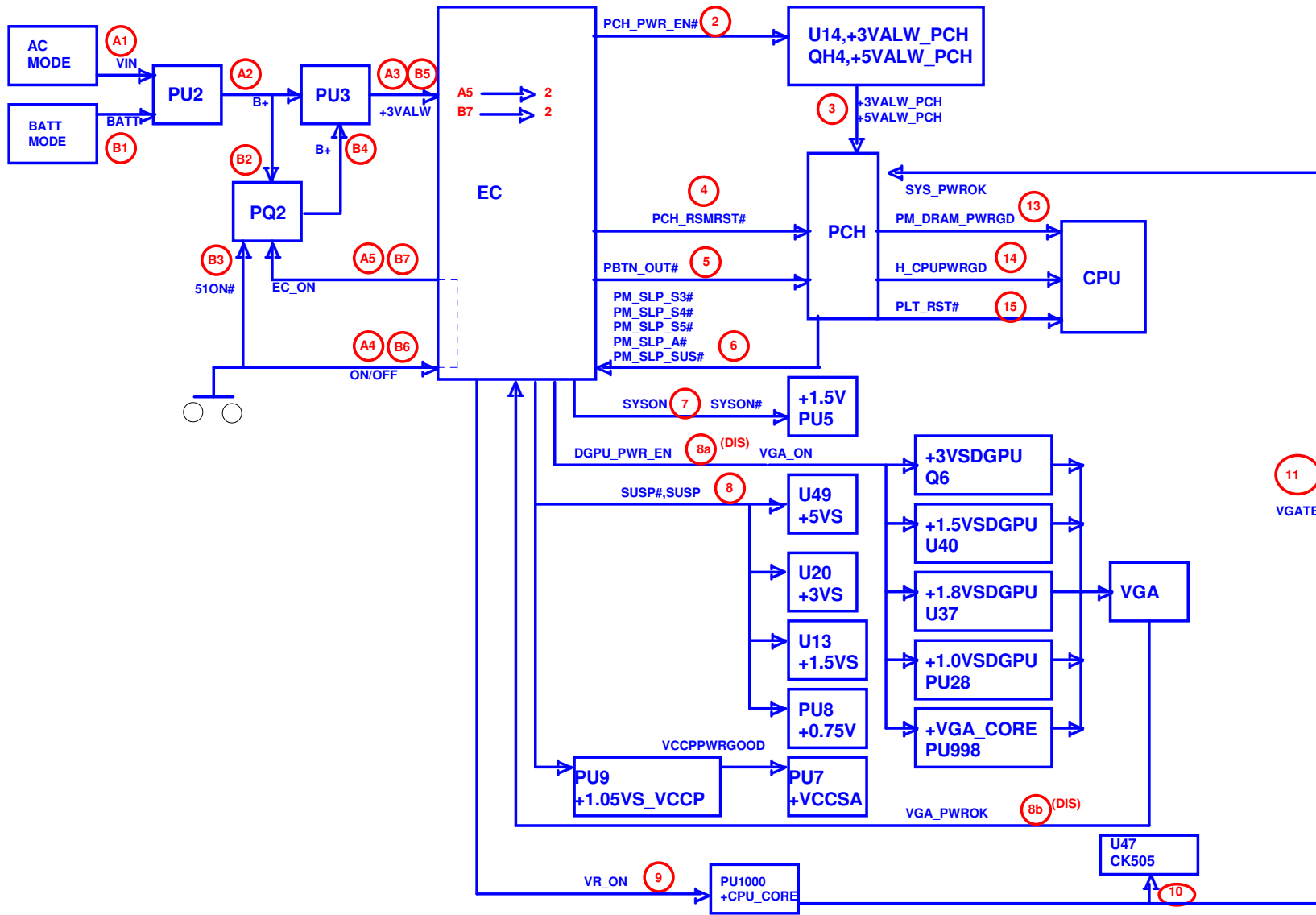
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (HW)	
Size	Document Number	Rev		1.0	
Custom	LA-6882P				
Date:	Monday, January 16, 2012	Sheet	62	of	64

QIWIY4 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1		P46	change JP21 type (SP010011A00)	For ASSY issue
2		P23	RV208 change to contact +VDD33MISC	For N13P-GT/N13E-GE shutdown issue
3		P23	Reserve RV14	For N13P-GT/N13E-GE +VDD33MISC leakage issue
4		P41	Swap HP R/L	For HP R/L reverse issue
5		P42	Add R1415, R1419	T/P SM BUS pull high voltage change

PVT TO SVT

Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	PIR (HW)	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size Custom	Document Number LA-6882P
				Date:	Monday, January 16, 2012
				Sheet	63 of 64
				Rev	1.0



Security Classification	Compal Secret Data			Compal Electronics, Inc. Power sequence		
Issued Date	2011/07/21	Deciphered Date	2012/12/31			
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Document Number	Rev
				Customer	QIWIY4 LA-8002P	1.0
				Date:	Monday, January 16, 2012	Sheet 64 of 64