

Compal Confidential

NIWE2

Schematics Document

Arrandale

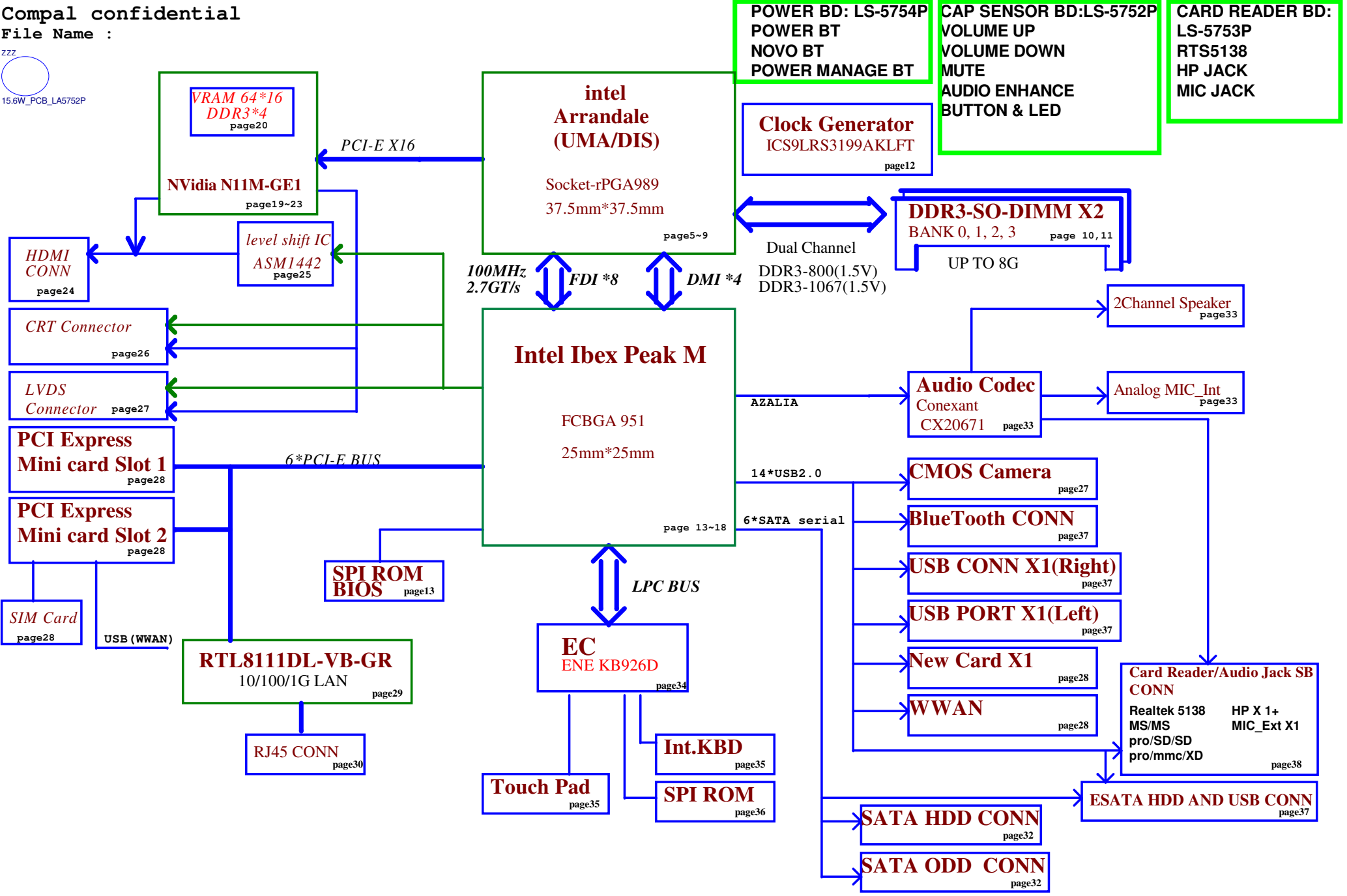
with Intel IBEX PEAK-M core logic

REV: 0.3

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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				Custom	LA-5752P	0.3
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15.6W_PCB_LA5752P



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Issued Date	2008/03/24	Deciphered Date	2008/04/	Compal Electronics, Inc.		
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MB Block Diagram

DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
				State
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
10M@	FOR 10M CHIP	
11M@	FOR 11M CHIP	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
VGA@	FOR NVIDIA PART	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arrandale (dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale (iGPU) UMA only	UMA@ / 100@ for EVT
Arrandale (iGPU+dGPU) SWITCHABLE	VGA@+HD@+HU@+HYBRID@

PCIe PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0, 10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

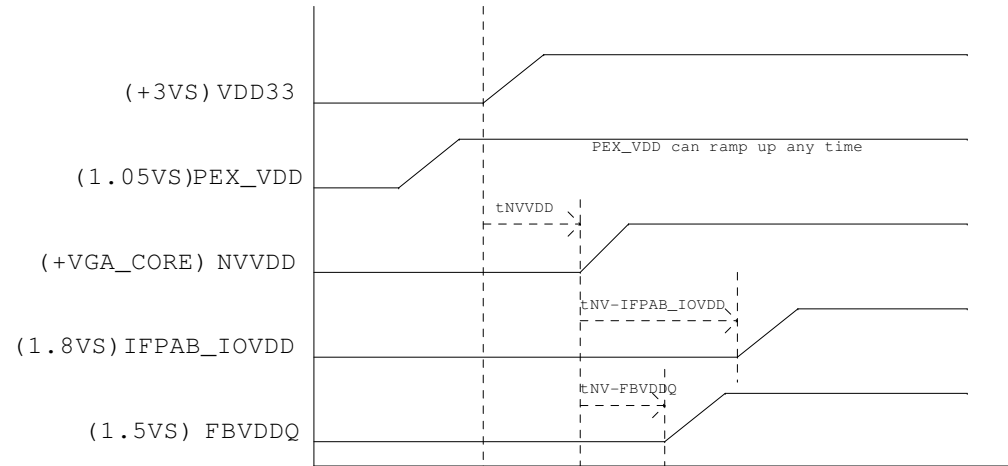
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

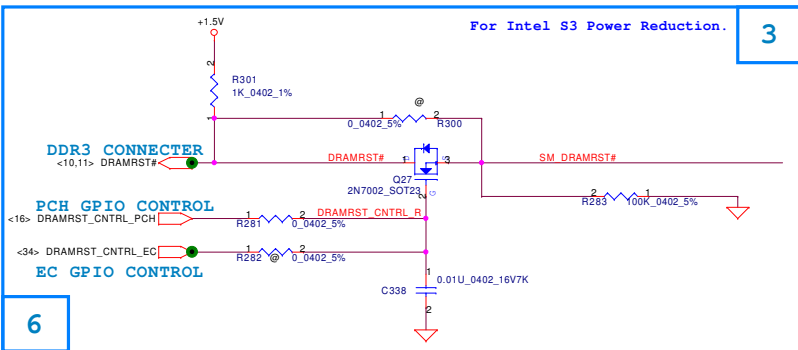
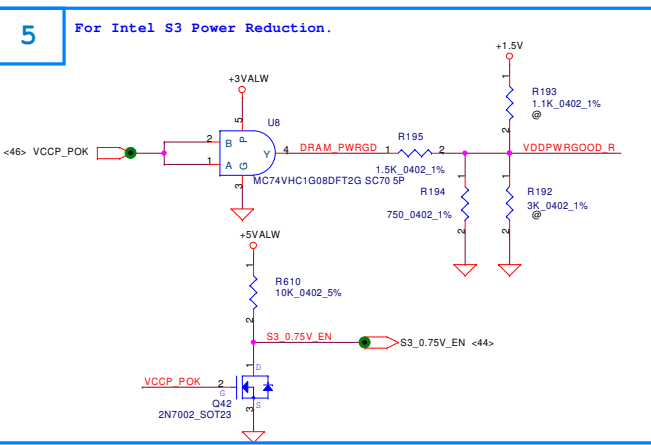
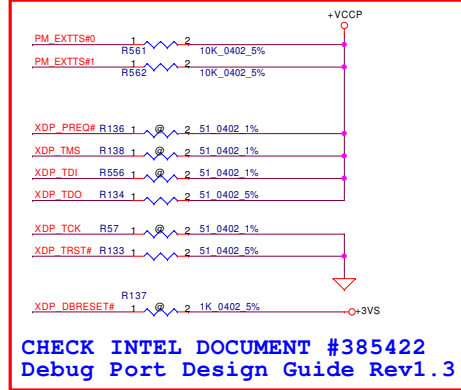
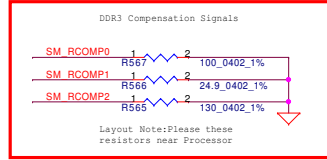
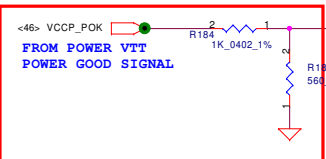
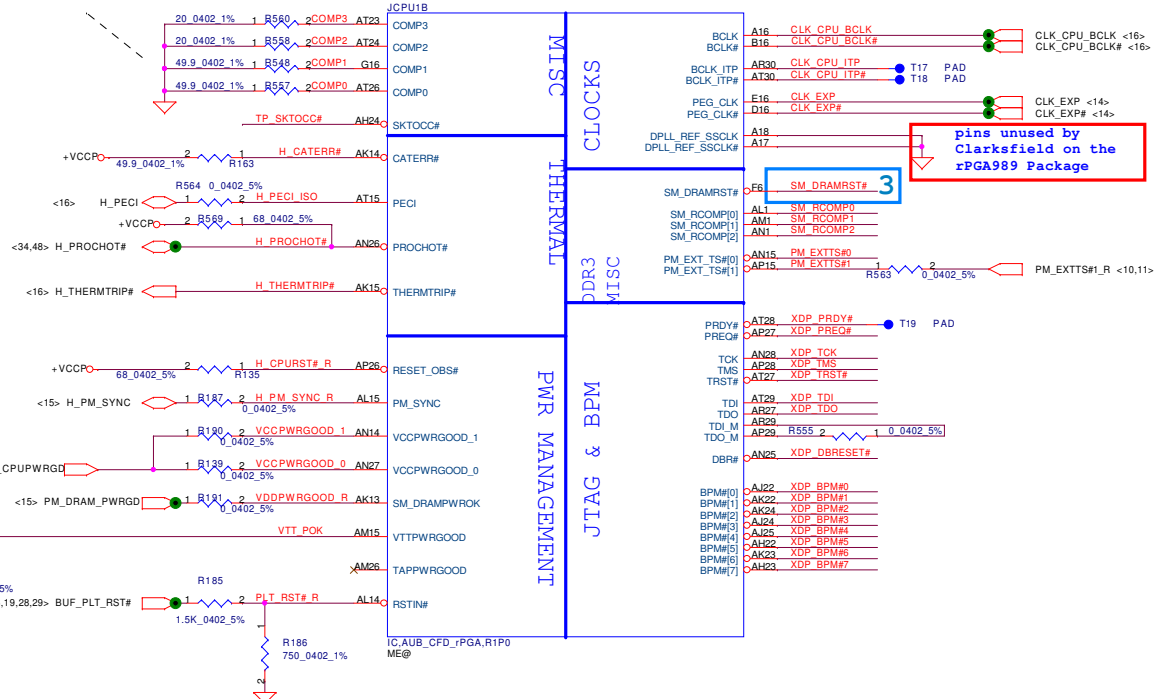
Power Sequence

The ramp time for any rail must be more than 40us

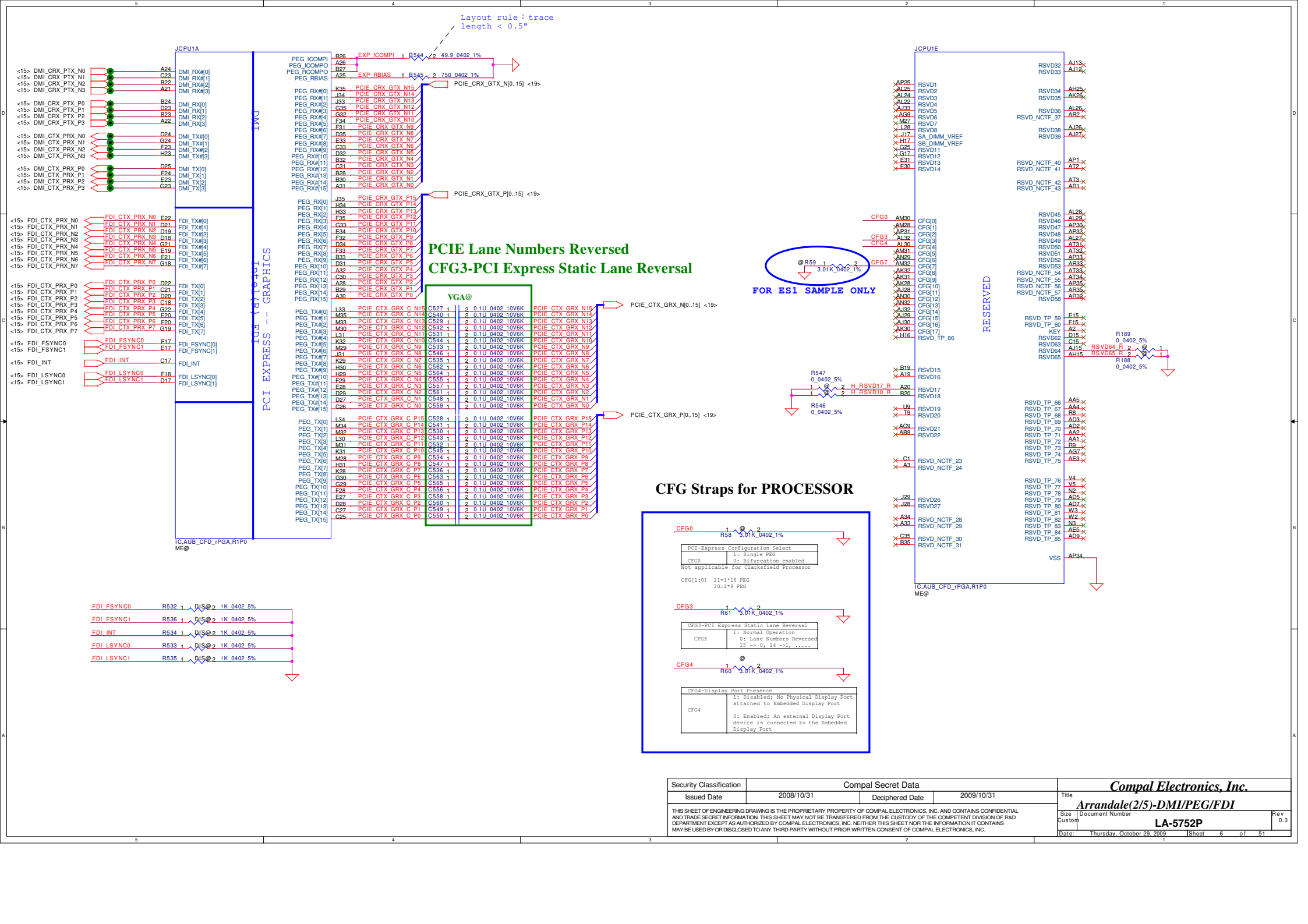


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				VGA Notes List		
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Layout rule: 10mil width trace
length < 0.5", spacing 20mil



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Layout rule: trace length < 0.5"

**PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal**

FOR ES1 SAMPLE ONLY

CFG Straps for PROCESSOR

CFG0

1: Single PEG
0: Bifurcation enabled
Not applicable for Clarkfield Processor

CFG[1:0] 11=1*16 PEG
10=2*8 PEG

CFG3

CFG3-PCI Express Static Lane Reversal

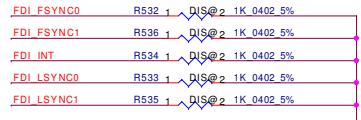
CFG3 1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4

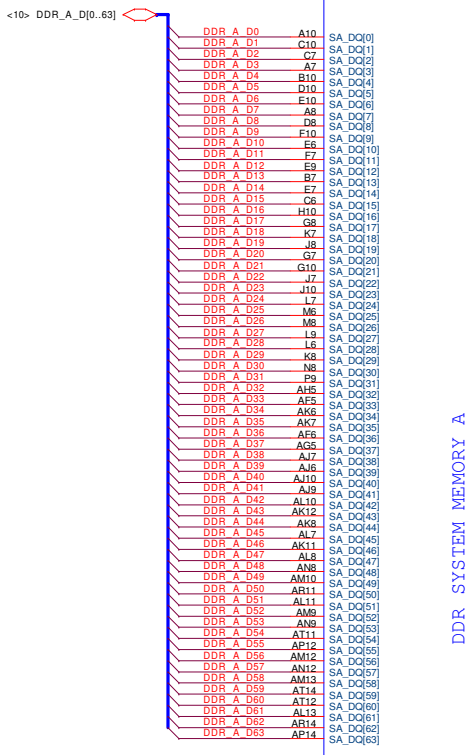
CFG4-Display Port Presence

CFG4 1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

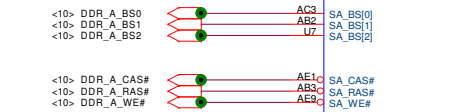
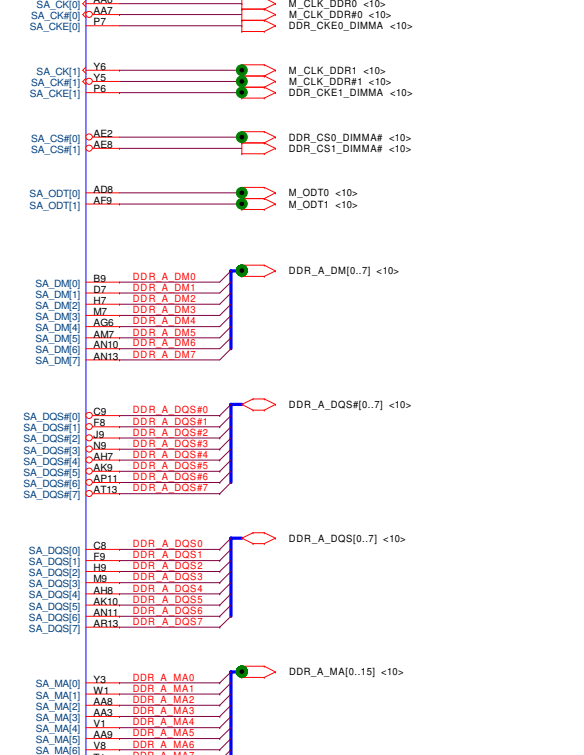
PEG	TX#	PCIE CRX GTX	PCIE CRX GTX NO.	PCIE CRX GTX P#	PCIE CRX GTX N#	PCIE CRX GTX NO.	PCIE CRX GTX P#	PCIE CRX GTX N#
PEG_RX[0]	K36	PCIE CRX GTX N15	15	15	15	15	15	15
PEG_RX[1]	J34	PCIE CRX GTX N14	14	14	14	14	14	14
PEG_RX[2]	J33	PCIE CRX GTX N13	13	13	13	13	13	13
PEG_RX[3]	G35	PCIE CRX GTX N12	12	12	12	12	12	12
PEG_RX[4]	G32	PCIE CRX GTX N11	11	11	11	11	11	11
PEG_RX[5]	F34	PCIE CRX GTX N10	10	10	10	10	10	10
PEG_RX[6]	F31	PCIE CRX GTX N9	9	9	9	9	9	9
PEG_RX[7]	D35	PCIE CRX GTX N8	8	8	8	8	8	8
PEG_RX[8]	E33	PCIE CRX GTX N7	7	7	7	7	7	7
PEG_RX[9]	C33	PCIE CRX GTX N6	6	6	6	6	6	6
PEG_RX[10]	D32	PCIE CRX GTX N5	5	5	5	5	5	5
PEG_RX[11]	B32	PCIE CRX GTX N4	4	4	4	4	4	4
PEG_RX[12]	C31	PCIE CRX GTX N3	3	3	3	3	3	3
PEG_RX[13]	B28	PCIE CRX GTX N2	2	2	2	2	2	2
PEG_RX[14]	B30	PCIE CRX GTX N1	1	1	1	1	1	1
PEG_RX[15]	A31	PCIE CRX GTX N0	0	0	0	0	0	0
PEG_RX[0]	J35	PCIE CRX GTX P15	15	15	15	15	15	15
PEG_RX[1]	H34	PCIE CRX GTX P14	14	14	14	14	14	14
PEG_RX[2]	J33	PCIE CRX GTX P13	13	13	13	13	13	13
PEG_RX[3]	F35	PCIE CRX GTX P12	12	12	12	12	12	12
PEG_RX[4]	G32	PCIE CRX GTX P11	11	11	11	11	11	11
PEG_RX[5]	F34	PCIE CRX GTX P10	10	10	10	10	10	10
PEG_RX[6]	F31	PCIE CRX GTX P9	9	9	9	9	9	9
PEG_RX[7]	D34	PCIE CRX GTX P8	8	8	8	8	8	8
PEG_RX[8]	E33	PCIE CRX GTX P7	7	7	7	7	7	7
PEG_RX[9]	D31	PCIE CRX GTX P6	6	6	6	6	6	6
PEG_RX[10]	A32	PCIE CRX GTX P5	5	5	5	5	5	5
PEG_RX[11]	C30	PCIE CRX GTX P4	4	4	4	4	4	4
PEG_RX[12]	A28	PCIE CRX GTX P2	2	2	2	2	2	2
PEG_RX[13]	B29	PCIE CRX GTX P1	1	1	1	1	1	1
PEG_RX[14]	A30	PCIE CRX GTX P0	0	0	0	0	0	0
PEG_TX[0]	L33	PCIE CTX GRX C N15	C527	1	2	0.1U	0.402	10V6K
PEG_TX[1]	M35	PCIE CTX GRX C N13	C540	1	2	0.1U	0.402	10V6K
PEG_TX[2]	M30	PCIE CTX GRX C N12	C542	1	2	0.1U	0.402	10V6K
PEG_TX[3]	L31	PCIE CTX GRX C N11	C531	1	2	0.1U	0.402	10V6K
PEG_TX[4]	K32	PCIE CTX GRX C N10	C544	1	2	0.1U	0.402	10V6K
PEG_TX[5]	M29	PCIE CTX GRX C N9	C533	1	2	0.1U	0.402	10V6K
PEG_TX[6]	J31	PCIE CTX GRX C N8	C546	1	2	0.1U	0.402	10V6K
PEG_TX[7]	K29	PCIE CTX GRX C N7	C535	1	2	0.1U	0.402	10V6K
PEG_TX[8]	H30	PCIE CTX GRX C N6	C562	1	2	0.1U	0.402	10V6K
PEG_TX[9]	H29	PCIE CTX GRX C N5	C564	1	2	0.1U	0.402	10V6K
PEG_TX[10]	E29	PCIE CTX GRX C N4	C555	1	2	0.1U	0.402	10V6K
PEG_TX[11]	E28	PCIE CTX GRX C N3	C557	1	2	0.1U	0.402	10V6K
PEG_TX[12]	D29	PCIE CTX GRX C N2	C561	1	2	0.1U	0.402	10V6K
PEG_TX[13]	D27	PCIE CTX GRX C N1	C548	1	2	0.1U	0.402	10V6K
PEG_TX[14]	C26	PCIE CTX GRX C N0	C559	1	2	0.1U	0.402	10V6K
PEG_TX[0]	L34	PCIE CTX GRX C P15	C528	1	2	0.1U	0.402	10V6K
PEG_TX[1]	M34	PCIE CTX GRX C P13	C541	1	2	0.1U	0.402	10V6K
PEG_TX[2]	L30	PCIE CTX GRX C P12	C543	1	2	0.1U	0.402	10V6K
PEG_TX[3]	M31	PCIE CTX GRX C P11	C532	1	2	0.1U	0.402	10V6K
PEG_TX[4]	K31	PCIE CTX GRX C P10	C545	1	2	0.1U	0.402	10V6K
PEG_TX[5]	M28	PCIE CTX GRX C P9	C534	1	2	0.1U	0.402	10V6K
PEG_TX[6]	H31	PCIE CTX GRX C P8	C547	1	2	0.1U	0.402	10V6K
PEG_TX[7]	K28	PCIE CTX GRX C P7	C536	1	2	0.1U	0.402	10V6K
PEG_TX[8]	G30	PCIE CTX GRX C P6	C563	1	2	0.1U	0.402	10V6K
PEG_TX[9]	G29	PCIE CTX GRX C P5	C565	1	2	0.1U	0.402	10V6K
PEG_TX[10]	E27	PCIE CTX GRX C P4	C556	1	2	0.1U	0.402	10V6K
PEG_TX[11]	E27	PCIE CTX GRX C P3	C558	1	2	0.1U	0.402	10V6K
PEG_TX[12]	D28	PCIE CTX GRX C P2	C560	1	2	0.1U	0.402	10V6K
PEG_TX[13]	C27	PCIE CTX GRX C P1	C549	1	2	0.1U	0.402	10V6K
PEG_TX[14]	C25	PCIE CTX GRX C P0	C550	1	2	0.1U	0.402	10V6K



JCPU1C

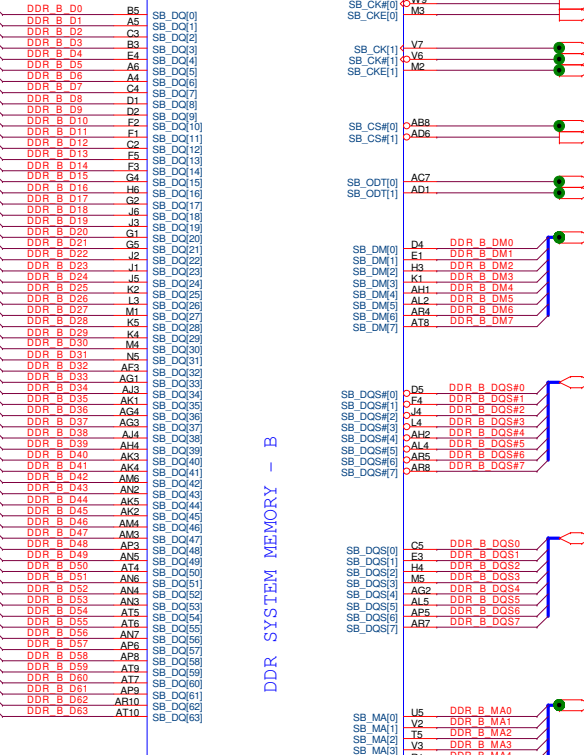


DDR SYSTEM MEMORY A



IC:AUB_CFD_rPGA,R1P0 ME@

JCPU1D



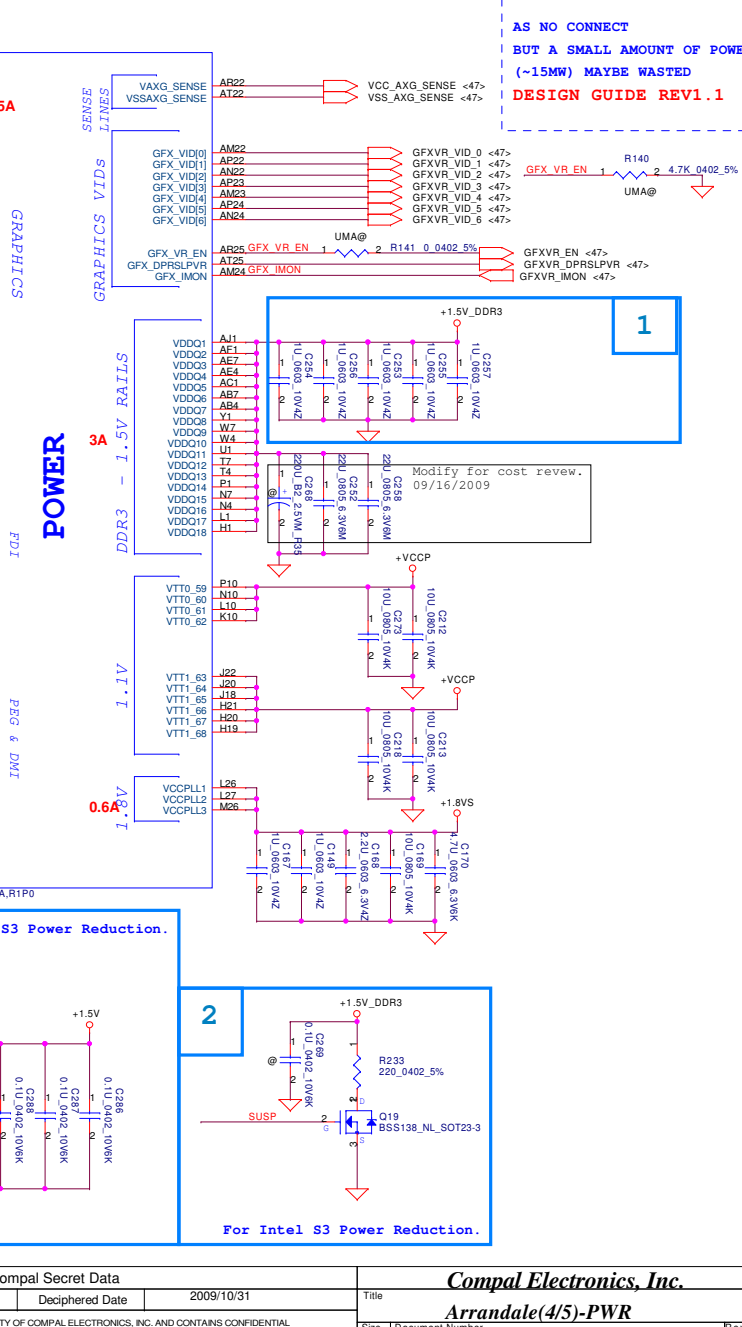
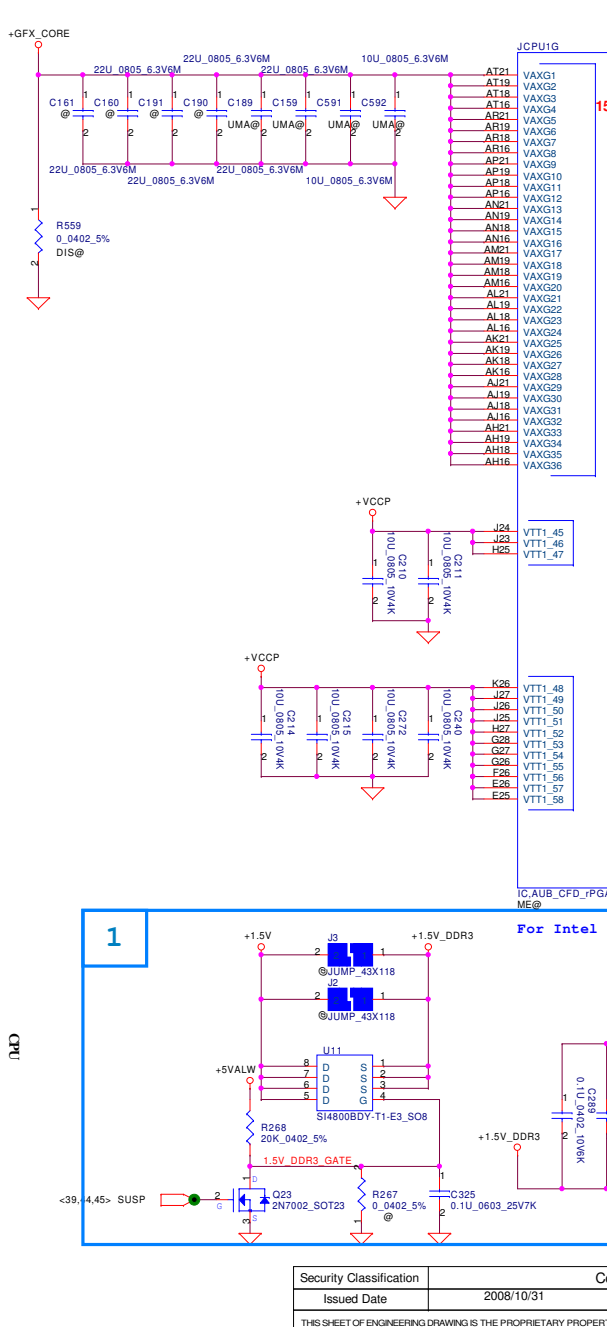
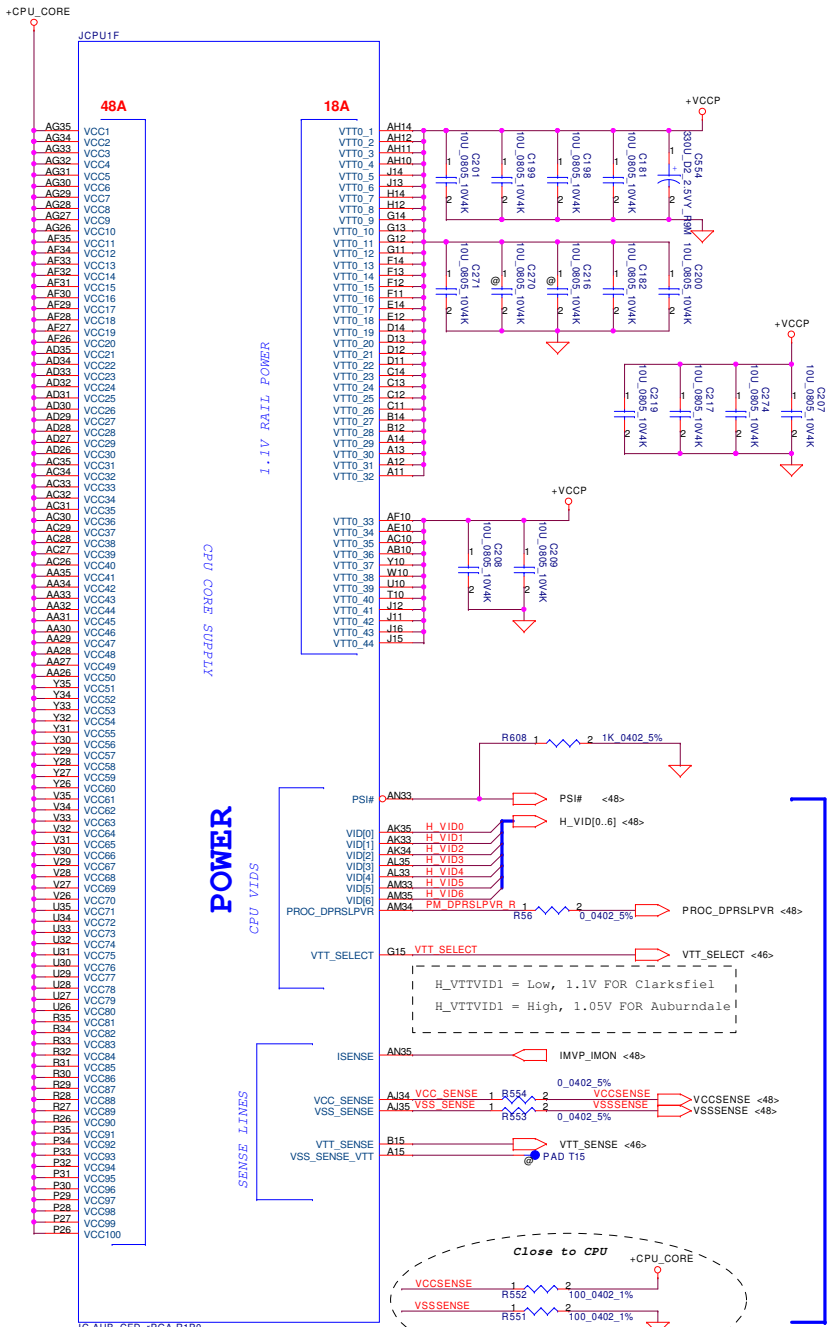
DDR SYSTEM MEMORY - B



IC:AUB_CFD_rPGA,R1P0 ME@

Security Classification	Compal Secret Data		2009/10/31		Title Compal Electronics, Inc. Arrandale(3/5)-DDR III
Issued Date	2008/10/31	Deciphered Date	2009/10/31		
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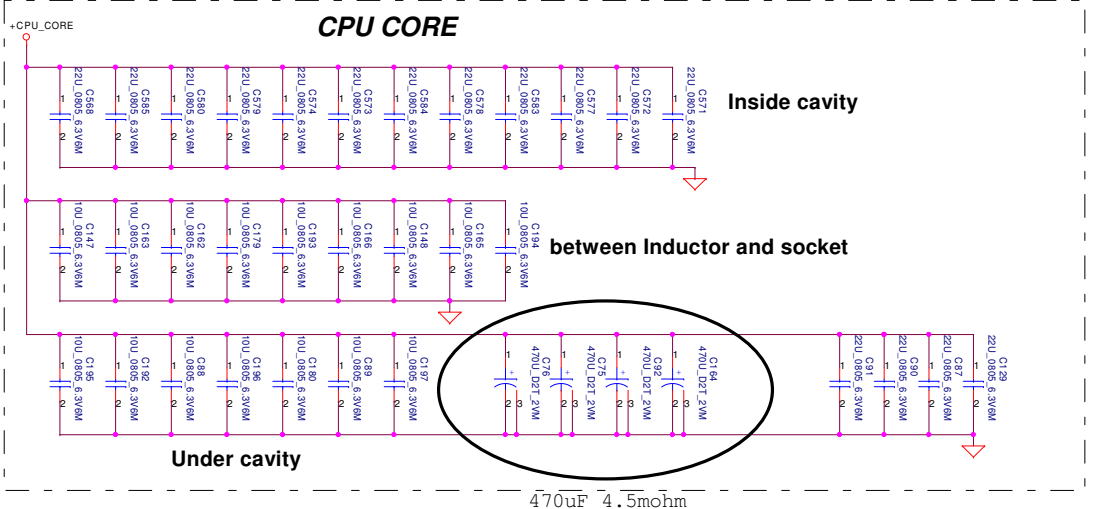
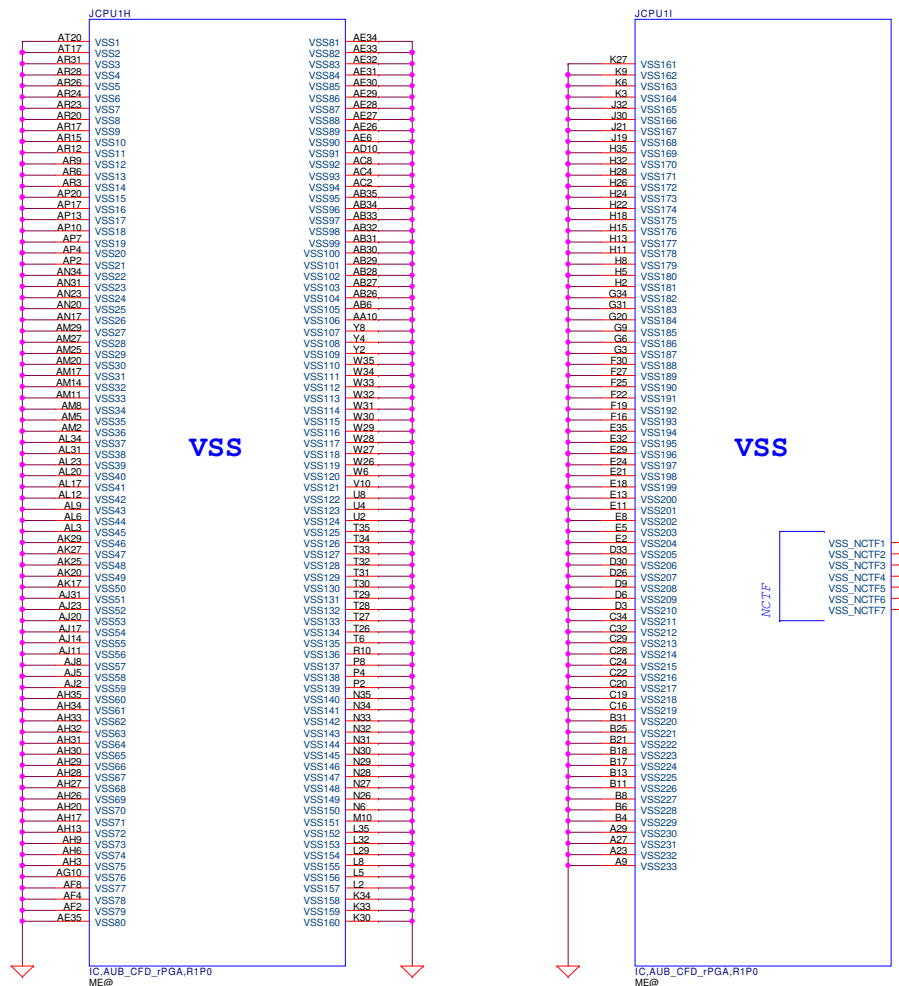
AS NO CONNECT
BUT A SMALL AMOUNT OF POWER
(~15MW) MAYBE WASTED
DESIGN GUIDE REV1.1

IC_AUB_CFD_PGA_R1P0
ME@

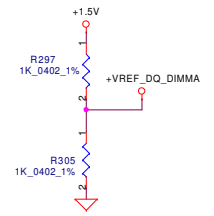
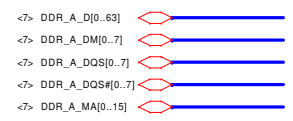
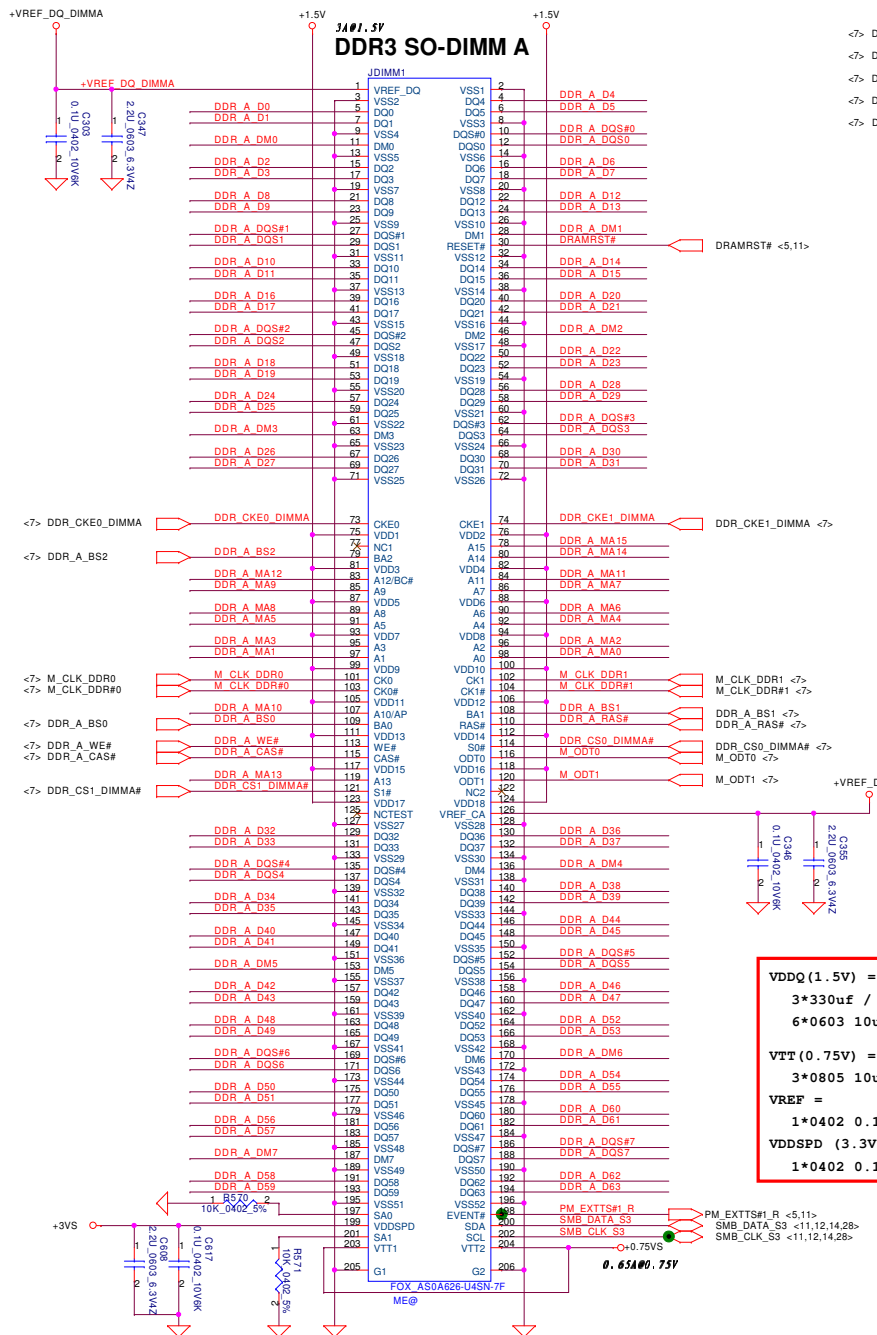
IC_AUB_CFD_PGA_R1P0
ME@

IC_AUB_CFD_PGA_R1P0
ME@

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Size	Document Number	Rev	
Custom	LA-5752P	0.3	
Date:	Thursday, October 29, 2009	Sheet	8 of 51

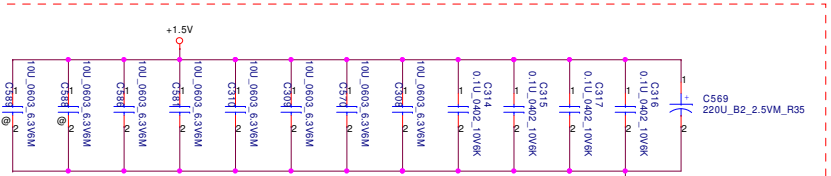


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Arrandale(5/5)-GND/Bypass
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Date: Thursday, October 29, 2009			Sheet 9 of 51	LA-5752P



For Arranale only +VREF_DQ_DIMMA supply from an external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

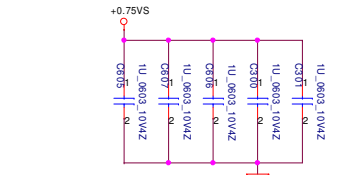


VDDQ (1.5V) =
 $3 \times 330\text{uF} / 12\text{m ohm (TOTAL FOR 2 SO-DIMMs)}$
 $6 \times 0603 \ 10\text{uF (PER CONNECTOR)}$

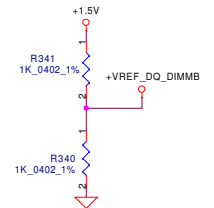
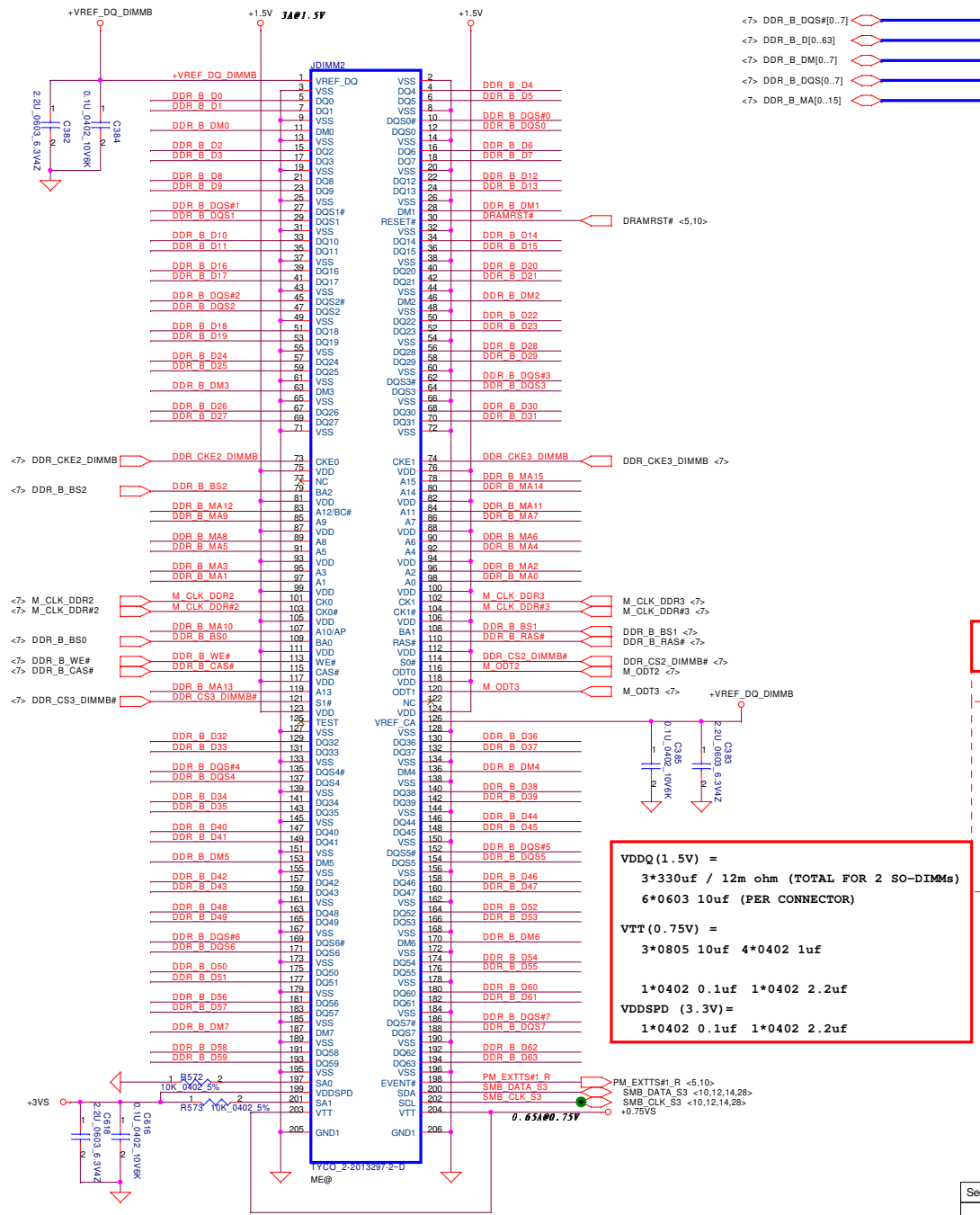
VTT (0.75V) =
 $3 \times 0805 \ 10\text{uF} \ 4 \times 0402 \ 1\text{uF}$

VREF =
 $1 \times 0402 \ 0.1\text{uF} \ 1 \times 0402 \ 2.2\text{uF}$

VDDSPD (3.3V) =
 $1 \times 0402 \ 0.1\text{uF} \ 1 \times 0402 \ 2.2\text{uF}$

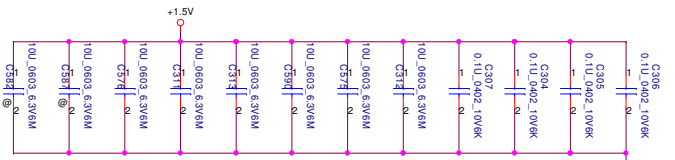


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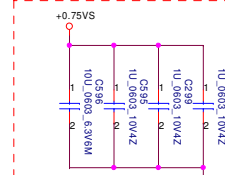


For Arranale only +VREF_DQ_DIMMB supply from an external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



VDDQ (1.5V) =
 $3 \times 330\mu\text{f} / 12\text{m ohm}$ (TOTAL FOR 2 SO-DIMMS)
6*0603 10uF (PER CONNECTOR)

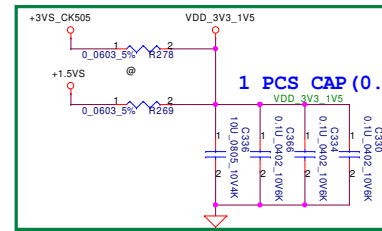
VTT (0.75V) =
 $3 \times 0805 10\mu\text{f} 4 \times 0402 1\mu\text{f}$

VDDSPD (3.3V) =
 $1 \times 0402 0.1\mu\text{f} 1 \times 0402 2.2\mu\text{f}$
 $1 \times 0402 0.1\mu\text{f} 1 \times 0402 2.2\mu\text{f}$

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	
Title			DDR3-SODIMM SLOT2	
Size	Document Number	Rev	0.3	
LA-5752P		Date:	Thursday, October 29, 2009	Sheet 11 of 51

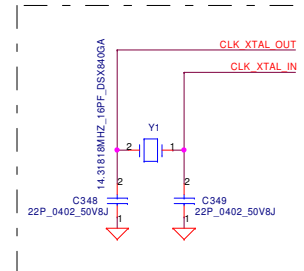
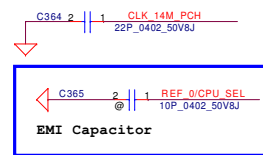
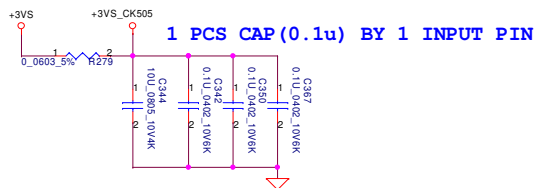
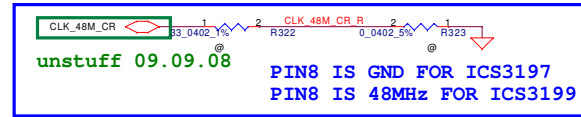
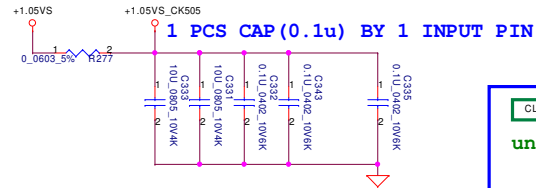
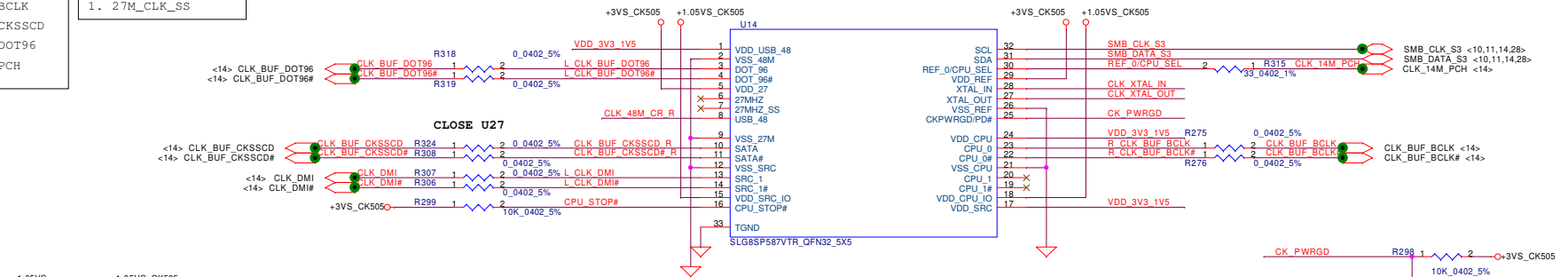
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Reserve for Low Power CLK GEN.
RTM890N-632
SLG8LV597VTR



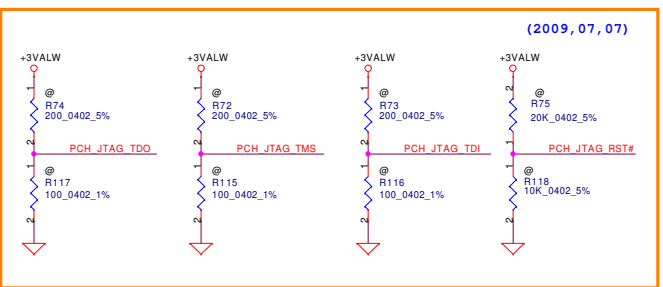
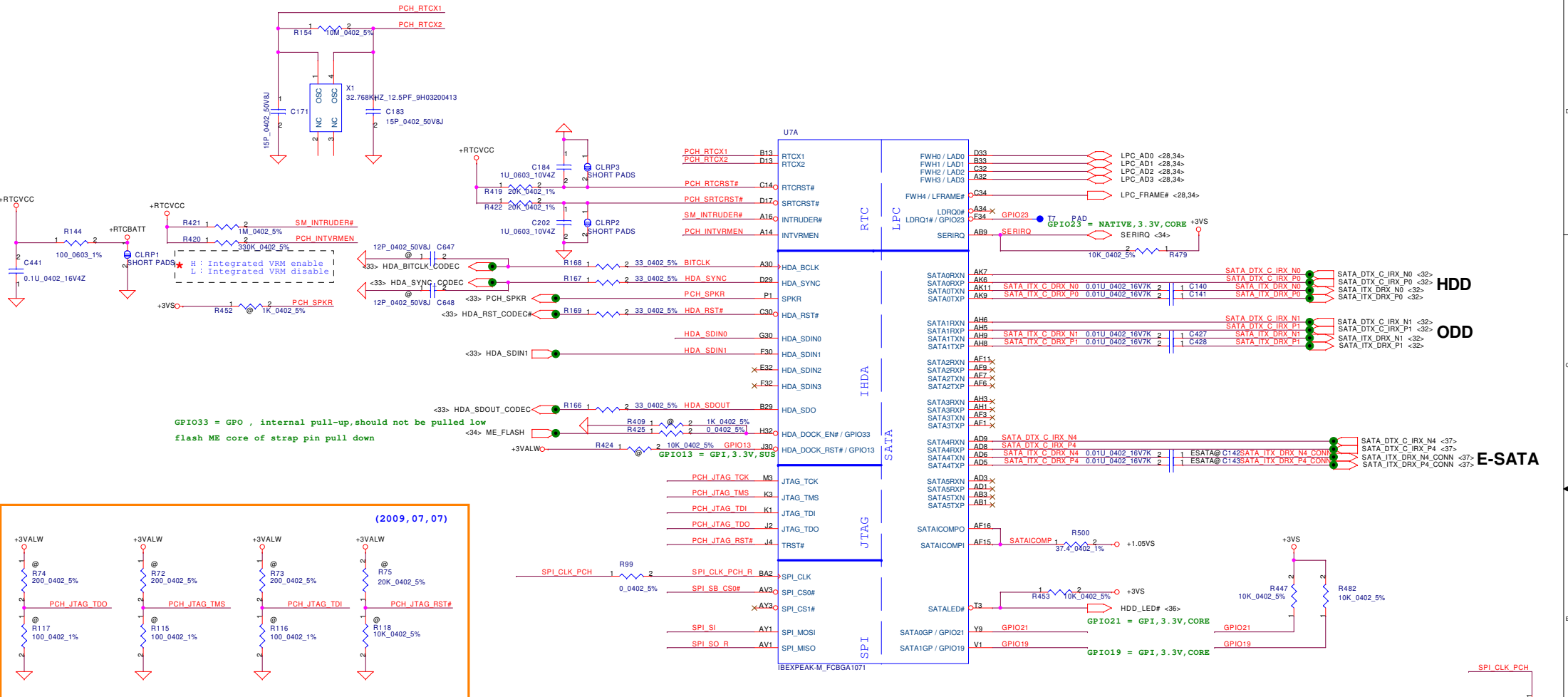
- CLK GEN TO PCH**
1. CLK_DMI
 2. CLK_BUF_BCLK
 3. CLK_BUF_CKSSCD
 4. CLK_BUF_DOT96
 5. CLK_14M_PCH

- CLK GEN TO VGA**
1. 27M_CLK
 1. 27M_CLK_SS



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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Issued Date	2008/10/31	Deciphered Date			
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Size	Document Number		Rev	0.3	
LA-5752P					
Date:	Thursday, October 29, 2009	Sheet	12	of	51

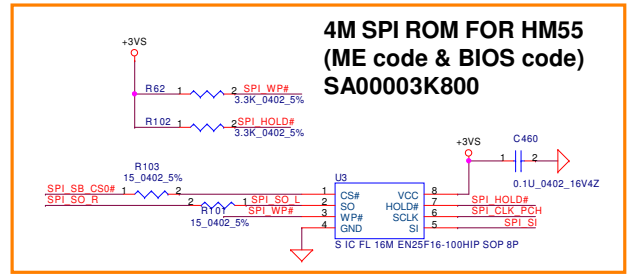


(2009, 05, 04)

PCH_JTAG_TCK R114 1 2 51 0402 5%

FOR INTEL DPDG REV1.6 (MAY 2009)

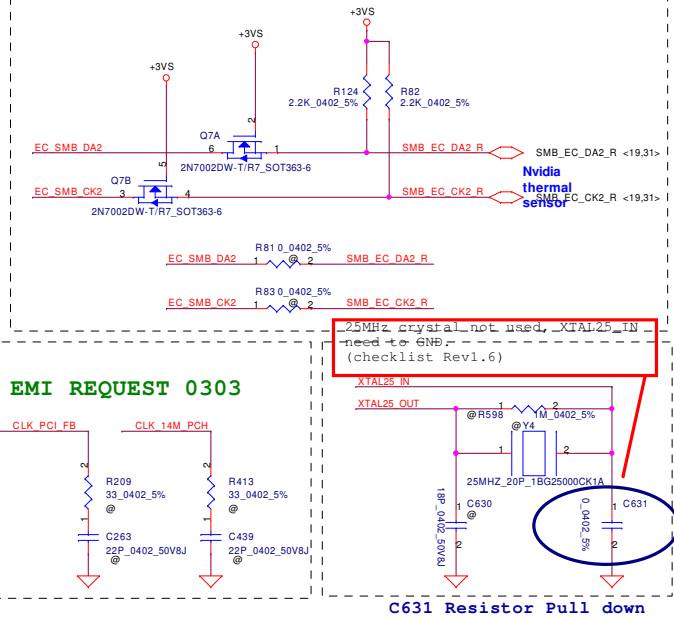
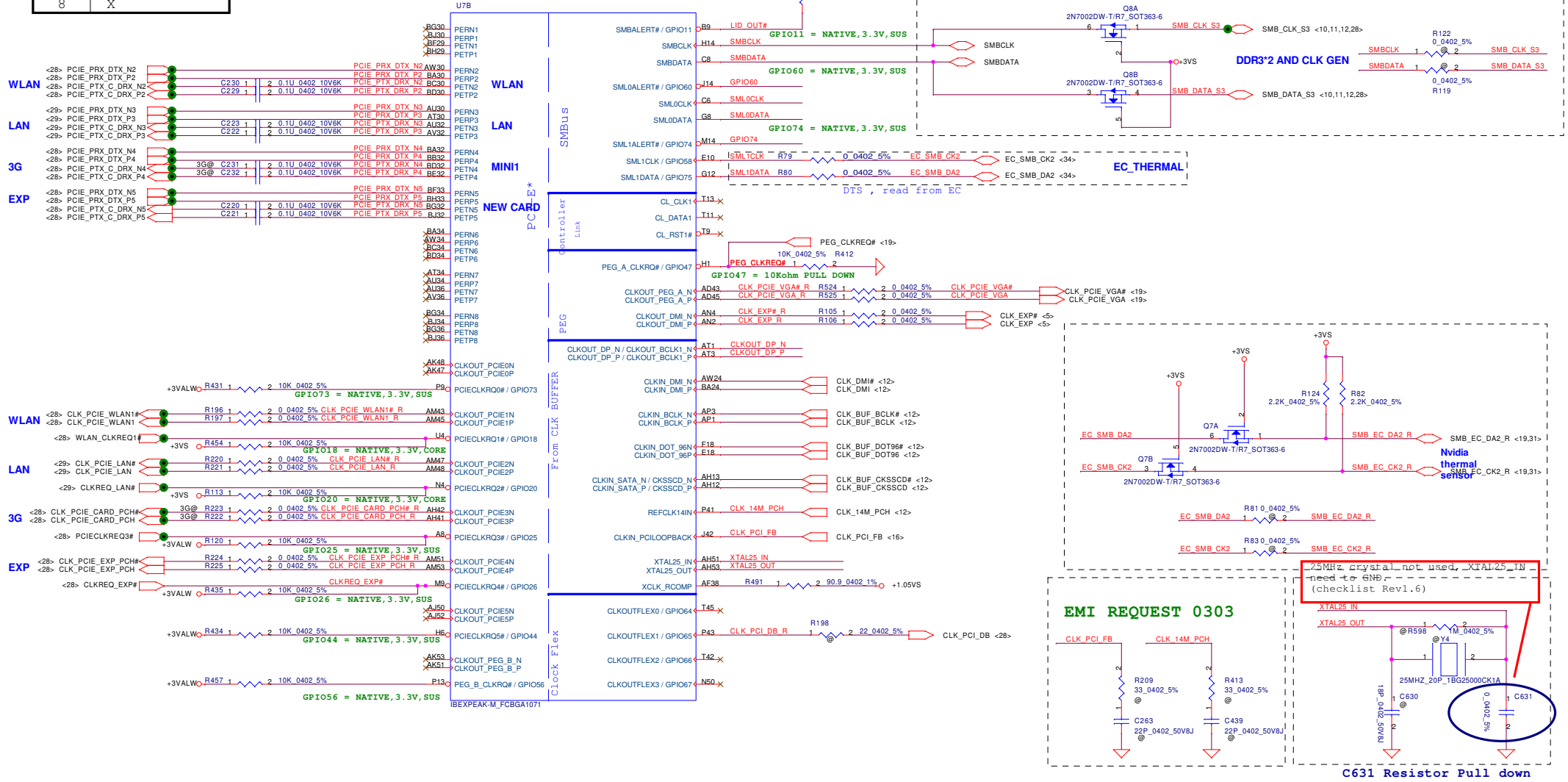
PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
	R595	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R594	10Kohm	10Kohm	No Install



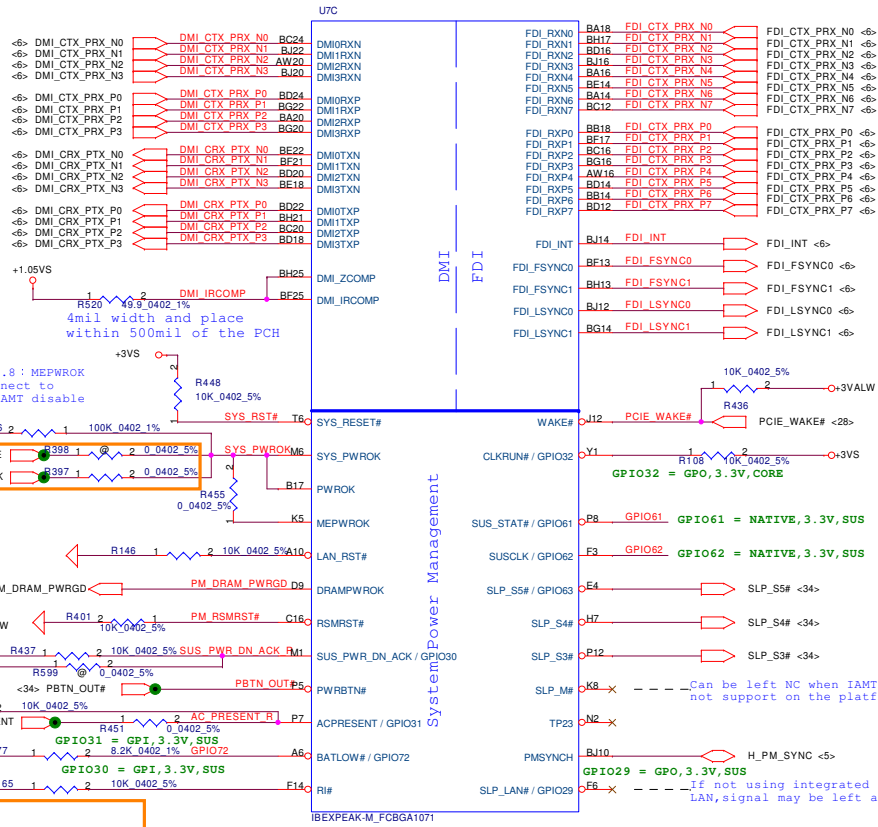
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(1/6)-HDA/JTAG/SATA	
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PCI-E PORT LIST

PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X

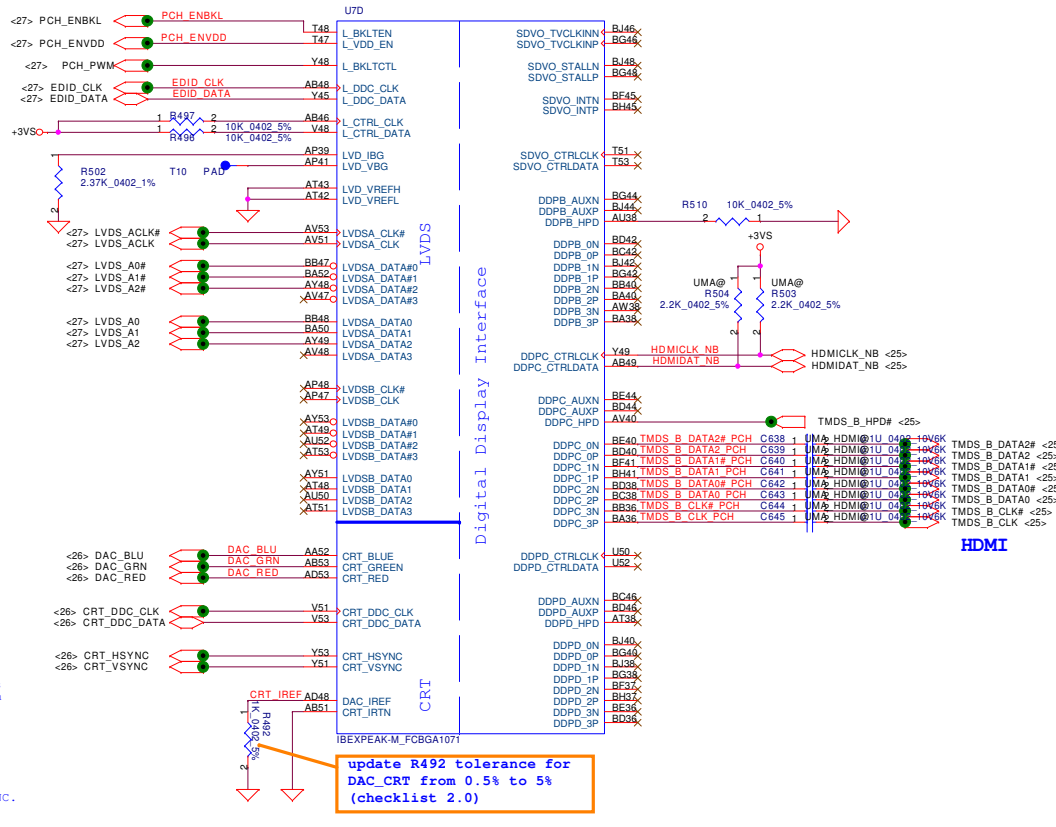
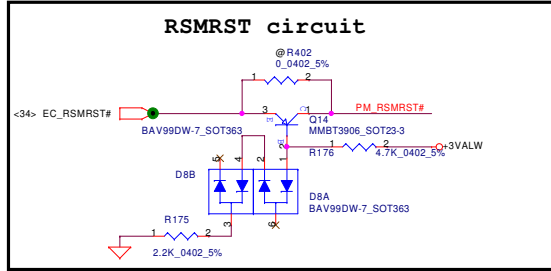
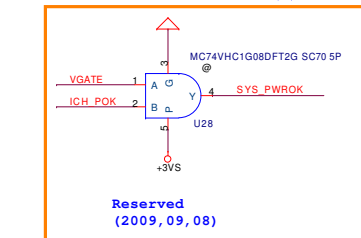


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(2/6)-PCI-E/SMBUS/CLK	
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			Custom	LA-5752P	0.3
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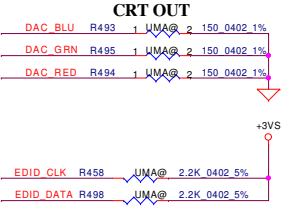


Checklist 0.8 : MEPWROK can be connect to PWROK if IAMT disable

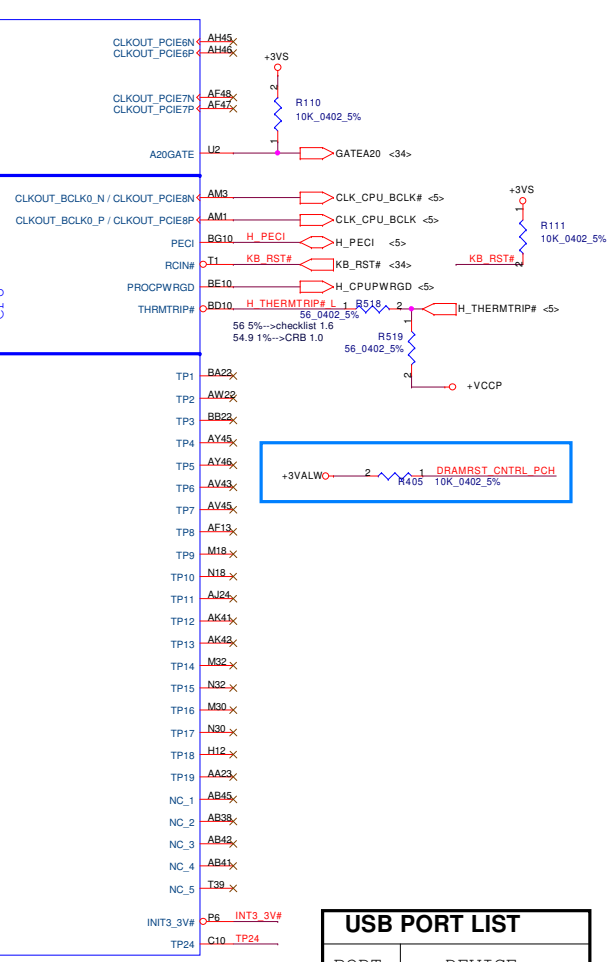
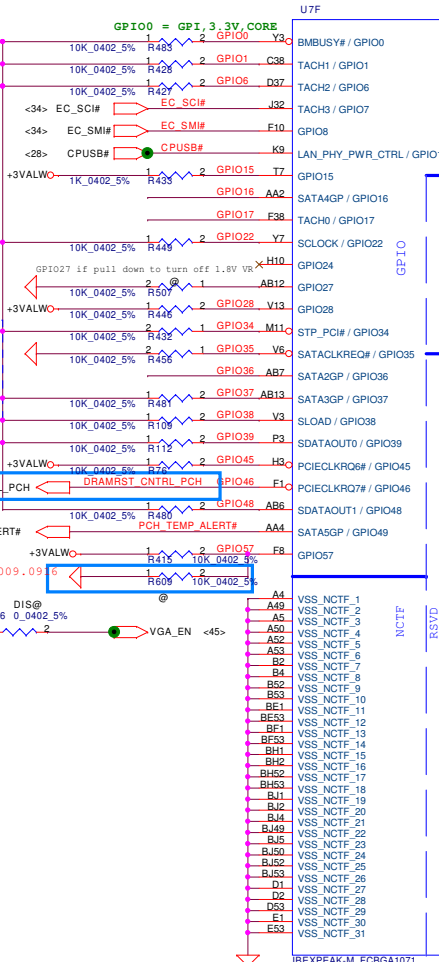
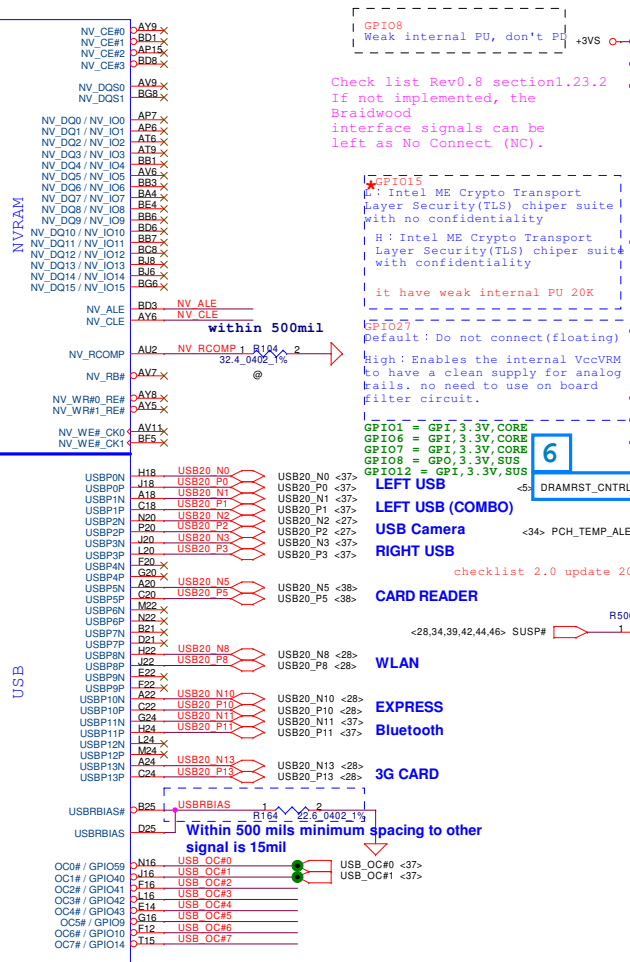
(2009, 05, 04)



update R492 tolerance for DAC_CRT from 0.5% to 5% (checklist 2.0)

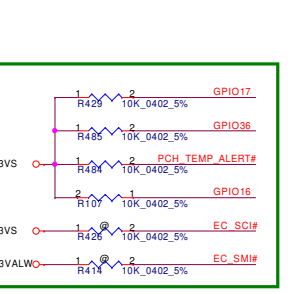
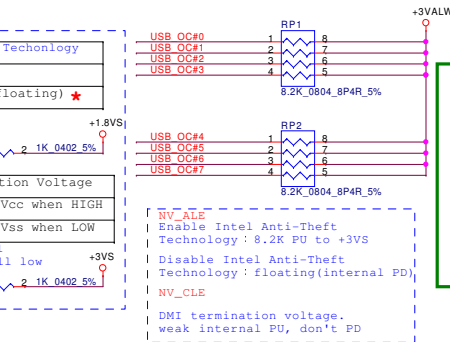


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Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(3/6)-DMI/GPIO/LVDS		
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Boot BIOS Strap

PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC *
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	
5	CARD READER
6	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.
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GPIO18 = NATIVE, 5V, CORE
GPIO52 = NATIVE, 5V, CORE
GPIO54 = NATIVE, 5V, CORE

GPIO2 = GPI, 5V, CORE
GPIO3 = GPI, 5V, CORE
GPIO4 = GPI, 5V, CORE
GPIO5 = GPI, 5V, CORE

Default-Internal pull up
Low-Configures DMI for ES1 compatible operation(for servers only.Not for mobile/desktops)

Check list Rev0.8 section.23.2
If not implemented, the Braidwood interface signals can be left as No Connect (NC).

GPIO15 Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H: Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
it have weak internal PU 20K

GPIO27
Default: Do not connect(floating)
High: Enables the internal VccVRM to have a clean supply for analog rails. no need to use on board filter circuit.

GPIO1 = GPI, 3.3V, CORE
GPIO6 = GPI, 3.3V, CORE
GPIO7 = GPI, 3.3V, CORE
GPIO8 = GPO, 3.3V, SUS
GPIO12 = GPI, 3.3V, SUS

LEFT USB
LEFT USB (COMBO)
USB Camera
RIGHT USB

CARD READER

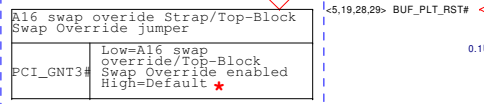
WLAN

EXPRESS
Bluetooth

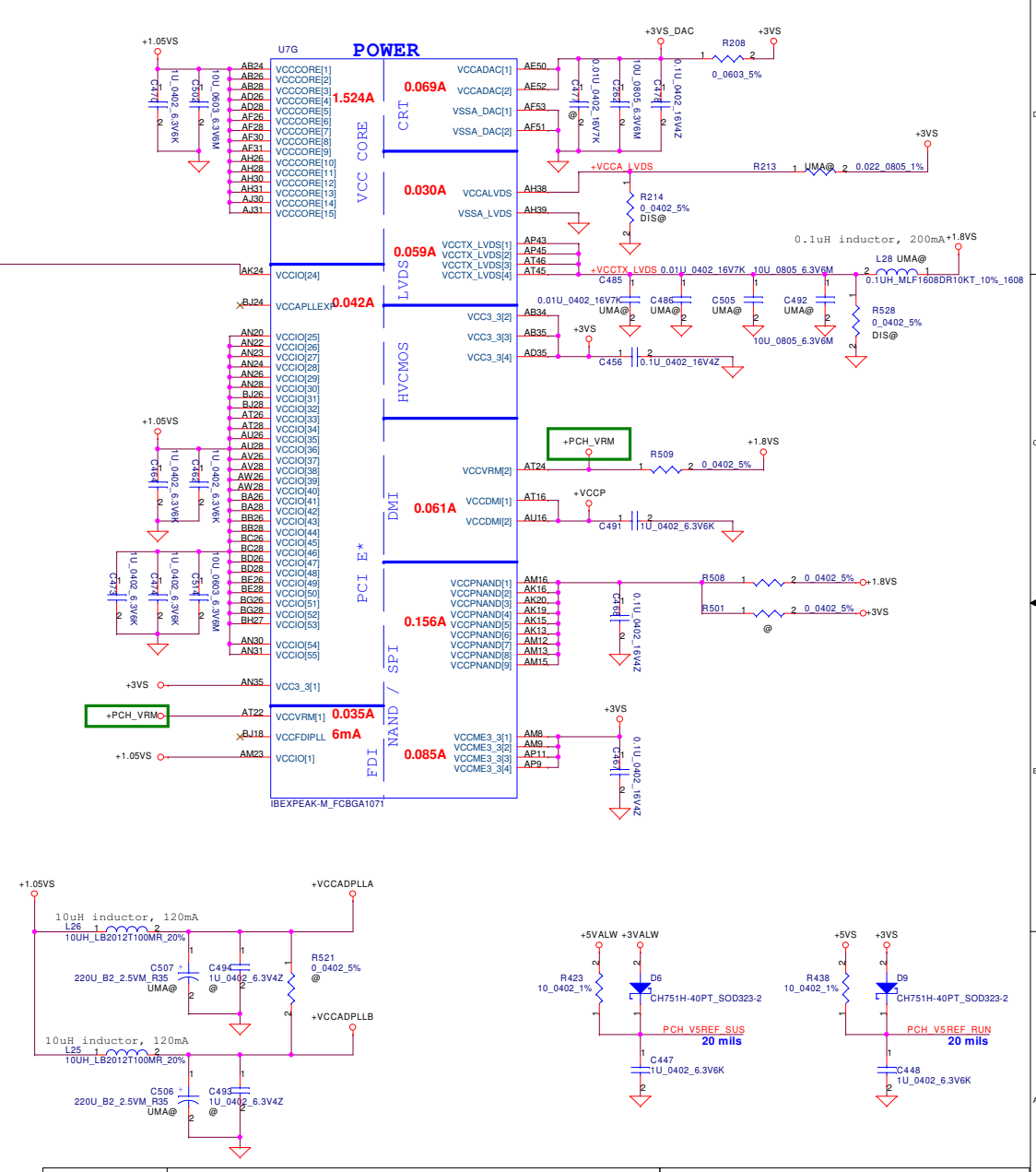
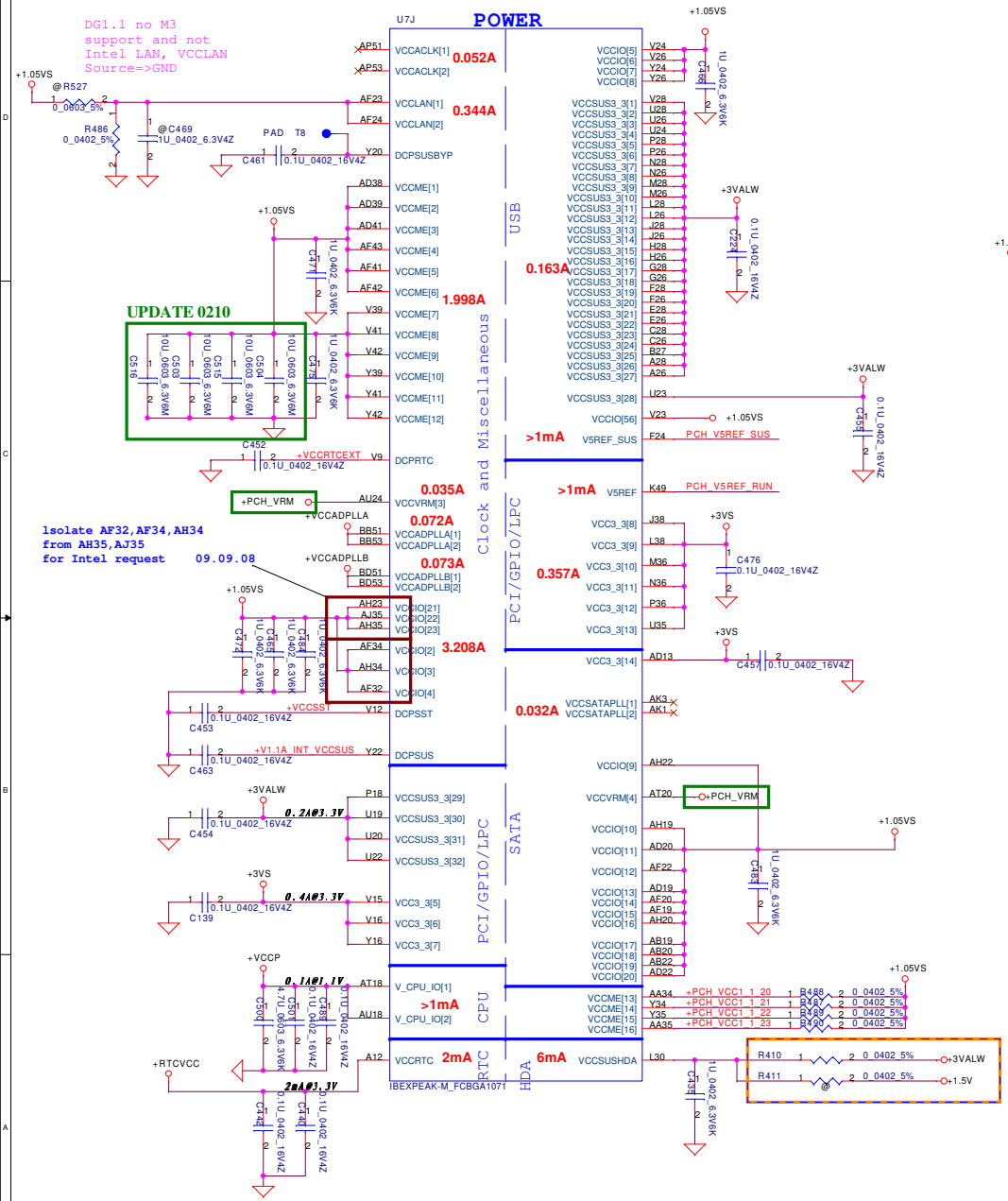
3G CARD

Within 500 mils minimum spacing to other signal is 15mil

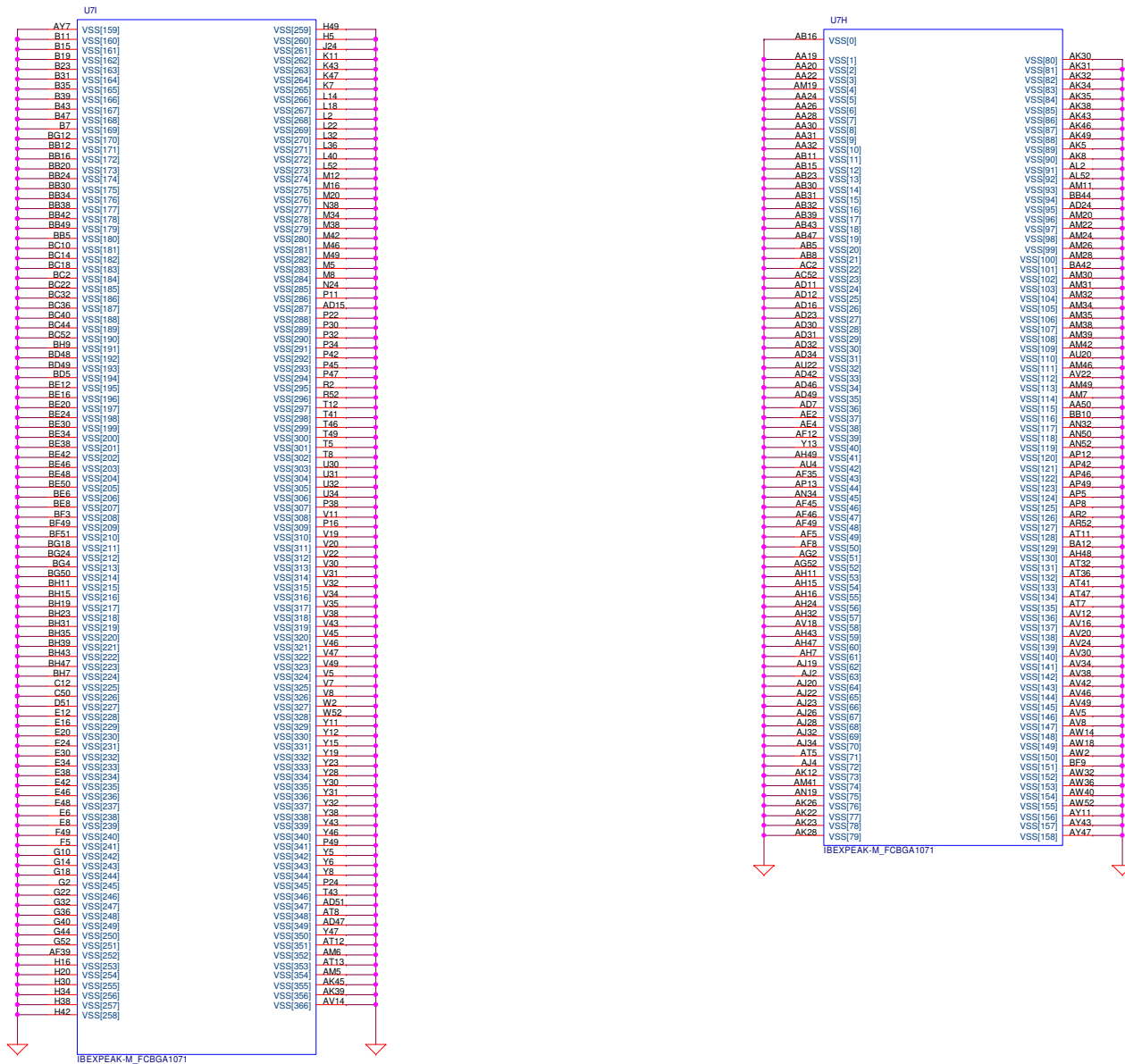
USB OC#0
USB OC#1
USB OC#2
USB OC#3
USB OC#4
USB OC#5
USB OC#6
USB OC#7



A16 swap override Strap/Top-Block Swap Override jumper
Low=A16 swap override/Top-Block Swap Override enabled
High=Default



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Issued Date	2008/08/12	Deciphered Date	2009/08/12	IBEX-M(5/6)-PWR	
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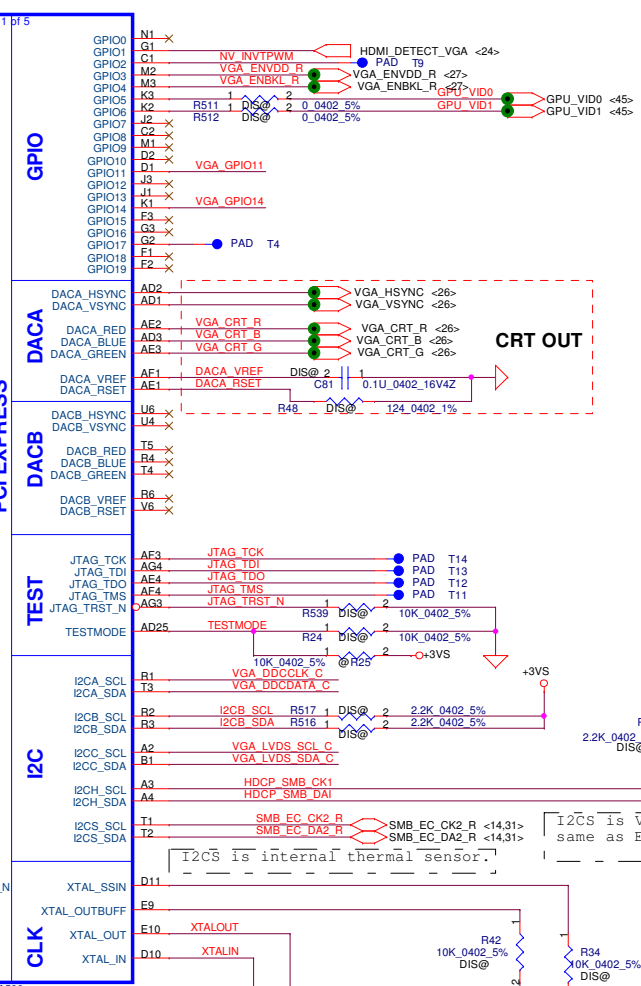
Size	Document Number	Rev
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- <6> PCIE_CTX_GRX_N0..15] → PCIE_CTX_GRX_N0..15]
- <6> PCIE_CTX_GRX_P0..15] → PCIE_CTX_GRX_P0..15]
- <6> PCIE_CRX_GTX_N0..15] → PCIE_CRX_GTX_N0..15]
- <6> PCIE_CRX_GTX_P0..15] → PCIE_CRX_GTX_P0..15]

- PCIE_CTX_GRX_P0 AE12
- PCIE_CTX_GRX_N0 AE12
- PCIE_CTX_GRX_P1 AE12
- PCIE_CTX_GRX_N1 AE12
- PCIE_CTX_GRX_P2 AE14
- PCIE_CTX_GRX_N2 AE14
- PCIE_CTX_GRX_P3 AE13
- PCIE_CTX_GRX_N3 AE13
- PCIE_CTX_GRX_P4 AG15
- PCIE_CTX_GRX_N4 AG16
- PCIE_CTX_GRX_P5 AE18
- PCIE_CTX_GRX_N5 AE18
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- PCIE_CTX_GRX_N13 AE25
- PCIE_CTX_GRX_P14 AE25
- PCIE_CTX_GRX_N14 AG26
- PCIE_CTX_GRX_P15 AE27
- PCIE_CTX_GRX_N15 AE27

- PCIE_CRX_GTX_P0 C120 DIS@ 1
- PCIE_CRX_GTX_N0 C119 DIS@ 1
- PCIE_CRX_GTX_P1 C118 DIS@ 1
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- PCIE_CRX_GTX_N3 C77 DIS@ 1
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- PCIE_CRX_GTX_P5 C114 DIS@ 1
- PCIE_CRX_GTX_N5 C113 DIS@ 1
- PCIE_CRX_GTX_P6 C112 DIS@ 1
- PCIE_CRX_GTX_N6 C111 DIS@ 1
- PCIE_CRX_GTX_P7 C109 DIS@ 1
- PCIE_CRX_GTX_N7 C110 DIS@ 1
- PCIE_CRX_GTX_P8 C108 DIS@ 1
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- PCIE_CRX_GTX_P11 C102 DIS@ 1
- PCIE_CRX_GTX_N11 C101 DIS@ 1
- PCIE_CRX_GTX_P12 C100 DIS@ 1
- PCIE_CRX_GTX_N12 C99 DIS@ 1
- PCIE_CRX_GTX_P13 C98 DIS@ 1
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- PCIE_CRX_GTX_P15 C93 DIS@ 1
- PCIE_CRX_GTX_N15 C93 DIS@ 1

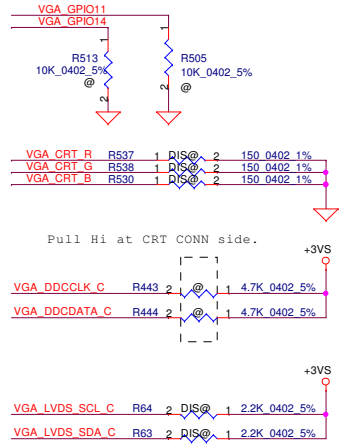
- <14> CLK_PCIE_VGA → CLK_PCIE_VGA#
- <14> CLK_PCIE_VGA# → CLK_PCIE_VGA#
- <14> PEG_CLKREQ# → PEG_CLKREQ#
- <14> BUF_PLT_RST# → BUF_PLT_RST#



Device ID	Device ID
N10M-GS (40nm)	0x0A74
N11M-GE1/LP1 (40nm)	0x0A7D

GPIO5 GPU_VID0	GPIO6 GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.0V	P0

GPIO5 GPU_VID0	GPIO6 GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.9V	P0

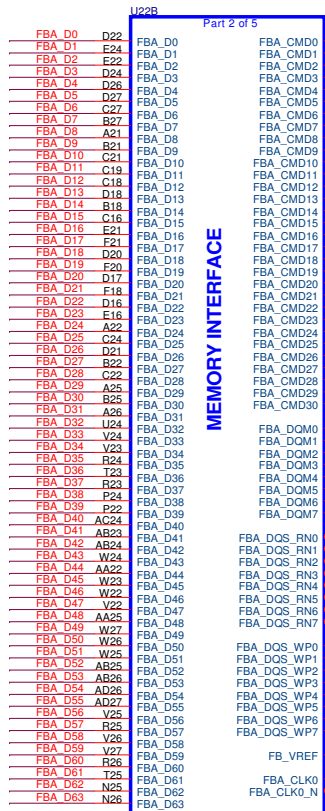
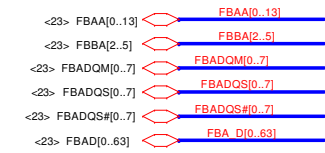


Removed external HDCP. 07/17/2009

Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15

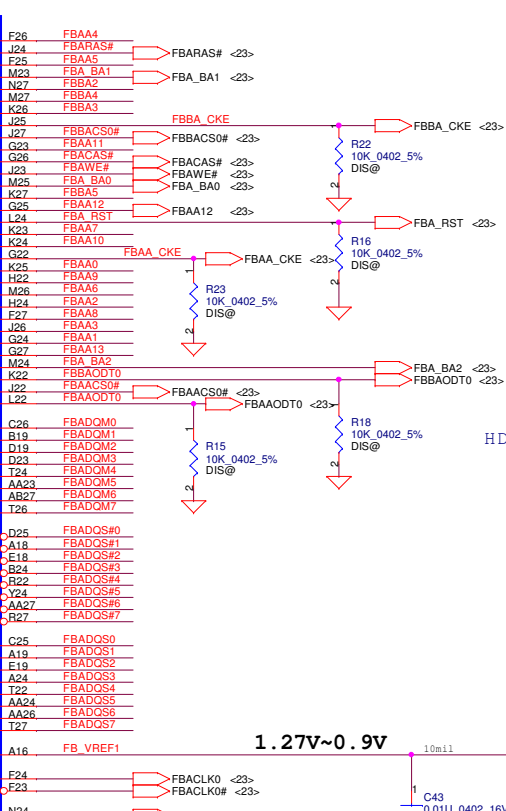
Compal Electronics, Inc.			
Title			
N10M-GE1 PCIE,GPIO,CLK			
Size B	Document Number	Rev	
	LA-5752P	0.3	
Date:	Thursday, October 29, 2009	Sheet	19 of 51

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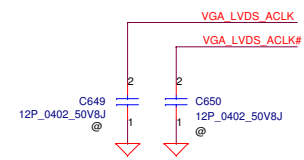


MEMORY INTERFACE

Part 2 of 5

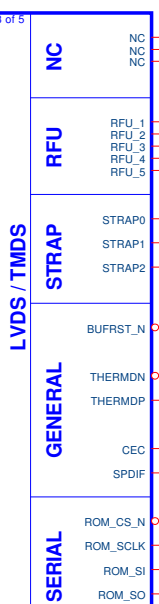
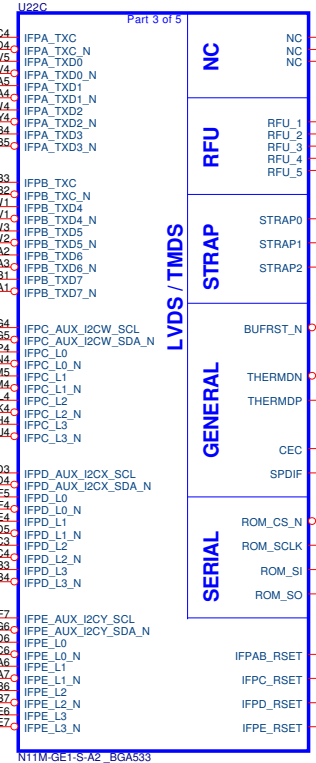
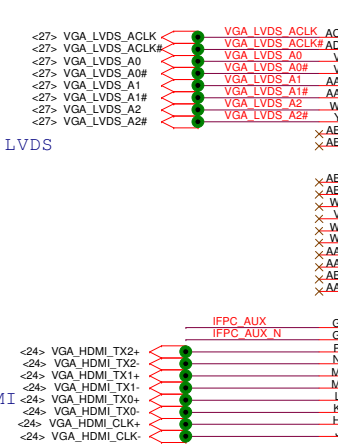


Part 3 of 5

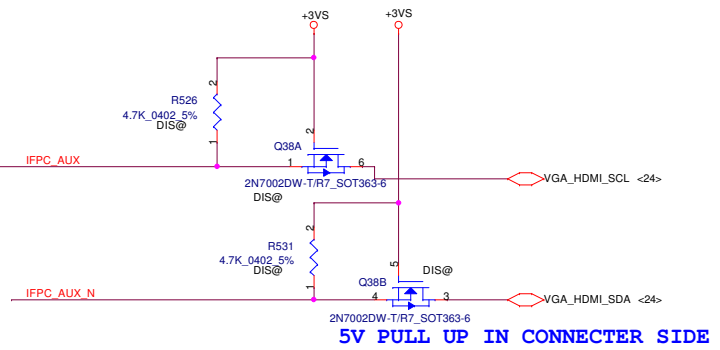
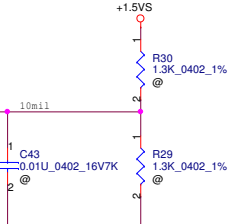


LVDS

HDMI



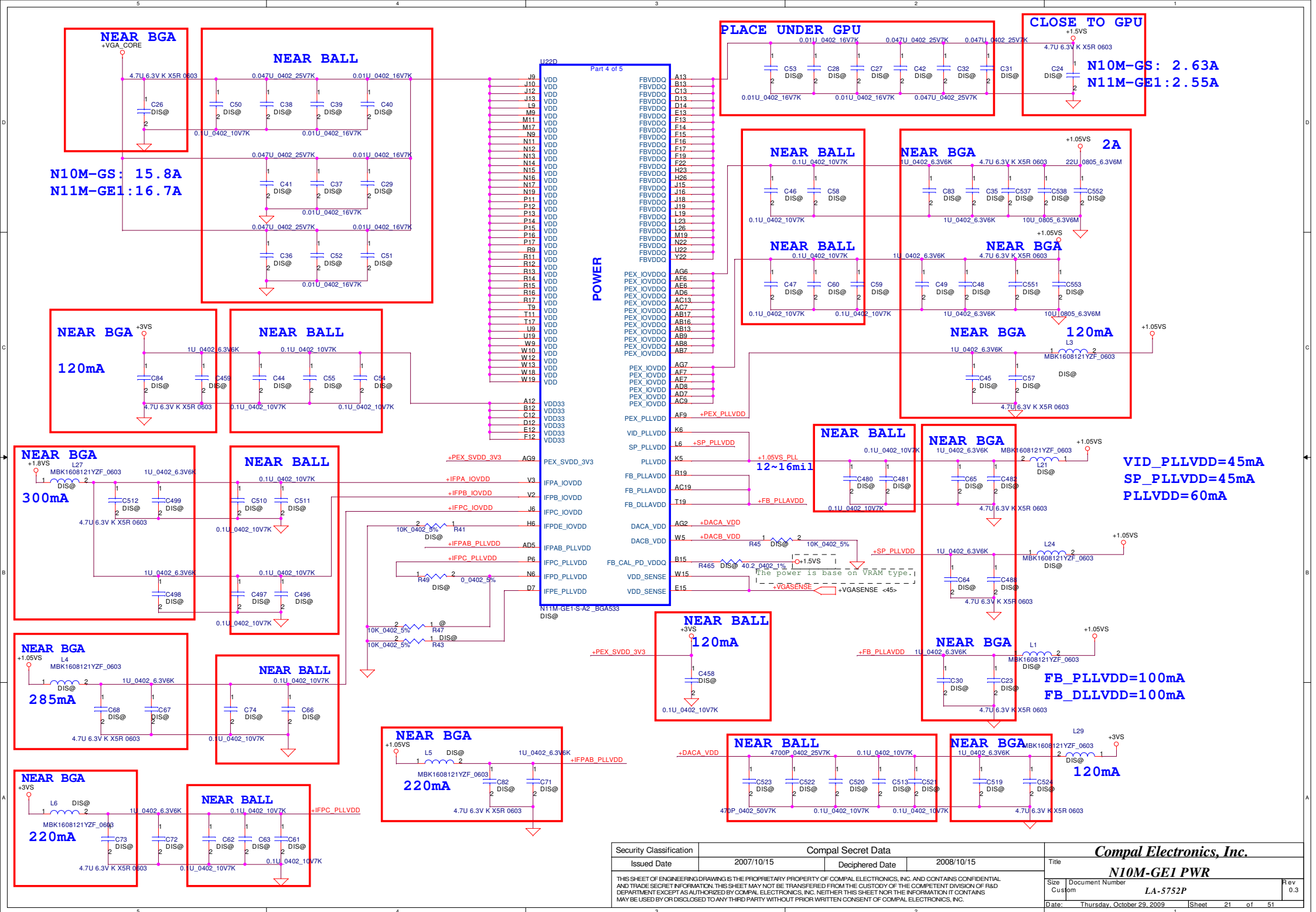
1.27V~0.9V



5V PULL UP IN CONNECTER SIDE

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		2008/10/15
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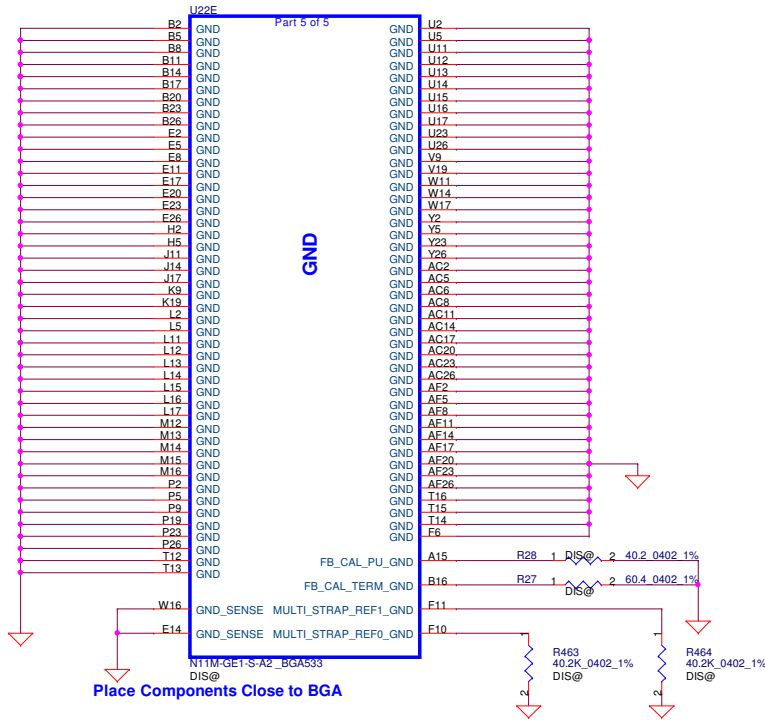
Compal Electronics, Inc.		
N10M-GE1 LVDS, Memory Bus		
Size	Document Number	Rev
B	LA-5752P	0.3
Date:	Thursday, October 29, 2009	Sheet 20 of 51



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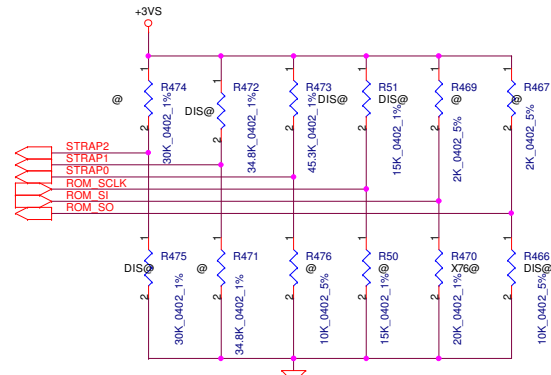
Title			Rev
N10M-GE1 PWR			
Size	Document Number	Rev	
Custom	LA-5752P	0.3	
Date	Thursday, October 29, 2009	Sheet	51 of 51

A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



Place Components Close to BGA

<20> STRAP2
 <20> STRAP1
 <20> STRAP0
 <20> ROM_SCLK
 <20> ROM_SI
 <20> ROM_SO



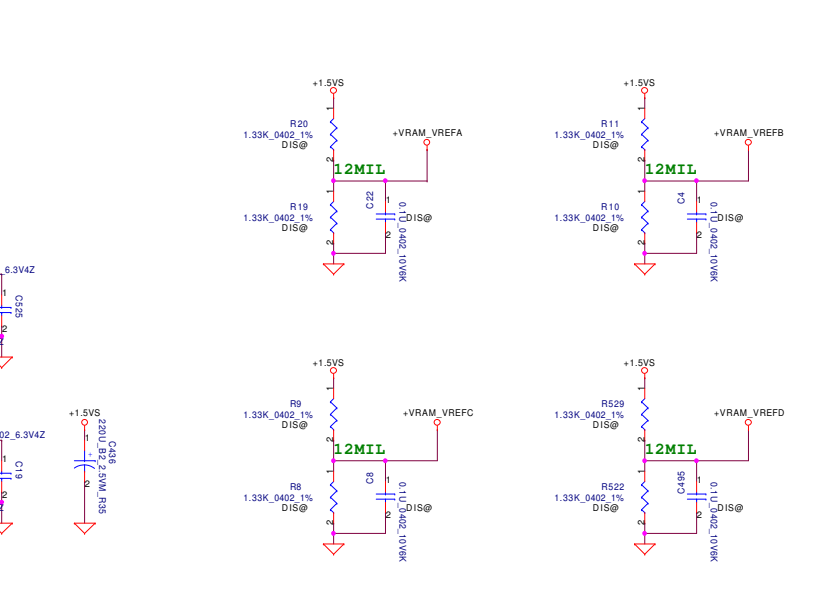
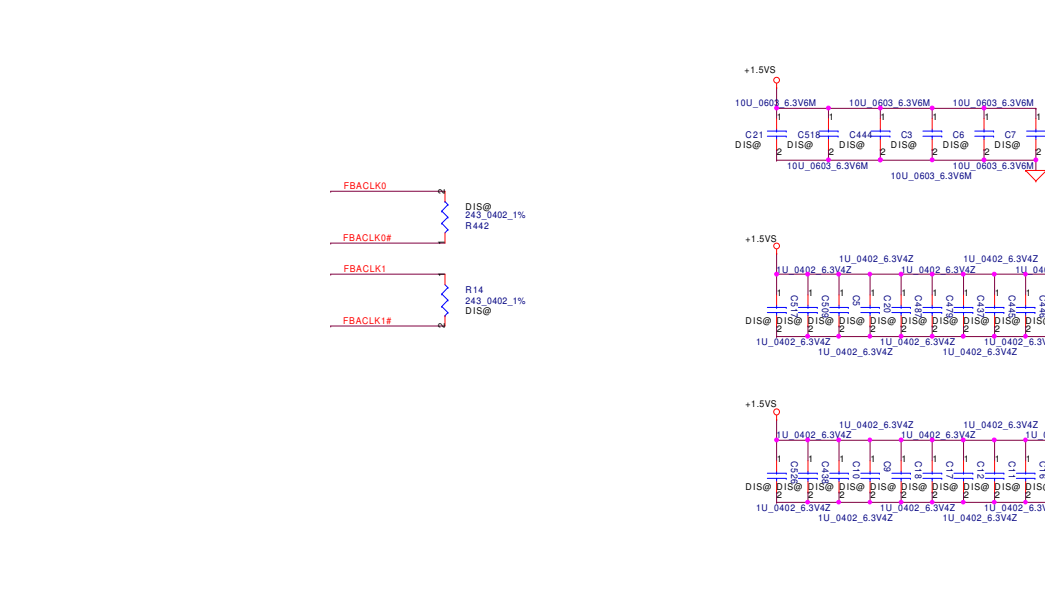
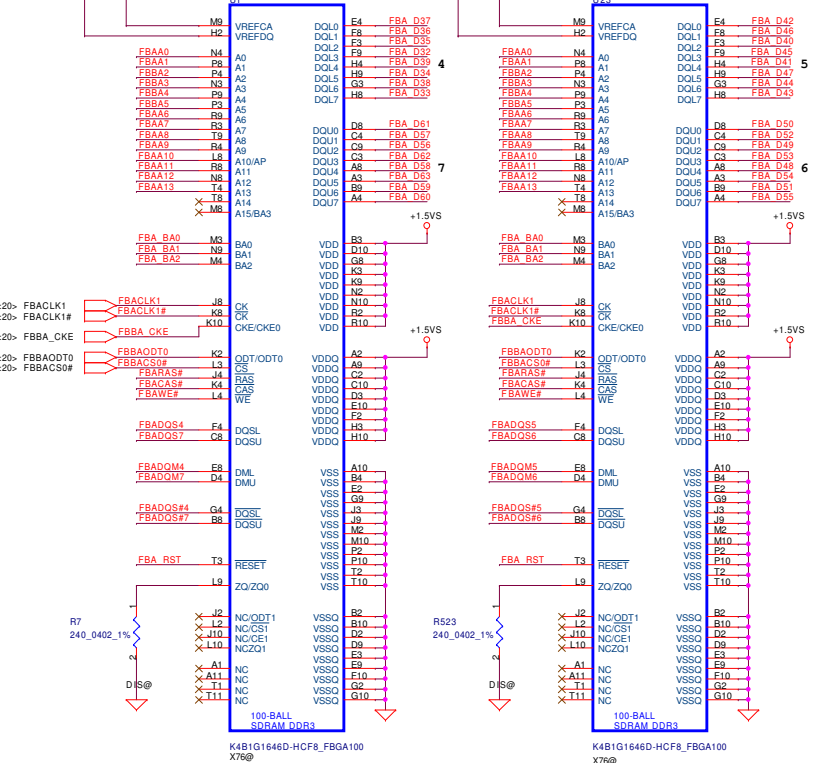
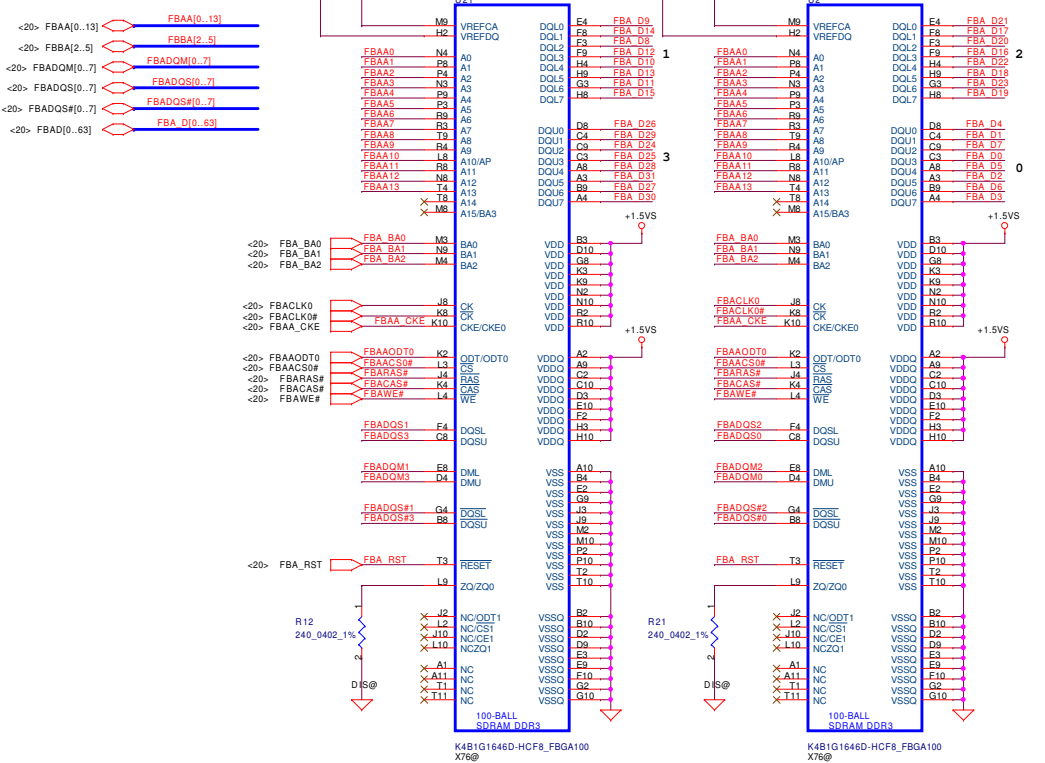
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
	64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
Hynix 800MHz	H5TQ1G63BFR-12C						
	64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
				X76			

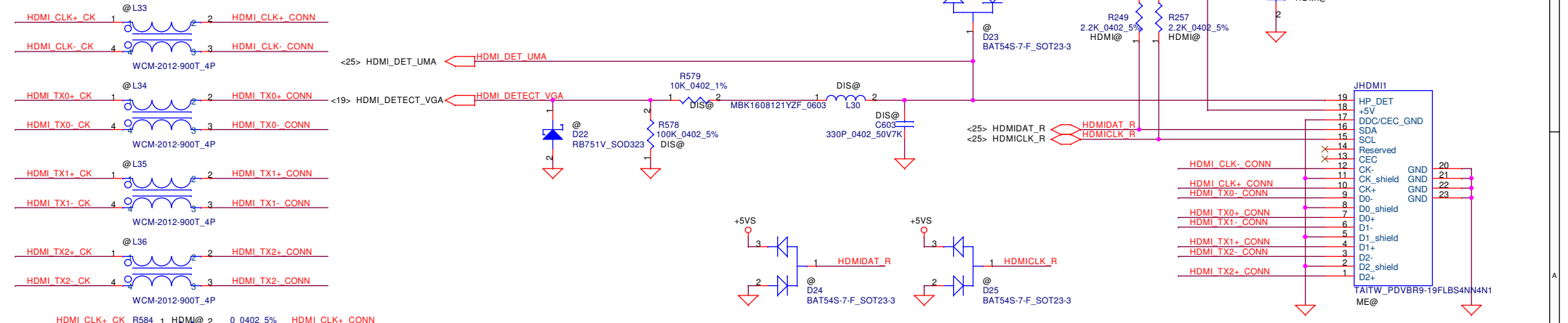
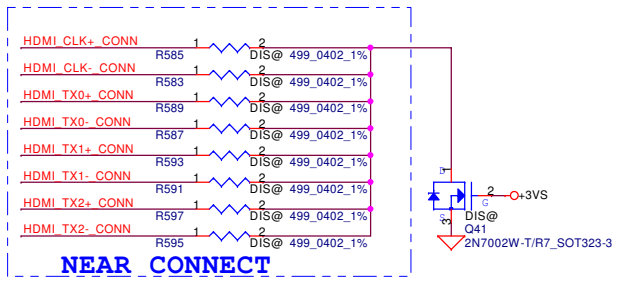
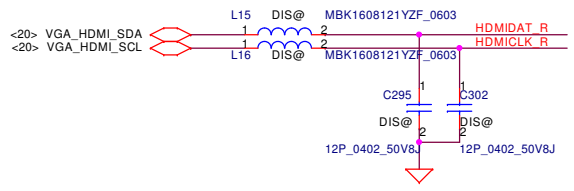
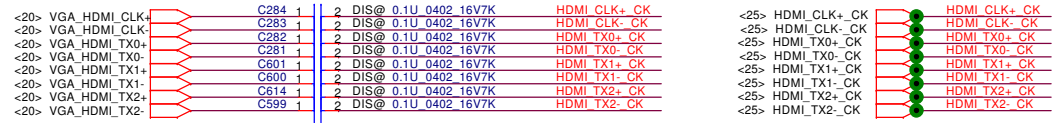
N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



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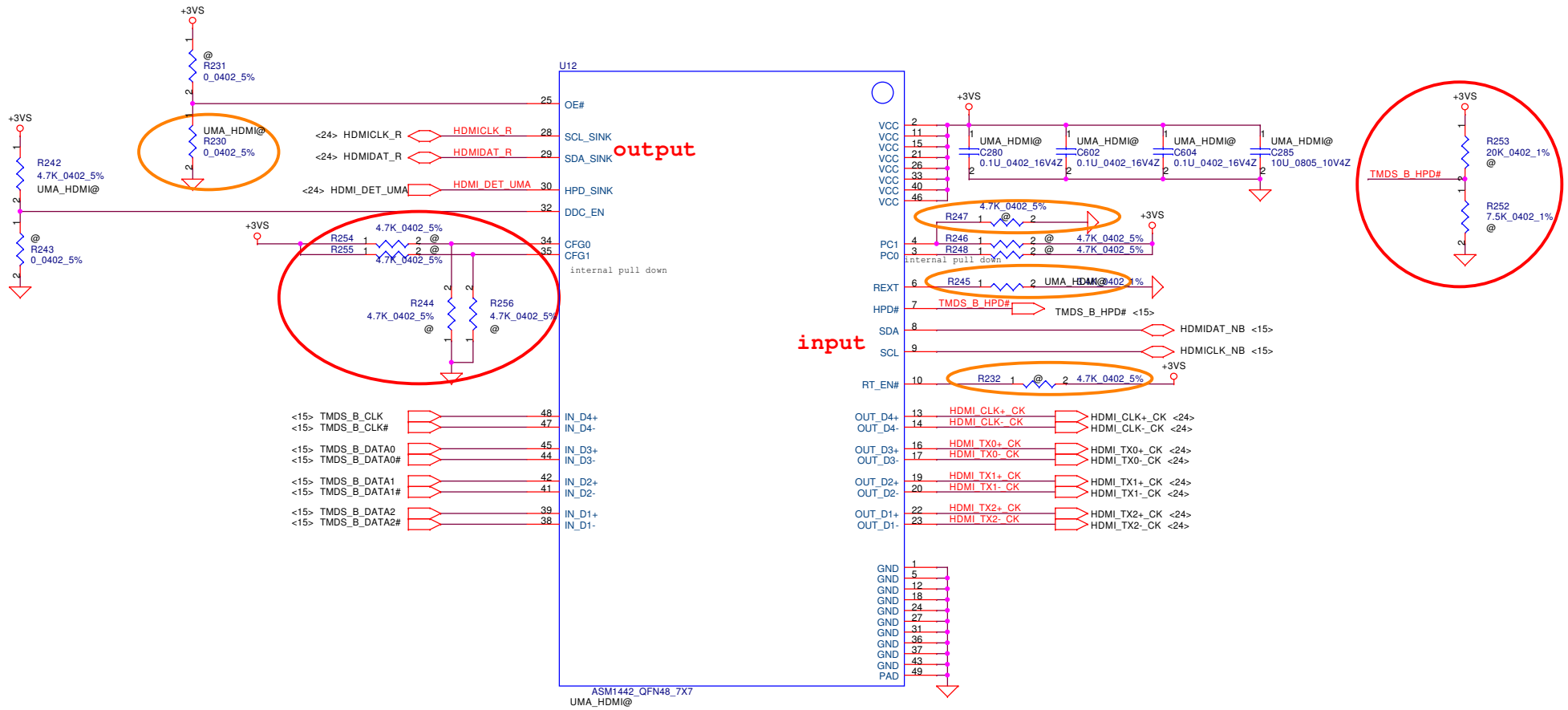
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDMI CONN	
2008/03/25		2008/04/		LA-5752P	
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Size	Document Number	Date: Thursday, October 29, 2009		Sheet	Rev
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				of	51

P/N:SA00003GT00 (ASM1442)

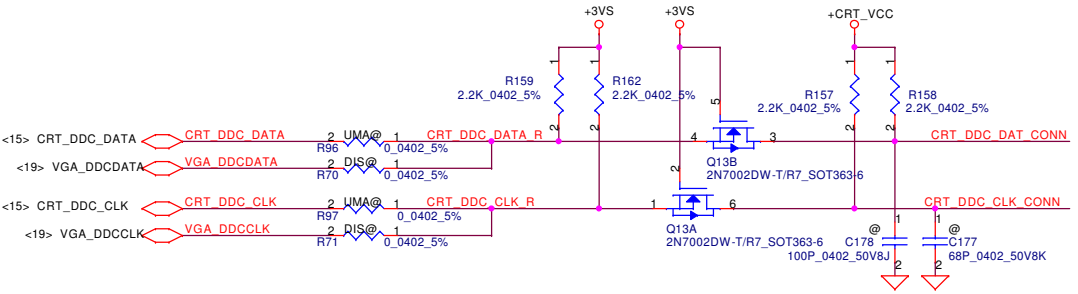
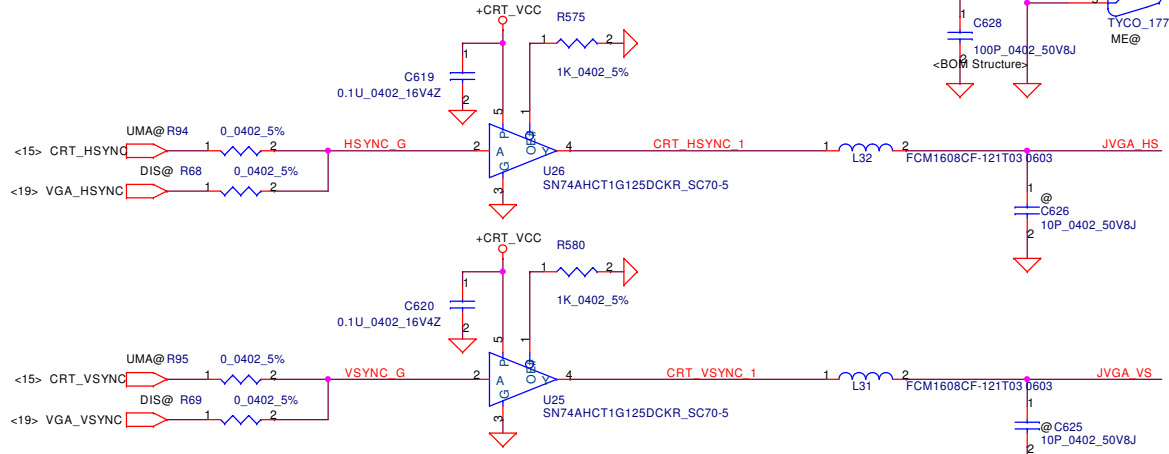
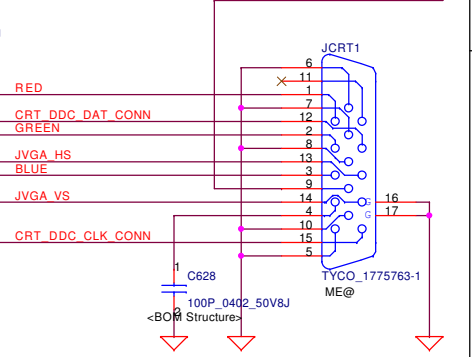
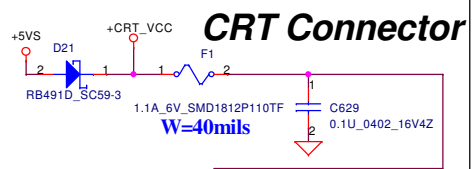
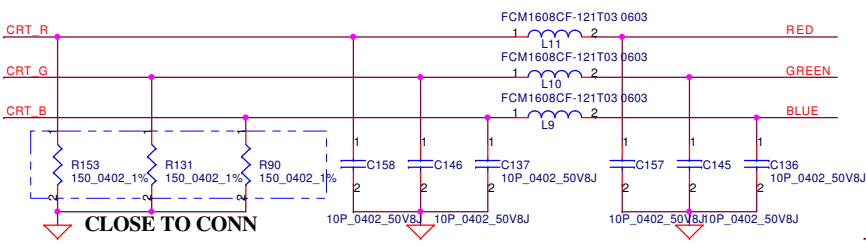
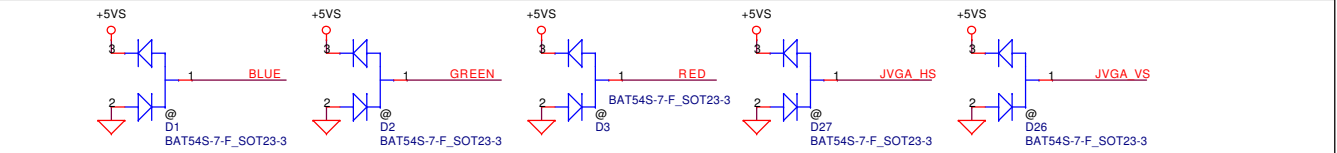
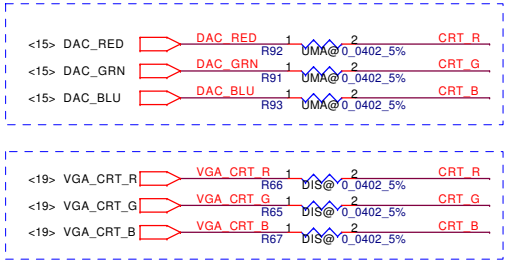
P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm

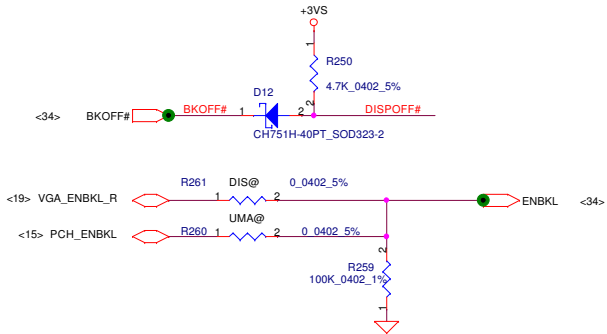
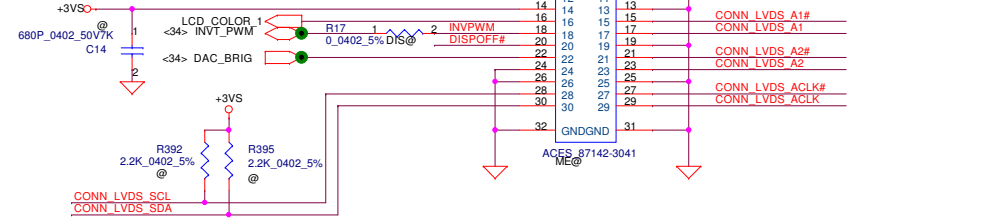
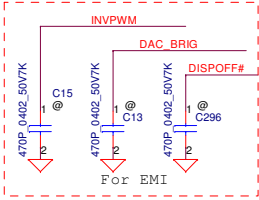
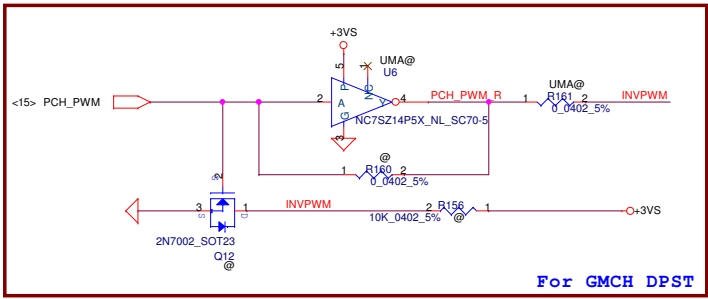
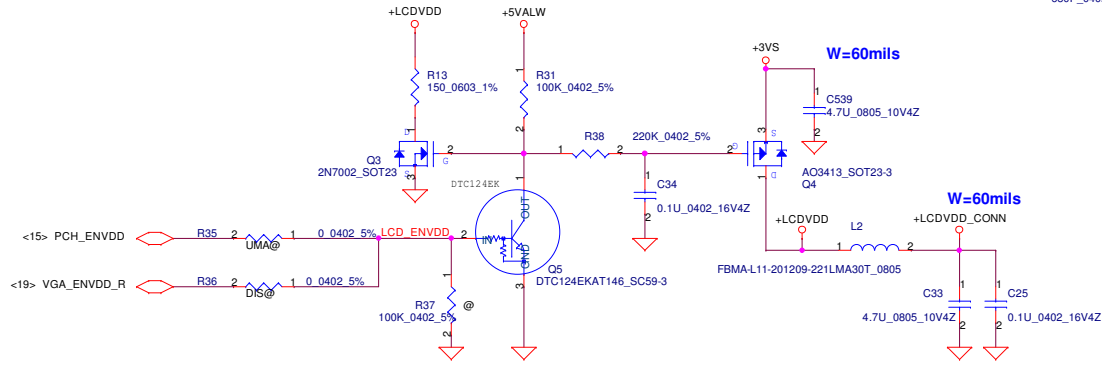


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				Rev	0.3



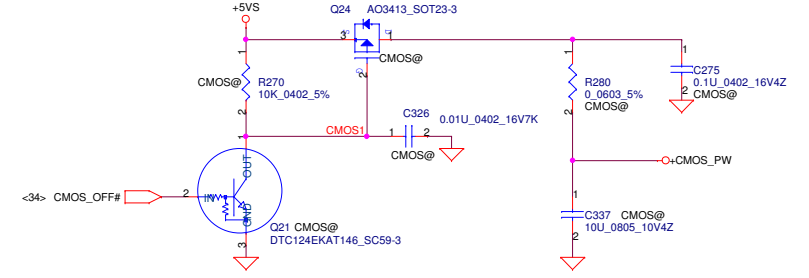
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Size	Document Number	Rev		0.3	
Custom	LA-5752P				
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LCD POWER CIRCUIT



<19> VGA_LVDS_SCL	VGA_LVDS_SCL	0.0402_5%	2	DIS@	1	R390	CONN_LVDS_SCL
<19> VGA_LVDS_SDA	VGA_LVDS_SDA	0.0402_5%	2	DIS@	1	R391	CONN_LVDS_SDA
<20> VGA_LVDS_A0	VGA_LVDS_A0	0.0402_5%	2	DIS@	1	R86	CONN_LVDS_A0
<20> VGA_LVDS_A0#	VGA_LVDS_A0#	0.0402_5%	2	DIS@	1	R85	CONN_LVDS_A0#
<20> VGA_LVDS_A1	VGA_LVDS_A1	0.0402_5%	2	DIS@	1	R150	CONN_LVDS_A1
<20> VGA_LVDS_A1#	VGA_LVDS_A1#	0.0402_5%	2	DIS@	1	R128	CONN_LVDS_A1#
<20> VGA_LVDS_A2	VGA_LVDS_A2	0.0402_5%	2	DIS@	1	R126	CONN_LVDS_A2
<20> VGA_LVDS_A2#	VGA_LVDS_A2#	0.0402_5%	2	DIS@	1	R127	CONN_LVDS_A2#
<20> VGA_LVDS_ACLK	VGA_LVDS_ACLK	0.0402_5%	2	DIS@	1	R84	CONN_LVDS_ACLK
<20> VGA_LVDS_ACLK#	VGA_LVDS_ACLK#	0.0402_5%	2	DIS@	1	R125	CONN_LVDS_ACLK#
<15> EDID_CLK	EDID_CLK	0.0402_5%	2	UMA@	1	R393	CONN_LVDS_SCL
<15> EDID_DATA	EDID_DATA	0.0402_5%	2	UMA@	1	R394	CONN_LVDS_SDA
<15> LVDS_A0	LVDS_A0	0.0402_5%	2	UMA@	1	R383	CONN_LVDS_A0
<15> LVDS_A0#	LVDS_A0#	0.0402_5%	2	UMA@	1	R382	CONN_LVDS_A0#
<15> LVDS_A1	LVDS_A1	0.0402_5%	2	UMA@	1	R389	CONN_LVDS_A1
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<15> LVDS_A2	LVDS_A2	0.0402_5%	2	UMA@	1	R386	CONN_LVDS_A2
<15> LVDS_A2#	LVDS_A2#	0.0402_5%	2	UMA@	1	R387	CONN_LVDS_A2#
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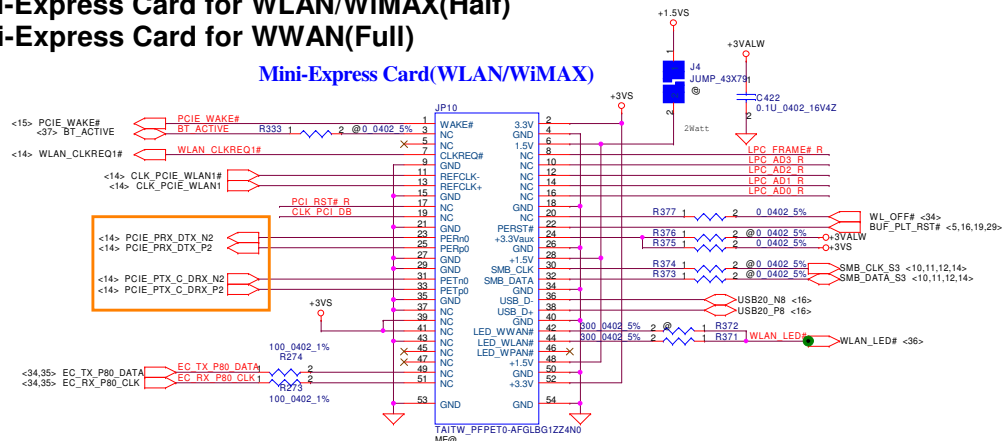
CMOS Camera



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Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for WWAN(Full)

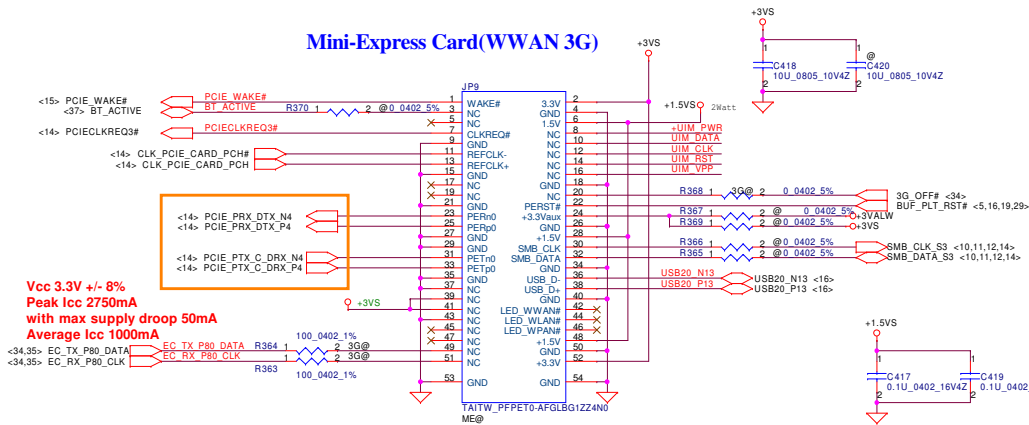
Mini-Express Card(WLAN/WiMAX)



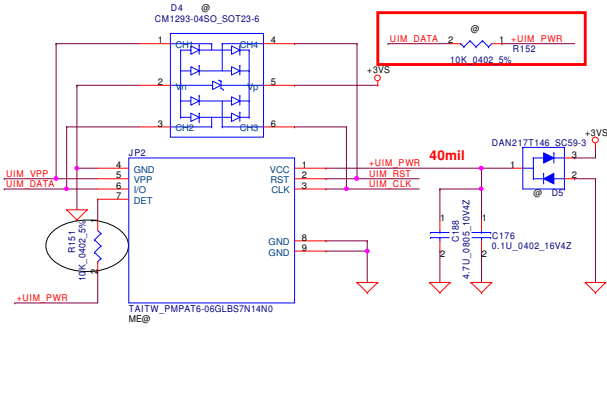
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R284	1	2 @ 0.0402 5%	LPC_FRAME#	LPC_FRAME# <13,34>
LPC_AD3 R	R285	1	2 @ 0.0402 5%	LPC_AD3	LPC_AD3 <13,34>
LPC_AD2 R	R286	1	2 @ 0.0402 5%	LPC_AD2	LPC_AD2 <13,34>
LPC_AD1 R	R287	1	2 @ 0.0402 5%	LPC_AD1	LPC_AD1 <13,34>
LPC_ADD0 R	R288	1	2 @ 0.0402 5%	LPC_ADD0	LPC_ADD0 <13,34>
PCI_RST# R	R290	1	2 @ 0.0402 5%	PCI_RST#	PCI_RST# <16,34>
CLK_PCI_DB				CLK_PCI_DB	CLK_PCI_DB <14>

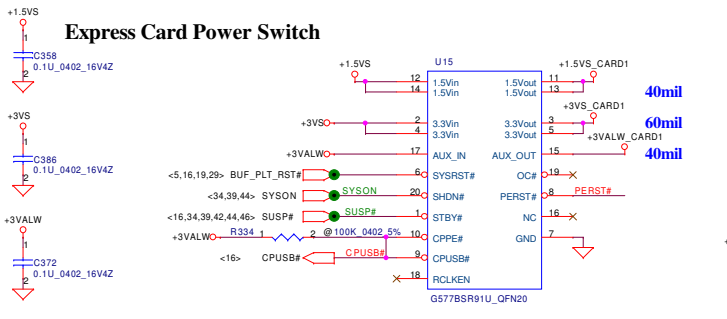
Mini-Express Card(WWAN 3G)



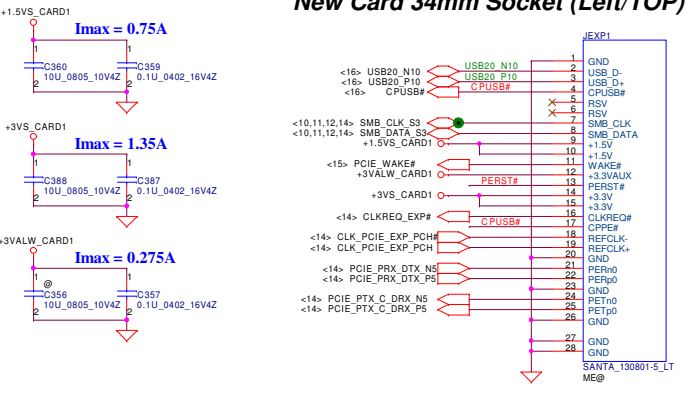
Vcc 3.3V +/- 0%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



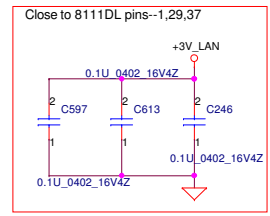
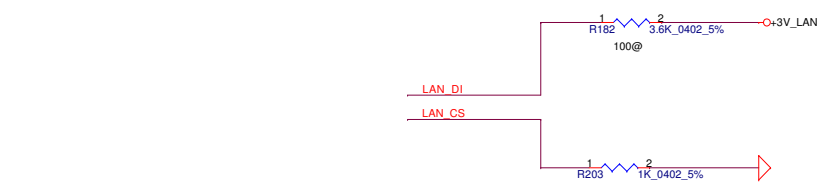
Express Card Power Switch



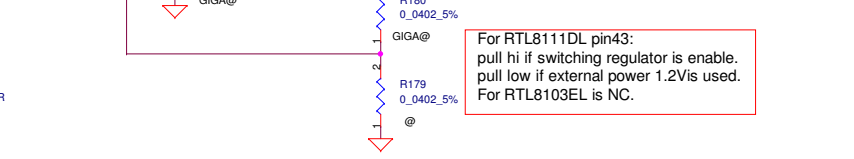
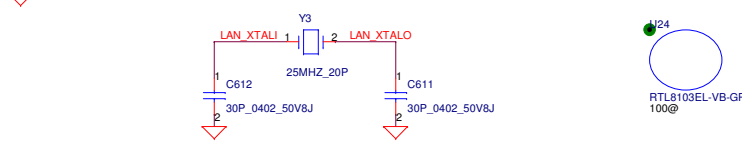
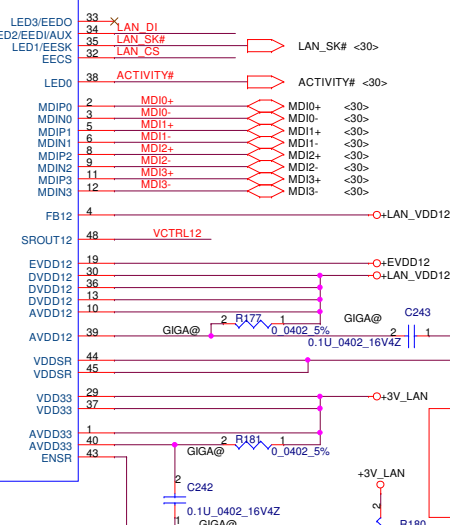
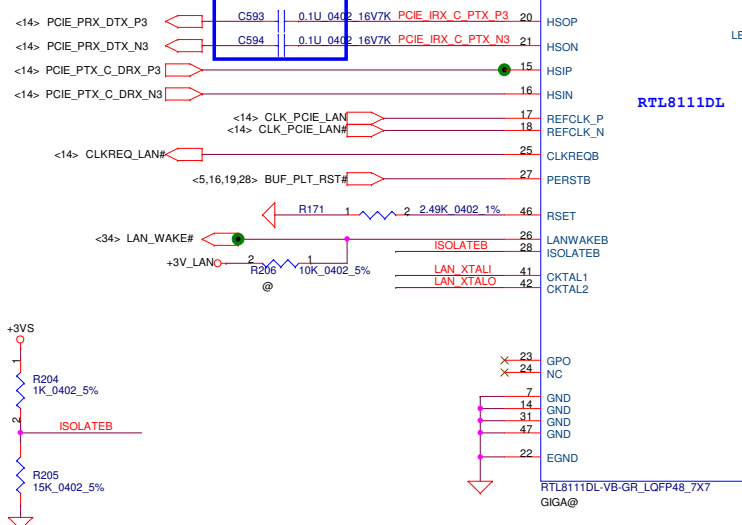
New Card 34mm Socket (Left/TOP)



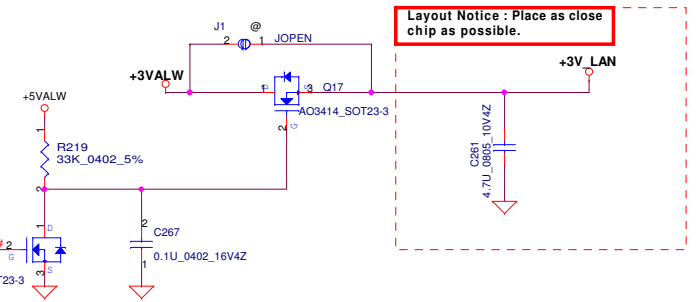
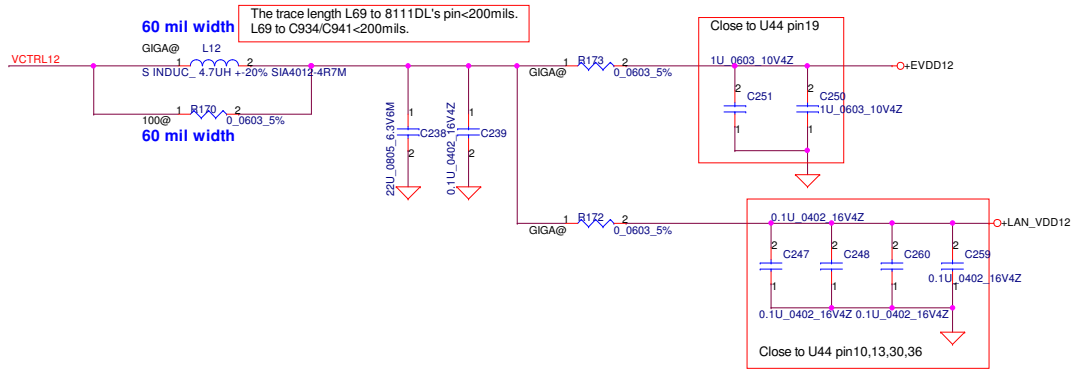
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	LA-5752P		Rev
Date:	Thursday, October 29, 2009	Sheet	28	of 51



Place Close to Chip



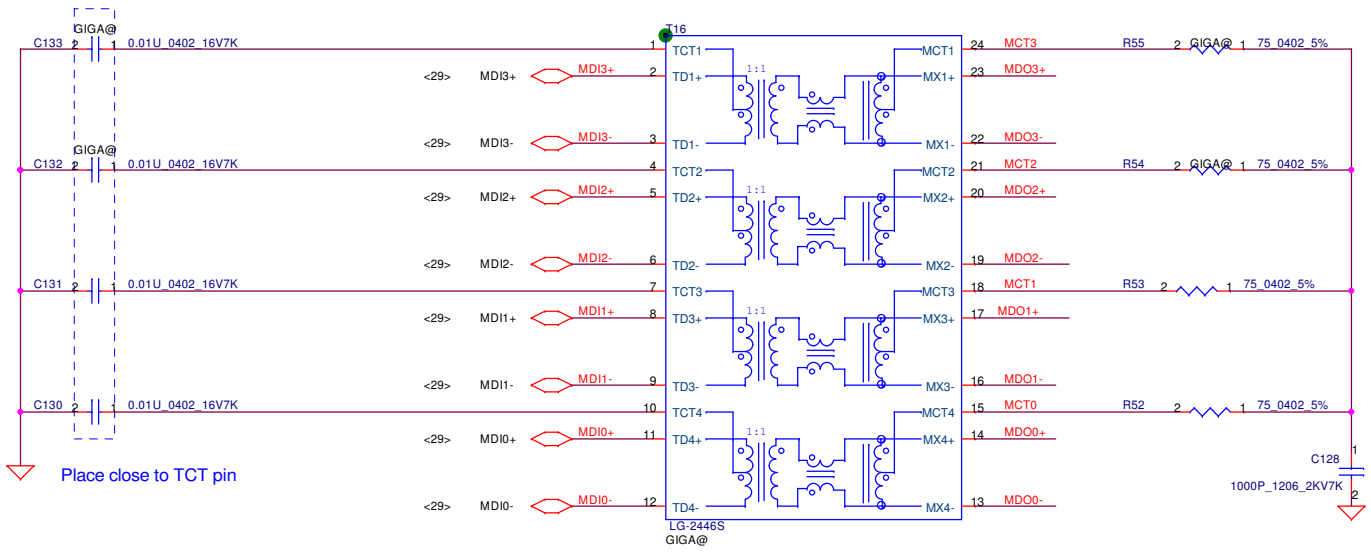
For RTL8111DL pin43:
pull hi if switching regulator is enable.
pull low if external power 1.2Vis used.
For RTL8103EL is NC.



Layout Notice : Place as close
chip as possible.

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	RTL8103EL
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				Document Number LA-5752P
				Rev 0.3
				Date: Thursday, October 23, 2009
				Sheet 29 of 51

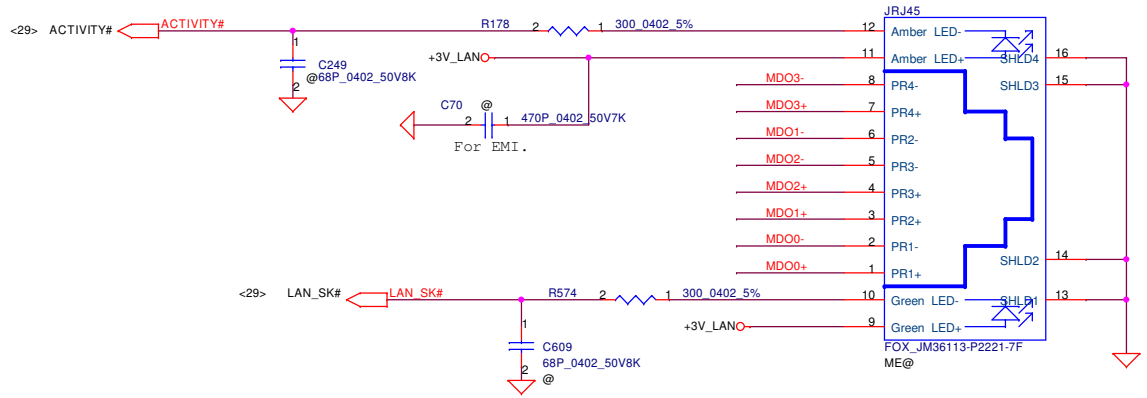
Close to T14



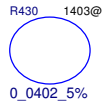
Place close to TCT pin



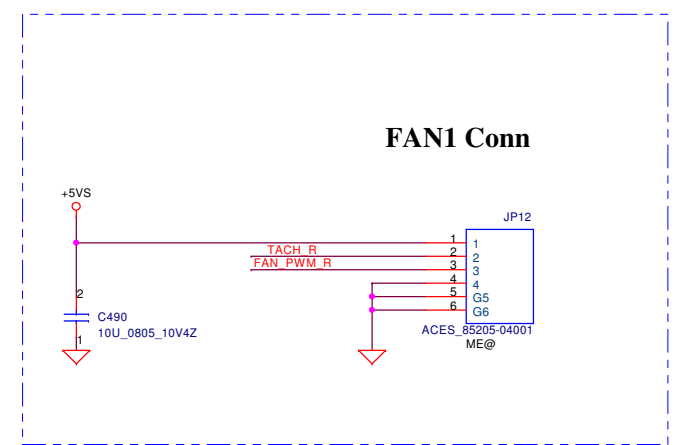
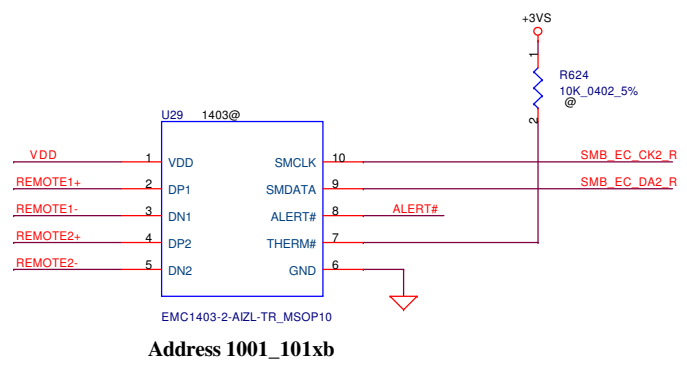
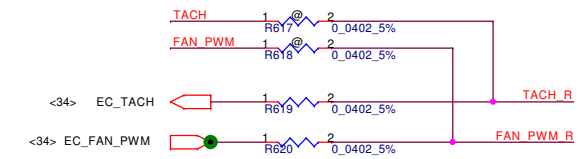
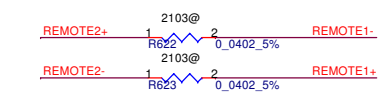
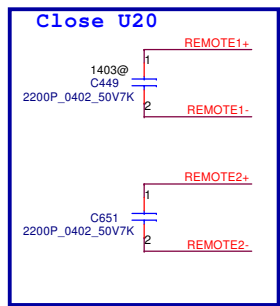
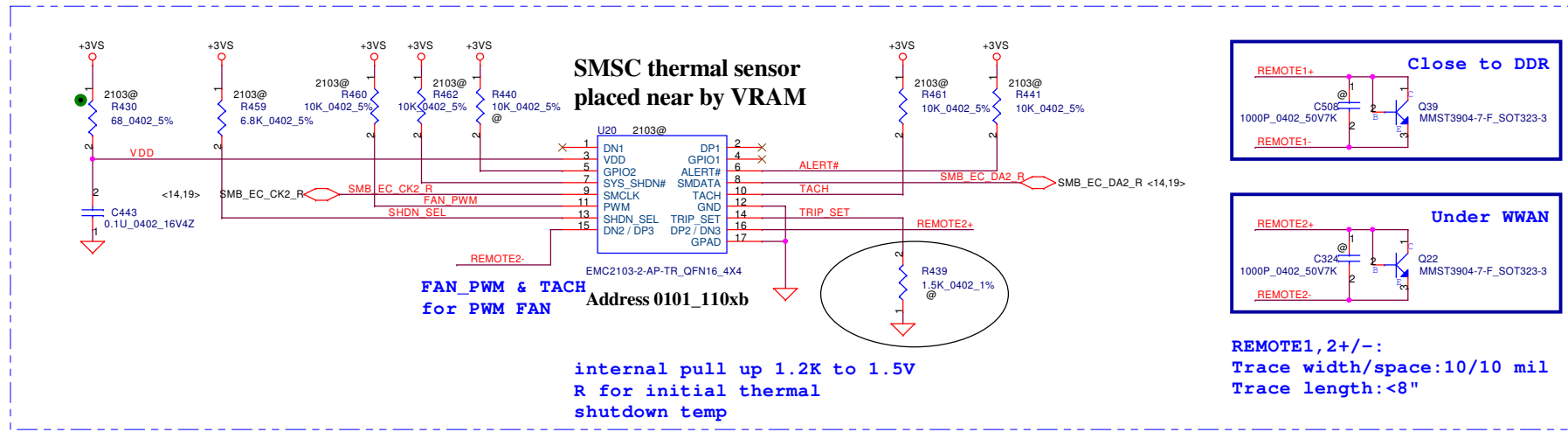
RJ45 Conn.



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Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
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Size	Custom	Document Number	LA-5752P	Rev	0.3
Date:	Thursday, October 29, 2009	Sheet	30 of 51		



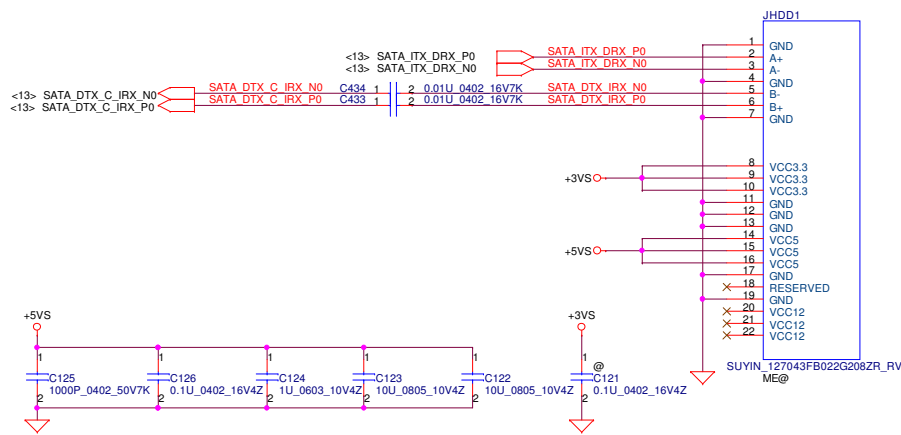
1403:
@C508/@C324=100p



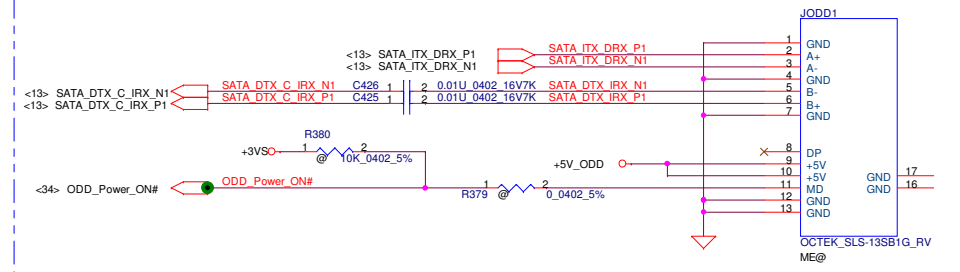
Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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Date: Thursday, October 29, 2009	Sheet 31	of 51	Rev 0.3		

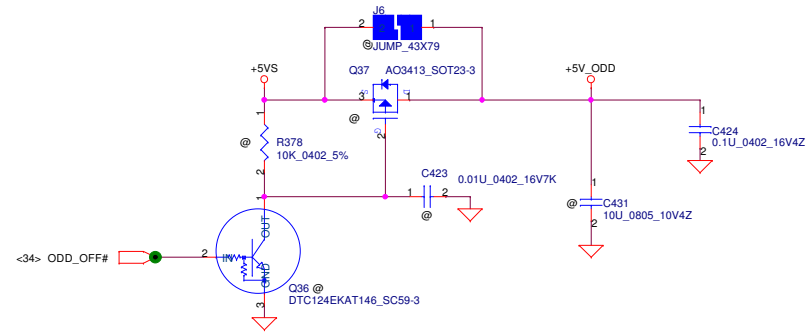
SATA HDD Conn.



SATA ODD Conn.

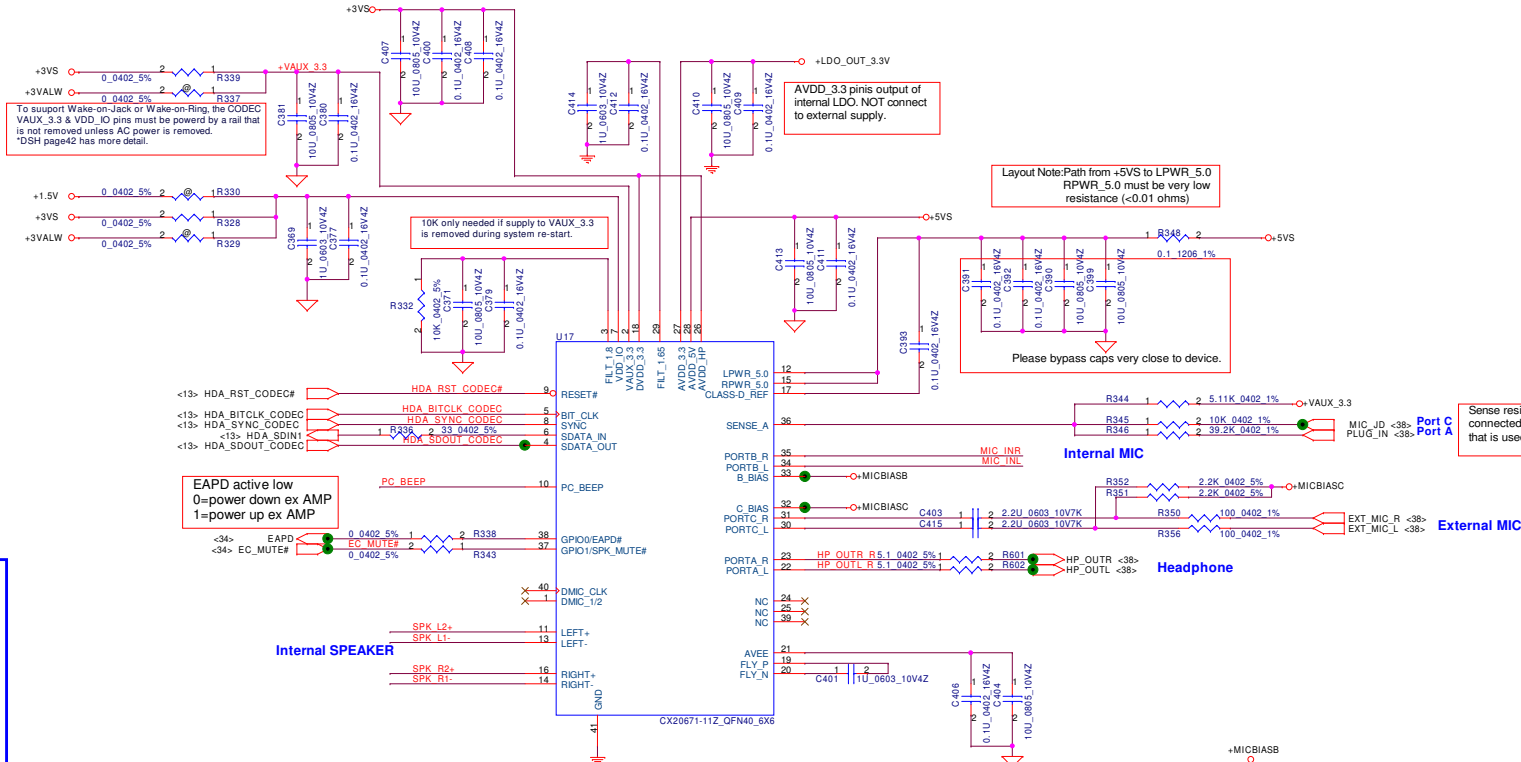
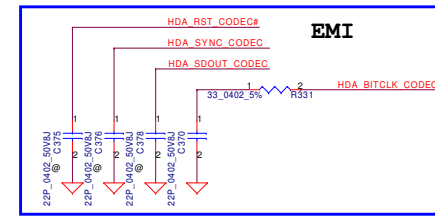


ODD Power Control



Security Classification	Compal Secret Data			Title		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.		
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				LA-5752P		
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



To support Wake-on-Lack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powered by a rail that is not removed unless AC power is removed.
 *DSH page42 has more detail.

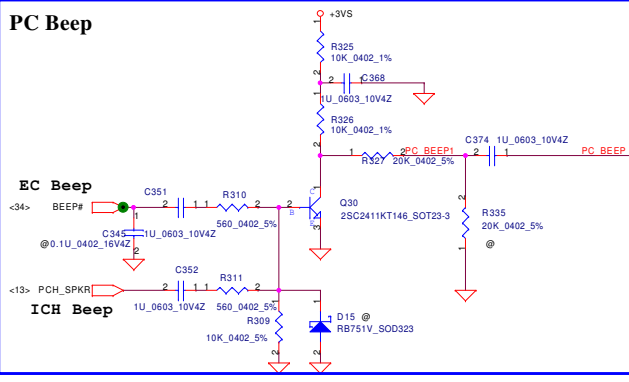
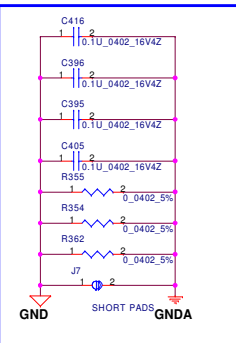
AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

Layout Note: Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

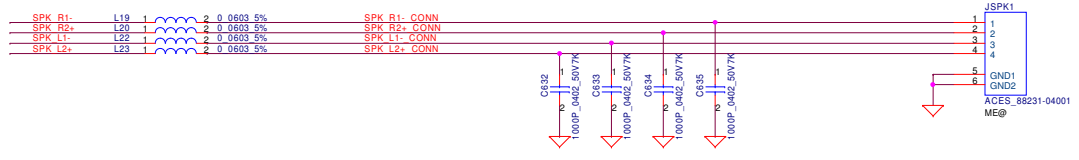
Please bypass caps very close to device.

Sense resistors must be connected same power that is used for VAUX_3.3

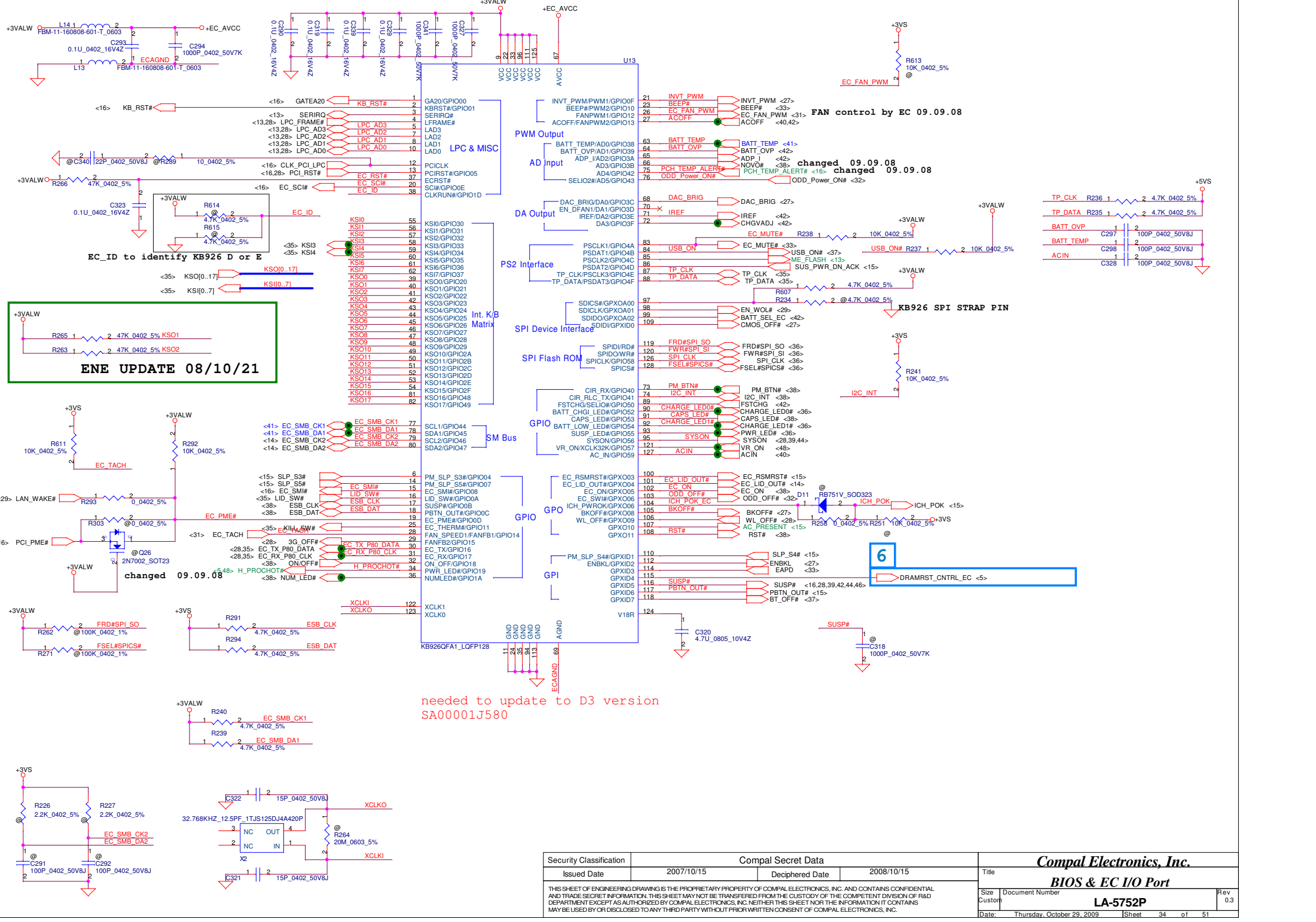
EAPD active low
 0=power down ex AMP
 1=power up ex AMP



wide 20MIL



Security Classification	Compal Secret Data		Title	
Issued Date	2008/03/25	Deciphered Date	2008/04/	CX20671 Codec
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				Document Number
				LA-5752P
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				0.3
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				Sheet 33 of 51



Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	BIOS & EC I/O Port
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Size	Document Number	Rev		
Custom	LA-5752P	0.3		
Date:	Thursday, October 29, 2009	Sheet	34	of 51

Compal Electronics, Inc.

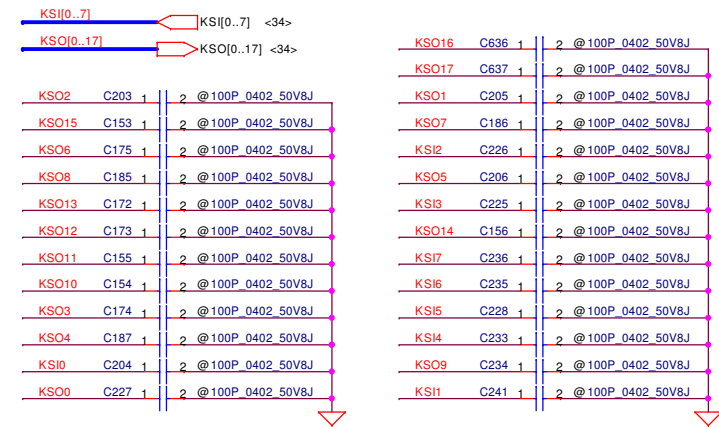
BIOS & EC I/O Port

LA-5752P

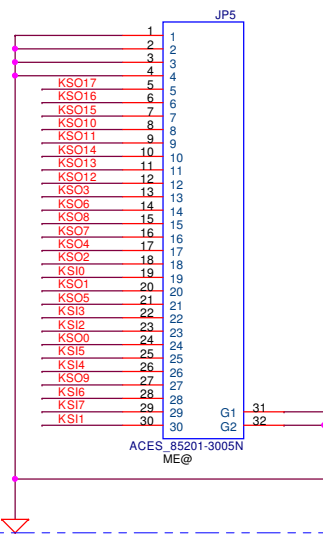
Rev 0.3

Date: Thursday, October 29, 2009 Sheet 34 of 51

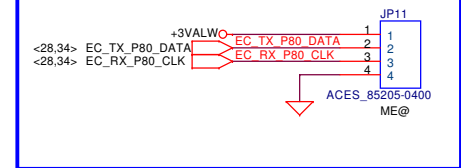
INT_KBD Conn.



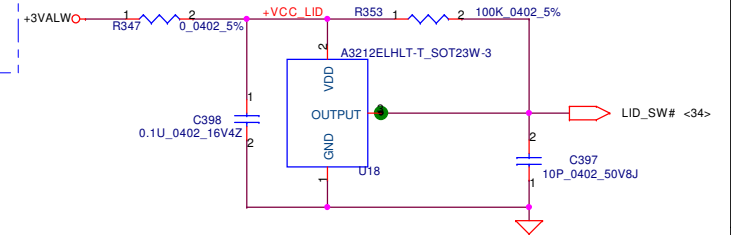
reversal of NIWE1



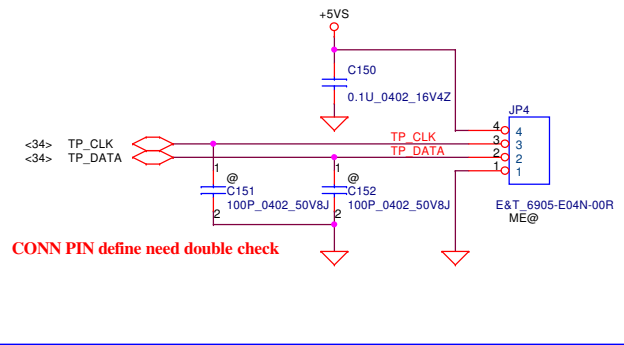
EC DEBUG PORT



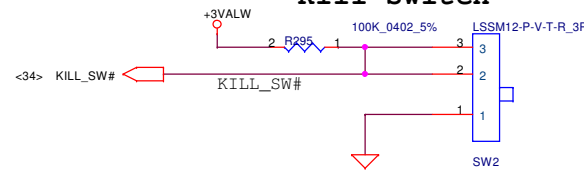
Lid Switch



To TP/B Conn.



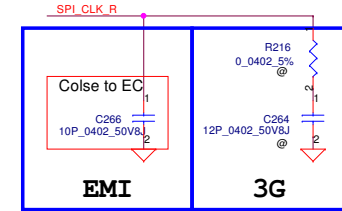
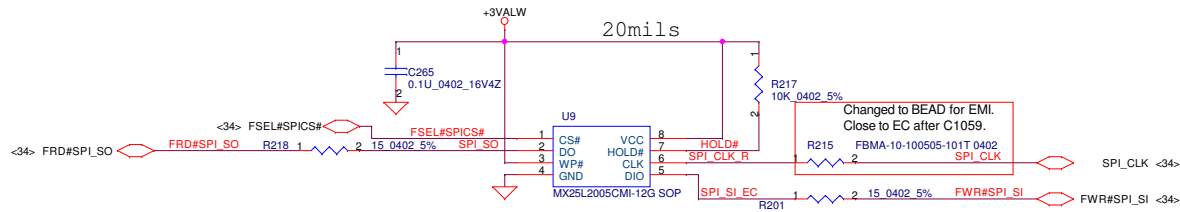
Kill Switch



Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

**FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00**

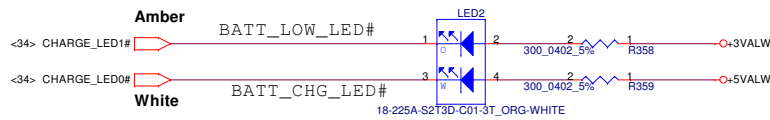


LED

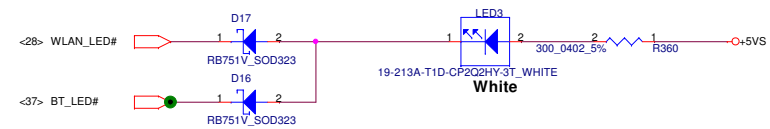
SC500005B00



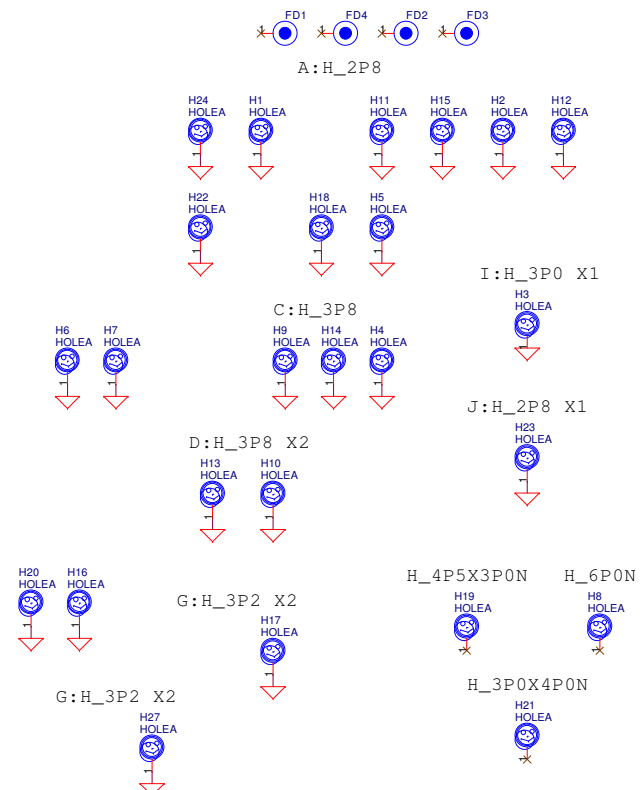
SC500006M00



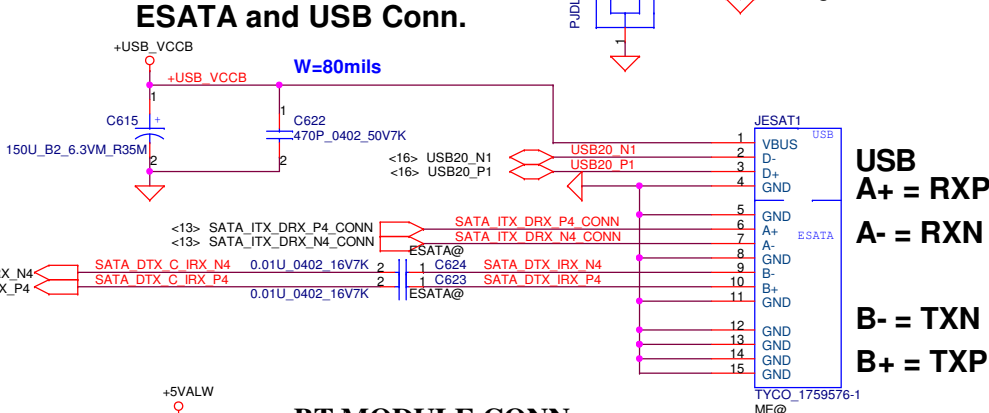
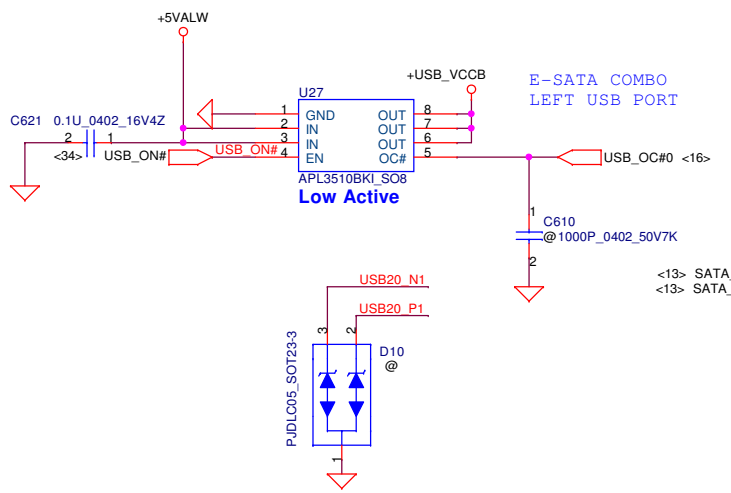
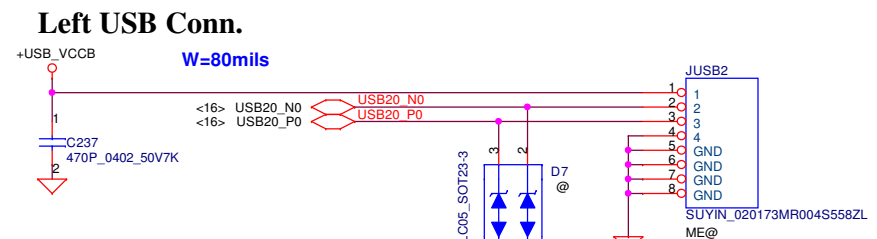
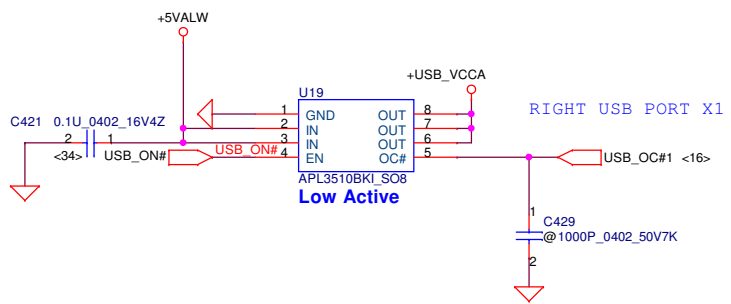
SC500005B00



SC500005B00



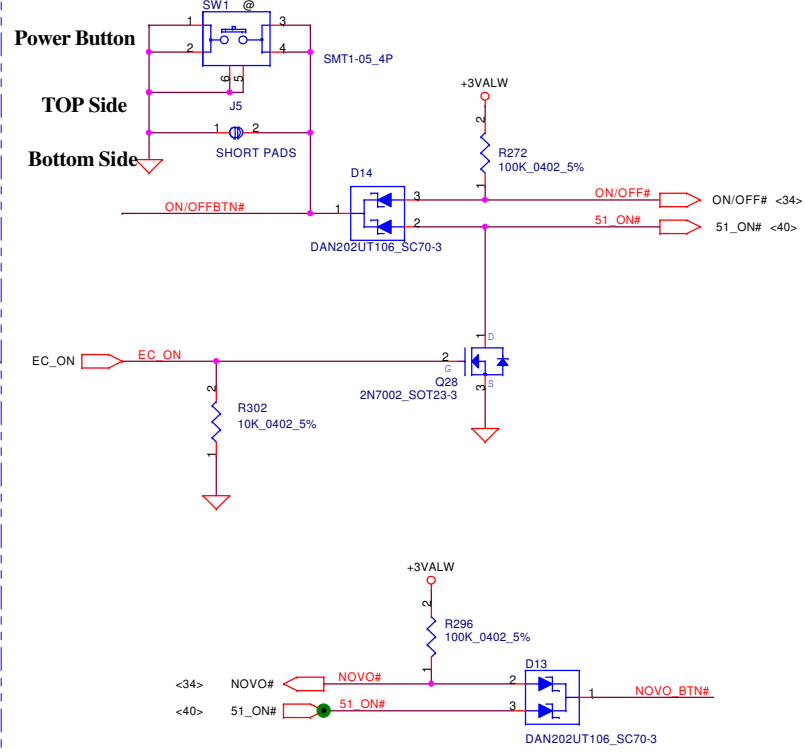
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Issued Date	2007/10/15	Deciphered Date			2008/10/15
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Size	Document Number		Rev		
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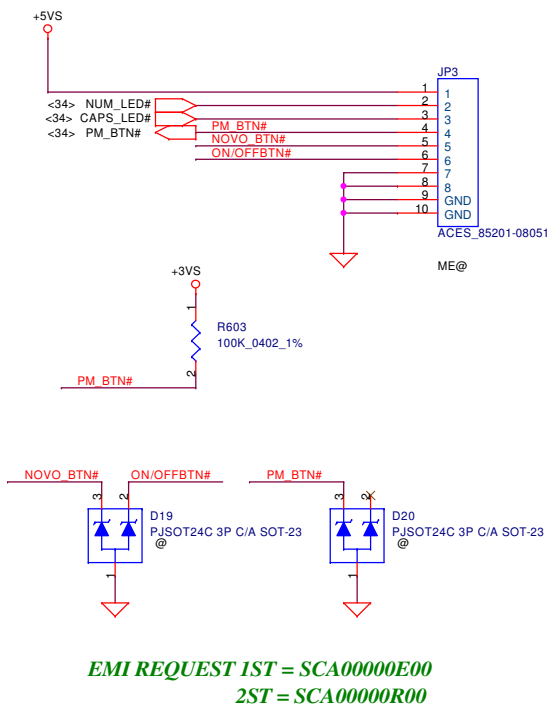
USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

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Date:	Thursday, October 29, 2009	Sheet:	37 of 51	

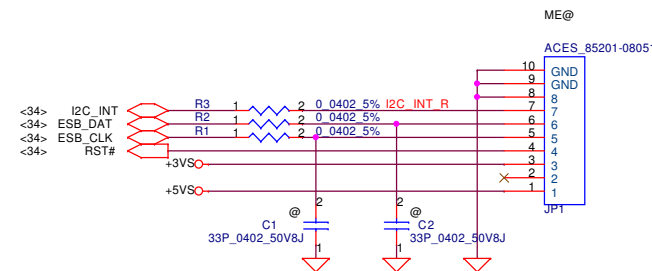
ON/OFF switch



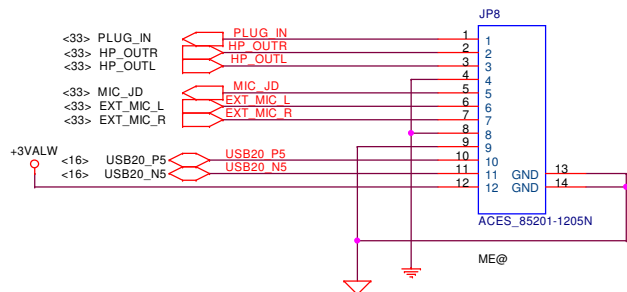
Power Bottom Board Conn. 8pin



Cap Sensor Board Conn. 6pin ENE SB3534

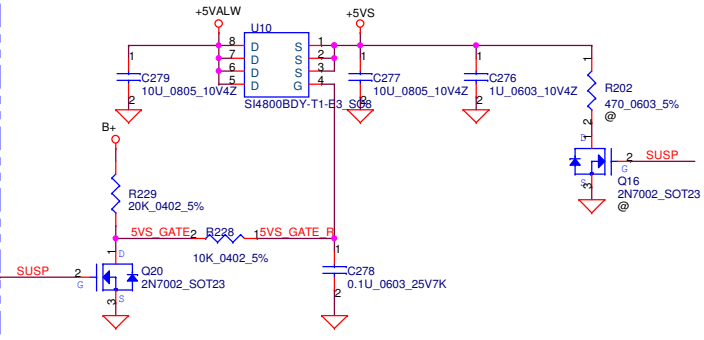


Card Reader/Audio Jack SB CONN

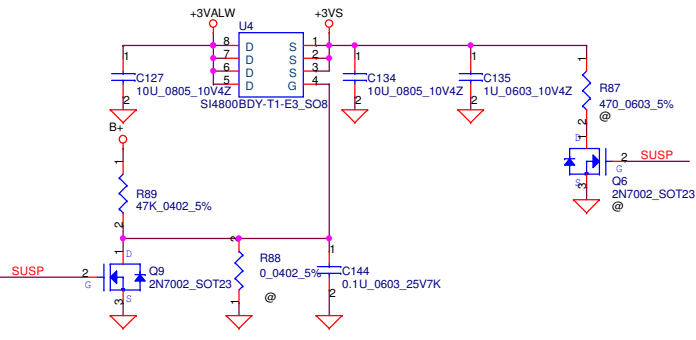


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Audio Jack & SW connector
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				Document Number LA-5752P
				Rev 0.3
Date: Thursday, October 29, 2009		Sheet 38 of 51		

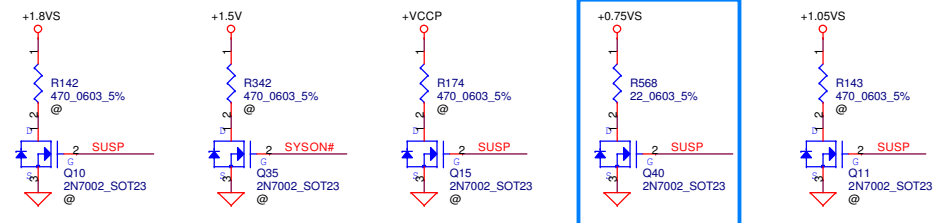
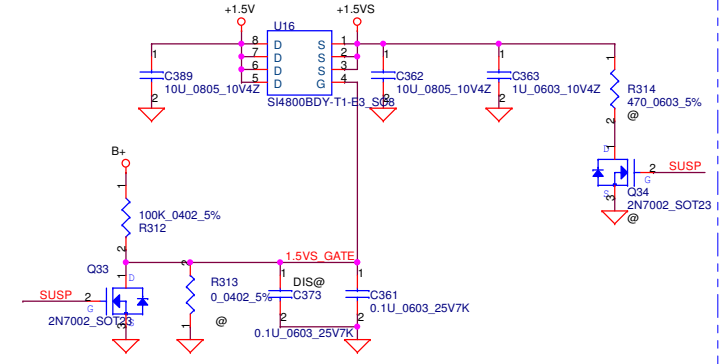
+5VALW TO +5VS



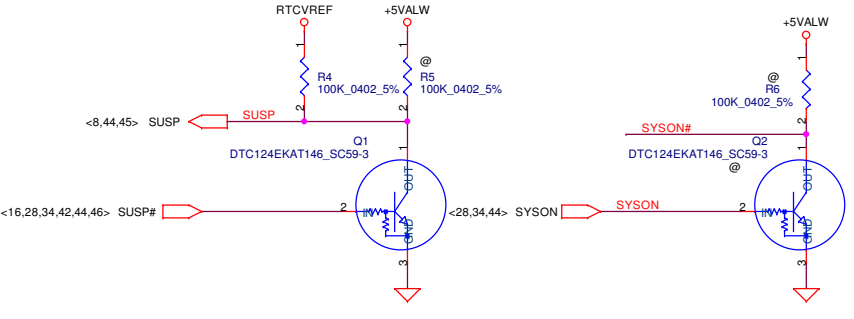
+3VALW TO +3VS



+1.5V to +1.5VS



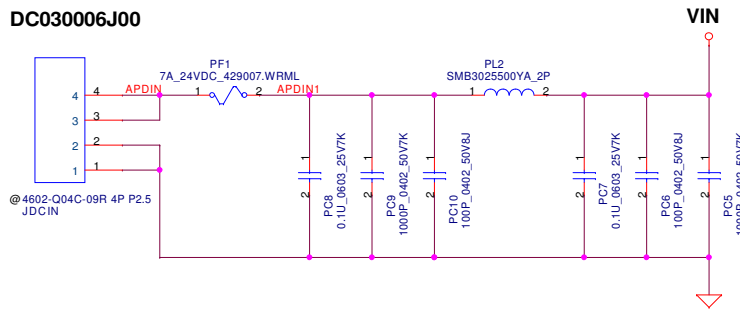
For Intel S3 Power Reduction.



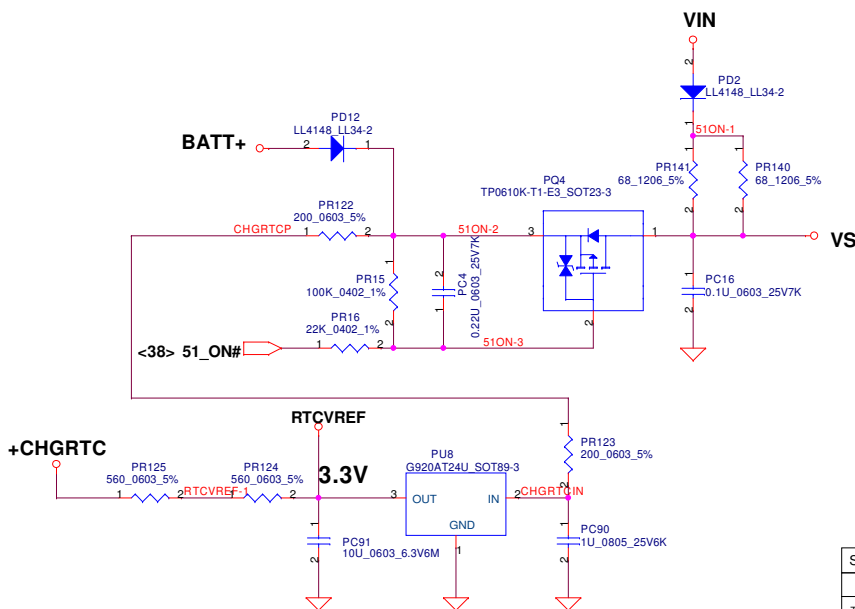
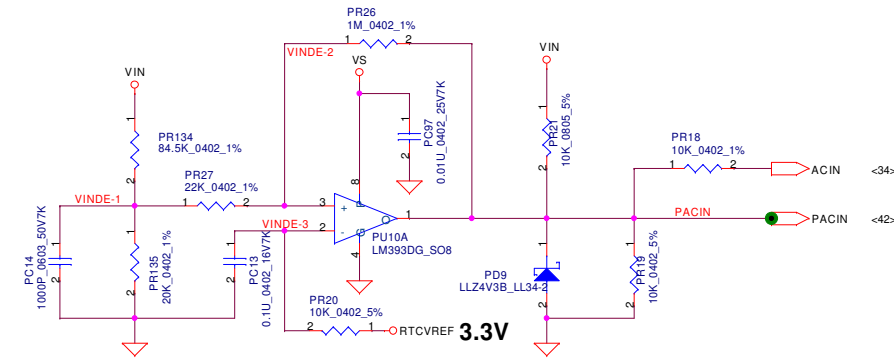
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2006/08/18	Deciphered Date		2007/8/18
Title DC Interface					
Size		Document Number		Rev	
Custom		LA-5752P		0.3	
Date: Thursday, October 29, 2009 Sheet 39 of 51					

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DC030006J00

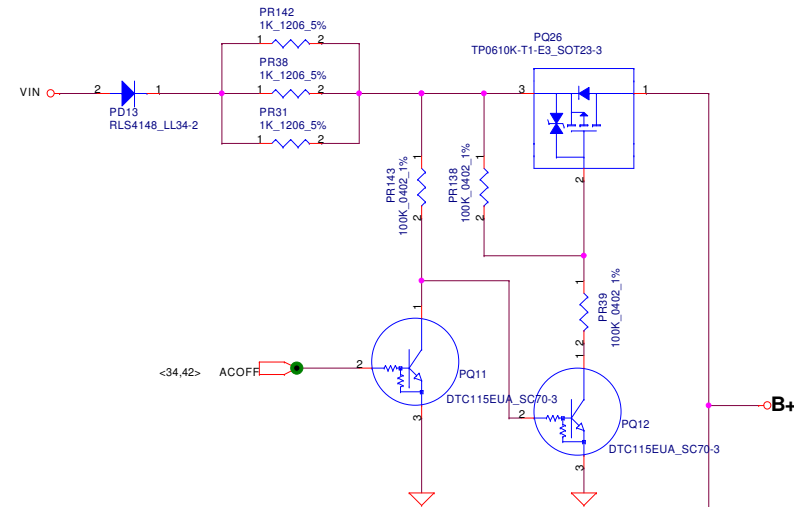


Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



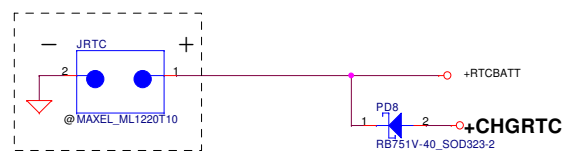
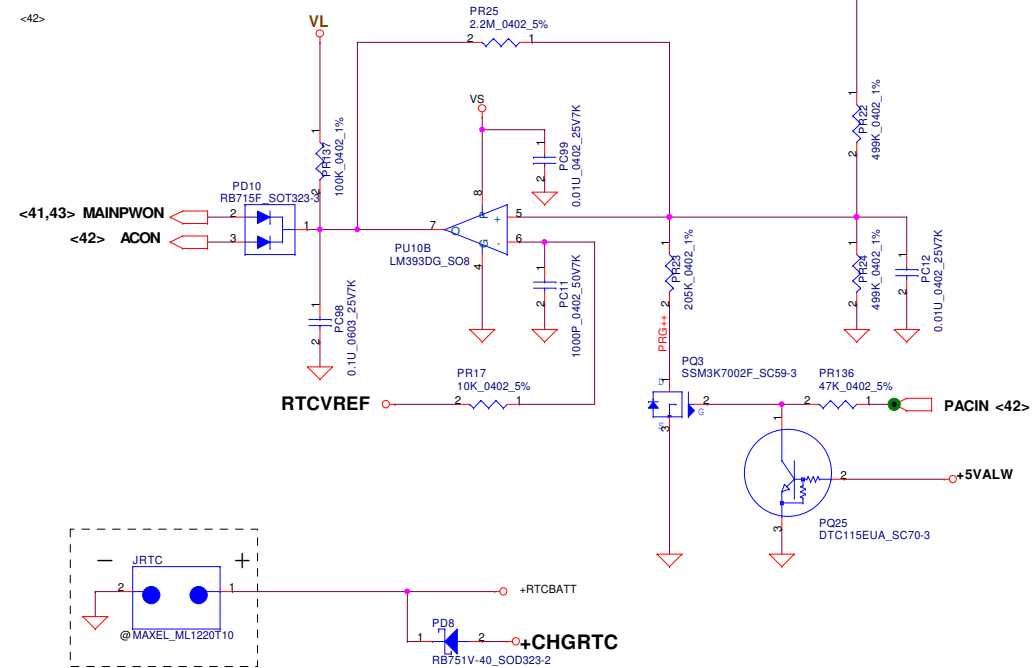
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

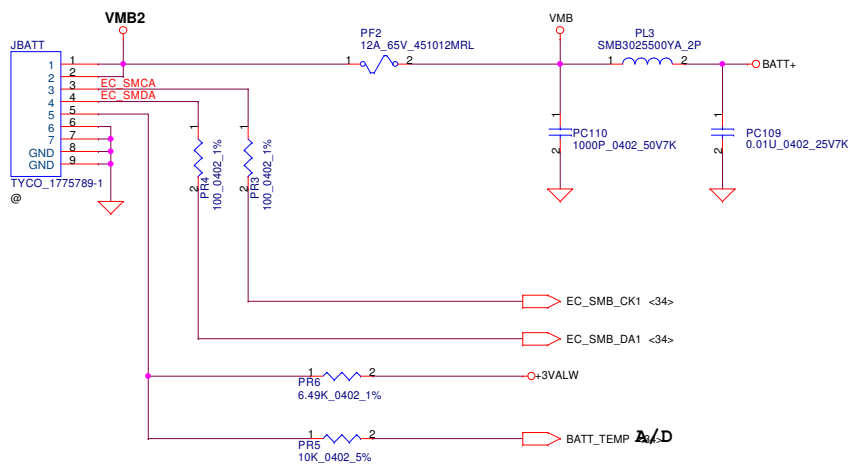


BATT ONLY

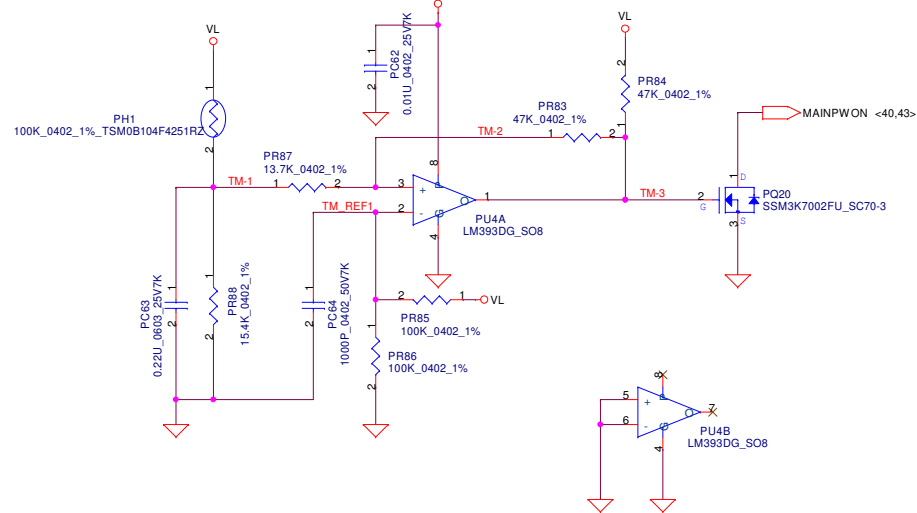
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



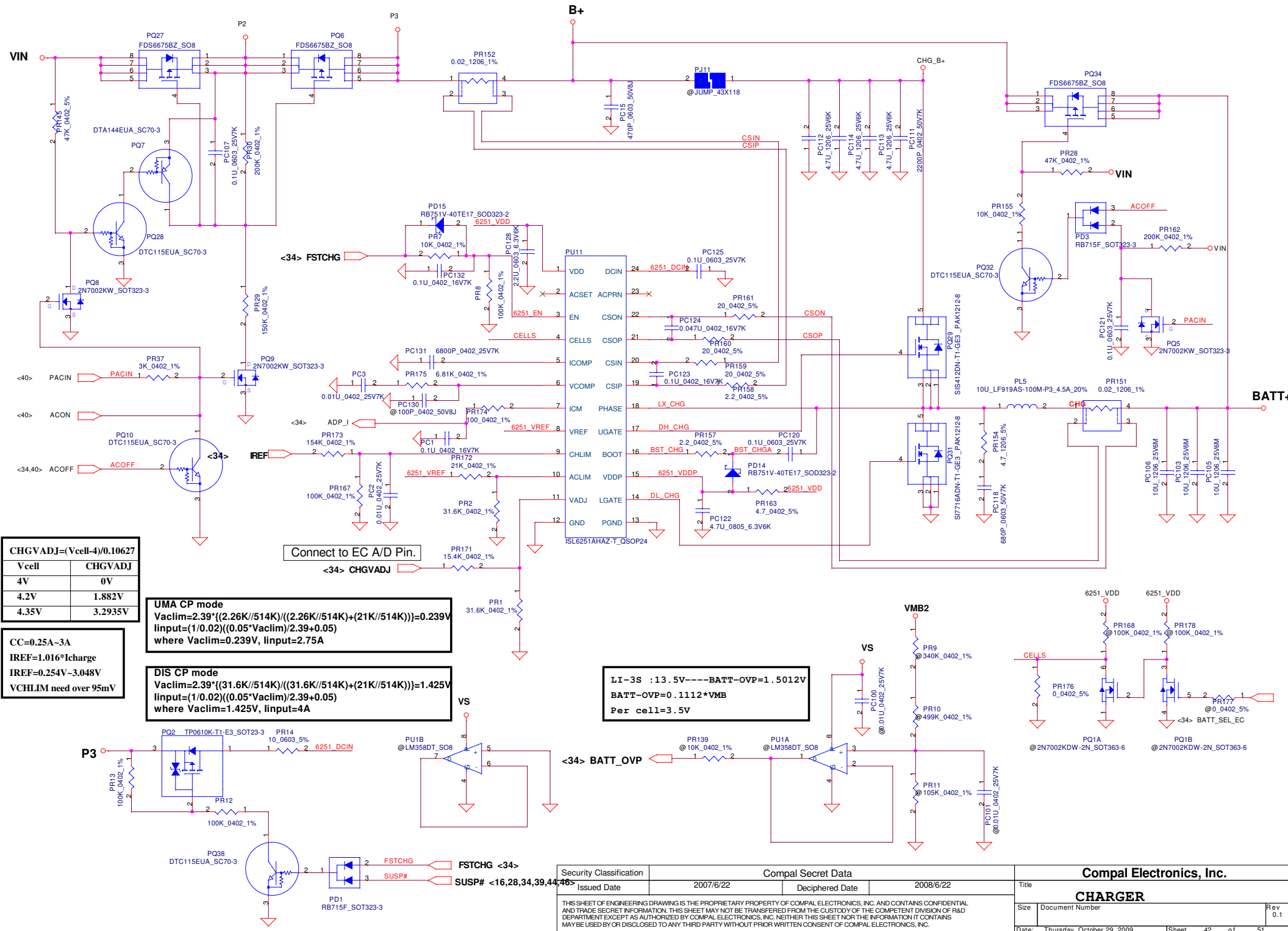
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title	DCIN & DETECTOR
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V-3.048V
VCHLIM need over 95mV

UMA CP mode
 $Va_{lim}=2.39 \cdot \left(\frac{2.26K/514K}{(2.26K/514K)+(21K/514K)} \right) = 0.239V$
 $I_{in_{put}} = (1/0.02) \cdot \left((0.05 \cdot Va_{lim}) / (2.39+0.05) \right)$
 where $Va_{lim}=0.239V$, $I_{in_{put}}=2.75A$

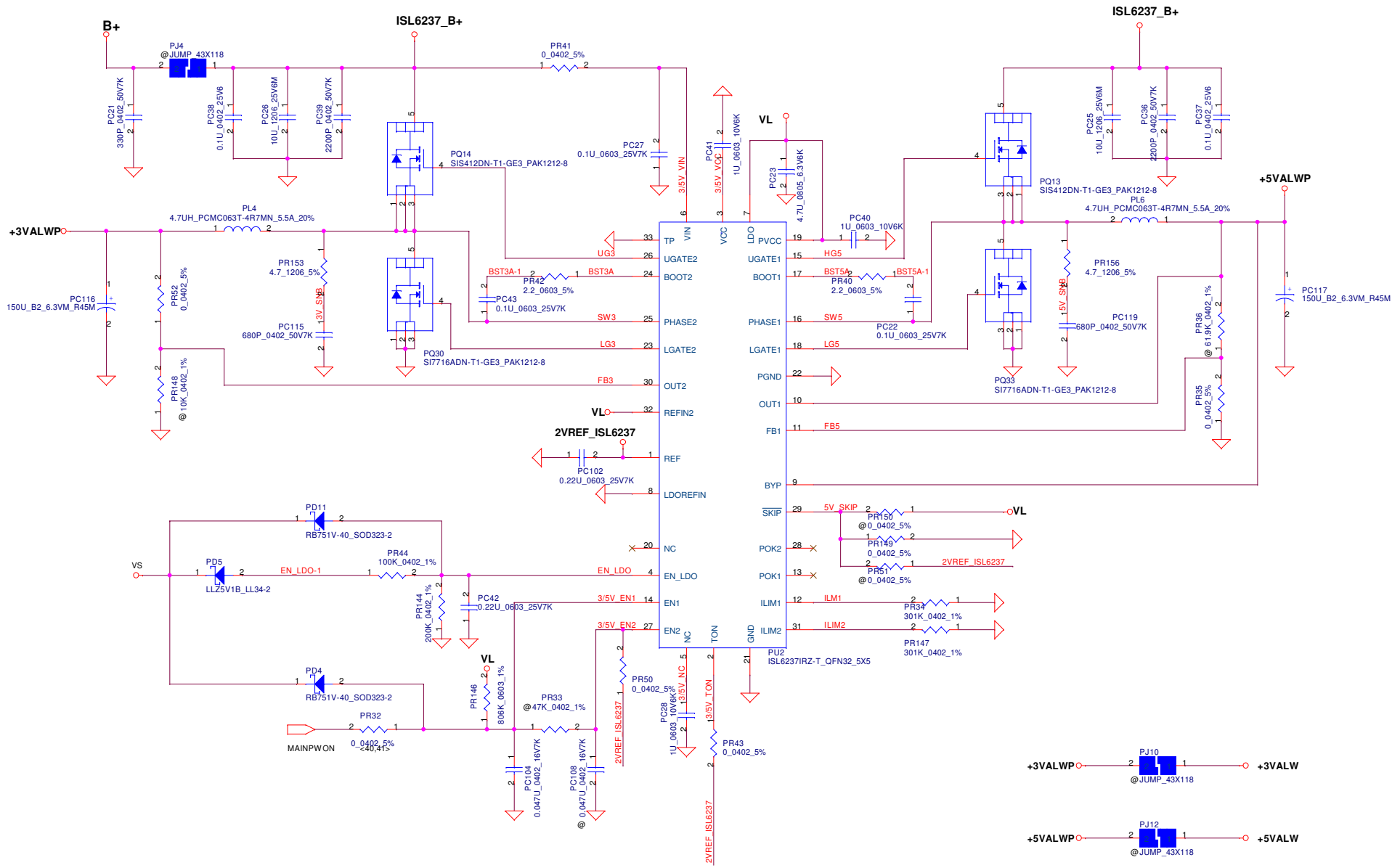
DIS CP mode
 $Va_{lim}=2.39 \cdot \left(\frac{31.6K/514K}{(31.6K/514K)+(21K/514K)} \right) = 1.425V$
 $I_{in_{put}} = (1/0.02) \cdot \left((0.05 \cdot Va_{lim}) / (2.39+0.05) \right)$
 where $Va_{lim}=1.425V$, $I_{in_{put}}=4A$

LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

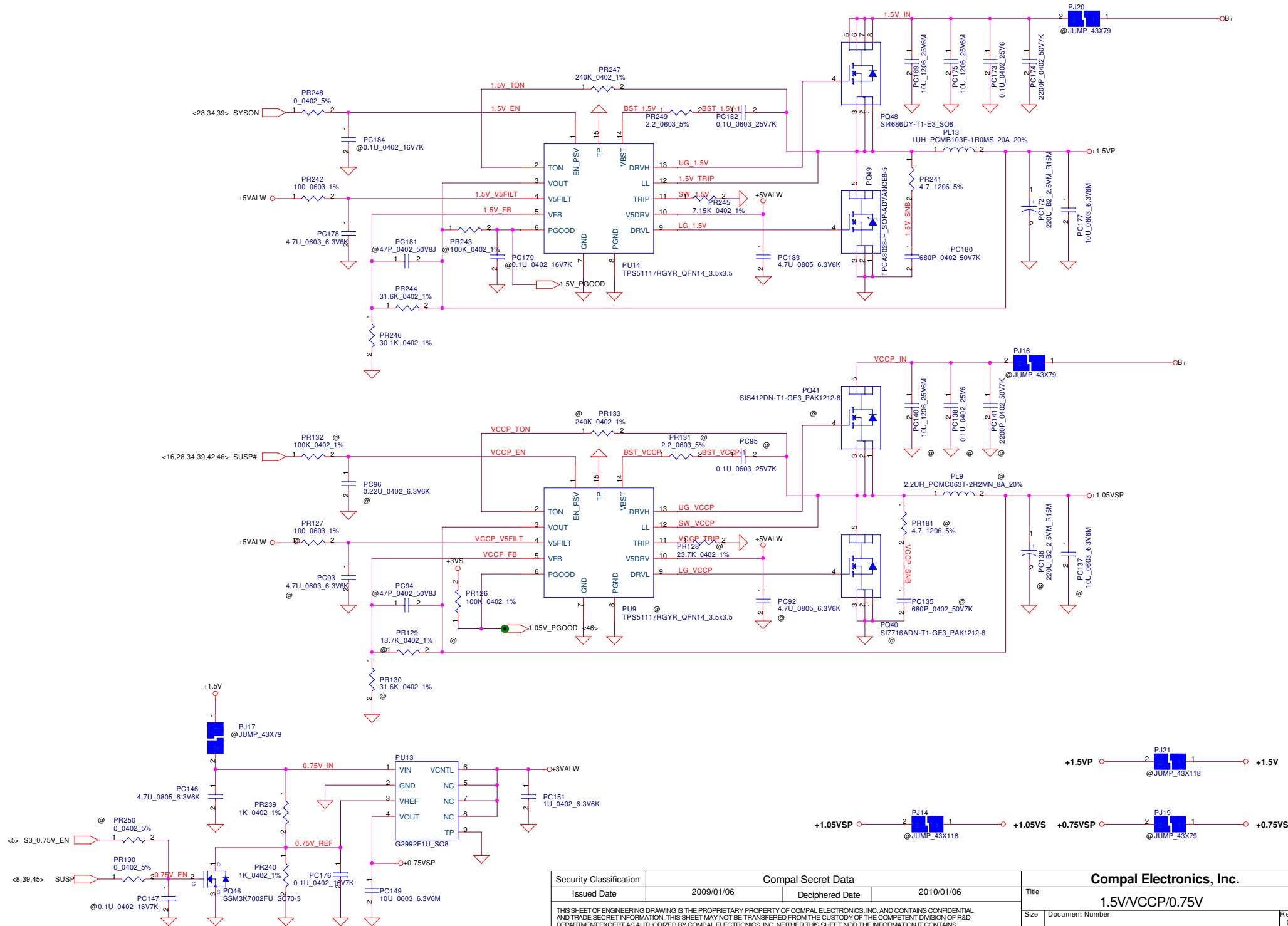
Connect to EC A/D Pin.
<34> CHGVADJ

<34> BATT_OVP

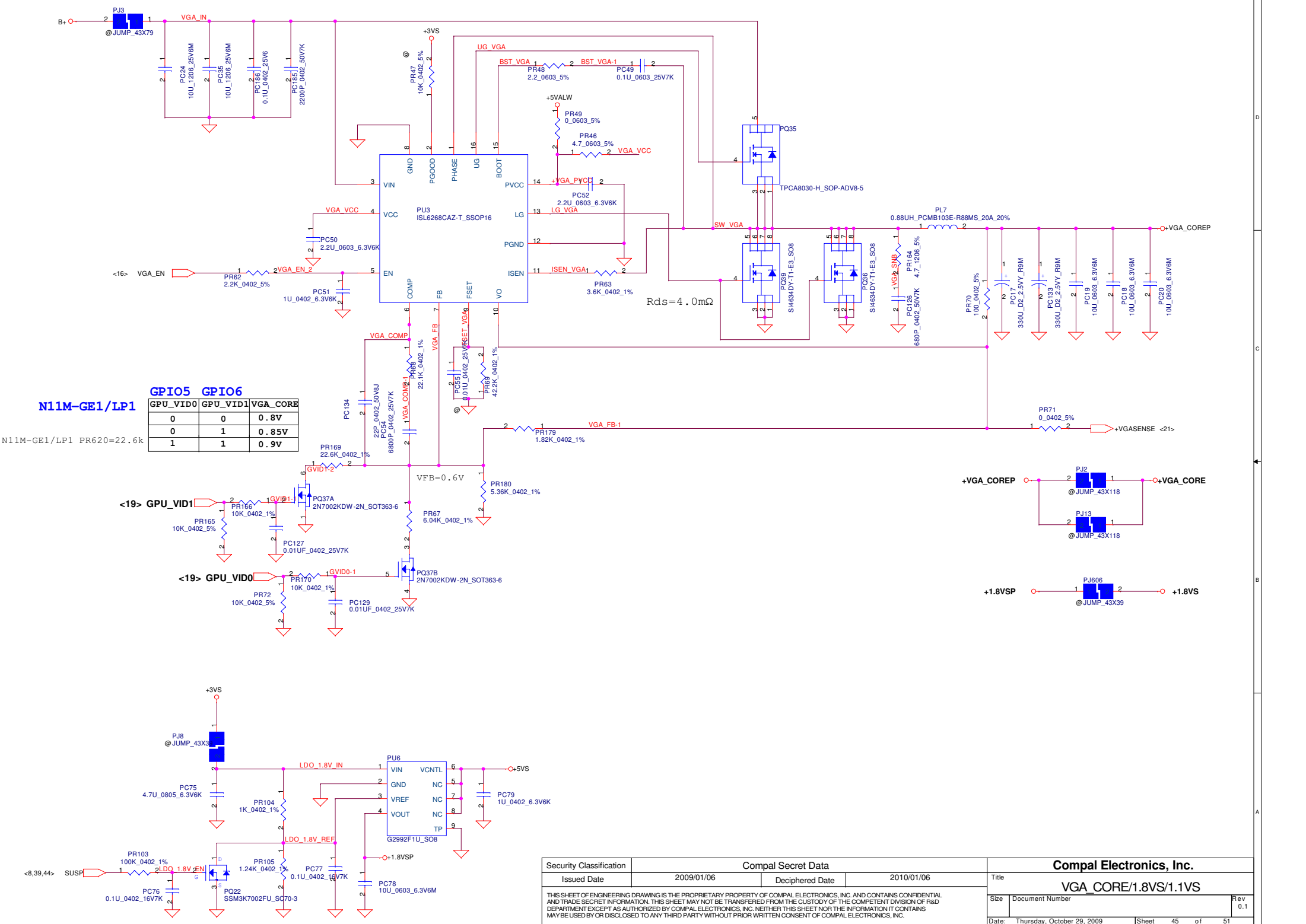
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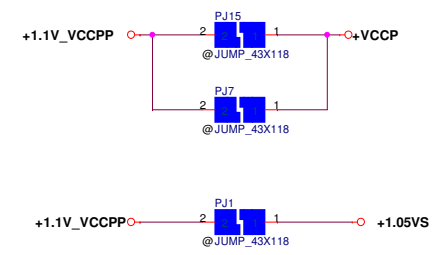
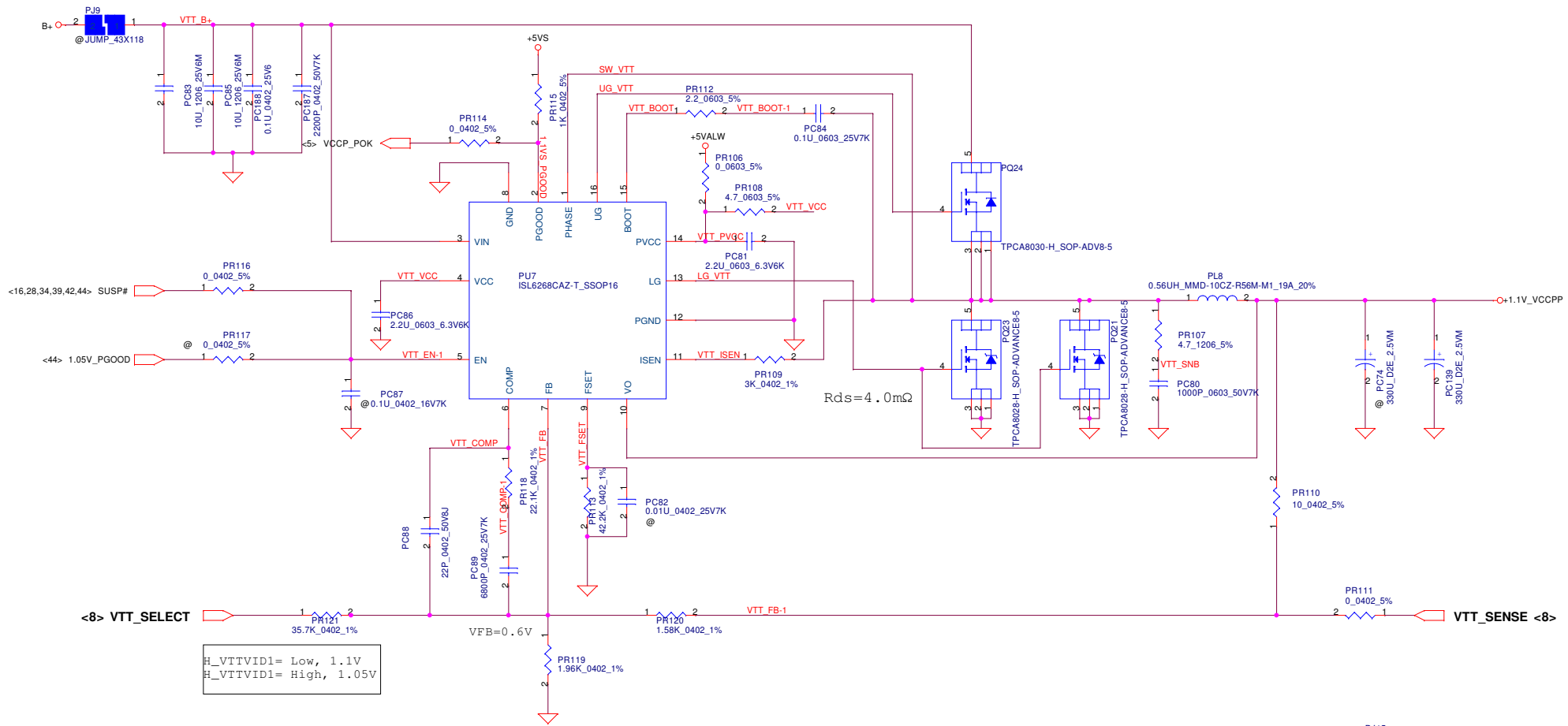
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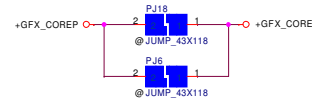
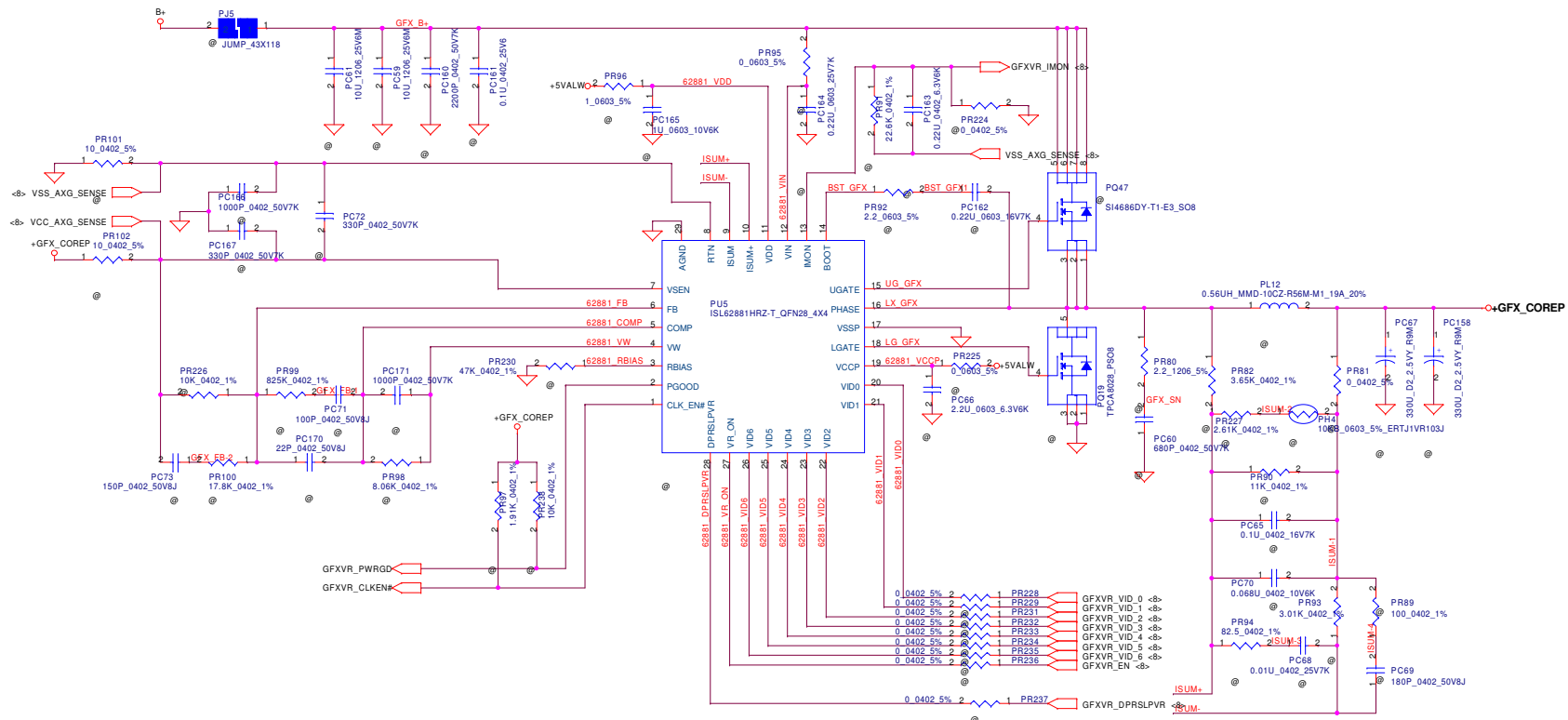
N11M-GE1/LP1 PR620=22.6k

GPIO5		GPIO6	
GPU_VID0	GPU_VID1	VGA_CORE	VGA_CORE
0	0	0.8V	
0	1	0.85V	
1	1	0.9V	

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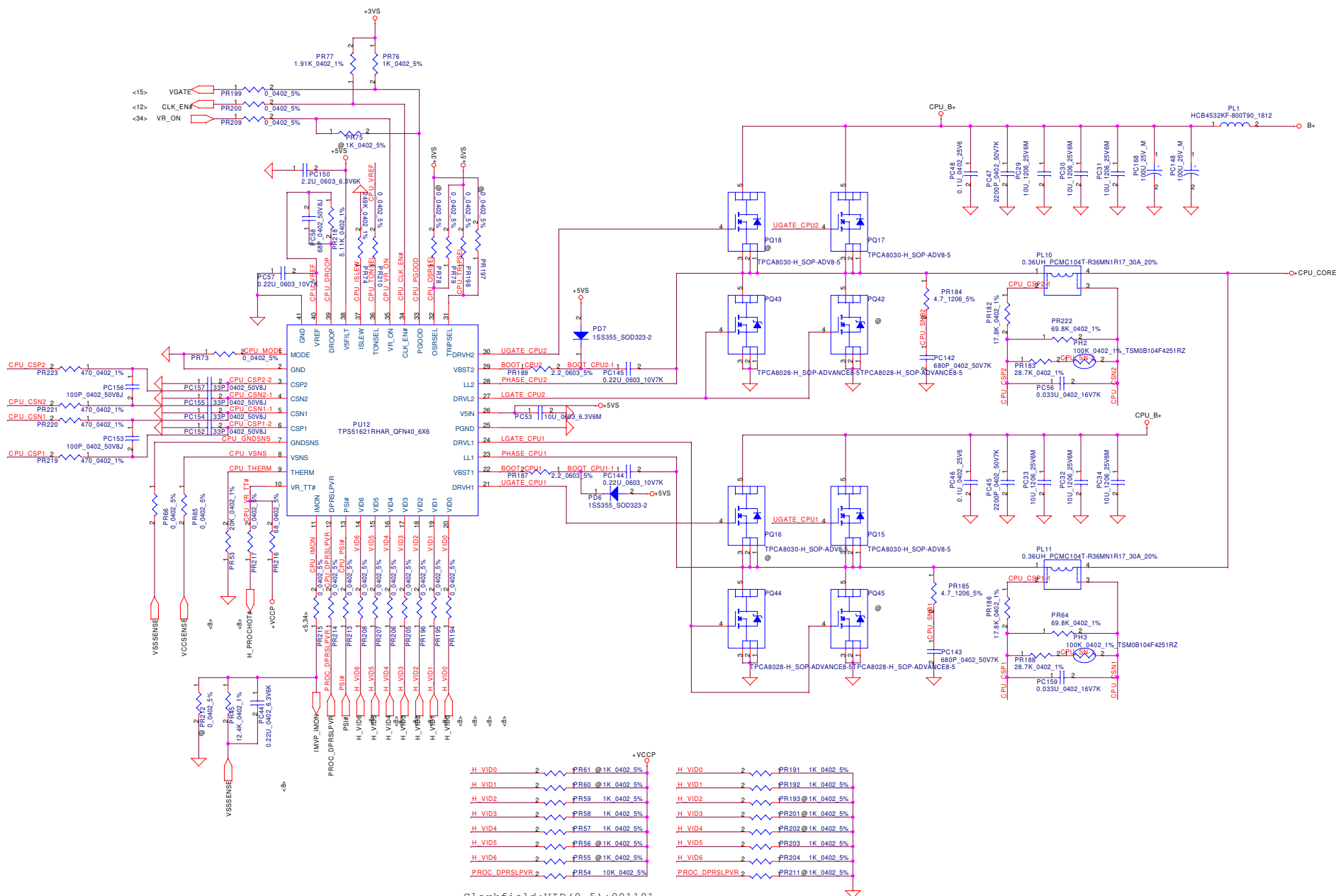


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Clarkfield:VID(0-5):001101
 Auburndale:VID(0-5):001110

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NO DATE PAGE MODIFICATION LIST PURPOSE EVT TO DVT

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Title			
<i>HW PIR</i>			
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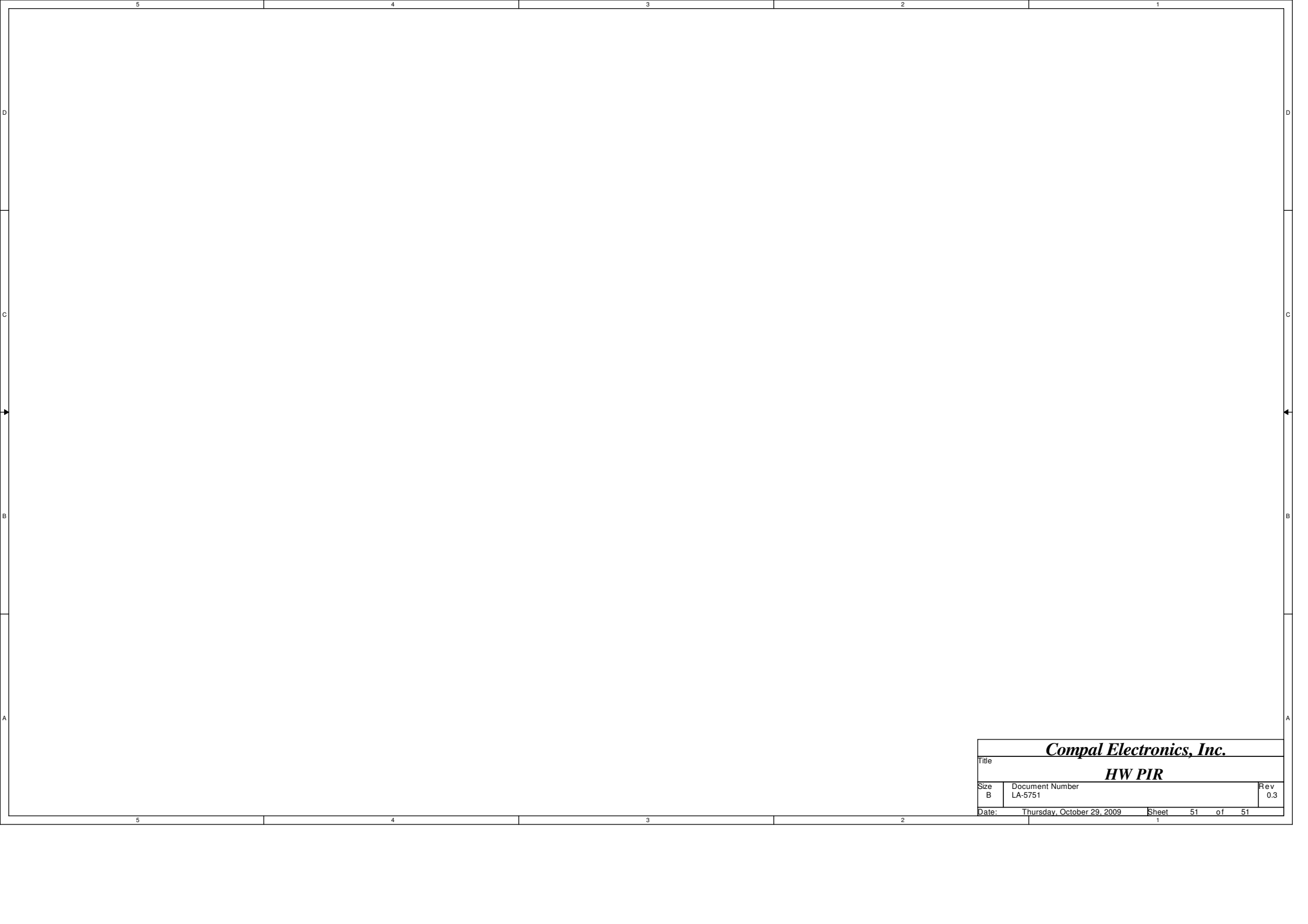
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<i>HW PIR</i>			
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