PHQAA

Marseille 10R/10RG

LA-6831P REV 0.1 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-07-05 Rev 0.1

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.		
Title: *Cover Page*		
Size: B	Document Number: PHQAA LA-6831P M/B	Rev: 0.1
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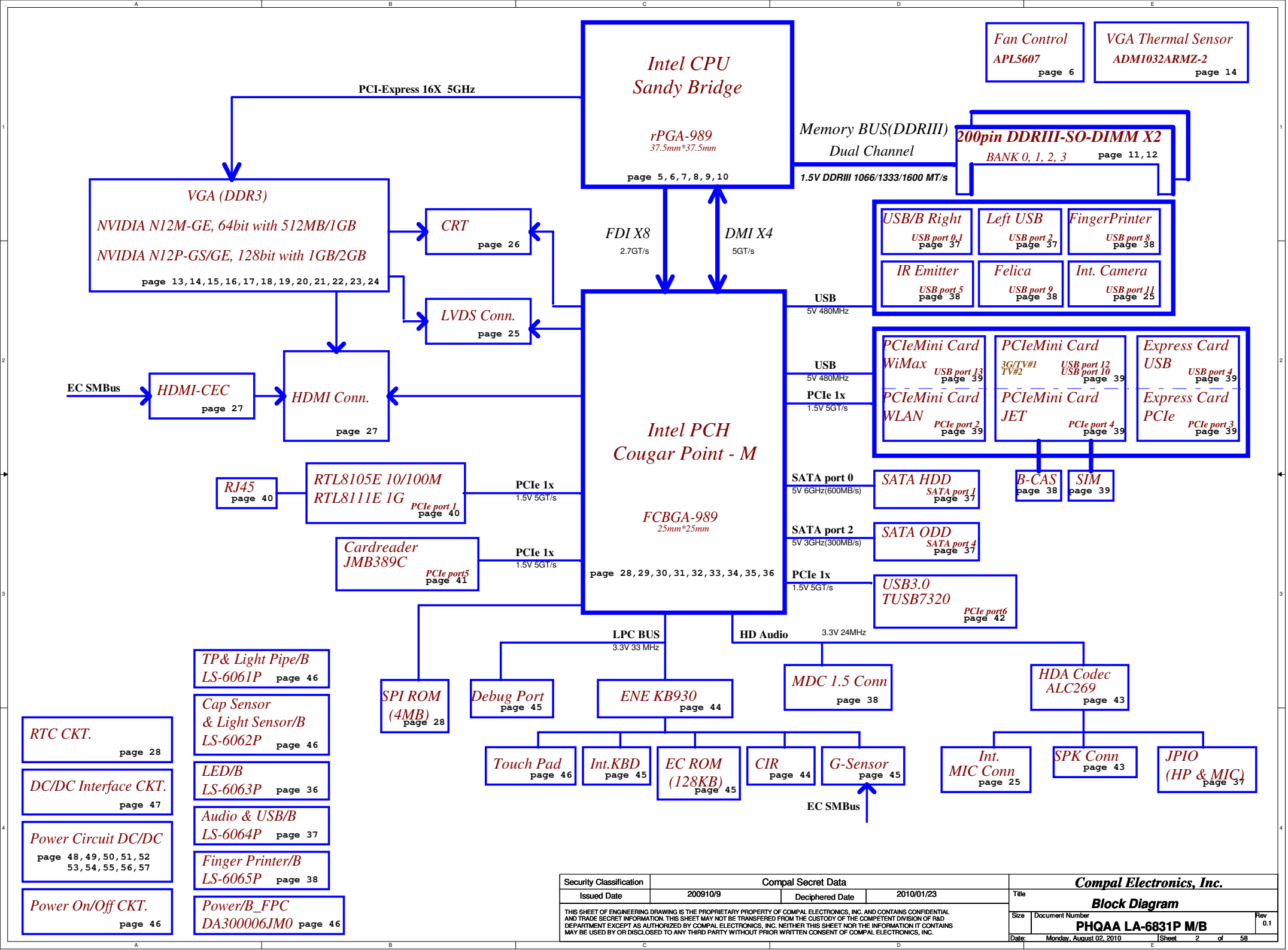

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Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: PHQAA LA-6831P M/B		Rev: 0.1
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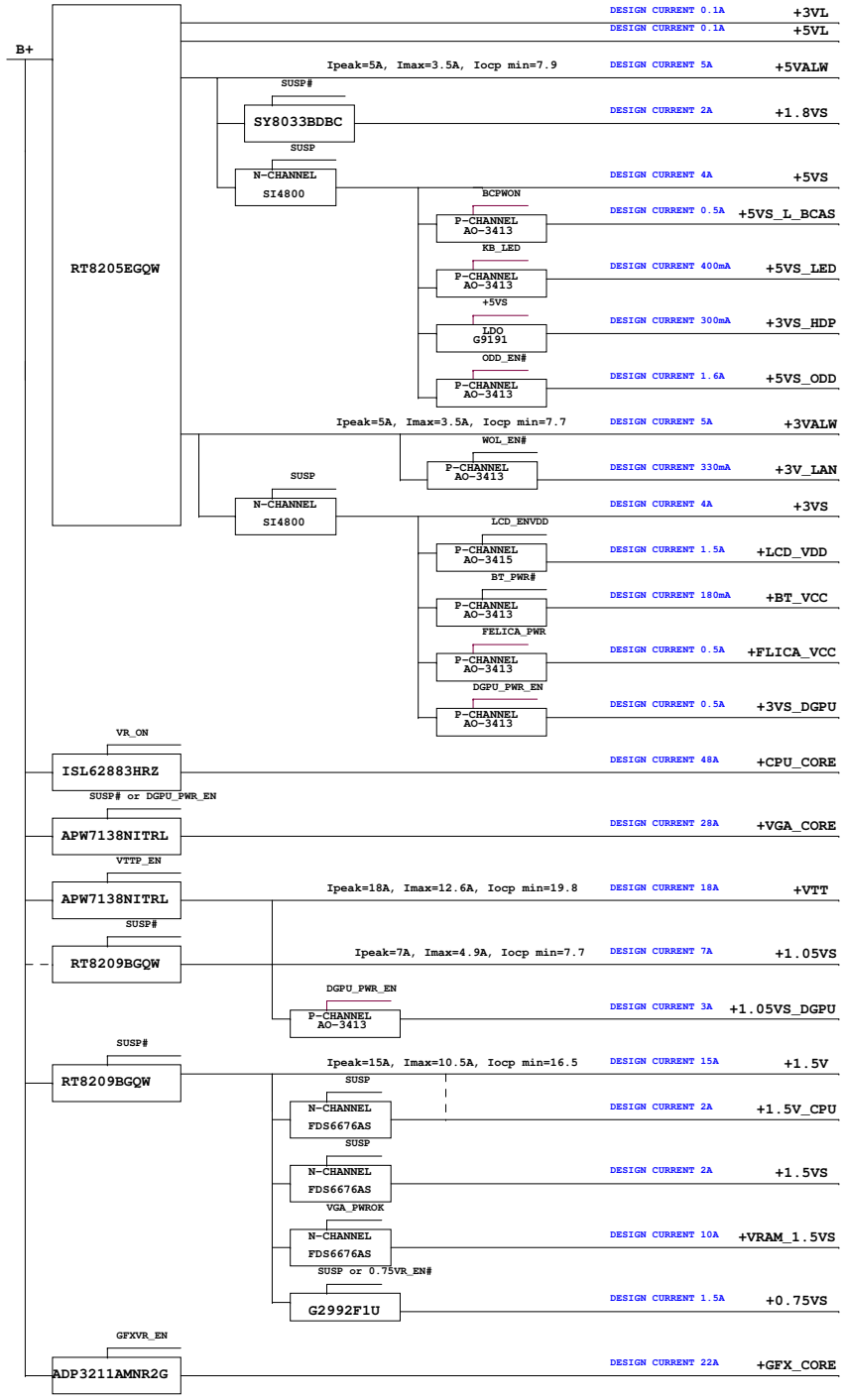

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Title: Power Tree

Size	Document Number	Rev
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/ Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS			Camera & Mic
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel			Camera & Mic
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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Title: Notes List

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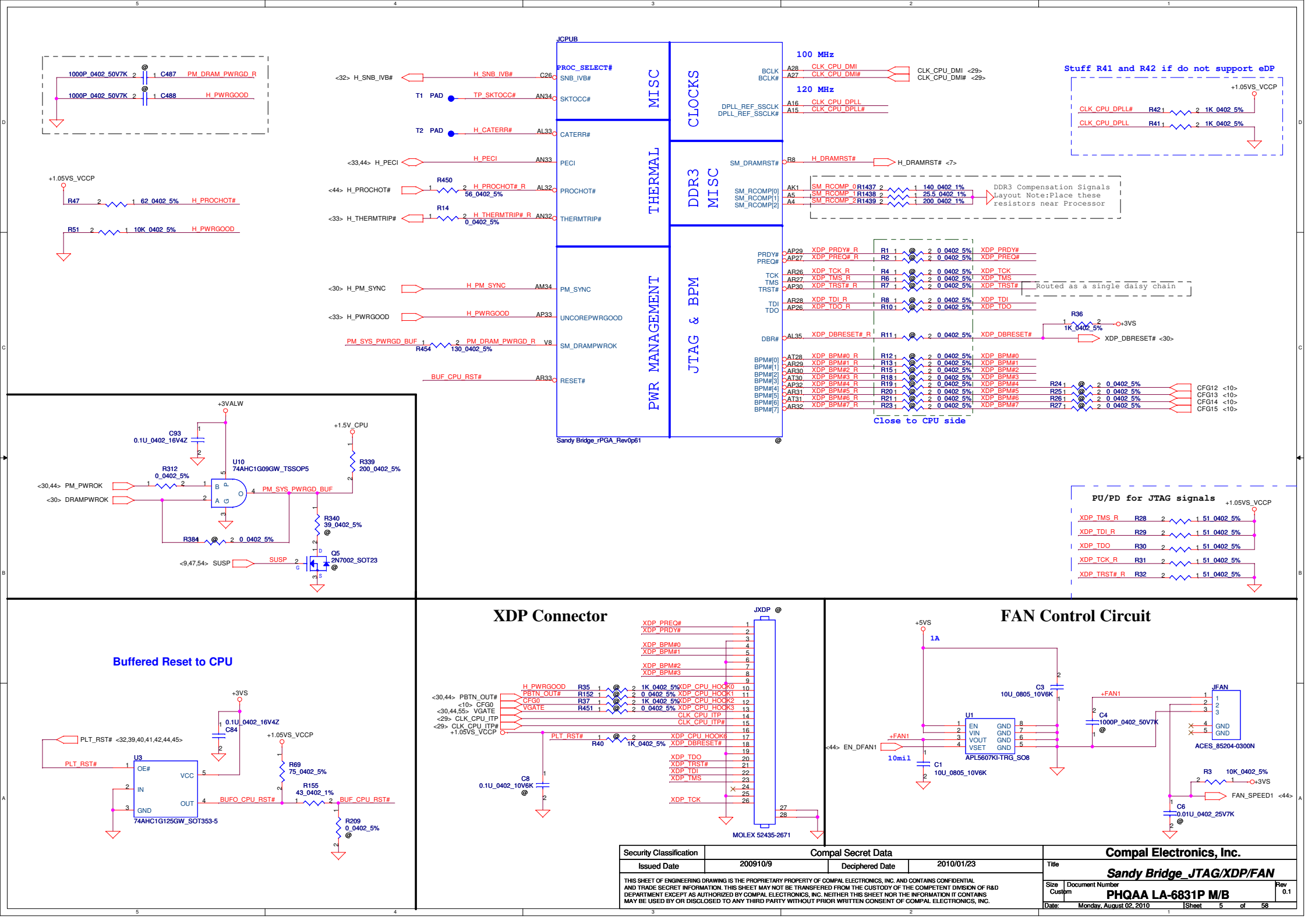

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Compal Electronics, Inc.

Title: *Sandy Bridge_JTAG/XDP/FAN*

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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

Close to CPU

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Compal Electronics, Inc.

Title: Sandy Bridge_DMI/PEG/FDI

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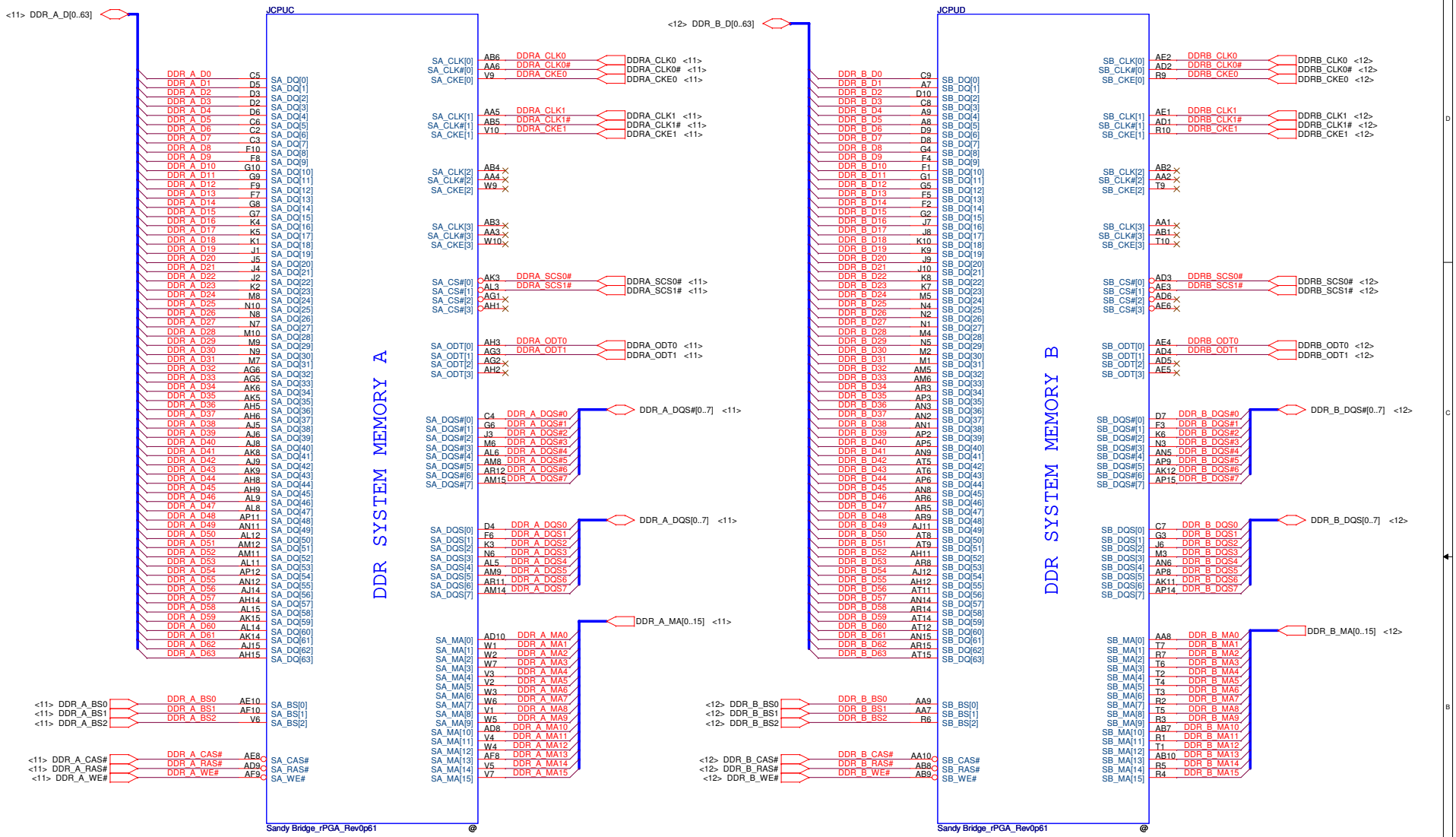

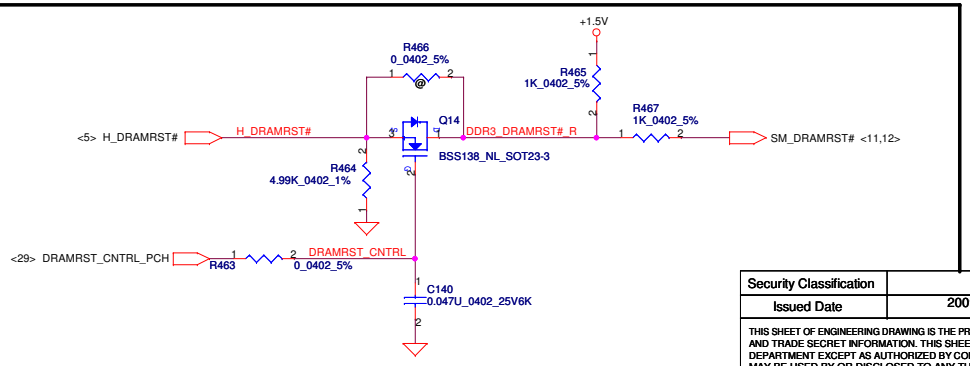

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Compal Electronics, Inc.

Title: *Sandy Bridge_DDR3*

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POWER

+CPU_CORE

JCPUF

94A (Quad Core 45W)
53A (SV 35W)

8.5A

CORE SUPPLY

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PEG AND DDR

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

SVID

VIDALERT# VIDSCLK VIDSOUT

SENSE LINES

VCC_SENSE VSS_SENSE VCCIO_SENSE VSS_SENSE_VCCIO

Sandy Bridge_rPGA_Rev0p61 @

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

TOP Socket Cavity x 7

Bottom Socket Cavity x 5

22U_0805_6.3V6M

330U_D2_2V_Y

ESR 9mohm

330U_D2_2V_Y

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

Bottom Socket Cavity

10U_0805_10V6K

Top Socket Edge

Top Socket Cavity

Co-Lay with C2, C5, C7, C9

330U_D2_2VM_R6M

Bottom Socket Edge

330U_D2_2V_Y

R70 130_0402_5%

R68 75_0402_5%

R67 43_0402_1%

R63 0_0402_5%

R66 0_0402_5%

Pull high resistor on VR side

R64 100_0402_1%

Close to CPU

R62 100_0402_1%

R65 0_0402_5%

R52 0_0402_5%

R102 0_0402_5%

R105 100_0402_1%

Close to CPU

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Title: Sandy Bridge_POWER-1

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POWER

+GFX_CORE Decoupling: 2X 470U (4m ohm), 12X 22U

Bottom Socket Edge
Co-lay for Cost Down Plan

Bottom Socket Cavity
Top Socket Cavity

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU Decoupling: 1X 330U (6m ohm), 6X 10U

Co-lay for Cost Down Plan

+VCCSA Decoupling: 1X 330U (6m ohm), 3X 10U

Bottom Socket Cavity
Co-lay for Cost Down Plan
Bottom Socket Edge

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge

VCCPLL Decoupling: 1X 330U (6m ohm), 1X 10U, 2x1U

Follow CRB 1.0.

JCPUG

SENSE LINES
VREF
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
MISC
1.8V RAIL

33A
5A
6A
1.2A

Sandy Bridge_rPGA_Rev0p61

C112 330U_D2_2VM_R6M @	C267 22U_0805_6.3V6M UMA@	C338 22U_0805_6.3V6M UMA@	C271 22U_0805_6.3V6M UMA@
C347 22U_0805_6.3V6M UMA@	C343 22U_0805_6.3V6M UMA@	C345 22U_0805_6.3V6M UMA@	C873 330U_2.5V_M_R17 UMA@
C348 22U_0805_6.3V6M UMA@	C344 22U_0805_6.3V6M UMA@	C346 22U_0805_6.3V6M UMA@	
C266 22U_0805_6.3V6M UMA@	C341 22U_0805_6.3V6M UMA@	C342 22U_0805_6.3V6M UMA@	

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *Sandy Bridge_POWER-2*

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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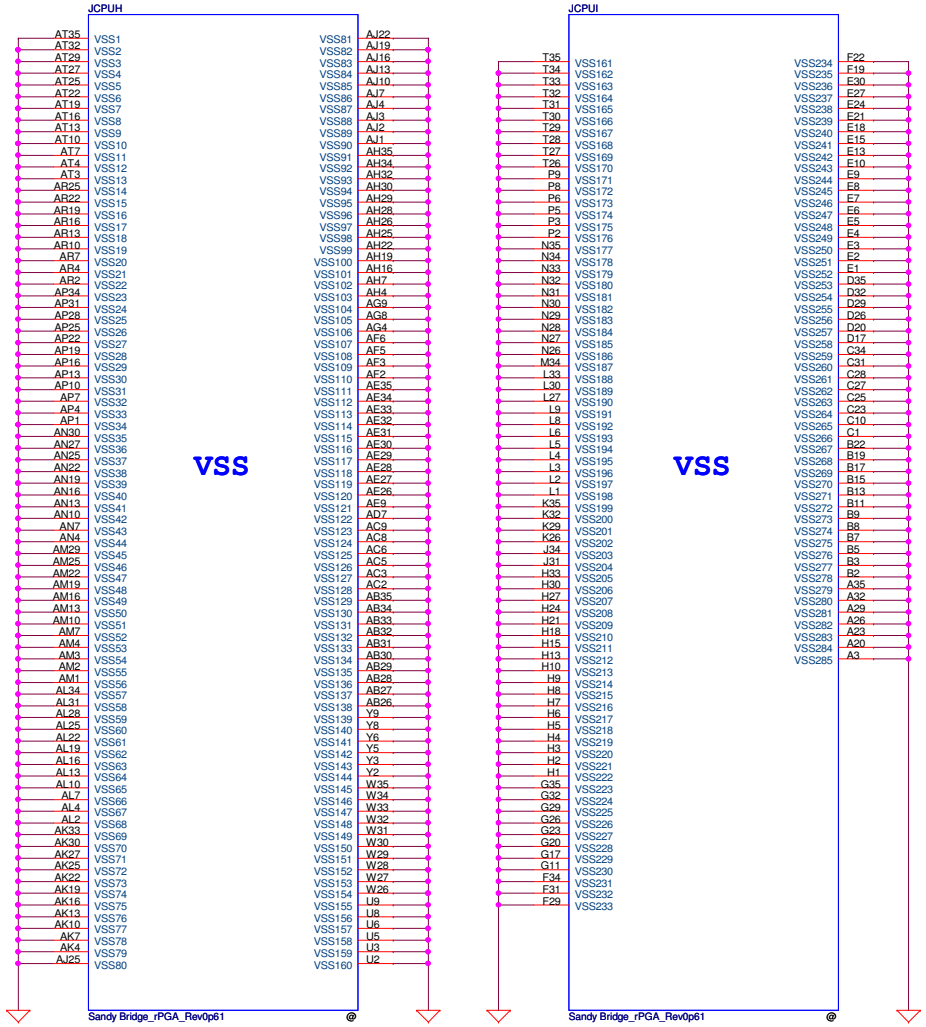
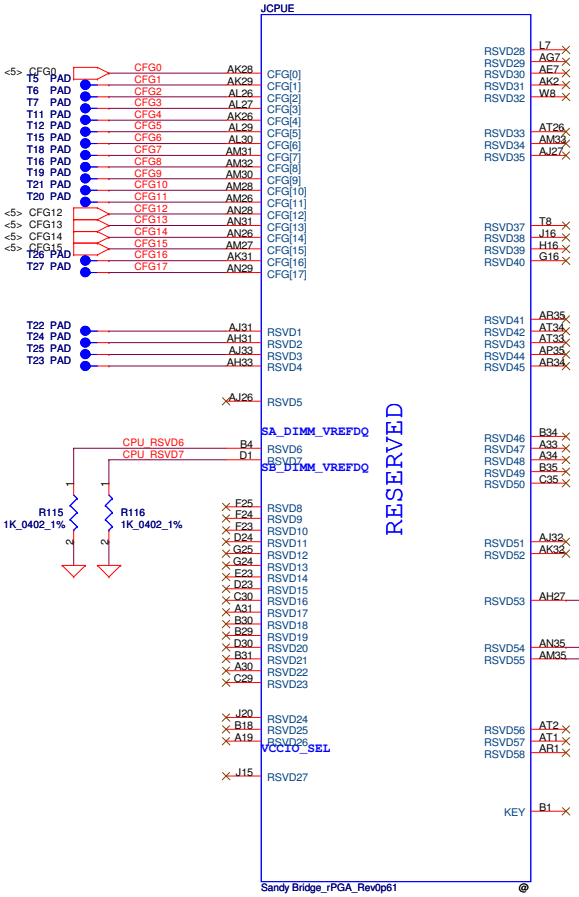
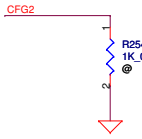


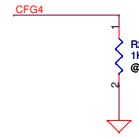


CFG Straps for Processor

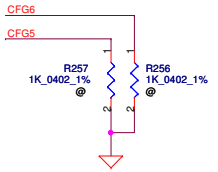
(CFG[17:0] internal pull high to VCCIO)



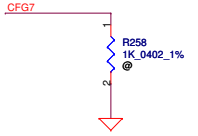
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: *Sandy Bridge_GND/RSVD/CFG*

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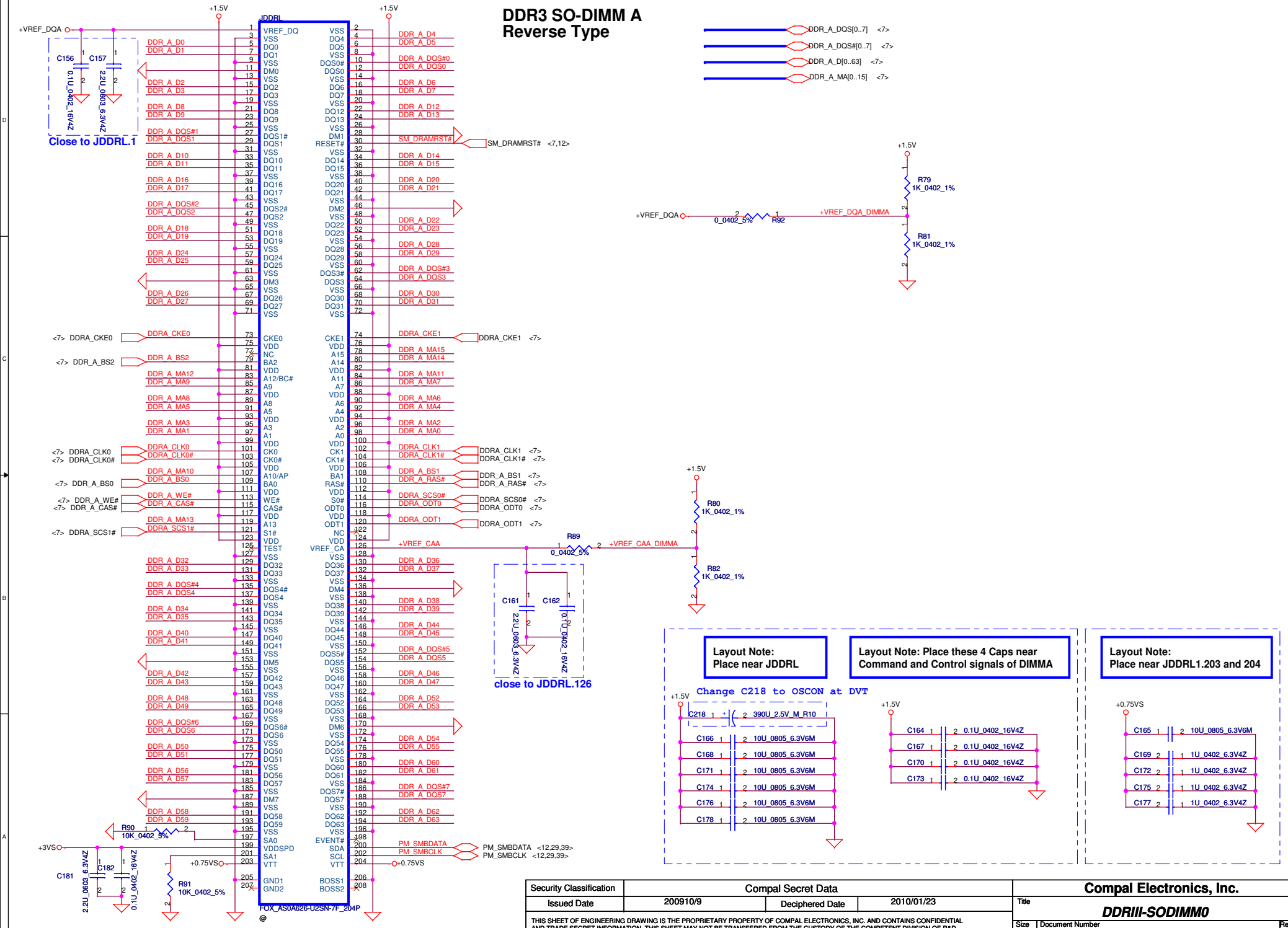
DDR3 SO-DIMM A
Reverse Type



Security Classification	Compal Secret Data		
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Title: ***DDRIII-SODIMM0***

Size	Document Number	Rev
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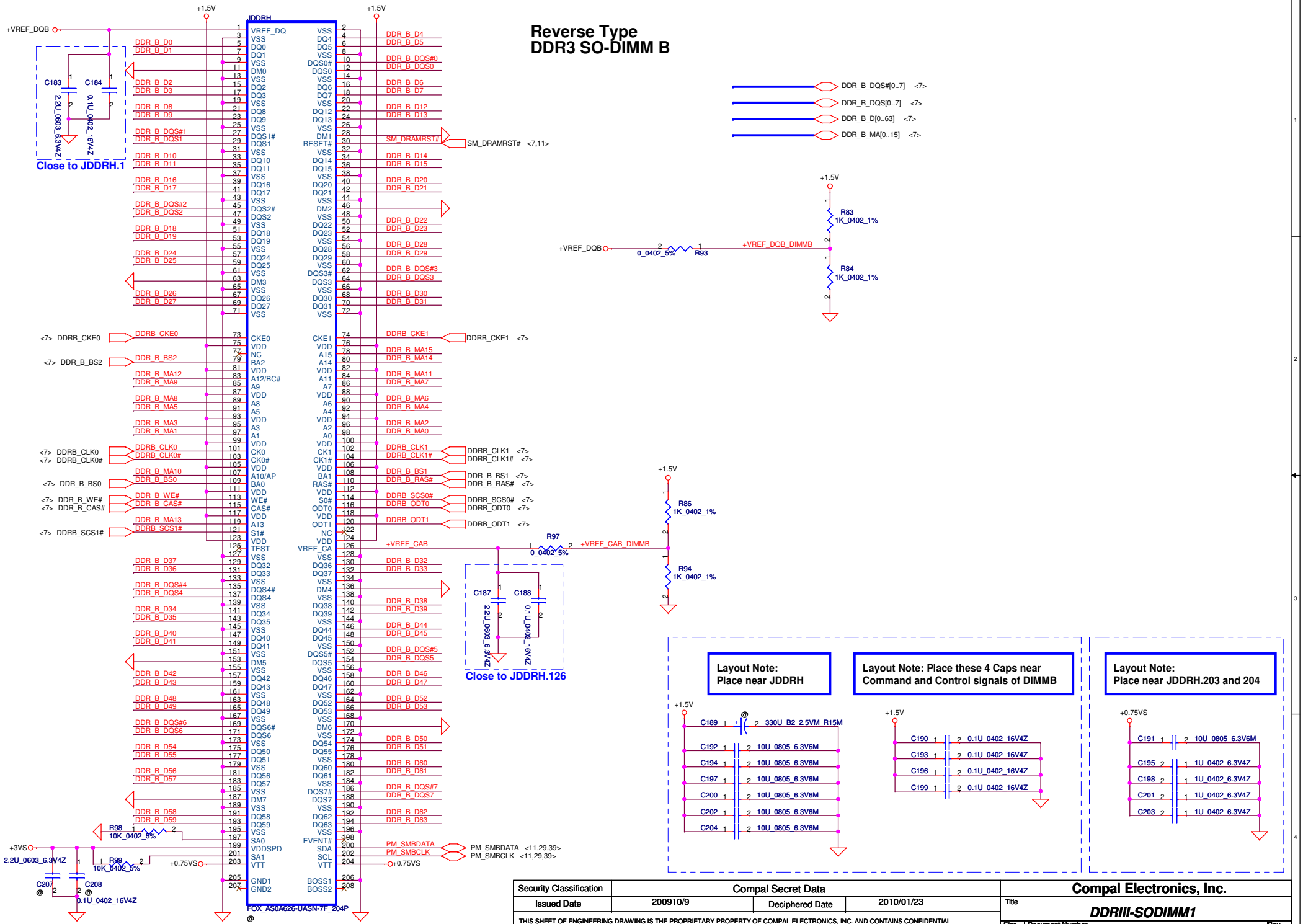
Reverse Type
DDR3 SO-DIMM B



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM1***

Size	Document Number	Rev
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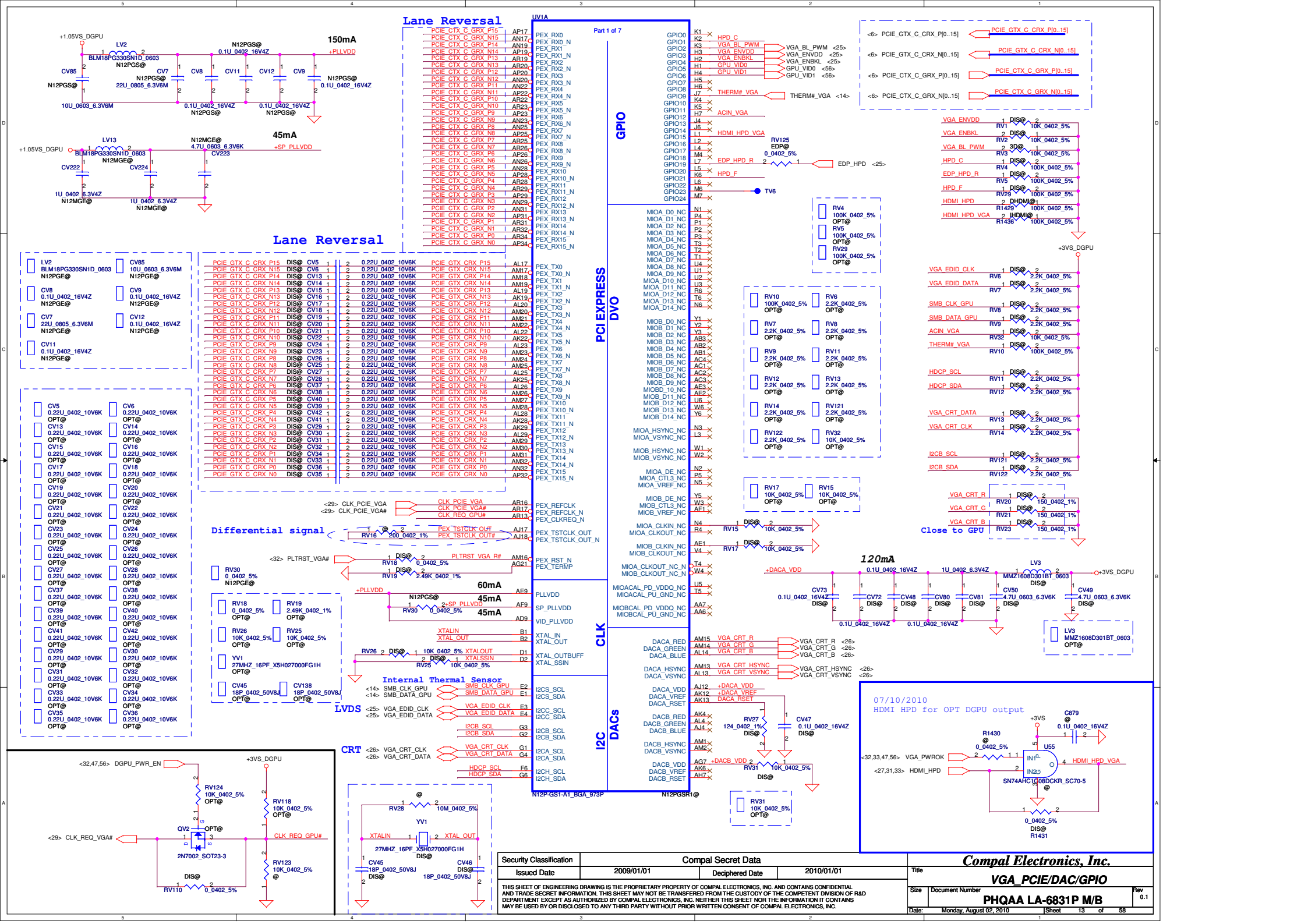
Lane Reversal
Lane Reversal
Differential signal
Internal Thermal Sensor
LVDS
CRT
Close to GPU
120mA
60mA
45mA
45mA
150mA
45mA
07/10/2010
HDMI HPD for OPT DGPU output
GPIO
PCI EXPRESS
DVO
CLK
I2C
DACs
Part 1 of 7
N12P-GS1-A1_BGA_973P
N12PGSR1@
Security Classification
Compal Secret Data
Issued Date
2009/01/01
Deciphered Date
2010/01/01
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VGA_PCIE/DAC/GPIO
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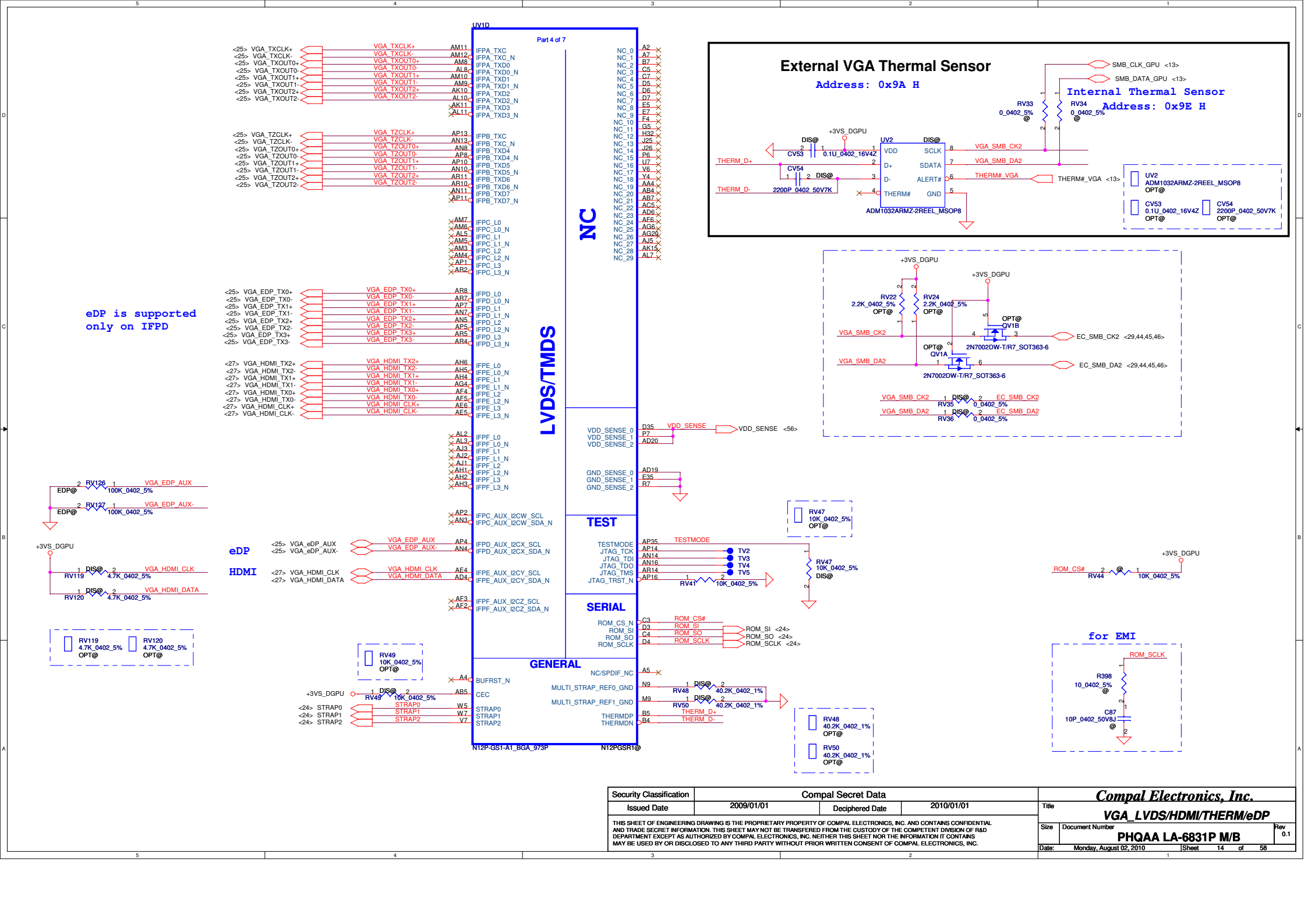

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_LVDS/HDMI/THERM/eDP

Size	Document Number	Rev
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N12M-GE Performance Mode

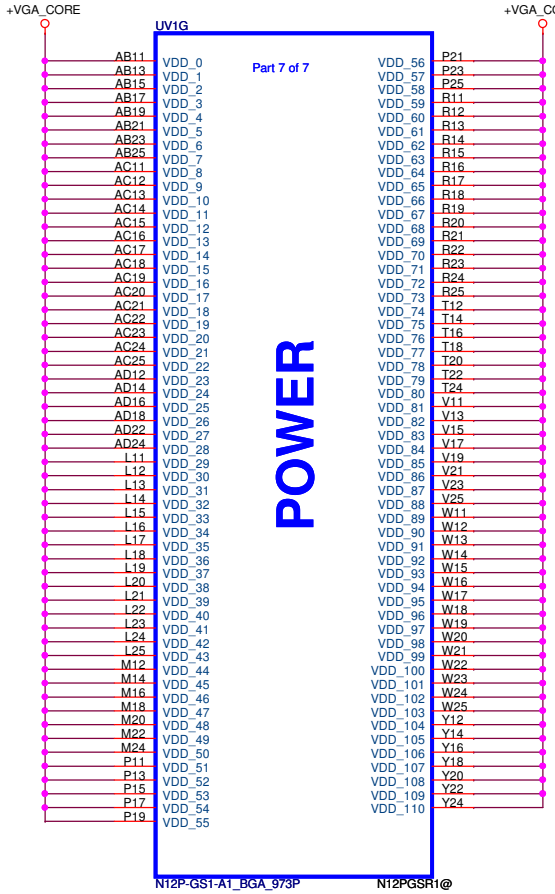
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GS Performance Mode

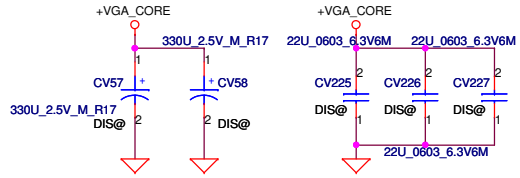
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

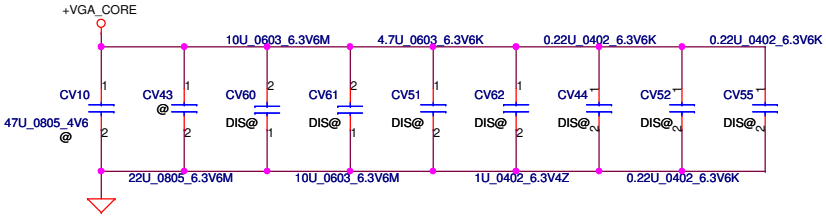
N12P-GE Performance Mode

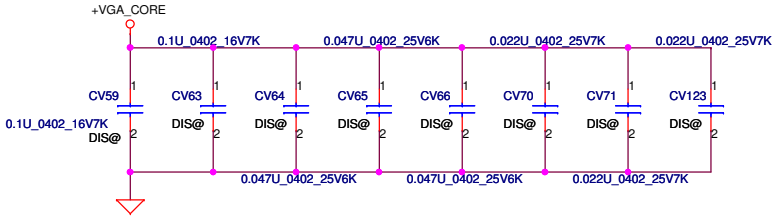
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

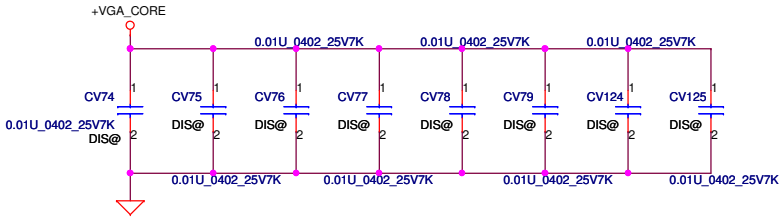


32A for N11E-GE1-LP
28A for N11P-GE1
16A for N11M-GE1 & N11M-OP1
14A for N11M-GE2









CV225 22U_0603_6.3V6M OPT@			
CV226 22U_0603_6.3V6M OPT@	CV227 22U_0603_6.3V6M OPT@		
CV57 330U_2.5V_M_R17 OPT@	CV58 330U_2.5V_M_R17 OPT@		
CV10 47U_0805_4V6 OPT@	CV43 22U_0805_6.3V6M OPT@		
CV60 10U_0603_6.3V6M OPT@	CV61 10U_0603_6.3V6M OPT@		
CV51 4.7U_0603_6.3V6K OPT@	CV62 1U_0402_6.3V4Z OPT@		
CV44 0.22U_0402_6.3V6K OPT@	CV52 0.22U_0402_6.3V6K OPT@		
CV55 0.22U_0402_6.3V6K OPT@	CV59 0.1U_0402_16V7K OPT@		
CV63 0.1U_0402_16V7K OPT@	CV64 0.047U_0402_25V6K OPT@		
CV65 0.047U_0402_25V6K OPT@	CV66 0.047U_0402_25V6K OPT@		
CV70 0.022U_0402_25V7K OPT@	CV71 0.022U_0402_25V7K OPT@		
CV123 0.022U_0402_25V7K OPT@	CV74 0.01U_0402_25V7K OPT@		
CV75 0.01U_0402_25V7K OPT@	CV76 0.01U_0402_25V7K OPT@		
CV77 0.01U_0402_25V7K OPT@	CV78 0.01U_0402_25V7K OPT@		
CV79 0.01U_0402_25V7K OPT@	CV124 0.01U_0402_25V7K OPT@		
CV125 0.01U_0402_25V7K OPT@			

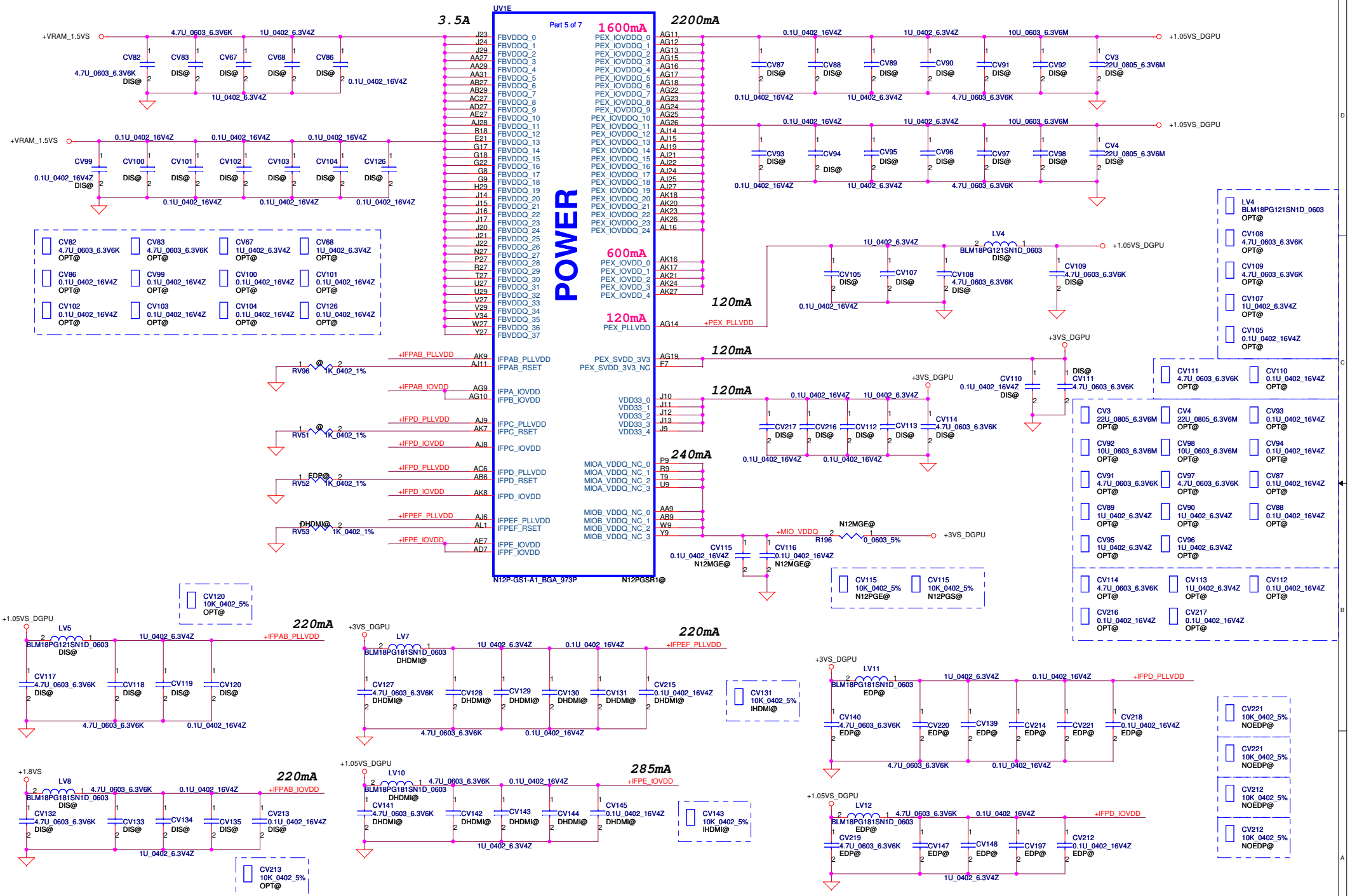
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_VGA CORE

Size | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

Date: Monday, August 02, 2010 | Sheet 15 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.			
Title	VGA_POWER		
Size	Document Number	PHQAA LA-6831P M/B	Rev 0.1
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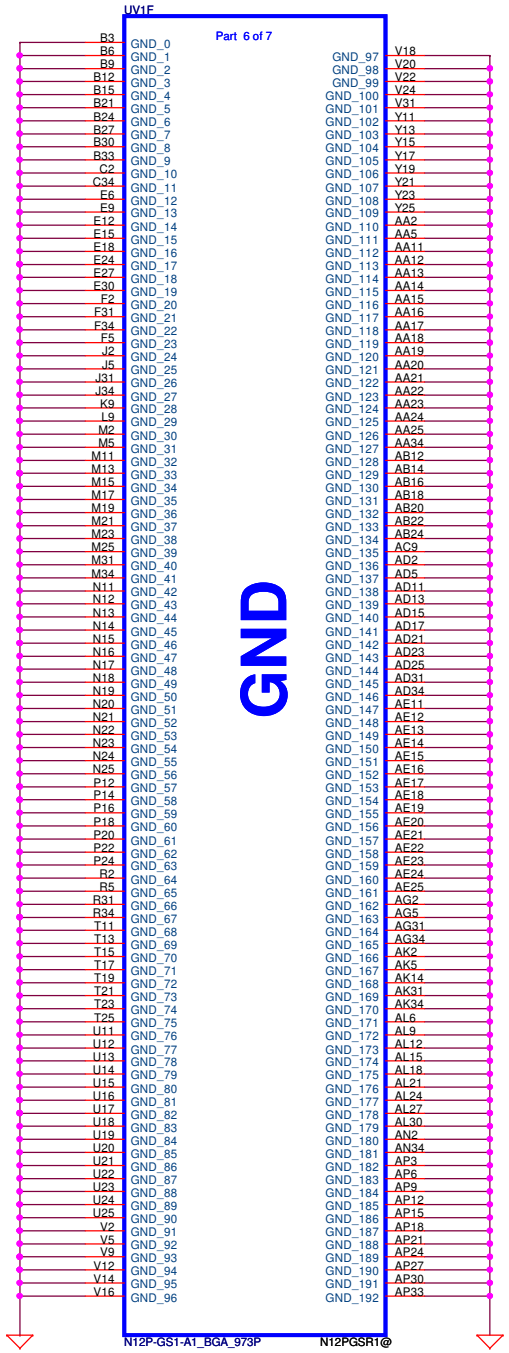


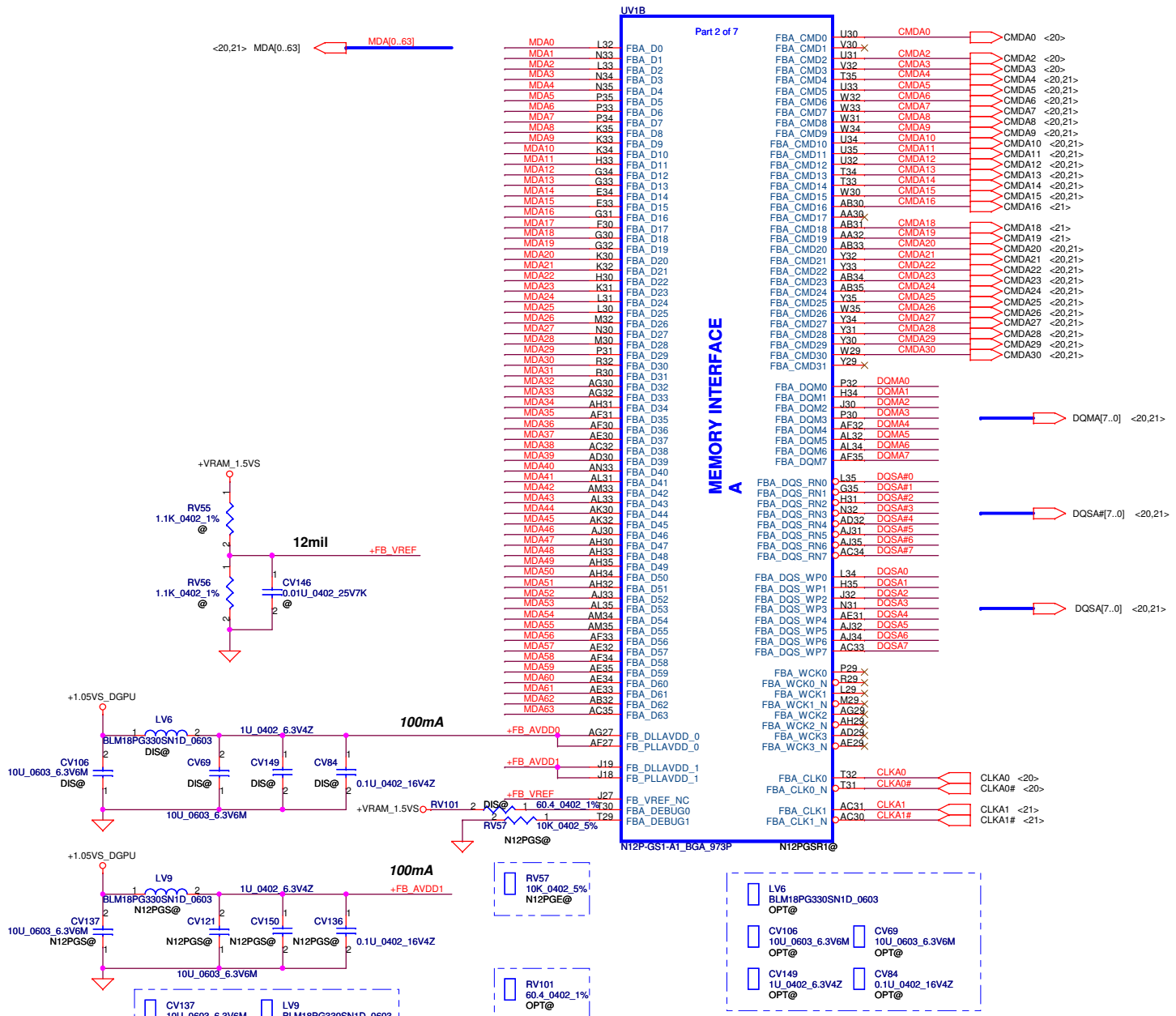
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: **VGA_GND**

Size | Document Number: **PHQAA LA-6831P M/B** | Rev: 0.1

Date: Monday, August 02, 2010 | Sheet 17 of 58



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

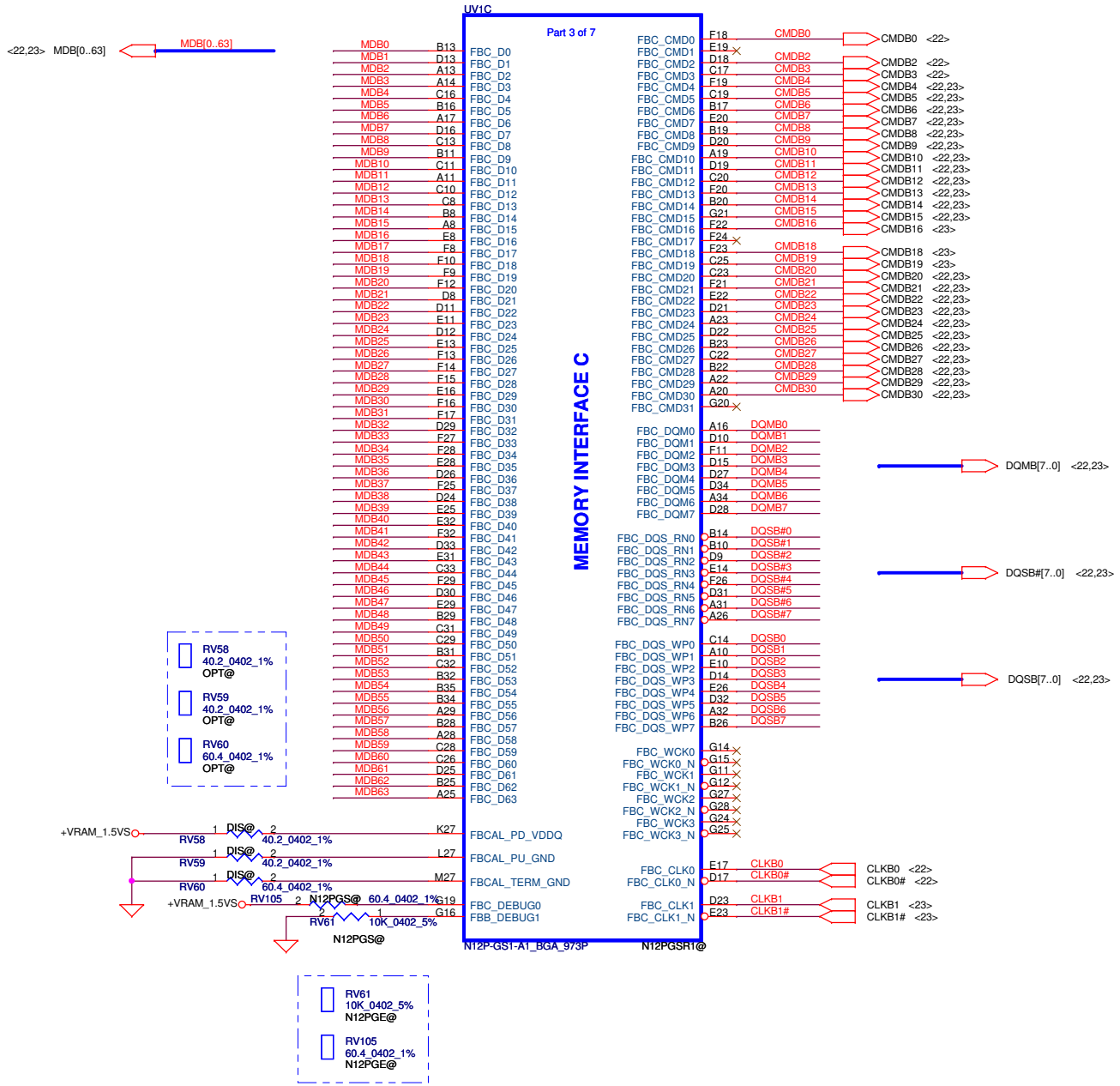
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_MEM Interface A

Size | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

Date: Monday, August 02, 2010 | Sheet 18 of 58



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_MEM Interface C

Size | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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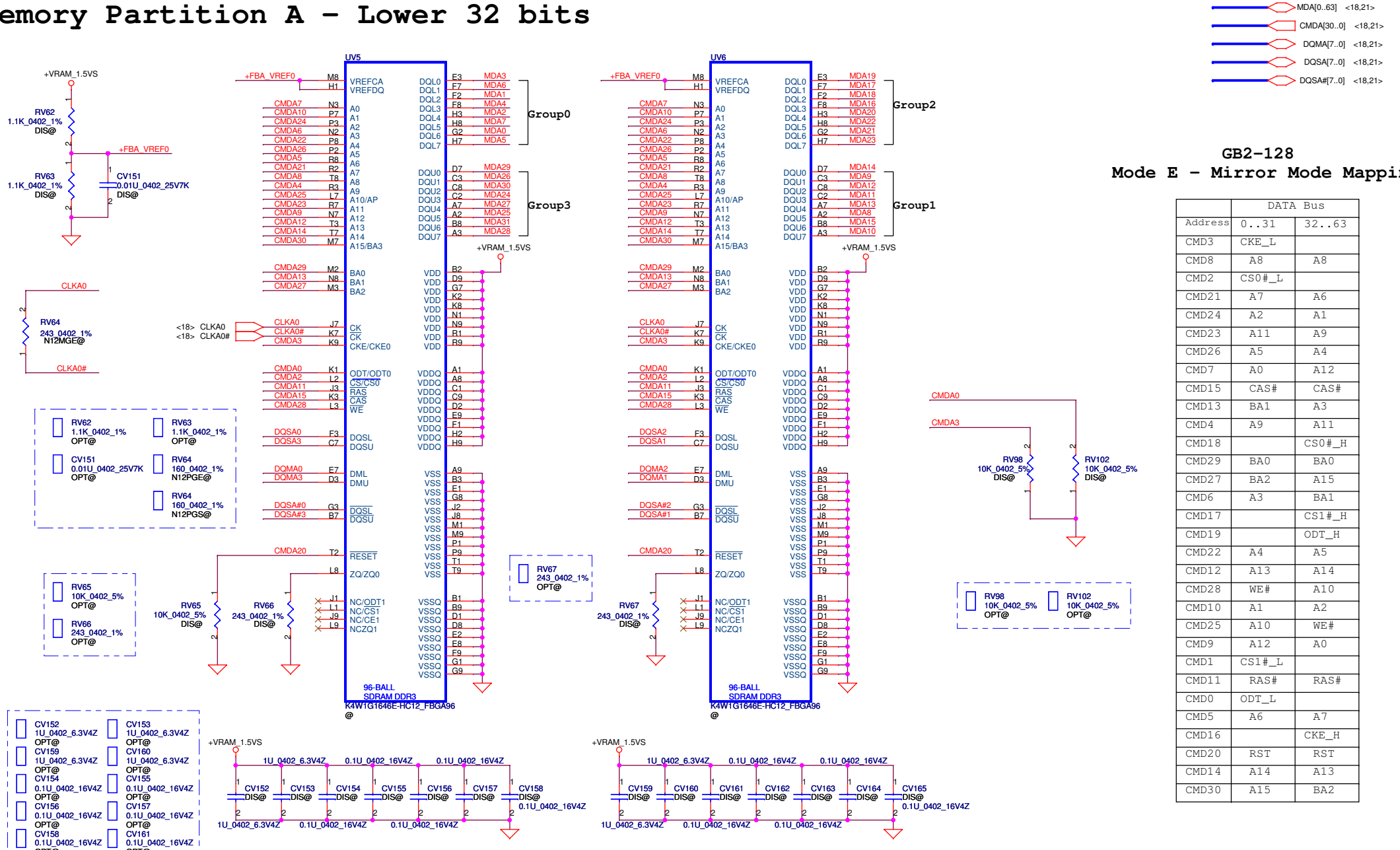
Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.			
Title: VGA_VRAM_A Lower			
Size	Document Number: PHQAA LA-6831P M/B		Rev: 0.1
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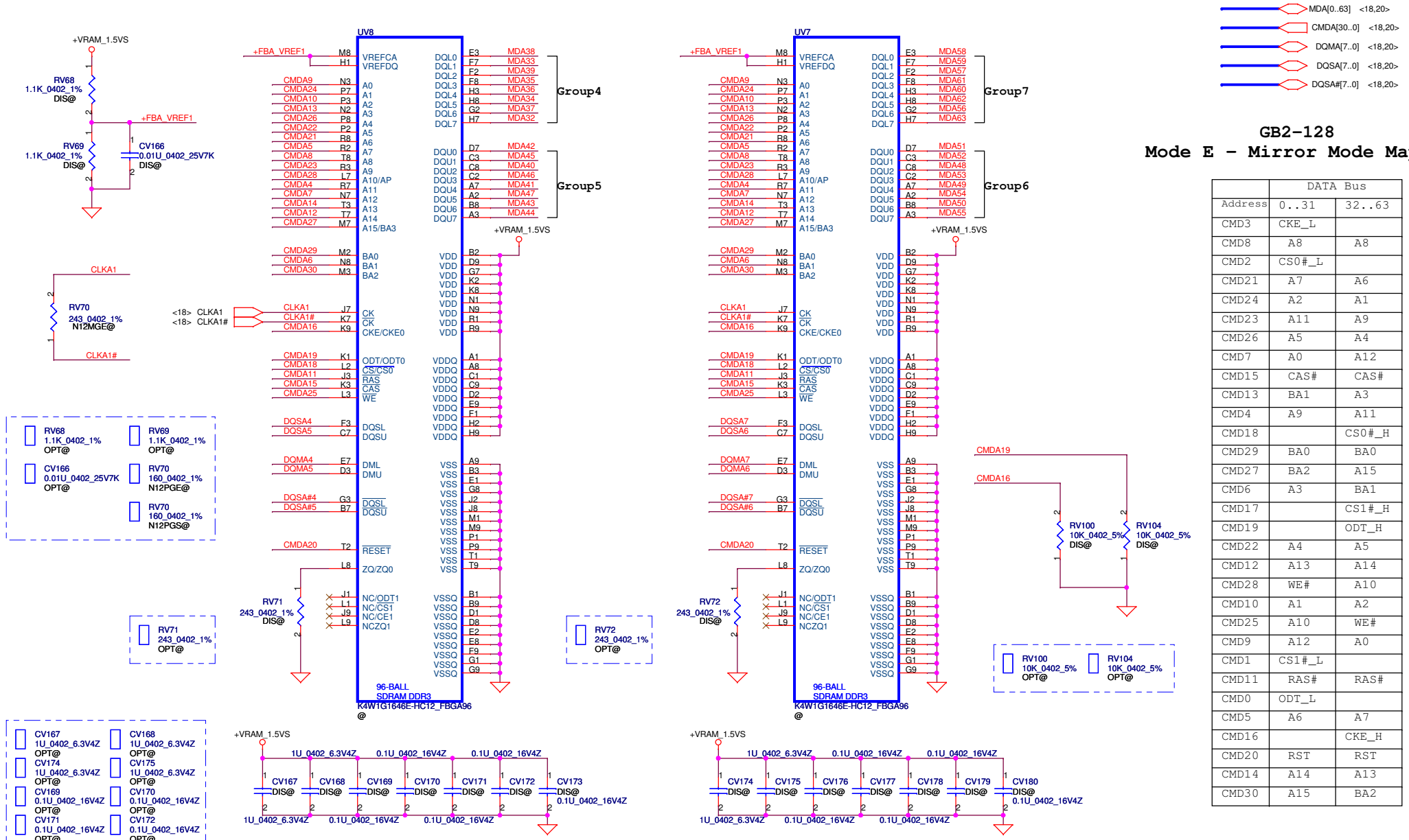
Memory Partition A - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA_VRAM_A Upper

Size | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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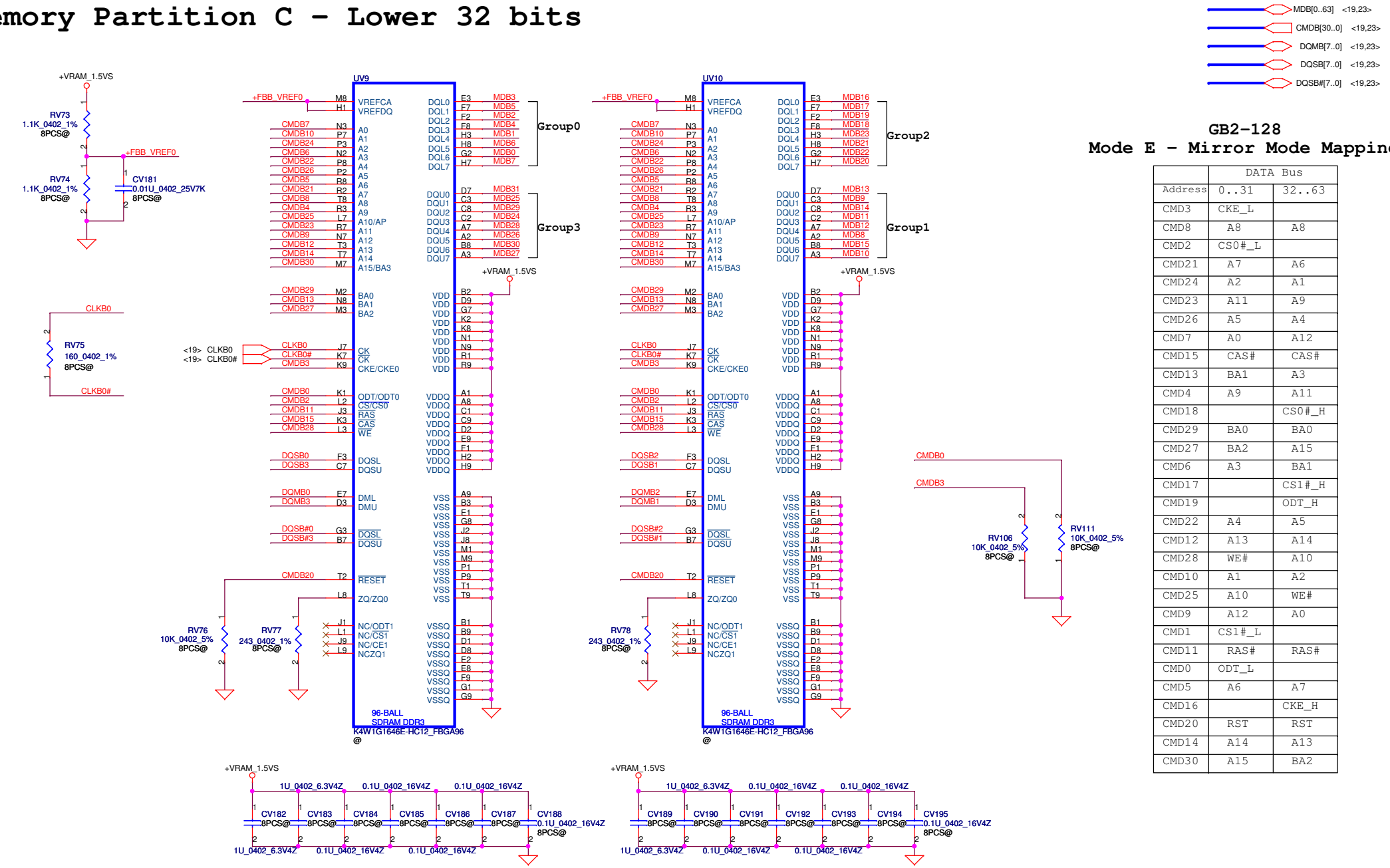
Memory Partition C - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA_VRAM_C Lower

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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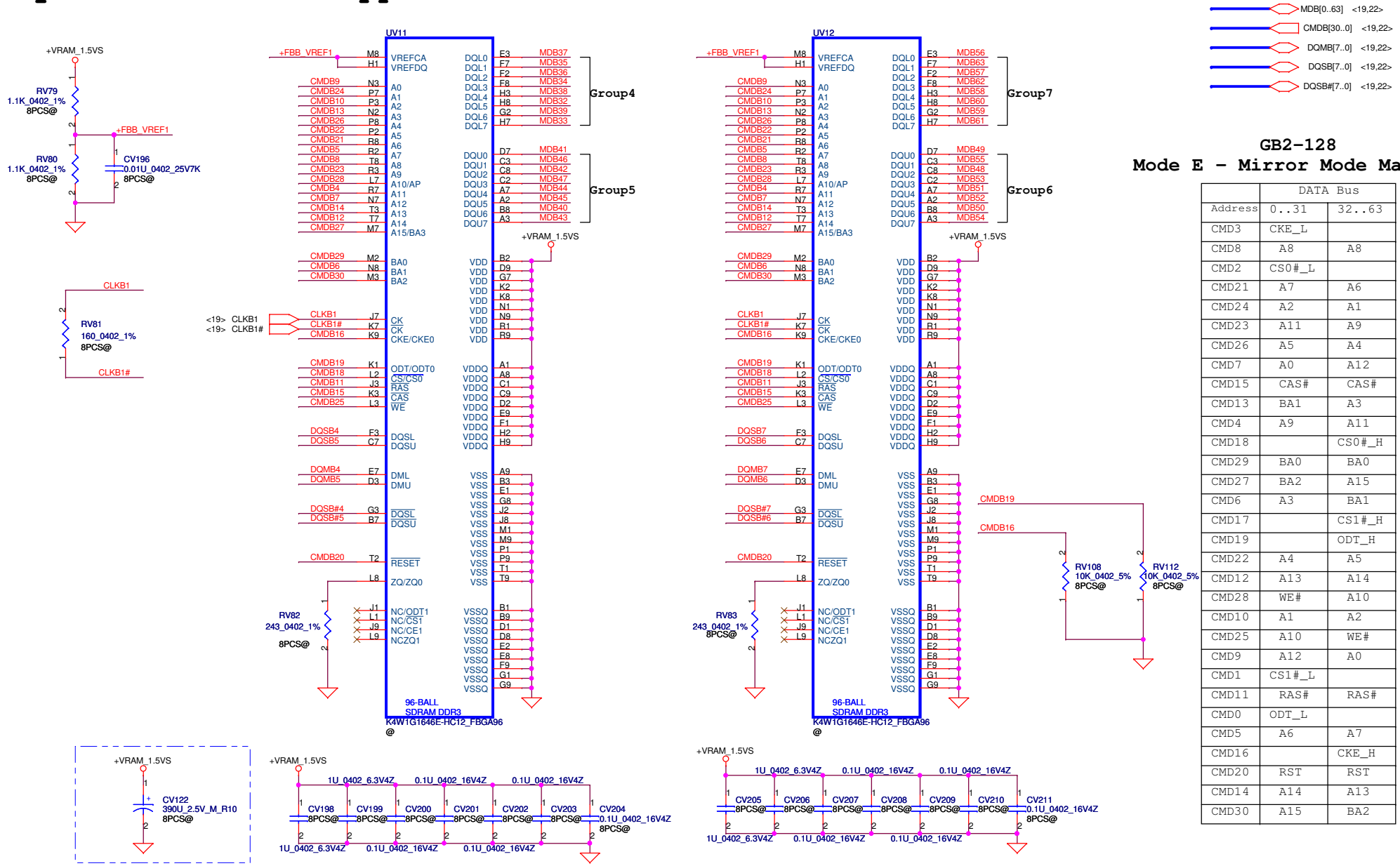
Memory Partition C - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_VRAM_C Upper

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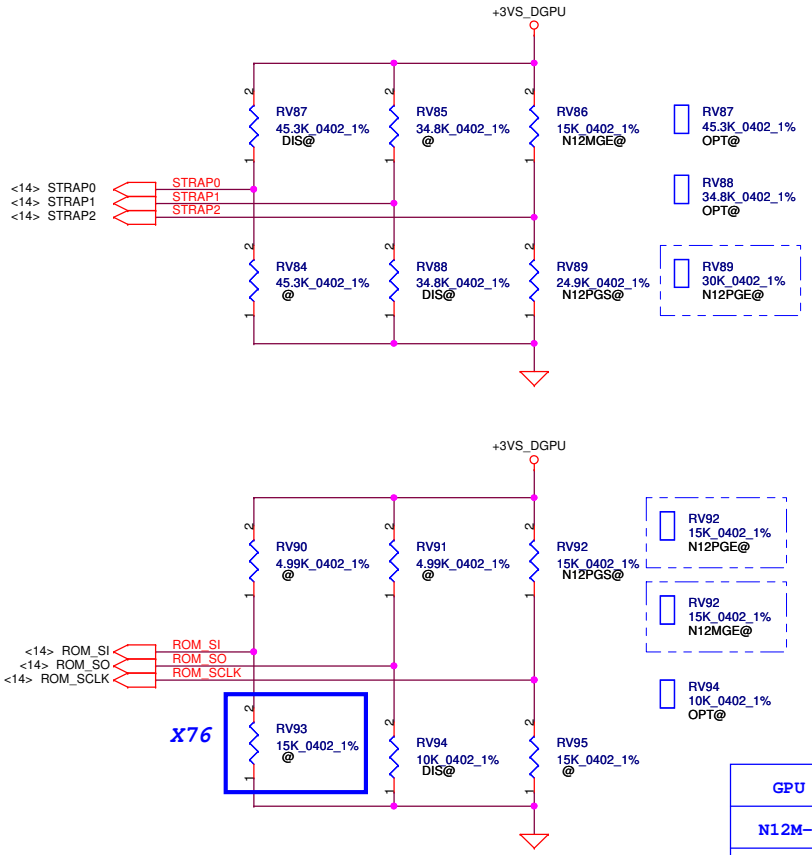

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

Hynix H5TQ1G63BFR-12C	512M	0010	PD 15K
SA000032400	1G	0010	PD 15K
Samsung K4W1G1646E-HC12	512M	0011	PD 20K
SA000035700	1G	0011	PD 20K

SD034150280

SD034200280

SUB_VENDOR

0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	256MB (Default)
1	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_MSIC

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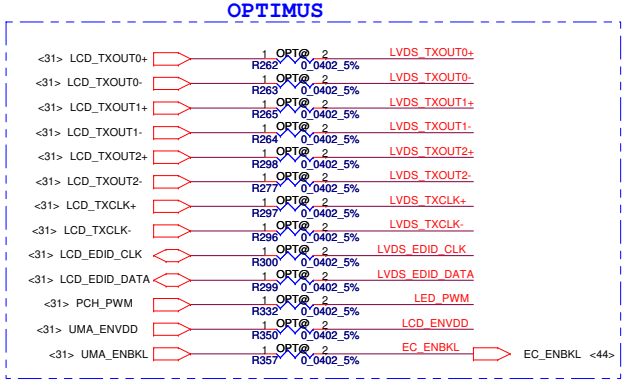
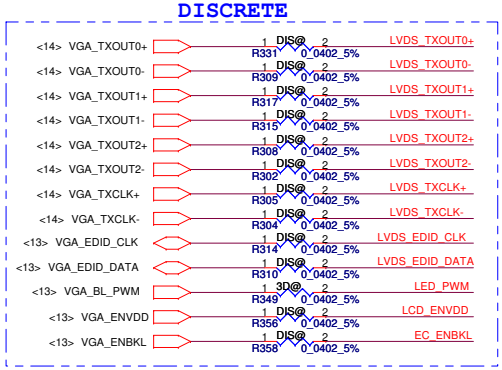
OPTIMUS



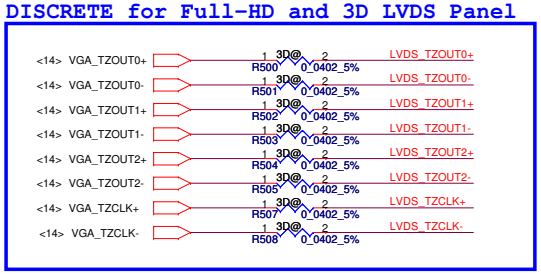
Close to LVDS Connector

DISCRETE



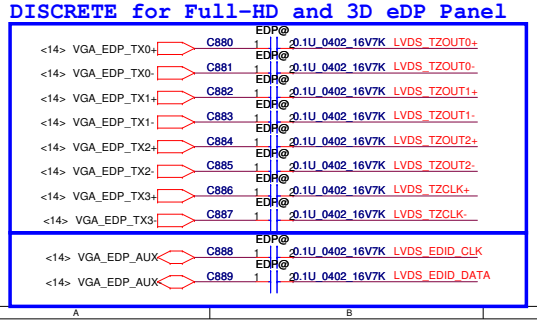
Close to LVDS Connector

DISCRETE for Full-HD and 3D LVDS Panel



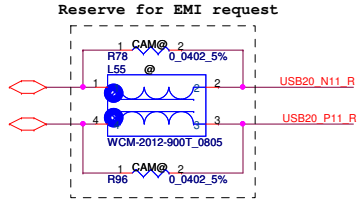
Close to LVDS1 Connector

DISCRETE for Full-HD and 3D eDP Panel

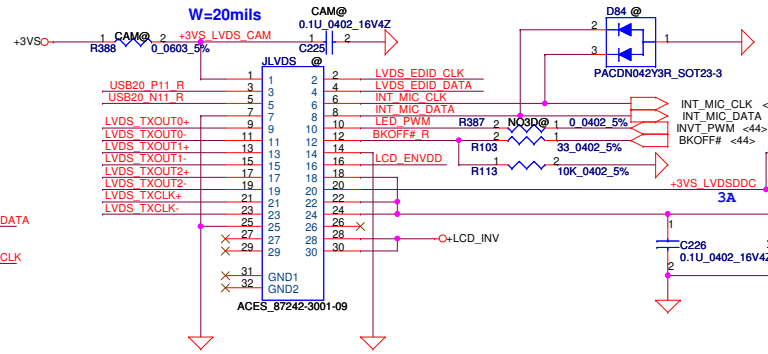


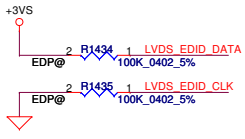
Close to LVDS Connector

Reserve for EMI request

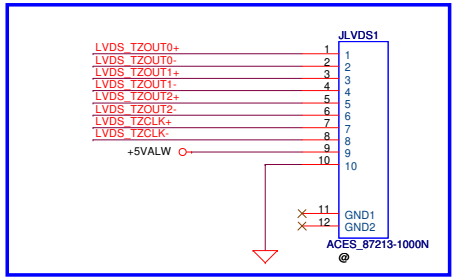


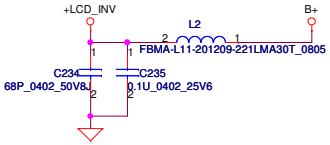
LCD/PANEL BD. Conn.

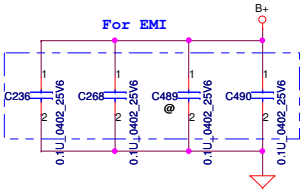


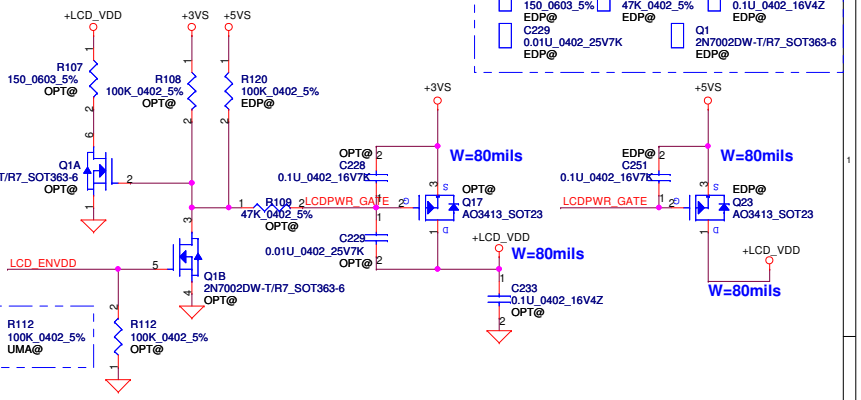


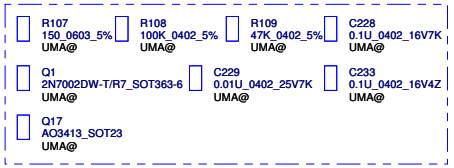
For 3D Panel

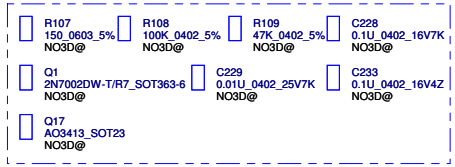












Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title: LVDS/eDP			
Size: Custom	Document Number: PHQAA LA-6831P M/B		Rev: 0.1
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CRT CONNECTOR

OPTIMUS

<31> UMA_CRT_R — R200 OPT@ 0_0402_5% — CRT_R
<31> UMA_CRT_G — R204 OPT@ 0_0402_5% — CRT_G
<31> UMA_CRT_B — R211 OPT@ 0_0402_5% — CRT_B
<31> UMA_CRT_HSYNC — R213 OPT@ 0_0402_5% — CRT_HSYNC
<31> UMA_CRT_VSYNC — R235 OPT@ 0_0402_5% — CRT_VSYNC
<31> UMA_CRT_CLK — R236 OPT@ 0_0402_5% — CRT_CLK
<31> UMA_CRT_DATA — R261 OPT@ 0_0402_5% — CRT_DATA

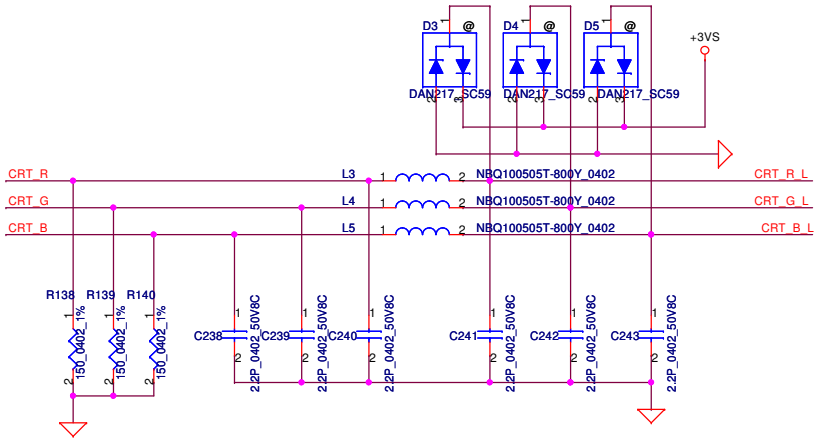
Close to CRT Connector

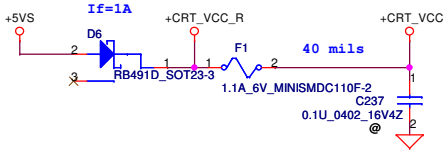
R200 0_0402_5% UMA@
R204 0_0402_5% UMA@
R211 0_0402_5% UMA@
R213 0_0402_5% UMA@
R235 0_0402_5% UMA@
R236 0_0402_5% UMA@
R261 0_0402_5% UMA@

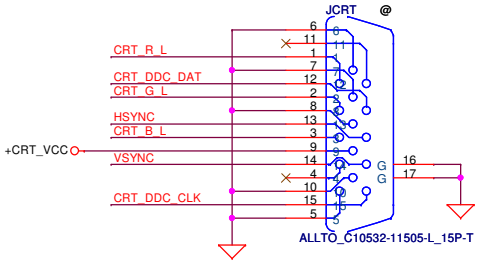
DISCRETE

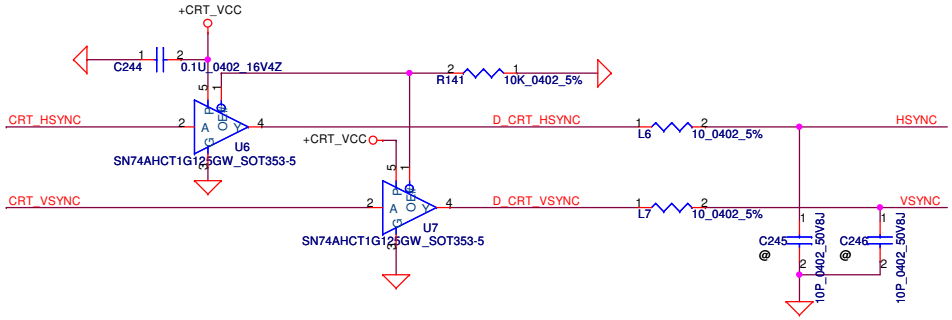
<13> VGA_CRT_R — R178 DIS@ 0_0402_5% — CRT_R
<13> VGA_CRT_G — R181 DIS@ 0_0402_5% — CRT_G
<13> VGA_CRT_B — R167 DIS@ 0_0402_5% — CRT_B
<13> VGA_CRT_HSYNC — R177 DIS@ 0_0402_5% — CRT_HSYNC
<13> VGA_CRT_VSYNC — R179 DIS@ 0_0402_5% — CRT_VSYNC
<13> VGA_CRT_CLK — R193 DIS@ 0_0402_5% — CRT_CLK
<13> VGA_CRT_DATA — R194 DIS@ 0_0402_5% — CRT_DATA

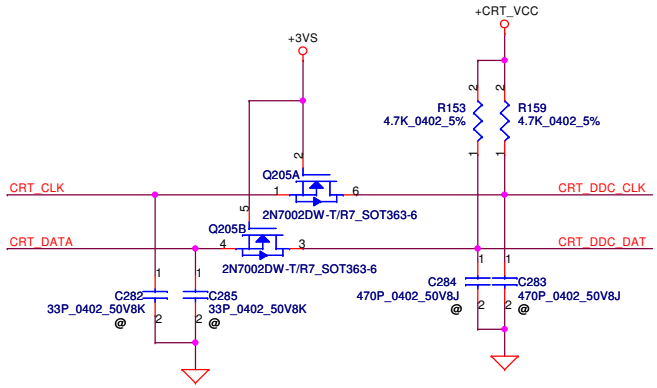
Close to CRT Connector











Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *CRT*

Size | Document Number: **PHQAA LA-6831P M/B** | Rev: 0.1

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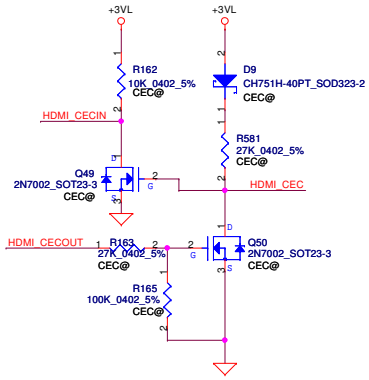
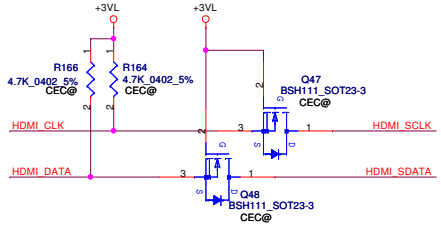
HDMI CEC Controller



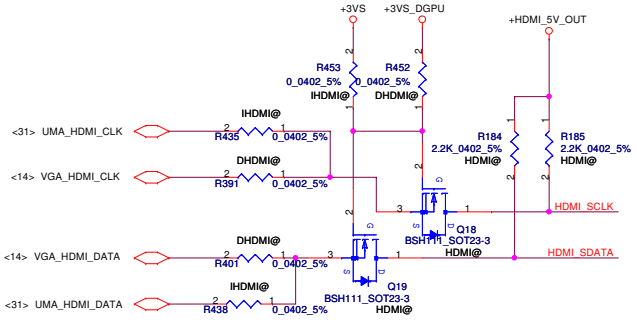


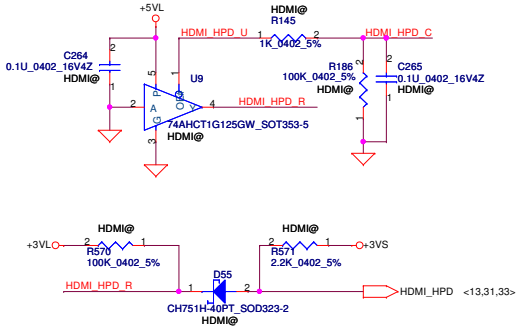
For DISCRETE

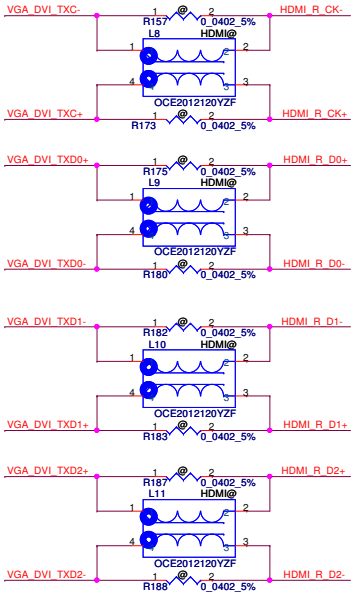
<14> VGA_HDMI_CLK+	CV296	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC+
<14> VGA_HDMI_CLK-	CV293	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC-
<14> VGA_HDMI_TX0+	CV294	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0+
<14> VGA_HDMI_TX0-	CV297	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0-
<14> VGA_HDMI_TX1+	CV299	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1+
<14> VGA_HDMI_TX1-	CV298	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1-
<14> VGA_HDMI_TX2+	CV295	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2+
<14> VGA_HDMI_TX2-	CV300	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2-

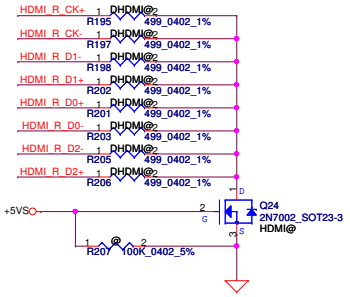
For Optimus

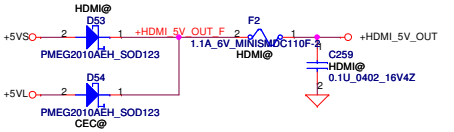
<31> UMA_HDMI_TXC+	CV308	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC+
<31> UMA_HDMI_TXC-	CV304	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC-
<31> UMA_HDMI_TX0+	CV306	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0+
<31> UMA_HDMI_TX0-	CV302	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0-
<31> UMA_HDMI_TX1+	CV303	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1+
<31> UMA_HDMI_TX1-	CV301	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1-
<31> UMA_HDMI_TX2+	CV307	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2+
<31> UMA_HDMI_TX2-	CV305	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2-

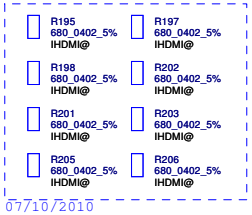






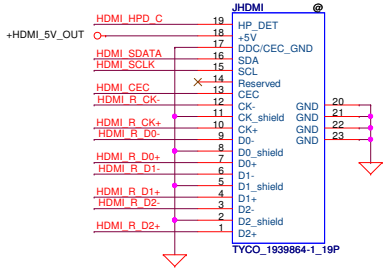






07710/2010
Intel DG P.132

HDMI Connector



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	HDMI Conn./CEC		
Size	Document Number	PHQAA LA-6831P M/B	Rev 0.1
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CMOS Setting, near DDR Door

+RTCVCC — R292 20K_0402_5% — PCH_RTCRST# — C247 1U_0402_6.3V4Z — JCOMS @

iME Setting.

R293 20K_0402_5% — PCH_SRTCRST# — C248 1U_0402_6.3V4Z — JME @

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High = Enable Internal VRs (must be always pulled high)

+RTCVCC
- R117 1M_0402_5% — SM_INTRUDER#
- R118 330K_0402_5% — PCH_INTVRMEN

+3VS
- R276 1K_0402_5% — PCH_SPKR

High = Enabled (No Reboot)
★ Low = Disabled (Default)

+3VALW_PCH
- R560 10K_0402_5% — CR_CPPE#
- R274 1K_0402_5% — PWRME_CTRL#

HDA_SDO

ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC

★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

+3VALW_PCH — R284 1K_0402_5% — AZ_SYNC
+5VS — Q21 BSS138_NL_SOT23-3
<43> AZ_SYNC_HD — R156 33_0402_5% — AZ_SYNC_R
R285 @ 0_0402_5%

For MP phase

PCH_SPIDI	R572	@ 0_0402_5% DI
PCH_SPICLK	R573	@ 0_0402_5% CLK
PCH_SPICS#	R574	@ 0_0402_5% CS#
PCH_SPIDO	R575	@ 0_0402_5% DO

+3VS — R569 @ 0_0603_5% — +3V_SPI

U51 SN74CBT3125PWRG4_TSSOP14 SPI@
- PCH_SPIDI 2A — DI 2B
- PCH_SPICLK 3A — CLK 3B
- PCH_SPICS# 4A — CS# 4B
- PCH_SPIDO 1A — DO 1B
- +3VS — VCC
- C455 SPI@ 0.1U_0402_16V4Z

U53 SN74CBT3125PWRG4_TSSOP14 SPI@
- <44,46,51> EC_ON — 1OE# 2OE# 3OE# 4OE#
- SPIDI <44,45,46> KSI6
- SPICLK <44,45> KSI5
- SPICS# <44,45> KSI4
- SPIDO <44,45> KSI7
- 1A 2A 3A 4A — 1B 2B 3B 4B — DI CLK CS# DO
- +3V_SPI — VCC
- C456 SPI@ 0.1U_0402_16V4Z

8M Byte

+3V_SPI — C494 0.1U_0402_16V4Z — U13 W25Q64BVSSIG_SO8 45@
VCC VSS W HOLD S C D Q
CS# CLK DI DO

Socket: SP07000F500/SP07000H900

for EMI

CLK — R397 10_0402_5% @ — C86 10P_0402_50V8J @

Please close to U2 PCH

+5VALW — C249 SPI@ 0.1U_0402_16V4Z
<44,45> KSO6 — R217 SPI@ 100K_0402_5% — EC_ON
U56A SPI@ LM393DG_SO8
R418 SPI@ 10K_0402_5% — C483 SPI@ 0.1U_0402_16V4Z

U56B SPI@ LM393DG_SO8
<39,44,47,52,54,56> SUSP#
R432 SPI@ 10K_0402_5% — C482 SPI@ 0.1U_0402_16V4Z

D43 RB715FGT106_UMD3 SPI@
R226 SPI@ 100K_0402_5%
Q37 SPI@ AO3416_SOT23-3
+3V_SPI

Please close to U2 PCH,and between U2 & U13

U2A — COUGARPOINT_FCBGA989-D — Q65R1@

RTC
- PCH_RTCX1 A20 RTCX1
- PCH_RTCX2 C20 RTCX2
- PCH_RTCRST# D20 RTCRST#
- PCH_SRTCRST# G22 SRTCRST#
- SM_INTRUDER# K22 INTRUDER#
- PCH_INTVRMEN C17 INTVRMEN

LPC
- FWH0 / LAD0 C38 — LPC_AD0 <44,45>
- FWH1 / LAD1 A38 — LPC_AD1 <44,45>
- FWH2 / LAD2 B37 — LPC_AD2 <44,45>
- FWH3 / LAD3 C37 — LPC_AD3 <44,45>
- FWH4 / LFRAME# D36 — LPC_FRAME# <44,45>
- LDRQ# E36
- LDRQ1# / GPIO23 K36 — FELICA_PWR <38>
- SERIRQ V5 — SERIRQ <44,45>

HDA
- <43> AZ_BITCLK_HD — R286 33_0402_5% — AZ_BITCLK — N34 HDA_BCLK
- AZ_SYNC L34 HDA_SYNC
- <43> PCH_SPKR — PCH_SPKR T10 SPKR
- <43> AZ_RST_HD# — R142 33_0402_5% — AZ_RST# — K34 HDA_RST#
- <43> AZ_SDIN0_HD — AZ_SDIN0_HD E34 HDA_SDIN0
- G34 HDA_SDIN1
- C34 HDA_SDIN2
- +3VALW_PCH — R273 @ 1K_0402_5% — A34 HDA_SDIN3
- <43> AZ_SDOUT_HD — R289 33_0402_5% — AZ_SDOUT — A36 HDA_SDO
- <44> PWRME_CTRL# — PWRME_CTRL# — C36 HDA_DOCK_EN# / GPIO33
- <41> CR_CPPE# — CR_CPPE# — N32 HDA_DOCK_RST# / GPIO13

JTAG
- PCH_JTAG_TCK J3 JTAG_TCK
- T37 PAD — PCH_JTAG_TMS H7 JTAG_TMS
- T38 PAD — PCH_JTAG_TDI K5 JTAG_TDI
- T39 PAD — PCH_JTAG_TDO H1 JTAG_TDO

SPI
- PCH_SPICLK T3 SPI_CLK
- PCH_SPICS# Y14 SPI_CS0#
- T1 SPI_CS1#
- PCH_SPIDI V4 SPI_MOSI
- PCH_SPIDO U3 SPI_MISO

SATA
- SATA0RXN AM3 — SATA_PRX_C_DTX_N0 — SATA_PRX_C_DTX_N0 <37>
- SATA0RXP AM1 — SATA_PRX_C_DTX_P0 — SATA_PRX_C_DTX_P0 <37>
- SATA0TXN AP7 — SATA_PTX_DRX_N0 — SATA_PTX_DRX_N0 <37>
- SATA0TXP AP5 — SATA_PTX_DRX_P0 — SATA_PTX_DRX_P0 <37>

HDD

- SATA1RXN AM10
- SATA1RXP AM8
- SATA1TXN AP11
- SATA1TXP AP10

- SATA2RXN AD7 — SATA_PRX_C_DTX_N2 — SATA_PRX_C_DTX_N2 <37>
- SATA2RXP AD5 — SATA_PRX_C_DTX_P2 — SATA_PRX_C_DTX_P2 <37>
- SATA2TXN AH5 — SATA_PTX_DRX_N2 — SATA_PTX_DRX_N2 <37>
- SATA2TXP AH4 — SATA_PTX_DRX_P2 — SATA_PTX_DRX_P2 <37>

ODD

- SATA3RXN AB8
- SATA3RXP AB10
- SATA3TXN AF3
- SATA3TXP AF1

- SATA4RXN Y7
- SATA4RXP Y5
- SATA4TXN AD3
- SATA4TXP AD1

- SATA5RXN Y3
- SATA5RXP Y1
- SATA5TXN AB3
- SATA5TXP AB1

- SATAICOMPO Y11
- SATAICOMPI Y10 — SATAICOMP — R279 37.4_0402_1% — +1.05VS_VCC_SATA
- SATA3RCOMPO AB12
- SATA3COMPI AB13 — SATA3_COMP — R280 49.9_0402_1% — +1.05VS_SATA3
- SATA3RBIAS AH1 — RBIAS_SATA3 — R281 750_0402_1%
- SATALED# P3 — SATA_LED# — SATA_LED# <46>
- SATA0GP / GPIO21 V14 — CR_WAKE# — CR_WAKE# <41>
- SATA1GP / GPIO19 P1 — PCH_GPIO19 — PCH_GPIO19 <32>

BOOT BIOS Strap Bit 0

+3VS
- SERIRQ — R136 10K_0402_5%
- SATA_LED# — R336 10K_0402_5%
- CR_WAKE# — R334 10K_0402_5%
- PCH_GPIO19 — R335 10K_0402_5%

+RTCBATT — D13 BAS40-04_SOT23-3 — +3VL
+RTCVCC — C486 0.1U_0402_16V4Z

+3VALW_PCH
- R363 200_0402_5% — PCH_JTAG_TMS — R306 100_0402_1%
- R330 200_0402_5% — PCH_JTAG_TDO — R295 100_0402_1%
- R278 200_0402_5% — PCH_JTAG_TDI — R301 100_0402_1%
- R355 51_0402_1% — PCH_JTAG_TCK

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCH_HDA/JTAG/SATA/SPI/LPC

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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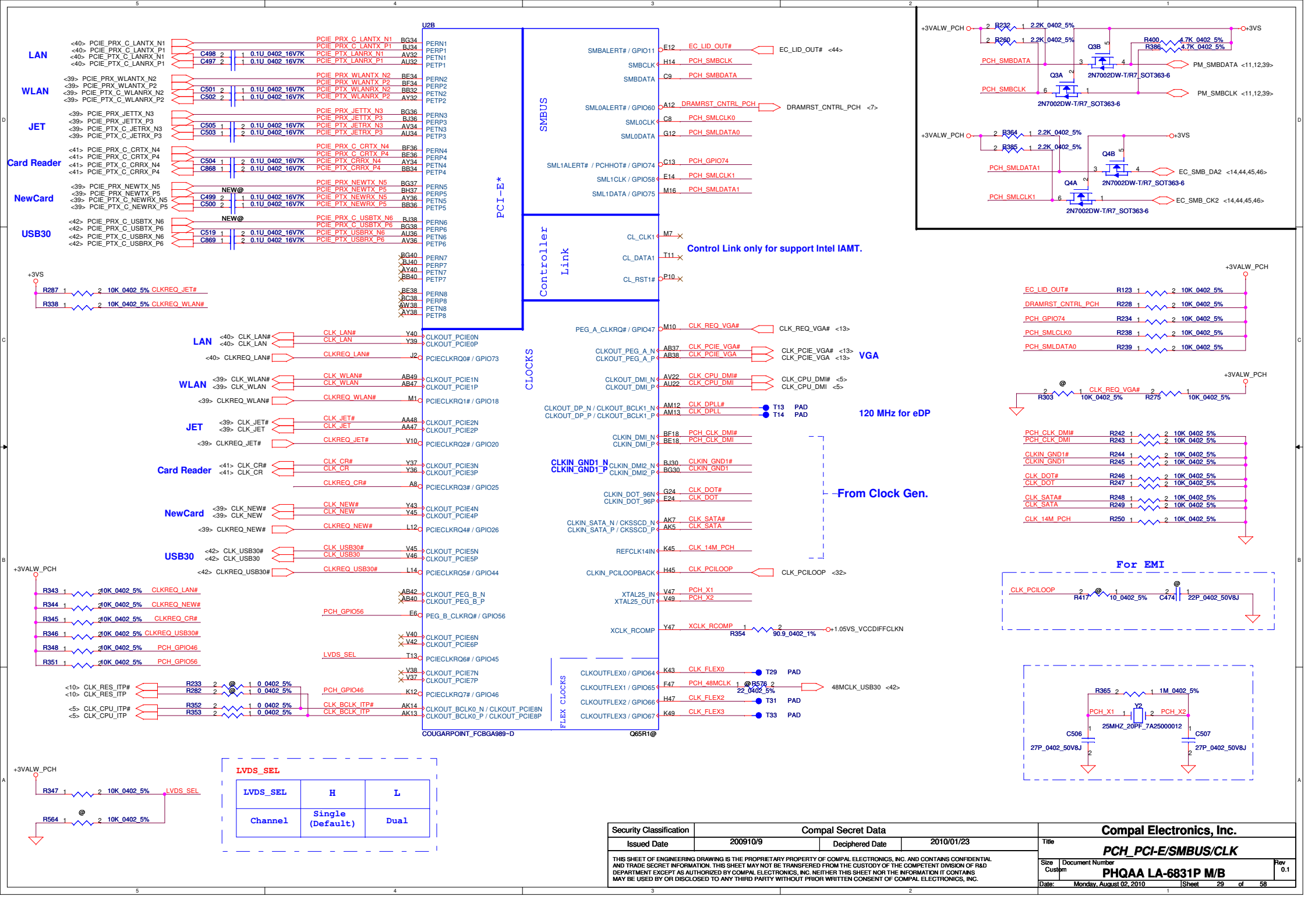
U2B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGARPOINT_FCBGA989~D
Q65R1@
LAN
WLAN
JET
Card Reader
NewCard
USB30
Control Link only for support Intel IAMT.
VGA
120 MHz for eDP
From Clock Gen.
For EMI
LVDS_SEL
LVDS_SEL | H | L
Channel | Single (Default) | Dual
Security Classification
Compal Secret Data
Issued Date
200910/9
Deciphered Date
2010/01/23
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Title
PCH_PCI-E/SMBUS/CLK
Size Custom
Document Number
PHQAA LA-6831P M/B
Rev 0.1
Date: Monday, August 02, 2010
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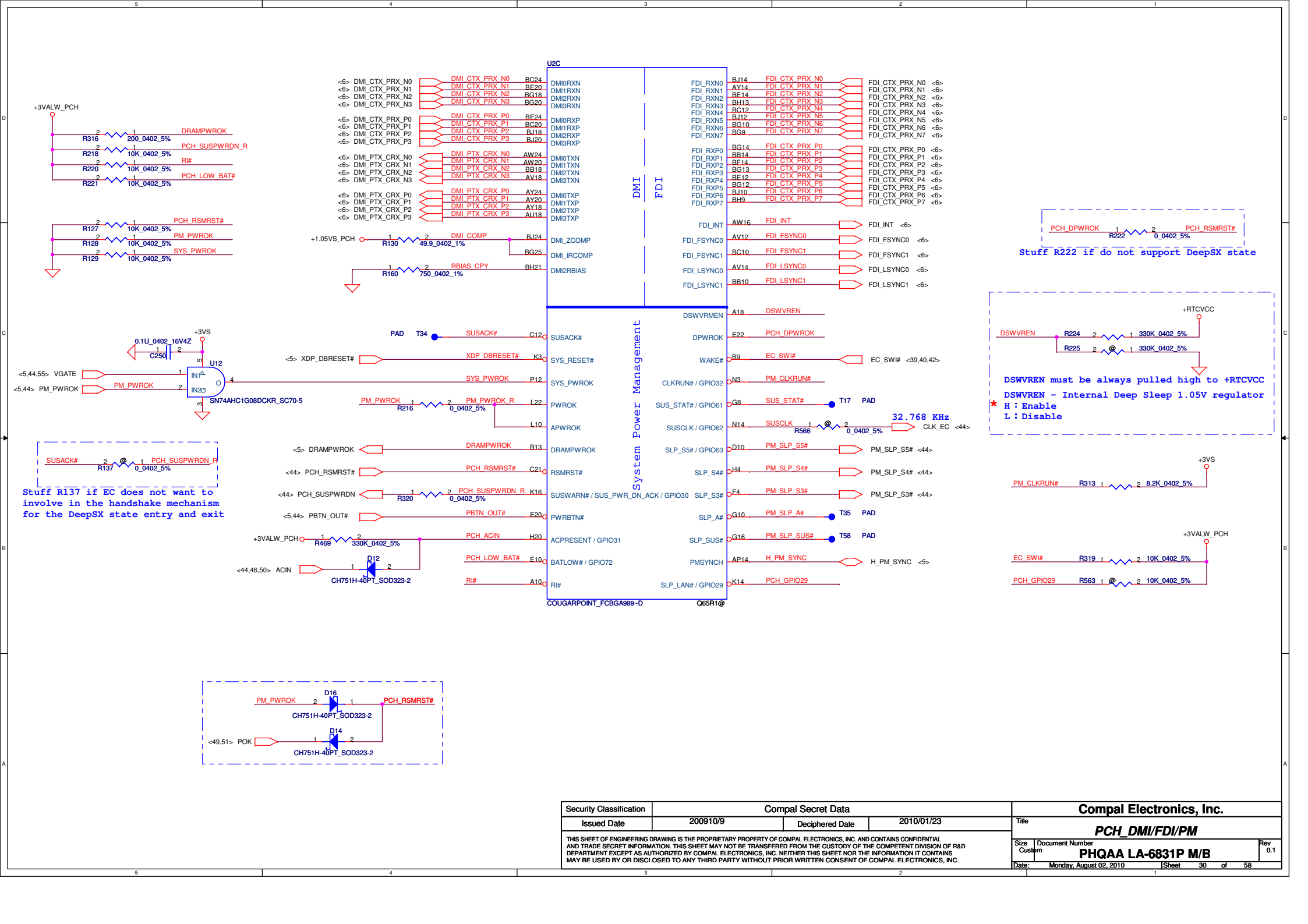

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Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *PCH_DMI/FDI/PM*

Size	Document Number	Rev
Custom	PHQAA LA-6831P M/B	0.1

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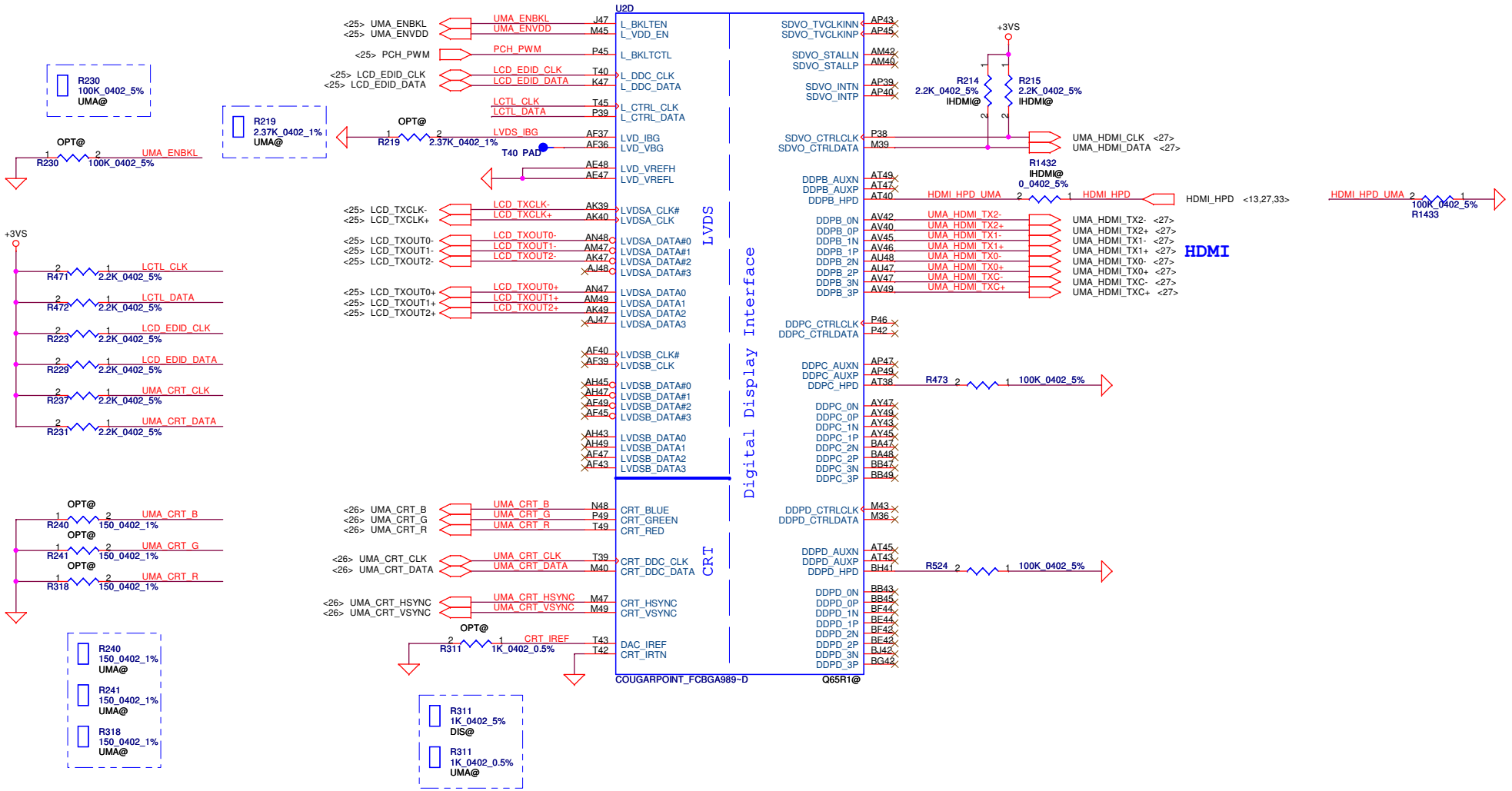

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ***PCH_CRT/LVDS/HDMI***

Size	Document Number	Rev
Custom	**PHQAA LA-6831P M/B**	0.1

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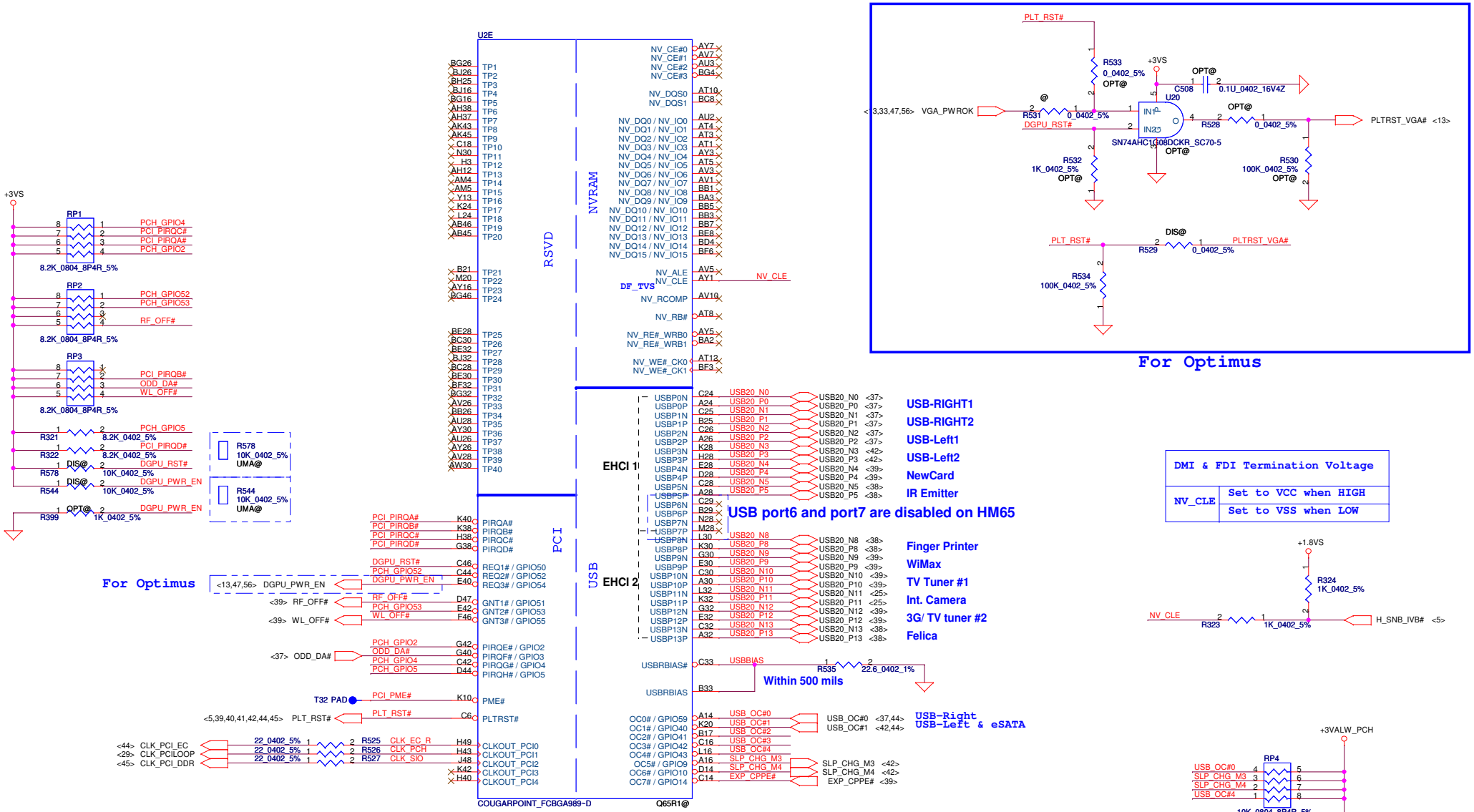


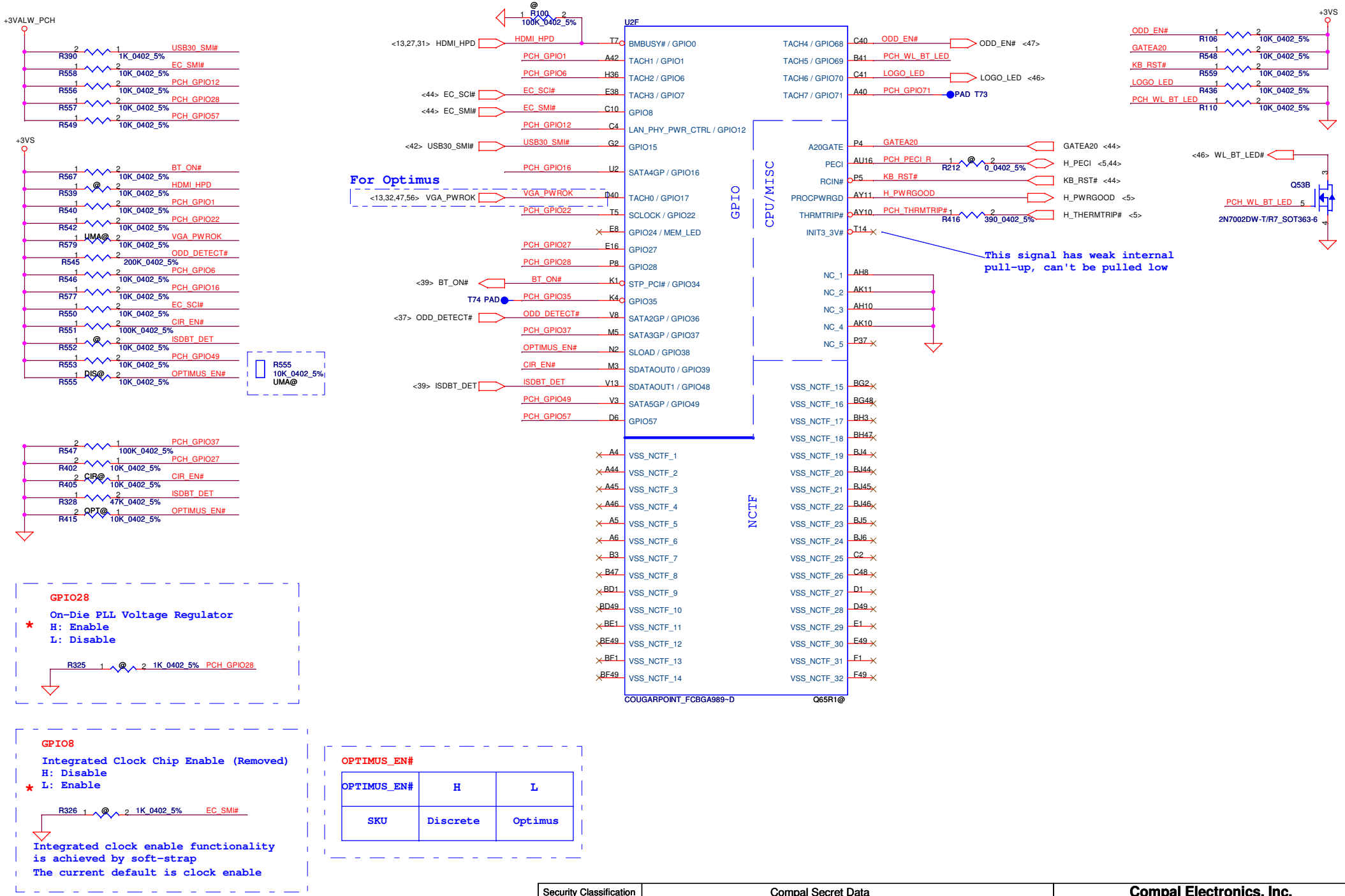
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *PCH_PCI/USB/NAND*

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

Date: Monday, August 02, 2010 | Sheet 32 of 58



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCH_CPU/GPIO

Size: B | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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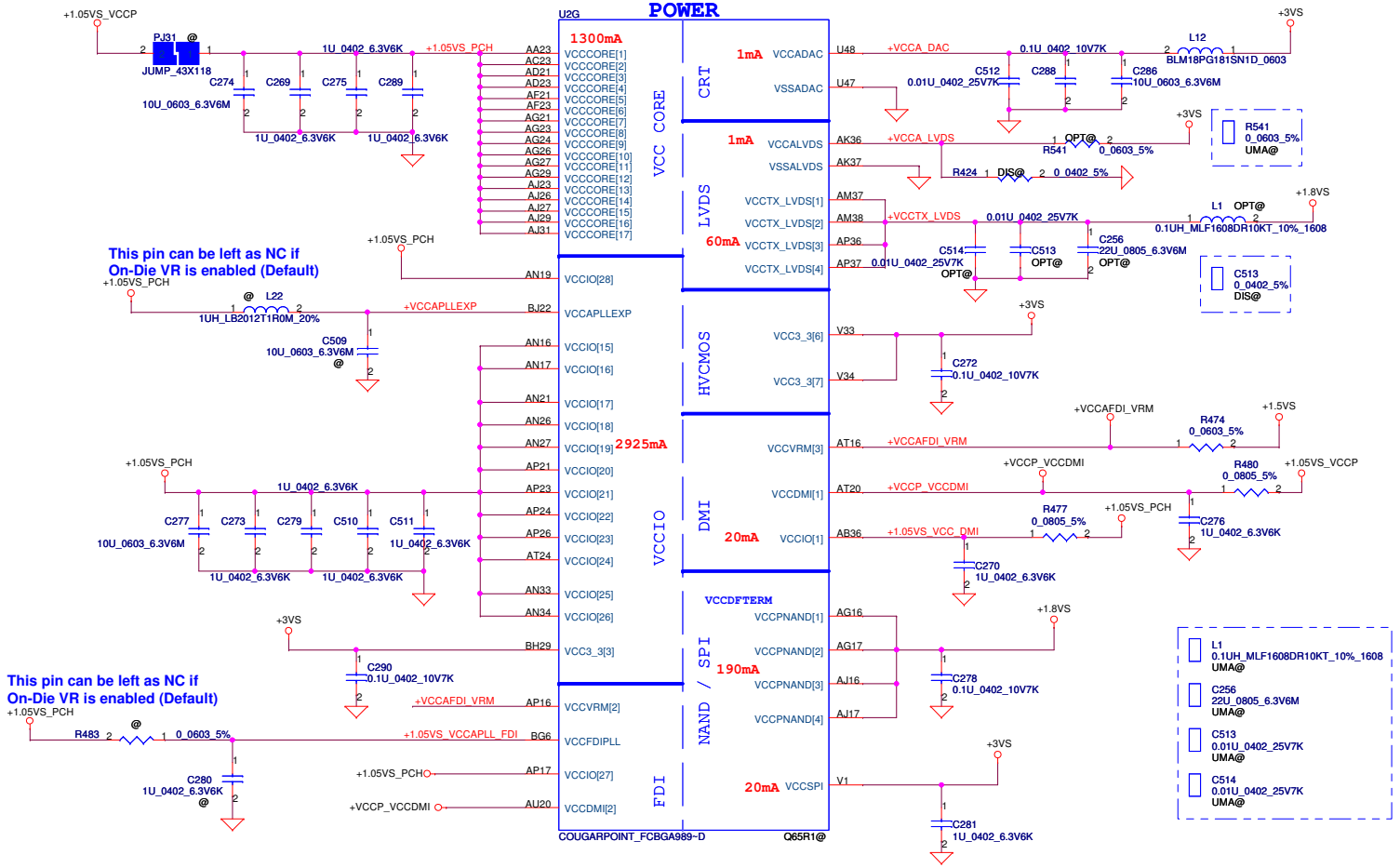
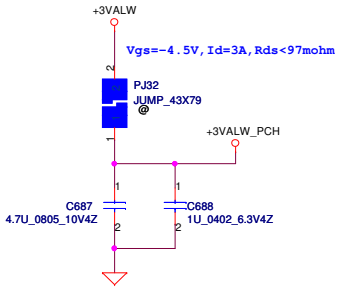


PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSusHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: *PCH_POWER-1*

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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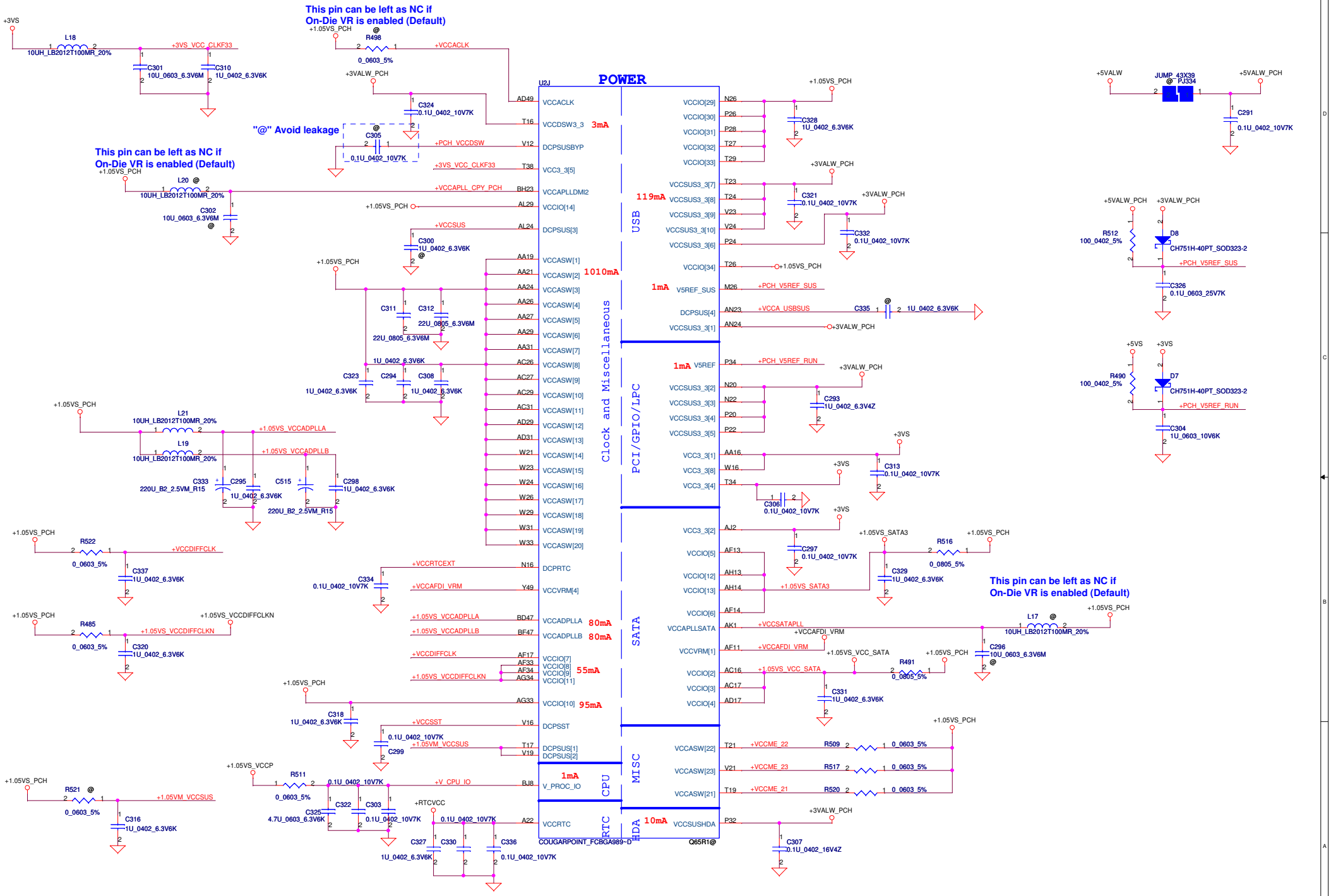

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ***PCH_POWER-2***

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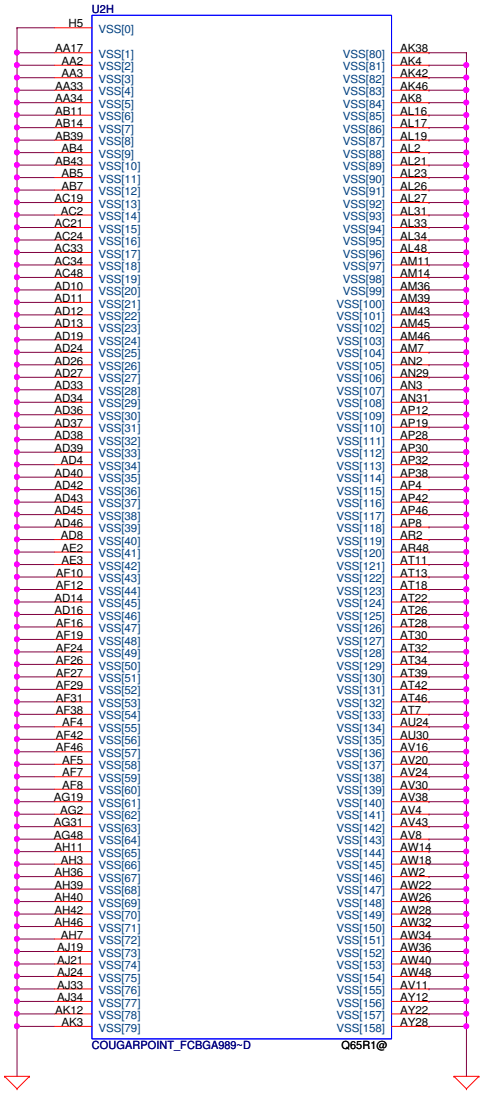

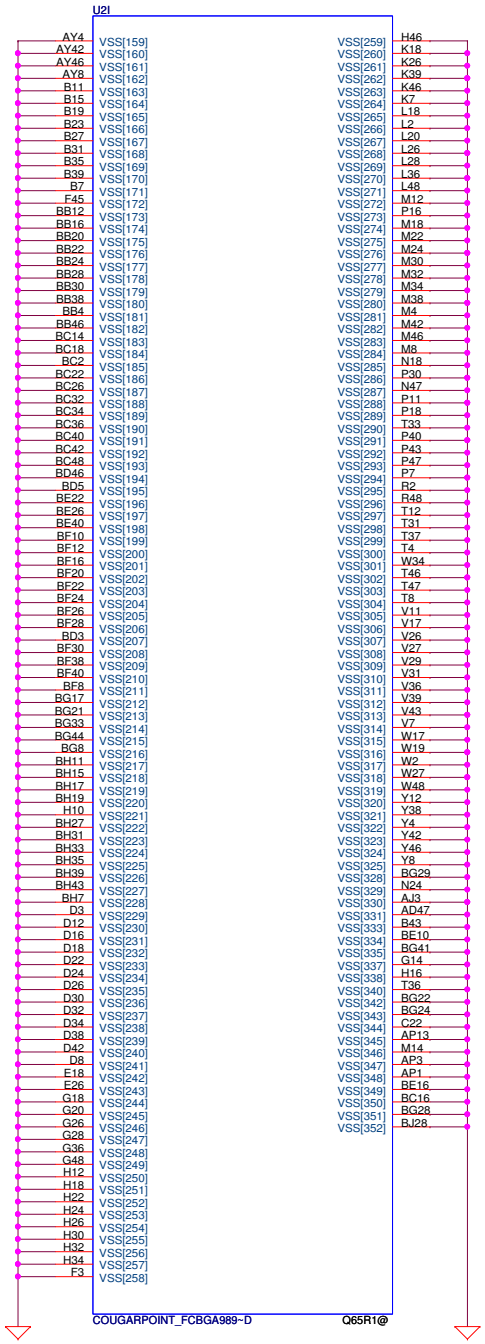

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: ***PCH_GND***

Size	Document Number	Rev
Custom	PHQAA LA-6831P M/B	0.1

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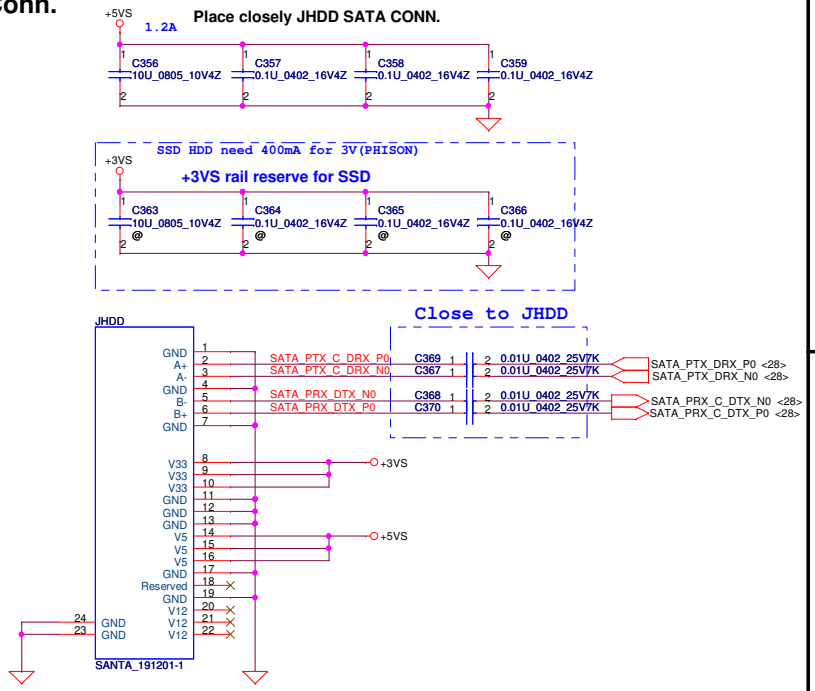
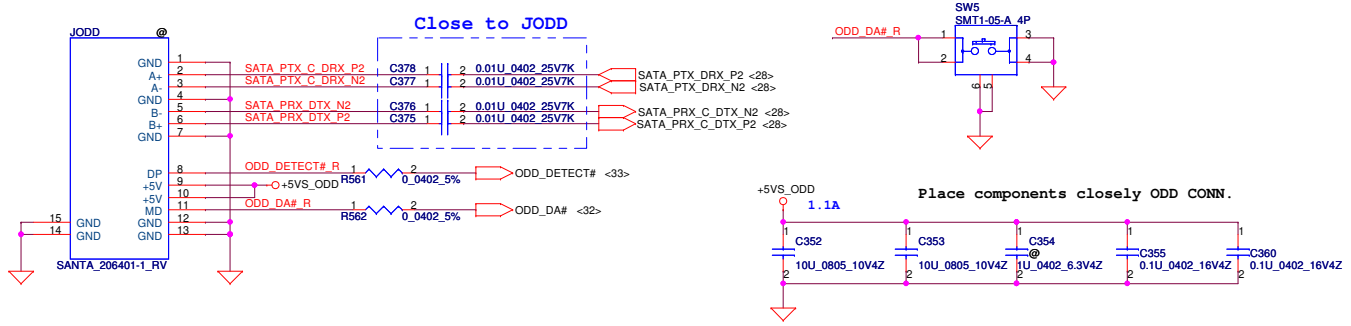
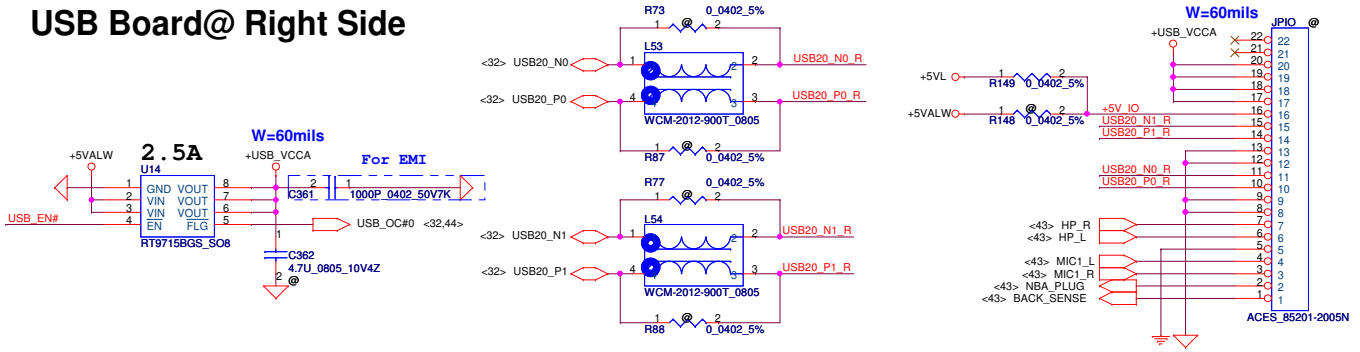
SATA HDD Conn.



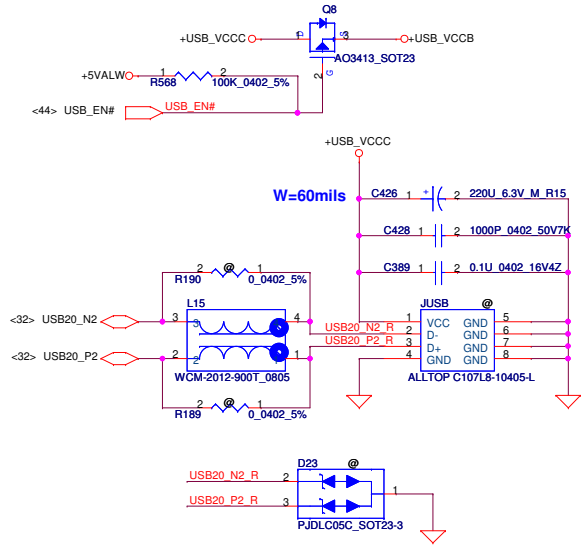
SATA ODD Conn



USB Board@ Right Side



USB Board@ Left Side



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **SATA-HDD/ODD/USB**

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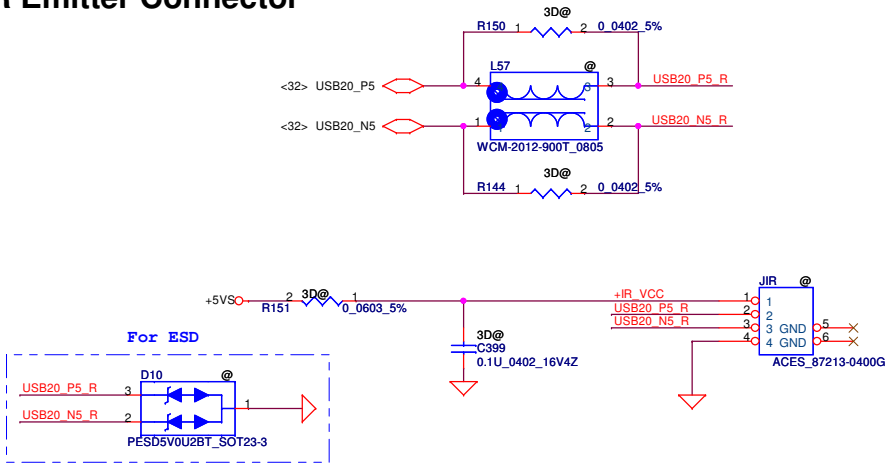
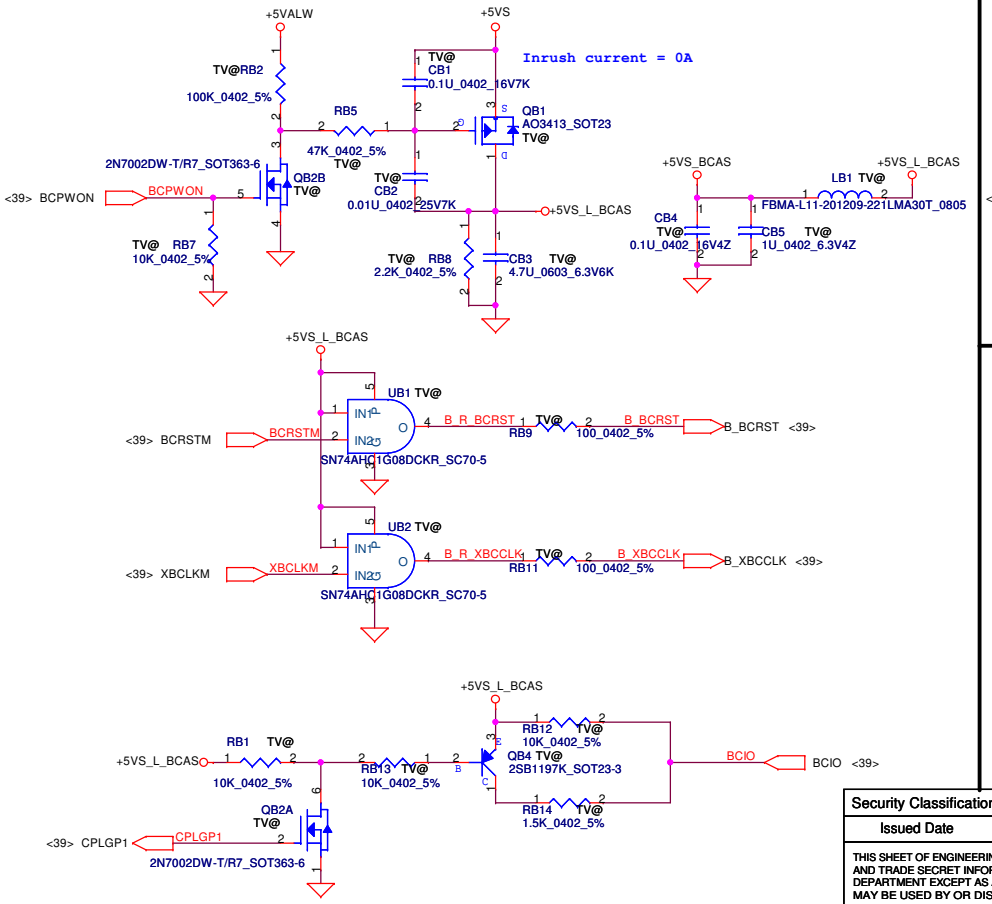
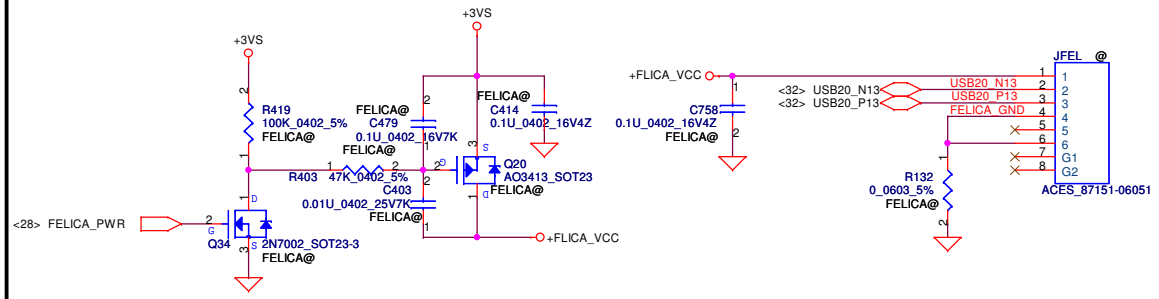
IR Emitter Connector



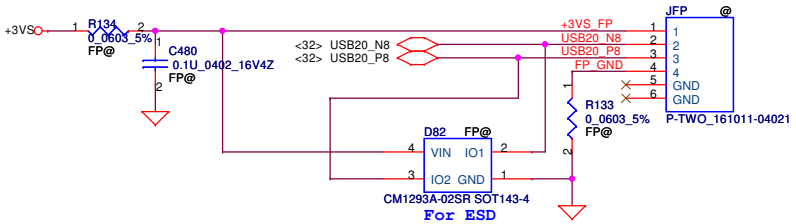
B-CAS Circuit



Felica



Finger printer



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	IR/FP/B-CAS/Felica		
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax

+3VALW — PJ27@ JUMP_43X79 — +3V_WLAN
+3VS — PJ26@ JUMP_43X79

Short PJ27 for Wimax
Short PJ26 for WLAN

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24

SUSP# — D24 CH751H-40PT_SOD323-2 — BT_CTRL
<33> BT_ON# — Q36 2N7002_SOT23-3

+3V_WLAN — 40 mils — For SED
0.1U_0402_16V4Z — CM1 CM2 CM3 C253 47P_0402_50V8J @
0.01U_0402_25V7K 4.7U_0805_10V4Z

+1.5VS — For SED
0.1U_0402_16V4Z — CM7 CM8 CM9 C254 47P_0402_50V8J @
0.01U_0402_25V7K 4.7U_0805_10V4Z

JWLAN @ — FOX_AS0B226-S40N-7F

<29> CLKREQ_WLAN#
<29> CLK_WLAN#
<29> CLK_WLAN
BT_CTRL
<29> PCIE_PRX_WLANTX_N2
<29> PCIE_PRX_WLANTX_P2
<29> PCIE_PTX_C_WLANRX_N2
<29> PCIE_PTX_C_WLANRX_P2

WLAN/ WiFi

+3V_WLAN
R16 0_0402_5% — <44> E51_TXD
R17 0_0402_5% — <44> E51_RXD
E51_RXD_R
Debug card using

PLT_RST# — WL_OFF# <32> — PLT_RST# <5,32,40,41,42,44,45>
PM_SMBCLK <11,12,29>
PM_SMBDATA <11,12,29>
USB20_N9 <32>
USB20_P9 <32>
WiMax
LED_WIMAX# — LED_WIMAX# <46>
RM6 100K_0402_5% — +3VS — WIMAX@

BT_CTRL — R327 1K_0402_5% — E51_RXD_R
For isolate Intel Rainbow Peak and Compal Debug Card.

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET

PCIE--JET
B-CAS

<38> XBCLKM
BCCDET
<29> CLKREQ_JET#
<29> CLK_JET#
<29> CLK_JET
<38> BCRSTM
<38> BCPWON
<29> PCIE_PRX_JETTX_N3
<29> PCIE_PRX_JETTX_P3
<29> PCIE_PTX_C_JETRX_N3
<29> PCIE_PTX_C_JETRX_P3
<44> TMPTU2_SXP

J3G @ — FOX_AS0B226-S40N-7F — **2.75A**

+1.5VS +3VS
UIM_DATA — +UIM_PWR
UIM_CLK
UIM_RESET
COMMON
ISDBT_DET — ISDBT_DET <33>
RF_OFF# — RF_OFF# <32>
PLT_RST#
USB20_P10_TV — R126 TV@ 0_0402_5% — USB20_P10 <32>
USB20_N10_TV — R135 TV@ 0_0402_5% — USB20_N10 <32>
USB--TV#2
R72 3G@ 0_0402_5% — PM_SMBCLK
R85 3G@ 0_0402_5% — PM_SMBDATA
USB20_N12 <32>
USB20_P12 <32> **USB--3G/TV#1**
LED_WIMAX#
CPLGP1 — CPLGP1 <38> TMPTU1_SXP <44>
B-CAS

Add BCCDET pull down
BCCDET — R307 TV@ 470_0402_5%

+3VS 120 mils For SED
0.1U_0402_16V4Z — CM4 CM5 CM6 C255 47P_0402_50V8J @
0.01U_0402_25V7K 4.7U_0805_10V4Z

RM3 0_0402_5% — 3G@ — UIM_VPP
COMMON — TV@ — BCIO — BCIO <38>
RM7 0_0402_5%

Close to J3G
+5VS_BCAS — RM4 TV@ 0_0603_5% — +VCC_SIM
+UIM_PWR — RM1 3G@ 0_0603_5%
UIM_RESET — RM5 3G@ 0_0402_5% — SIM_RESET
<38> B_BCRST — B_BCRST — RM8 TV@ 0_0402_5%
UIM_CLK — RM9 3G@ 0_0402_5% — SIM_CLK
<38> B_XBCCLK — B_XBCCLK — RM10 TV@ 0_0402_5%
UIM_DATA — RM11 3G@ 0_0402_5% — SIM_DATA
BCIO — RM12 TV@ 0_0402_5%

+VCC_SIM
SIM_RESET
SIM_CLK
J3GSIM @ — MOLEX_47273-0001~D
VCC GND RST VPP CLK I/O NC NC
UIM_VPP
SIM_DATA
+UIM_PWR — RM2 4.7K_0402_5%
CM13 0.1U_0402_16V4Z 3G@
DM1 RLZ20A_LL34 3G@
CM15 10P_0402_50V8J 3G@
CM16 10P_0402_50V8J 3G@
CM14 22P_0402_50V8J @

+3VALW
NEW@ — RN4 — CP_USB# — 100K_0402_5%

+3VALW_CARD — Imax = 0.275A — CN1 10U_0805_10V4Z NEW@ — CN2 0.1U_0402_16V4Z NEW@
+3VS_CARD — Imax = 1.35A — CN3 10U_0805_10V4Z NEW@ — CN4 0.1U_0402_16V4Z NEW@
+1.5VS_CARD — Imax = 0.75A — CN5 10U_0805_10V4Z NEW@ — CN6 0.1U_0402_16V4Z NEW@

UN1 NEW@ — TPS2231MRGPR-2 QFN
+1.5VS — 1.5Vin 1.5Vin — 1.5Vout 1.5Vout — **40mils** — +1.5VS_CARD
+3VS — 3.3Vin 3.3Vin — 3.3Vout 3.3Vout — **60mils** — +3VS_CARD
+3VALW — AUX_IN — AUX_OUT — **20mils** — +3VALW_CARD
PLT_RST# — SYSRST# — OC#
<42,44,52> SYSON — SYSON — SHDN# — PERST# — PERST#
<28,44,47,52,54,56> SUSP# — SUSP# — STBY# — NC
EXP_CPPE# — CPPE# — GND
CP_USB# — CPUSB# — Thermal_Pad
RCLKEN — RCLKEN

Reserve for EMI request
R125 NEW@ 0_0402_5%
L56 @ — WCM-2012-900T_0805
R124 NEW@ 0_0402_5%
<32> USB20_P4 — USB20_P4_R
<32> USB20_N4 — USB20_N4_R

JEXP @ — SANTA_130801-5_NR
USB20_N4_R
USB20_P4_R
CP_USB#
PM_SMBCLK
PM_SMBDATA
+1.5VS_CARD
<30,40,42> EC_SWI# — +3VALW_CARD
PERST# — +3VS_CARD
CLKREQ#
<32> EXP_CPPE#
<29> CLK_NEW#
<29> CLK_NEW
<29> PCIE_PRX_NEWTX_N5
<29> PCIE_PRX_NEWTX_P5
<29> PCIE_PTX_C_NEWRX_N5
<29> PCIE_PTX_C_NEWRX_P5

+3VS — RN6 10K_0402_5% @ — CN7 0.1U_0402_16V4Z @
RN7 10K_0402_5% @
CLKREQ# — UN2 NC7SZ32P5X_NL_SC70-5 — CLKREQ_NEW# — CLKREQ_NEW# <29>
RCLKEN — Q27 2N7002_SOT23-3 @

NEW@ — CLKREQ# — RN8 — CLKREQ_NEW# — 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.
Title: PCIe-WLAN/JET/3G/TV/NewCard
Size: Document Number: PHQAA LA-6831P M/B
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Date: Monday, August 02, 2010
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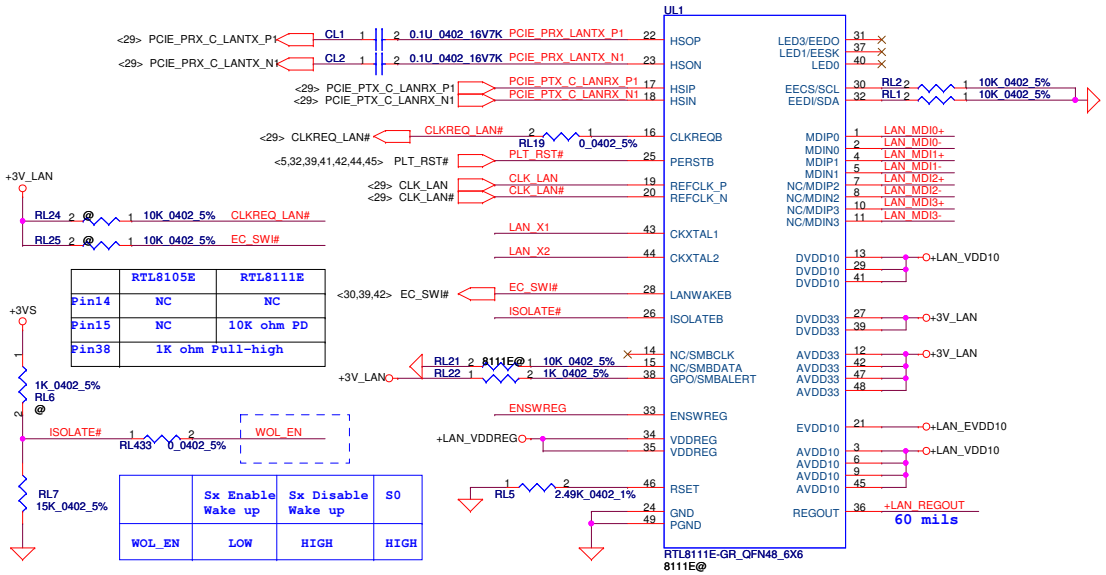
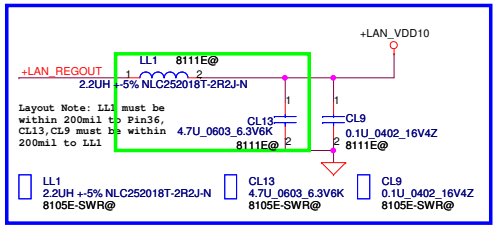
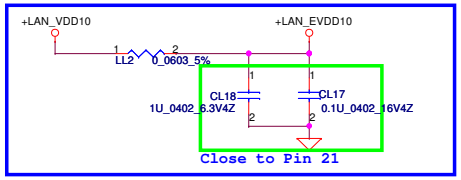
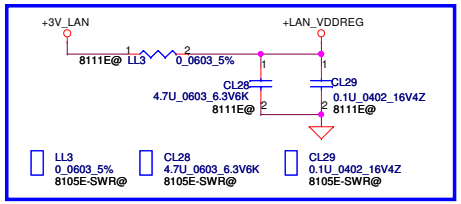


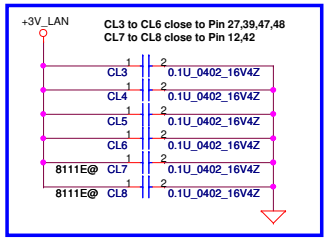
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

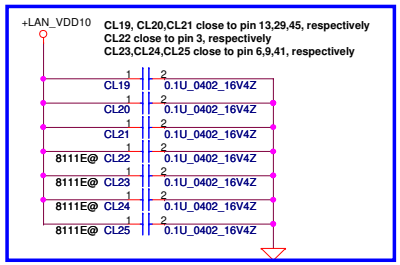
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN	LOW	HIGH	HIGH

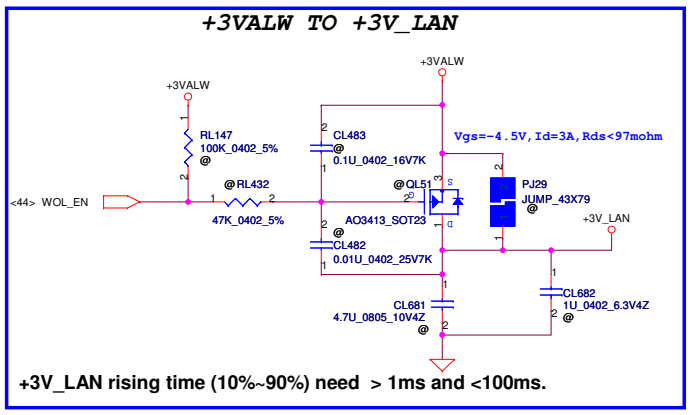


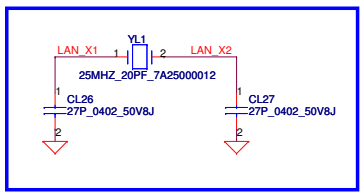


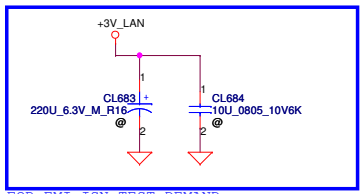




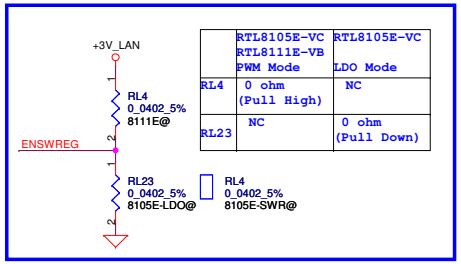






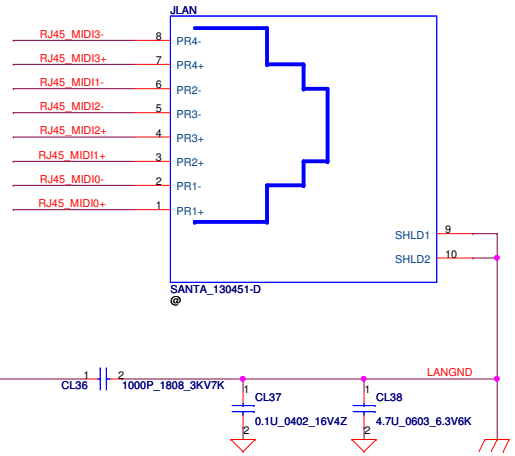


FOR EMI ISN TEST DEMAND.



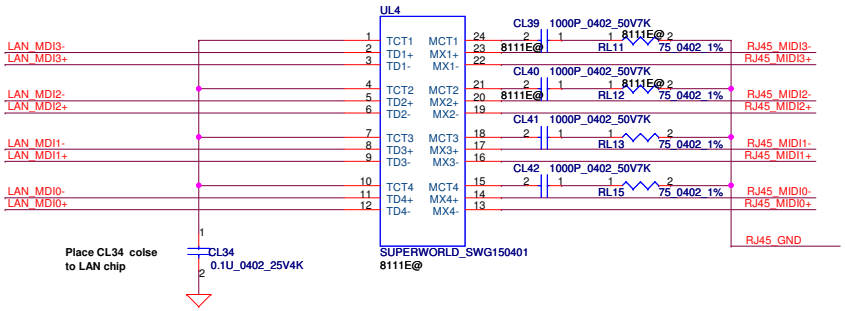
	RTL8105E-VC RTL8111E-VB PWM Mode	RTL8105E-VC RTL8111E-VB LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

LAN Conn.



For P/N and footprint
Please place them to ISPD page

UL1 — 8105E-VC 10/100M 8105E-LDO@
UL1 — 8105E-VC 10/100M 8105E-SWR@
UL4 — 10/100M transformer 8105E-LDO@
UL4 — 10/100M transformer 8105E-SWR@



Security Classification	Compal Secret Data		
Issued Date	2009/10/05	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E/8111E

Size: Custom | Document Number: PHQAA LA-6831P M/B | Rev: 0.1

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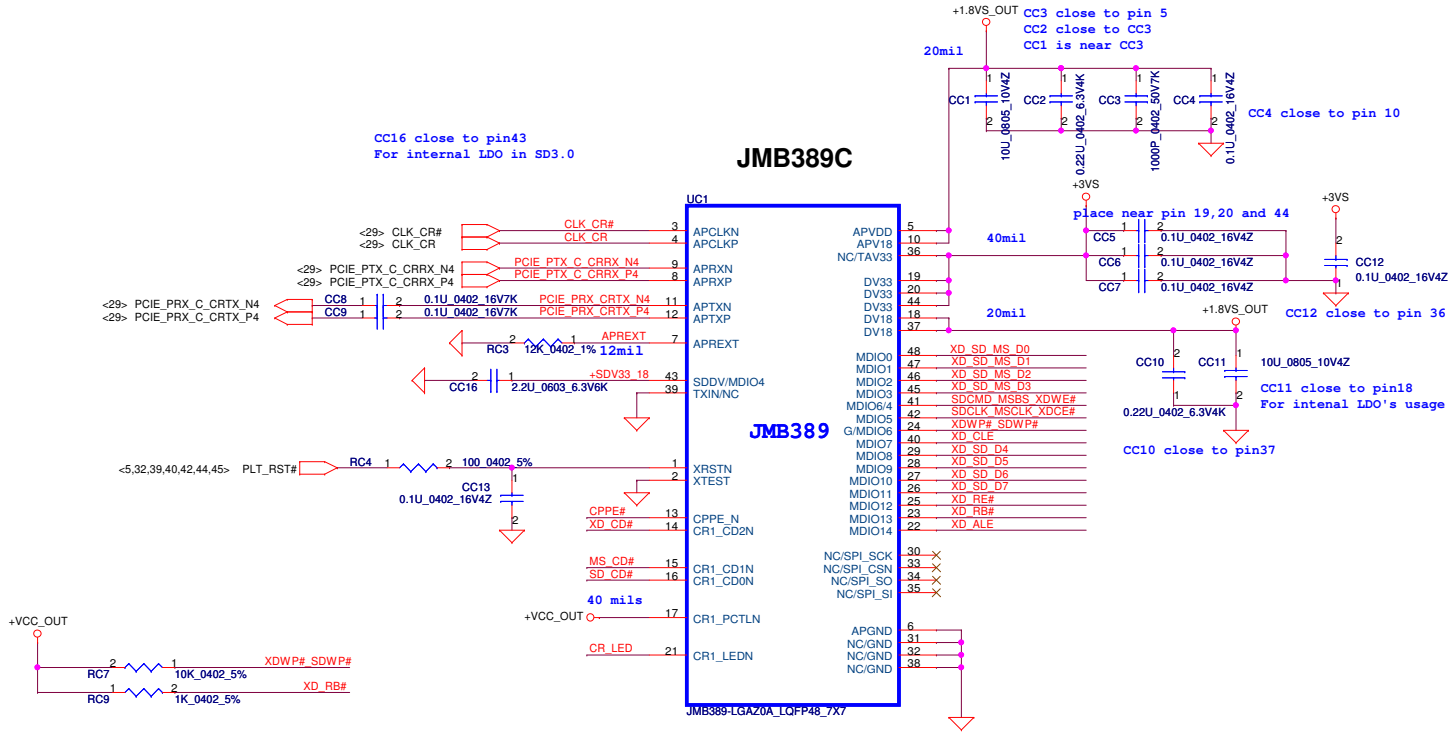
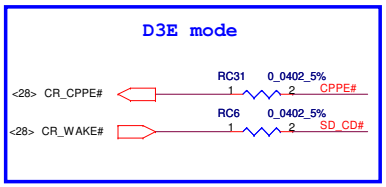
JMB389C

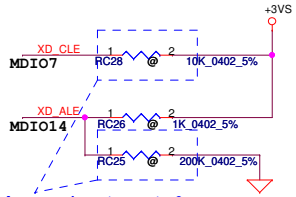


D3E mode

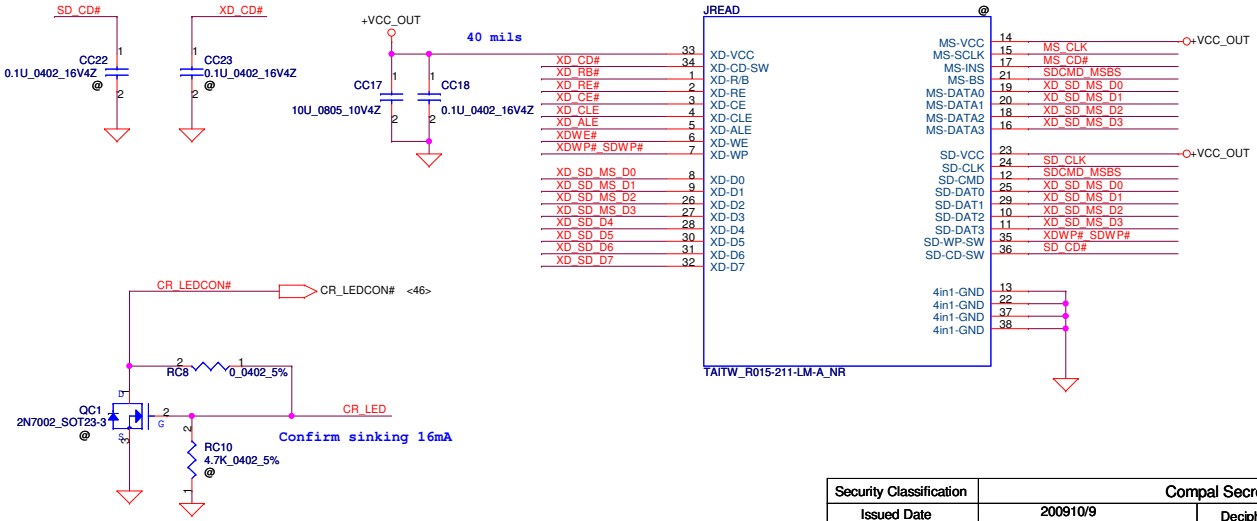


Power On Strapping setting

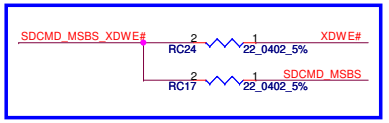
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★

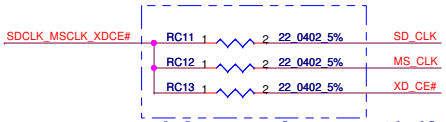


5 in 1 Card Reader

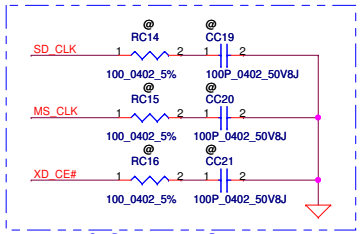


Add RC24 and RC17 close to UC1 for xD issue





Reserved for EMI,close to UC1.42



Reserved for EMI,close to JREAD

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.	
Title	PCIe-CardReader JMB389
Size: Custom	Document Number: PHQAA LA-6831P M/B
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+1.5V to +1.05V Transfer

UT2 APL5930KAI-TRG_SO8 — 1A

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

Close to U102.D7 / Close to U102.P13

Follow Vendor recommend.

<BOM Structure>
UT1

+3V:200mA
+1.05V:800mA

CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock

Place as close as possibile to UU102.N14 and UU102.M14

UPD720200AF1-XXX-A_FBGA176

Close to UU37.6

UT4 MX25L5121EMC-20G SOP 8P — 35mA

USB Sleep & Charge Auto-Mode

07/08/2010
Need EC to set these signals to high active
SLP_CHG, USB_CHG_EN

OCP: 2A
W=80mils

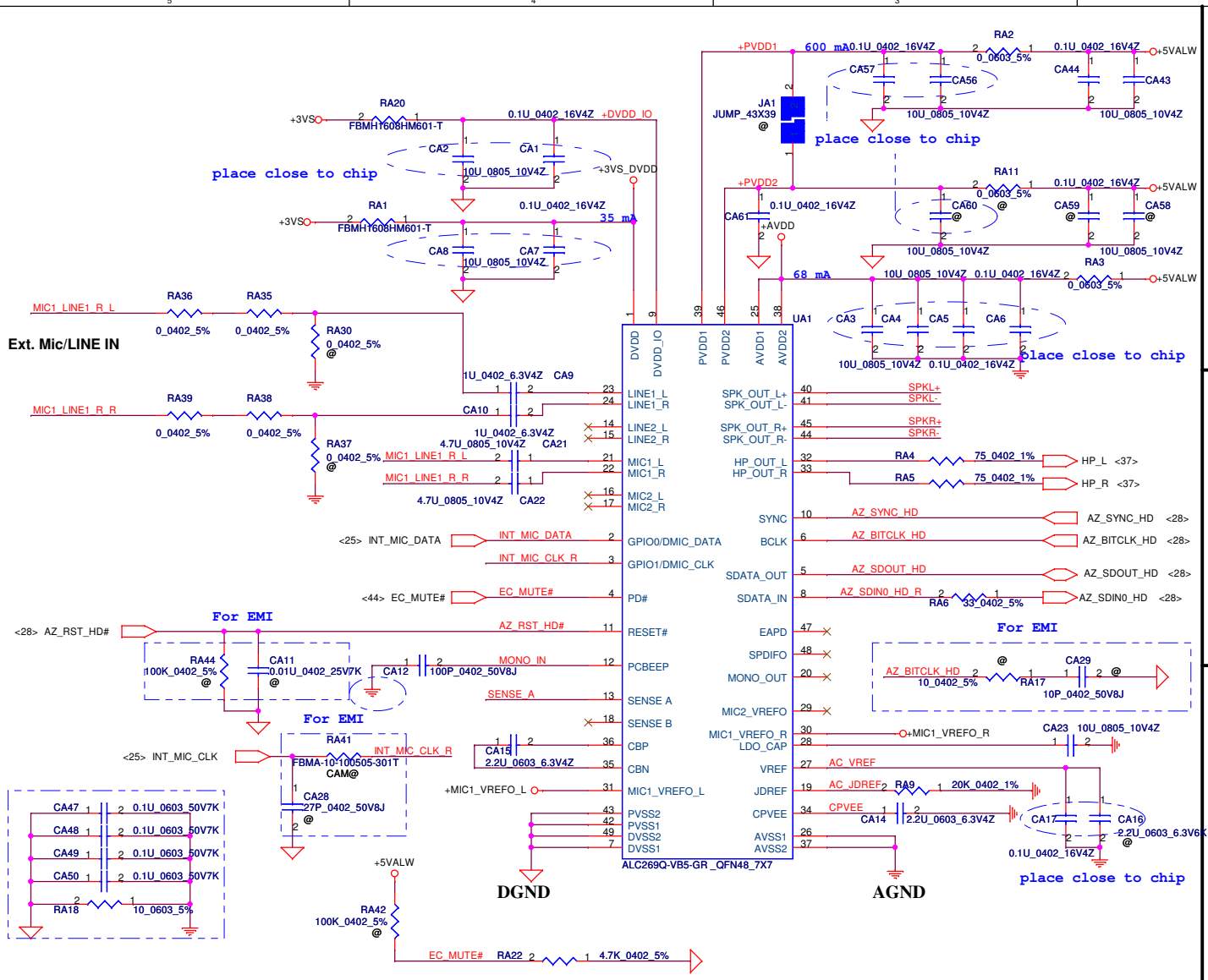
TPS2541RTER_QFN16_3X3

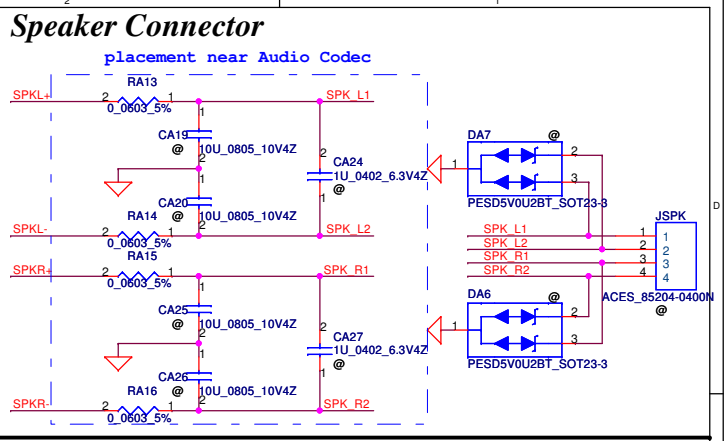
SLP_CHG_M4	SLP_CHG_M3	SLP_CHG	Mode
0	0	X(1)	Dedicated Charging Port, Auto-detect
0	1	X(1)	Dedicated Charging Port, BC Specification 1.1 Only (Mode 3)
1	0	X(1)	Dedicated Charging Port, Apple Only (Mode 4)
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

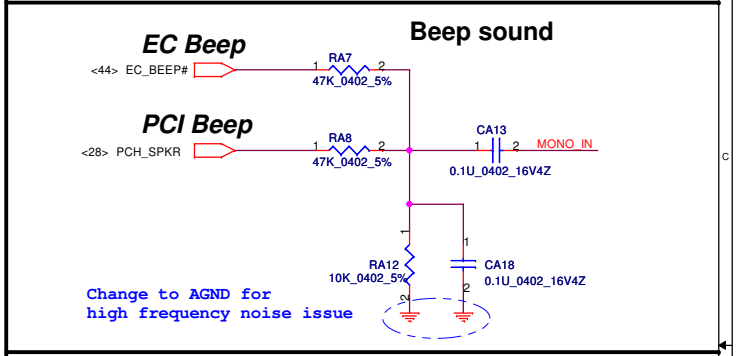
Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

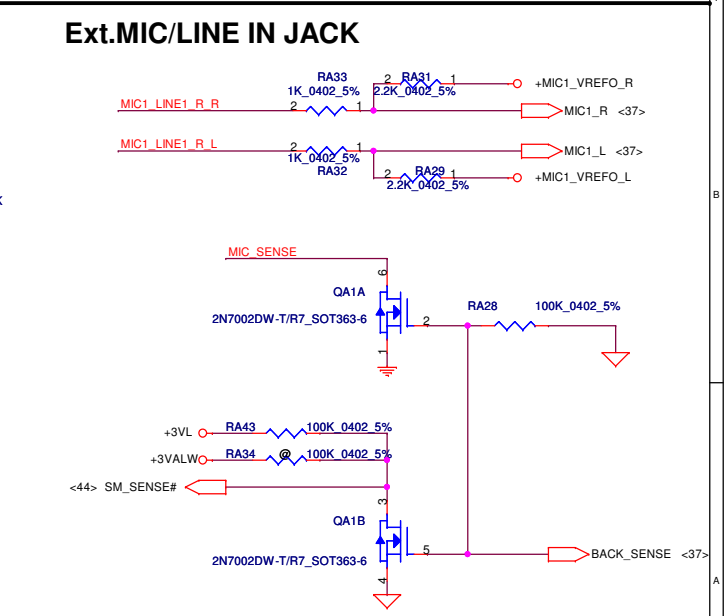
Compal Electronics, Inc.

Title	PCIe-USB3.0 UPD720200A		
Size: Custom	Document Number: PHQAA LA-6831P M/B		Rev: 0.1
Date: Monday, August 02, 2010	Sheet 42 of 58		

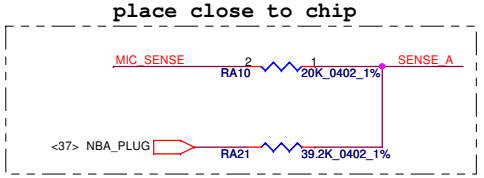








Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	HDA-ALC269/HP/MIC		
Size	Document Number		Rev
	PHQAA LA-6831P M/B		0.1
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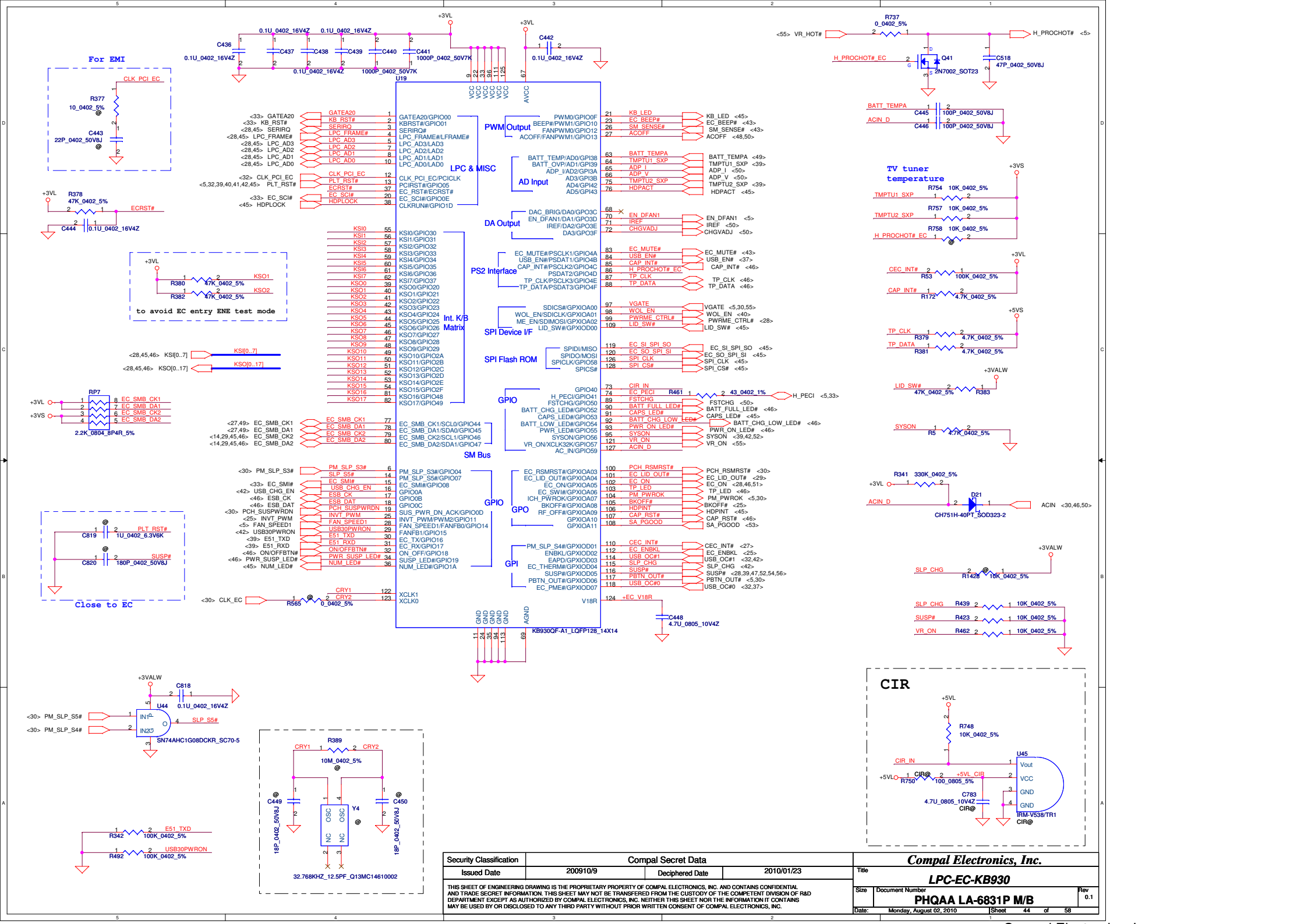

Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **LPC-EC-KB930**

Size	Document Number	Rev
	PHQAA LA-6831P M/B	0.1

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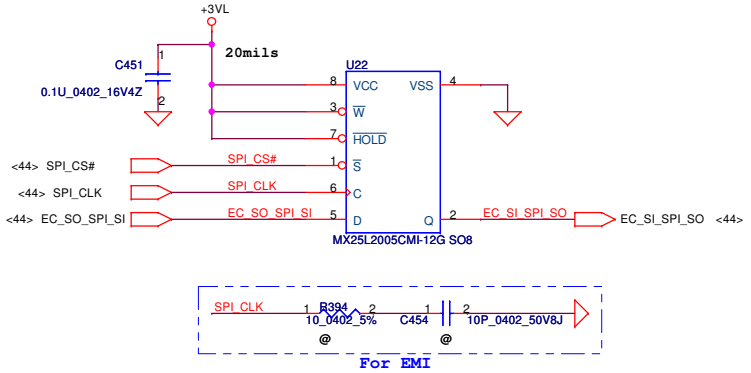
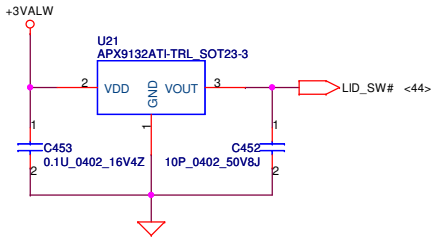
SPI Flash (256KB)

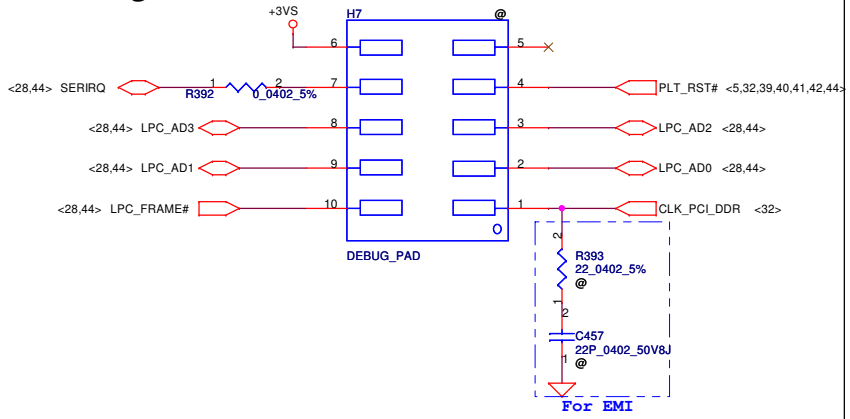


Lid SW

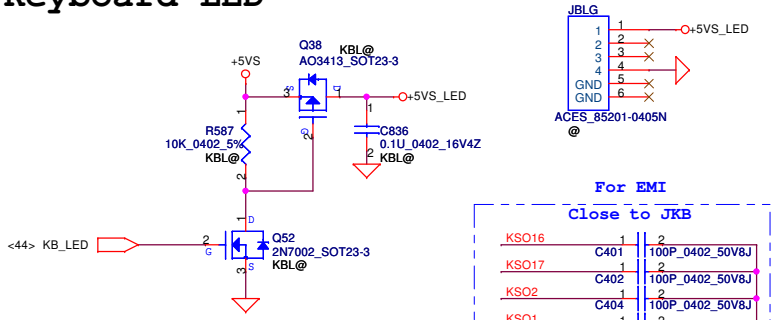


LPC Debug Port

Place the PAD under DDR DIMM.



Keyboard LED

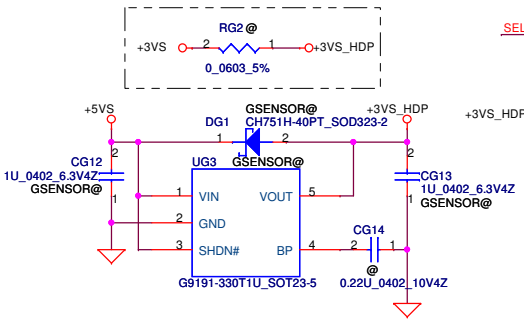


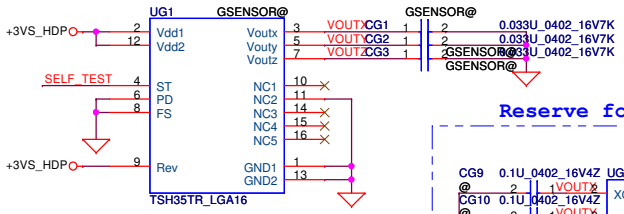
KEYBOARD CONN.

For EMI

Close to JKB

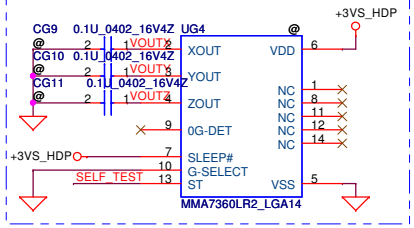
G-Sensor

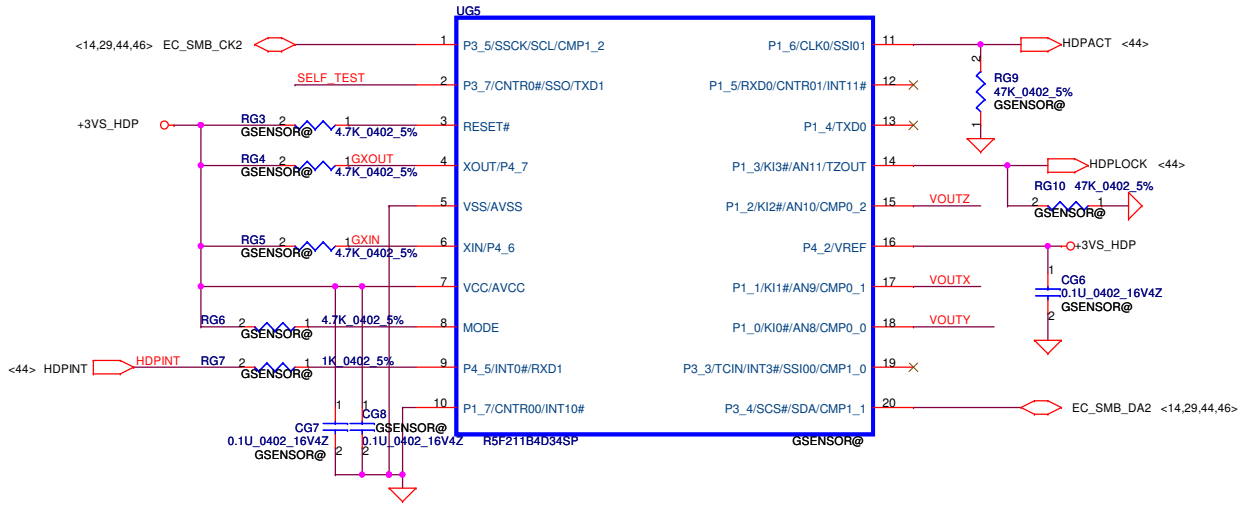




Place UG1 and UG4 on TOP Layer

Reserve for 2nd Source





Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: SPI ROM/LID/Debug/KB/G-Sen

Size	Document Number	Rev
	PHQAA LA-6831P M/B	0.1

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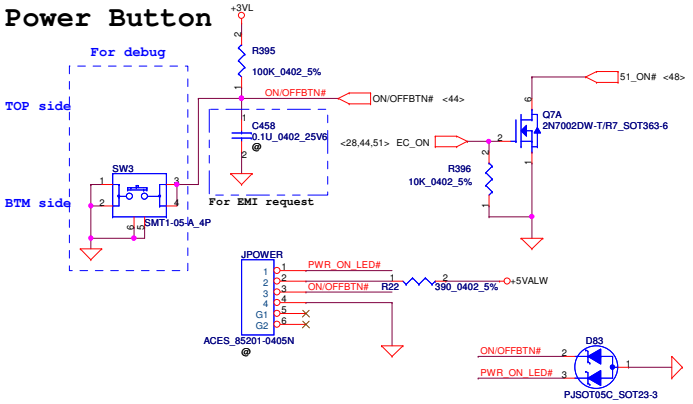
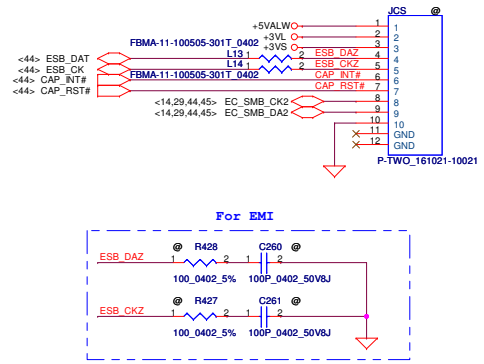
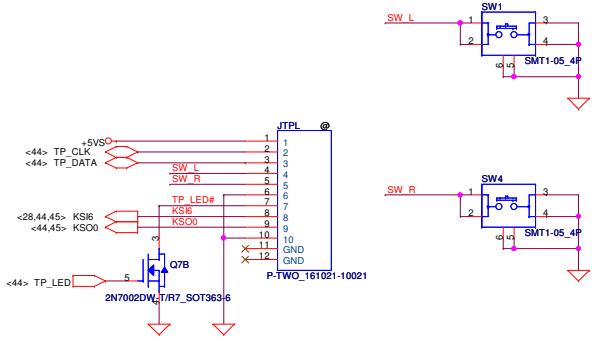
Power Button



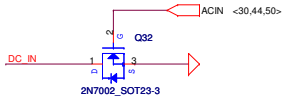
Caps Sensor/Light Sensor Conn.



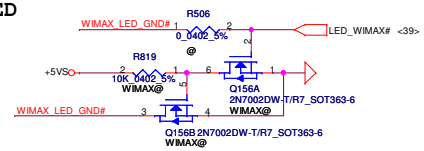
Touchpad & Light Pipe Connector



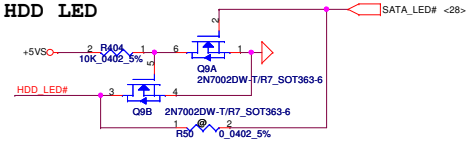
DC-IN LED



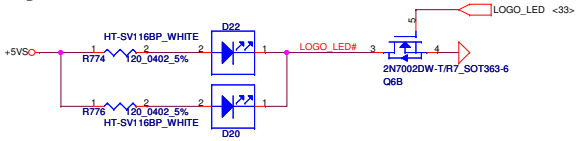
WiMAX LED



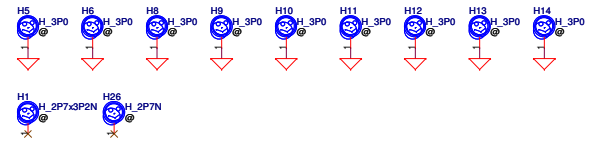
HDD LED



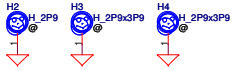
Logo LED



Screw Hole

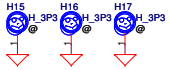


VGA



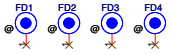
CPU

MINI CARD -- 3G

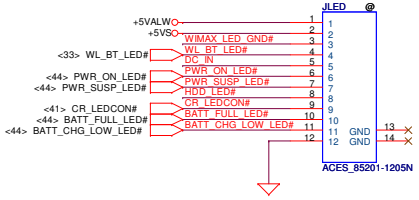


MINI CARD -- WLAN

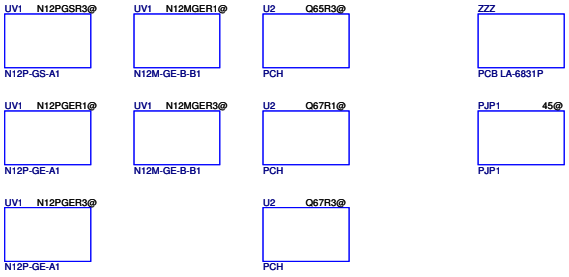
PCB Fedical Mark PAD



LED/B Connector



ISPD



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR/Cap./TP/LED/LP/LS/Screw

Size	Document Number	Rev
	PHQAA LA-6831P M/B	0.1

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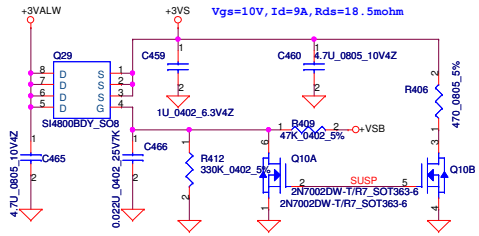
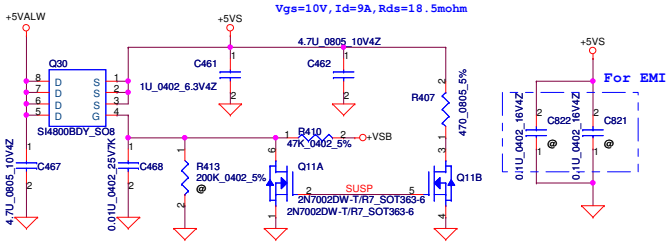
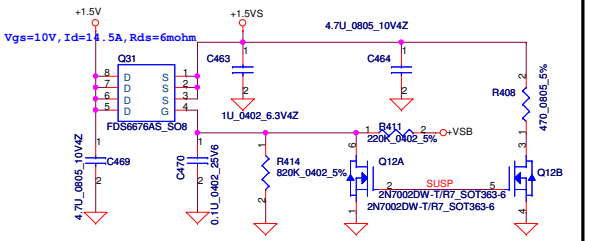
+3VALW TO +3VS

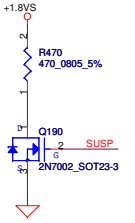


+5VALW TO +5VS

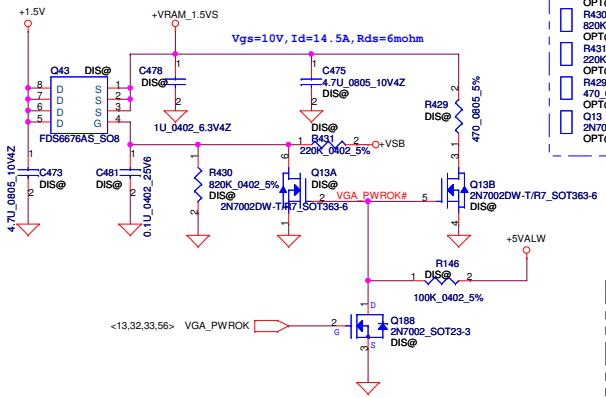


+1.5V to +1.5VS





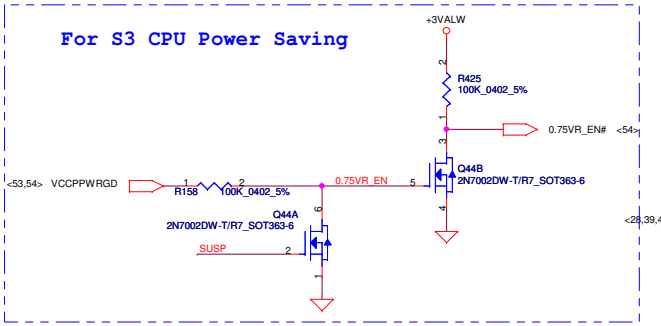
+1.5V to +VRAM_1.5VS

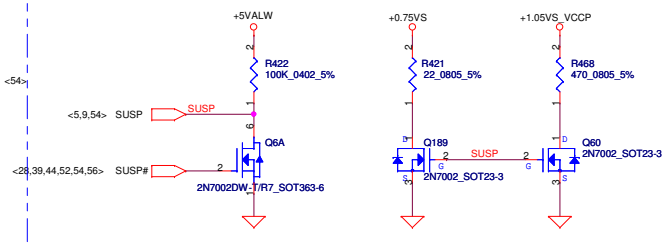


OPT@ parts:

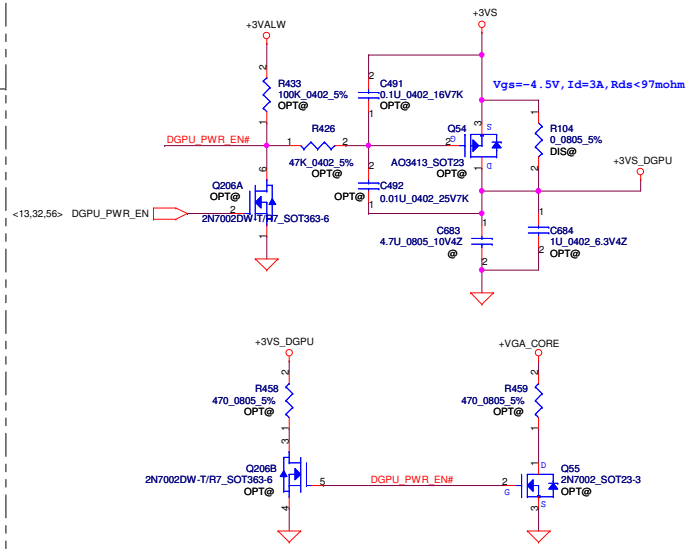
Q43	FDS6676AS_SO8	C473	4.7U_0805_10V4Z
C481	0.1U_0402_25V6	C478	1U_0402_6.3V4Z
R430	820K_0402_5%	C475	4.7U_0805_10V4Z
R431	220K_0402_5%	R146	100K_0402_5%
R429	470_0805_5%	Q188	2N7002_SOT23-3
Q13	2N7002DW-T/R7_SOT363-6		

For S3 CPU Power Saving

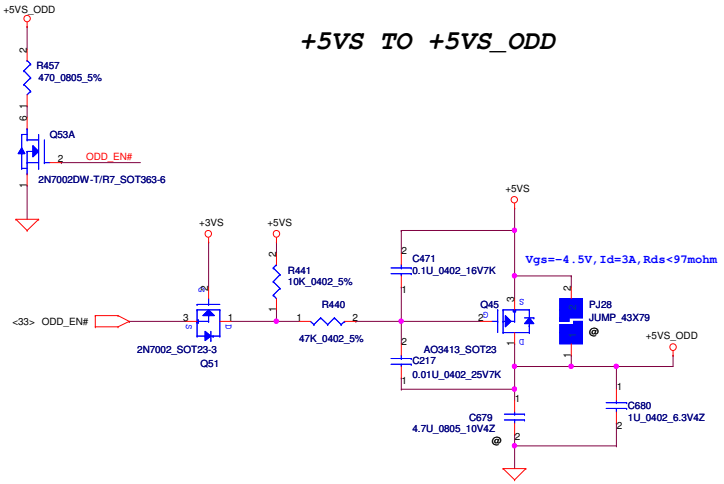




+3VS to +3VS_DGPU

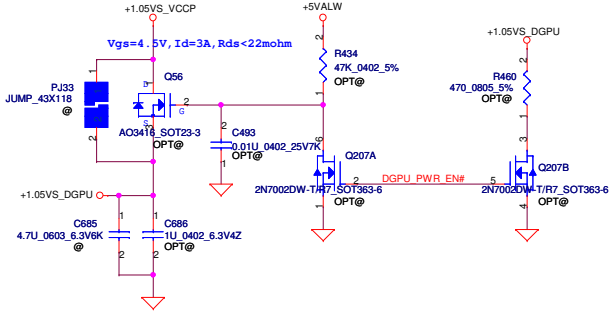


+5VS TO +5VS_ODD



+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs



Security Classification	Compal Secret Data		
Issued Date	200910/9	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DC-DC INTERFACE**

Size	Document Number	Rev
	PHQAA LA-6831P M/B	0.1

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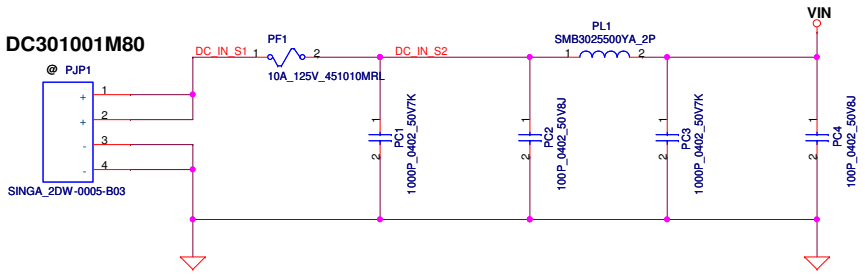
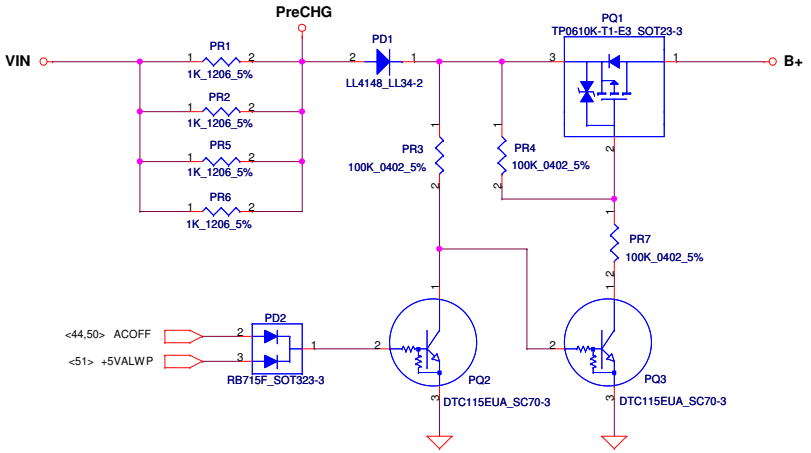
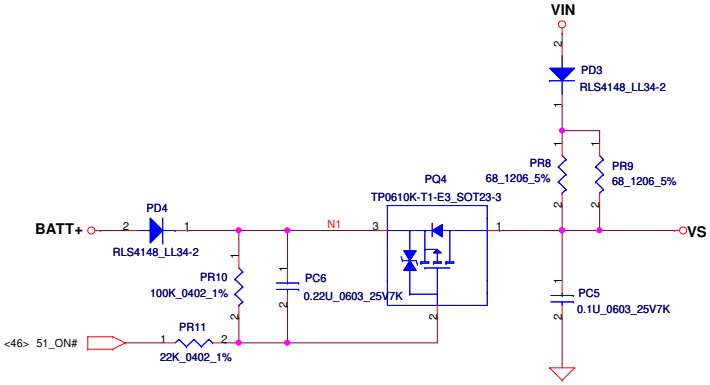
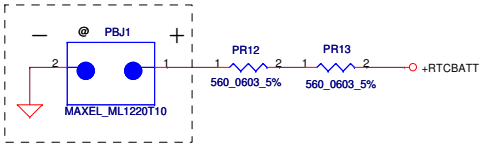






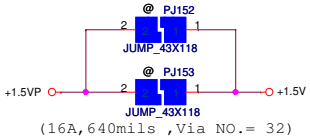
RTC Battery



SP093MX0000

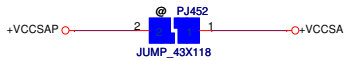
(5A,200mils ,Via NO.= 10)
OCP=8.6A

(1A,40mils ,Via NO.= 2)

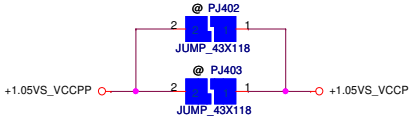


(16A,640mils ,Via NO.= 32)

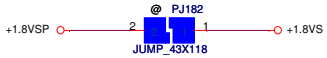
(5A,200mils ,Via NO.= 10)
OCP=7.9A



(6A,240mils ,Via NO.= 12)

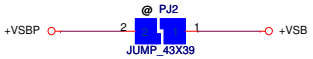


(17A,680mils ,Via NO.=34)

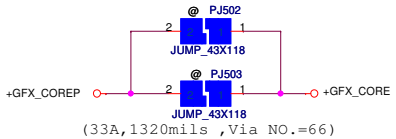


(1.65A,70mils ,Via NO.= 4)
OCP=4.2A

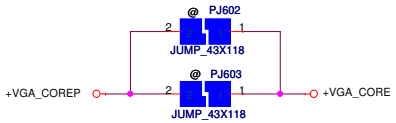
(100mA,40mils ,Via NO.= 2)



(120mA,40mils ,Via NO.= 1)



(33A,1320mils ,Via NO.=66)
OCP=40A



(30A,1200mils ,Via NO.=60)

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

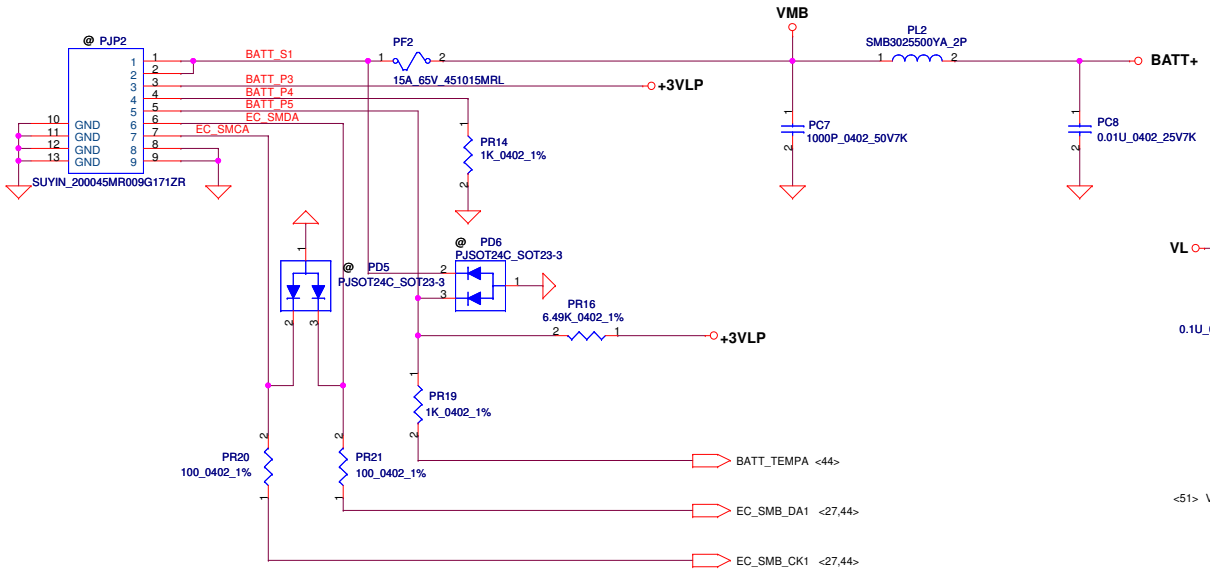
Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: ***DCIN/VIN DECTOR***

Size | Document Number: NHQAA LA-6831P M/B | Rev: 0.1

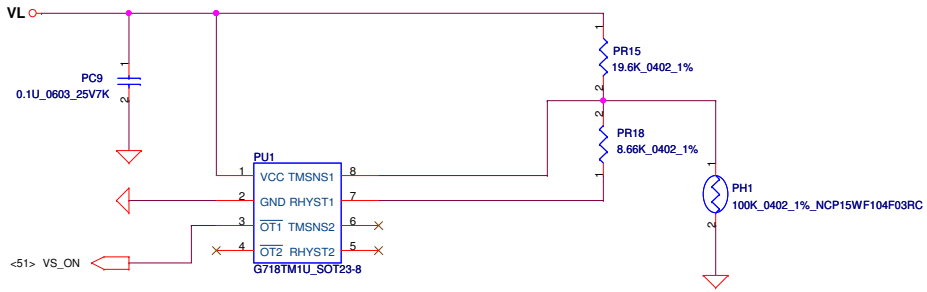
Date: Monday, August 02, 2010 | Sheet 48 of 58

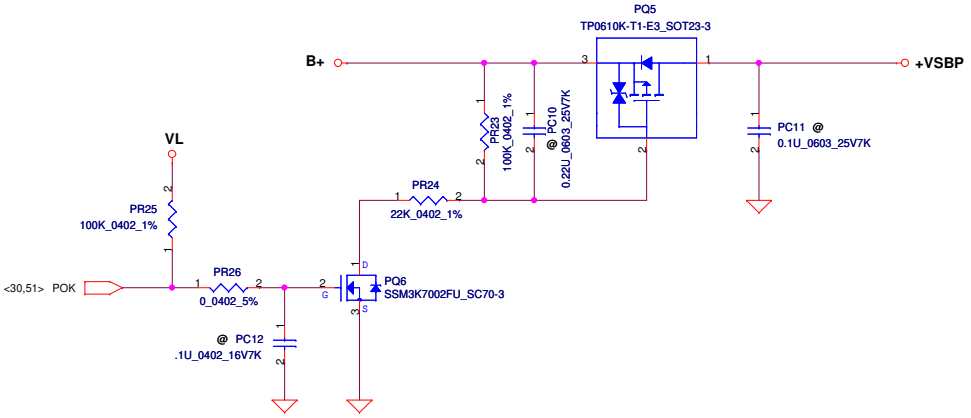


PH1 under CPU botten side :

CPU thermal protection at 95 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size	Document Number	Rev
	NHQAA LA-6831P M/B	0.1

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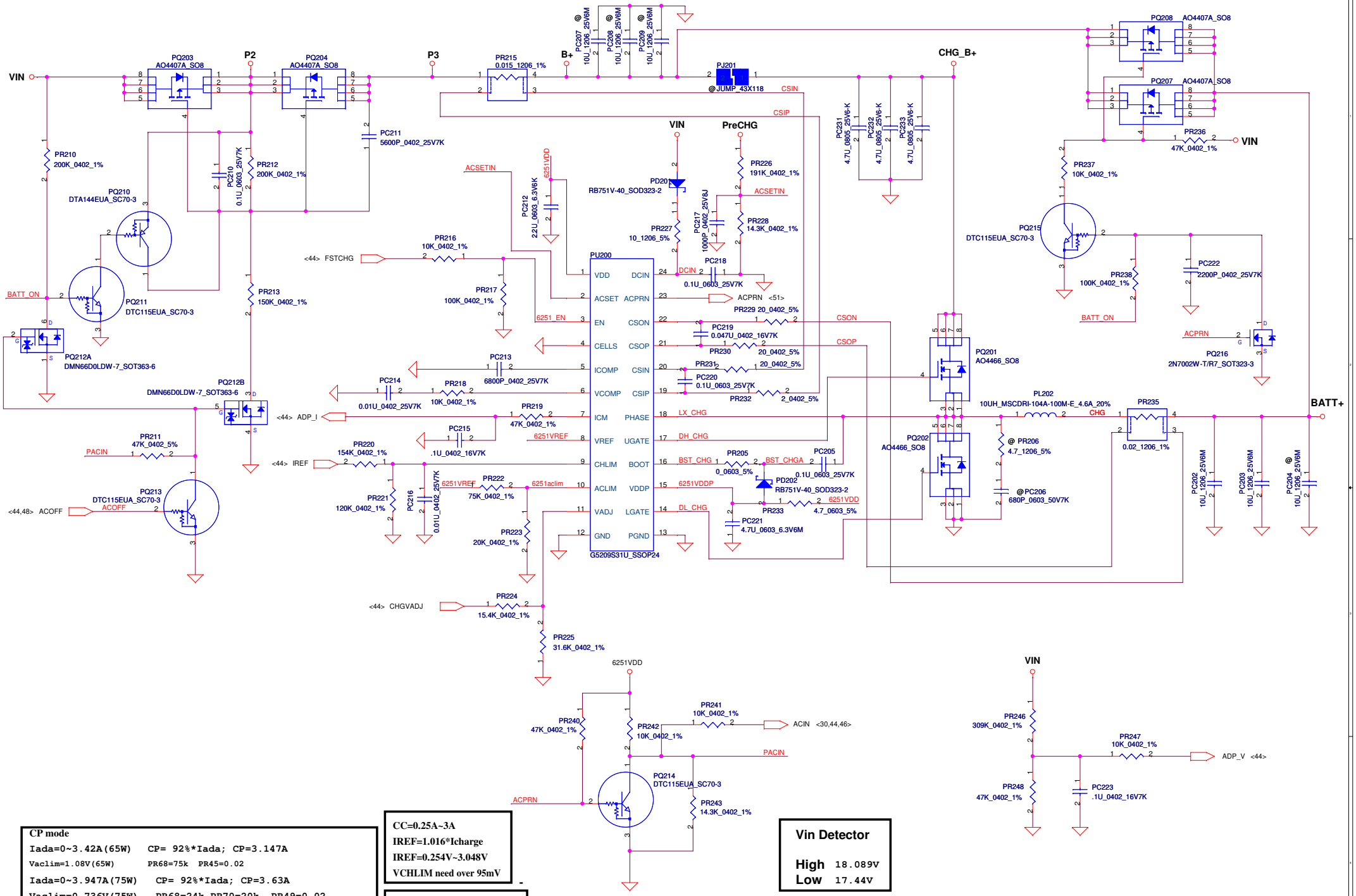

CP mode

```
Iada=0~3.42A(65W)   CP= 92%*Iada; CP=3.147A
Vaclim=1.08V(65W)   PR68=75k  PR45=0.02
Iada=0~3.947A(75W)   CP= 92%*Iada; CP=3.63A
Vaclim=0.736V(75W)   PR68=24k PR70=20k  PR49=0.02
Iada=0~4.737A(90W)   CP= 92%*Iada; CP=4.36A
Vaclim=0.736V(90W)   PR68=53.6k PR70=20k  PR49=0.015
Iada=0~6.316A(120W)  CP= 92%*Iada; CP=5.81A
Vaclim=0.736V(120W)  PR68=8.25k PR70=26.7k  PR49=0.015
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector

High 18.089V
Low 17.44V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
Custom	NHQAA LA-6831P M/B	0.1

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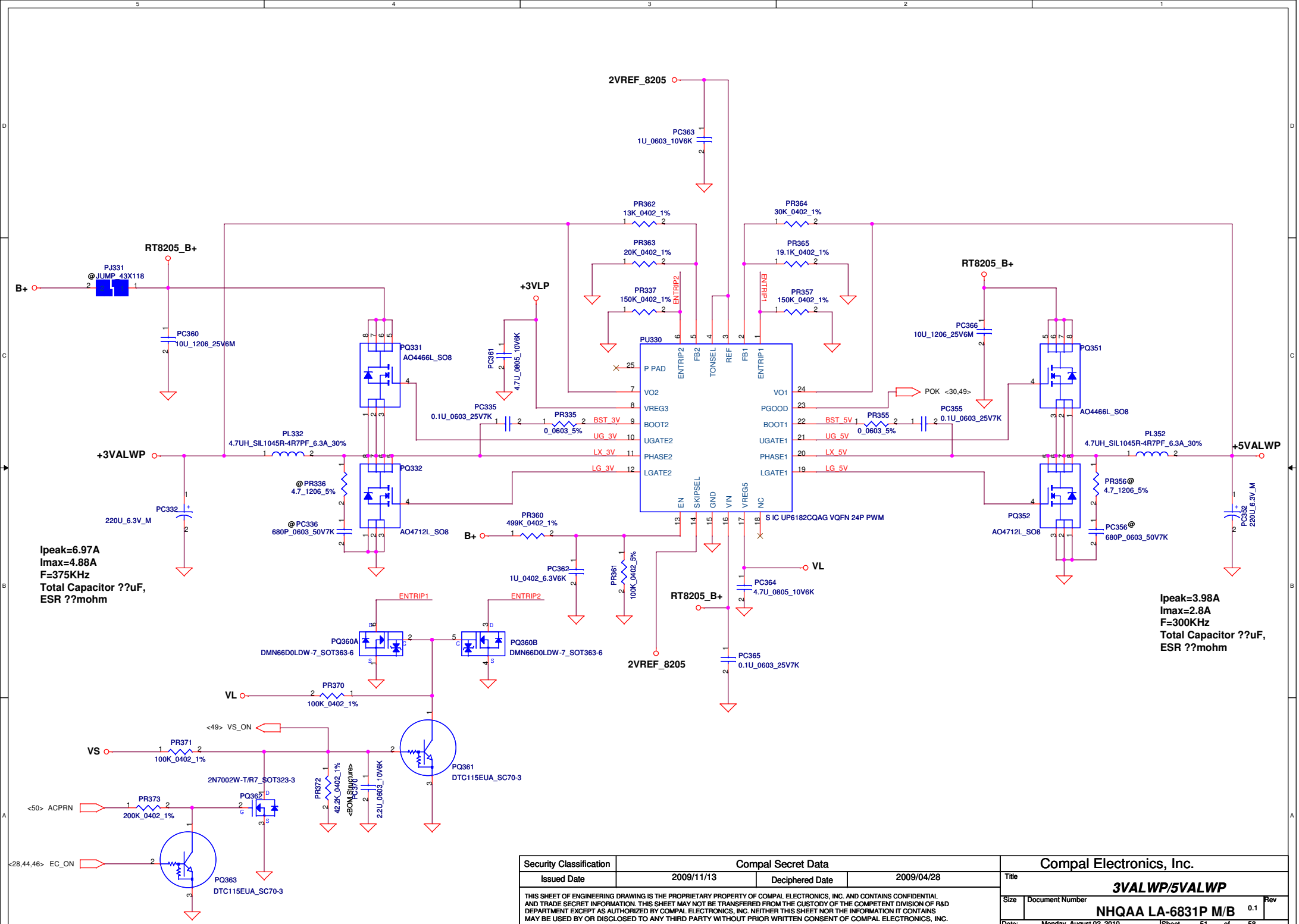

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: *3VALWP/5VALWP*

Size	Document Number	Rev
	NHQAA LA-6831P M/B	0.1

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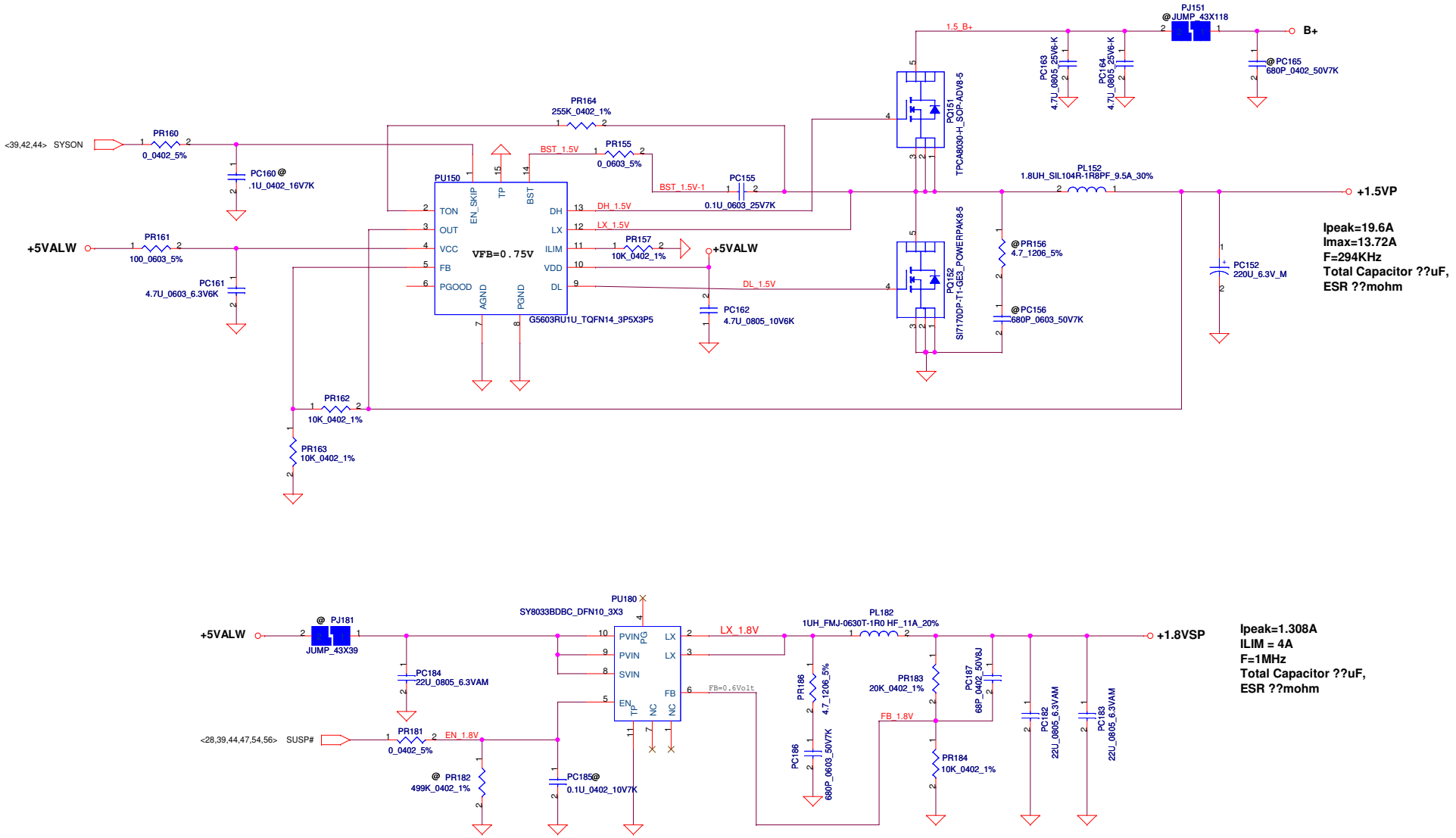


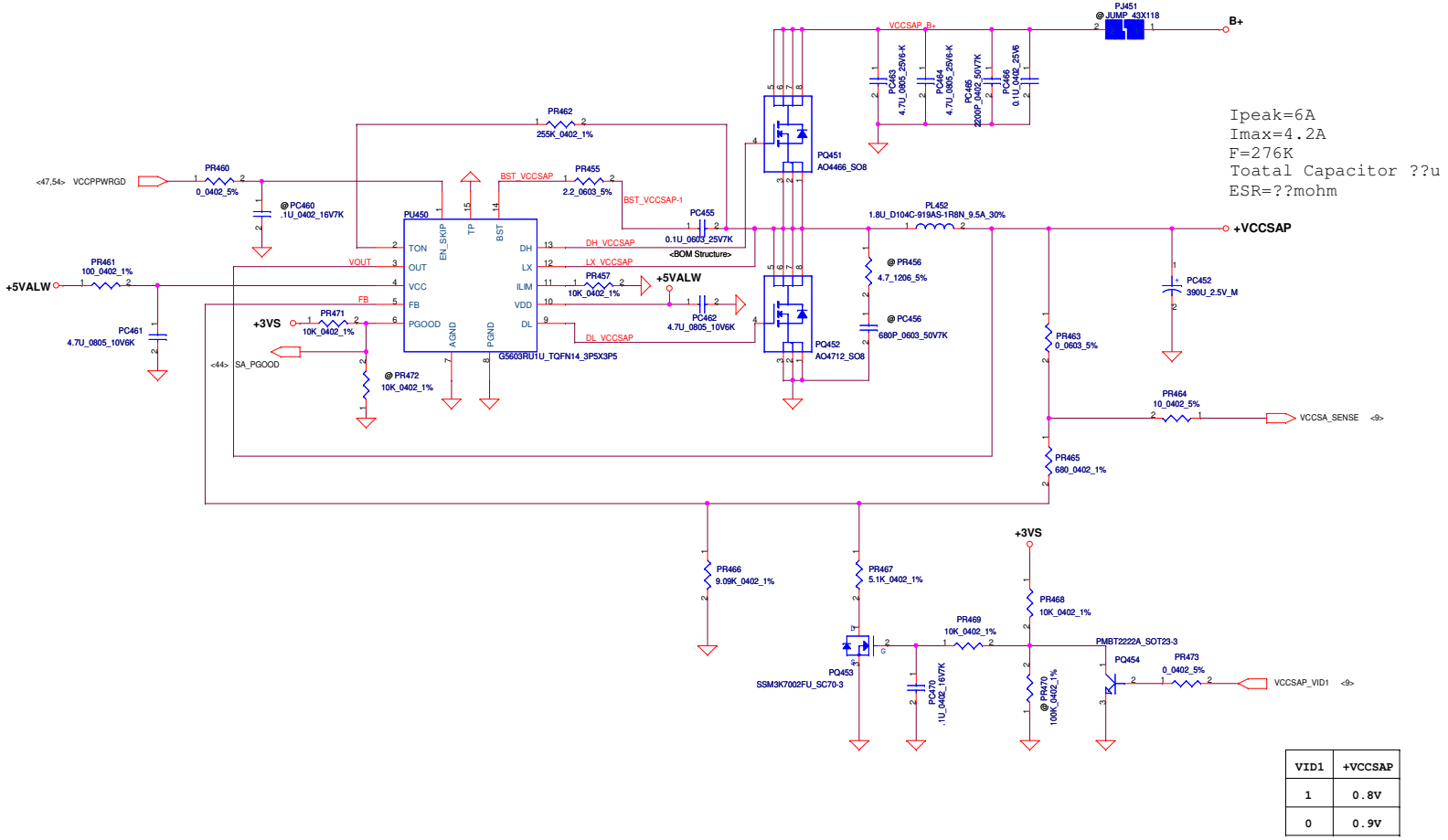
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: ***+1.5VP/+1.8VSP***

Size	Document Number	Rev
Custom	NHQAA LA-6831P M/B	0.1

Date: Monday, August 02, 2010 | Sheet 52 of 58



VID1	+VCCSAP
1	0.8V
0	0.9V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: *+VCCSAP/+1.0VSDGPUP*

Size	Document Number	Rev
C	NHQAA LA-6831P M/B	0.1

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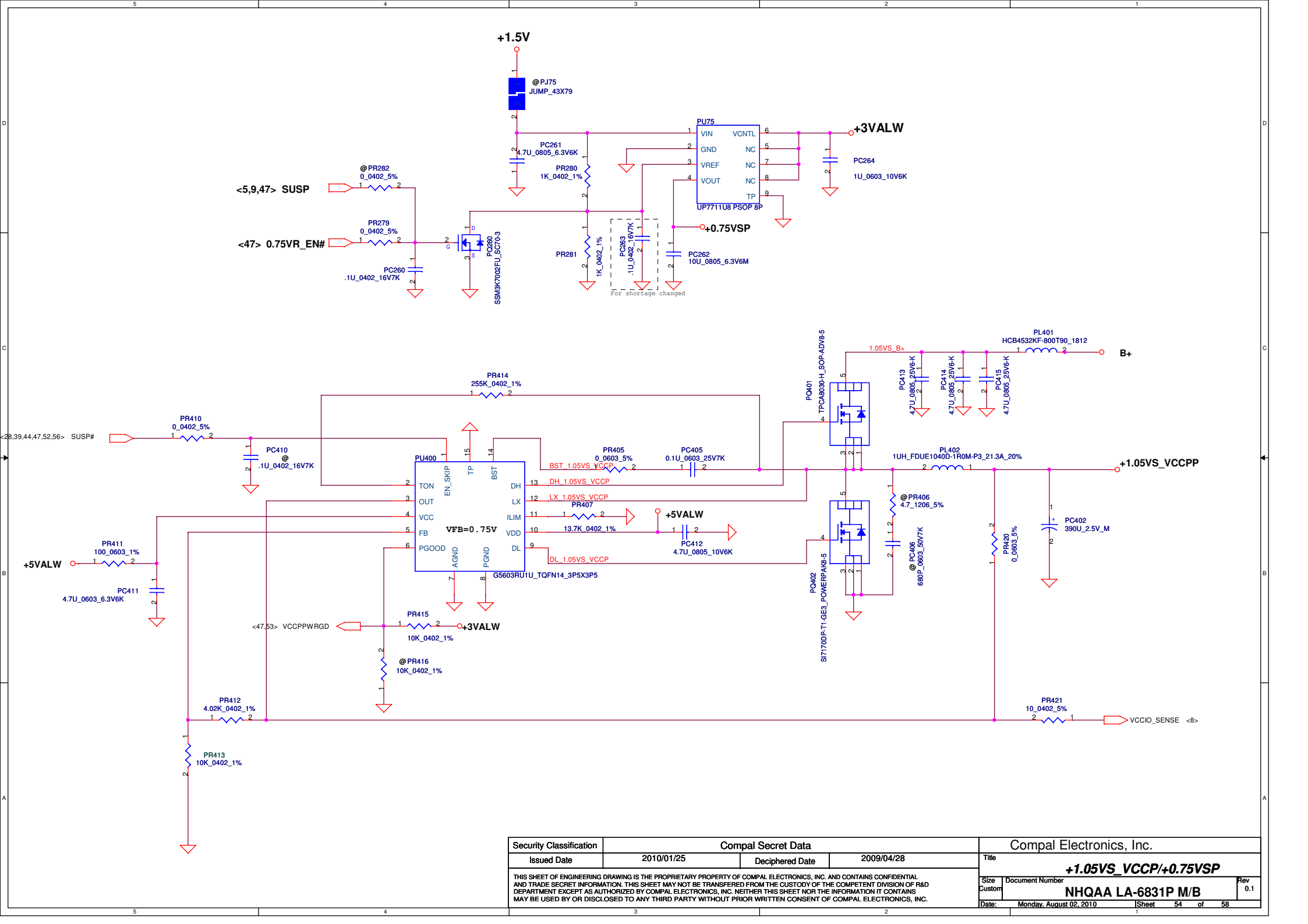
+1.5V
@PJ75
JUMP_43X79
PU75
VIN
GND
VREF
VOUT
VCNTL
NC
TP
UP7711U8 PSOP 8P
+3VALW
PC261
4.7U_0805_6.3V6K
PR280
1K_0402_1%
PC264
1U_0603_10V6K
@PR282
0_0402_5%
<5,9,47> SUSP
PR279
0_0402_5%
<47> 0.75VR_EN#
PC260
.1U_0402_16V7K
PQ260
SSM3K7002FU_SC70-3
PR281
1K_0402_1%
PC263
.1U_0402_16V7K
For shortage changed
PC262
10U_0805_6.3V6M
+0.75VSP
PL401
HCB4532KF-800T90_1812
1.05VS_B+
B+
PQ401
TPCA8030-H_SOP-ADV8-5
PC413
4.7U_0805_25V6-K
PC414
4.7U_0805_25V6-K
PC415
4.7U_0805_25V6-K
PR414
255K_0402_1%
PR410
0_0402_5%
<28,39,44,47,52,56> SUSP#
PC410
@
.1U_0402_16V7K
PU400
TON
OUT
VCC
FB
PGOOD
EN_SKIP
TP
BST
DH
LX
ILIM
VDD
DL
AGND
PGND
VFB=0.75V
G5603RU1U_TQFN14_3P5X3P5
PR405
0_0603_5%
BST_1.05VS_VCCP
DH_1.05VS_VCCP
LX_1.05VS_VCCP
PR407
13.7K_0402_1%
DL_1.05VS_VCCP
PC405
0.1U_0603_25V7K
PL402
1UH_FDUE1040D-1R0M-P3_21.3A_20%
+1.05VS_VCCPP
@PR406
4.7_1206_5%
@PC406
680P_0603_50V7K
PR420
0_0603_5%
PC402
390U_2.5V_M
PQ402
SI7170DP-T1-GE3_POWERPAK8-5
+5VALW
PC412
4.7U_0805_10V6K
PR411
100_0603_1%
PC411
4.7U_0603_6.3V6K
<47,53> VCCPPWRGD
PR415
10K_0402_1%
@PR416
10K_0402_1%
PR412
4.02K_0402_1%
PR413
10K_0402_1%
PR421
10_0402_5%
VCCIO_SENSE <8>
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2009/04/28
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Title
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Custom
Document Number
NHQAA LA-6831P M/B
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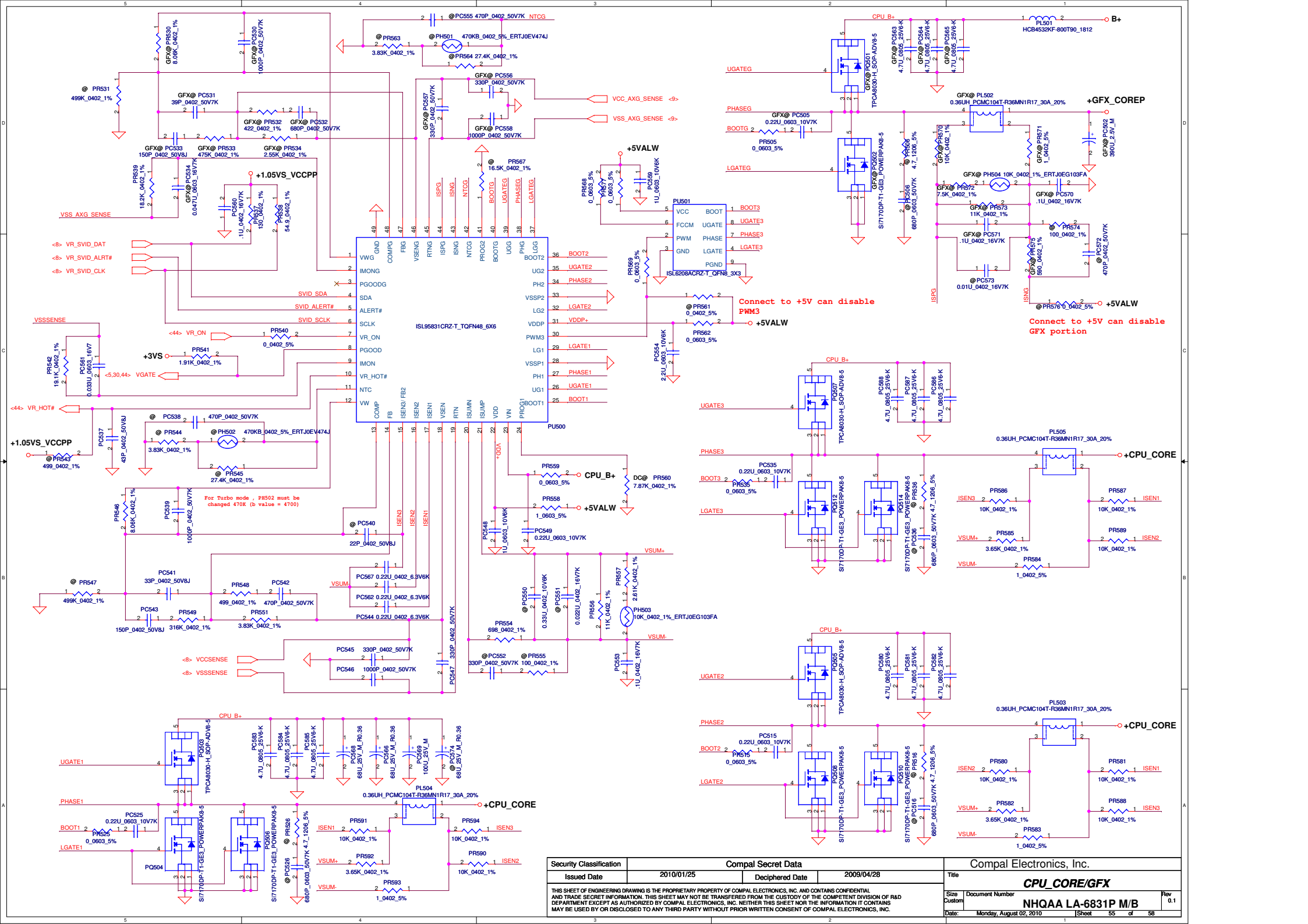


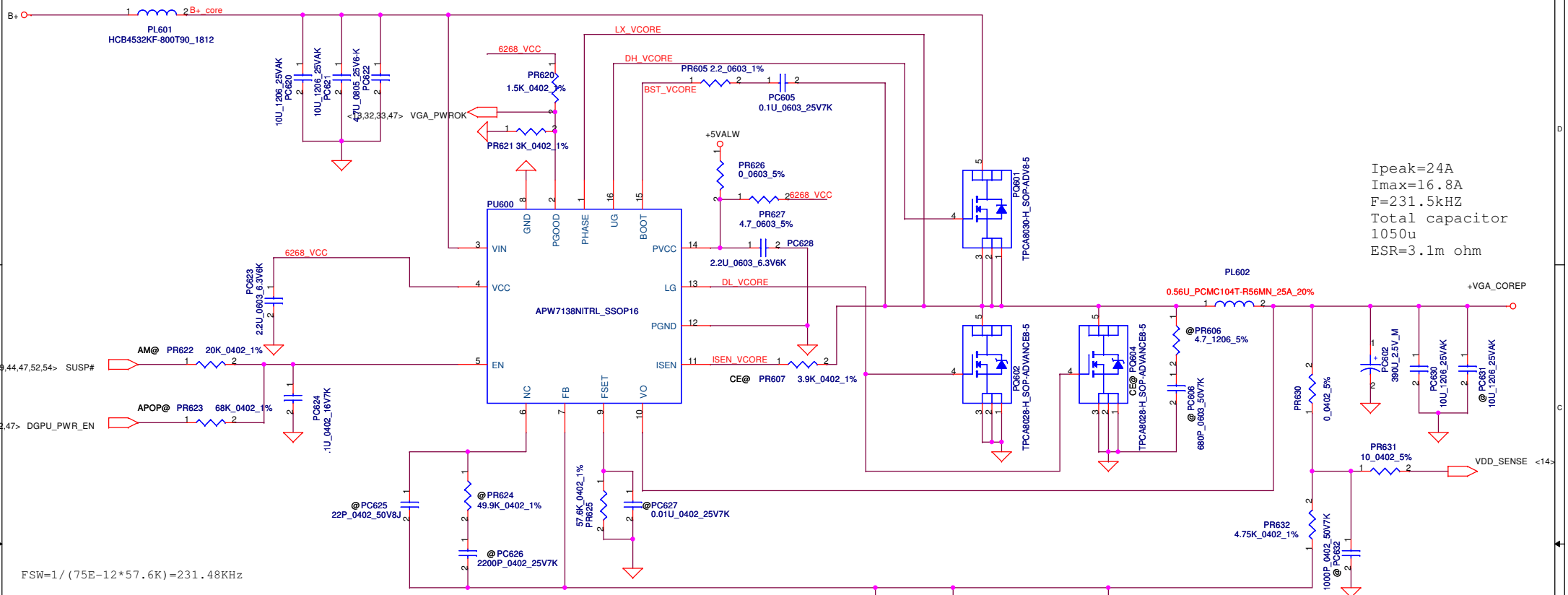
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: **CPU_CORE/GFX**

Size	Document Number	Rev
Custom	NHQAA LA-6831P M/B	0.1

Date: Monday, August 02, 2010 | Sheet 55 of 58



N11M-GE1/GE2	N11P-GE1/GE2	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=32.14A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

GPU_VID0	GPU_VID1	N11M-GE1	N11M-GE2	N11P-GE1	N11P-GE2	N11E-GE1-LP
0	0			0.80V	0.80V	0.80V
1	0	0.85V	0.85V	0.85V	0.85V	0.85V
0	1					
1	1	1.03V	1V	0.95V	0.925V	0.9V
		PR260=4.75K PR262=14K PR261=56.2K PR263=16.2K	PR260=4.75K PR262=14K PR261=56.2K PR263=19.6K	PR260=4.75K PR262=14K PR261=56.2K PR263=29.4K	PR260=4.75K PR262=14K PR261=56.2K PR263=40.2K	PR260=4.75K PR262=14K PR261=56.2K PR263=63.4K

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: NHQAA LA-6831P M/B | Rev: 1.0

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HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

Compal Electronics, Inc.		
Title: *HW-PIR*		
Size: Custom	Document Number: NHQAA LA-6831P M/B	Rev: 0.1
Date: Monday, August 02, 2010	Sheet 57 of 57	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: ***Power PIR***

Size	Document Number	Rev
	NHQAA LA-6831P M/B	0.1