

Compal Confidential

VIWZ1/VIWZ2 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13P

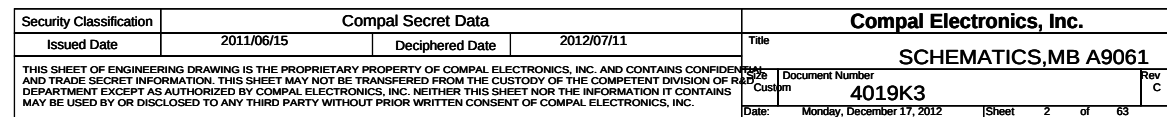
2012-11-10

LA-9061P

REV:2.A

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VIWZ2
LS9061P PWR/B
LS9062P USB/B
LS9063P ODD/B
LS9064P LED/B



Voltage Rails

State	power plane			
				+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403	1001_101xb
USB Charger	1010 111X b		

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
0	0	0 V	0 V	0 V	Z-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	Z-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	Z-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	Z-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Reserved	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Reserved	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Reserved	PVT
7	NC	2.500 V	3.300 V	3.300 V	Reserved	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	Touch Screen
		2	Blue Tooth
		3	Camera
EHCI1	UHCI2	4	
		5	
		6	
		7	
EHCI2	UHCI4	8	USB Port (Right Side USB-BD)
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GS&GL	N13P@
OPTIMUS part	OPT@
Integrate Graphic part	UMA@
GPU:N13P-GS&GSR	GS@
GPU:N13P-GL&GLR	GL@
GPU:N13P-GS Strap	GS1@
GPU:N13P-GL Strap	GL1@
GPU:N13P-GSR Strap	GSR@
GPU:N13P-GLR Strap	GLR@
OPTIMUS no support GCLK	OPTNOGCLK@
OPTIMUS support GCLK	OPTGCLK@
Support Green CLK	GCLK@
not Support Green CLK	NOGCLK@
Support Green CLK 244	GCLK244@
Support Green CLK 304	GCLK304@
Cardreader	CR@
Support HP Woofer	woofer@
Gastube	Gastube@
EC RESET function	RESET@
HDMI	HDMI@
BlueTooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8105@
GIGA LAN	GIGA@
Deep Sleep S3	DS3@
Not Support Deep Sleep S3	NODS3@
ISCT	AOAC@
ISCT not support	NOAOAC@
Camera	CMOS@
For Z490 (14")	14@
For Z590 (15")	15@
Unpop	@
USB Charger	CHG@
not USBCharger	NOCHG@
Keyboard Back Light	KBL@
Touch Screen	TS@
HM76 by PCH	HM76@
HM70 by PCH	HM70@
Cardreader RTS5178	RTS5178@
Cardreader RTS5170	RTS5170@
for 14" Touch Screen	TS_14@
for 15" Touch Screen	TS_15@

GPU BOM Structure Table

BOM Structure	N13P-GS	N13P-GL	N13P-GSR	N13P-GLR
OPT@	V	V	V	V
OPTNOGCLK@	V	V	V	V
N13P@	V	V	V	V
GS@	V		V	
GL@		V		V
GS1@	V			
GL1@		V		
GSR@			V	
GLR@				V

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	TP
SMB_EC_CK1		X	V	X	X	X	X	X	X
SMB_EC_DA1	KB9012 +3VALW	X	+3VALW	X	X	X	X	X	X
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	X
SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	+3VS	X
SMBCLK	PCH	X	X	X	+3VS	+3VS	X	X	+3VS
SMBDATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK	PCH	V	X	V	X	X	V	X	X
SML1DATA	PCH +3VALW	+3VS	X	+3VS	X	X	+3VS	X	X

Hot plug detect for IFP link C

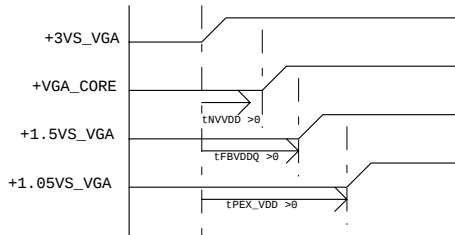
VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

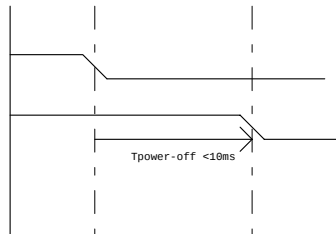
Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V



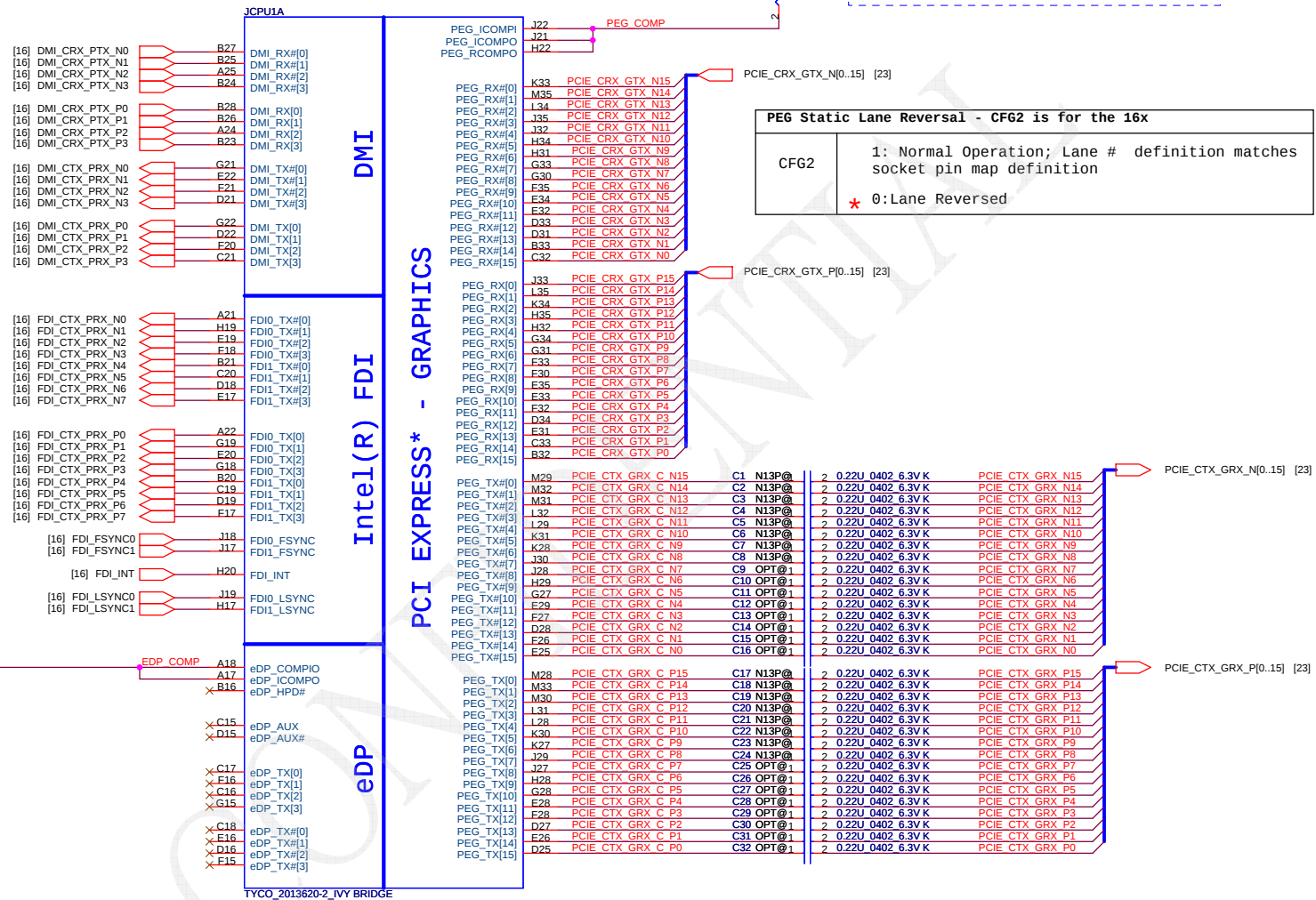
- all power rail ramp up time should be larger than 40us
- Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



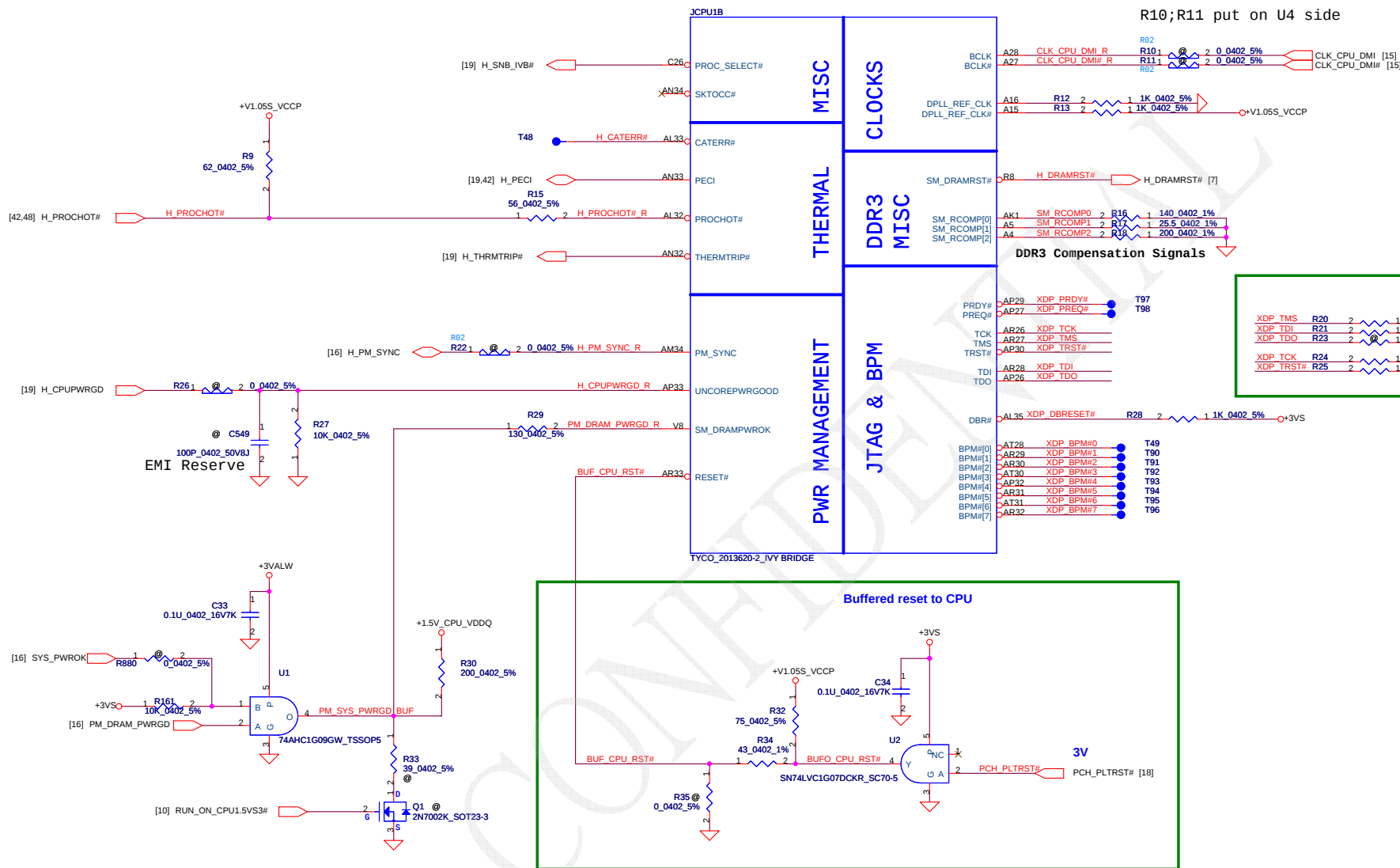
- all GPU power rails should be turned off within 10ms

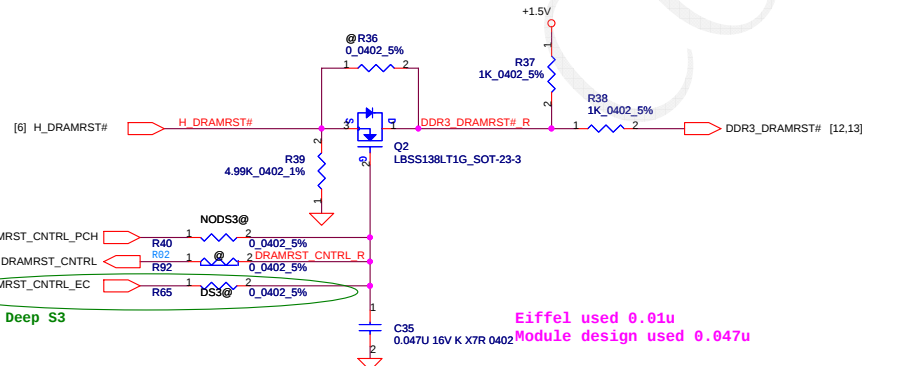
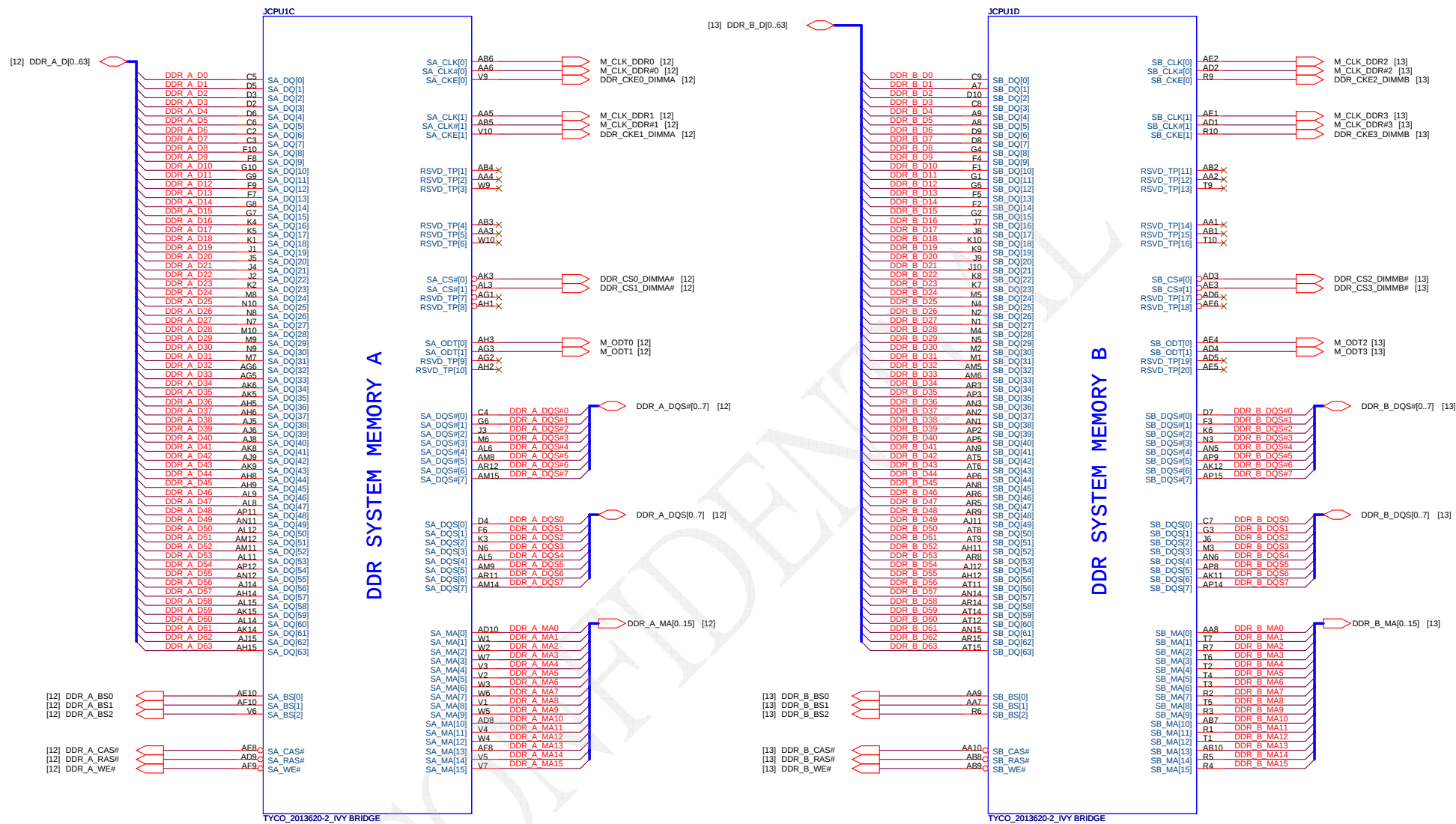
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eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



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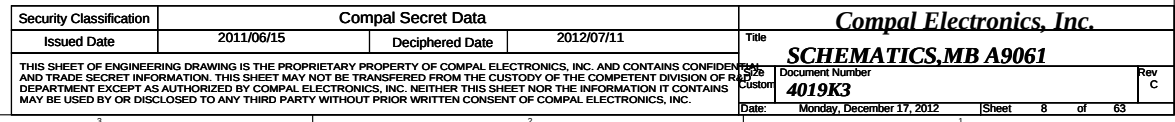
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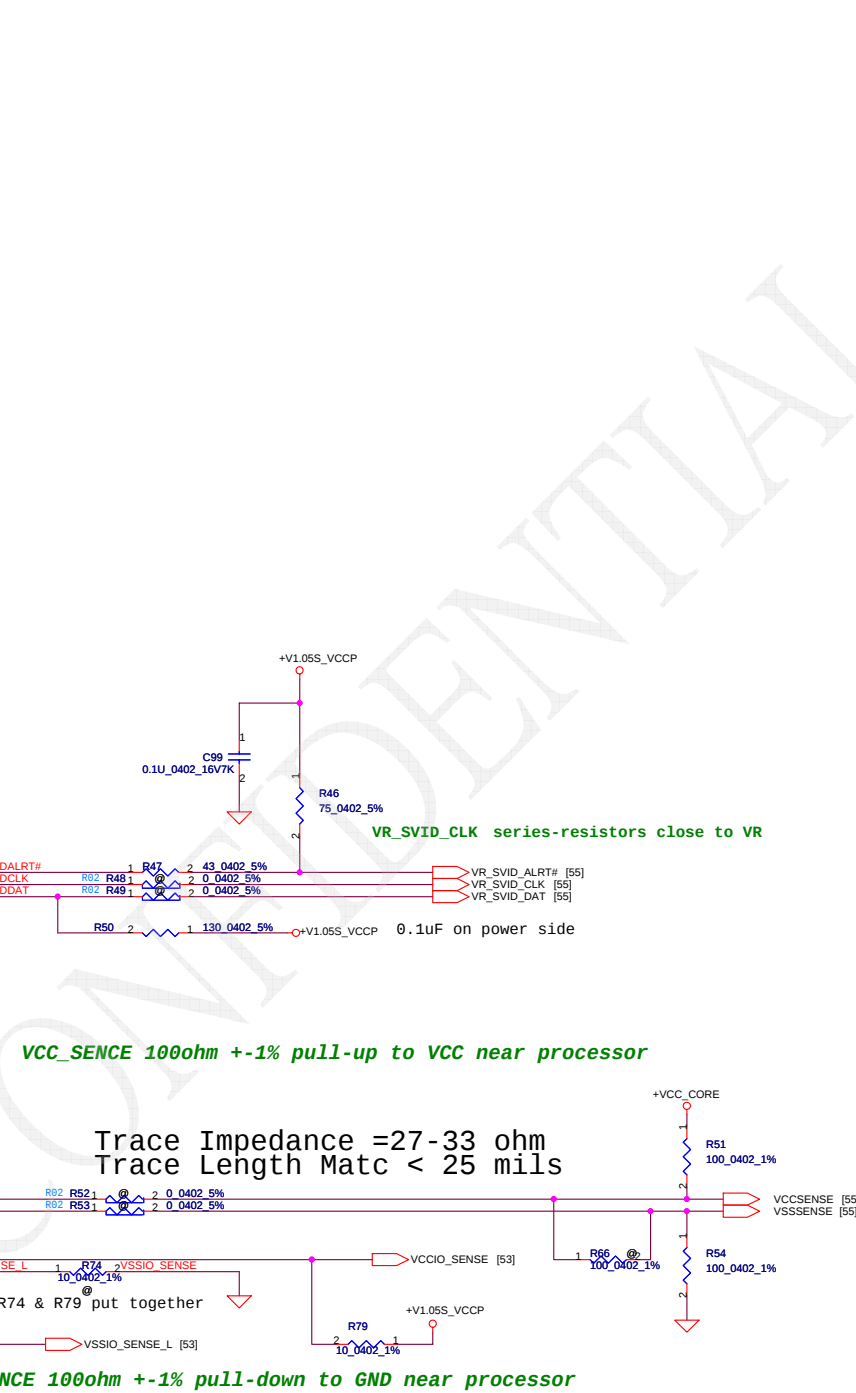
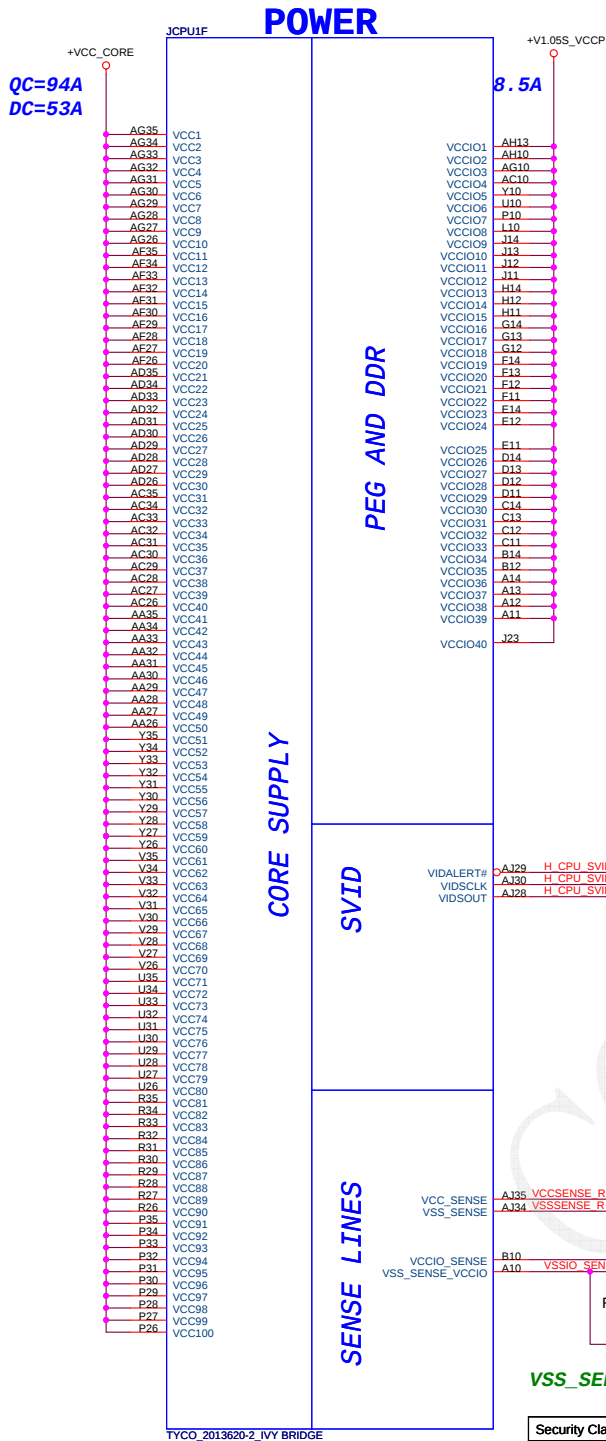
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

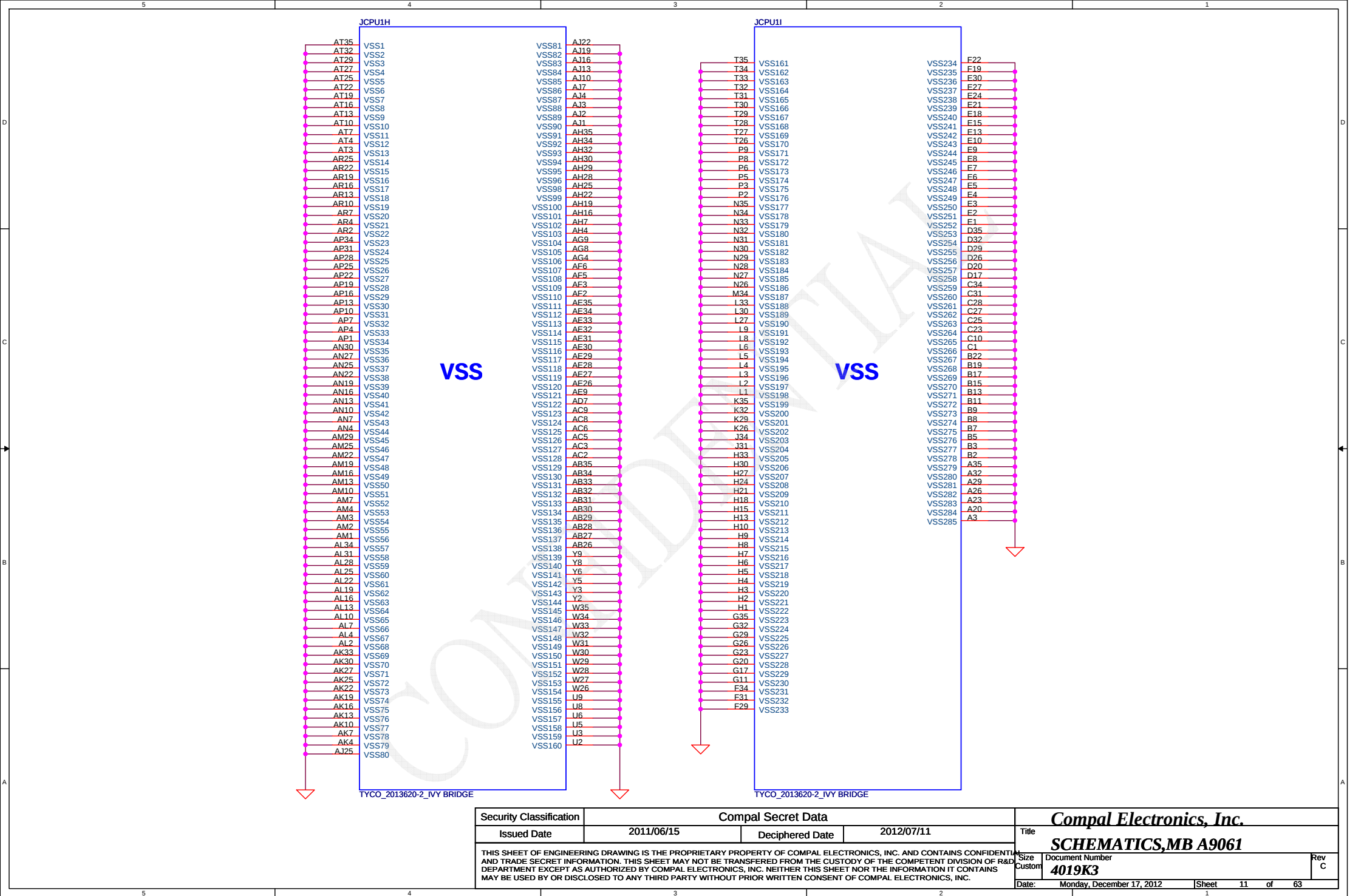
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESE de assertion 0: PEG Wait for BIOS for training

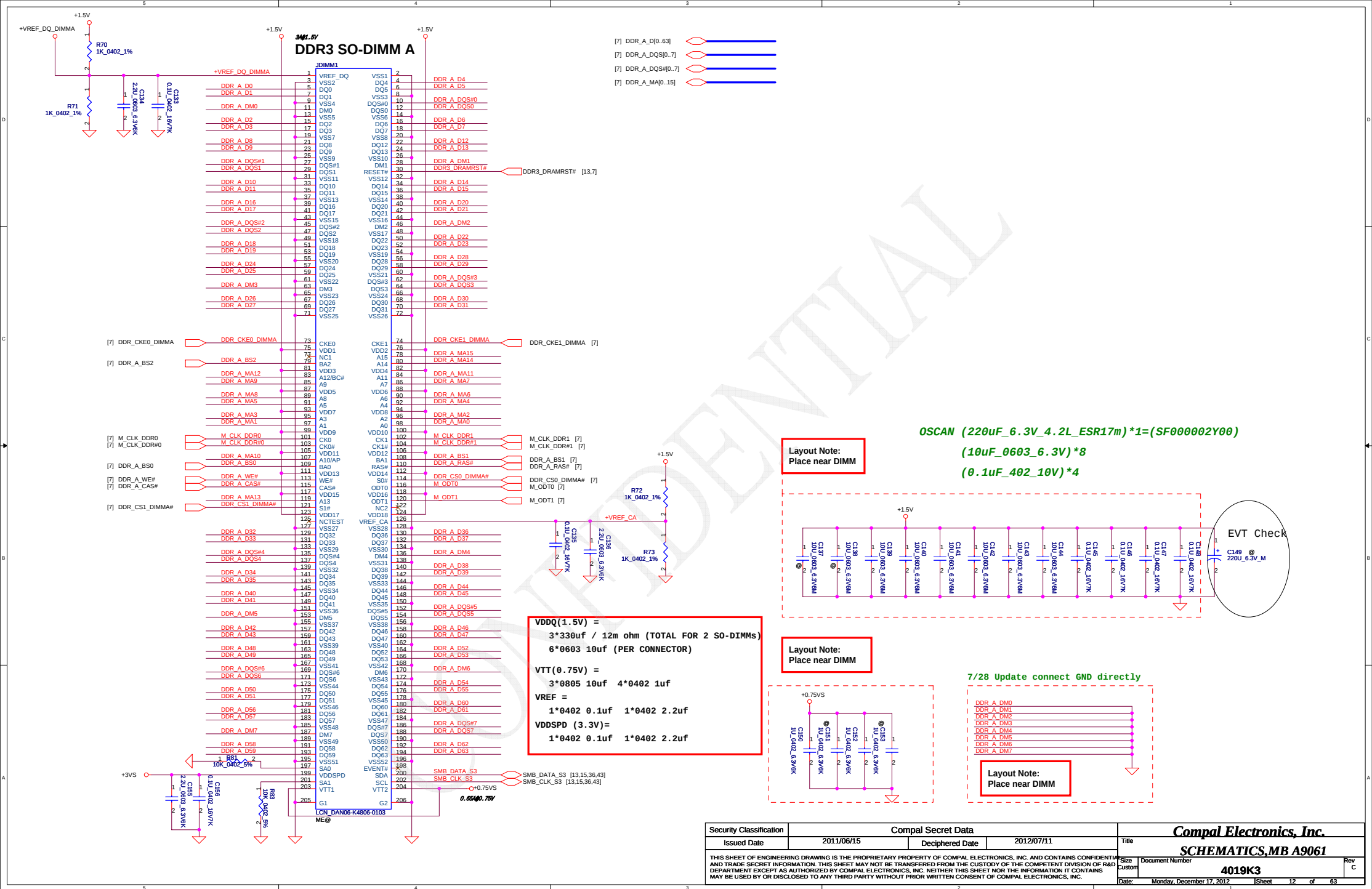


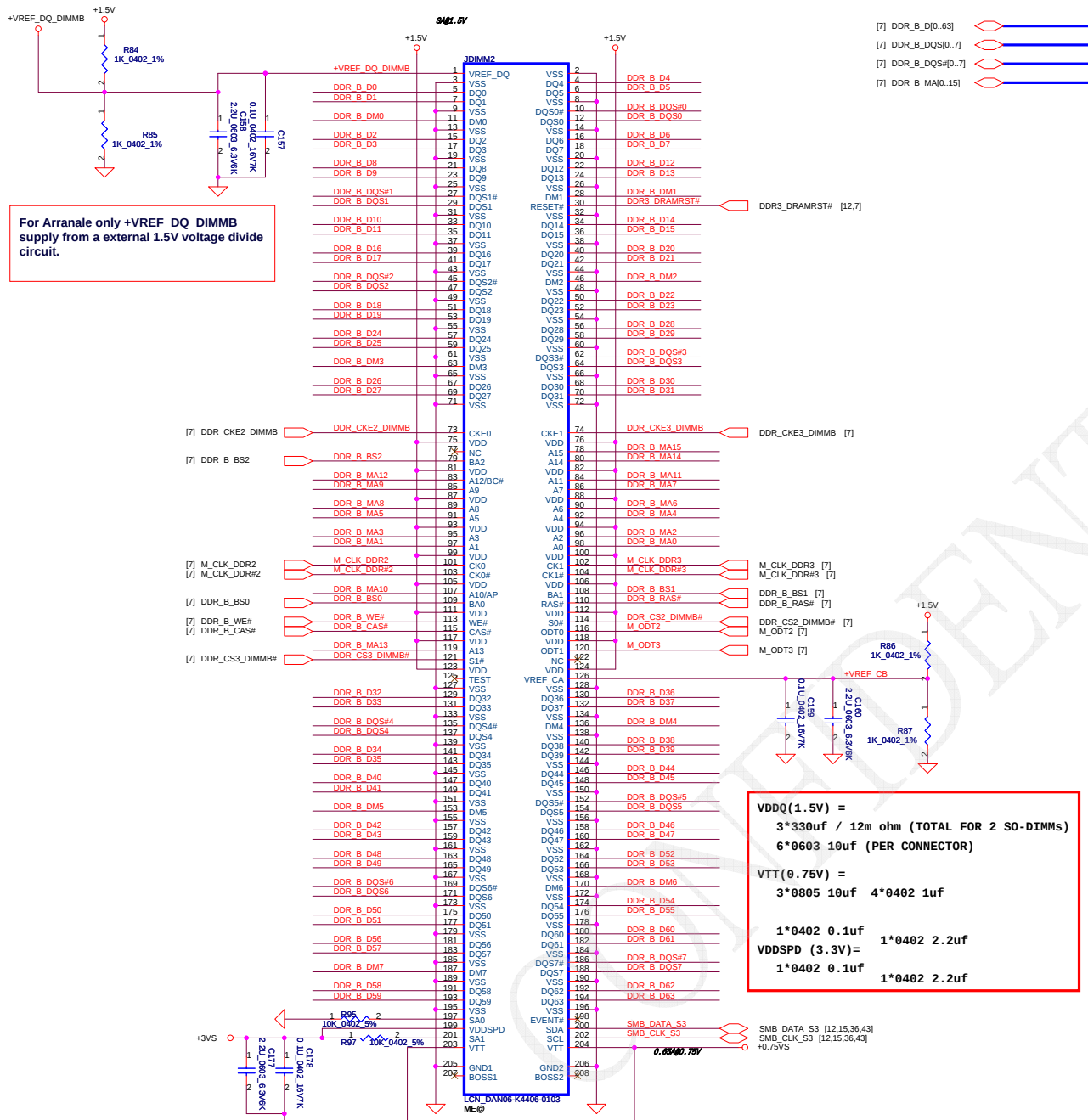


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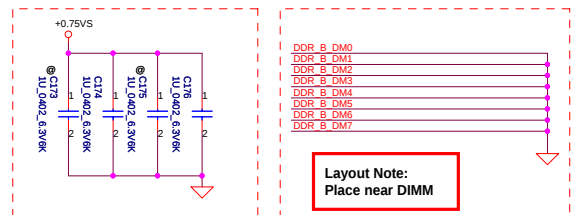
For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

- [7] DDR_B_D[0..63]
- [7] DDR_B_DQS[0..7]
- [7] DDR_B_DQS# [0..7]
- [7] DDR_B_MA[0..15]

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM



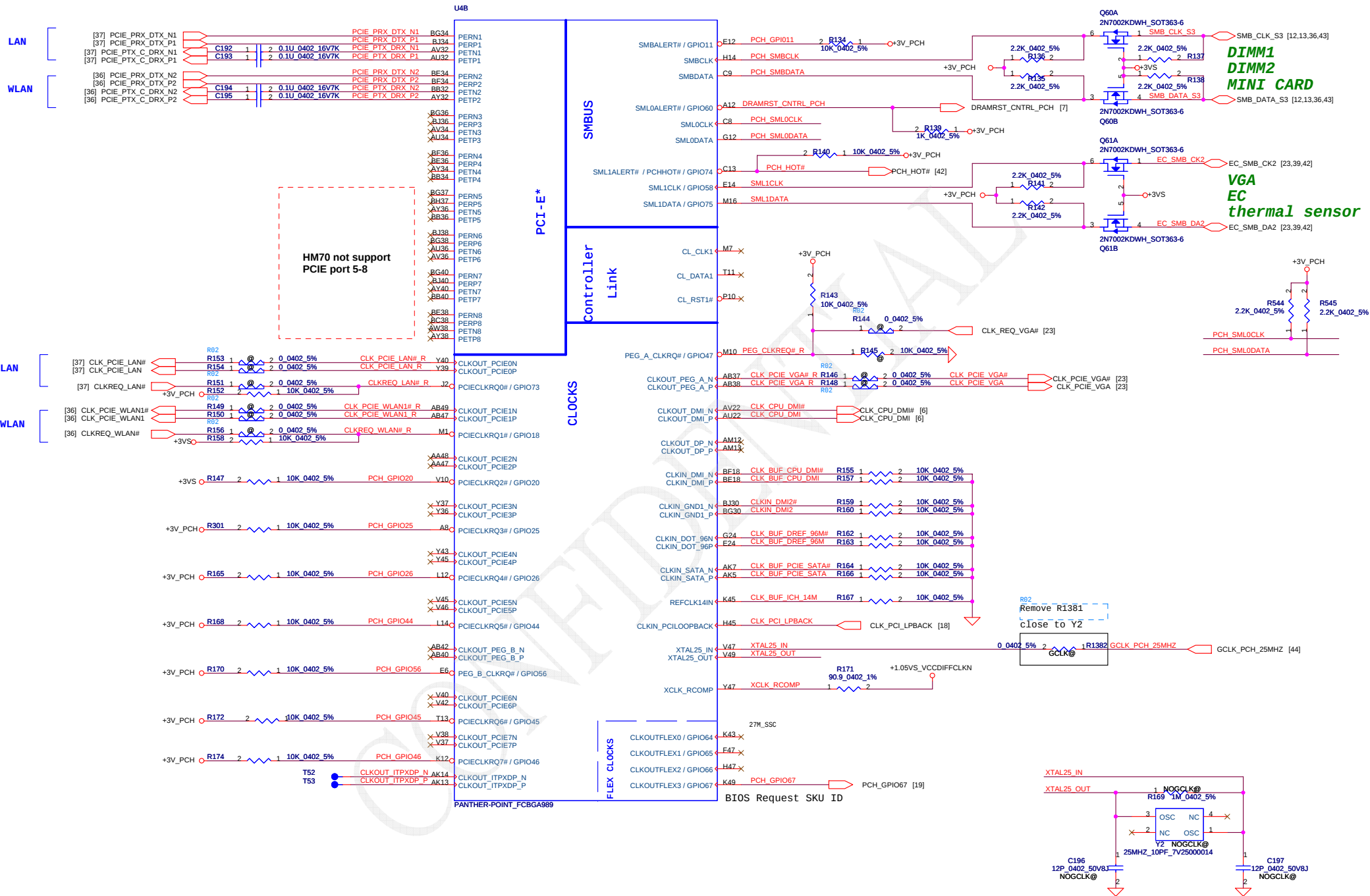
Layout Note:
Place near DIMM

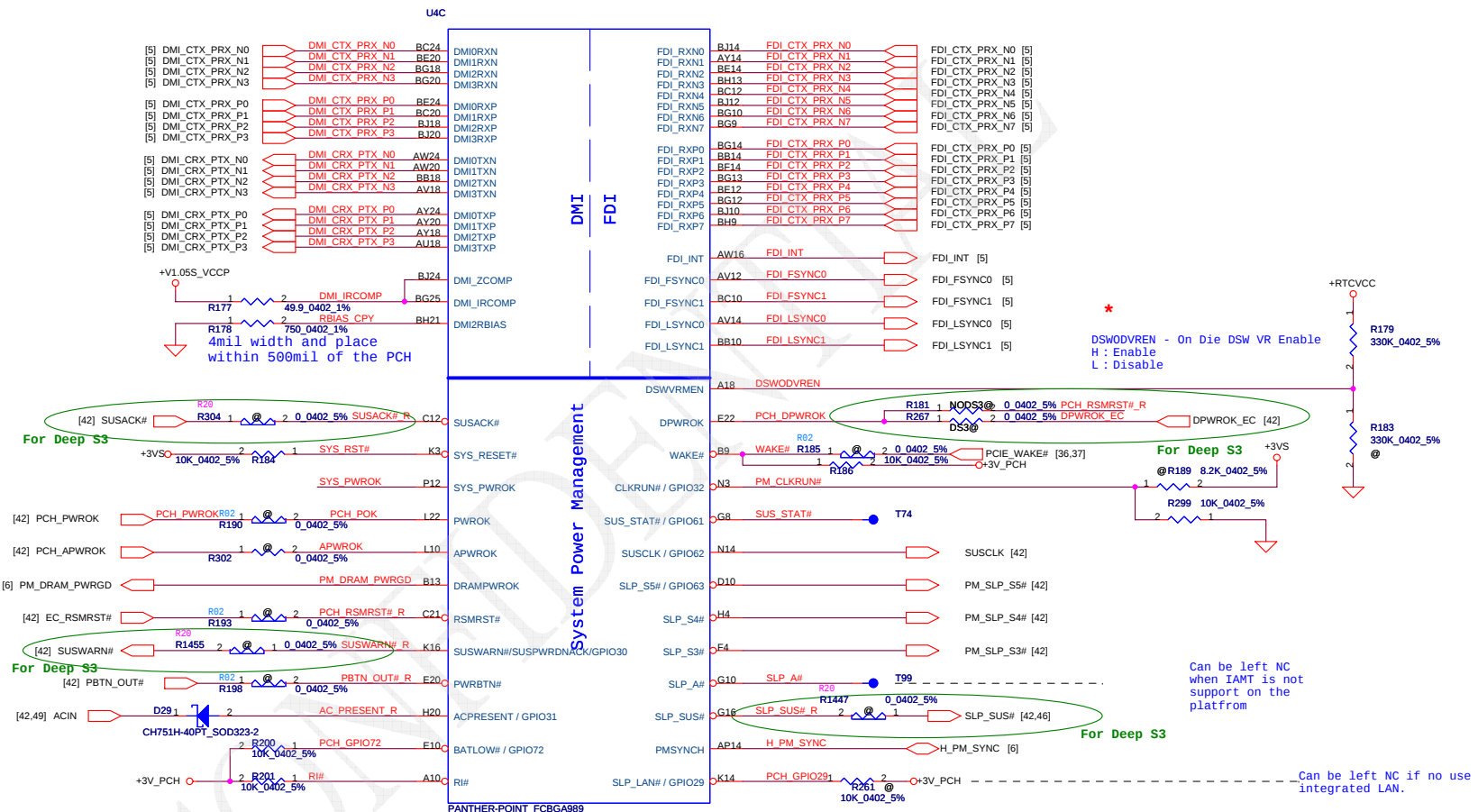
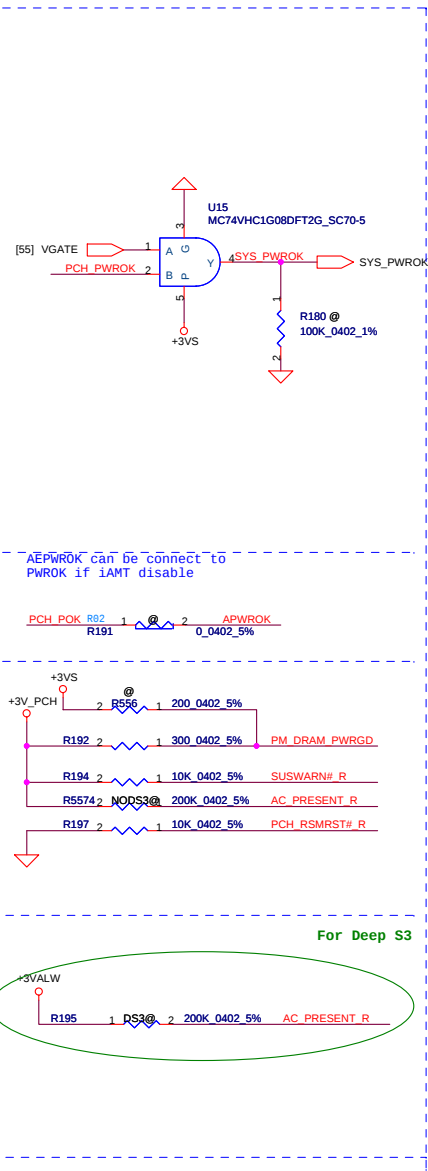
VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

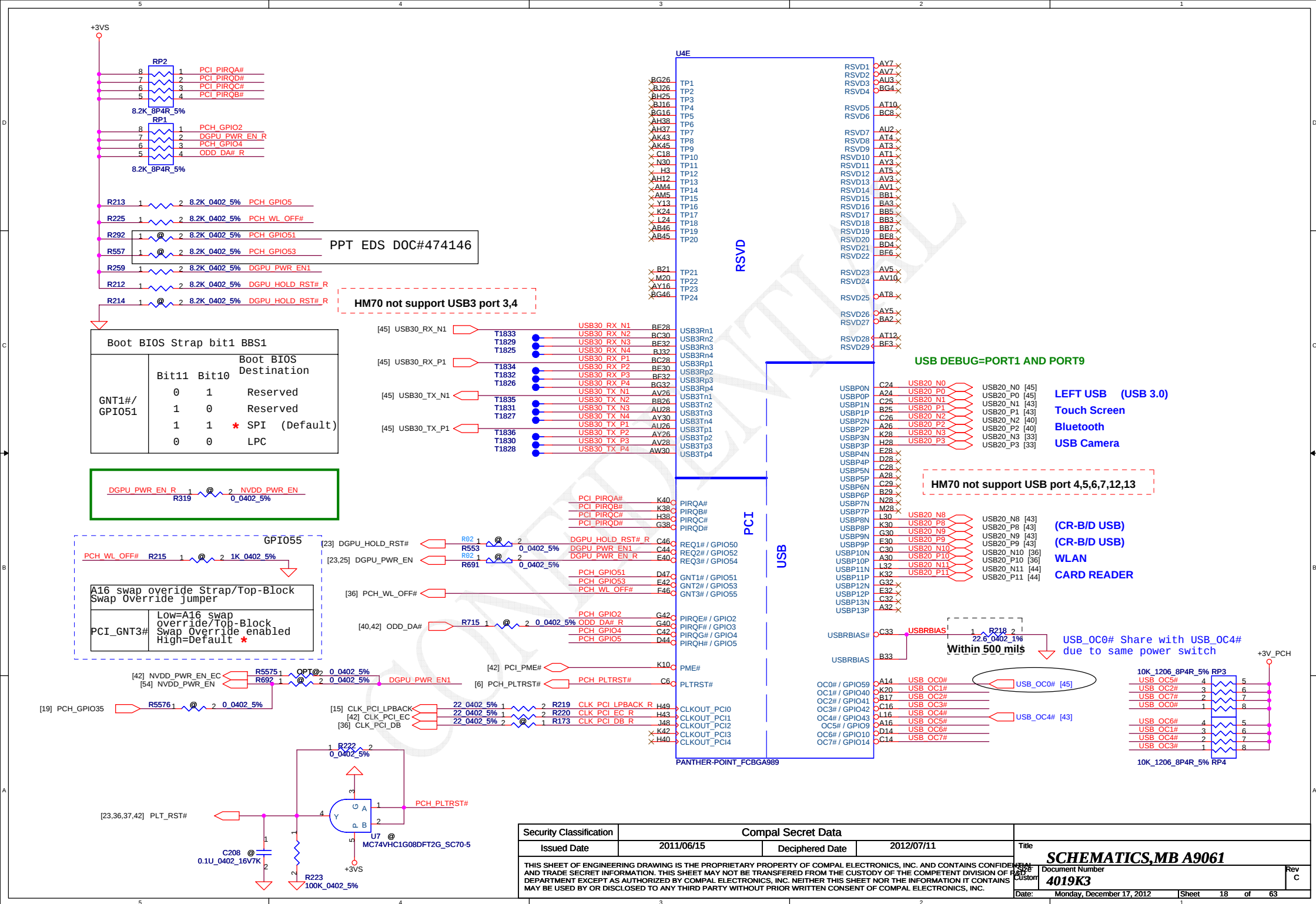
VTT(0.75V) =
3*0805 10uf 4*0402 1uf

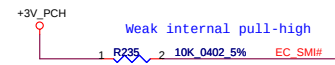
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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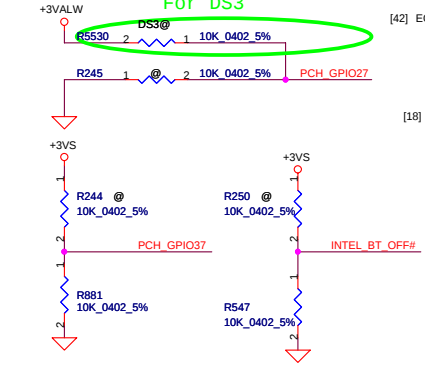




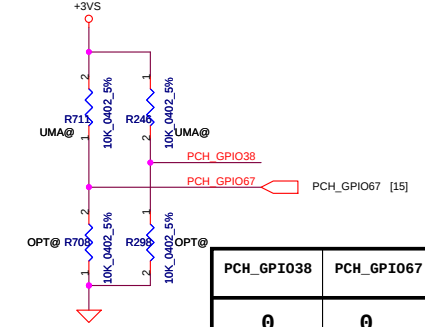


GPI028
On-Die PLL Voltage Regulator
This signal has a Weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

★ Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPI027
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
For DS3

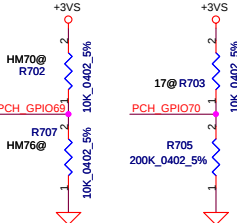


BIOS Request SKU ID

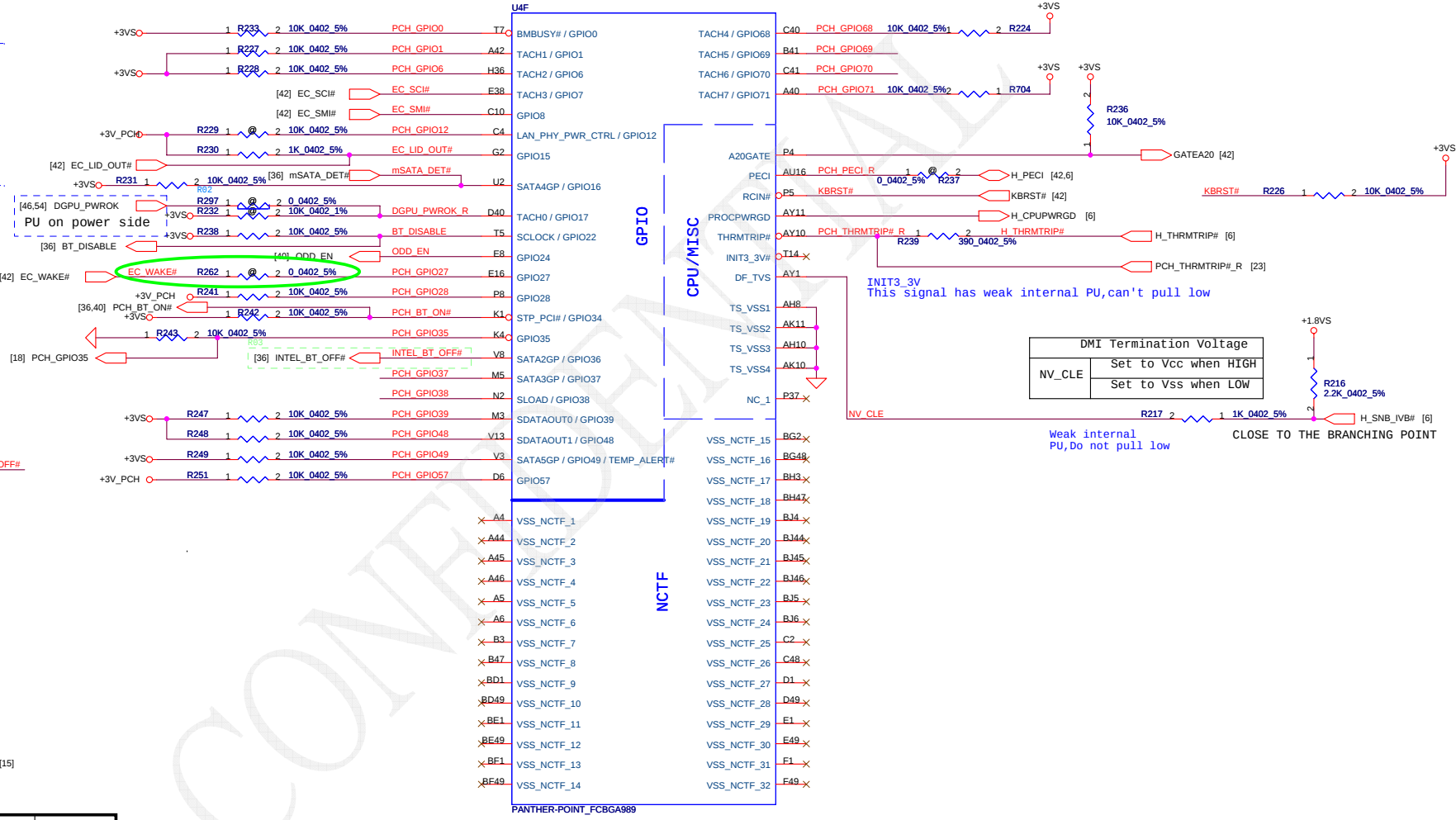


PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
1	1	UMA

PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

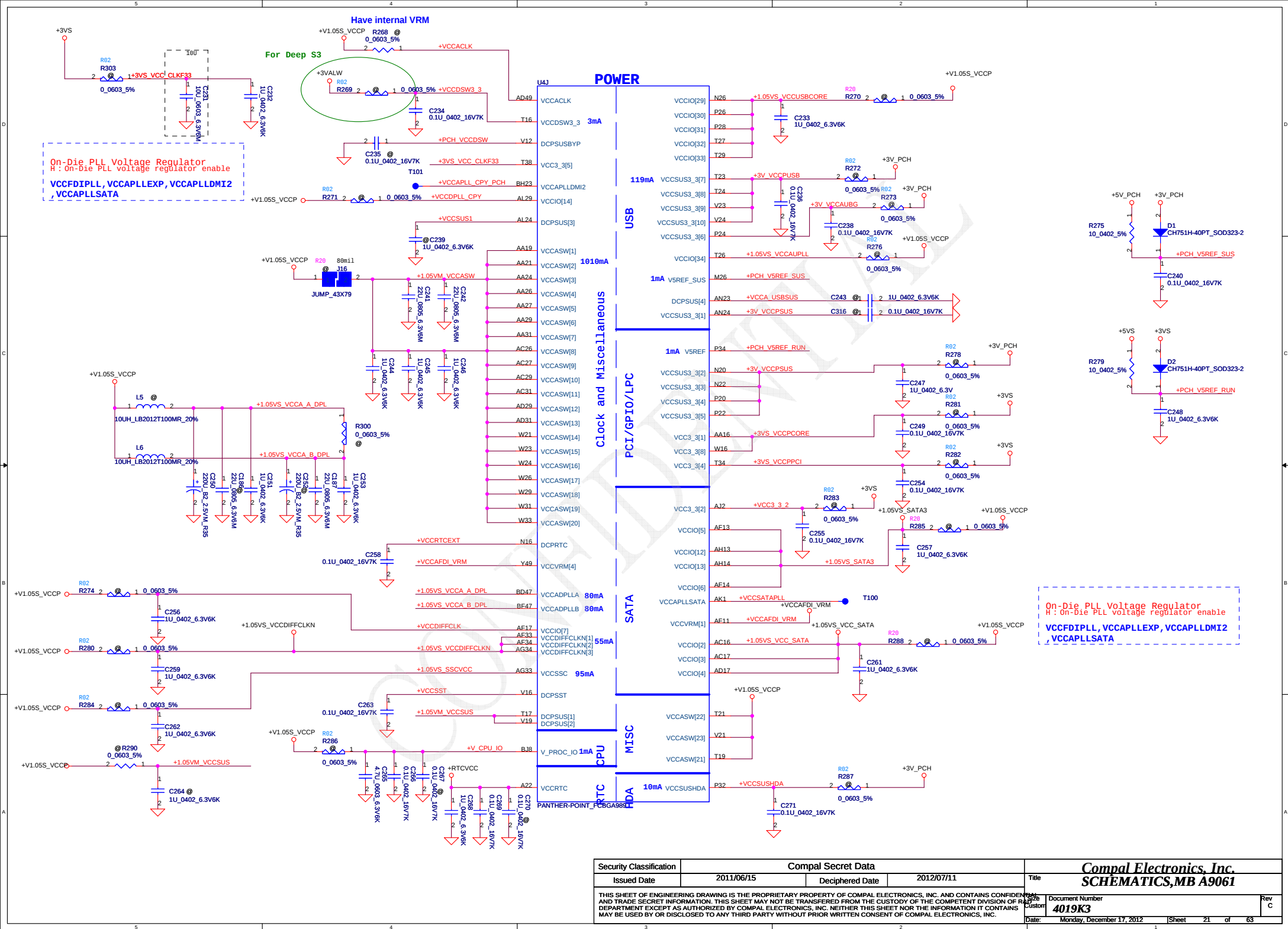


PCH_GPIO70	Function
0	14/15"
1	17"

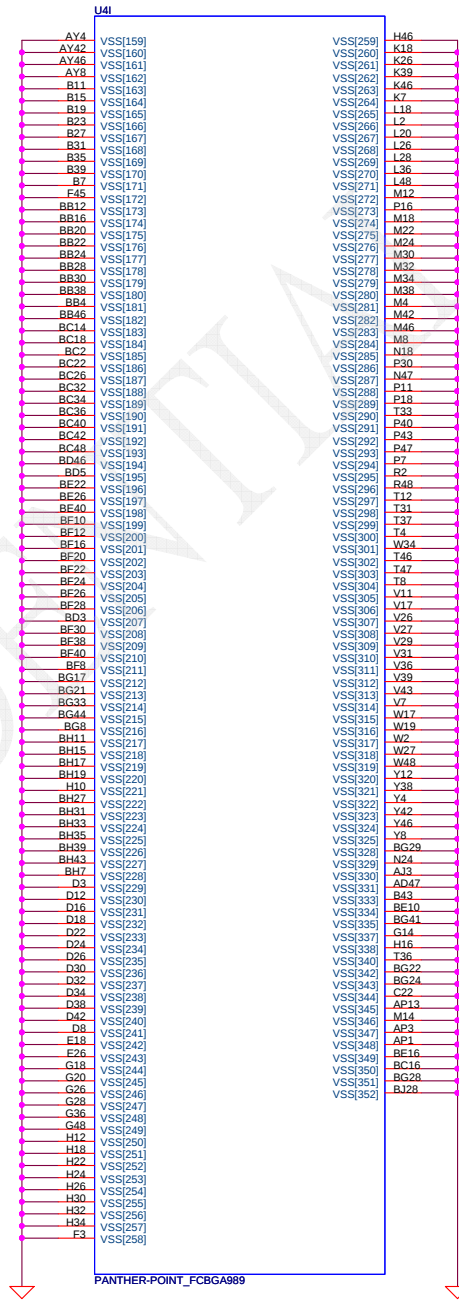
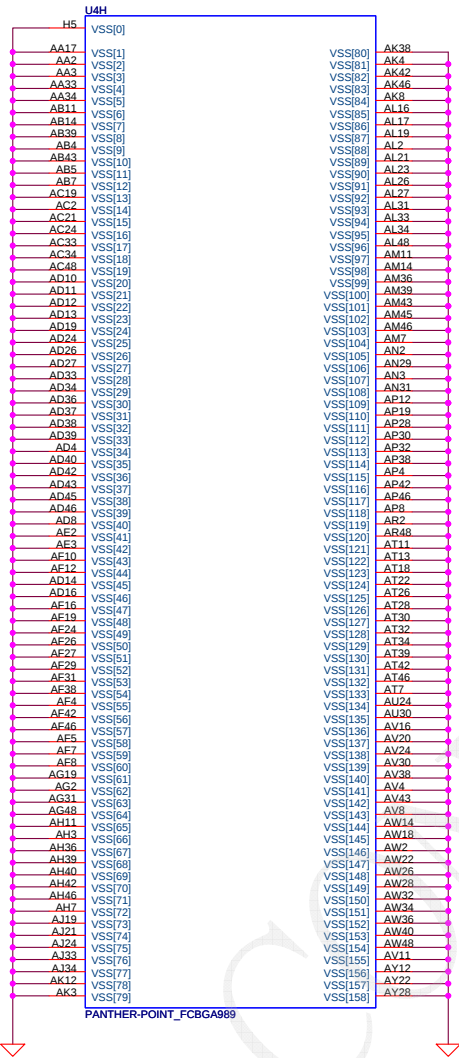


DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

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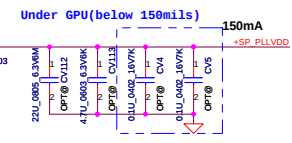
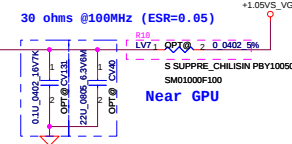
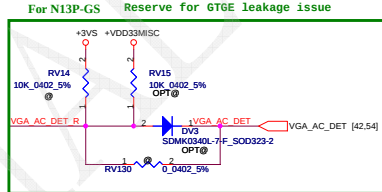
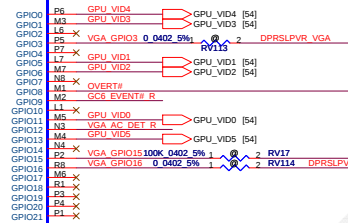
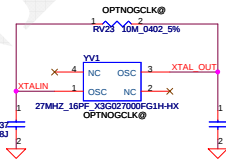
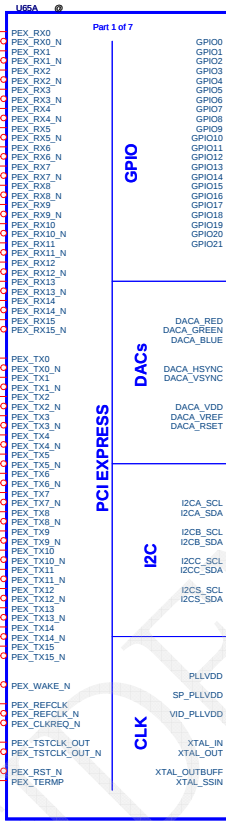
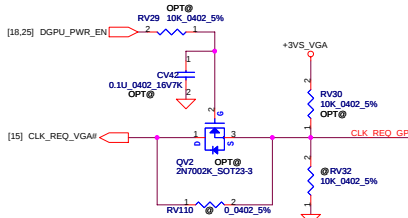
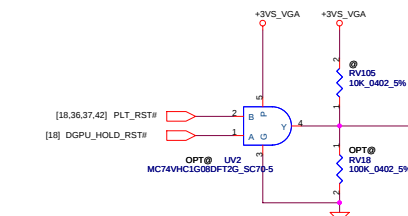
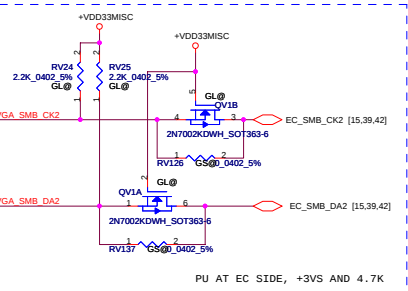
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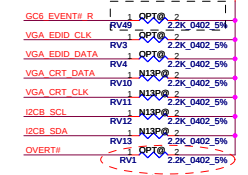
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PCIE_CTX_GRP_P0	CV5	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P0	AK34	PEX_TX0
PCIE_CRX_GRP_N0	CV7	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N0	AJ14	PEX_TX0_N
PCIE_CTX_GRP_P1	CV8	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P1	AH14	PEX_TX1
PCIE_CRX_GRP_N1	CV9	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N1	AJ14	PEX_TX1_N
PCIE_CTX_GRP_P2	CV10	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P2	AK15	PEX_TX2
PCIE_CRX_GRP_N2	CV11	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N2	AJ15	PEX_TX2_N
PCIE_CTX_GRP_P3	CV12	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P3	AL16	PEX_TX3
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PCIE_CTX_GRP_P4	CV14	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P4	AL17	PEX_TX4
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PCIE_CRX_GRP_N5	CV17	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N5	AJ18	PEX_TX5_N
PCIE_CTX_GRP_P6	CV18	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P6	AL19	PEX_TX6
PCIE_CRX_GRP_N6	CV19	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N6	AK19	PEX_TX6_N
PCIE_CTX_GRP_P7	CV20	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P7	AL20	PEX_TX7
PCIE_CRX_GRP_N7	CV21	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N7	AK20	PEX_TX7_N
PCIE_CTX_GRP_P8	CV22	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P8	AG20	PEX_TX8
PCIE_CRX_GRP_N8	CV23	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N8	AJ20	PEX_TX8_N
PCIE_CTX_GRP_P9	CV24	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P9	AG21	PEX_TX9
PCIE_CRX_GRP_N9	CV25	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N9	AJ21	PEX_TX9_N
PCIE_CTX_GRP_P10	CV26	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P10	AK21	PEX_TX10
PCIE_CRX_GRP_N10	CV27	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N10	AJ21	PEX_TX10_N
PCIE_CTX_GRP_P11	CV28	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P11	AL22	PEX_TX11
PCIE_CRX_GRP_N11	CV29	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N11	AK22	PEX_TX11_N
PCIE_CTX_GRP_P12	CV30	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_P12	AK23	PEX_TX12
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PCIE_CRX_GRP_N13	CV33	1	2	0.22u 0.402 5% K	OPT@	PCIE_CRX_C_GRP_N13	AJ24	PEX_TX13_N
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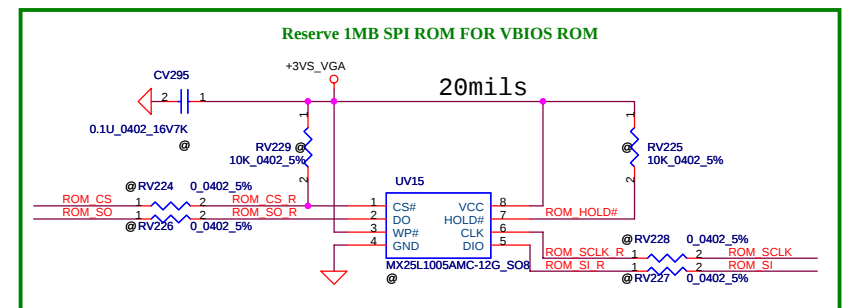
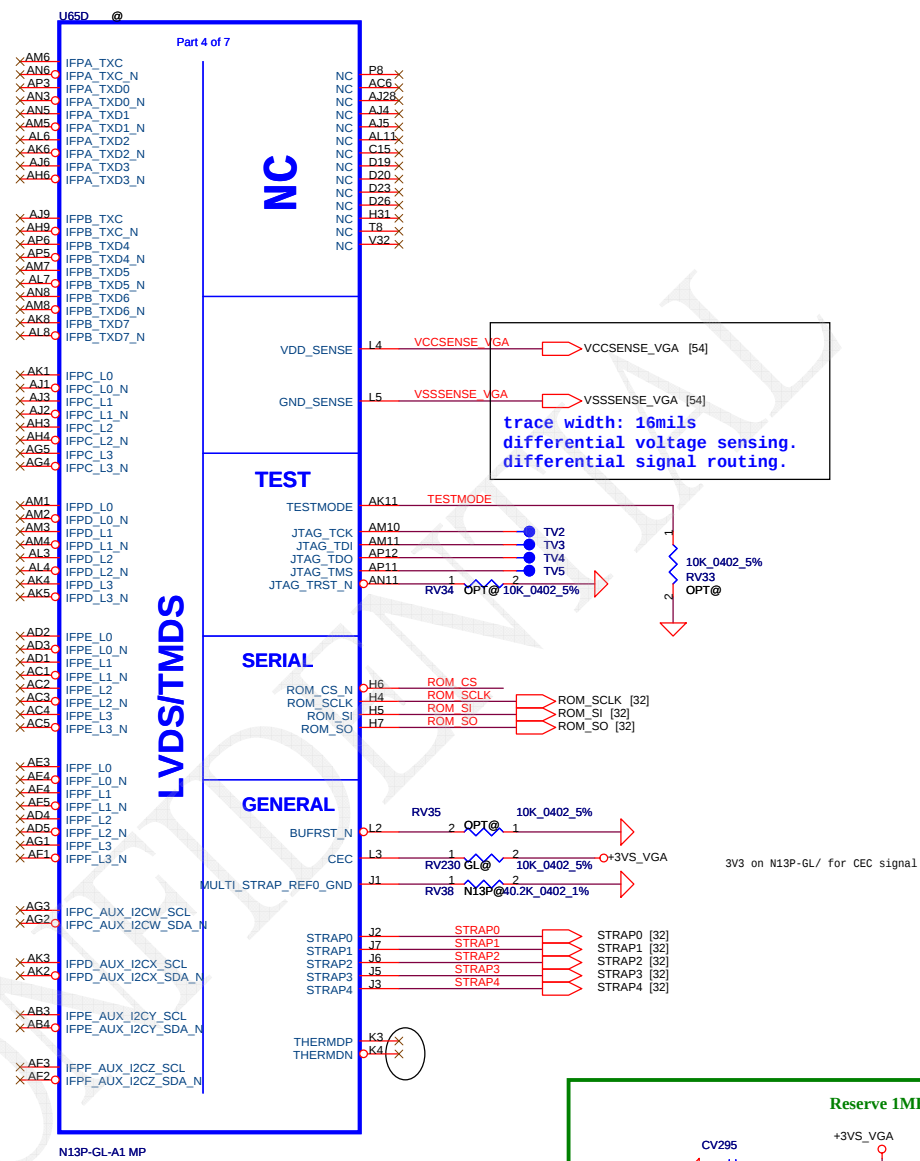
Differential signal



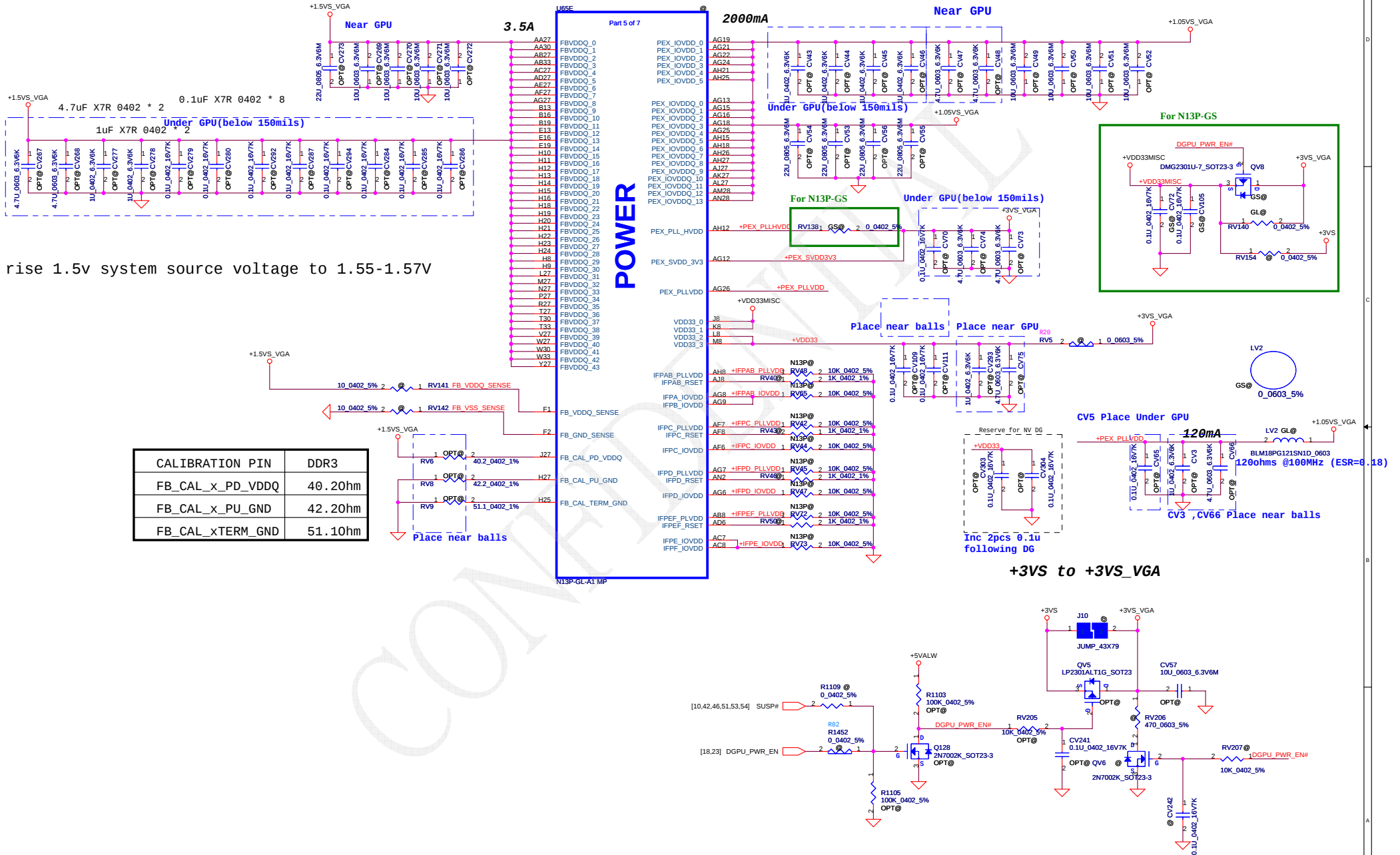
If GCE is supported, stuff the BOM option to pull high to 3.3vs system power, if not, stuff the BOM option to pull high to nv3vs;

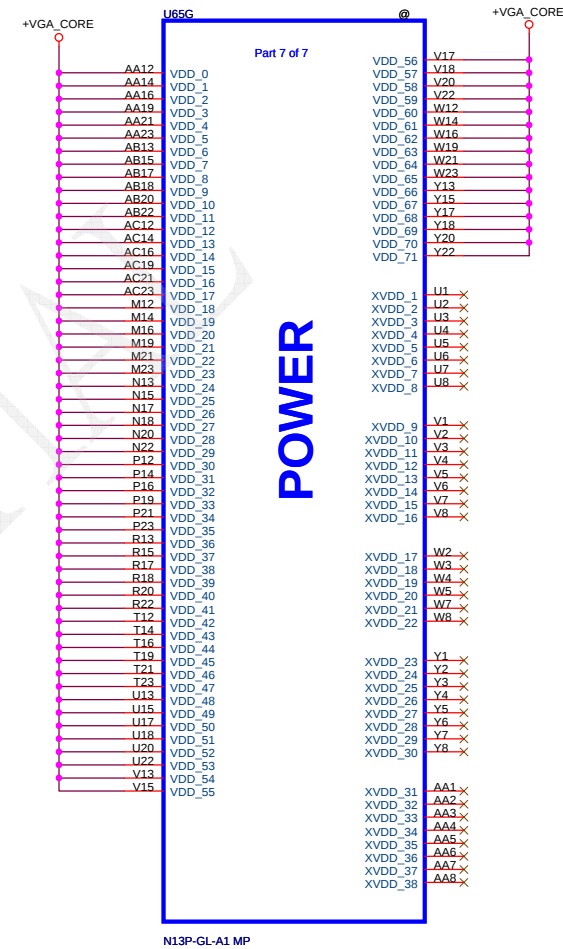
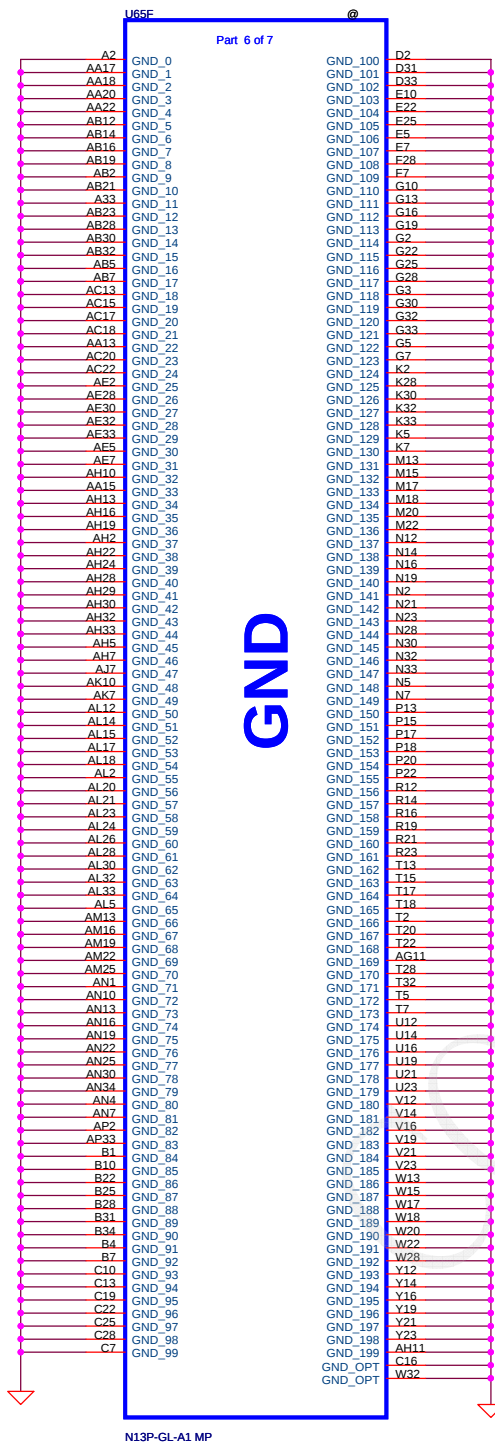


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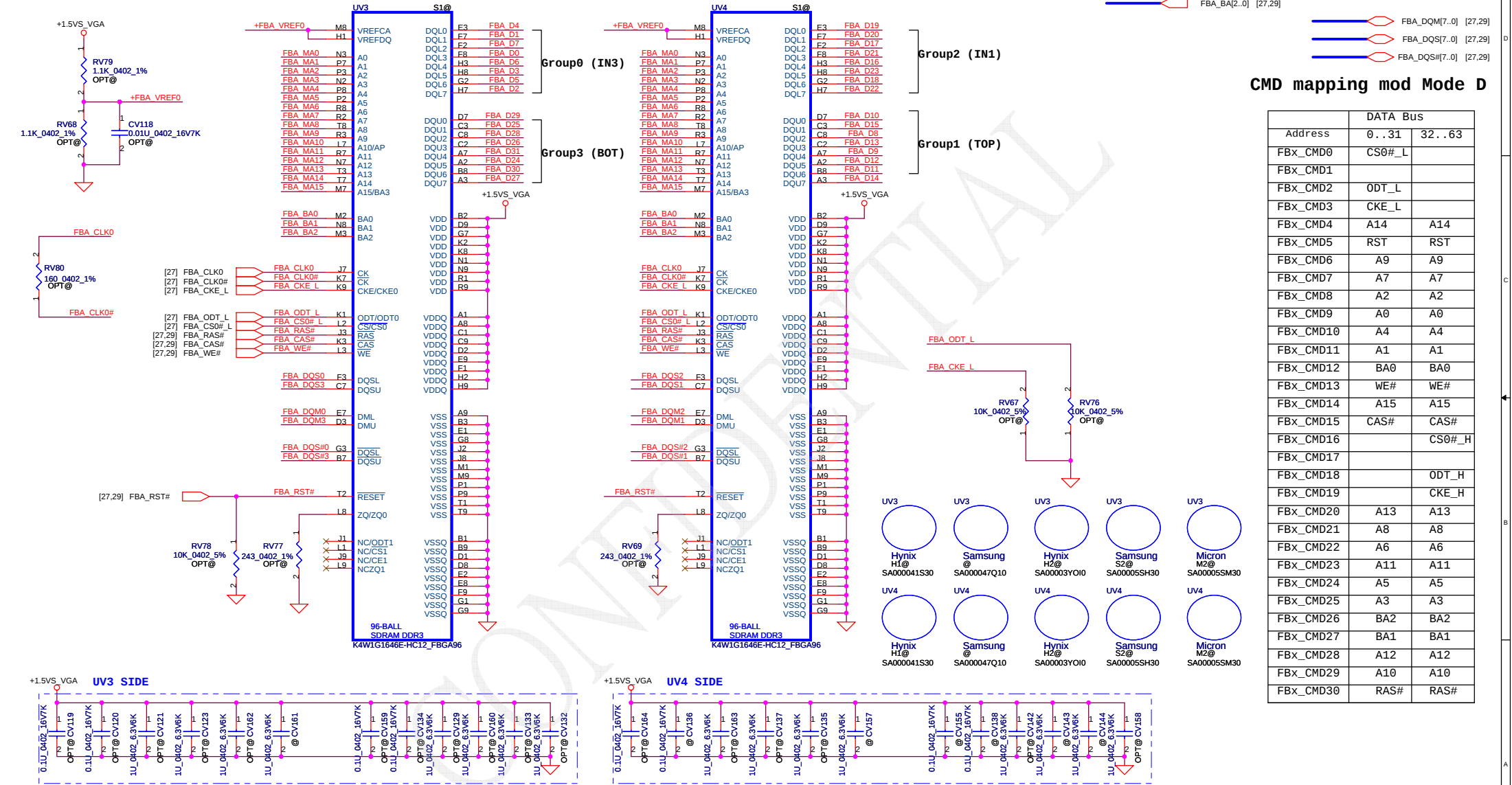
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						Size		Document Number		Rev	
								4019K3		C	
						Date:		Monday, December 17, 2012		Sheet	
								1		26 of 63	

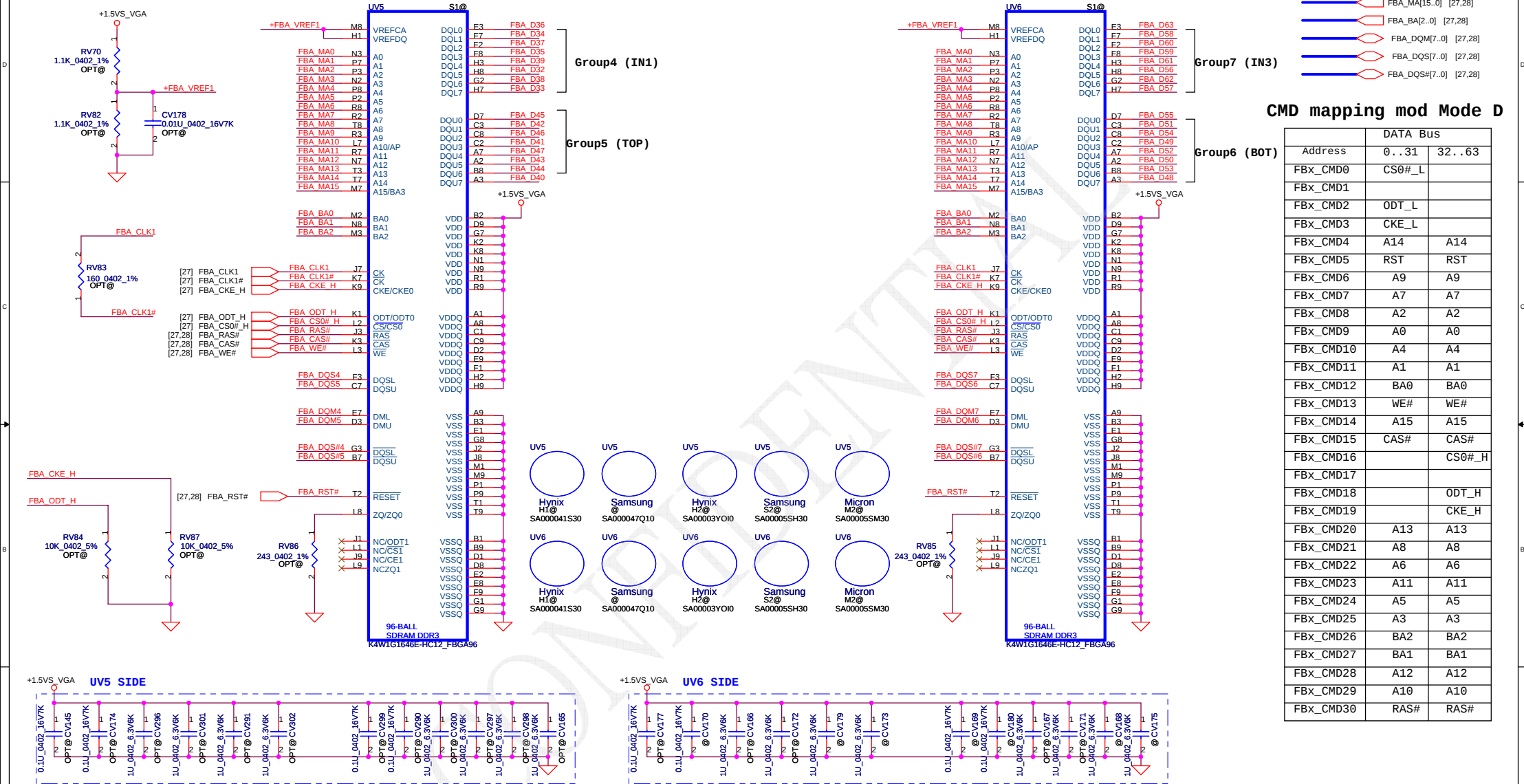
Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

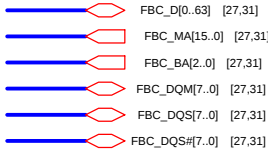
DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

Memory Partition A - Upper 32 bits



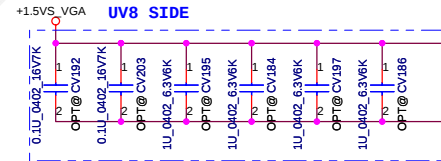
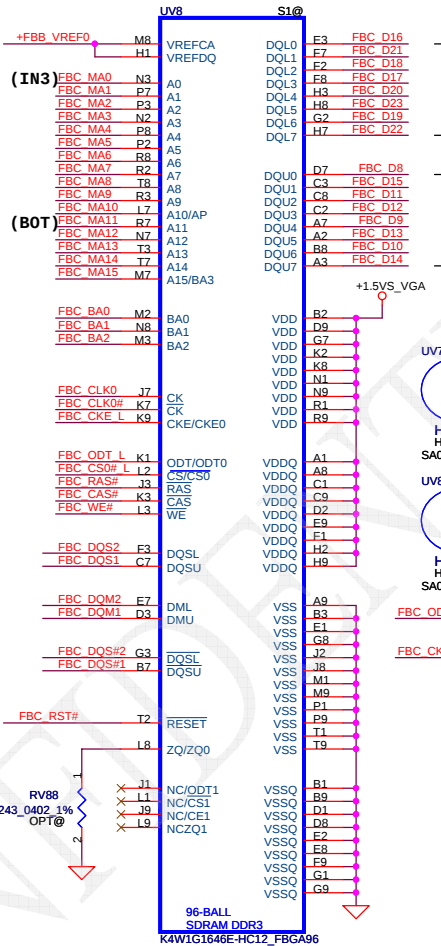
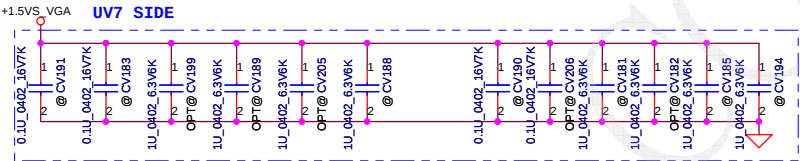
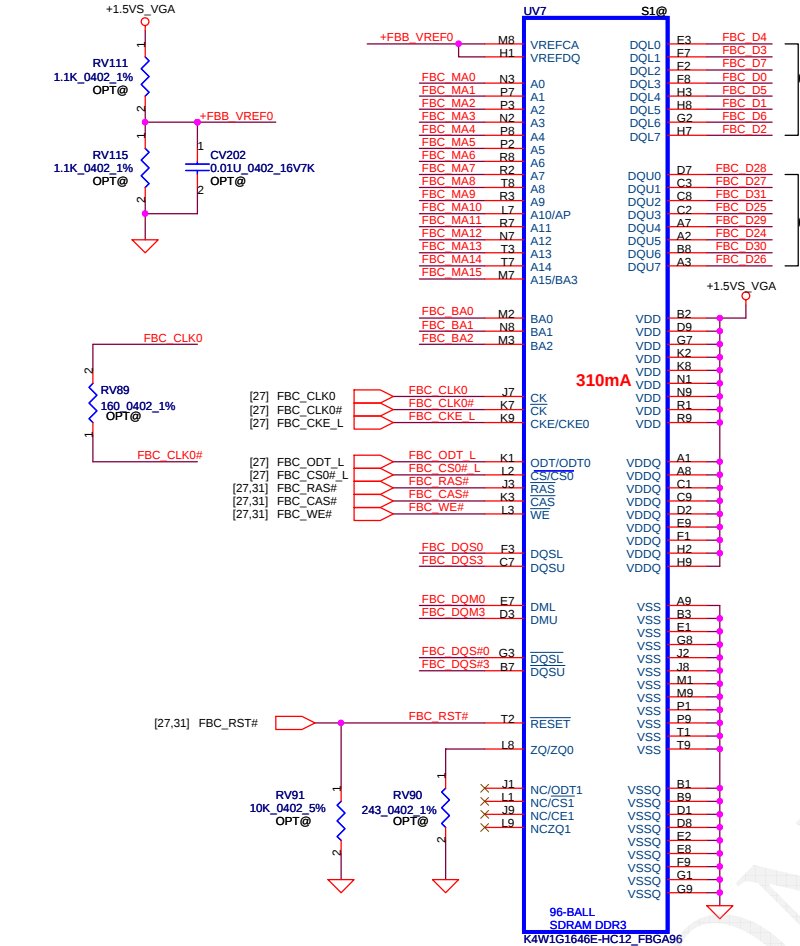
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Memory Partition C - Lower 32 bits

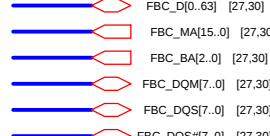
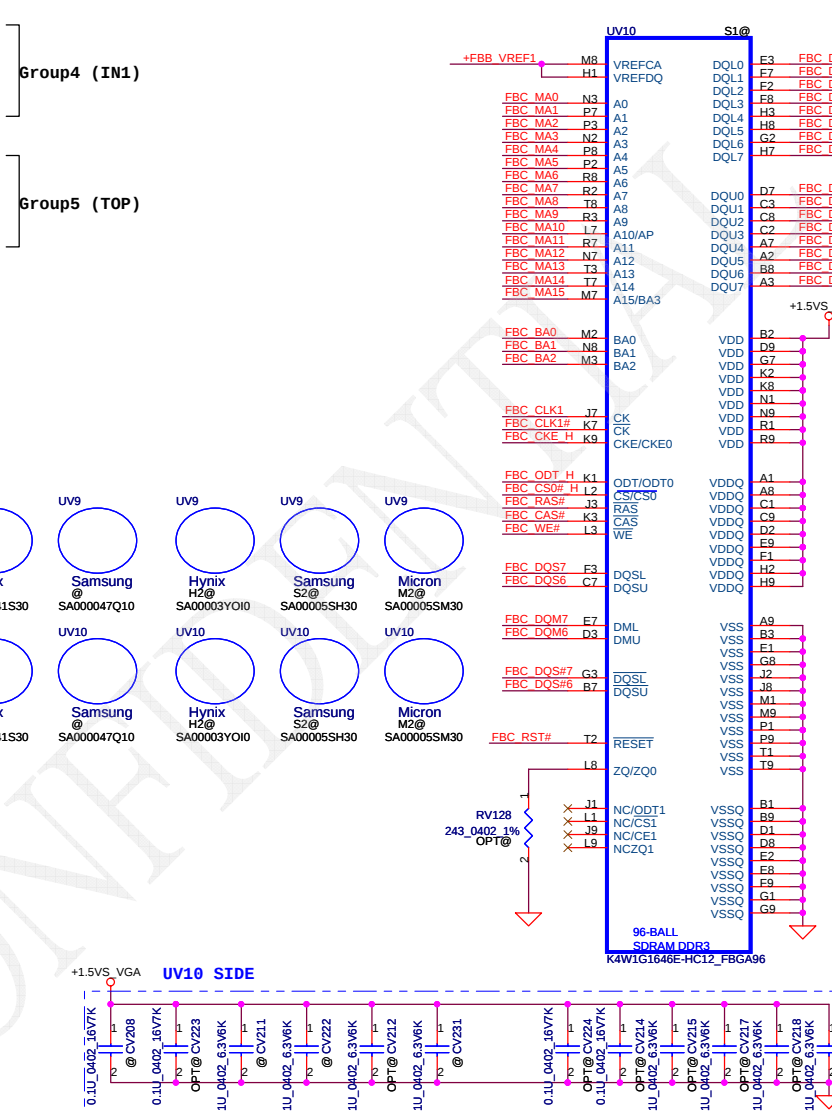
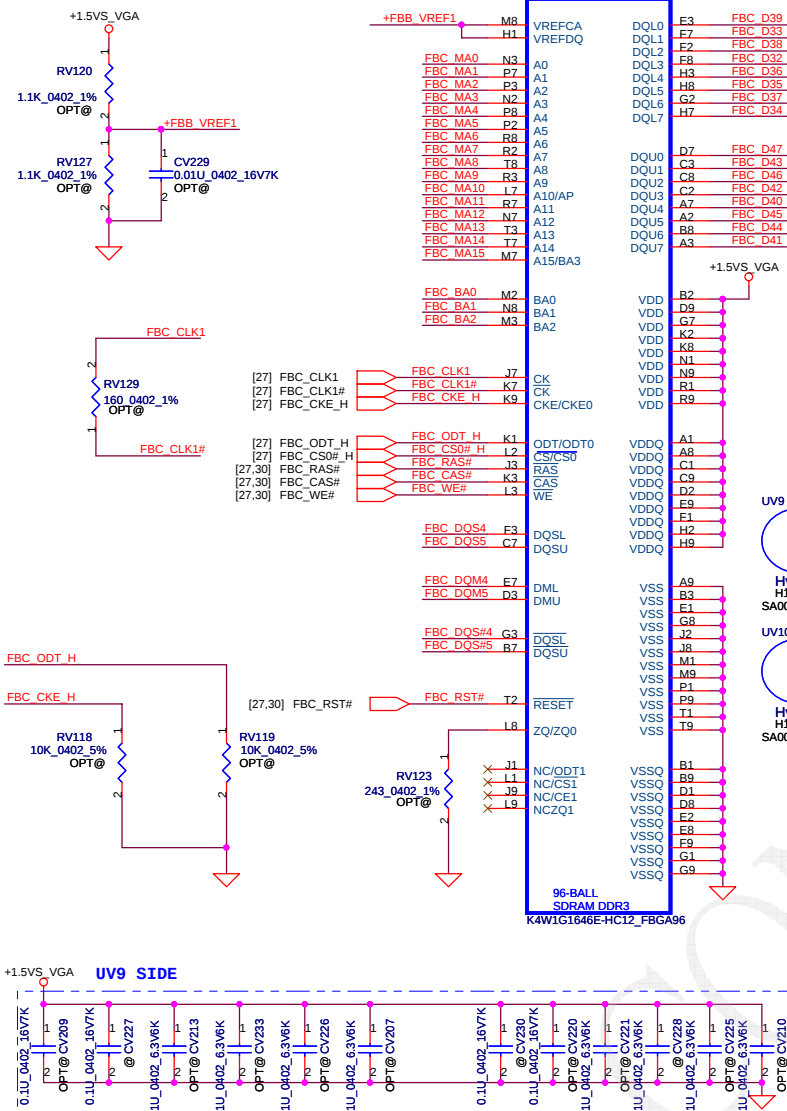


CMD mapping mod Mode D

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



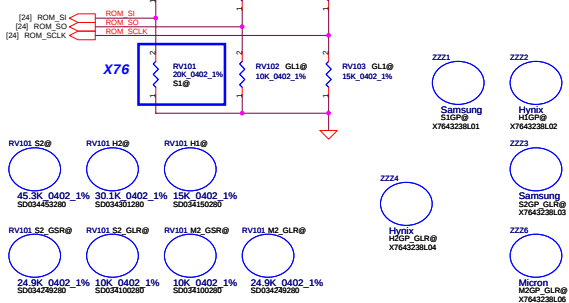
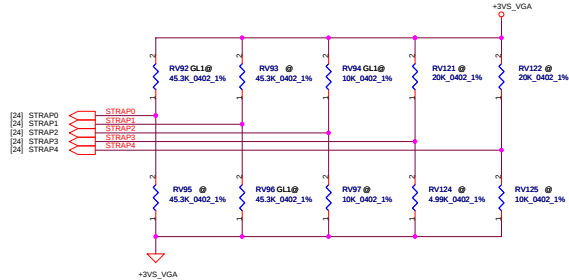
Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

Address	DATA Bus	
	0...31	32...63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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For N13P-GS strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 Mhz	128M*16*8	Samsung (2GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	2GB	K4W2G1646C-HC11	PU 45K	PD 3K	PD 10K	PD 5K	PD 45K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	128M*16*8	Hynix (2GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	2GB	H5TQ2G3K3FER-11C	PU 45K	PD 3K	PD 10K	PD 5K	PD 30 1K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	64M*16*8	Samsung (1GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	1GB	K4W1G1646C-BC11	PU 45K	PD 3K	PD 10K	PD 5K	PD 20K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	64M*16*8	Hynix (1GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	1GB	H5TQ1G3K3FER-11C	PU 45K	PD 3K	PD 10K	PD 5K	PD 10K	PU 10K	PU 5K	PU 5K

For N13P-GSR strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 Mhz	128M*16*8	Samsung (2GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	2GB	K4W2G1646C-HC11	PU 45K	PD 3K	PU 10K	PD 3K	PD 45K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	128M*16*8	Hynix (2GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	2GB	H5TQ2G3K3FER-11C	PU 45K	PD 3K	PU 10K	PD 3K	PD 30 1K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	64M*16*8	Samsung (1GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	1GB	K4W1G1646C-BC11	PU 45K	PD 3K	PU 10K	PD 3K	PD 20K	PU 10K	PU 5K	PU 5K
N13P-GS	900 Mhz	64M*16*8	Hynix (1GB)	R	R	R	R	R	R	R	R
N13P-GS	900 Mhz	1GB	H5TQ1G3K3FER-11C	PU 45K	PD 3K	PU 10K	PD 3K	PD 10K	PU 10K	PU 5K	PU 5K

For N13P-GL strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 Mhz	128M*16*8	Samsung (2GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	2GB	K4W2G1646C-HC11	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 45K	PU 10K	PD 10K
N13P-GL	900 Mhz	128M*16*8	Hynix (2GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	2GB	H5TQ2G3K3FER-11C	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 30 1K	PU 10K	PD 10K
N13P-GL	900 Mhz	64M*16*8	Samsung (1GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	1GB	K4W1G1646C-BC11	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 20K	PU 10K	PD 10K
N13P-GL	900 Mhz	64M*16*8	Hynix (1GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	1GB	H5TQ1G3K3FER-11C	PU 45K	PD 45K	PU 10K	n/a	n/a	PD 10K	PU 10K	PD 10K

For N13P-GLR strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 Mhz	128M*16*8	Samsung (2GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	2GB	K4W2G1646C-HC11	PU 45K	PD 45K	PD 20K	n/a	n/a	PD 45K	PU 10K	PD 10K
N13P-GL	900 Mhz	128M*16*8	Hynix (2GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	2GB	H5TQ2G3K3FER-11C	PU 45K	PD 45K	PD 20K	n/a	n/a	PD 30 1K	PU 10K	PD 10K
N13P-GL	900 Mhz	64M*16*8	Samsung (1GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	1GB	K4W1G1646C-BC11	PU 45K	PD 45K	PD 20K	n/a	n/a	PD 20K	PU 10K	PD 10K
N13P-GL	900 Mhz	64M*16*8	Hynix (1GB)	R	R	R	R	R	R	R	R
N13P-GL	900 Mhz	1GB	H5TQ1G3K3FER-11C	PU 45K	PD 45K	PD 20K	n/a	n/a	PD 10K	PU 10K	PD 10K



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	SMB_ALT_ADDR	VGA_DEVICE	
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3G10_PAD_CFG_ADDR[3]	3G10_PAD_CFG_ADDR[2]	3G10_PAD_CFG_ADDR[1]	3G10_PAD_CFG_ADDR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Vendor	VRAM Sturcture
Samsung 2G	S2@
Hynix 2G	H2@
Samsung 1G	S1@
Hynix 1G	H1@

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

FB_0 BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

PCIE_MAX_SPEED

0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

3G10_PADCFG

3G10_PADCFG[3:0]	
0110	Notebook Default

XCLK_417

0	277MHz (Default)
1	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

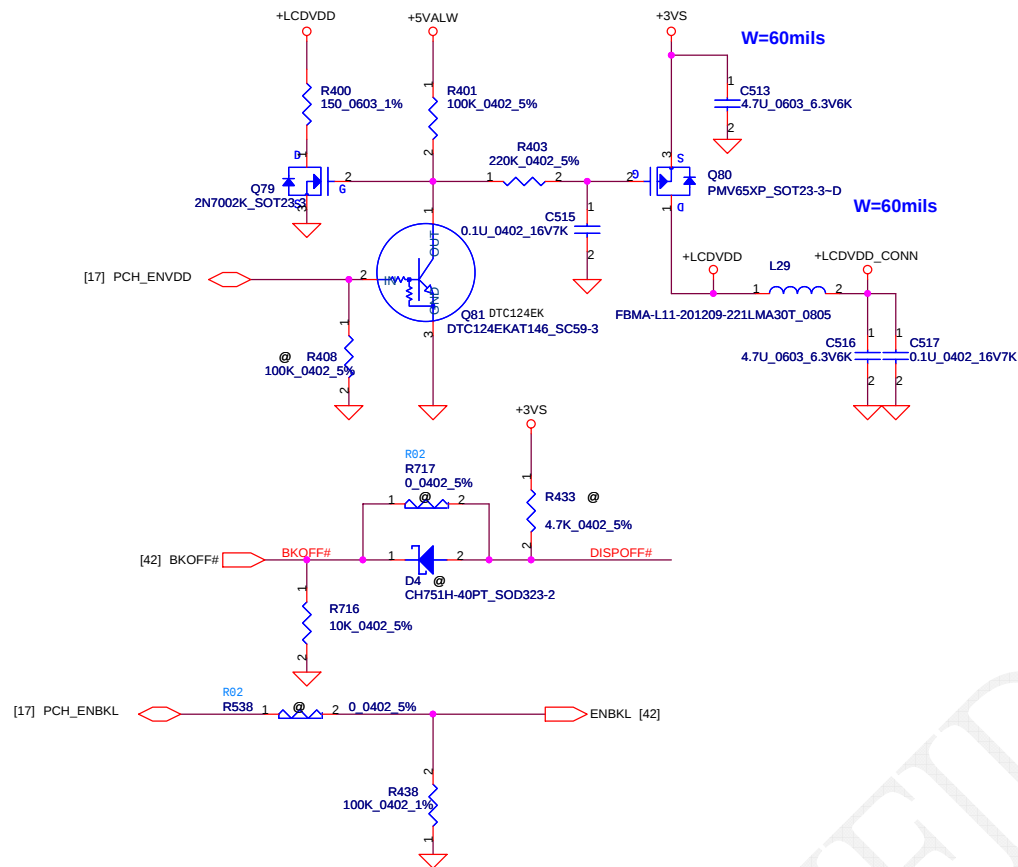
SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

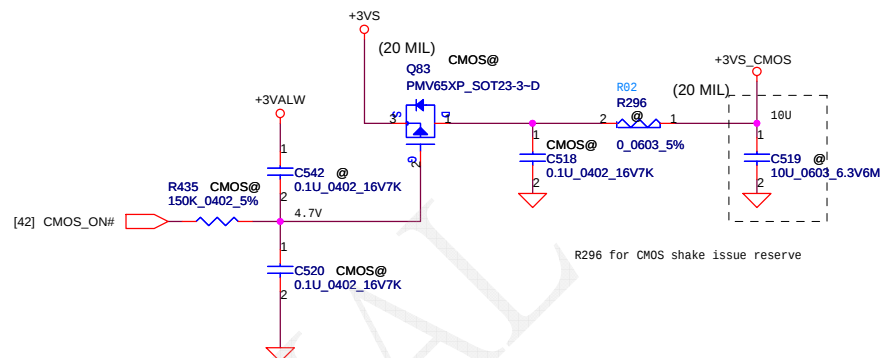
VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

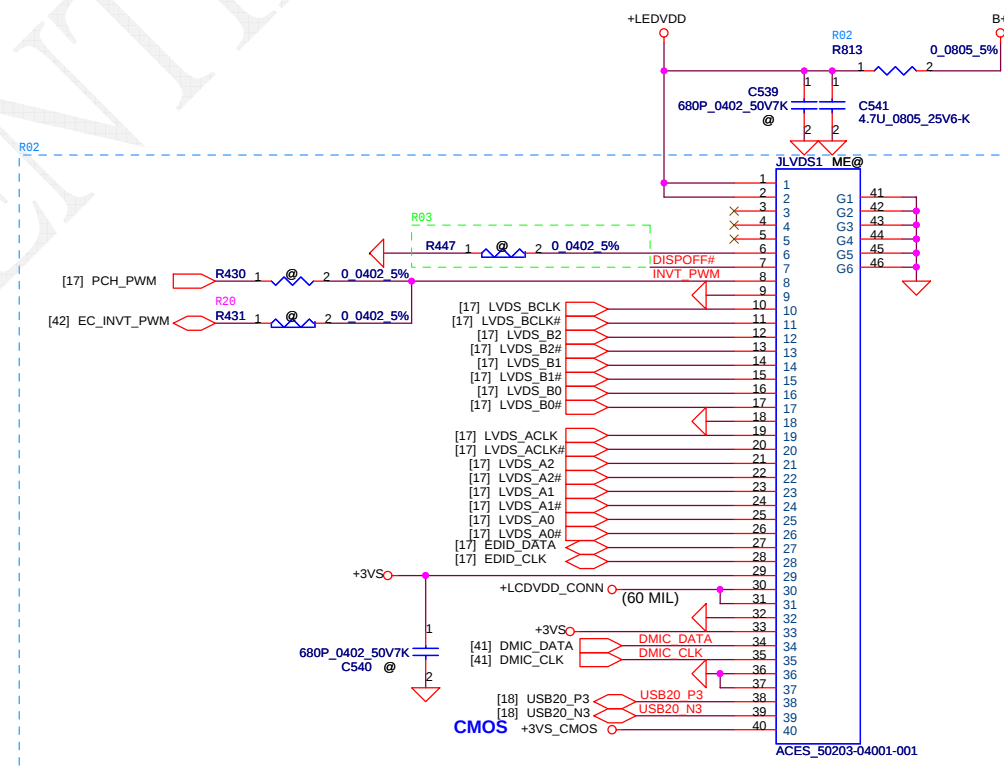
LCD POWER CIRCUIT



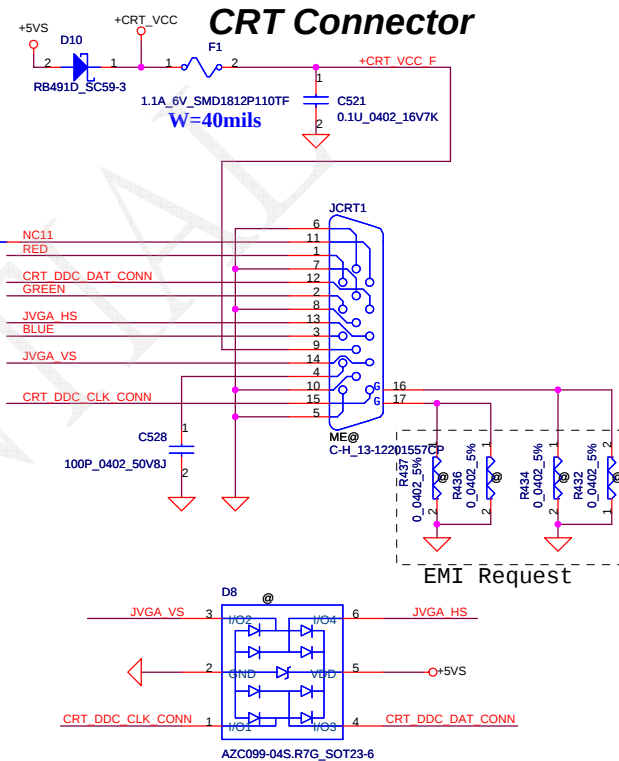
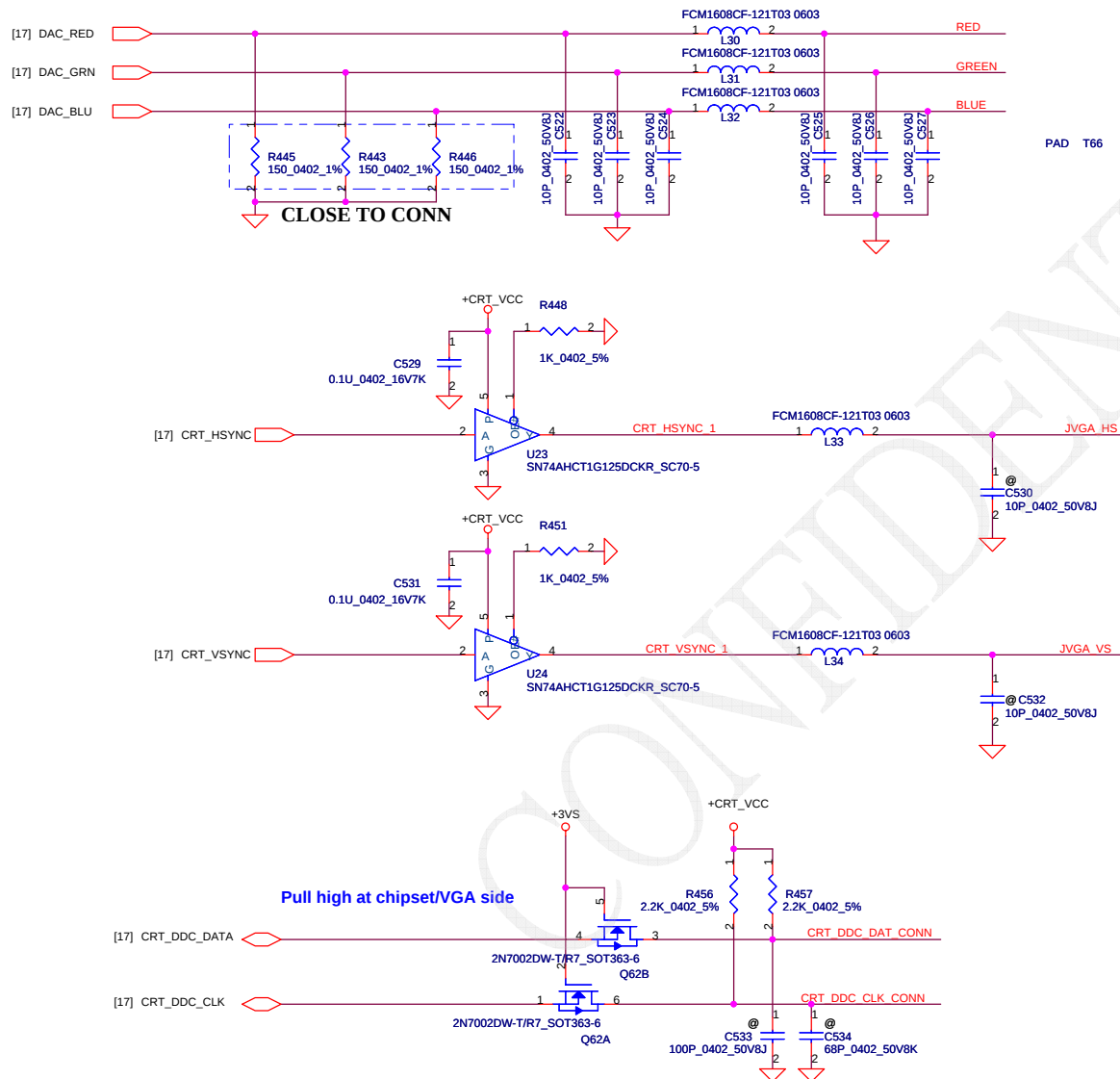
CMOS Camera



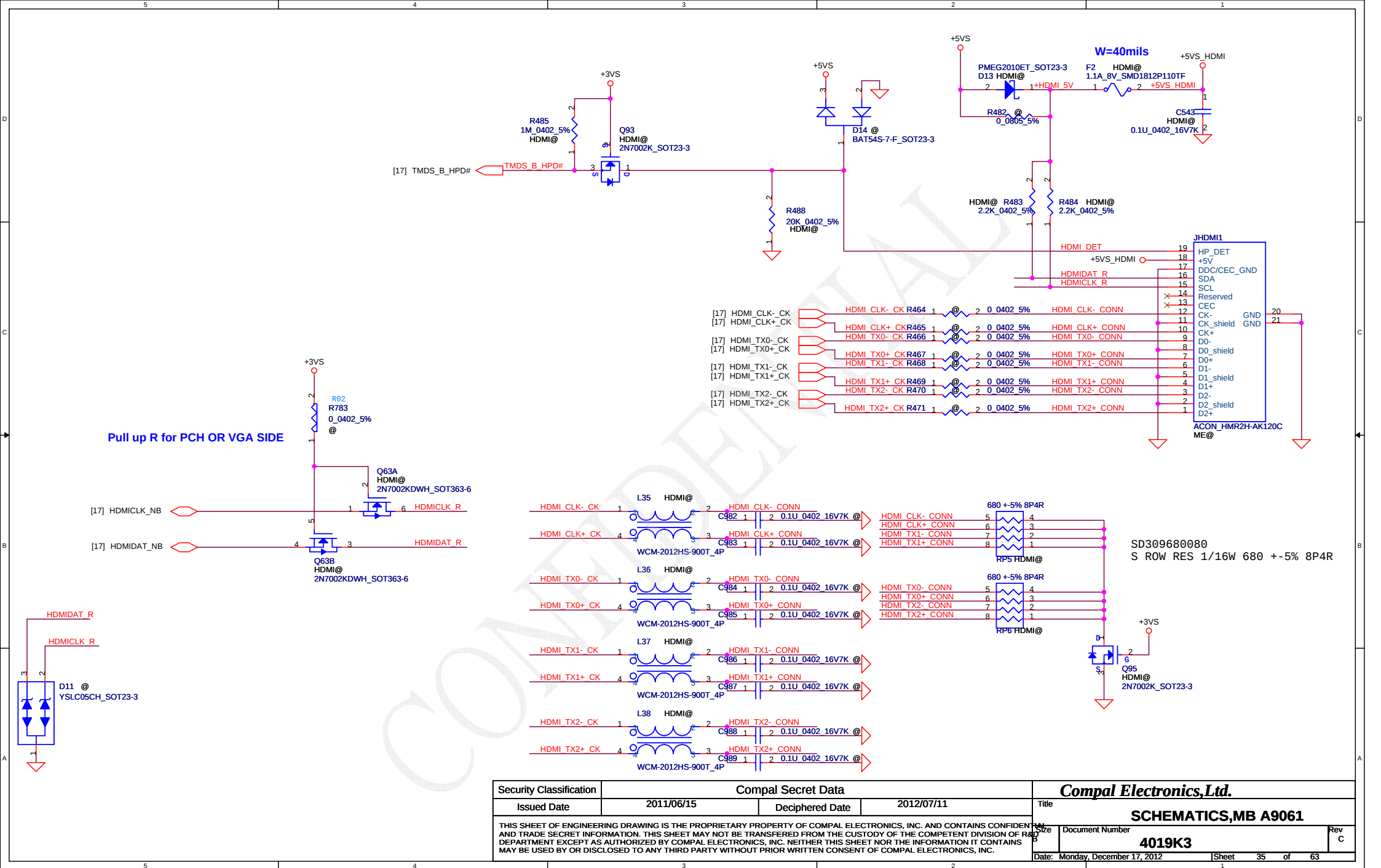
VGA LCD/PANEL BD. Conn.



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				Sheet	33 of 63

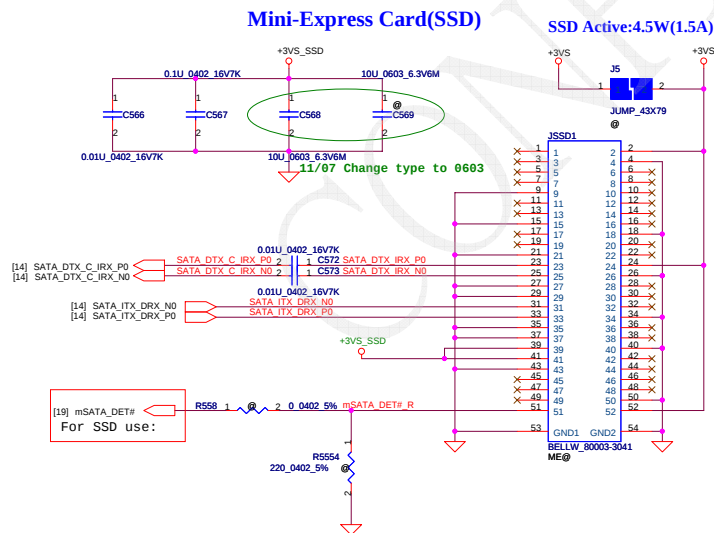
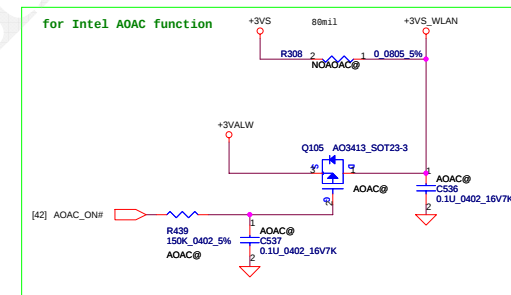
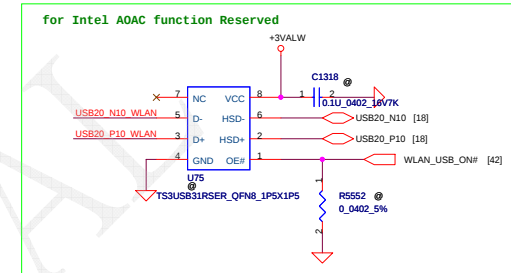
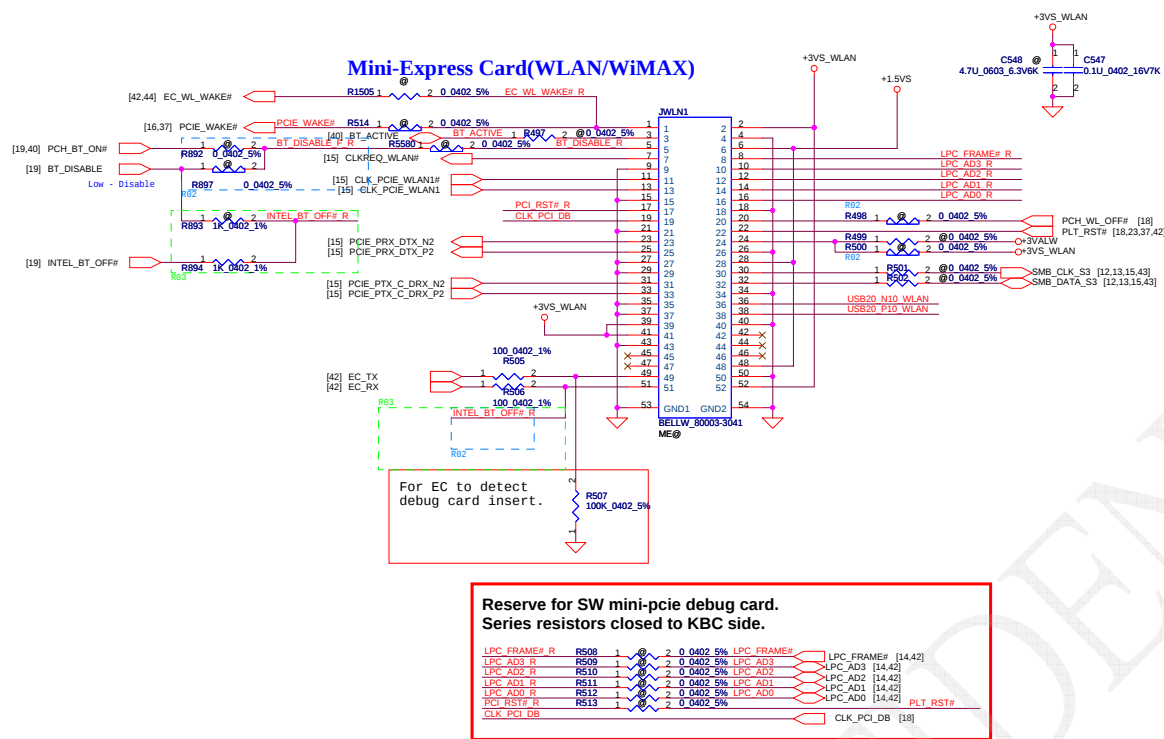


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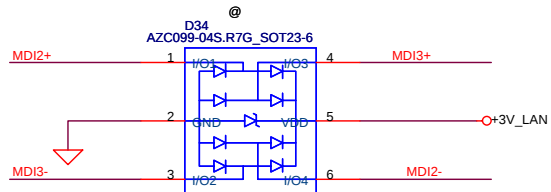


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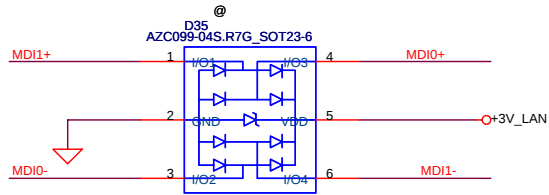
Mini-Express Card for WLAN/WiMAX(Half)



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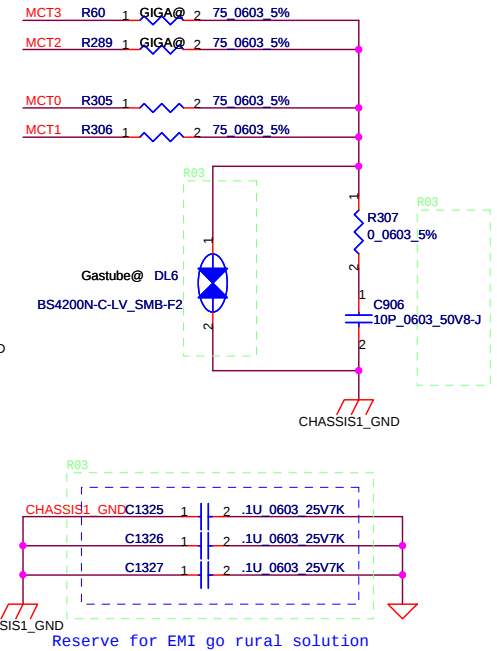
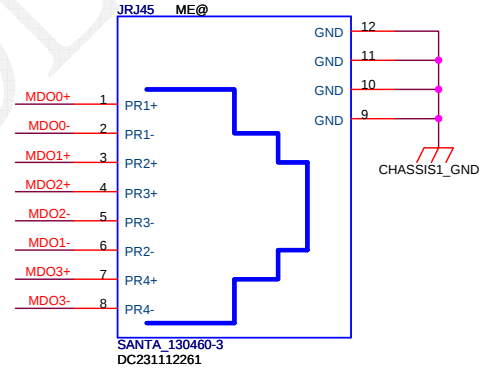
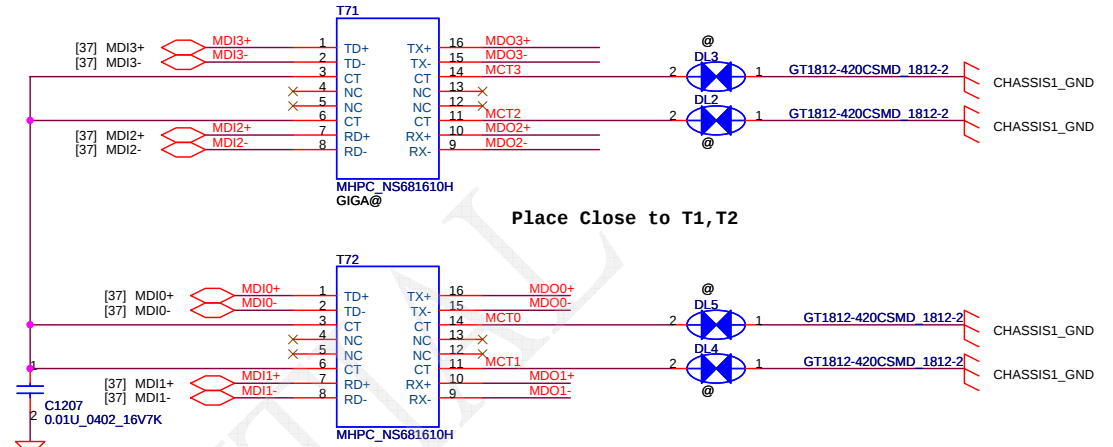


Place Close to T71



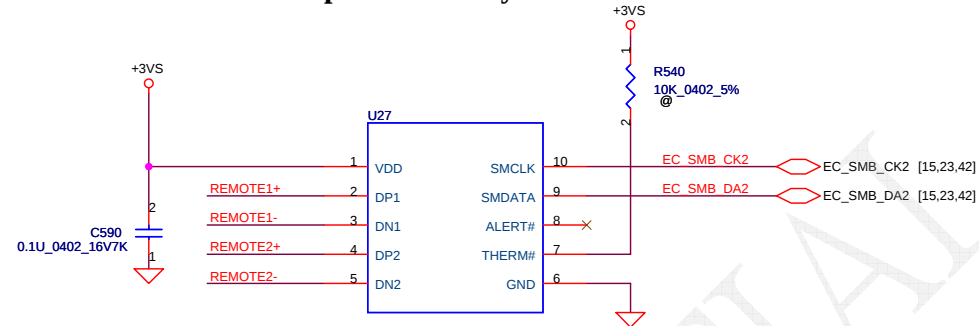
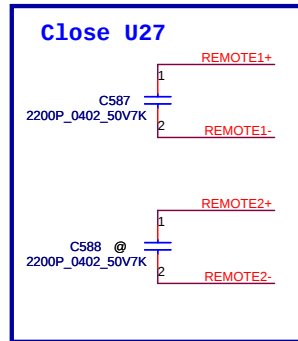
Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

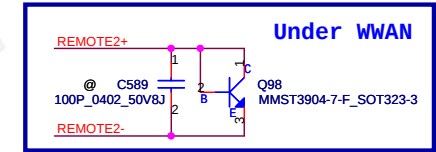
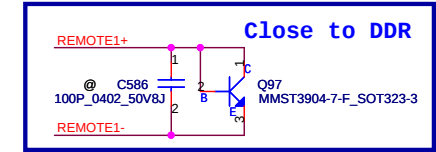


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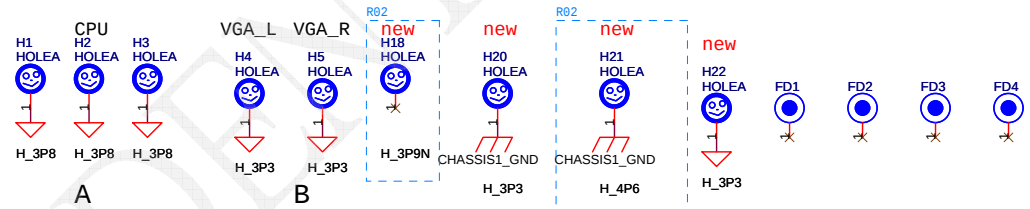
SMSC thermal sensor placed near by VRAM



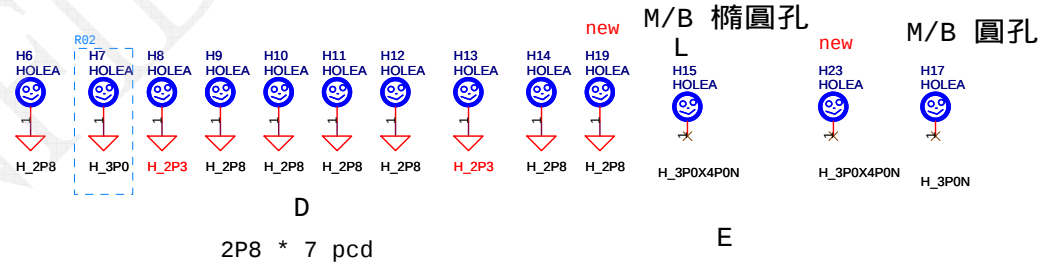
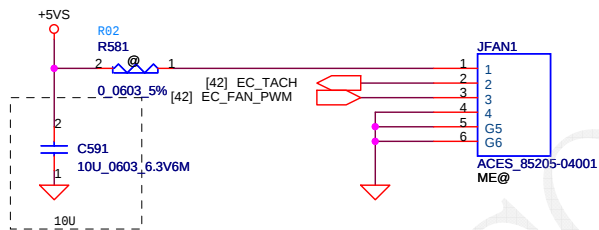
Address 1001_101xb



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

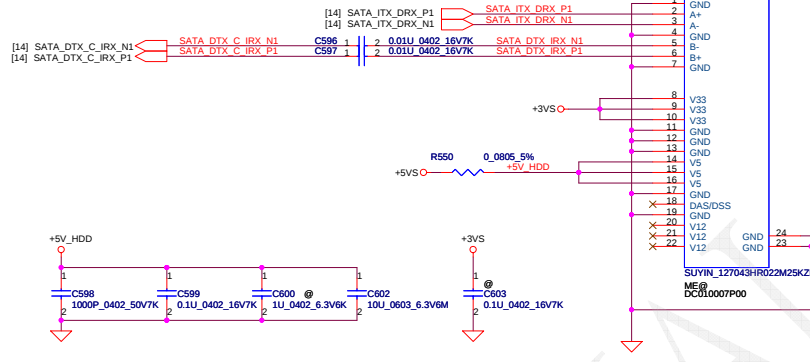


FAN1 Conn

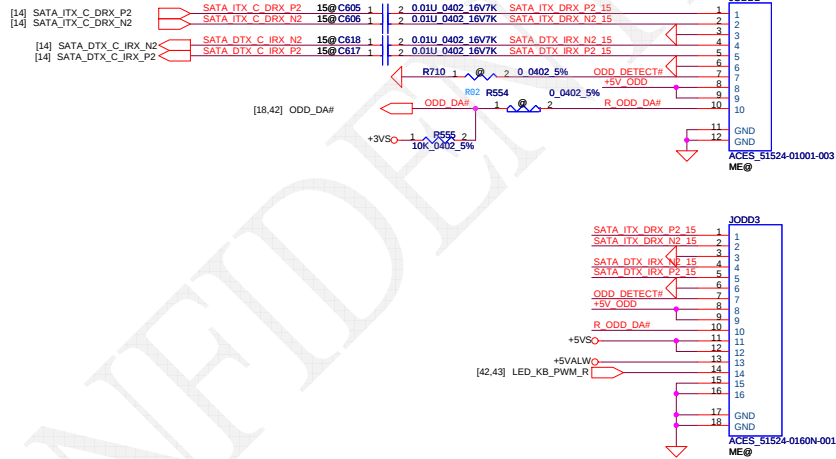


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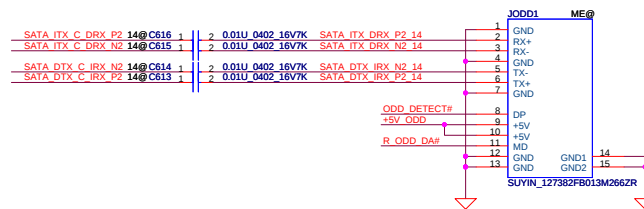
SATA HDD Conn.



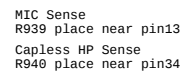
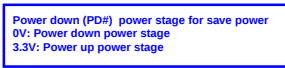
FOR 15"
SATA ODD FFC Conn.



FOR 14"
SATA ODD Conn.



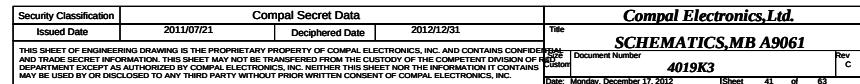
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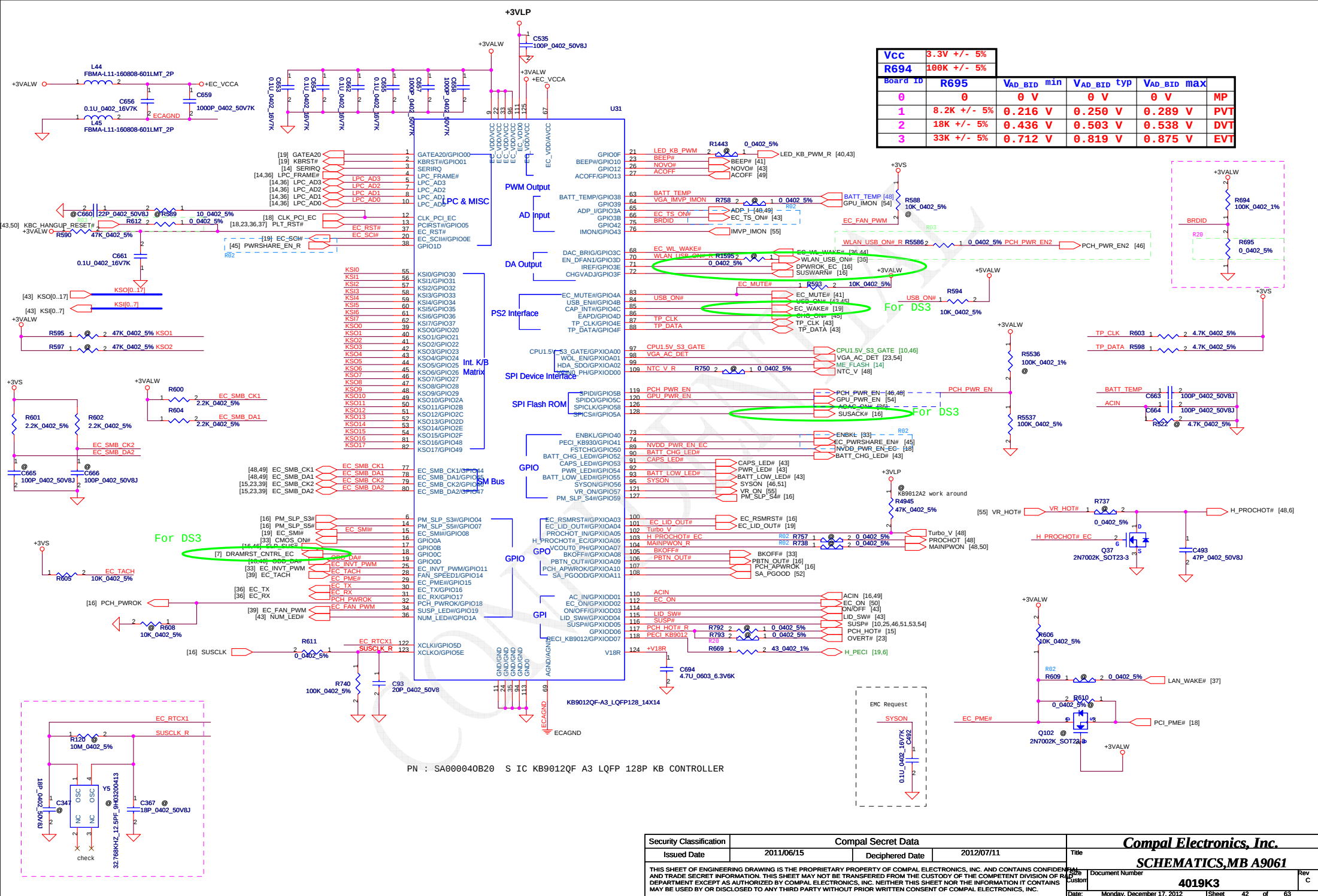


```
SPK L+L-R+R- trace width
Speaker 4 ohm ==>40 mils
Speaker 8 ohm ==>20 mils
```



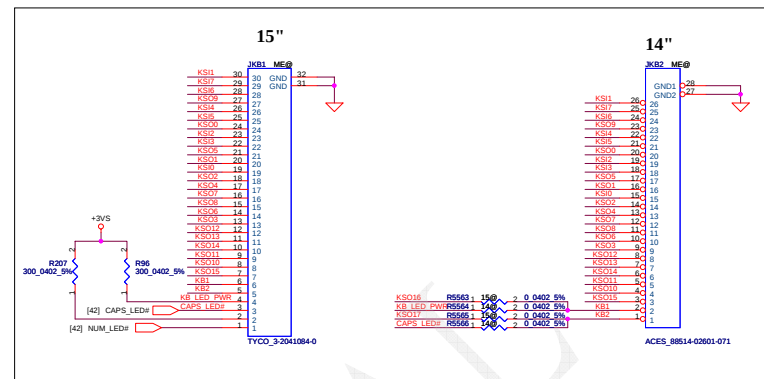
Combo Jack detect (normal open)





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Schematic diagram of the DAN202UT106_SCT0-3 component. The diagram shows a package with pins 1 through 4. Pin 1 is labeled 'NOVO BIT#'. Pin 2 is labeled 'D20'. Pin 3 is labeled 'ON/OFF BIT#'. Pin 4 is labeled 'ON/OFF'. Internal components include a resistor R642 (100K_0402_5%) connected to a +3V1W supply, a resistor R62 (100K_0402_5%) connected to a +3VLP supply, and a resistor R720 (100K_0402_5%) connected to a GND symbol. The component is identified as DAN202UT106_SCT0-3.

[illegible]

0_0402_5M

Pin	Signal
1	SMB_CLK_S3 R
2	SMB_DATA_S3 R
3	SMB_DATA_S3 R

Pin connection diagram for the PJS0T24C 3P C/A SOT-23 package. The package is shown with pins 1 through 10. Pin 1 is connected to +5VALW. Pin 2 is connected to +3VALW. Pin 3 is connected to SWR1. Pin 4 is connected to ME#. Pin 5 is connected to NOVO BIT#. Pin 6 is connected to OFFSET#. Pin 7 is connected to FIVE LSW#. Pin 8 is connected to LID SW#. Pin 9 is connected to GND. Pin 10 is connected to GND. The package is labeled @ D24 and PJS0T24C 3P C/A SOT-23. The diagram also shows a connection to ACES_S1524-00801-001.

[illegible]

Pin configuration diagram for the LED module:

- Pin 1: +5VALWO
- Pin 2: +3VALWO
- Pin 3: PWR_LED#
- Pin 4: BAT+ LOW LED#
- Pin 5: BAT+ CHG LED#
- Pin 6: GND
- Pin 7: GND
- Pin 8: GND

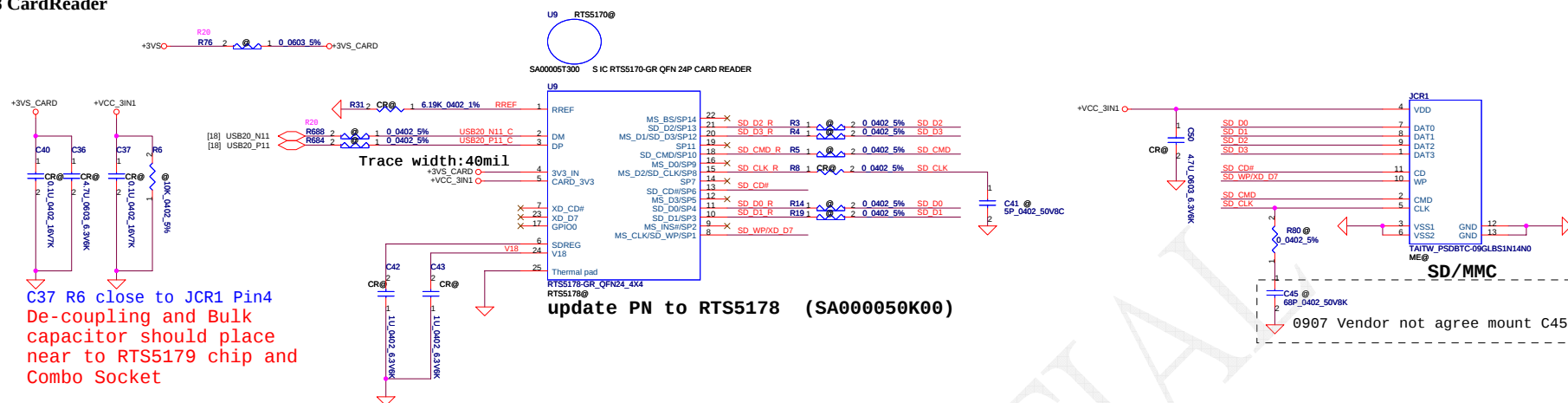
Module Label: LED1_ME@

Part Number: ACES_88514-00601-071

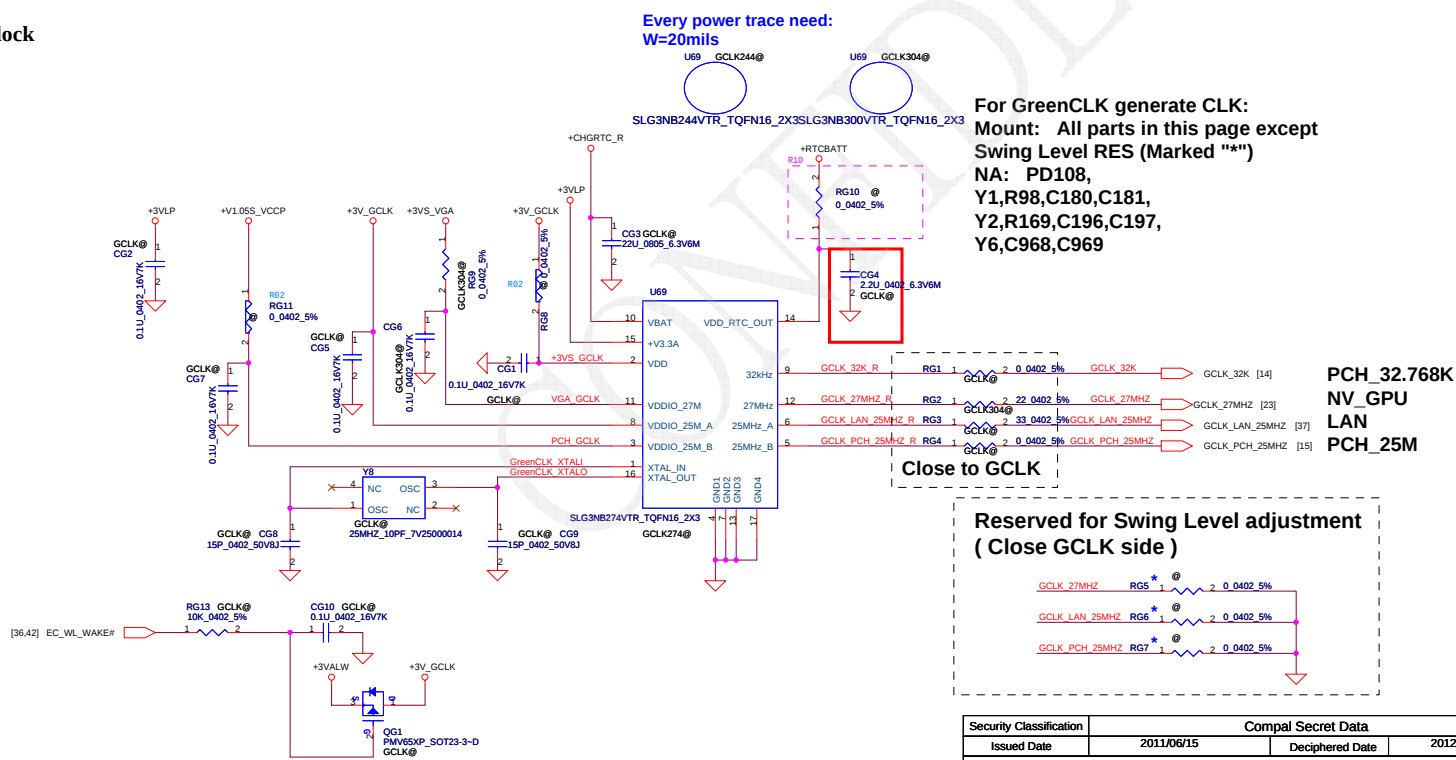
[illegible]

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Date: 2011/06/15 Time: 10:53				Date: 2012/07/11 Time: 10:53	Date: 2012/07/11 Time: 10:53

RTS5178 CardReader



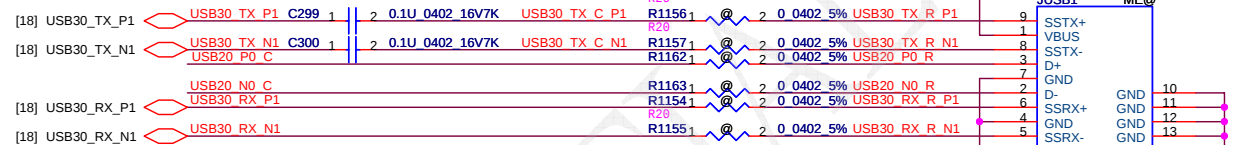
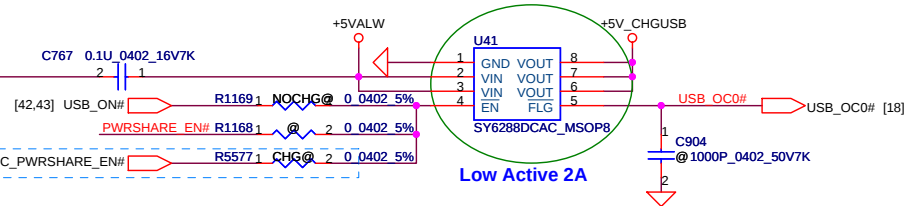
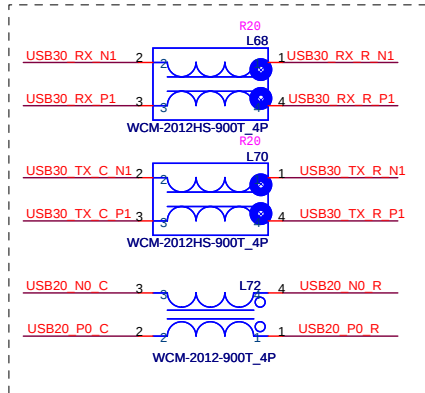
Green Clock



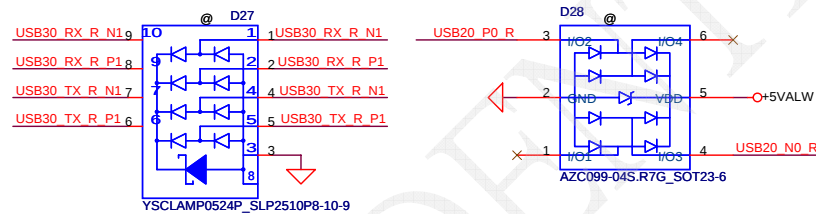
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LEFT SIDE USB3.0 PORT X1

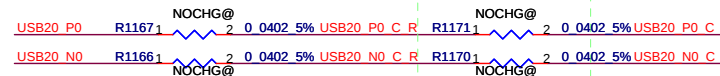
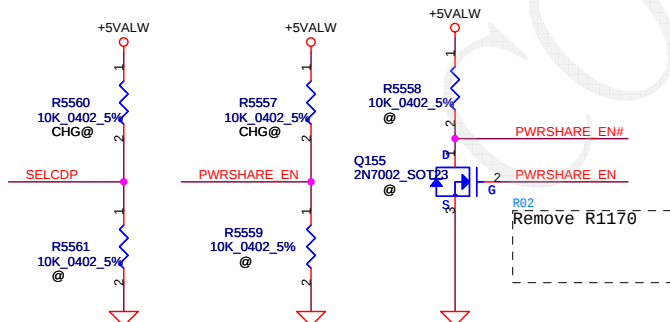
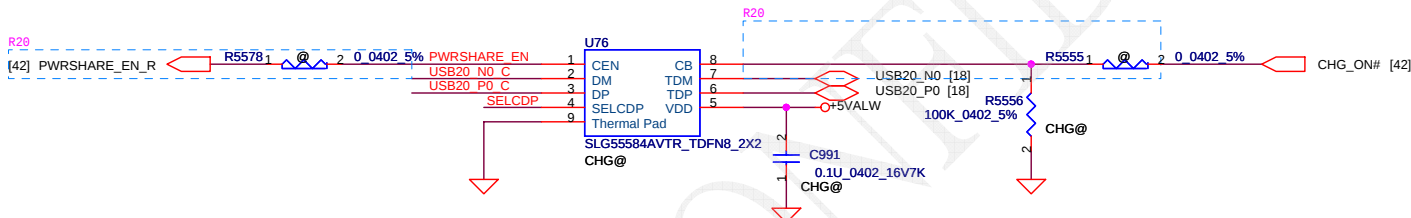
For EMI request
USB2.0 choke --> SM070000K00
USB3.0 Choke --> SM070001S00



For ESD request



Left Side Charger USB3.0 Port

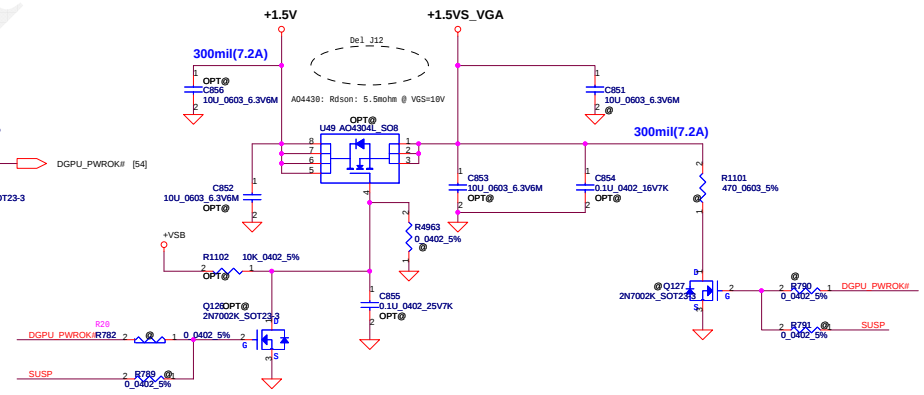
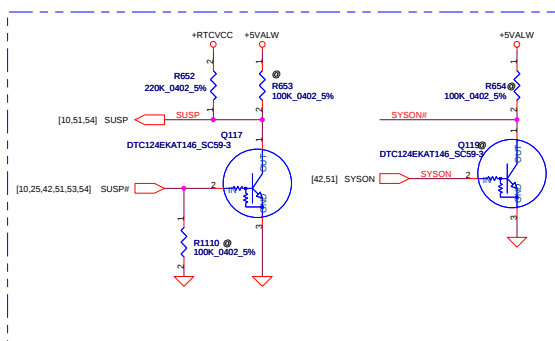
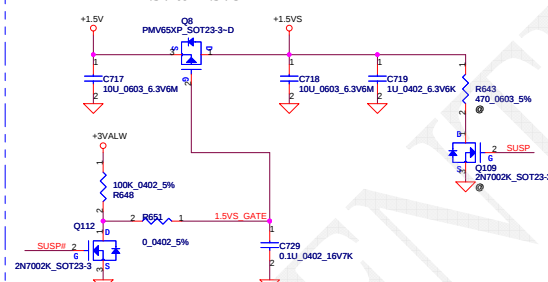
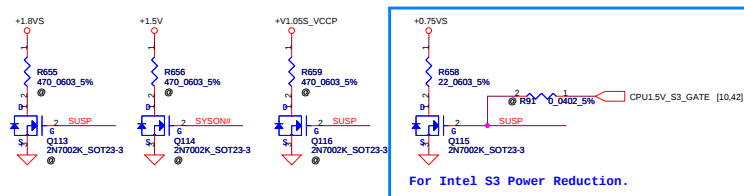
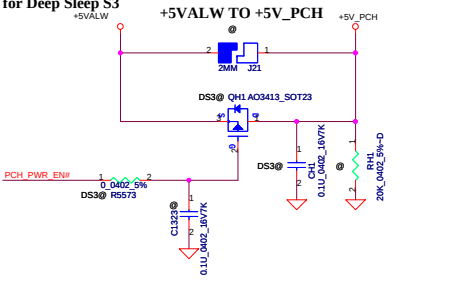
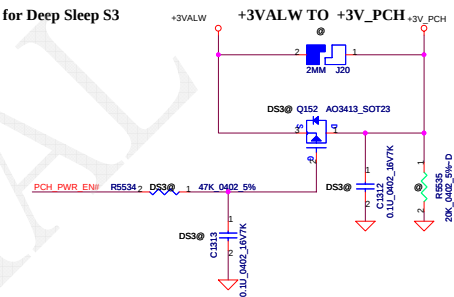
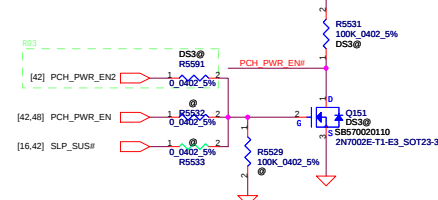
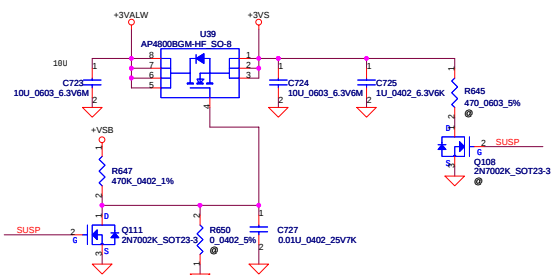
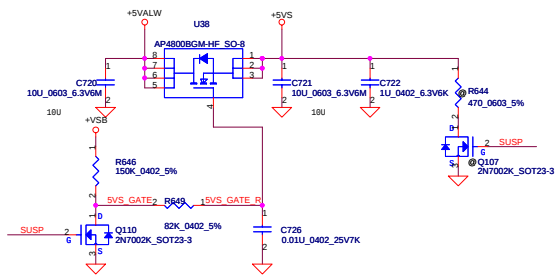


CB	SELCDP	Function
0	X	DCP autotetect with mouse /keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

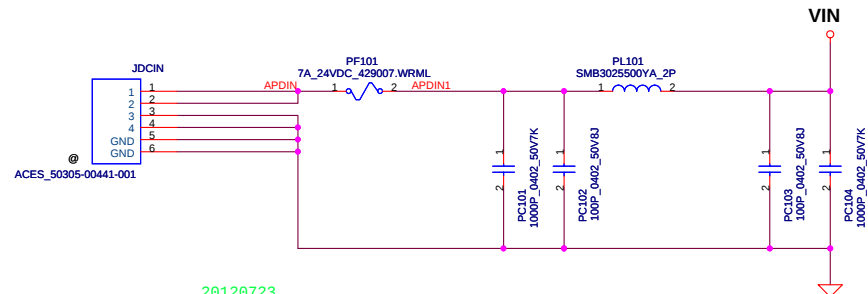
USB2.0/3.0 choke and ESD diode at sub-B.

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				Date: Monday, December 17, 2012	
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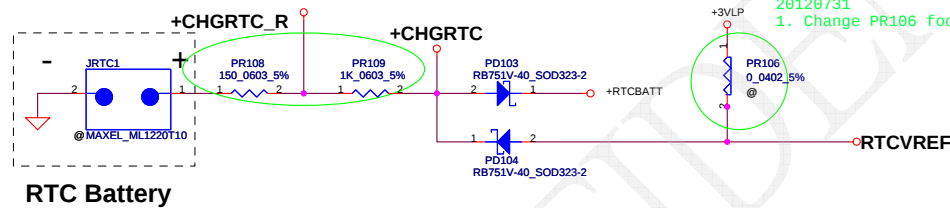
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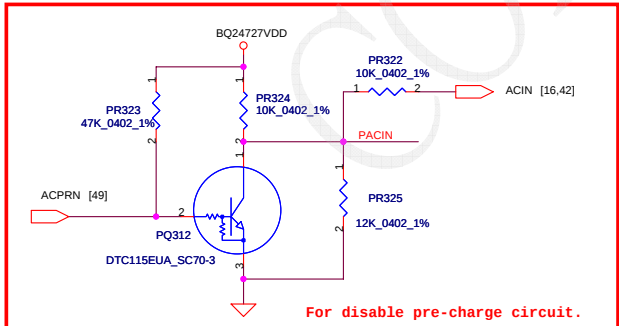
20120723
For all sku
1. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080
Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080



20120731
1. Change PR106 footprint to R0402_0ohm-NEW

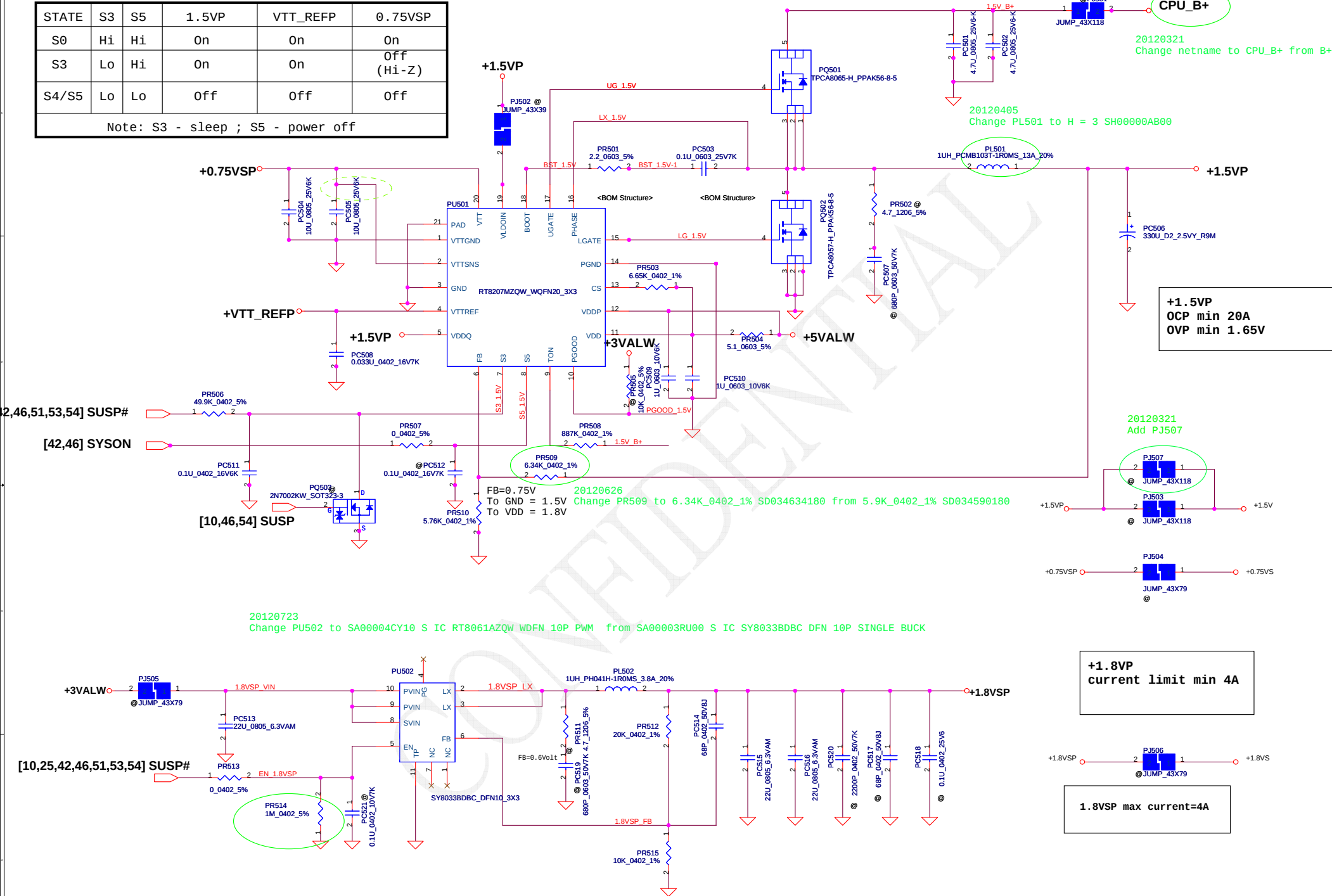
20120731
1. Add PR110 SD013000080 0_0603_5%
Add PR111 SD013150080 150_0603_5%

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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



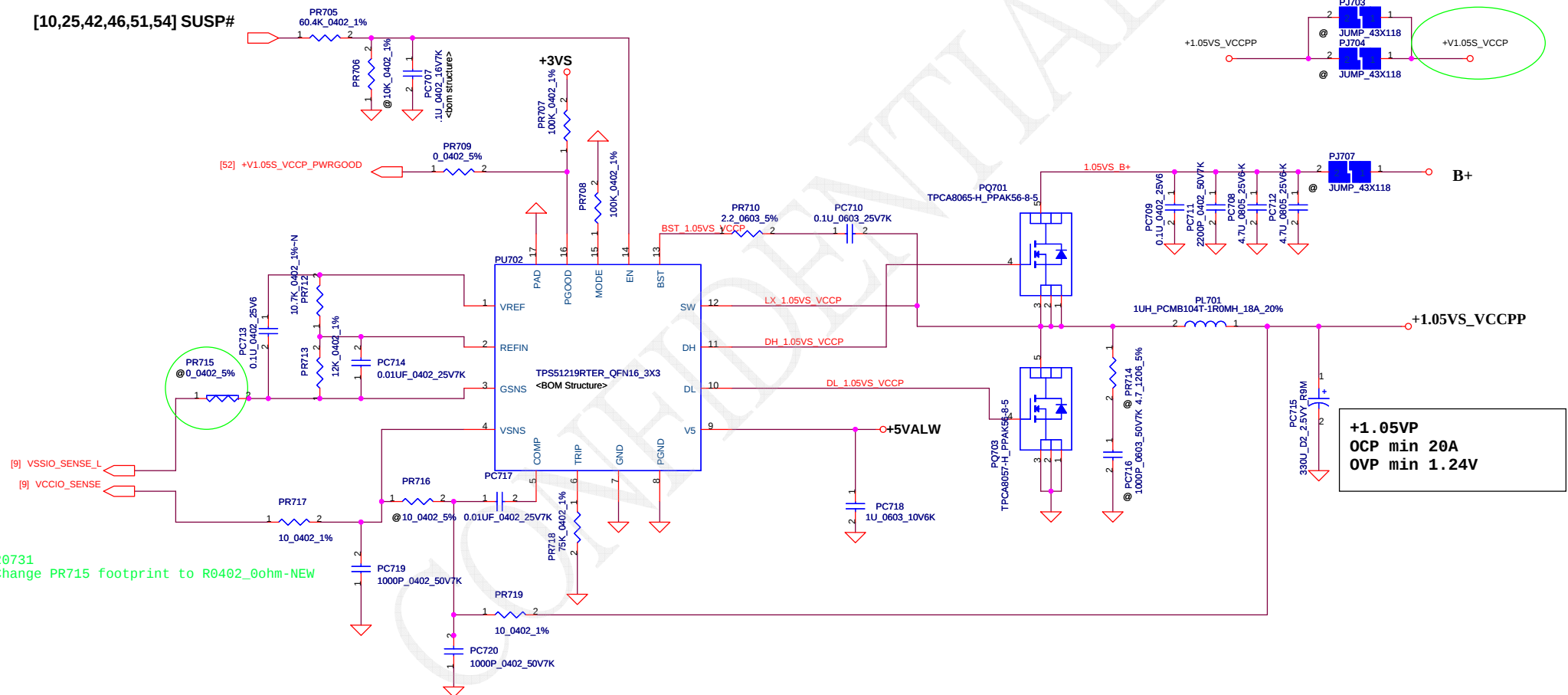
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output voltage adjustable network



[10,25,42,46,51,54] SUSP#

20120330
Change net name to +V1.05S_VCCP from +1.05S_VCCP



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20120514
Change PH901, PH904 to SL200000L00 220K_0402_5%_TSM08224J4702RE
from SL2000000500 220K_0402_5%_ERTJ0EV224J

PR915, PR946=200K(setting 113 degreeC)
PR915, PR946=8.25K(setting 93 degreeC)

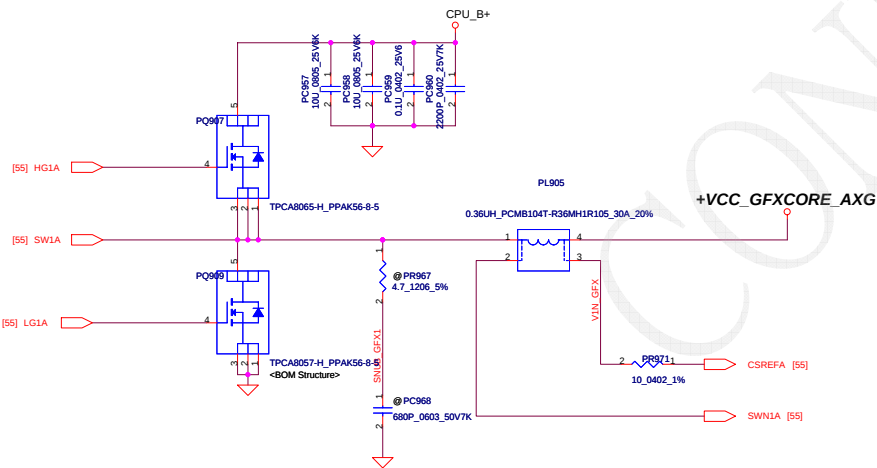
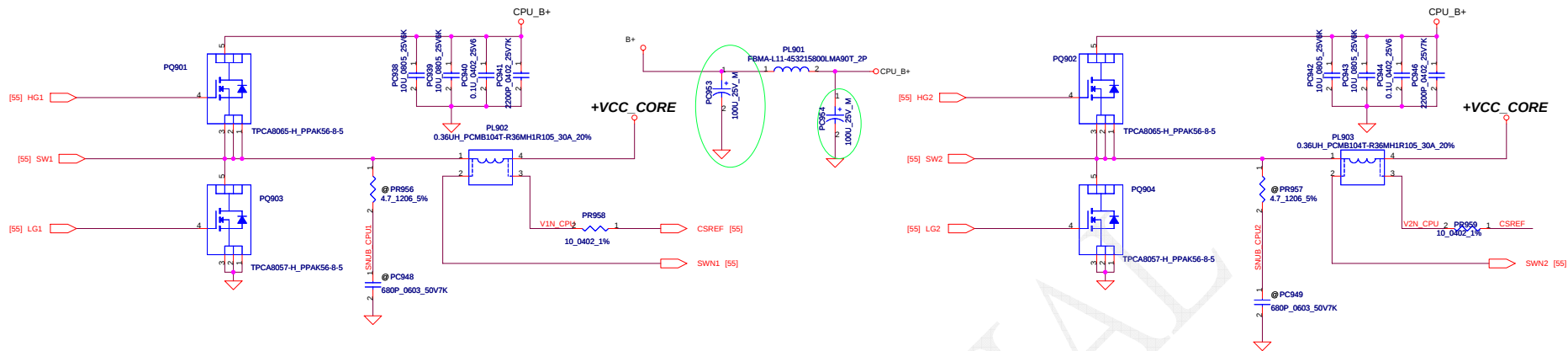
20120731
1. Change PR937, PR954, PR926, PR936, PR938
footprint to R6402_0ohm-NEW

20120514
Change PR921 to 71.5K_0603_1% SD014715280
from 63.4K_0603_1% SD014634280

20120514
Change PR949, PR951 to 143K_0603_1% SD014143380 from 130K_0603_1% SD014130380
20120514
Change PC936 to 1000P_0402_50V7K SE074102K80 from 680P_0402_50V7K SE074681K80

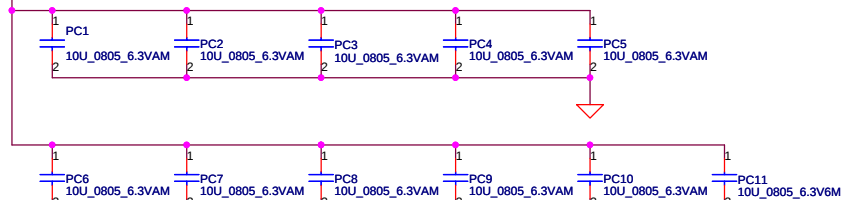
20120723
unmount PR915 and PR946

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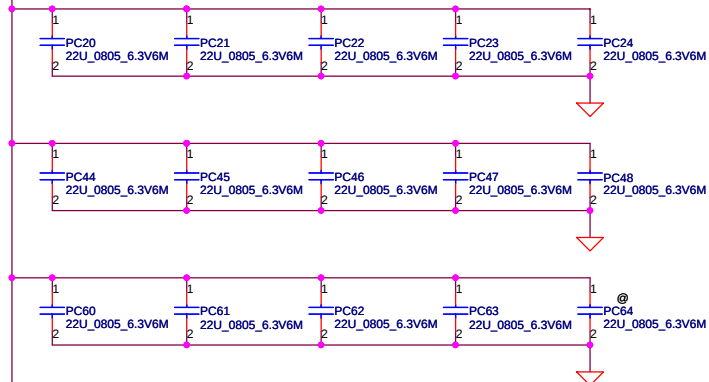


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				C38-G series Chief River Schematic	C
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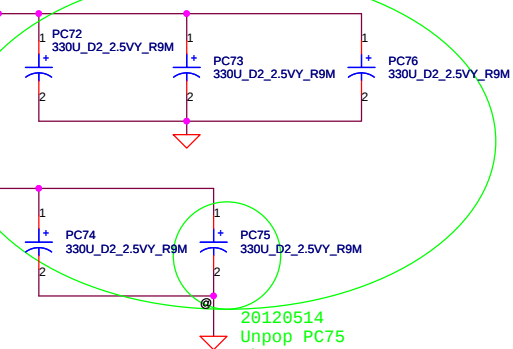
+VCC_CORE



+VCC_CORE



+VCC_CORE



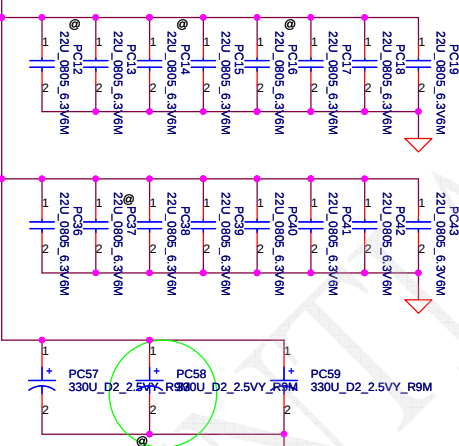
20120318
Change PC72,PC73,PC74,PC75 to 2 pin footprint

20120514
Unpop PC75
Change PC72,PC73,PC74,PC76 to SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680

+VCC_CORE

+VCC_GFXCORE_AXG

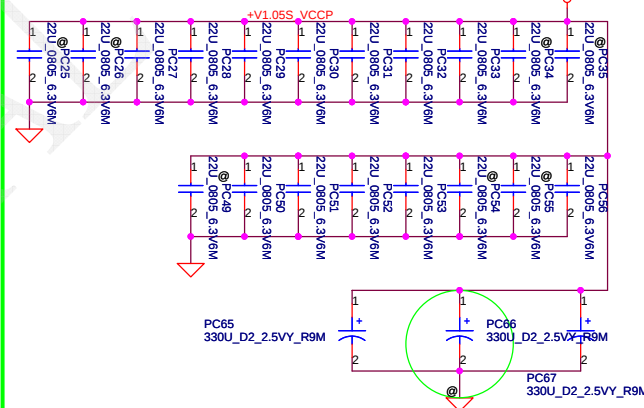
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP



20120514
Unpop PC66

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Item	Reason for change	PG#	Modify List	Date	Phase
1	For EC net name	P48	PR206 change pull high voltage to +EC_VCCA from +3VLP	20120316	EVT
2	Intersil advise	P54	1.Change PR848 to 1.47K SD000009480 from 1.15K 2.Unmount PC864	20120316	EVT
3	VGA IMON setting	P54	Change PR853 to 11K SD034110280 from 11.3K	20120316	EVT
4	set OCP is 56A	P54	Change PR869 to 1.58K (SD00000SJ80) from 1K	20120316	EVT
5	For 1.5V current	P51	Add PJ507 for 1.5V	20120321	EVT
6	For B+ layout	P55 P50 P51 P50	1.Change PC954 pull high to CPU_B+ from B+ 2.Change 3/5VALWP B+ input netname to CPU_B+ 3.Change 1.5VALWP B+ input netname to CPU_B+ 4.Change PR411 netname to CPU_B+ from B+	20120321	EVT
7	For HW net name	P53 P54	1.Change +1.05S_VCCP netname to +V1.05S_VCCP 2.Change PQ802.5 netname to +V1.05S_VCCP from +1.05VS	20120330	EVT
8	For HW power sequence	P54	1.Add control PU801 pin GPU_PWR_EN and reserve PR956 0_0402_5% 2.Change PR820 to SD034150380 150K_0402_1% from 100K 3.Change PC810 to SE071101J80 100P_0402_50V8J from 0.1u	20120330	EVT
9	For Intersil advise	P54	Change PR853 pull down netname to gnd	20120409	EVT
10	For IMON design	P55	Change PU901 to NCP6132A from ISL95836	20120412	EVT
11	For layout design	P54	1.Del PJ803 PJ804 2.Change net name to VGACORE from VGACOREP	20120511	DVT
12	For 1.05V, GFX_CORE,CPU_CORE design fine tune	P57	Unpop PC58, PC66,PC75 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
13	For CPU_CORE design fine tune and ON advise	P57	Change PC72,PC73,PC74,PC76 to S POLY C 330U 2V M D2 ESR9M SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
14	For CPU_CORE design fine tune and ON advise	P55	1.Change PC928 to 560P_0402_50V7K SE074561K80 from 680P_0402_50V7K SE074681K80 2.Change PR949,PR951 to 140K from 130K 3.Change PR912 to 71.5K_0603_1% SD014715280 from 63.4K_0603_1% SD014634280 4.Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
15	For material EOL	P55	Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
16	For HW VGA power sequence	P54	Add PR972 SD028000080 0_0402_5% Unmount PD801 Change PR820 to 0_0402_5% SD028000080 from 150K_0402_1% SD034150380 Unmount PC810	20120516	DVT

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Item	Reason for change	PG#	Modify List	Date	Phase
17	For HW reset function	P50	1.Add PR420 SD028000080 0_0402_5% for reserve 2 reserve.PR419 and PR420	20120606	PVT
18	For ACDET function	P49	1.Change PR313 to 60.4K_0603_1% SD014604280 from 64.9K_0603_1% SD014649280	20120615	PVT
19	For HW Grenn clock UMA sku trial tun	P47	1. unmount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120625	PVT
20	For ACDET function	P49	1.Change PR313 to 59K_0603_1% SD014590280 from 60.4K_0603_1% SD014604280	20120705	PVT
21	For VR_HOT	P55	1.unmount PR915 and PR946	20120705	PVT
22	For HW Grenn clock	P47	1. mount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120723	SVT
23	For material issue	P51	1.Change PU502 to SA00004CY10 S IC RT8061AZQW WDFN 10P PWM from SA00003RU00 S IC SY8033BDBC DFN 10P SINGLE BUCK	20120723	SVT

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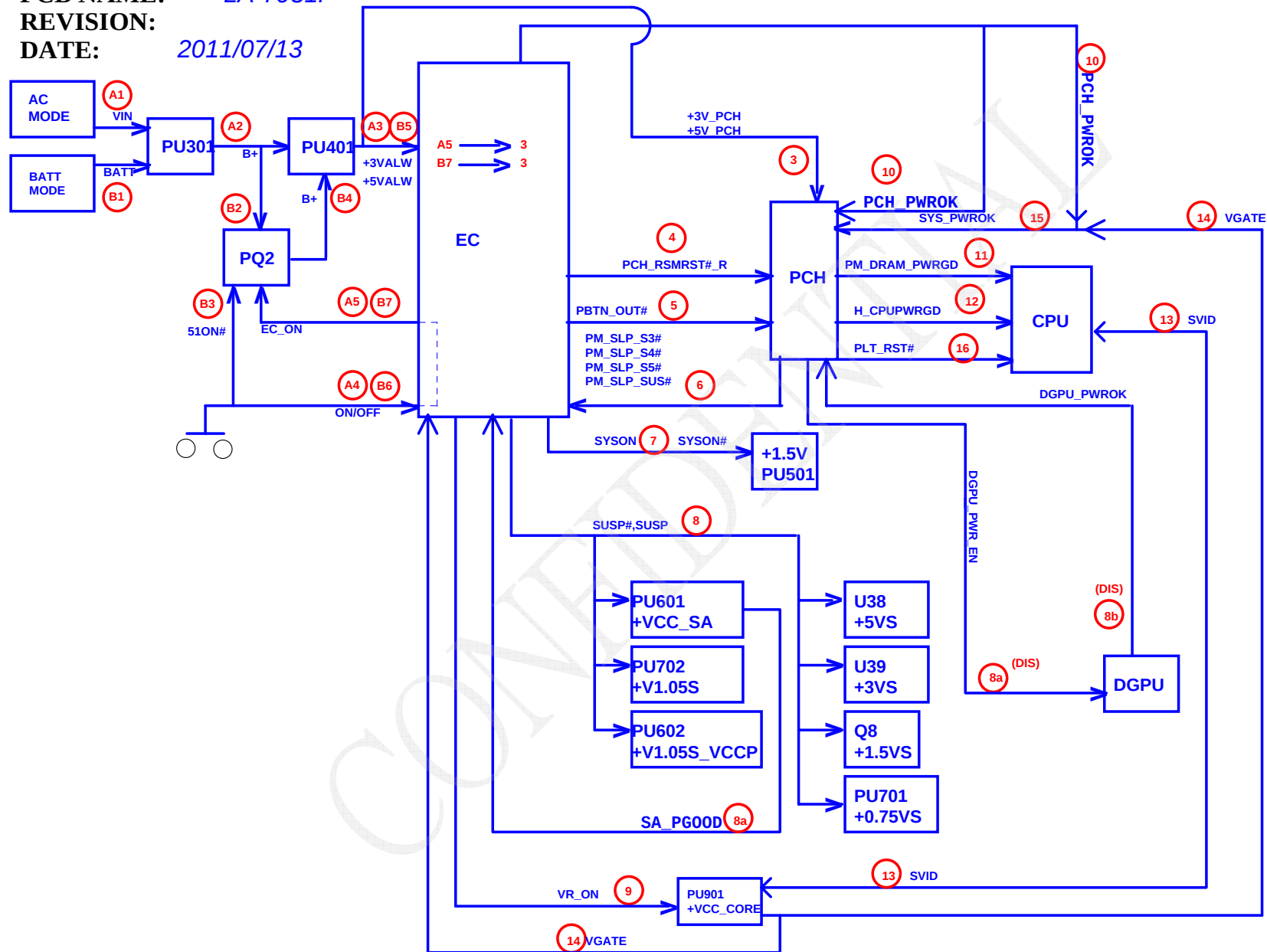
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: *LA-7981P*

REVISION:

DATE: *2011/07/13*



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Version change list (P.I.R. List)

Page 1 of 2 for HW PIR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial			5/7	DVT
2	For Green CLK and Crystal co-lay better layout	P14 P15 P23	Delete R176,R1381 and RV232	5/7	DVT
3	For Change Audio Woofer MOSFET from Dual to single channel	P15	Changer Part from SB000000E010 to SB000000EN00	5/7	DVT
4	For OVERT# Glitch issue at Power on status	P23	Add QV9	5/7	DVT
5	For BT&WLAN Combo Card	P36	to modify R897 value from 0 ohm to 1K ohm add BT_DISABLE_F_R on JWLN1.51 add R5580	5/8	DVT
6	For Factory request and cost down LVDS PIN Define	P33	To Modify LVDS PIN Define	5/8	DVT
7	For USB Charger mode control request	P45 P42	To Add PWRSHARE_EN_R on U31.38 To Add EC_PWRSHARE_EN# on U31.74 add R5577 and R5578, delete CHG_ON#	5/8	DVT
8	To change Reset IC G601	P42	to change R4959 value from 200K ohm to 0 ohm add R5579 0 ohm	5/8	DVT
9	Reserved Touch Screen Power Control	P42 P43	add R5581,C1331,R5572,R5583,R5584 and Q156 add EC_TS_ON on U31.66 add +3VS_TS,+3VS_TS_R	5/8	DVT
10	To change Speaker PIN define for ME routing request	P41	SPK_L2+ R1556 net in JSPK1.1 SPK_L1- R1554 net in JSPK1.2 SPK_R1- R1555 net in JSPK1.3 SPK_R2+ R1553 net in JSPK1.4	5/8	DVT
11	for Realtek Vendor recommand	P41	R1123,C1134 close to U50.47 R5582,R1559 and C1135 Close to U73.1 EXT_MIC_R	5/8	DVT
12	for ME request	P39	To Modify H21,H7,H18 PCB Footprint as below H21 from H_3P3 to H_4P6 H7 from H_2P8 to H_3P0 H18 from H_3P3 to H_3P9N	5/8	DVT
13	for LAN Clock be better	P37	change C990 value from 5PF to 0 ohm.	5/9	DVT
14	for Audio Vendor recommand	P43	change JUSB3.11 from GND to +3VS change JUSB3.12 from +3VS to AGND	5/10	DVT
15	for Crystal finetune Capacitor	P43	C180,C181 from 18PF to 12PF	5/16	DVT
16	for DVT Board ID request	P42	R695 from 33K to 18K	5/17	DVT
17	for PVT request	P37	Change Reference from C990 to R5585	5/23	PVT
18	for Surge request	P38	C1325,C1326,C1327 change package from 0402 to 0603	5/23	PVT
19	for Reset IC function	P42, P50,P43	add R612,PR420,R4960,R4961 Delete R4959	5/24	PVT

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Item	Reason for change	PG#	Modify List	Date	Phase
20	for USB2.0 Port 0 TLC fine tune	P45	add R1170,R1171	5/29	PVT
21	for INTEL Combo card BT off	P36 P19	add R893,R894 1Kohm ,change R897 to 0 ohm change net name from PCH_GPI036 to INTEL_BT_OFF# add INTEL_BT_OFF#_R JWLN1.51 chnage NET from BT_DISABLE_F_R to INTEL_BT_OFF#_R	6/5	PVT
22	for LVDS prevent short EC DISPOFF#	P33	R447 change value from no stuff to stuff 0ohm	6/12	PVT
23	for VSB and PCH Power rail control issue	P42 P46	add R5586 and R5591	6/21	PVT
24	add common choke for USB port 8, port 9	P43	add L78, L79, R5587, R5588, R5589, R5590	6/21	PVT
25	no need reserved C1330	P38	remove C1330	6/21	PVT
26	for PVT Board ID request	P42	R695 from 18K to 8.2K	6/21	PVT
27	for Surge modify	P38	DL6 change Part from SCV00001C00 to SCV00001D00	6/21	PVT
28	for Crystal finetune Capacitor	P14 P37	C180,C181 change value from 12P to 18P C1204,C1205 change value from 27P to 12P	6/25	PVT
29	for SMT Request	P23	LV7 change value from KC_FBMA-10-100505-300T_2P to 0ohm_0402	07/11	SVT
30	for Vendor recommand	P23	add RG10 0ohm	07/19	SVT
31	for Touch Screen request	P43	add R5592,R721 0 ohm,	07/25	SVT
32	for Green CLK request	P44	add QG1,RG13,CG10	8/1	SVT
33	for LED Brightness	P44	modify R623,R765 value from 300 ohm to 560 ohm	8/1	SVT
34	for reduce component count	P10 P	Modify footprint to jumper R69 to J14 R277 to J16	8/1	SVT
35	for SVT Board ID request	P42	R695 from 8.2K to 0 ohm	8/1	SVT

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