

COMPAL CONFIDENTIAL

MODEL NAME : NAL60
PCB NO : LA-5691P (DAA00001K00)
BOM P/N : 43178731L01/43178731L02



笔记本技术联盟
www.bblianmeng.com

M10 Lafite
BGA Arrandale (34 x 28 mm) +
SFF IBEXPEAK-M

2009-07-07
REV : 0.1(X00)

@ : Nopop Component

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN,TPM EN	43178731L01	SV 2.4G	*			*	*		1@,4@,5@
BLT EN,TPM EN	43178731L02	SV 2.0G	*		*			*	1@,3@,6@
BLT DIS,TCM EN	43178731L03	LV 1.8G		*		*	*		2@,4@,5@

MB PCB	
Part Number	Description
DAA00001K00	PCB QAW LA-5691P REV0 M/B

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Title

Cover Sheet

Size

Document Number

LA-5691P

Rev

0.1

Date

Monday, July 13, 2009

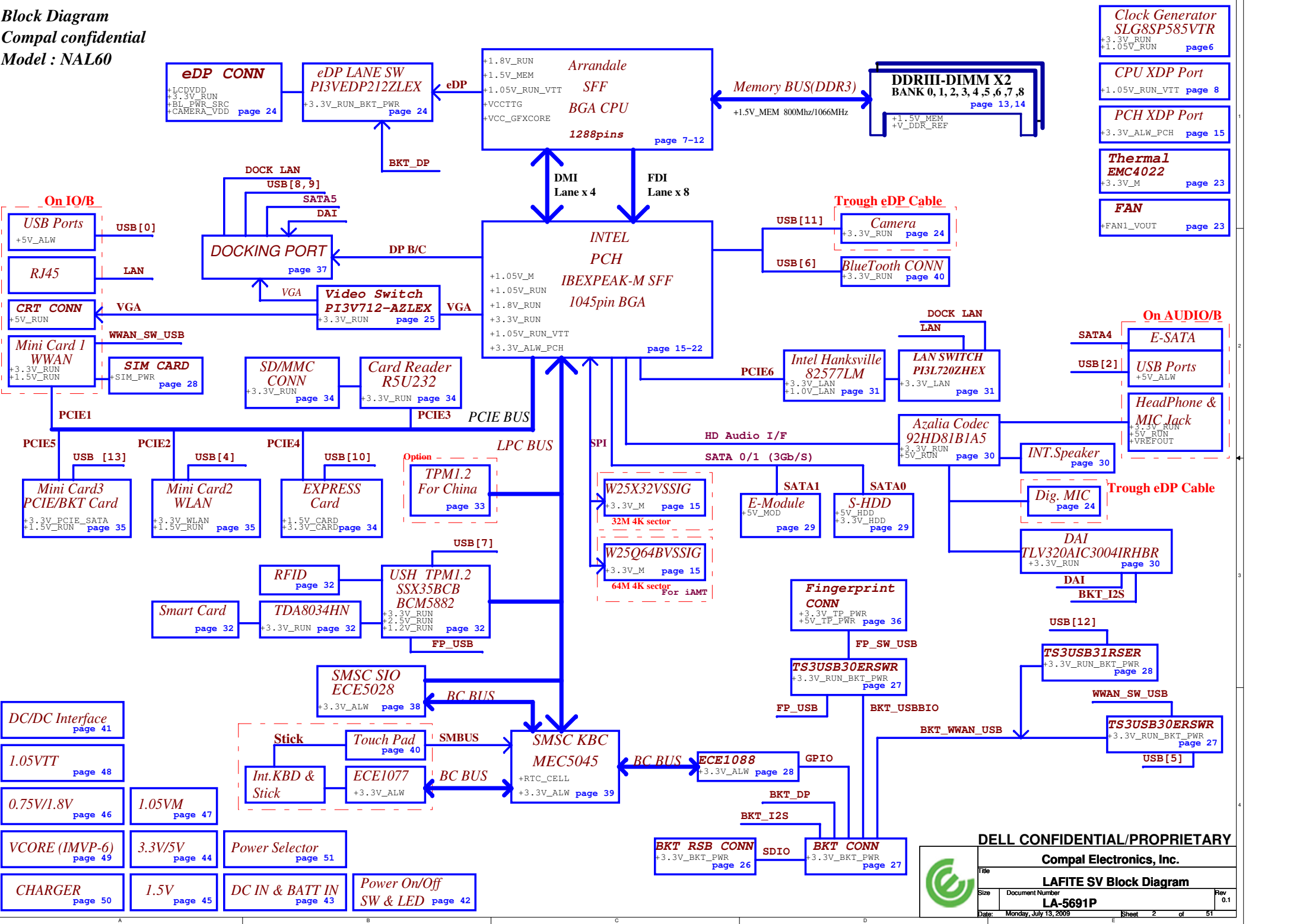
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Block Diagram
Compal confidential
Model : NAL60



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LAFITE SV Block Diagram

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

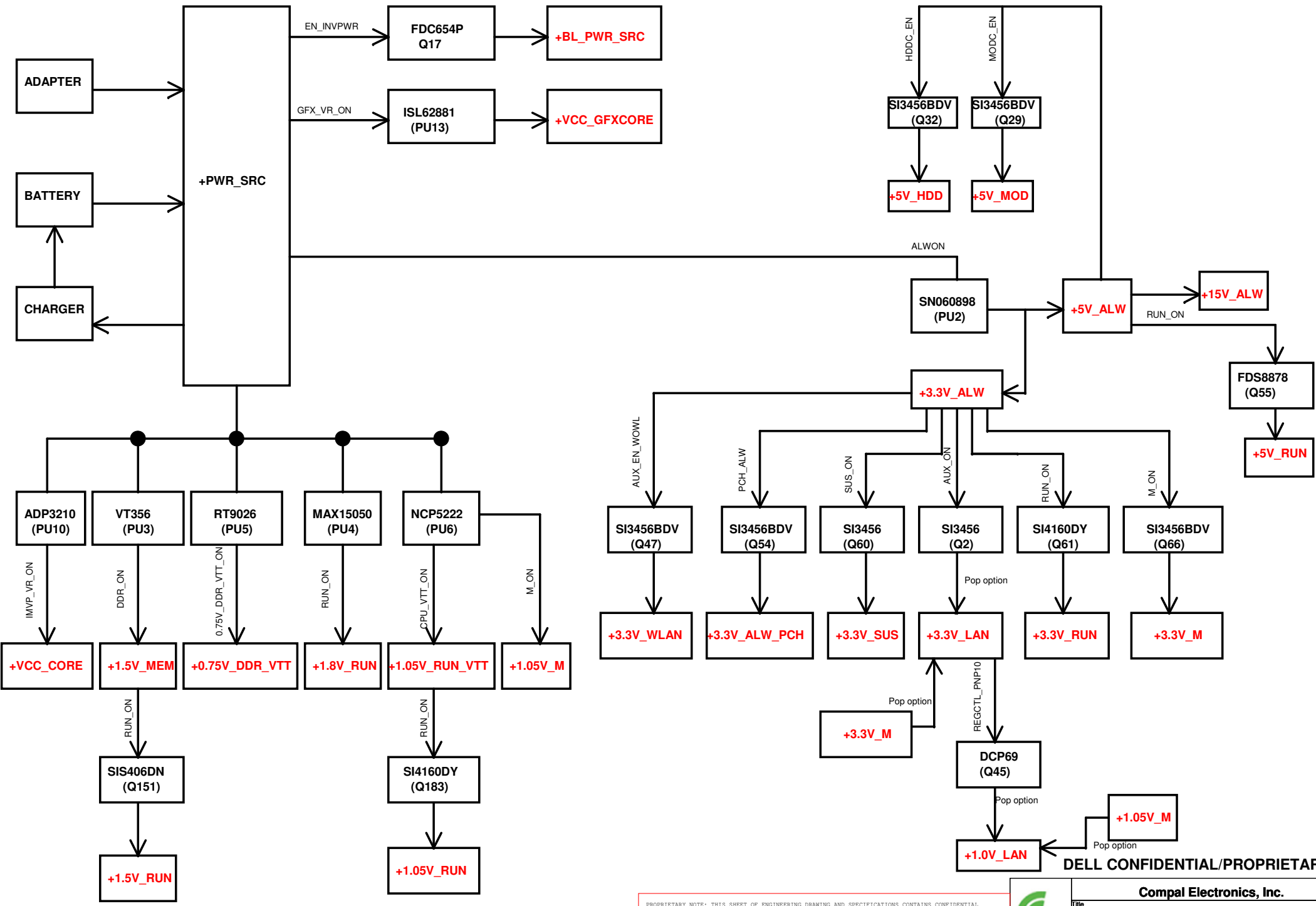
PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side)
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
	13	WPAN/NVMHCI

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

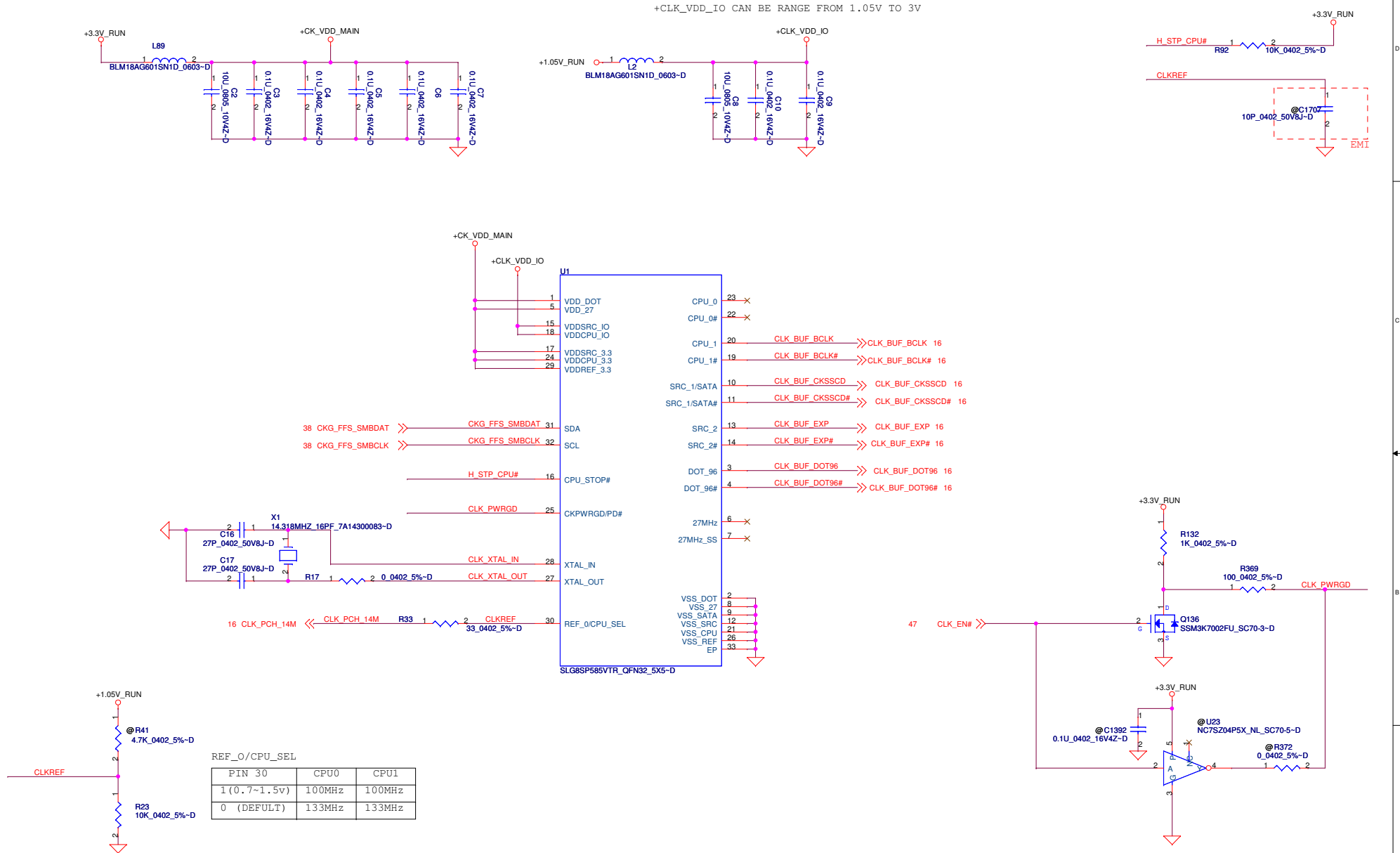
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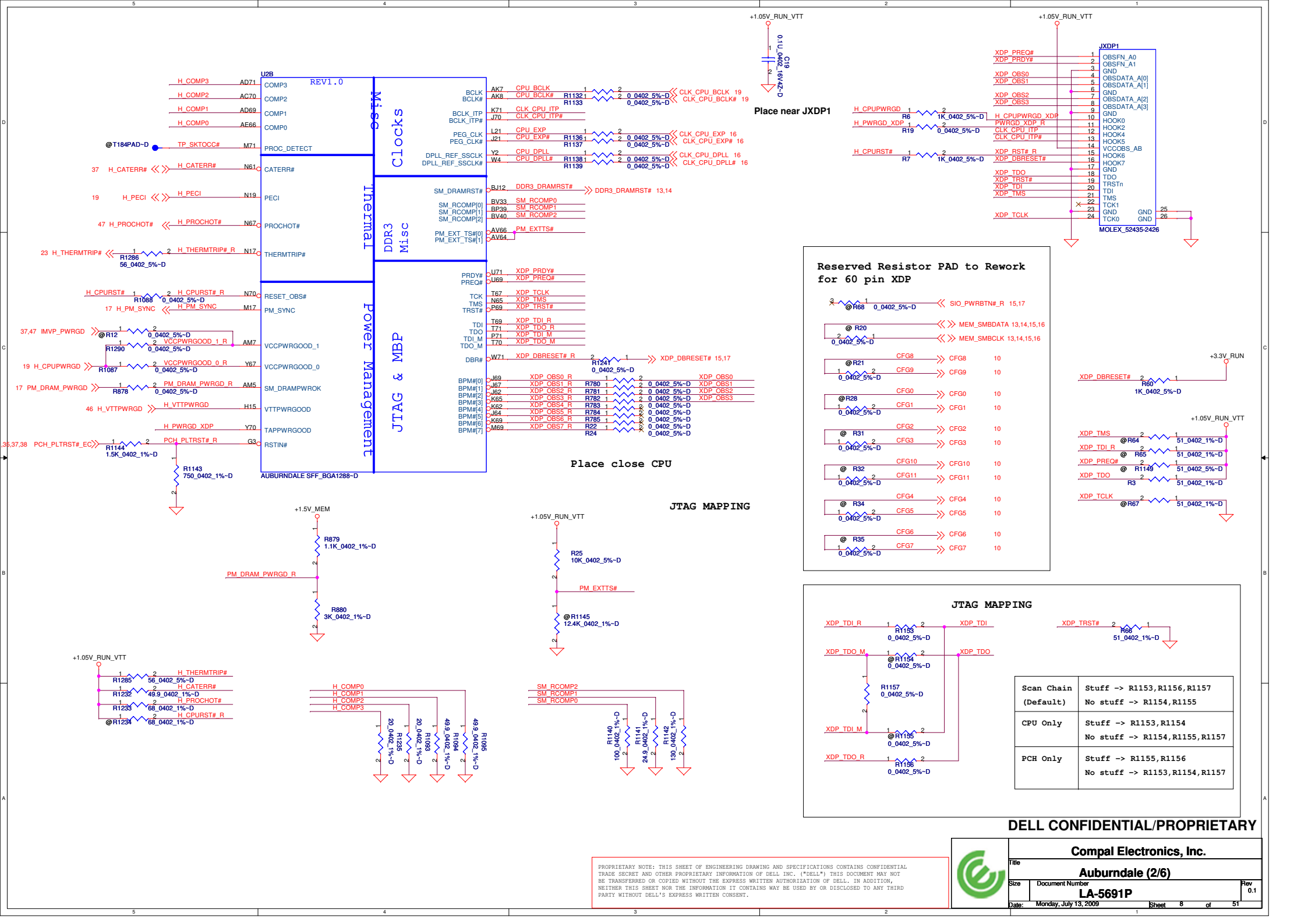
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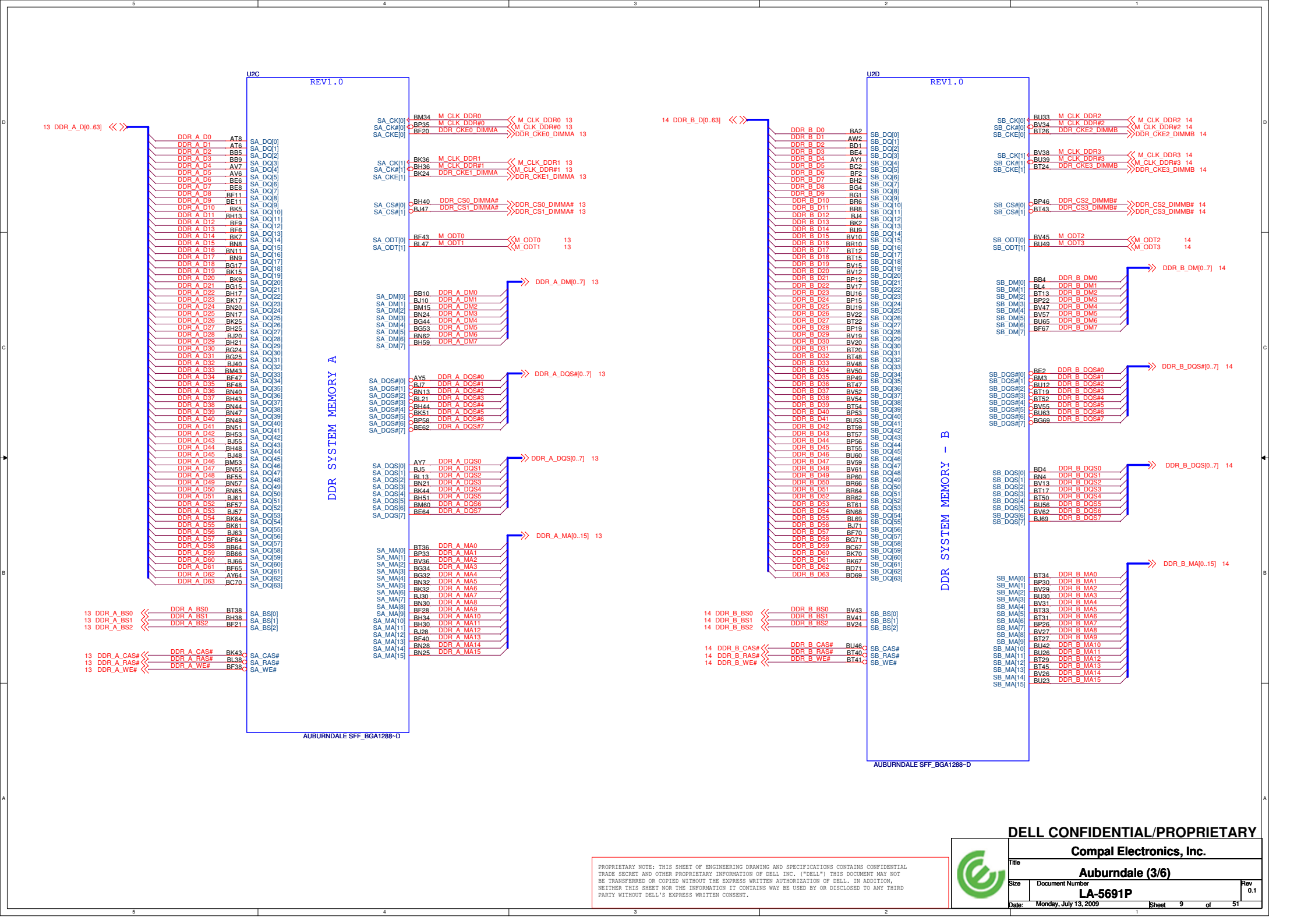


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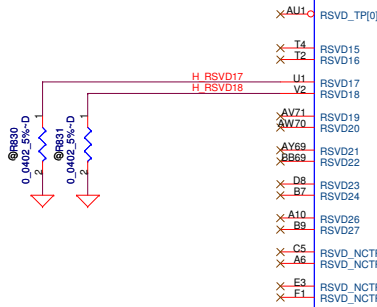
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Clock Generator			
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Reserve VIA on PCB



AUBURNDAL SFF_BGA1288-D

RESERVED

Package Daisy Chain:

- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
- 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
- 3: A5 - pkg - C3
- 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5

PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable

PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...

Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

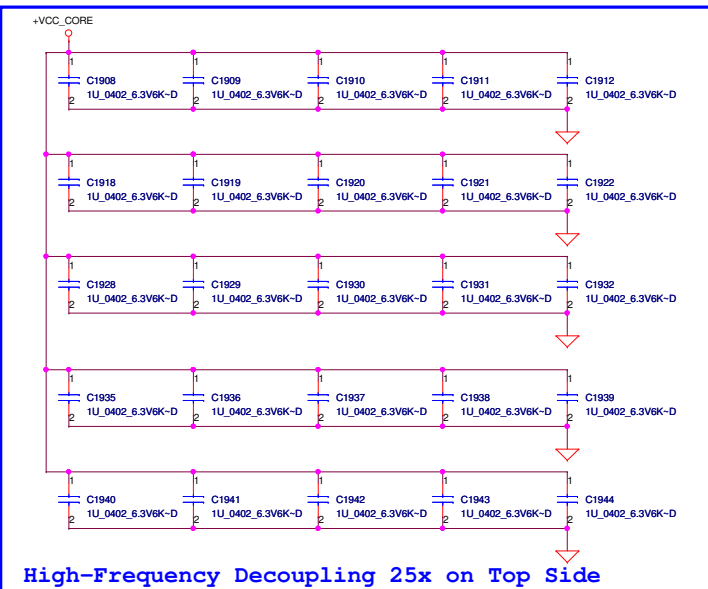
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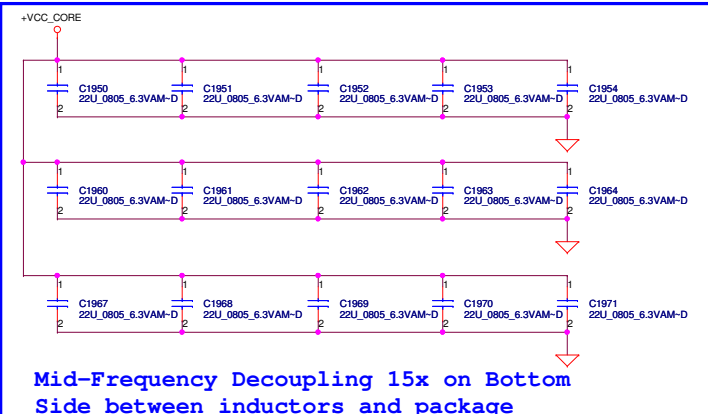
Auburndale (4/6)

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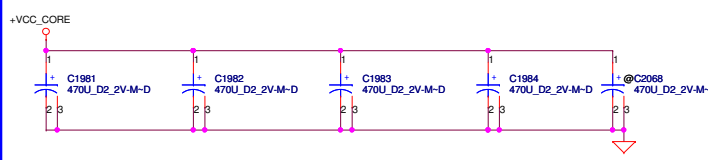
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High-Frequency Decoupling 25x on Top Side

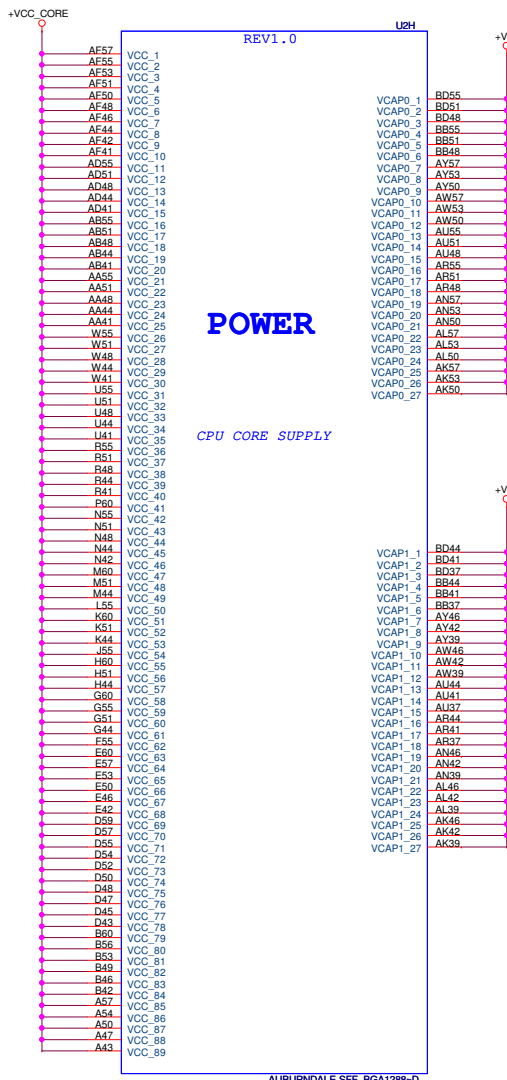


Mid-Frequency Decoupling 15x on Bottom Side between inductors and package



Low-Frequency Bulk 4x on Bottom Side, 1x on Top

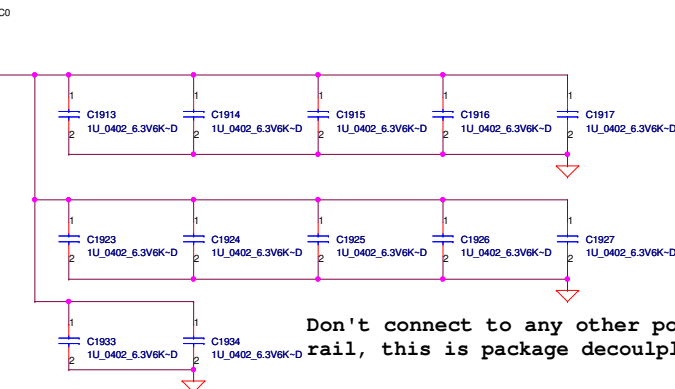
Current =48A



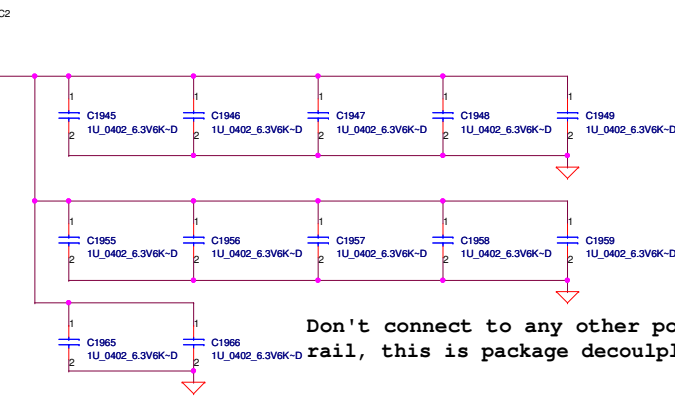
POWER

CPU CORE SUPPLY

AUBURNDALD SFF_BGA1288-D



Don't connect to any other power rail, this is package decoupling



Don't connect to any other power rail, this is package decoupling

PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VXMG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

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Auburndale (5/6)

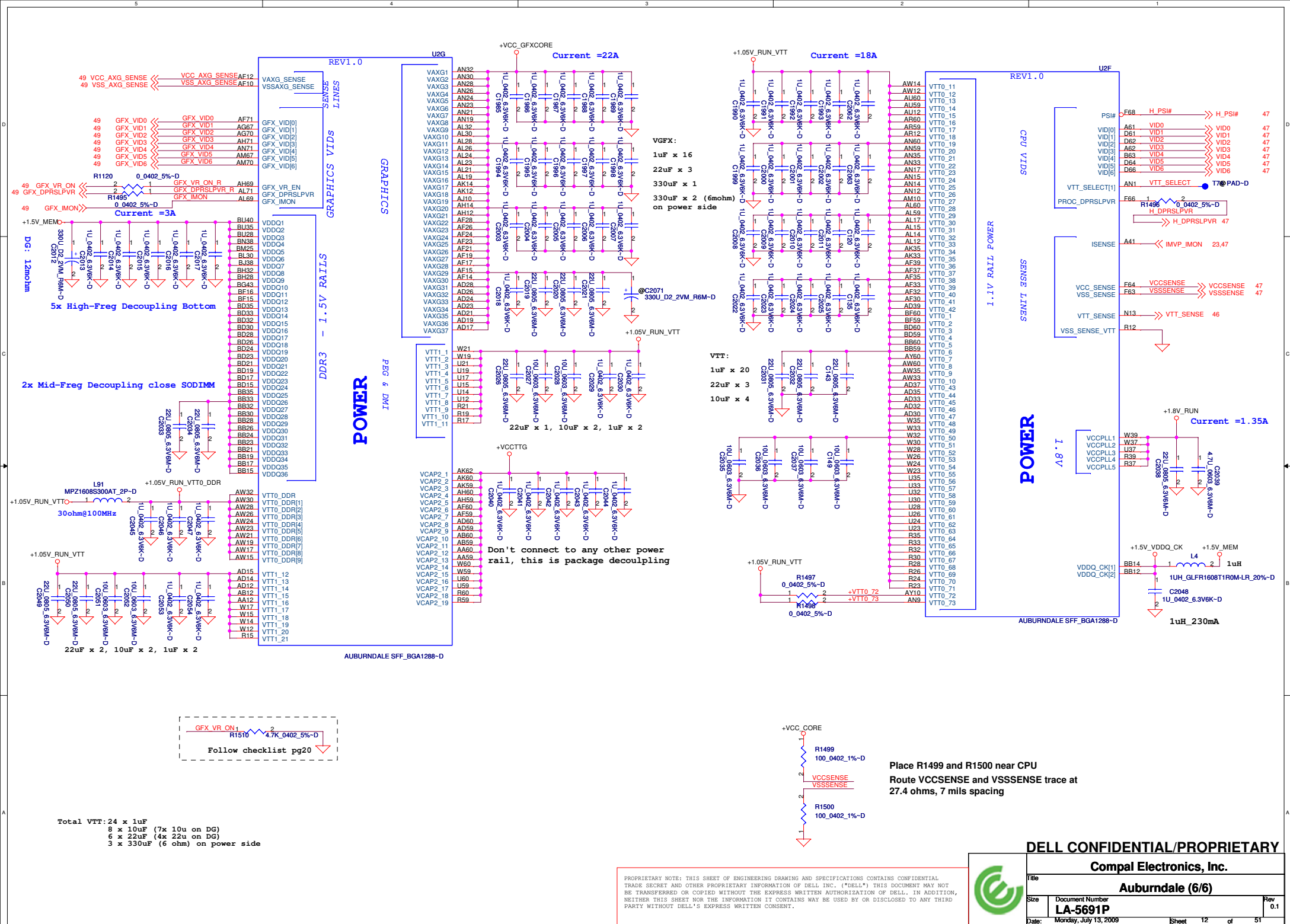
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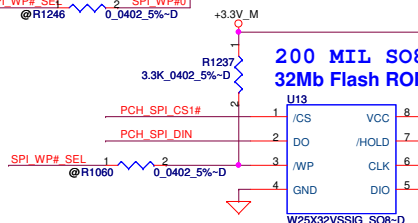
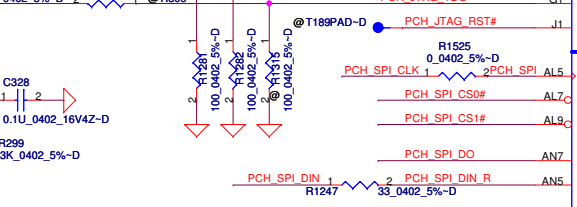
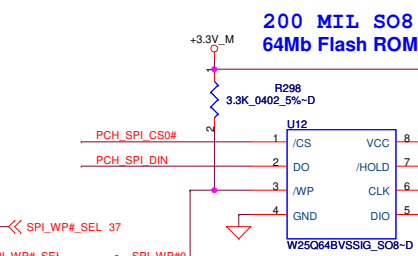
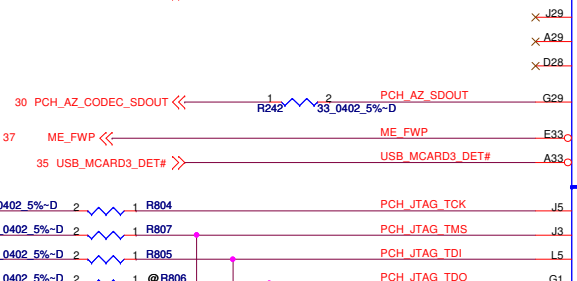
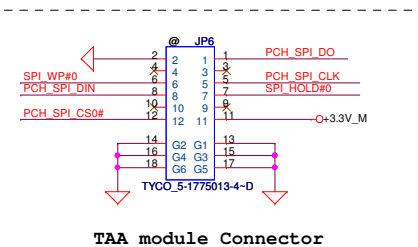
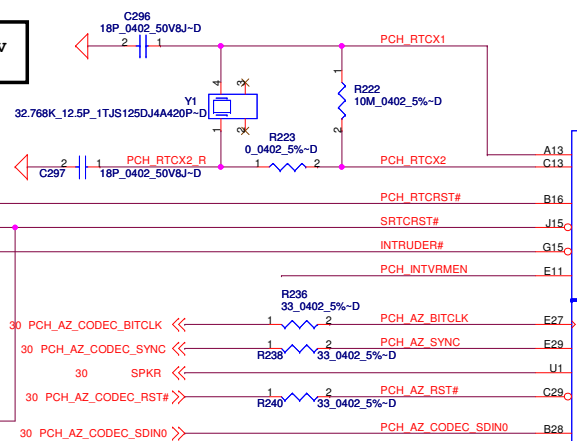
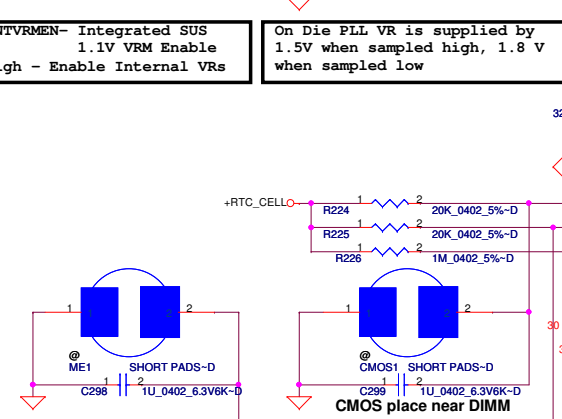
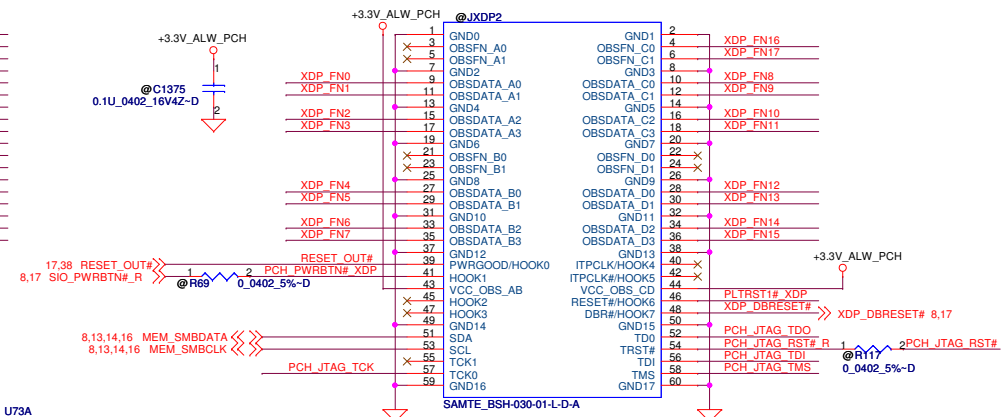
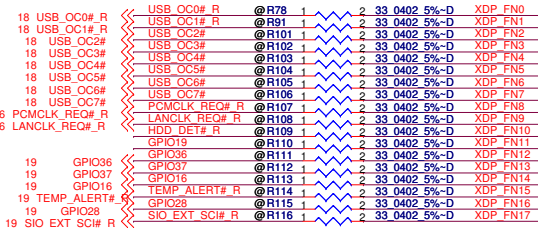
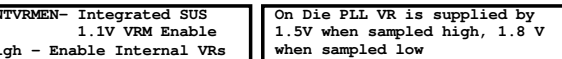
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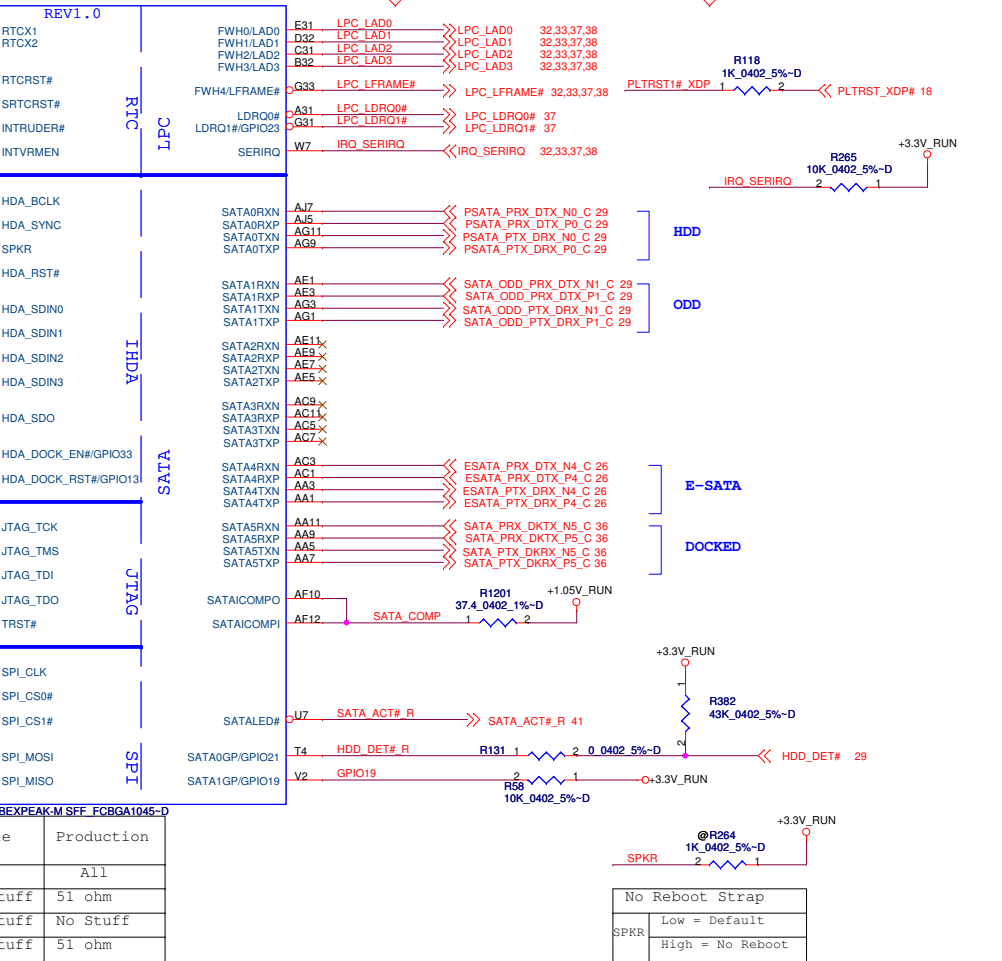
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ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	All
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	
	R1316	10K ohm	10K ohm	No Stuff	No Stuff	



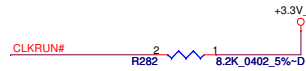
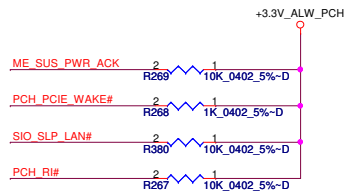
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DMI Lane Number Reversed

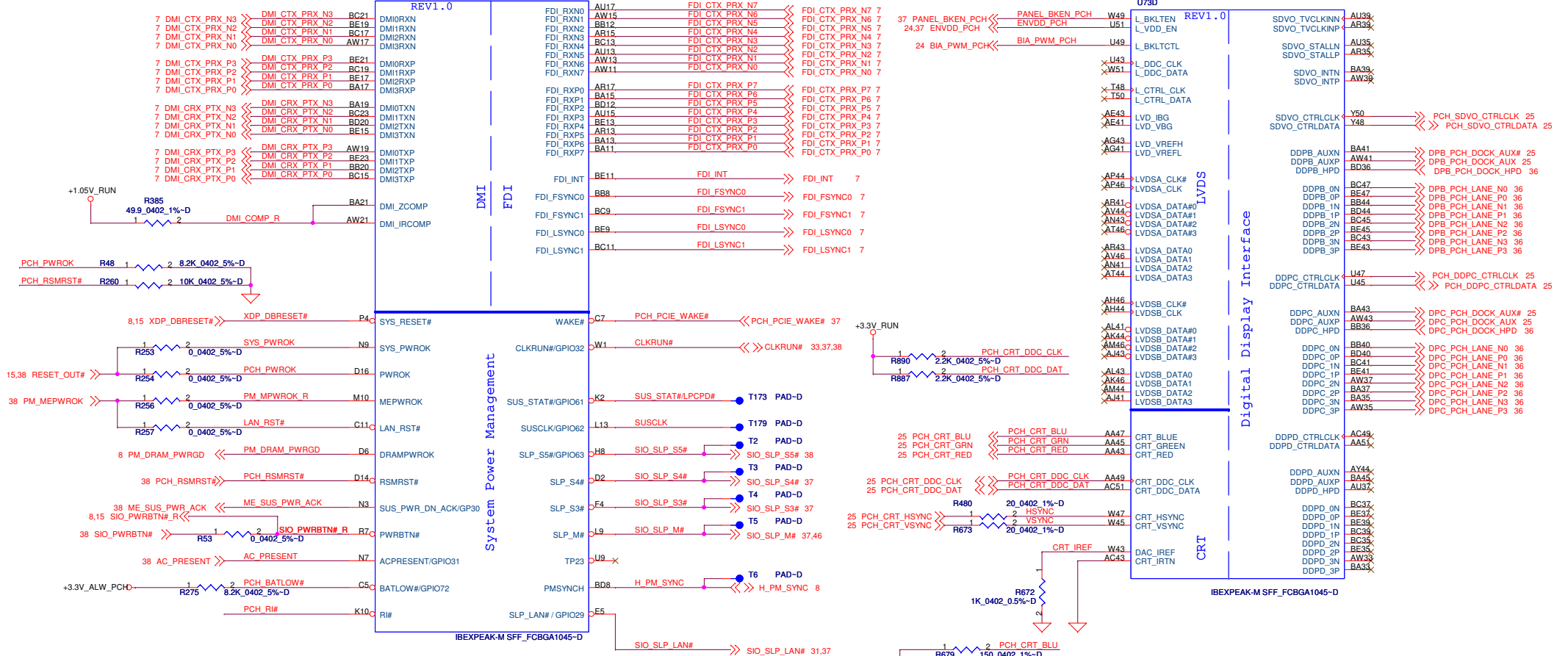
U73C

REV1.0

FDI Lane Number Reversed

U73D

REV1.0

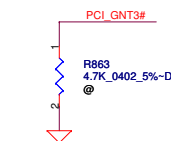
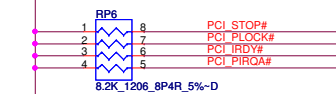
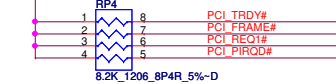


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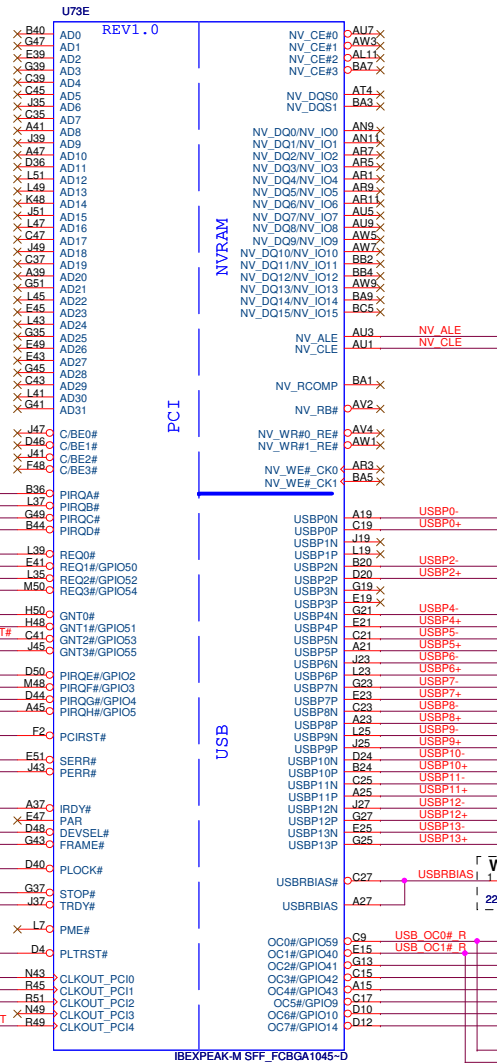
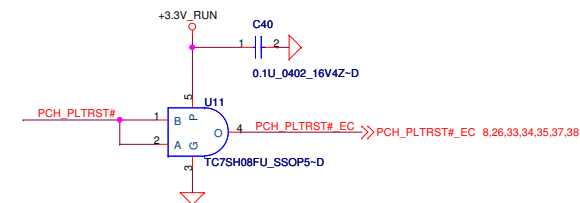
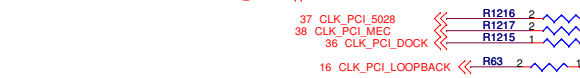
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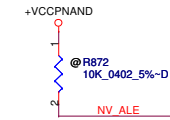
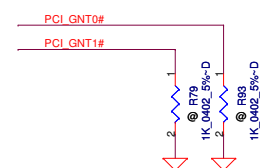
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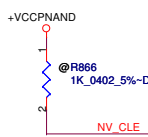
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



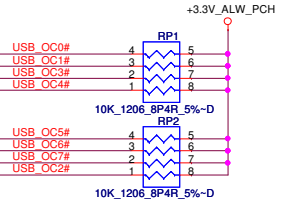
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

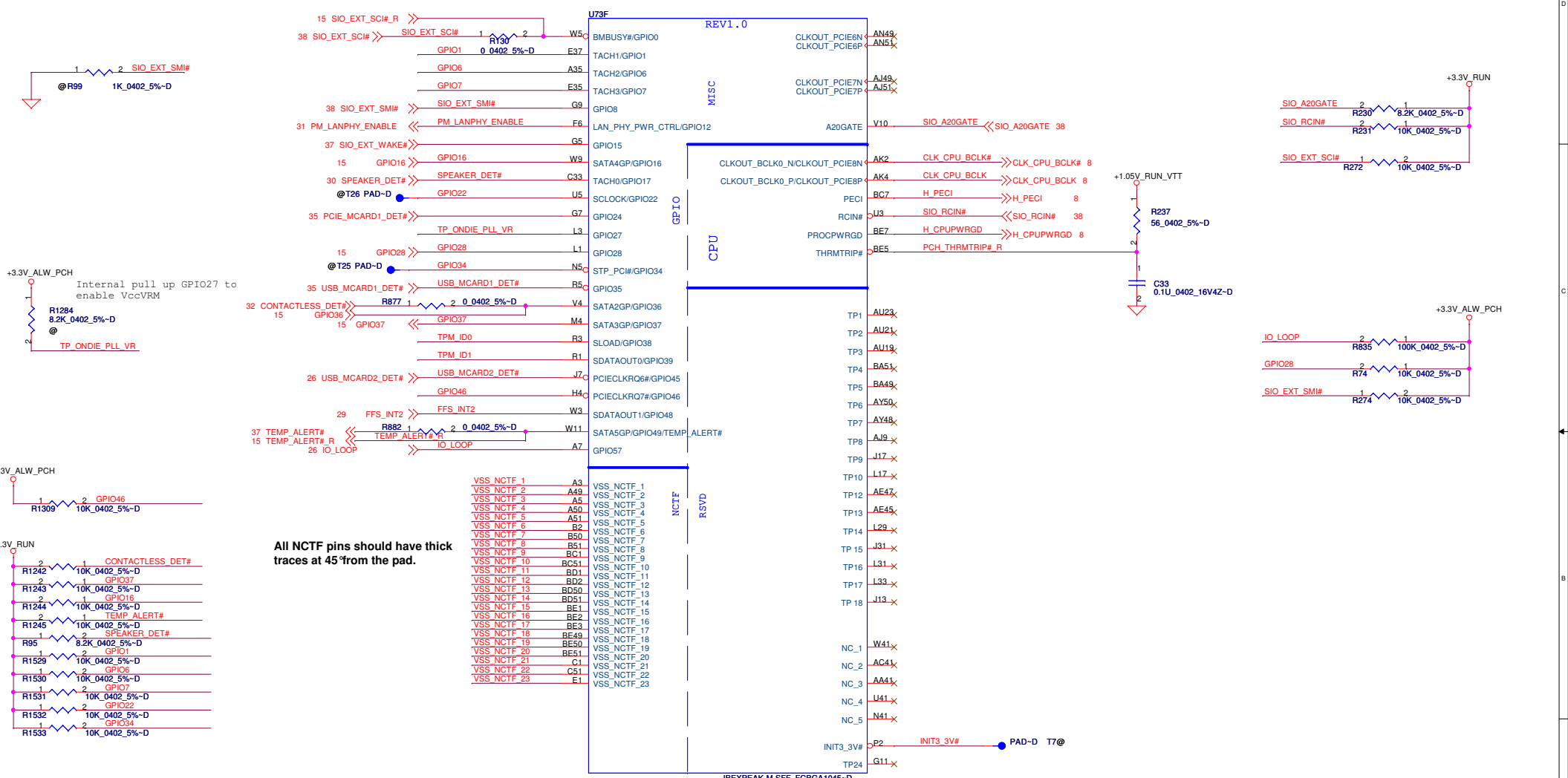


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All NCTF pins should have thick traces at 45° from the pad.

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1

-----> will use MEMO control pop R339 & de-pop R787 when USH1.0 enable for SSI build only

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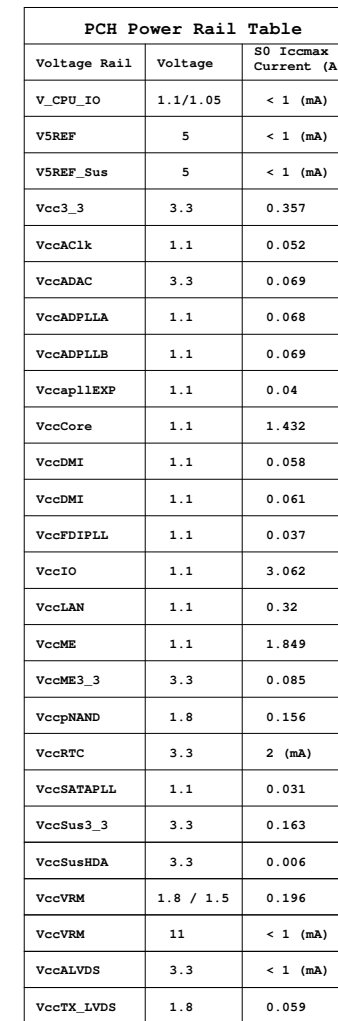
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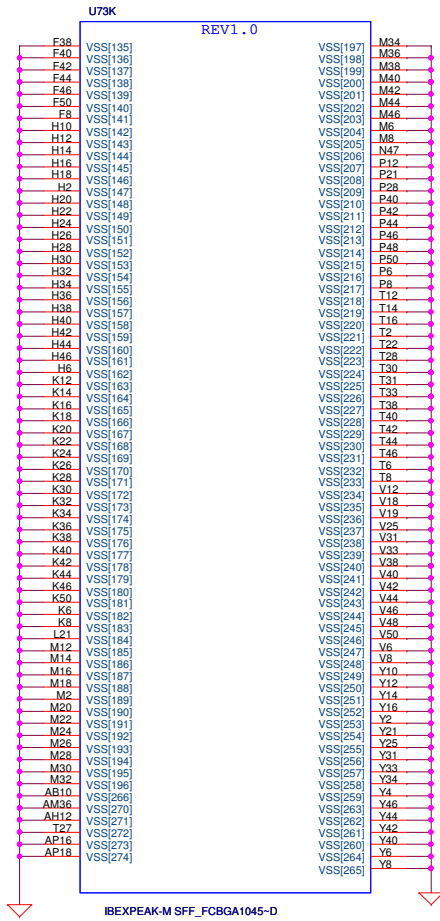
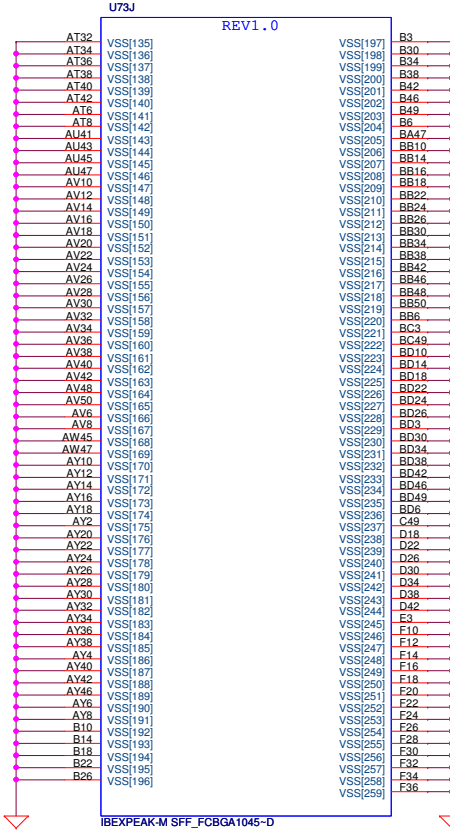
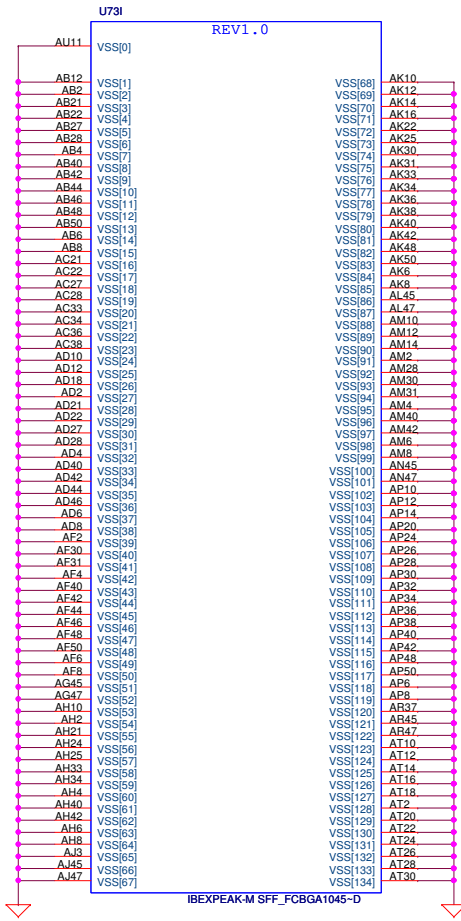
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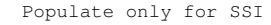
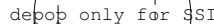
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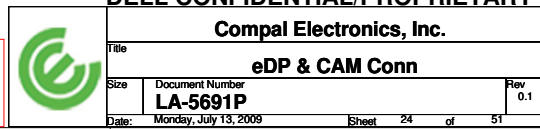
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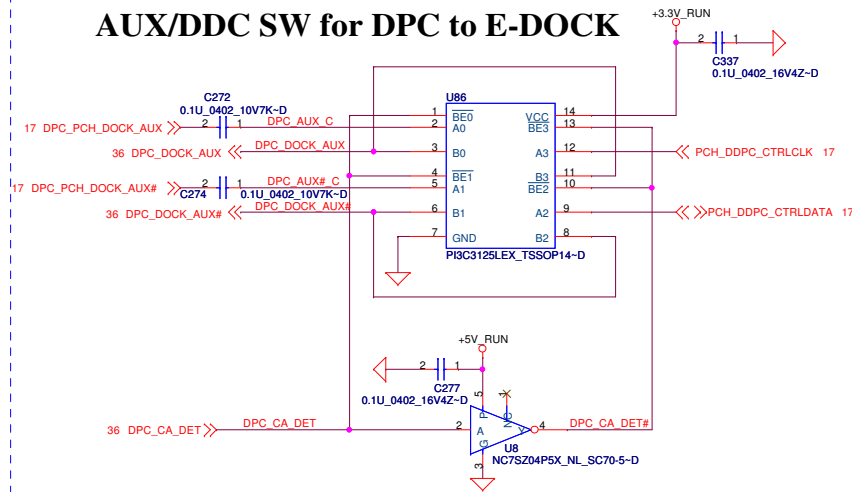
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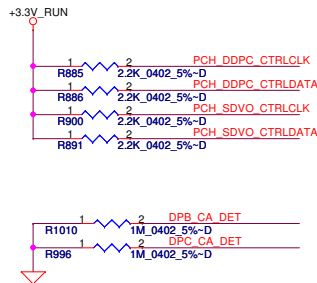
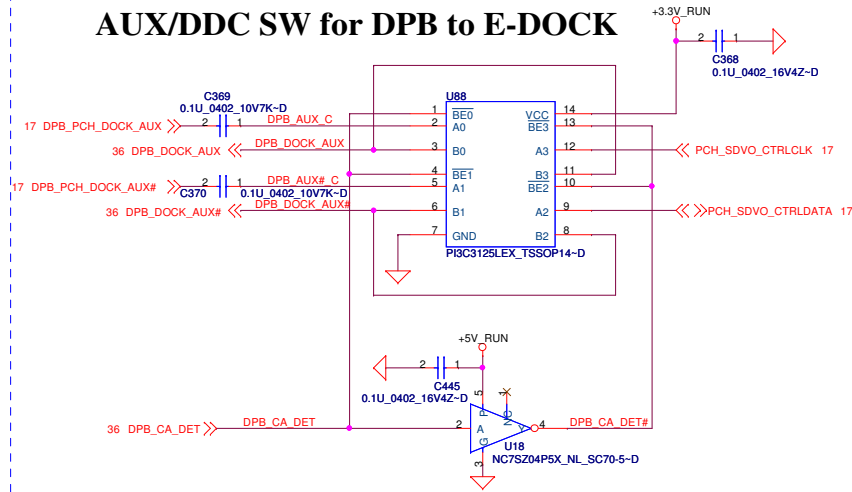
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AUX/DDC SW for DPC to E-DOCK



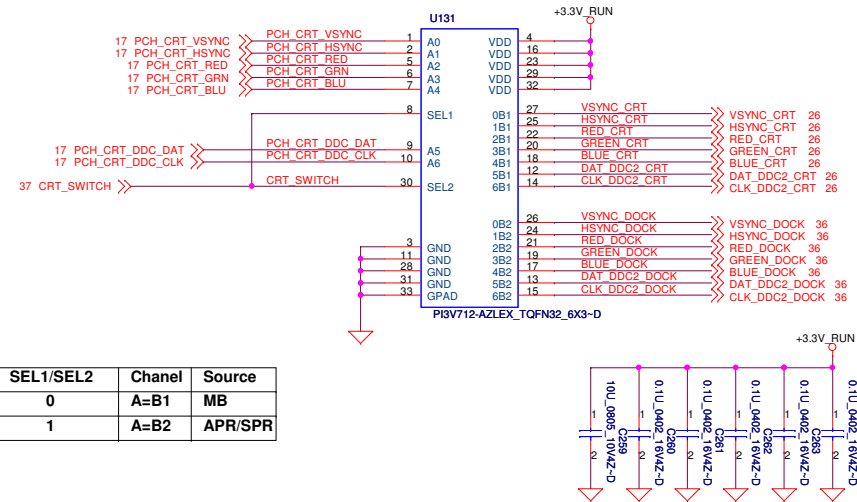
AUX/DDC SW for DPB to E-DOCK



Intel WW18 Strapping option

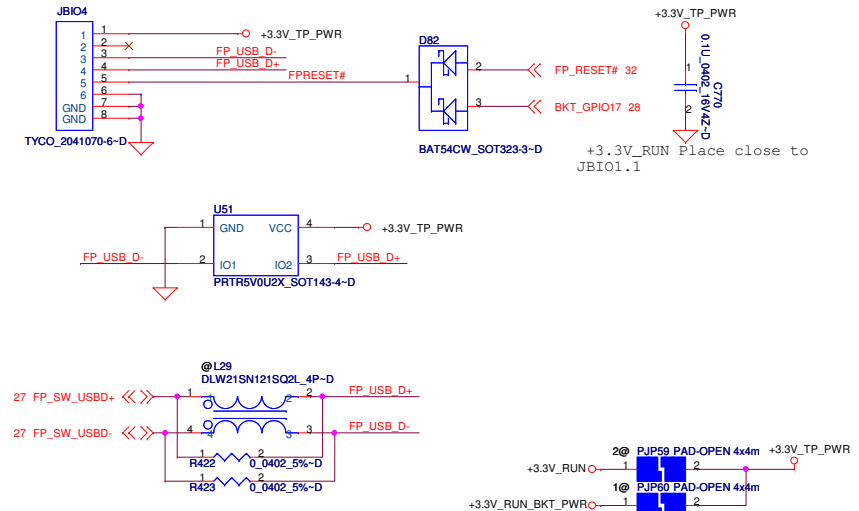
Intel WW18 Strapping option

VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

Fingerprint CONN.



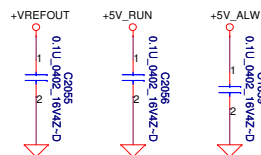
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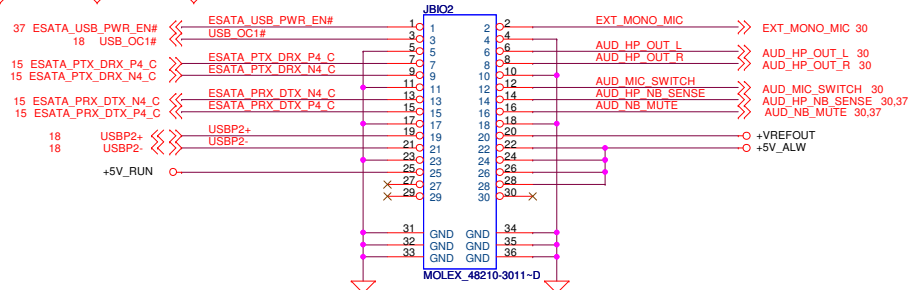
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Size	Document Number	Rev	
	LA-5691P	0.1	
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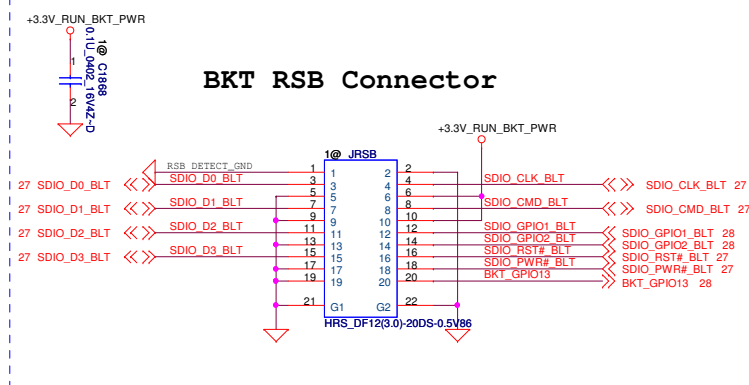
Close to JP1



E-SATA/Jack Connector

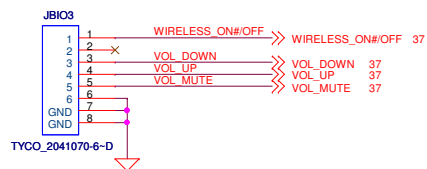


BKT RSB Connector

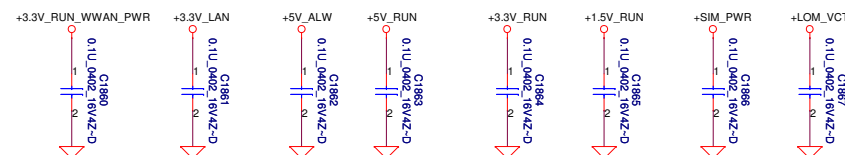
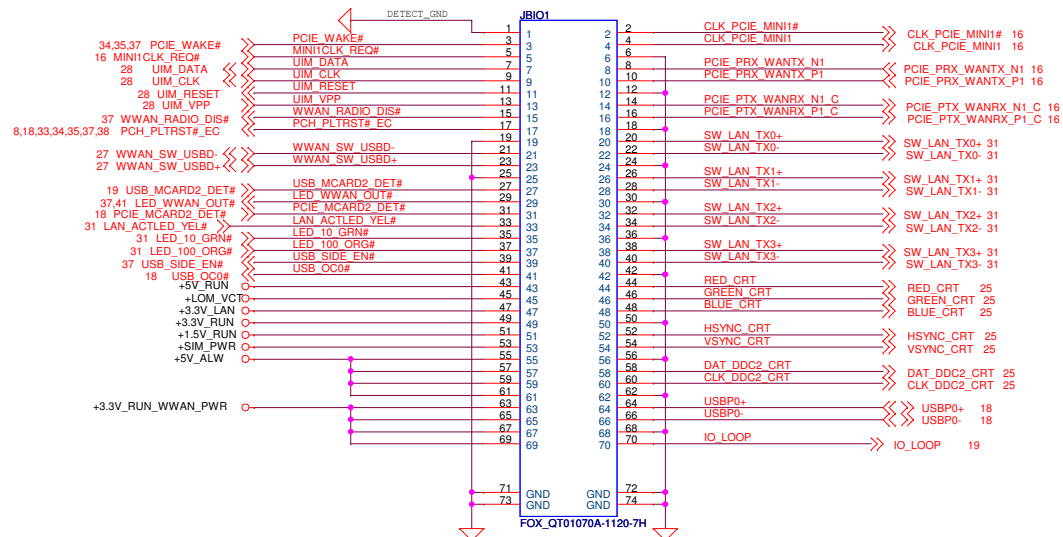


Volume + Sniffer

Change to 6 pins connector



BTB Connector

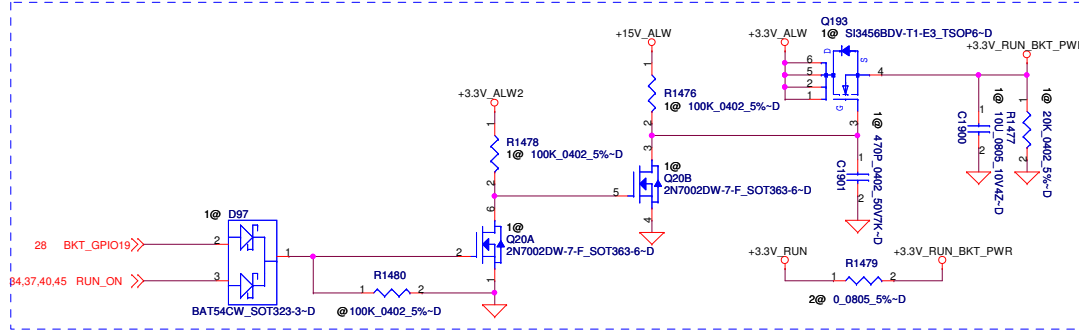


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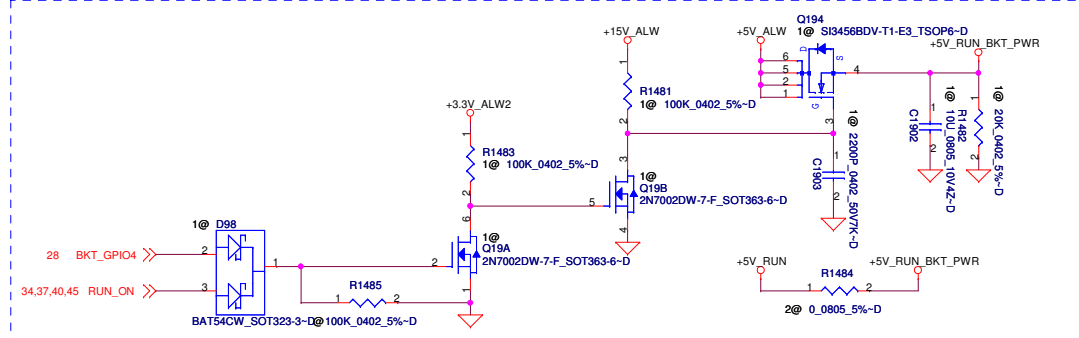
Compal Electronics, Inc.			
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Display port			
Size	Document Number	Rev	
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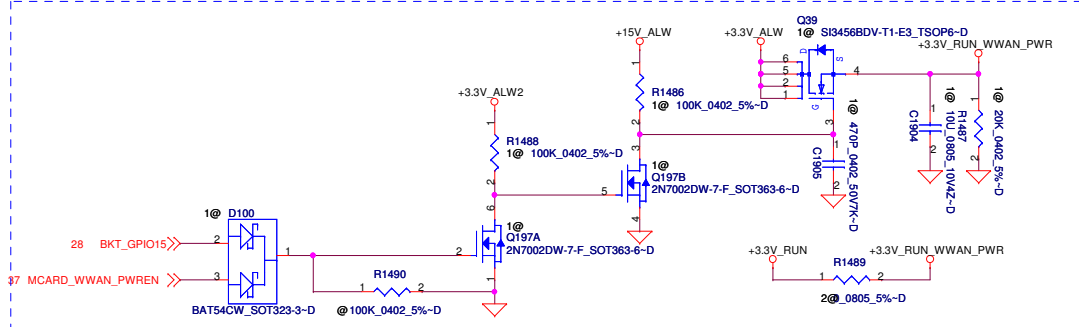
+3.3V_RUN_BKT_PWR Source



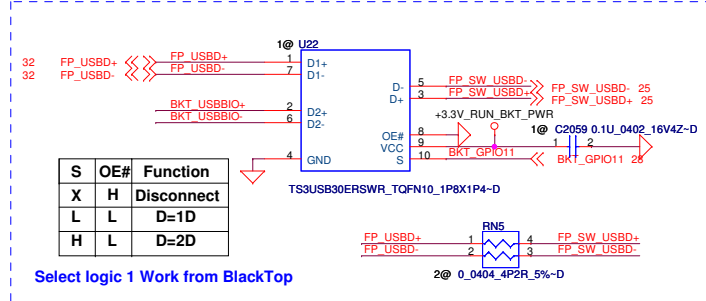
+5V_RUN_BKT_PWR Source, for Touch Pad and Audio Amplifier



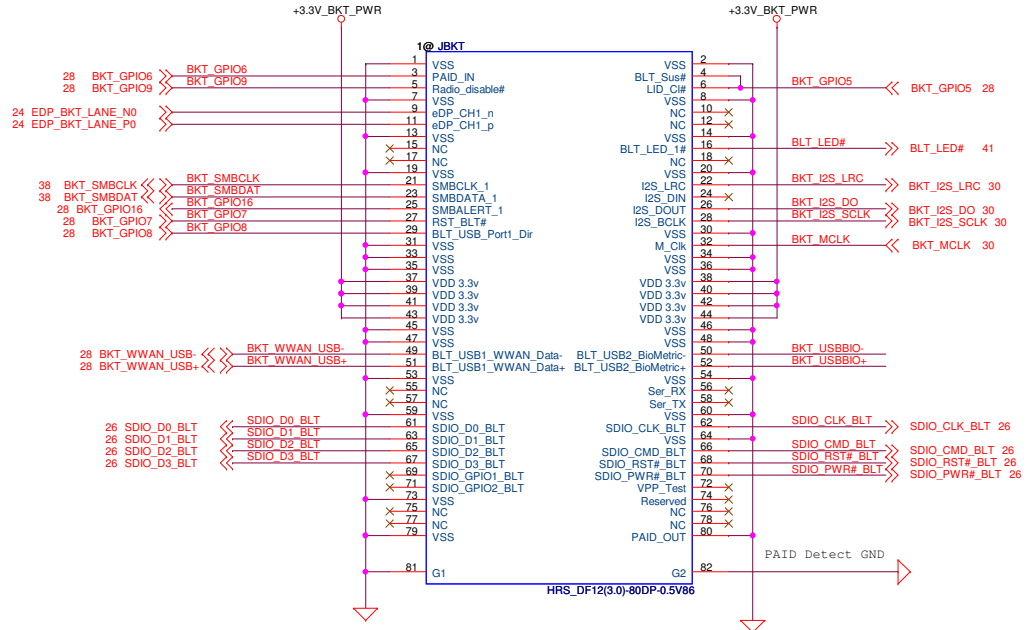
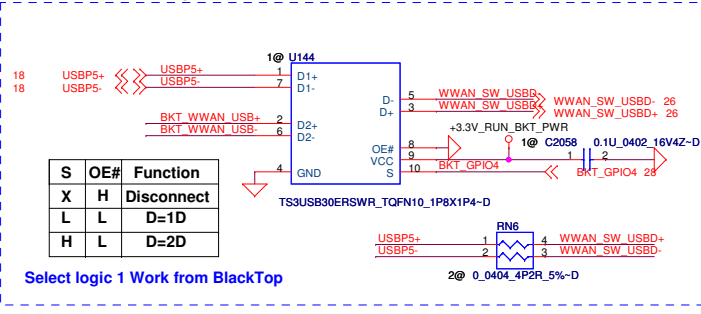
+3.3V_RUN_WWAN_PWR Source, for WWAN



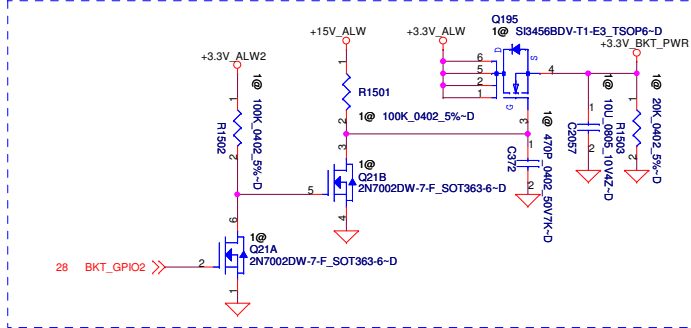
For Biometric USB signals isolation



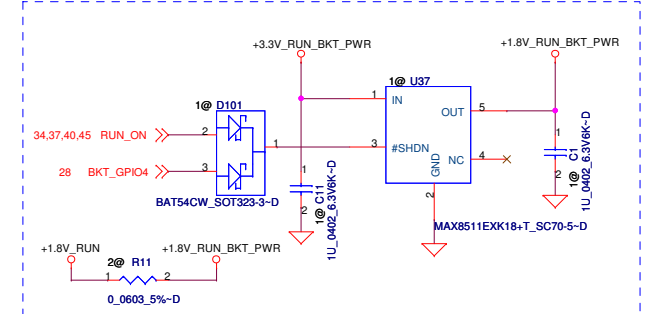
For WWAN USB signals isolation



Enable BlackTop POWER



For Audio I2S



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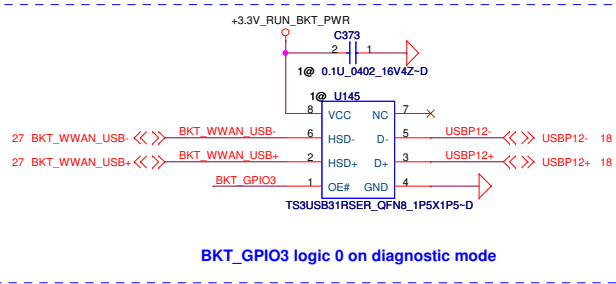


BlackTop POWER and CONN			
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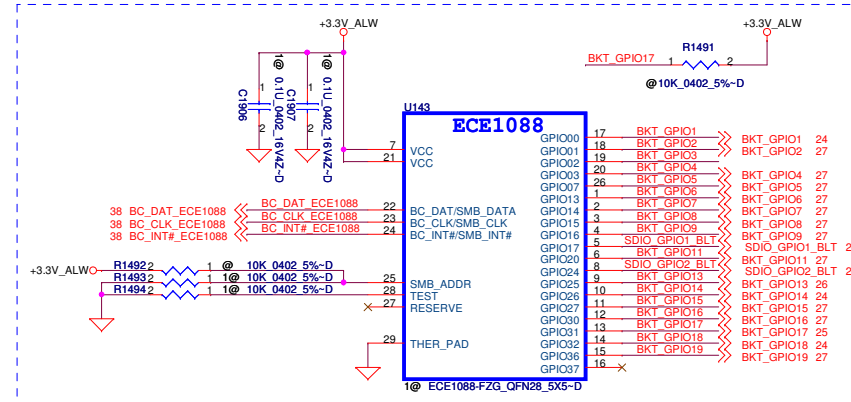
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GPIO Expander for BlackTop

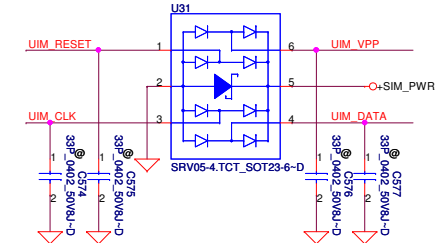
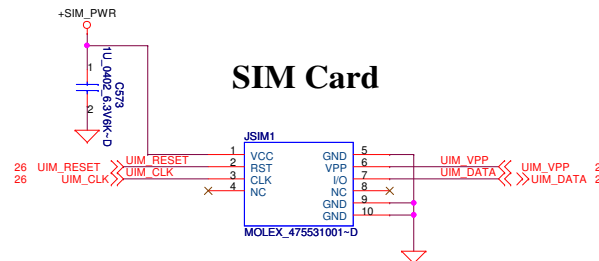
Add BlackTop to PCH interface by USB signal when diagnostic mode



- BKT_GPIO1 → For eDP signals switch
- BKT_GPIO2 → For BKT power switch
- BKT_GPIO3 → For TP power switch&USB signal switch
- BKT_GPIO4 → For AMP/TP power source&USB signal switch
- BKT_GPIO5 → For LID_Closed
- BKT_GPIO6 → For PAD_Out
- BKT_GPIO7 → For BKT Reset
- BKT_GPIO8 → For USB_SEL_BLK
- BKT_GPIO9 → For Radio_OFF
- BKT_GPIO11 → Biometric mux switch
- BKT_GPIO12 → For WLAN antenna mux control
- BKT_GPIO13 → RSB_DET#
- BKT_GPIO14 → For Inverter Power
- BKT_GPIO15 → For WWAN Power
- BKT_GPIO16 → For SMBALERT
- BKT_GPIO17 → For Biometric reset signal
- BKT_GPIO18 → For LVDS Power switch
- BKT_GPIO19 → For TP Power



SIM Card



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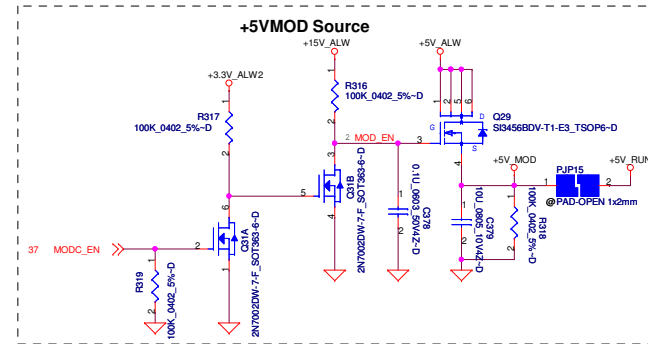
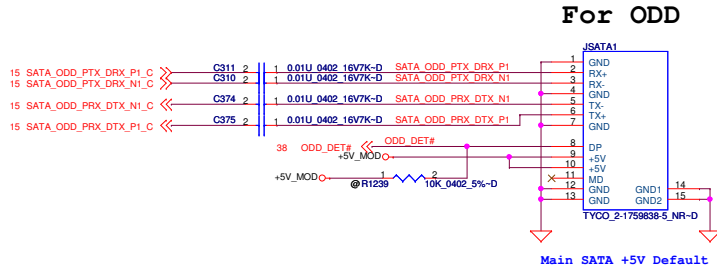
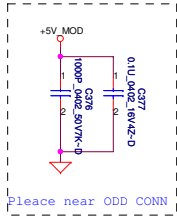
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Title
Braidwood/ SATA repeater & PCIe SATA SW

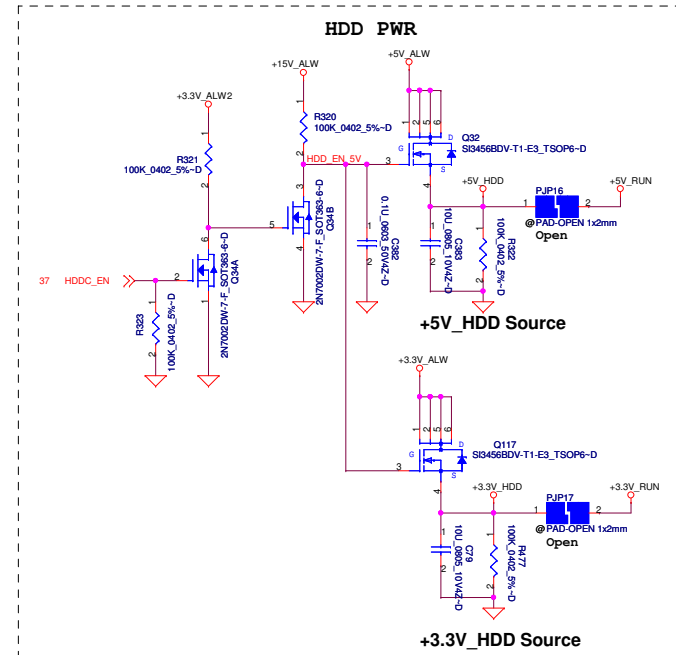
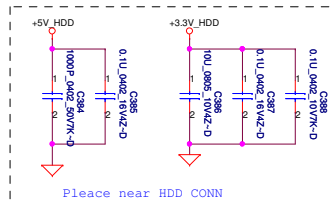
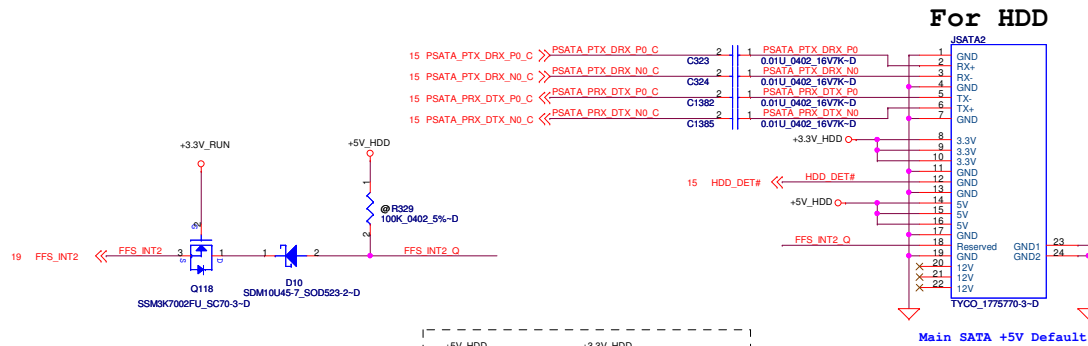
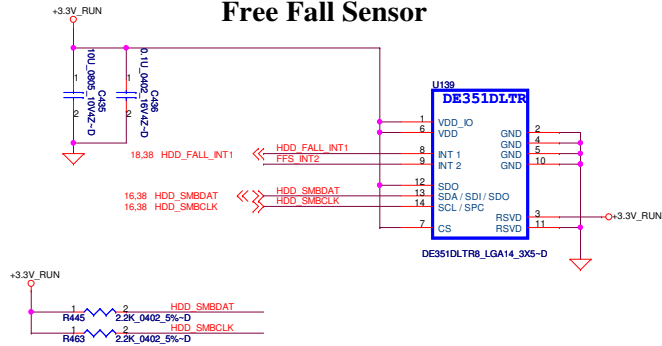
Size Document Number
LA-5691P

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Free Fall Sensor

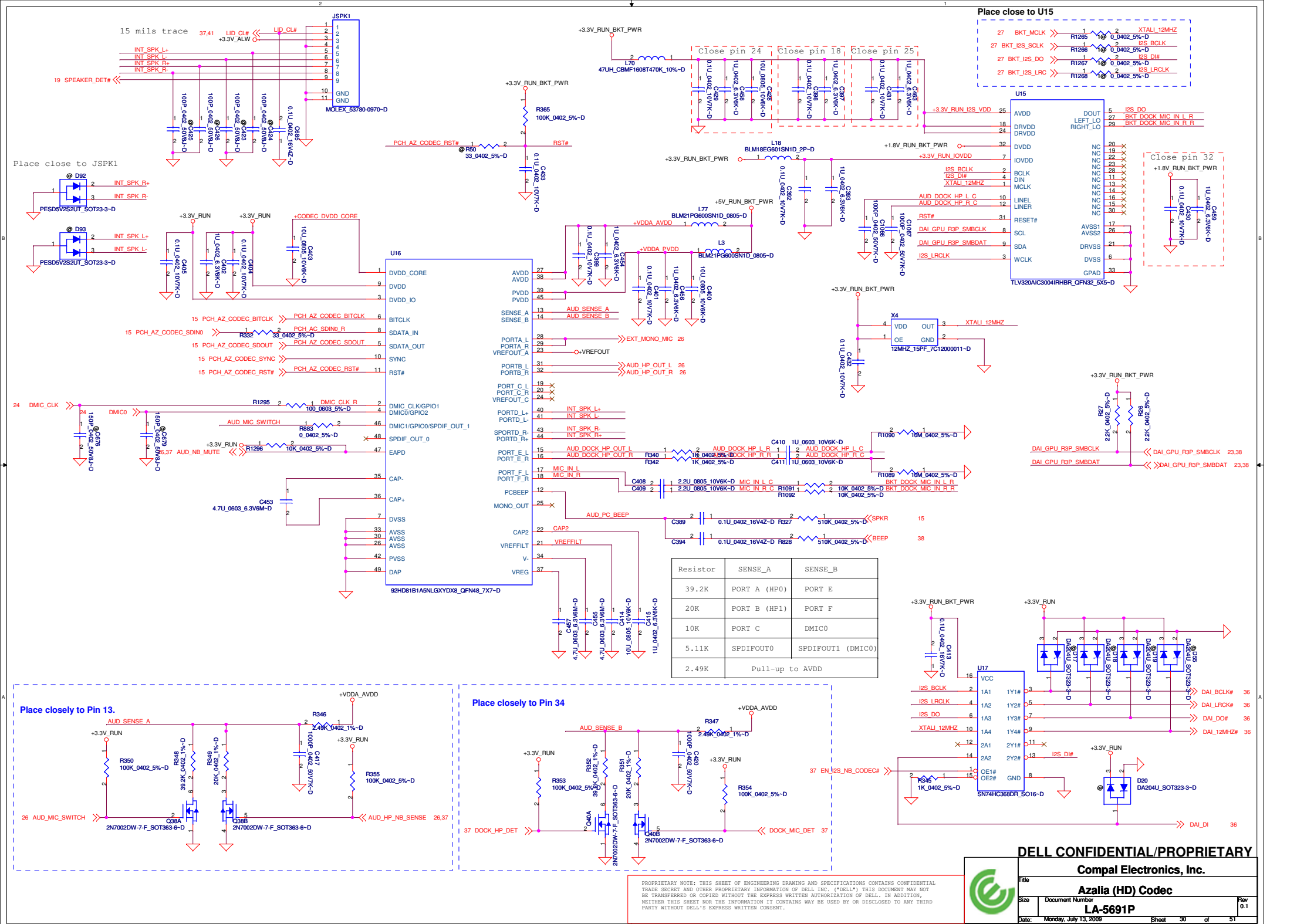


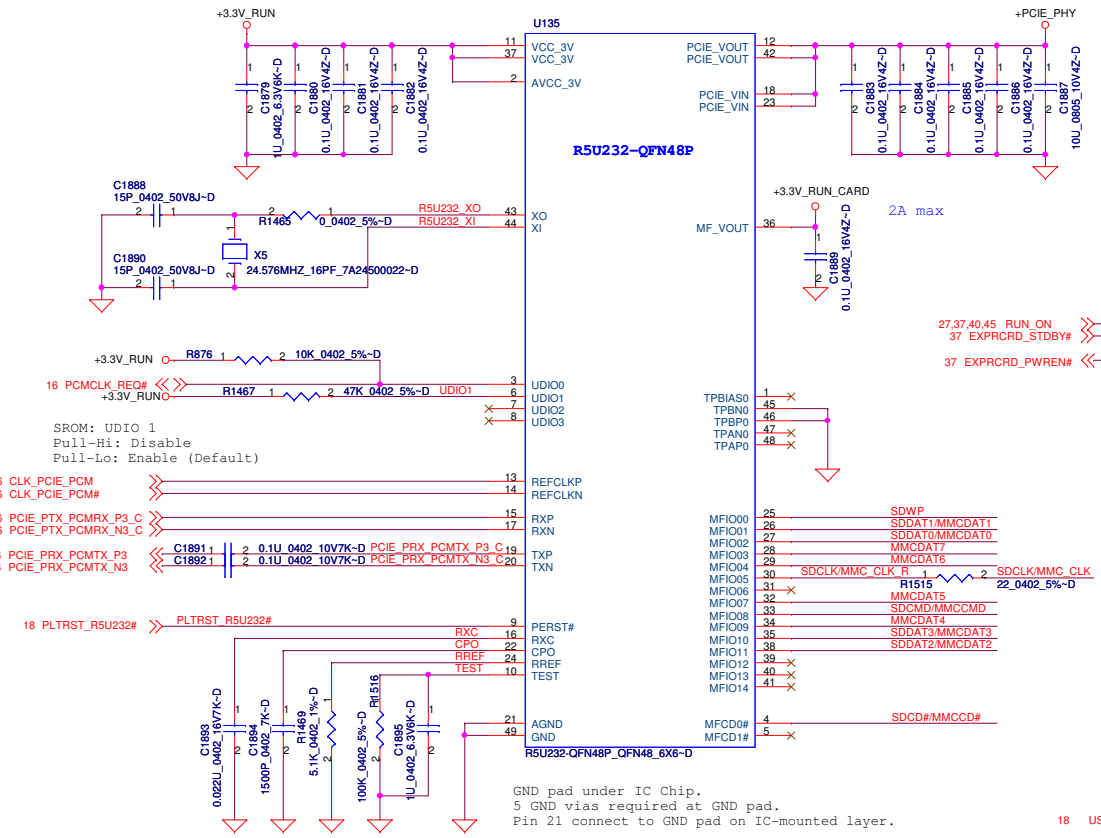
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Title		ODD/HDD CONNECTOR	
Size	Document Number	LA-5691P	
Date	Monday, July 13, 2009	Sheet	29 of 51

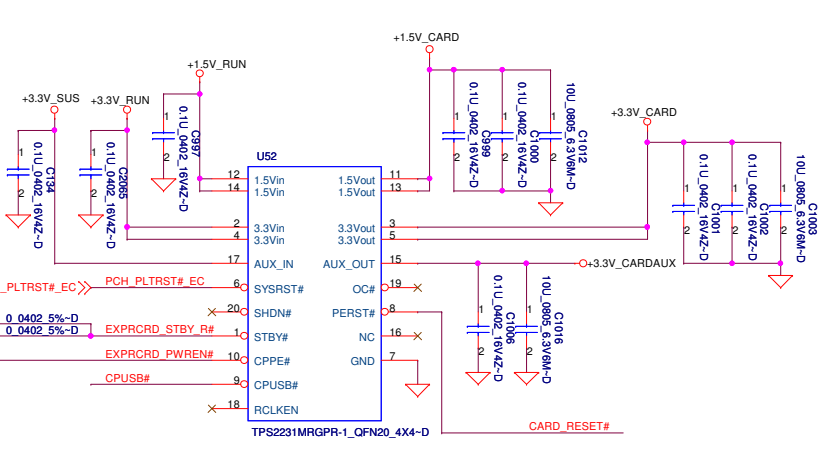
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GND pad under IC Chip.
5 GND vias required at GND pad.
Pin 21 connect to GND pad on IC-mounted layer.

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK

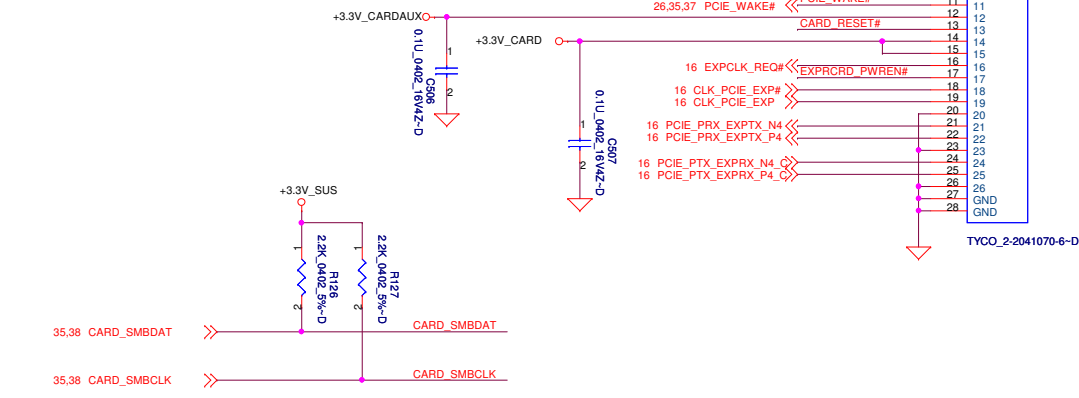


Express Card

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

MFIO Pin Assignment Table

@L64 DLW21SN900SQ2_0805-D



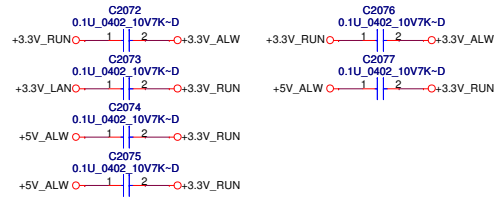
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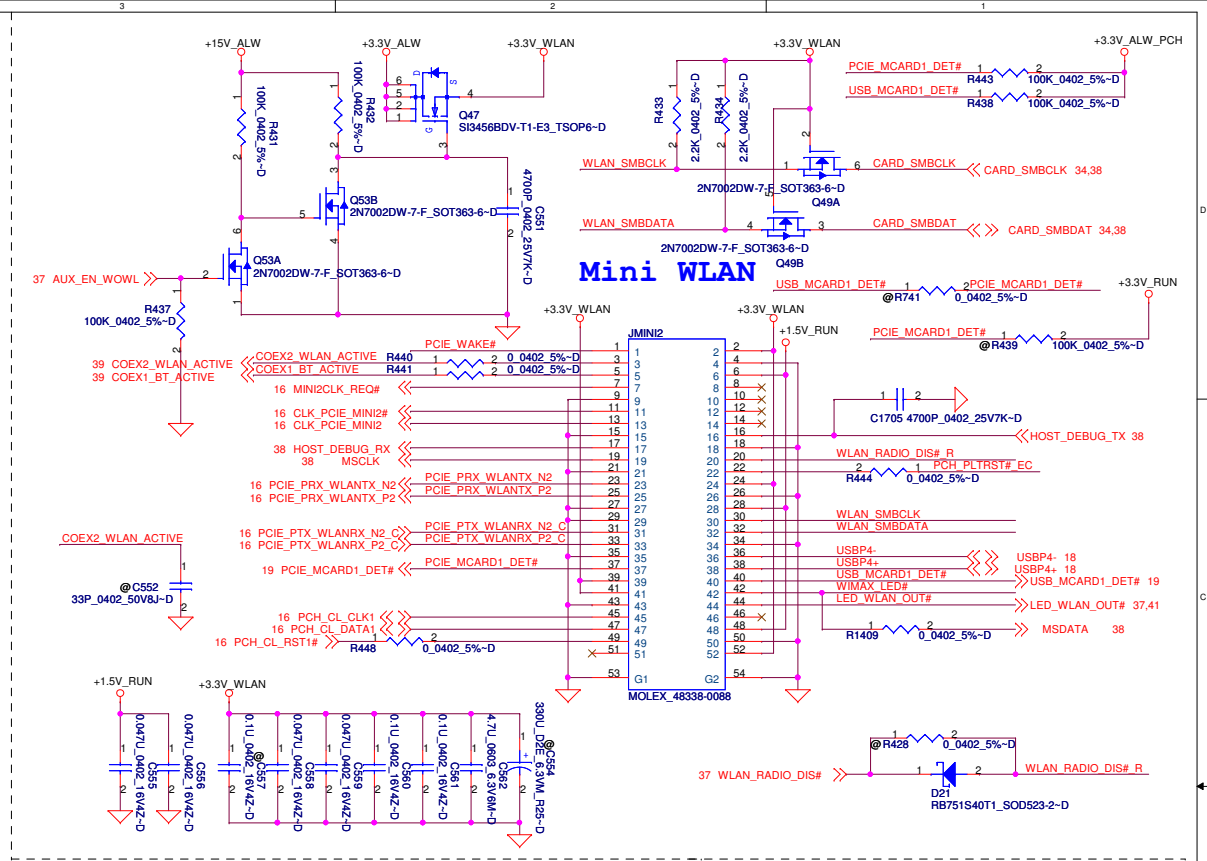
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R5U232			
Size	Document Number	Rev	
Custom	LA-5691P	0.1	
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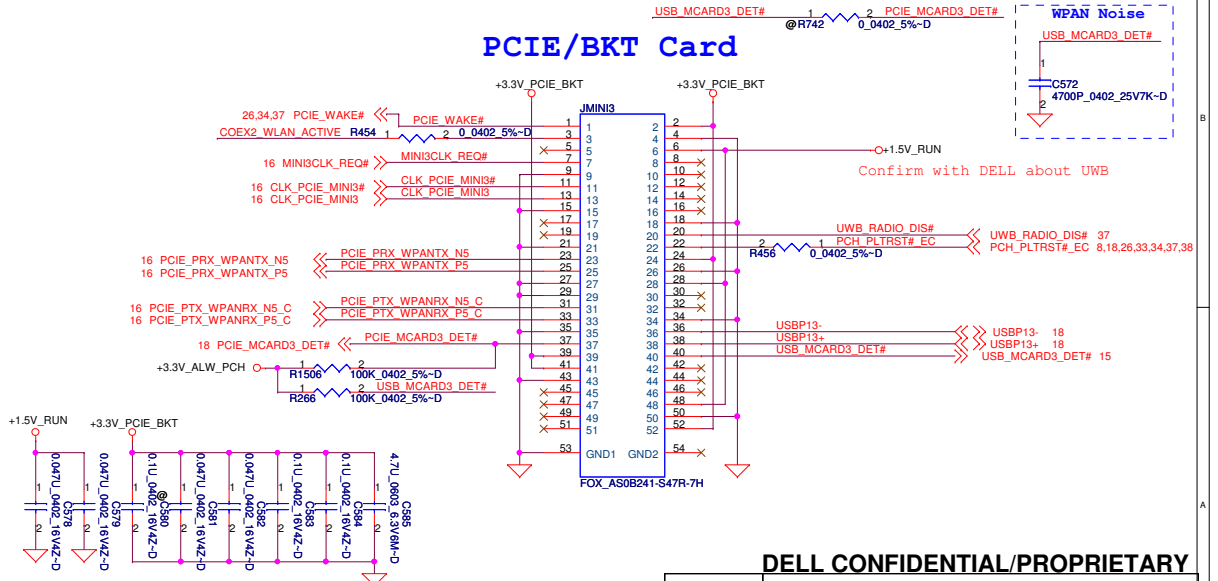
Stitching caps for MDI



Stitching caps for PCIE6



PCIE/BKT Card



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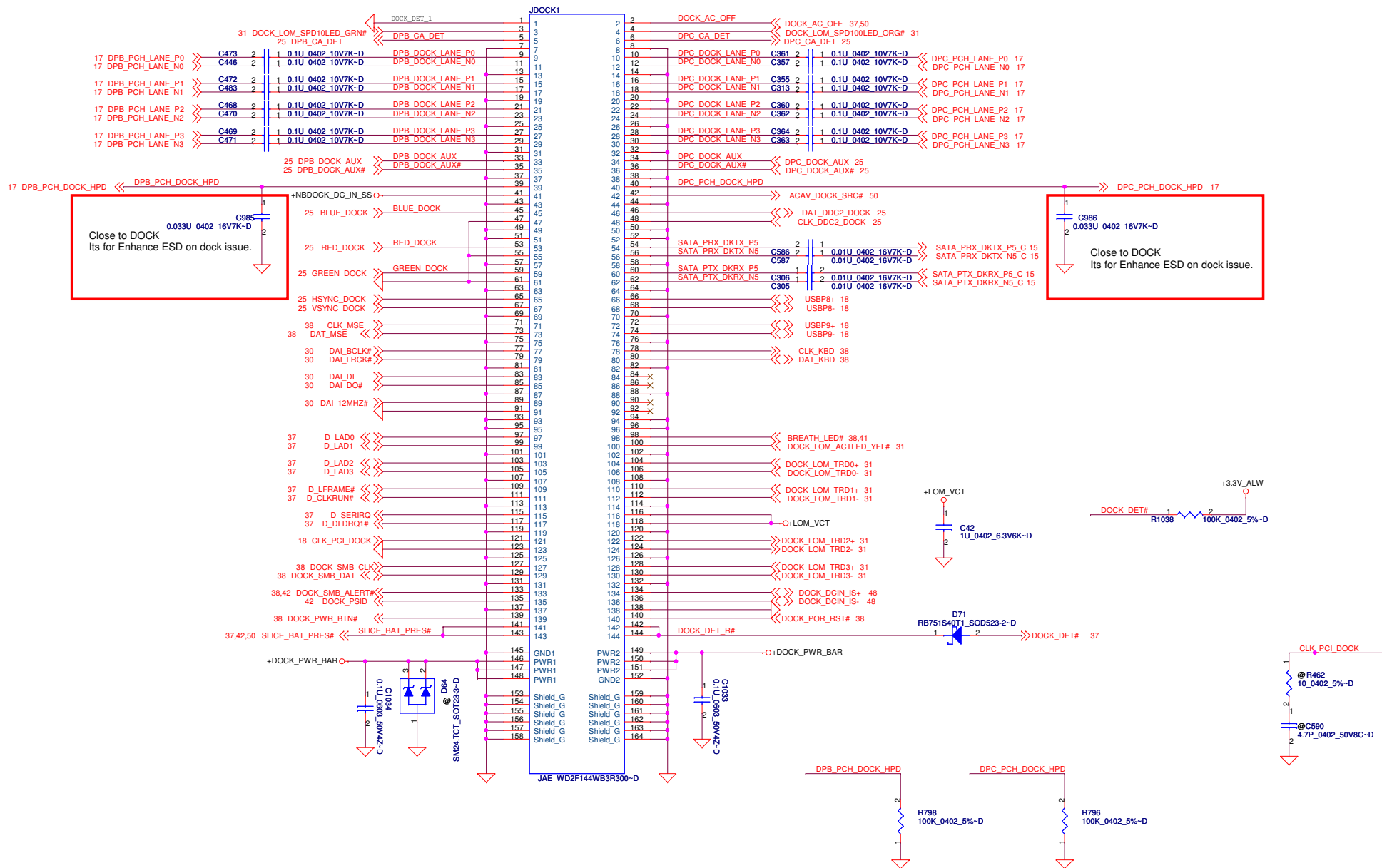
Compal Electronics, Inc.

Mini Card

LA-5691P

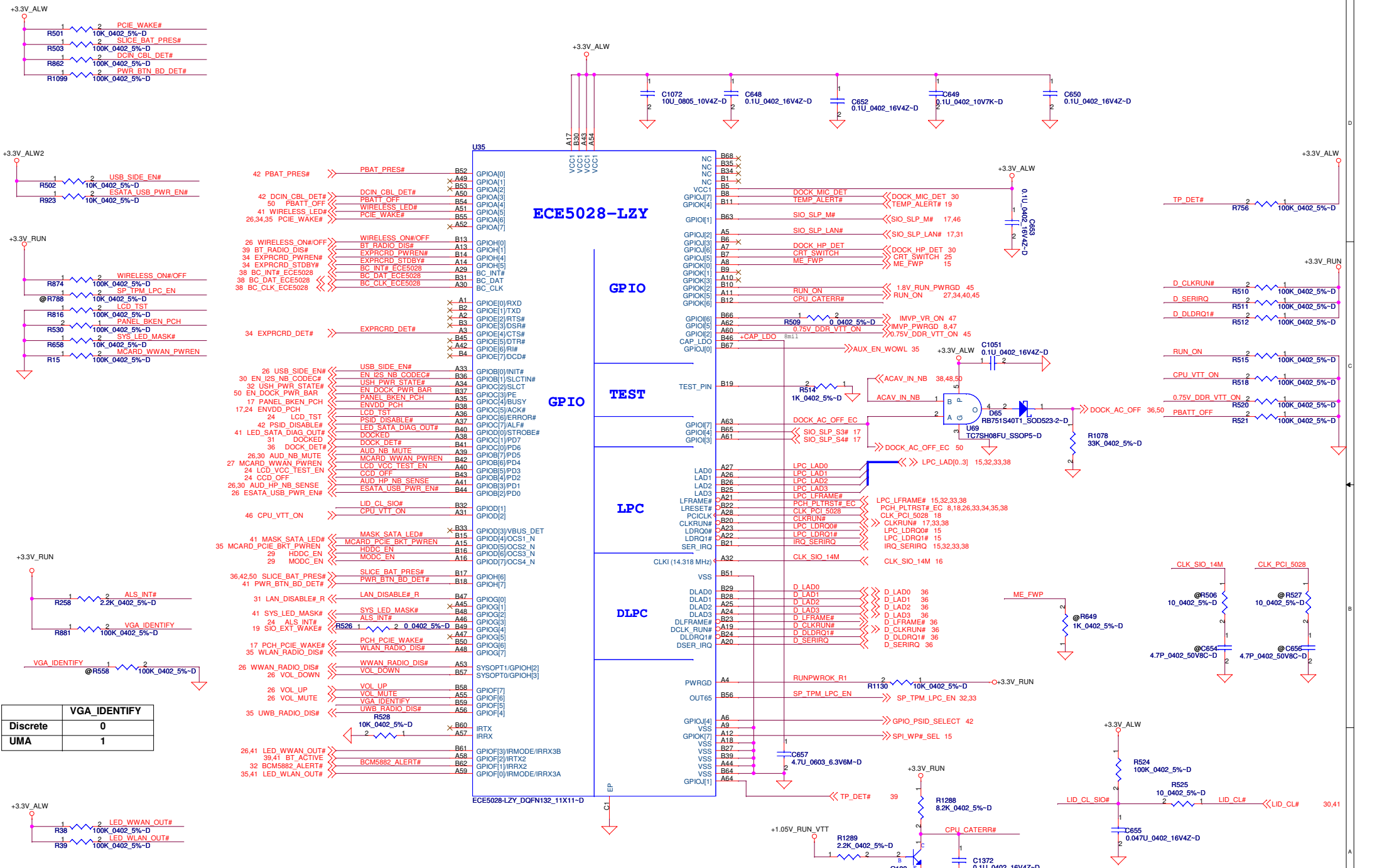
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Compal Electronics, Inc.			
DOCKING CONN			
Title Size Date: Monday, July 13, 2009	Document Number LA-5691P	Rev 0.1	Sheet 36 of 51

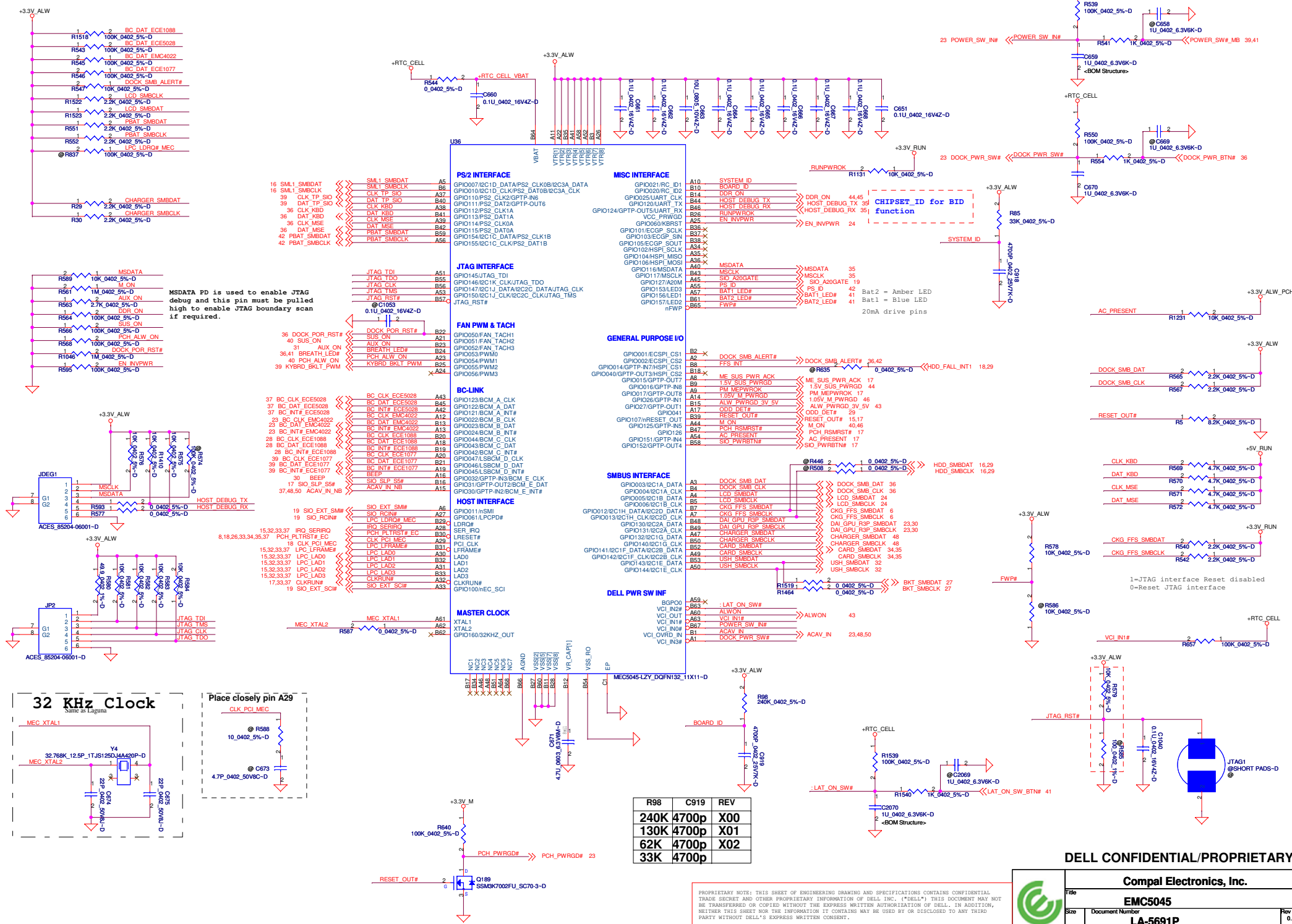


	VGA_IDENTIFY
Discrete	0
UMA	1

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ECE5028			
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R98	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	

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EMC5045

Size: **EMC5045**

Number: **LA-5691P**

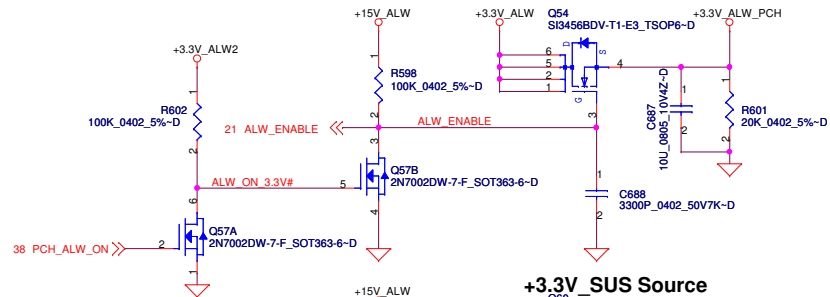
Date: Monday, July 13, 2009

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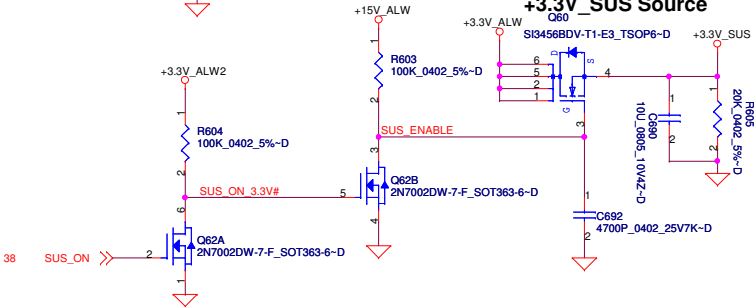
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DC/DC Interface

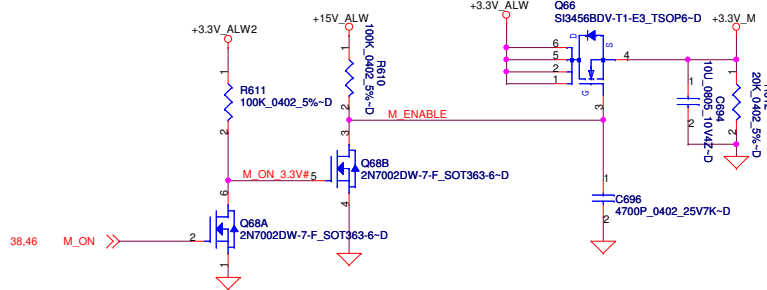
+3.3V_ALW_PCH Source



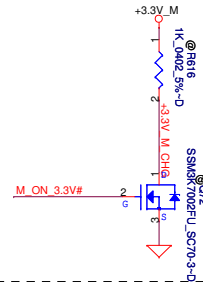
+3.3V_SUS Source



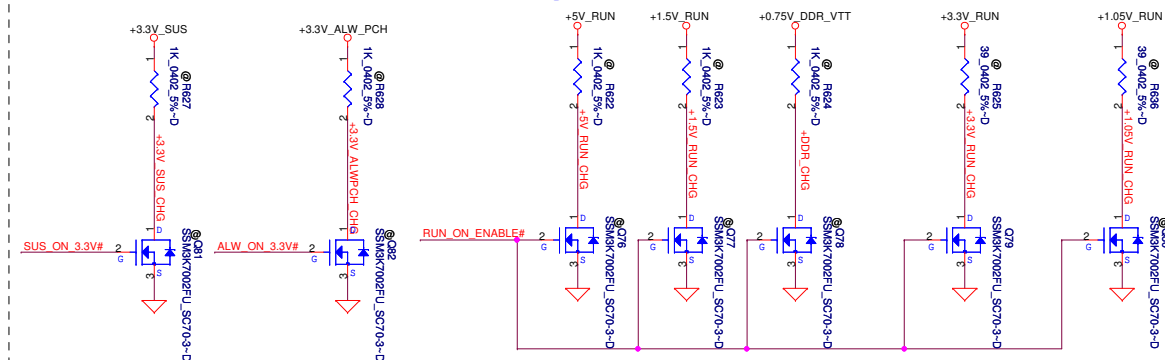
+3.3VM Source



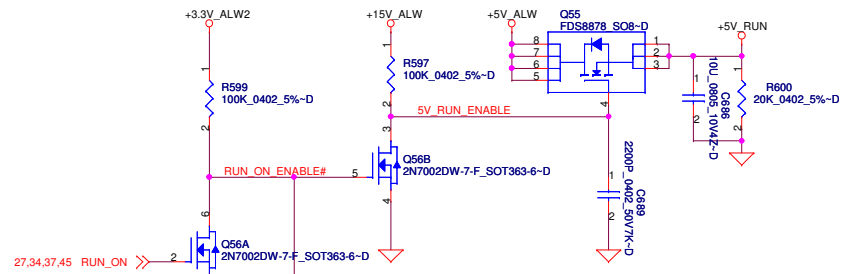
Discharg Circuit



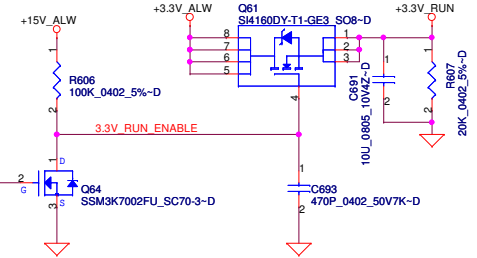
Discharg Circuit



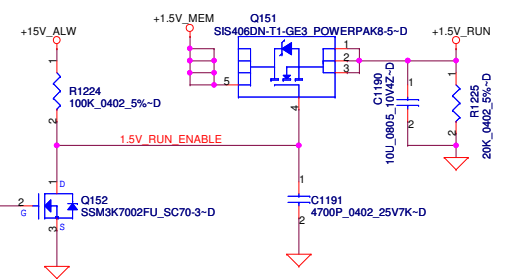
+5VRUN Source



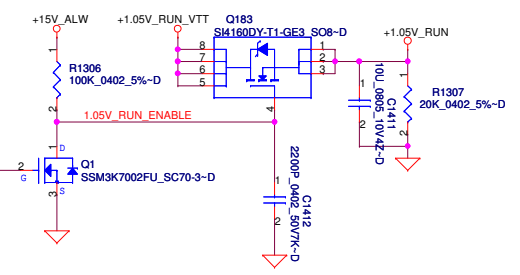
+3.3V_RUN Source



+1.5V_RUN Source



+1.05V_RUN Source



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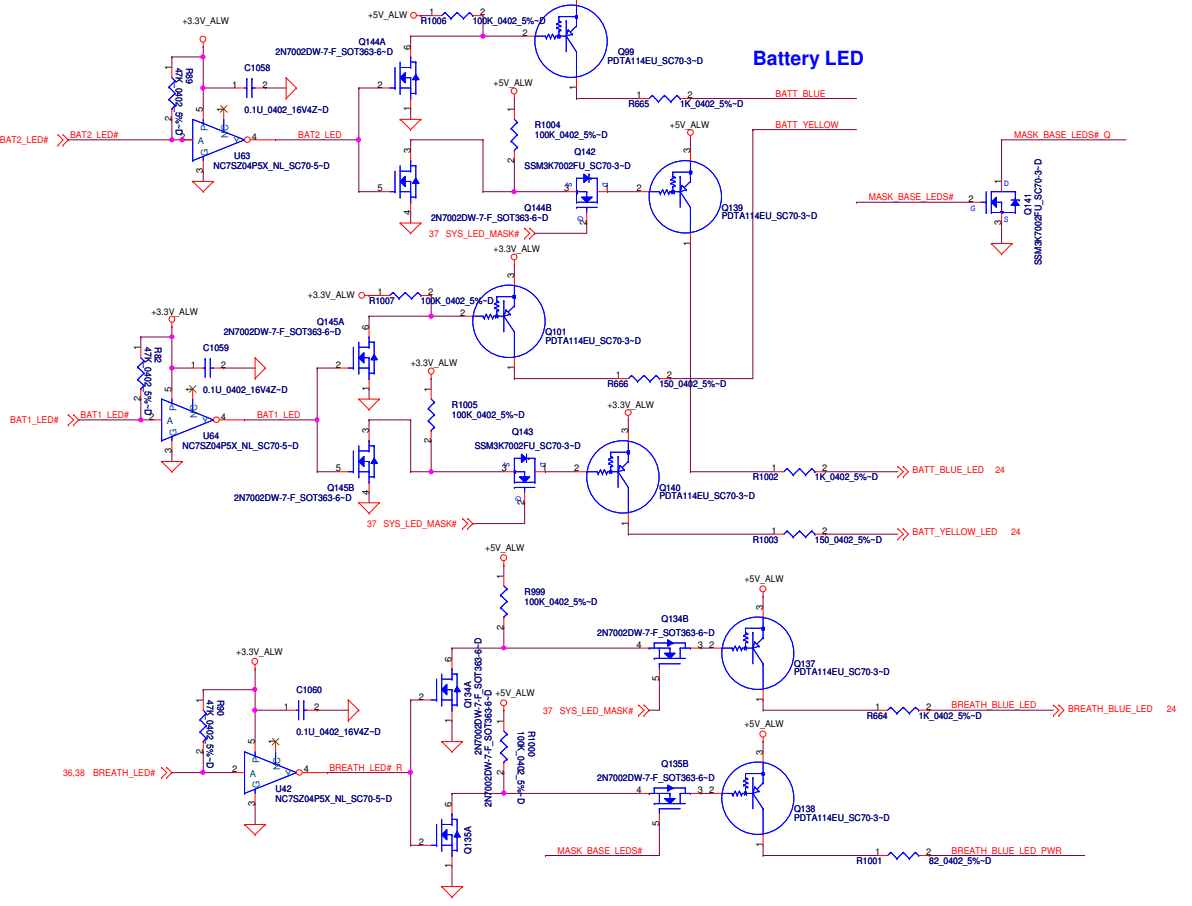
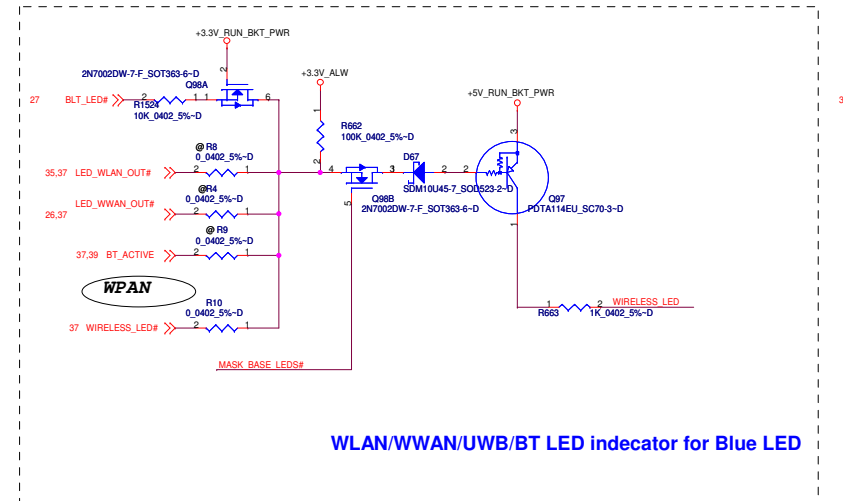
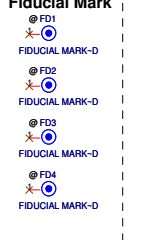
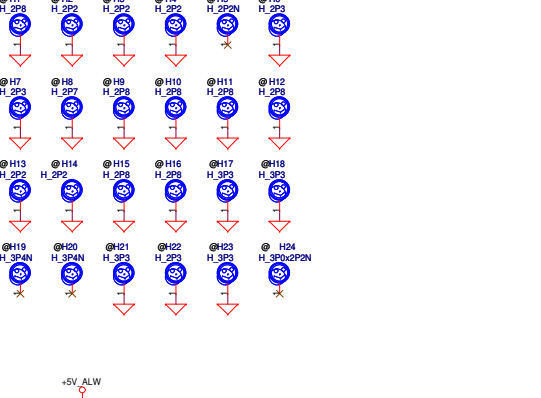
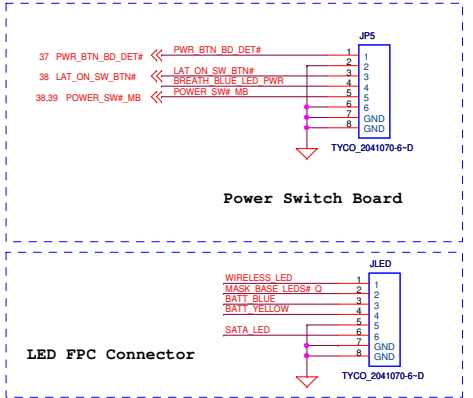
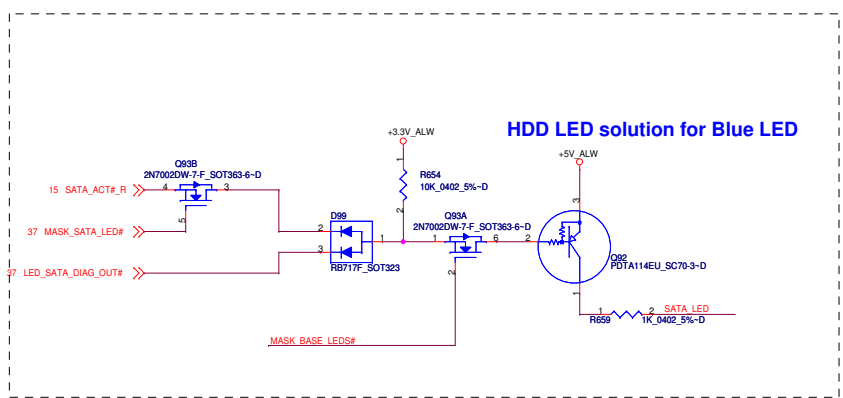
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POWER CONTROL

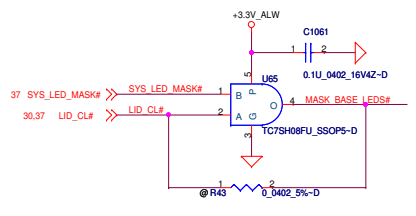
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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PAD and Standoff

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+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO

5 Volt +/-5%
Thermal Design Current:4.854A
Peak Current:6.935A
OCP_MIN:8.322A

3.3 Volt +/-5%
Thermal Design Current: 3.133A
Peak current: 4.475A
OCP_MIN:5.37A

VOUT2=5V
L=2.8uF
Fsw=400KHz
D=0.256
Input Ripple Current=TDC*(D*(1-D))^0.5=3.641A
Output Ripple Current=(19-5)*0.263/3u/400K=3.32A
Output Ripple Voltage=3.32*25m=83mV

VOUT2=3.3V
L=2.8uF
Fsw=300KHz
D=0.169
Input Ripple Current=TDC*(D*(1-D))^0.5=2.051A
Output ripple current=(19-3.3)*0.173/3u/300K=3.264A
Output ripple Voltage=3.264*25=81.6mV

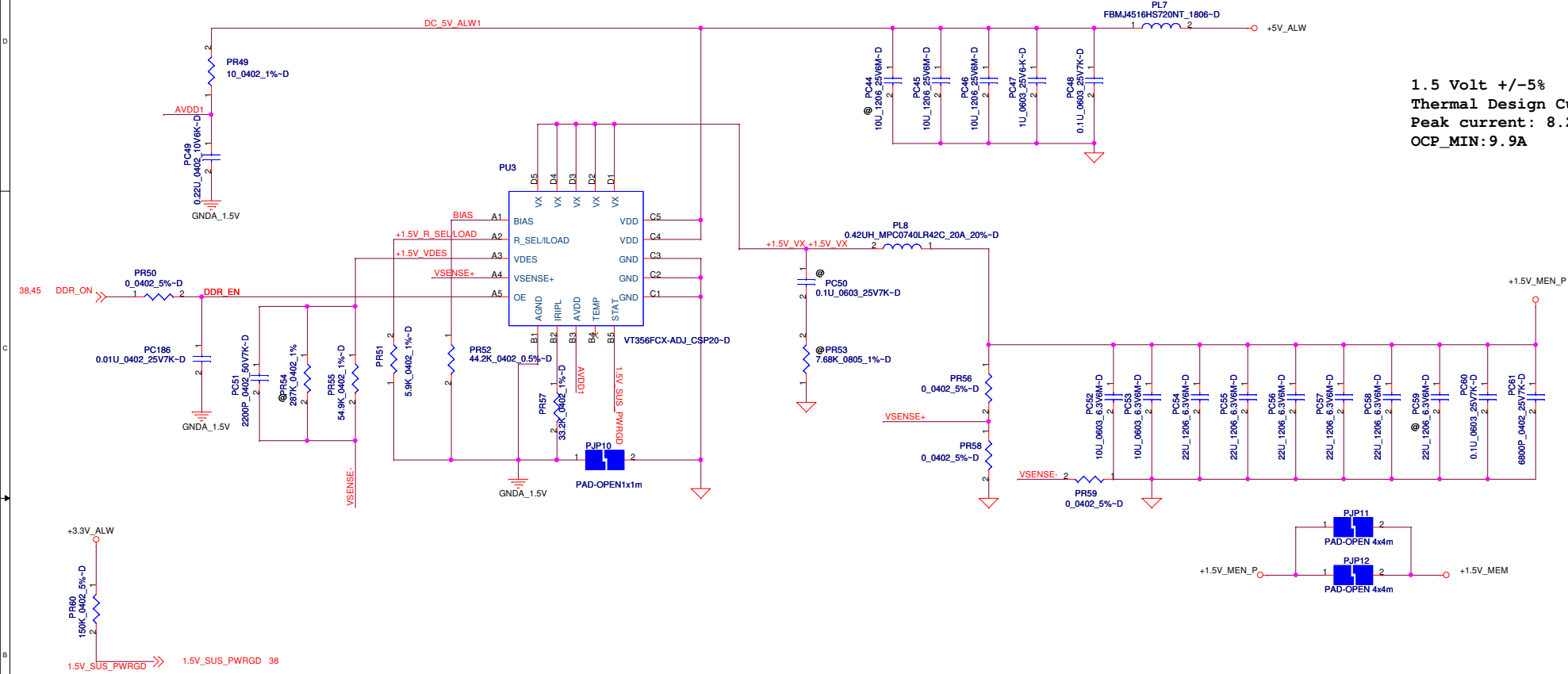
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		Compal Electronics, Inc.	
		DC/DC +3V/ +5V	
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+1.5V_MEN_P (VT356)

1.5 Volt +/-5%
Thermal Design Current: 5.775A
Peak current: 8.25A
OCP_MIN: 9.9A



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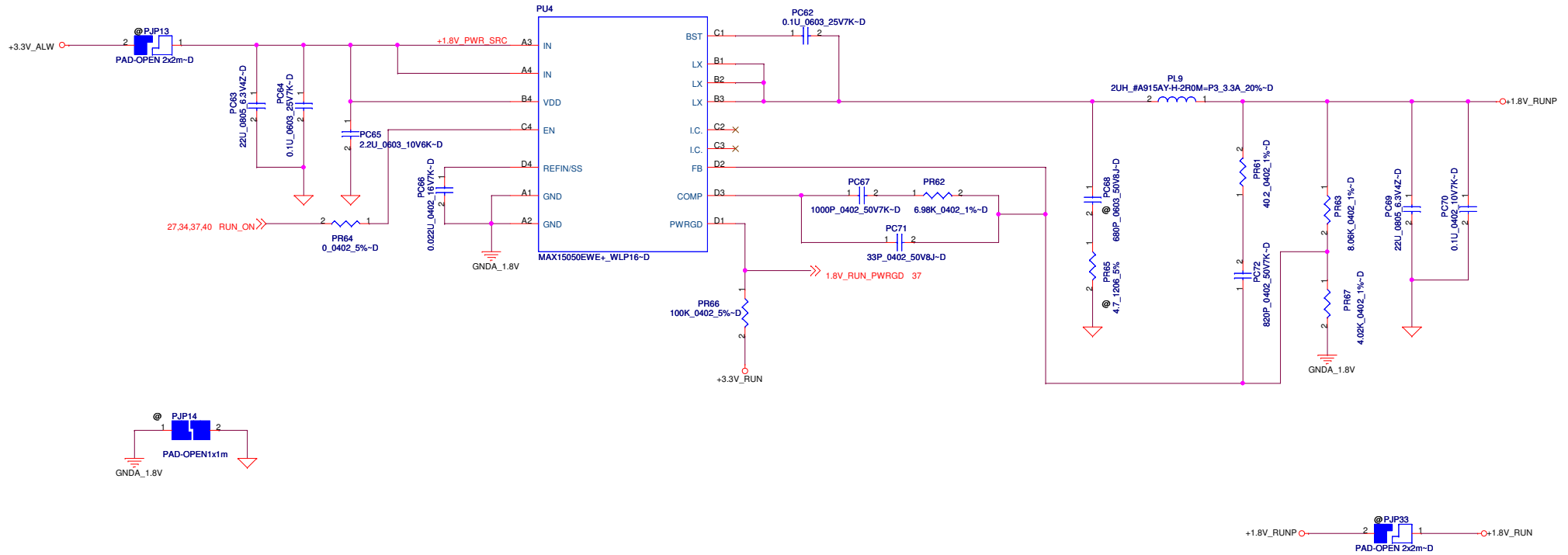
+1.5V_MEM

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+1.8V_RUN

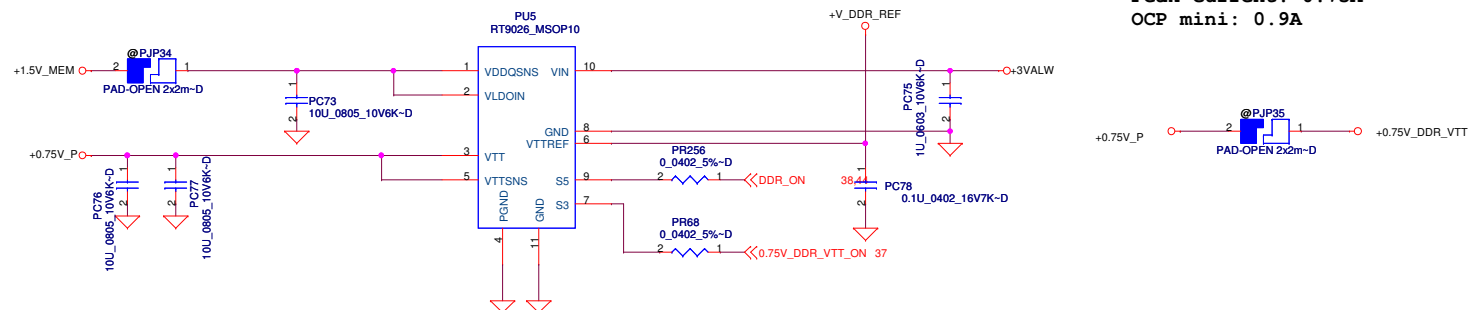
1.8 Volt +/-5%
Thermal Design Current: 0.894A
Peak current: 1.277A
OCP_min:1.532A



+0.75V_DDR_VTT

DDR3 Termination

0.75Volt +/-5%
Thermal Design Current: 0.525A
Peak current: 0.75A
OCP mini: 0.9A



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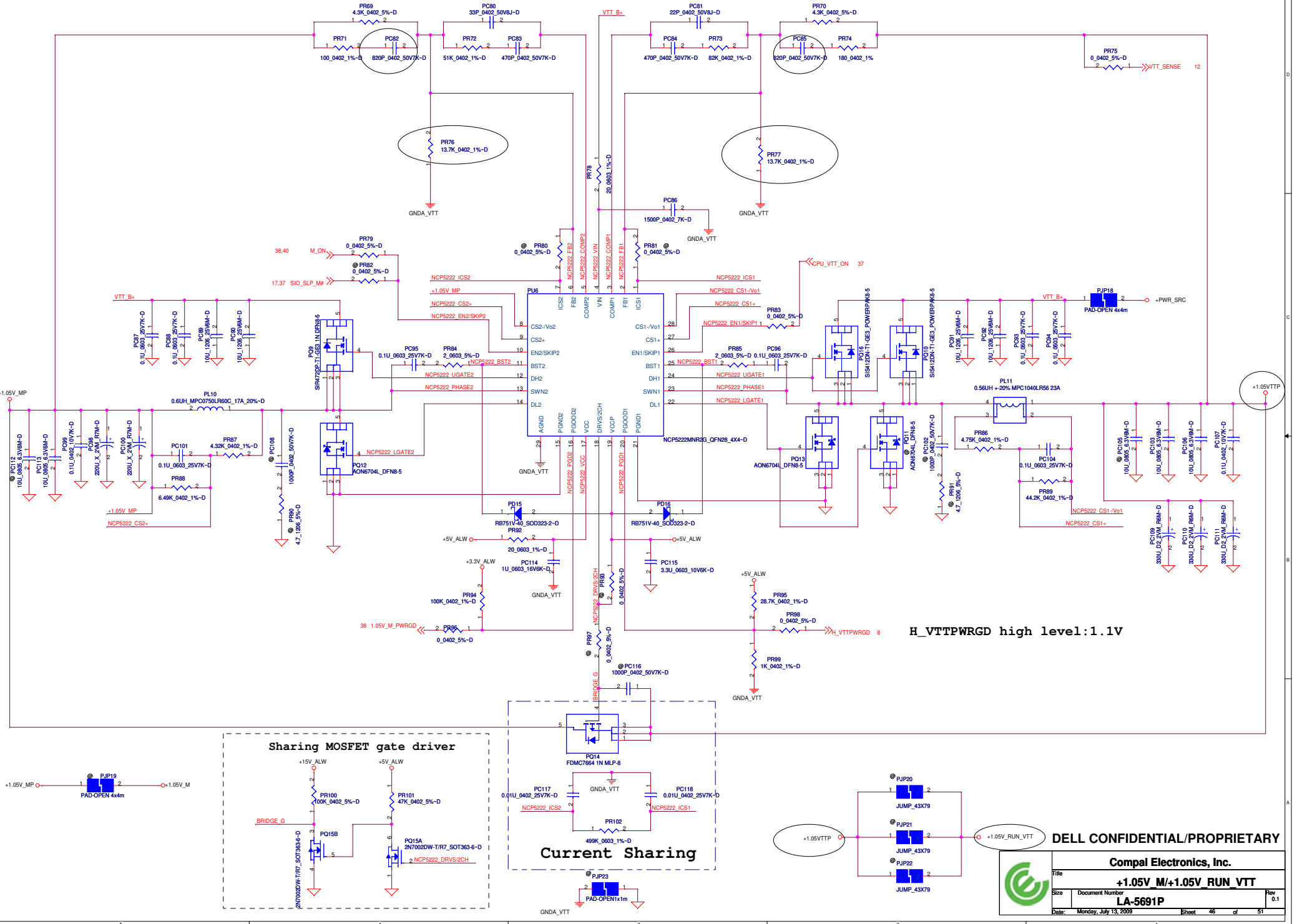
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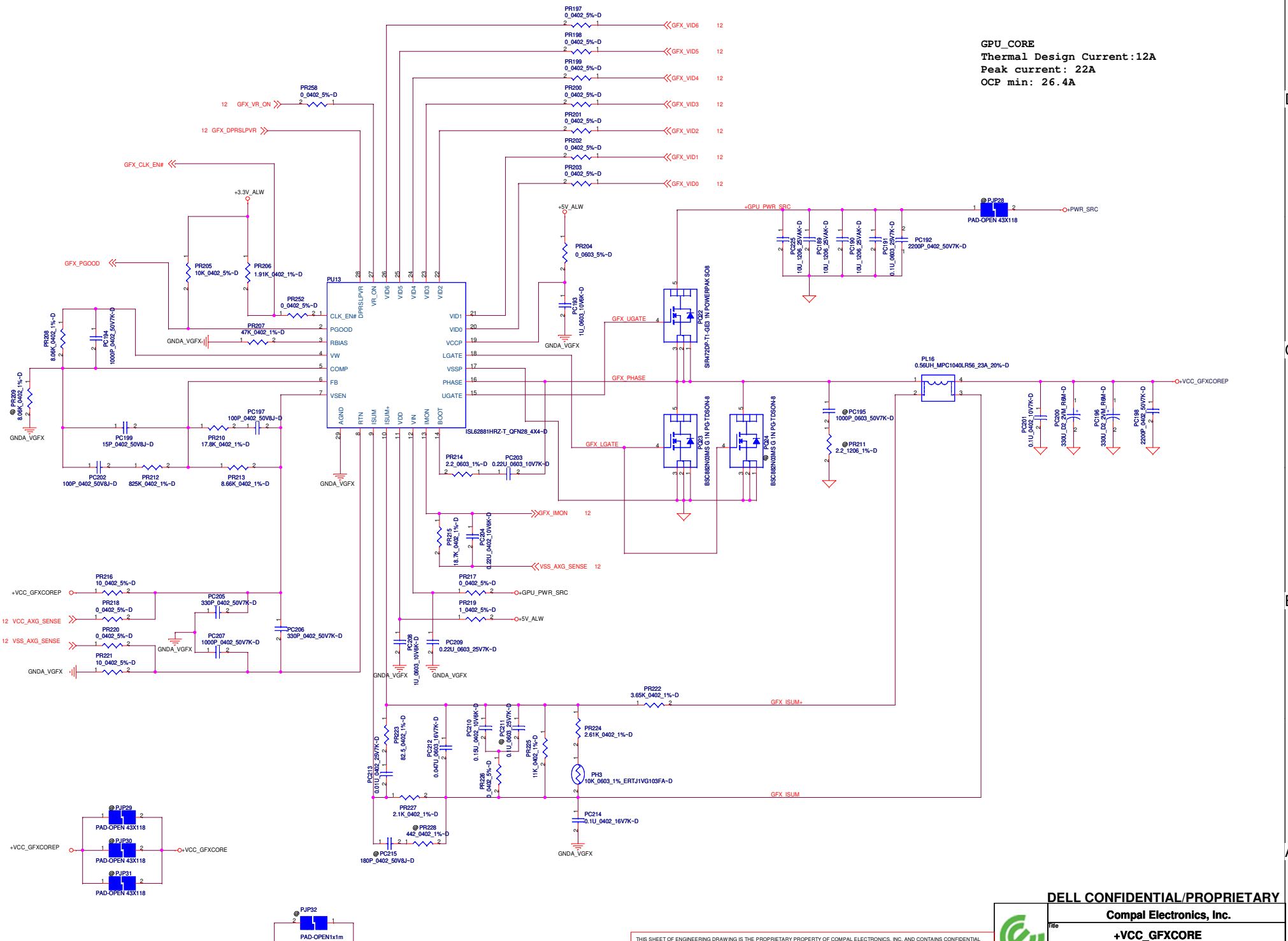
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1.05 Volt +/-5%
Thermal Design Current: 1.51A
Peak current: 2.17A

+1.05V_M/+1.05VTT_RUN

1.05 Volt +/-5%
Thermal Design Current: 15.9A
Peak current: 22.7A



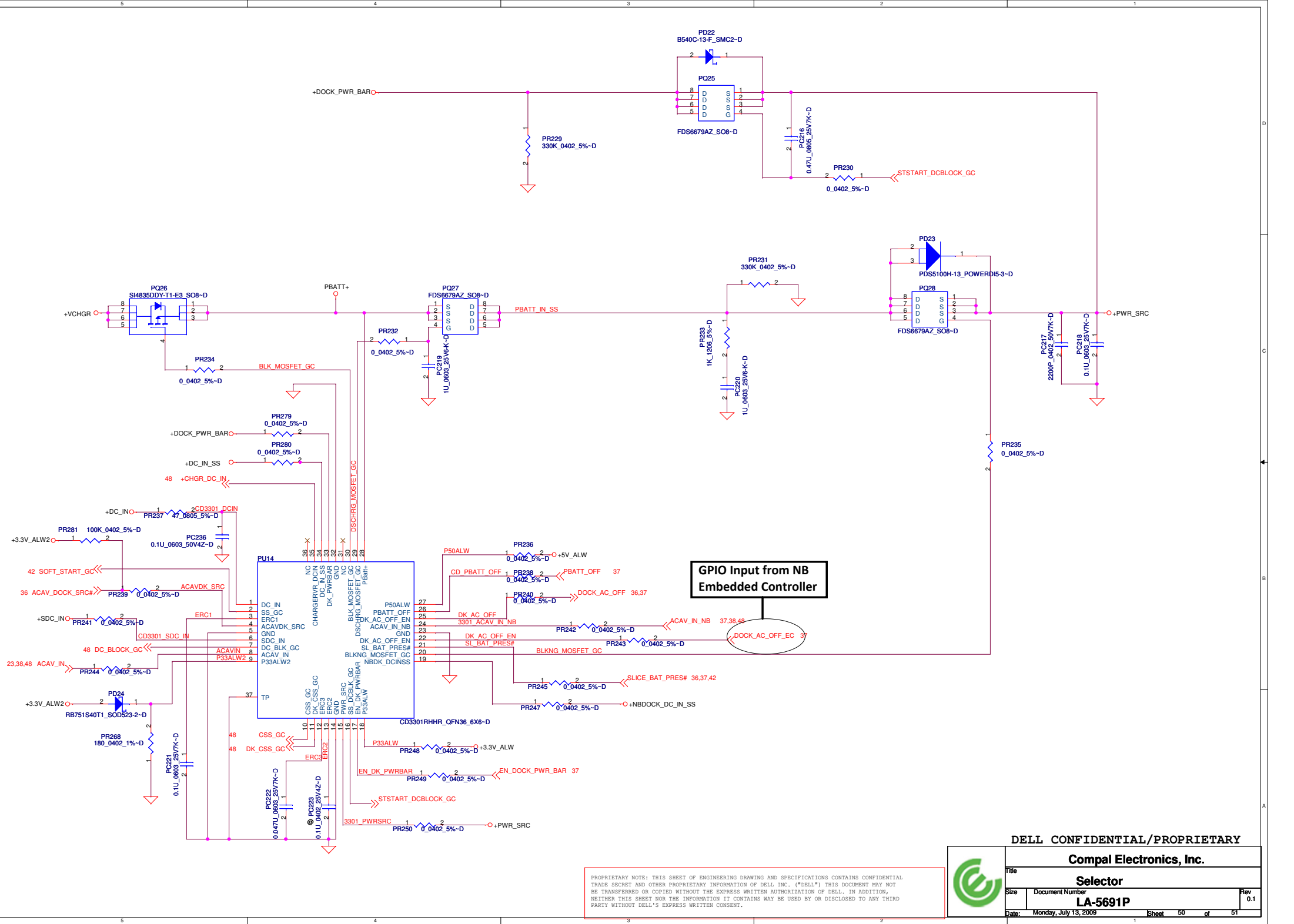


GPU_CORE
Thermal Design Current:12A
Peak current: 22A
OCP min: 26.4A

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