

JSKAA

Irving 10 / 10G

LA4161P REV 1.0 Schematic

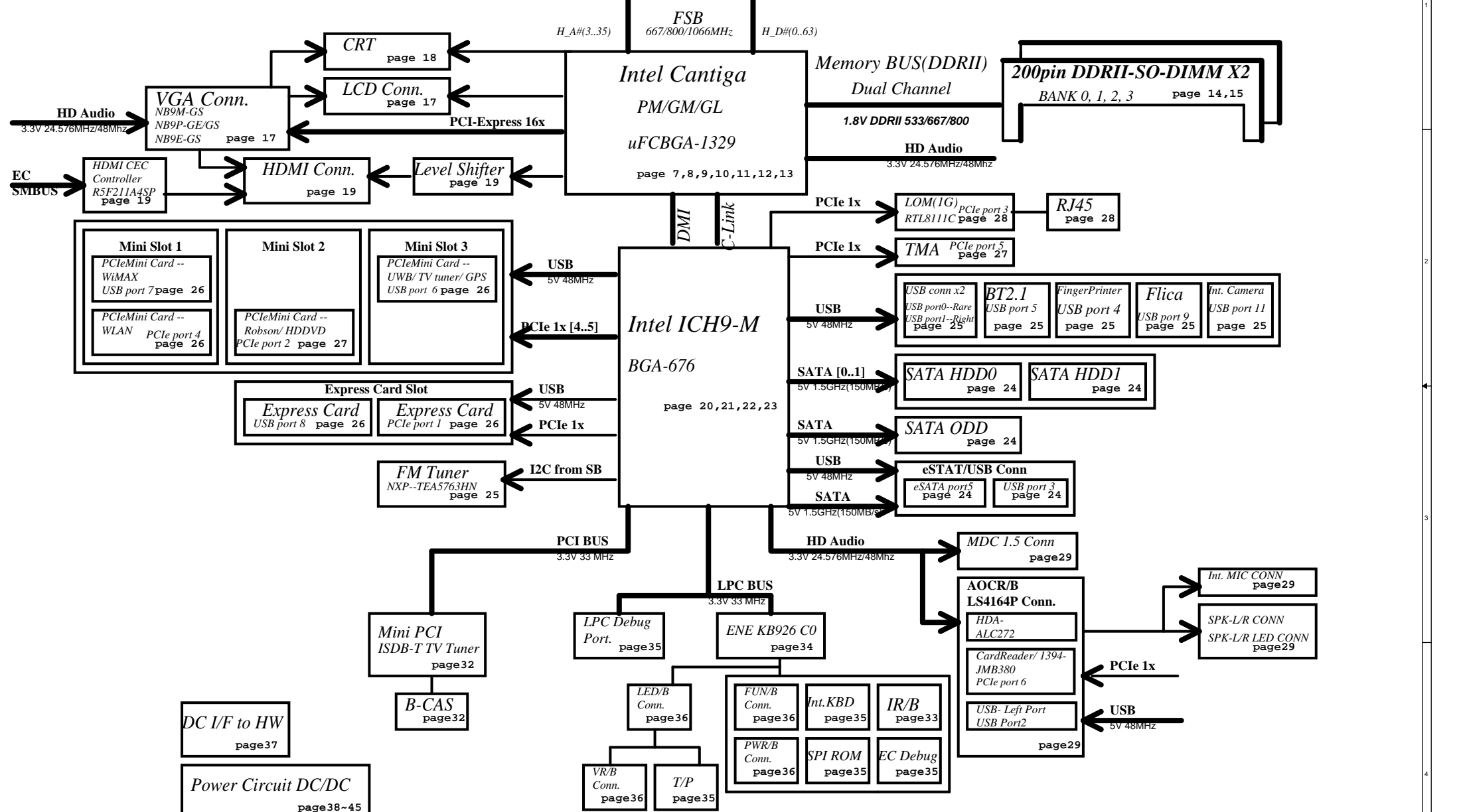
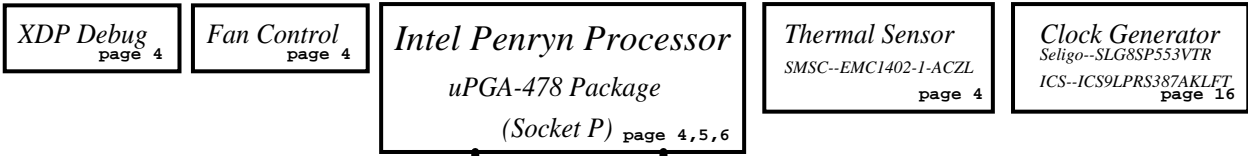
Intel Penryn/ Cantiga (GL45/GM45/PM45)/ ICH9M
2008-10-01 Rev. 1.0

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Compal Confidential

Model Name : JSKAA

File Name :



Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
PCI TV Tuner	AD18 (Master) AD19 (Slave)	1/1 (Master) 2/2 (Slave)	PIRQG (Master) PIRQH (Slave)

EC SM Bus1 address

EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+5VL	EC KB926 C0		+3VS	EC KB926 C0	
+5VL	Smart Battery	0001 01X b	+3VS	CPU THM Sen. SMSC	1001 100x b
+5VL	HDMI-CEC	0011 010x b	+3VS	EMC1402-1-ACZL-TR	1001 1110 b
+5VL	FUN/B (CAP Sensor)		+3VS	VGA THM Sen. nVidia	1001 1110 b

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	Vertical I2C

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH	HIGH
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW	LOW
G3		LOW	LOW	LOW	LOW

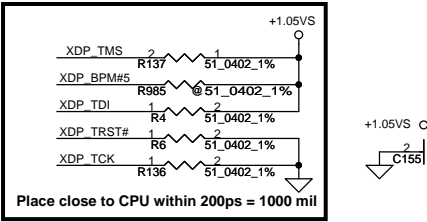
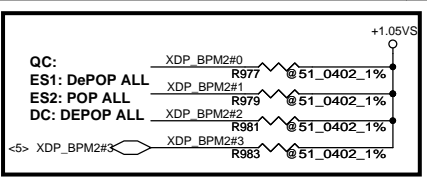
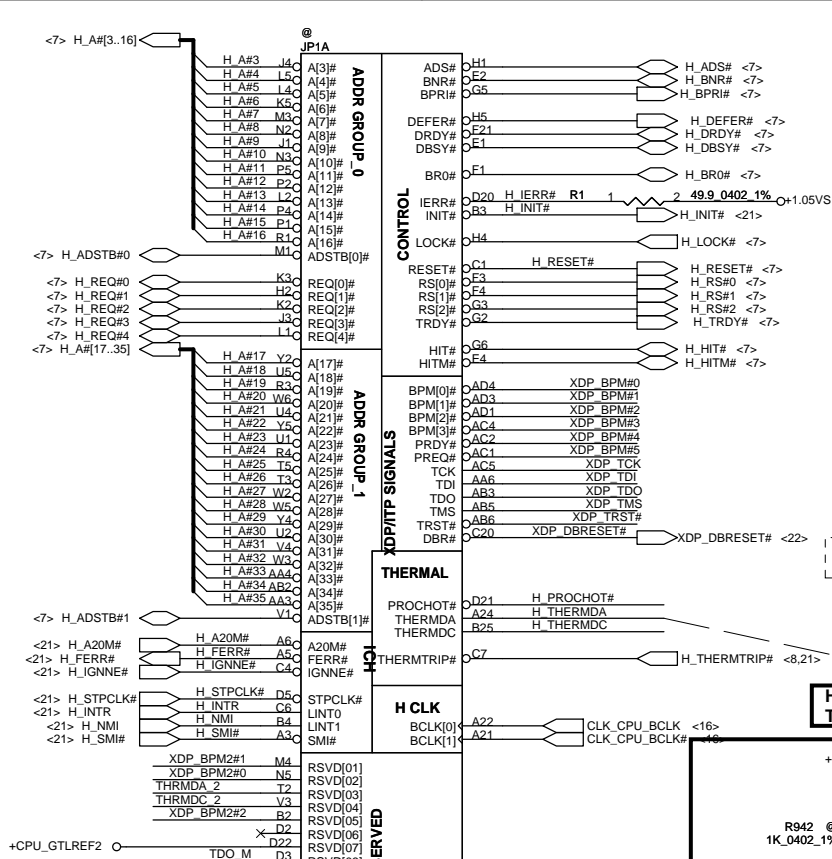
Reserve for AD channel define.

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BTO Option Table

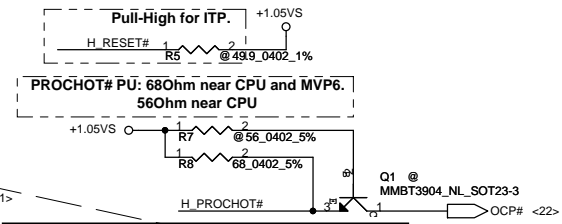
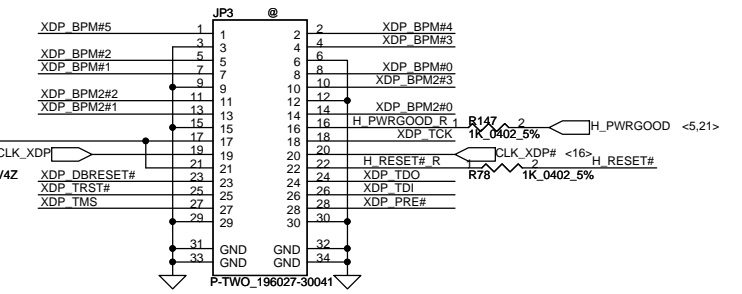
BTO Item	BOM Structure

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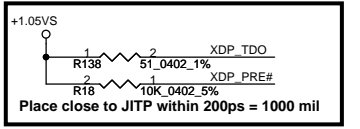


DVT- Change CPU Debug port.

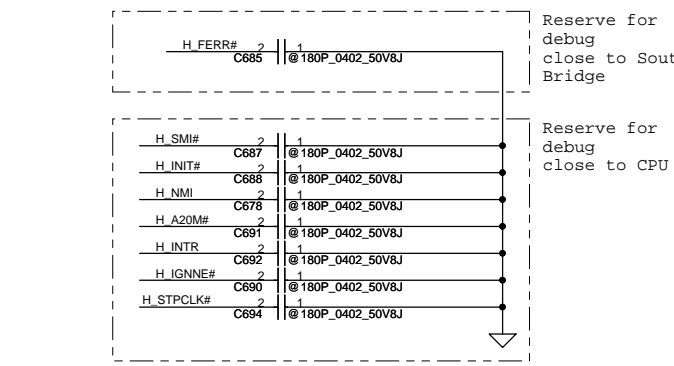
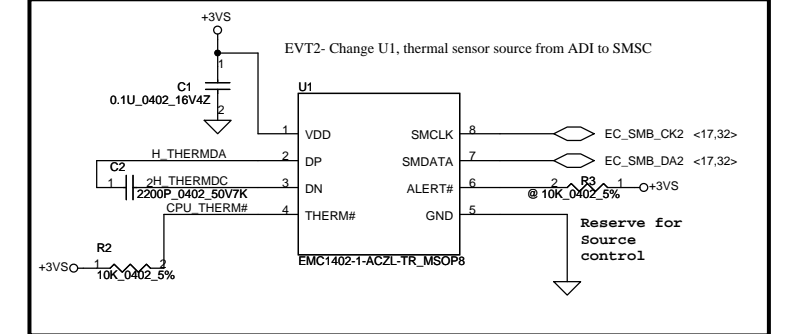
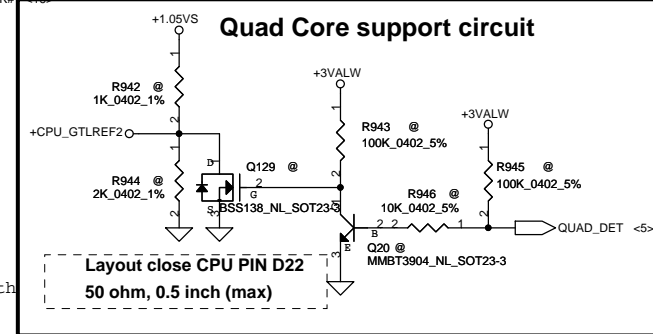
XDP Connector



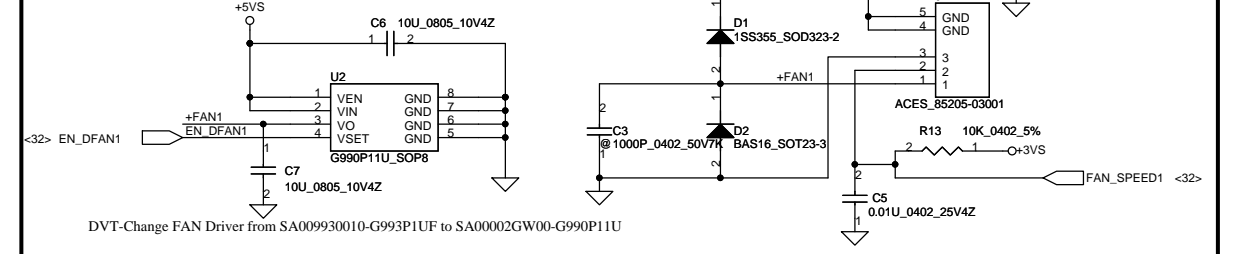
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



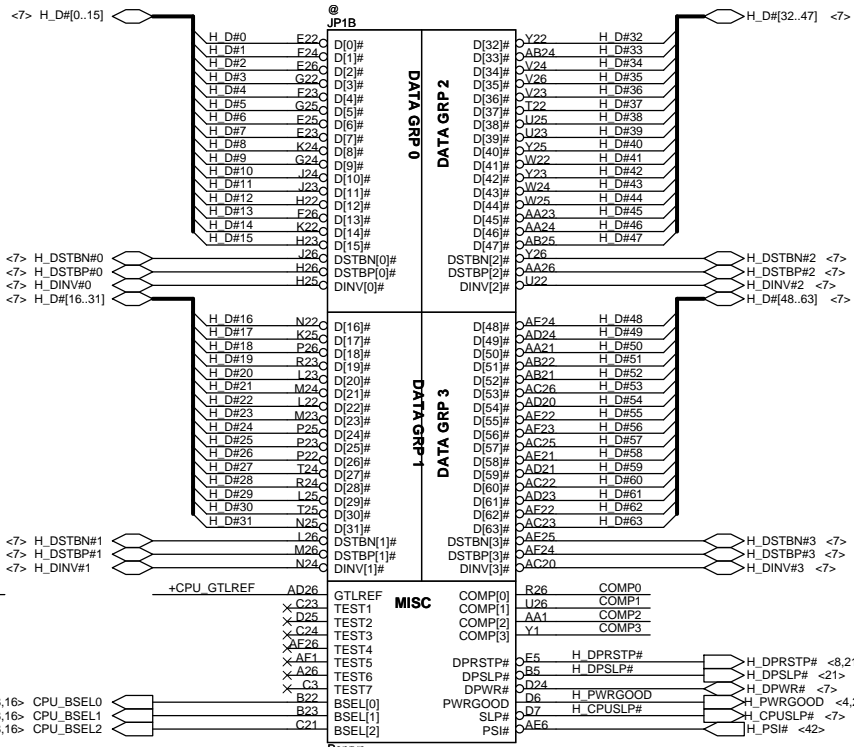
QC: POP @ R984
DC: DEPOP @ 51_0402_1%



FAN Control Circuit



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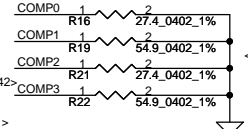
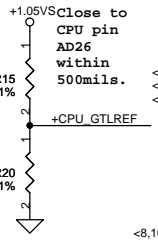
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

D8 pin Reserved for QC

AA8 pin Reserved for QC

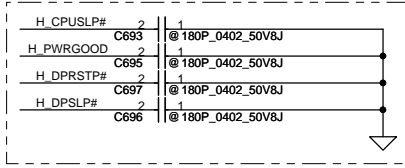
AC8 pin Reserved for QC

XDP_BPM2#3 <-> For QC



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

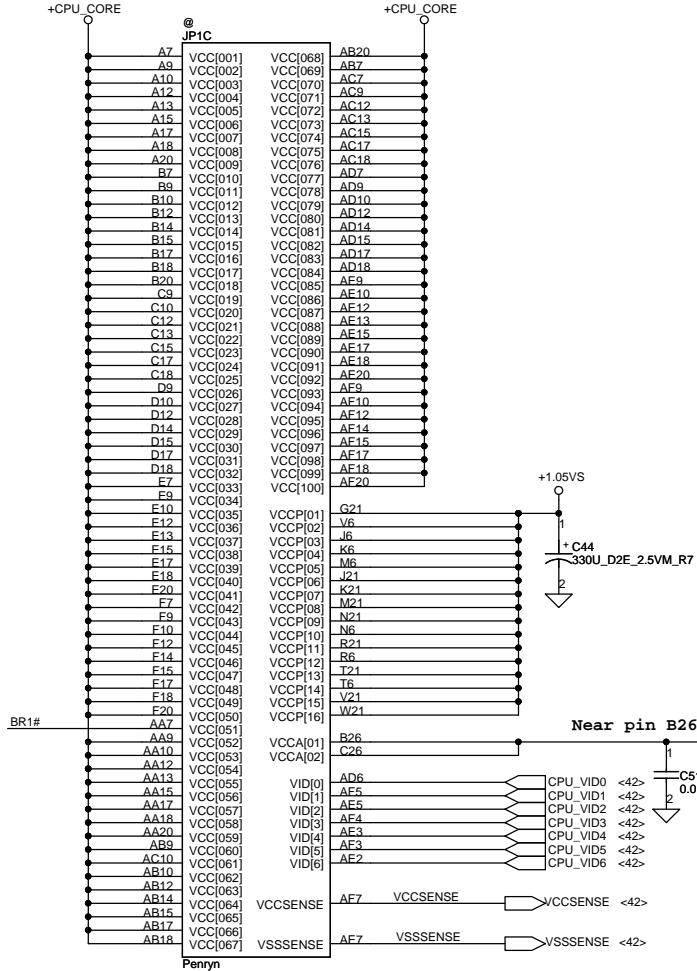
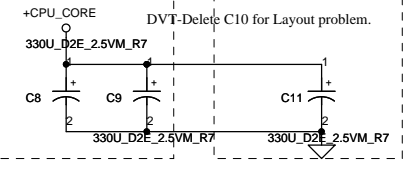
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



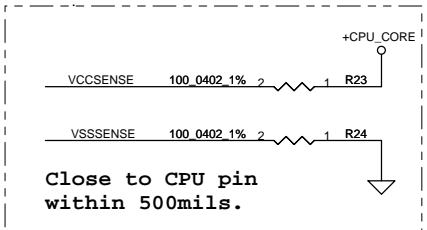
Reserve for debug close to CPU

Near CPU CORE regulator

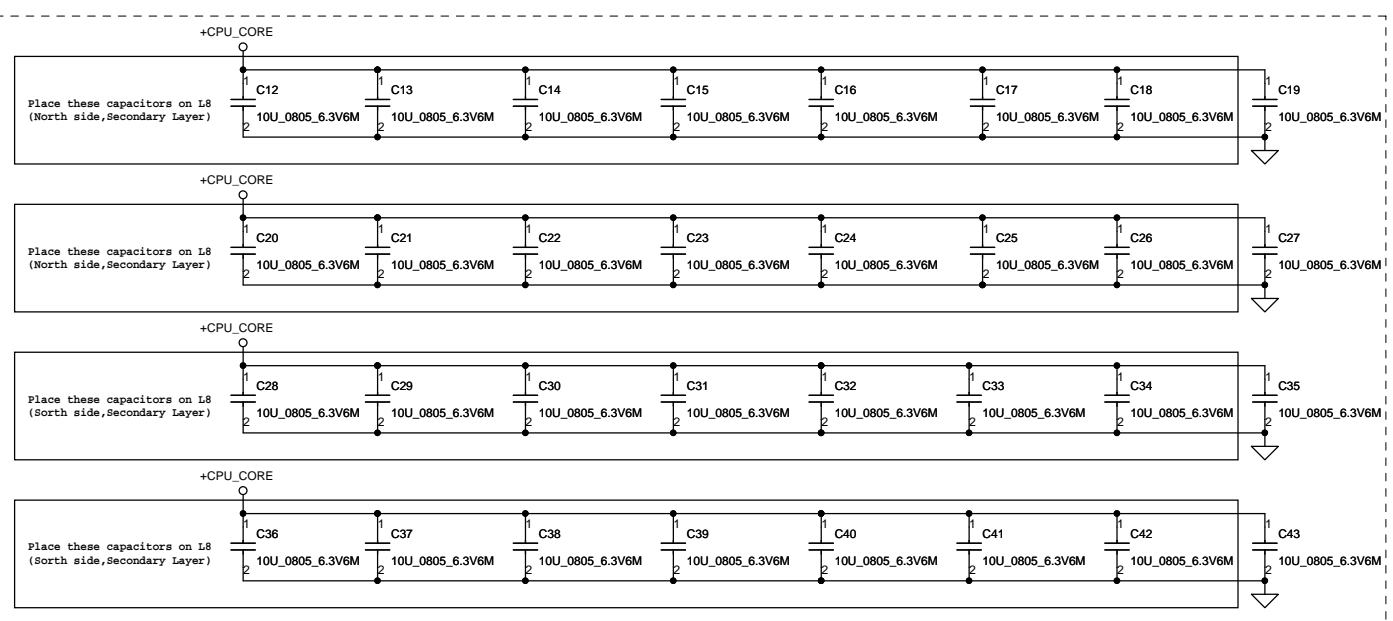
**ESR <= 1.5m ohm
Capacitor > 1980uF**



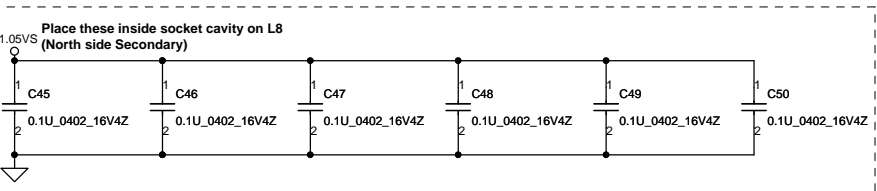
BR1#



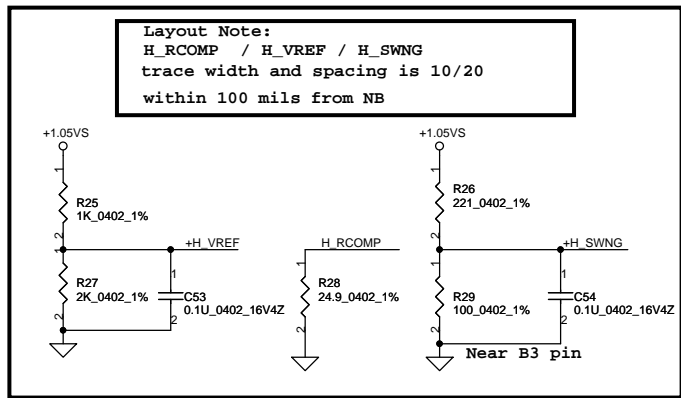
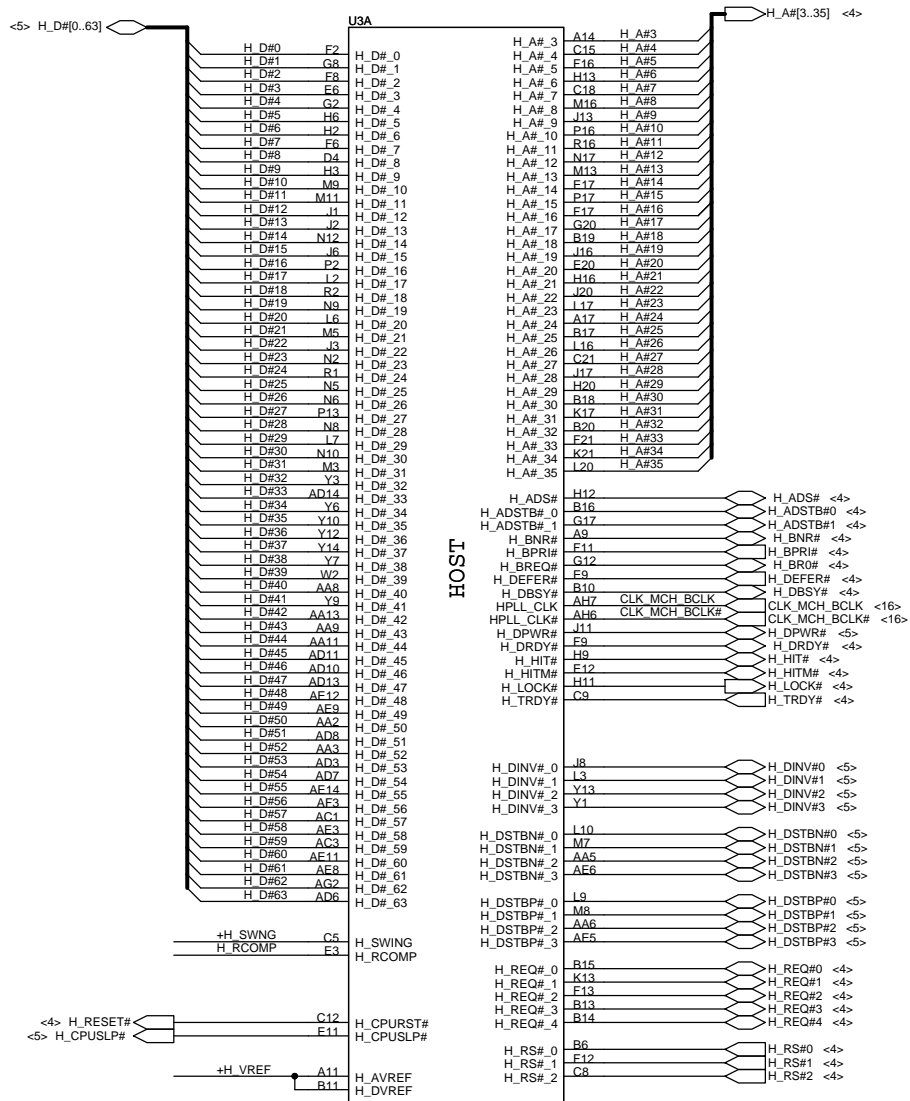
**Length match within 25 mils.
The trace width/space/other is
20/7/25.**



Mid Frequency Decoupling



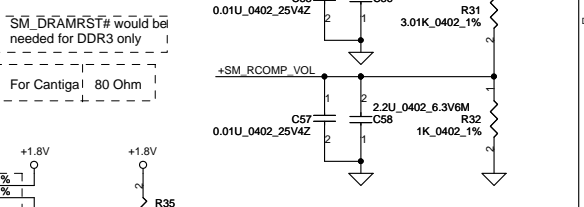
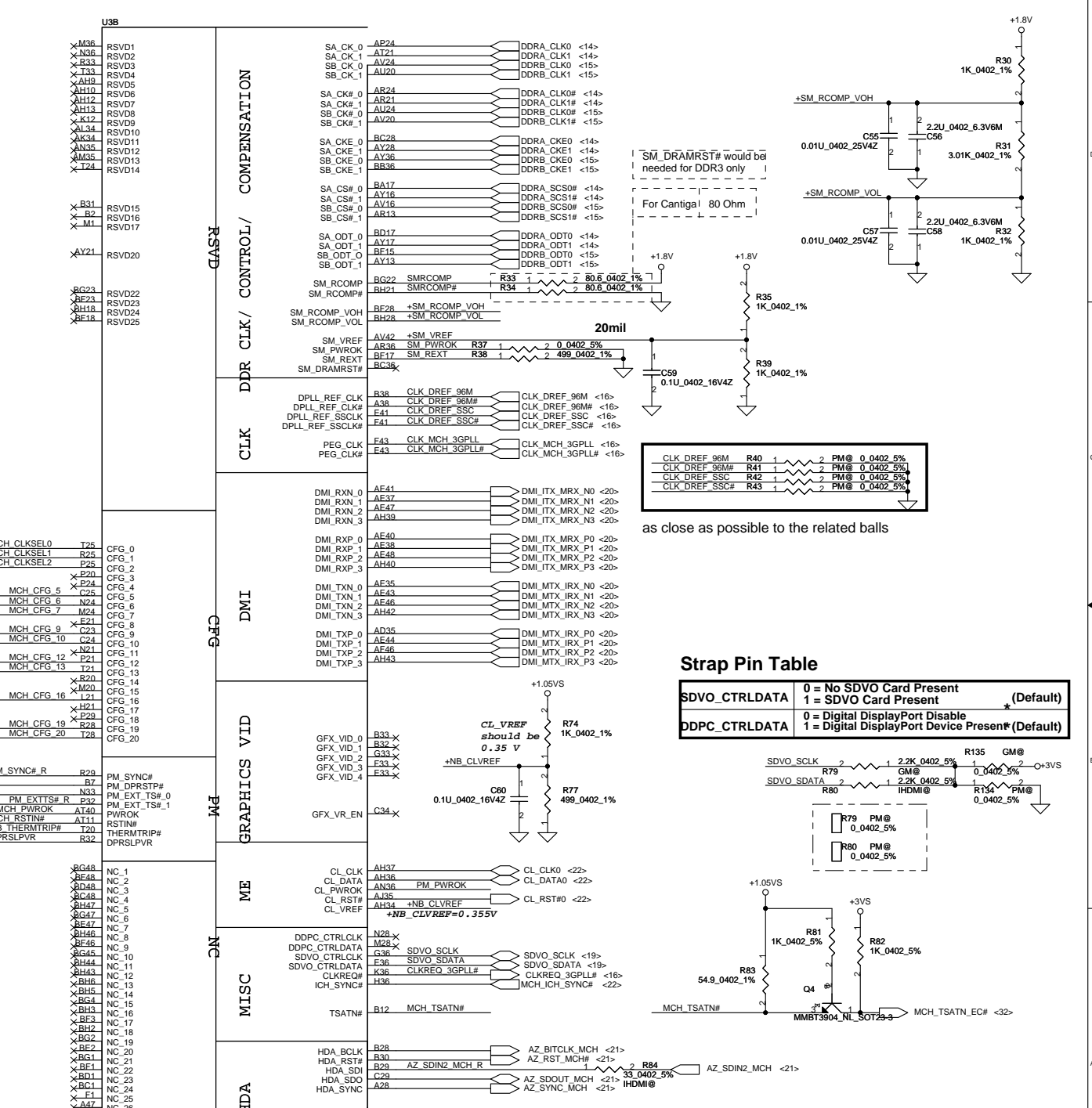
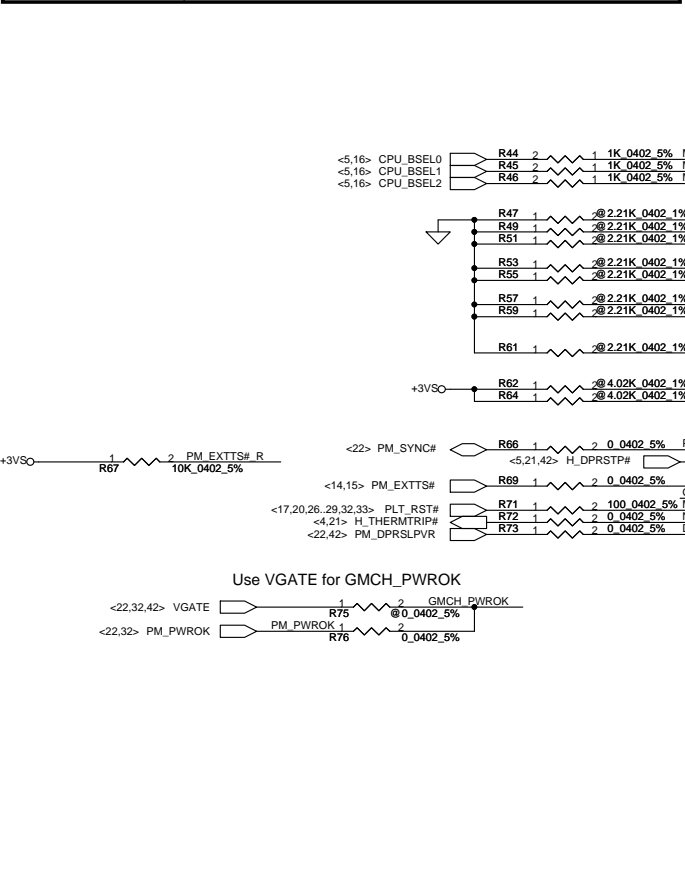
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Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	0 = iTPM Host Interface is enabled*(Default) - can support disable by SW. 1 = iTPM Host Interface is Disabled
CFG7	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable *(Default)
CFG[13:12]	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.

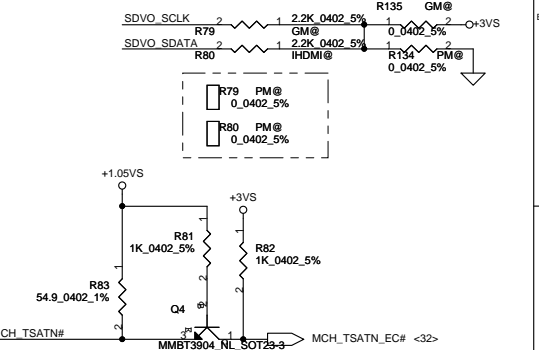


CLK_DREF_96M	R40	1	2	PM@	0.0402 5%
CLK_DREF_96M#	R41	1	2	PM@	0.0402 5%
CLK_DREF_SSC#	R42	1	2	PM@	0.0402 5%
CLK_DREF_SSC#	R43	1	2	PM@	0.0402 5%

as close as possible to the related balls

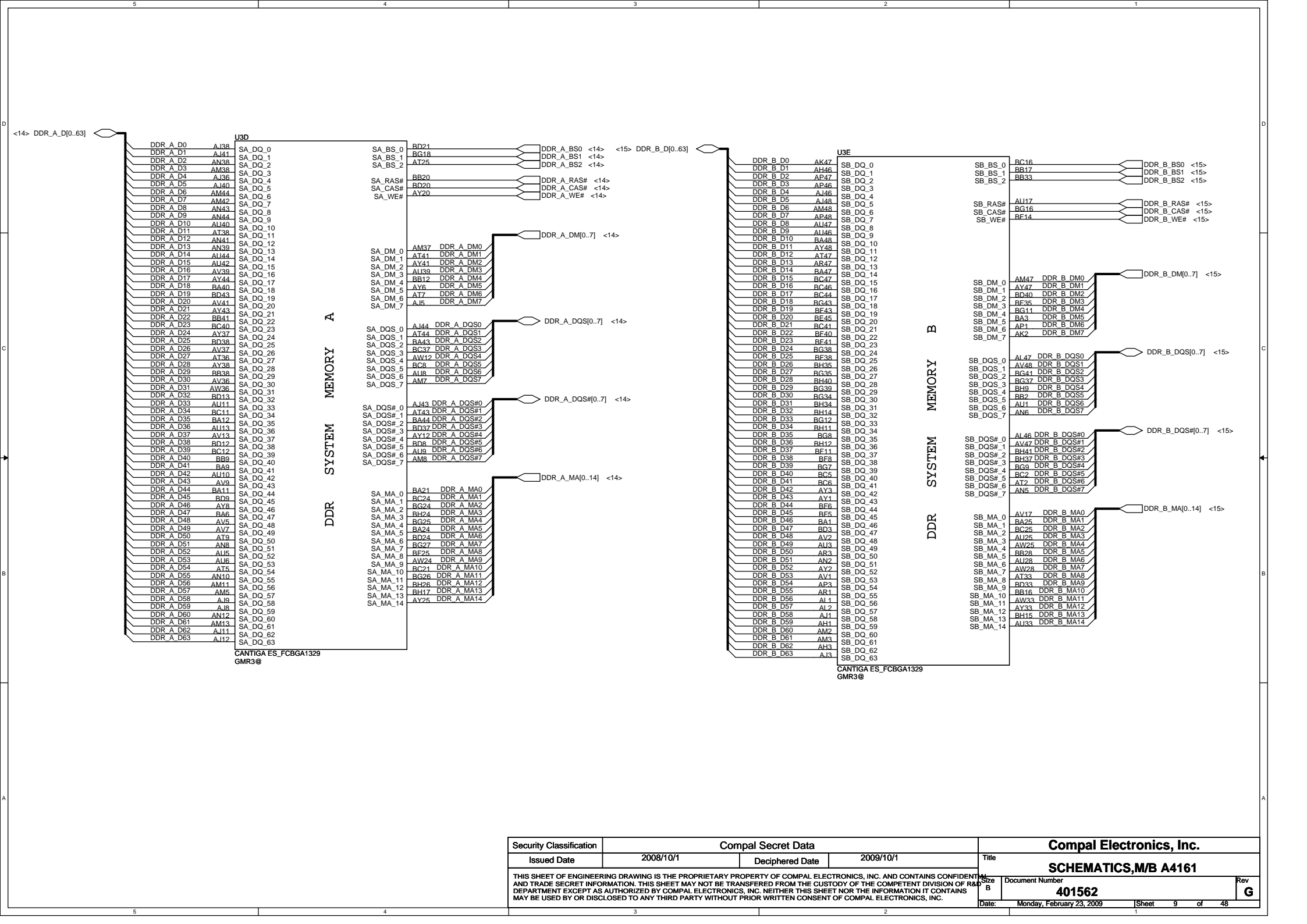
Strap Pin Table

SDVO_CTRLDATA	0 = No SDVO Card Present 1 = SDVO Card Present *(Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present*(Default)



CANTIGA ES_FCBGA1329
GMR3@

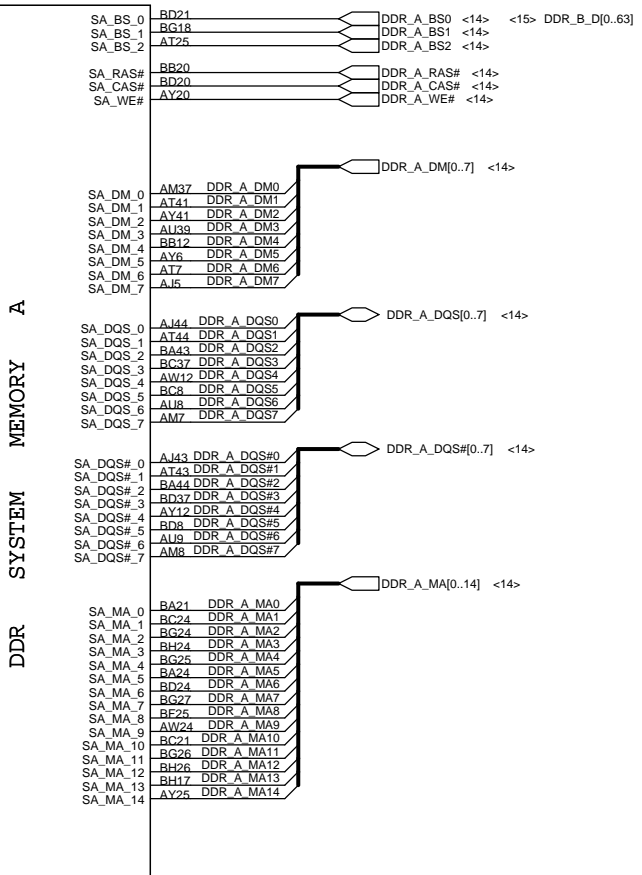
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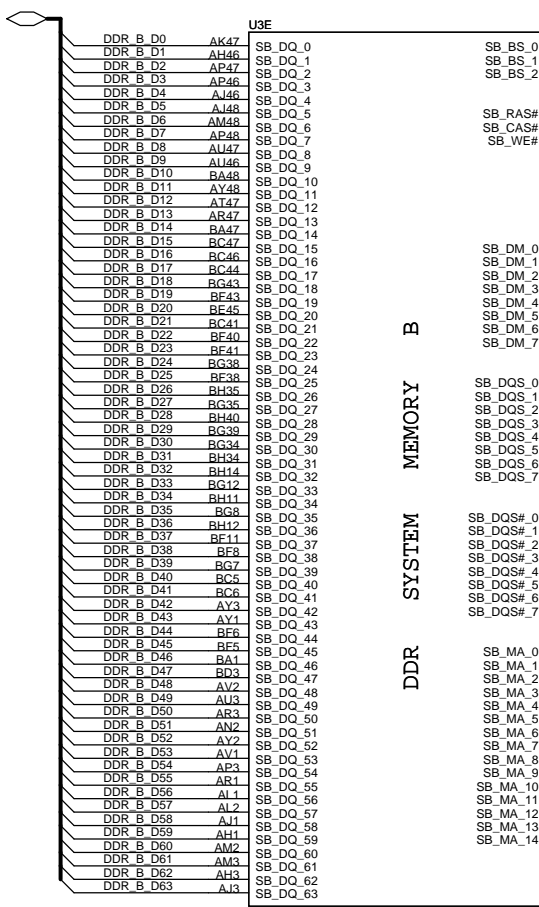
<14> DDR_A_D[0..63]

- DDR A D0 AJ38 SA_DQ_0
- DDR A D1 AJ41 SA_DQ_1
- DDR A D2 AN38 SA_DQ_2
- DDR A D3 AM38 SA_DQ_3
- DDR A D4 AJ36 SA_DQ_4
- DDR A D5 AJ40 SA_DQ_5
- DDR A D6 AM44 SA_DQ_6
- DDR A D7 AM42 SA_DQ_7
- DDR A D8 AN43 SA_DQ_8
- DDR A D9 AN44 SA_DQ_9
- DDR A D10 AU40 SA_DQ_10
- DDR A D11 AT38 SA_DQ_11
- DDR A D12 AN41 SA_DQ_12
- DDR A D13 AN39 SA_DQ_13
- DDR A D14 AU44 SA_DQ_14
- DDR A D15 AU42 SA_DQ_15
- DDR A D16 AV39 SA_DQ_16
- DDR A D17 AY44 SA_DQ_17
- DDR A D18 BA40 SA_DQ_18
- DDR A D19 BD43 SA_DQ_19
- DDR A D20 AV41 SA_DQ_20
- DDR A D21 AY43 SA_DQ_21
- DDR A D22 BB41 SA_DQ_22
- DDR A D23 BC40 SA_DQ_23
- DDR A D24 BD38 SA_DQ_24
- DDR A D25 AY47 SA_DQ_25
- DDR A D26 AV37 SA_DQ_26
- DDR A D27 AT36 SA_DQ_27
- DDR A D28 AY38 SA_DQ_28
- DDR A D29 BB38 SA_DQ_29
- DDR A D30 AV36 SA_DQ_30
- DDR A D31 AV36 SA_DQ_31
- DDR A D32 BD13 SA_DQ_32
- DDR A D33 AU11 SA_DQ_33
- DDR A D34 BC11 SA_DQ_34
- DDR A D35 BA12 SA_DQ_35
- DDR A D36 AU13 SA_DQ_36
- DDR A D37 AV13 SA_DQ_37
- DDR A D38 BD12 SA_DQ_38
- DDR A D39 BC12 SA_DQ_39
- DDR A D40 BB9 SA_DQ_40
- DDR A D41 BA9 SA_DQ_41
- DDR A D42 AU10 SA_DQ_42
- DDR A D43 AV9 SA_DQ_43
- DDR A D44 BA11 SA_DQ_44
- DDR A D45 BD9 SA_DQ_45
- DDR A D46 AY8 SA_DQ_46
- DDR A D47 BA6 SA_DQ_47
- DDR A D48 AV5 SA_DQ_48
- DDR A D49 AV7 SA_DQ_49
- DDR A D50 AT9 SA_DQ_50
- DDR A D51 AN8 SA_DQ_51
- DDR A D52 AU5 SA_DQ_52
- DDR A D53 AU6 SA_DQ_53
- DDR A D54 AT5 SA_DQ_54
- DDR A D55 AN10 SA_DQ_55
- DDR A D56 AM11 SA_DQ_56
- DDR A D57 AM5 SA_DQ_57
- DDR A D58 AU9 SA_DQ_58
- DDR A D59 AJ8 SA_DQ_59
- DDR A D60 AN12 SA_DQ_60
- DDR A D61 AM13 SA_DQ_61
- DDR A D62 AJ11 SA_DQ_62
- DDR A D63 AJ12 SA_DQ_63

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GMR3@

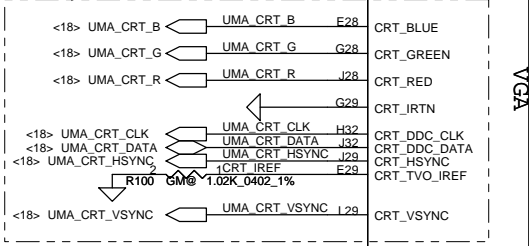
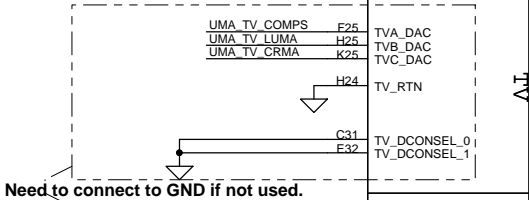
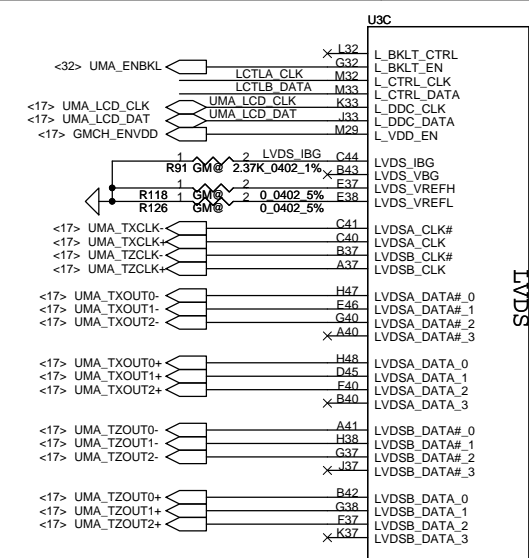
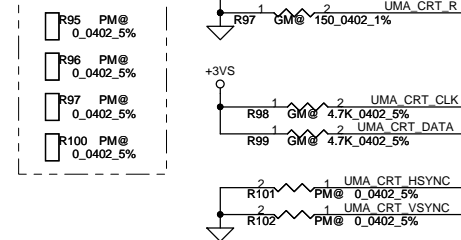
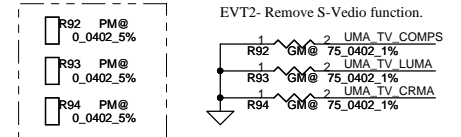
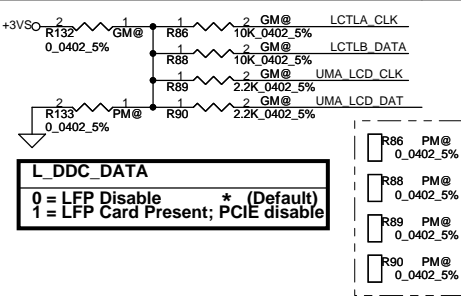


<15> DDR_B_D[0..63]



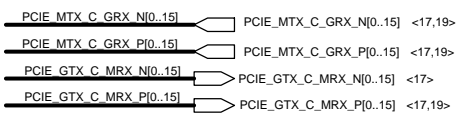
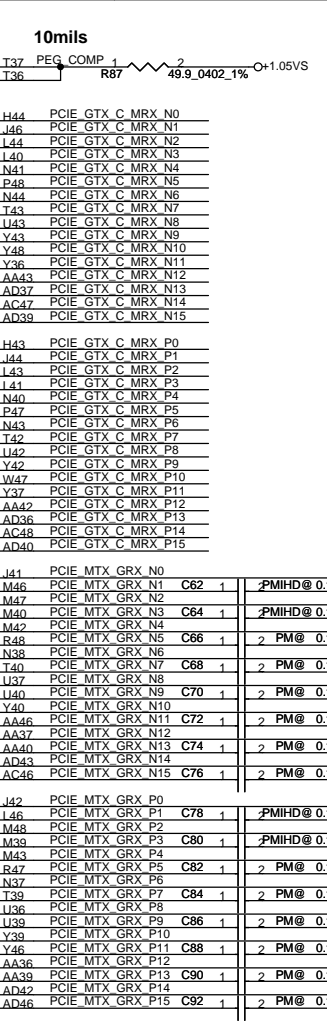
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GMR3@

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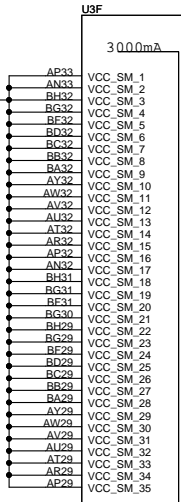
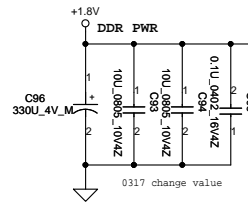
CANTIGEA ES_FCBGA1329
 GMR3@

SCVT
 PCI-EXPRESS
 AT
 VGA



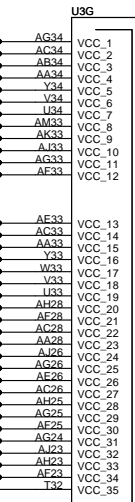
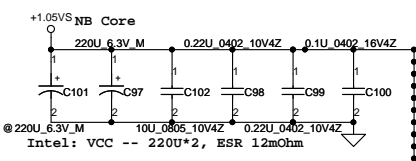
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M46	PCI_E MTX GRX N1	C62	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX N1
M47	PCI_E MTX GRX N2	C63	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX N2
M40	PCI_E MTX GRX N3	C64	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX N3
M42	PCI_E MTX GRX N4	C65	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N4
R48	PCI_E MTX GRX N5	C66	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N5
N38	PCI_E MTX GRX N6	C67	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N6
T40	PCI_E MTX GRX N7	C68	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N7
U37	PCI_E MTX GRX N8	C69	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N8
U40	PCI_E MTX GRX N9	C70	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N9
Y40	PCI_E MTX GRX N10	C71	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N10
AA46	PCI_E MTX GRX N11	C72	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N11
AA37	PCI_E MTX GRX N12	C73	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N12
AA40	PCI_E MTX GRX N13	C74	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N13
AD43	PCI_E MTX GRX N14	C75	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N14
AD46	PCI_E MTX GRX N15	C76	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX N15
J42	PCI_E MTX GRX P0	C77	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX P0
L46	PCI_E MTX GRX P1	C78	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX P1
M48	PCI_E MTX GRX P2	C79	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX P2
M39	PCI_E MTX GRX P3	C80	1	PMIHD@ 0.1U_0402_16V7K	PCI_E MTX C GRX P3
M43	PCI_E MTX GRX P4	C81	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P4
R47	PCI_E MTX GRX P5	C82	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P5
N37	PCI_E MTX GRX P6	C83	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P6
T39	PCI_E MTX GRX P7	C84	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P7
U36	PCI_E MTX GRX P8	C85	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P8
U29	PCI_E MTX GRX P9	C86	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P9
Y39	PCI_E MTX GRX P10	C87	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P10
Y46	PCI_E MTX GRX P11	C88	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P11
AA36	PCI_E MTX GRX P12	C89	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P12
AA39	PCI_E MTX GRX P13	C90	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P13
AD42	PCI_E MTX GRX P14	C91	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P14
AD46	PCI_E MTX GRX P15	C92	1	PM@ 0.1U_0402_16V7K	PCI_E MTX C GRX P15

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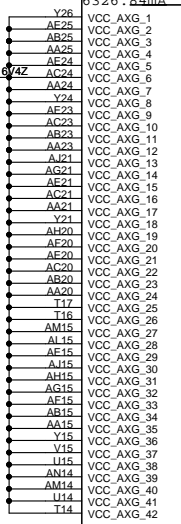
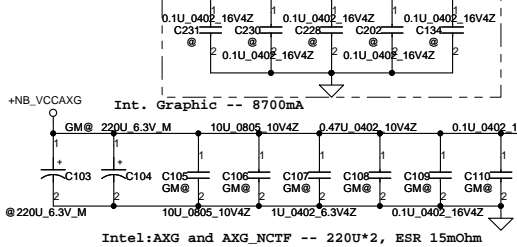
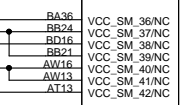
+NB_VCCAXG
Int. Graphic Core -- 8700mA

Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



VCC CORE
POWER

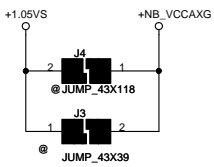
Could be NC for DDR2 Board.



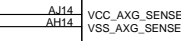
POWER
VCC GFX NCTF
VCC DDA
X4E DDA

C106 PM@
0.0805_5%

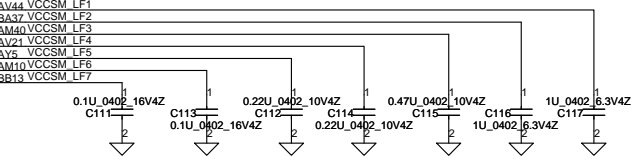
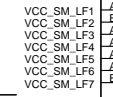
DVT-R707 change to J3. and R693 and R697. change to J4 for power rating issue.



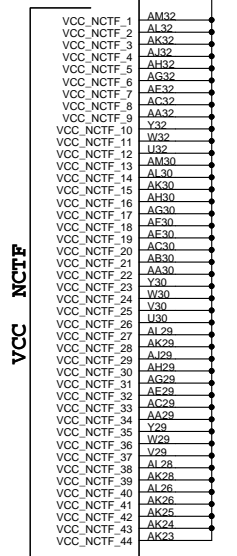
PAD T3
PAD T4



VCC SM LF



CANTIGA ES_FCBGA1329
GMR3@

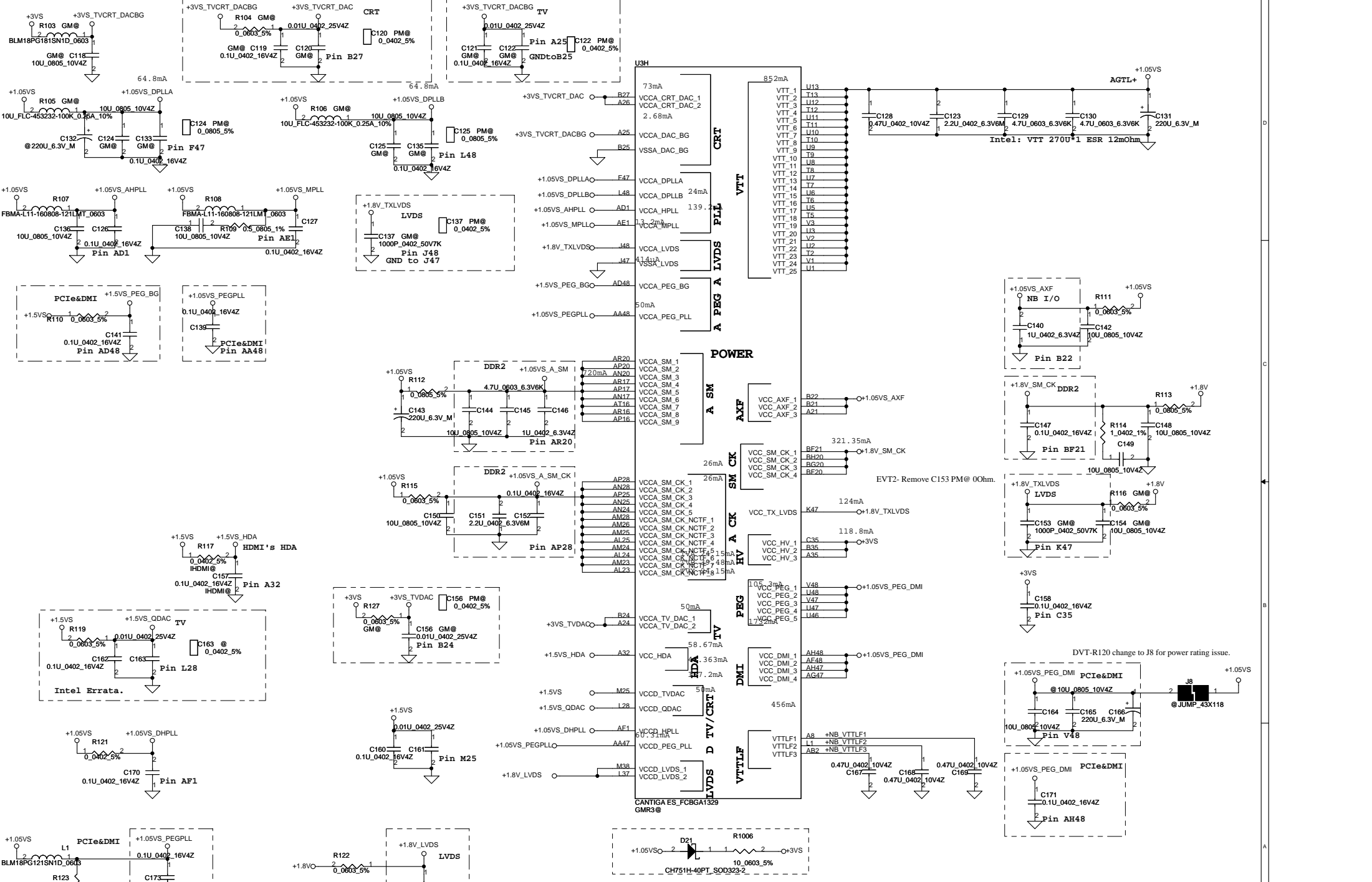


VCC NCTF

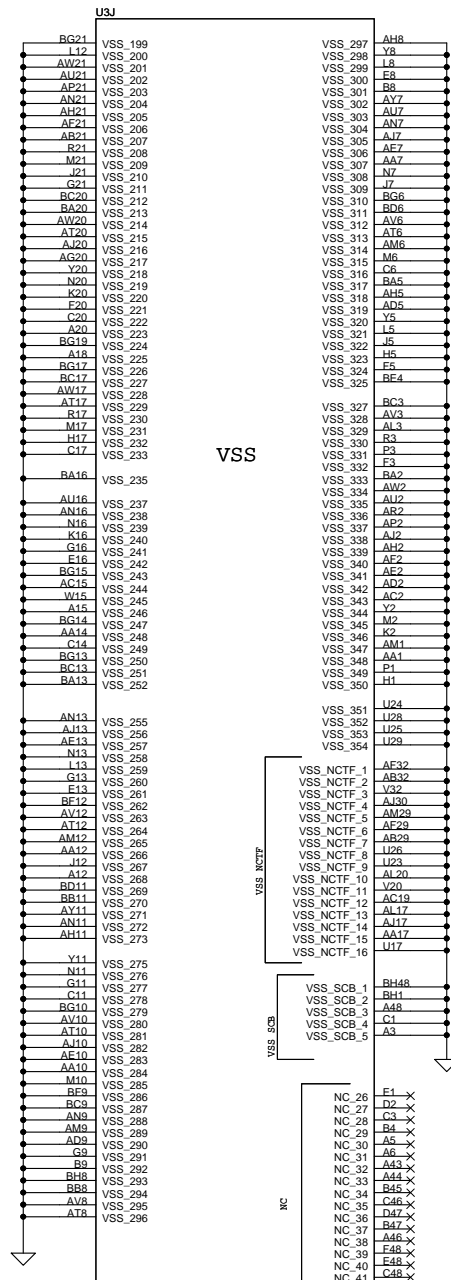
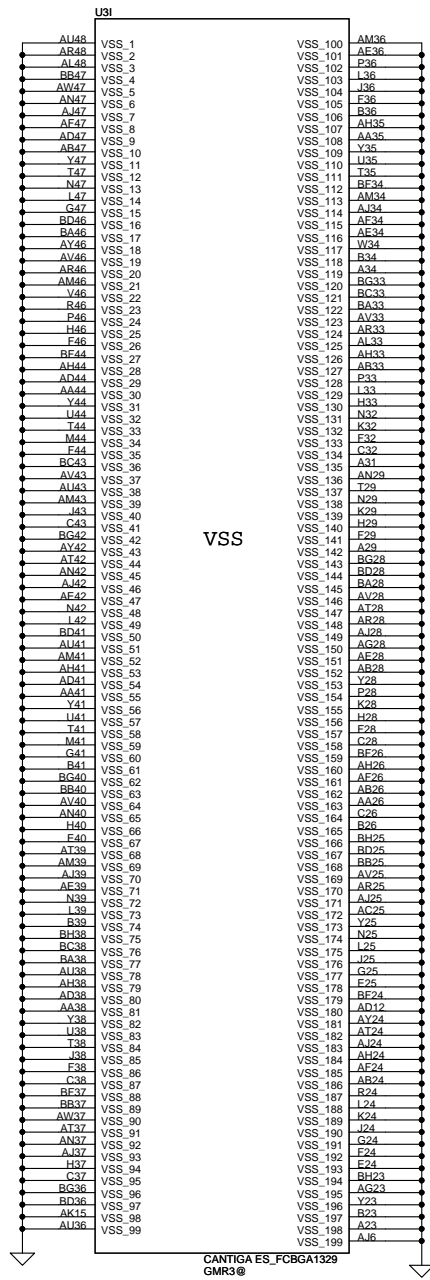
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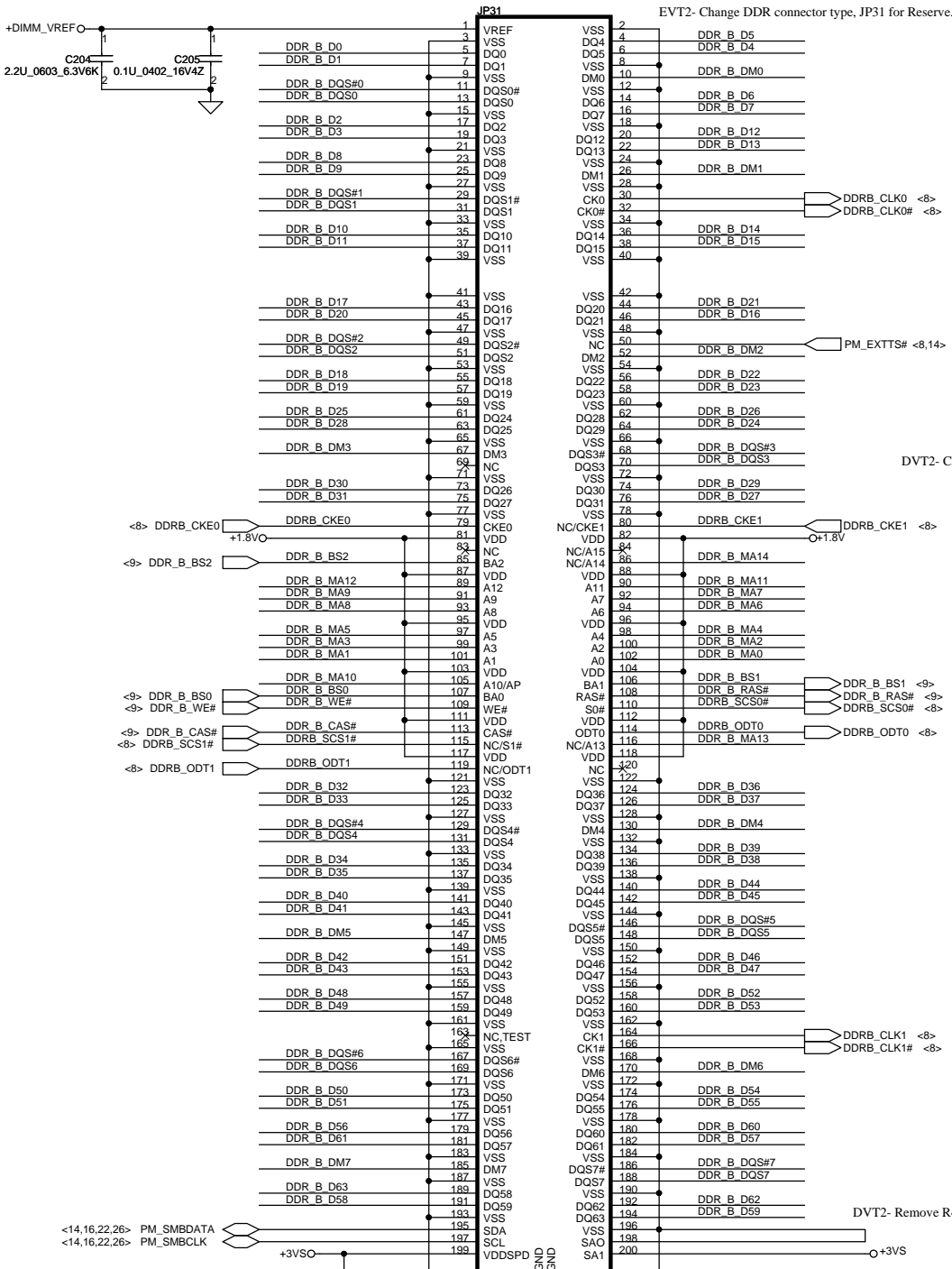
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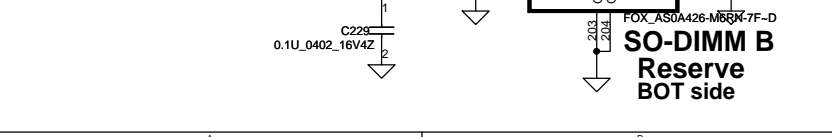
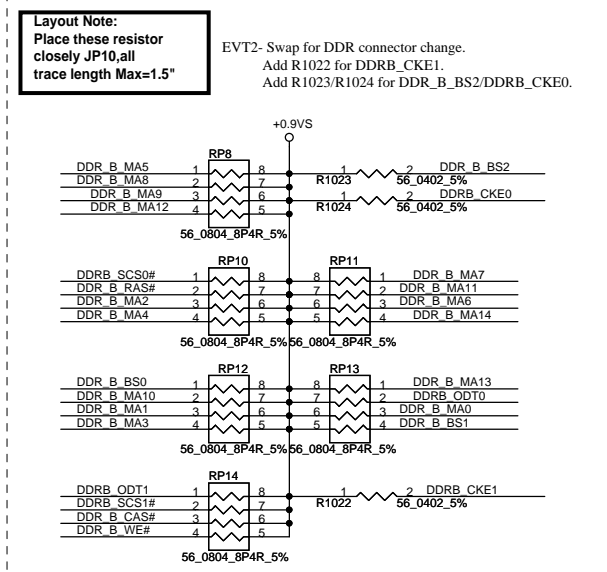
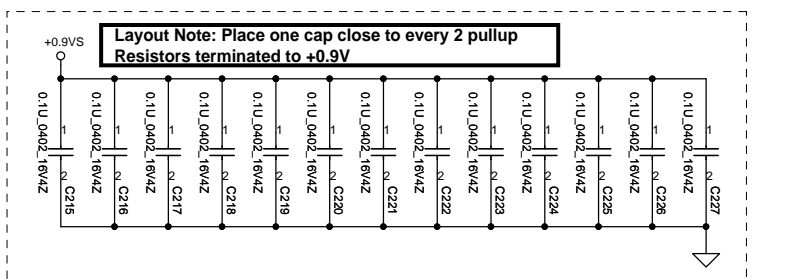
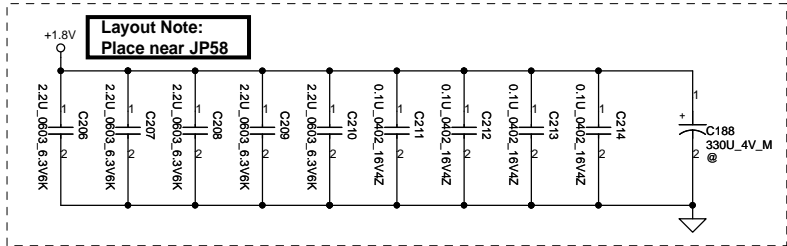
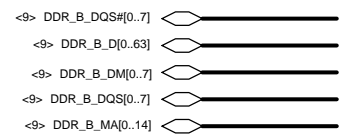
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EVT2- Change DDR connector type, JP31 for Reserve.

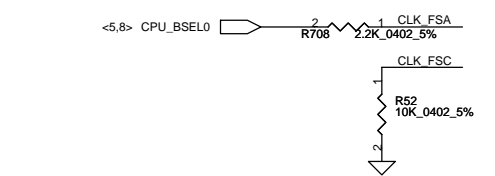
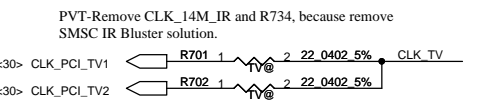
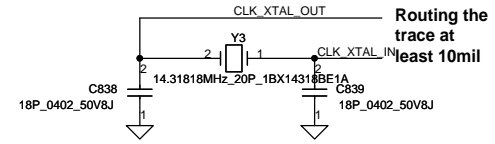
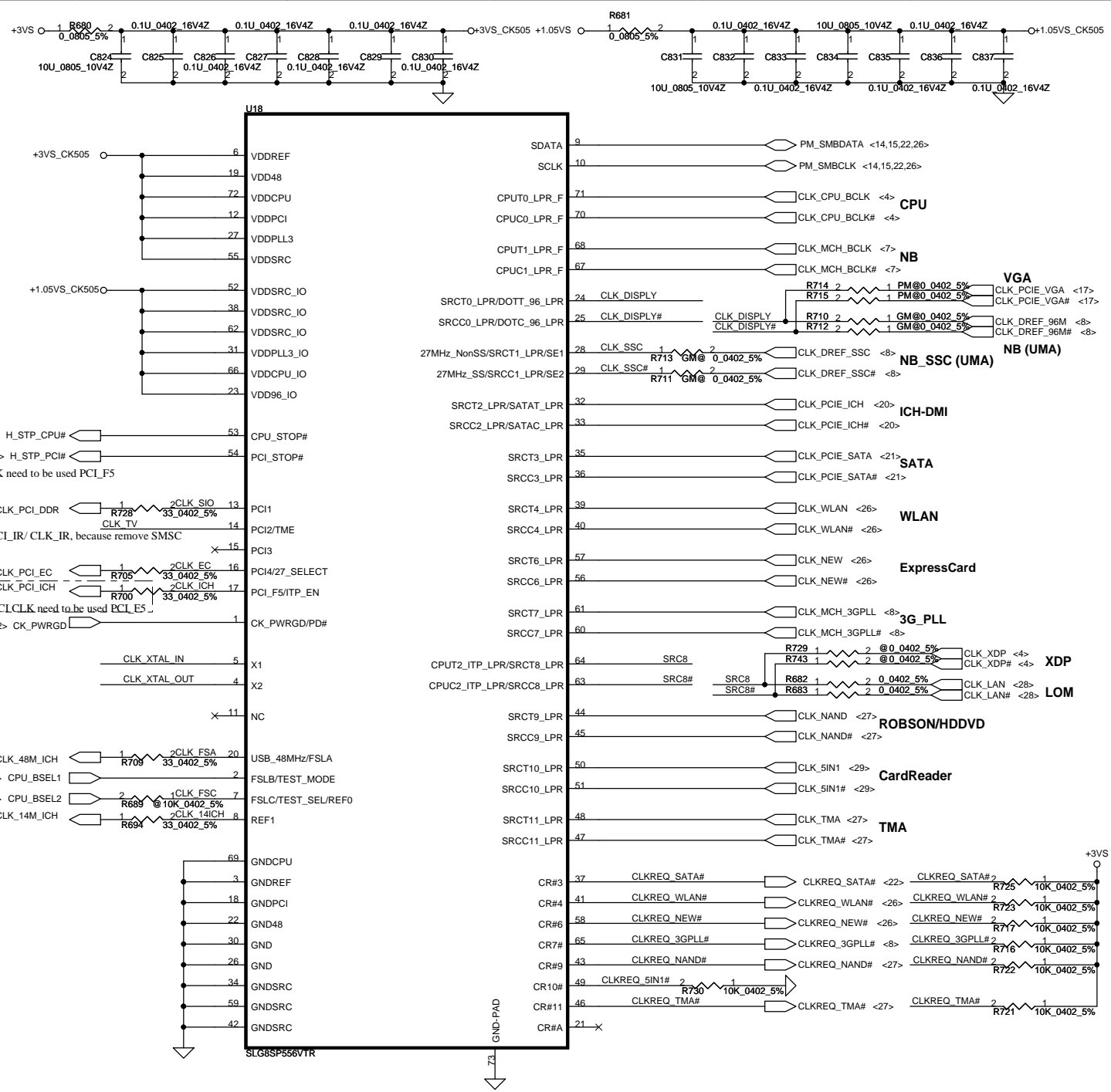
DVT2- Change +0.9V to +0.9VS

DVT2- Remove R407/R408 of DDR address resistors.



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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



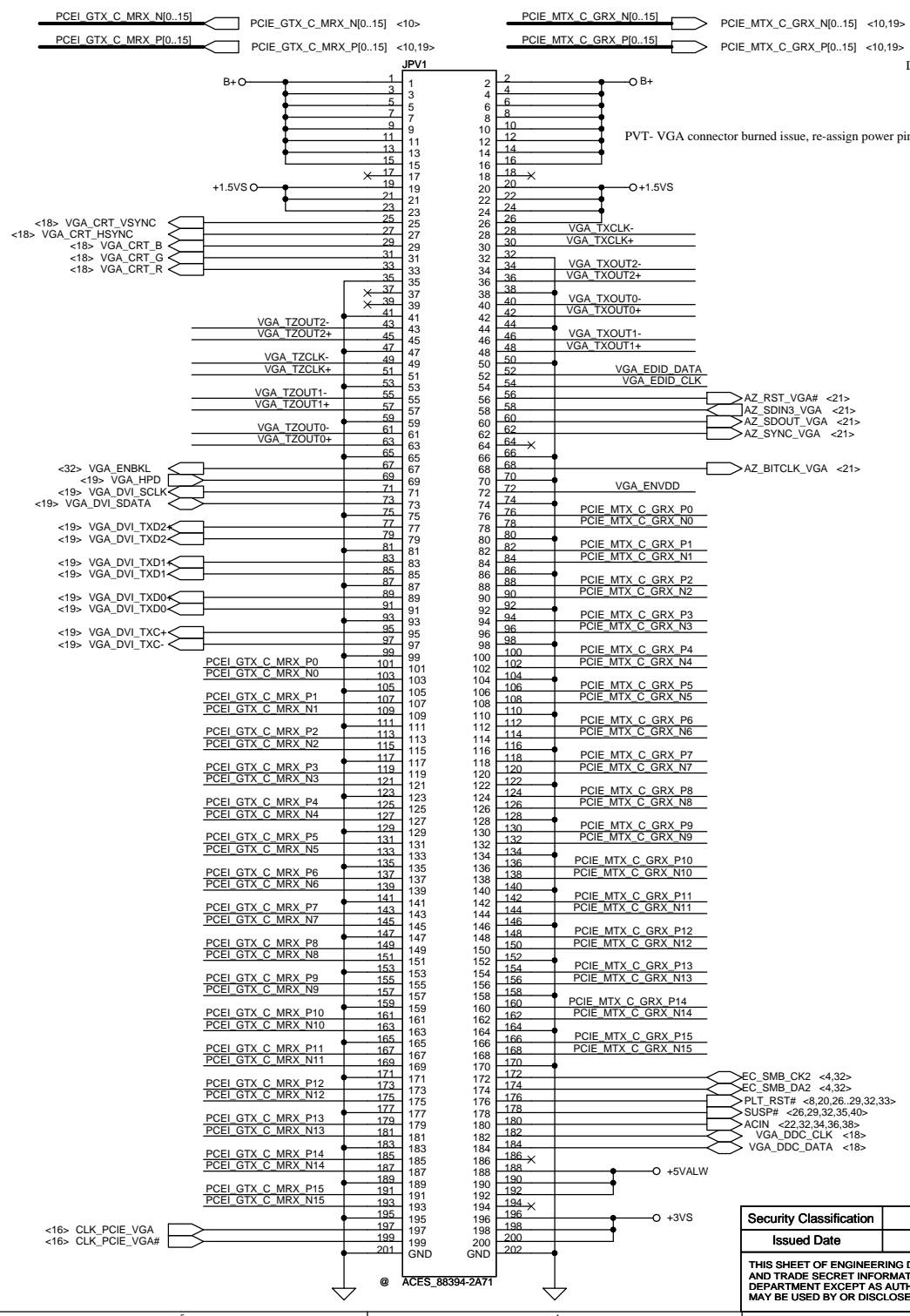
- <22> H_STP_CPU#
- <22> H_STP_PCI#
- EVT2- ICH PCI CLK need to be used PCI_F5
- <33> CLK_PCI_DDR
- PVT-Delete CLK_PCI_IR/ CLK_IR, because remove SMSC IR Bluster solution.
- <32> CLK_PCI_EC
- <20> CLK_PCI_ICH
- EVT2- ICH PCI CLK need to be used ECL_E5
- <22> CK_PWRGD
- CLK_XTAL_IN
- CLK_XTAL_OUT
- NC
- <22> CLK_48M_ICH
- <5,8> CPU_BSEL1
- <5,8> CPU_BSEL2
- <22> CLK_14M_ICH

CLK_ICH	0 = SRC8/SRC8# 1 = ITP/ITP#
CLK_EC	0 = Enable DOT96 & SRC1 (UMA) 1 = Enable SRC0 & 27MHz (DIS)

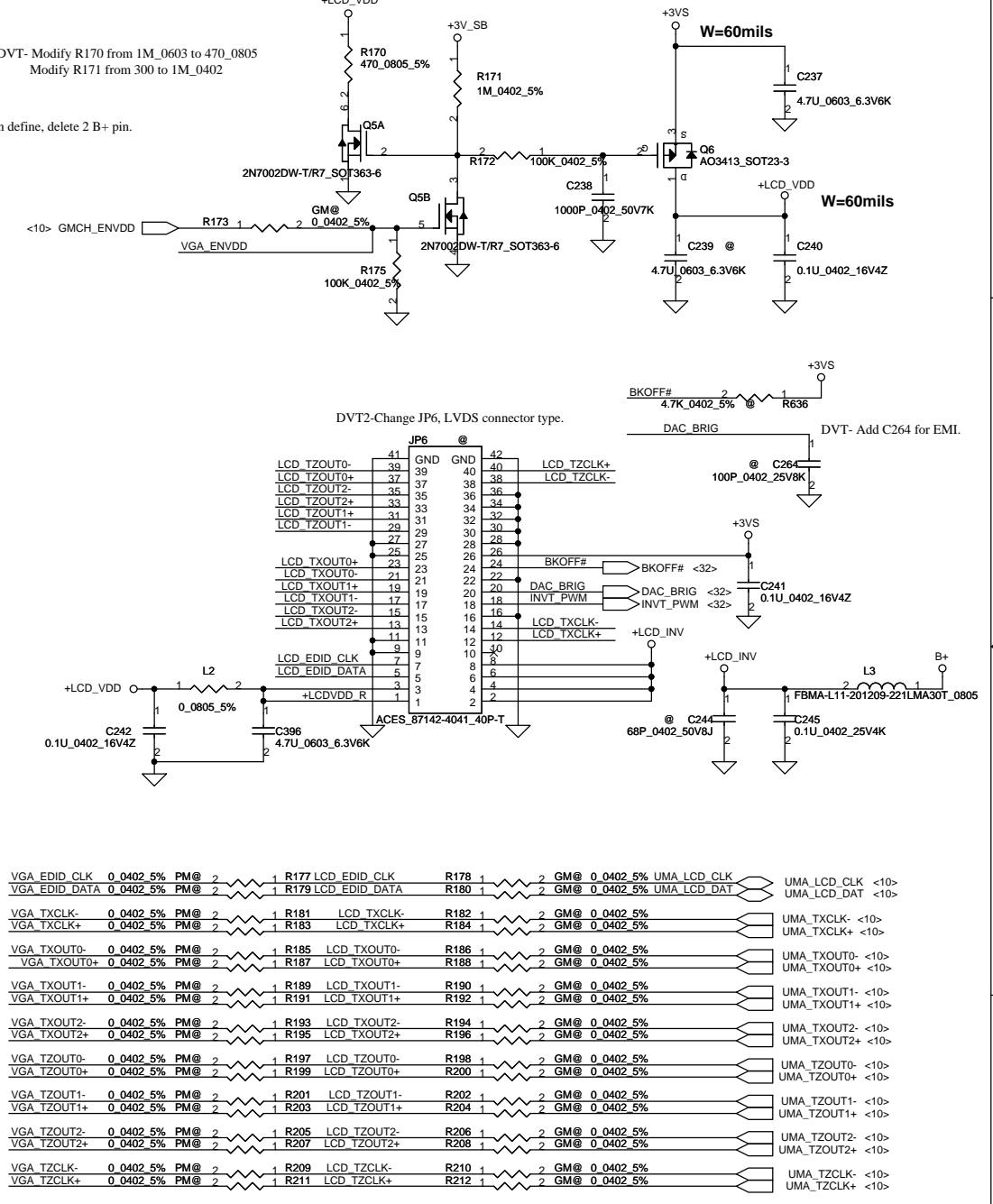
PVT-modify R719/R724 signal from CLK_SIO to CLK_ICH.

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VGA BOARD Conn.

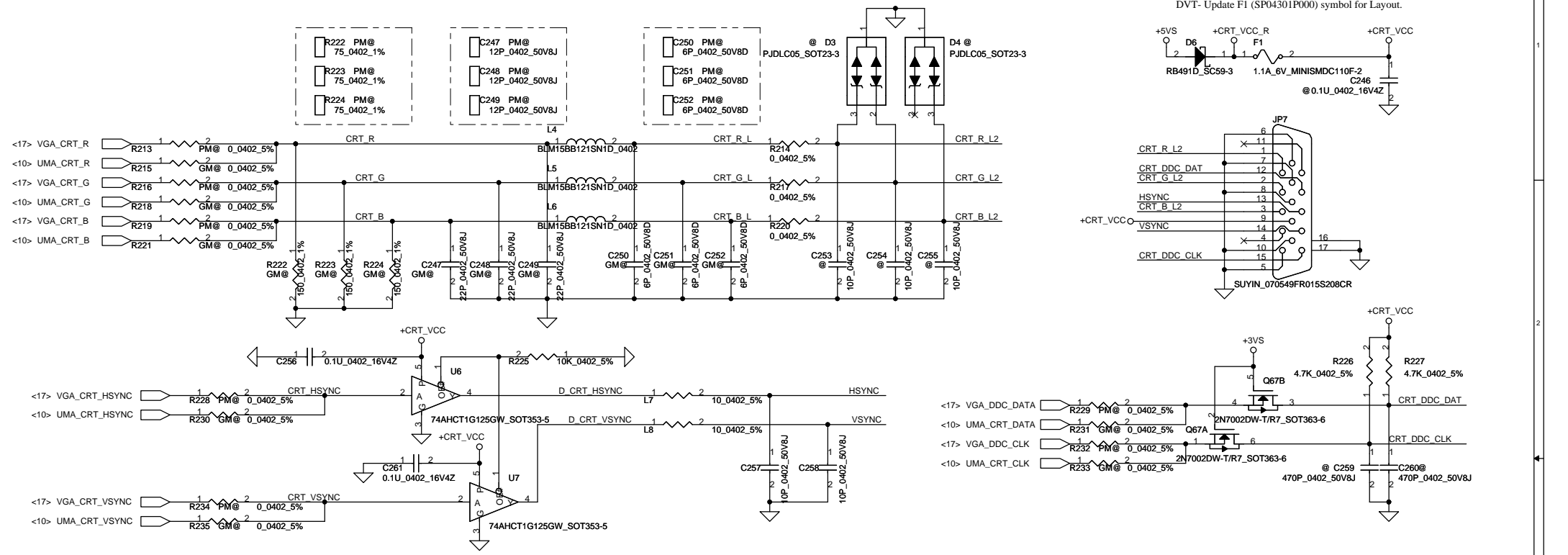


LCD/PANEL BD. Conn.

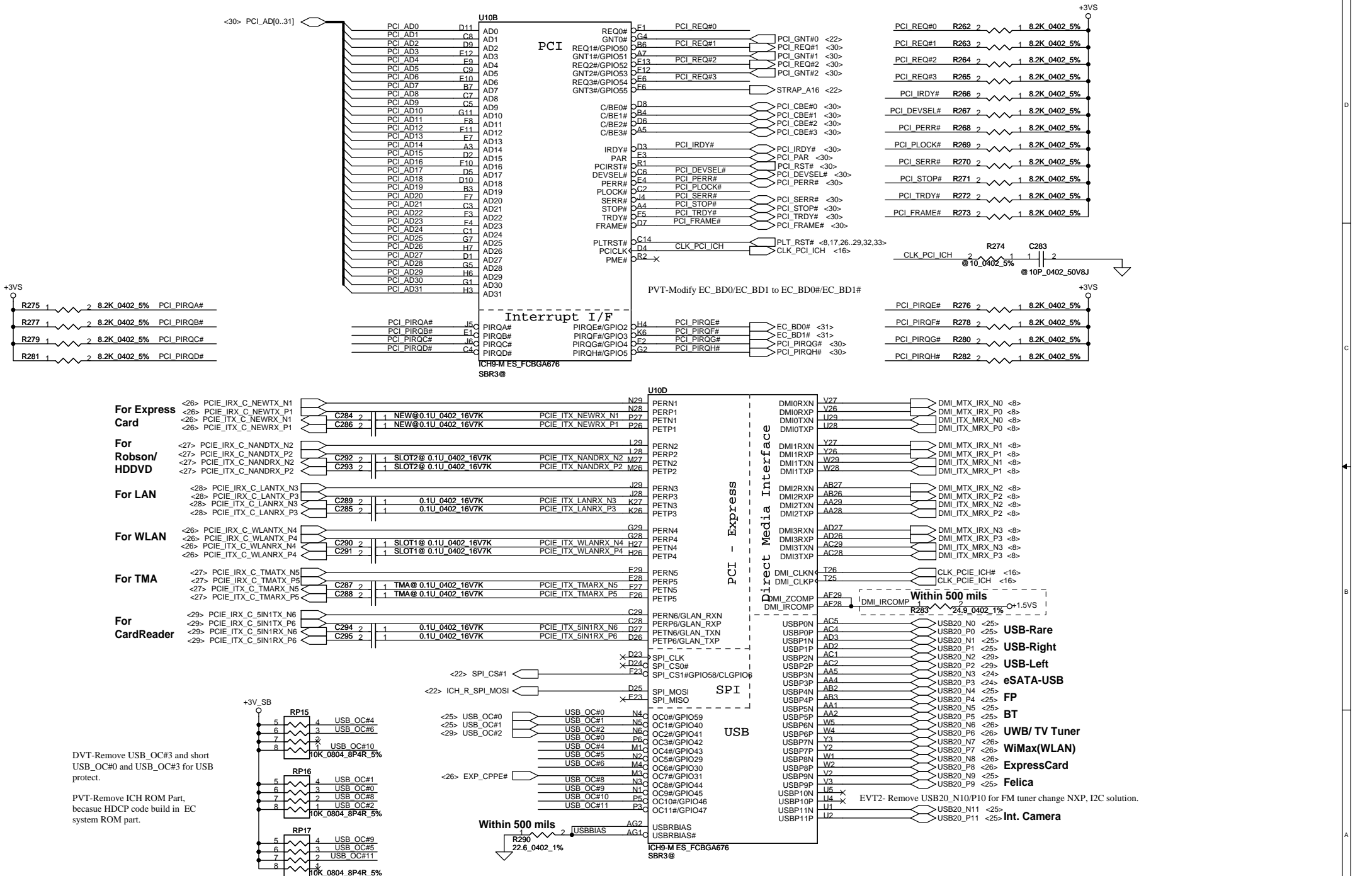


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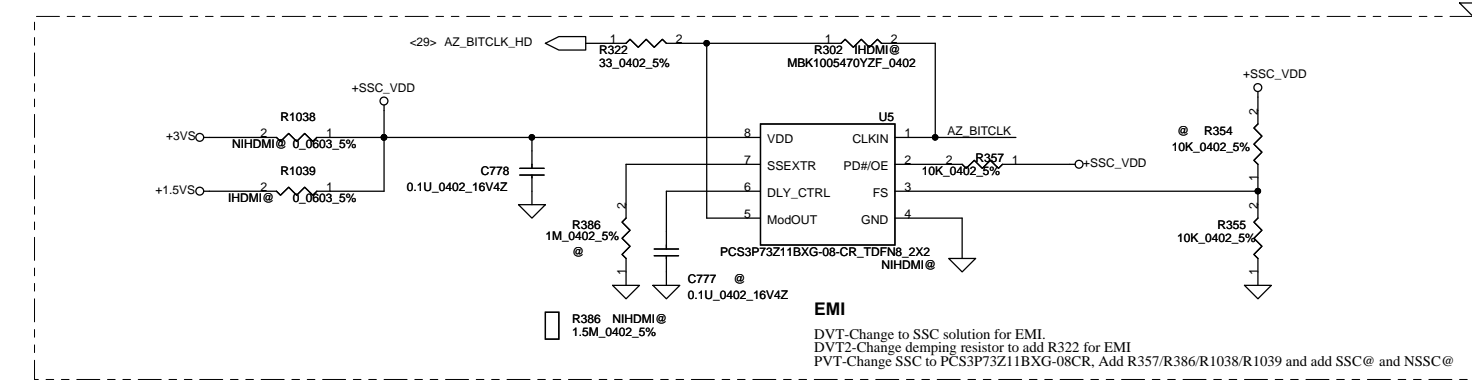
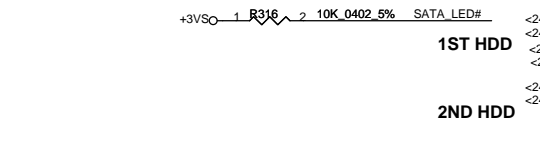
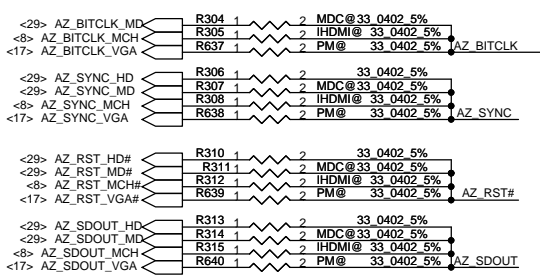
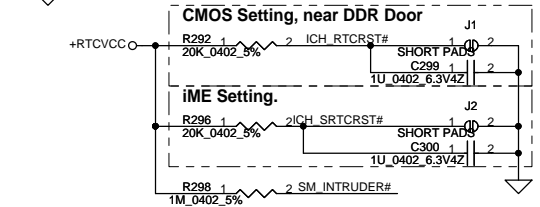
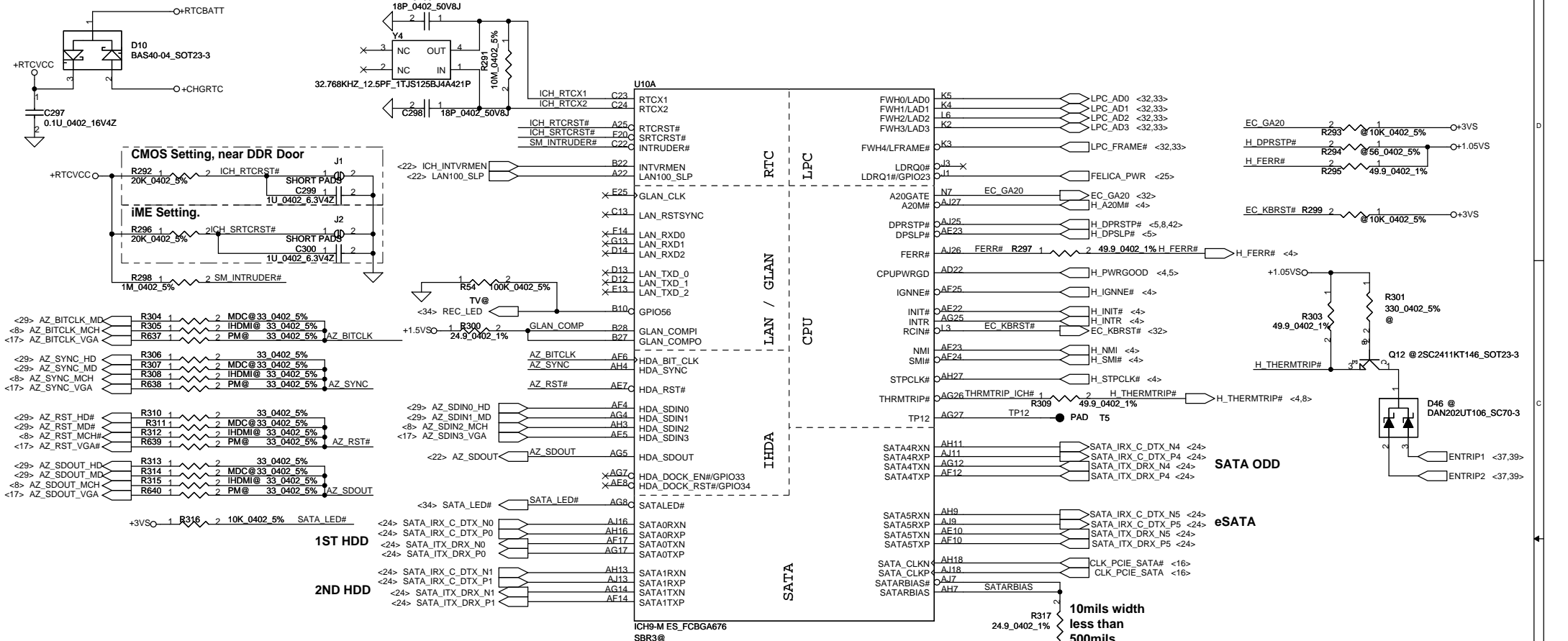
CRT CONNECTOR



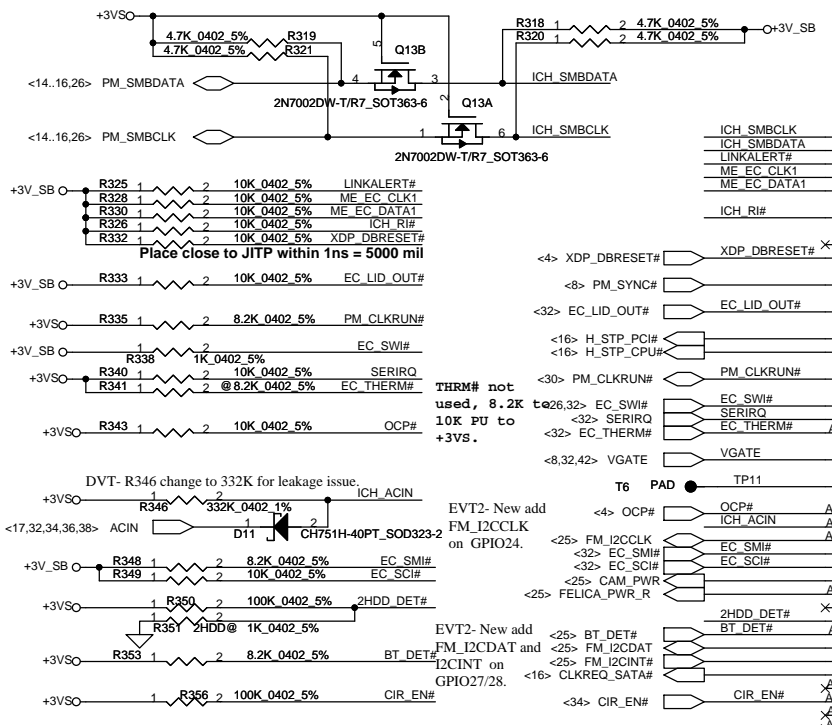
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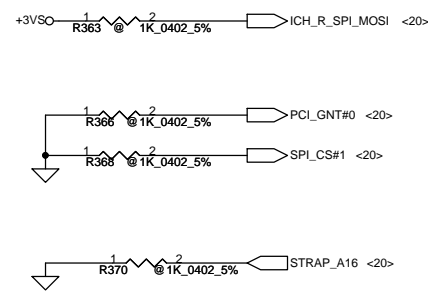


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DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)
iTPM Physical Presence	
CLGPIO5	Assert = iTPM Physical Presence Enable
Mobil Platform	De-assert = iTPM disable
GPIO57	**Only used in iAMT w/ME Firmware
	Desktop Platform used only

ICH9M Strap Pin

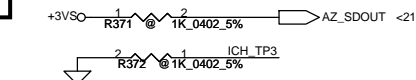
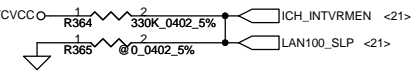


Internal TPM Strap	
SPI_MOSI	Low= Disable* High= iTPM enable by MCH strap

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

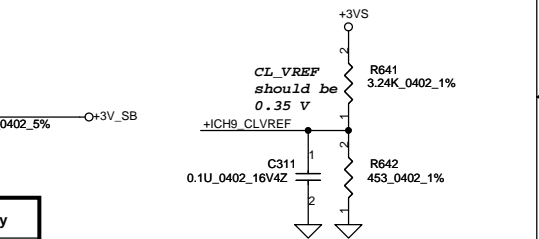
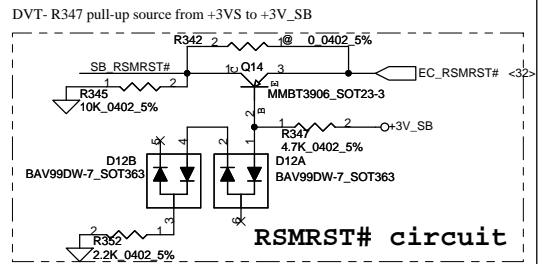
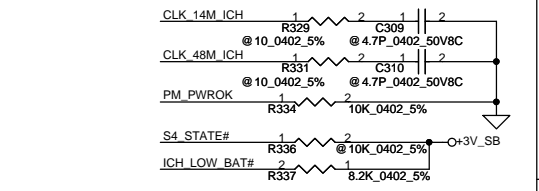
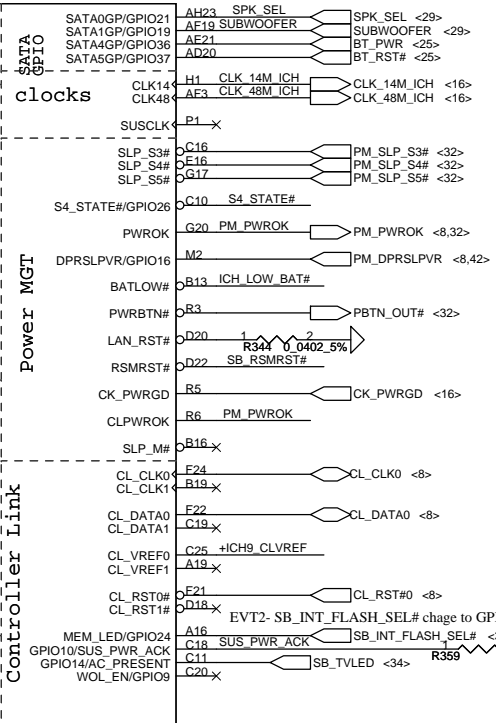


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EVT2- Remove R322/R323/R324/R327 and set these four signal as GPIOs.
DVT- Change BT_PWR and BT_RST# from EC to SB.

Default: De-POP PU/PD Resistors, BIOS set GPIO



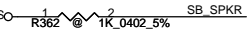
SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

Internal VR Enable Strap	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

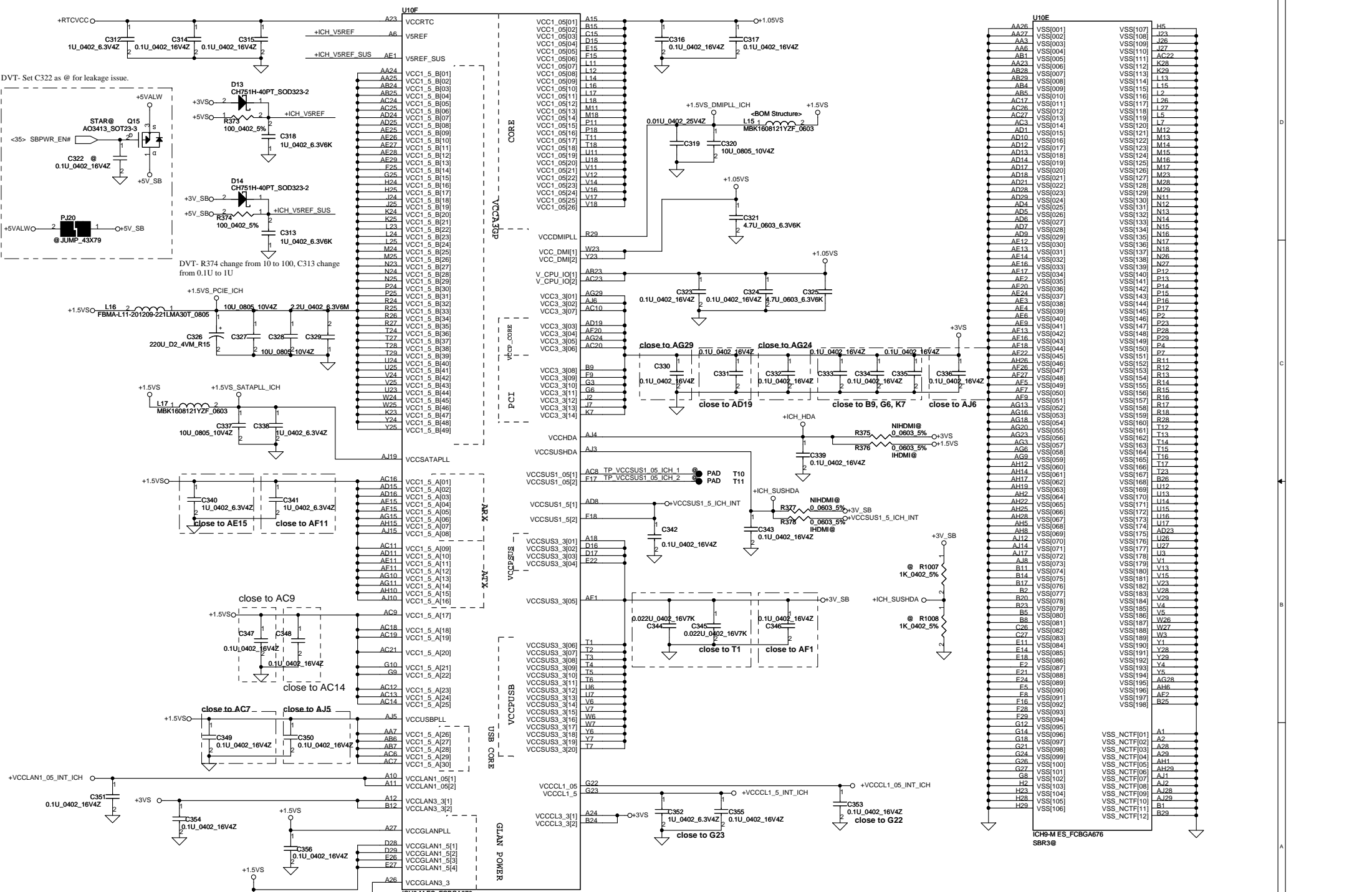
No Reboot Strap	
SB_SPKR	Low= Default* High= "No Reboot"

ICH9M LAN100 SLP Strap	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



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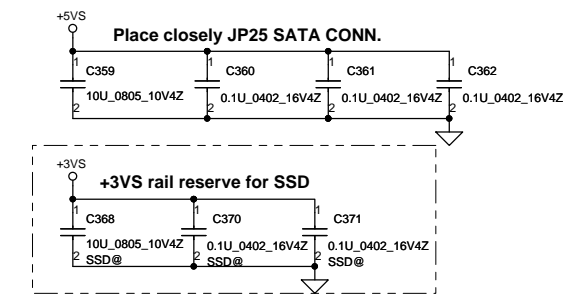
Compal Electronics, Inc.

Schematics, M/B A4161

401562

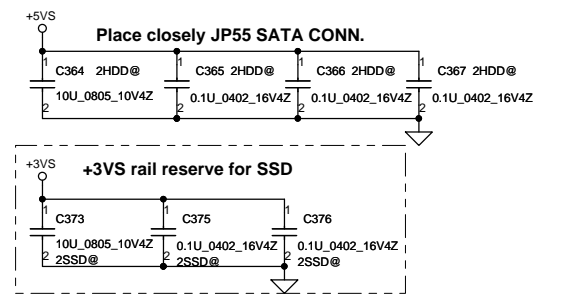
Monday, February 23, 2009

1st SATA HDD Conn.

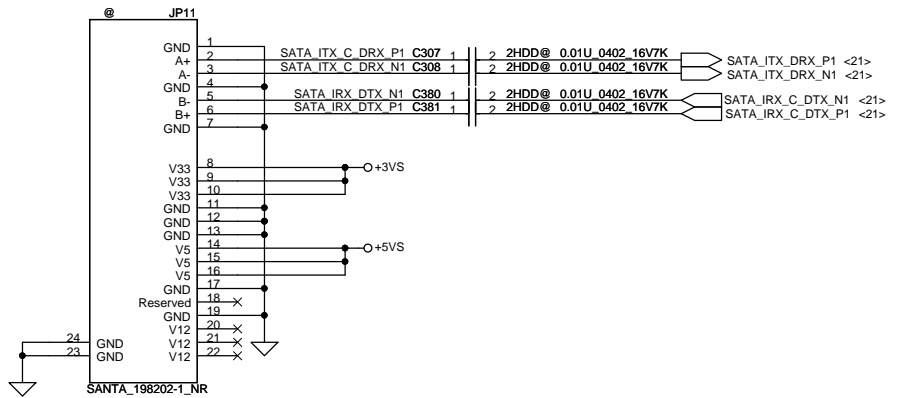
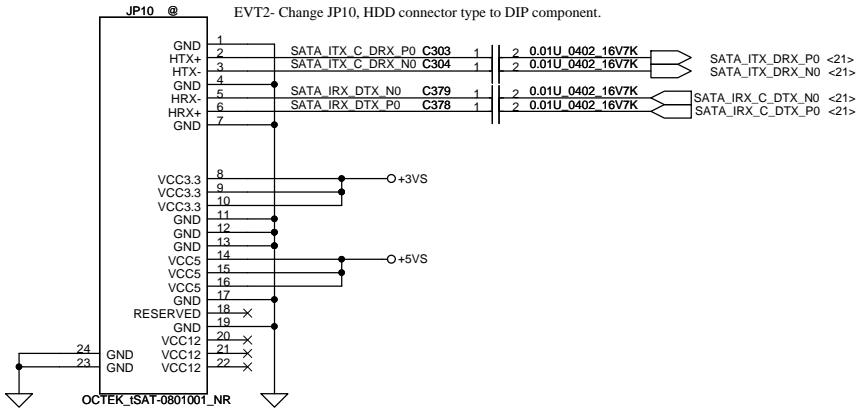


EVT2- For HDD change issue, remove C374/C369/C377/C372
Delete C358/C363

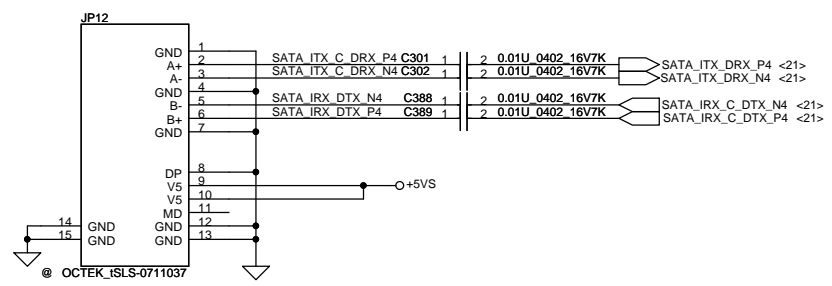
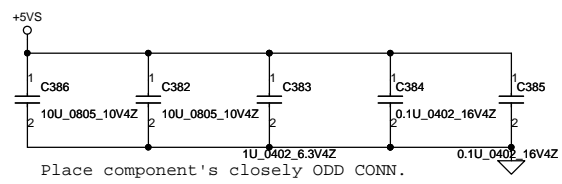
2nd SATA HDD Conn.



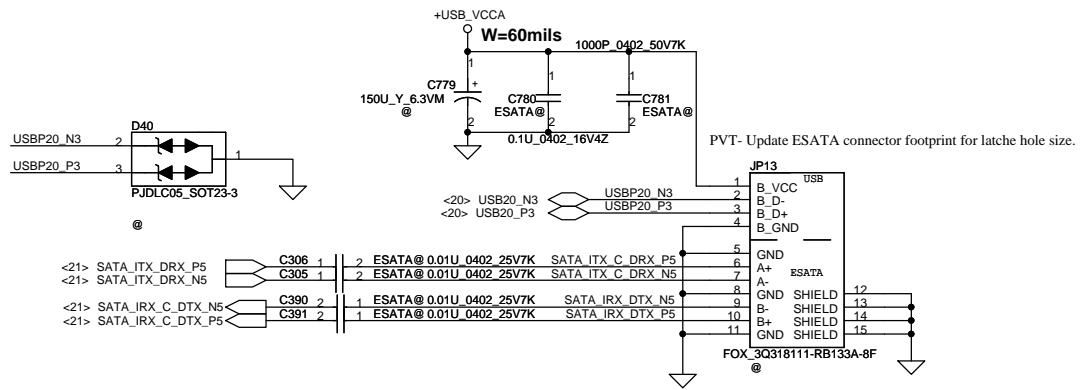
EVT2- Change JP11, HDD connector type for screw issue.



SATA ODD Conn

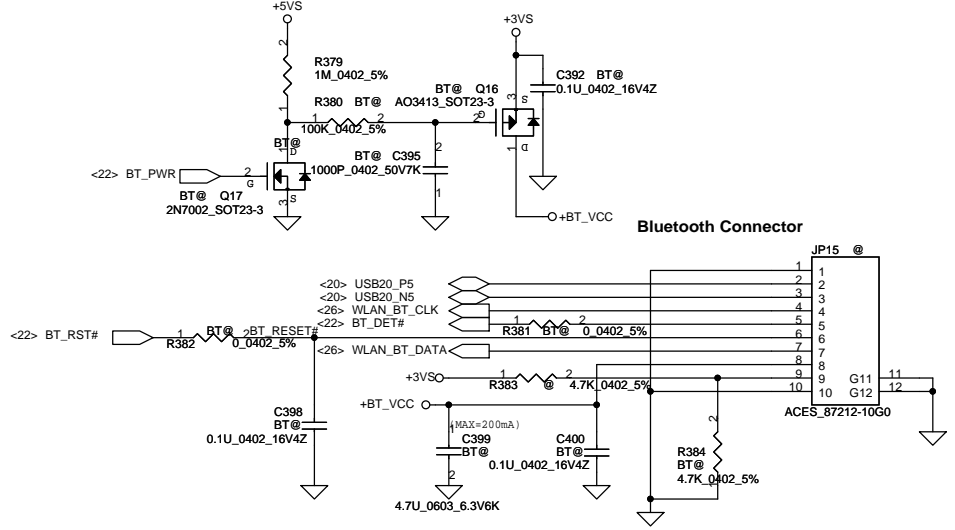


eSATA w/ USB port

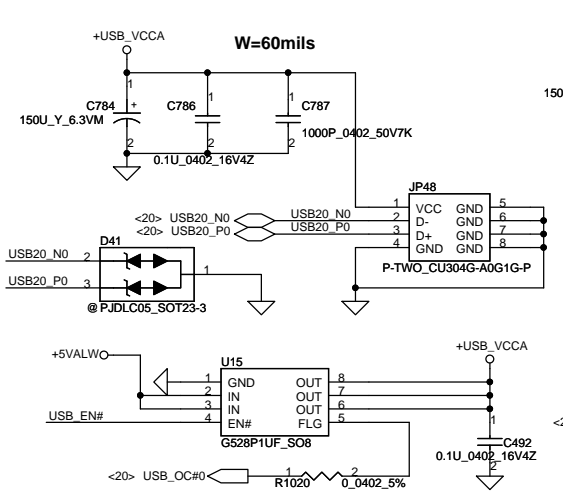


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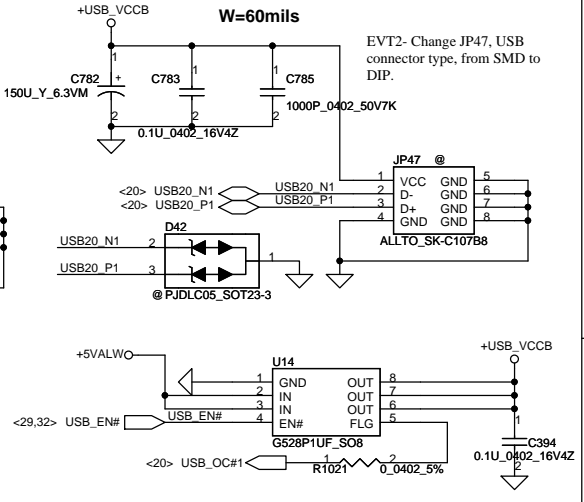
Bluetooth Interface



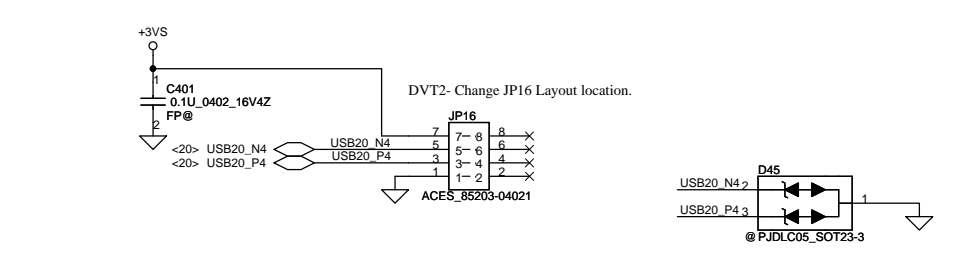
USB CONN. 1 -- Rear



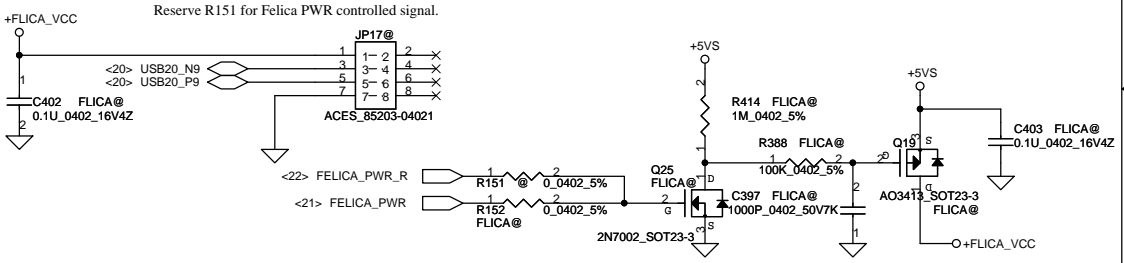
USB CONN.2 -- Right



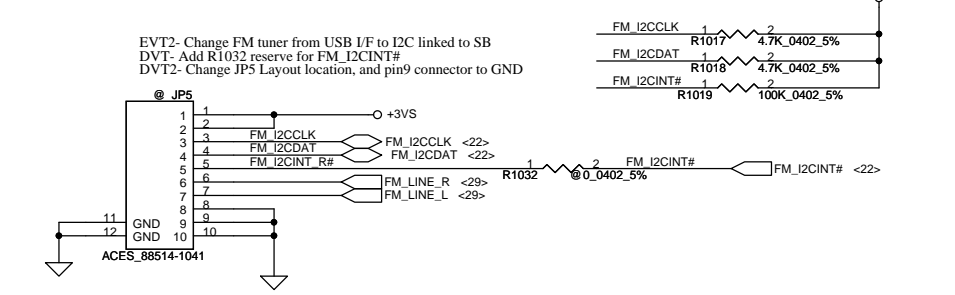
Finger printer



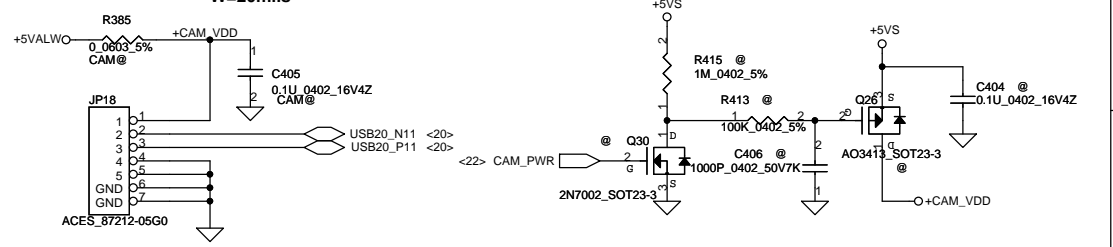
Felica



FM Module

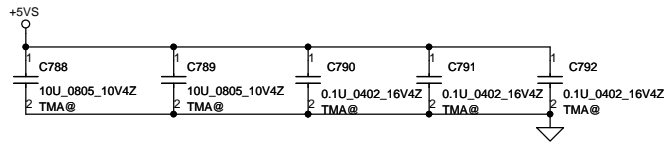
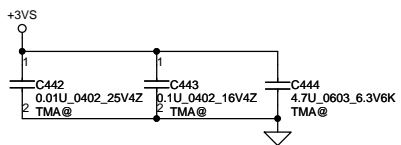


Int. Camera

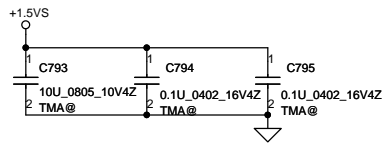
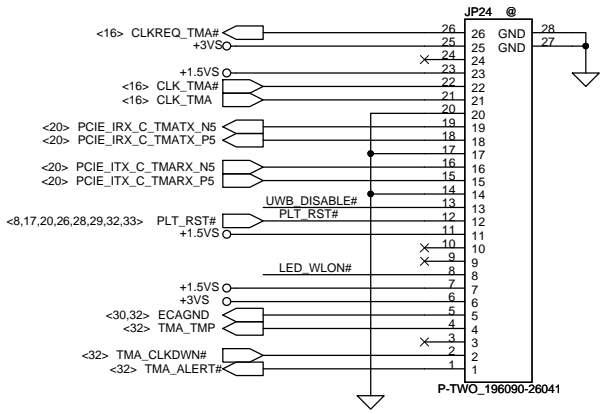


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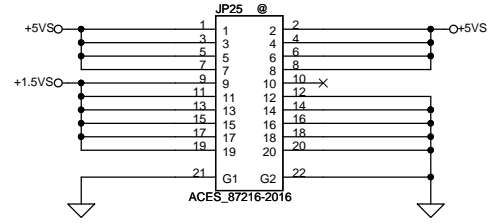
PCIe Mini Card for TMA



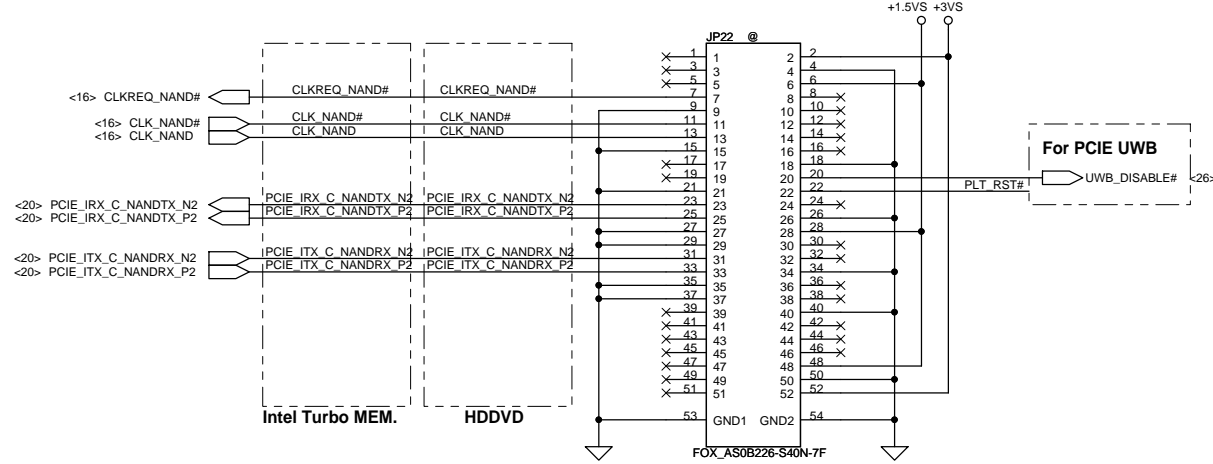
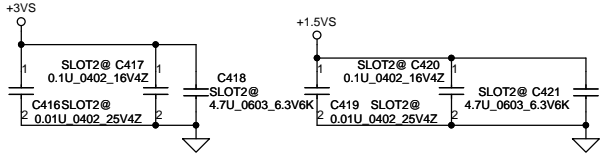
EVT2- Change JP24, TMA connector from 34pin to 24pin type.
 DVT- Change JP24, TMA connector from 24pin to 26pin type. To add TMA_TMP and ECAGND.
 PVT- Change JP24 pin24 as NC because near power pin to prevent assembly issue.



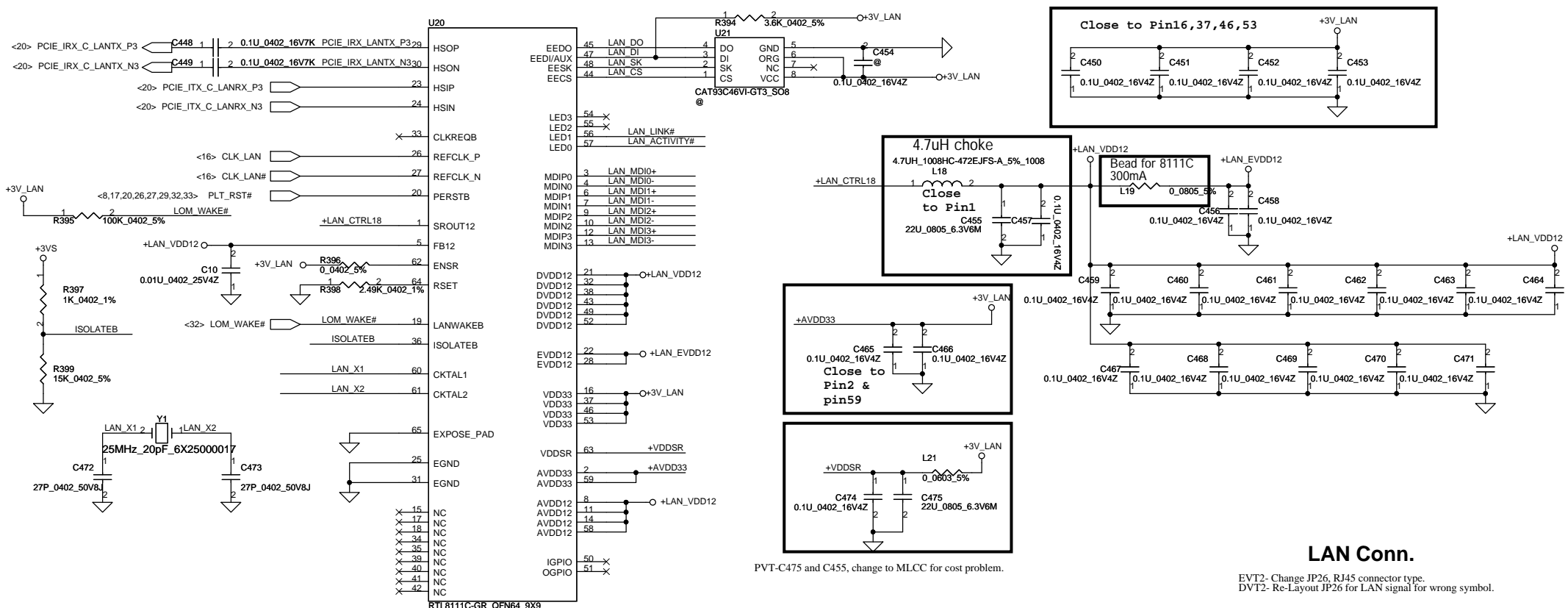
EVT2- Change JP25, TMA power connector type, from right-angle to Horizontal.



Slot 2 - PCIe Mini Card for Robson/ HDDVD



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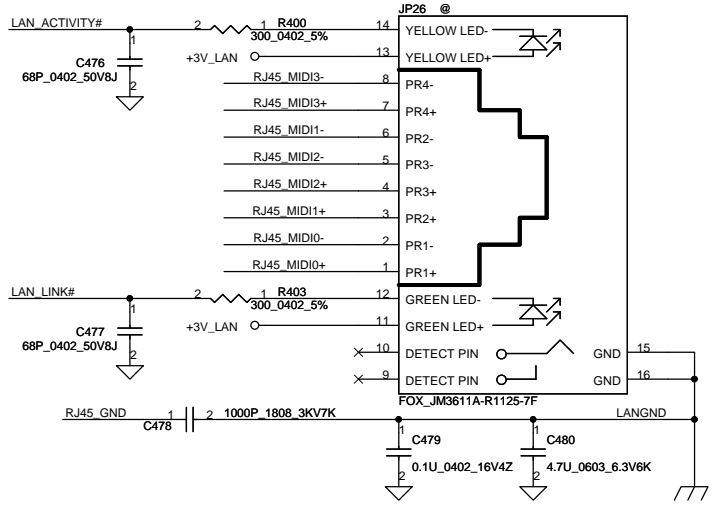
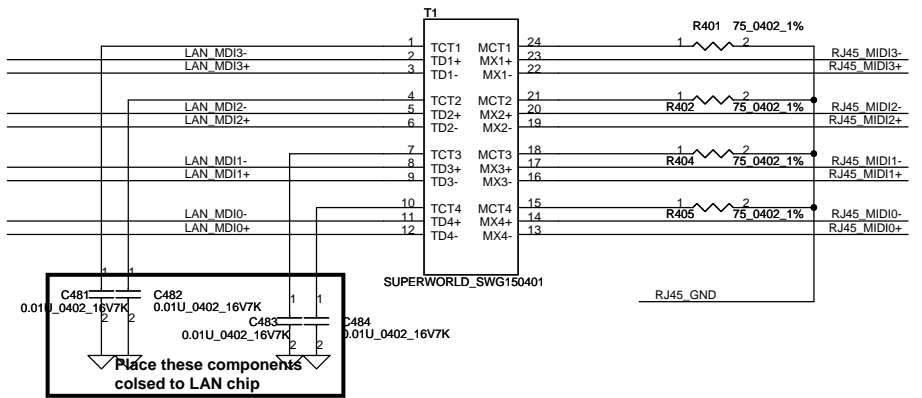


PVT-C475 and C455, change to MLCC for cost problem.

LAN Conn.

EVT2- Change JP26, RJ45 connector type.
DVT2- Re-Layout JP26 for LAN signal for wrong symbol.

DVT-Change transformer vendor from Bothand to Superworld

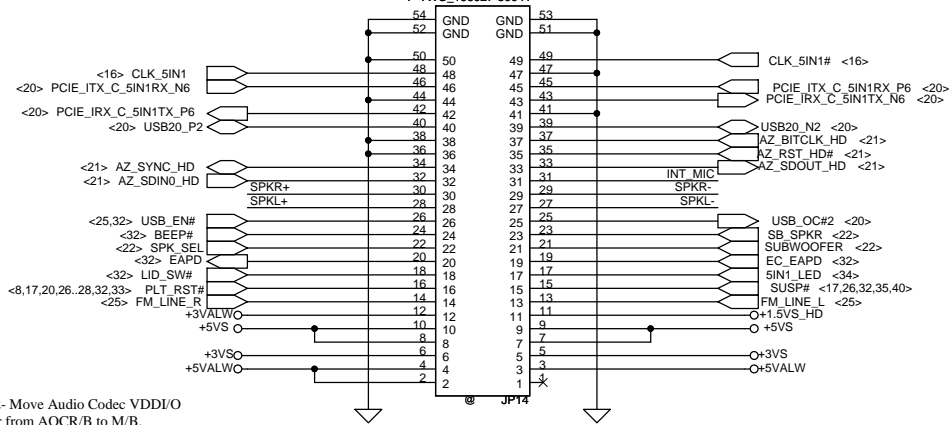


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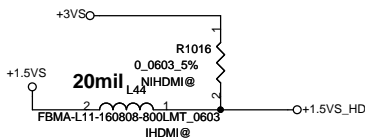
AOCR/B LS-4164P

DVT2-ME shift left 1mm.
PVT-Remove Pin1 GND for shortage issue.

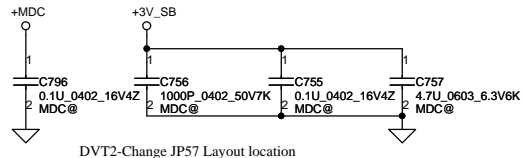
P-TWO_196027-50041



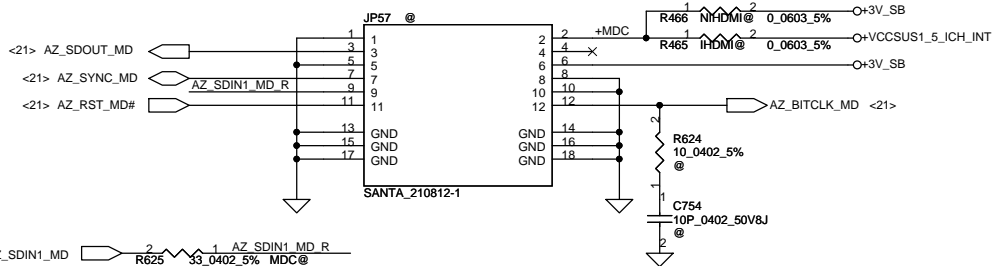
EVT2- Move Audio Codec VDDI/O power from AOCR/B to M/B.



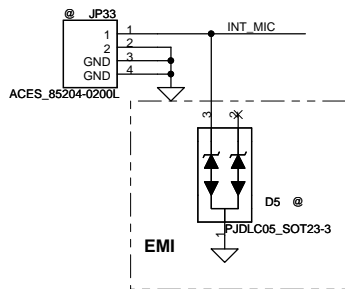
MDC 1.5 Conn.



DVT2-Change JP57 Layout location

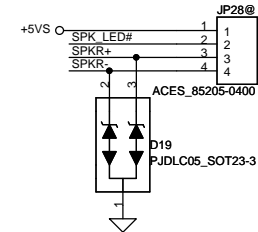
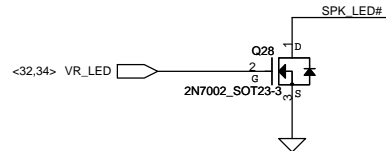


DVT2-Change JP33 Layout footprint.



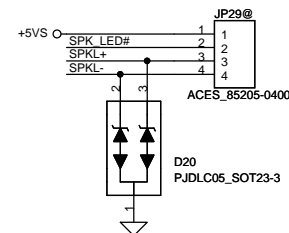
Right Main Speaker & SPKR-LED/B Connector

EVT2- JP28, JP29 chage footprint to meet ME.
Remove SPK ALC269 circuit.

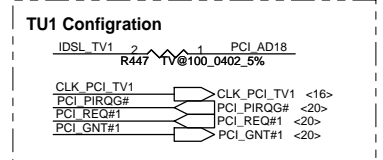
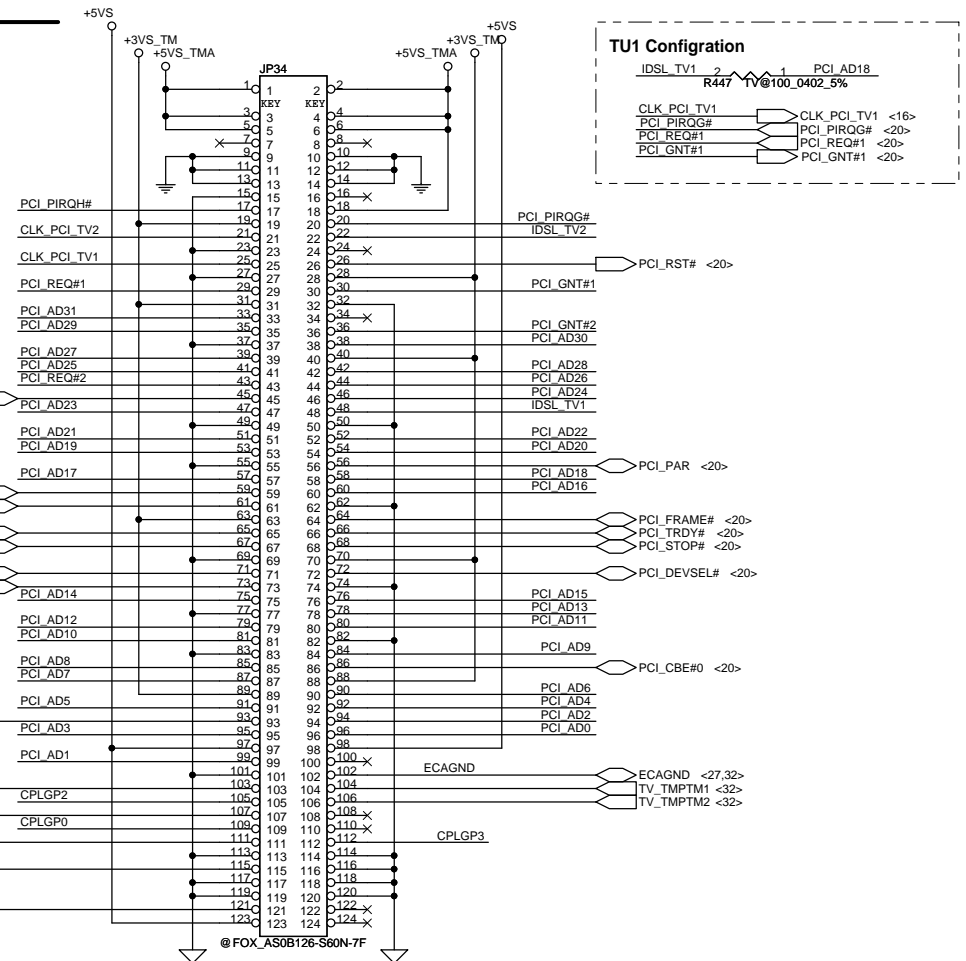
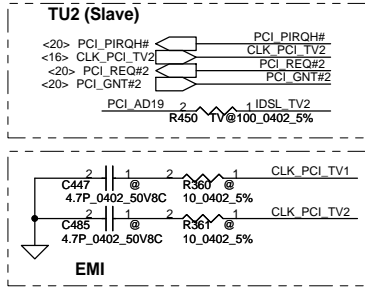
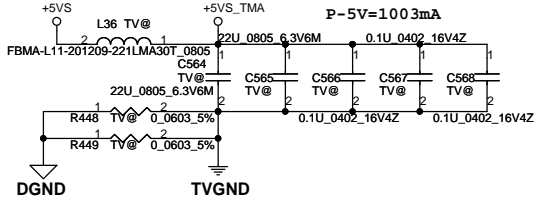
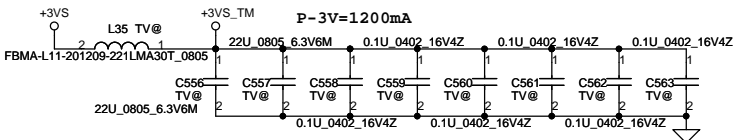


Left Main Speaker & SPKR-LED/B Connector

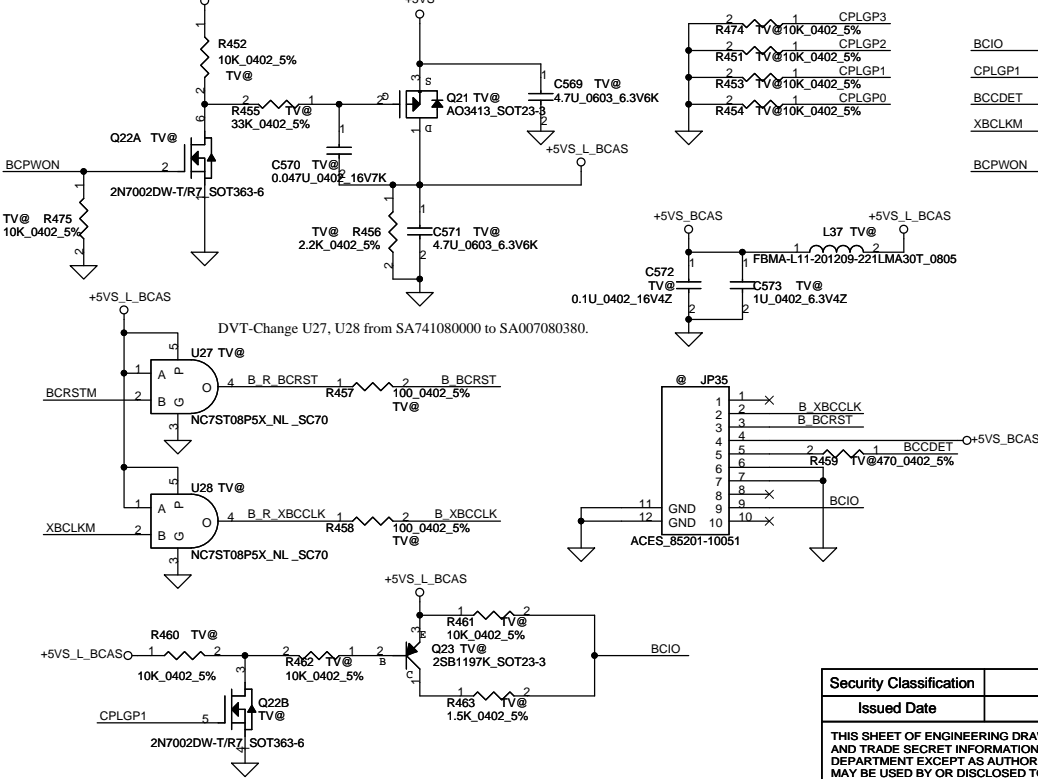
EVT2- JP28, JP29 chage footprint to meet ME.
Remove SPK ALC269 circuit.



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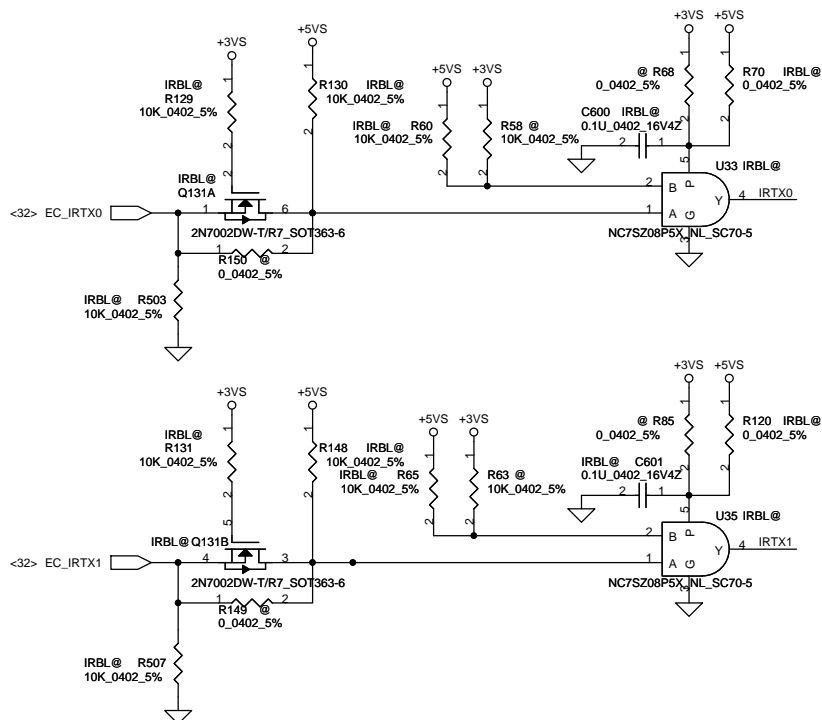
B-CAS Circuit



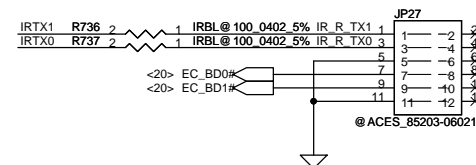
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DVT- Modify IRTX circuit for vottage drop problem.
 Add C601 for U35, for Layout placement update for DFB

EVT2- LEARNIR change to LEARNIR#
 PVT-Delete SMC IR Bluster solution
 Delete R738,R739, R748,R749



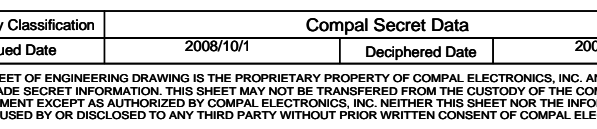
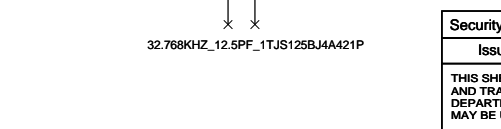
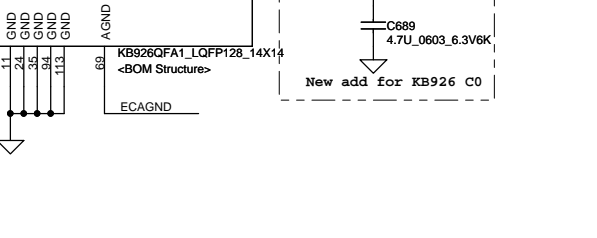
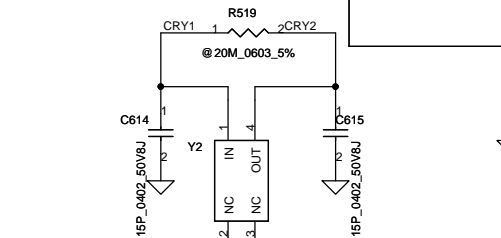
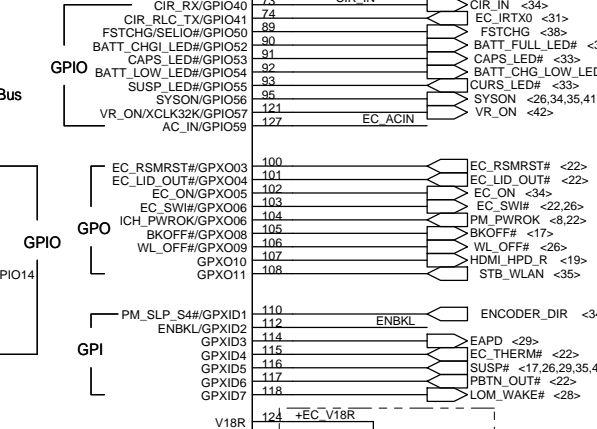
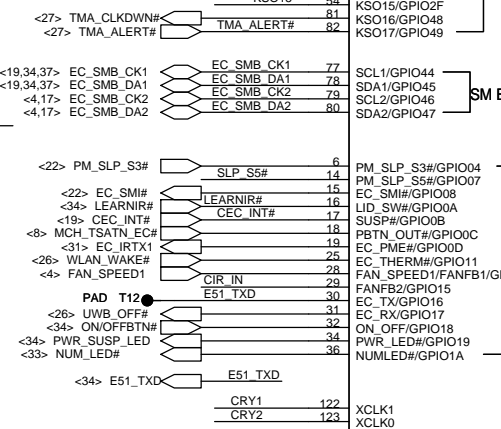
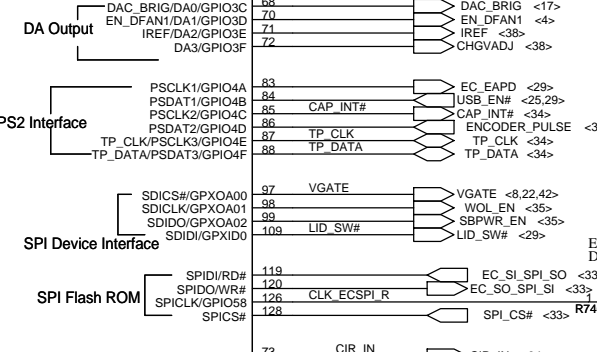
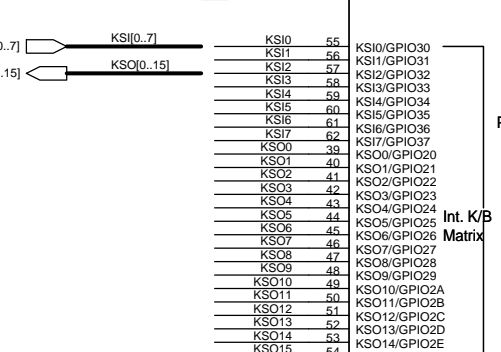
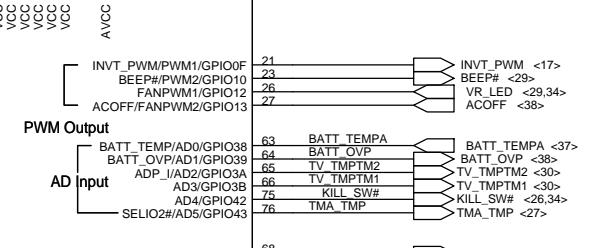
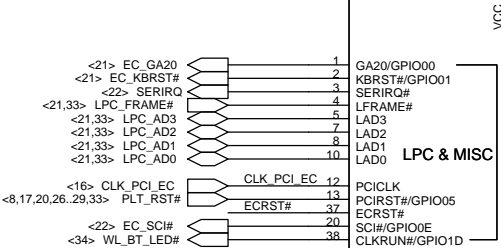
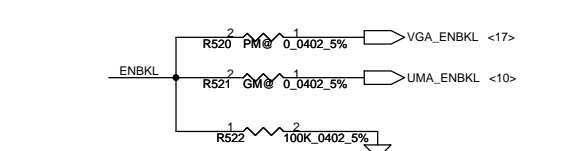
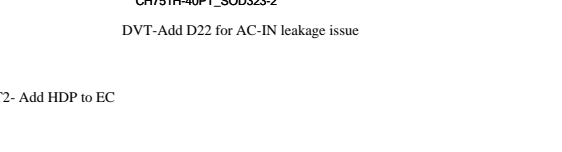
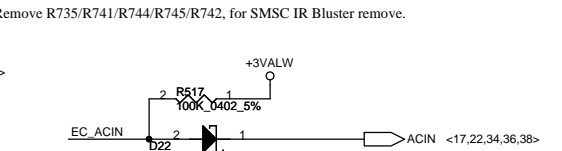
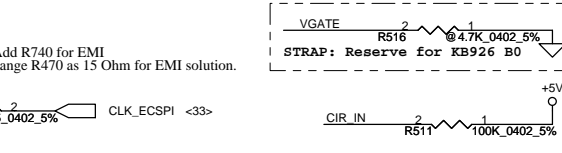
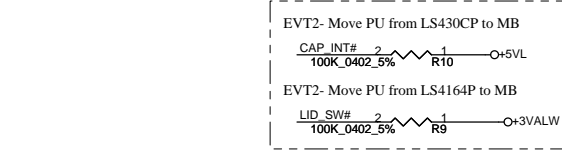
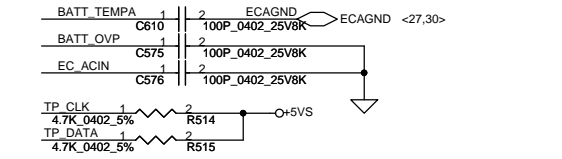
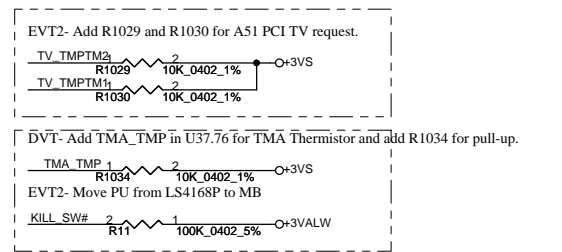
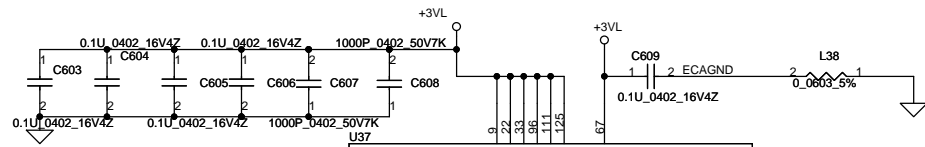
DVT- Delete R508 and R510, duplicate with R276 and R278.
 R736 and R737, change from 100 to 33.



PVT-Modify EC_BD0/EC_BD1 to EC_BD0#/EC_BD1#
 Modify BD0/BD1 to BD0#/BD1#

DVT2- Reserve Q3/Q8/Q136/R1013/R1037 for IR Blaster test

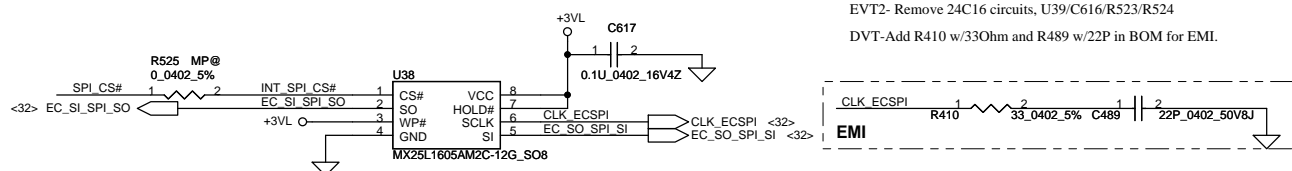
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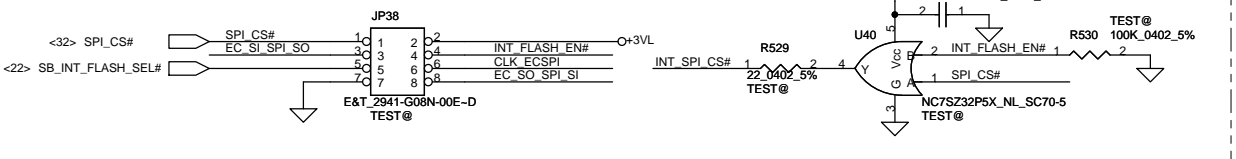
32.768KHZ_12.5PF_1TUS125BJAA421P

SPI Flash (16Mb*1)



EVT2- Remove 24C16 circuits, U39/C616/R523/R524
 DVT-Add R410 w/330Ohm and R489 w/22P in BOM for EMI.

External Flash ROM



SB_INT_FLASH_SEL	H	L	L	SB_INT_FLASH_SEL	H	L	L
SPI#	L	L	H	INT_FLASH_EN#	L	H	H
EXT_CS#	H	L	H	SPI#	L	L	H
External Flash ROM	STOP	RUN	STOP	INT_SPI_CS#	L	H	H
				External Flash ROM	RUN	STOP	STOP

SI/O Debug

TP CONN.

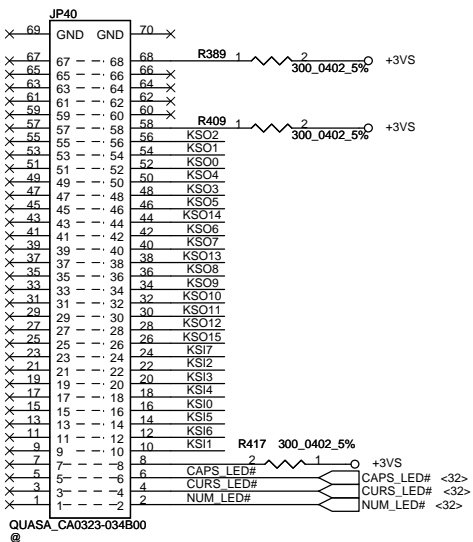
DVT2- Remove JP39, TP/B connector, and C621, because combined in LED/B connector

KEYBOARD CONN.

DVT- Change Keyboard capacitors to mount components for EMI.

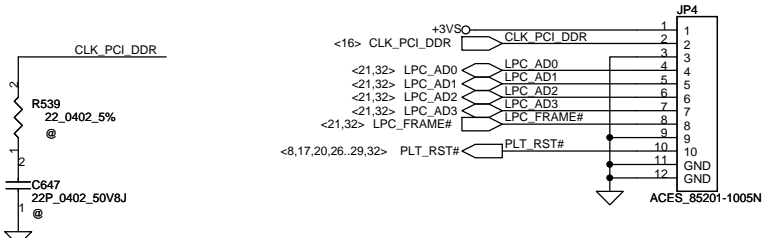


KSO2	C619	100P_0402_25V8K
KSO1	C620	100P_0402_25V8K
KSO0	C622	100P_0402_25V8K
KSO4	C623	100P_0402_25V8K
KSO3	C624	100P_0402_25V8K
KSO5	C625	100P_0402_25V8K
KSO14	C626	100P_0402_25V8K
KSO6	C627	100P_0402_25V8K
KSO7	C628	100P_0402_25V8K
KSO13	C629	100P_0402_25V8K
KSO8	C630	100P_0402_25V8K
KSO9	C631	100P_0402_25V8K
KSO10	C632	100P_0402_25V8K
KSO11	C633	100P_0402_25V8K
KSO12	C634	100P_0402_25V8K
KSO15	C635	100P_0402_25V8K
KSI7	C636	100P_0402_25V8K
KSI2	C637	100P_0402_25V8K
KSI3	C638	100P_0402_25V8K
KSI4	C639	100P_0402_25V8K
KSI0	C640	100P_0402_25V8K
KSI5	C641	100P_0402_25V8K
KSI6	C642	100P_0402_25V8K
KSI1	C643	100P_0402_25V8K
CAPS_LED#	C644	100P_0402_25V8K
CURS_LED#	C645	100P_0402_25V8K
NUM_LED#	C646	100P_0402_25V8K

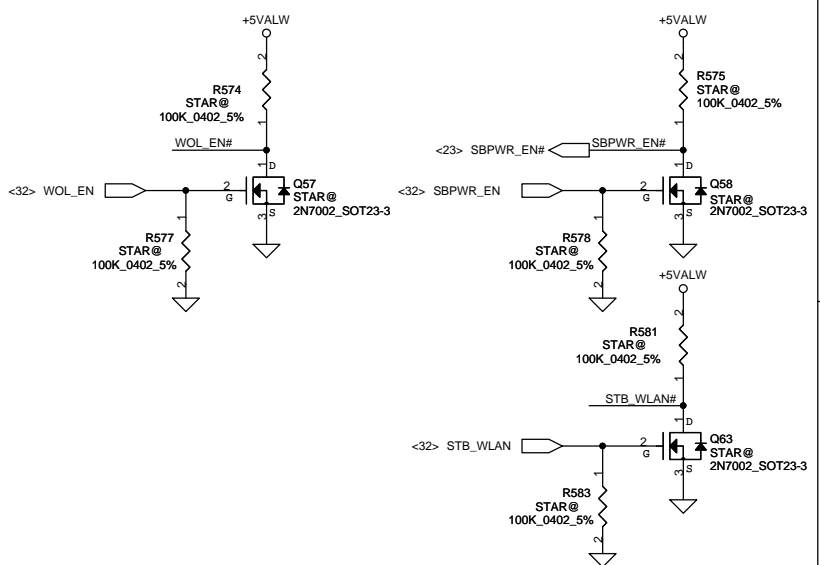
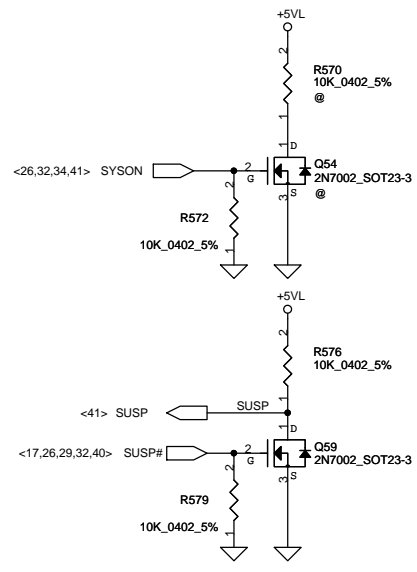
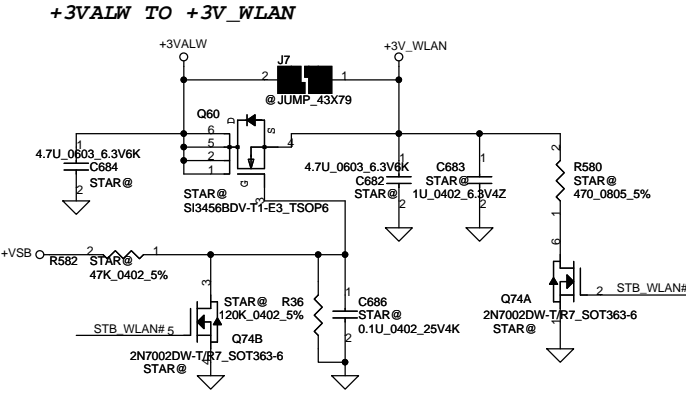
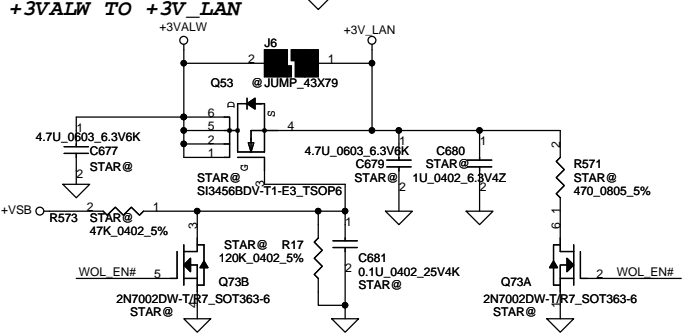
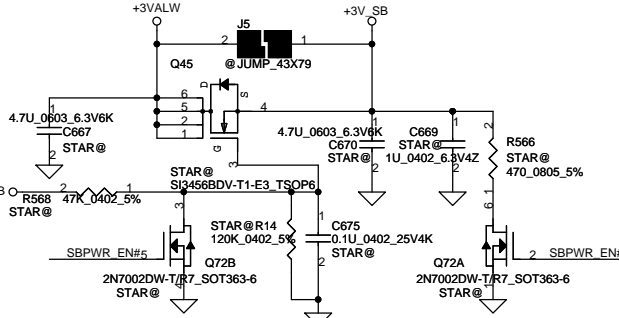
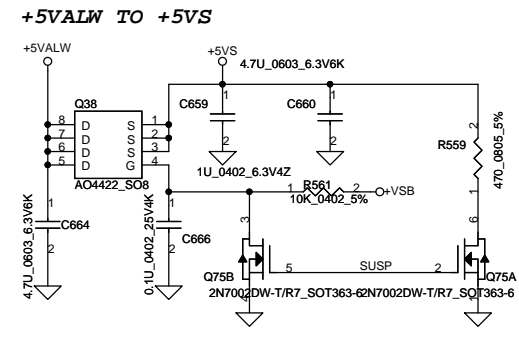
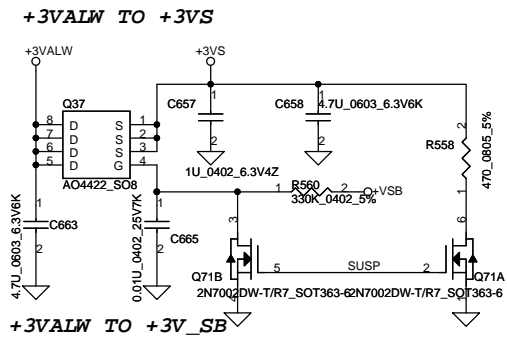
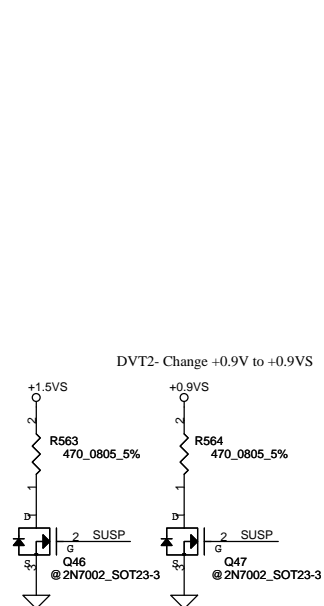


LPC Debug Port

EVT2- Delete EC debug port to reduce space for Layout.
 Change Debug PAD to 10pin connector.

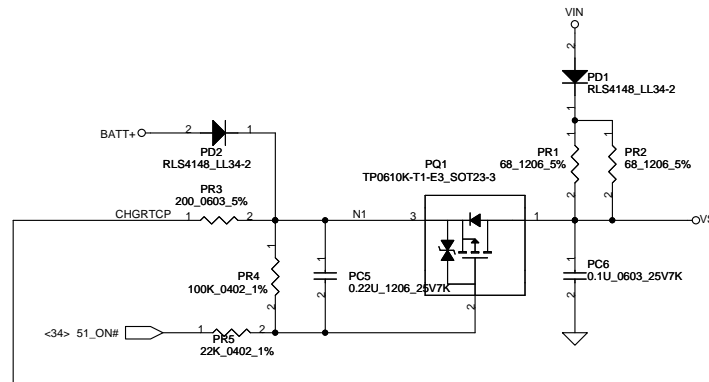
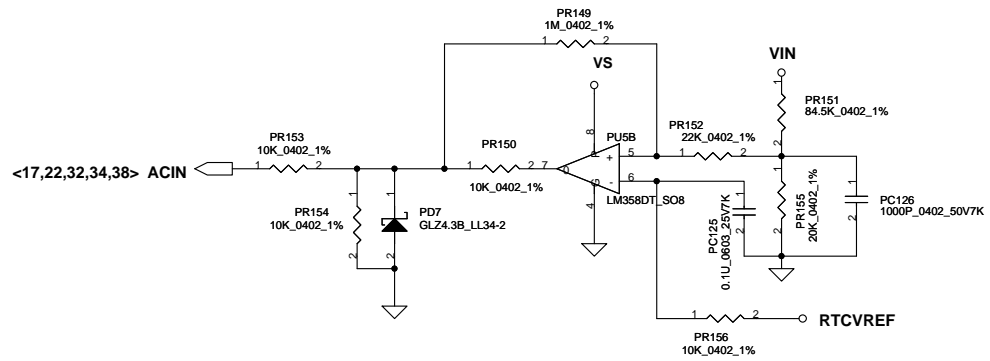
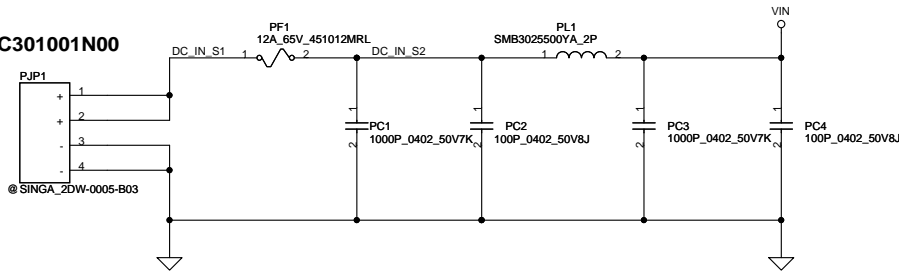


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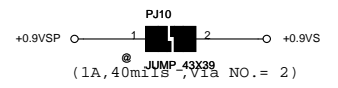
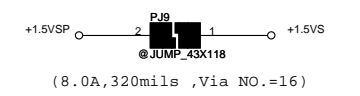
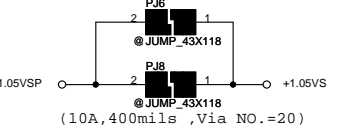
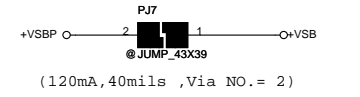
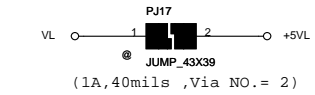
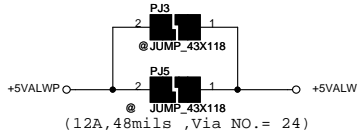
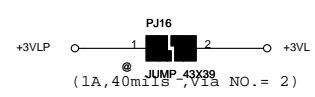
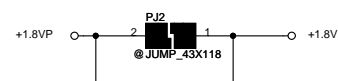
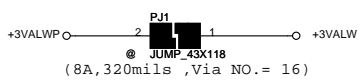
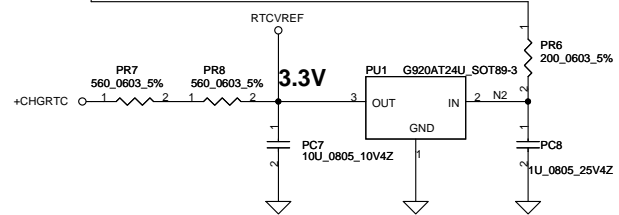
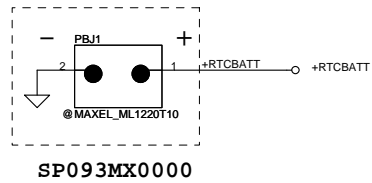


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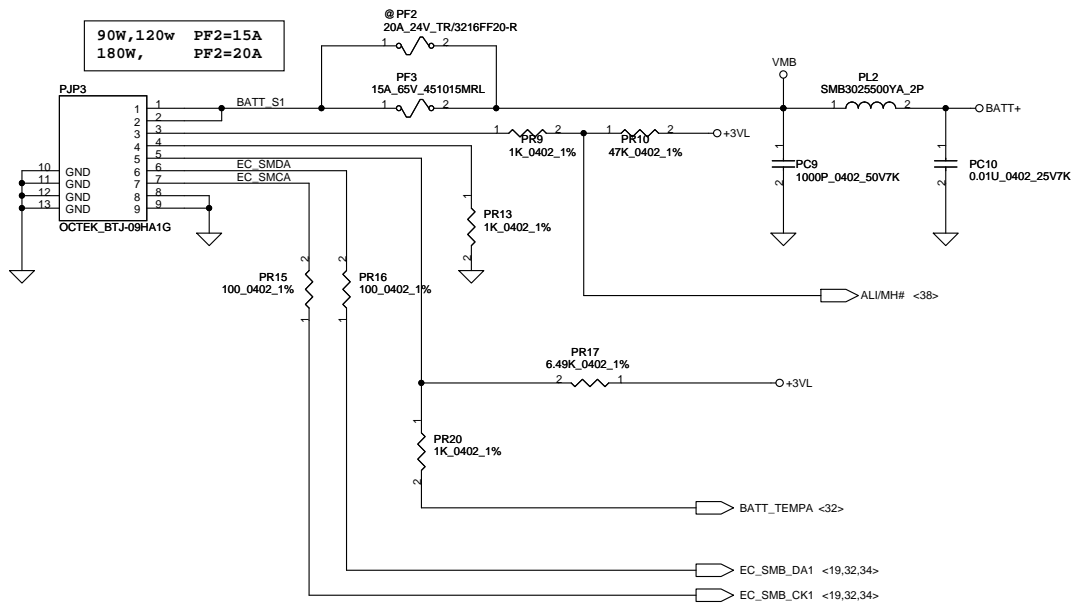
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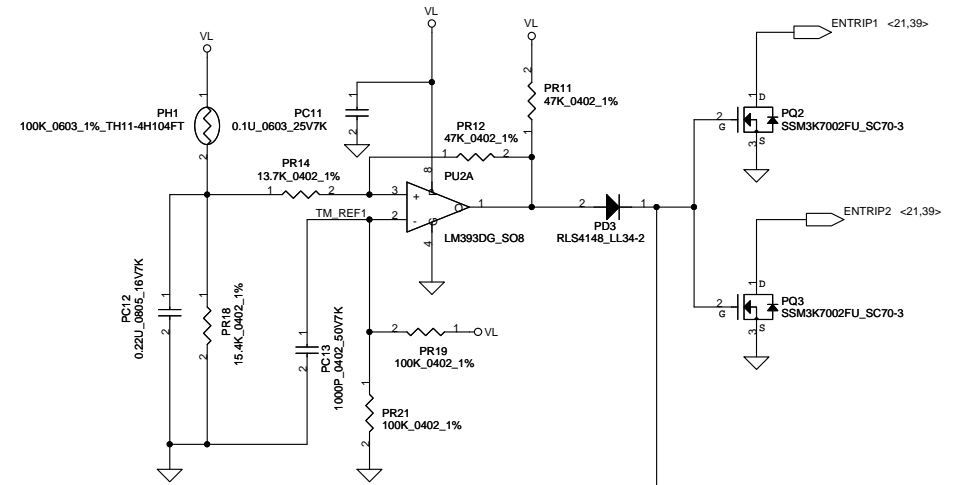
RTC Battery



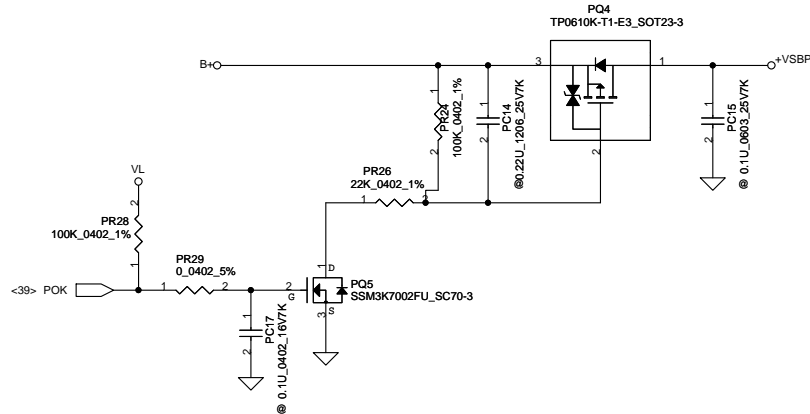
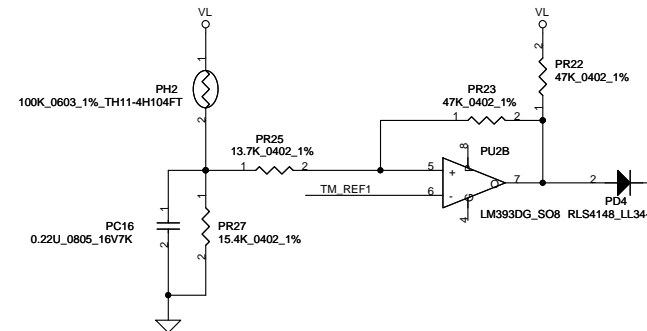
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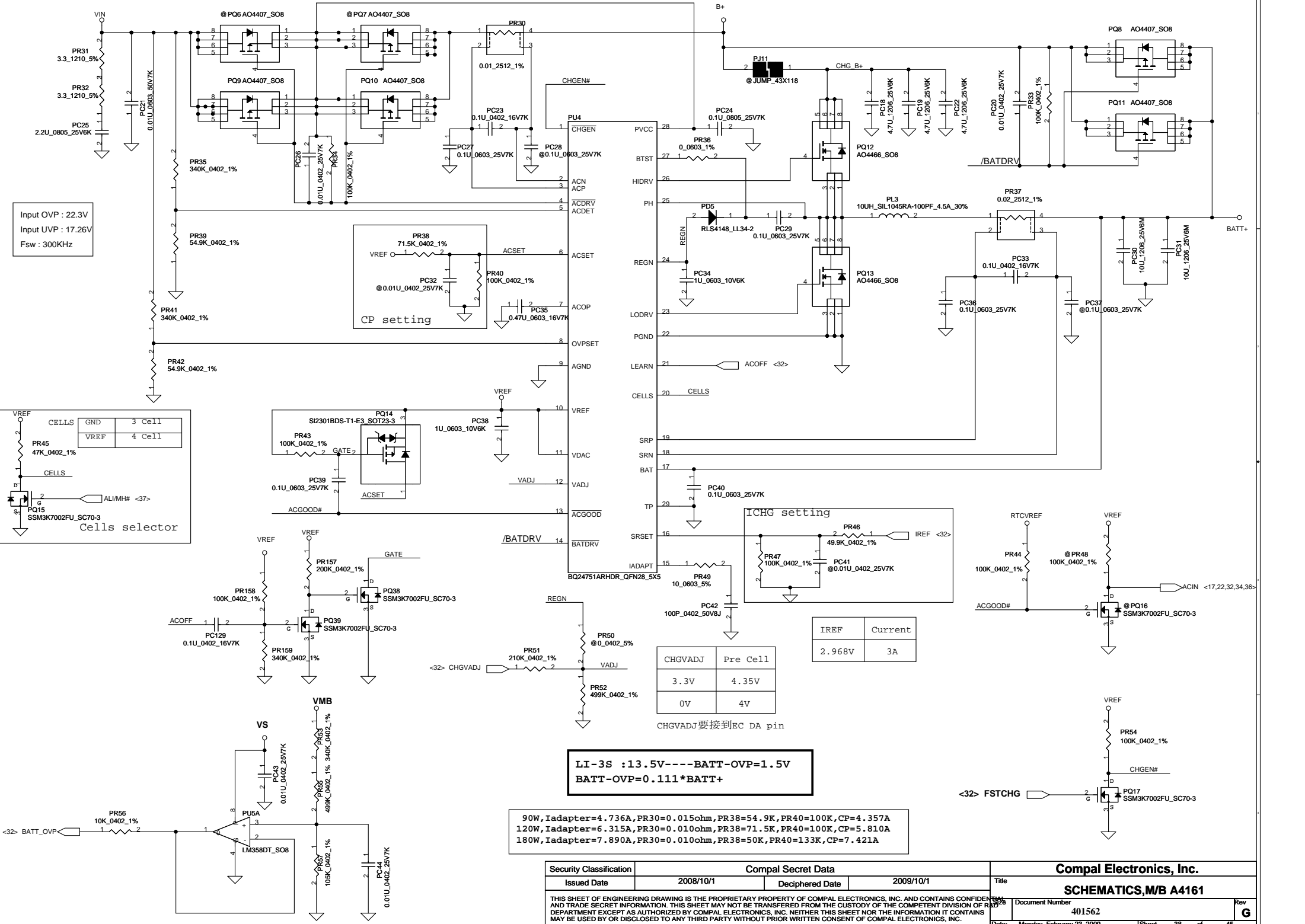
PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



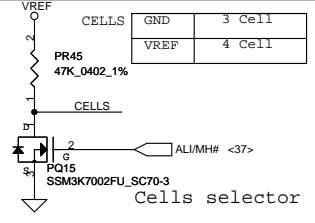
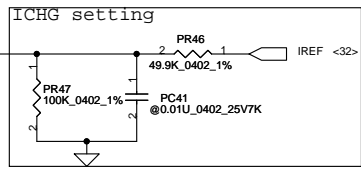
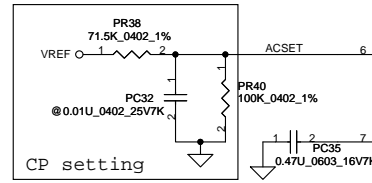
PH2 near main Battery CONN :
 BAT. thermal protection at 92 degree C
 Recovery at 56 degree C



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Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



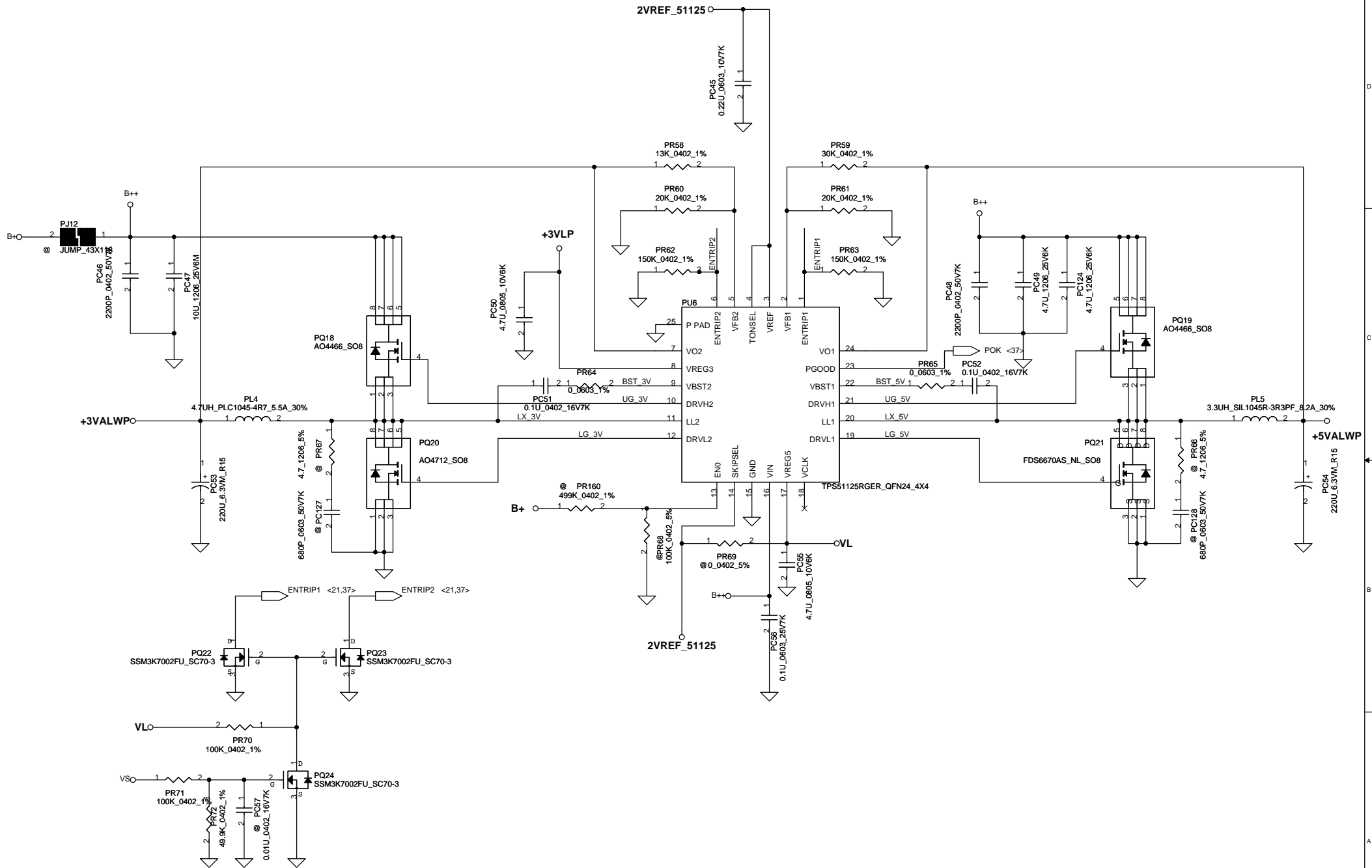
CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

LI-3S : 13.5V --- BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

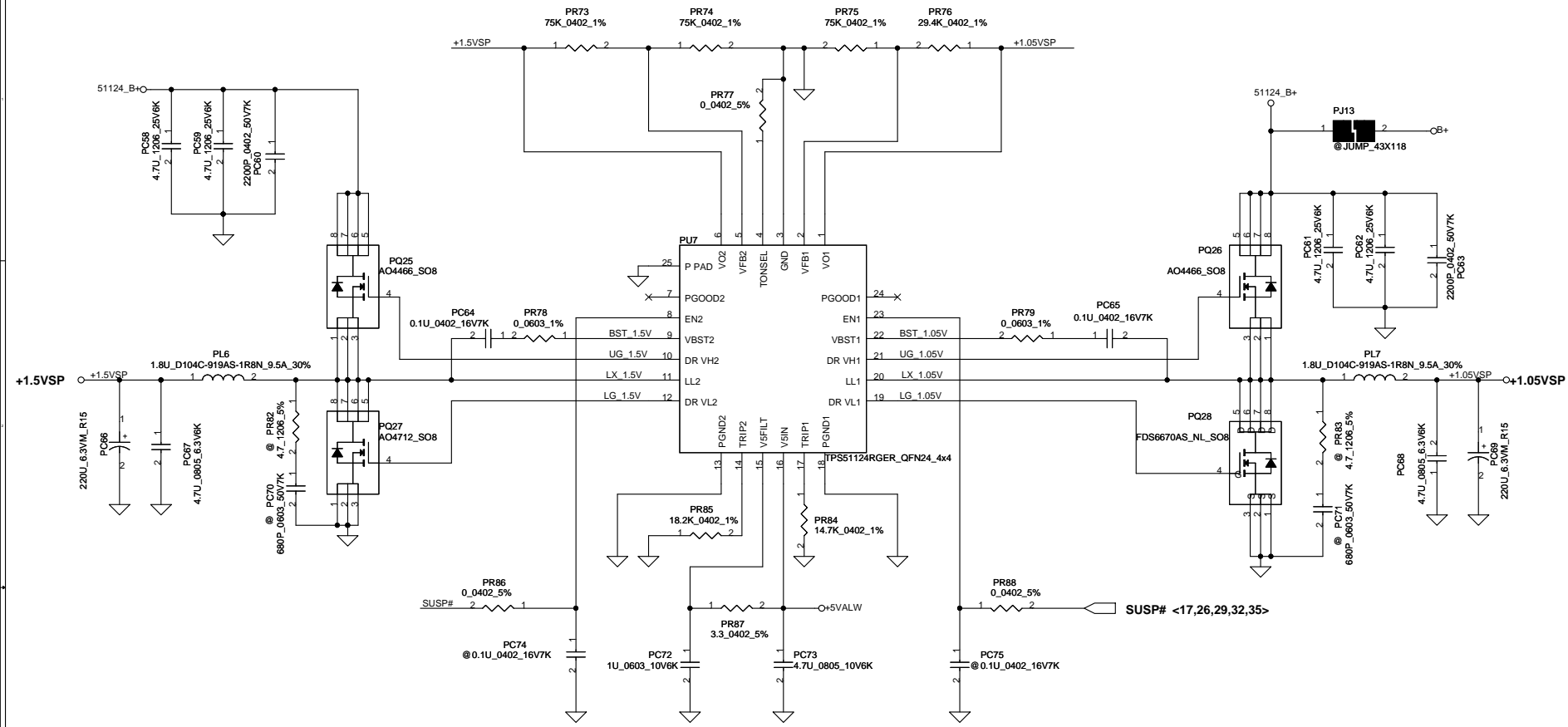
90W, Iadapter=4.736A, PR30=0.015ohm, PR38=54.9K, PR40=100K, CP=4.357A
 120W, Iadapter=6.315A, PR30=0.010ohm, PR38=71.5K, PR40=100K, CP=5.810A
 180W, Iadapter=7.890A, PR30=0.010ohm, PR38=50K, PR40=133K, CP=7.421A

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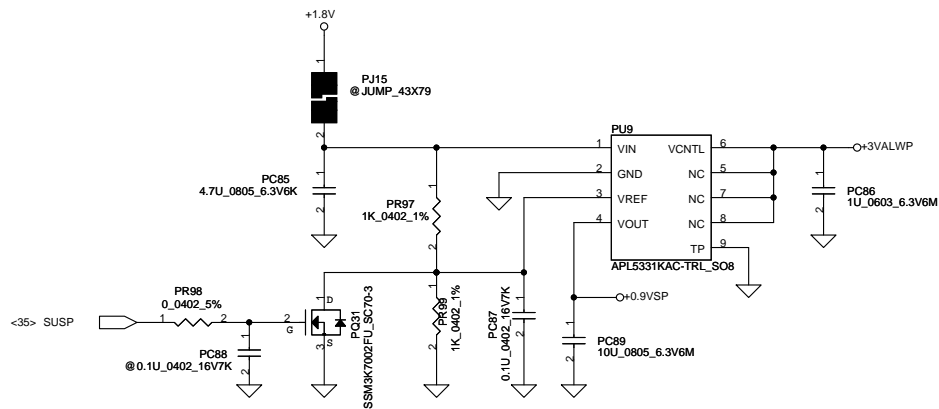
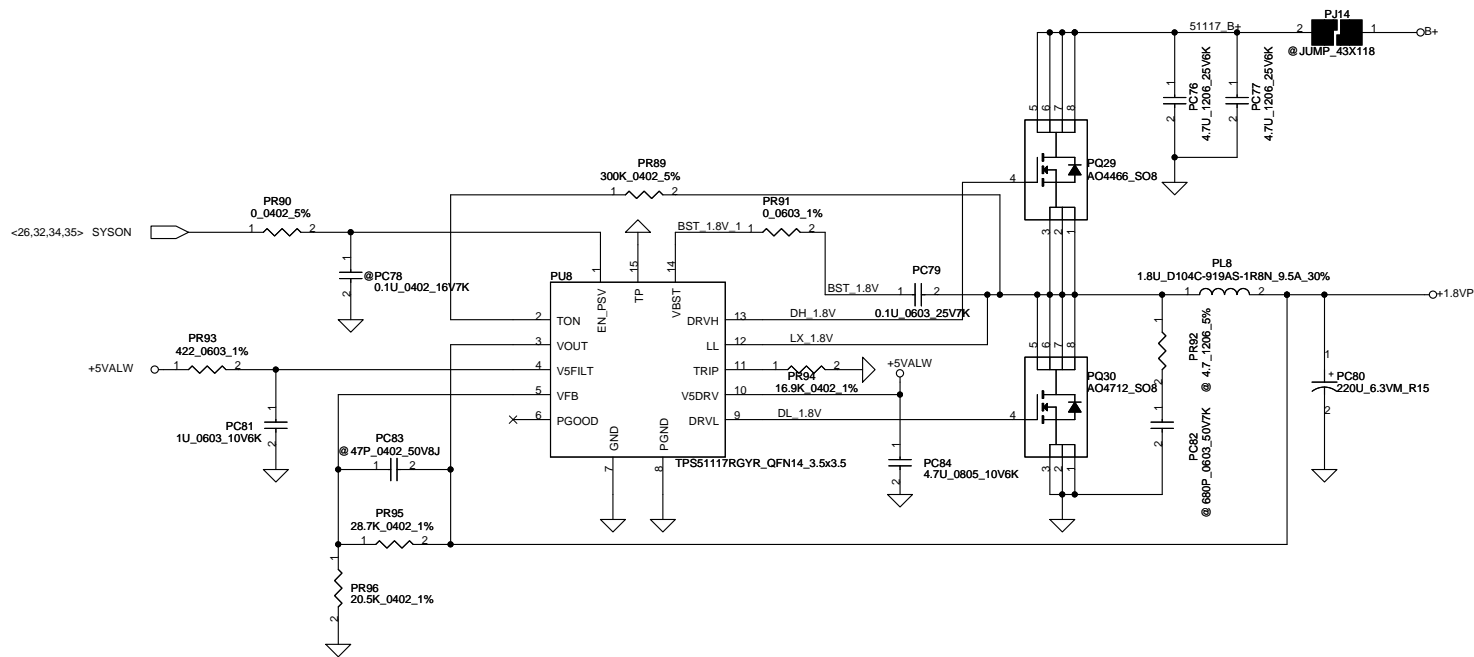
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PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	11/01'07		Release	
2	12/25'07	P.36 P.38 P.39	Add AC-IN schematic move PR44 PR66,PR67,PC127,PC128	Add AC-IN detect function Add AC-IN pull-higher resistor Add 3VALWP and 5VALWP snubber
3	2/13'08	P.38 P.42	change PR51, PR52 Change PR113,PR127,PR117,PC101,PR129,PC110 Change PQ33,PQ34,PQ36,PQ37	Change CHGVADJ voltage Add CPU boost and snubber for EMI request Change low side Mosfet
4	3/5'08	P.38	Add PQ38,PQ39,PR159,PC129,PR157,PR158	Add wrong adapter protection function
5	3/23'08	P.39 P.37	Add PR160 Change +3VALW->+3VL on Battery port	Add TPS51125/RT8205A p2p Change battery temperature action
6	4/28'08	P.36 P.39 P.39 P.40 P.41	Delete PD6,change PR150 and PR153 Change +3VL->B+ in PU6 pin13 Add PR67,PC127,PR66,PC128 Add PR82,PR83,PC70,PC71 Add PR92,PC82	For ACIN detect to meet wrong adapter function Add 2nd source RT8205A P2P GPS noise GPS noise GPS noise
6	6/219'08	P.38	Change PR45 from 100K_0402_1% to 47K_0402_1%(SD034470280)	For ACIN detect to meet wrong adapter function

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45@ Part

PJP1 45@
DC-JACK

PCB

ZZZ
LA-4161P DAZ BOM--DAZ04G00101

CHIPSET (R1)

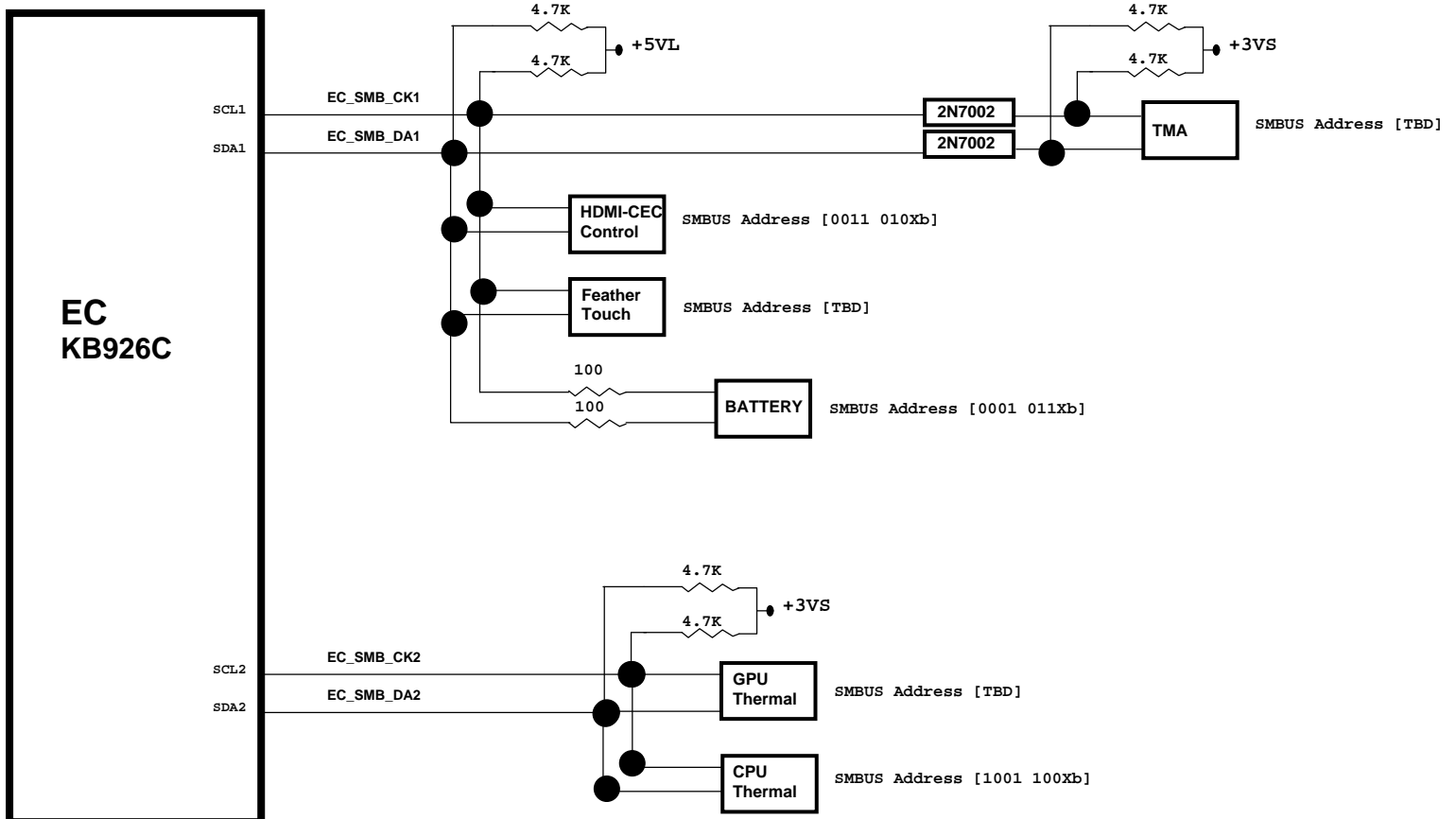
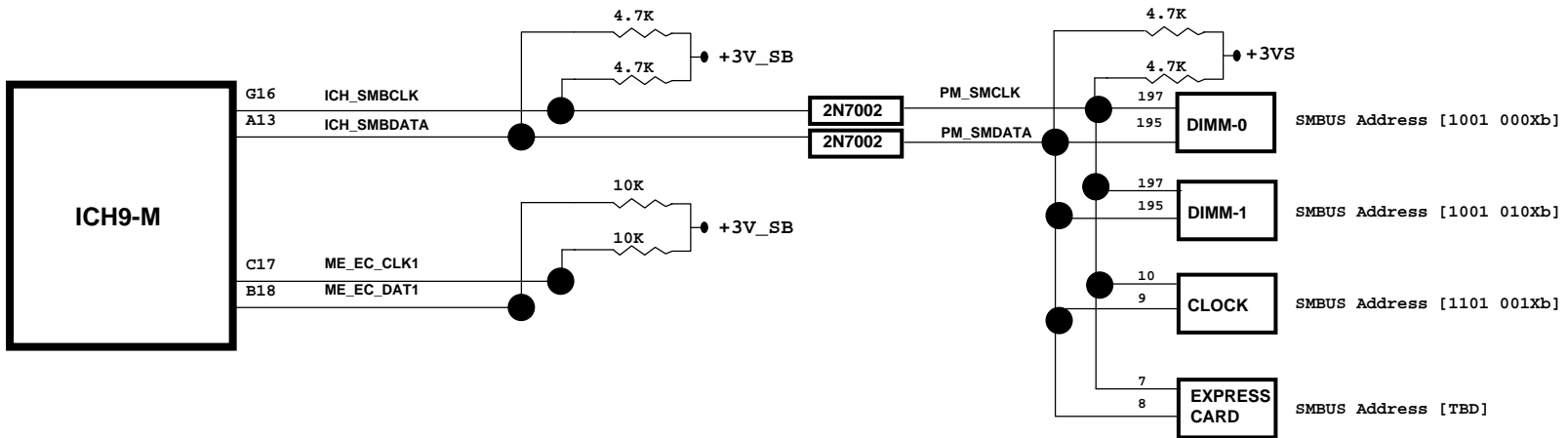
U3 PMR1@ NB-R1 U3 GMLR1@ NB-R1 U3 GMR1@ NB-R1 U10 SBR1@ SB-R1

U3 PMR3@ NB-R3 U3 GMLR3@ NB-R3

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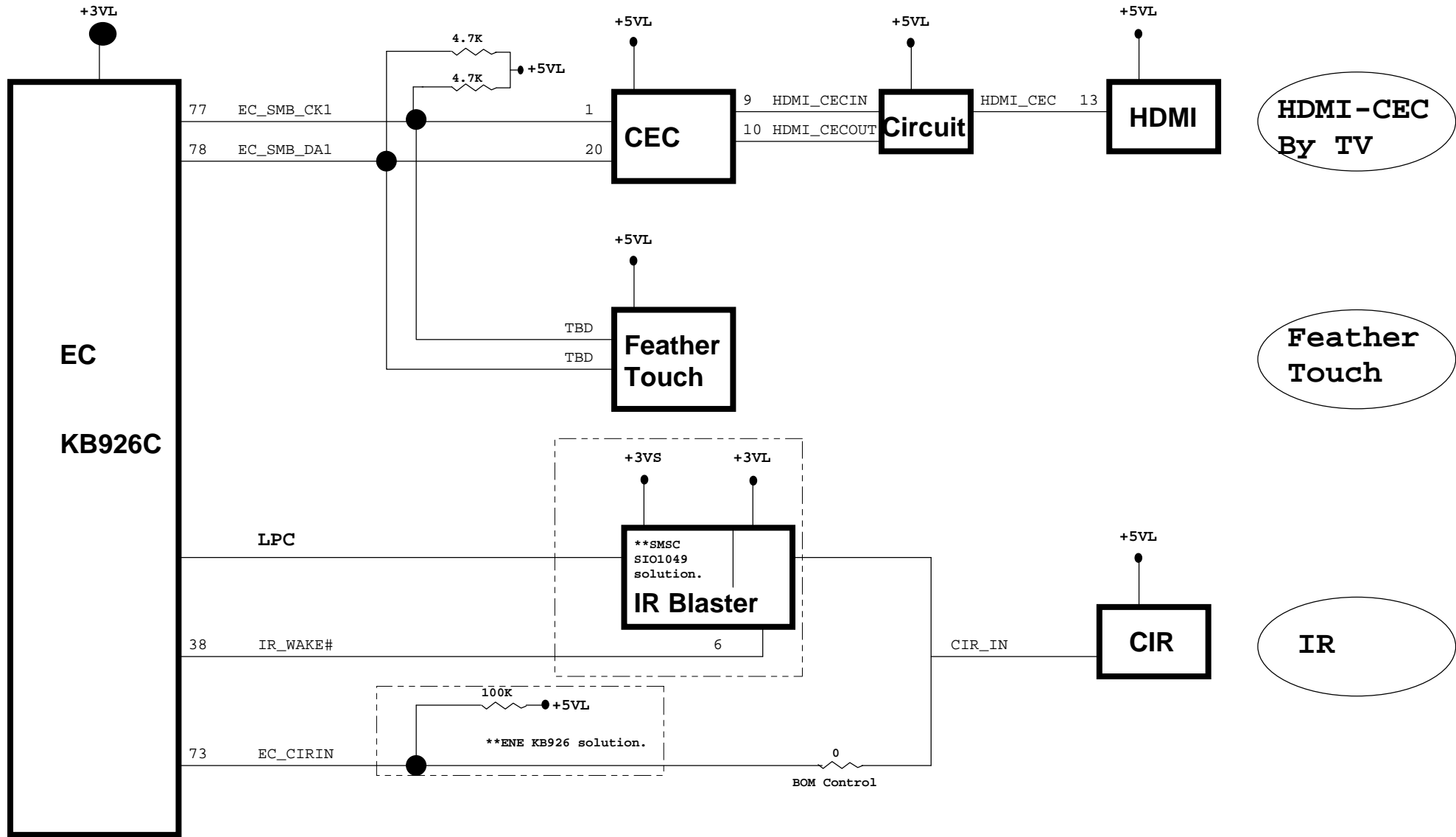
Date	Item	P.	Phase-Description
	1	P.03	PreMP-Remove TMA SMBus, because TMA remove thermal sensor.
	2		PreMP-Change VGA Thermal sensor IC
	3	P.04	PreMP-Set Q20 as @
	4		PreMP-D2 part number change from SC100000Y10 to SC100001M00 for cost.
	5	P.16	PreMP-Delete R727, because remove S I/O debug port.
	6		PreMP-Delete R696, because remove S I/O debug port.
	7		PreMP-Add R52, reserve for GPS test.
	8	P.19	PreMP-R249 change to 976_1% (SD000003280).
	9		PreMP-R253 change to 240_1%, and R255/R257/R258 change to 270_1%.
	10		PreMP-Modify JP9, to increase hole size to 0.5mm
	11		PreMP-Add R48 and R50 for HDMI DEC.
	12		PreMP-Delete Q10A/B dual 2N7002 and add Q10 and Q32 with ow cp, SB501110010.
	13		PreMP-Delete Q130A/B dual 2N7002 and add Q29 and Q31 with ow cp, SB501110010.
	14	P.21	PreMP-Change from LPC_DRQ1# to FELICA_PWR because remove S I/O debug port and Felica enable power not enough.
	15		PreMP-Remove FELICA_PWR because voltage not enough issue.
	16		PreMP-Add R54 for REC_LED
	17		PreMP-Change SSC@ to IHDMI@ and IHDMI@
	18	P.22	PreMP-Remove R358, and place to LED/B
	19		PreMP-Add TV_LED for JPN_TV model
	20	P.24	PreMP-Change HDD connector type to increase two screw hole size.
	21		PreMP-Change HDD type.
	22	P.25	PreMP-Change Felica FFC to FPC and decrease pin to 4pins, and change pin define.
	23	P.26	PreMP-Delete R420/D17, request separate disable pin.
	24		PreMP-Reserve U22/C430 for UWB_OFF#. Add R128 for pass, controlled by EC.
	25	P.27	PreMP-Delete R419/R418/Q135 and remove TMA_THERM#, because TMA remove Thermal sensor, don't need SMBUS again.
	26		PreMP-Change JP22 pin13 to USB_DISABLE#
	27		PreMP-Change JP22 pin20 to USB_DISABLE#
	28	P.28	PreMP-L19 change to 0_0805_5%
	29		PreMP-Delete L20.
	30		PreMP-Add C10 near U20 pins
	31		PreMP-Remove U21 and C545 for cost down plane for new BIOS code.
	32	P.31	PreMP- Remove Q3/Q8/Q136/R1013/R1037 for IR Blaster test
	33		PreMP-Delete R499 and R506, and add R58, R60, R63, R65, R68, R70, R85, R120, R129, R130, R131, R148.
	34		Add Q131, R149 and R150.
	35		
	36	P.32	PreMP-Delete R1031, because TMA remove Thermal Sensor.
	37		PreMP-Delete TMA_THERM# from EC pin31, because TMA remove Thermal Sensor.
	38		PreMP-Add UWB_OFF# on U37 pin31 to separate UWB disable controlled.
	39	P.33	PreMP- Remove JP42, S I/O debug connector.
	40	P.34	PreMP-remove J9 and Pop Q9 for LED behavior.
	41		PreMP-Add TV_LED on JPS2 pin43 for REC Amber LED.
	42		PreMP-Add SW1 at BTN for Debug.
	43		PreMP-Remove R358, and place to LED/B
	44		PreMP-Add R56 for TV_LED
	45	P.35	PreMP-Add R14/R17/R36 near C675/C681/C686 for MOS burned issue. And set all part as STAR@
	46	P.16	PreMP-R689 set as @ and POP R52.
	47		PreMP-For RTC delay, modify C838 and C839 to 18P.
	48	P.18	PreMP-Modify L4/L5/L6, to SM010005X00.
	49	P.19	PreMP-Set HDMI power R1036 as @ and POP D9.
	50	P.31	PreMP-Change R736 and R737 from 33 to 1000hm
	51	P.21	PreMP-Change R386 to 1.5M Ohm (SD028150480) for Discrete; and 1M Ohm (SD028100480) for UMA
	52	P.16	PreMP-Change R728 from 22 to 330hm
	62	P.19	MP-For EMI L11-L14 set as "HDMI@" add and set pass resistor as "@"
	63	P.35	MP-For cost to set SYSON circuit Q54/R570 as "@"
	64	P.21	MP-Modify US VDD circuit (+SSC, VDD) for EMI report.
	65		MP-R302 change to 47-Ohm@100M Bead in JSKAA UMA.
	66		MP- Replace SB00000AR00 (2N7002KDW) by SB00000EO00 (2N7002KDW)
	67		MP- R80, change GM@ to IHDMI@ for Intel display straping define.
	68		MP- 2nd Source problem, L15,L17 change to SM010016720
2009/2/6	69	P.16	MP- Y3: SJ114P3M700 is AP code=X1, change to SJ114P3M210/SJ100001700/SJ114P3MG00

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System support S5(DC) Turn On

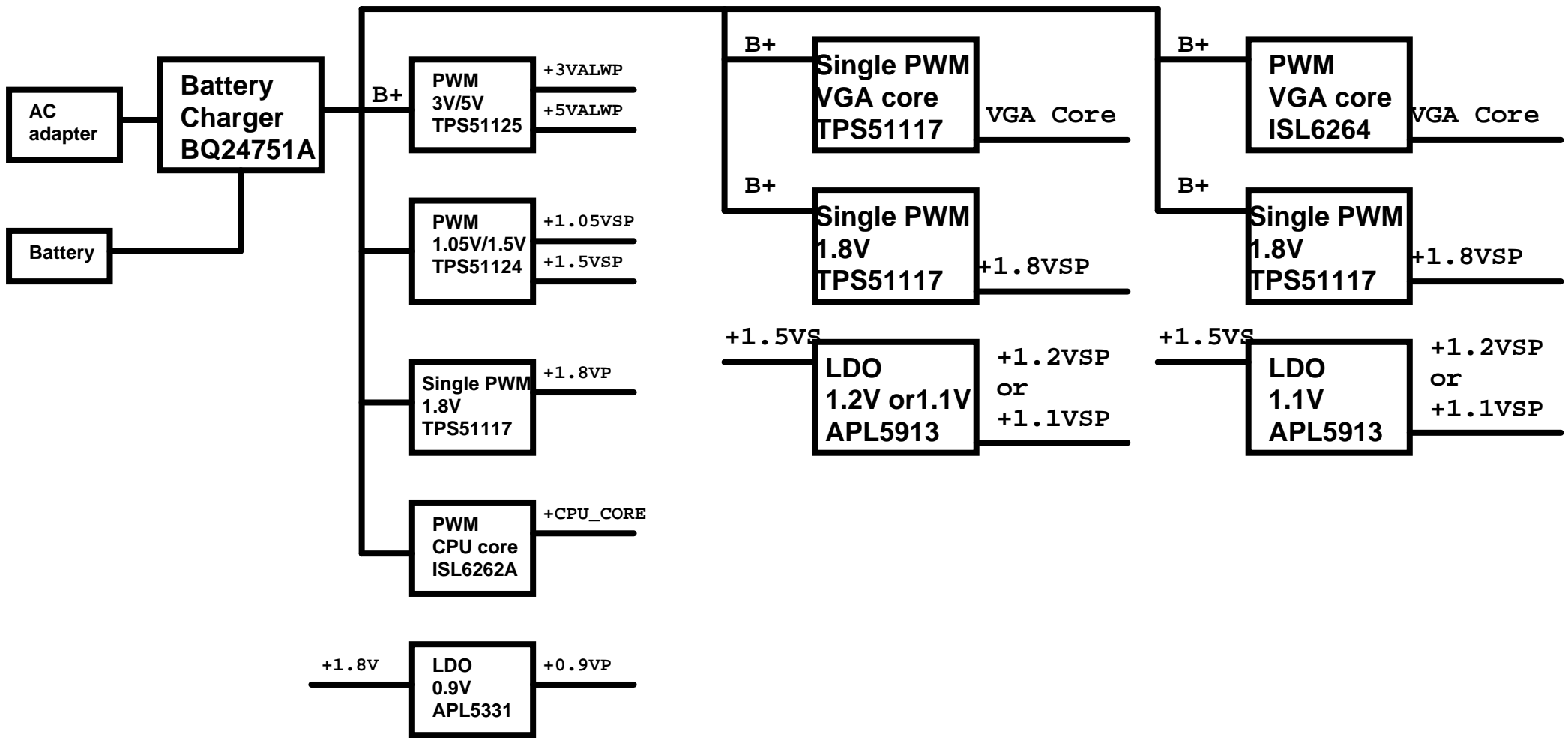


HDMI-CEC
By TV

Feather
Touch

IR

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