Compal Confidential

C560 LA-A061P Schematics Document

INTEL Haswell CPU with DDRIII + PCH Lynx-Point

AIO M/B

September 24, 2013

REV:1.0

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Title: *Cover Page*			
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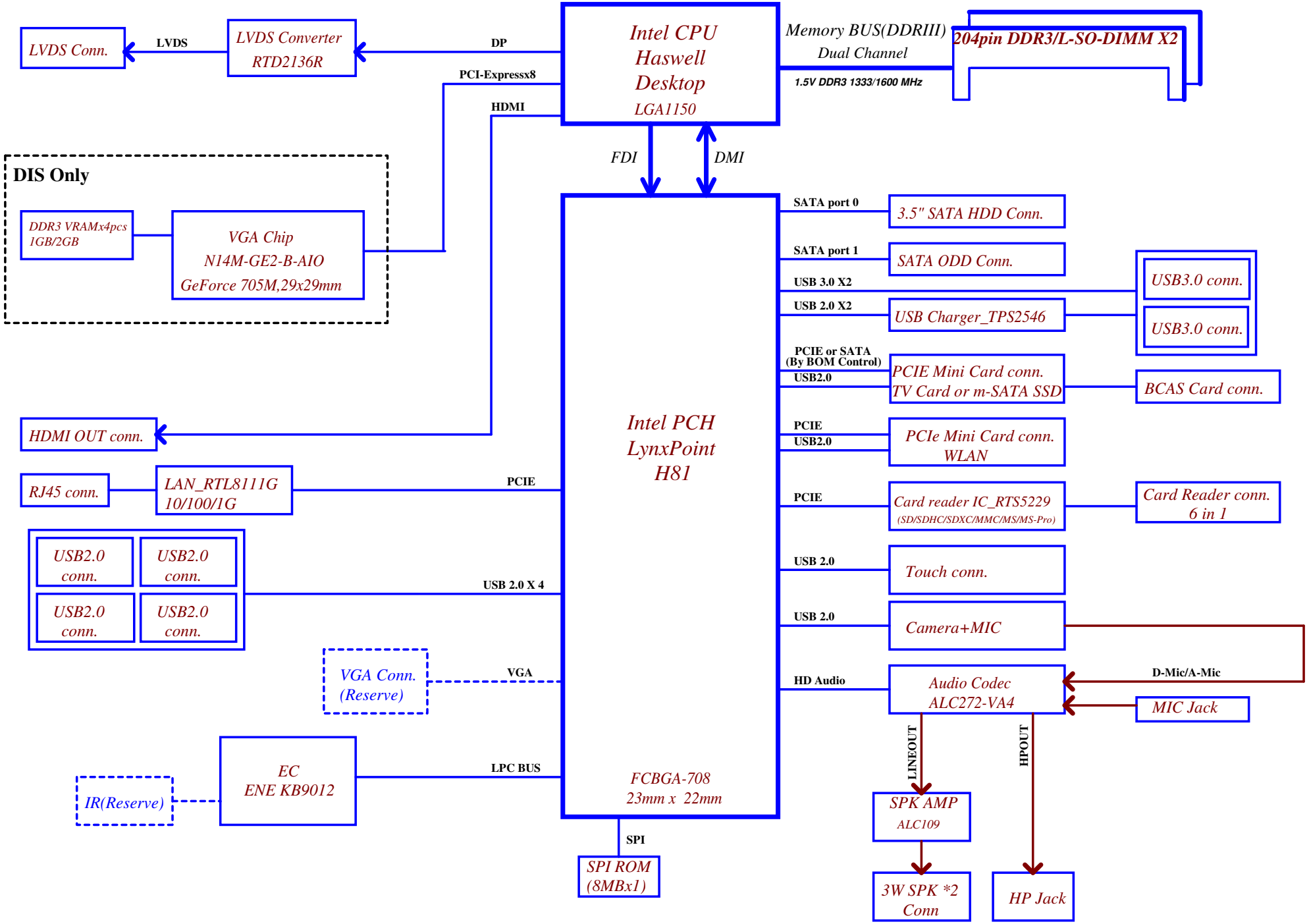

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Title: **Block Diagram**

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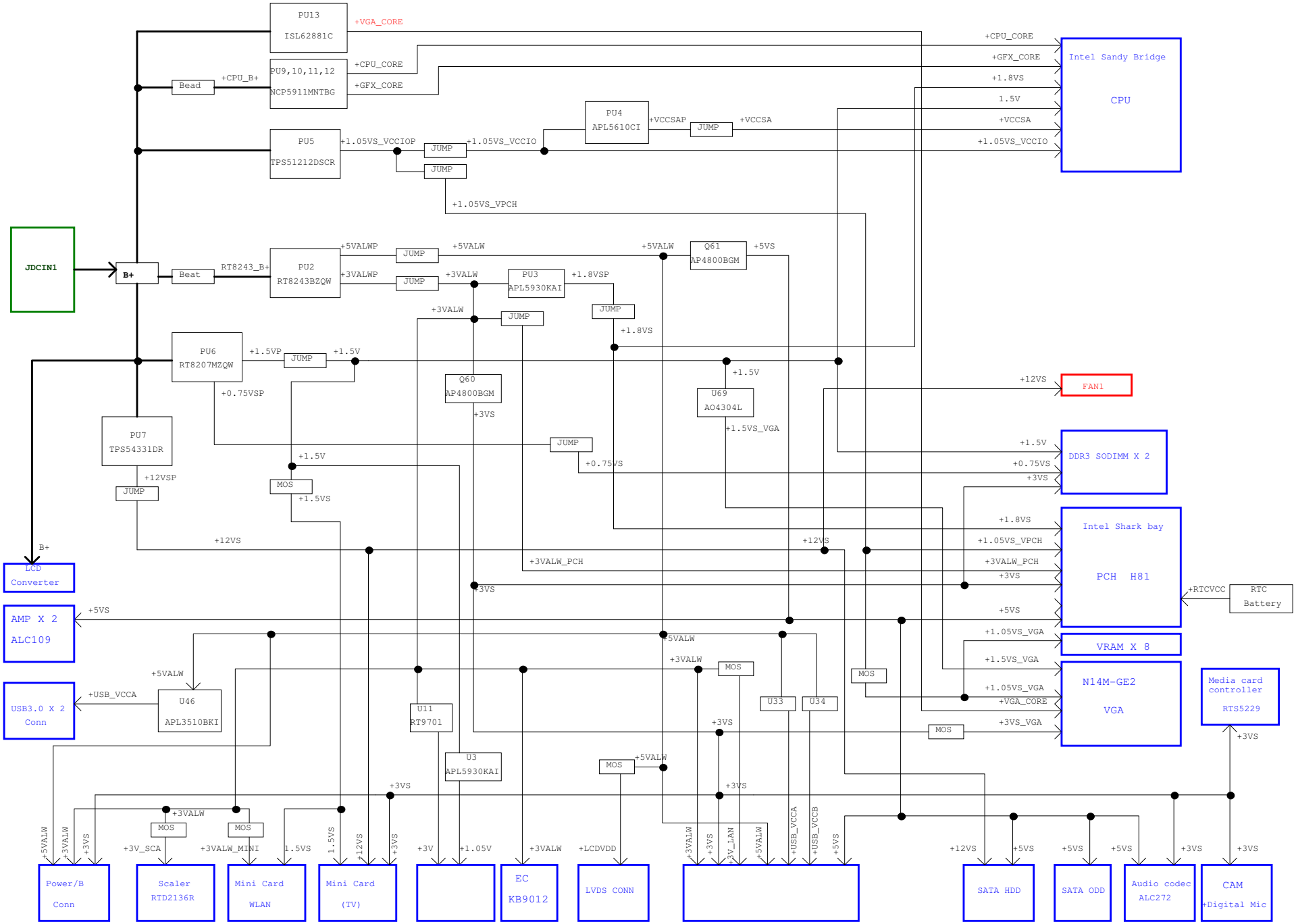

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Title: **Power Tree**

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STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW *1	+VS *2	+1.5V	+0.75VS	+RTCVCC
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	OFF	ON	OFF	ON
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	ON
S5(Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	ON

Note:

*1:+VALW power reail include +3VALW,+5VALW,B+,+VSB,+3VALW_PCH

*2:+VS power reail include +3VS,+5VS,+12VS,+1.05VS_VPCH,+1.5VS_VGA,+VGA_CORE,+CPU_CORE

USB Port Table

USB 2.0	USB 1.1	Port	Device
RMH1	UHCI0	0	Co-lay w/USB30 PORT0
		1	Co-lay w/USB30 PORT1(Debug)
	EHCI1	2	Rear IO USB20 Conn
		3	Rear IO USB20 Conn
	UHCI2	4	WLAN
		5	Touch
	UHCI3	6	Disabled on H81
		7	Disabled on H81
RMH2	UHCI4	8	Rear IO USB20 Conn
		9	Rear IO USB20 Conn(Debug)
	UHCI5	10	TV
		11	Camera
	UHCI6	12	Disabled on H81
		13	Disabled on H81

BOM Structure Table

BTO Item	BOM Structure
ME components	CONN@
UMA Only	UMA@
DISCRETE Only	DIS@
EMI Pop components	EMI@
ESD Pop components	ESD@
EMI Unpop components	@EMI@
ESD Unpop components	@ESD@
HDMI OUT	HDMIO@
TV	TV@
SSD	SSD@
CRT	CRT@(EVTonly)
Unpop	@
VRAM select	X76@
EVT for Reserve components	EVT@
PCB	PCB@
SKU IO Select	GPIO68_H@
	GPIO68_L@
	GPIO69_H@
	GPIO69_L@
	GPIO70_H@
	GPIO70_L@
Touch	TOUCH@
Non Charger	NCHG@
Charger	CHG@

SATA Port Table

Port		Device
6G	0	HDD
	1	m-SATA
3G	2	Disabled on H81
	3	Disabled on H81
	4	ODD
	5	NC

PCIE Port Table

Port	Device
1	LAN
2	Card Reader
3	WLAN
4	TV
5	NC
6	NC
7	Disabled on H81
8	Disabled on H81

BOARD ID Table

Board ID	PCB Revision
0	0.1
3	0.2
4	0.3
5	

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR(JDDRL2)		1010 000X b
+3VS	DDR(JDDRH1)		1010 010X b

EC SM Bus1 Address

Power	Device	HEX	Address
	ALC106	48H	0100_100xb

PCH SML1 Bus Address

Power	Device	HEX	Address
	VGA Ext. thermal sensor		
	VGA Int. thermal sensor (default)		0x9b

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0x0C
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31 - 0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A - 0x59
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A - 0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F - 0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC - 0xFF

SKU ID(Project) Table

Project_ID2 (GPIO68)	Project_ID1 (GPIO69)	Project_ID0 (GPIO70)	SKU	
0	0	0	UMA 4519QH38L04	TV@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_L@ CHG@ GPIO69_L@ GPIO70_L@ PCB@
0	0	1	UMA_W/HDMI 4519QH38L05	HDMIO@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_L@ NCHG@ GPIO69_L@ TOUCH@ GPIO70_H@ PCB@
0	1	0	DIS-MIC1G 4519QH38L06	DIS@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_L@ TOUCH@ GPIO69_H@ GPIO70_L@ PCB@
0	1	1	DIS-SAM1G_W/HDMI 4519QH38L07	DIS@ TV@ HDMIO@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_L@ NCHG@ GPIO69_H@ GPIO70_H@ PCB@
1	0	0	DIS-MIC2G_W/HDMI 4519QH38L08	DIS@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_H@ NCHG@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	0	1	DIS-MIC2G_W/HDMI 4519QH38L09	DIS@ TV@ HDMIO@ NLDO@ EMI@ ESD@ 8111G@ GPIO68_H@ NCHG@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	1	0		
1	1	1		

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Title: Notes List

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Trace width=12mil, spacing 20mil, max L=500mil

PECI 10mil spacing and Max Length < 15"

R11 follow CDB R42PR add 0ohm serial resistor

R12 follow CDB R34PR add 0ohm serial resistor

ESD request Close to CPU as possible

Place C6 close to CPU pin J40 as close as possible. No stub

100 MHz

For BDW new CPU

v0.2 update

HDMI OUT (To Conn.)

FDI For VGA

eDP brightness

eDP (To LVDS Converter)

DP_RCOMP trace width=20mil spacing 25mil length<200mil

v1.0 update

ESD request Close to JCPU1 G40

PU/PD for JTAG signals

v0.2 update
ESD request Close to JCPU1

v0.2 update

PDG P132

HSW A0+LPT A0 change R21 to 4.7K, R19 to 3.3K

Table 8-1. Configuration-wise Mapping of HDMI signals for Processor on DDI ports

Port	Digital Display Interface Differential Pairs	HDMI Signals	Processor Digital Display Interface Pins
Port B	DDIB_TXBN0	HDMIB_TX2_DP	DDIB_TXB[0]
	DDIB_TXBN0	HDMIB_TX2_DN	DDIB_TXB#[0]
	DDIB_TXBP1	HDMIB_TX1_DP	DDIB_TXB[1]
	DDIB_TXBN1	HDMIB_TX1_DN	DDIB_TXB#[1]
	DDIB_TXBP2	HDMIB_TX0_DP	DDIB_TXB[2]
	DDIB_TXBN2	HDMIB_TX0_DN	DDIB_TXB#[2]
	DDIB_TXBP3	HDMIB_CLK_DP	DDIB_TXB[3]
	DDIB_TXBN3	HDMIB_CLK_DN	DDIB_TXB#[3]
	DDPB_HPD	DDSP_1_HPD0	Hot plug detect used by HDMI Port B
	DDPB_CTRLCLK	DDPB_CTRL_CLK	HDMI DDC lines for Port B
	DDPB_CTRLDATA	DDPB_CTRL_CLK	
Port C	DDIC_TXBP0	HDMIC_TX2_DP	DDIC_TXB[0]
	DDIC_TXBN0	HDMIC_TX2_DN	DDIC_TXB#[0]
	DDIC_TXBP1	HDMIC_TX1_DP	DDIC_TXB[1]
	DDIC_TXBN1	HDMIC_TX1_DN	DDIC_TXB#[1]
	DDIC_TXBP2	HDMIC_TX0_DP	DDIC_TXB[2]
	DDIC_TXBN2	HDMIC_TX0_DN	DDIC_TXB#[2]
	DDIC_TXBP3	HDMIC_CLK_DP	DDIC_TXB[3]
	DDIC_TXBN3	HDMIC_CLK_DN	DDIC_TXB#[3]
	DDIPC_HPD	DDSP_2_HPD1	Hot plug detect used by HDMI Port C
	DDIPC_CTRLCLK	DDIPC_CTRL_CLK	HDMI DDC lines for Port C
	DDIPC_CTRLDATA	DDIPC_CTRL_CLK	
Port D	DDID_TXBP0	HDMID_TX2_DP	DDID_TXB[0]
	DDID_TXBN0	HDMID_TX2_DN	DDID_TXB#[0]
	DDID_TXBP1	HDMID_TX1_DP	DDID_TXB[1]
	DDID_TXBN1	HDMID_TX1_DN	DDID_TXB#[1]
	DDID_TXBP2	HDMID_TX0_DP	DDID_TXB[2]
	DDID_TXBN2	HDMID_TX0_DN	DDID_TXB#[2]
	DDID_TXBP3	HDMID_CLK_DP	DDID_TXB[3]
	DDID_TXBN3	HDMID_CLK_DN	DDID_TXB#[3]
	DDIPD_HPD	DDSP_3_HPD2	Hot plug detect used by HDMI Port D
	DDIPD_CTRLCLK	DDIPD_CTRL_CLK	HDMI DDC lines for Port D
	DDIPD_CTRLDATA	DDIPD_CTRL_CLK	

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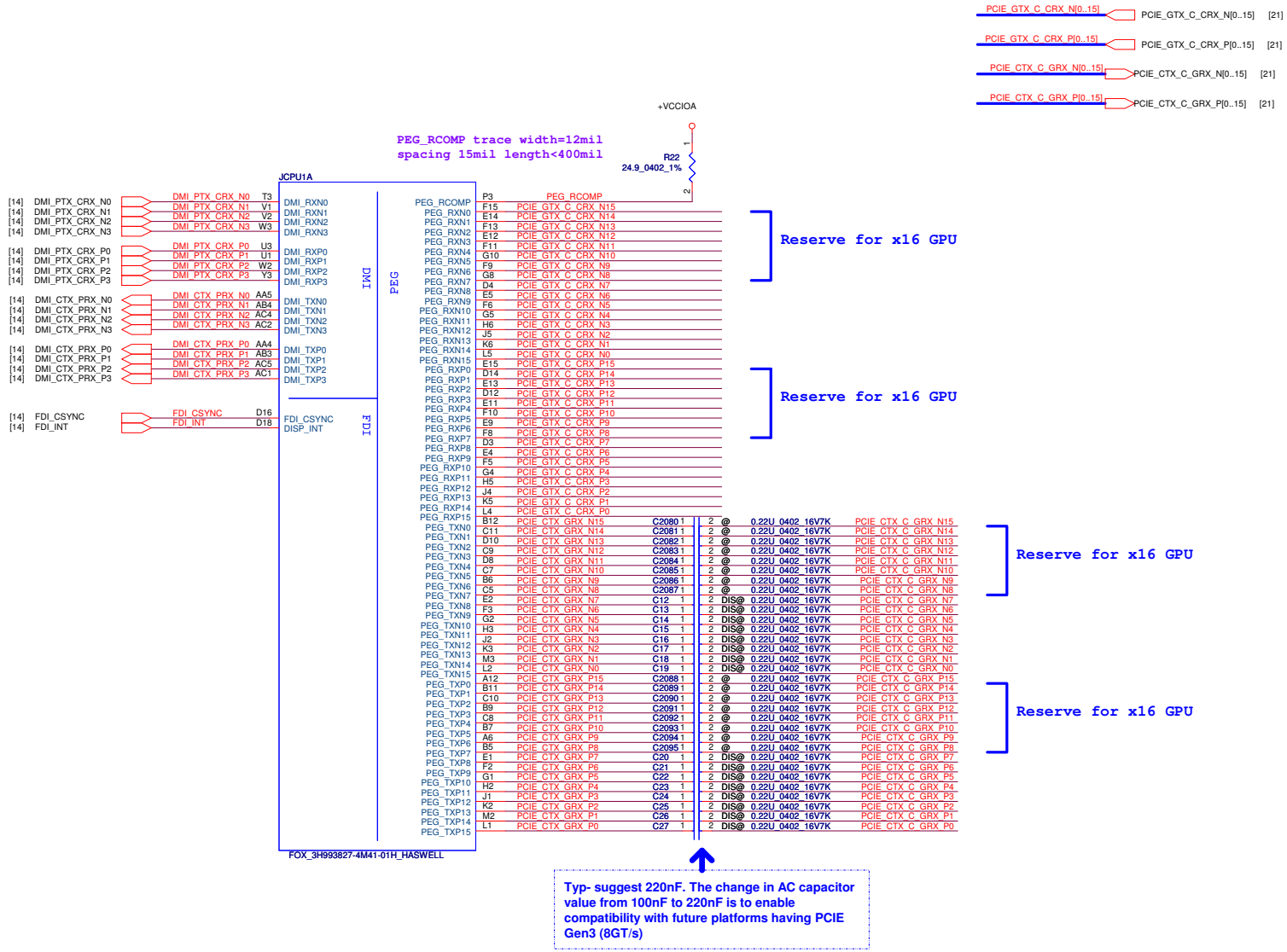

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Title: ***Haswell_DMI/PEG/FDI***

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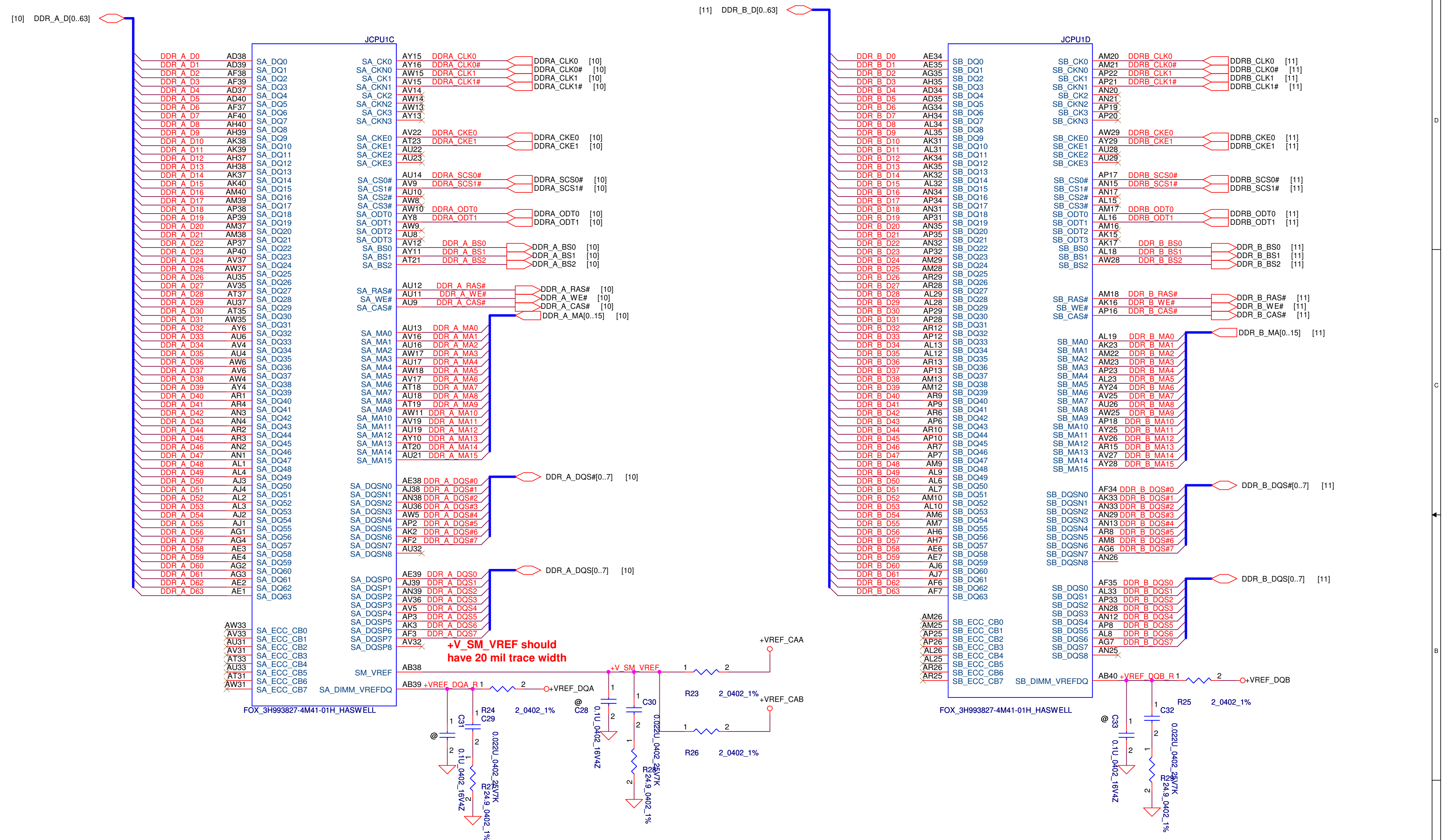

[10] DDR_A_D[0..63]
JCPU1C
DDR_A_D0 AD38 SA_DQ0
DDR_A_D1 AD39 SA_DQ1
DDR_A_D2 AF38 SA_DQ2
DDR_A_D3 AF39 SA_DQ3
DDR_A_D4 AD37 SA_DQ4
DDR_A_D5 AD40 SA_DQ5
DDR_A_D6 AF37 SA_DQ6
DDR_A_D7 AF40 SA_DQ7
DDR_A_D8 AH40 SA_DQ8
DDR_A_D9 AH39 SA_DQ9
DDR_A_D10 AK38 SA_DQ10
DDR_A_D11 AK39 SA_DQ11
DDR_A_D12 AH37 SA_DQ12
DDR_A_D13 AH38 SA_DQ13
DDR_A_D14 AK37 SA_DQ14
DDR_A_D15 AK40 SA_DQ15
DDR_A_D16 AM40 SA_DQ16
DDR_A_D17 AM39 SA_DQ17
DDR_A_D18 AP38 SA_DQ18
DDR_A_D19 AP39 SA_DQ19
DDR_A_D20 AM37 SA_DQ20
DDR_A_D21 AM38 SA_DQ21
DDR_A_D22 AP37 SA_DQ22
DDR_A_D23 AP40 SA_DQ23
DDR_A_D24 AV37 SA_DQ24
DDR_A_D25 AW37 SA_DQ25
DDR_A_D26 AU35 SA_DQ26
DDR_A_D27 AV35 SA_DQ27
DDR_A_D28 AT37 SA_DQ28
DDR_A_D29 AU37 SA_DQ29
DDR_A_D30 AT35 SA_DQ30
DDR_A_D31 AW35 SA_DQ31
DDR_A_D32 AY6 SA_DQ32
DDR_A_D33 AU6 SA_DQ33
DDR_A_D34 AV4 SA_DQ34
DDR_A_D35 AU4 SA_DQ35
DDR_A_D36 AW6 SA_DQ36
DDR_A_D37 AV6 SA_DQ37
DDR_A_D38 AW4 SA_DQ38
DDR_A_D39 AY4 SA_DQ39
DDR_A_D40 AR1 SA_DQ40
DDR_A_D41 AR4 SA_DQ41
DDR_A_D42 AN3 SA_DQ42
DDR_A_D43 AN4 SA_DQ43
DDR_A_D44 AR2 SA_DQ44
DDR_A_D45 AR3 SA_DQ45
DDR_A_D46 AN2 SA_DQ46
DDR_A_D47 AN1 SA_DQ47
DDR_A_D48 AL1 SA_DQ48
DDR_A_D49 AL4 SA_DQ49
DDR_A_D50 AJ3 SA_DQ50
DDR_A_D51 AJ4 SA_DQ51
DDR_A_D52 AL2 SA_DQ52
DDR_A_D53 AL3 SA_DQ53
DDR_A_D54 AJ2 SA_DQ54
DDR_A_D55 AJ1 SA_DQ55
DDR_A_D56 AG1 SA_DQ56
DDR_A_D57 AG4 SA_DQ57
DDR_A_D58 AE3 SA_DQ58
DDR_A_D59 AE4 SA_DQ59
DDR_A_D60 AG2 SA_DQ60
DDR_A_D61 AG3 SA_DQ61
DDR_A_D62 AE2 SA_DQ62
DDR_A_D63 AE1 SA_DQ63
AW33 SA_ECC_CB0
AV33 SA_ECC_CB1
AU31 SA_ECC_CB2
AV31 SA_ECC_CB3
AT33 SA_ECC_CB4
AU33 SA_ECC_CB5
AT31 SA_ECC_CB6
AW31 SA_ECC_CB7
SA_CK0 AY15 DDRA_CLK0 DDRA_CLK0 [10]
SA_CKN0 AY16 DDRA_CLK0# DDRA_CLK0# [10]
SA_CK1 AW15 DDRA_CLK1 DDRA_CLK1 [10]
SA_CKN1 AV15 DDRA_CLK1# DDRA_CLK1# [10]
SA_CK2 AV14
SA_CKN2 AW14
SA_CK3 AW13
SA_CKN3 AY13
SA_CKE0 AV22 DDRA_CKE0 DDRA_CKE0 [10]
SA_CKE1 AT23 DDRA_CKE1 DDRA_CKE1 [10]
SA_CKE2 AU22
SA_CKE3 AU23
SA_CS0# AU14 DDRA_SCS0# DDRA_SCS0# [10]
SA_CS1# AV9 DDRA_SCS1# DDRA_SCS1# [10]
SA_CS2# AU10
SA_CS3# AW8
SA_ODT0 AW10 DDRA_ODT0 DDRA_ODT0 [10]
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SA_ODT2 AW9
SA_ODT3 AU8
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SA_BS1 AY11 DDR_A_BS1 DDR_A_BS1 [10]
SA_BS2 AT21 DDR_A_BS2 DDR_A_BS2 [10]
SA_RAS# AU12 DDR_A_RAS# DDR_A_RAS# [10]
SA_WE# AU11 DDR_A_WE# DDR_A_WE# [10]
SA_CAS# AU9 DDR_A_CAS# DDR_A_CAS# [10]
DDR_A_MA[0..15] [10]
SA_MA0 AU13 DDR_A_MA0
SA_MA1 AV16 DDR_A_MA1
SA_MA2 AU16 DDR_A_MA2
SA_MA3 AW17 DDR_A_MA3
SA_MA4 AU17 DDR_A_MA4
SA_MA5 AW18 DDR_A_MA5
SA_MA6 AV17 DDR_A_MA6
SA_MA7 AT18 DDR_A_MA7
SA_MA8 AU18 DDR_A_MA8
SA_MA9 AT19 DDR_A_MA9
SA_MA10 AW11 DDR_A_MA10
SA_MA11 AV19 DDR_A_MA11
SA_MA12 AU19 DDR_A_MA12
SA_MA13 AY10 DDR_A_MA13
SA_MA14 AT20 DDR_A_MA14
SA_MA15 AU21 DDR_A_MA15
DDR_A_DQS#[0..7] [10]
SA_DQSN0 AE38 DDR_A_DQS#0
SA_DQSN1 AJ38 DDR_A_DQS#1
SA_DQSN2 AN38 DDR_A_DQS#2
SA_DQSN3 AU36 DDR_A_DQS#3
SA_DQSN4 AW5 DDR_A_DQS#4
SA_DQSN5 AP2 DDR_A_DQS#5
SA_DQSN6 AK2 DDR_A_DQS#6
SA_DQSN7 AF2 DDR_A_DQS#7
SA_DQSN8 AU32
DDR_A_DQS[0..7] [10]
SA_DQSP0 AE39 DDR_A_DQS0
SA_DQSP1 AJ39 DDR_A_DQS1
SA_DQSP2 AN39 DDR_A_DQS2
SA_DQSP3 AV36 DDR_A_DQS3
SA_DQSP4 AV5 DDR_A_DQS4
SA_DQSP5 AP3 DDR_A_DQS5
SA_DQSP6 AK3 DDR_A_DQS6
SA_DQSP7 AF3 DDR_A_DQS7
SA_DQSP8 AV32
+V_SM_VREF should
have 20 mil trace width
SM_VREF AB38 +V_SM_VREF
SA_DIMM_VREFDQ AB39 +VREF_DQA_R
FOX_3H993827-4M41-01H_HASWELL
R24 2_0402_1% +VREF_DQA
C29 0.022U_0402_25V7K
C31 0.1U_0402_16V4Z @
R27 24.9_0402_1%
C28 0.1U_0402_16V4Z @
C30 0.022U_0402_25V7K
R28 24.9_0402_1%
R23 2_0402_1% +VREF_CAA
R26 2_0402_1% +VREF_CAB
[11] DDR_B_D[0..63]
JCPU1D
DDR_B_D0 AE34 SB_DQ0
DDR_B_D1 AE35 SB_DQ1
DDR_B_D2 AG35 SB_DQ2
DDR_B_D3 AH35 SB_DQ3
DDR_B_D4 AD34 SB_DQ4
DDR_B_D5 AD35 SB_DQ5
DDR_B_D6 AG34 SB_DQ6
DDR_B_D7 AH34 SB_DQ7
DDR_B_D8 AL34 SB_DQ8
DDR_B_D9 AL35 SB_DQ9
DDR_B_D10 AK31 SB_DQ10
DDR_B_D11 AL31 SB_DQ11
DDR_B_D12 AK34 SB_DQ12
DDR_B_D13 AK35 SB_DQ13
DDR_B_D14 AK32 SB_DQ14
DDR_B_D15 AL32 SB_DQ15
DDR_B_D16 AN34 SB_DQ16
DDR_B_D17 AP34 SB_DQ17
DDR_B_D18 AN31 SB_DQ18
DDR_B_D19 AP31 SB_DQ19
DDR_B_D20 AN35 SB_DQ20
DDR_B_D21 AP35 SB_DQ21
DDR_B_D22 AN32 SB_DQ22
DDR_B_D23 AP32 SB_DQ23
DDR_B_D24 AM29 SB_DQ24
DDR_B_D25 AM28 SB_DQ25
DDR_B_D26 AR29 SB_DQ26
DDR_B_D27 AR28 SB_DQ27
DDR_B_D28 AL29 SB_DQ28
DDR_B_D29 AL28 SB_DQ29
DDR_B_D30 AP29 SB_DQ30
DDR_B_D31 AP28 SB_DQ31
DDR_B_D32 AR12 SB_DQ32
DDR_B_D33 AP12 SB_DQ33
DDR_B_D34 AL13 SB_DQ34
DDR_B_D35 AL12 SB_DQ35
DDR_B_D36 AR13 SB_DQ36
DDR_B_D37 AP13 SB_DQ37
DDR_B_D38 AM13 SB_DQ38
DDR_B_D39 AM12 SB_DQ39
DDR_B_D40 AR9 SB_DQ40
DDR_B_D41 AP9 SB_DQ41
DDR_B_D42 AR6 SB_DQ42
DDR_B_D43 AP6 SB_DQ43
DDR_B_D44 AR10 SB_DQ44
DDR_B_D45 AP10 SB_DQ45
DDR_B_D46 AR7 SB_DQ46
DDR_B_D47 AP7 SB_DQ47
DDR_B_D48 AM9 SB_DQ48
DDR_B_D49 AL9 SB_DQ49
DDR_B_D50 AL6 SB_DQ50
DDR_B_D51 AL7 SB_DQ51
DDR_B_D52 AM10 SB_DQ52
DDR_B_D53 AL10 SB_DQ53
DDR_B_D54 AM6 SB_DQ54
DDR_B_D55 AM7 SB_DQ55
DDR_B_D56 AH6 SB_DQ56
DDR_B_D57 AH7 SB_DQ57
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DDR_B_D60 AJ6 SB_DQ60
DDR_B_D61 AJ7 SB_DQ61
DDR_B_D62 AF6 SB_DQ62
DDR_B_D63 AF7 SB_DQ63
AM26 SB_ECC_CB0
AM25 SB_ECC_CB1
AP25 SB_ECC_CB2
AP26 SB_ECC_CB3
AL26 SB_ECC_CB4
AL25 SB_ECC_CB5
AR26 SB_ECC_CB6
AR25 SB_ECC_CB7
SB_CK0 AM20 DDRB_CLK0 DDRB_CLK0 [11]
SB_CKN0 AM21 DDRB_CLK0# DDRB_CLK0# [11]
SB_CK1 AP22 DDRB_CLK1 DDRB_CLK1 [11]
SB_CKN1 AP21 DDRB_CLK1# DDRB_CLK1# [11]
SB_CK2 AN20
SB_CKN2 AN21
SB_CK3 AP19
SB_CKN3 AP20
SB_CKE0 AW29 DDRB_CKE0 DDRB_CKE0 [11]
SB_CKE1 AY29 DDRB_CKE1 DDRB_CKE1 [11]
SB_CKE2 AU28
SB_CKE3 AU29
SB_CS0# AP17 DDRB_SCS0# DDRB_SCS0# [11]
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SB_CAS# AP16 DDR_B_CAS# DDR_B_CAS# [11]
DDR_B_MA[0..15] [11]
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SB_MA1 AK23 DDR_B_MA1
SB_MA2 AM22 DDR_B_MA2
SB_MA3 AM23 DDR_B_MA3
SB_MA4 AP23 DDR_B_MA4
SB_MA5 AL23 DDR_B_MA5
SB_MA6 AY24 DDR_B_MA6
SB_MA7 AV25 DDR_B_MA7
SB_MA8 AU26 DDR_B_MA8
SB_MA9 AW25 DDR_B_MA9
SB_MA10 AP18 DDR_B_MA10
SB_MA11 AY25 DDR_B_MA11
SB_MA12 AV26 DDR_B_MA12
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SB_MA15 AY28 DDR_B_MA15
DDR_B_DQS#[0..7] [11]
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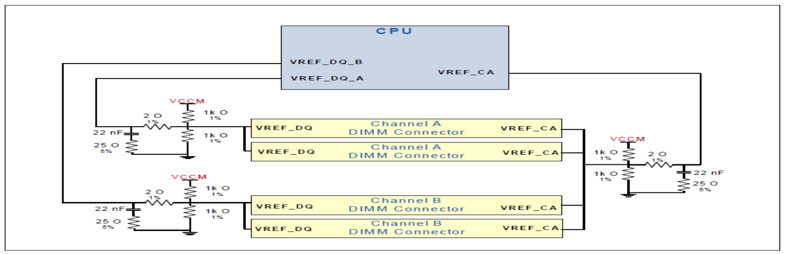
SB_DQSN1 AK33 DDR_B_DQS#1
SB_DQSN2 AN33 DDR_B_DQS#2
SB_DQSN3 AN29 DDR_B_DQS#3
SB_DQSN4 AN13 DDR_B_DQS#4
SB_DQSN5 AR8 DDR_B_DQS#5
SB_DQSN6 AM8 DDR_B_DQS#6
SB_DQSN7 AG6 DDR_B_DQS#7
SB_DQSN8 AN26
DDR_B_DQS[0..7] [11]
SB_DQS0 AF35 DDR_B_DQS0
SB_DQS1 AL33 DDR_B_DQS1
SB_DQS2 AP33 DDR_B_DQS2
SB_DQS3 AN28 DDR_B_DQS3
SB_DQS4 AN12 DDR_B_DQS4
SB_DQS5 AP8 DDR_B_DQS5
SB_DQS6 AL8 DDR_B_DQS6
SB_DQS7 AG7 DDR_B_DQS7
SB_DQS8 AN25
SB_DIMM_VREFDQ AB40 +VREF_DQB_R
R25 2_0402_1% +VREF_DQB
C32 0.022U_0402_25V7K
C33 0.1U_0402_16V4Z @
R29 24.9_0402_1%
FOX_3H993827-4M41-01H_HASWELL

DDR3 VREF Topologies

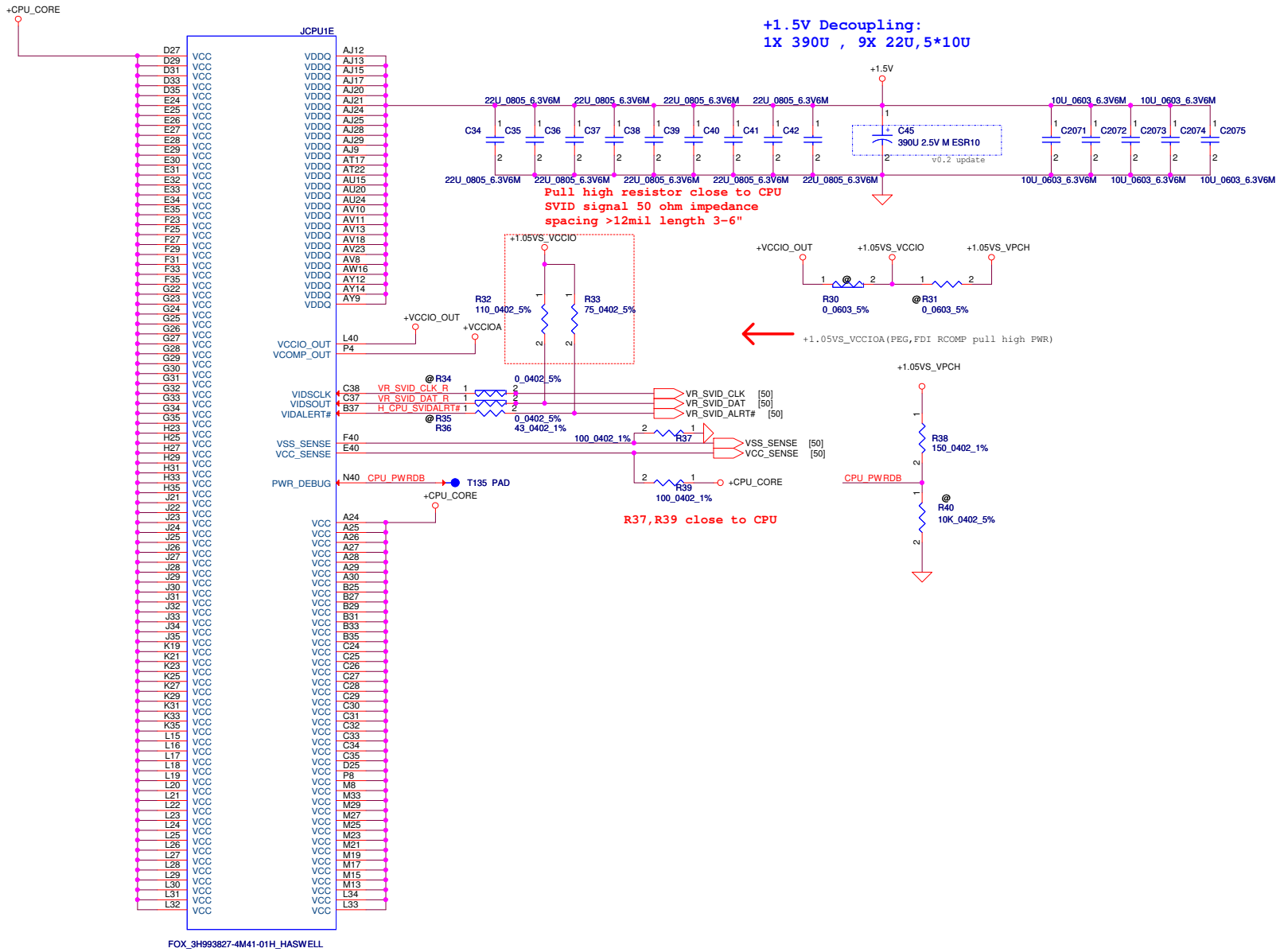


Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: *Haswell_DDR3*

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3



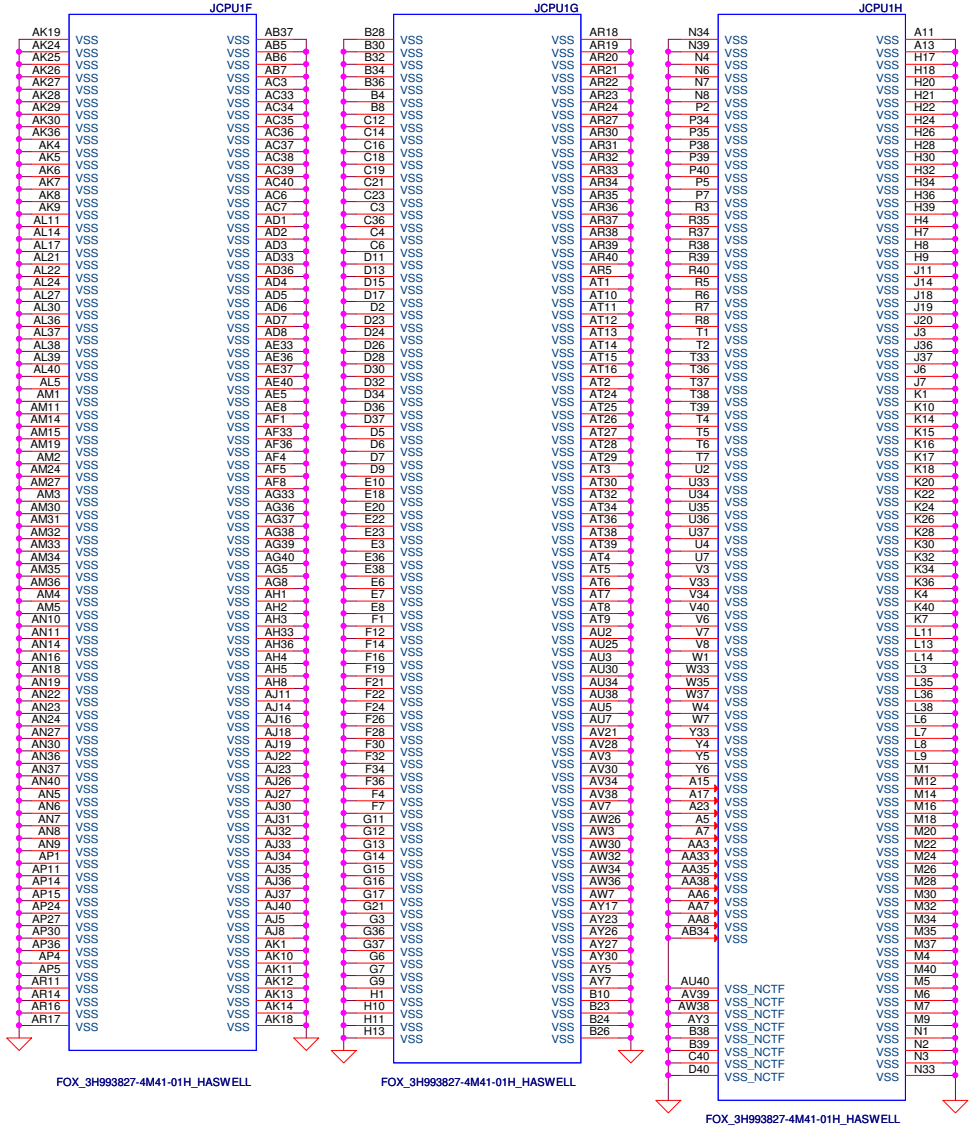
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

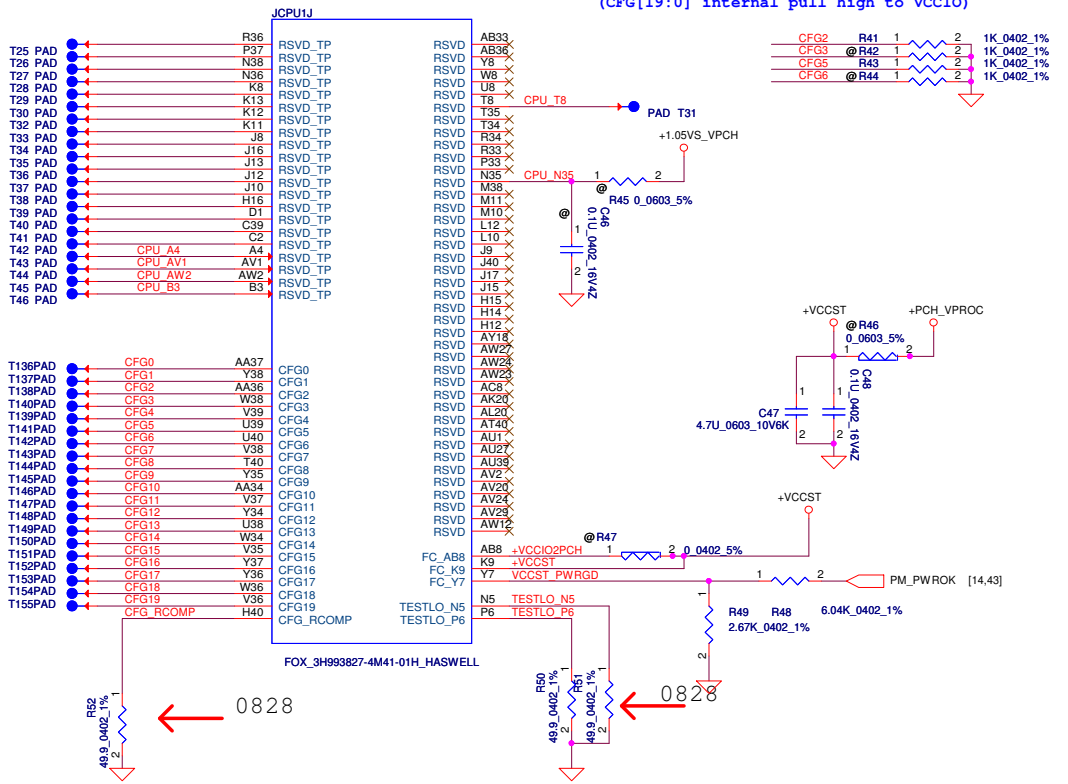
Compal Electronics, Inc.

Title: ***Haswell_POWER***

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 8 of 59





Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting – 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:**[1] – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	Haswell_GND/CFG		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
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[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..15]

CHA SO-DIMM 0(A0)

R626 1K_0402_1% +1.5V +VREF_DQA
R627 1K_0402_1%
C2030 0.1U_0402_16V4Z
C2031 2.2U_0603_6.3V6K
Close to JDIMM1

JDIMM1

1	VREF_DQ	+VREF_DQA	2	VSS1		
3	VSS2		4	DQ4	DDR_A_D4	
5	DQ0	DDR_A_D0	6	DQ5	DDR_A_D5	
7	DQ1	DDR_A_D1	8	VSS3		
9	VSS4		10	DQS#0	DDR_A_DQS#0	
11	DM0		12	DQS0	DDR_A_DQS0	
13	VSS5		14	VSS6		
15	DQ2	DDR_A_D2	16	DQ6	DDR_A_D6	
17	DQ3	DDR_A_D3	18	DQ7	DDR_A_D7	
19	VSS7		20	VSS8		
21	DQ8	DDR_A_D8	22	DQ12	DDR_A_D12	
23	DQ9	DDR_A_D9	24	DQ13	DDR_A_D13	
25	VSS9		26	VSS10		
27	DQS#1	DDR_A_DQS#1	28	DM1		
29	DQS1	DDR_A_DQS1	30	RESET#	SM_DRAMRST#	[11,5]
31	VSS11		32	VSS12		
33	DQ10	DDR_A_D10	34	DQ14	DDR_A_D14	
35	DQ11	DDR_A_D11	36	DQ15	DDR_A_D15	
37	VSS13		38	VSS14		
39	DQ16	DDR_A_D16	40	DQ20	DDR_A_D20	
41	DQ17	DDR_A_D17	42	DQ21	DDR_A_D21	
43	VSS15		44	VSS16		
45	DQS#2	DDR_A_DQS#2	46	DM2		
47	DQS2	DDR_A_DQS2	48	VSS17		
49	VSS18		50	DQ22	DDR_A_D22	
51	DQ18	DDR_A_D18	52	DQ23	DDR_A_D23	
53	DQ19	DDR_A_D19	54	VSS19		
55	VSS20		56	DQ28	DDR_A_D28	
57	DQ24	DDR_A_D24	58	DQ29	DDR_A_D29	
59	DQ25	DDR_A_D25	60	VSS21		
61	VSS22		62	DQS#3	DDR_A_DQS#3	
63	DM3		64	DQS3	DDR_A_DQS3	
65	VSS23		66	VSS24		
67	DQ26	DDR_A_D26	68	DQ30	DDR_A_D30	
69	DQ27	DDR_A_D27	70	DQ31	DDR_A_D31	
71	VSS25		72	VSS26		
73	CKE0	[7] DDRA_CKE0 DDRA_CKE0	74	CKE1	DDRA_CKE1	DDRA_CKE1 [7]
75	VDD1		76	VDD2		
77	NC1		78	A15	DDR_A_MA15	
79	BA2	[7] DDR_A_BS2	80	A14	DDR_A_MA14	
81	VDD3		82	VDD4		
83	A12/BC#	DDR_A_MA12	84	A11	DDR_A_MA11	
85	A9	DDR_A_MA9	86	A7	DDR_A_MA7	
87	VDD5		88	VDD6		
89	A8	DDR_A_MA8	90	A6	DDR_A_MA6	
91	A5	DDR_A_MA5	92	A4	DDR_A_MA4	
93	VDD7		94	VDD8		
95	A3	DDR_A_MA3	96	A2	DDR_A_MA2	
97	A1	DDR_A_MA1	98	A0	DDR_A_MA0	
99	VDD9		100	VDD10		
101	CK0	DDRA_CLK0 [7] DDRA_CLK0#	102	CK1	DDRA_CLK1	DDRA_CLK1 [7]
103	CK0#	DDRA_CLK0#	104	CK1#	DDRA_CLK1#	DDRA_CLK1# [7]
105	VDD11		106	VDD12		
107	A10/AP	DDR_A_MA10	108	BA1	DDR_A_BS1	DDR_A_BS1 [7]
109	BA0	[7] DDR_A_BS0	110	RAS#	DDR_A_RAS#	DDR_A_RAS# [7]
111	VDD13		112	VDD14		
113	WE#	[7] DDR_A_WE# DDR_A_WE#	114	S0#	DDRA_SCS0#	DDRA_SCS0# [7]
115	CAS#	[7] DDR_A_CAS# DDR_A_CAS#	116	ODT0	DDRA_ODT0	DDRA_ODT0 [7]
117	VDD15		118	VDD16		
119	A13	DDR_A_MA13	120	ODT1	DDRA_ODT1	DDRA_ODT1 [7]
121	S1#	[7] DDRA_SCS1# DDRA_SCS1#	122	NC2		
123	VDD17		124	VDD18		
125	NCTEST		126	VREF_CA	+VREF_CAA	
127	VSS27		128	VSS28		
129	DQ32	DDR_A_D32	130	DQ36	DDR_A_D36	
131	DQ33	DDR_A_D33	132	DQ37	DDR_A_D37	
133	VSS29		134	VSS30		
135	DQS#4	DDR_A_DQS#4	136	DM4		
137	DQS4	DDR_A_DQS4	138	VSS31		
139	VSS32		140	DQ38	DDR_A_D38	
141	DQ34	DDR_A_D34	142	DQ39	DDR_A_D39	
143	DQ35	DDR_A_D35	144	VSS33		
145	VSS34		146	DQ44	DDR_A_D44	
147	DQ40	DDR_A_D40	148	DQ45	DDR_A_D45	
149	DQ41	DDR_A_D41	150	VSS35		
151	VSS36		152	DQS#5	DDR_A_DQS#5	
153	DM5		154	DQS5	DDR_A_DQS5	
155	VSS37		156	VSS38		
157	DQ42	DDR_A_D42	158	DQ46	DDR_A_D46	
159	DQ43	DDR_A_D43	160	DQ47	DDR_A_D47	
161	VSS39		162	VSS40		
163	DQ48	DDR_A_D48	164	DQ52	DDR_A_D52	
165	DQ49	DDR_A_D49	166	DQ53	DDR_A_D53	
167	VSS41		168	VSS42		
169	DQS#6	DDR_A_DQS#6	170	DM6		
171	DQS6	DDR_A_DQS6	172	VSS43		
173	VSS44		174	DQ54	DDR_A_D54	
175	DQ50	DDR_A_D50	176	DQ55	DDR_A_D55	
177	DQ51	DDR_A_D51	178	VSS45		
179	VSS46		180	DQ60	DDR_A_D60	
181	DQ56	DDR_A_D56	182	DQ61	DDR_A_D61	
183	DQ57	DDR_A_D57	184	VSS47		
185	VSS48		186	DQS#7	DDR_A_DQS#7	
187	DM7		188	DQS7	DDR_A_DQS7	
189	VSS49		190	VSS50		
191	DQ58	DDR_A_D58	192	DQ62	DDR_A_D62	
193	DQ59	DDR_A_D59	194	DQ63	DDR_A_D63	
195	VSS51		196	VSS52		
197	SA0		198	EVENT#		
199	VDDSPD		200	SDA	PM_SMBDATA	PM_SMBDATA [11,13,40,5]
201	SA1		202	SCL	PM_SMBCLK	PM_SMBCLK [11,13,40,5]
203	VTT1		204	VTT2	+0.75VS	
205	G1		206	G2		

FOX_AS0A626-U2SN-7F
CONN@

Standard H:5.2mm

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

+3VS +0.75VS
C2045 2.2U_0603_6.3V6K
C2046 0.1U_0402_16V4Z
R630 @ 0_0402_5% @

Layout Note: Place near JDIMM1

+1.5V
C2032 390U 2.5V M ESR10
C2033 10U_0805_6.3V6M
C2034 10U_0805_6.3V6M
C2035 10U_0805_6.3V6M
C2036 C2037 C2038 C2039 C2040 C2041 C2042 C2043 0.1U_0402_16V4Z

Layout Note: Place these Caps near +1.5V of JDIMM1

+1.5V
R628 1K_0402_1%
+VREF_CAA
R629 1K_0402_1%
C2044 2.2U_0603_6.3V6K
C2045 0.1U_0402_16V4Z
close to JDIMM1.126

Layout Note: Place near JDIMM1 Pin203 and 204

+0.75VS
C2046 4.7U_0603_6.3V6K
C2047 0.1U_0402_16V4Z

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Issued Date	2013/04/01	Deciphered Date	2014/04/01

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Compal Electronics, Inc.

Title: ***DDRIII-SODIMMA***

Size	Document Number	Rev
C	ZEA00 LA-A061P M/B	0.3

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[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]
[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..15]

CHB SO-DIMM

JDIMM2

1	VREF_DQ	VSS1	2		3	VSS2	DQ0	4	DDR_B_D4
5	DDR_B_D0	DQ1	6	DDR_B_D5	7	DDR_B_D1	VSS3	8	
9	VSS4	DQS#0	10	DDR_B_DQS#0	11	DM0	DQS0	12	DDR_B_DQS0
13	VSS5	DQ2	14		15	DDR_B_D2	VSS6	16	DDR_B_D6
17	DDR_B_D3	DQ3	18	DDR_B_D7	19	DQ4	VSS7	20	
21	DDR_B_D8	DQ5	22	DDR_B_D12	23	DDR_B_D9	VSS8	24	DDR_B_D13
25	DQ6	DQ12	26		27	VSS9	DQ7	28	
29	DDR_B_DQS#1	DQ13	30	SM_DRAMRST#	31	DDR_B_DQS1	VSS10	32	
33	VSS11	DQS#1	34	DDR_B_D14	35	DDR_B_D11	DM1	36	DDR_B_D15
37	DQ10	RESET#	38		39	VSS13	VSS12	40	DDR_B_D20
41	DDR_B_D16	DQ11	42	DDR_B_D21	43	DDR_B_D17	VSS14	44	
45	VSS15	DQ16	46		47	DDR_B_DQS#2	DQ17	48	
49	DQS2	VSS16	50	DDR_B_D22	51	DDR_B_D18	DM2	52	DDR_B_D23
53	DDR_B_D19	DQS#2	54		55	VSS18	DQ18	56	DDR_B_D28
57	DDR_B_D24	DQ19	58	DDR_B_D29	59	DDR_B_D25	VSS19	60	
61	VSS20	DQ24	62	DDR_B_DQS#3	63	VSS22	DQ25	64	DDR_B_DQS3
65	DM3	DQS3	66		67	DDR_B_D26	VSS23	68	DDR_B_D30
69	DDR_B_D27	DQ26	70	DDR_B_D31	71	VSS25	DQ27	72	
73	[7] DDRB_CKE0	CKE0	74	DDRB_CKE1	75	VDD1	CKE1	76	DDRB_CKE1 [7]
77	NC1	VDD2	78	DDR_B_MA15	79	[7] DDR_B_BS2	BA2	80	DDR_B_MA14
81	VDD3	A15	82		83	DDR_B_MA12	A12/BC#	84	DDR_B_MA11
85	DDR_B_MA9	A11	86	DDR_B_MA7	87	A9	A7	88	
89	DDR_B_MA8	VDD5	90	DDR_B_MA6	91	DDR_B_MA5	A8	92	DDR_B_MA4
93	A5	A4	94		95	DDR_B_MA3	VDD7	96	DDR_B_MA2
97	DDR_B_MA1	A3	98	DDR_B_MA0	99	A1	A0	100	
101	[7] DDRB_CLK0	VDD9	102	DDRB_CLK1	103	[7] DDRB_CLK0#	CK0	104	DDRB_CLK1# [7] DDRB_CLK1 [7]
105	CK0#	CK1#	106		107	DDR_B_MA10	VDD11	108	DDR_B_BS1
109	DDR_B_BS0 [7]	A10/AP	110	DDR_B_RAS# [7] DDR_B_BS1 [7]	111	BA0	RAS#	112	
113	[7] DDR_B_WE#	VDD13	114	DDRB_SCS0#	115	[7] DDR_B_CAS#	WE#	116	DDRB_ODT0 [7] DDRB_SCS0# [7]
117	CAS#	ODT0	118		119	DDR_B_MA13	VDD15	120	DDRB_ODT1 [7] DDRB_ODT1
121	[7] DDRB_SCS1#	A13	122		123	S1#	ODT1	124	
125	VDD17	NC2	126	+VREF_CAB	127	NCTEST	VREF_CA	128	
129	DDR_B_D32	VSS27	130	DDR_B_D36	131	DDR_B_D33	DQ32	132	DDR_B_D37
133	DQ33	VSS29	134		135	DDR_B_DQS#4	VSS30	136	
137	DDR_B_DQS4	DQS#4	138		139	DQS4	DM4	140	DDR_B_D38
141	DDR_B_D34	VSS31	142	DDR_B_D39	143	DDR_B_D35	DQ34	144	
145	DQ35	VSS32	146	DDR_B_D44	147	DDR_B_D40	DQ38	148	DDR_B_D45
149	DDR_B_D41	DQ39	150		151	DQ40	VSS33	152	DDR_B_DQS#5
153	VSS34	DQ44	154	DDR_B_DQS5	155	DM5	DQS5	156	
157	DDR_B_D42	VSS36	158	DDR_B_D46	159	DDR_B_D43	VSS37	160	DDR_B_D47
161	DQ42	DQ43	162		163	DDR_B_D48	VSS39	164	DDR_B_D52
165	DDR_B_D49	DQ48	166	DDR_B_D53	167	DQ49	DQ52	168	
169	DDR_B_DQS#6	VSS41	170		171	DDR_B_DQS6	DQS#6	172	
173	DQS6	VSS43	174	DDR_B_D54	175	DDR_B_D50	VSS44	176	DDR_B_D55
177	DDR_B_D51	DQ54	178		179	DQ51	DQ55	180	DDR_B_D60
181	VSS46	DQ60	182	DDR_B_D61	183	DDR_B_D56	DQ61	184	
185	DQ56	VSS47	186	DDR_B_DQS#7	187	DDR_B_D57	DQS#7	188	DDR_B_DQS7
189	DM7	DQS7	190		191	VSS48	VSS50	192	DDR_B_D62
193	DDR_B_D58	DQ58	194	DDR_B_D63	195	DDR_B_D59	DQ59	196	
197	DQ62	VSS52	198		199	VSS51	DQ63	200	PM_SMBDATA
201	SA0	EVENT#	202	PM_SMBCLK	203	VDDSPD	SDA	204	PM_SMBDATA [10,13,40,5] PM_SMBCLK [10,13,40,5]
205	SA1	SCL				VTT1	VTT2		+0.75VS
	G1	G2	206						

SUYIN_600023HB204G208ZL
CONN@

+1.5V
R631 1K_0402_1%
+VREF_DQB
R632 1K_0402_1%
C2050 2.2U_0603_6.3V6K
C2051 0.1U_0402_16V4Z
Close to JDIMM2

+1.5V
R633 1K_0402_1%
+VREF_CAB
R634 1K_0402_1%
C2064 2.2U_0603_6.3V6K
C2065 0.1U_0402_16V4Z
Close to JDIMM2

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

+3VS
R635 10K_0402_5%
+0.75VS
@C2068 2.2U_0603_6.3V6K
C2069 0.1U_0402_16V4Z

Standard H:9.2mm

Layout Note:
Place near JDIMM2

+1.5V
C2052 @ 390U 2.5V M ESR10
C2053 10U_0805_6.3V6M
C2054 10U_0805_6.3V6M
C2055 10U_0805_6.3V6M

+1.5V
C2056 0.1U_0402_16V4Z
C2057 0.1U_0402_16V4Z
C2058 0.1U_0402_16V4Z
C2059 0.1U_0402_16V4Z
C2060 0.1U_0402_16V4Z
C2061 0.1U_0402_16V4Z
C2062 0.1U_0402_16V4Z
C2063 0.1U_0402_16V4Z

Layout Note: Place these Caps near +1.5V of JDIMM2

+0.75VS
C2066 4.7U_0603_6.3V6K
C2067 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2 Pin203 and 204

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

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Title: DDRIII-SODIMM B

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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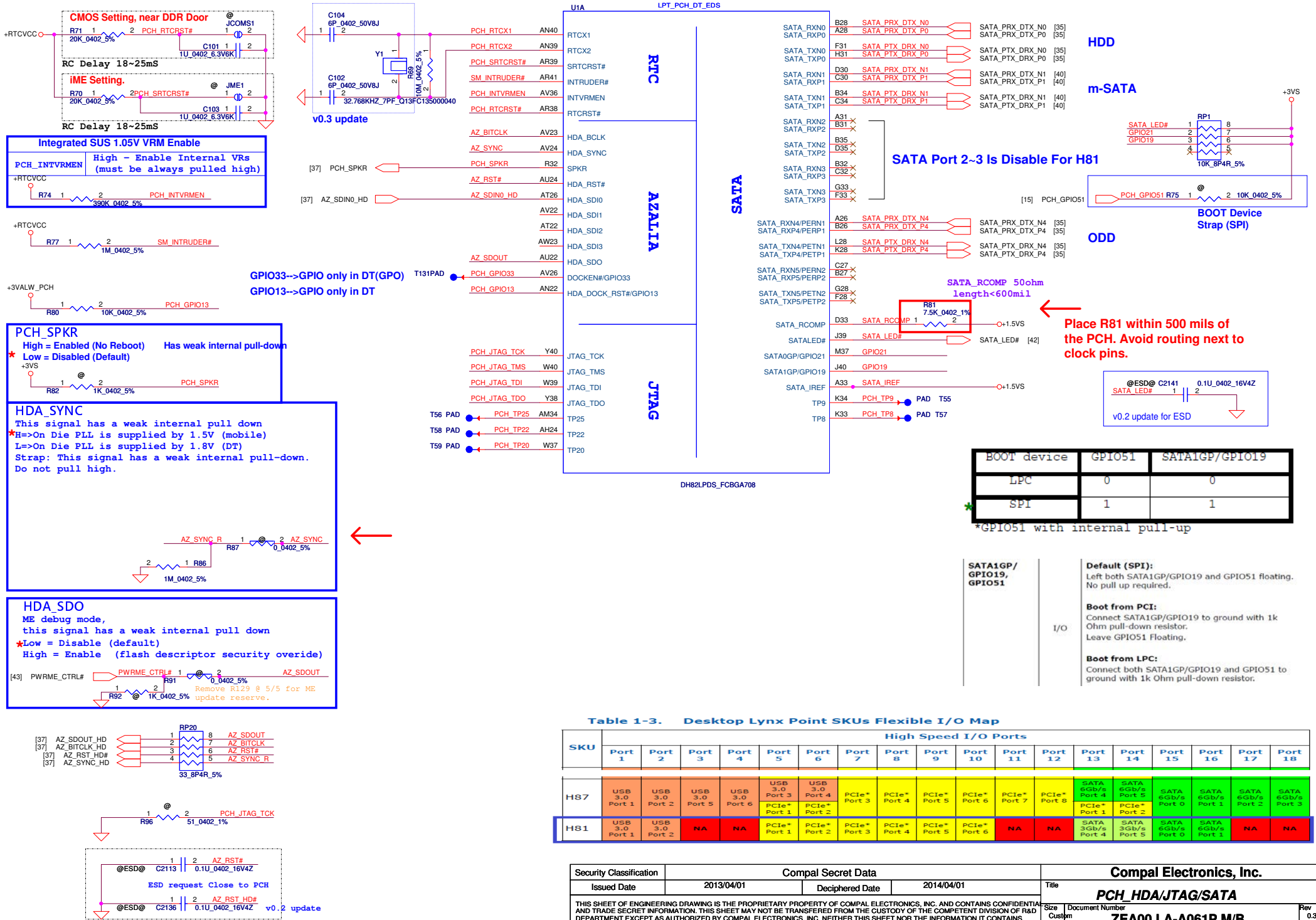

BOOT device	GPIO51	SATA1GP/GPIO19
LPC	0	0
SPI	1	1

Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	NA	NA	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	NA	NA

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Issued Date	2013/04/01	Deciphered Date 2014/04/01	Title: PCH_HDA/JTAG/SATA
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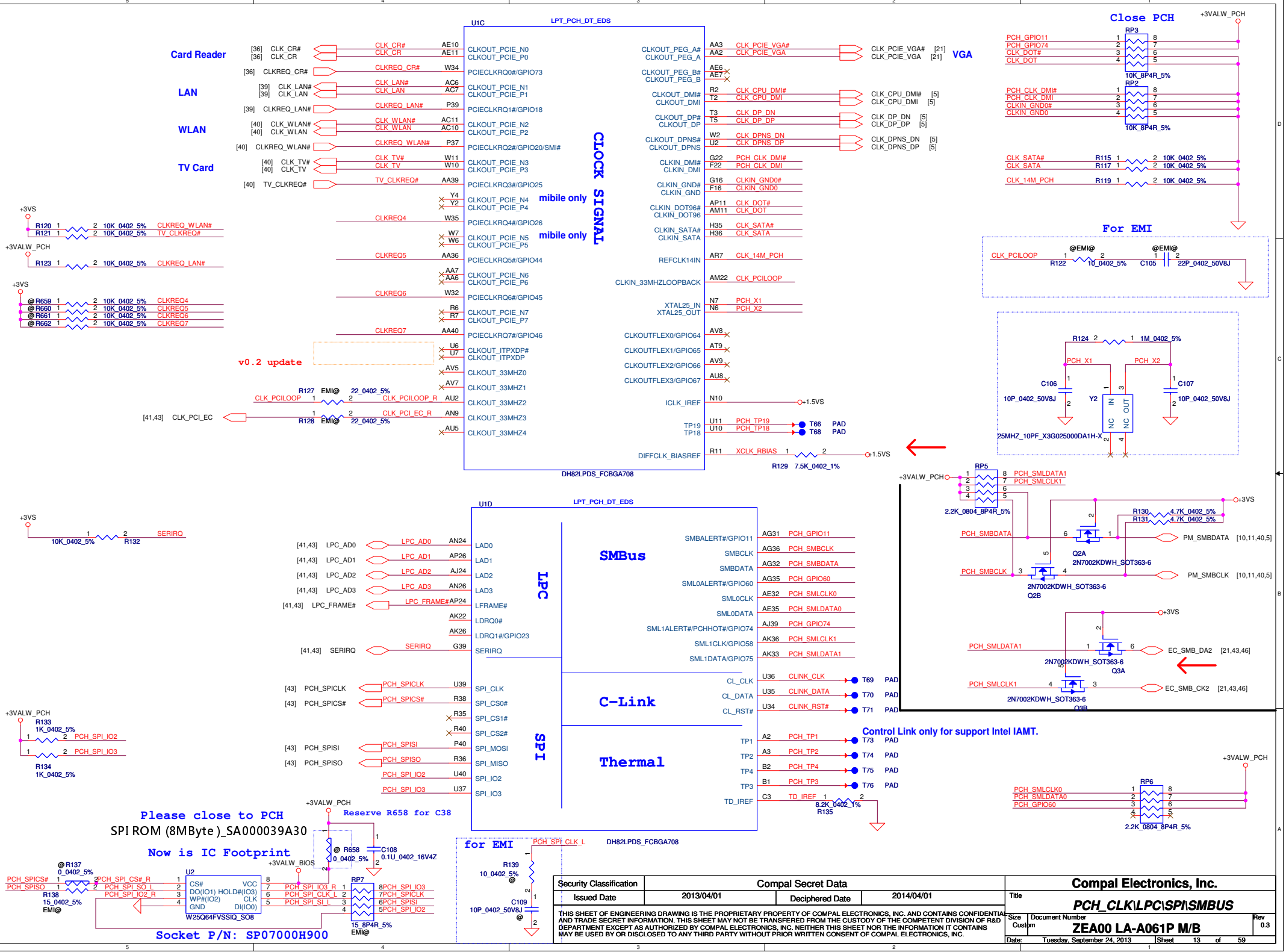
			Date: Tuesday, September 24, 2013; Sheet 12 of 59


Close PCH
For EMI
Card Reader
LAN
WLAN
TV Card
VGA
CLOCK SIGNAL
mibile only
v0.2 update
U1C
LPT_PCH_DT_EDS
DH82LPDS_FCBGA708
U1D
LPC
SPI
SMBus
C-Link
Thermal
Control Link only for support Intel IAMT.
Please close to PCH
SPI ROM (8MByte)_SA000039A30
Now is IC Footprint
Reserve R658 for C38
Socket P/N: SP07000H900
for EMI
Compal Electronics, Inc.
PCH_CLK\LPC\SPI\SMBUS
ZEA00 LA-A061P M/B
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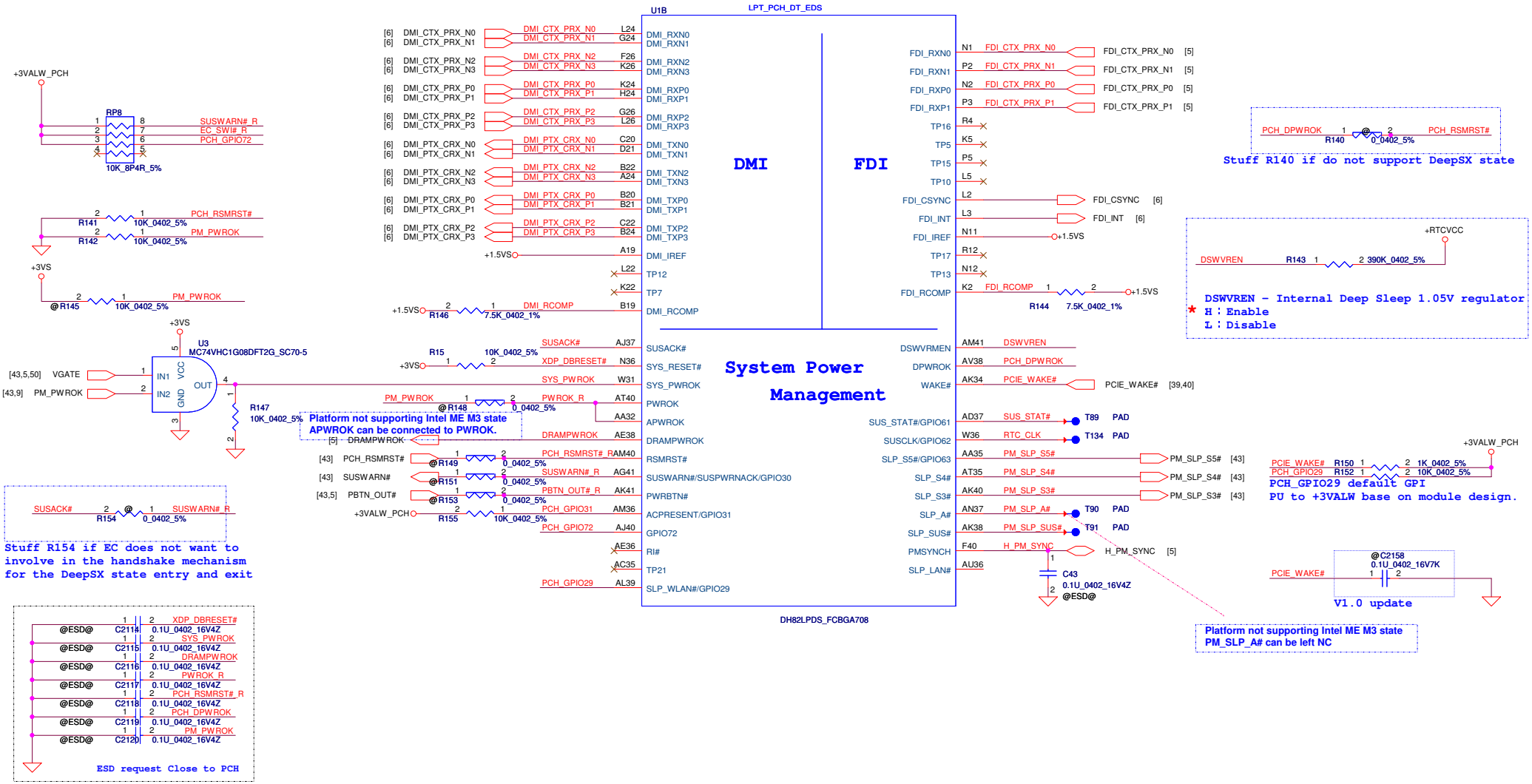

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Title	PCH_DMI/FDI/PM		
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PCI PU resistor

RP9
1 8 PCI_PIRQD#
2 7 PCI_PIRQB#
3 6 PCH_GPIO5
4 5 PCI_PIRQC#
8.2K_8P4R_5%

R159 1 2 8.2K_0402_5% PCH_GPIO50
R160 1 2 8.2K_0402_5% PCH_GPIO52
R161 1 2 8.2K_0402_5% PCH_GPIO54

RP10
1 8 PCH_GPIO4
2 7 PCI_PIRQA#
3 6 PCH_GPIO3
4 5 PCH_GPIO2
8.2K_8P4R_5%

1 CRT@ 2 PCH_CRT_CLK
R162 2.2K_0402_5%
1 CRT@ 2 PCH_CRT_DATA
R163 2.2K_0402_5%

RP11
1 8 PCH_CRT_B
2 7 PCH_CRT_G
3 6 PCH_CRT_R
4 5
150_0804_8P4R_1% CRT@

Close to PCH <250mils

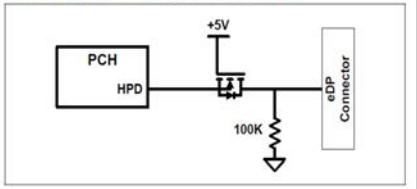
2 1 PCH_GPIO53
@R157 10K_0402_5%
2 1 PCH_GPIO55
@R158 10K_0402_5%

Internal pull high
Strap defalut high
GPIO53 DMI AC mode if Low
GPIO55 A16 SWAP OVERRIDE if Low

NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

RP17
PCH_DPD_CLK 1 8
PCH_DPD_DAT 2 7
PCH_HDMIOUT_CLK 3 6
PCH_HDMIOUT_DATA 4 5
+3VS
2.2K_0804_8P4R_5%

Figure 9-3. Processor Graphics eDP* HPD Signal off of Digital Port D



+5VS
Q57 BSS138LT1G_SOT23-3
DDPD_HPD 3 1 PCH_DDPD_HPD [29]
R605 @ 0_0402_5%
R606 100K_0402_5%

U1E LPT_PCH_DT_EDS

Data Need longer than CLK 1 inch

HDMI OUT (To Conn.)

eDP (LVDS Converter)

Seperate U10, U57 location

CRT
[41] PCH_CRT_B PCH_CRT_B AC3 VGA_BLUE
[41] PCH_CRT_G PCH_CRT_G AE2 VGA_GREEN
[41] PCH_CRT_R PCH_CRT_R AC2 VGA_RED
[41] PCH_CRT_CLK PCH_CRT_CLK AL2 VGA_DDC_CLK
[41] PCH_CRT_DATA PCH_CRT_DATA AL3 VGA_DDC_DATA
[41] PCH_CRT_HSYNC PCH_CRT_HSYNC AH3 VGA_HSYNC
[41] PCH_CRT_VSYNC PCH_CRT_VSYNC AH2 VGA_VSYNC
Disable use 1K on mobile
1 2 CRT_IREF AF5 DAC_IREF
R165 649_0402_1%
AG4 VGA_IRTN
CRT_IREF Close to PCH <500mils

LVDS
To Converter [29] PCH_EDP_PWM PCH_EDP_PWM AP2 EDP_BKLTCTL
[29] PCH_EDP_BLEN PCH_EDP_BLEN AT2 EDP_BKLTEN
v0.2 update T133 PAD PCH_EDP_VDDEN AP1 EDP_VDDEN

DISPLAY

PCI
PCI_PIRQA# AU29 PIRQA#
PCI_PIRQB# AU27 PIRQB#
PCI_PIRQC# AW28 PIRQC#
PCI_PIRQD# AV27 PIRQD#
[21,43] DGPU_HOLD_RST# 1 2 @R167 0_0402_5% PCH_GPIO50 AH26 GPIO50
PCH_GPIO52 AJ26 GPIO52
[23,43] DGPU_PWR_EN 1 2 @R170 0_0402_5% PCH_GPIO54 AW33 GPIO54
[12] PCH_GPIO51 PCH_GPIO51 AU31 GPIO51
PCH_GPIO53 AV31 GPIO53
PCH_GPIO55 R30 GPIO55

DDPB_CTRLCLK AM1 PCH_HDMIOUT_CLK PCH_HDMIOUT_CLK [30]
DDPB_CTRLDATA AJ5 PCH_HDMIOUT_DATA PCH_HDMIOUT_DATA [30]
DDPC_CTRLCLK AN3 PCH_HDMI_CLK PAD T92
DDPC_CTRLDATA AM2 PCH_HDMI_DATA PAD T93
DDPD_CTRLCLK AN4 PCH_DPD_CLK
DDPD_CTRLDATA AN2 PCH_DPD_DAT

DDPB_AUXN AK6 DDPB_AUXN PAD T96
DDPC_AUXN AG7 DDPC_AUXN PAD T97
DDPD_AUXN AG11 PCH_DDPD_AUXN C112 1 2 0.1U_0402_16V4Z PCH_DDPD_AUXN_C [29] LVDS Converter
DDPB_AUXP AK8 DDPB_AUXP PAD T98
DDPC_AUXP AG6 DDPC_AUXP PAD T99
DDPD_AUXP AG10 PCH_DDPD_AUXP C113 1 2 0.1U_0402_16V4Z PCH_DDPD_AUXP_C [29] LVDS Converter
DDPB_HPD AJ2 PCH_HDMIOUT_HPD PCH_HDMIOUT_HPD [30] HDMI OUT
DDPC_HPD AH5 DPD_HPD PAD T100
DDPD_HPD AJ4 DDPD_HPD LVDS Converter

PIRQE#/GPIO2 AR30 PCH_GPIO2
PIRQF#/GPIO3 AV29 PCH_GPIO3
PIRQG#/GPIO4 AV28 PCH_GPIO4
PIRQH#/GPIO5 AT27 PCH_GPIO5
PME# AA31 PCI_PME# PADT101
PLTRST# AA37 PCH_PLT_RST#
C2121 0.1U_0402_16V4Z @ESD@

DH82LPDS_FCBGA708

PCH_DDPD_AUXN_C R172 1 @ 2 100K_0402_5% +3VS
PCH_DDPD_AUXP_C R173 1 @ 2 100K_0402_5%
CRB Reserve PU/PL

@R164 0_0402_5%
+3VS
C111 0.1U_0402_16V4Z
U4 MC74VHC1G08DFT2G_SC70-5
PCH_PLT_RST# IN1 IN2 VCC GND OUT PLT_RST# PLT_RST# [21,41,43]
For GPU/TPM/EC
R166 100K_0402_5%

R677 0_0402_5% +3VALW_PCH
@R678 0_0402_5% +3VS
v0.3 update for wake from WLAN(BCM43142)
@ C2029 0.1U_0402_16V4Z
For Card reader/ LAN/WLAN/TV
U5 MC74VHC1G08DFT2G_SC70-5
PLT_A_RST# [36,39,40]
R171 100K_0402_5%
C2135 ESD@ 0.1U_0402_16V4Z
v0.2 update

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Title: PCH_CRT/DDC

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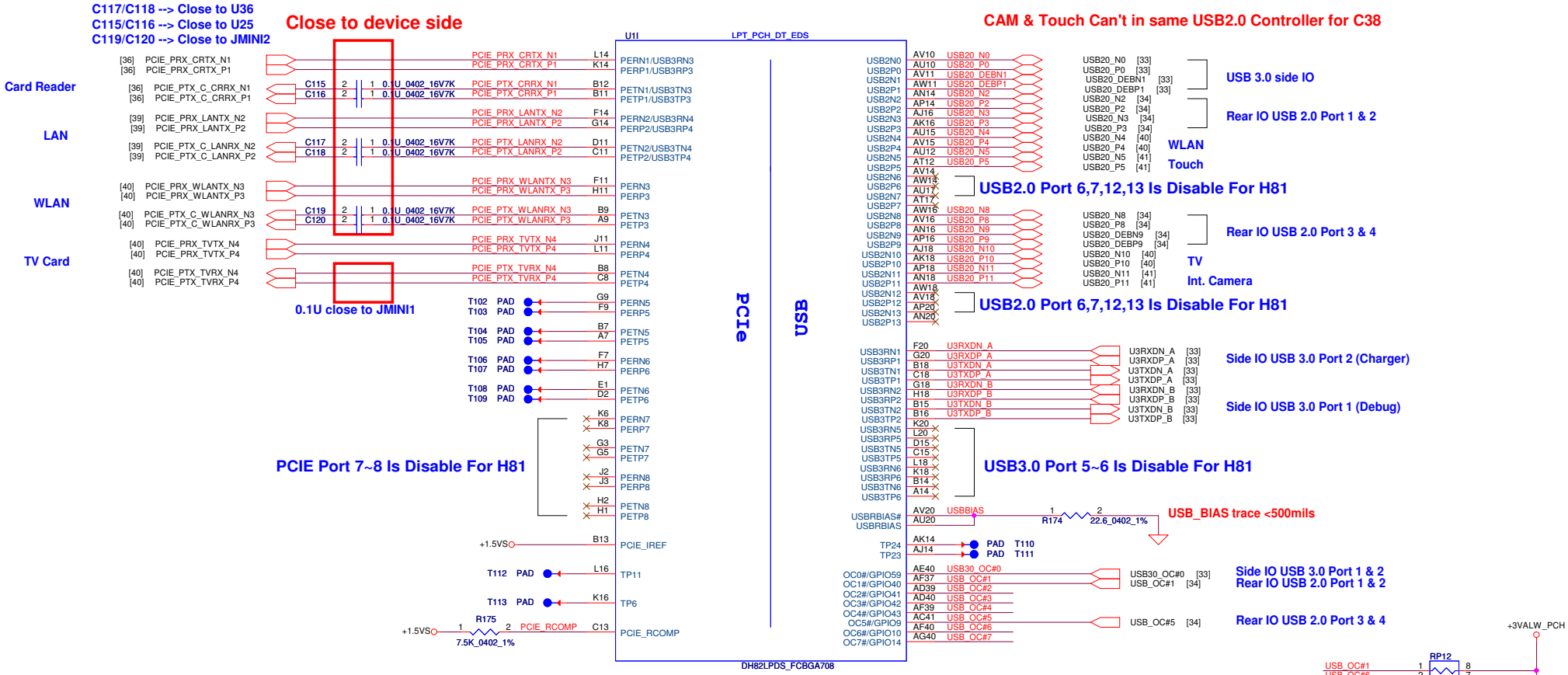
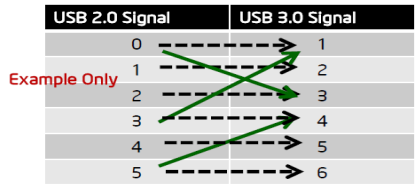


- Port mapping restrictions removed
  - USB 3.0 signals can now be paired with any of USB2.0 signal 0-13
  - Custom mapping through ACPI table/BIOS
  - Default mapping USB 3.0 1-6 to USB 2.0 0-5 ports



- Better USB 2.0 performance than EHCI
- Windows* 8 is expected to include a native inbox xHCI driver

Table 14-4. Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Title: PCH_PCI-E/USB

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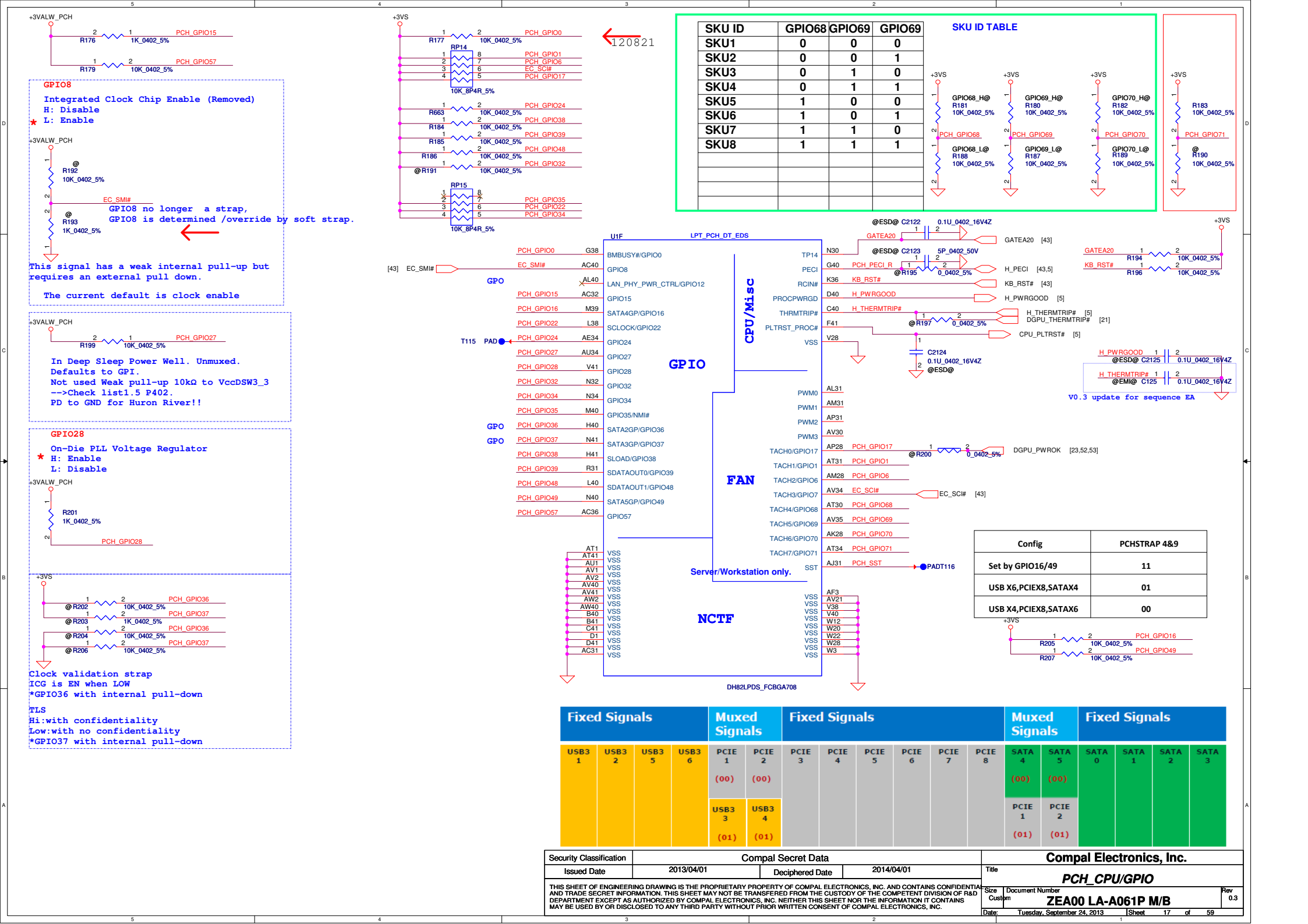

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Title: PCH_CPU/GPIO

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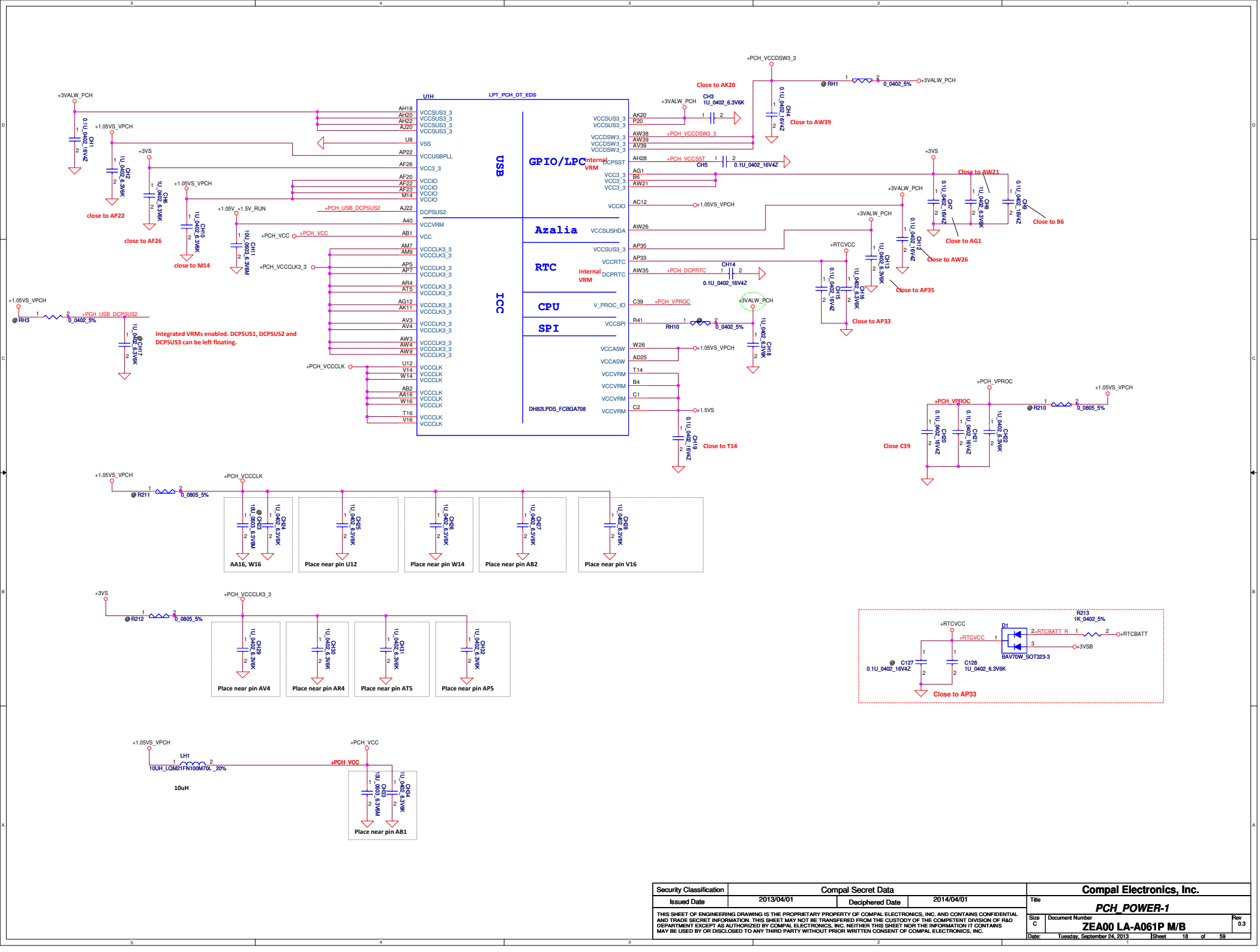

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Title: ***PCH_POWER-1***

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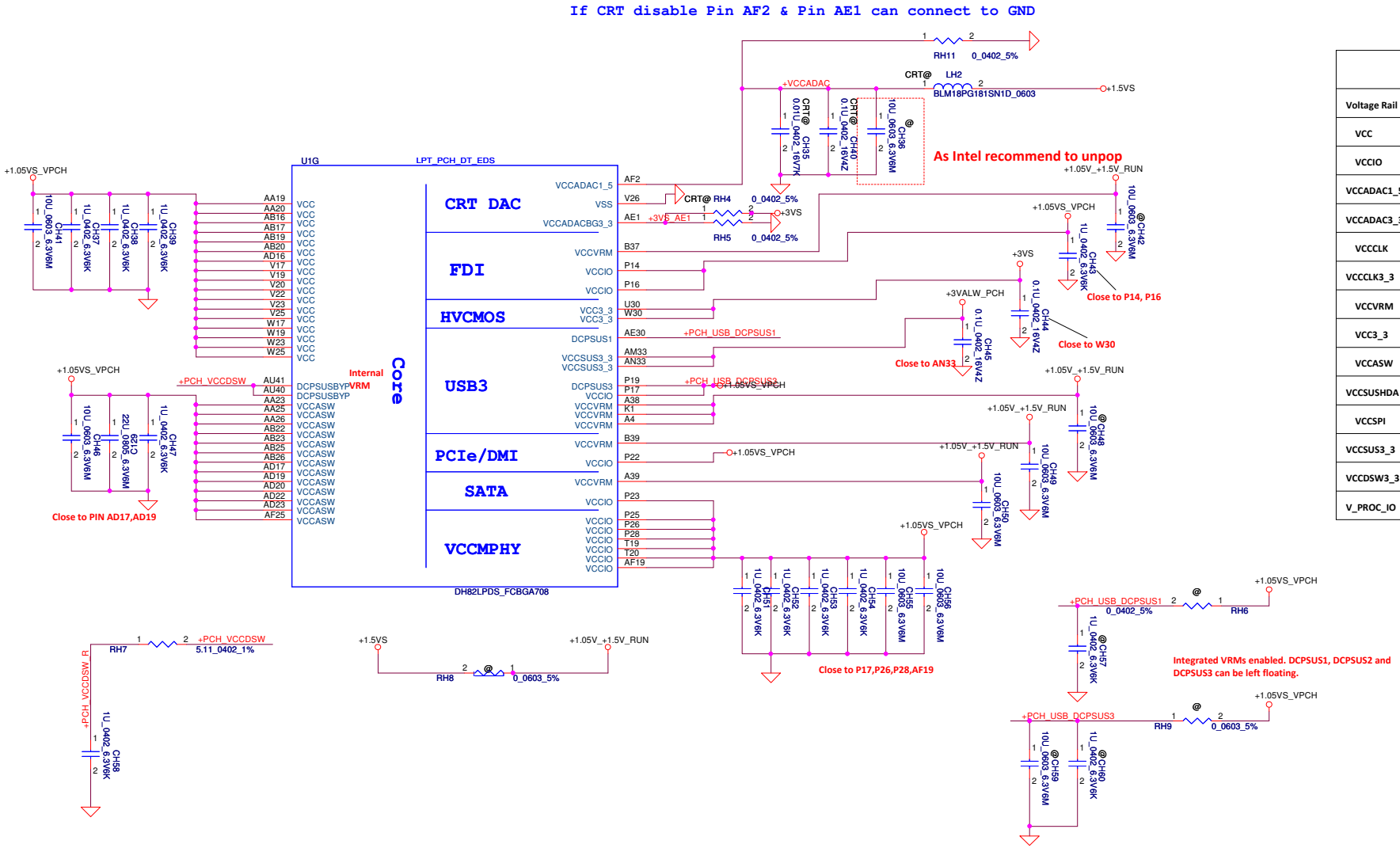

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: PCH_POWER-2

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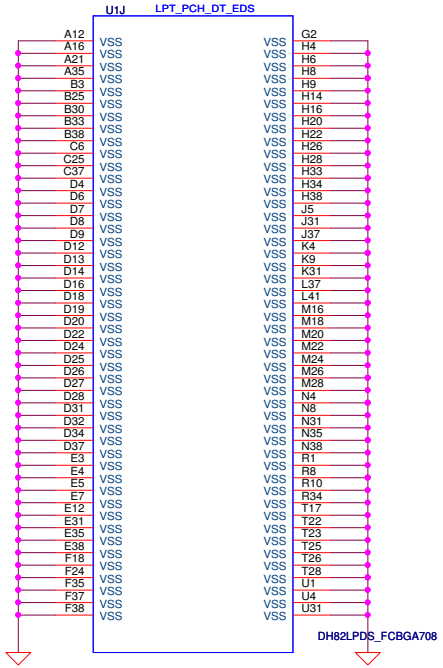

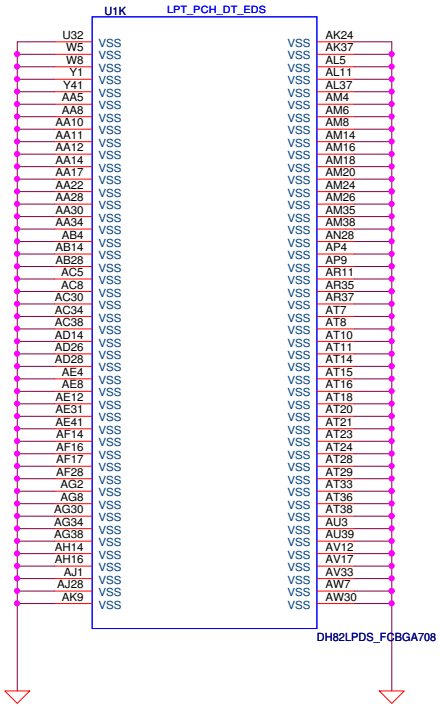

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Compal Electronics, Inc.

Title: ***PCH_GND***

Size	Document Number	Rev
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[6] PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
[6] PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]
[6] PCIE_GTX_C_CRX_P[0..15] PCIE_GTX_C_CRX_P[0..15]
[6] PCIE_GTX_C_CRX_N[0..15] PCIE_GTX_C_CRX_N[0..15]

U6A DIS@ Part 1 of 7

PCIE_CTX_C_GRX_P0 AN12 PEX_RX0
PCIE_CTX_C_GRX_N0 AM12 PEX_RX0_N
PCIE_CTX_C_GRX_P1 AN14 PEX_RX1
PCIE_CTX_C_GRX_N1 AM14 PEX_RX1_N
PCIE_CTX_C_GRX_P2 AP14 PEX_RX2
PCIE_CTX_C_GRX_N2 AP15 PEX_RX2_N
PCIE_CTX_C_GRX_P3 AN15 PEX_RX3
PCIE_CTX_C_GRX_N3 AM15 PEX_RX3_N
PCIE_CTX_C_GRX_P4 AN17 PEX_RX4
PCIE_CTX_C_GRX_N4 AM17 PEX_RX4_N
PCIE_CTX_C_GRX_P5 AP17 PEX_RX5
PCIE_CTX_C_GRX_N5 AP18 PEX_RX5_N
PCIE_CTX_C_GRX_P6 AN18 PEX_RX6
PCIE_CTX_C_GRX_N6 AM18 PEX_RX6_N
PCIE_CTX_C_GRX_P7 AN20 PEX_RX7
PCIE_CTX_C_GRX_N7 AM20 PEX_RX7_N
PCIE_CTX_C_GRX_P8 AP20 PEX_RX8
PCIE_CTX_C_GRX_N8 AP21 PEX_RX8_N
PCIE_CTX_C_GRX_P9 AN21 PEX_RX9
PCIE_CTX_C_GRX_N9 AM21 PEX_RX9_N
PCIE_CTX_C_GRX_P10 AN23 PEX_RX10
PCIE_CTX_C_GRX_N10 AM23 PEX_RX10_N
PCIE_CTX_C_GRX_P11 AP23 PEX_RX11
PCIE_CTX_C_GRX_N11 AP24 PEX_RX11_N
PCIE_CTX_C_GRX_P12 AN24 PEX_RX12
PCIE_CTX_C_GRX_N12 AM24 PEX_RX12_N
PCIE_CTX_C_GRX_P13 AN26 PEX_RX13
PCIE_CTX_C_GRX_N13 AM26 PEX_RX13_N
PCIE_CTX_C_GRX_P14 AP26 PEX_RX14
PCIE_CTX_C_GRX_N14 AP27 PEX_RX14_N
PCIE_CTX_C_GRX_P15 AN27 PEX_RX15
PCIE_CTX_C_GRX_N15 AM27 PEX_RX15_N

Reserve for x16 GPU

PCIE_GTX_C_CRX_P0 DIS@ C131 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P0 AK14 PEX_TX0
PCIE_GTX_C_CRX_N0 DIS@ C132 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N0 AJ14 PEX_TX0_N
PCIE_GTX_C_CRX_P1 DIS@ C133 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P1 AH14 PEX_TX1
PCIE_GTX_C_CRX_N1 DIS@ C134 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N1 AG14 PEX_TX1_N
PCIE_GTX_C_CRX_P2 DIS@ C135 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P2 AK15 PEX_TX2
PCIE_GTX_C_CRX_N2 DIS@ C136 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N2 AJ15 PEX_TX2_N
PCIE_GTX_C_CRX_P3 DIS@ C137 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P3 AL16 PEX_TX3
PCIE_GTX_C_CRX_N3 DIS@ C138 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N3 AK16 PEX_TX3_N
PCIE_GTX_C_CRX_P4 DIS@ C139 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P4 AK17 PEX_TX4
PCIE_GTX_C_CRX_N4 DIS@ C140 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N4 AJ17 PEX_TX4_N
PCIE_GTX_C_CRX_P5 DIS@ C141 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P5 AH17 PEX_TX5
PCIE_GTX_C_CRX_N5 DIS@ C142 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N5 AG17 PEX_TX5_N
PCIE_GTX_C_CRX_P6 DIS@ C143 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P6 AK18 PEX_TX6
PCIE_GTX_C_CRX_N6 DIS@ C144 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N6 AJ18 PEX_TX6_N
PCIE_GTX_C_CRX_P7 DIS@ C145 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P7 AL19 PEX_TX7
PCIE_GTX_C_CRX_N7 DIS@ C146 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N7 AK19 PEX_TX7_N
PCIE_GTX_C_CRX_P8 @ C2096 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P8 AK20 PEX_TX8
PCIE_GTX_C_CRX_N8 @ C2097 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N8 AJ20 PEX_TX8_N
PCIE_GTX_C_CRX_P9 @ C2098 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P9 AH20 PEX_TX9
PCIE_GTX_C_CRX_N9 @ C2099 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N9 AG20 PEX_TX9_N
PCIE_GTX_C_CRX_P10 @ C2100 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P10 AK21 PEX_TX10
PCIE_GTX_C_CRX_N10 @ C2101 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N10 AJ21 PEX_TX10_N
PCIE_GTX_C_CRX_P11 @ C2102 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P11 AL22 PEX_TX11
PCIE_GTX_C_CRX_N11 @ C2103 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N11 AK22 PEX_TX11_N
PCIE_GTX_C_CRX_P12 @ C2104 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P12 AK23 PEX_TX12
PCIE_GTX_C_CRX_N12 @ C2105 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N12 AJ23 PEX_TX12_N
PCIE_GTX_C_CRX_P13 @ C2106 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P13 AH23 PEX_TX13
PCIE_GTX_C_CRX_N13 @ C2107 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N13 AG23 PEX_TX13_N
PCIE_GTX_C_CRX_P14 @ C2108 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P14 AK24 PEX_TX14
PCIE_GTX_C_CRX_N14 @ C2109 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N14 AJ24 PEX_TX14_N
PCIE_GTX_C_CRX_P15 @ C2110 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_P15 AL25 PEX_TX15
PCIE_GTX_C_CRX_N15 @ C2111 1 2 0.22U_0402_16V7K PCIE_GTX_C_CRX_N15 AK25 PEX_TX15_N

Reserve for x16 GPU

AJ11 PEX_WAKE_N
AL13 PEX_REFCLK
AK13 PEX_REFCLK_N
AK12 PEX_CLKREQ_N
AJ26 PEX_TSTCLK_OUT
AK26 PEX_TSTCLK_OUT_N
AJ12 PEX_RST_N
AP29 PEX_TERMP

PCI EXPRESS

GPIO

P6 GPU_VID4 — T117 T118 0327 Update
M3 GPU_VID3
L6
P5 VGA_GPIO3 — T129
P7
L7 GPU_VID1 — T119 T120 0327 Update
M7 GPU_VID2
N8
M1 OVERT#
M2 EVENT#_R
L1
M5 GPU_PWM_VID — GPU_PWM_VID [52] 0327 Update
N3 VGA_GPIO12 — NVVDD_PSI [52]
M4 NVVDD_PSI
N4
P2
R8 VGA_GPIO16 — T130 0327 Update
M6
R1
P3 0327 Update
P4
P1

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21

DACs

AK9 DACA_RED
AL10 DACA_GREEN
AL9 DACA_BLUE
AM9 DACA_HSYNC
AN9 DACA_VSYNC
AG10 DACA_VDD — +DACA_VDD 2 1 DIS@ R224 10K_0402_5%
AP9 DACA_VREF
AP8 DACA_RSET

I2C

R4 VGA_CRT_CLK — I2CA_SCL
R5 VGA_CRT_DATA — I2CA_SDA
R7 I2CB_SCL — I2CB_SCL
R6 I2CB_SDA — I2CB_SDA
R2 VGA_EDID_CLK — I2CC_SCL
R3 VGA_EDID_DATA — I2CC_SDA
T4 VGA_SMB_CK2 — I2CS_SCL
T3 VGA_SMB_DA2 — I2CS_SDA

CLK

AD8 PLLVDD
AE8 SP_PLLVDD
AD7 VID_PLLVDD
H3 XTALIN — XTAL_IN
H2 XTAL_OUT
J4 XTALOUT — XTAL_OUTBUFF
H1 XTALSSIN — XTAL_SSIN

N14M-GE2-B-AIO-A2

+3VS_VGA R214 1 2 10K_0402_5% C130 2 1 0.1U_0402_10V6K
DGPU_THERMTRIP# [17]
Q4B DMN66D0LDW-7 2N_SOT363-6 DIS@
Q4A DMN66D0LDW-7 2N_SOT363-6 DIS@

Table 102. GB2-64 and GB4-128 GPIO Description

GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3DVision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	CPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

+3VS_VGA
EVENT# R R217 DIS@ 10K_0402_5%
VGA_EDID_CLK R218 DIS@ 2.2K_0402_5%
VGA_EDID_DATA R219 DIS@ 2.2K_0402_5%
VGA_CRT_DATA R220 DIS@ 2.2K_0402_5%
VGA_CRT_CLK R221 DIS@ 2.2K_0402_5%
I2CB_SCL R222 DIS@ 2.2K_0402_5%
I2CB_SDA R223 DIS@ 2.2K_0402_5%
OVERT# R225 DIS@ 10K_0402_5%
VGA_GPIO12 R226 10K_0402_5%

0327 Update

+1.05VS_VGA
30 ohms @100MHz (ESR=0.05)
DIS@ L1 SBY100505T-300Y-N_0402
60mA +PLLVDD R227 @ 0_0402_5%
45mA +SP_PLLVDD
45mA
0.1U_0402_10V6K C163 22U_0805_6.3V6M C164 DIS@
Near GPU
Under GPU

PLT_RST# R228 @ 0_0402_5% +3VS_VGA
R229 @ 10K_0402_5%
[15,41,43] PLT_RST#
[15,43] DGPU_HOLD_RST#
U7 MC74VHC1G08DFT2G SC70 5P
R231 100K_0402_5%
v0.2 update
v0.2 update

[13] CLK_PCIE_VGA
[13] CLK_PCIE_VGA#
CLK_REQ_GPU#
Differential signal
R230 @ 200_0402_1%
PLT_RST_VGA#
PEX_TERMP
R234 2.49K_0402_1% DIS@
R232 10K_0402_5% DIS@
R233 10K_0402_5% DIS@

Under GPU(below 150mils)
Put C169 close to U65.AE8
+1.05VS_VGA
DIS@ L2 BLM18PG330SN1D_0603
180ohms (ESR=0.2) Bead
150mA
+SP_PLLVDD
22U_0805_6.3V6M C165 4.7U_0402_6.3V6M C166 0.1U_0402_10V6K C167 0.1U_0402_10V6K C168 0.1U_0402_10V6K C169 DIS@

+3VS_VGA
DIS@ R236 2.2K_0402_5%
DIS@ R237 2.2K_0402_5%
VGA_SMB_CK2
DIS@ Q5B
2N7002DW-T/R7_SOT363-6
EC_SMB_CK2 [13,43,46]
VGA_SMB_DA2
DIS@ Q5A
2N7002DW-T/R7_SOT363-6
EC_SMB_DA2 [13,43,46]

+3VS_VGA
@ R238 10K_0402_5%
CLK_REQ_GPU#
@ R239 10K_0402_5%
Reserve pull-up and down.
Don't have to install component for default, NV reply on 5/4. when system no support CLKREQ

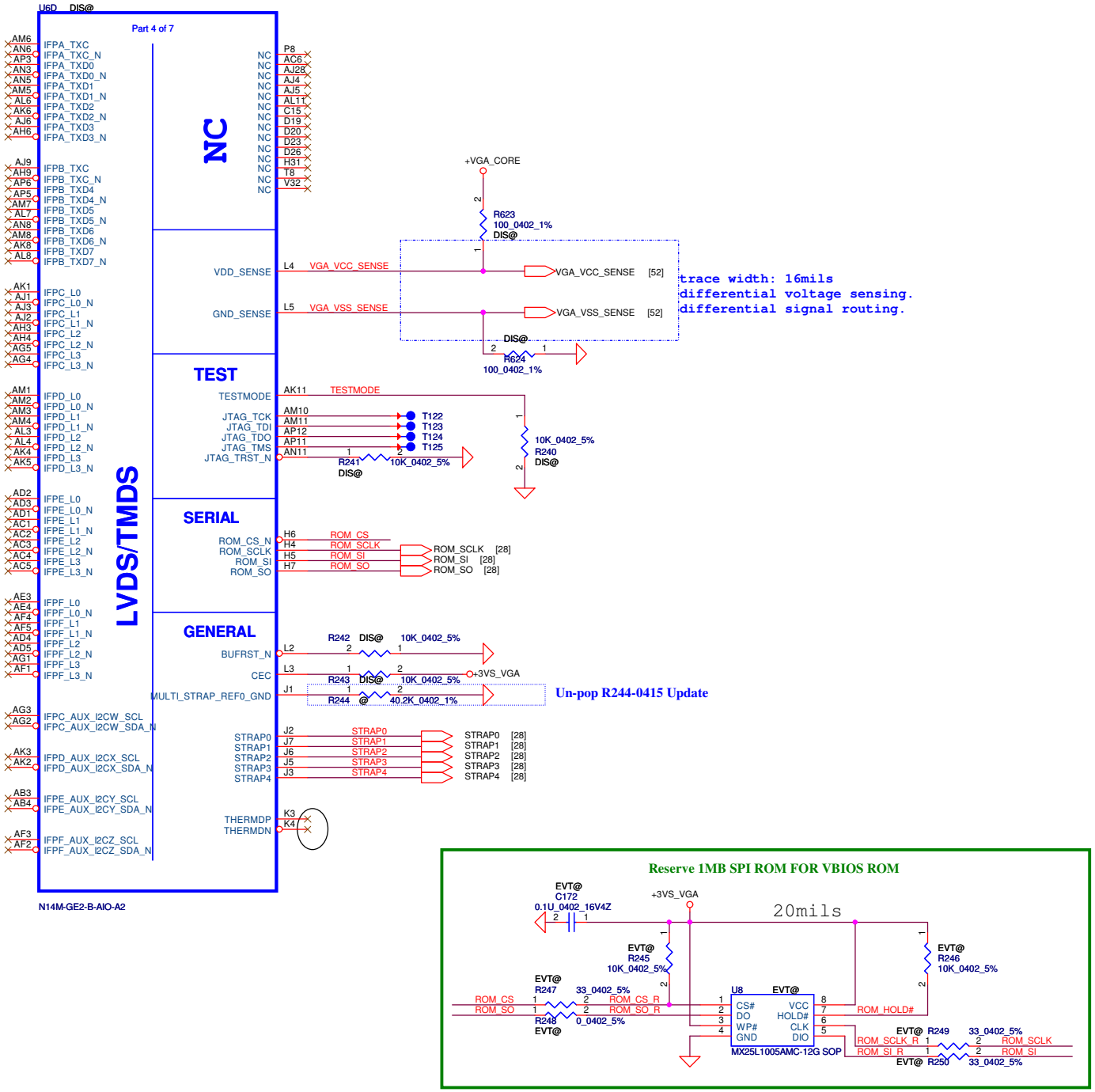
DIS@ R235 10M_0402_5%
DIS@ Y3 NC OSC XTALIN XTAL_OUT 27MHZ 10PF +-20PPM X3G027000DA1H
DIS@ C170 10P_0402_50V8J
DIS@ C171 10P_0402_50V8J
v0.3 update

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.
Title: N14M-GE2-PCIE/DAC/GPIO
Size: Document Number: ZEA00 LA-A061P M/B Rev: 0.3
Date: Tuesday, September 24, 2013 Sheet 21 of 59

Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI



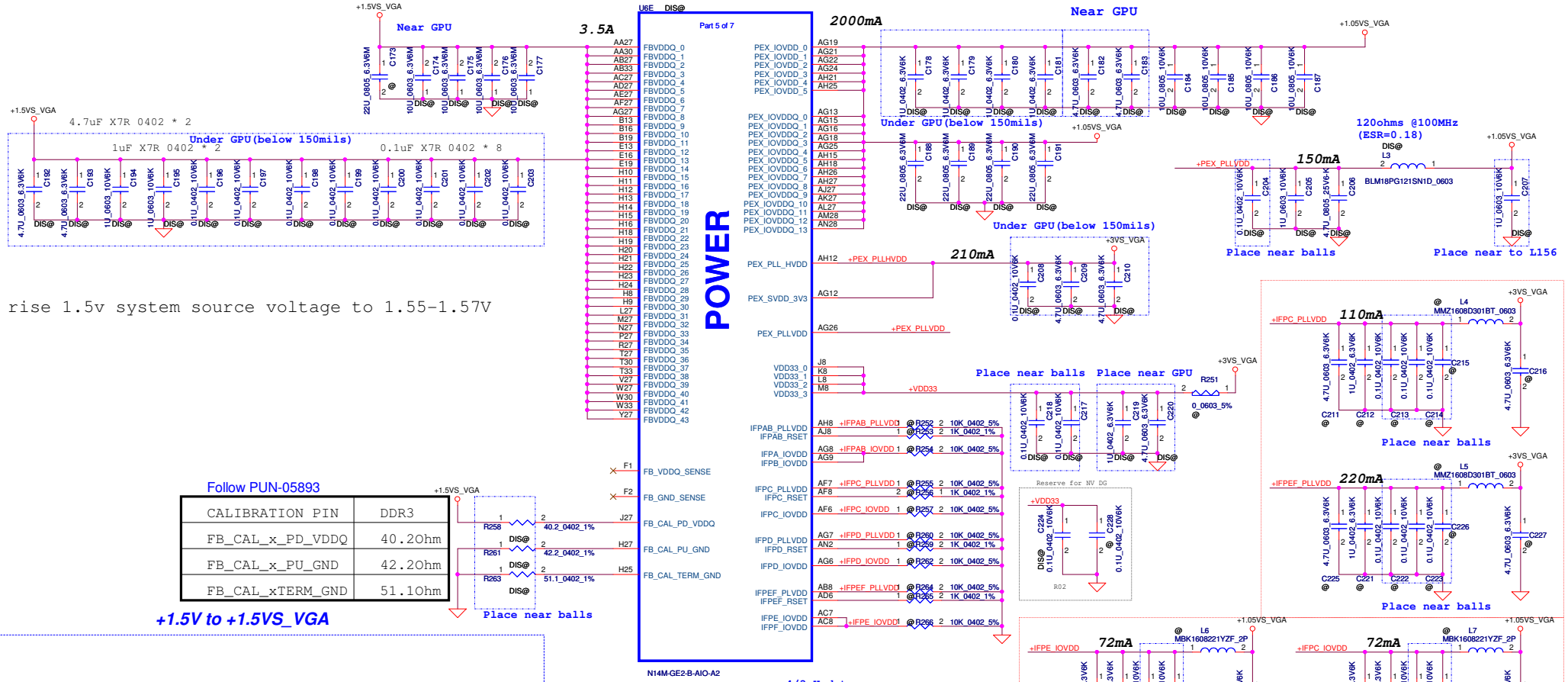
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-LVDS/HDMI/DP/THM

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 22 of 59



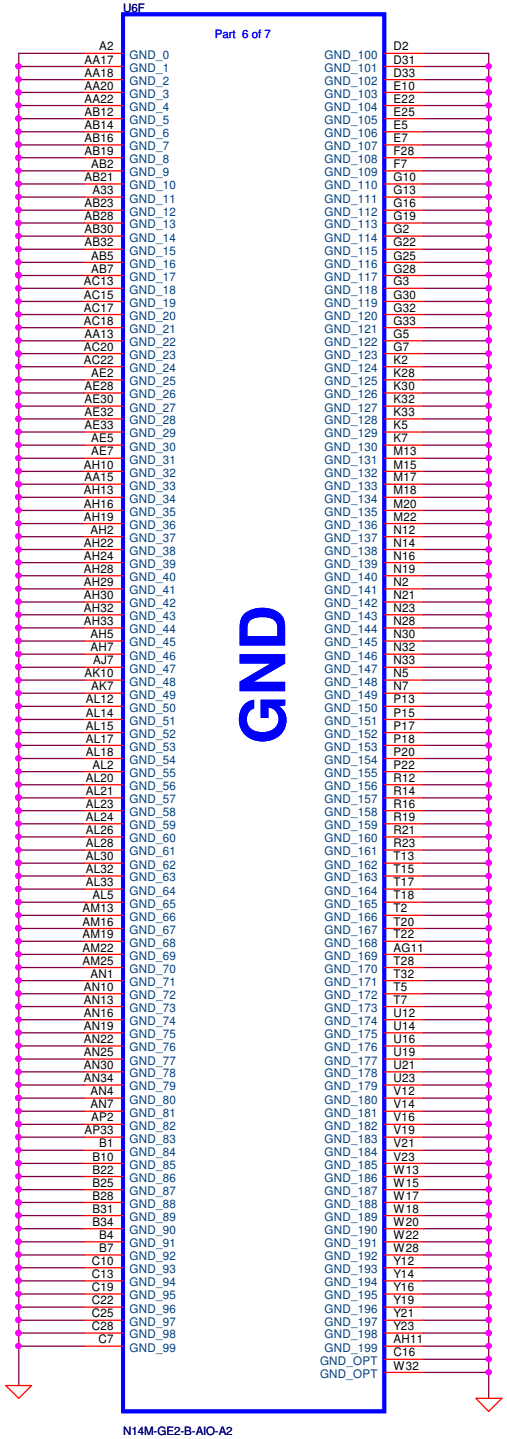
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

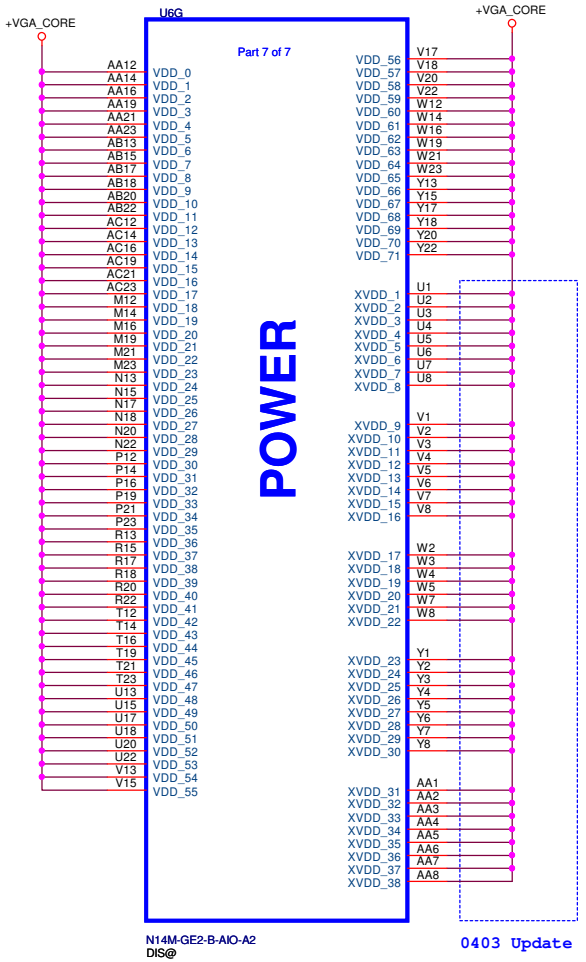
Compal Electronics, Inc.

Title: N14M-GE2-POWER

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 23 of 59





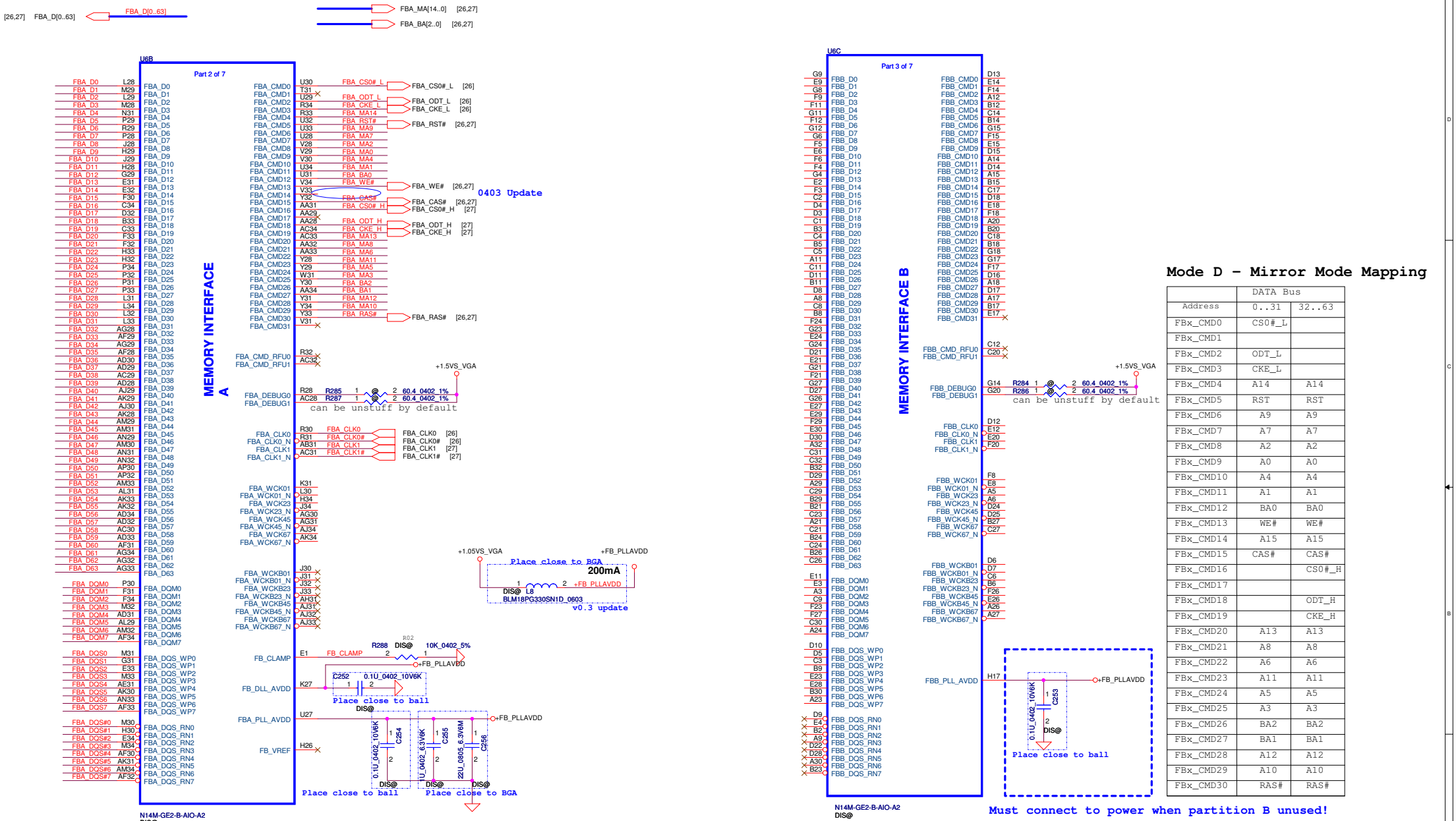
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-VGA CORE, GND

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 24 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-MEM Interface

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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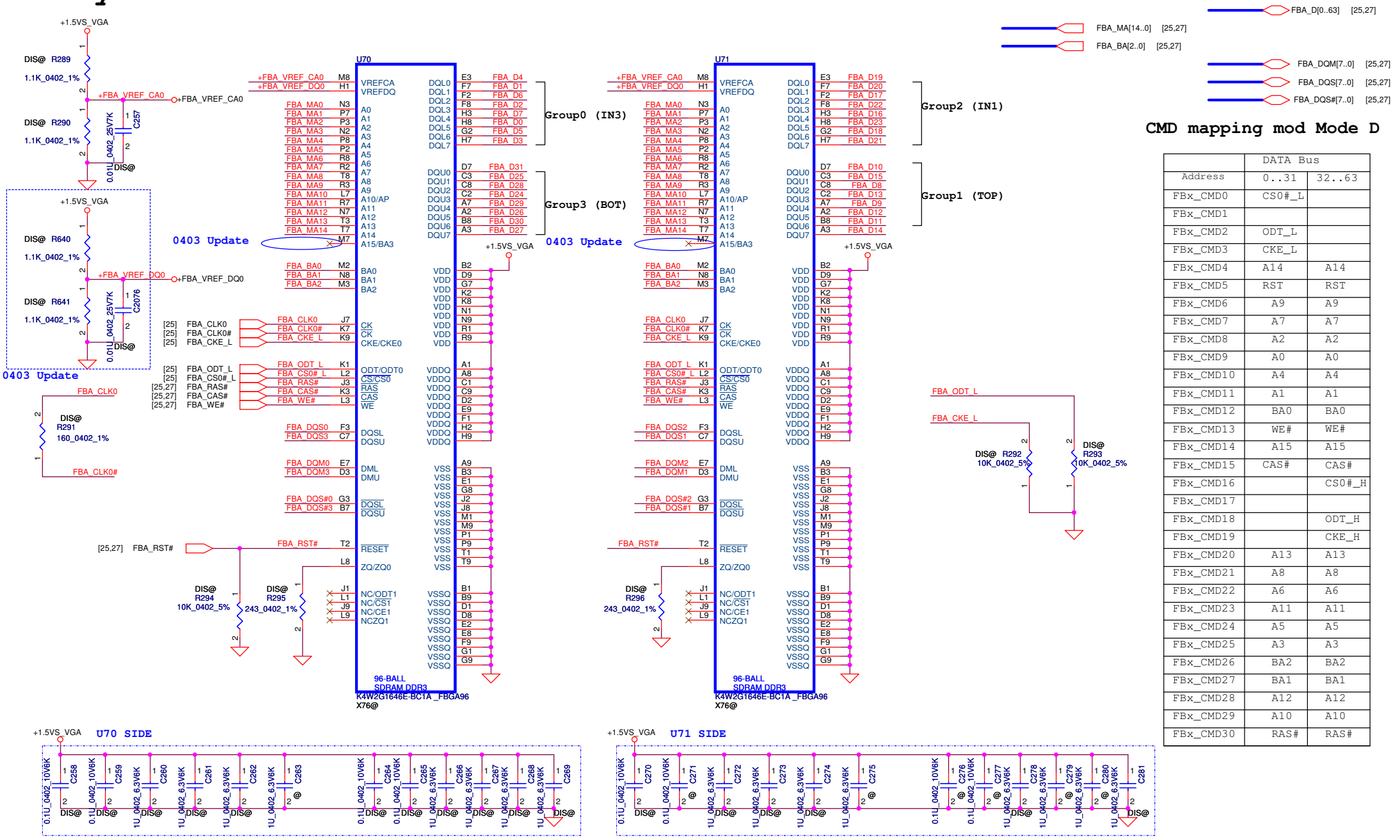
Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	N14M-GE2-VRAM A Lower		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
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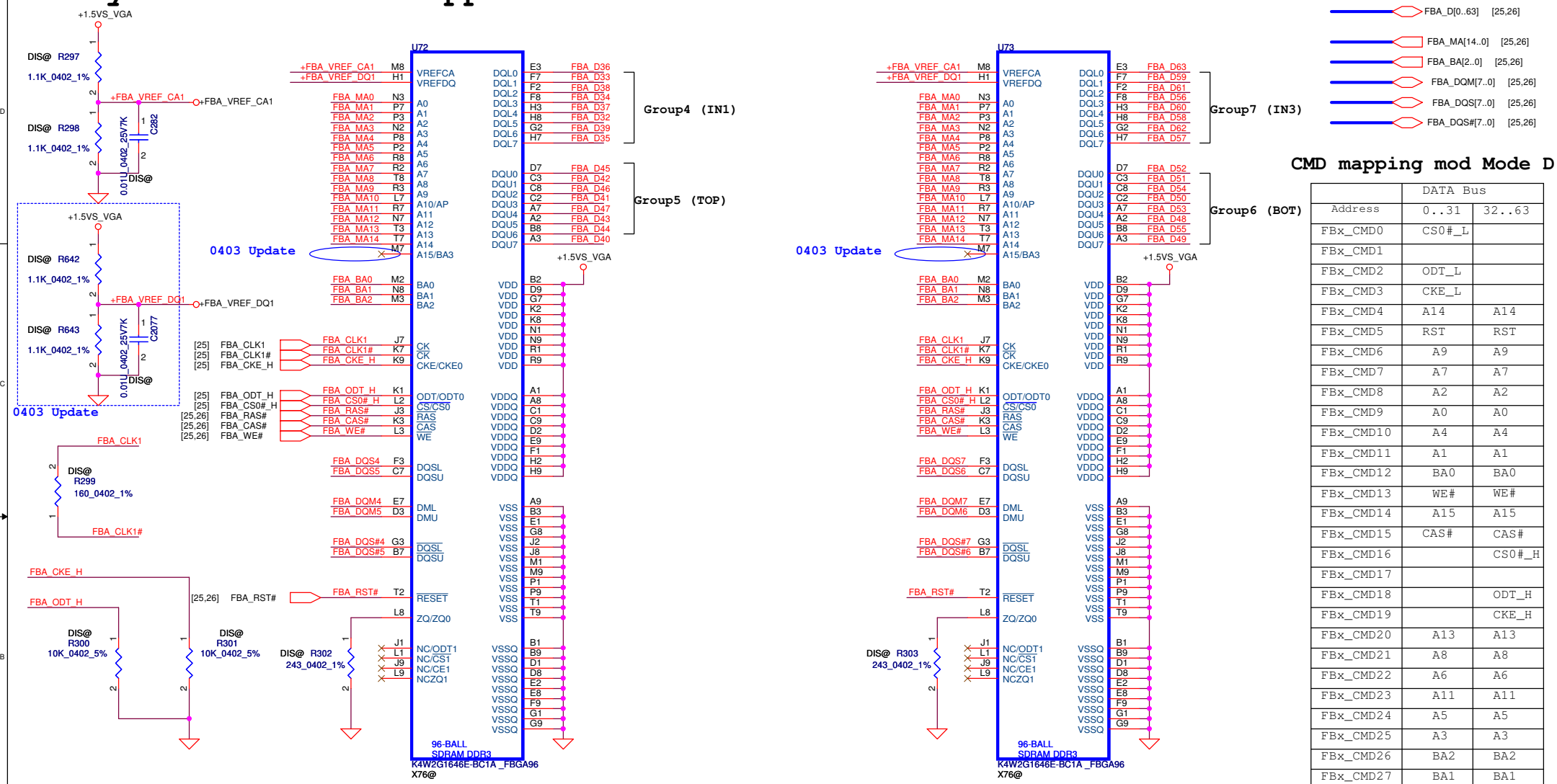
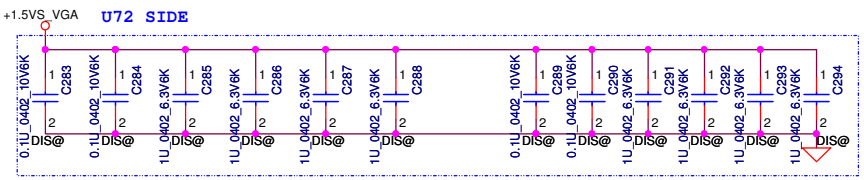
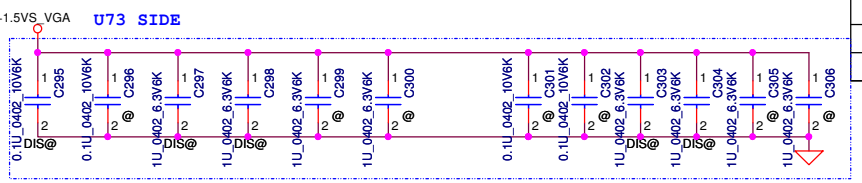
Memory Partition A - Upper 32 bits







FBA_D[0..63] [25,26]
FBA_MA[14..0] [25,26]
FBA_BA[2..0] [25,26]
FBA_DQM[7..0] [25,26]
FBA_DQS[7..0] [25,26]
FBA_DQS#[7..0] [25,26]

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Title: N14M-GE2-VRAM A Upper

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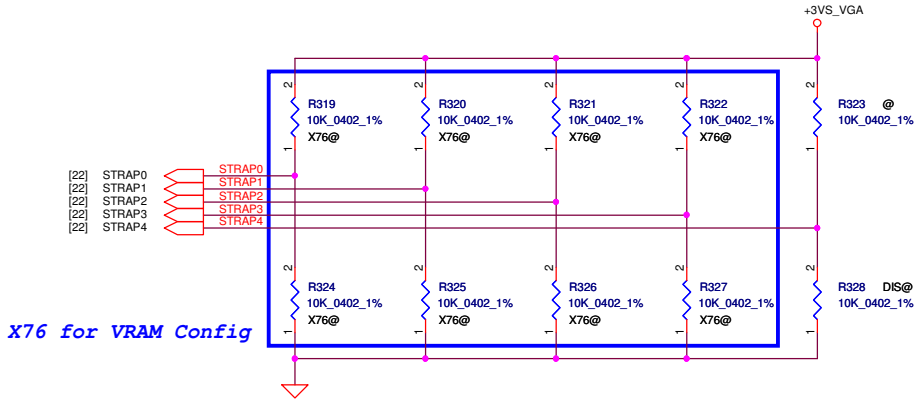
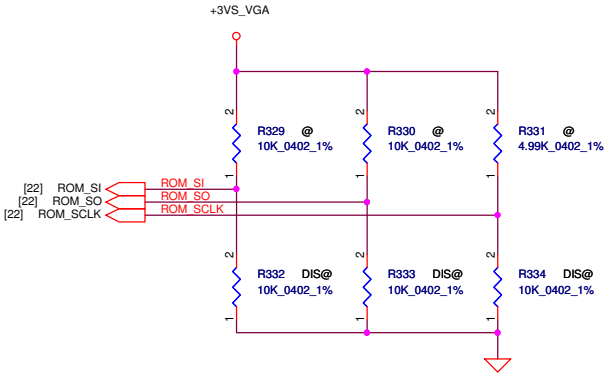


X76 for VRAM Config



[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

[VRAM Config-RVL-06366-001]

GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G:K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G:E SA000065D20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AFR-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

Compal Electronics, Inc.

Title: N14M-GE2_MISC

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Power Consumption:

Pin 22 (PVCC) < 50 mA
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 43 (VCCK) < 50mA
Pin 11 (DPV12) < 100mA

SE070104Z80
S CER CAP .1U 16V Z Y5V 0402
S CER CAP .1U 16V Z Y5V 0402

v0.2 update

v0.2 update

Vendor suggest to reserve for FW/EDID debug

+3VS_DVCCTL
EVT@ U19
CAT24C02WI-GT3_SO8
EESCL
EESDA
Addr:A8 (1010 100x)

EVT Debug Only, un-pop for DVT

+3VS_DVCCTL
@C363
C361 10U_0603_6.3V6M
C362 0.1U_0402_16V4Z
C364 0.1U_0402_16V4Z
C365 22U_0805_6.3V6M

+3VS_AVCCTL
C366 10U_0603_6.3V6M
C367 0.1U_0402_16V4Z
C368 0.1U_0402_16V4Z

+1.2VS_SWR
C369 10U_0603_6.3V6M
C370 0.1U_0402_16V4Z
C371 10U_0603_6.3V6M
C372 0.1U_0402_16V4Z

+3VS
+3VS_RTD
@R337 0_0805_5%
C358 1U_0402_6.3V6K

+3VS_RTD
@R353 1K_0402_5%
PreMP
PCH_DDPD_HPD

+3VS_AVCCTL
+3VS_DVCCTL
+3VS_RTD
+1.2VS_SWR
TAI_HCB2012KF-221T30 L9
TAI_HCB2012KF-221T30 L10
@R340 0_0603_5%
+SW_LX

U20
RTD2136R
PVCC
SWR_VDD
DP_V33
SWR_LX
SWR_VCCK
VCCK
DP_V12
PWR

LANE0P
LANE0N
LANE1P
LANE1N
AUX-CH_P
AUX-CH_N
DP_HPD
DP

PWMIN
TESTMODE
DP_REXT
MODE_CFG1
MODE_CFG0
CIICSCL1
CIICSDA1
OTHERS

DP_GND
GND
PAD
GND

RTD2136R-CG_QFN48_6x6

LVDS

TXOC+ TXOC- [32]
TXO0+ TXO0- [32]
TXO1+ TXO1- [32]
TXO2+ TXO2- [32]
TXO3+ TXO3- [32]
TXEC+ TXEC- [32]
TXE0+ TXE0- [32]
TXE1+ TXE1- [32]
TXE2+ TXE2- [32]
TXE3+ TXE3- [32]
MIICSCL1 MIICSDA1 EESCL EESDA
PANEL_VCC PWMOUT BL_EN S_ENVDD S_BKOFF#
S_ENVDD [32,43]
S_BKOFF# [32,43]
S_INVT_PWM [32]

eDP portD
[5] CPU_EDP_TXP0_C CPU_EDP_TXN0_C
[5] CPU_EDP_TXP1_C CPU_EDP_TXN1_C
[15] PCH_DDPD_AUXP_C PCH_DDPD_AUXN_C
[15] PCH_DDPD_HPD
PCH_DDPD_HPD 1 R344 2 LVDS_HPD_R 1K_0402_5%

CPU [5] EDP_DISP_UTIL @R345 0_0402_5%
PCH [15] PCH_EDP_PWM @R347 0_0402_5%
R349 12K_0402_1%

MODE_CFG1 MODE_CFG0

To EC
[32,43] EC_SMB_CK1 EC_SMB_DA1
@R351 0_0402_5%
@R352 0_0402_5%
EC_SMB_CK1_R EC_SMB_DA1_R

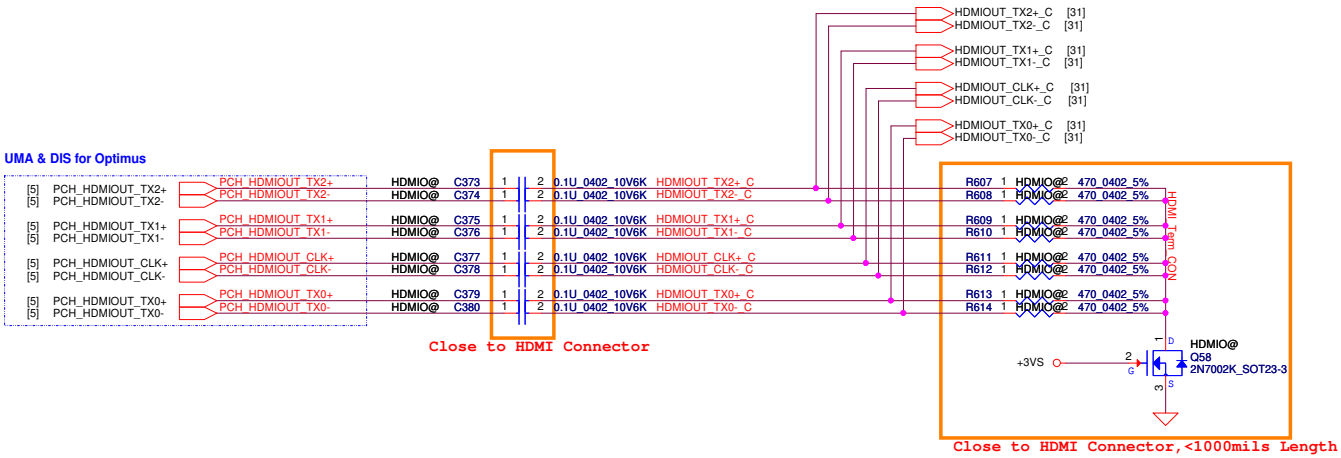
R343 4.7K_0402_5%
@R346 4.7K_0402_5%
MODE_CFG0
@R341 4.7K_0402_5%
R342 4.7K_0402_5%
MODE_CFG1

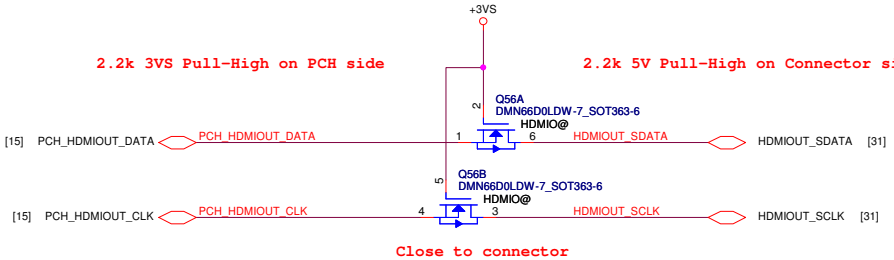
R636 4.7K_0402_5%
@R638 4.7K_0402_5%
EESCL
R637 4.7K_0402_5%
@R639 4.7K_0402_5%
EESDA

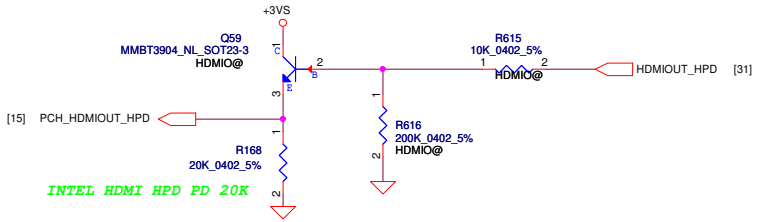
	Pin 47	
	0	1
Pin 48 0	X	EP Mode
Pin 48 1	ROM	EEPROM

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	LVDS Converter RTD2136S		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 29 of 59		







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ***HDMI-OUT Level Shift***

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

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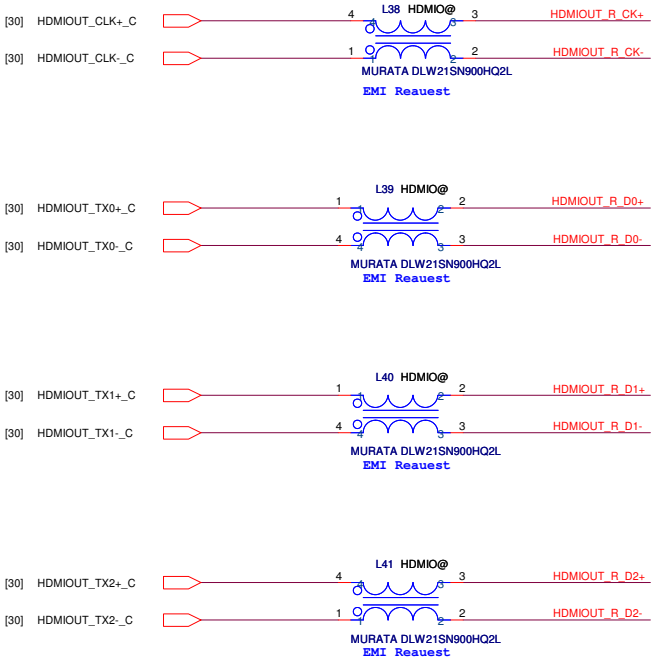
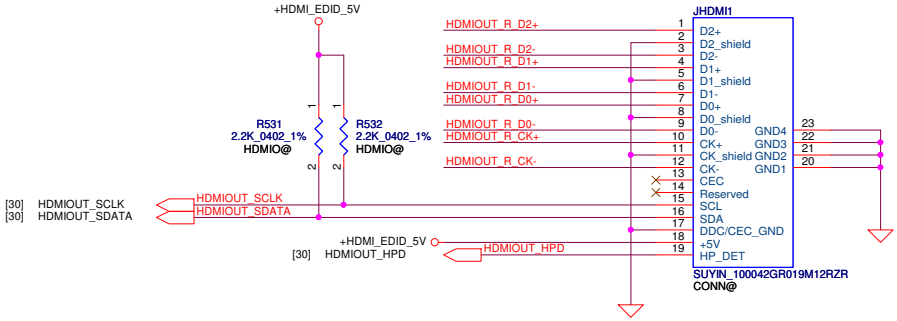
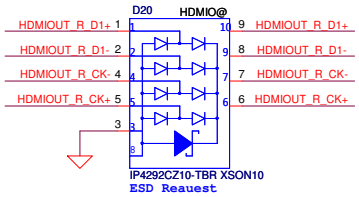
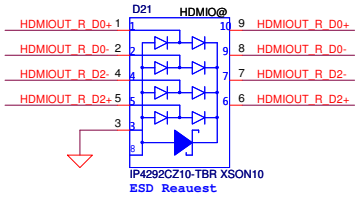
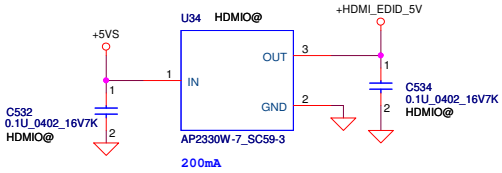
HDMI-OUT Connector

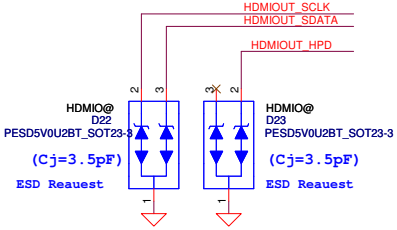












Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: HDMI-OUT

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Custom	ZEA00 LA-A061P M/B	0.3

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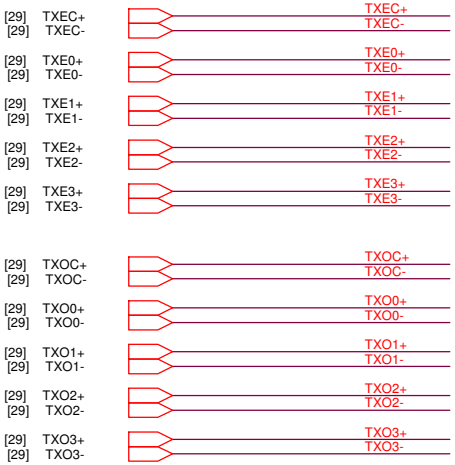
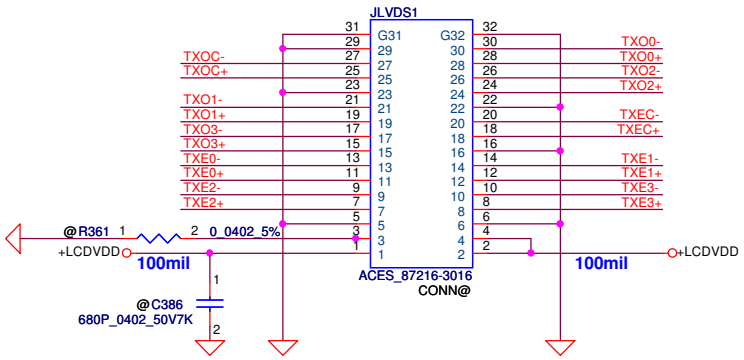
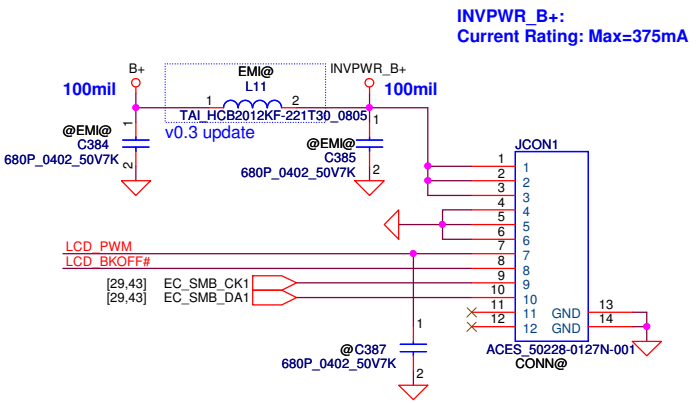
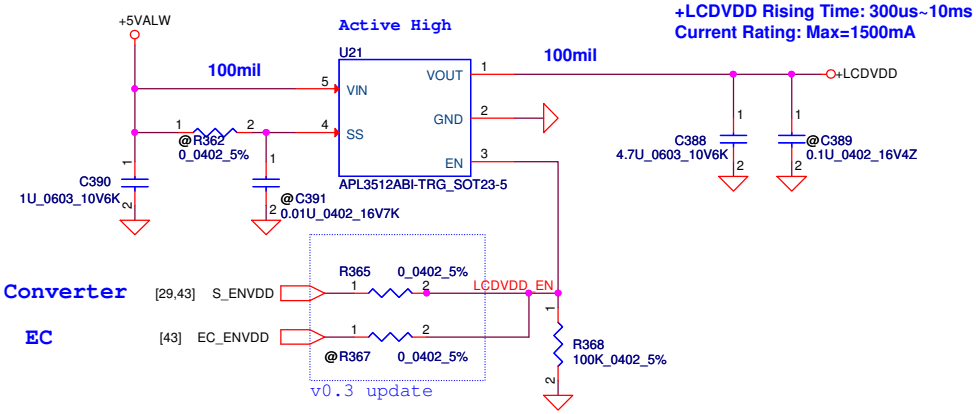
LVDS Conn.

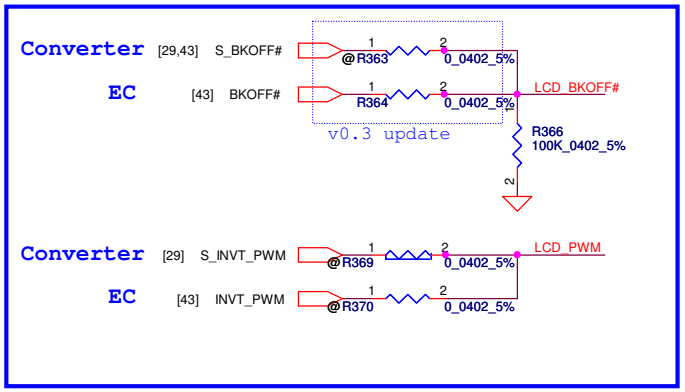




Converter







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **LVDS**

Size	Document Number	Rev
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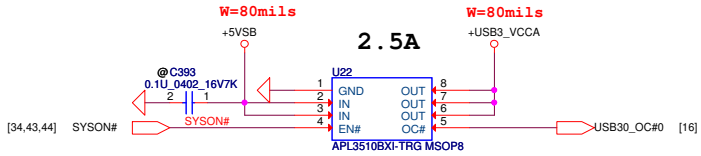
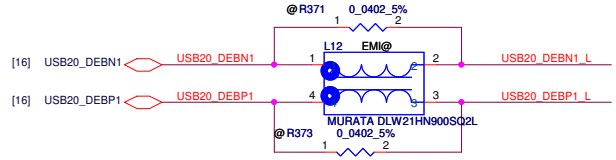
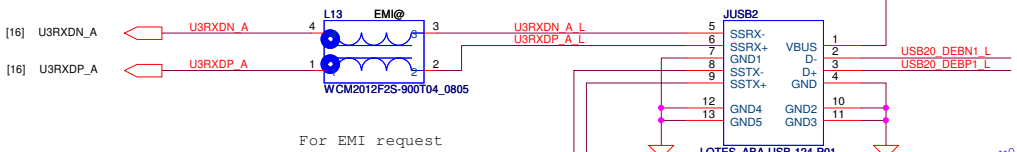
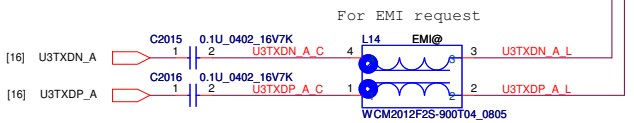
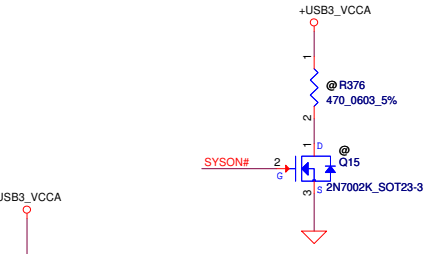
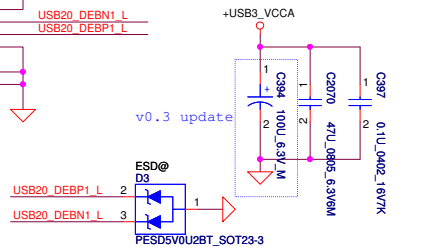


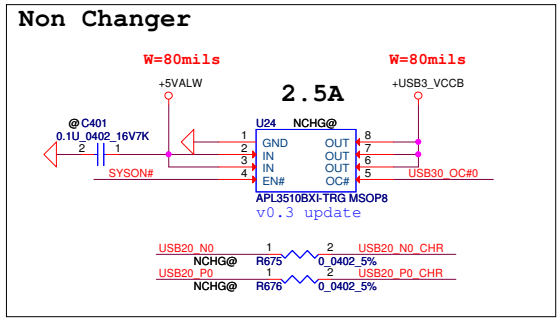


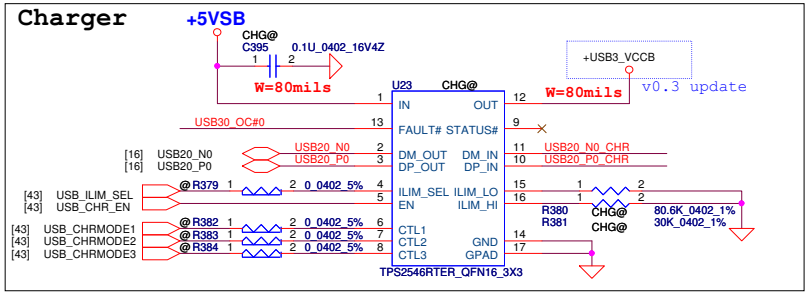






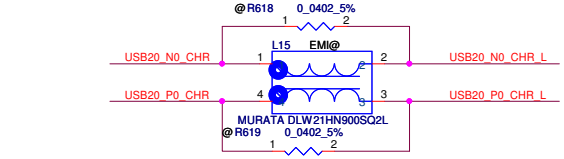


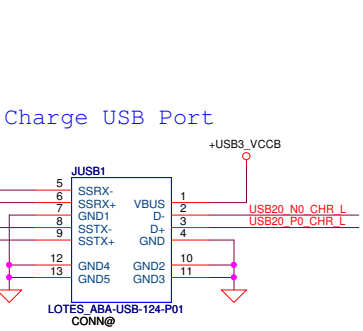


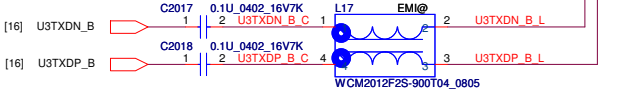


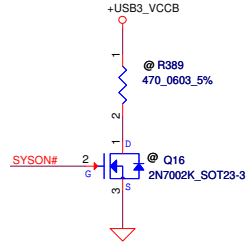
Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07(pin104)	GPIO22(pin41)	GPXIOA11(pin108)	GPIO21(pin40)
S0(CDP)	1	1	1	1
S3(SDP)	1	1	1	0
S4/S5(DCP)	0	0	1	1

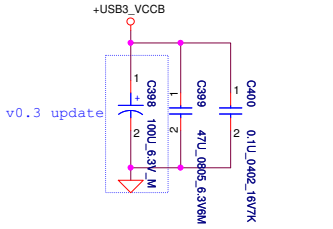
System Global Power State	TPS2546/TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake	0	0	1	1	ILIM_HI

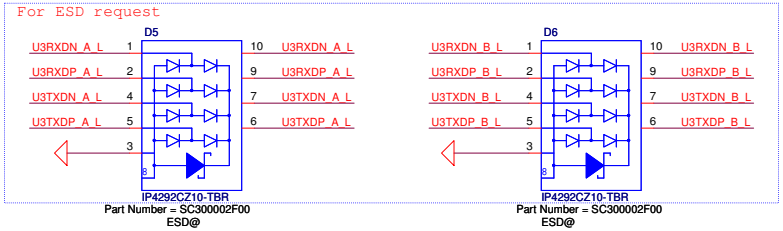












Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: USB 3.0 CONN

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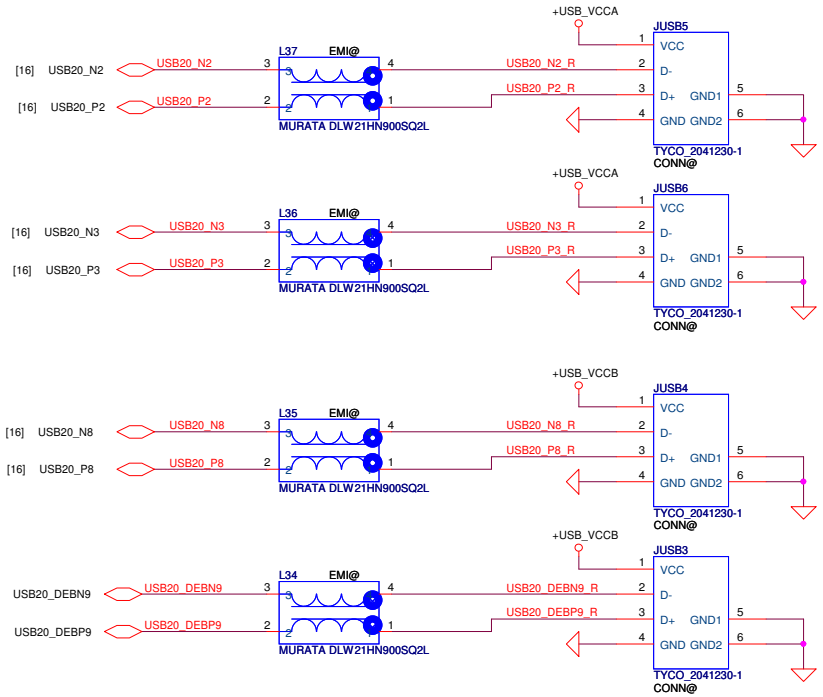
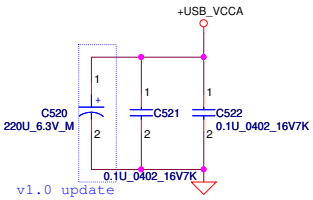
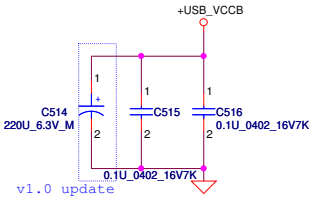
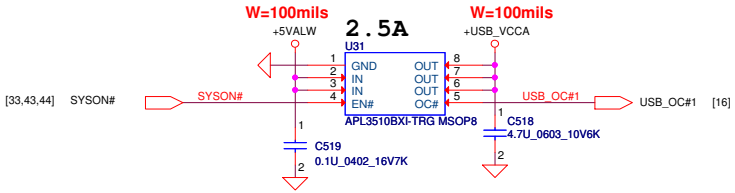
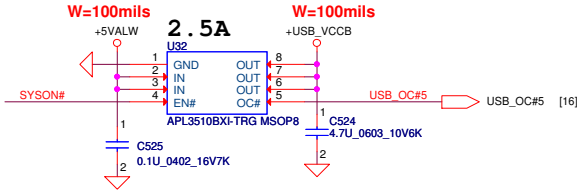
USB20



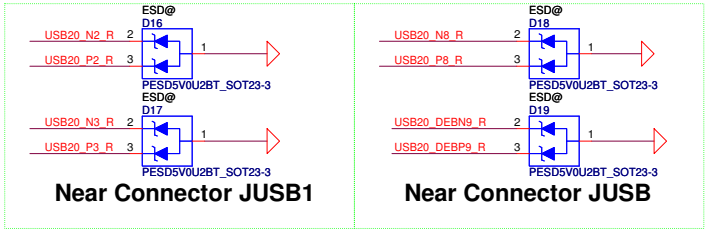


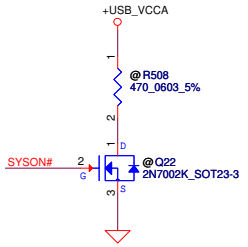


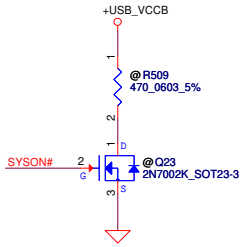




For USB2.0 ESD diode







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	USB20		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
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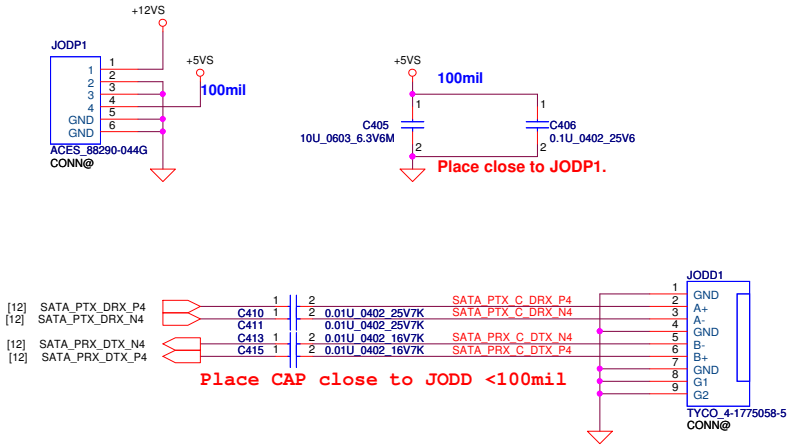
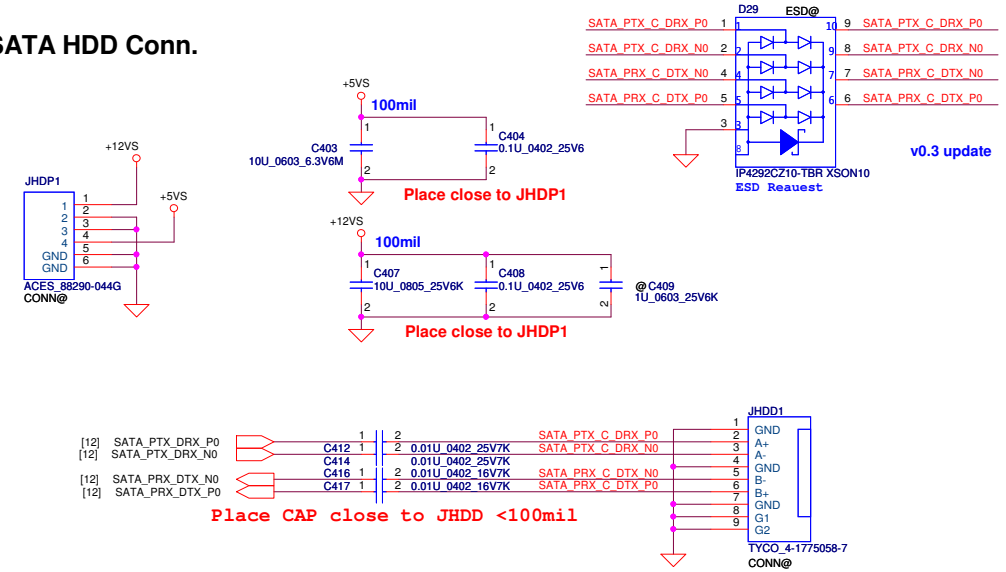
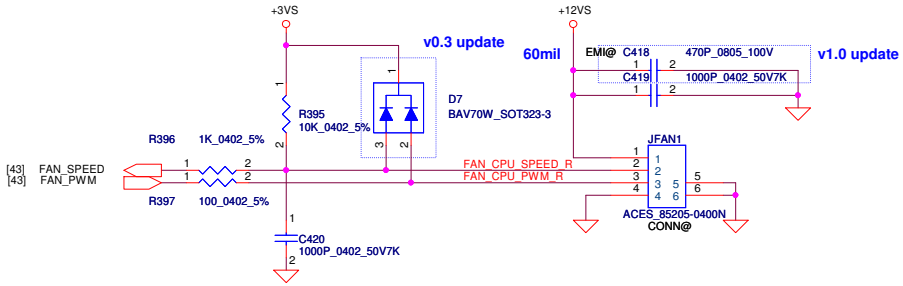
SATA ODD Conn



SATA HDD Conn.



FAN Control Circuit



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	SATA-HDD/ODD/USB		
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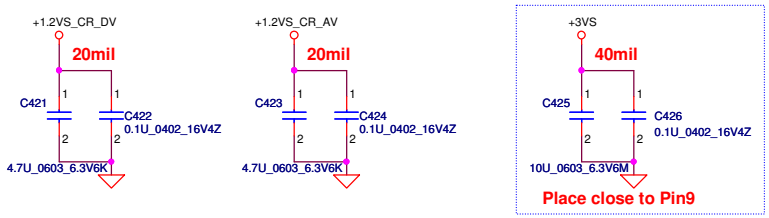
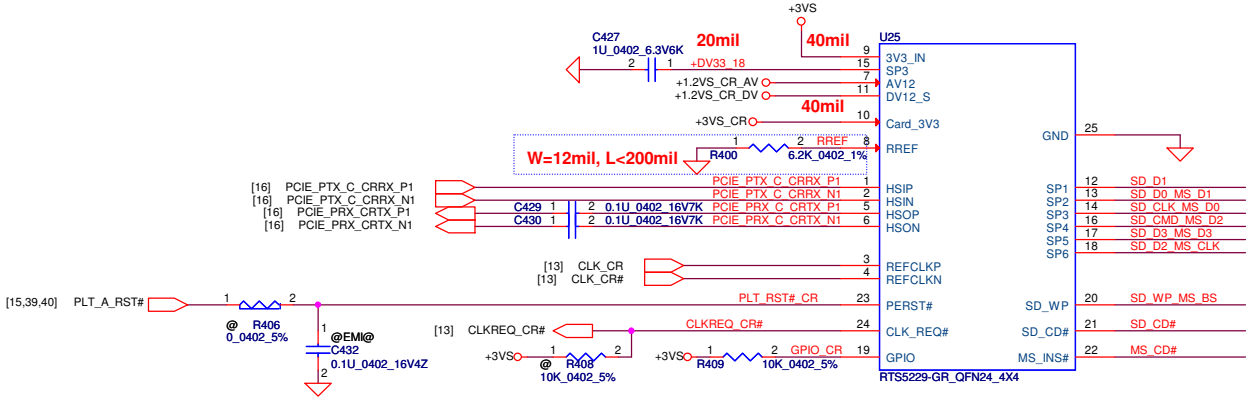
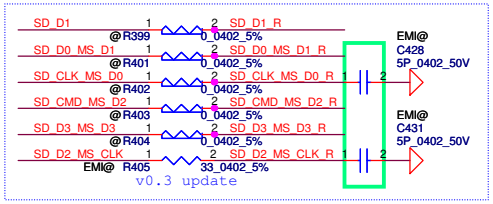
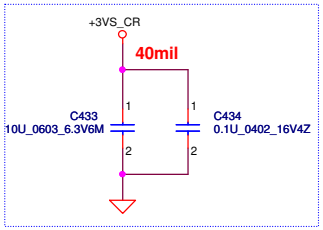


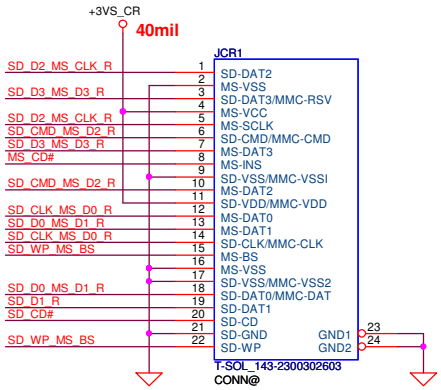


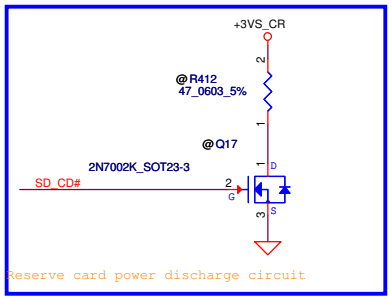
Length of per trace 2inch no more 2 via
mismatch trace length <100mil
50ohm +-15% impedance.



Place close to JCR1 pin 12,21







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: RTS5229 Media Card Controller

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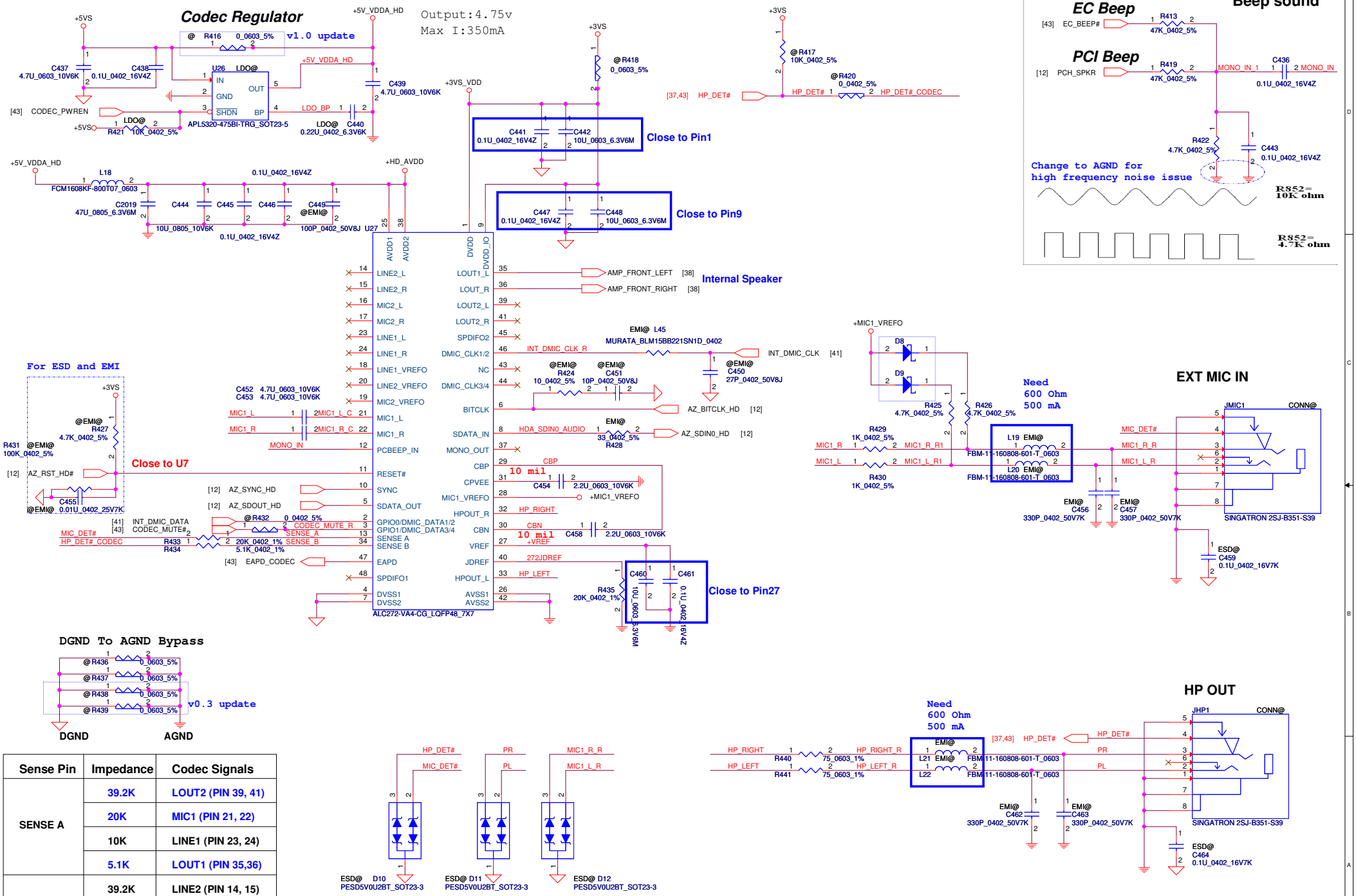

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
	5.1K	HP-OUT (PIN 32,33)

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	HDA-ALC272/HP/MIC		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
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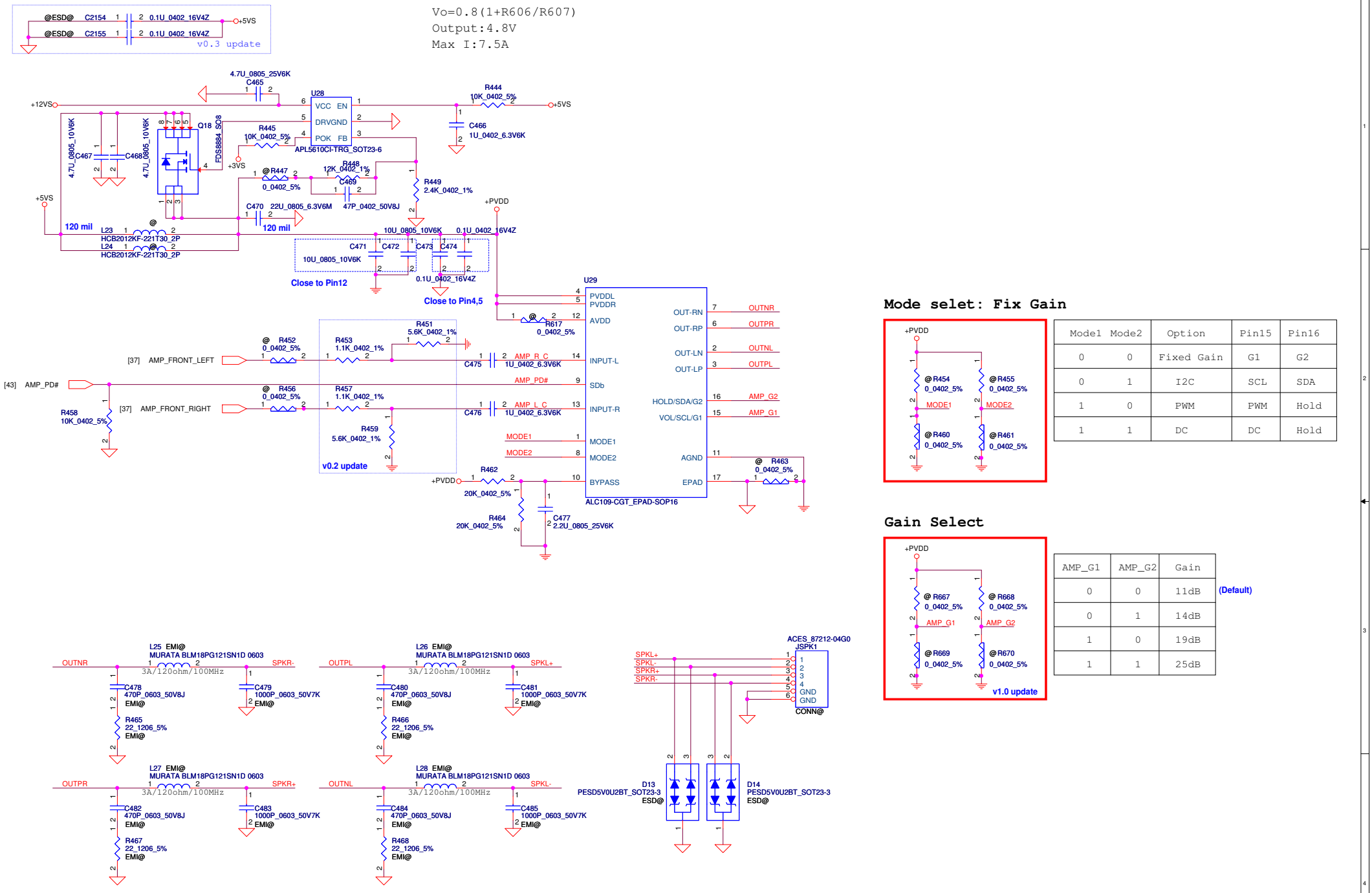

Mode selet: Fix Gain

Mode1	Mode2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

Gain Select

AMP_G1	AMP_G2	Gain	
0	0	11dB	(Default)
0	1	14dB	
1	0	19dB	
1	1	25dB	

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: AMP

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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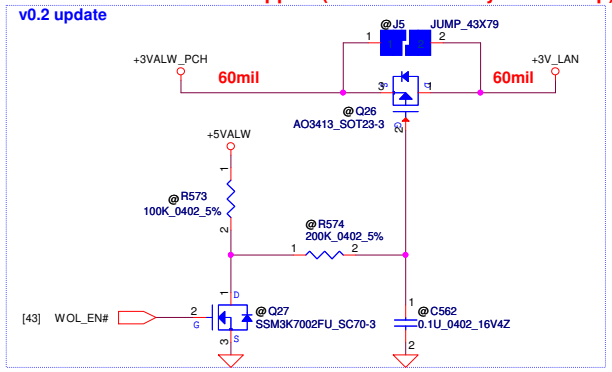
WOL circuit

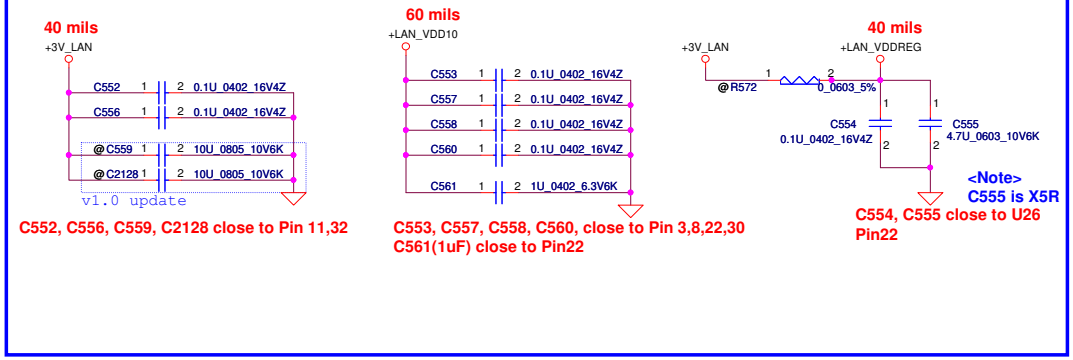
Short J5 for WOL support (Enable/Disable by BIOS setup)

v0.2 update



+3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)



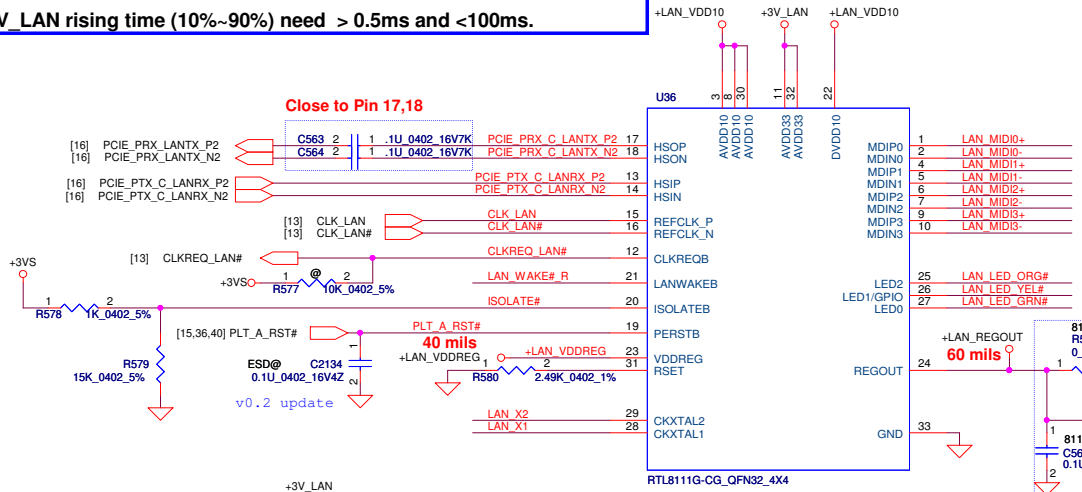
C552, C556, C559, C2128 close to Pin 11,32

C553, C557, C558, C560, close to Pin 3,8,22,30
C561(1uF) close to Pin22

<Note>
C555 is X5R

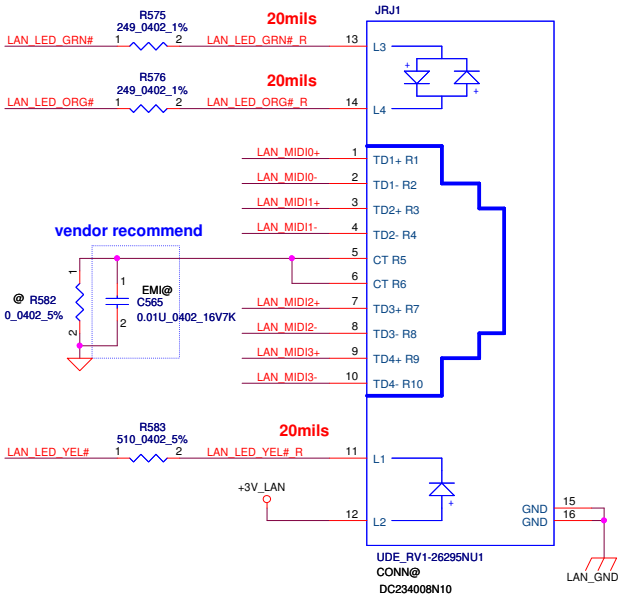
C554, C555 close to U26 Pin22

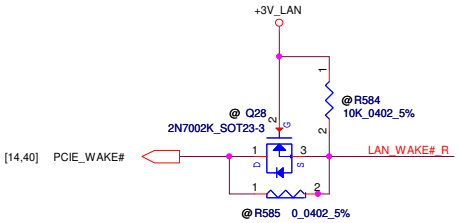
Close to Pin 17,18

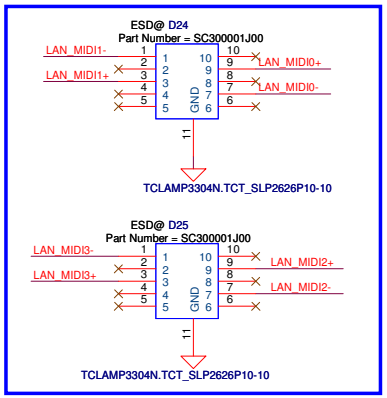


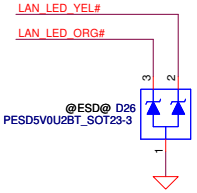
Green / Orage

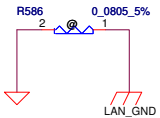
Yellow



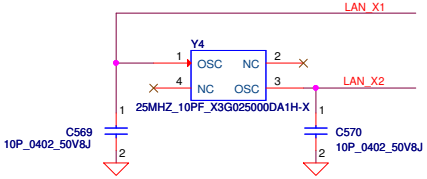








Crystal



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: LAN RTL8111G

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

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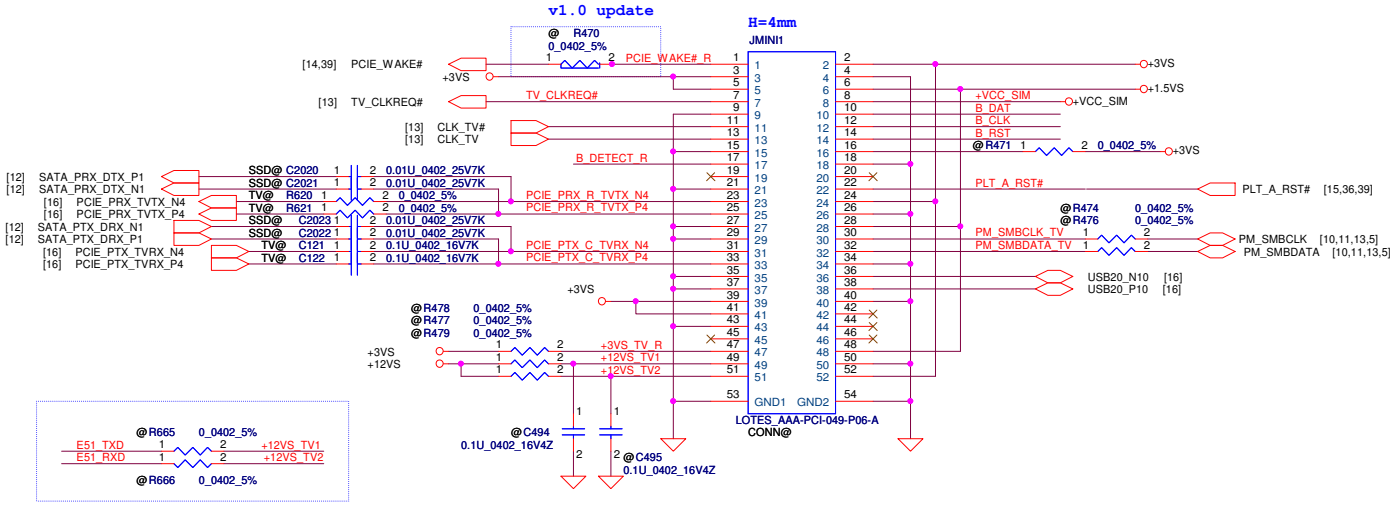
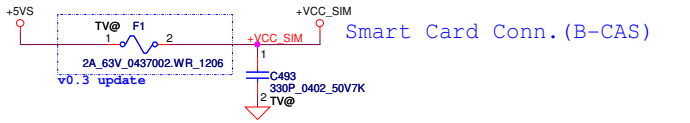
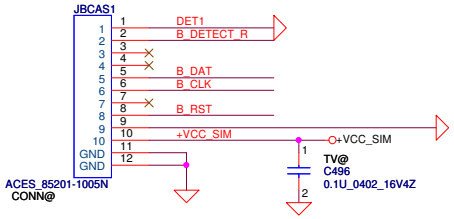
MINI (TV) /m-SATA SSD

Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA

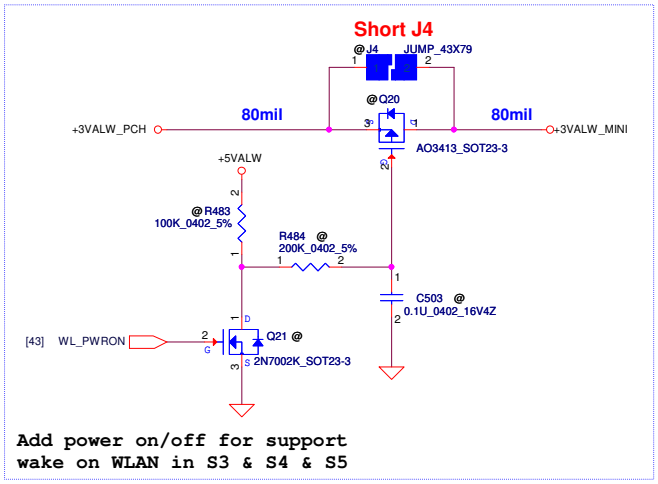


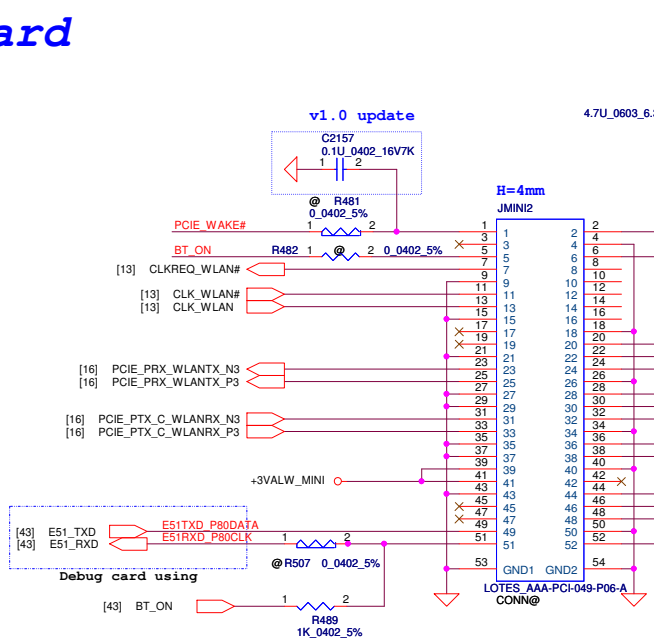


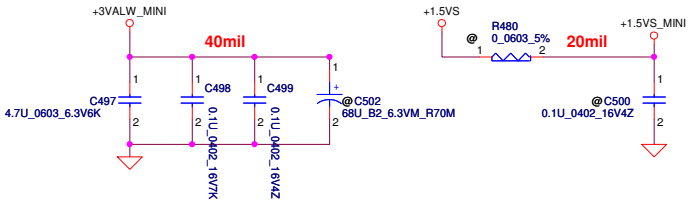


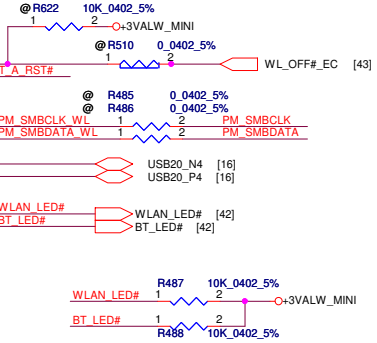
WLAN & Bluetooth Combo Card

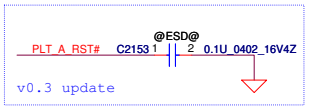
Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,











Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	PCIe-WLAN/TV_B-CAS		
Size	Document Number		Rev
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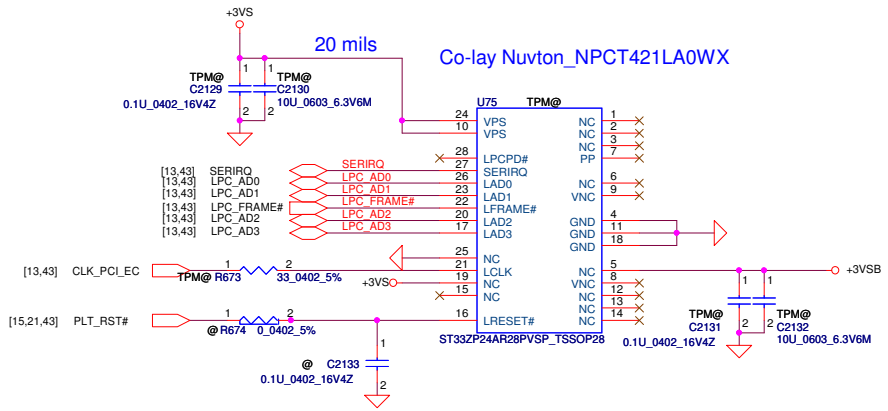
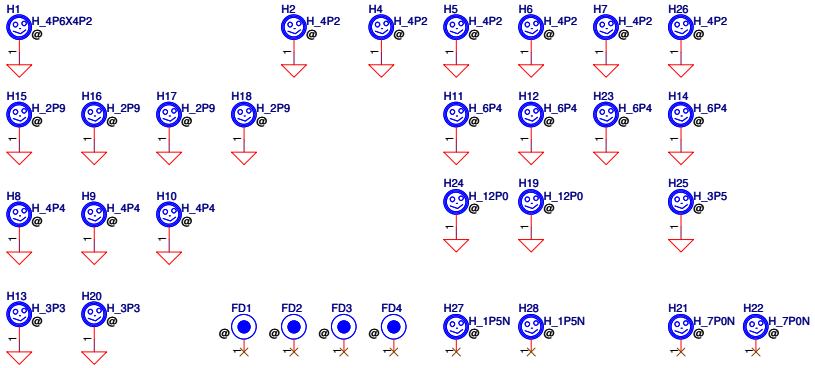
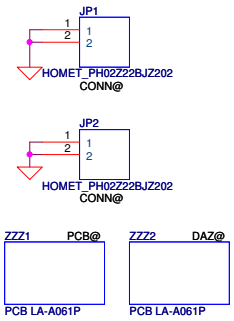
TPM(Reserve)



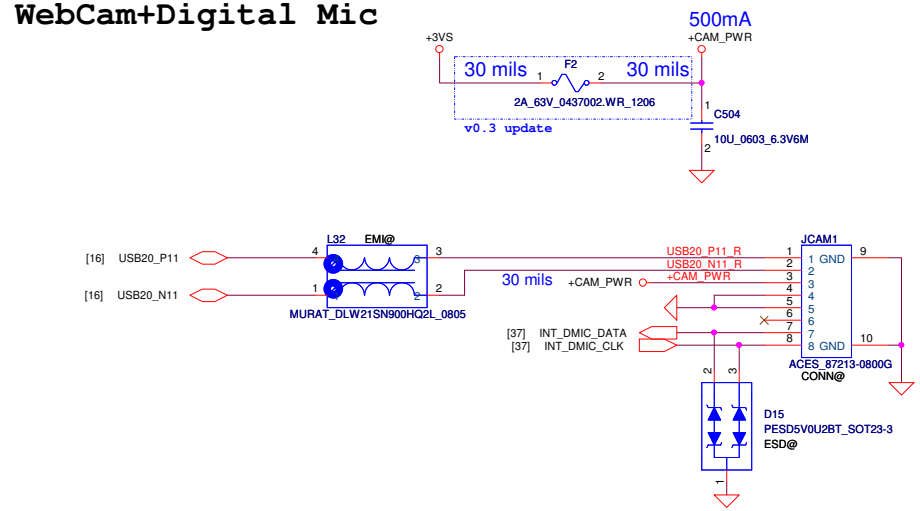
Screw Hole



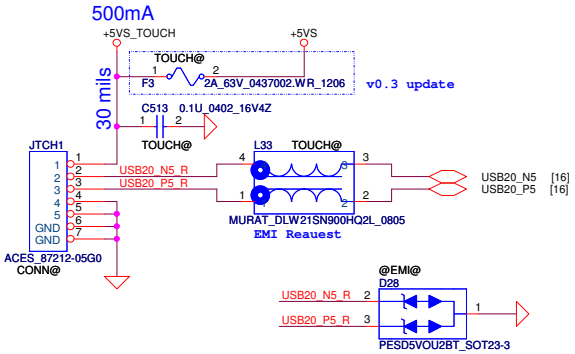
PCH heat sink



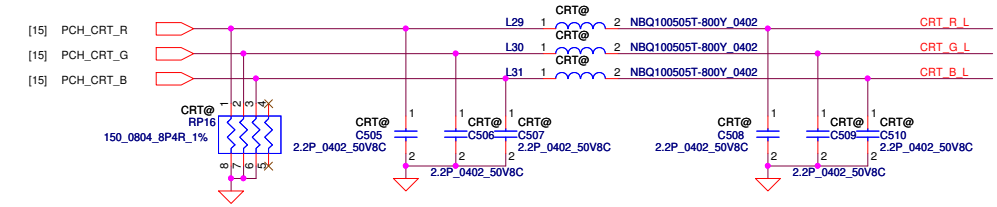
WebCam+Digital Mic



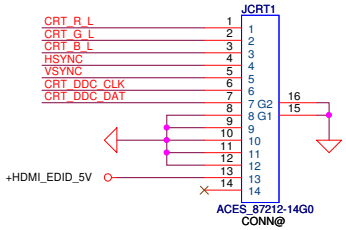
Touch

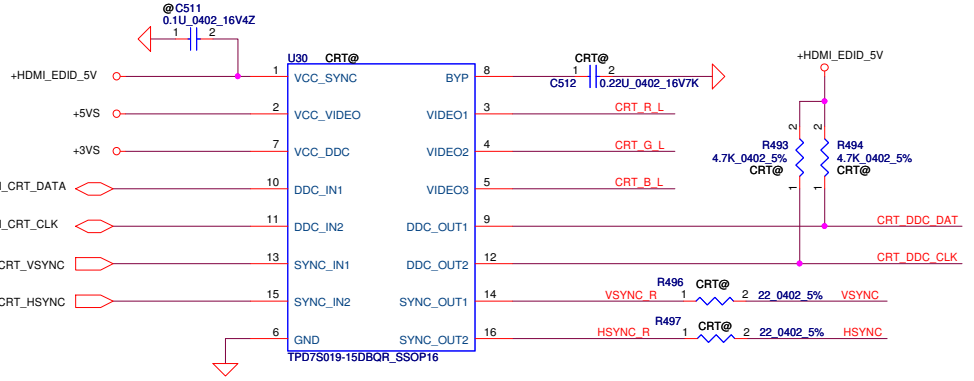


CRT Conn(Reserve 15pin)



Need PU/PL on PCH/FCH side
(2.2K*2pcs for DDC & 150_8P4R*1pcs for RGB)





Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	PWR/Cap./TP/LED/LP/LS/Screw		
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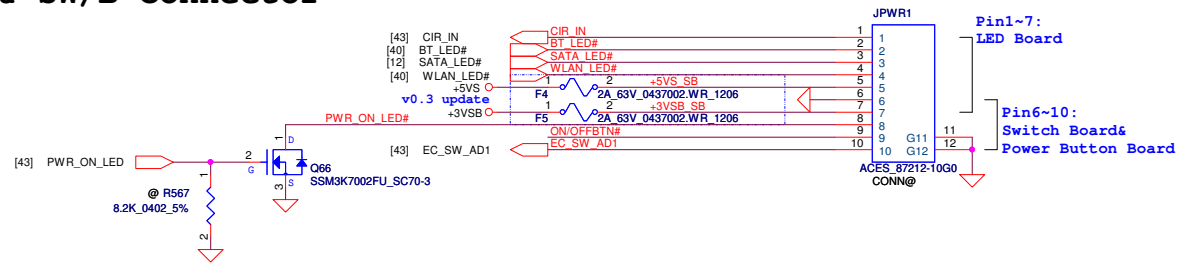
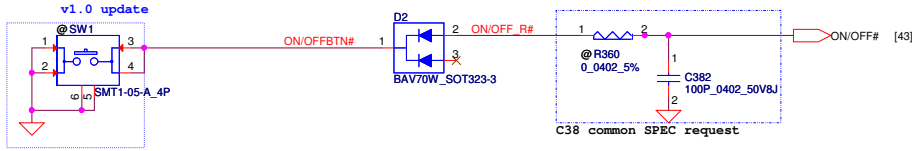
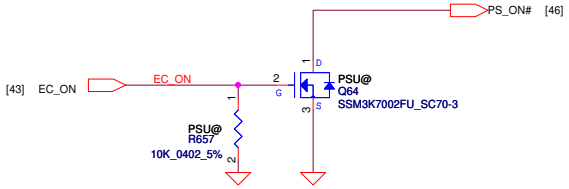
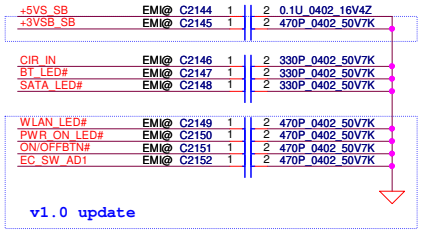
Power/B & SW/B Connector

8Pin sub-board Conncetor









Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	Sub-board Connector		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
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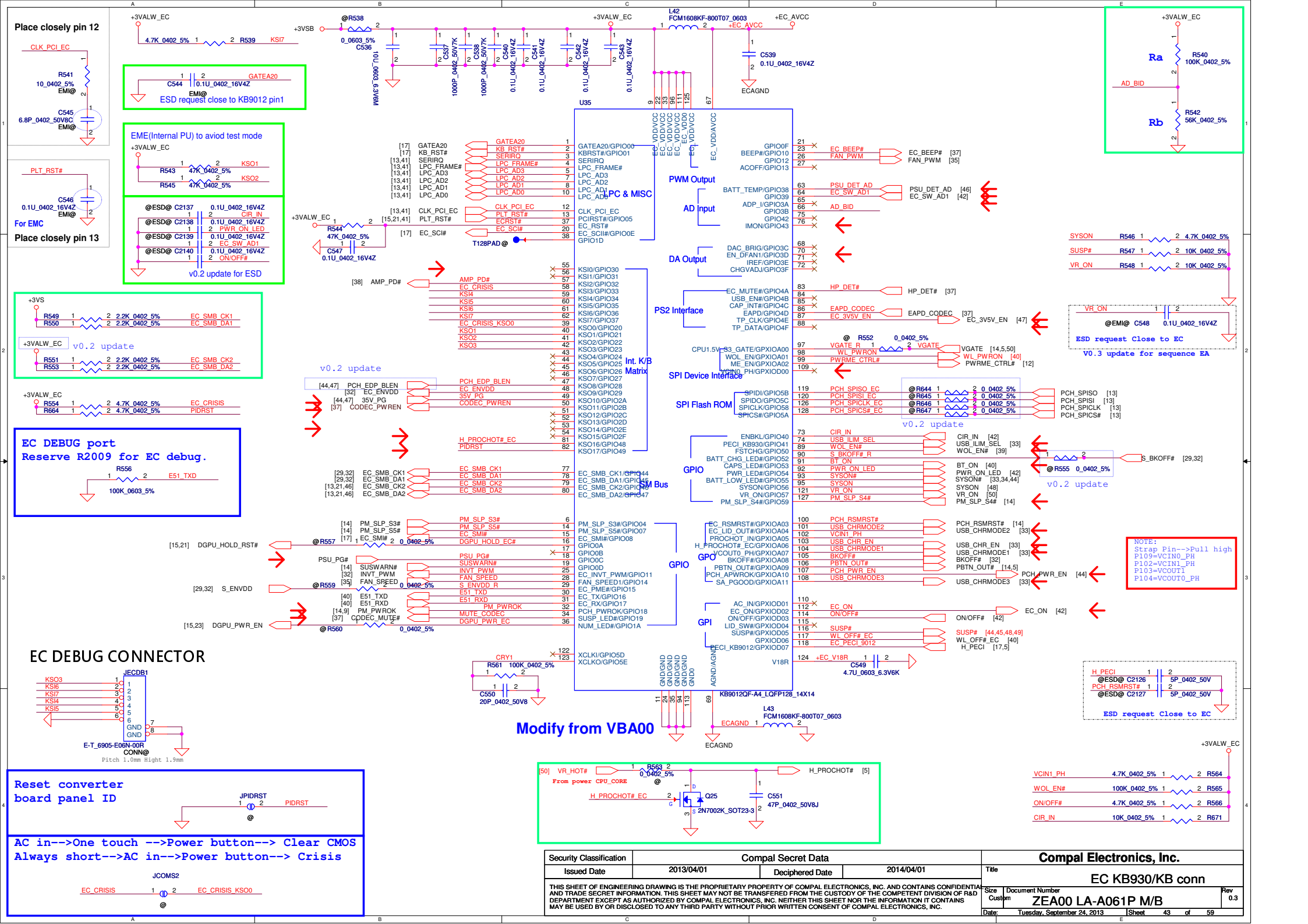
Place closely pin 12
Place closely pin 13
For EMC
EME(Internal PU) to aviod test mode
ESD request close to KB9012 pin1
v0.2 update for ESD
v0.2 update
EC DEBUG port
Reserve R2009 for EC debug.
EC DEBUG CONNECTOR
Reset converter board panel ID
AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis
Modify from VBA00
U35
KB9012QF-A4_LQFP128_14X14
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
SM Bus
Int. K/B Matrix
PC & MISC
ESD request Close to EC
V0.3 update for sequence EA
NOTE:
Strap Pin-->Pull high
P109=VCIN0_PH
P102=VCIN1_PH
P103=VCOUT1
P104=VCOUT0_PH
From power CPU_CORE
Compal Electronics, Inc.
EC KB930/KB conn
ZEA00 LA-A061P M/B
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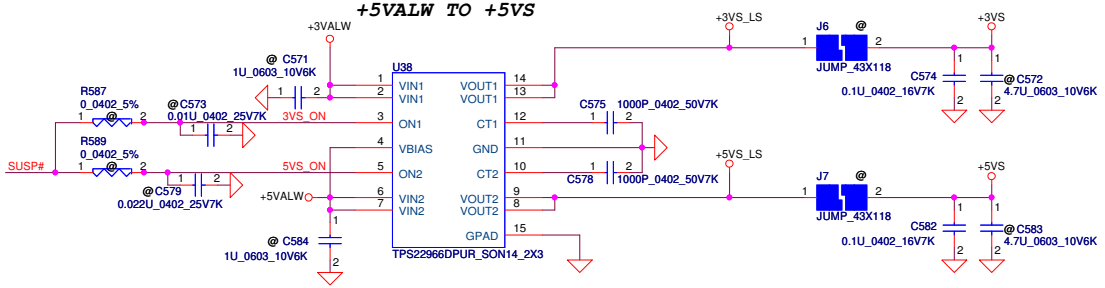
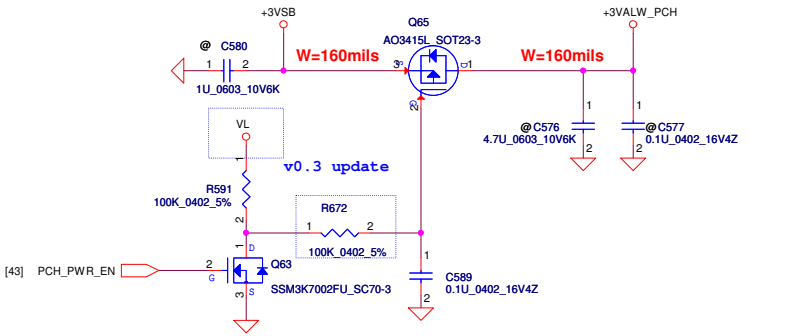
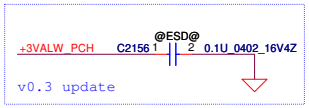
+3VALW TO +3VS
+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm



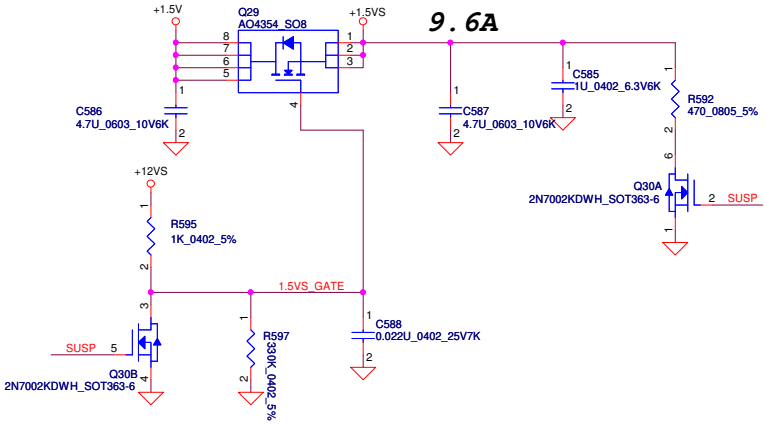
+3VALW TO +3VALW_PCH

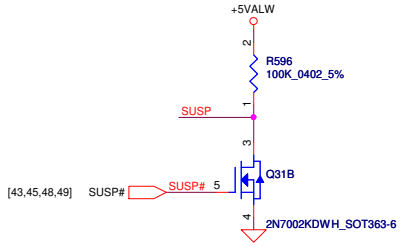




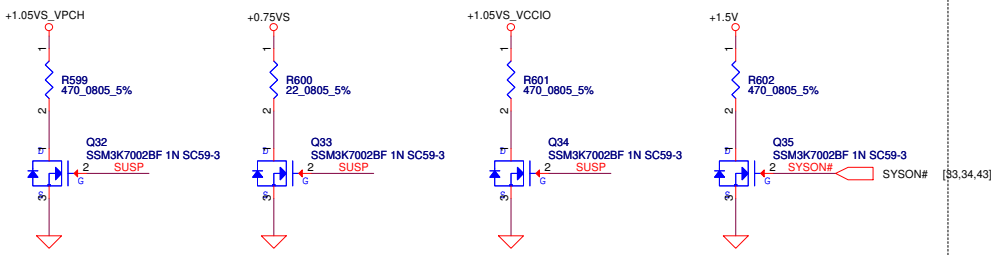
+1.5V to +1.5VS

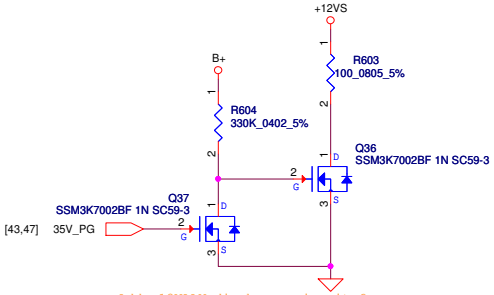
9.6A





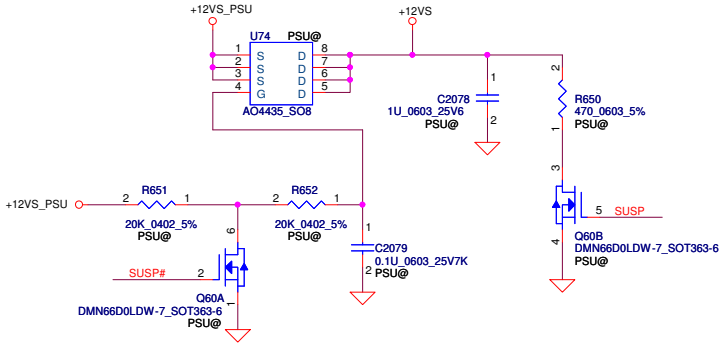
Discharge circuit





Add +12VALW discharge circuit for prevent DC plug in leakage 5/5.

+12V1 TO +12VS (Reserve for PSU)



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size: | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

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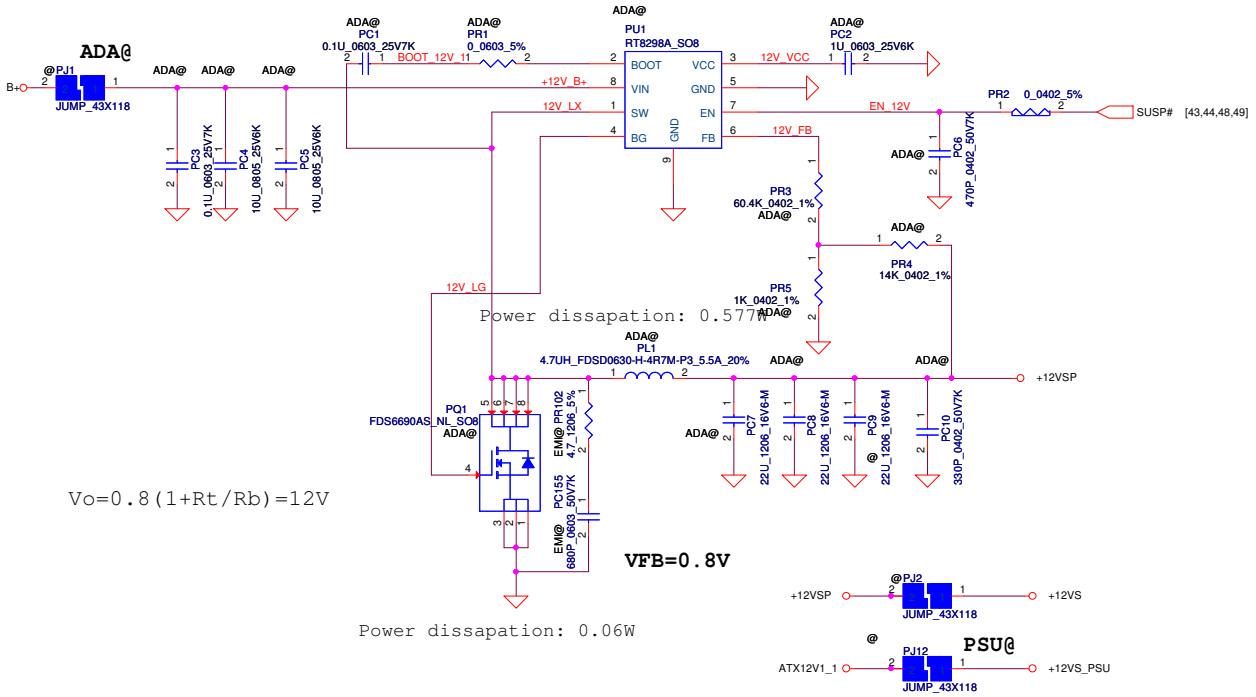
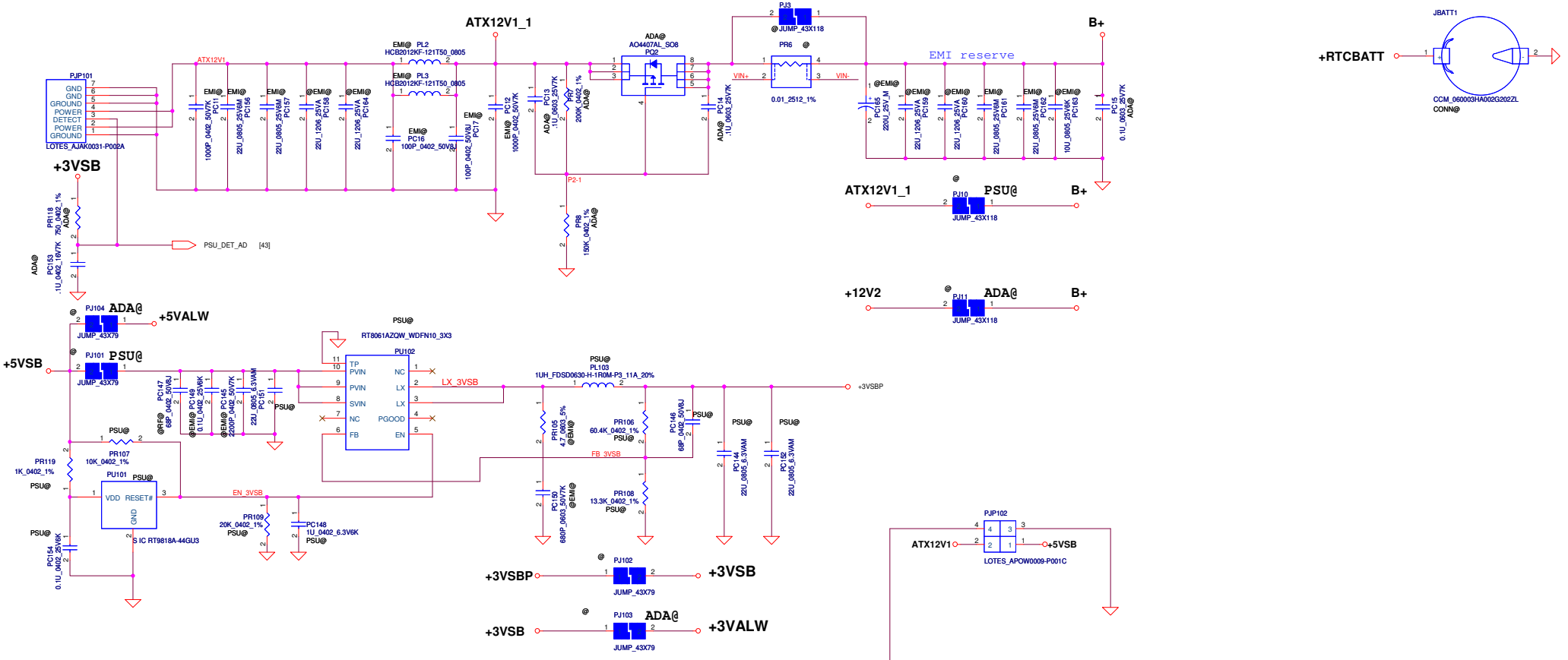


Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

Compal Electronics, Inc.			
Title: PWR- 12VSP			
Size: Custom	Document Number: VBA11 LA-A111 M/B		Rev: 0.1
Date: Tuesday, September 24, 2013	Sheet 45 of 56		



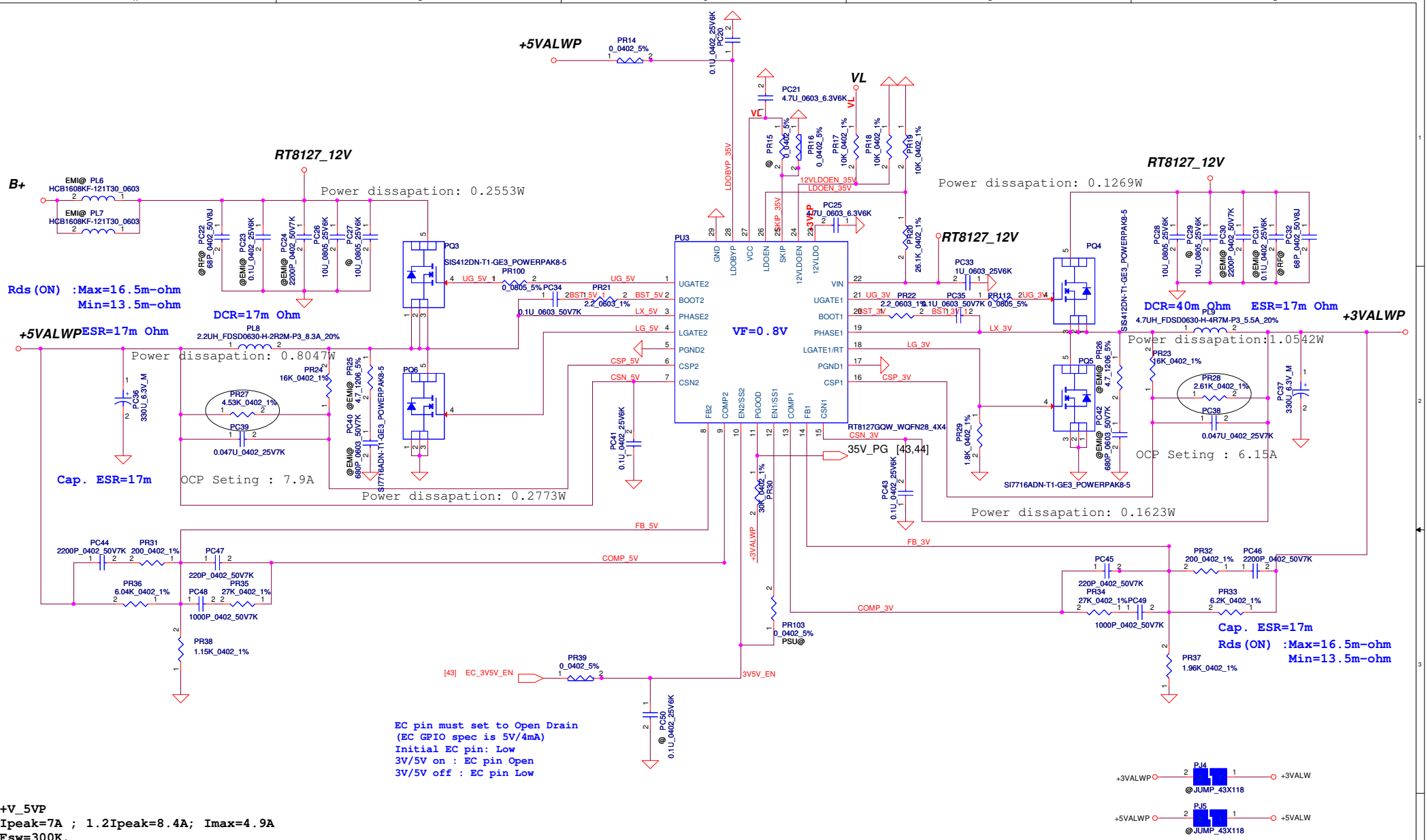
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2012/11/12

Compal Electronics, Inc.

Title: PSU IN

Size	Document Number	Rev
C		0.1

Date: Tuesday, September 24, 2013 | Sheet 46 of 56



+V_5VP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
Fsw=300K,
Iocp>=8.66A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

+V_3.3VP
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A
Fsw=300K
Iocp>=5.33A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

TON (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=300KHZ (+3VALWP)

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR- 3VALWP/5VALWP

Size: Custom | Document Number: VCA00 LA-9792P M/B | Rev: 0.1

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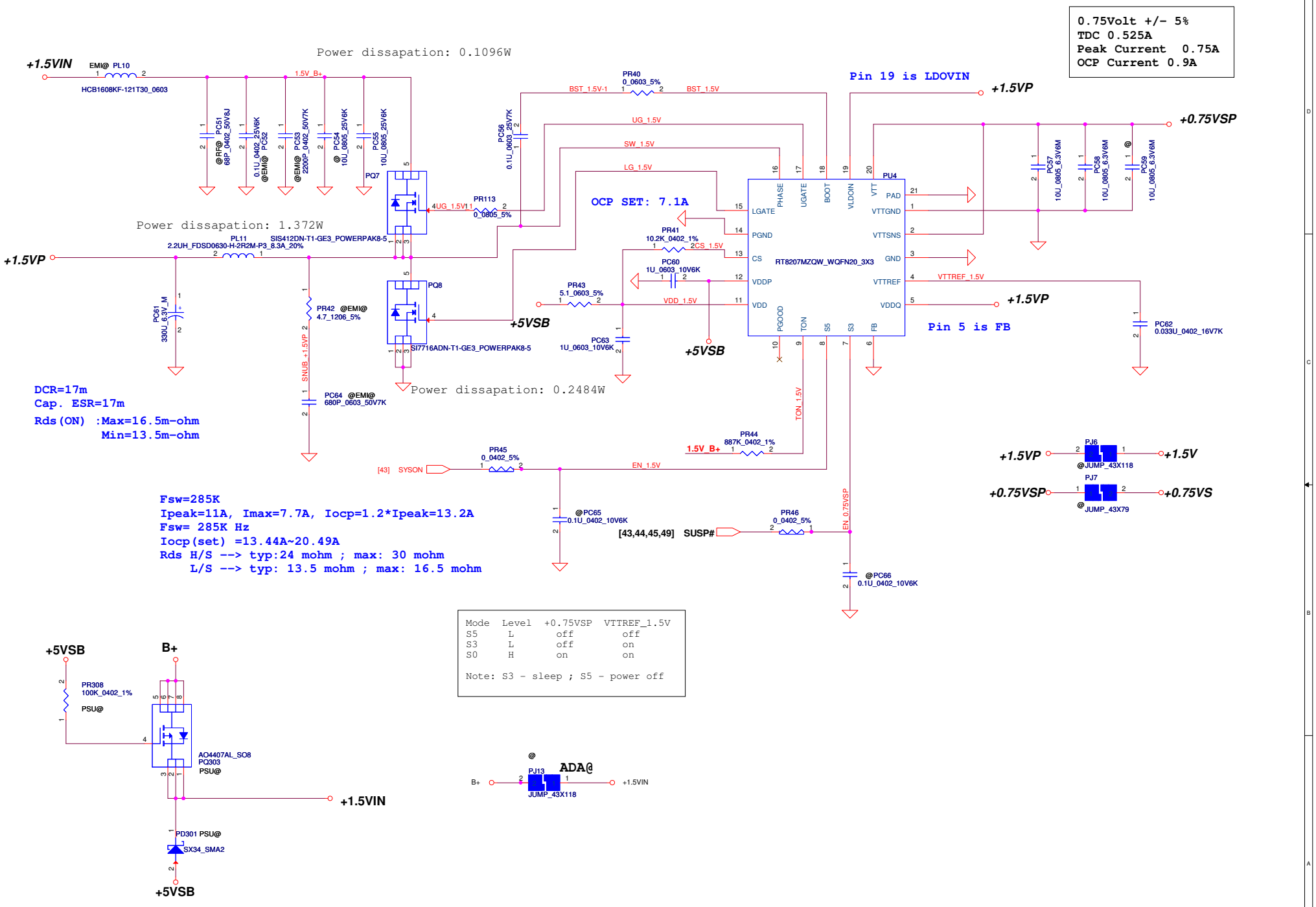

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
Title: 1.5VP			
Size: B	Document Number		Rev: 0.1
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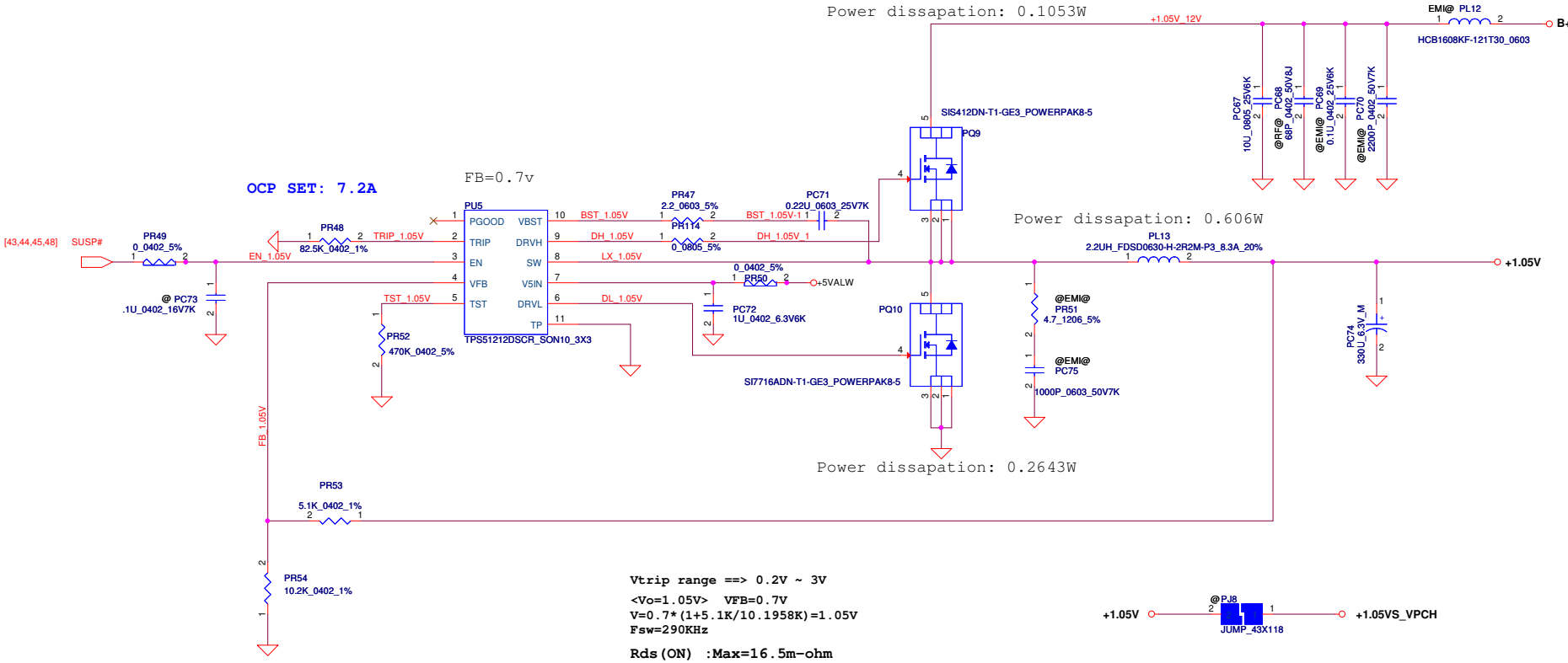

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: +1.05VSP

Size: Custom | Document Number | Rev: 0.1

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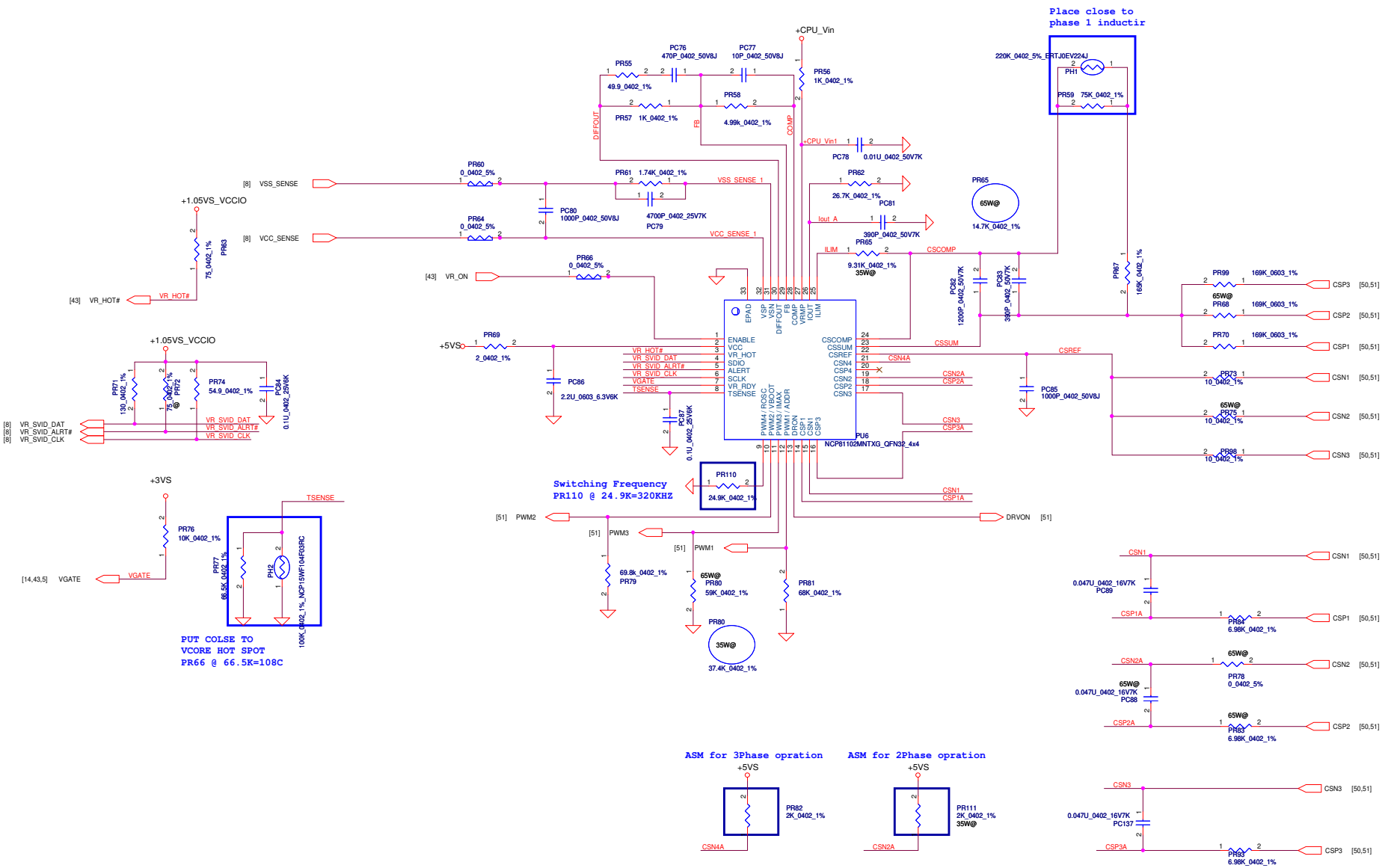
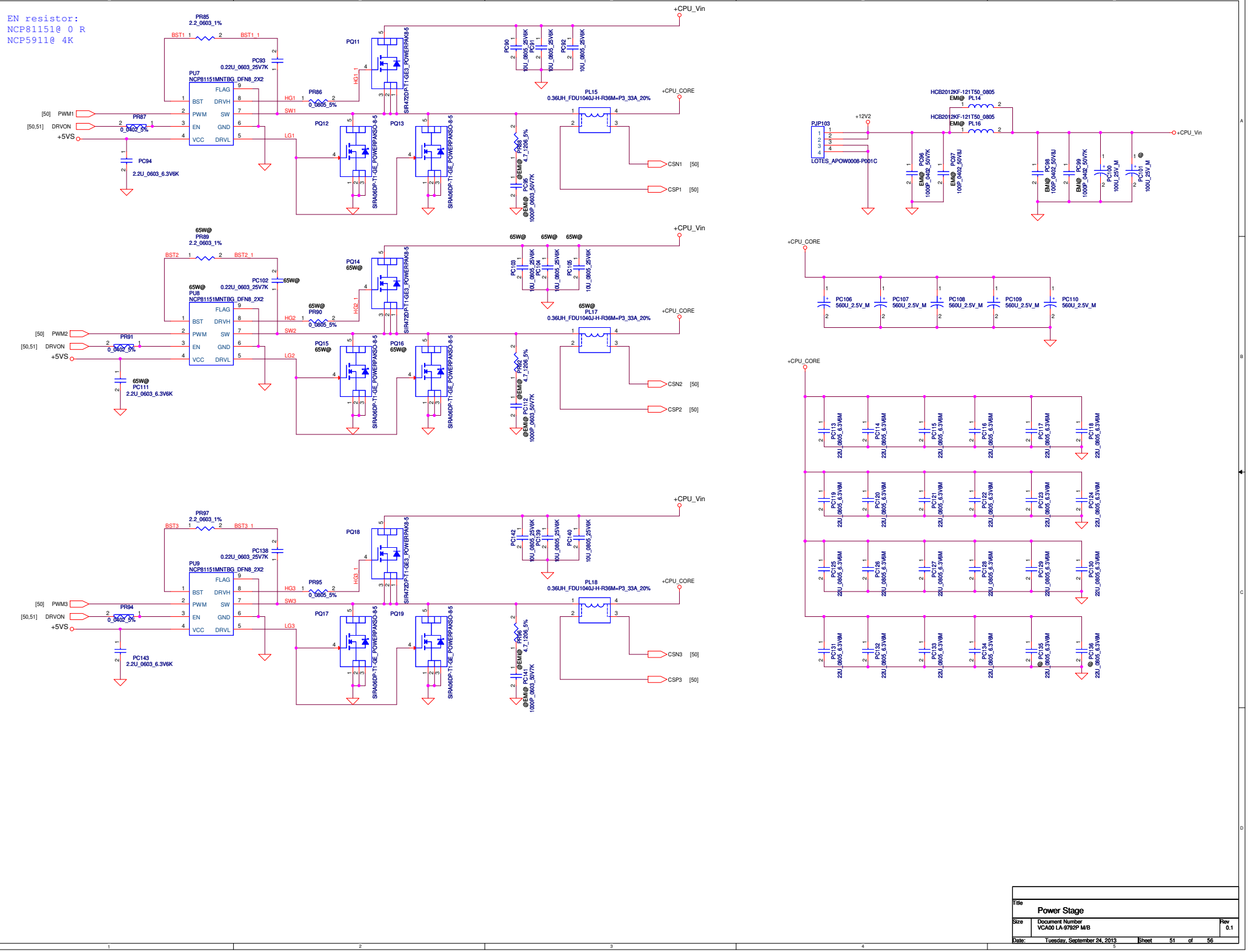


Title	NCP81102	
Size	Document Number VCA00 LA-9792P M/B	Rev 0.1
Date: Tuesday, September 24, 2013	Sheet 50 of 56	


EN resistor:
NCP81151@ 0 R
NCP5911@ 4K
PU7
NCP81151MNTBG_DFN8_2X2
PU8
NCP81151MNTBG_DFN8_2X2
PU9
NCP81151MNTBG_DFN8_2X2
FLAG
BST
PWM
EN
VCC
DRVH
SW
GND
DRVL
PR85
2.2_0603_1%
PR86
0_0805_5%
PR87
0_0402_5%
PR89
2.2_0603_1%
PR90
0_0805_5%
PR91
0_0402_5%
PR97
2.2_0603_1%
PR95
0_0805_5%
PR94
0_0402_5%
PC93
0.22U_0603_25V7K
PC102
0.22U_0603_25V7K
PC138
0.22U_0603_25V7K
PC94
2.2U_0603_6.3V6K
PC111
2.2U_0603_6.3V6K
PC143
2.2U_0603_6.3V6K
PQ11
PQ12
PQ13
PQ14
PQ15
PQ16
PQ17
PQ18
PQ19
SIR472DP-T1-GE3_POWERPAK8-5
SIRA06DP-T1-GE_POWERPAKSO-8-5
PL15
PL17
PL18
0.36UH_FDU1040J-H-R36M=P3_33A_20%
PC90
PC91
PC92
PC103
PC104
PC105
PC139
PC140
PC142
10U_0805_25V6K
PR96
4.7_1206_5%
PC95
PC112
PC141
@EMI@
1000P_0603_50V7K
+CPU_Vin
+CPU_CORE
+5VS
+12V2
65W@
[50] PWM1
[50,51] DRVON
[50] PWM2
[50] PWM3
CSN1 [50]
CSP1 [50]
CSN2 [50]
CSP2 [50]
CSN3 [50]
CSP3 [50]
PJP103
LOTES_APOW0008-P001C
HCB2012KF-121T50_0805
EMI@ PL14
EMI@ PL16
PC96
EMI@ 1000P_0402_50V7K
PC97
EMI@ 100P_0402_50V8J
PC98
EMI@ 100P_0402_50V8J
PC99
EMI@ 1000P_0402_50V7K
PC100
100U_25V_M
PC101
100U_25V_M
PC106
560U_2.5V_M
PC107
560U_2.5V_M
PC108
560U_2.5V_M
PC109
560U_2.5V_M
PC110
560U_2.5V_M
PC113
PC114
PC115
PC116
PC117
PC118
PC119
PC120
PC121
PC122
PC123
PC124
PC125
PC126
PC127
PC128
PC129
PC130
PC131
PC132
PC133
PC134
PC135
PC136
22U_0805_6.3V6M
Title
Power Stage
Size
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of
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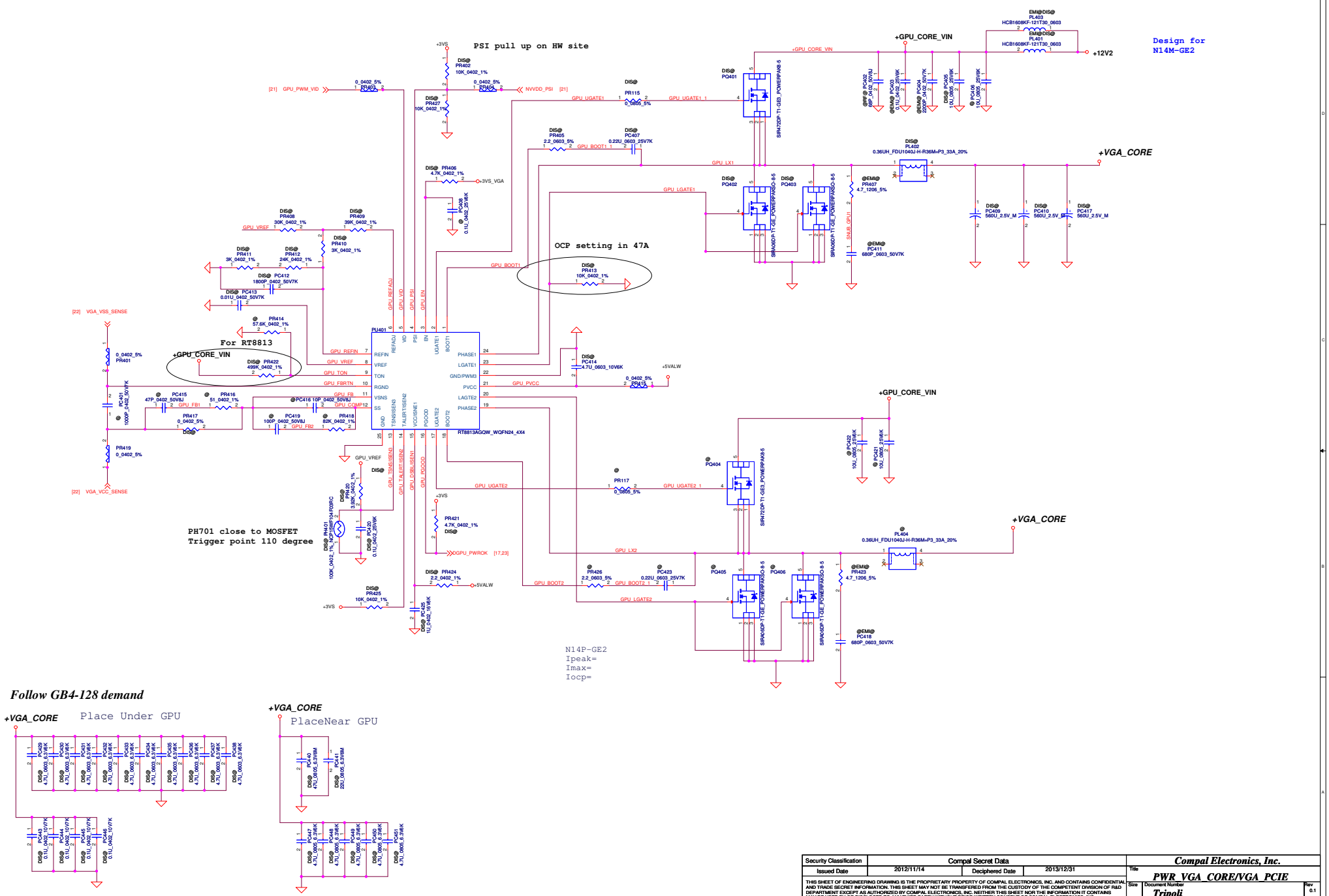

Security Classification	Compal Secret Data		
Issued Date	2012/11/14	Deciphered Date	2013/12/31

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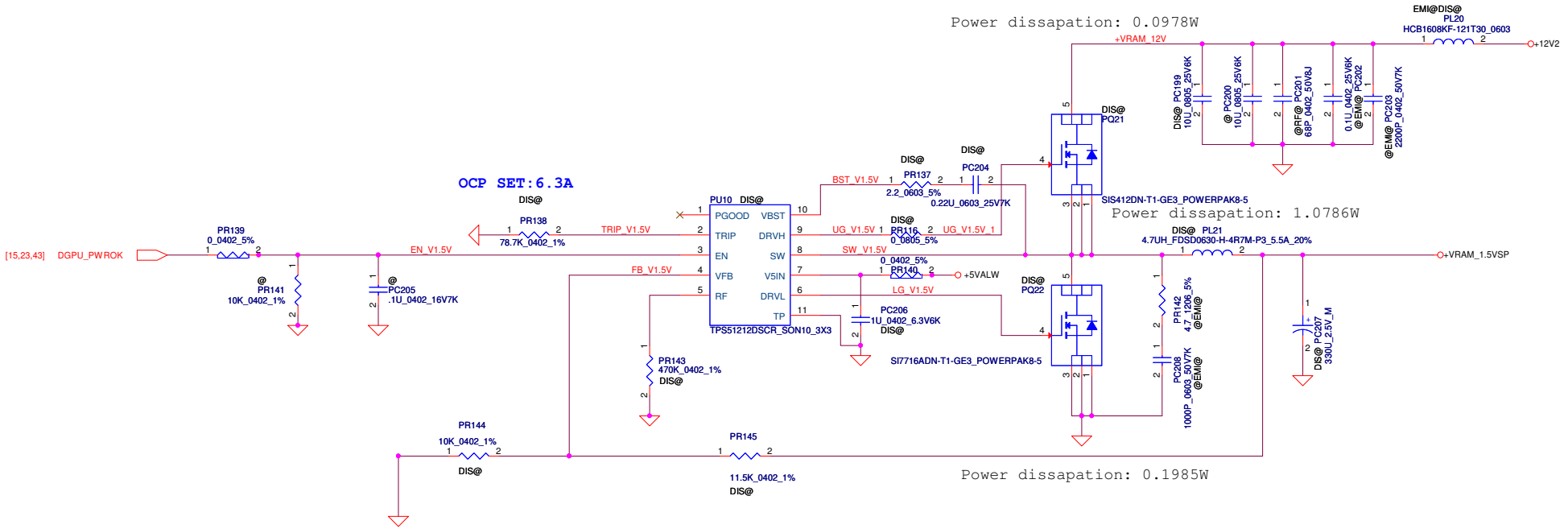
Compal Electronics, Inc.

Title: **PWR_VGA_CORE/VGA_PCIE**

Size | Document Number: **Tripoli** | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 52 of 56



Cap. ESR=17m
Rds(ON) :Max=15m-ohm
Typ=12m-ohm
Vtrip range ==> 0.2V ~ 3V
<Vo=1.5V> VFB=0.7V
V=0.7*(1+11.5K/10K)=1.505V
Fsw=290KHz

Ipeak=4.7A, Imax=3.29A, Iocp=1.2*Ipeak=5.64A

Iocp(set)=5.718A~8.304A

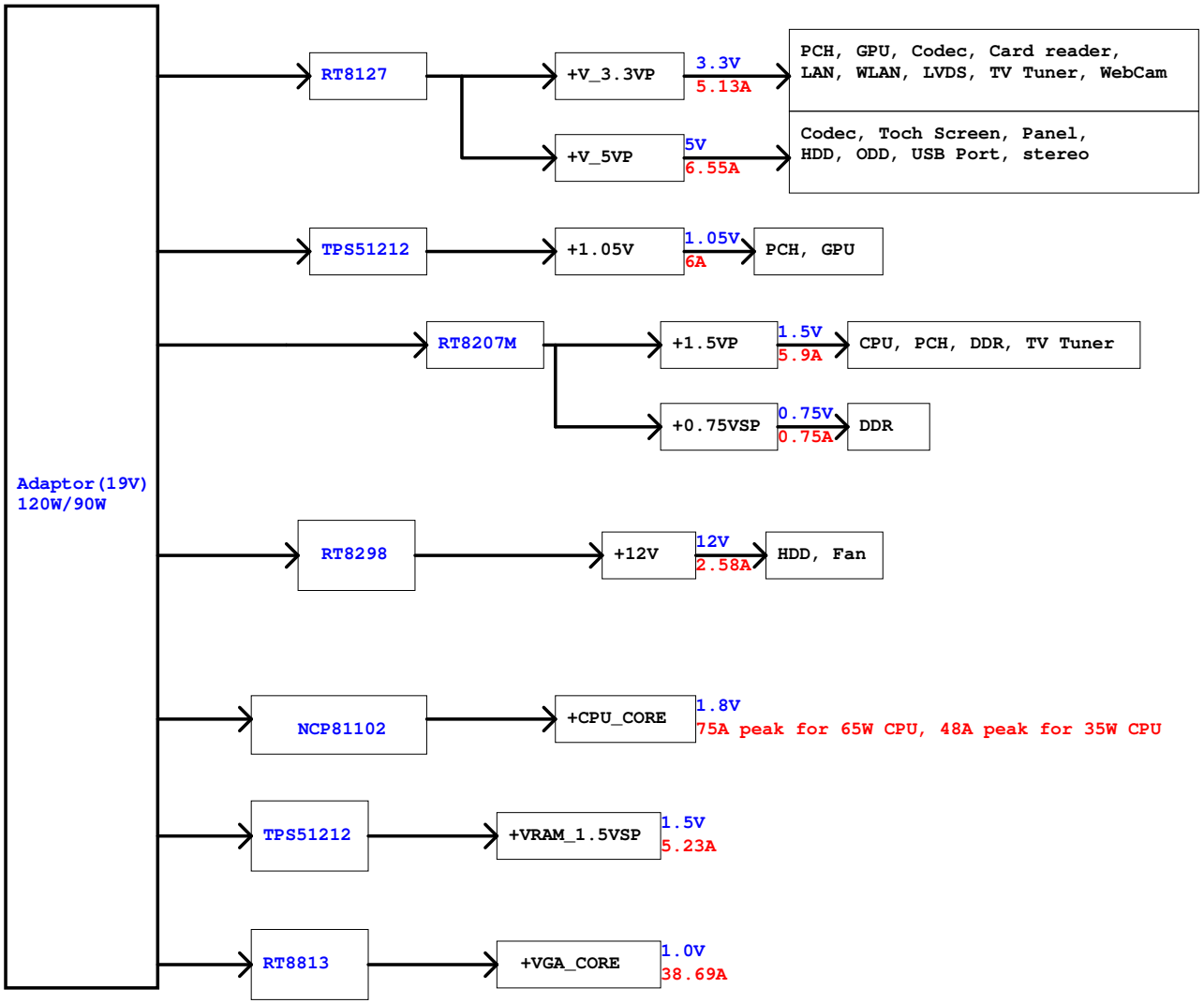
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR-VRAM_1.5VSP

Size	Document Number	Rev
Custom	VCA00 LA-9792P M/B	0.1

Date: Tuesday, September 24, 2013 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

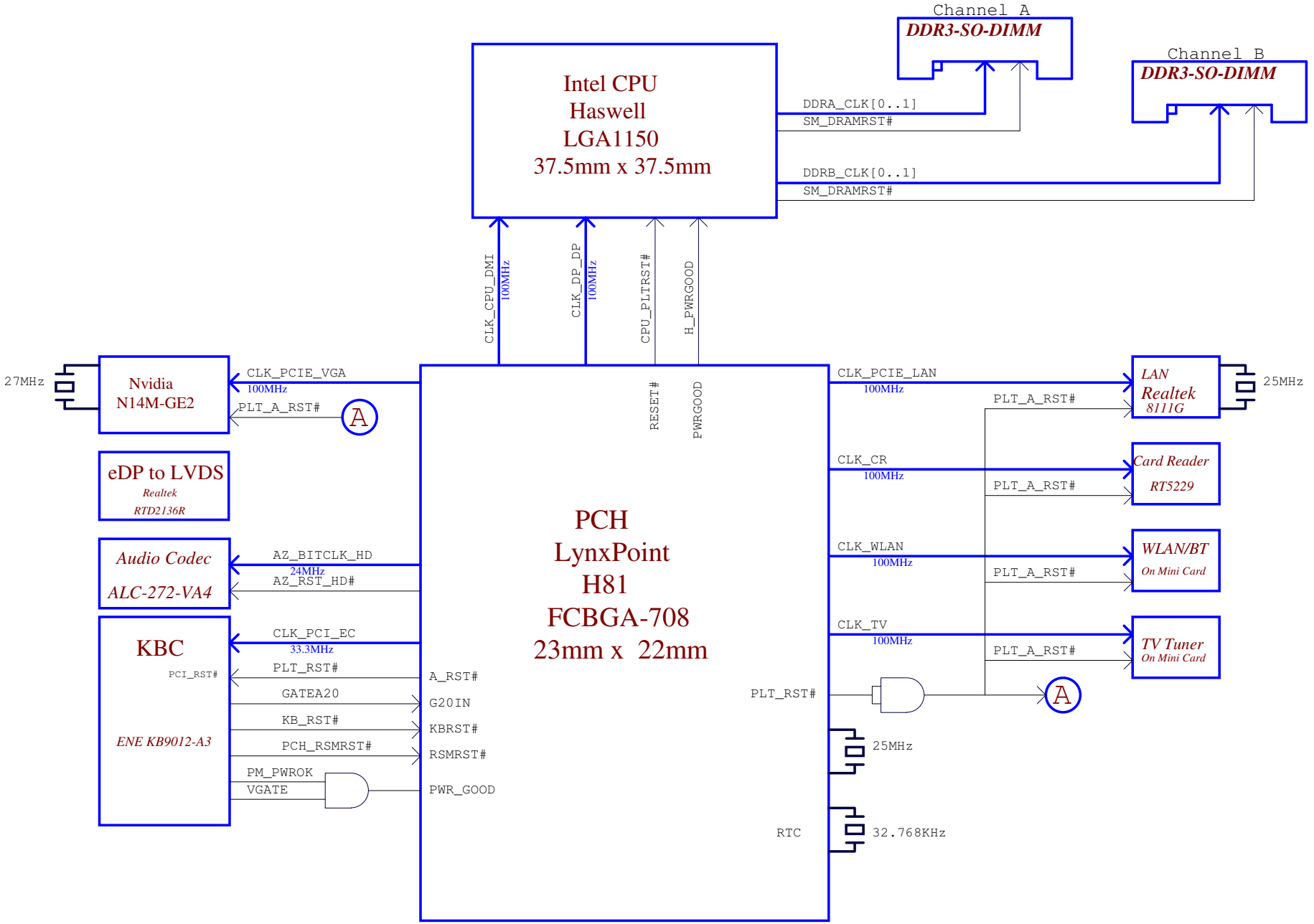
Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: QLA13/15 LA-8501P M/B | Rev: 0.4

Date: Tuesday, September 24, 2013 | Sheet 55 of 59

Clock and Reset Diagram



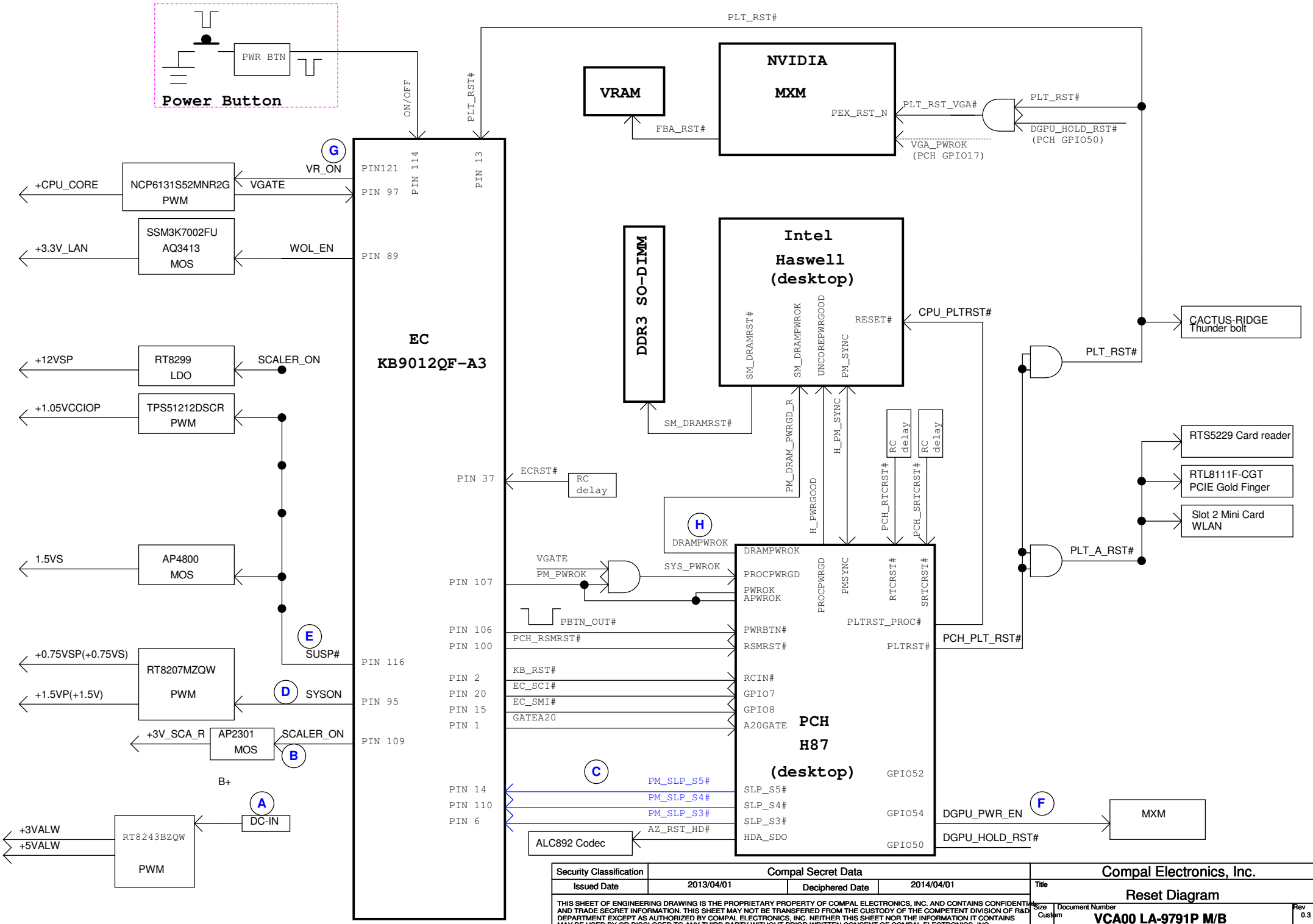
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Clock/Reset Diagram

Size: Custom | Document Number: VIA15 LA-A071P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 56 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Reset Diagram

Size	Document Number	Rev
Custom	VCA00 LA-9791P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 57 of 59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20130604	P47	Add PC154 and Change the part number is SA00005A600	
2.	20130729	P45	Add PR105 ,PC155 Snaber	For EMI Request
3.	20130729 Add PR1	P45		For EMI Request
3.	20130729 Add PR39	P45		For S5 power loss issue

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/09/12	Deciphered Date	2012/09/12

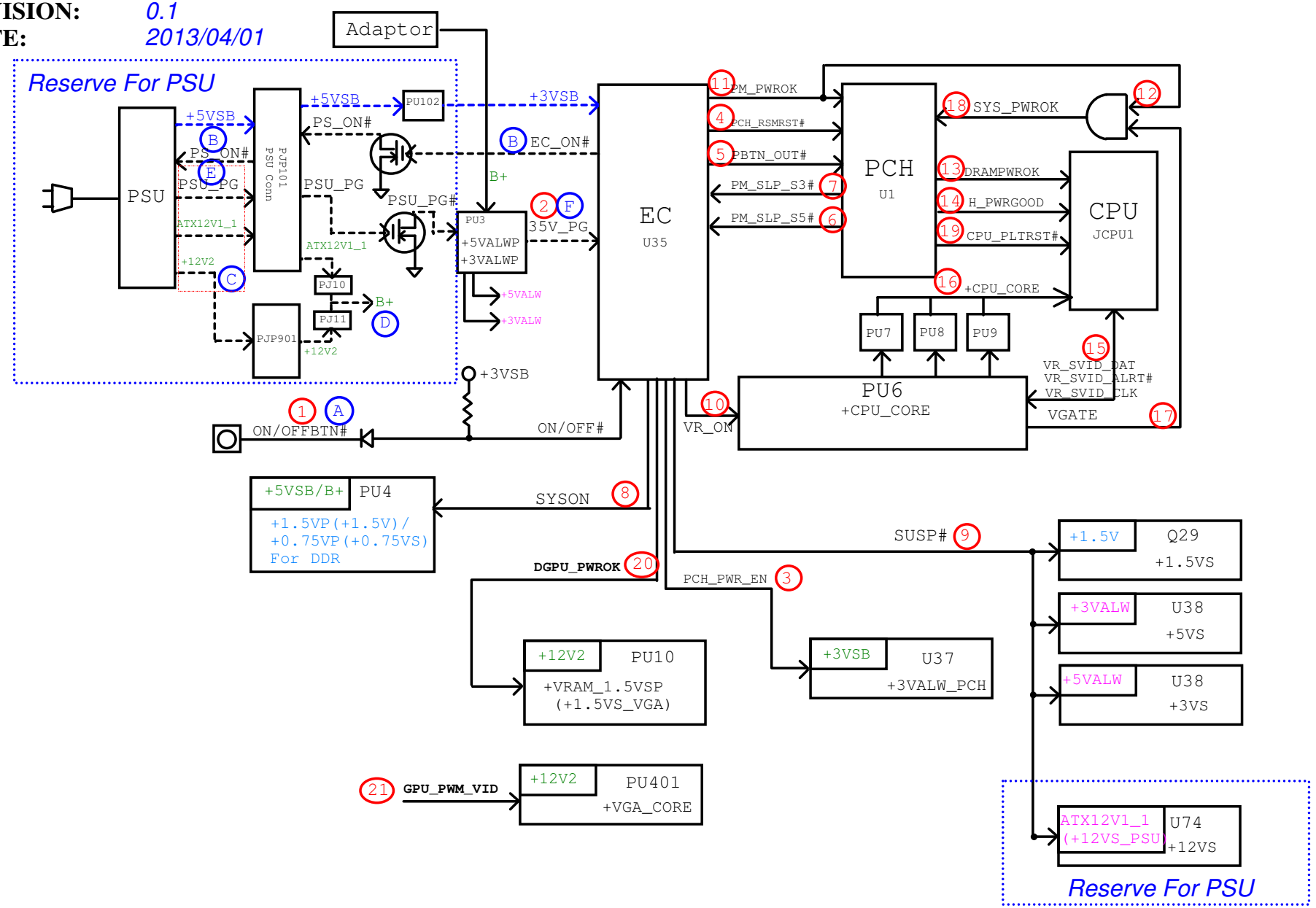
Title: PWR_PIR

Size	Document Number	Rev
Custom	B555 VAA15 LA-A072P MB	0.5

Date: Tuesday, September 24, 2013 Sheet 57 of 60

COMPAL CONFIDENTIAL

MODEL NAME: *ZEA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA-A061P*
REVISION: *0.1*
DATE: *2013/04/01*



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date	2014/04/01
Title	Power Sequence Diagram		
Size: B/26 Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 58 of 59		

HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 --> 0.2
GERBER-OUT DATE: 2013/06/20

NO DATE PAGE MODIFICATION LIST PURPOSE

1. Change C45 from SF000002V00 to SF000003X00
2. Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.
3. ~~Change LCD_BKOFF# control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.~~
4. Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.
5. Pop R428 for AZ_SDIN0_HD.
6. U2 footprint change from socket to IC.
7. Add RH11
8. Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF
9. Change R423 location to L45
10. Change D7 from SC2N202U010 to SC600000B00 for 雹
11. Change Q29 from SB548000210 to SB00000ZN00.
12. Change D8&D9 from SCS00002G00 to SCS00000Z00
13. X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000EO00. 2.Change Q9 from SB934130020 to SB934130000.
    3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.
14. Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.
15. Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).
16. Change Q10 from SB00000FC00 to SB00000L800 for 雹
17. Remove R469 0ohm for TV.
18. Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.
19. Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.
20. Pop U7&R231, un-pop R228 for PLT_RST_VGA#.
21. Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.
22. Un-pop LAN power components Q26,Q27,R573,R574,C562.
23.0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647
24.Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.
25.Pop R438,R439 for ESD request.

PVT change list:
1. Change Q10 from SB00000FC00(EOL soon) to SB00000ZN00(同Q29),SB00000FC00 as 2nd source.Schematic,體
2. Change U23 pin12_+USB3_VCCA to +USB3_VCCB, pop U22, un-pop U24 for USB charger
3. R365 change from short pad to 0ohm.
4. U5 pin5 change from +3VSto +3VALW_PCH for BCM43142 wake from WLAN issue.
5. Change R473,R490,R677,R678,R679 from SP040005X00_0603 size to F1,F2,F4,F5,F3 SP040003S00_1206 size.
6. Change L11 from SM010014520 to SM01000EJ00 for ACL request
7. Change L8 from SM010007W00 to SM010019400 for ACL request
8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
11. Change R276 from 10k to 100k for +3VS_VGA rise time.
12. Change R672 from 10k to 100k for +3VALW_PCH rise time.
14. Change R438 & R439 from 0_0603 to short pad.
15. Un-pop C125 & C548 for sequence EA.
16. Change C394, C398,C520 & C514 from 220uF(LELON_SF000001F00) to 100uF (Panasonic_SF000005100) to meet Inrush EA & ACL request.
17. Change C170 & C171 from 12pF to 10pF for EA.
20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
21. Add R677 & reserve R678 on U5 AND gate for PLT_A_RST#
13. Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.
22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
10. Add C2144~C2152 for EMI request.
18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

pre-MP change list:
1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.
2. Add C2157 and reserve C2158.
3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.
4. Un-pop JECDB1 & SW1.
5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
6. Change C520 & C514 from 100uF to 220uF.
7. Pop C2149~C2152 for ESD request.
8. Change C559 & C2128 from 0603 to 0805.
9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.
10. Add C418 for EMI.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date 2014/04/01	Title: HW-PIR
Size	Document Number: VCA00 LA-9791P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 59 of 59		