

MODEL NAME : ZAL00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WW000 LA-A491P M/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT OAK Mainstream2 UMA/DIS AMD Venus Pro

2013-05-15 Rev: 0.3

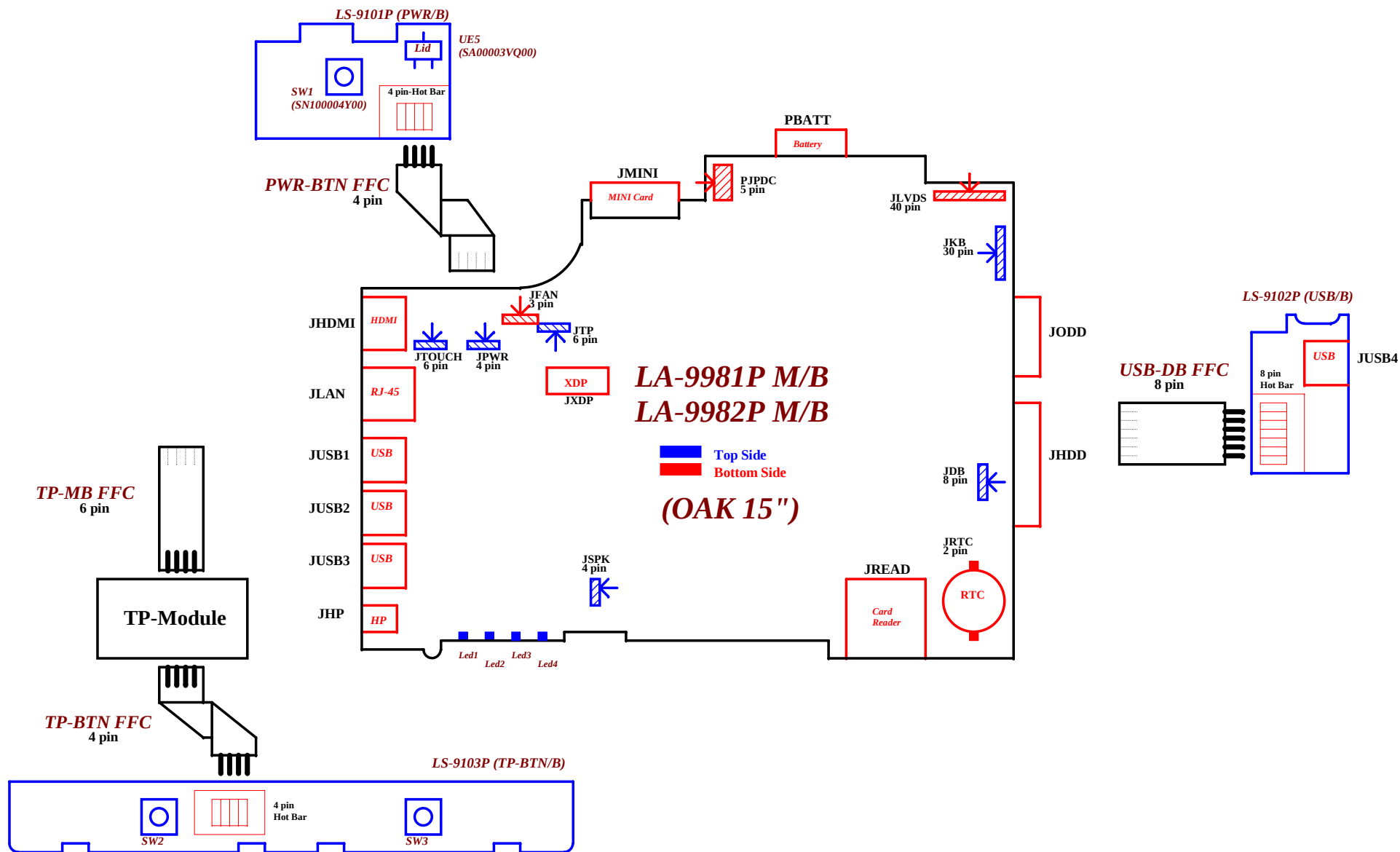
X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS VENUS : VENUS@,DIS@,EMI@,ESD@,RF@,XDP@



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Issued Date	2013/04/01	Deciphered Date	2014/05/01	Title	Cover Page
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Compal Confidential
Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

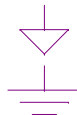
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0
16				

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

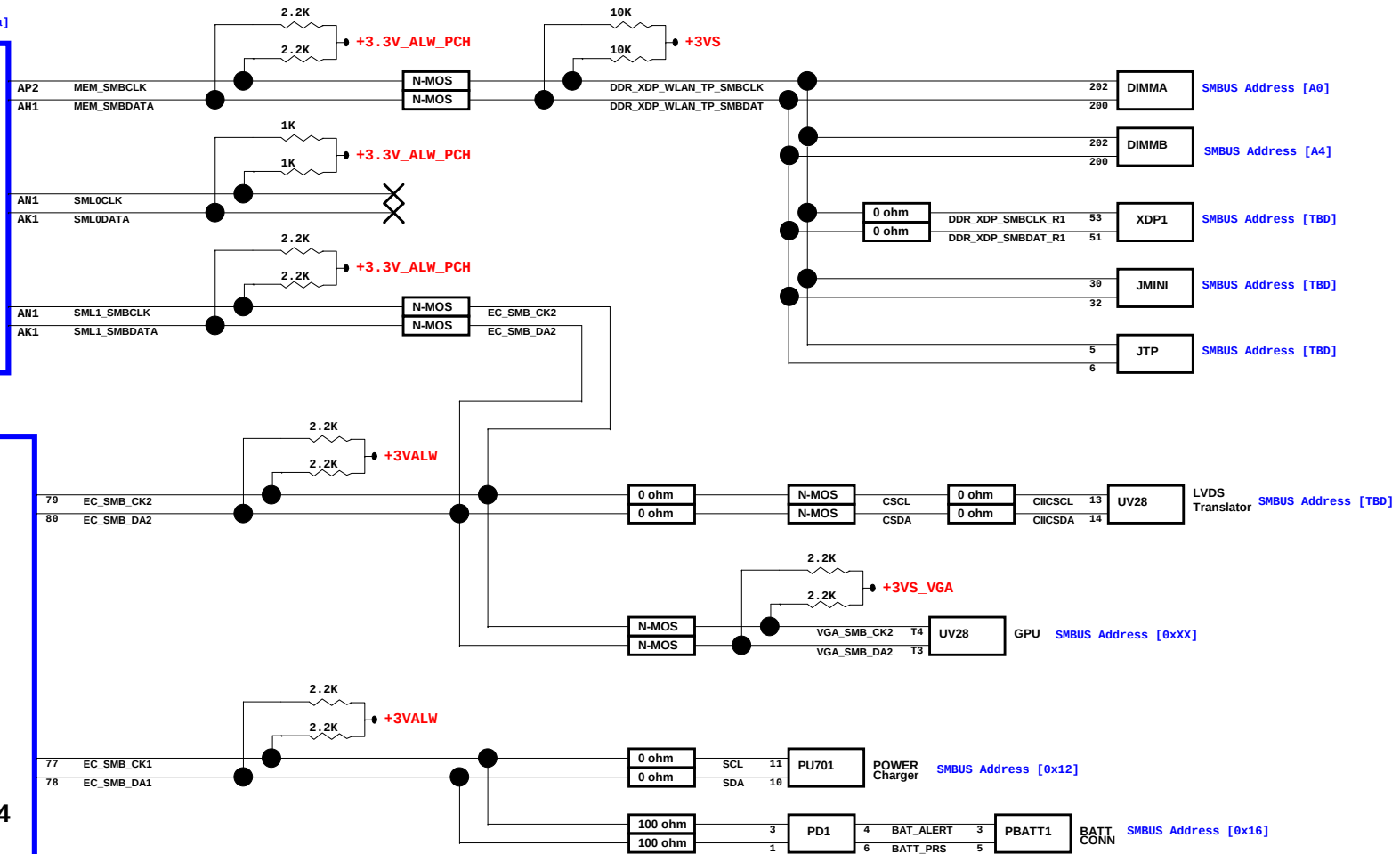
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

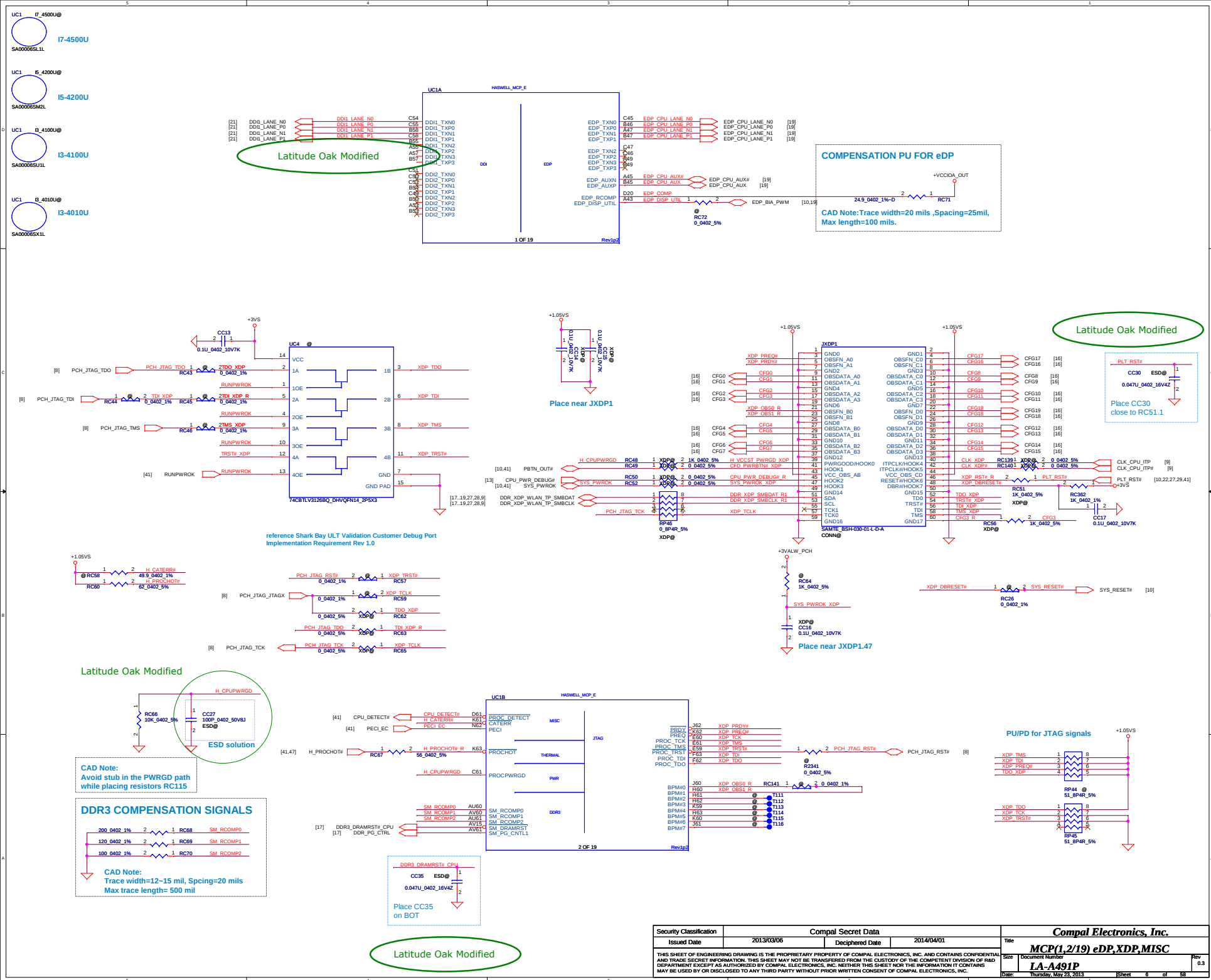
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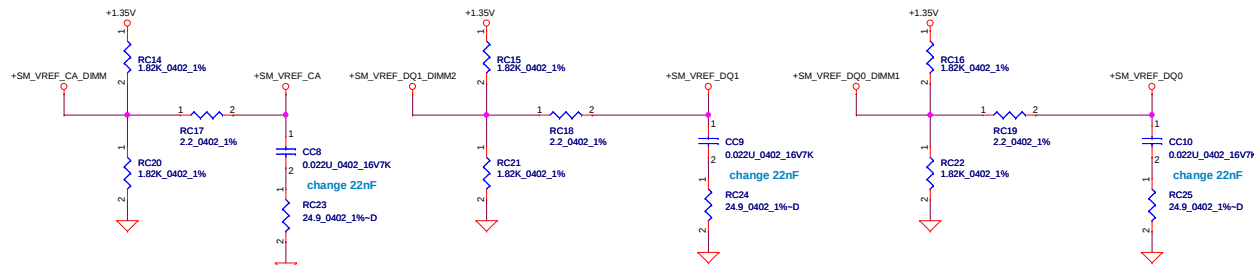
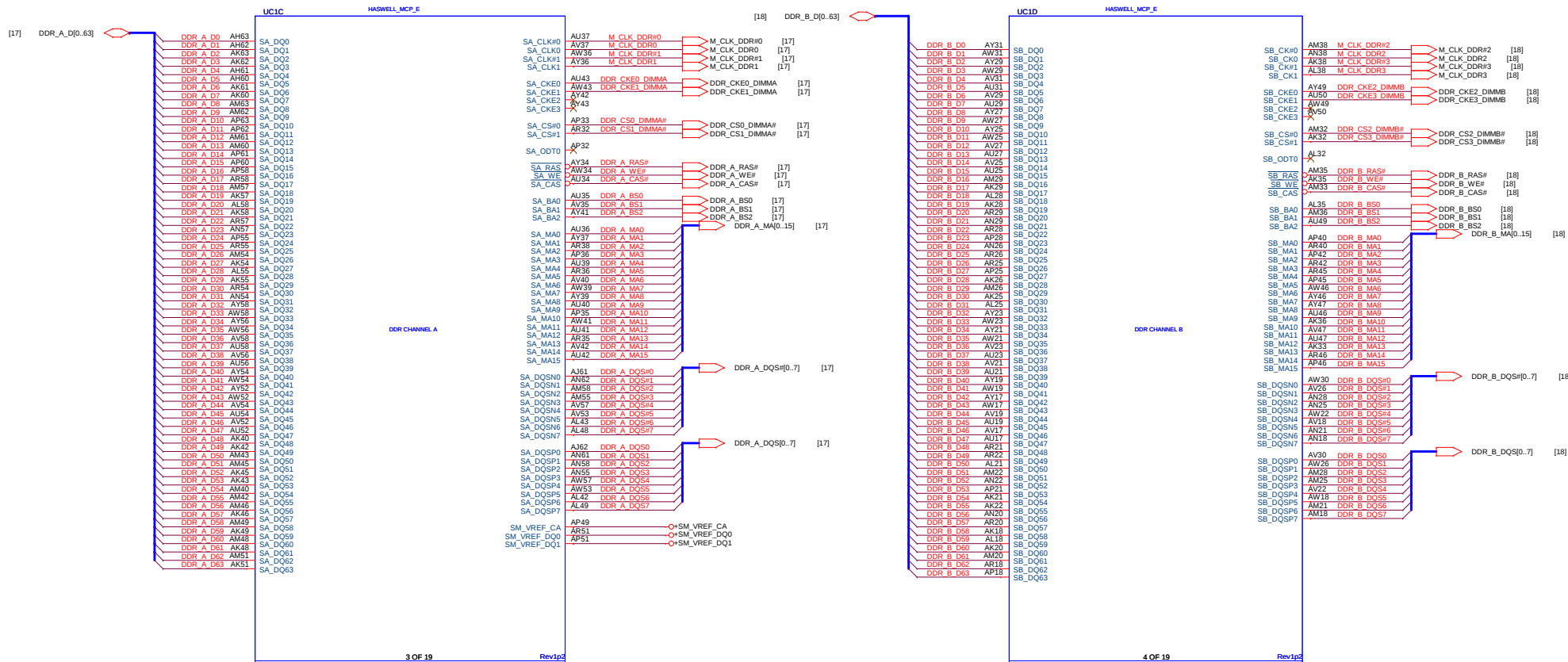
SMBUS Address [0x9a]

MCH
Shark bay

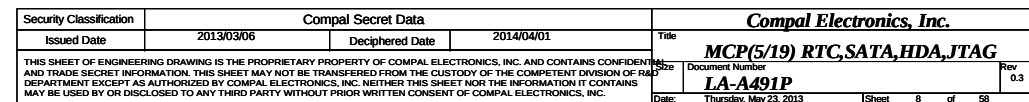
KBC
KB9012A4





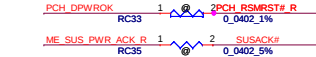
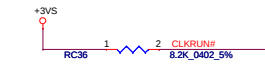
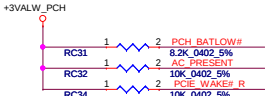
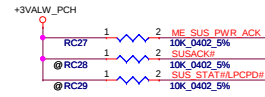


Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/06	Deciphered Date	2014/04/01	MCP(3,4/19) DDR3	
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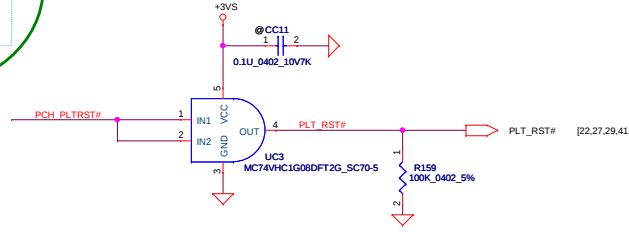


Latitude Oak Modified

PCH_PLTRST#
CC33 ESD@
0.047U_0402_16V4Z
Place CC33 close to UC3.1 & UC3.2



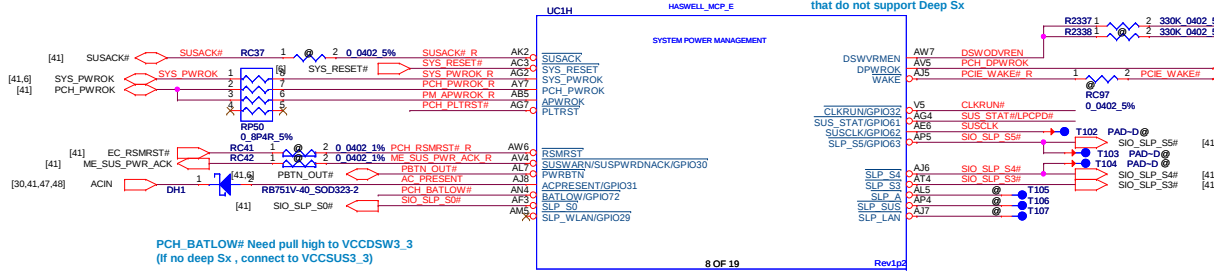
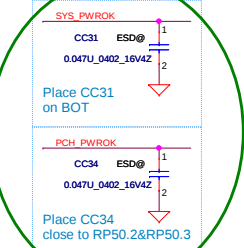
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC, if not support Deep Sx



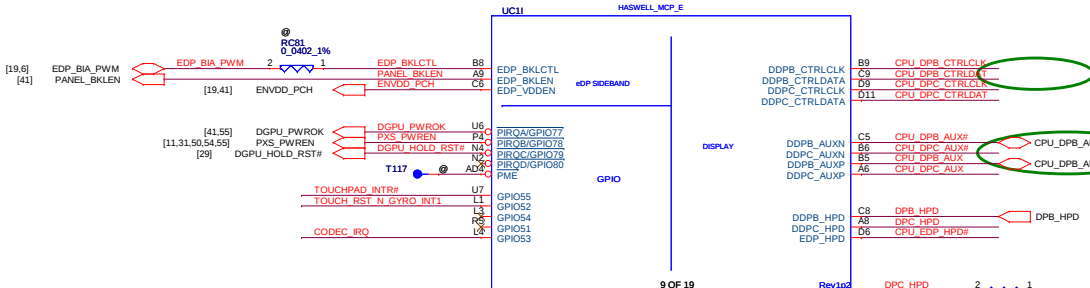
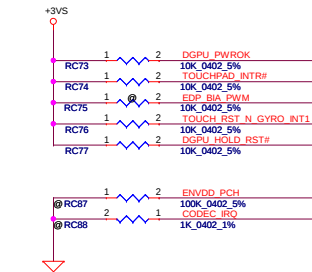
DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED(DEFAULT)
LOW = DISABLED

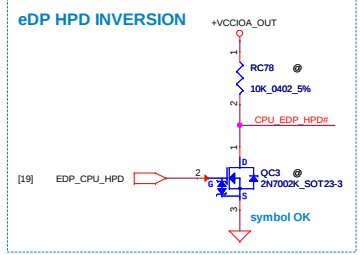
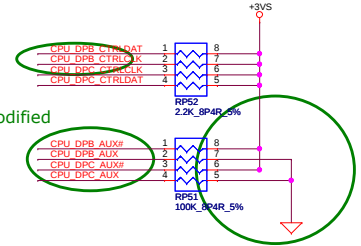
Latitude Oak Modified



PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx, connect to VCCSUS3_3)



Latitude Oak Modified



EDP_CPU_HPD Reserve for eDP

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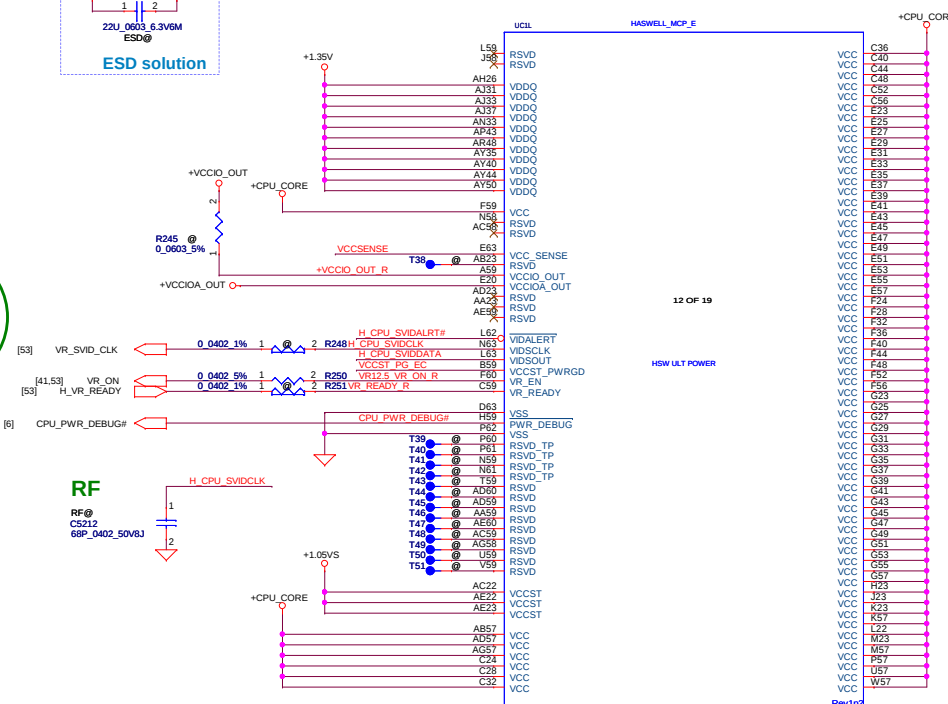
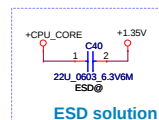
VCCST_PG_EC

C95 ESD@

220P_0402_50V8J

Place C95
between R286 and UC1.

Latitude Oak Modified



SVID ALERT

Diagram illustrating the SVID ALERT circuit. The circuit includes a +1.05VS supply connected to a resistor R252 (75_0402_5%) and a pull-up resistor R254 (43_0402_1%). The output of the circuit is labeled VR_SVID_ALERT# and is connected to the H_CPU_SVIDALRT# pin of the CPU. A note indicates: "Place the PU resistors close to CPU".

SVID_DAT need to pull-up double side (PWR_VR & CPU)

Place the PU resistors close to CPU

R256 130_0402_1%

R257 0_0402_1%

H_CPU_SVIDDATA

[53] VR_SVID_DAT

```
graph LR
    VR_SVID_DAT[VR_SVID_DAT] --- R257[R257 0_0402_1%] --- H_CPU_SVIDDATA[H_CPU_SVIDDATA]
    H_CPU_SVIDDATA --- R256[R256 130_0402_1%] --- GND[Ground]
```

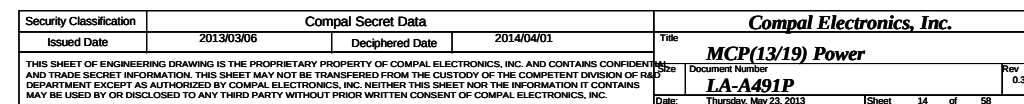
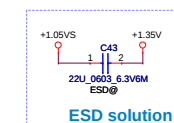
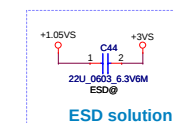
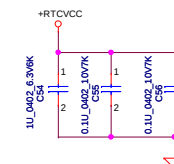
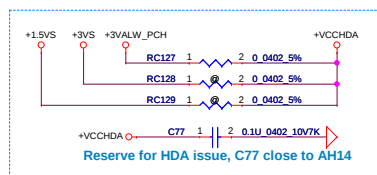
RF®
C5212
68P_0402_50V8J

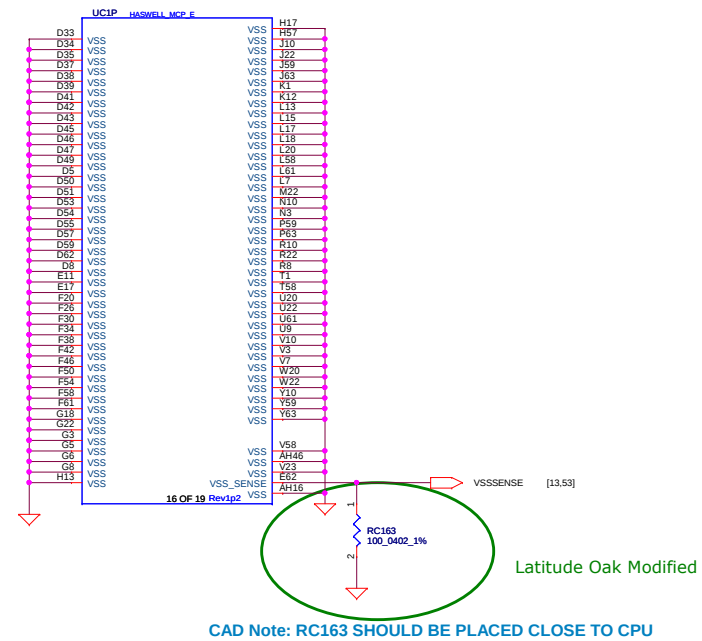
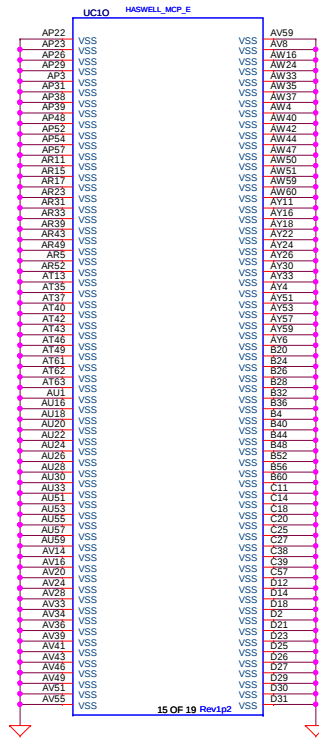
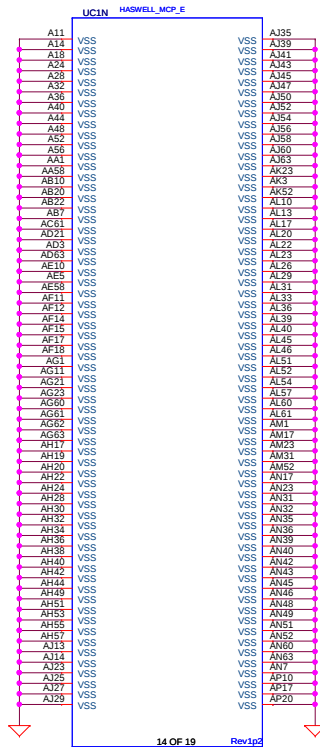
R253
INTEL Check list , XDP use only

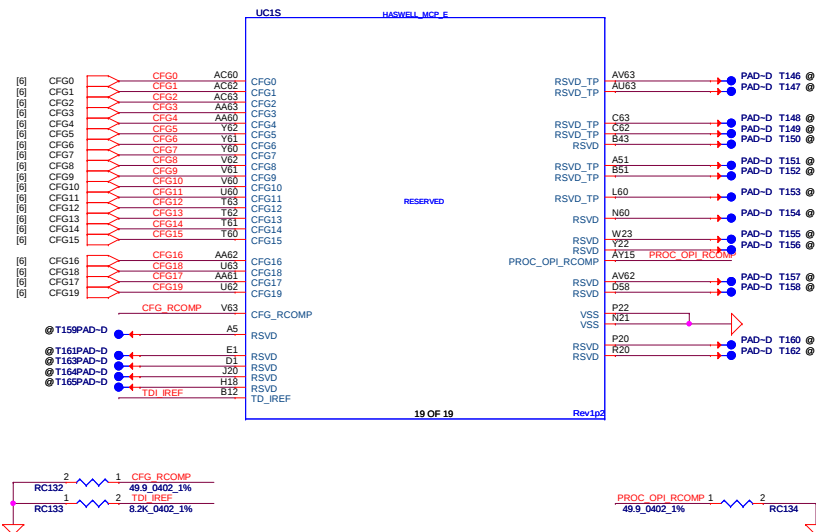
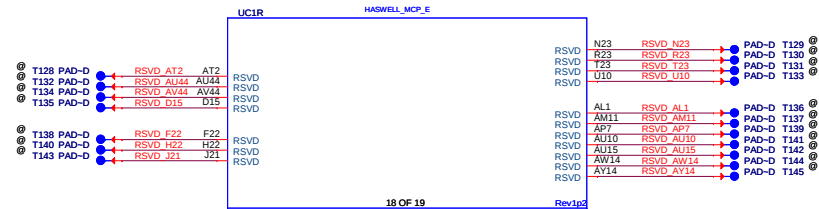
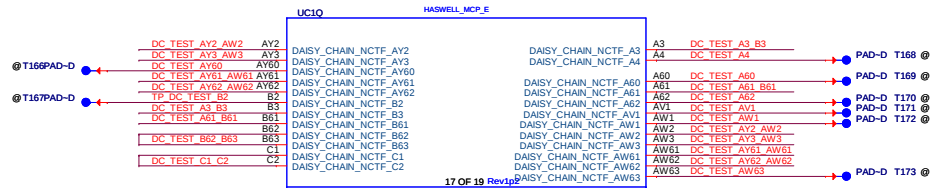
**+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4**

CAD Note: PD resistor on HW side

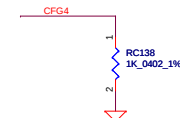
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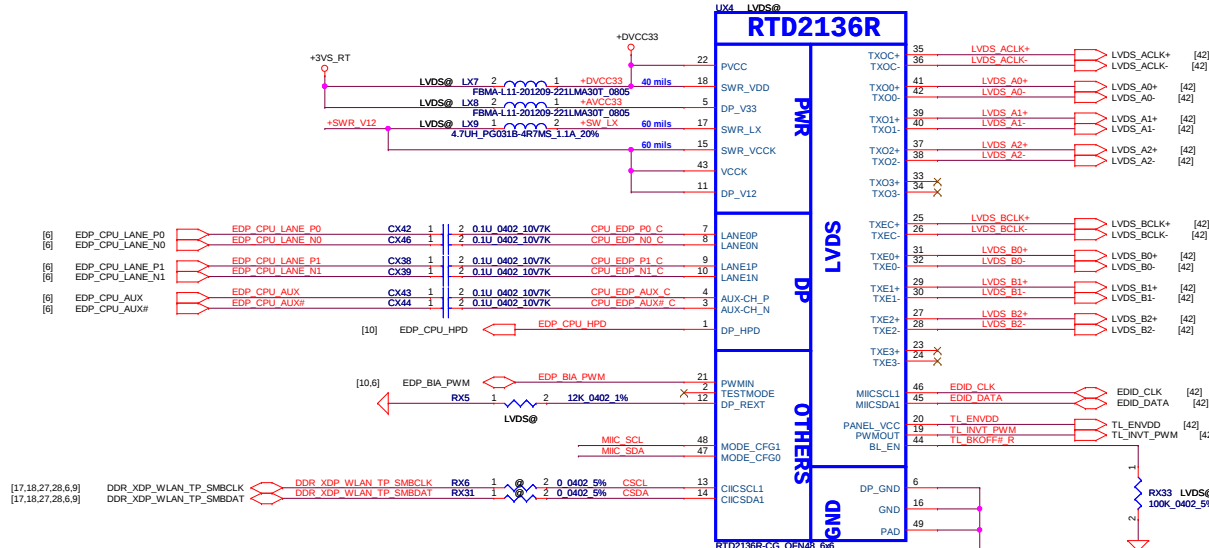
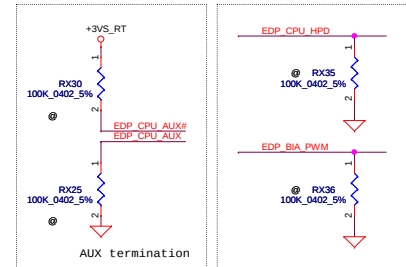
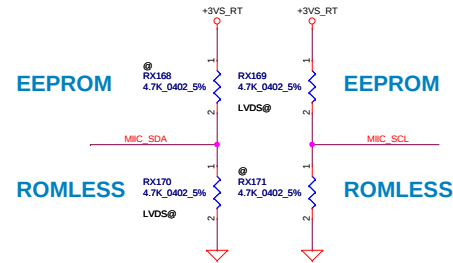
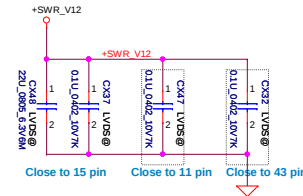
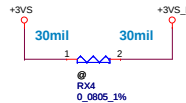
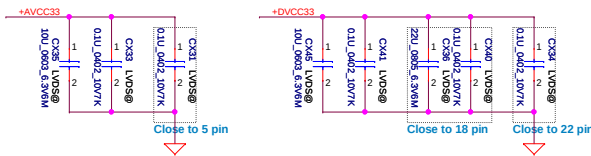




CFG STRAPS for CPU

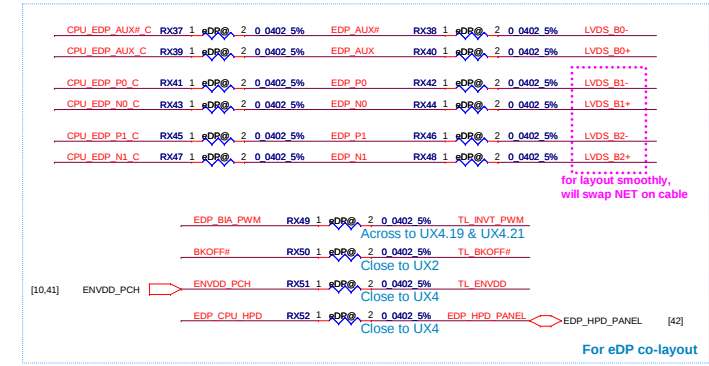
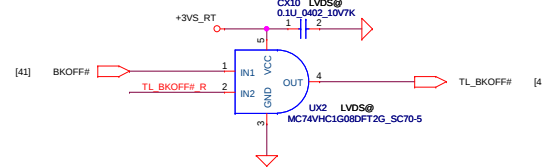


Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

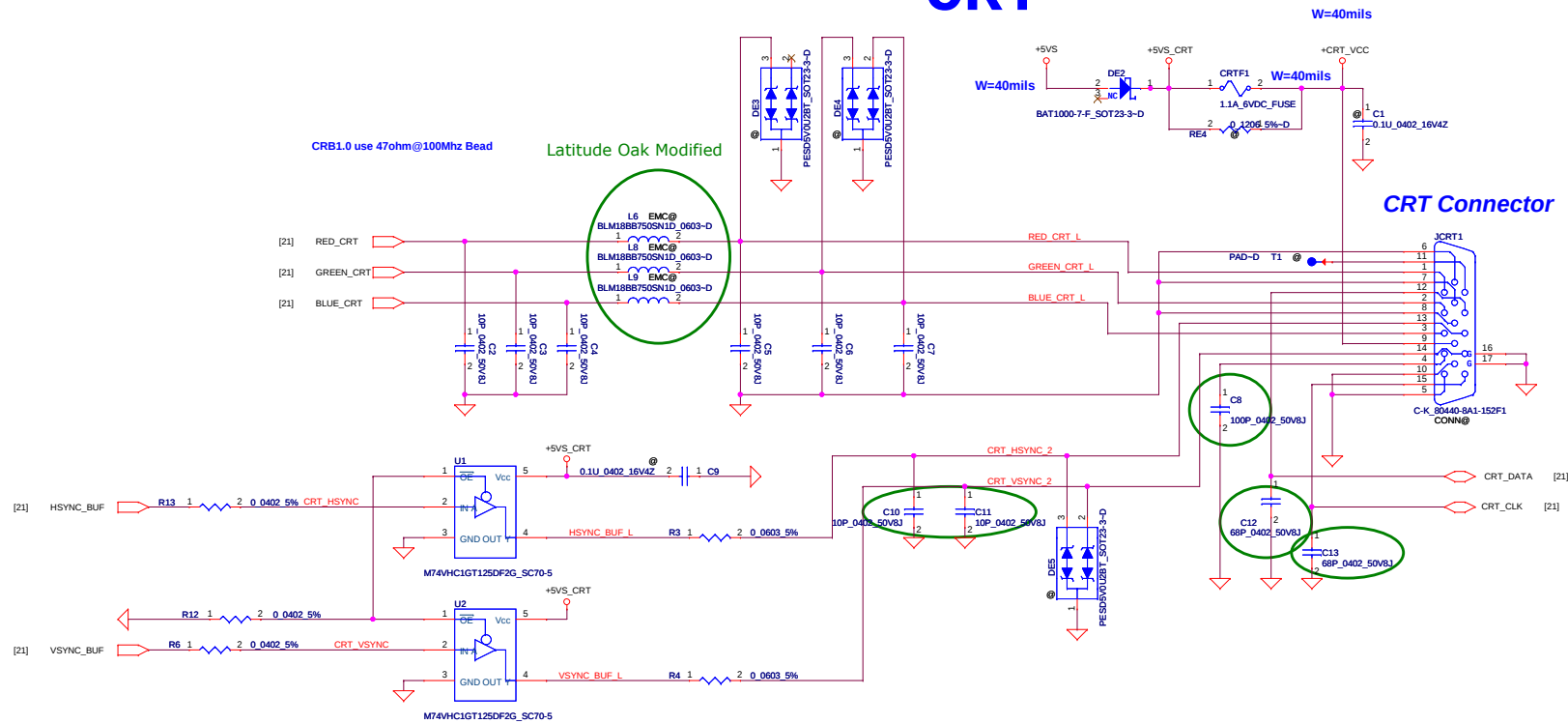


RTD2136S : SA00004NW10
RTD2136R : SA000067100

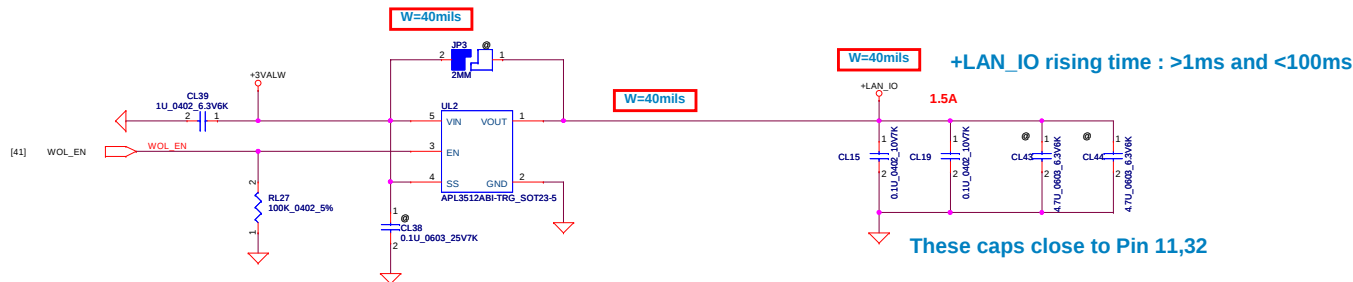
Vendor advise reserve it



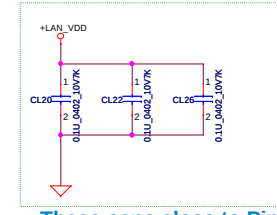
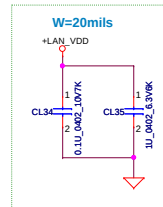
CRT



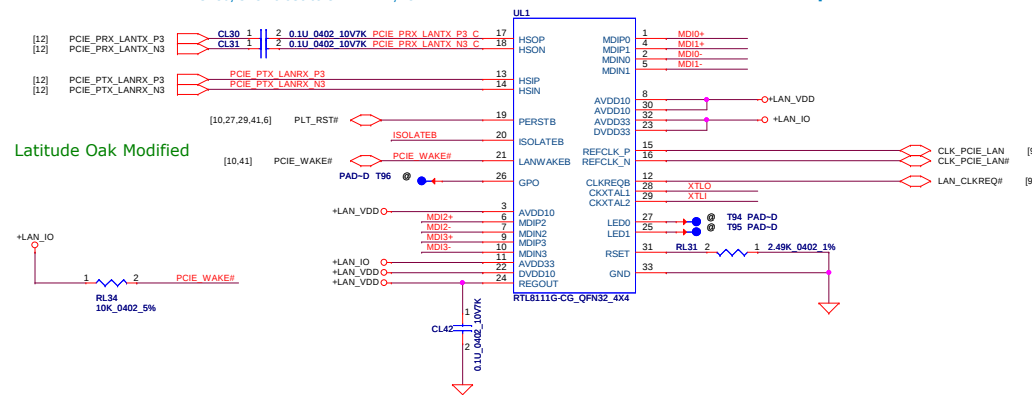
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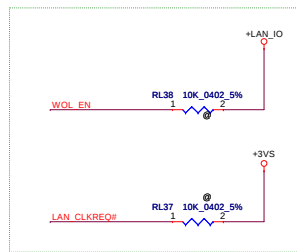
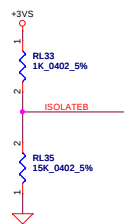
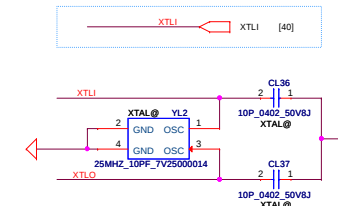
Latitude Oak Modified



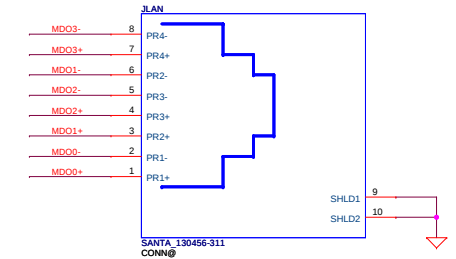
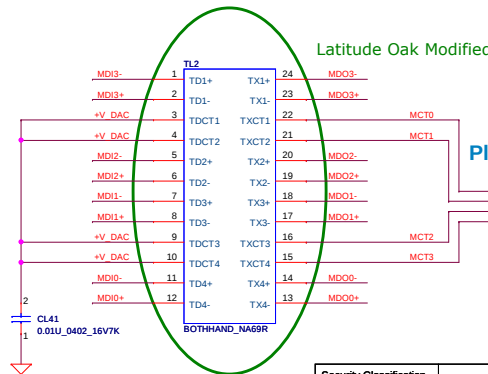
CL30, CL31 close to UL1 Pin 17, 18



For GCLK



Reserve 10K pull

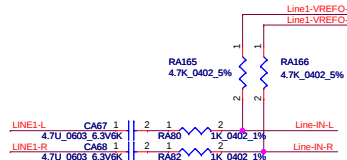
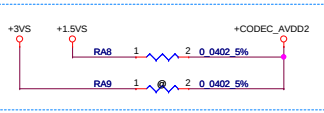


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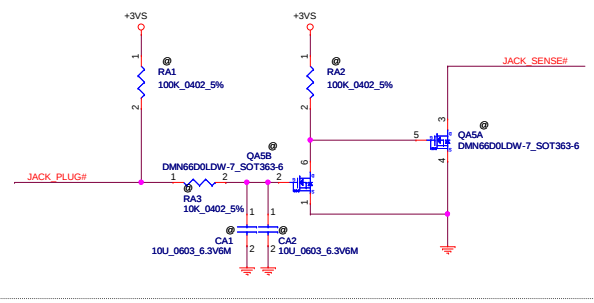
CA53, CA55 change Value
from 100U_0603_6.3V6K~D to
4.7U_0603_6.3V6K

CA71, CA51 place close to Pin 26

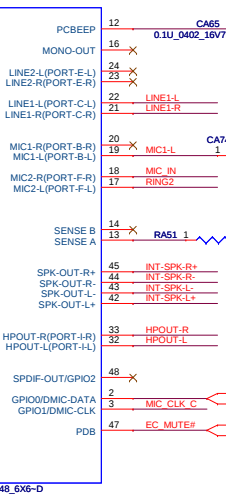
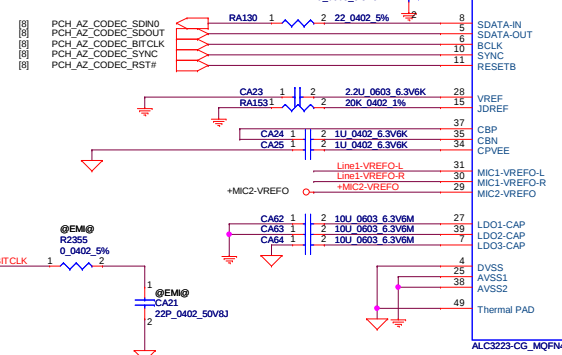
Reserve for HDA issue



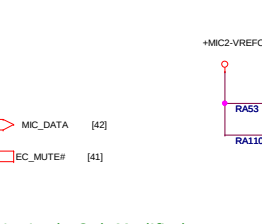
JACK_PLUG Delay circuitis



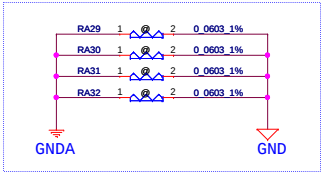
CA57,CA58 close
to UA1 pin1



RA51, RA33 place close to UA1

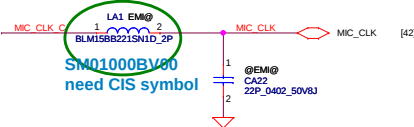


Reserve for cancel Delay circuitis

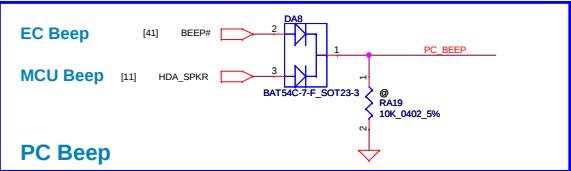


Place on the moat between GND & GNDA.

Latitude Oak Modified



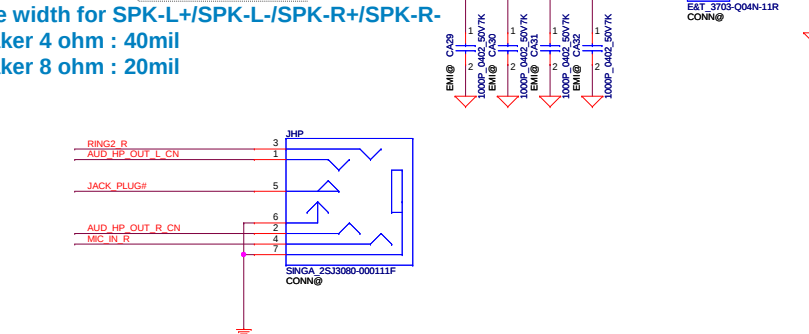
SM01000BV00
need CIS symbol



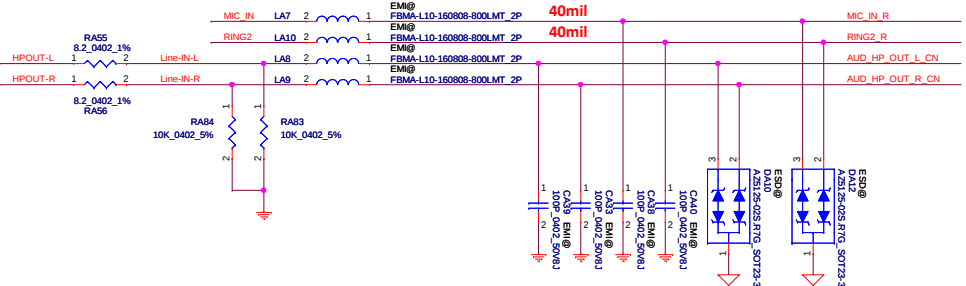
Close to UA1
Pin11,13,14,16



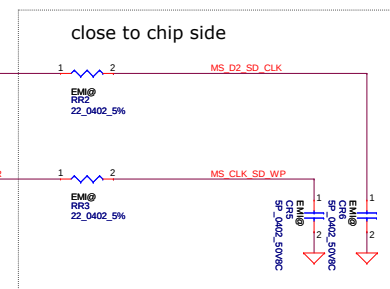
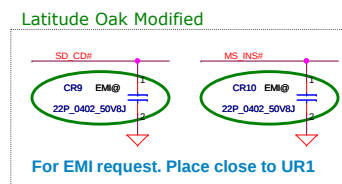
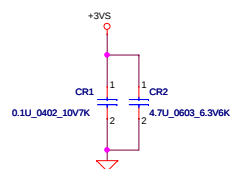
close to Codec



iPhone and Nokia type Combo Jack

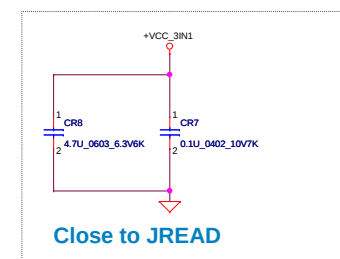


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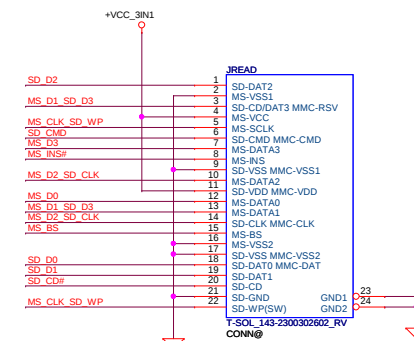
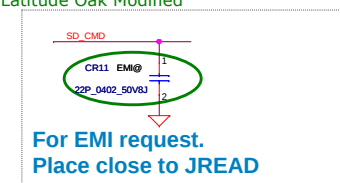


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

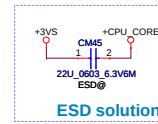
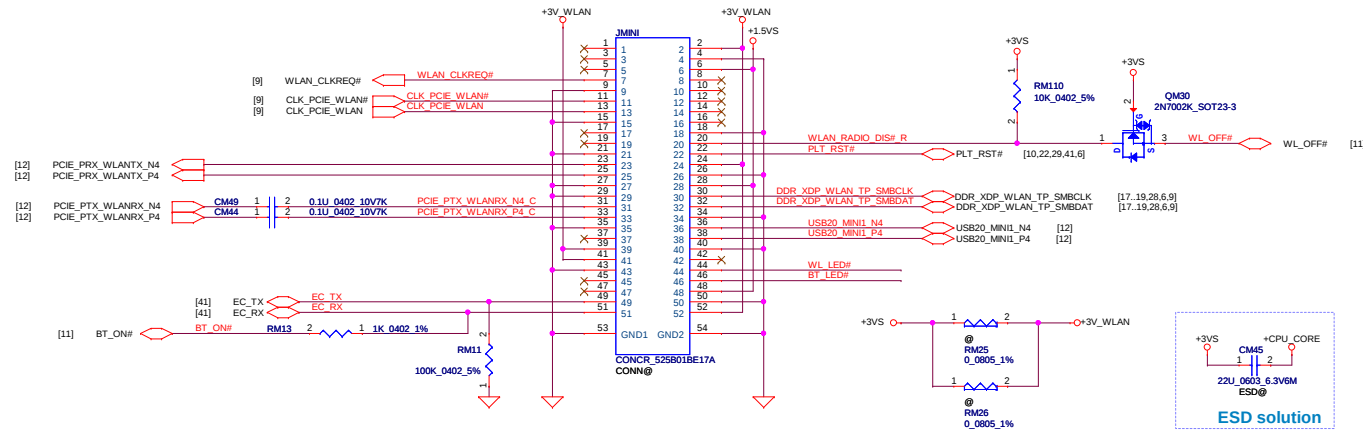
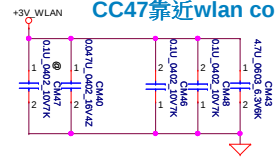


Latitude Oak Modified

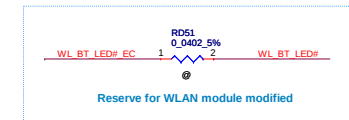
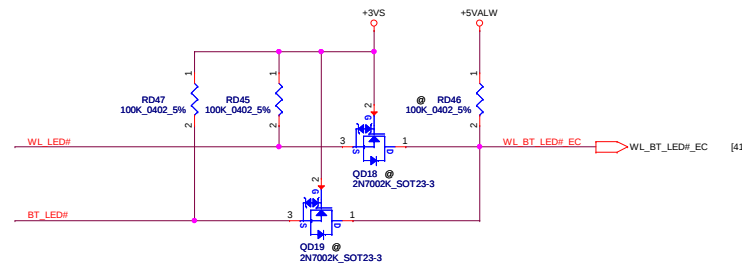
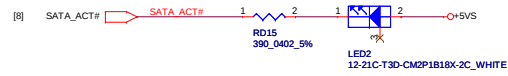


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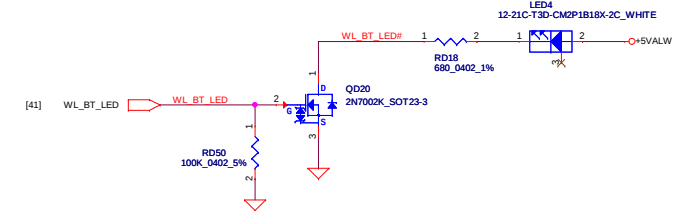
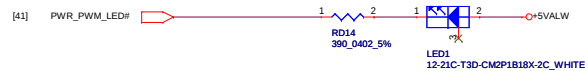
CC47靠近wlan connector



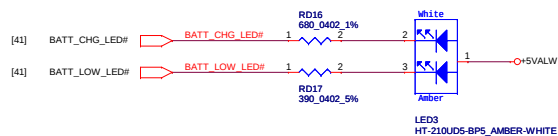
10mils, All pins



Wireless LED

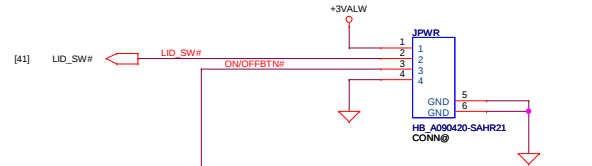


The schematic diagram shows the LED driver circuit for the WLAN module. It includes a 3V5V power source, a CD63 0.1uF 0402 10V7K capacitor, a UD1 MCT4VHC1G08DFT2G_SCT0-5 diode, and an RD52 100K_0402_5% resistor. The LED is connected to the output of the driver circuit.



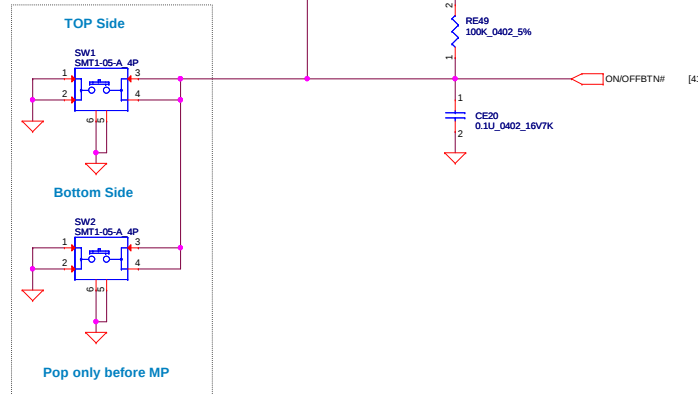
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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	Mini Card/LED
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POWER/B

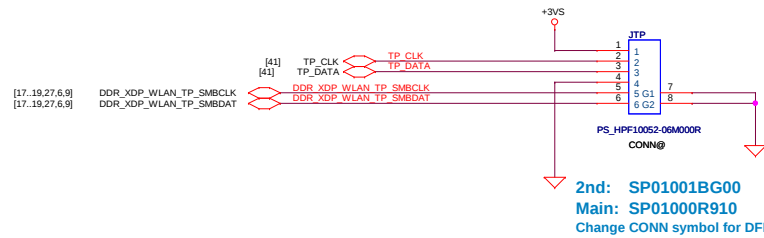


Power ON Circuit

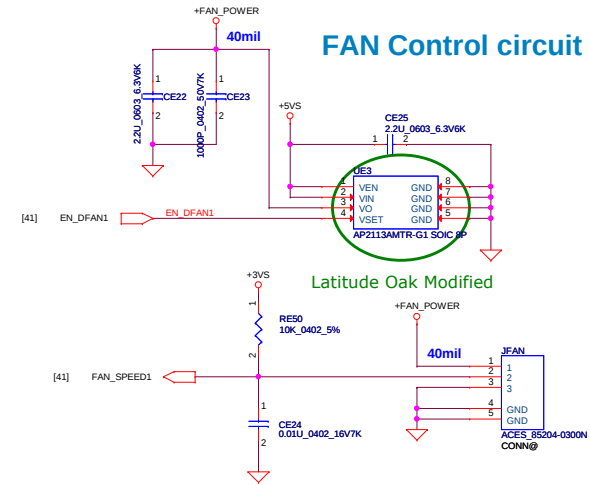
ON/OFF switch



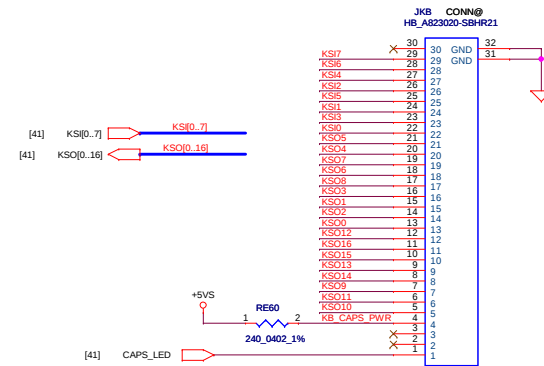
Touch pad



FAN Control circuit

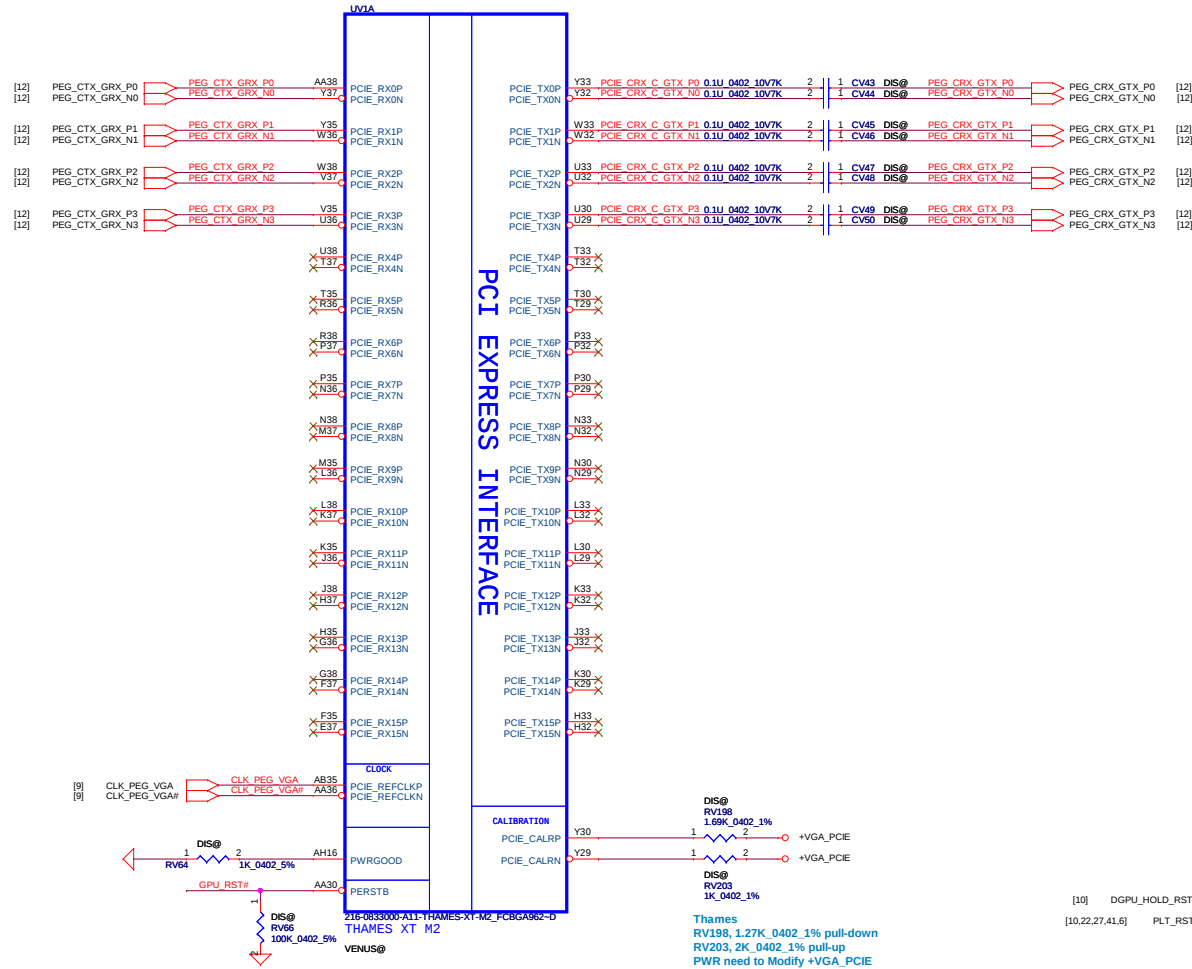


INT_KBD Connector

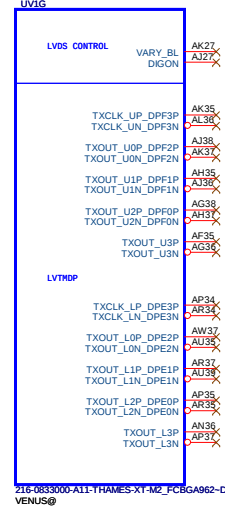


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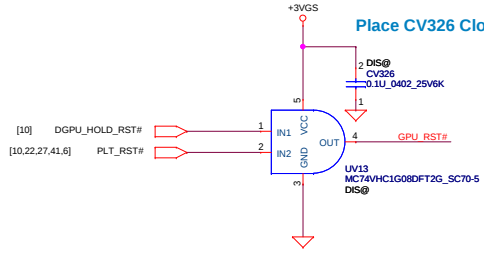
GFX PCIE LANE REVERSAL

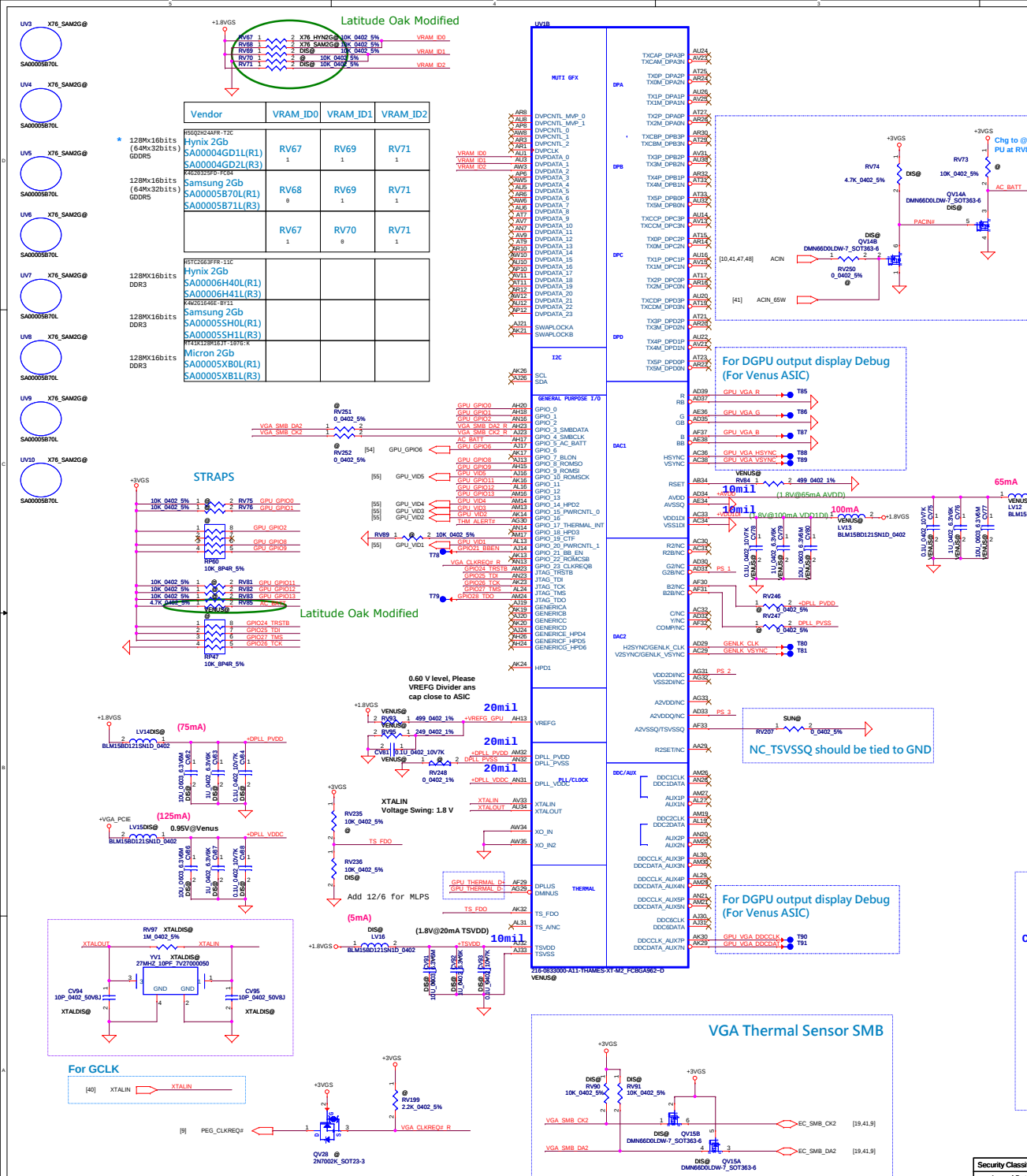


LVDS Interface

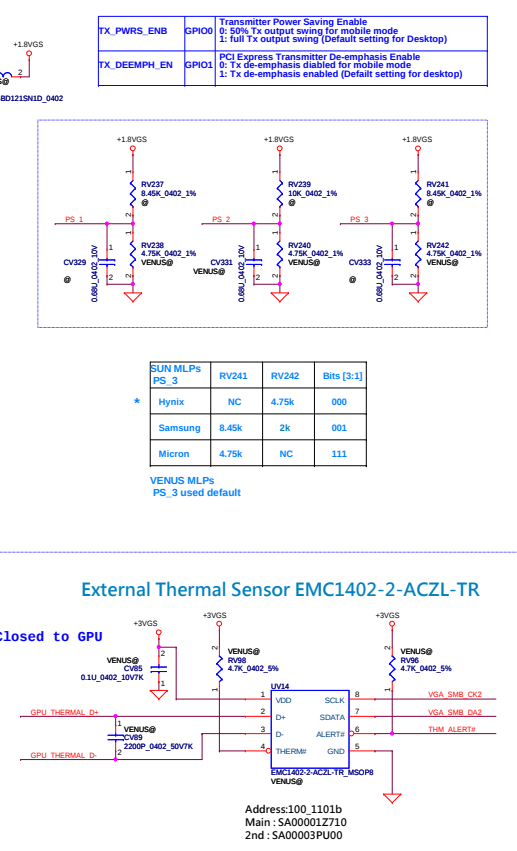


Place CV326 Close to UV13





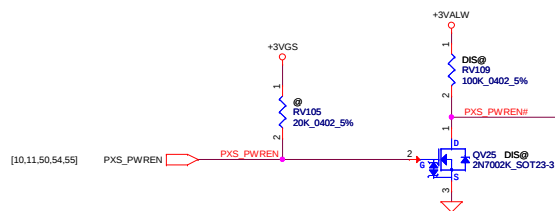
CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE	
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS	
TX_PWRS_ENB	GPIO0	PCI FULL TX OUTPUT SWING	0: 50% swing 1: full swing	X	
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X	
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5G/s 1: 5G/s	0	
RSVD	GPIO8	RESERVED		0	
BIF_VGA_DIS	GPIO9	VGA ENABLED		0	
RSVD	GPIO21	RESERVED		0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X	
ROMDCFG(2:0)	GPIO[3:1:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX	
VP_DEVICE_STRAP_SNA	V2SYNC	IGNORE VIP DEVICE STRAPS		0	
RSVD	H2SYNC			0	
RSVD	GENERICC			0	
AUD[1]	HSYNC	AUD[1] AUD[0] 0: No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 2 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI		11	
AUD[0]	VSYSNC				
AMD RESERVED CONFIGURATION STRAPS				ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET	
GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8	



SUN internal VGA Thermal Sensor
Address 0x714

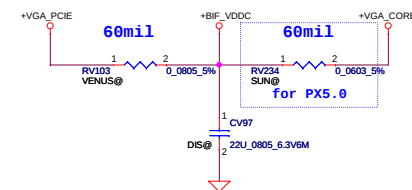
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE_VDDC and 1.8V rail

Note:
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

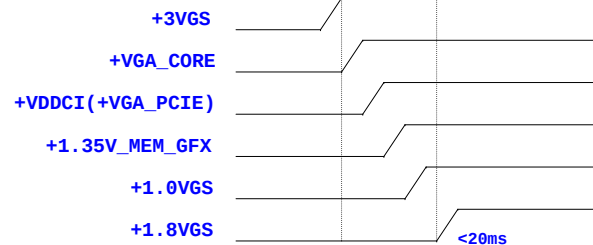


for PX4.0 and PX5.0

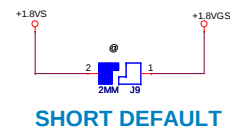
Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode



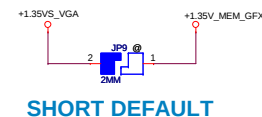
Power sequence of Sun XT,Venus Pro,Venus XT



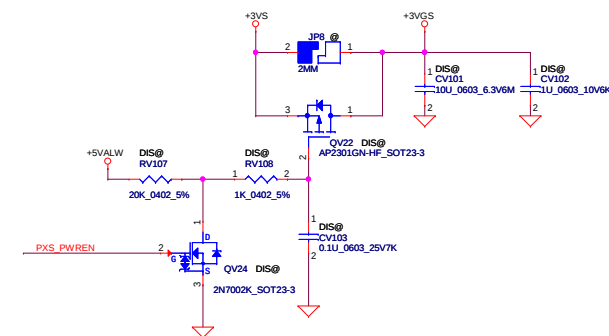
+1.8VS TO +1.8VGS



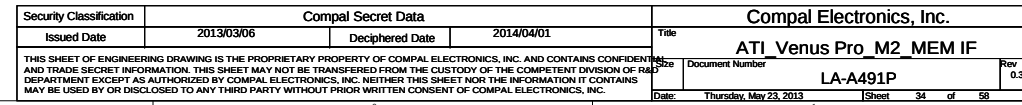
+1.35VS_VGA TO +1.35V_MEM_GFX



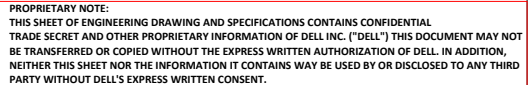
+3VS TO +3VGS



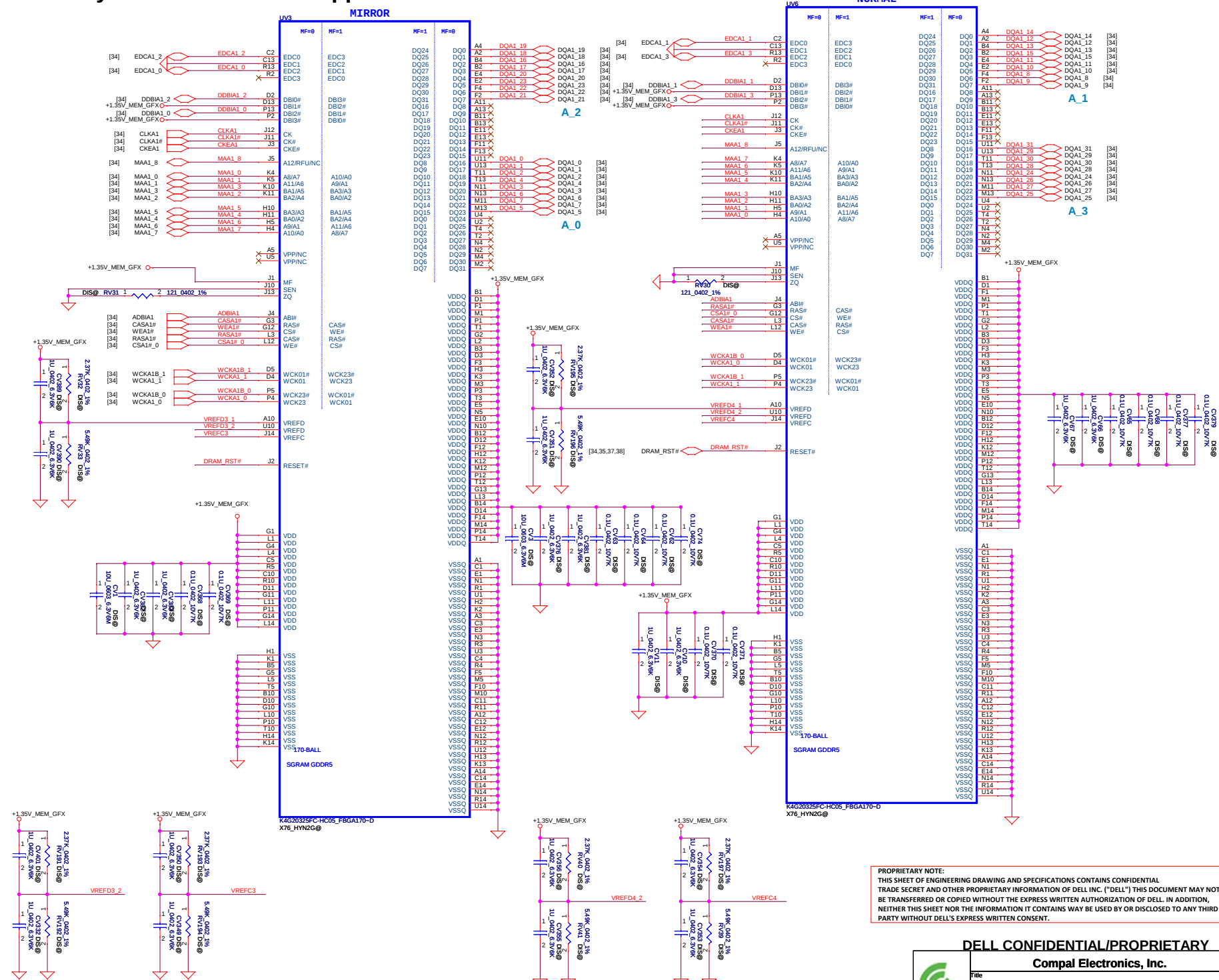
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64X32 GDDR5



Memory Partition A - Upper 16 bits



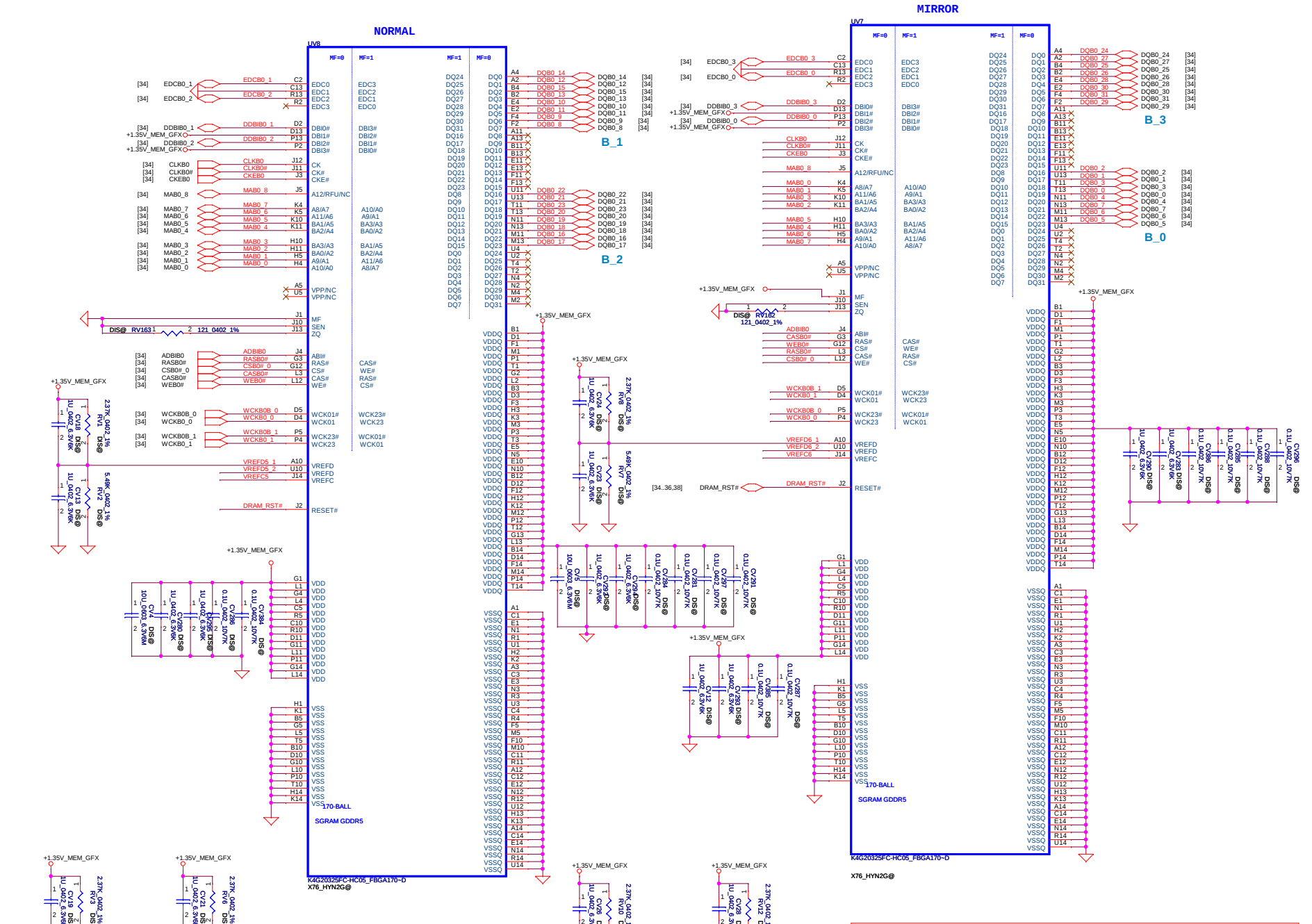
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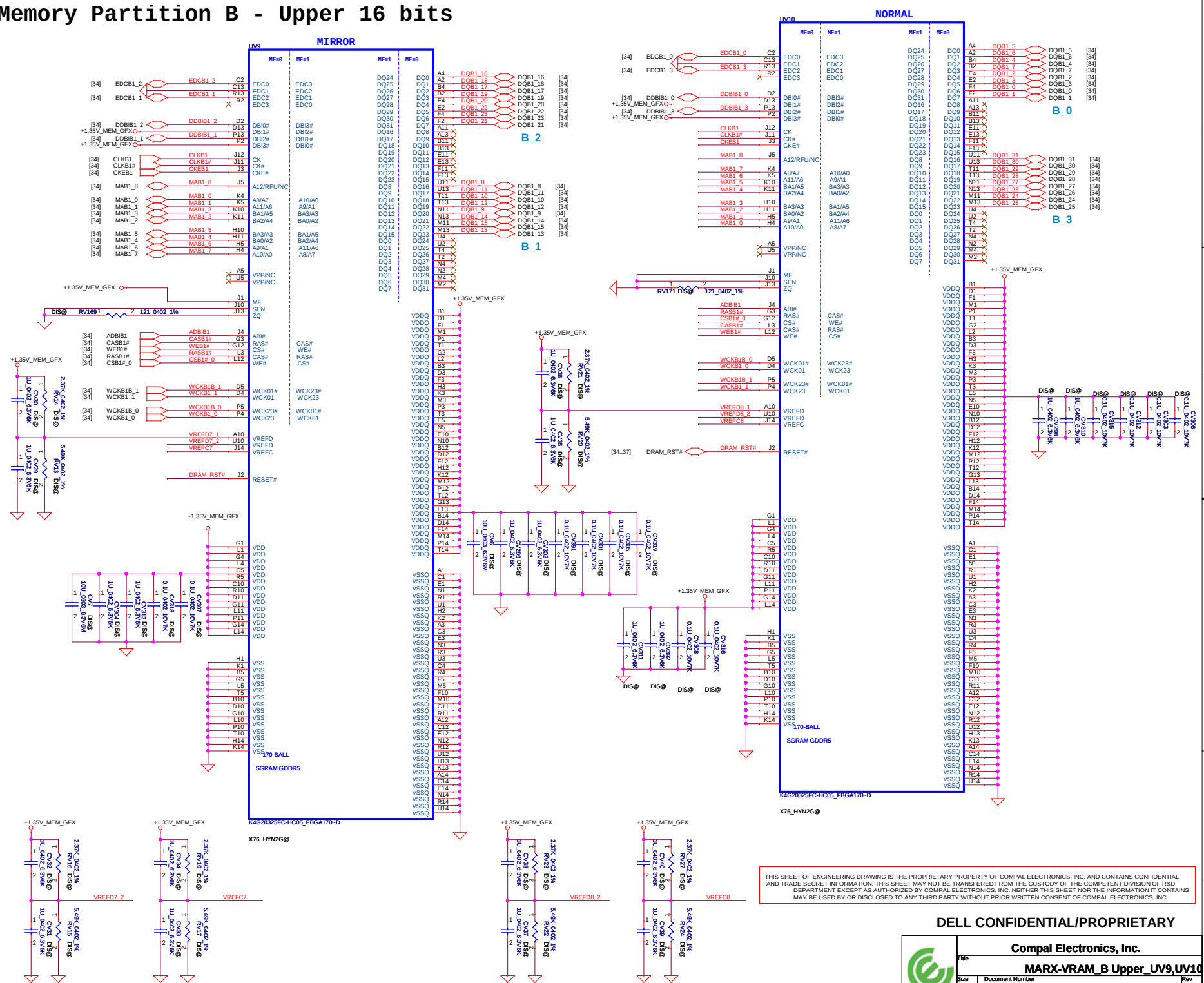
Title			MARX-VRAM_A Upper_UV3,UV6		
Size	Document Number				Rev
	LA-A491P				(

Memory Partition B - Lower 16 bits



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Memory Partition B - Upper 16 bits

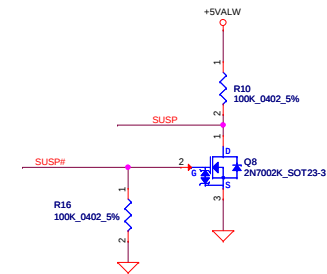
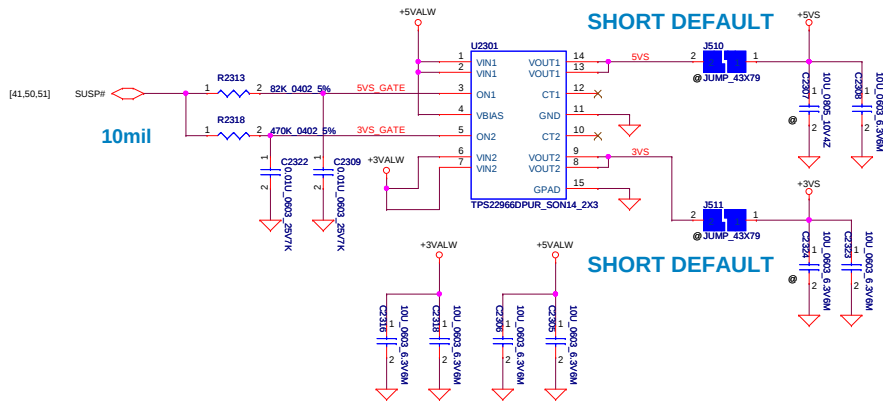


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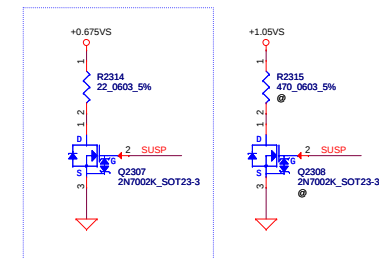
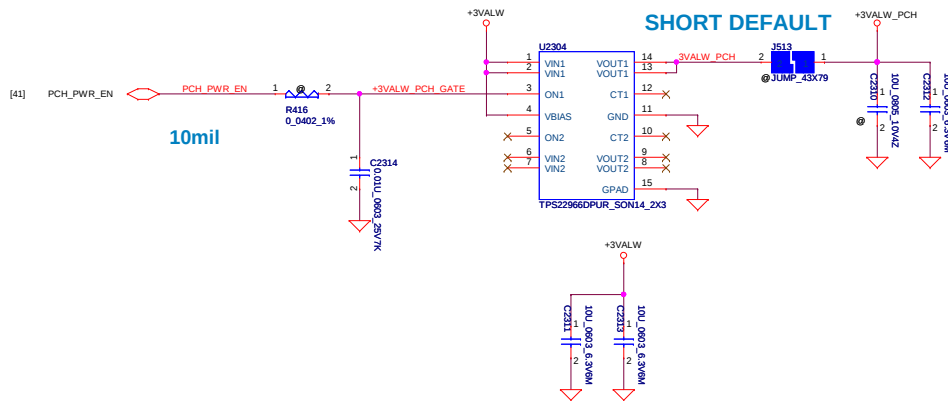
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	File MARX-VRAM_B Upper_UV9,UV10		
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+5VS and +3VS switch

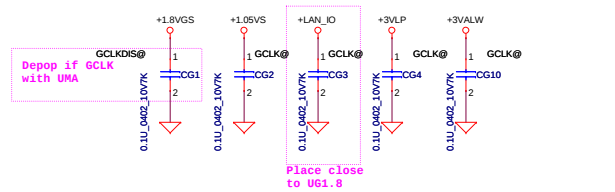


+3VALW_PCH switch

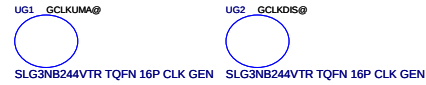
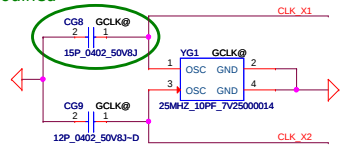


For Intel S3 Power Reduction

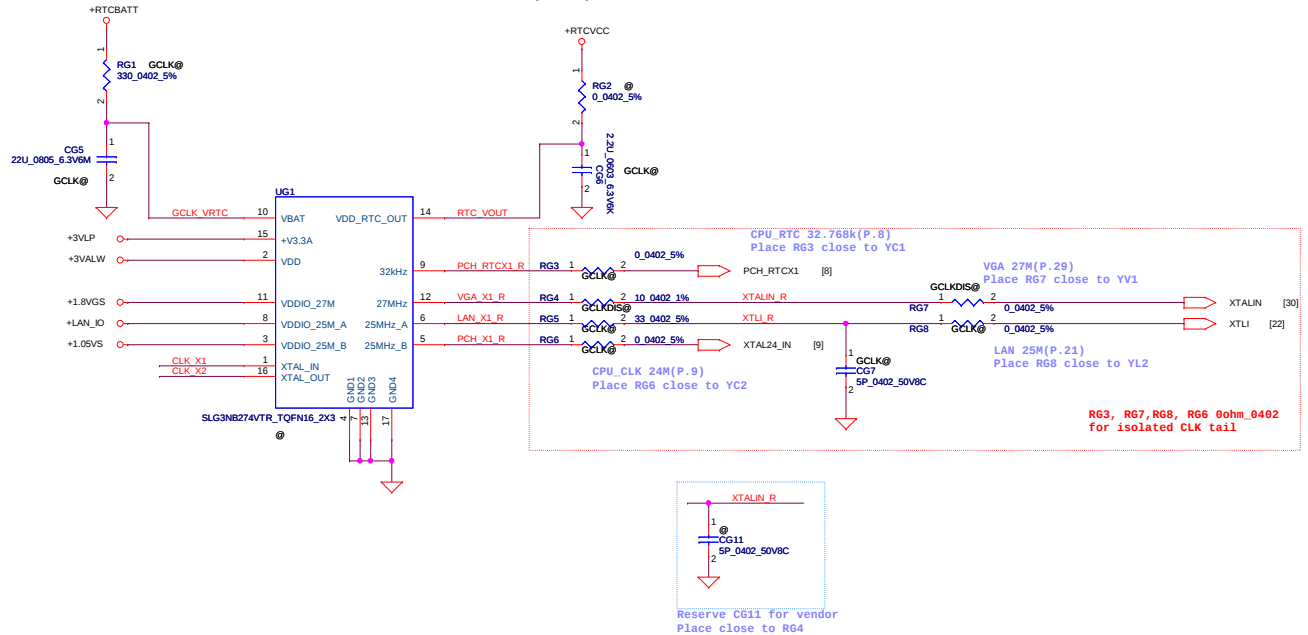
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				Rev	0.3



Latitude Oak Modified

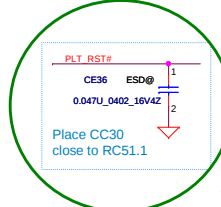


SLG3NB3374V is for DIS by output 24M*1, 25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1

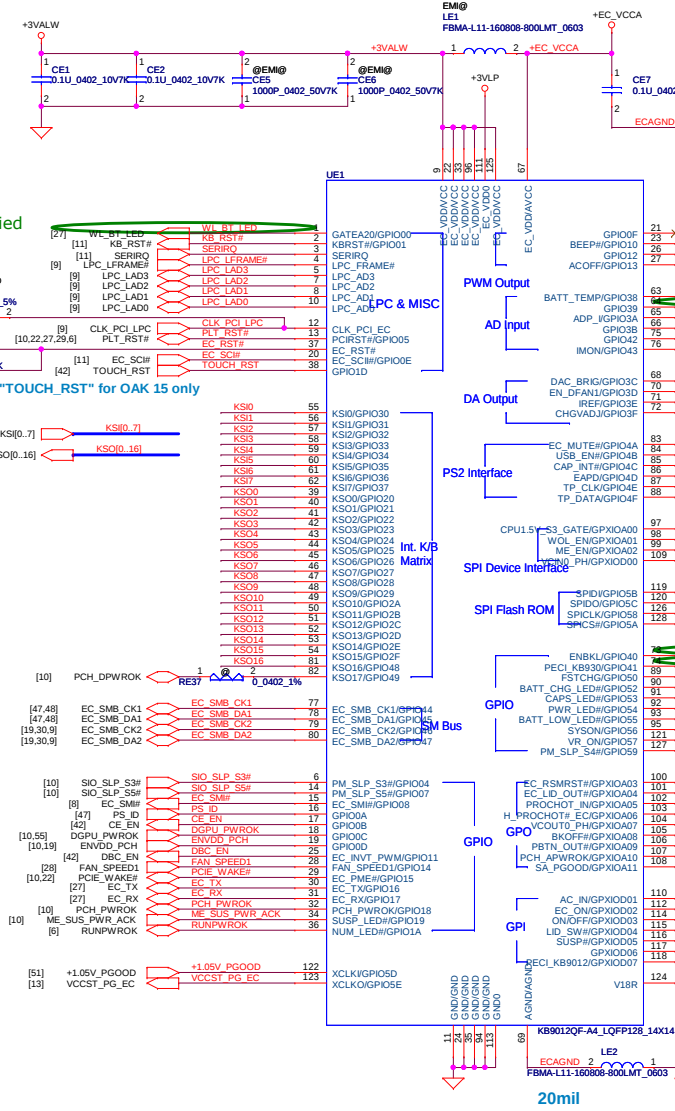
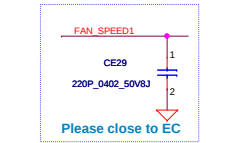
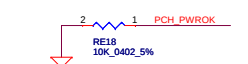
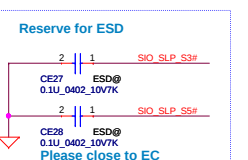
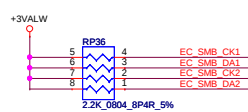
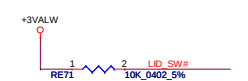
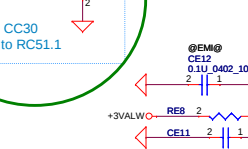


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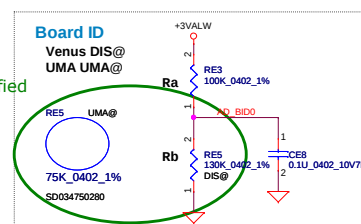
Latitude Oak Modified



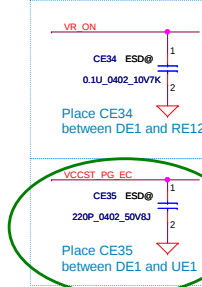
Latitude Oak Modified



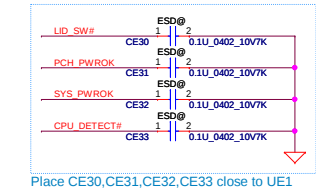
Latitude Oak Modified



Latitude Oak Modified



Latitude Oak Modified



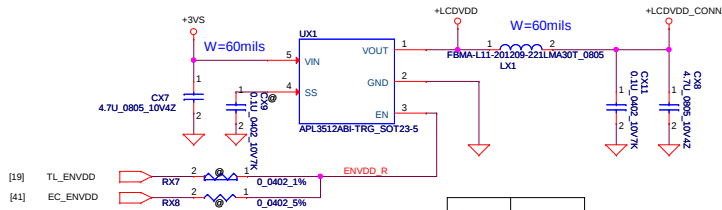
Place CE30, CE31, CE32, CE33 close to UE1

KB9012A3 change to KB9012A4 SA00004OB30

ME_FWP PCH has internal 20K PD. (suspend power rail)

Security Classification		Compal Secret Data		Title	
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2013/03/06		2014/04/01		LA-A491P	
2013/03/06		2014/04/01		Date	
2013/03/06		2014/04/01		Thursday, May 23, 2013	
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2013/03/06		2014/04/01		41 of 58	
2013/03/06		2014/04/01		Rev	
2013/03/06		2014/04/01		0.3	

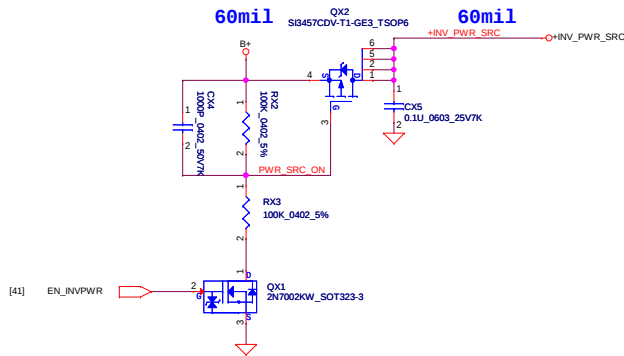
LCD PWR CTRL



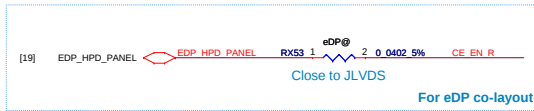
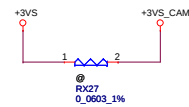
CSS	TSS
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

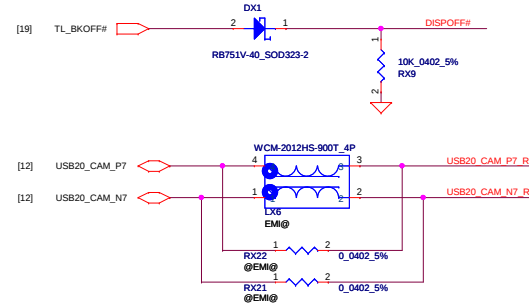
LCD backlight PWR CTRL



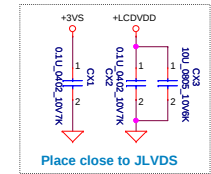
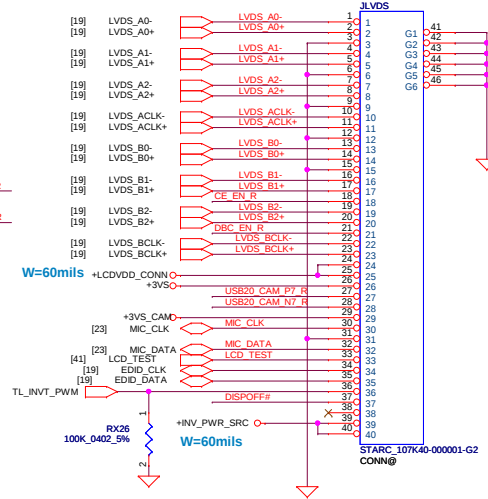
Webcam PWR CTRL



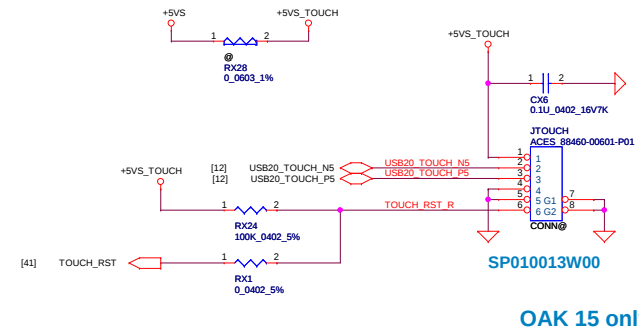
LVDS Connector



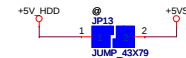
CE_EN_R only for reserve.



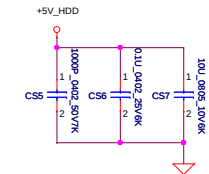
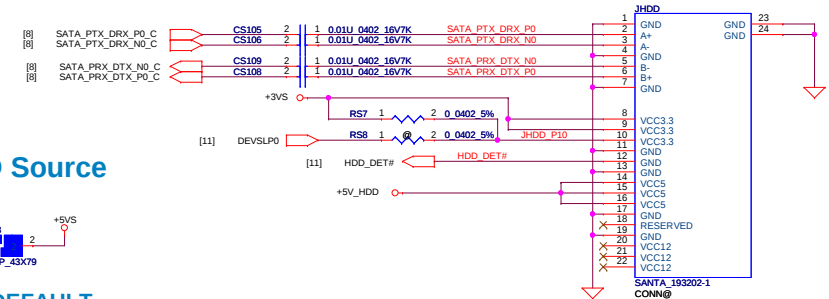
* Touch Screen Panel



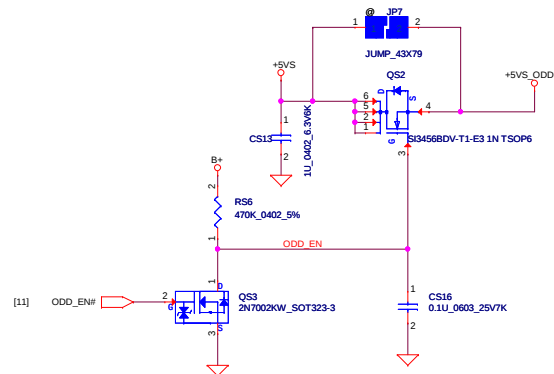
SATA HDD Connector



SHORT DEFAULT

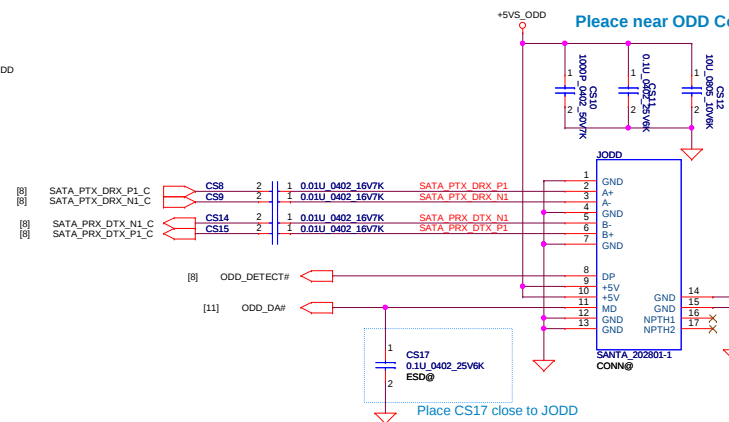


ODD Power Control

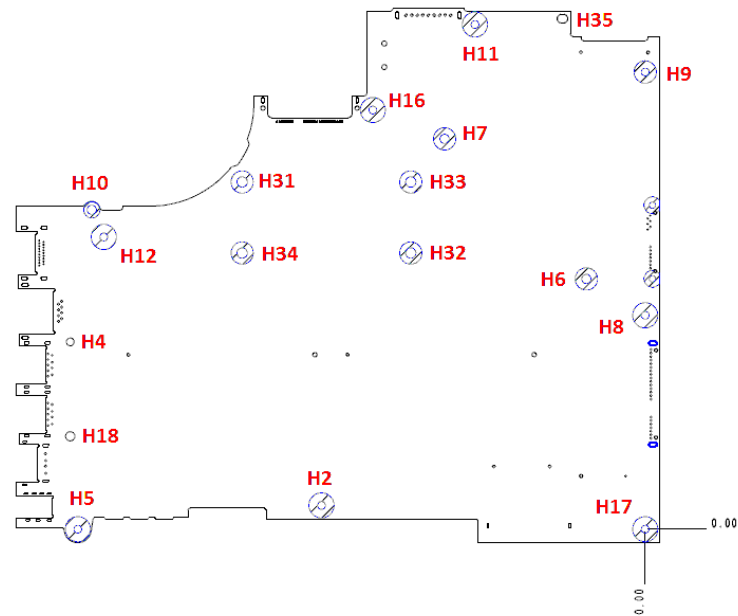
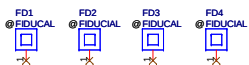
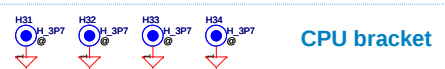


SATA ODD Connector

Please near ODD Connector



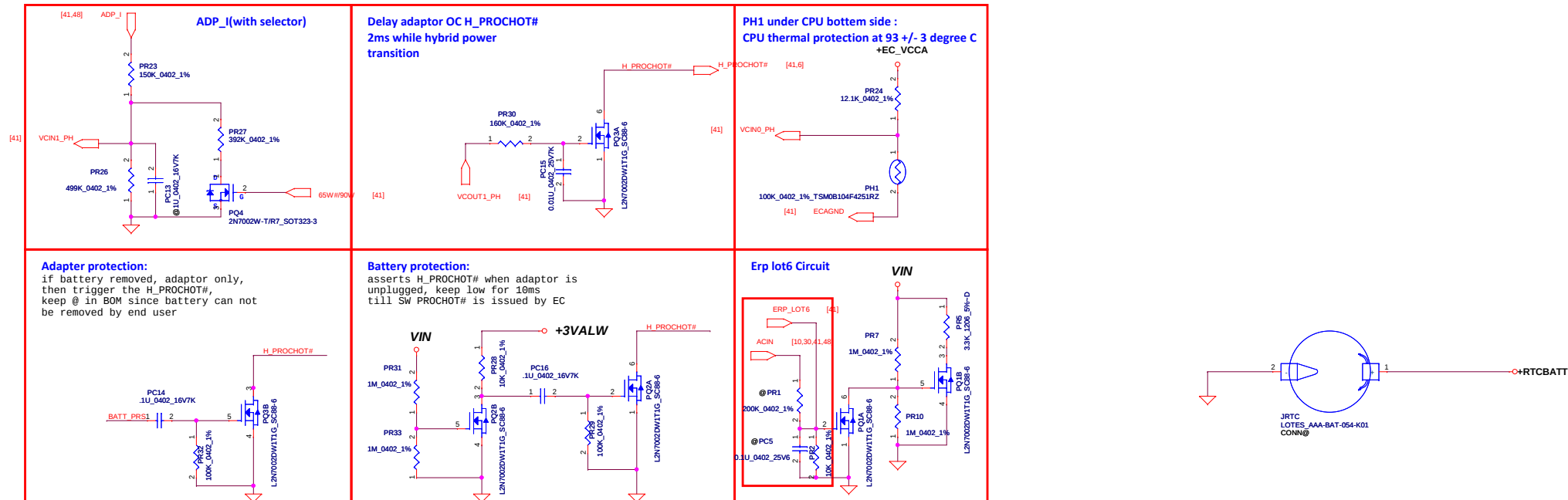
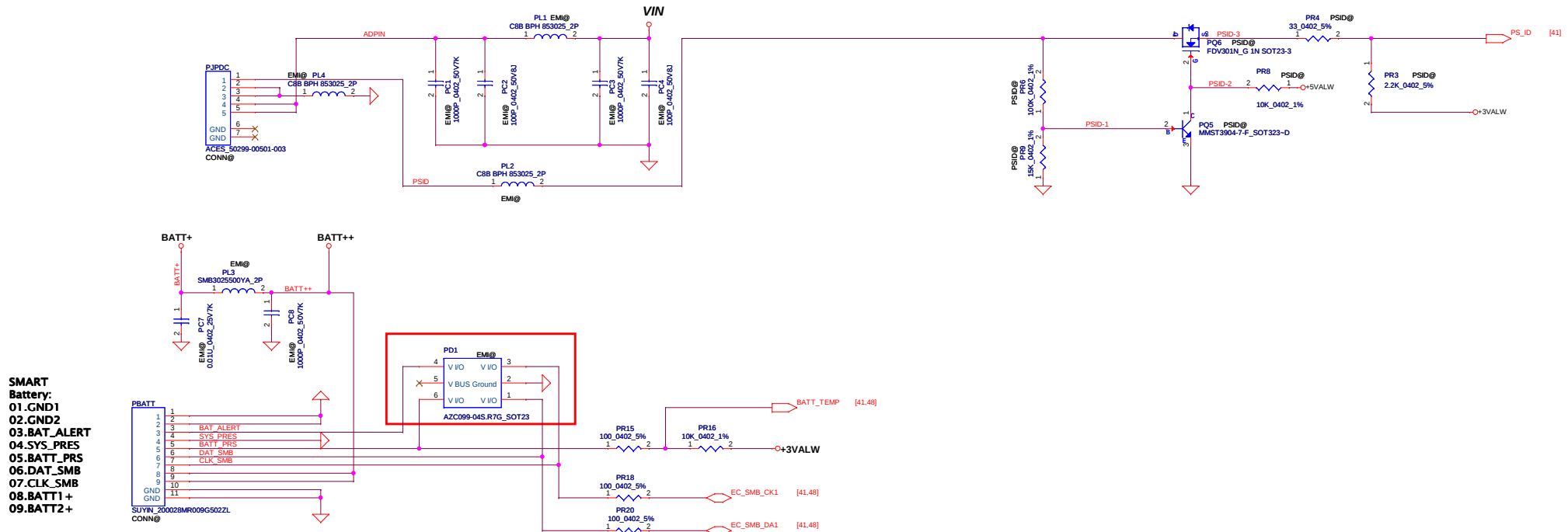
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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	HDD/ODD	
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
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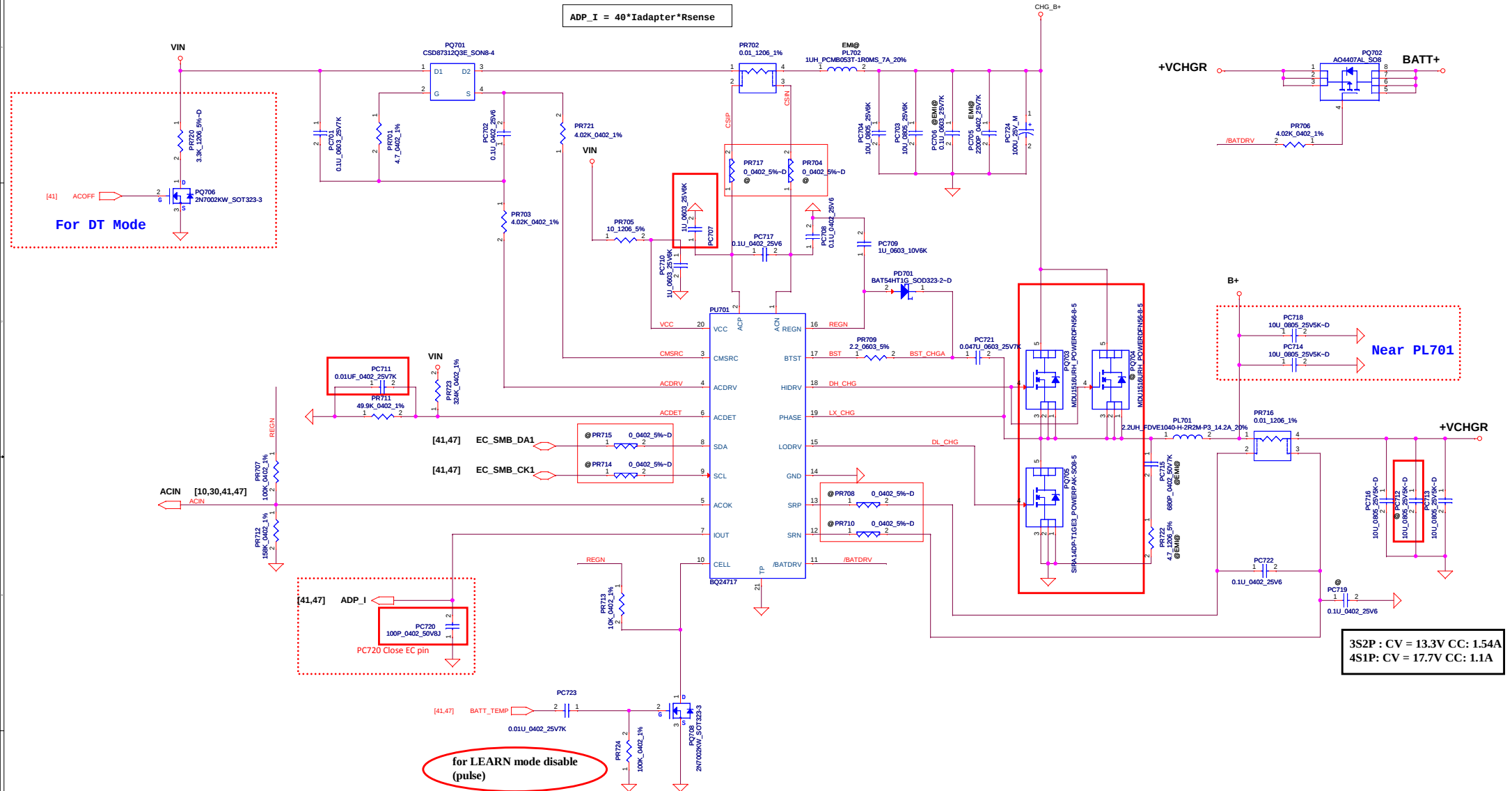
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
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54							

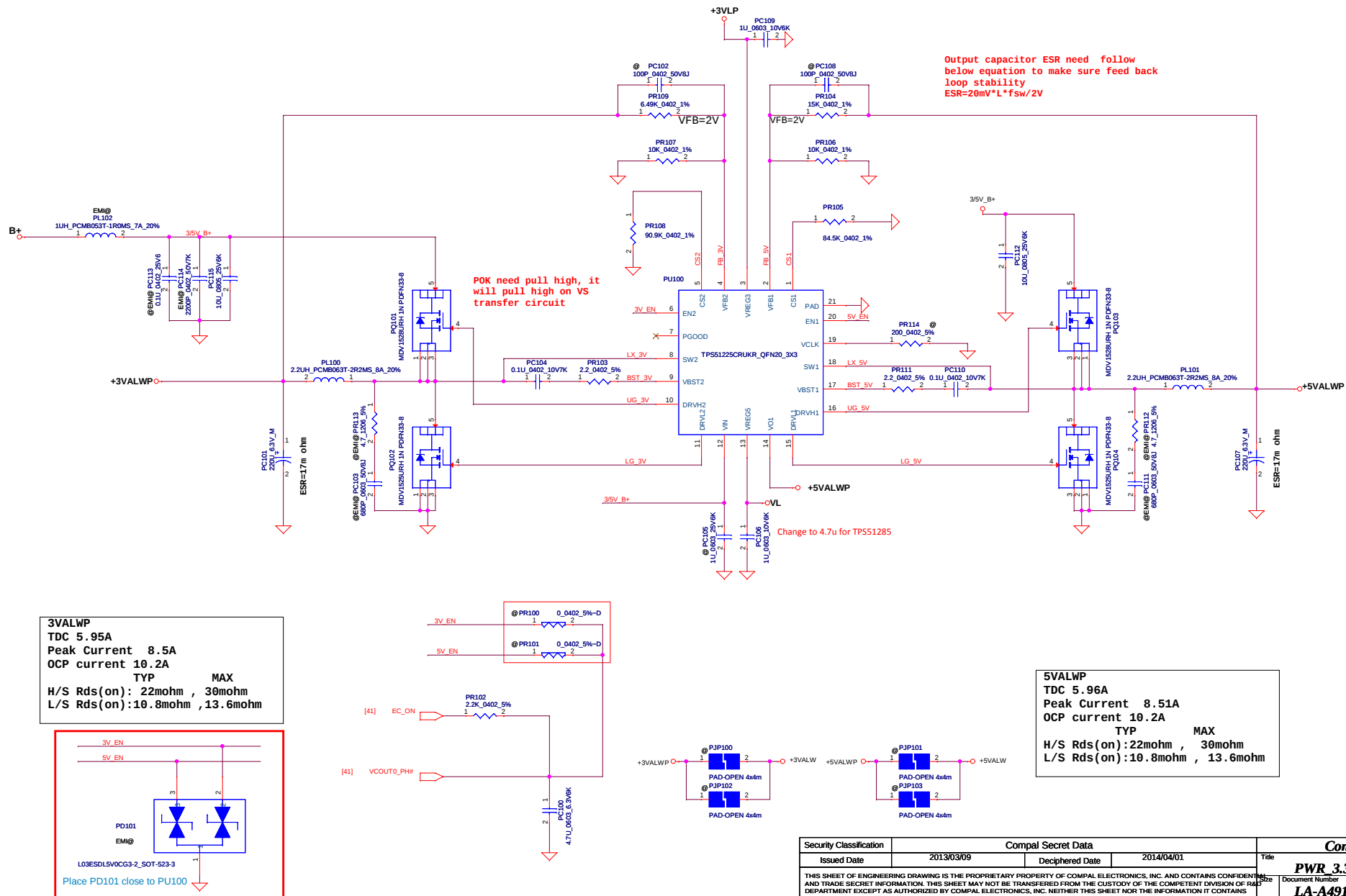


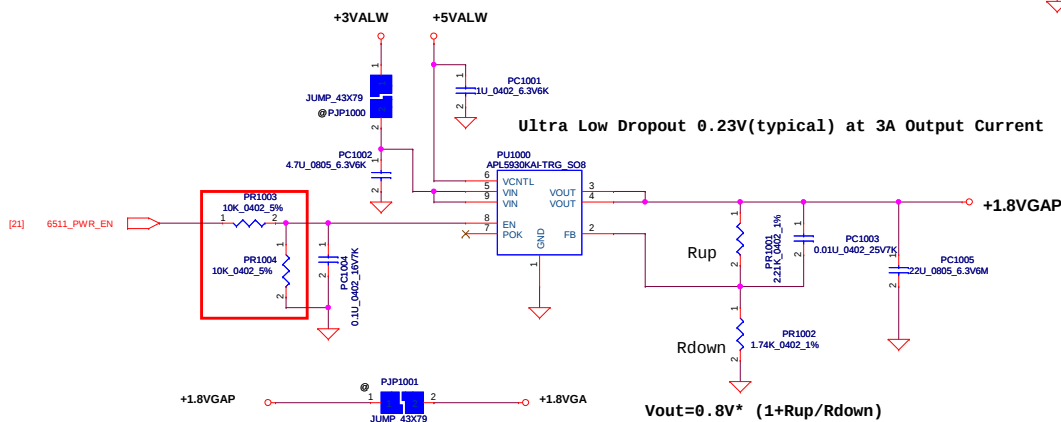
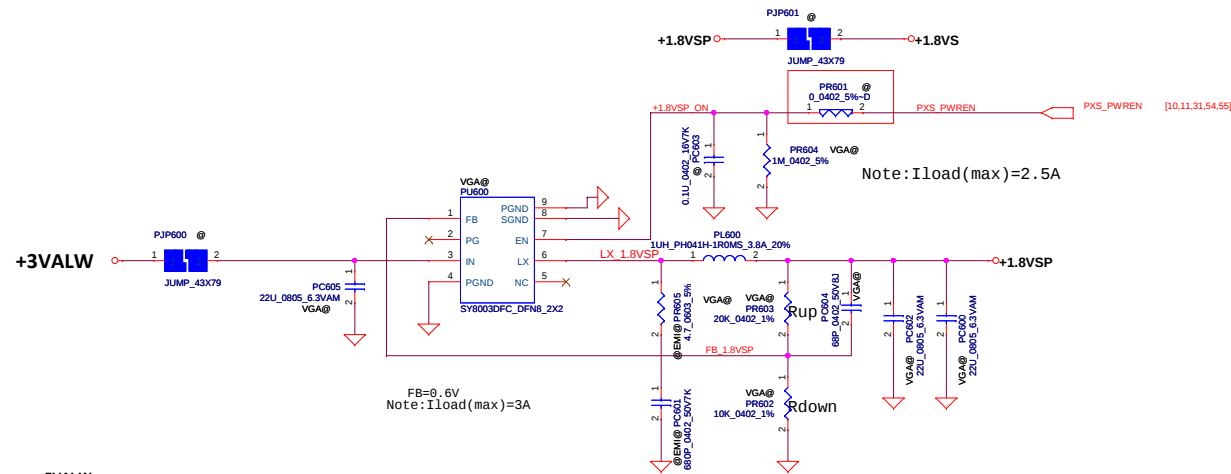
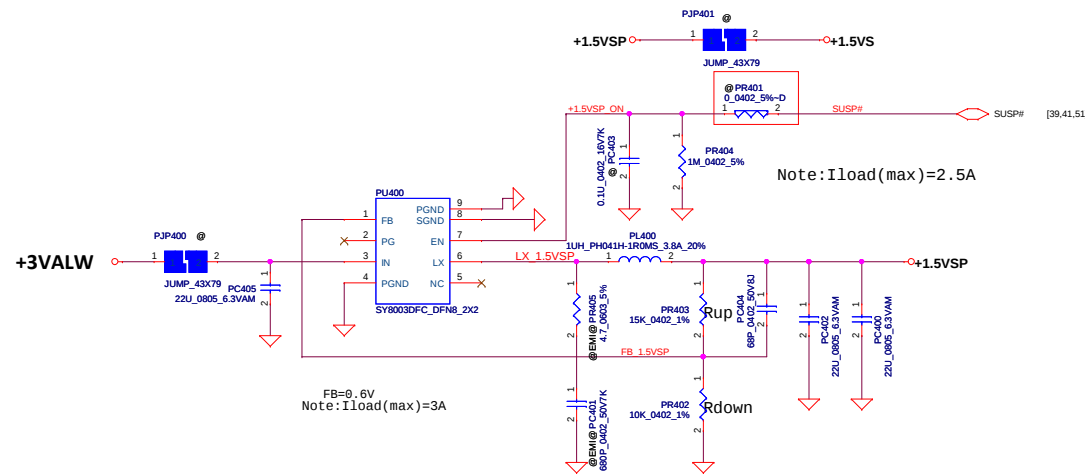
Iada=0~3.33A(65W)

Iada=0~4.62A(90W)

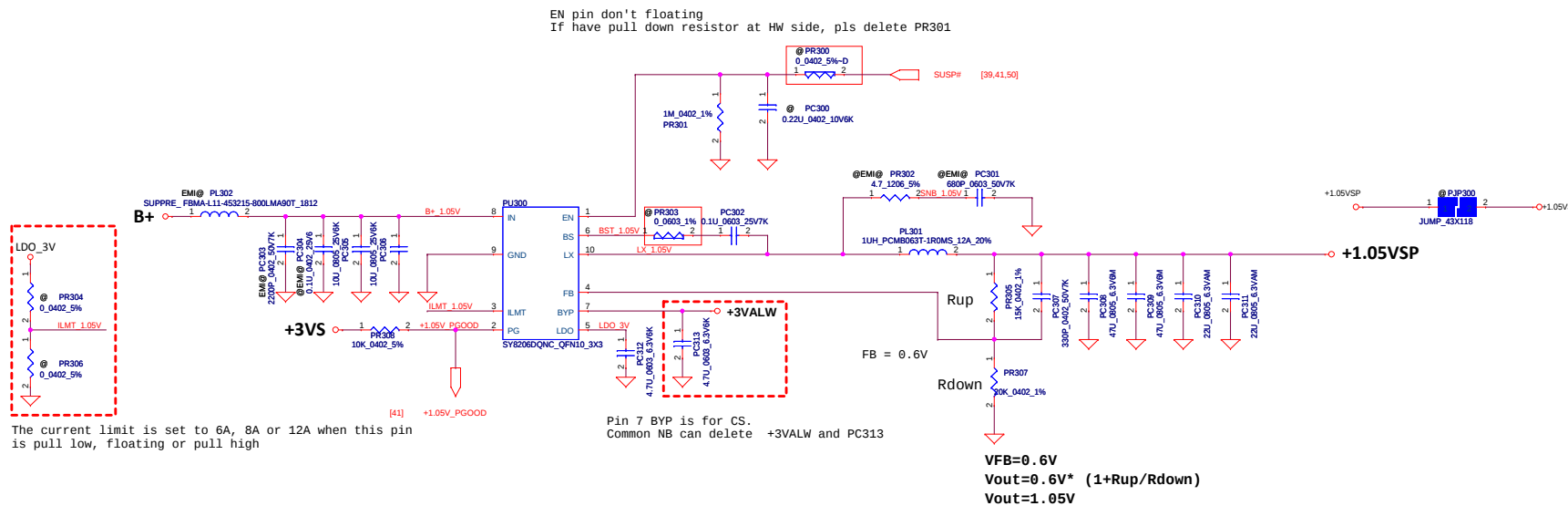
ADP_I = 40*Iadapter*Rsense







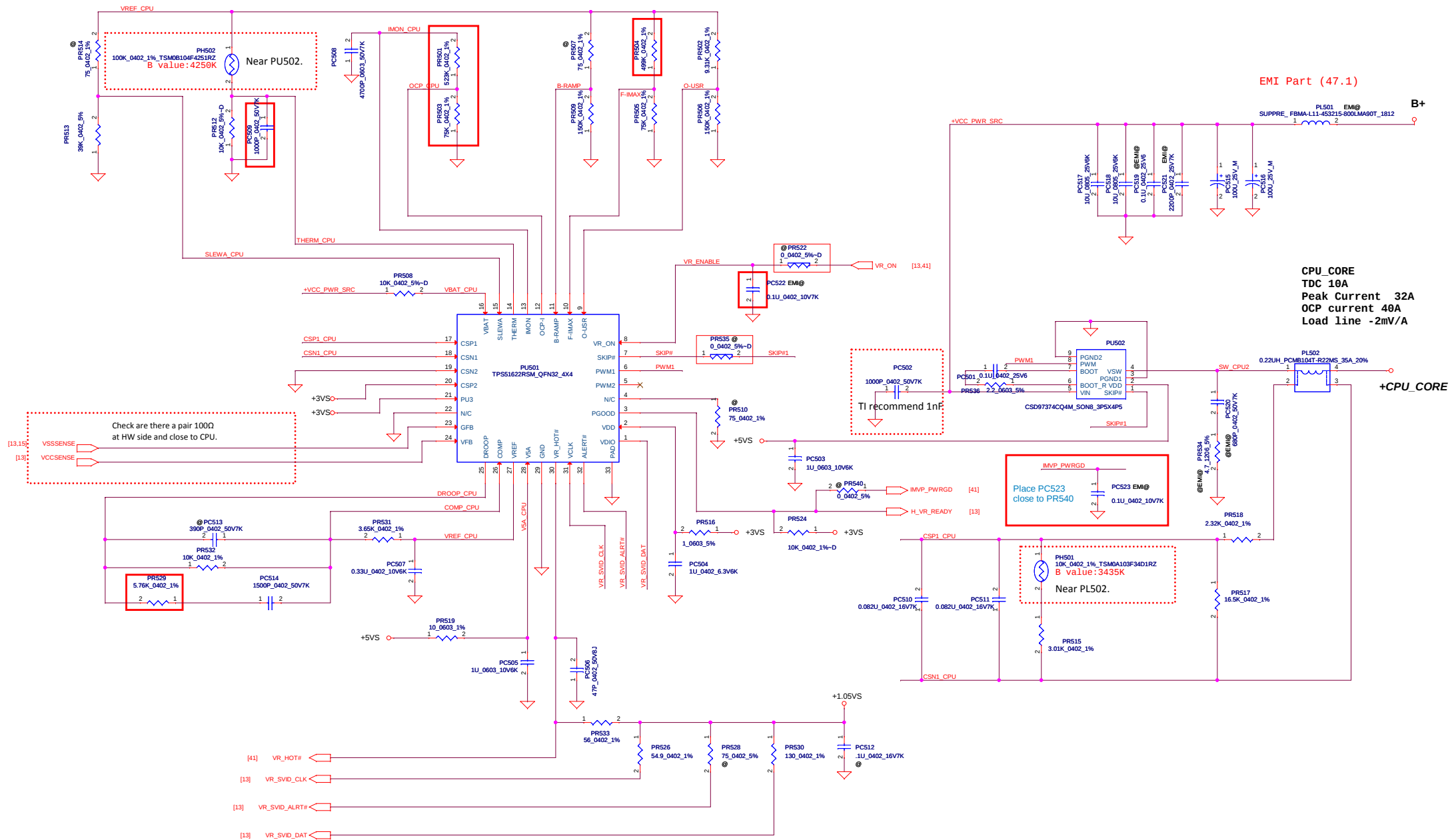
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	PWR 1.5VSP/1.8VSP/1.8VGAP
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The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

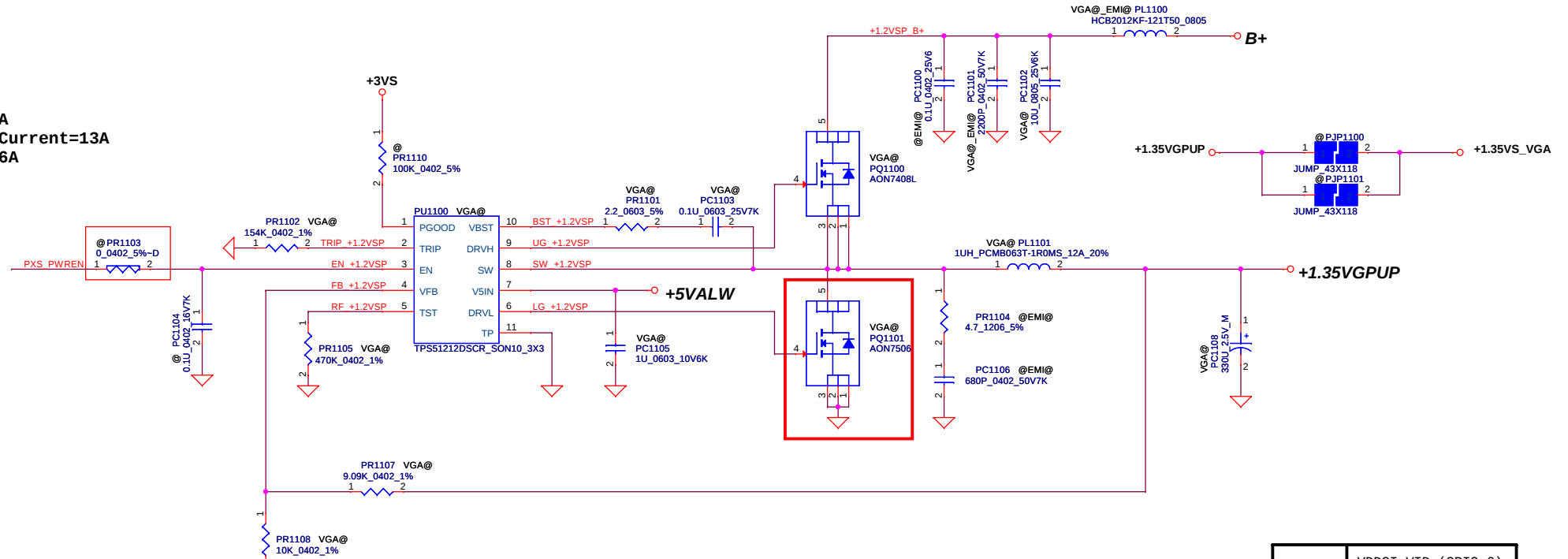
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC313

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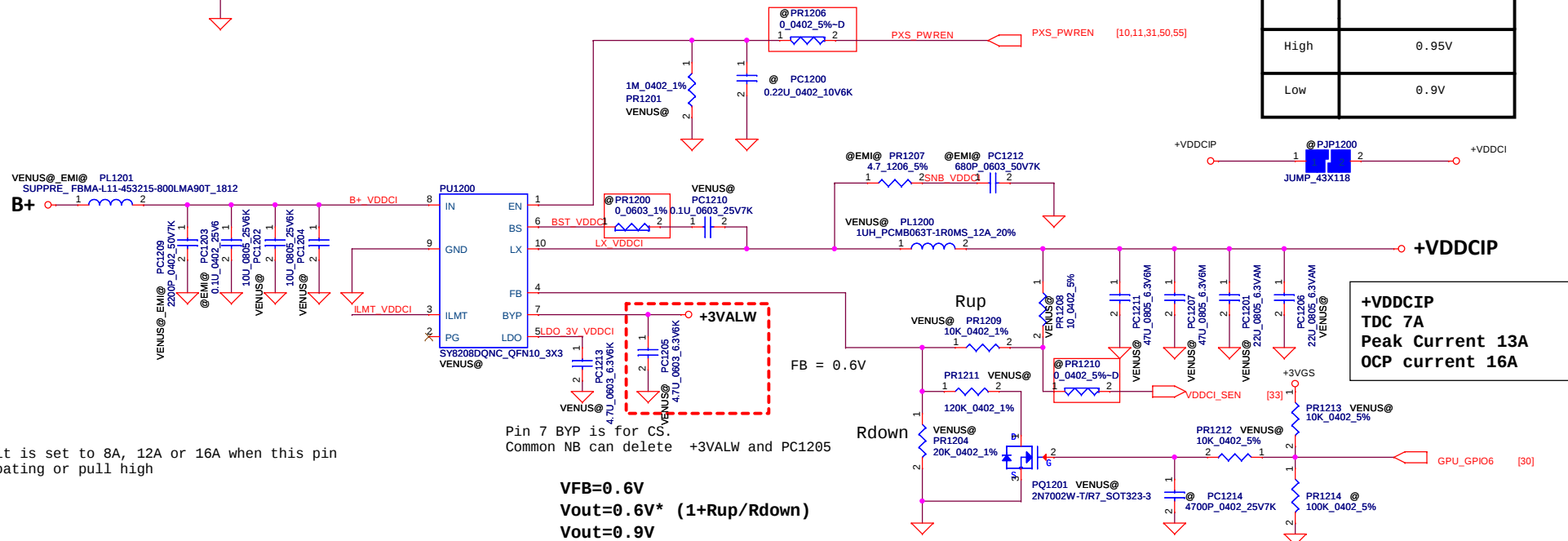


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TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VFB=0.6V
 $V_{out}=0.6V \cdot (1+R_{up}/R_{down})$
 Vout=0.9V

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	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE

Frequency 300kHz

TDC 23A(25W)/33A(32W)

Peak Current 30A(25W)/47A(32W)

OCp current 36A(25W)/56A(32W)

TYP MAX

H/S Rds(on) :12.2mohm , 15mohm

L/S Rds(on) :2.75mohm , 3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)

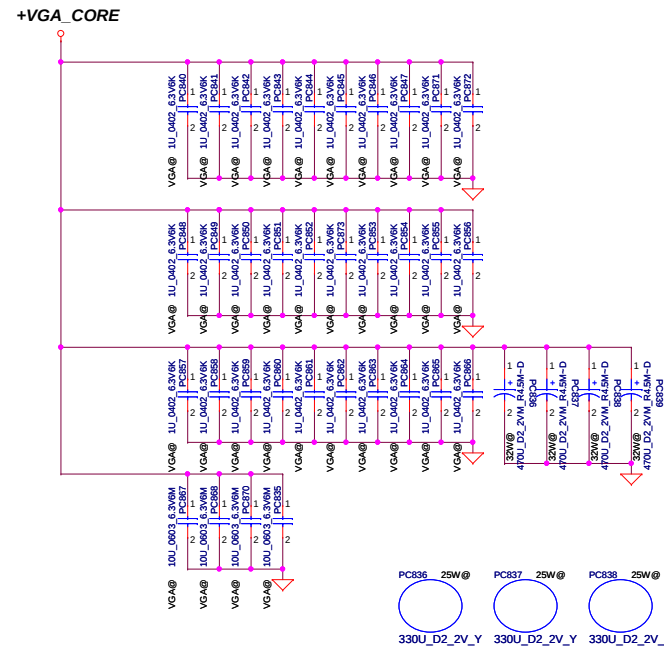
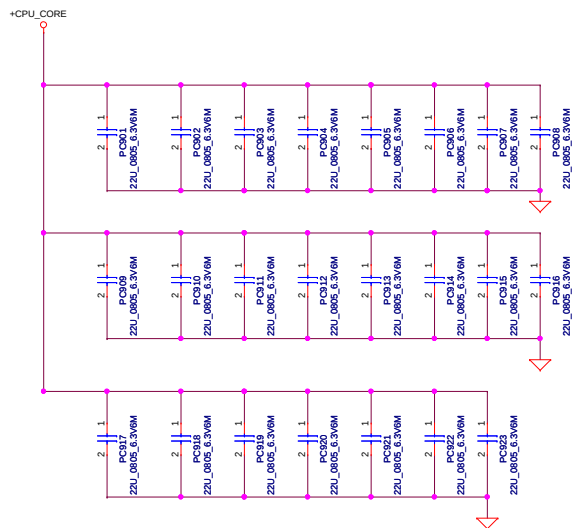
Load line : -1.5mV/A



GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

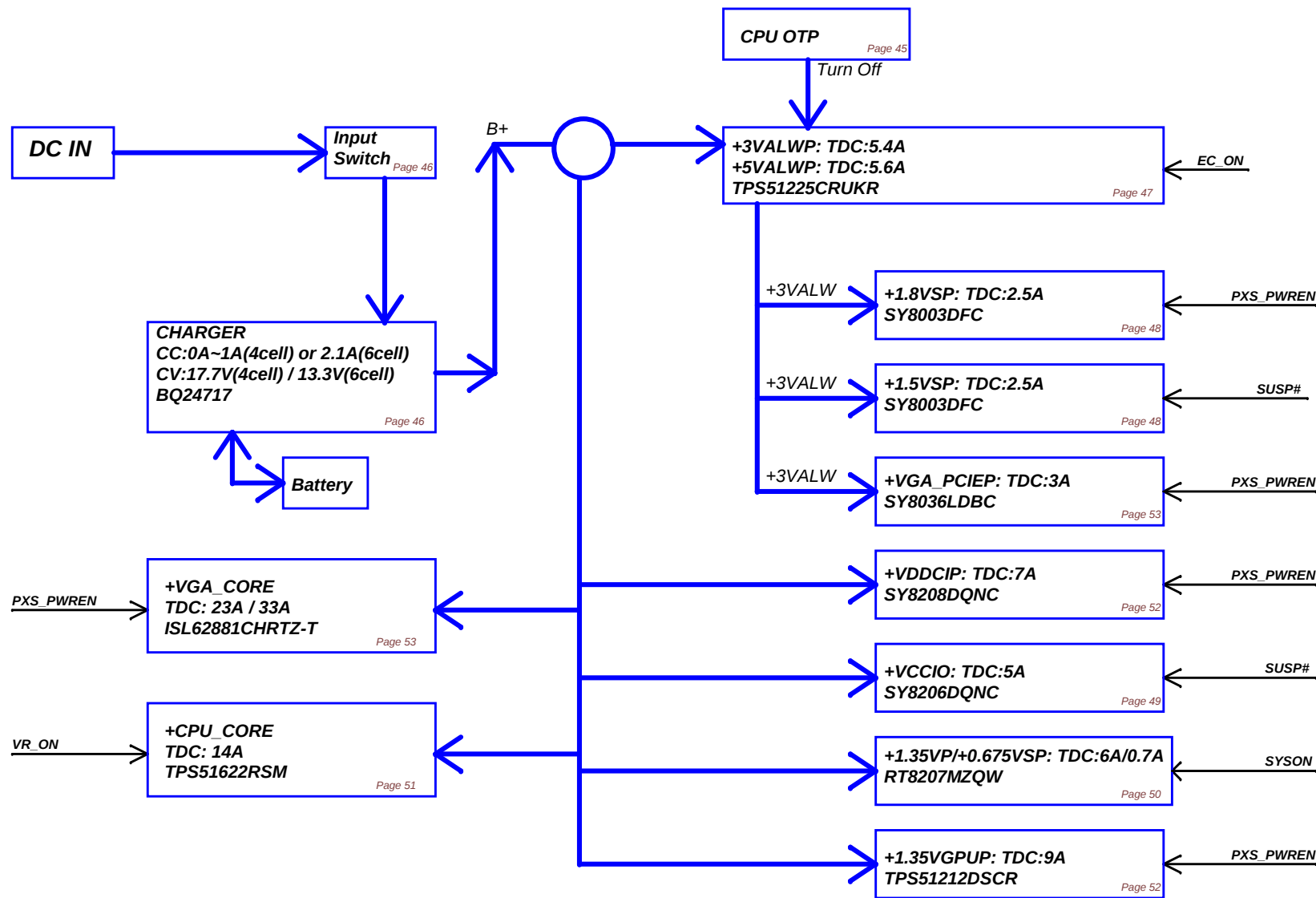
Initial voltage:0.85V(Venus)
0.9V(Sun)

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Power block



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				Date: Thursday, May 23, 2013	Sheet 58 of 58