Compal Confidential

PIQY1 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT1

2010-10-05

REV:0.2

Security Classification	Compal Secret Data		
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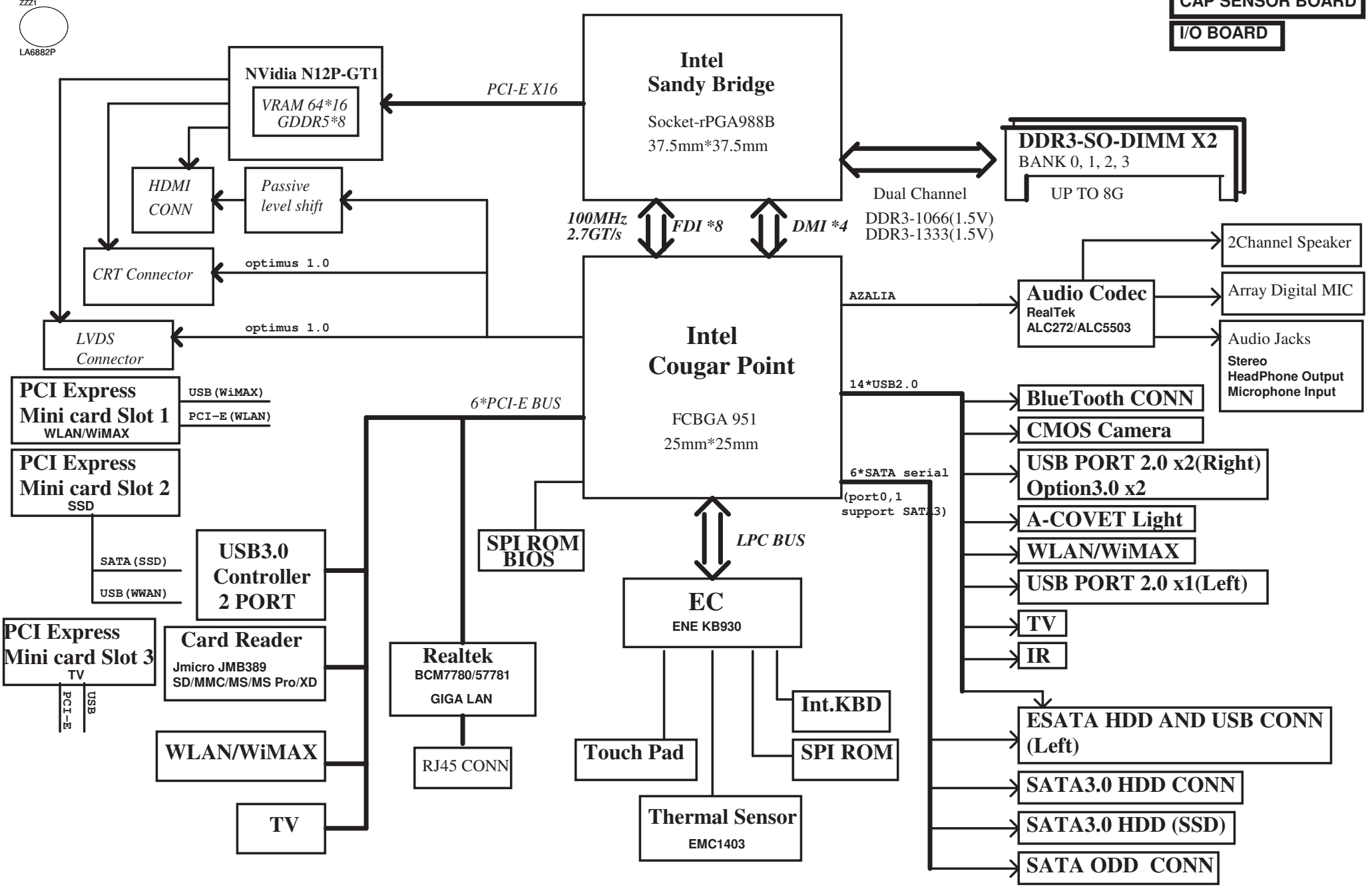
Title: *Cover Page*		
Size: Custom	Document Number: *LA-6882P*	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 1 of 63	

POWER & BOARD
CAP SENSOR BOARD
I/O BOARD

ZZZ1
LA6882P



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Compal Electronics, Inc.

Title: MB Block Diagram

Size	Document Number	Rev
Custom		0.2

Date: Wednesday, October 06, 2010 Sheet 2 of 63

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	10K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Right Side)
		3	USB Port (Right Side)
	UHCI2	4	Camera(3D)
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	IR
		9	Mini Card(WLAN)
	UHCI5	10	A Cover Light
		11	
	UHCI6	12	Mini Card(TV)
		13	Blue Tooth

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	USB3.0
5	Card Reader
6	TV
7	
8	

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
DIS@	Discrete part
UMA@	UMA part
DIS_ONLY@	Discrete only part
HDMI@	HDMI part (DIS and UMA)
UMA_HDMI@	HDMI part (UMA)
DIS_HDMI@	HDMI part (DIS)
USB20@	USB20 option (Right side 2 ports)
USB30@	USB30 option (Right side 2 ports)
USB30_SUB@	USB30 part at sub-board
TV@	TV module part
TV_SW@	TV module power swith part
NO_TVSW@	No TV module power swith part
USB_CHG@	USB charger part
NO_CHG@	No USB charger part
272@	ALC272 audio codec part
5503@	ALC5503 audio codec part
57780@	BCM57780 LAN part
57781@	BCM57781 LAN part
ACOVER@	A cover light part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
ESATA@	E-SATA part
VENTURA@	NVDIA VENTURA function part
X76@	X76 Level part
S1G@	Samsun VRAM 1G part
S2G@	Samsun VRAM 2G part
H1G@	Hynix VRAM 1G part
ME@	ME part
@	Unpop

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SKU

OPTIMUS	UMA@+DIS@+OPTI@
Discrete only	DIS@+DIS_ONLY@

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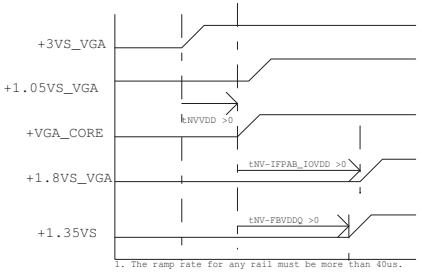
Title: *Notes List*

Size: B | Document Number: *LA-6882P* | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 3 of 63

VGA and GDDR5 Voltage Rails (N12Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	I/O	N/A	
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	N/A	
GPIO14	OUT	N/A	
GPIO15	IN		Hot Plug Detect for IFPE
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules specified in discrete GPU design guide.

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N12P-GT1 64bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

GPIO5 GPIO6

	Device ID
N12P-GT1 (40nm)	0x0DEB

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.825V	Deep P12
0	1	0.825V	P8
1	1	1.075V	P0

GPU	FB Memory (GDDR5)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (defaul)	K4G10325FE-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
					X76			

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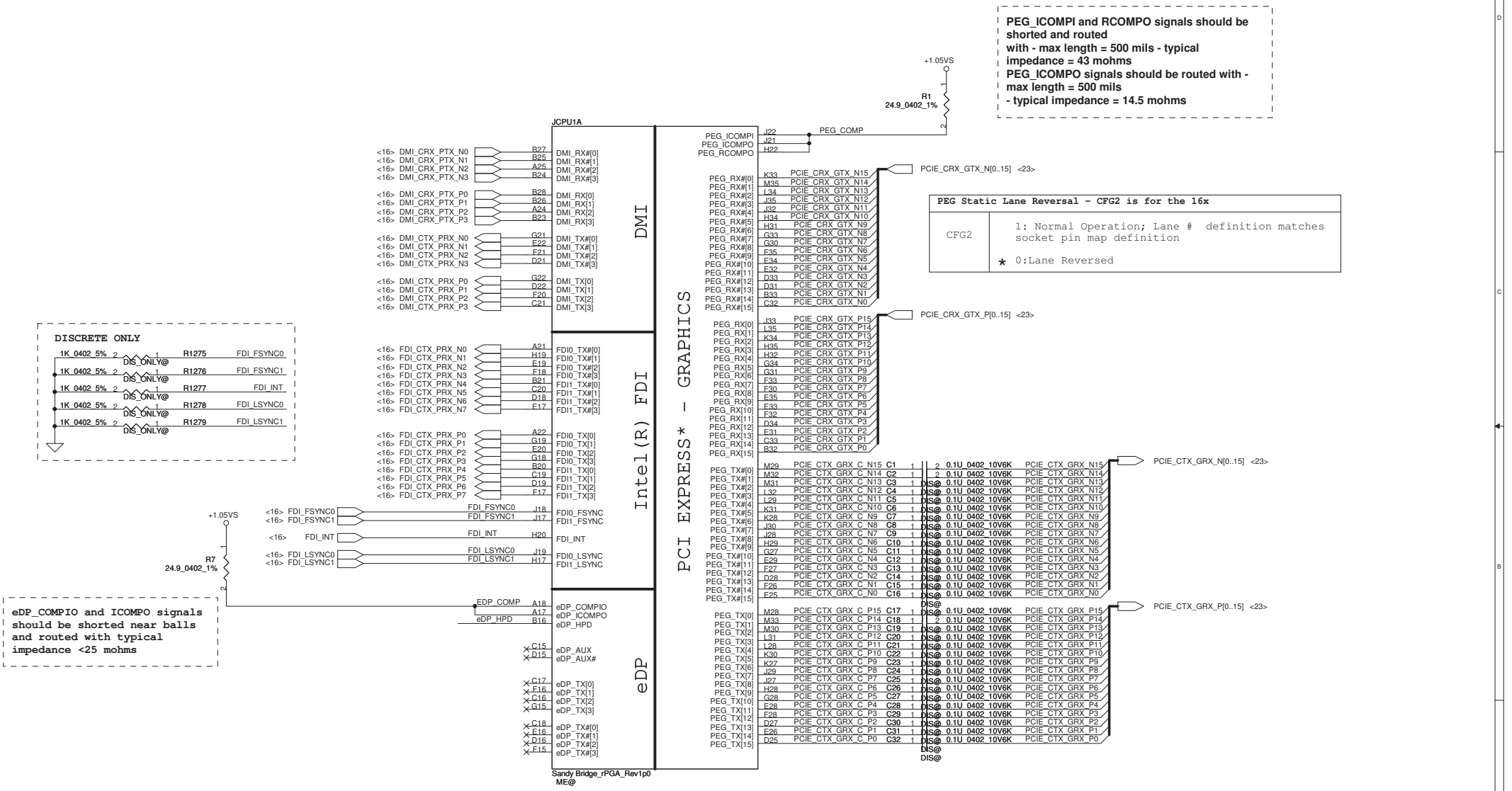
Title: VGA Notes List

Size | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 4 of 63



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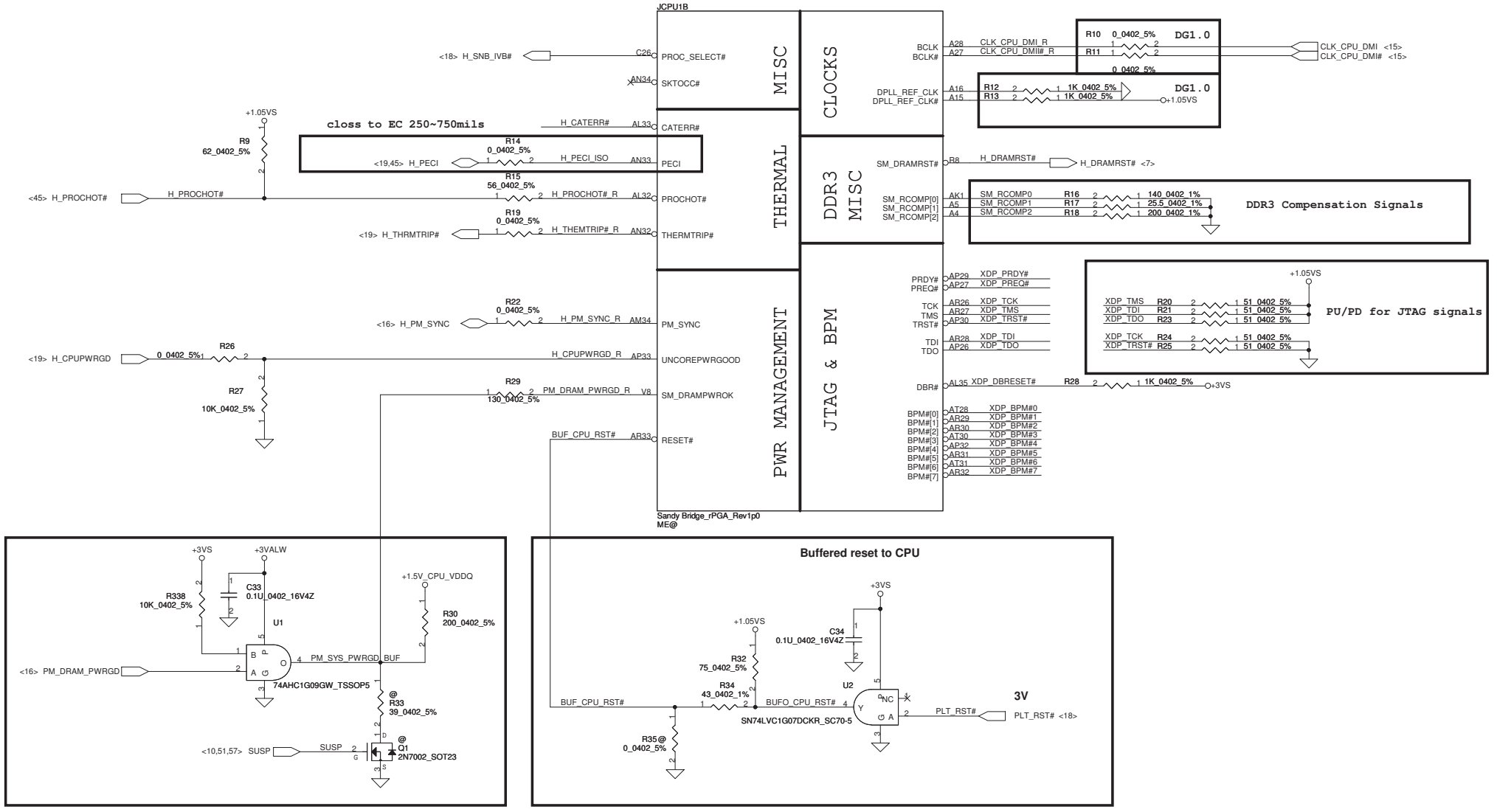
Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 5 of 63



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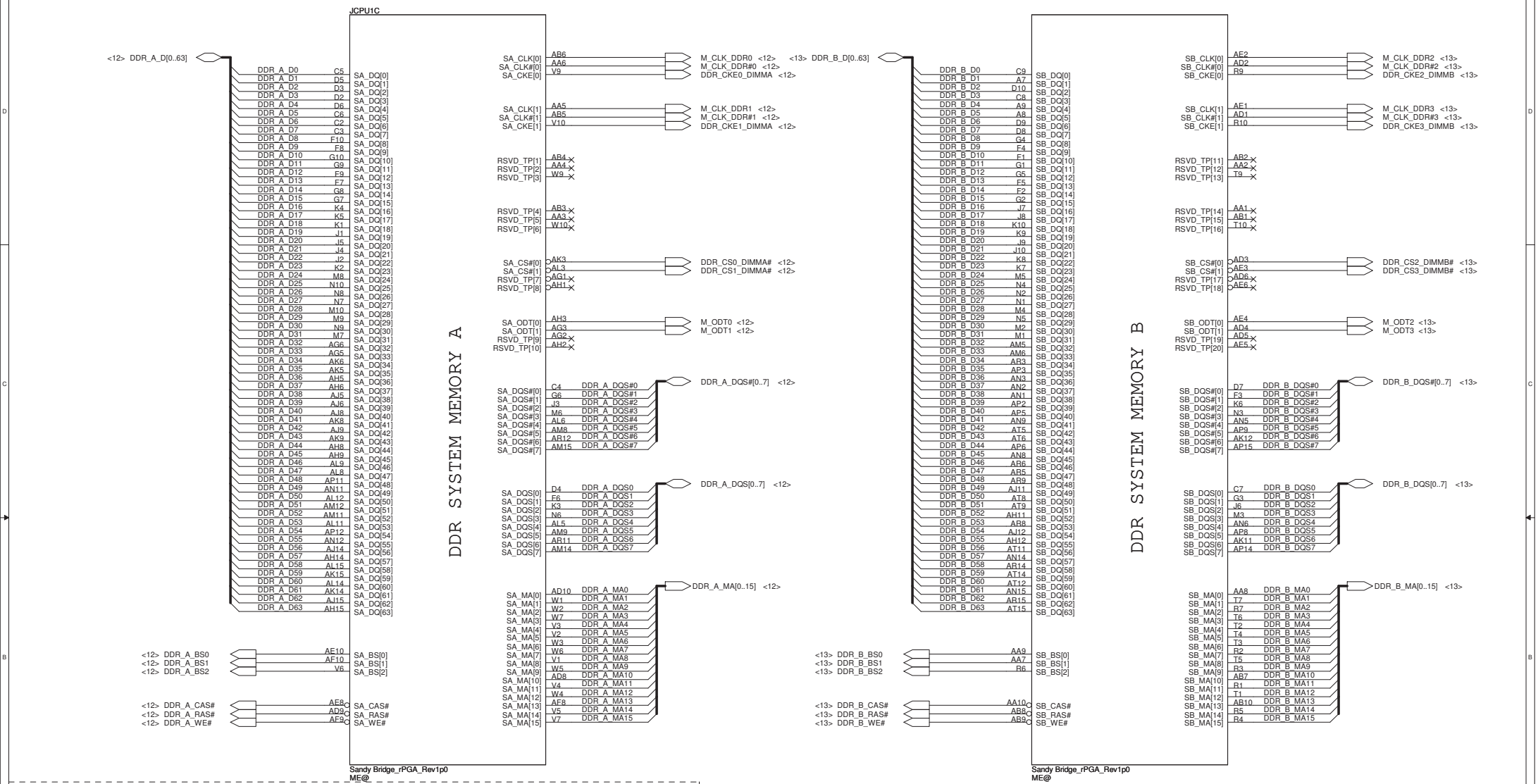
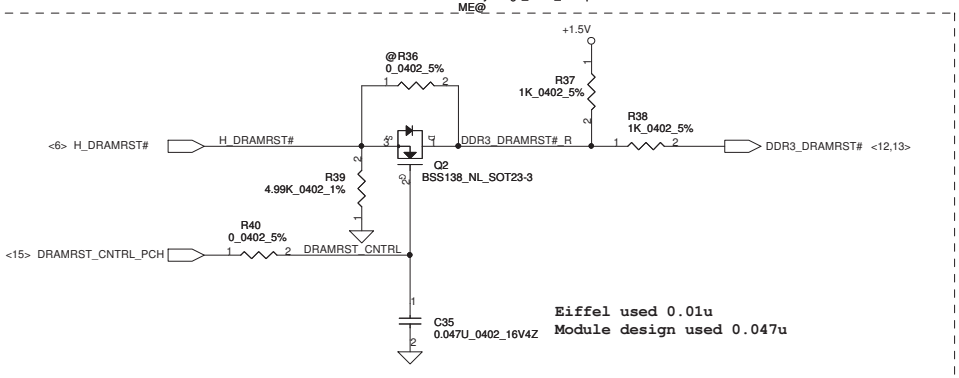
Title: PROCESSOR(2/7) PM,XDP,CLK			
Size: Custom	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 6 of 63		

JCPU1D





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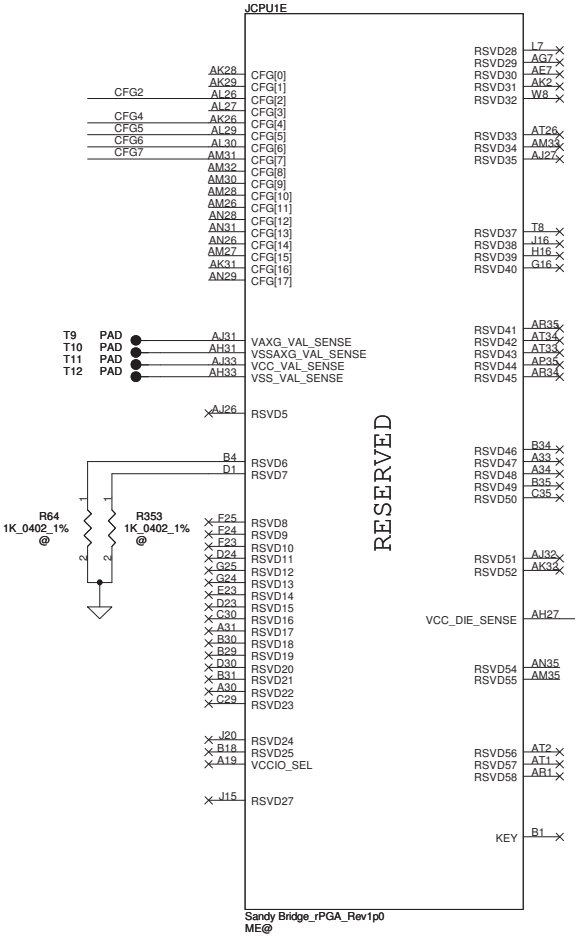
Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 7 of 63

CFG Straps for Processor



CFG2

R41 1K_0402_1%

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4

@ R42 1K_0402_1%

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6

CFG5

@R43 1K_0402_1%

@R44 1K_0402_1%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

CFG7

@R45 1K_0402_1%

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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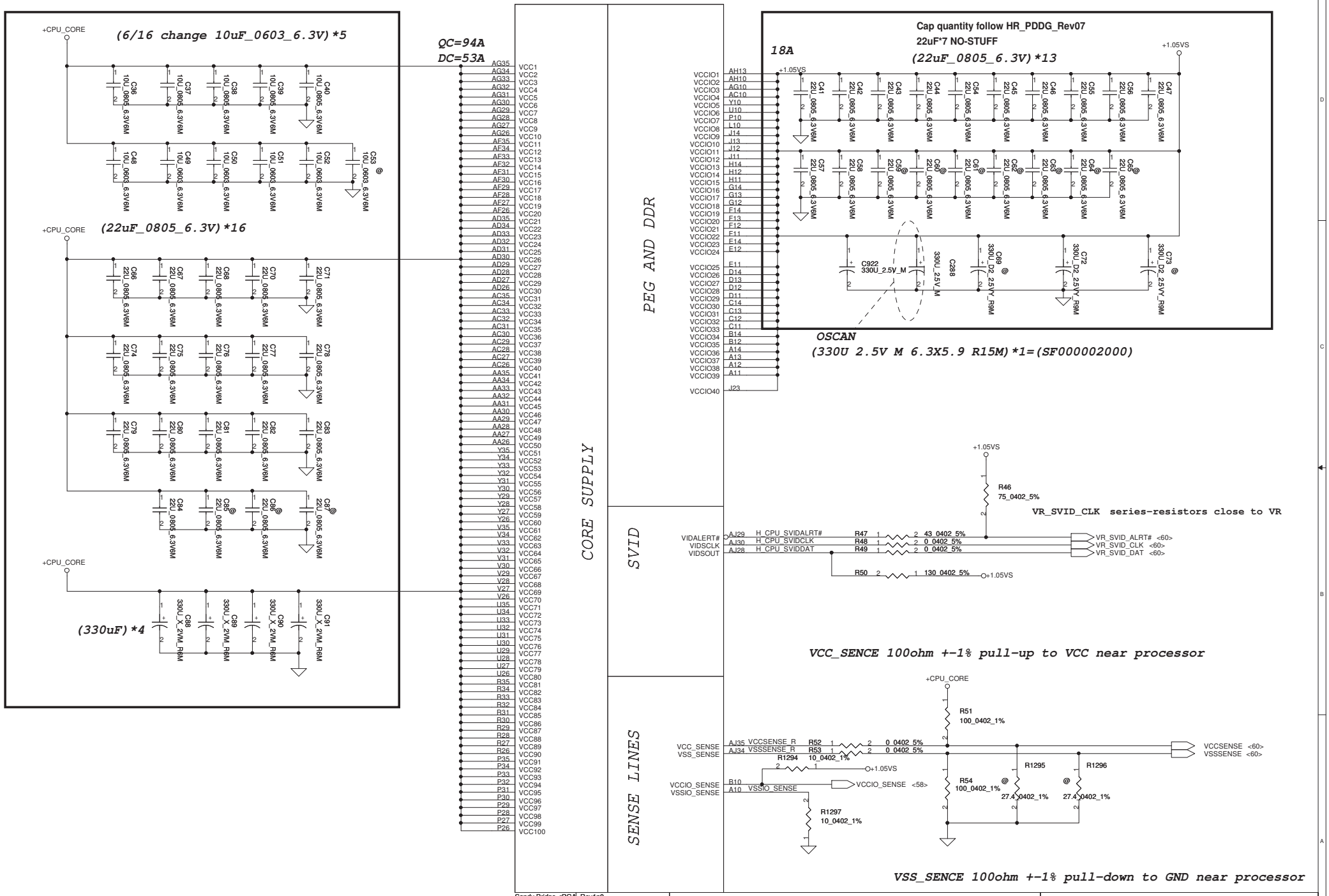
Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 8 of 63



Sandy Bridge_rPGA_Rev1p0
ME@

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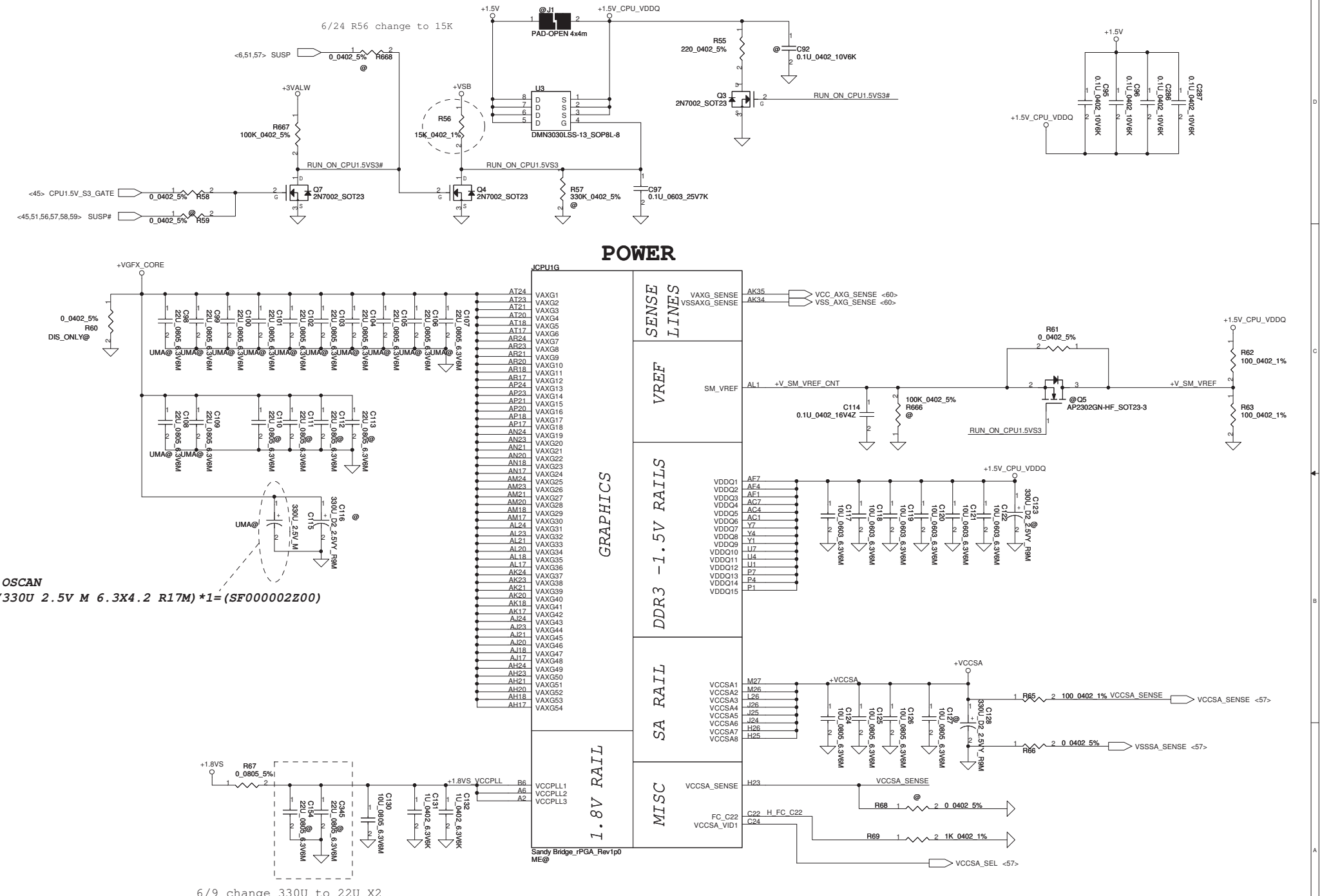
Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 9 of 63

POWER



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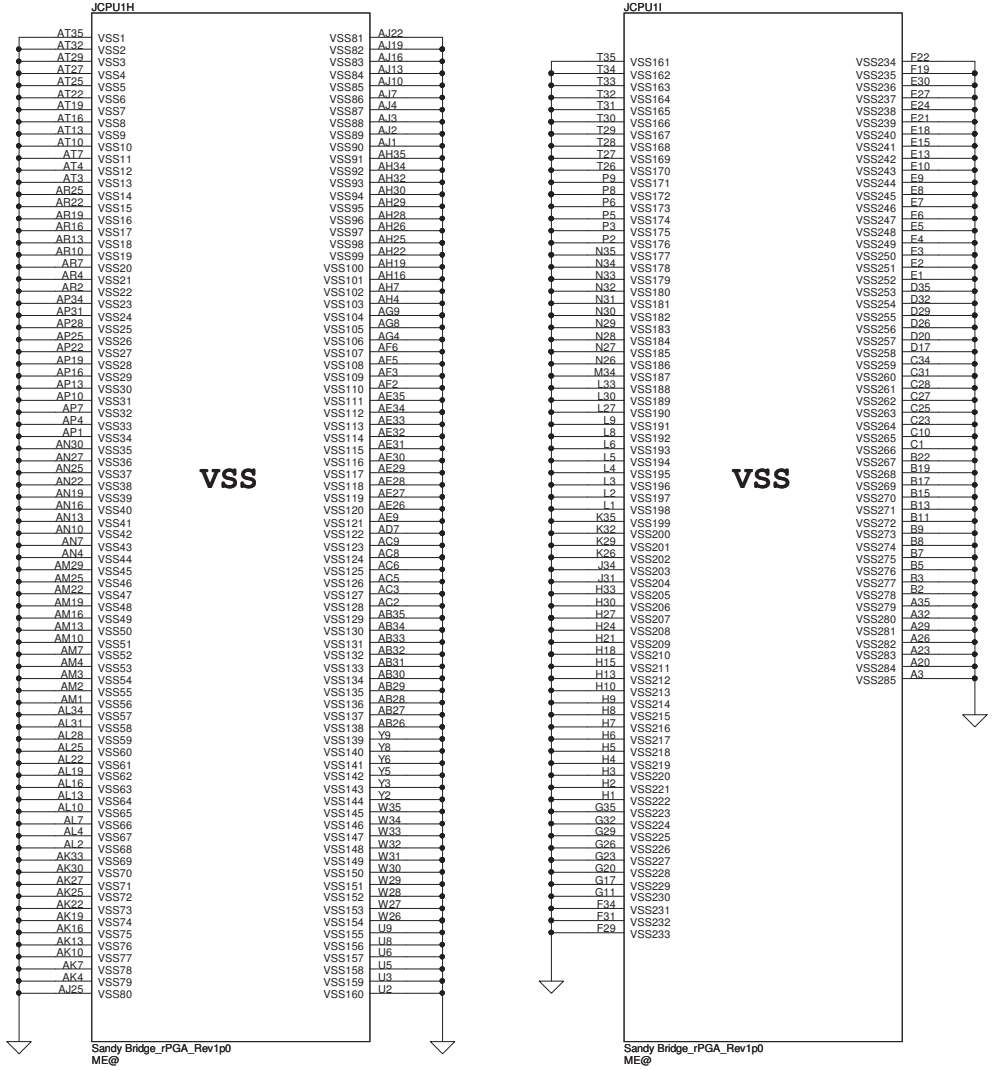
Title: **PROCESSOR(6/7) PWR**

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 10 of 63



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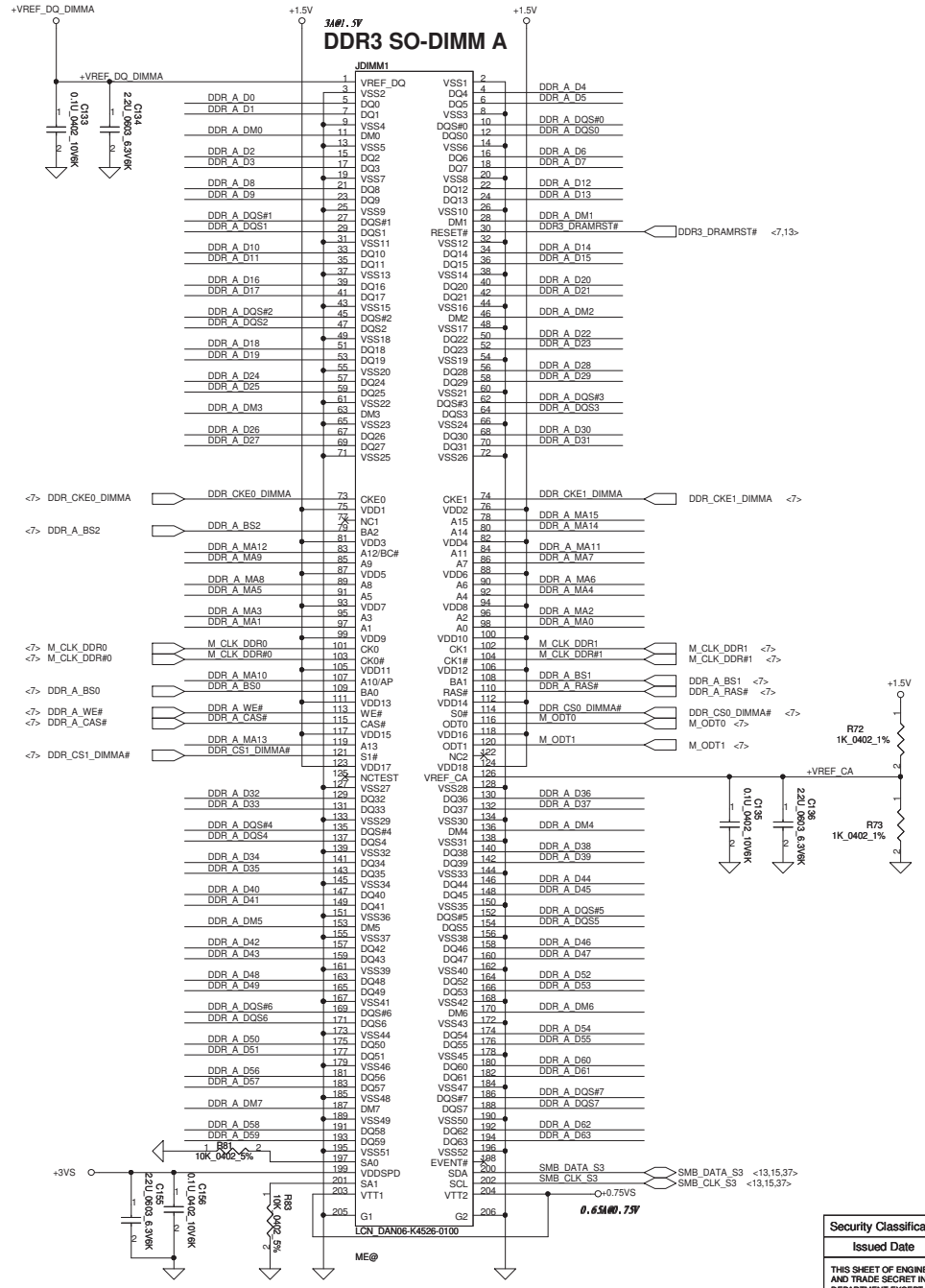
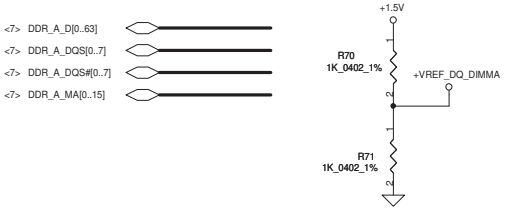
Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 11 of 63



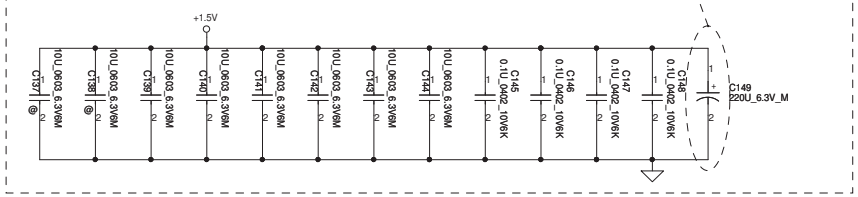


OSCAN (220uF_6.3V_5.9L_ESR15m)*1=(SF000001500)

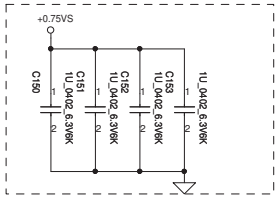
(10uF_0603_6.3V)*8

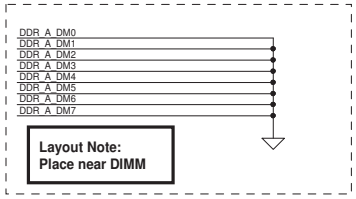
(0.1uF_402_10V)*4

Layout Note: Place near DIMM



Layout Note: Place near DIMM





Layout Note: Place near DIMM

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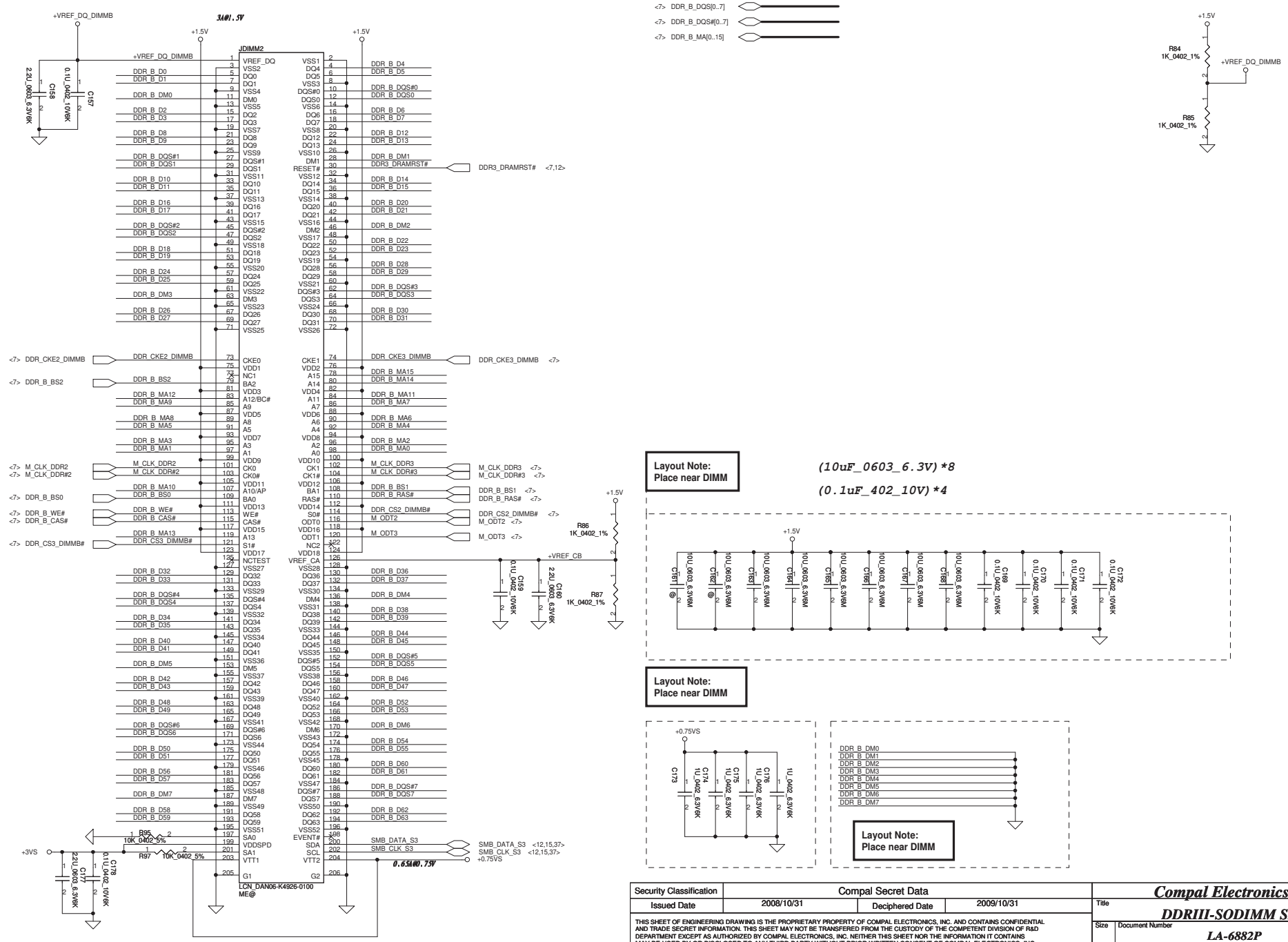
Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 12 of 63



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Title: **DDRIII-SODIMM SLOT2**

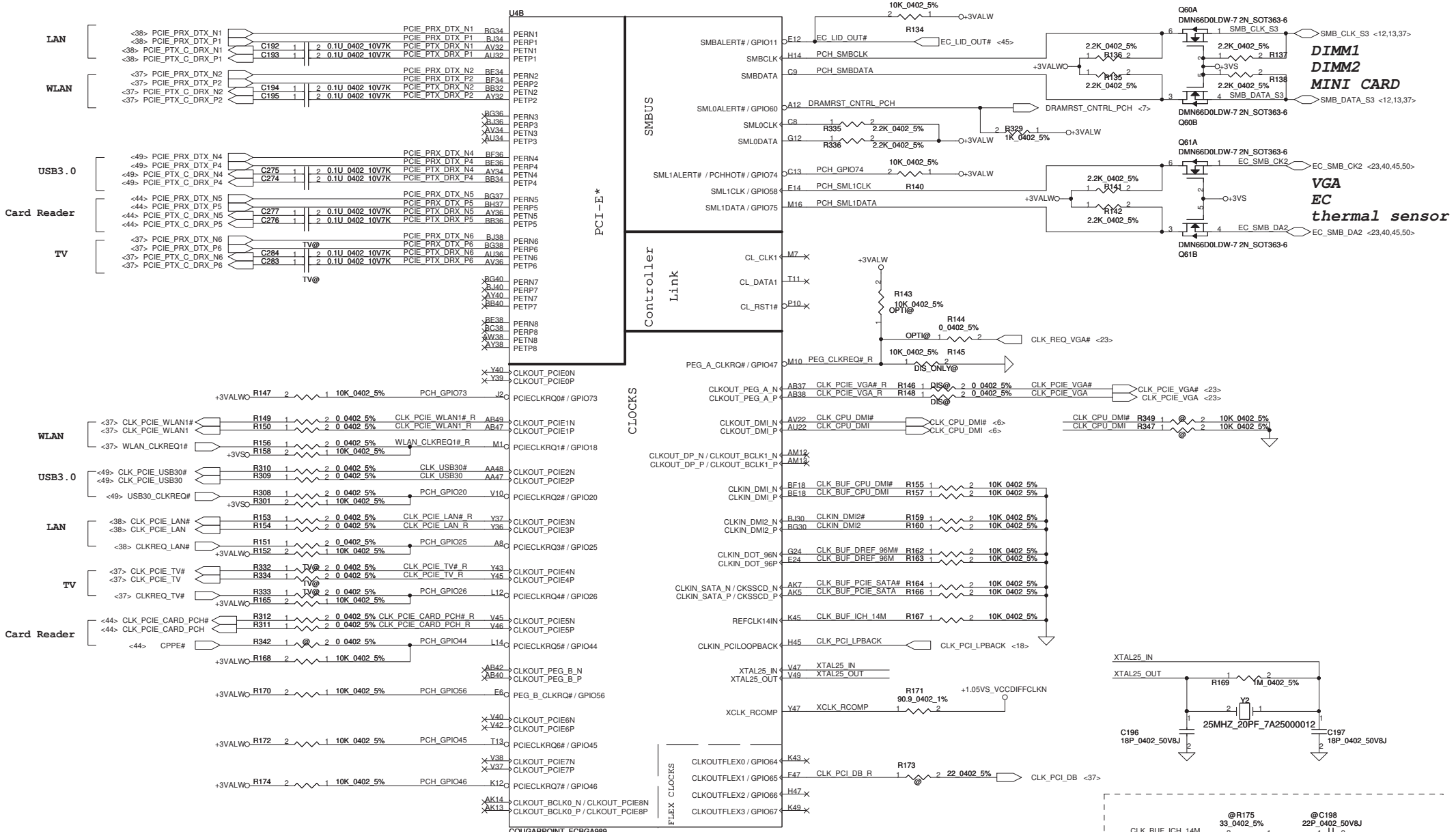
Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 13 of 63

W=20mils W=20mils
+RTCVCC +RTCBATT
R99 1K_0402_5%
C179 1U_0603_10V4Z
CLRP1 SHORT PADS
PCH_RTCX1 PCH_RTCX2
R98 10M_0402_5%
18P_0402_50V8J C180
Y1 32.768KHZ_12.5PF_9H03200413
C181 18P_0402_50V8J
CMOS
+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
R1330 330K_0402_5%
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
+3VS
R105 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)
★ LOW= Disable (Default)
+3VALW
R106 1K_0402_5% HDA_SDOUT
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
+3VALW
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR Select is supplied by
★ 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
R112 33_0402_5% HDA_BIT_CLK
R114 33_0402_5% HDA_SYNC_R
R116 33_0402_5% HDA_RST#
R118 33_0402_5% HDA_SDOUT
<42> HDA_BITCLK_AUDIO
<42> HDA_SYNC_AUDIO
<42> HDA_RST_AUDIO#
<42> HDA_SDOUT_AUDIO
+3VS
Q10 BSS138_NL_SOT23-3
@R325 0_0402_5%
+3VALW +3VALW +3VALW
R121 200_0402_5% PCH_JTAG_TDO
R122 200_0402_5% PCH_JTAG_TMS
R123 200_0402_5% PCH_JTAG_TDI
R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1
6/30 update R121, R122, R123
6/17 follow module design
U4A
COUGARPOINT_FCBGA989
RTC: PCH_RTCX1 A20, PCH_RTCX2 C20, PCH_RTCRST# D20, PCH_SRTCRST# G22, SM_INTRUDER# K22, PCH_INTVRMEN C17
IHDA: HDA_BIT_CLK N34, HDA_SYNC L34, HDA_SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN# / GPIO33 C36, HDA_DOCK_RST# / GPIO13 N32
<42> HDA_SPKR
<42> HDA_SDIN0
<45> ME_FLASH
R109 0_0402_5% HDA_SDOUT
R107 1K_0402_1% PCH_GPIO33
<49> Kill_SW#
JTAG: PCH_JTAG_TCK J3, PCH_JTAG_TMS H7, PCH_JTAG_TDI K5, PCH_JTAG_TDO H1
R110 51_0402_5%
SPI: SPI_CLK_PCH T3, SPI_SB_CS0# Y14, SPI_SB_CS1# T1, SPI_SI V4, SPI_SO_R U3
SPI_CS0#, SPI_MOSI, SPI_MISO
LPC: FWH0 / LAD0 C38, FWH1 / LAD1 A38, FWH2 / LAD2 B37, FWH3 / LAD3 C37, FWH4 / LFRAME# D36, LDRQ0# E36, LDRQ1# / GPIO23 K36, SERIRQ V5
LPC_AD0 <37,45>, LPC_AD1 <37,45>, LPC_AD2 <37,45>, LPC_AD3 <37,45>, LPC_FRAME# <37,45>
EC and Mini card debug port
R104 10K_0402_5% +3VS
SERIRQ <45>
SATA 6G: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5; SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10; SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4; SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1
SATA: SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1; SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1; SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP / GPIO21 V14, SATA1GP / GPIO19 P1
SATA_COMP R111 37.4_0402_1% +1.05VS_VCC_SATA
SATA3_COMP R113 49.9_0402_1% +1.05VS_SATA3
RBIAS_SATA3 R115 750_0402_1%
R117 10K_0402_5% +3VS
HDD_LED# <50>
PCH_GPIO21 R119 10K_0402_5% +3VS
SATA_DET# <37>
R316 10K_0402_5% +3VS
SATA_DTX_C_IRX_N0 / SATA_DTX_C_IRX_P0 <37>
SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184 SATA_ITX_DRX_N0
SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185 SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0 <37>, SATA_DTX_C_IRX_P0 <37>, SATA_ITX_DRX_N0 <37>, SATA_ITX_DRX_P0 <37>
SSD
SATA_DTX_C_IRX_N1 / SATA_DTX_C_IRX_P1 <41>
SATA_ITX_C_DRX_N1 0.01U_0402_16V7K C273 SATA_ITX_DRX_N1
SATA_ITX_C_DRX_P1 0.01U_0402_16V7K C272 SATA_ITX_DRX_P1
SATA_DTX_C_IRX_N1 <41>, SATA_DTX_C_IRX_P1 <41>, SATA_ITX_DRX_N1 <41>, SATA_ITX_DRX_P1 <41>
HDD
SATA_DTX_C_IRX_N2 / SATA_DTX_C_IRX_P2 <41>
SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186 SATA_ITX_DRX_N2_CONN
SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187 SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2 <41>, SATA_DTX_C_IRX_P2 <41>, SATA_ITX_DRX_N2_CONN <41>, SATA_ITX_DRX_P2_CONN <41>
ODD
ESATA@
SATA_DTX_C_IRX_N4 / SATA_DTX_C_IRX_P4 <48>
SATA_ITX_C_DRX_N4 0.01U_0402_16V7K C188 SATA_ITX_DRX_N4
SATA_ITX_C_DRX_P4 0.01U_0402_16V7K C189 SATA_ITX_DRX_P4
SATA_DTX_C_IRX_N4 <48>, SATA_DTX_C_IRX_P4 <48>, SATA_ITX_DRX_N4 <48>, SATA_ITX_DRX_P4 <48>
ESATA
4MB SPI ROM FOR ME & Non-share ROM.
For Fast Boot
R1334 3.3K_0402_5% SPI_WP#_1
R1335 3.3K_0402_5% SPI_HOLD#_1
@R1337 0_0402_5%
@33_0402_5% R1338
U61
S IC FL 32M W25Q32BVSSIG SOIC 8P
C923 0.1U_0402_16V4Z
33_0402_5% R1340
33_0402_5% R1339
R1346 10K_0402_5%
Q134 2N7002_SOT23-3
<45> SPI_SB_CS0#_R
SPI_SB_CS1#_R
4MB SPI ROM FOR ME & Non-share ROM.
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#
R130 0_0402_5%
33_0402_5% R131
U5
S IC FL 32M W25Q32BVSSIG SOIC 8P
C191 0.1U_0402_16V4Z
R124 33_0402_5%
C190 22P_0402_50V8J
33_0402_5% R1342
33_0402_5% R133

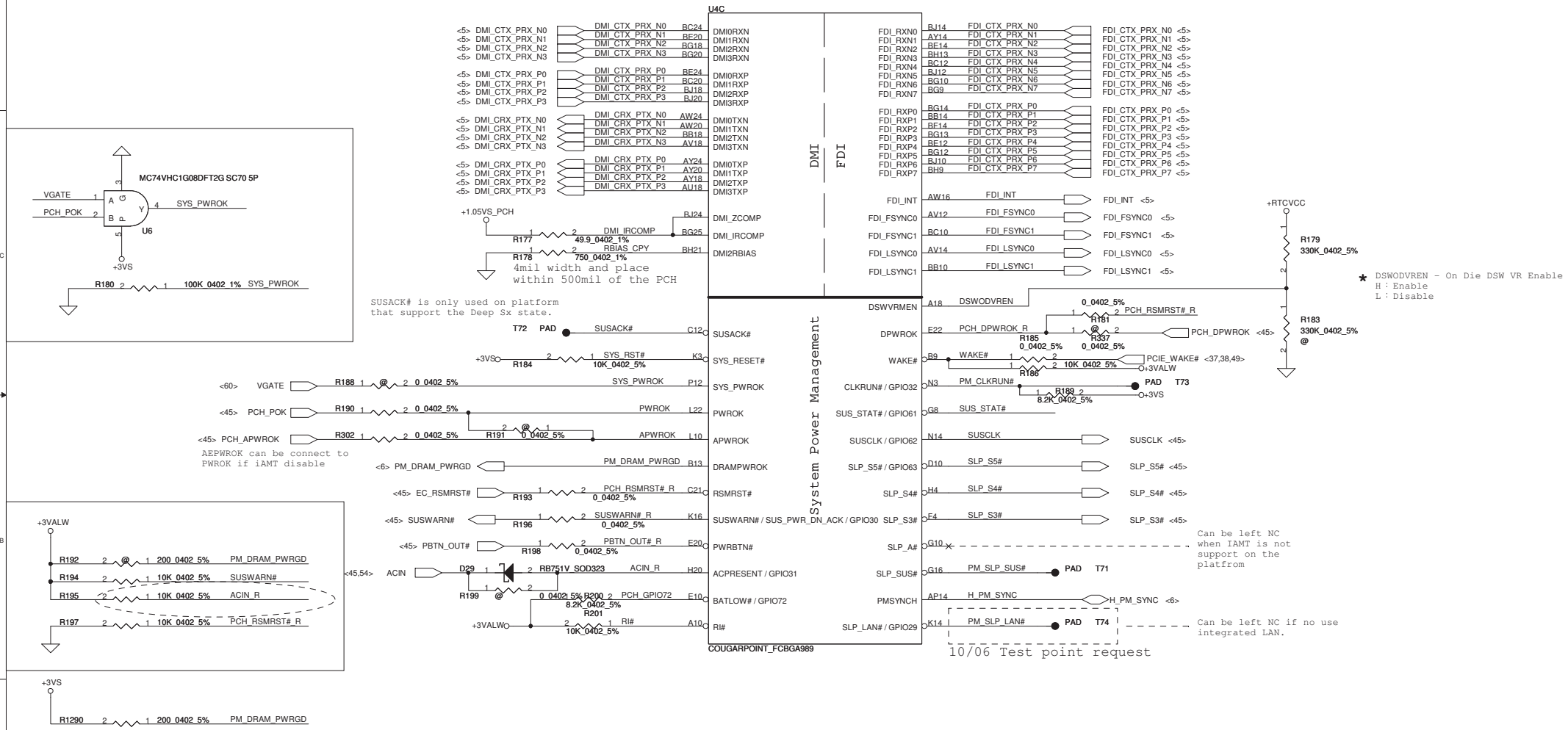
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-6882P | Rev: 0.2
Date: Wednesday, October 06, 2010 | Sheet 14 of 63



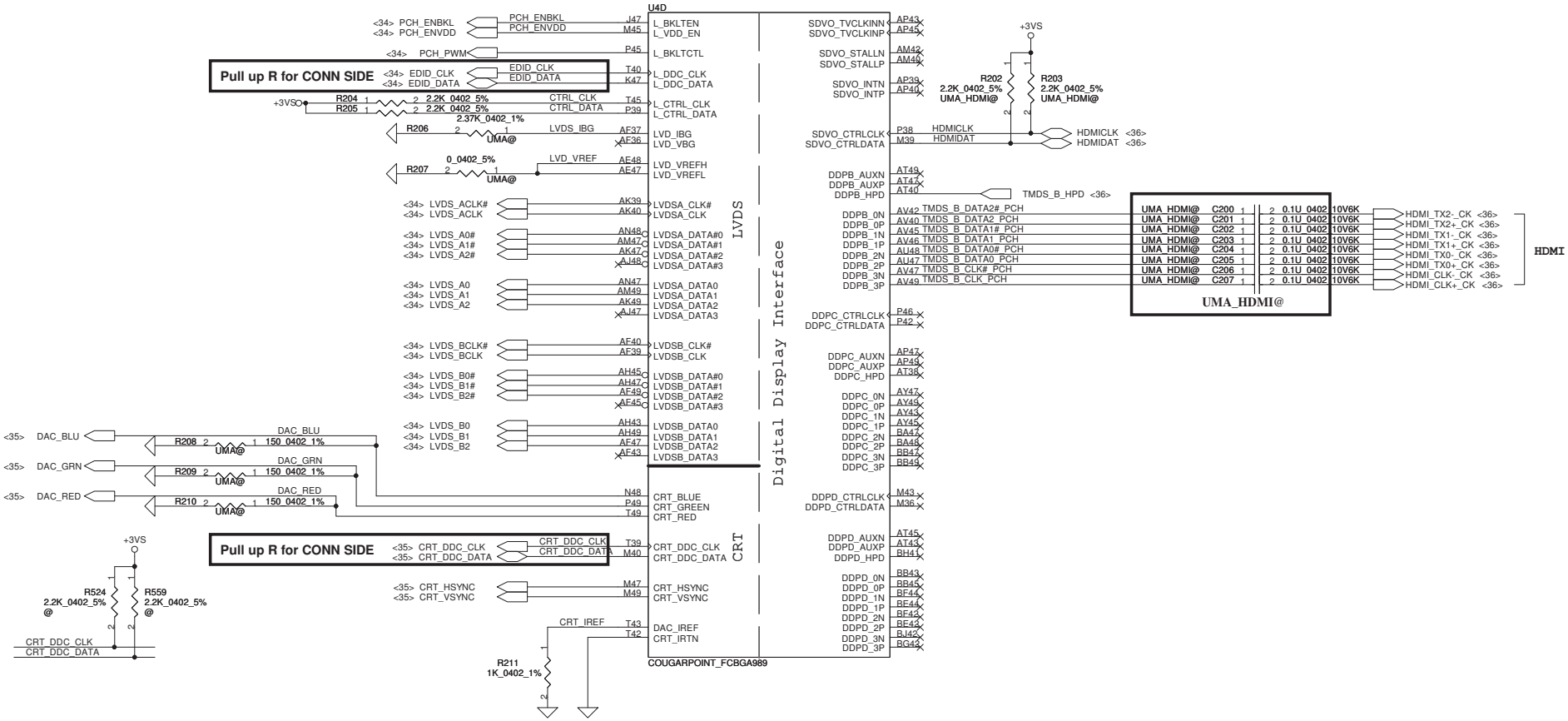
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	PCH (2/8) PCIE, SMBUS, CLK
Size: Custom	Document Number: LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 15 of 63



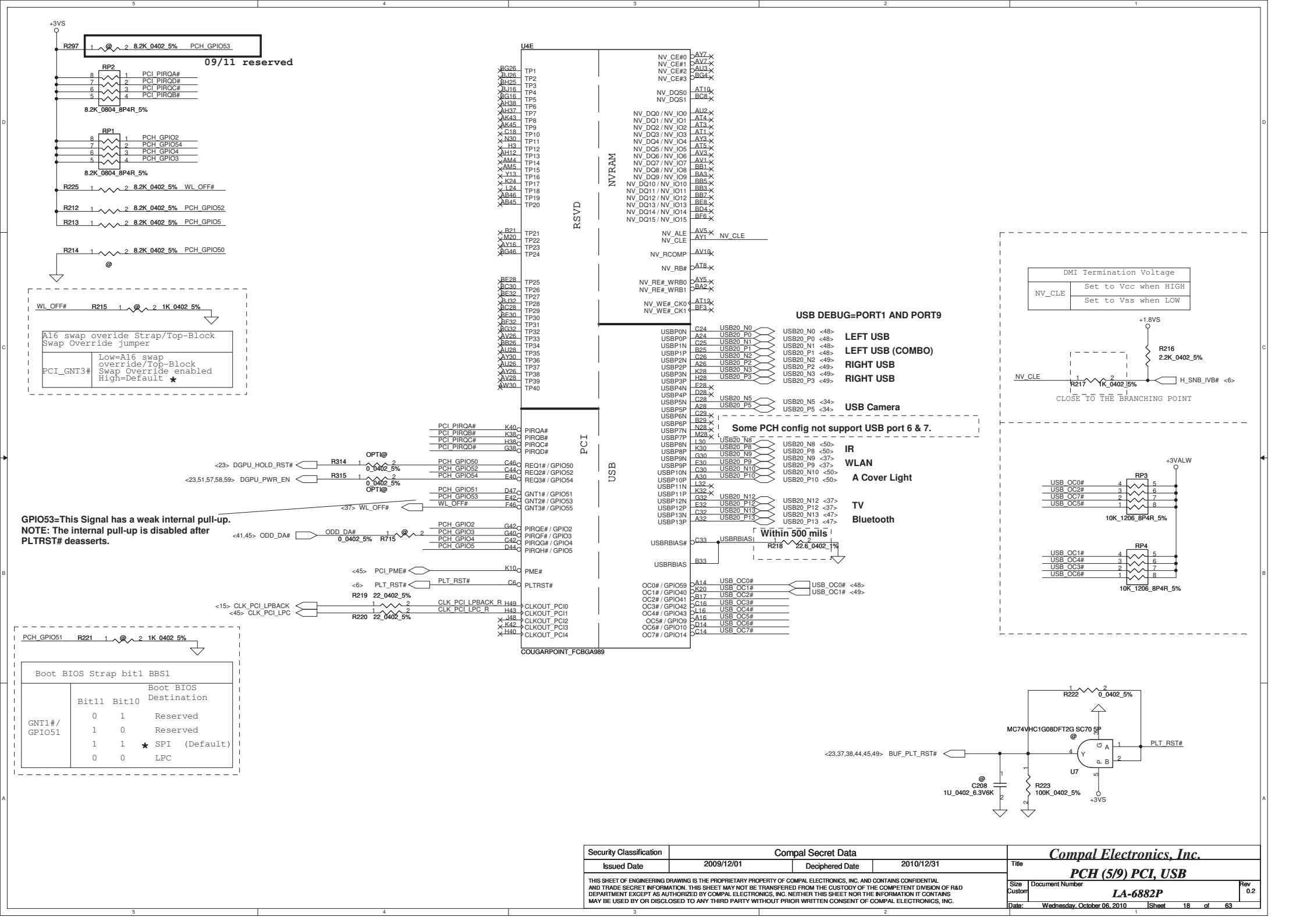
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,		
Size: Custom	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 16 of 63		



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

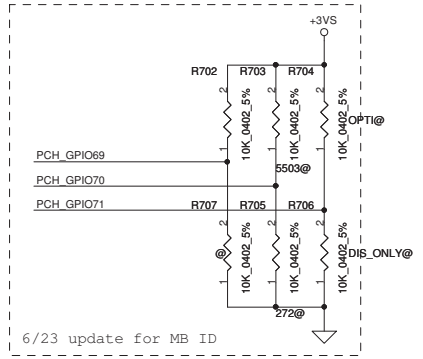
Compal Electronics, Inc.	
Title	PCH (4/9) LVDS,CRT,DP,HDMI
Size: Custom	Document Number: LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 17 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	PCH (5/9) PCI, USB
Size: Custom	Document Number: LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 18 of 63

GPIO69	GPIO70	GPIO71
14": Low 15": Hi	ALC272: Low ALC5503: Hi	DIS ONLY: Low OPTIMUS: Hi
1	0	0
1	0	1
1	1	0
1	1	1



6/24 Change to @ follow module design
and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
R235 @ 1K 0402 5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 @ 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 @ 10K 0402 5% PCH_GPIO27

+3VSO R250 @ 200_0402_5% PCH_GPIO36
R264 10K 0402 5%

<48> ESATA_DET# R340 0_0402_5% @ ESATA_DET_RR#
7/29 update for ESATA detect

+3VSO R233 10K 0402 5% PCH_GPIO0
<48> ESATA_DET# R303 0_0402_5% ESATA_DET_R#
+3VSO R227 10K 0402 5% ESATA_DET_R#
+3VSO R228 10K 0402 5% DEVICE_RST#
<37,38,44> DEVICE_RST#
<45> EC_SCI# EC_SCI#
<45> EC_SMI# EC_SMI#
+3VALWO R229 @ 10K 0402 5% PCH_GPIO12
R230 @ 1K_0402_5% SMIB
<49> SMIB
+3VSO R231 10K 0402 5% ESATA_DET_RR#
R232 @ 10K 0402 1%
<23,59> VGA_PGOOD R339 0_0402_5% VGA_PGOOD_R
+3VSO R238 10K 0402 5% BT_DISABLE
<37> BT_DISABLE
<41> ODD_EN ODD_EN
+3VALW
R241 10K 0402 5% PCH_GPIO28
<37,47> BT_OFF#
+3VSO R242 @ 10K 0402 5% BT_OFF#
R243 10K 0402 5% PCH_GPIO35
R259 10K 0402 5% PCH_GPIO36
+3VSO R244 @ 10K 0402 5% PCH_GPIO37
R246 10K 0402 5% PCH_GPIO38
R247 10K 0402 5% PCH_GPIO39
R248 10K 0402 5% PCH_GPIO48
+3VSO R249 10K 0402 5% PCH_GPIO49
+3VALWO R251 @ 10K 0402 5% PCH_GPIO57
NO_VENTURA@
R1345 10K 0402 5%
VENTURA@

U4F

BMBUSY# / GPIO0	T7	TACH4 / GPIO68	C40 PCH_GPIO68
TACH1 / GPIO1	A42	TACH5 / GPIO69	B41 PCH_GPIO69
TACH2 / GPIO6	H36	TACH6 / GPIO70	C41 PCH_GPIO70
TACH3 / GPIO7	E38	TACH7 / GPIO71	A40 PCH_GPIO71
GPIO8	C10		
LAN_PHY_PWR_CTRL / GPIO12	C4		
GPIO15	G2	A20GATE	P4 GATEA20 <45>
SATA4GP / GPIO16	U2	PECI	AU16 PCH_PECI_R 0_0402_5% R237 H_PECI <6,45>
TACH0 / GPIO17	D40	RCIN#	P5 KB_RST# KB_RST# <45>
SCLOCK / GPIO22	T5	PROCPWRGD	AY11 H_CPUPWRGD <6>
GPIO24 / MEM_LED	E8	THRMTRIP#	AY10 PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
GPIO27	E16	INIT3_3V#	T14 PCH_THRMTRIP#_R <23>
GPIO28	P8		
STP_PCI# / GPIO34	K1	NC_1	AH8
GPIO35	K4	NC_2	AK11
SATA2GP / GPIO36	V8	NC_3	AH10
SATA3GP / GPIO37	M5	NC_4	AK10
SLOAD / GPIO38	N2	NC_5	P37
SDATAOUT0 / GPIO39	M3		
SDATAOUT1 / GPIO48	V13		
SATA5GP / GPIO49	V3		
GPIO57	D6		

GPIO | CPU/MISC

VSS_NCTF_1	A4	VSS_NCTF_15	BG2 VSS_NCTF_15
VSS_NCTF_2	A44	VSS_NCTF_16	BG48 VSS_NCTF_16
VSS_NCTF_3	A45	VSS_NCTF_17	BH3 VSS_NCTF_17
VSS_NCTF_4	A46	VSS_NCTF_18	BH47 VSS_NCTF_18
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4 VSS_NCTF_19
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44 VSS_NCTF_20
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45 VSS_NCTF_21
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46 VSS_NCTF_22
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5 VSS_NCTF_23
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6 VSS_NCTF_24
VSS_NCTF_11	BE1	VSS_NCTF_25	C2 VSS_NCTF_25
VSS_NCTF_12	BE49	VSS_NCTF_26	C48 VSS_NCTF_26
VSS_NCTF_13	BF1	VSS_NCTF_27	D1 VSS_NCTF_27
VSS_NCTF_14	BF49	VSS_NCTF_28	D49 VSS_NCTF_28
		VSS_NCTF_29	F1 VSS_NCTF_29
		VSS_NCTF_30	F49 VSS_NCTF_30
		VSS_NCTF_31	F1 VSS_NCTF_31
		VSS_NCTF_32	F49 VSS_NCTF_32

NCTF

COUGARPOINT_FCBGA989

+3VS R236 10K_0402_5%
PCH_GPIO68 R224 10K_0402_5%
KB_RST# R226 10K_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

Change VSS_NCTF pin form TEST point to Trace for layout SPACE reducing..

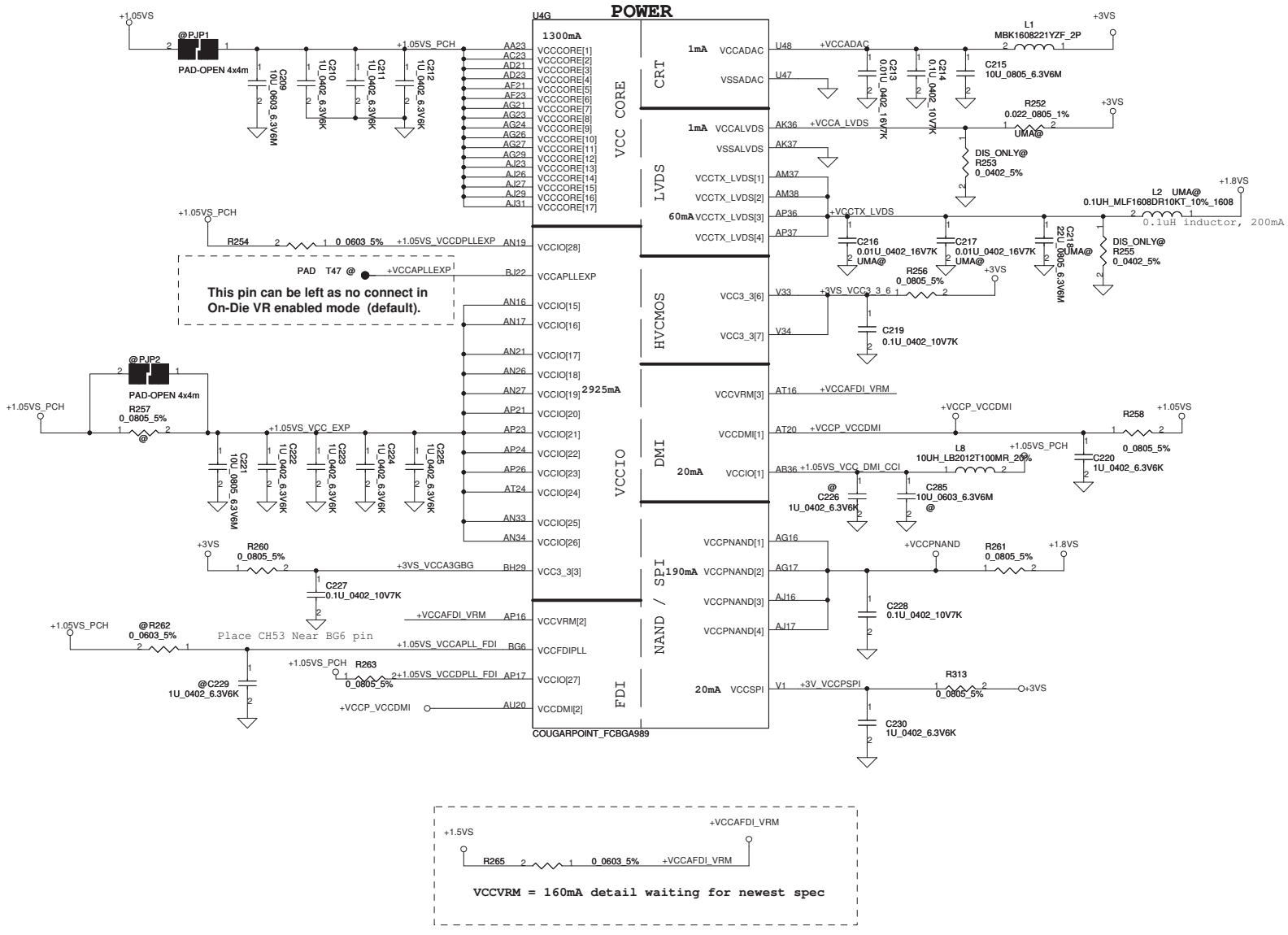
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 19 of 63



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

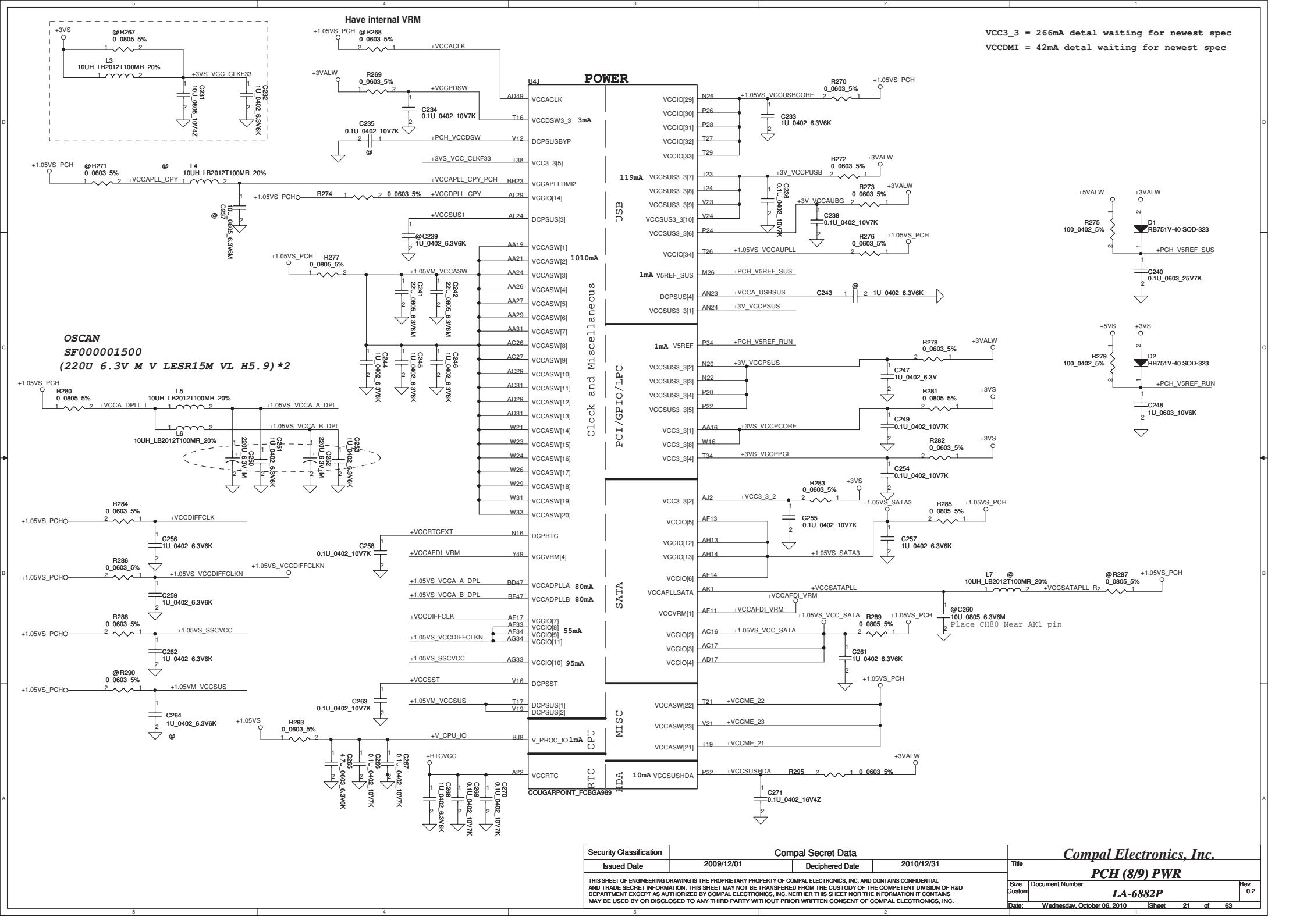
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (7/9) PWR

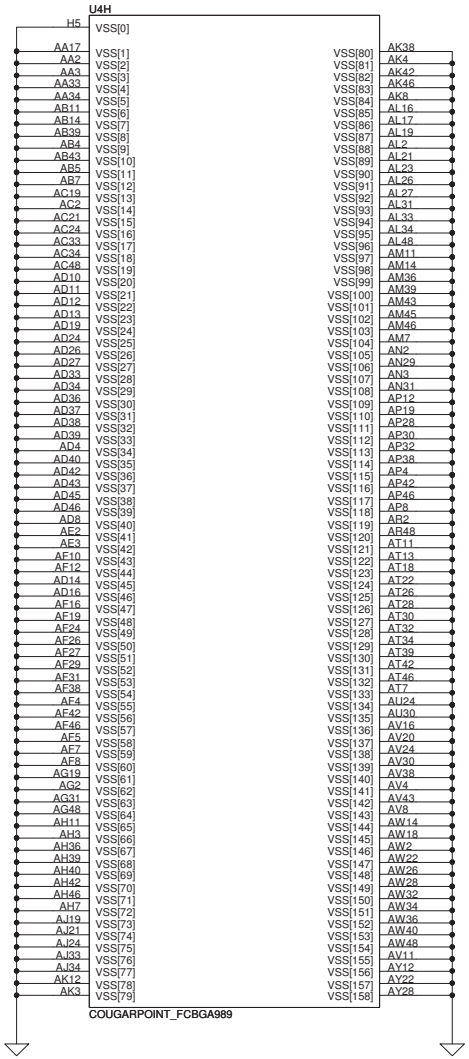
Size: Custom | Document Number: LA-6882P | Rev: 0.2

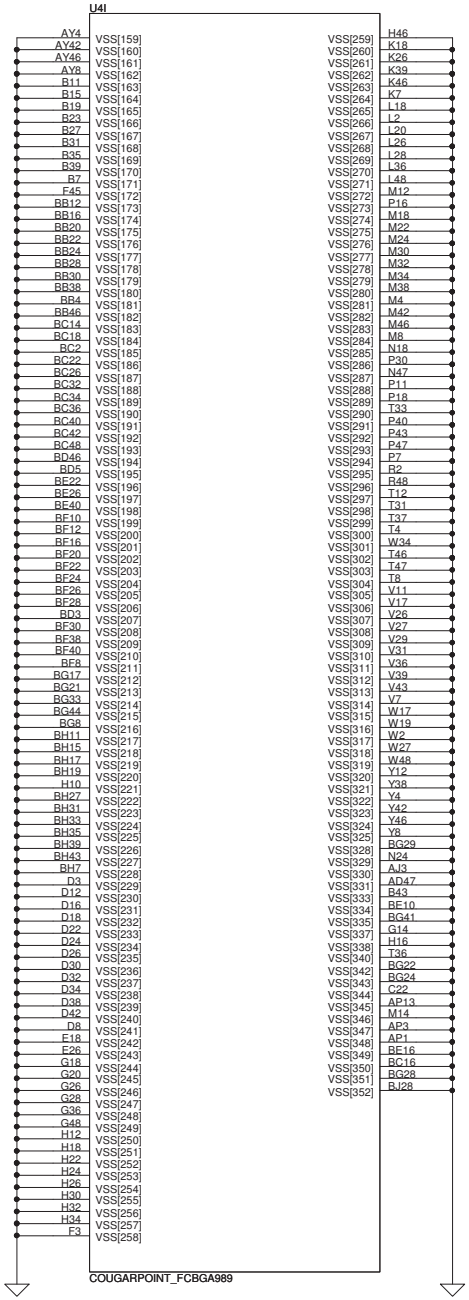
Date: Wednesday, October 06, 2010 | Sheet 20 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

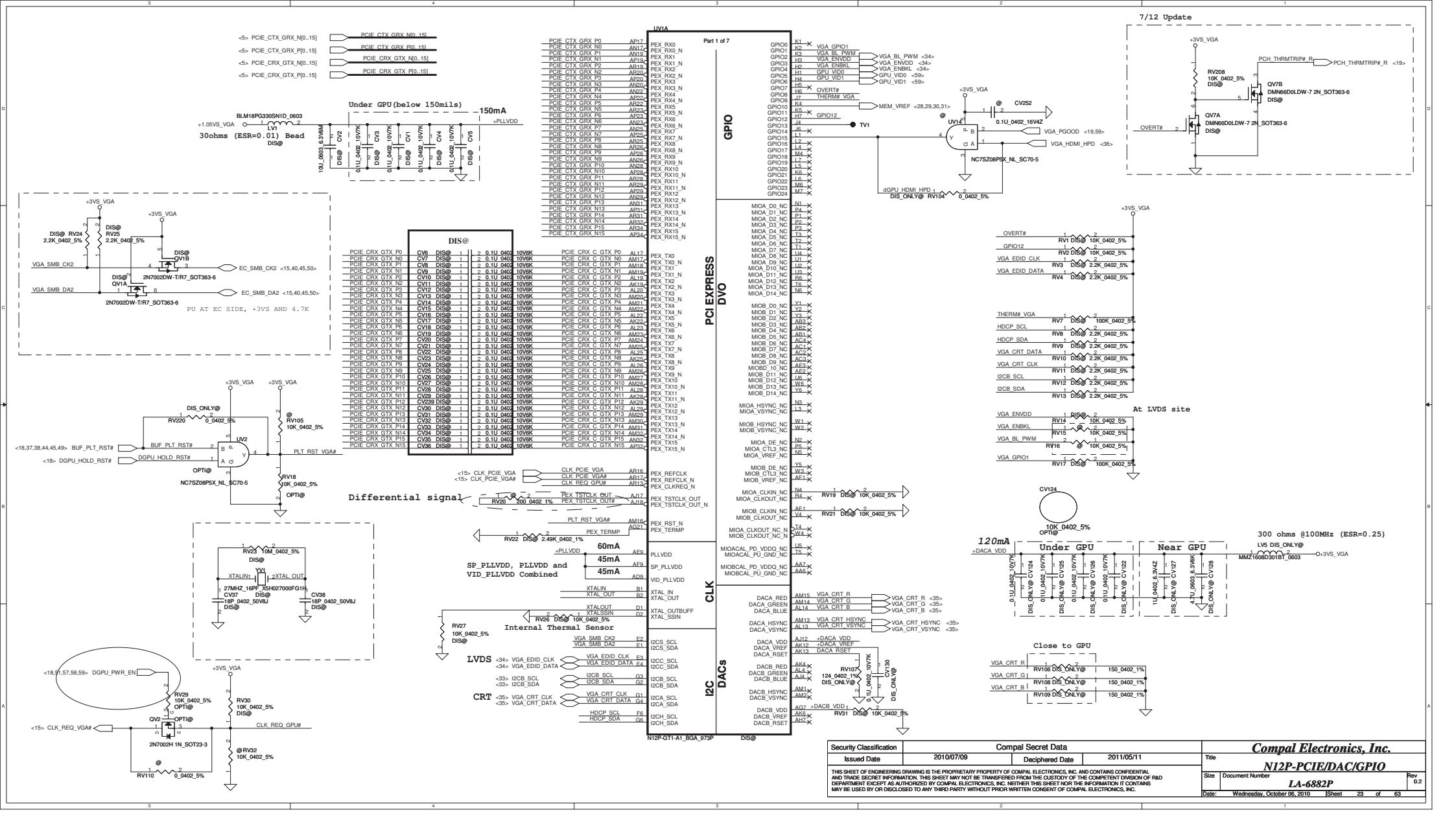
Compal Electronics, Inc.		
Title: PCH (8/9) PWR		
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 21 of 63	





Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.		
Title: PCH (9/9) VSS		
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 22 of 63	



Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

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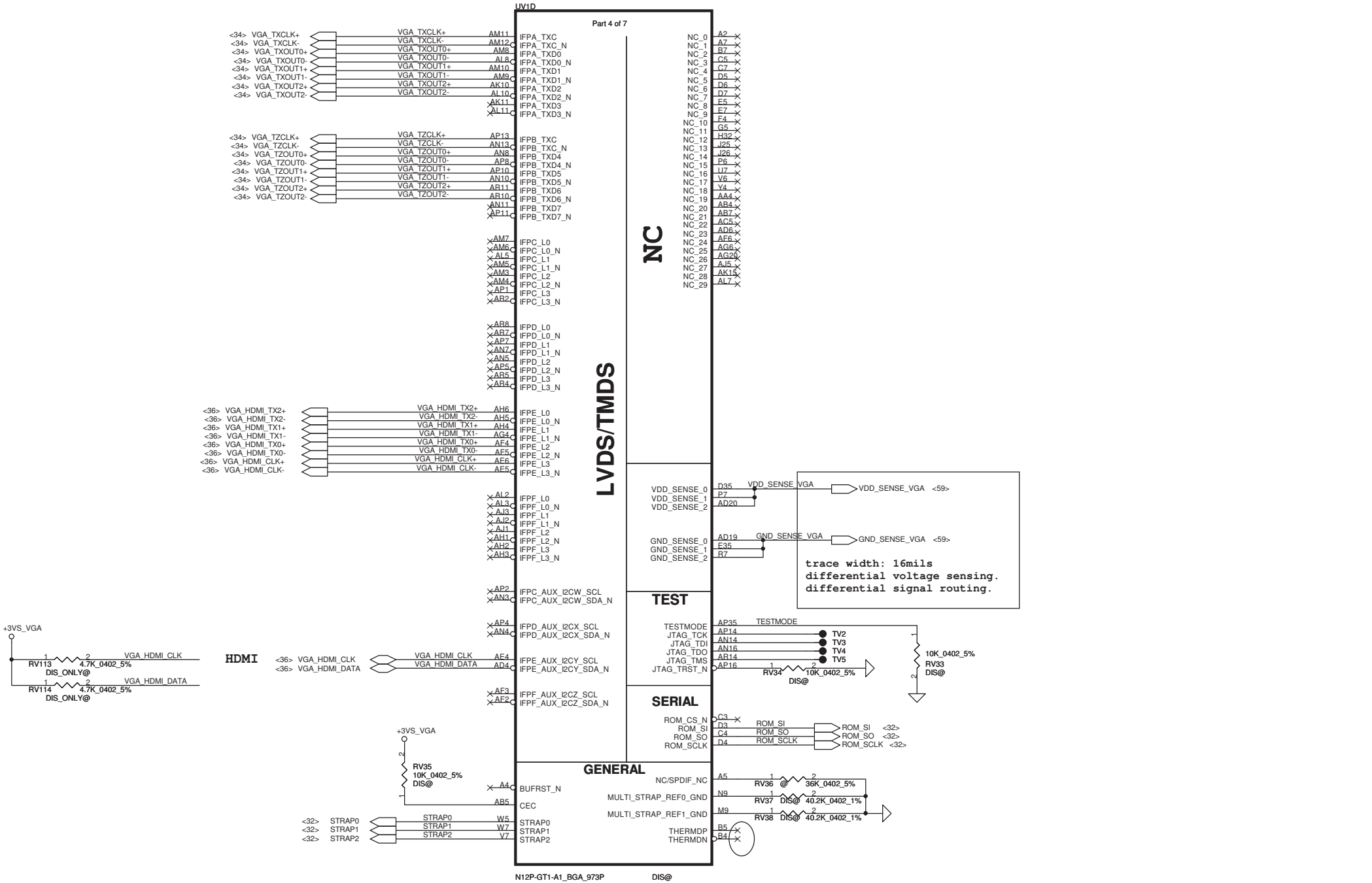
Compal Electronics, Inc.

Title: **N12P-PCIE/DAC/GPIO**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 23 of 63



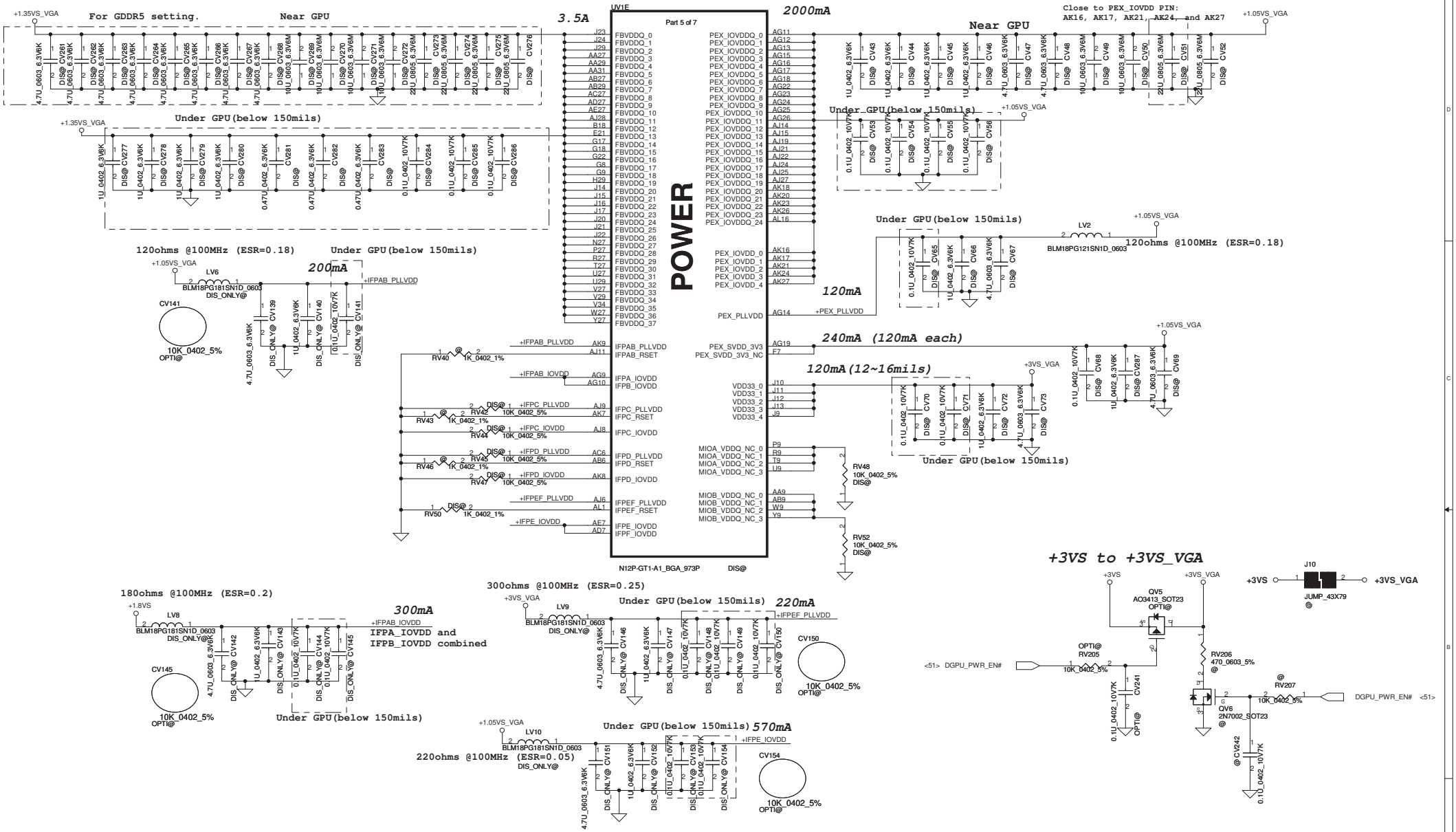
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: **N12P-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 24 of 63



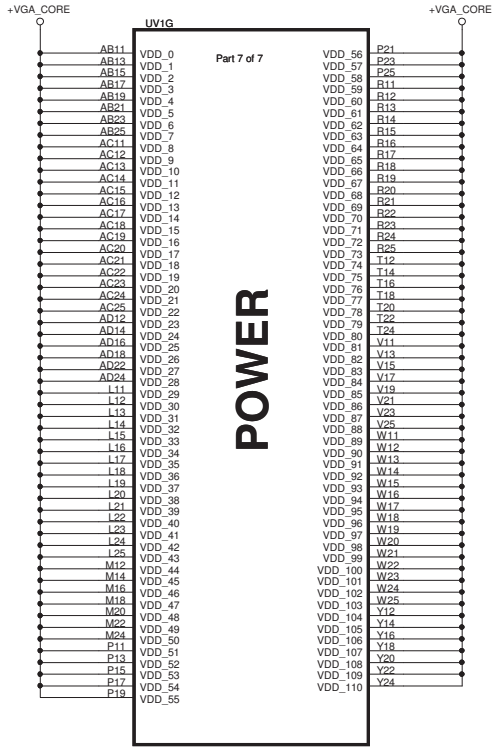
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: **N12P-POWER**

Size	Document Number	Rev
	LA-6882P	0.2

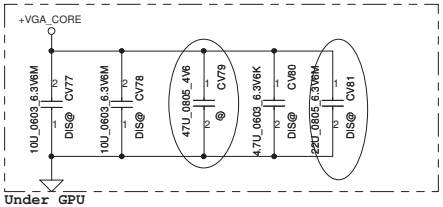
Date: Wednesday, October 06, 2010 | Sheet 25 of 63



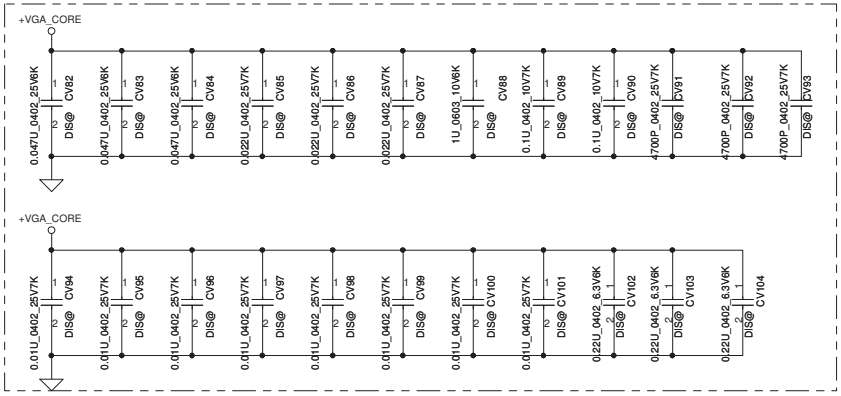
N12P-GT1-A1_BGA_973P

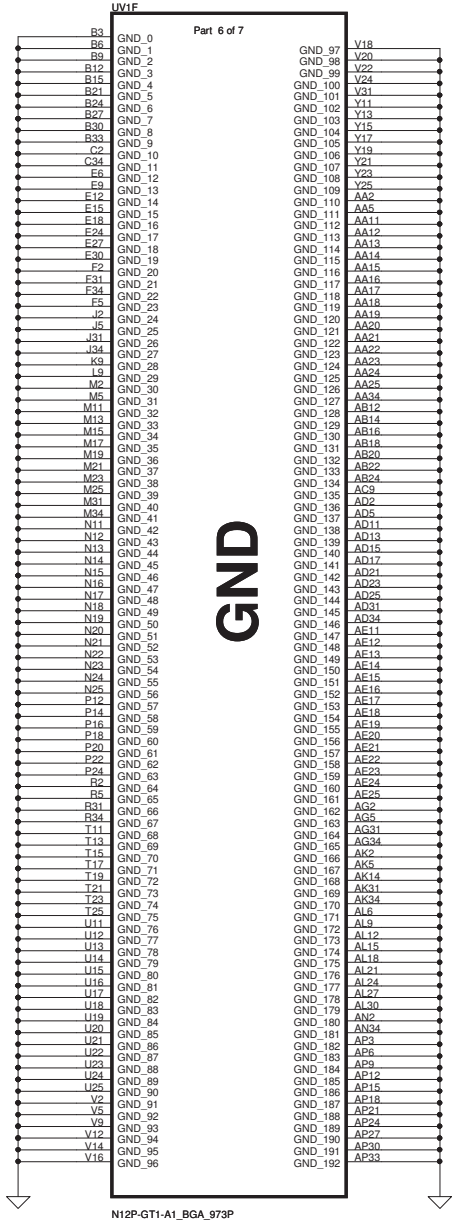
DIS@

Near GPU



Under GPU





N12P-GT1-A1_BGA_973P

DIS@

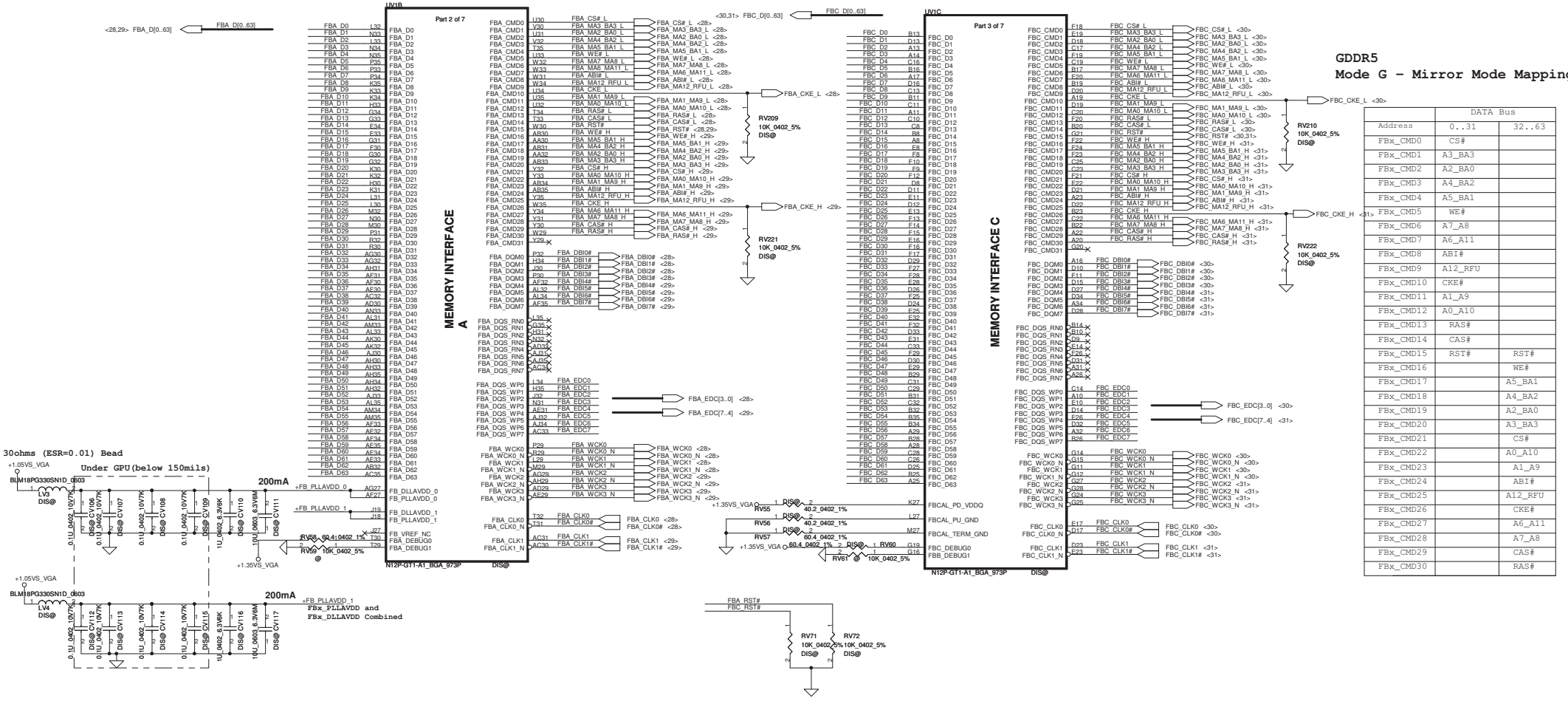
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: N12P-VGA CORE, GND

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 26 of 63



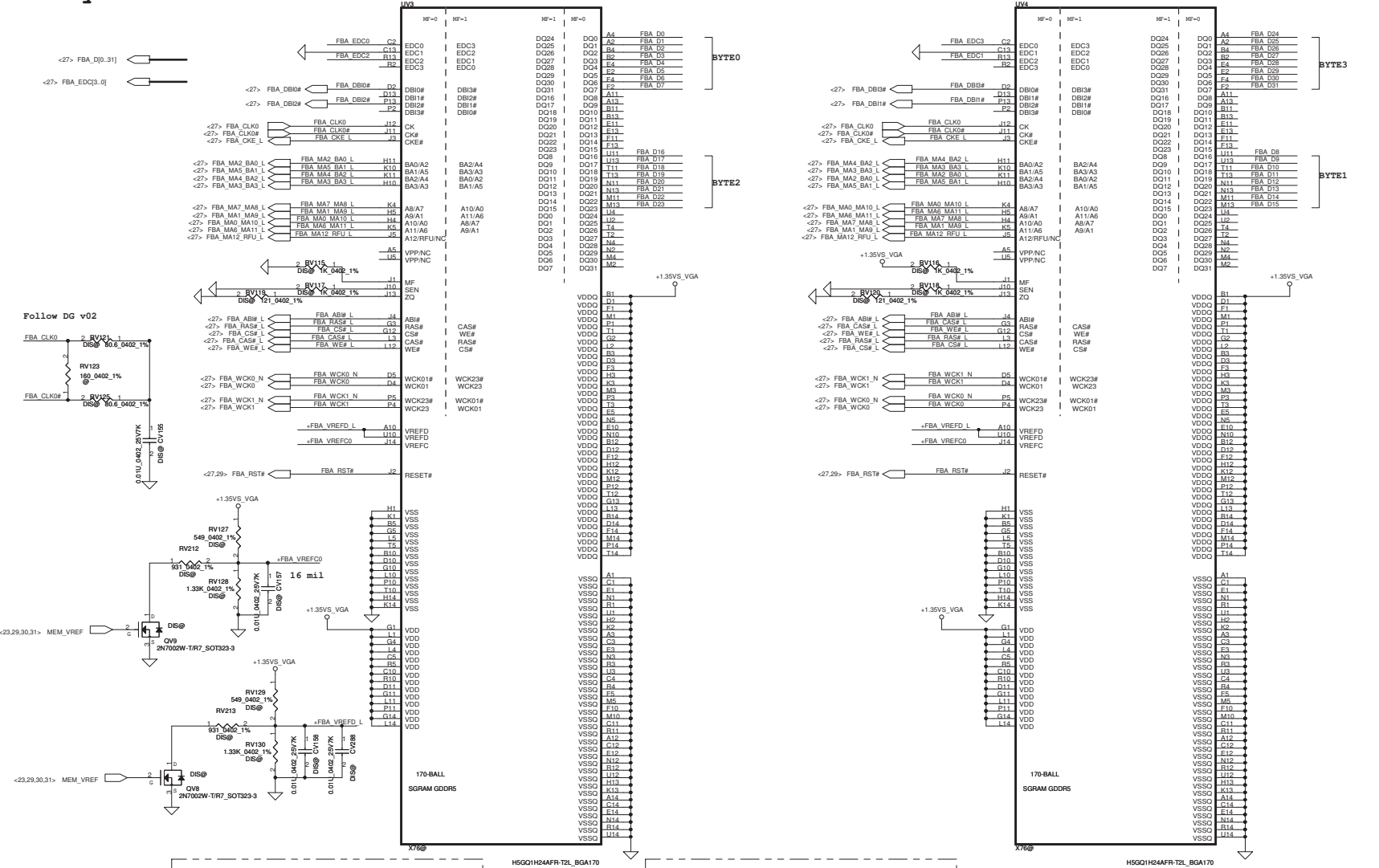
GDDR5
Mode G – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.	
Title	N12P-MEM Interface
Size	Document Number: LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 27 of 63

Memory Partition A - Lower 32 bits



GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

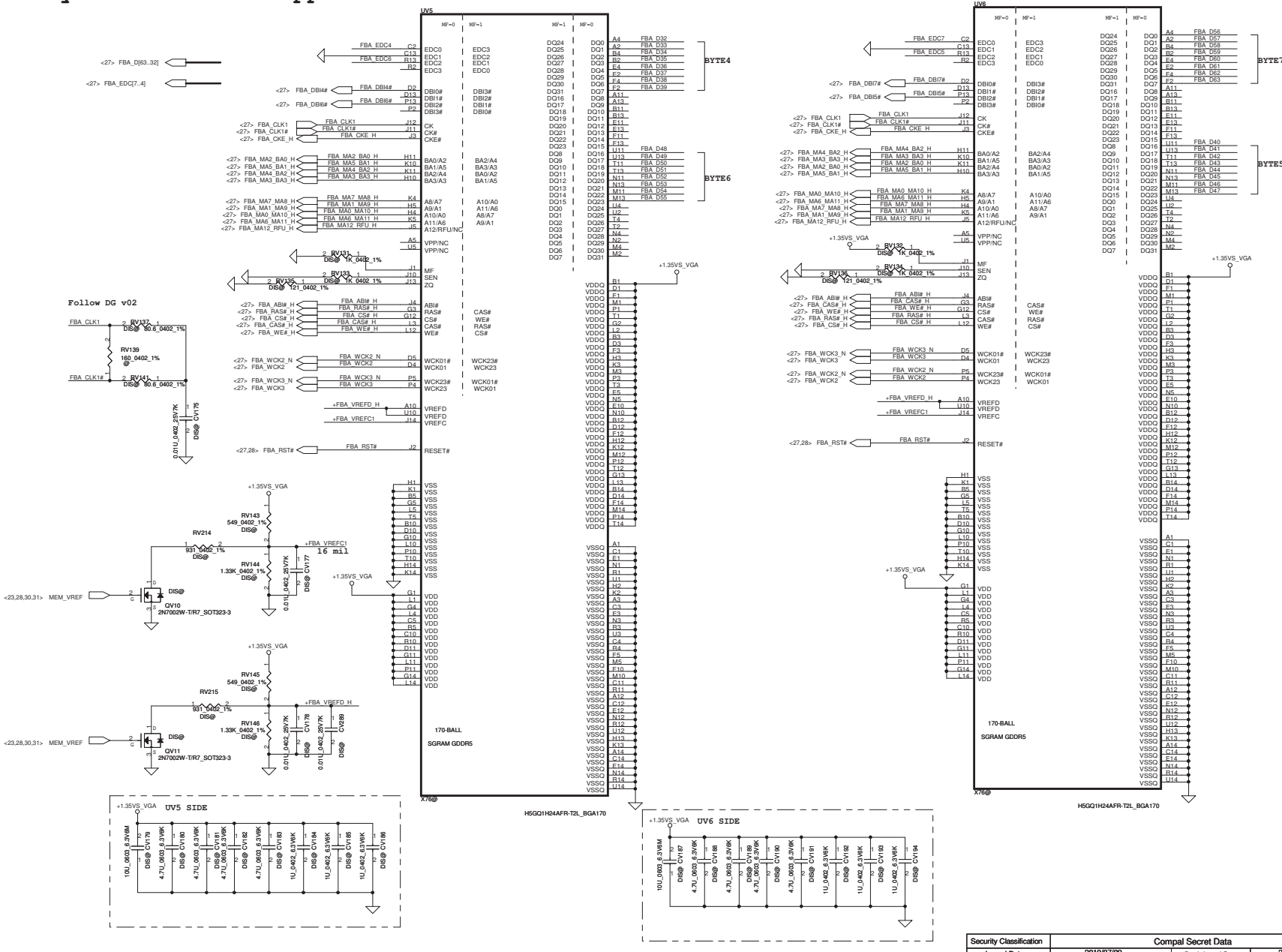
Compal Electronics, Inc.

Title: **N12P-VRAM A Lower**

Size: | Document Number: *LA-6882P* | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 28 of 83

Memory Partition A - Upper 32 bits



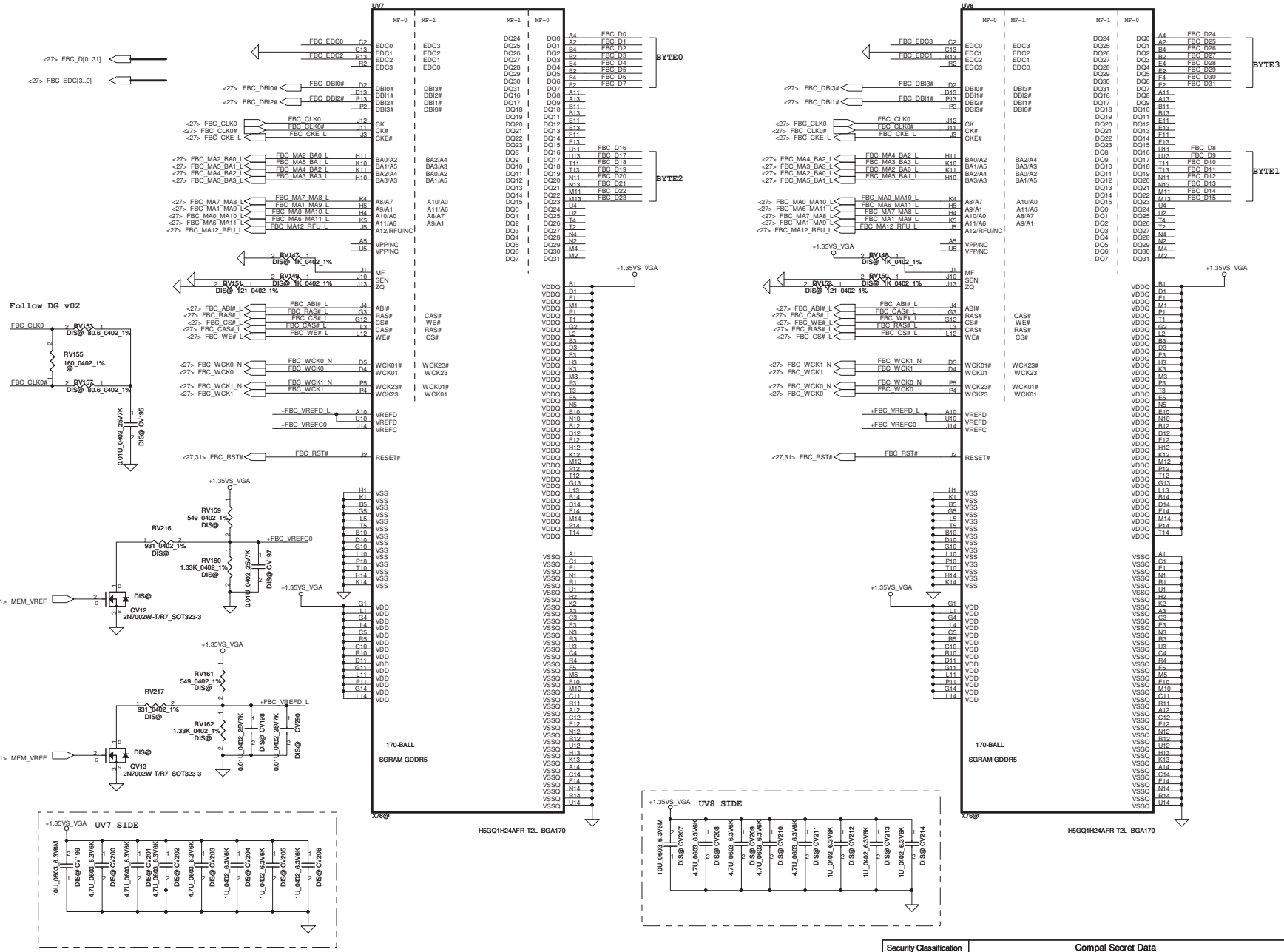
GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.		
Title: N12P-VRAM A Upper		
Size:	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 29 of 83	

Memory Partition C - Lower 32 bits



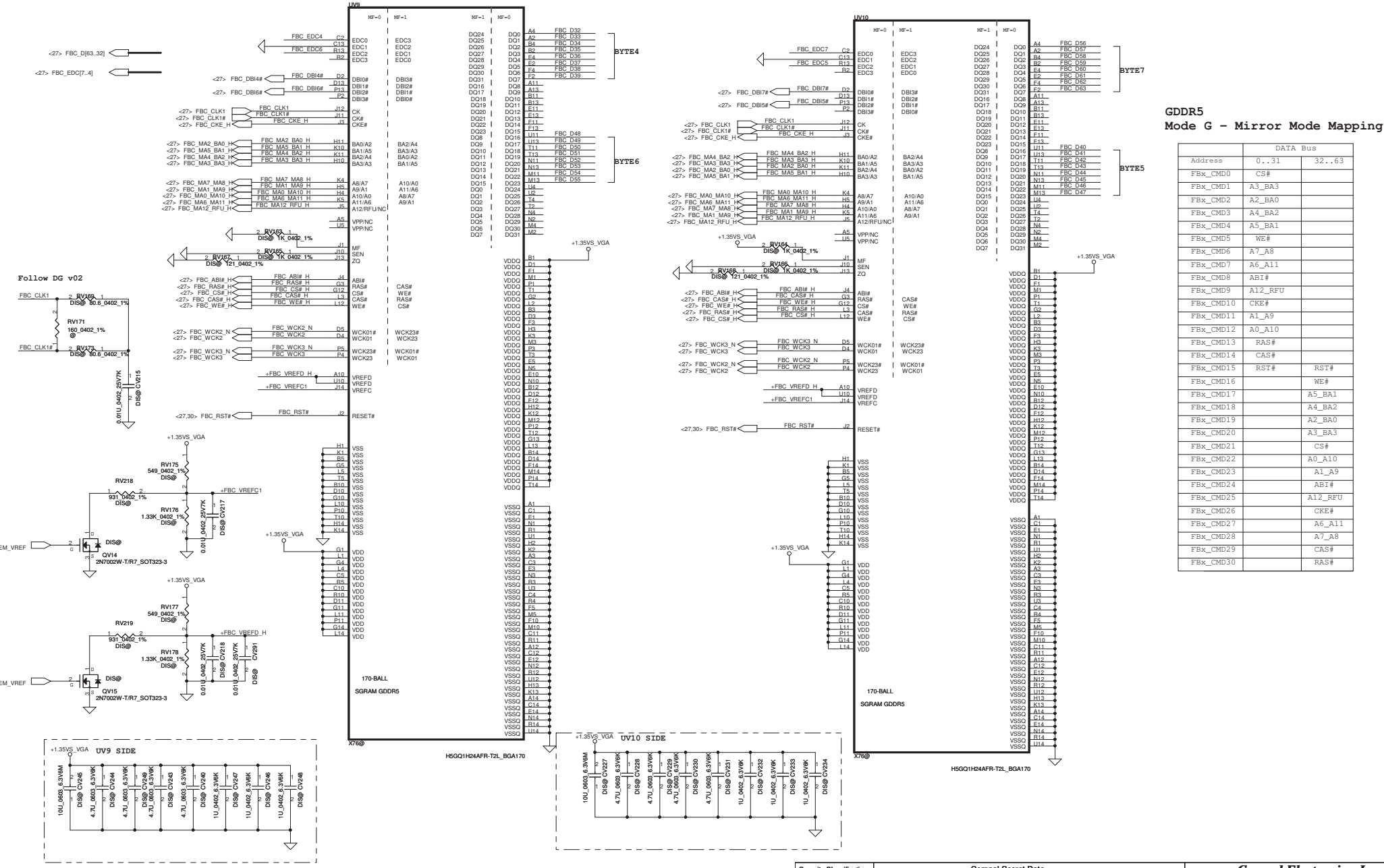
GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.		
Title: N12P-VRAM C Lower		
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 30 of 63	

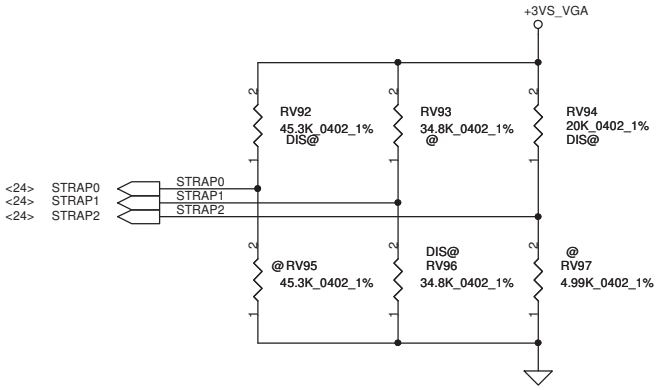
Memory Partition C - Upper 32 bits



GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

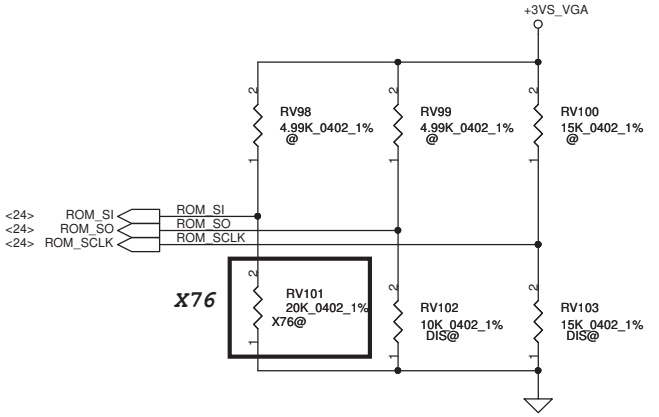
Compal Electronics, Inc.	
Title	N12P-VRAM C Upper
Size: Custom	Document Number: LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 31 of 63



ZZZ
Hynix
H1G@
X7625938L01

ZZZ
Samsung
S1G@
X7625938L02

ZZZ
Samsung
S2G@
X7625938L03



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	FB Memory (GDDR5)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (defaul)	K4G10325FE-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
					X76			

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

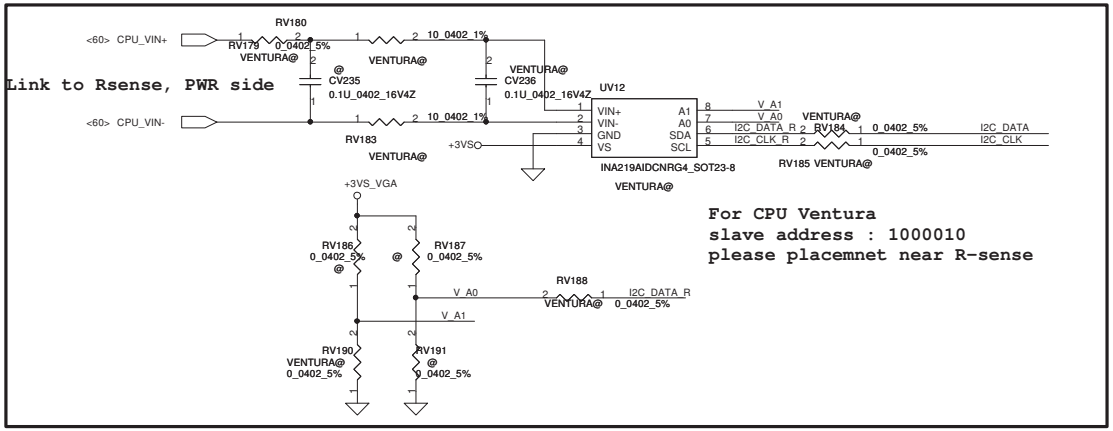
Compal Electronics, Inc.

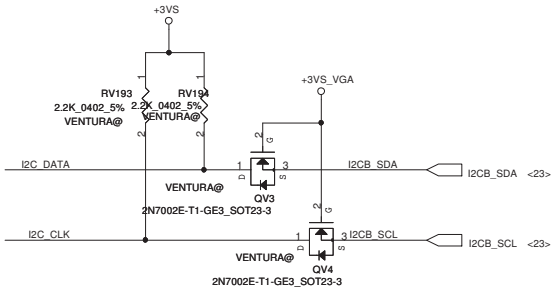
Title: N12P_MISC

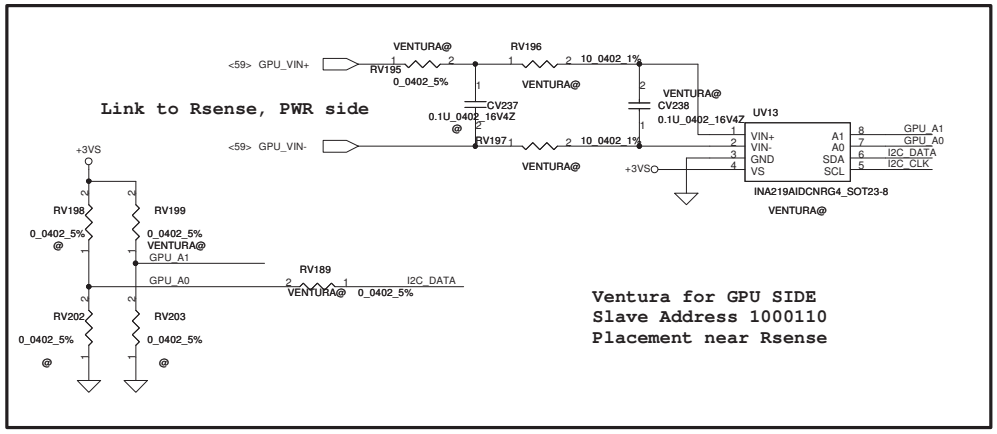
Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 32 of 63

TOP side (under inductor)







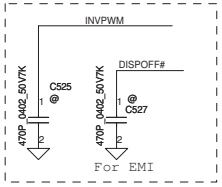
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

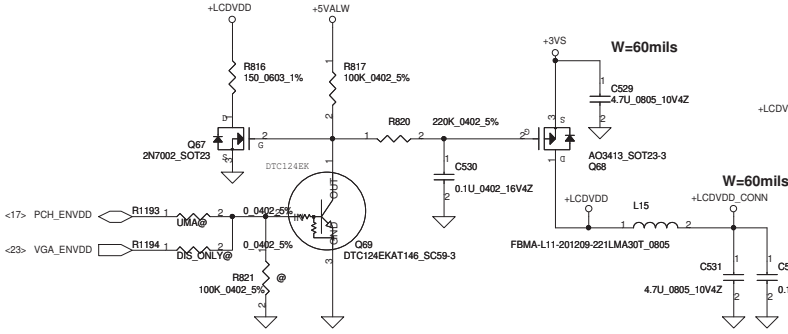
Title: **VENTURA Interface**

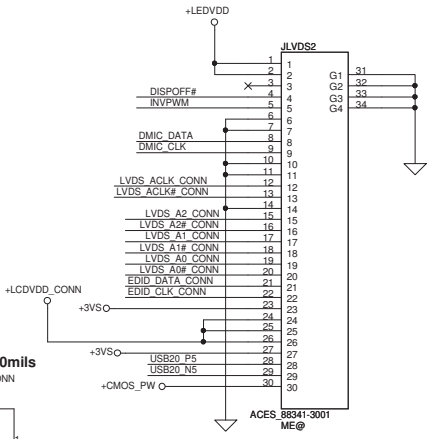
Size	Document Number	Rev
	LA-6882P	0.2

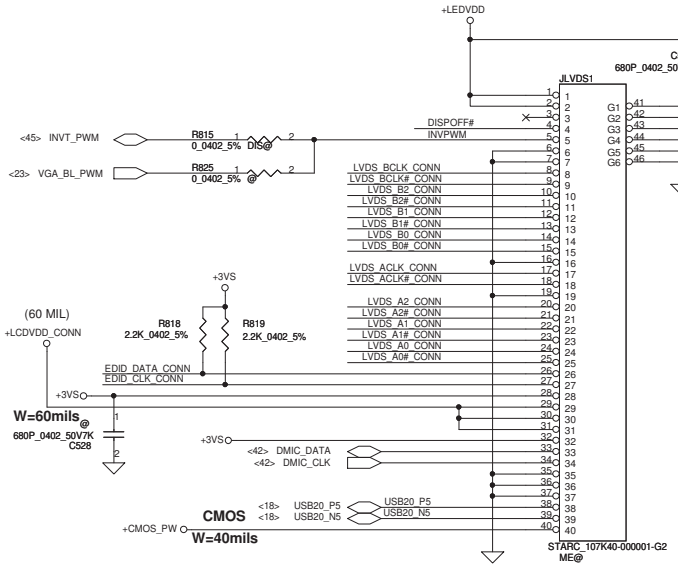
Date: Wednesday, October 06, 2010 Sheet 33 of 63

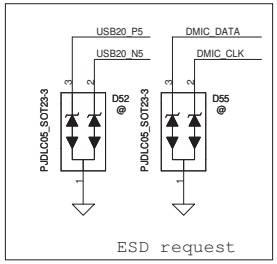


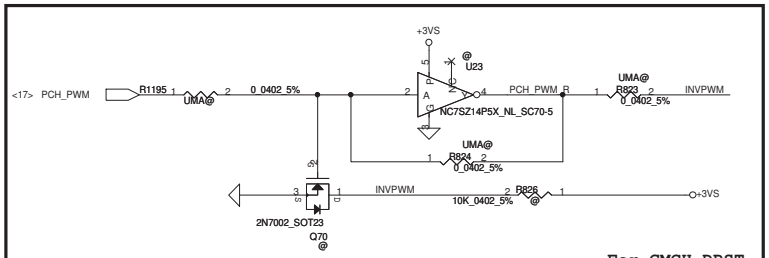
LCD POWER CIRCUIT

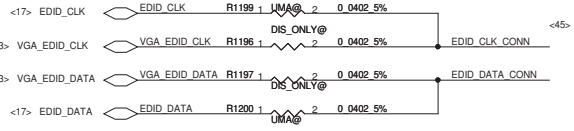


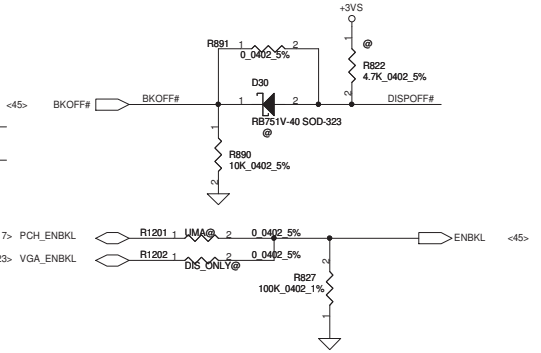


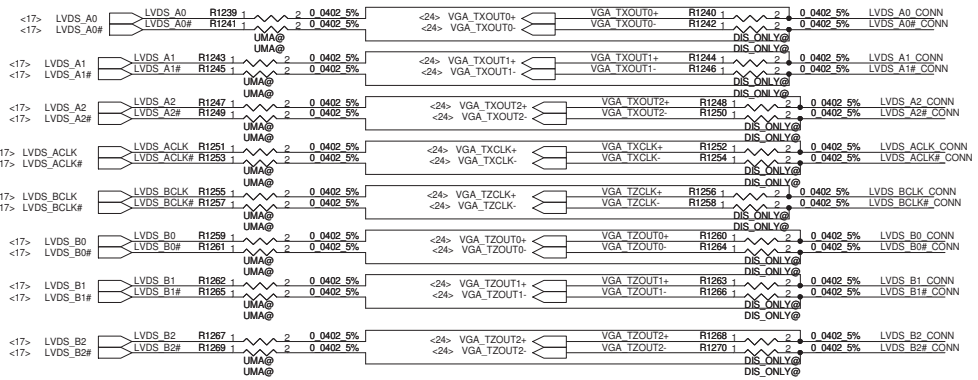


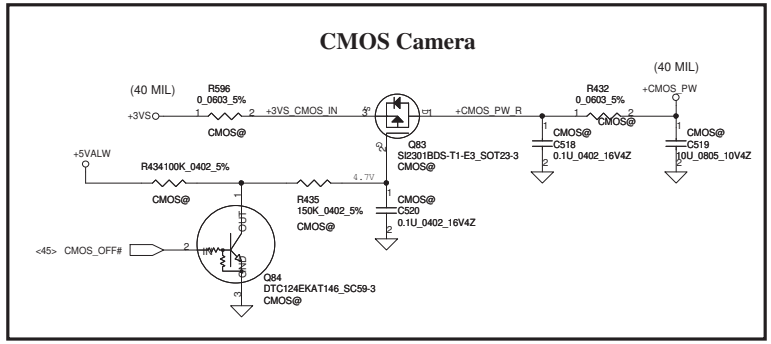












Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2008/10/15

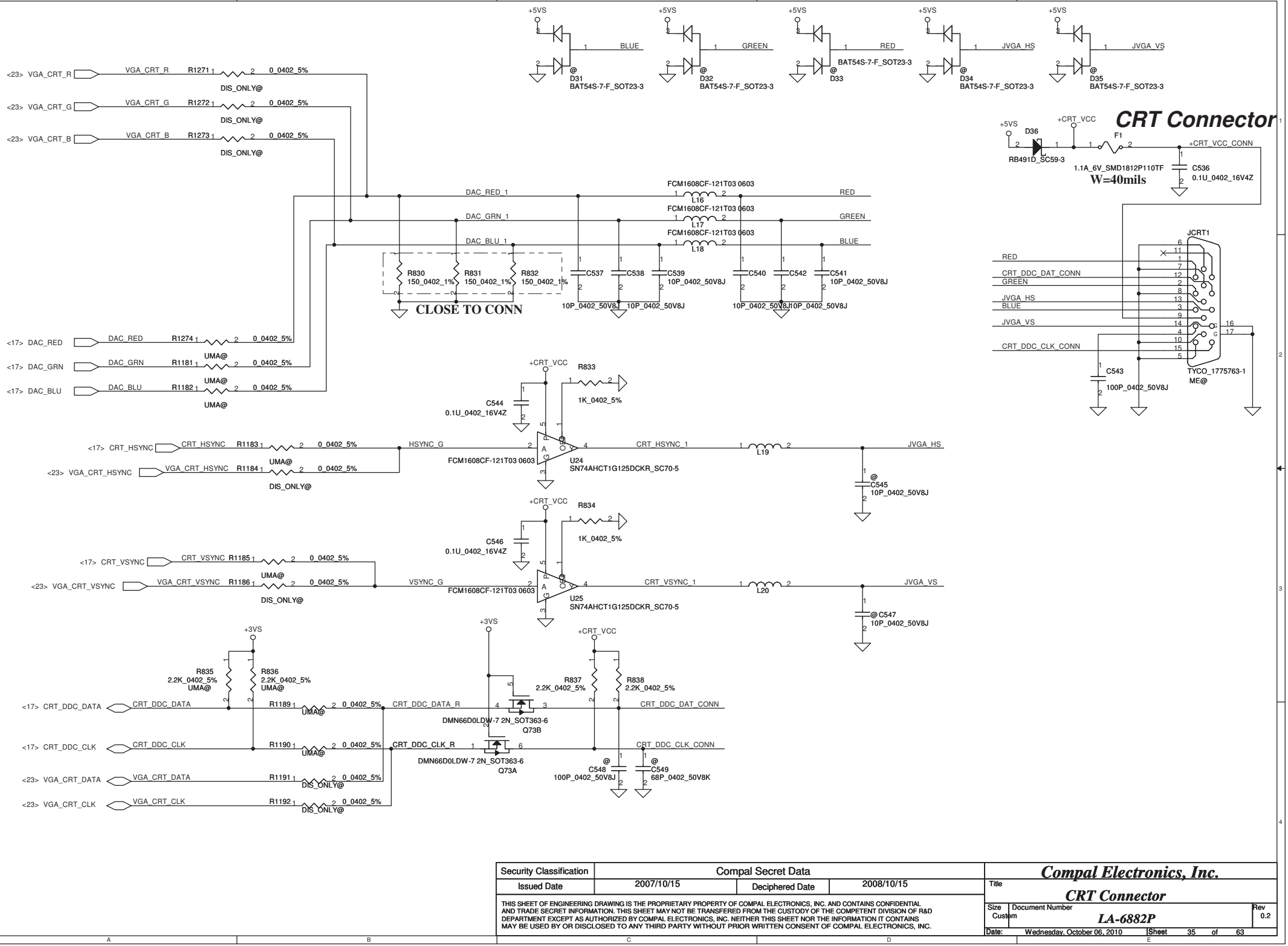
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size: Custom | Document Number: **LA-6882P** | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 34 of 63

CRT Connector



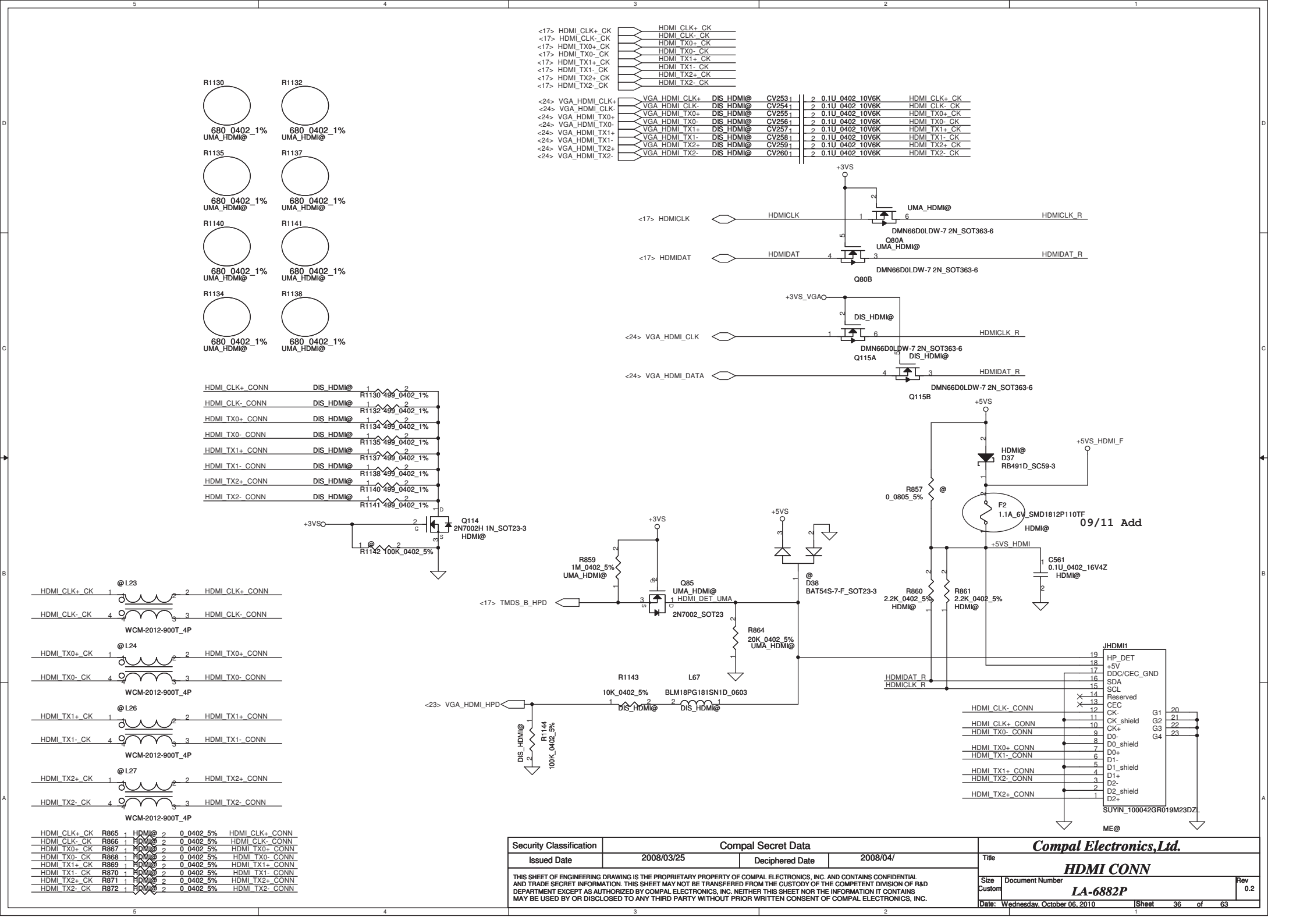
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **LA-6882P** | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 35 of 63



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

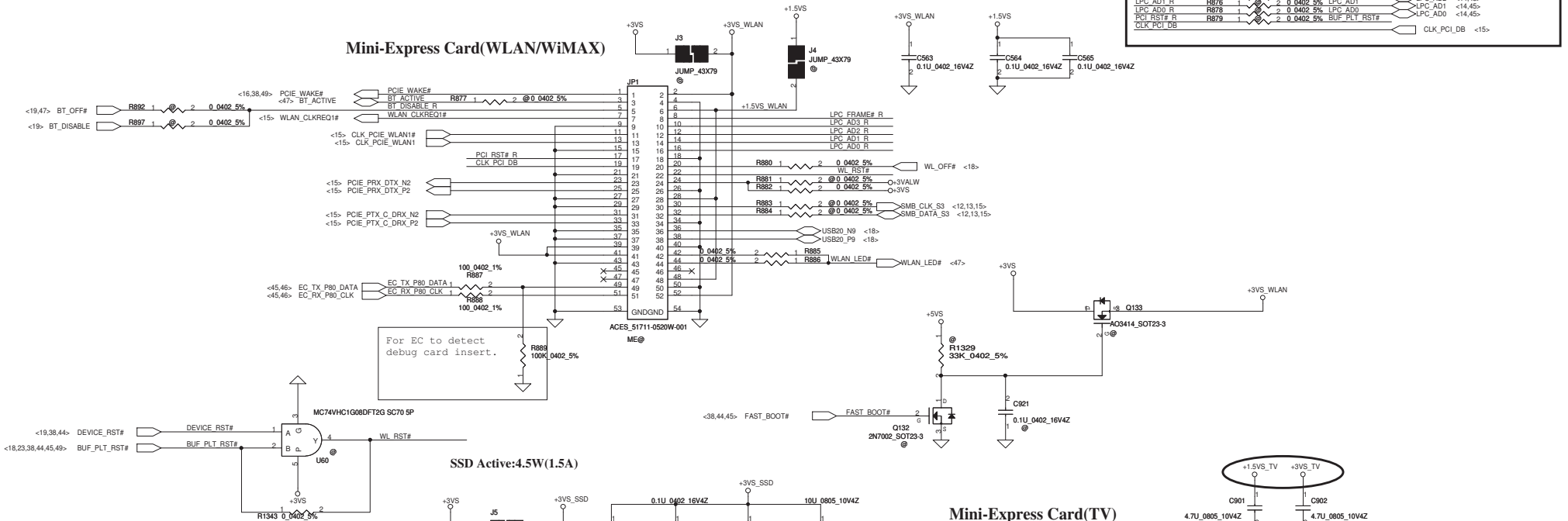
Compal Electronics,Ltd.
Title: HDMI CONN
Size: Custom
Document Number: LA-6882P
Rev: 0.2
Date: Wednesday, October 06, 2010
Sheet 36 of 63

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

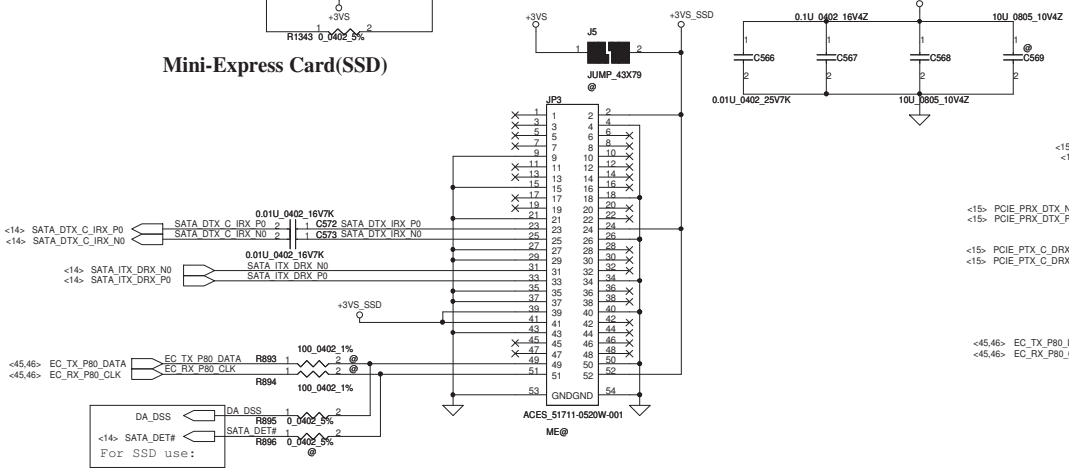
LPC_FRAME# R	R873	@	0 0402 5%	LPC_FRAME#	LPC_FRAME#	<14,45>
LPC_AD3 R	R874	@	0 0402 5%	LPC_AD3	LPC_AD3	<14,45>
LPC_AD2 R	R875	@	0 0402 5%	LPC_AD2	LPC_AD2	<14,45>
LPC_AD1 R	R876	@	0 0402 5%	LPC_AD1	LPC_AD1	<14,45>
LPC_AD0 R	R878	@	0 0402 5%	LPC_AD0	LPC_AD0	<14,45>
PCI RST# R	R879	@	0 0402 5%	BUF_PLT_RST#		
CLK_PCI_DB					CLK_PCI_DB	<15>

Mini-Express Card(WLAN/WiMAX)

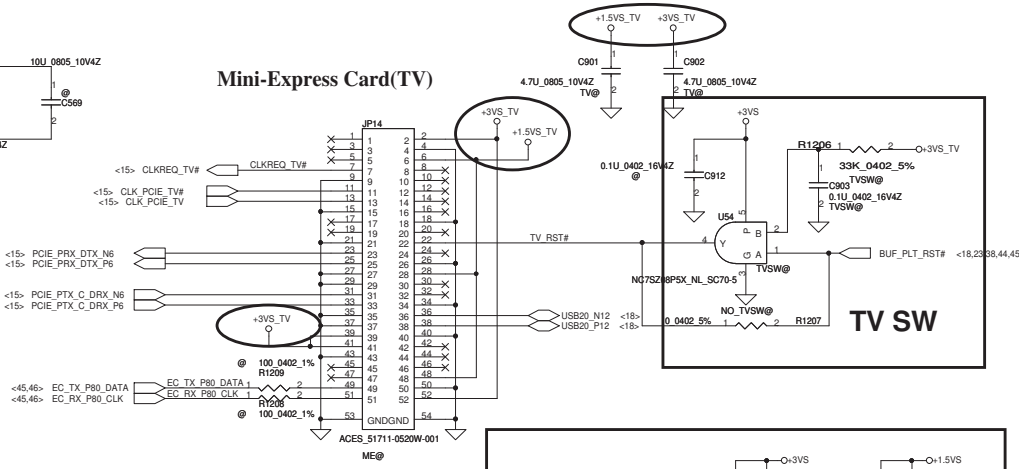


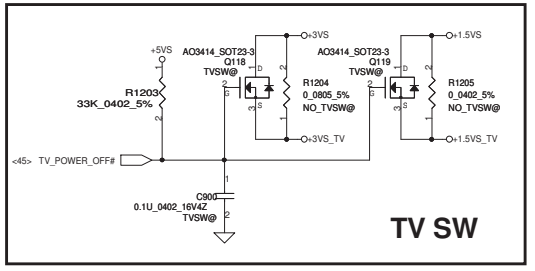
Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)



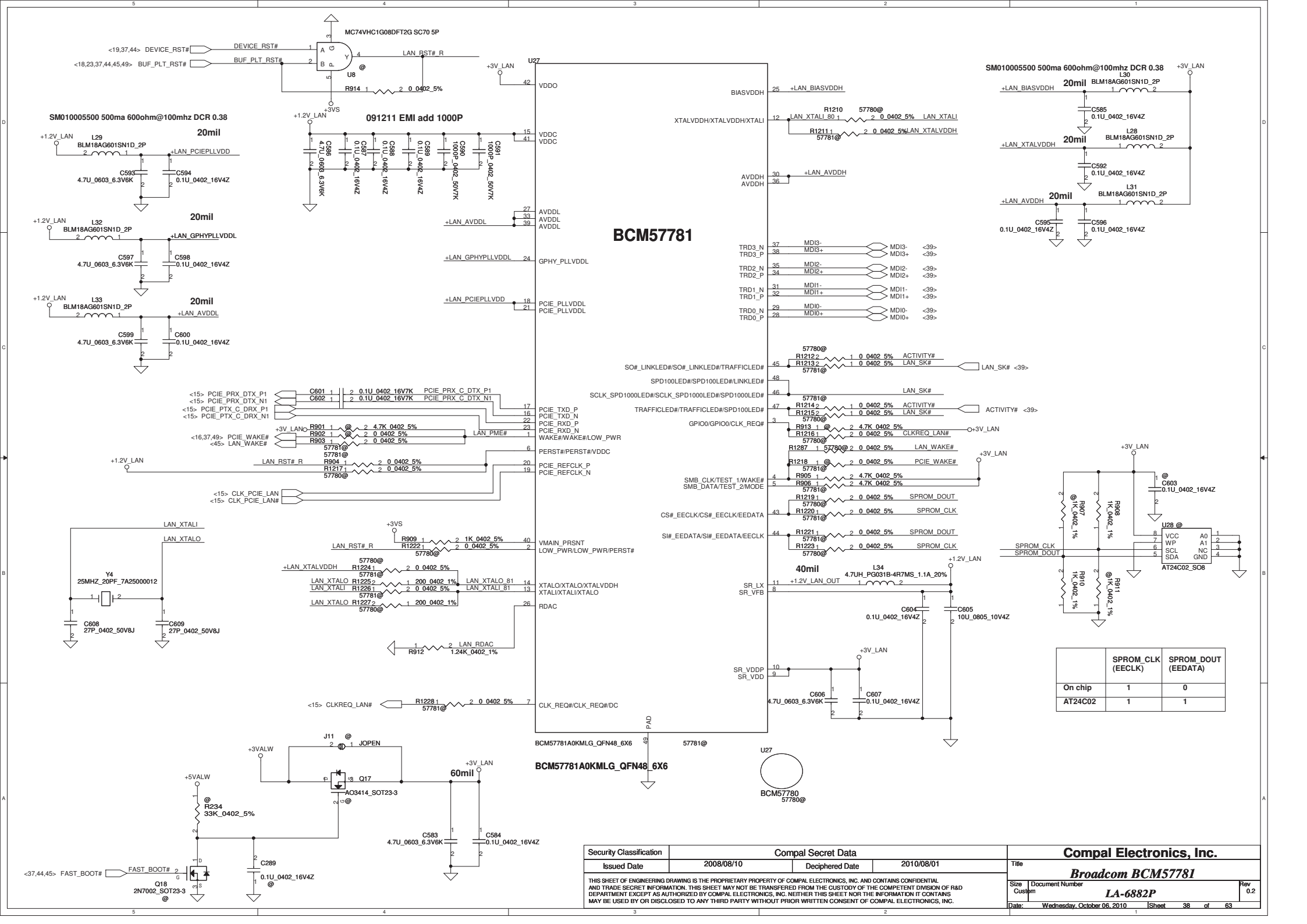
Mini-Express Card(TV)





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010		Sheet 37 of 63	


MC74VHC1G08DFT2G SC70 5P
<19,37,44> DEVICE_RST#
<18,23,37,44,45,49> BUF_PLT_RST#
DEVICE_RST#
BUF_PLT_RST#
LAN_RST#_R
U8
R914 0_0402_5%
+3VS
SM010005500 500ma 600ohm@100mhz DCR 0.38
091211 EMI add 1000P
+1.2V_LAN
+3V_LAN
U27
BCM57781
L29 BLM18AG601SN1D_2P
L32 BLM18AG601SN1D_2P
L33 BLM18AG601SN1D_2P
L30 BLM18AG601SN1D_2P
L28 BLM18AG601SN1D_2P
L31 BLM18AG601SN1D_2P
20mil
+LAN_PCIEPLLVDD
+LAN_GPHYPLLVDDL
+LAN_AVDDL
+LAN_BIASVDDH
+LAN_XTALVDDH
+LAN_AVDDH
C585 0.1U_0402_16V4Z
C586 4.7U_0603_6.3V6K
C587 0.1U_0402_16V4Z
C588 0.1U_0402_16V4Z
C589 0.1U_0402_16V4Z
C590 1000P_0402_50V7K
C591 1000P_0402_50V7K
C592 0.1U_0402_16V4Z
C593 4.7U_0603_6.3V6K
C594 0.1U_0402_16V4Z
C595 0.1U_0402_16V4Z
C596 0.1U_0402_16V4Z
C597 4.7U_0603_6.3V6K
C598 0.1U_0402_16V4Z
C599 4.7U_0603_6.3V6K
C600 0.1U_0402_16V4Z
VDDO
VDDC
AVDDL
AVDDH
GPHY_PLLVDDL
PCIE_PLLVDDL
BIASVDDH
XTALVDDH/XTALVDDH/XTALI
R1210 57780@ LAN_XTALI_80 0_0402_5% LAN_XTALI
R1211 57781@ 0_0402_5% LAN_XTALVDDH
AVDDH
TRD3_N TRD3_P MDI3- MDI3+ MDI3- <39> MDI3+ <39>
TRD2_N TRD2_P MDI2- MDI2+ MDI2- <39> MDI2+ <39>
TRD1_N TRD1_P MDI1- MDI1+ MDI1- <39> MDI1+ <39>
TRD0_N TRD0_P MDI0- MDI0+ MDI0- <39> MDI0+ <39>
SO#_LINKLED#/SO#_LINKLED#/TRAFFICLED#
SPD100LED#/SPD100LED#/LINKLED#
SCLK_SPD1000LED#/SCLK_SPD1000LED#/SPD1000LED#
TRAFFICLED#/TRAFFICLED#/SPD100LED#
GPIO0/GPIO0/CLK_REQ#
R1212 57780@ 0_0402_5% ACTIVITY#
R1213 57781@ 0_0402_5% LAN_SK#
LAN_SK# <39>
R1214 57781@ 0_0402_5% ACTIVITY#
R1215 57780@ 0_0402_5% LAN_SK#
ACTIVITY# <39>
R913 @ 4.7K_0402_5%
R1216 57780@ 0_0402_5% CLKREQ_LAN#
+3V_LAN
R1287 57780@ 0_0402_5% LAN_WAKE#
R1218 @ 57781@ 0_0402_5% PCIE_WAKE#
<15> PCIE_PRX_DTX_P1
<15> PCIE_PRX_DTX_N1
<15> PCIE_PTX_C_DRX_P1
<15> PCIE_PTX_C_DRX_N1
C601 0.1U_0402_16V7K PCIE_PRX_C_DTX_P1
C602 0.1U_0402_16V7K PCIE_PRX_C_DTX_N1
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#/WAKE#/LOW_PWR
PERST#/PERST#/VDDC
PCIE_REFCLK_P
PCIE_REFCLK_N
<15> CLK_PCIE_LAN
<15> CLK_PCIE_LAN#
<16,37,49> PCIE_WAKE#
<45> LAN_WAKE#
LAN_PME#
R901 @ 4.7K_0402_5%
R902 @ 0_0402_5%
R903 57781@ 57780@ 0_0402_5%
R904 0_0402_5%
R1217 57780@ 0_0402_5%
SMB_CLK/TEST_1/WAKE#
SMB_DATA/TEST_2/MODE
R905 4.7K_0402_5%
R906 4.7K_0402_5%
R1219 57780@ 0_0402_5% SPROM_DOUT
R1220 57781@ 0_0402_5% SPROM_CLK
CS#_EECLK/CS#_EECLK/EEDATA
SI#_EEDATA/SI#_EEDATA/EECLK
R1221 57781@ 0_0402_5% SPROM_DOUT
R1223 57780@ 0_0402_5% SPROM_CLK
SPROM_CLK
SPROM_DOUT
R907 @1K_0402_1%
R908 1K_0402_1%
R910 1K_0402_1%
R911 @1K_0402_1%
C603 @ 0.1U_0402_16V4Z
U28 @ AT24C02_SO8
VCC WP SCL SDA A0 A1 NC GND
LAN_XTALI
LAN_XTALO
Y4 25MHZ_20PF_7A25000012
C608 27P_0402_50V8J
C609 27P_0402_50V8J
+3VS
R909 1K_0402_5%
R1222 57780@ 0_0402_5%
LAN_RST#_R
+LAN_XTALVDDH
R1224 57780@ 57781@ 0_0402_5%
LAN_XTALO R1225 200_0402_1% LAN_XTALO_81
LAN_XTALI R1226 57781@ 0_0402_5% LAN_XTALI_81
LAN_XTALO R1227 57780@ 200_0402_1%
VMAIN_PRSNT
LOW_PWR/LOW_PWR/PERST#
XTALO/XTALO/XTALVDDH
XTALI/XTALI/XTALO
RDAC
LAN_RDAC
R912 1.24K_0402_1%
40mil
L34 4.7UH_PG031B-4R7MS_1.1A_20%
+1.2V_LAN_OUT
SR_LX
SR_VFB
C604 0.1U_0402_16V4Z
C605 10U_0805_10V4Z
SR_VDDP
SR_VDD
C606 4.7U_0603_6.3V6K
C607 0.1U_0402_16V4Z
<15> CLKREQ_LAN#
R1228 57781@ 0_0402_5%
CLK_REQ#/CLK_REQ#/DC
PAD
BCM57781A0KMLG_QFN48_6X6
57781@
BCM57780
57780@
J11 @ JOPEN
+3VALW
+5VALW
Q17 AO3414_SOT23-3
60mil
R234 @ 33K_0402_5%
C583 4.7U_0603_6.3V6K
C584 0.1U_0402_16V4Z
C289 0.1U_0402_16V4Z
<37,44,45> FAST_BOOT#
Q18 2N7002_SOT23-3
SPROM_CLK (EECLK)
SPROM_DOUT (EEDATA)
On chip 1 0
AT24C02 1 1
Security Classification
Compal Secret Data
Issued Date 2008/08/10
Deciphered Date 2010/08/01
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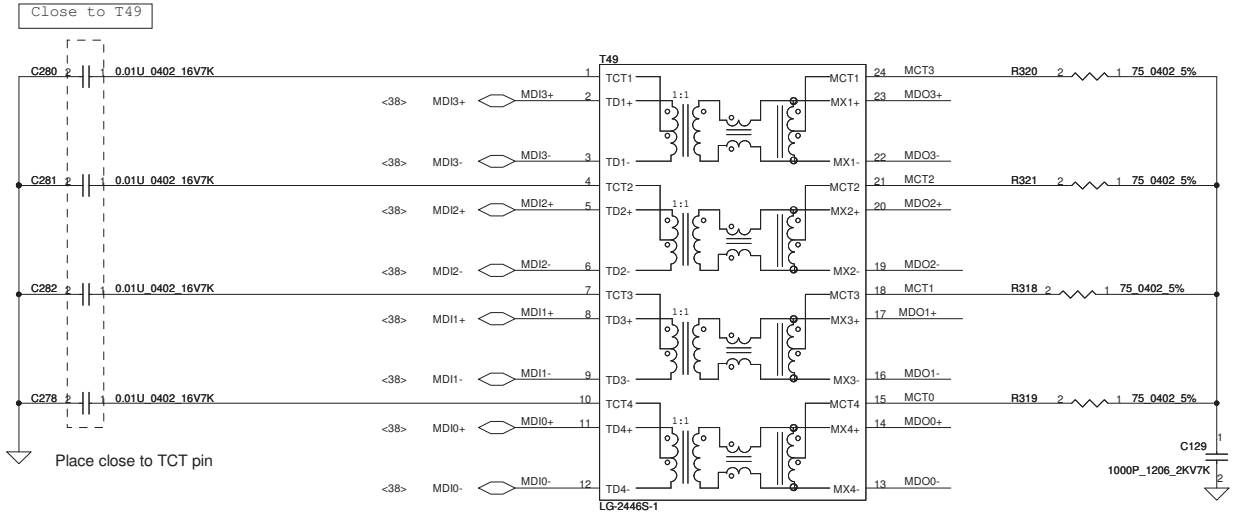
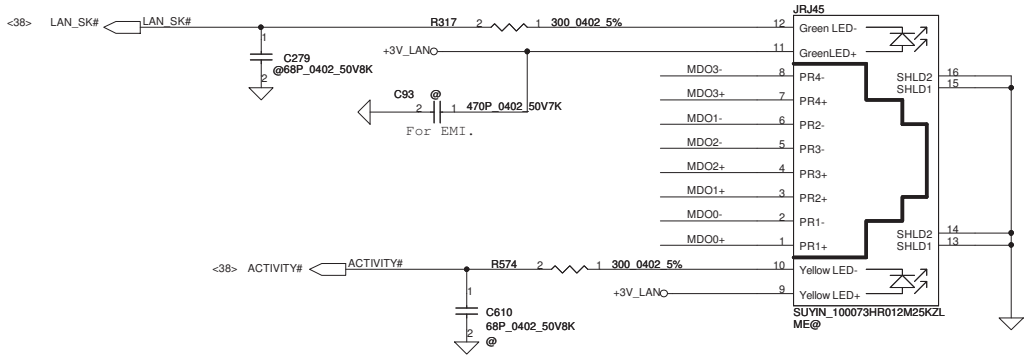
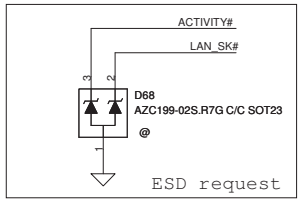
Compal Electronics, Inc.
Title
Broadcom BCM57781
Size Custom
Document Number
LA-6882P
Rev 0.2
Date: Wednesday, October 06, 2010
Sheet 38 of 63



RJ45 Conn.





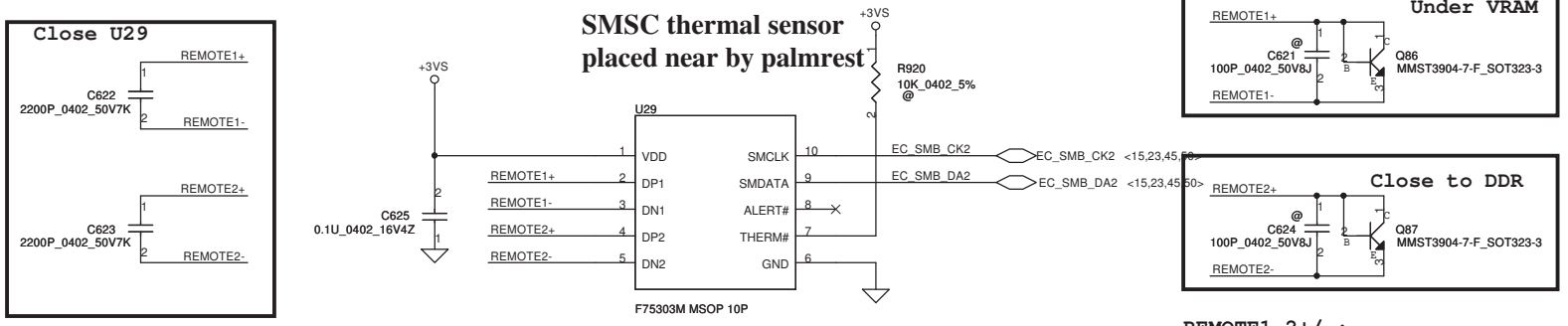
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

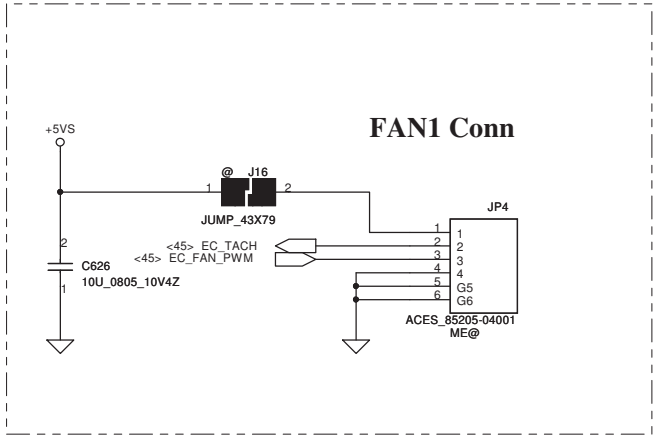
Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 39 of 63



Address 1001_101xb

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

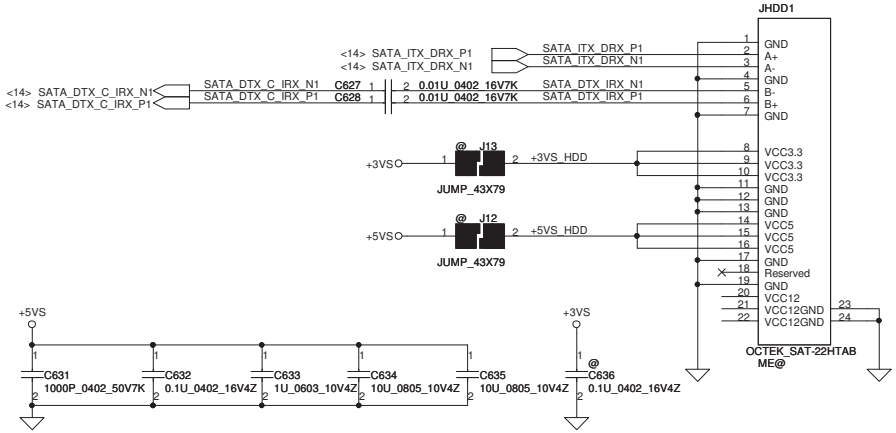
Compal Electronics,Ltd.

Title: ***EMC1403_Thermal sensor/FAN***

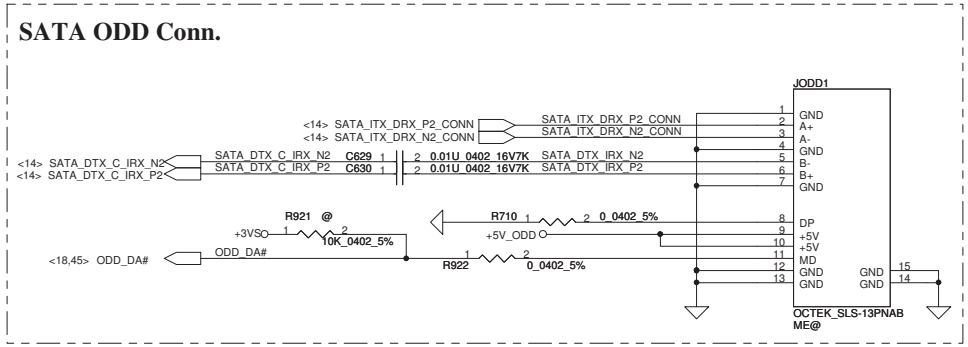
Size	Document Number	Rev
Custom	***LA-6882P***	0.2

Date: Wednesday, October 06, 2010 Sheet 40 of 63

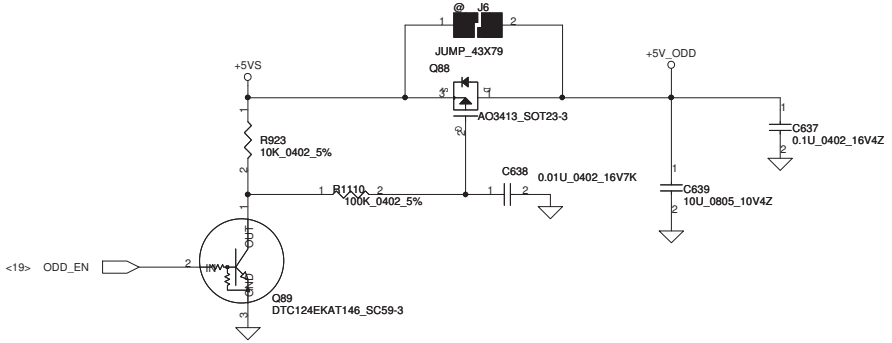
SATA HDD Conn.



SATA ODD Conn.

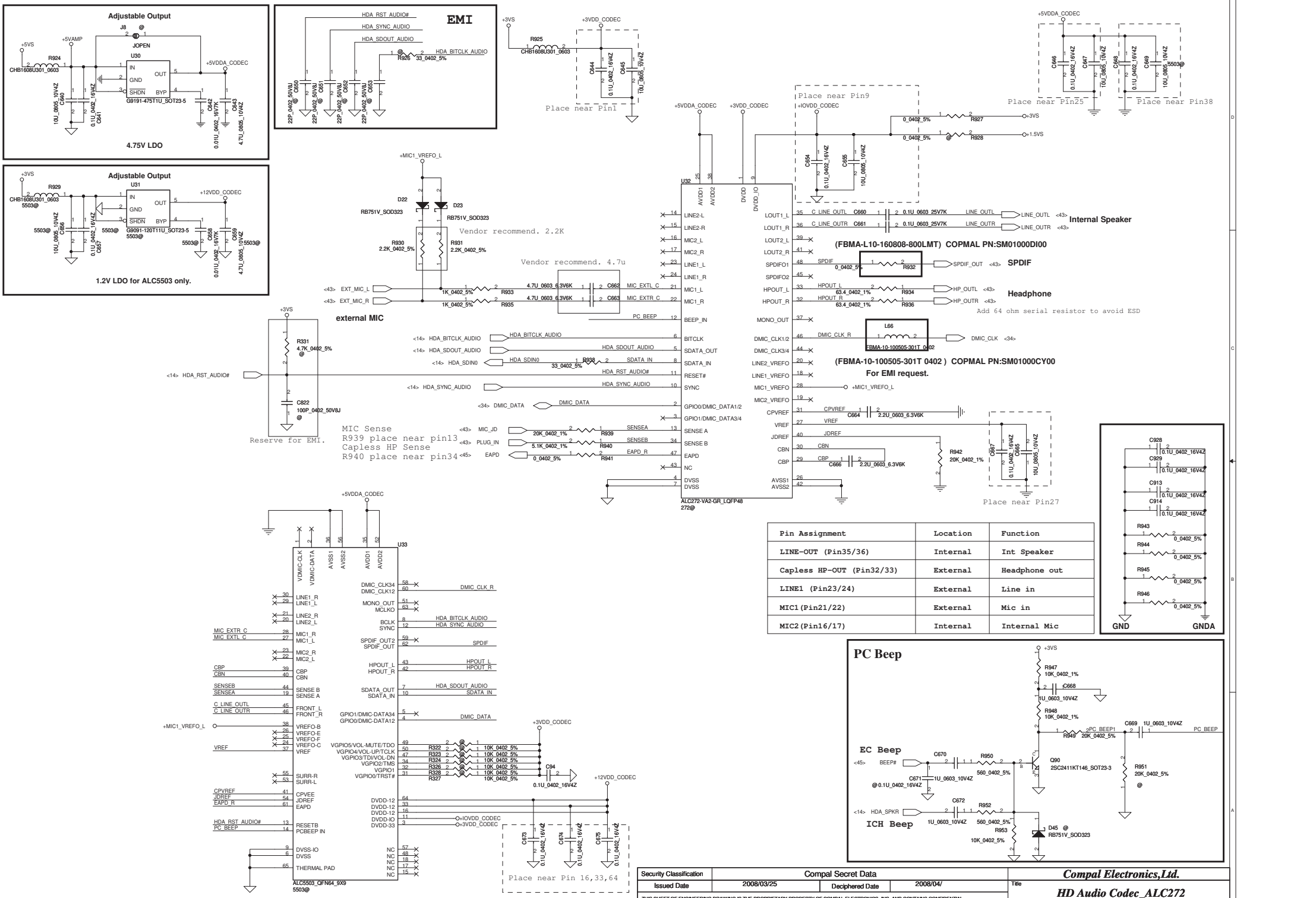


ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.	
Title	HDD/ODD Connector
Size B	Document Number LA-6882P
Rev	0.2
Date: Wednesday, October 06, 2010	Sheet 41 of 63



Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MIC2(Pin16/17)	Internal	Internal Mic

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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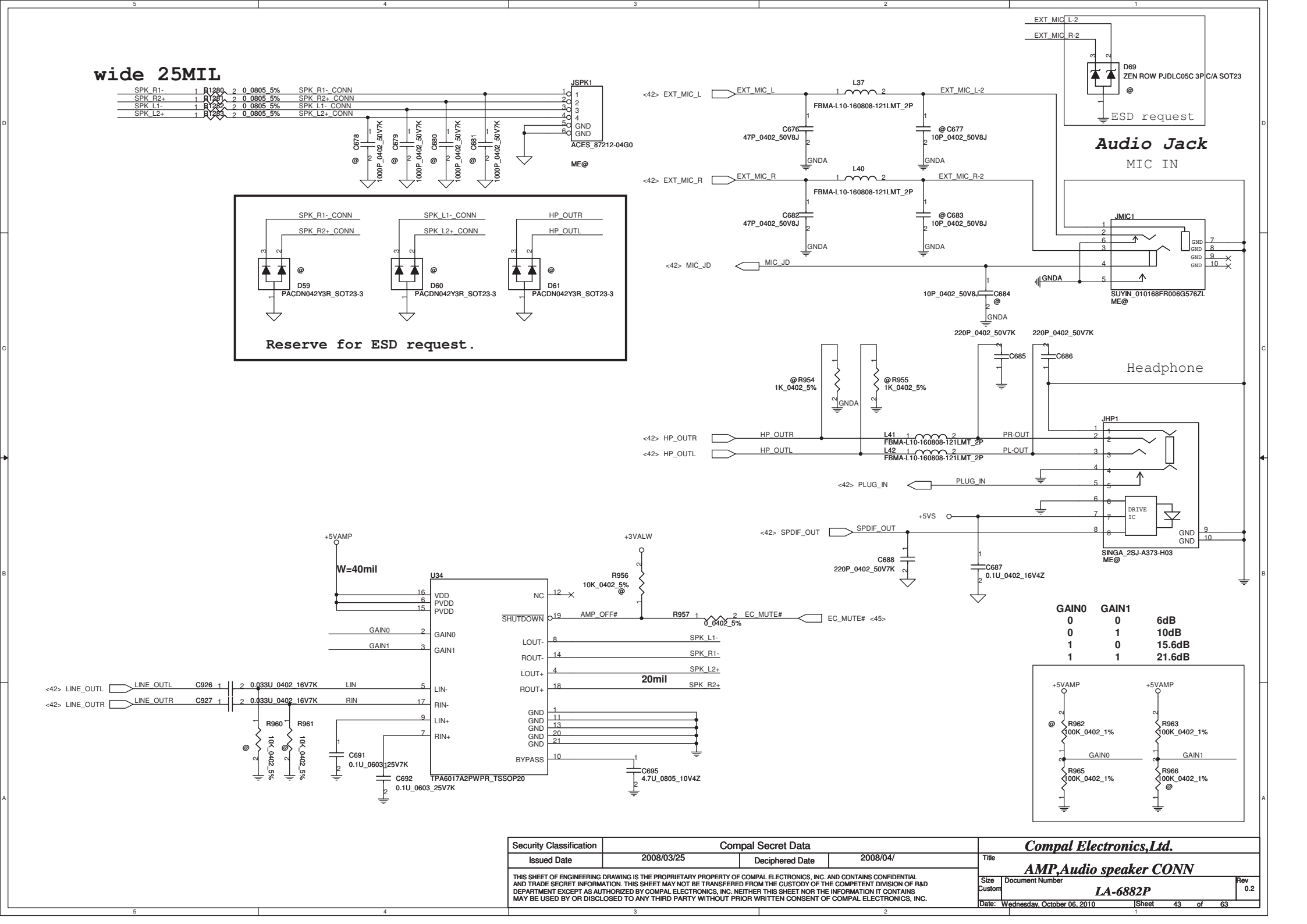
Compal Electronics,Ltd.

Title: HD Audio Codec_ALC272

Size: C | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 42 of 63



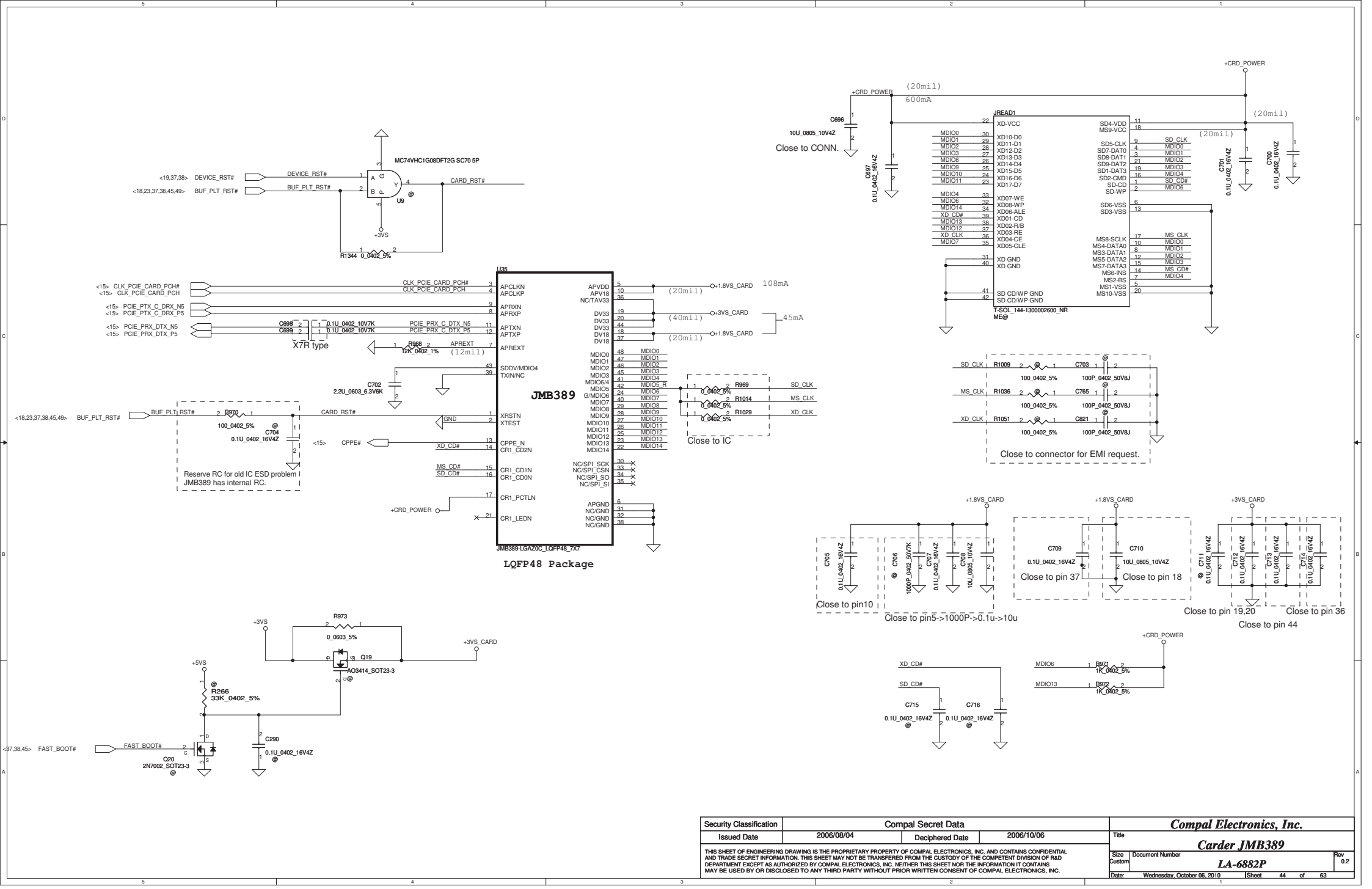
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **AMP,Audio speaker CONN**

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 43 of 63



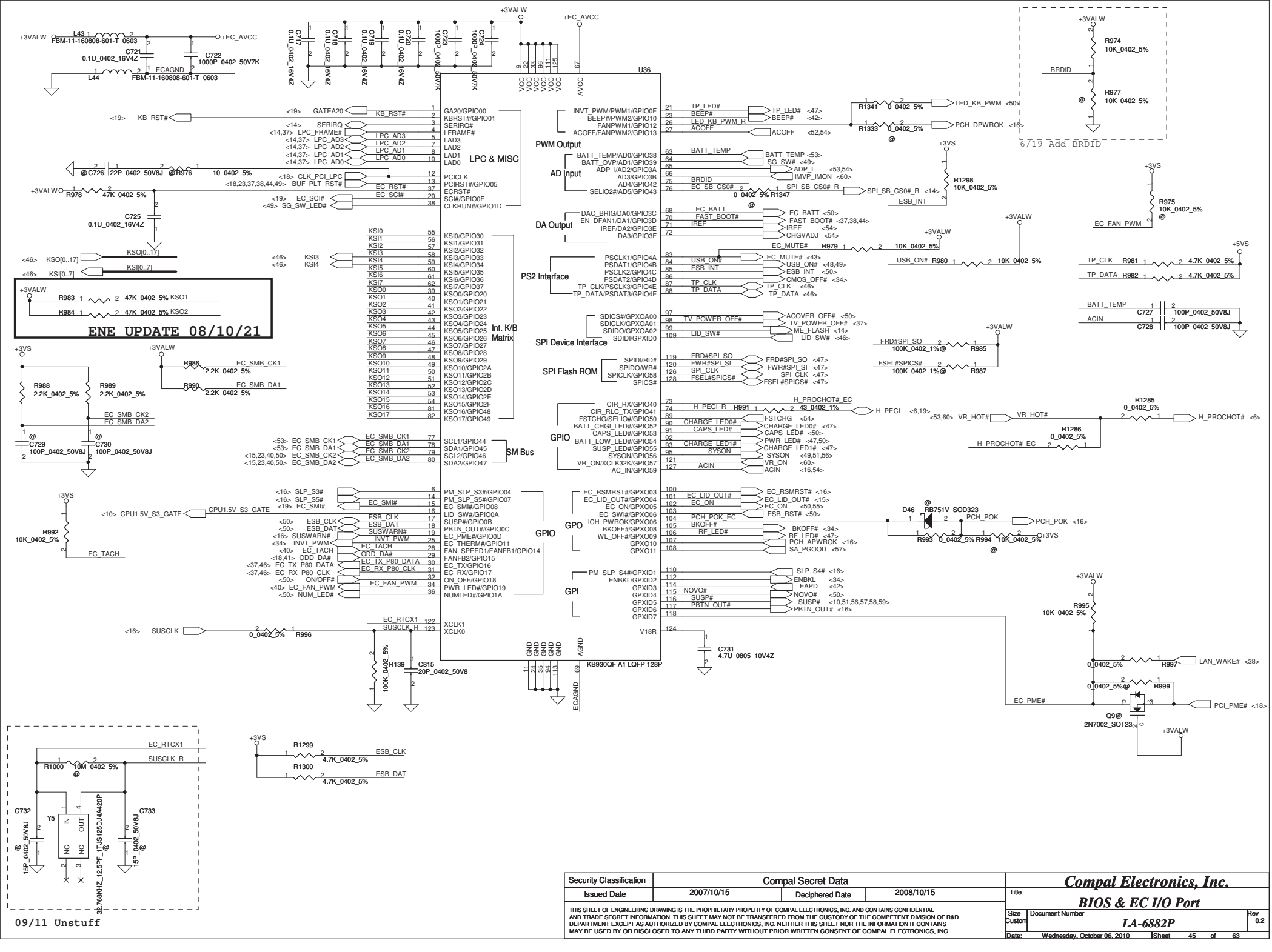
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: **Carder JMB389**

Size: Custom | Document Number: **LA-6882P** | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 44 of 63



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

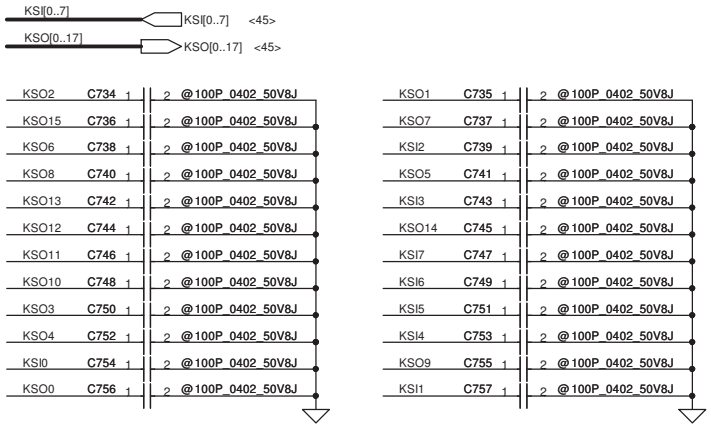
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

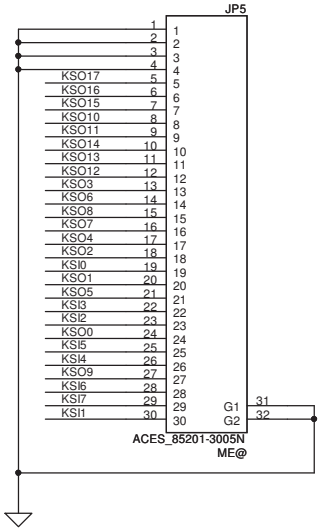
Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 45 of 63

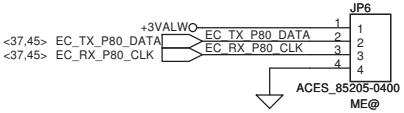
INT_KBD Conn.



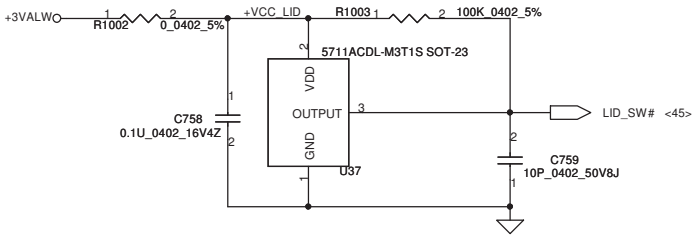
CONN PIN define need double check



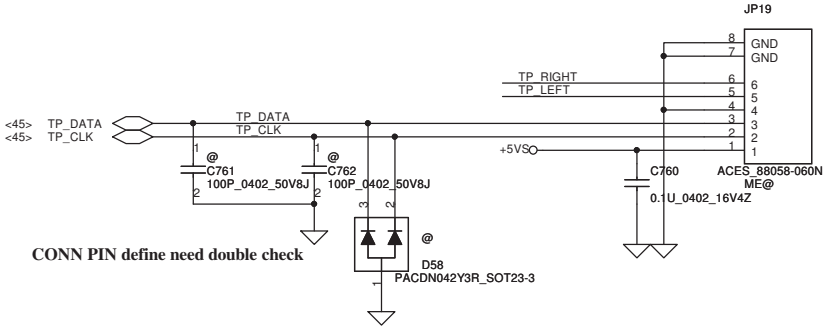
EC DEBUG PORT



Lid Switch

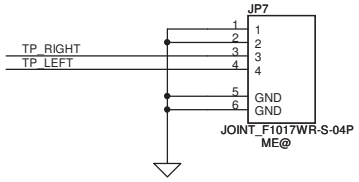


To TP/B Conn.



CONN PIN define need double check

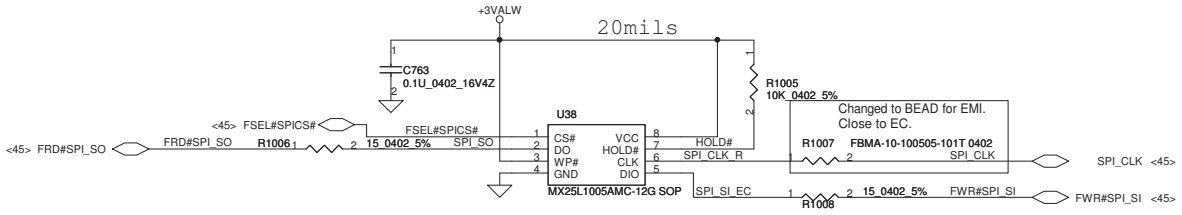
To TP Button/B Conn.

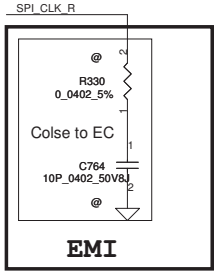


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

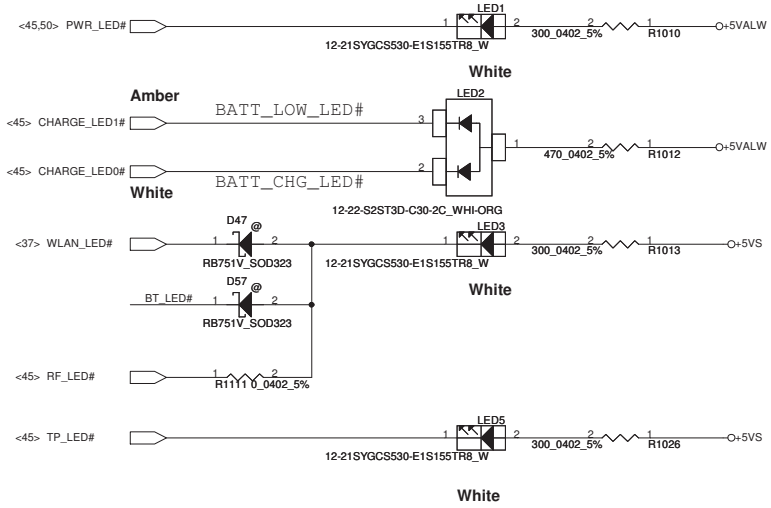
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 46 of 63		

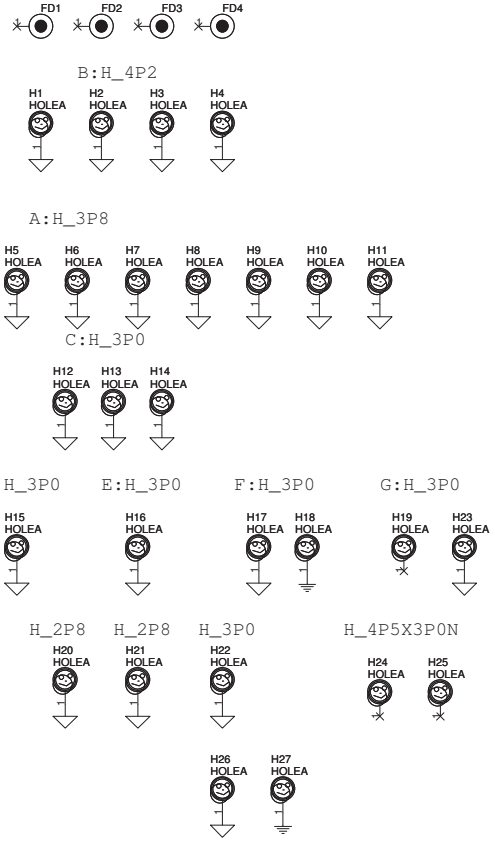
FOR EC 128KB SPI
(150mil PACKAGE)
P/N : SA00002C100



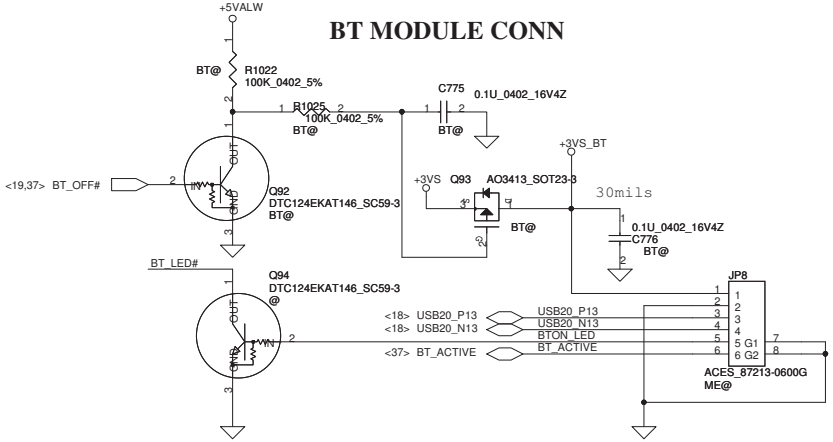


LED





BT MODULE CONN



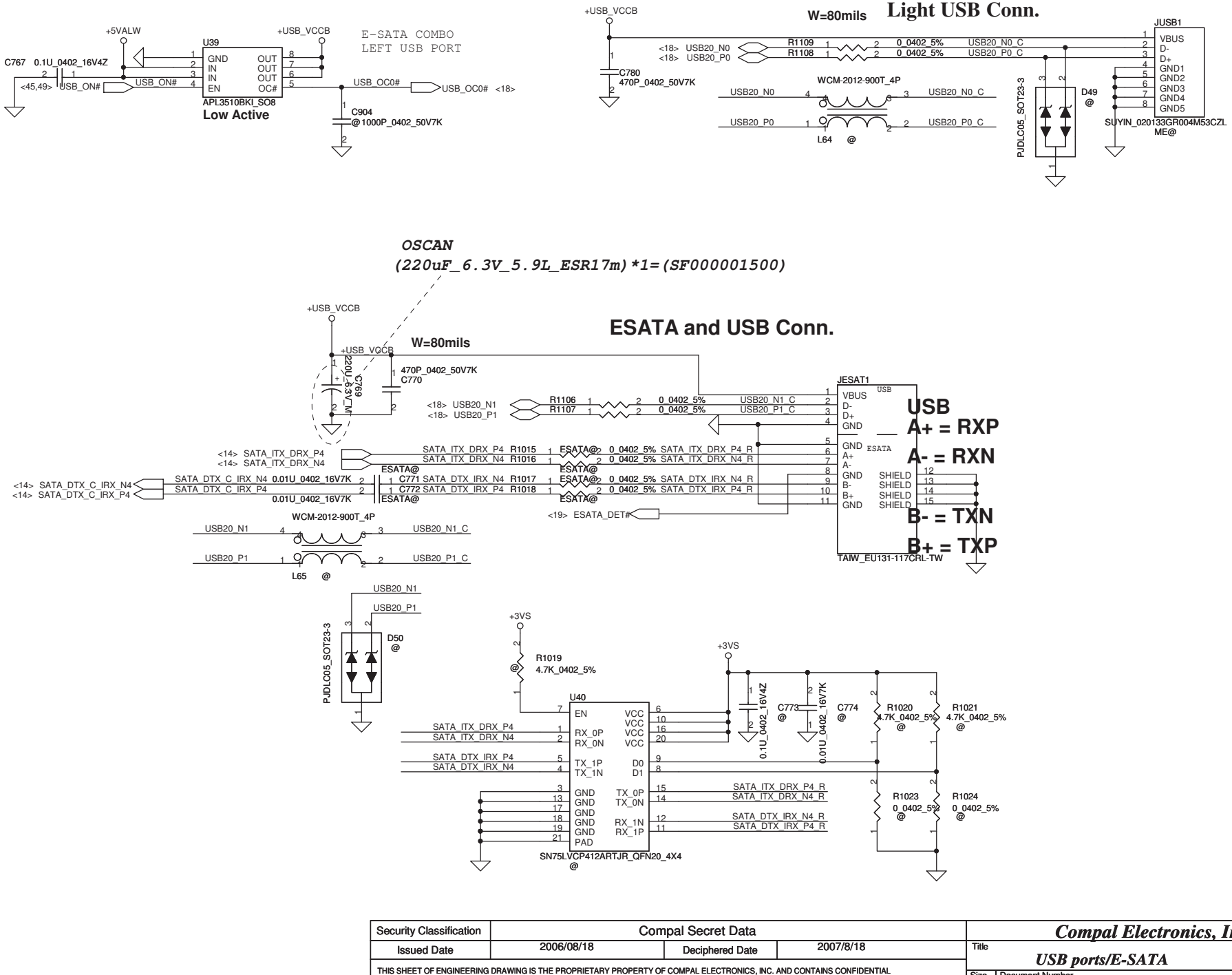
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LED/EC SPI ROM/BT**

Size	Document Number	Rev
B	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 47 of 63



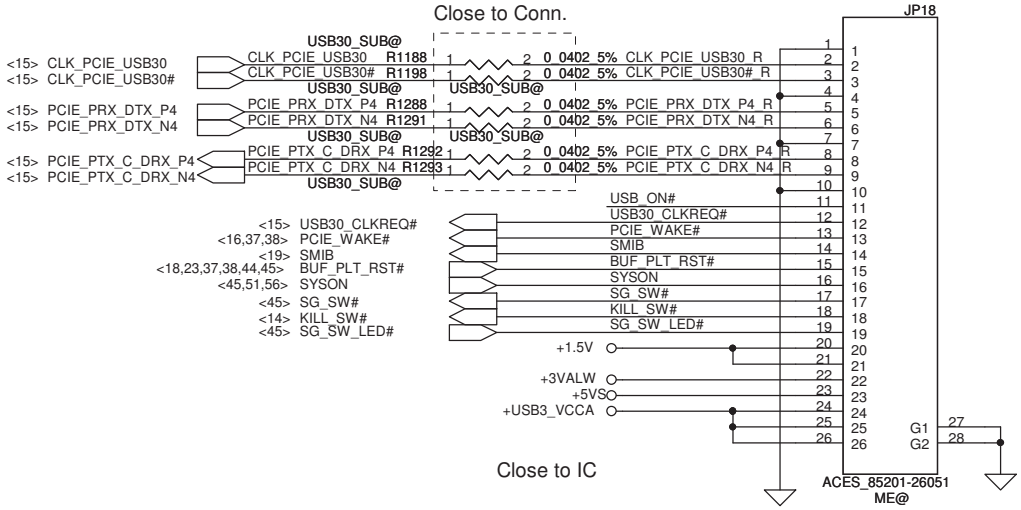
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: *USB ports/E-SATA*

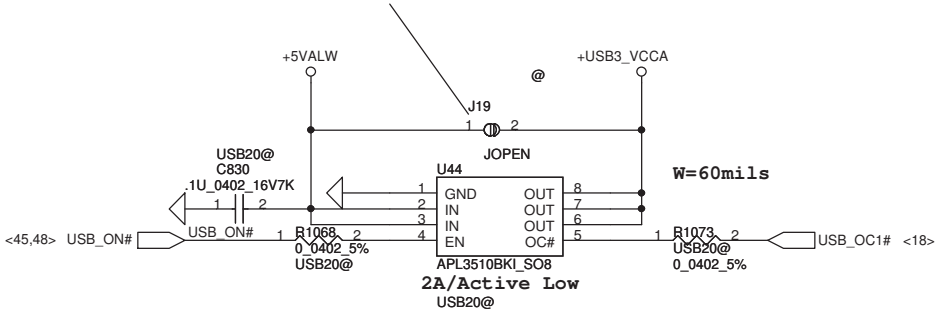
Size: Custom | Document Number: *LA-6882P* | Rev: 0.2

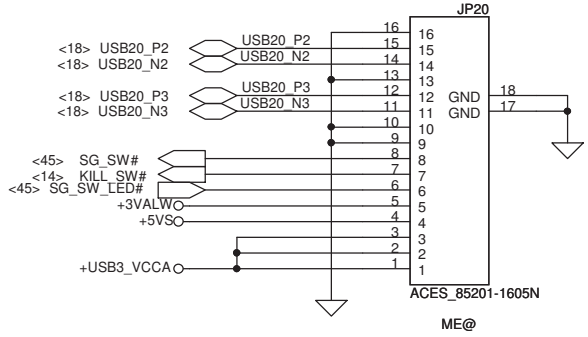
Date: Wednesday, October 06, 2010 | Sheet 48 of 63



09/30 Delete USB3.0 controller

10/04 Short J19 with JP18.





Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

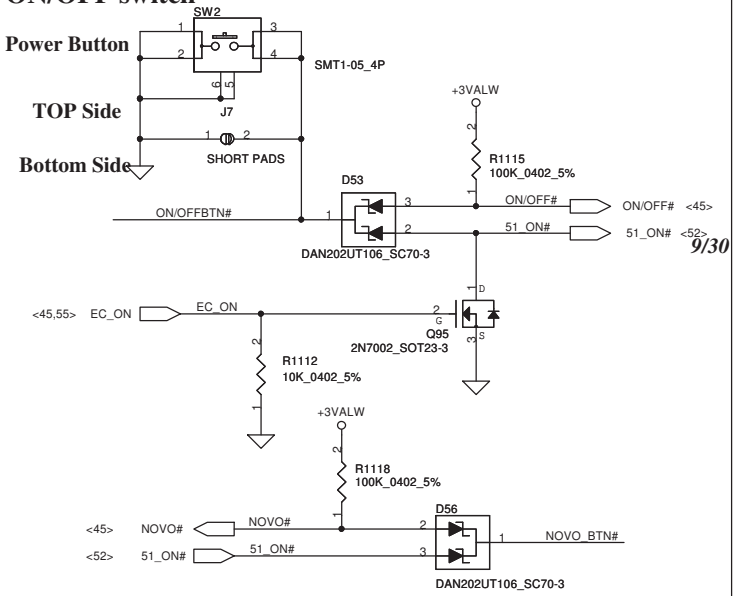
Compal Electronics, Inc.

Title: **USB Right Ports/ USB Brd Conn.**

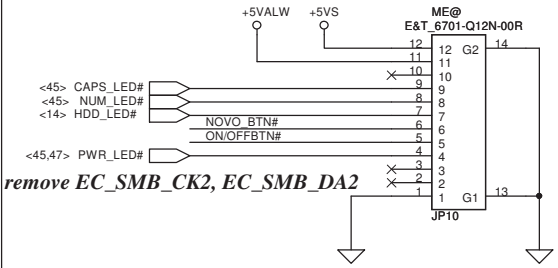
Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 49 of 63

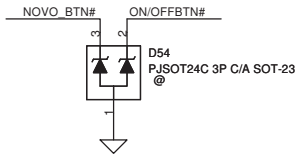
ON/OFF switch



P6



9/30 remove EC_SMB_CK2, EC_SMB_DA2

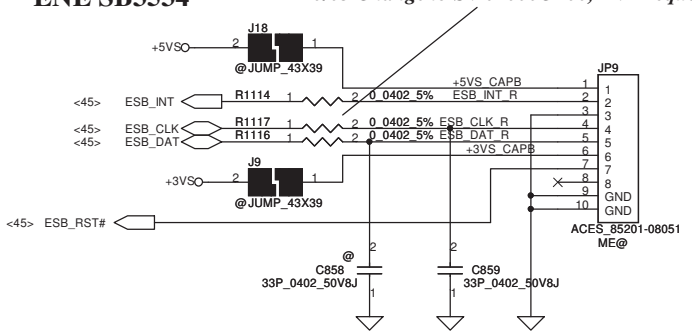


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

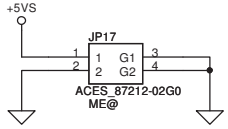
Cap Sensor Board Conn. 8pin

ENE SB3534

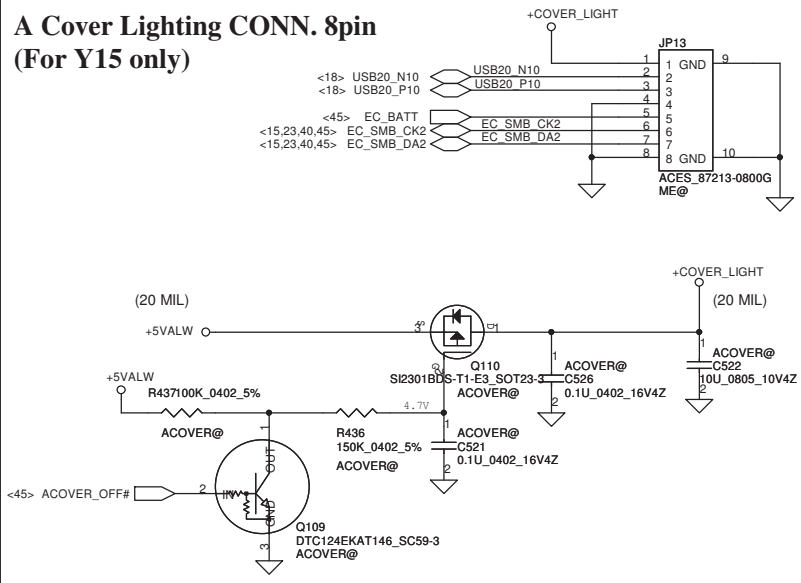
10/05 Change to SM01000CY00, EMI request



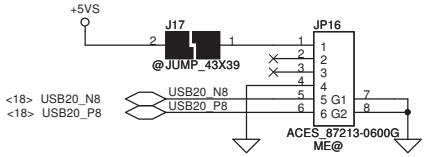
FAN Lighting Conn. 2pin (For Y15 only)



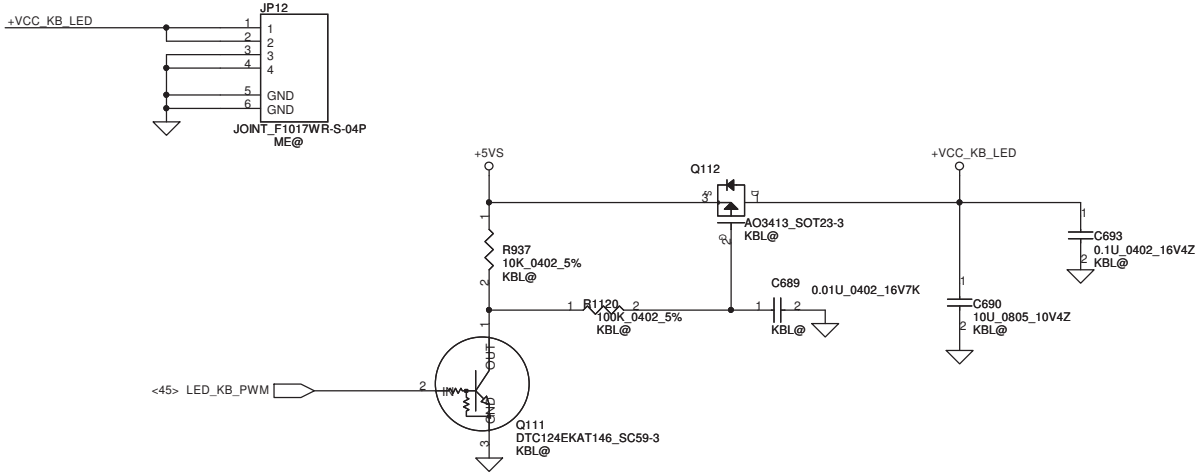
A Cover Lighting CONN. 8pin (For Y15 only)



IR CONN. 6pin (For Y15 only)



KB Lighting CONN.4pin



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

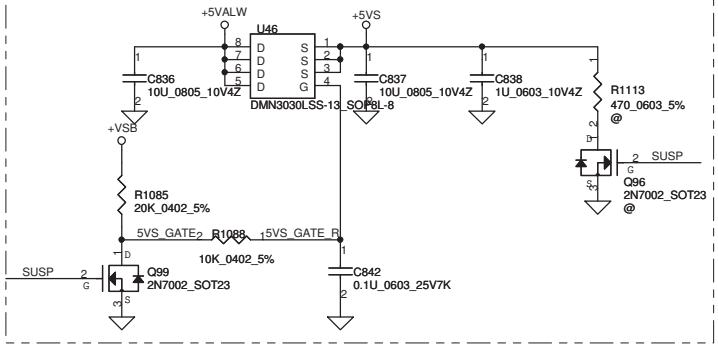
Title: ***other IO connector***

Size: Custom | Document Number: ***LA-6882P*** | Rev: 0.2

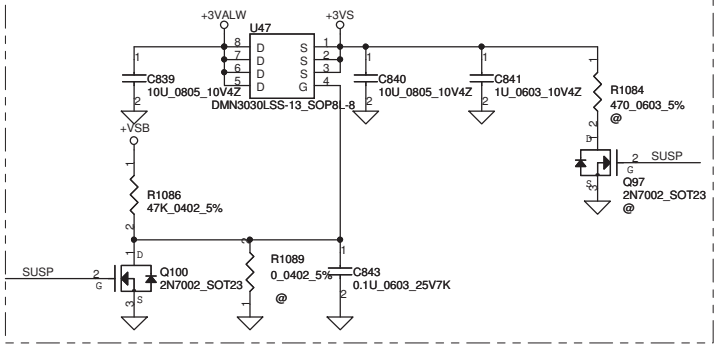
Date: Wednesday, October 06, 2010 | Sheet 50 of 63

7/26 change SI4800 to SI2301

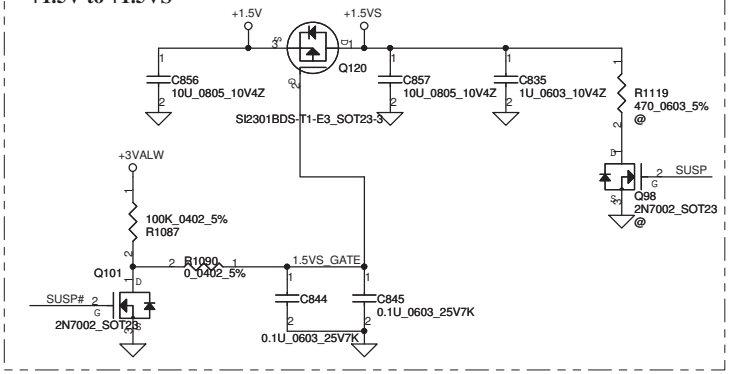
+5VALW TO +5VS

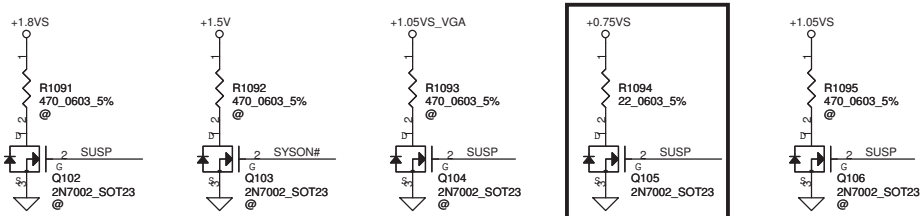


+3VALW TO +3VS

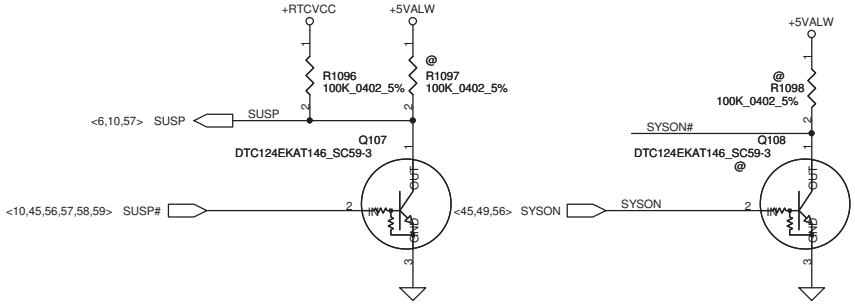


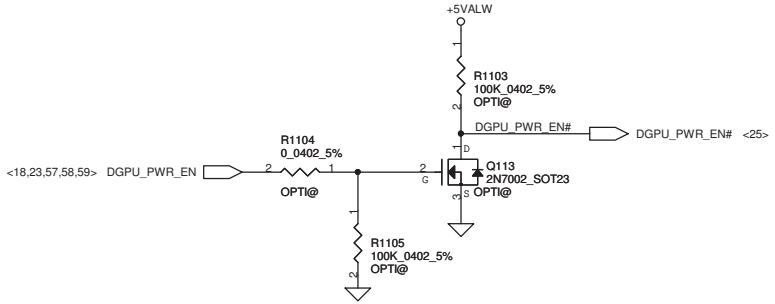
+1.5V to +1.5VS





For Intel S3 Power Reduction.





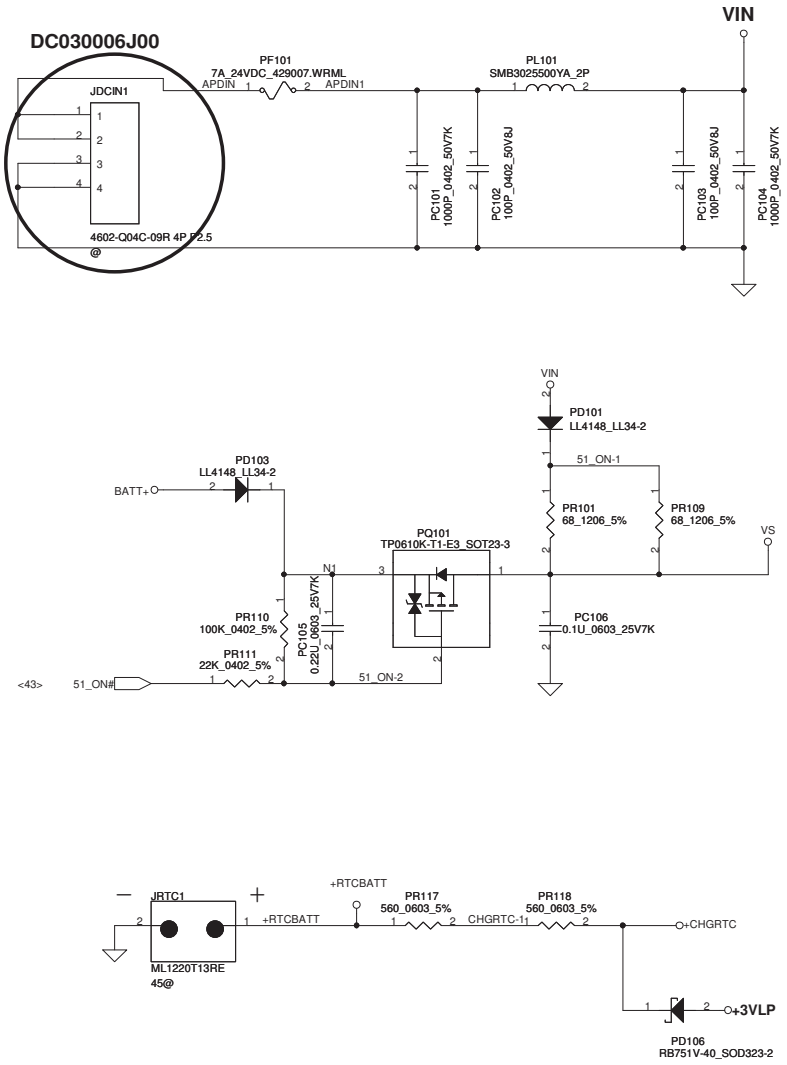
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

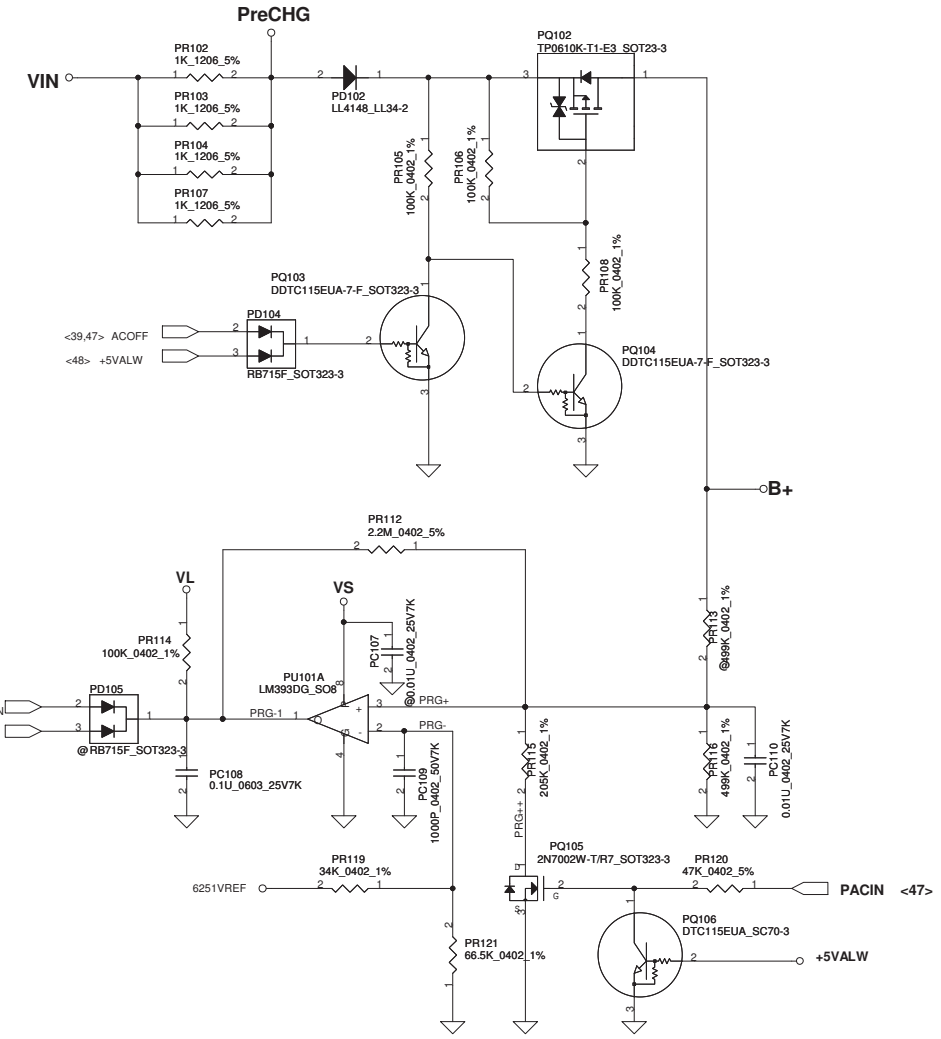
Title: **DC Interface**

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 51 of 63



Precharge detector
15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

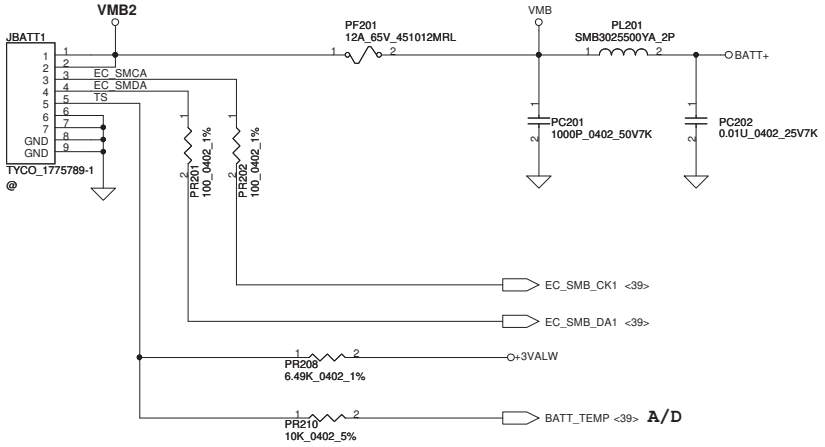
BATT ONLY

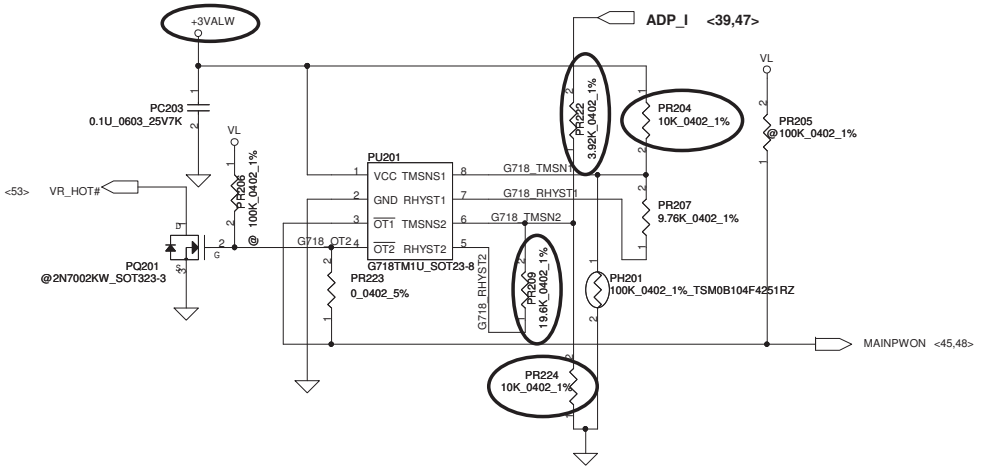
Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

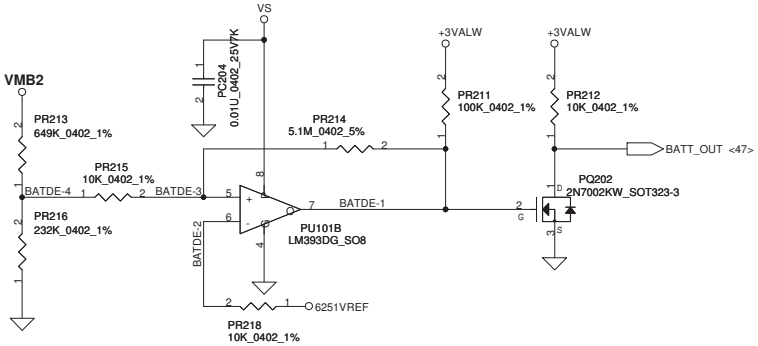
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

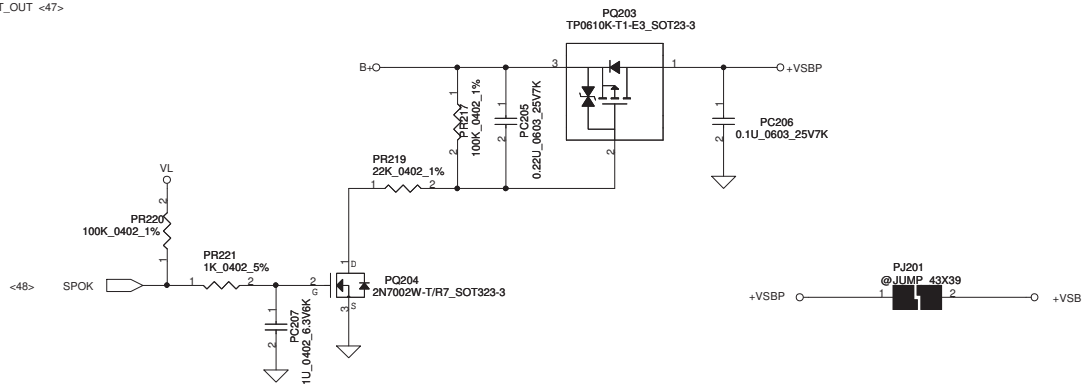
Compal Electronics, Inc.	
Title	PWR DCIN / Vin Detector /Pre-charge
Size: Custom	Document Number: PIQY0/Y1
Rev	0.1
Date: Wednesday, October 06, 2010	Sheet 52 of 63

PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



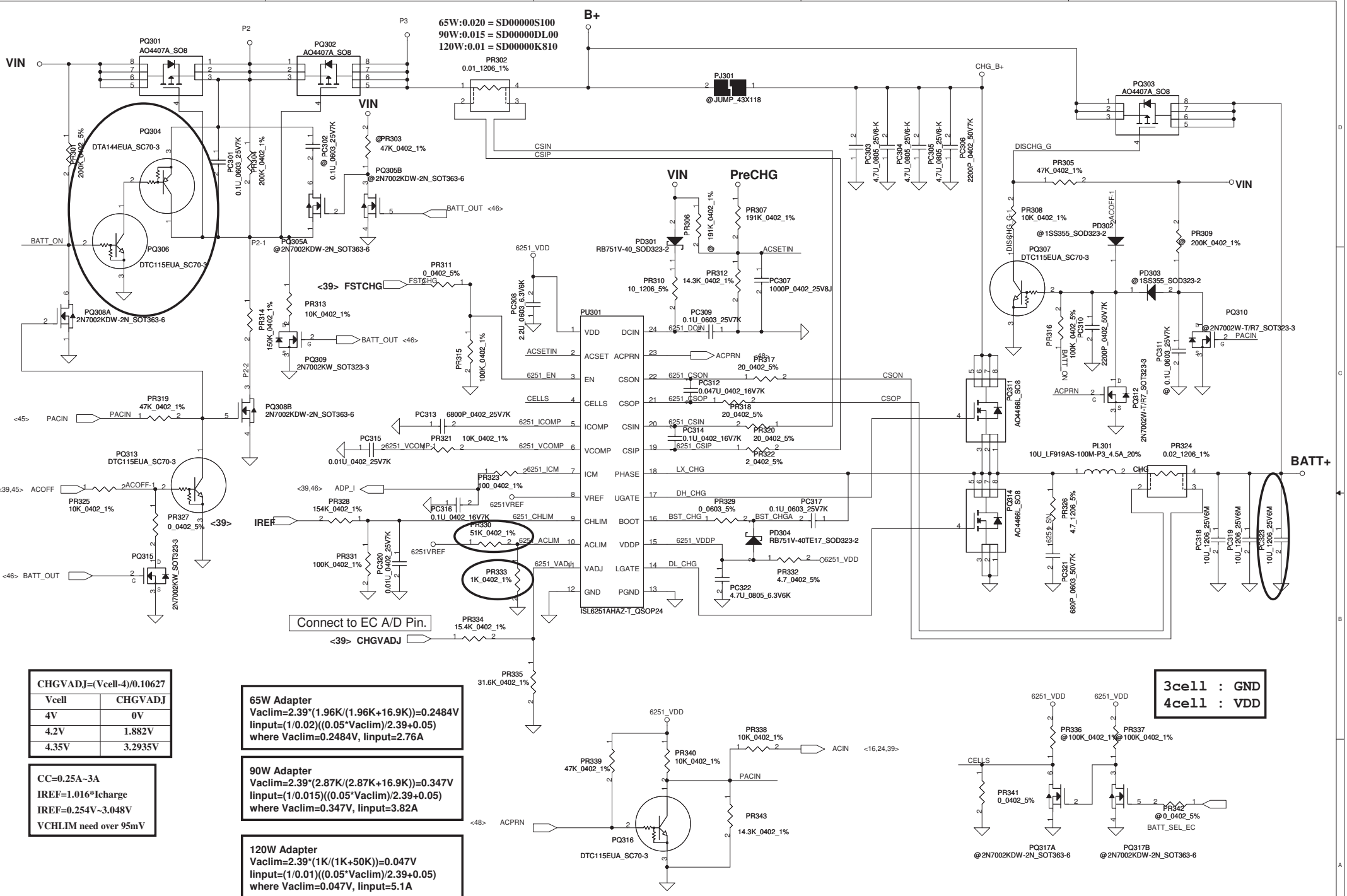






Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: PIQY0/Y1		Rev: 0.1
Date: Wednesday, October 06, 2010	Sheet 53 of 63		



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

65W Adapter
Vaclim=2.39*(1.96K/(1.96K+16.9K))=0.2484V
linput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2484V, linput=2.76A

90W Adapter
Vaclim=2.39*(2.87K/(2.87K+16.9K))=0.347V
linput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.347V, linput=3.82A

120W Adapter
Vaclim=2.39*(1K/(1K+50K))=0.047V
linput=(1/0.01)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.047V, linput=5.1A

65W : PR330=16.9K, PR333=1.96K
90W : PR330=16.9K, PR333=2.87K
120W : PR330=50K, PR333=1K

3cell : GND
4cell : VDD

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

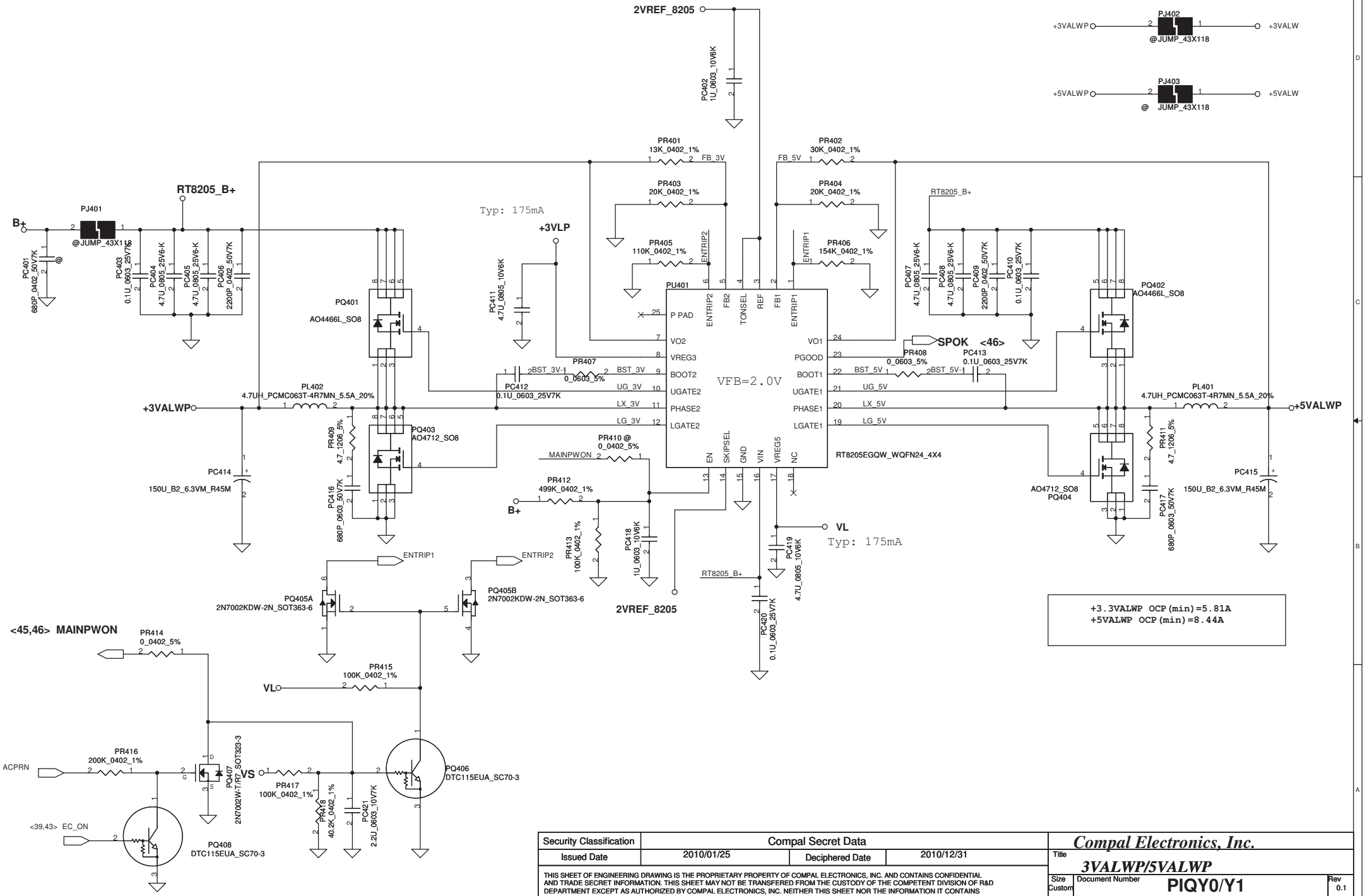
Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	PIQY0/Y1	0.2

Date: Wednesday, October 06, 2010 | Sheet 54 of 63

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



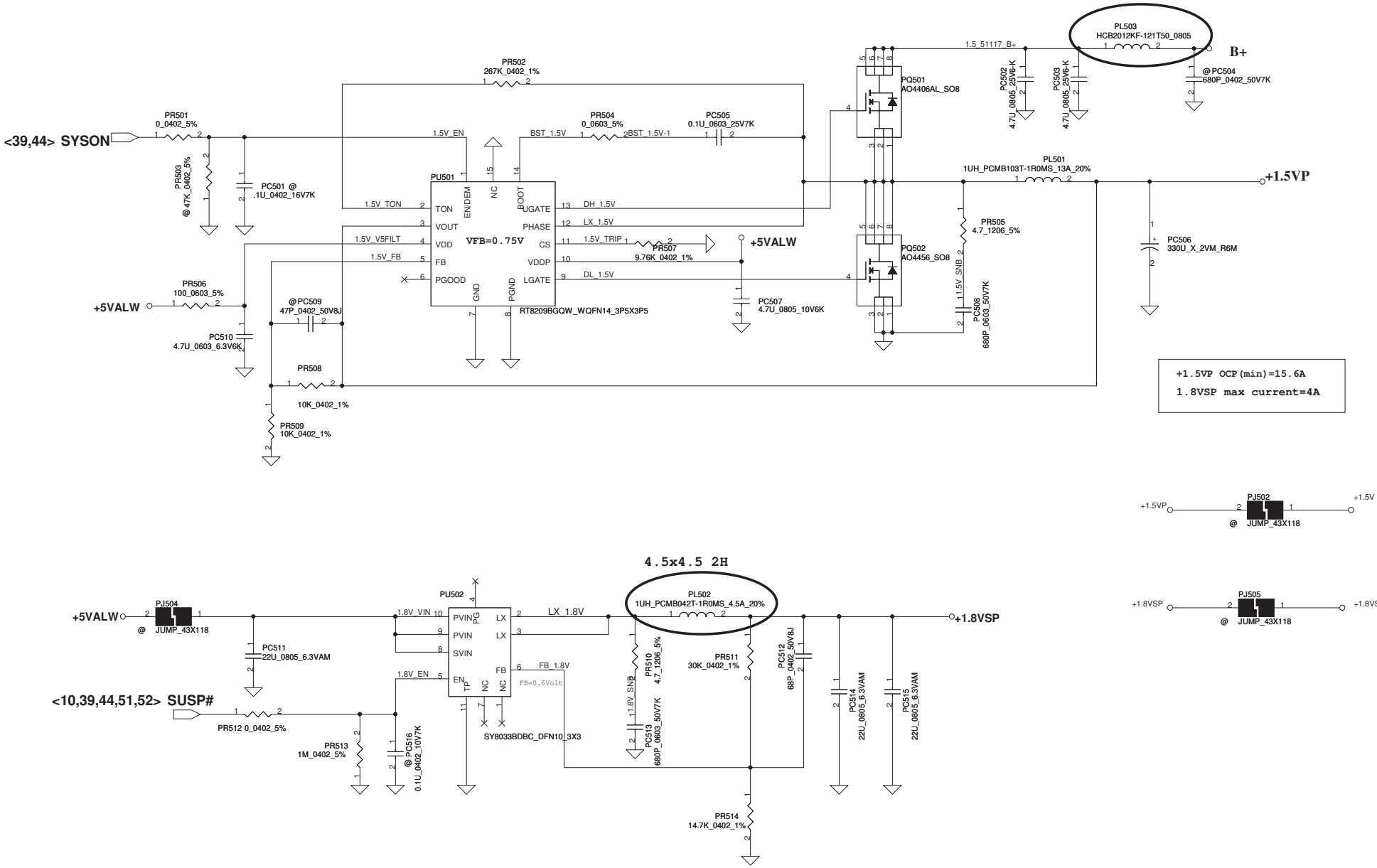
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 55 of 63



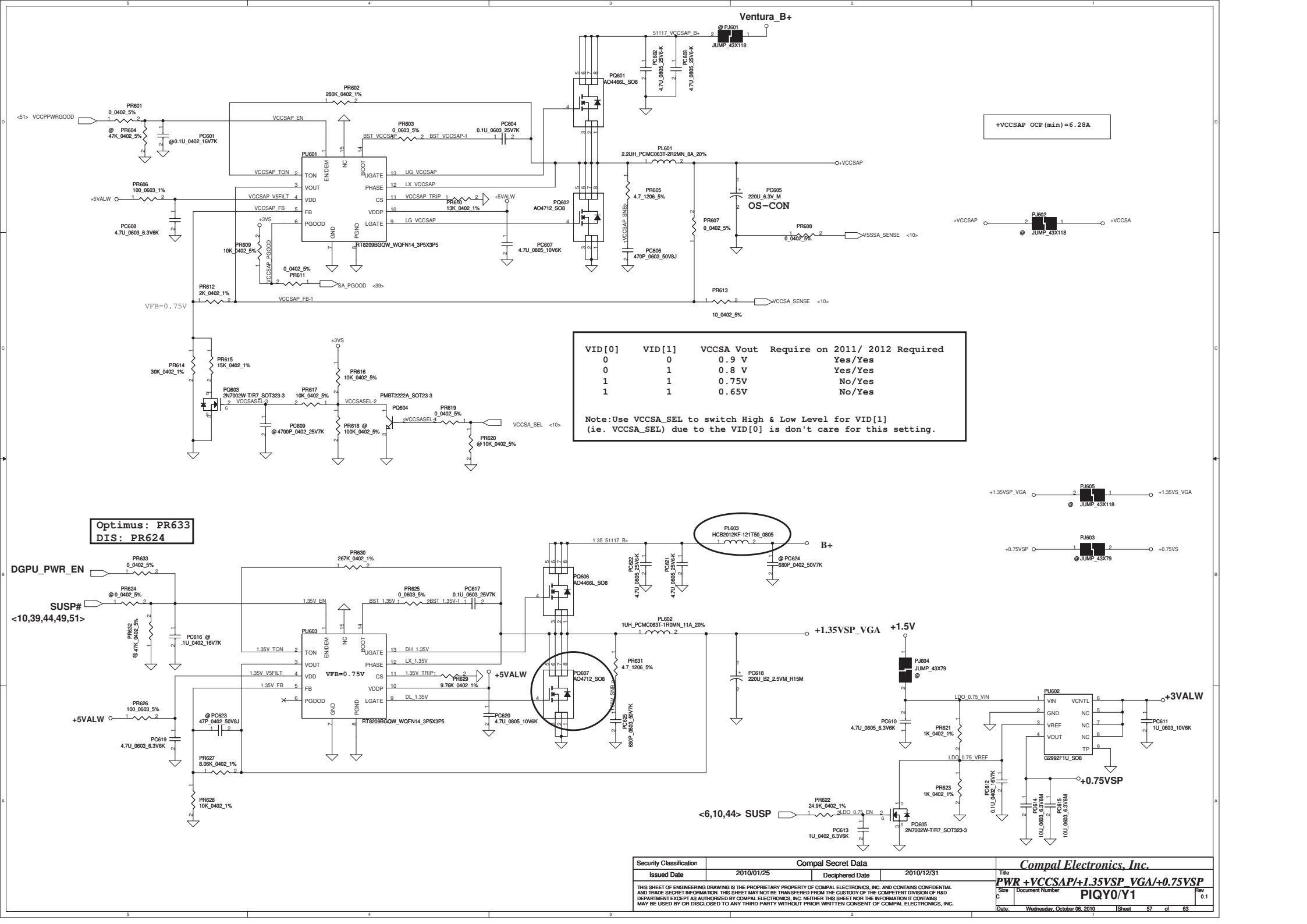
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size	Document Number	Rev
Custom	**PIQY0/Y1**	0.1

Date: Wednesday, October 06, 2010 | Sheet 56 of 63



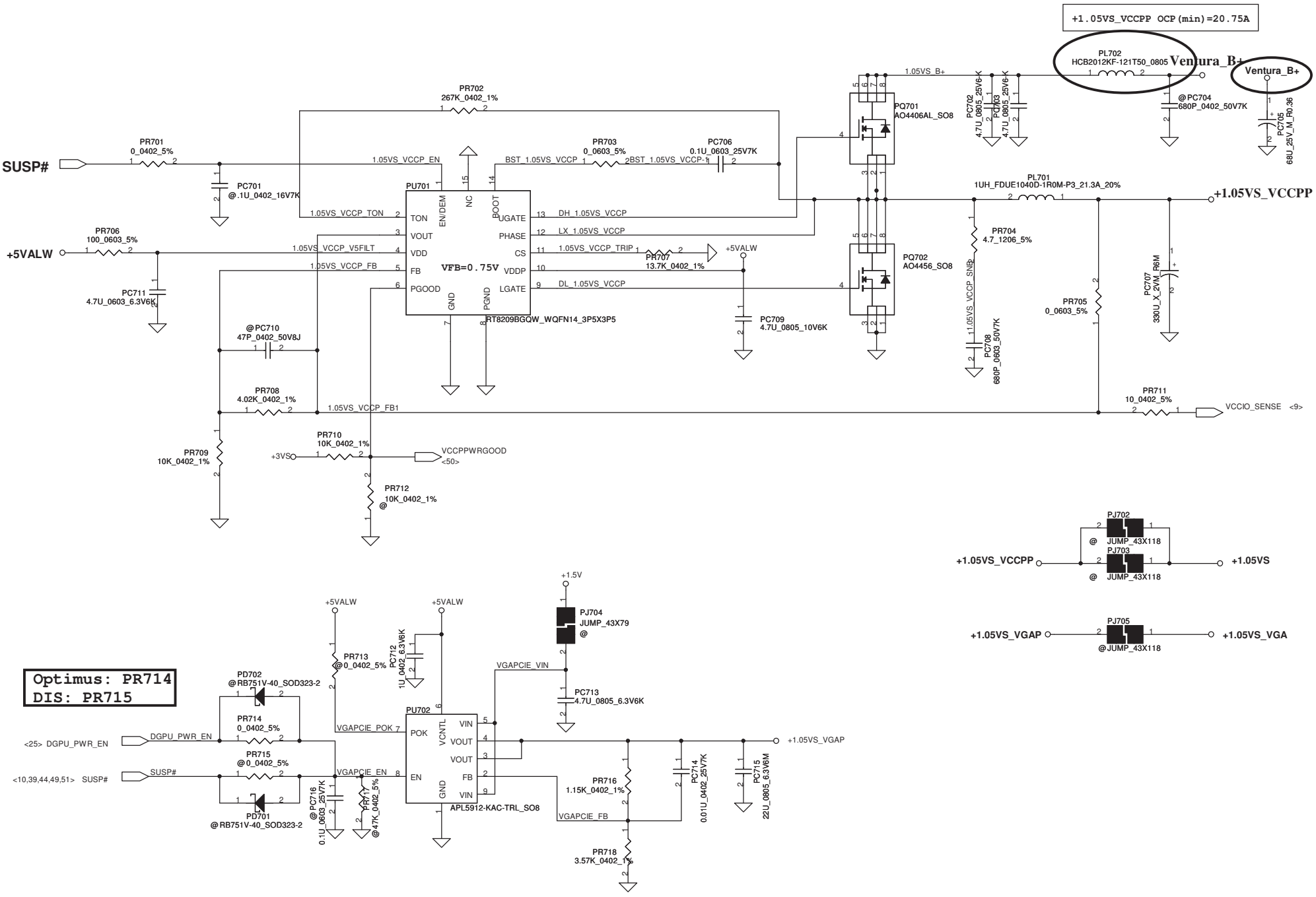
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +VCCSAP/+1.35VSP_VGA/+0.75VSP

Size	Document Number	Rev
C	PIQY0/Y1	0.1

Date: Wednesday, October 06, 2010 Sheet 57 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: *PWR +1.05VS_VCCPP/1.05VS_VGA*

Size	Document Number	Rev
Custom	PIQY0/Y1	0.1

Date: Wednesday, October 06, 2010 Sheet 58 of 63

N12P-GS

GPIO6 (GPU_VID1)	GPIO5 (GPU_VID0)	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6 (GPU_VID1)	GPIO5 (GPU_VID0)	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

Optimus: PR801
DIS: PR802

GS: PR840,PR845,PR847,PR853
GT/GT1:PR843,PR844.PR846,PR854

PU801 ISL6264CRZ-T_QFN40_6X6

PQ807 2N7002KW_SOT323-3
PQ806 2N7002KW_SOT323-3
PQ801 TPCA8030-H_SOP-ADV8-5
PQ802 TPCA8028-H_SOP-ADVANCE8-5
PQ803 TPCA8030-H_SOP-ADV8-5
PQ804 TPCA8028-H_SOP-ADVANCE8-5

PL801 HCB4532KF-800T90_1812
PL802 0.36UH_PCMC104T-R36MN1R17_30A_20%
PL803 0.36UH_PCMC104T-R36MN1R17_30A_20%

PH801 10K_0603_5%_TSM1A103J4302RE

GPU_VID1
GPU_VID0
+VGA_CORE
VGA_B+
VCC_PRM1
VSUM1
VGA_ISEN1
VGA_ISEN2
VDD_SENSE_VGA
GND_SENSE_VGA
B value=4300K

Security Classification	Compal Secret Data		
Issued Date	2006/12/12	Deciphered Date	2007/12/12

Compal Electronics, Inc.

Title: Power-VGA_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 59 of 63

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

PR956
QC:19.1K
DC:19.6K

change from 43P to 47P
for shortage problem
2010-03-15

QC: PC935
DC: PC933

PR956
QC:3.724K
DC:2.15K

PR959
QC:1.54K=120A
DC:887=70A

PR943
0 ohm =>98A (Vboot=0v)
590 ohm=>91A (Vboot=0v)

B value=4700K

B value=4700K

B value=4250K

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR +CPU_CORE/+VGFX_CORE			
Size: Custom	Document Number: PIQY0/Y1		Rev: 0.1
Date: Wednesday, October 06, 2010		Sheet 60 of 63	

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 61 of 63

PIQY1 HW PIR List

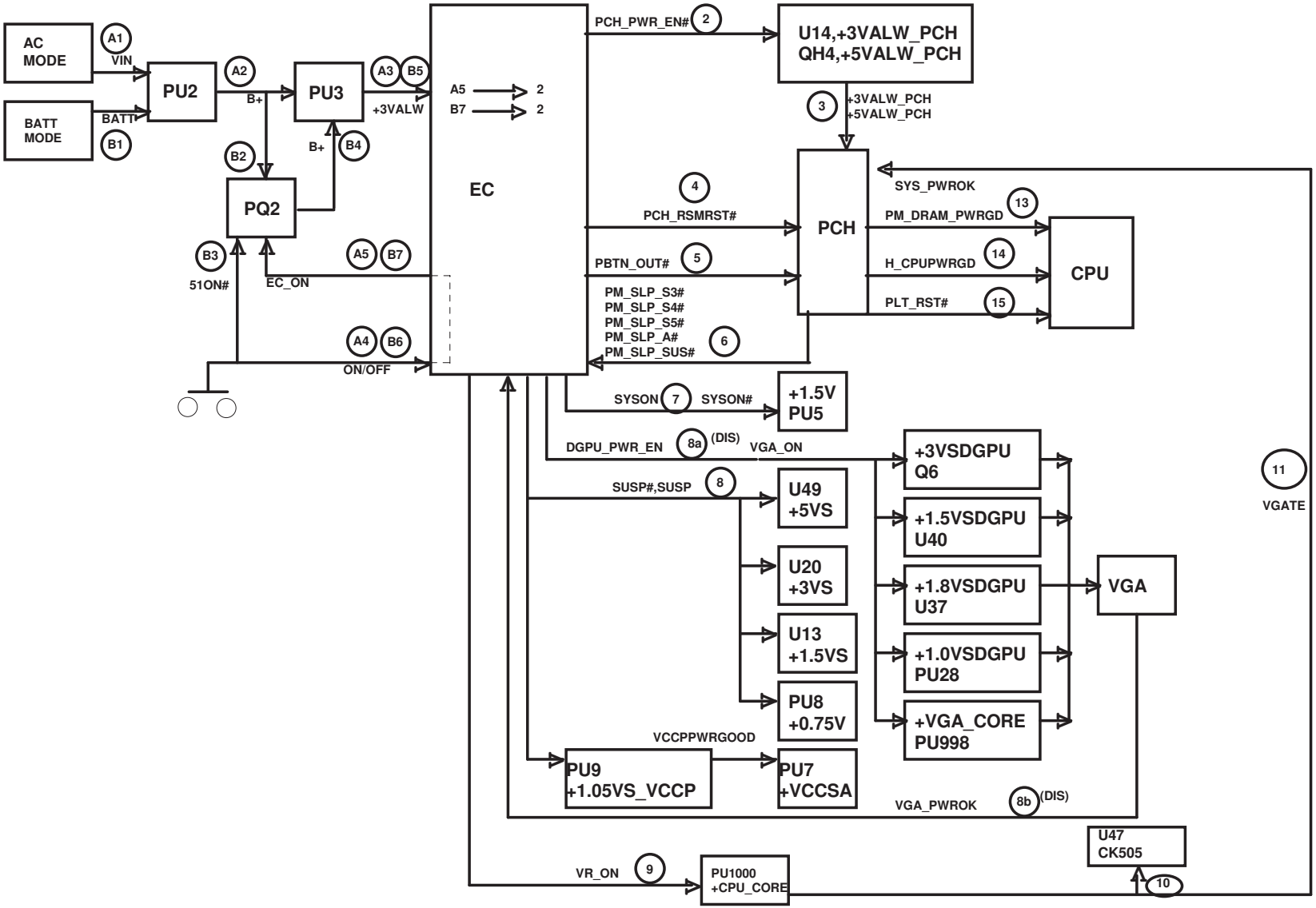
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1071,R1072,R1099,Q121	Reserve USB3.0 power swicth control inverter circuit.
7		P48	Add R1154	For CHG_ON# pull down.
8		P45	Stuff R996,R139,C815, unstuff R1000,C732,C733,Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P09	Add C922	Add C922 to place at CPU sdie.
11		P21	Add R1330	Add for INTVREN control
12		P47	Modify LED1,LED2,LED3,LED5	Change LED type
13		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
14		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
15		P48	Delete USB charger circuit	Remove USB charger function
16		P47	Modify H5,H6,H7 size	From H_3P0 to H_3P8
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C926, C927 0.033u	For 100Hz High Pass filter
19		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
20		P42	Add C928, C929	EMI Request
21		P49	Add J19	for USB30, USB20 colayout design
			Modify J18, J20	for USB30, USB20 colayout design
22		P14	Add Q134, R1347, R1346	Add for Fast boot SPI ROM selection by EC.
23		P37, P44	Add R1344,R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1345	Added for VENTURA detection.

Compal Electronics, Inc.

Title: PIR (HW)

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 62 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: Power sequence			
Size: Custom	Document Number: LA-6361P		Rev: 0.1
Date: Wednesday, October 06, 2010	Sheet 63 of 63		