

Compal confidential

Schematics Document

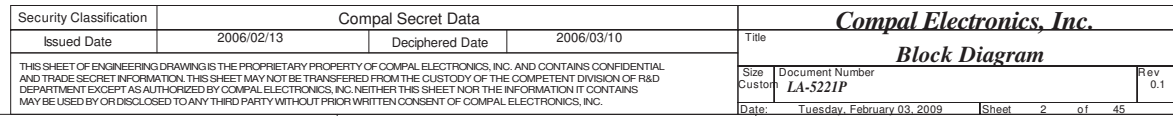
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

Fossil

2009-02-03

機 密	等級	硬體二部	
	產出人員		
	產出日期		
	解密日期		

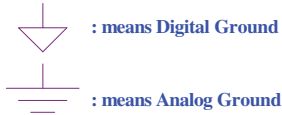
Security Classification		Compal Secret Data		Title		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.		
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				Size	Document Number	Rev
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

ULV723@ mean CPU ULV723 (U1) for L01
SU9300@ mean CPU SU9300 (U1) for L02



I2C / SMBUS ADDRESSING

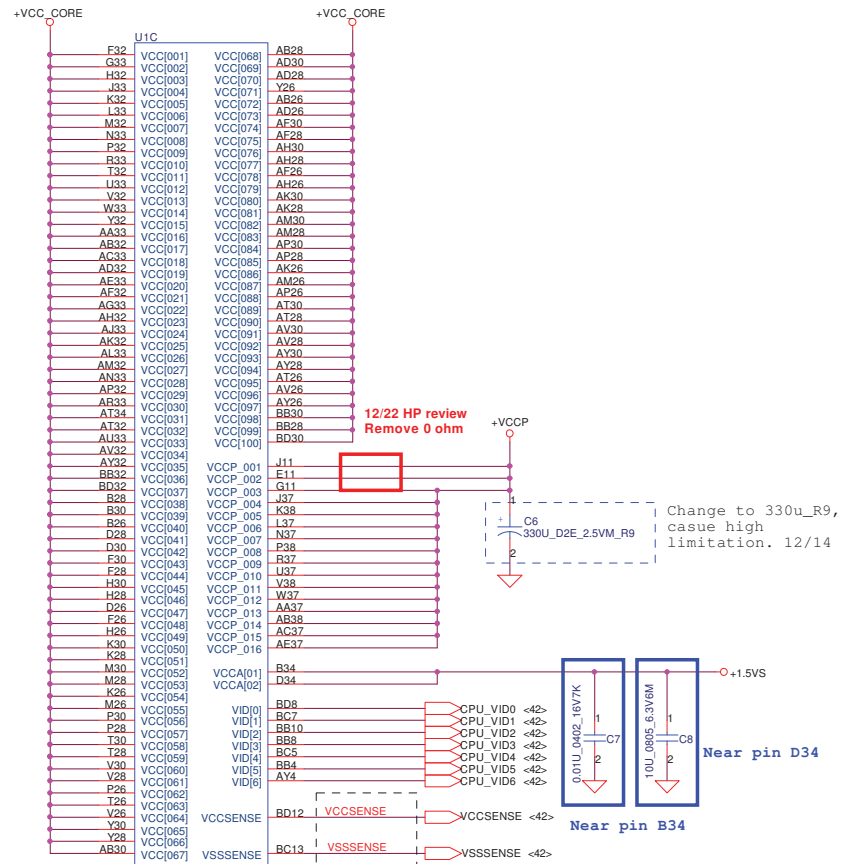
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

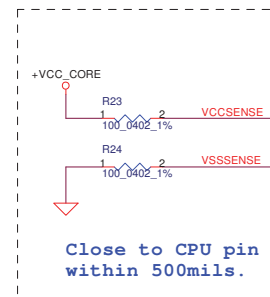
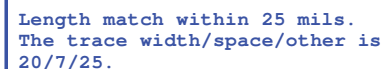
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				Size Custom	Document Number LA-5221P	Rev 0.1
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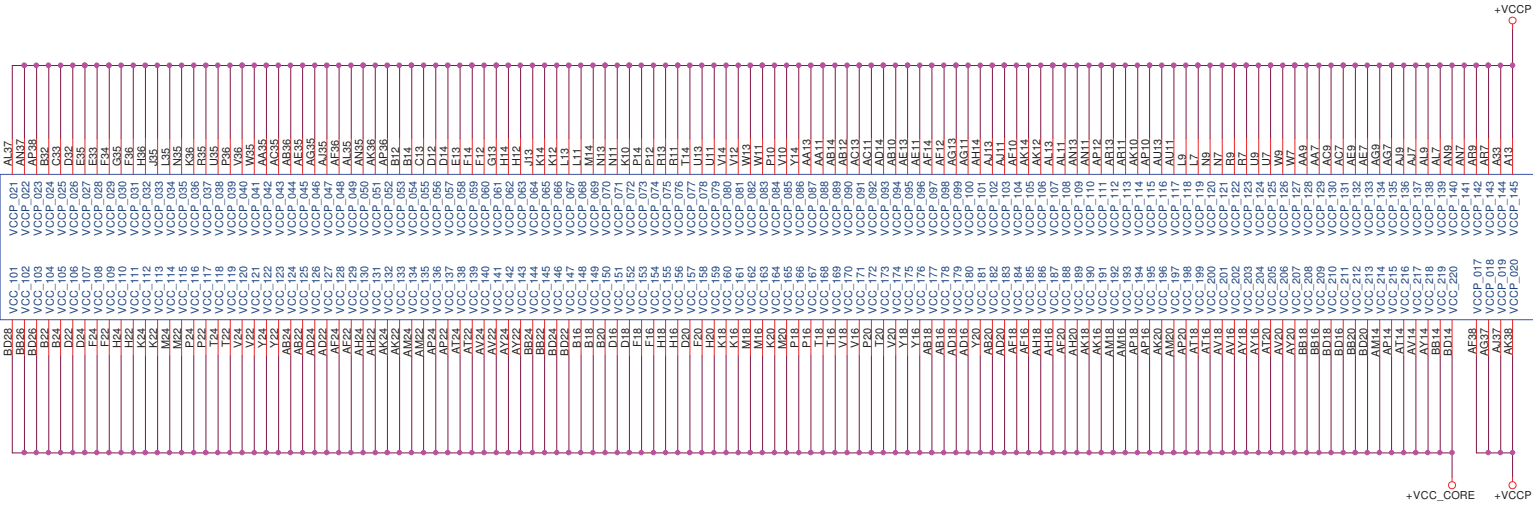
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



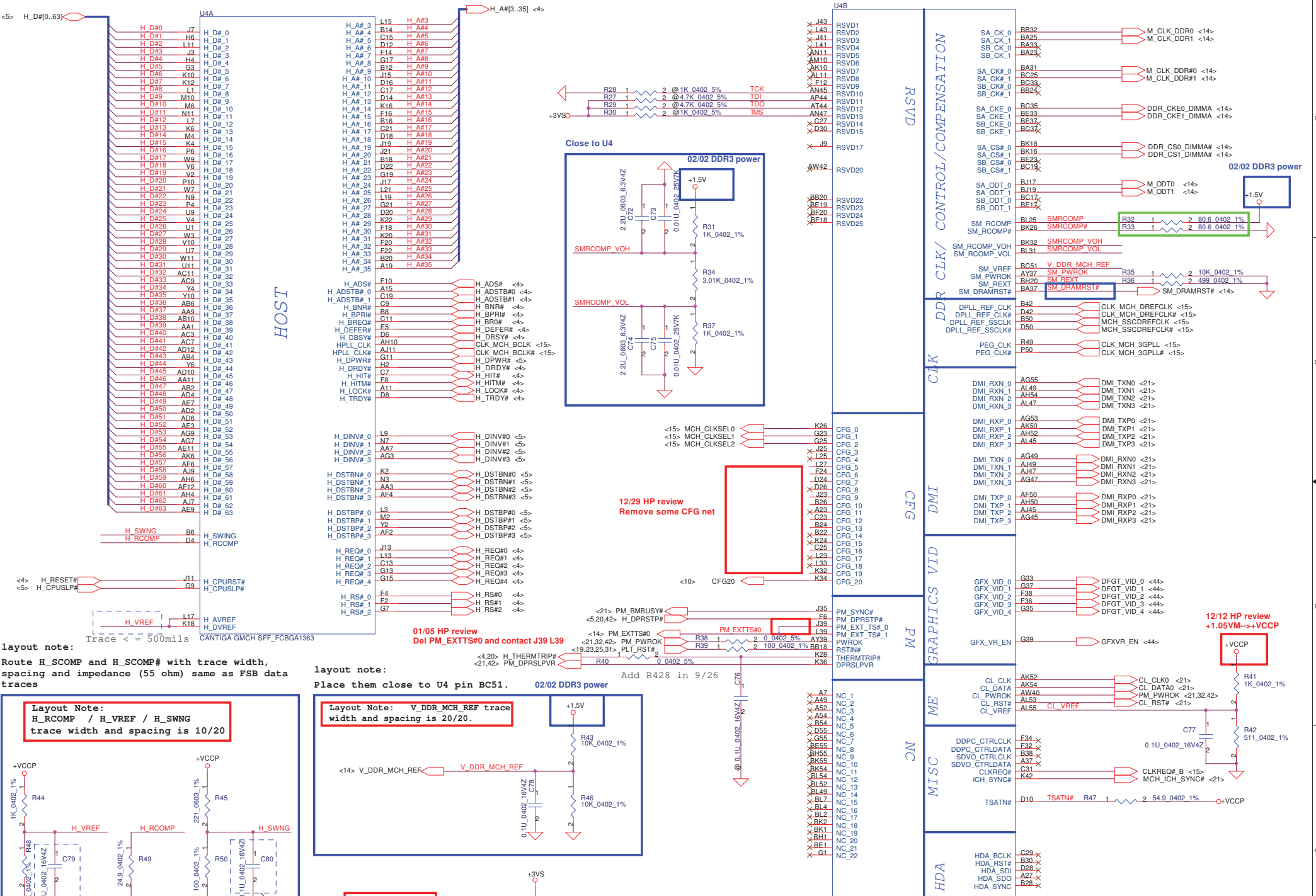
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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ULV723@



U1F
PENRYN SFF_UFCBGA956

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layout note:
Route H_SCMP and H_SCMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

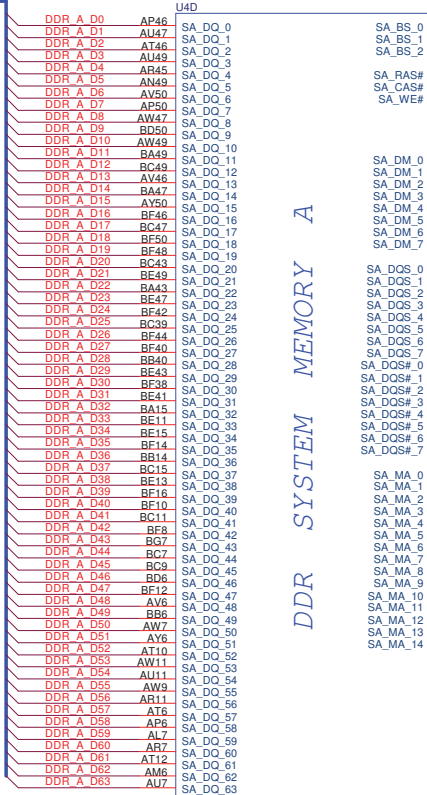
Near B6 pin

layout note:
Place them close to U4 pin BC51. 02/02 DDR3 power

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

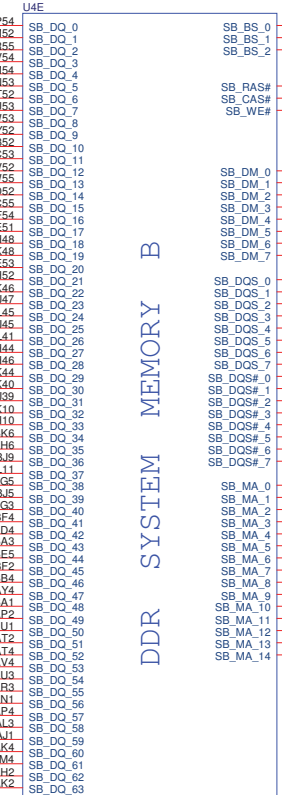
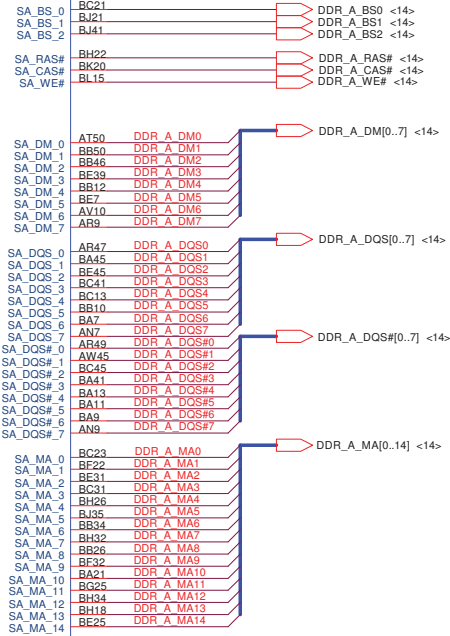
PM_EXTTS#0 R52

<14> DDR_A_D[0..63]



CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY A



CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY B

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title Cantiga(2/6)-DDR2 A/B CH	
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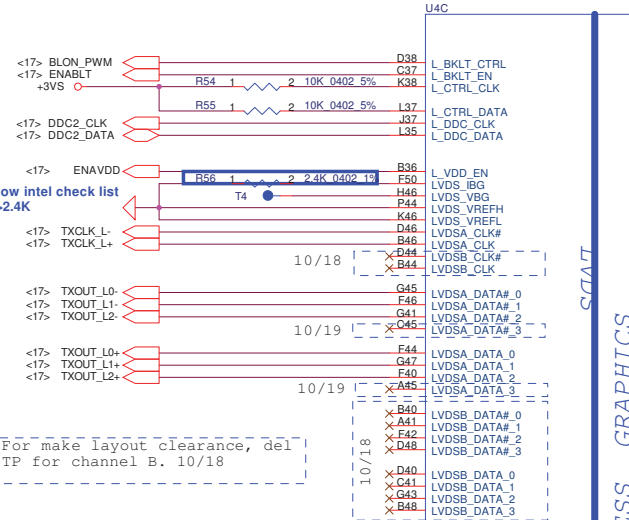
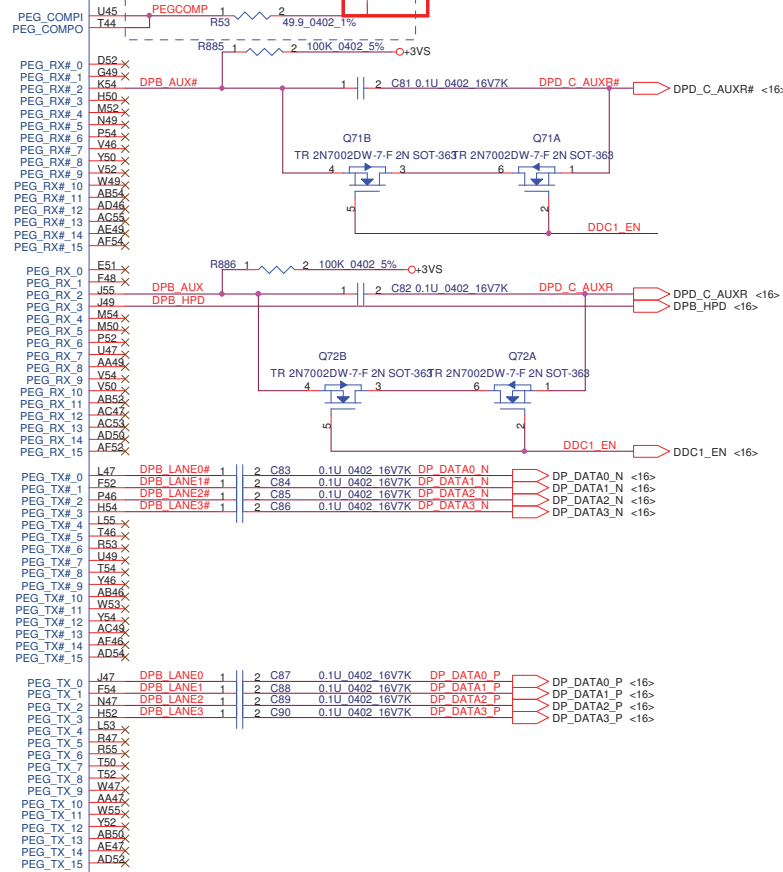
Place R53 <500mils to U4 pin U45&T44.

12/22 +VCC_PEG-->+VCCP

layout note:

PEGCOMP trace width and spacing is 20/25 mils.

+VCCP



For make layout clearance, del TP for channel B. 10/18

12/219 HP review
No TV out and contact to GND

12/19 HP review
CMOS buffers and can be left as NC

12/19 HP review
No CRT out and contact to GND

12/19 HP review
CMOS buffers and can be left as NC

Close to pin D32 and keep 30mil space to other part/trace.

Strap Pin Table

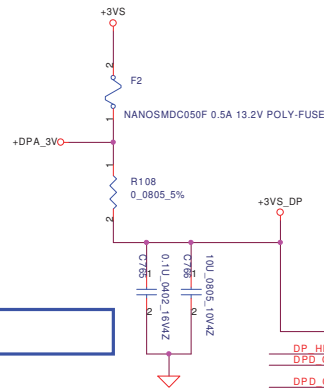
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

12/29 HP review
Remove some reserved R for CFG net

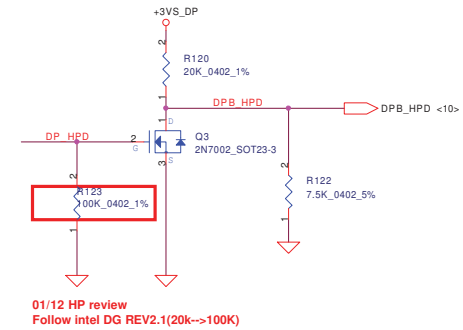
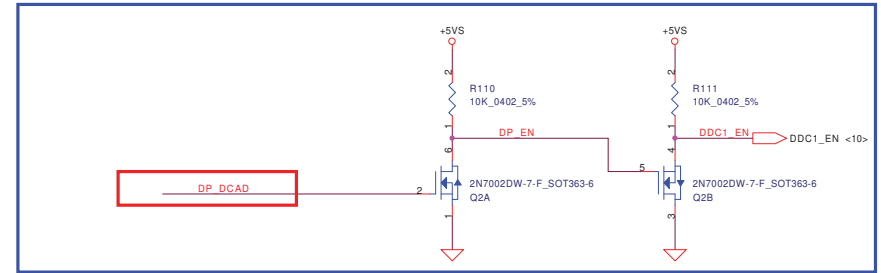
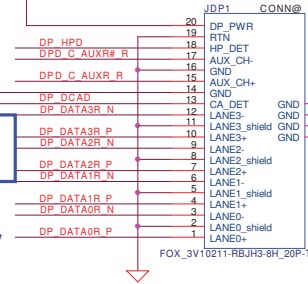
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01/12
Del reserved ESD part, because M/B no more space



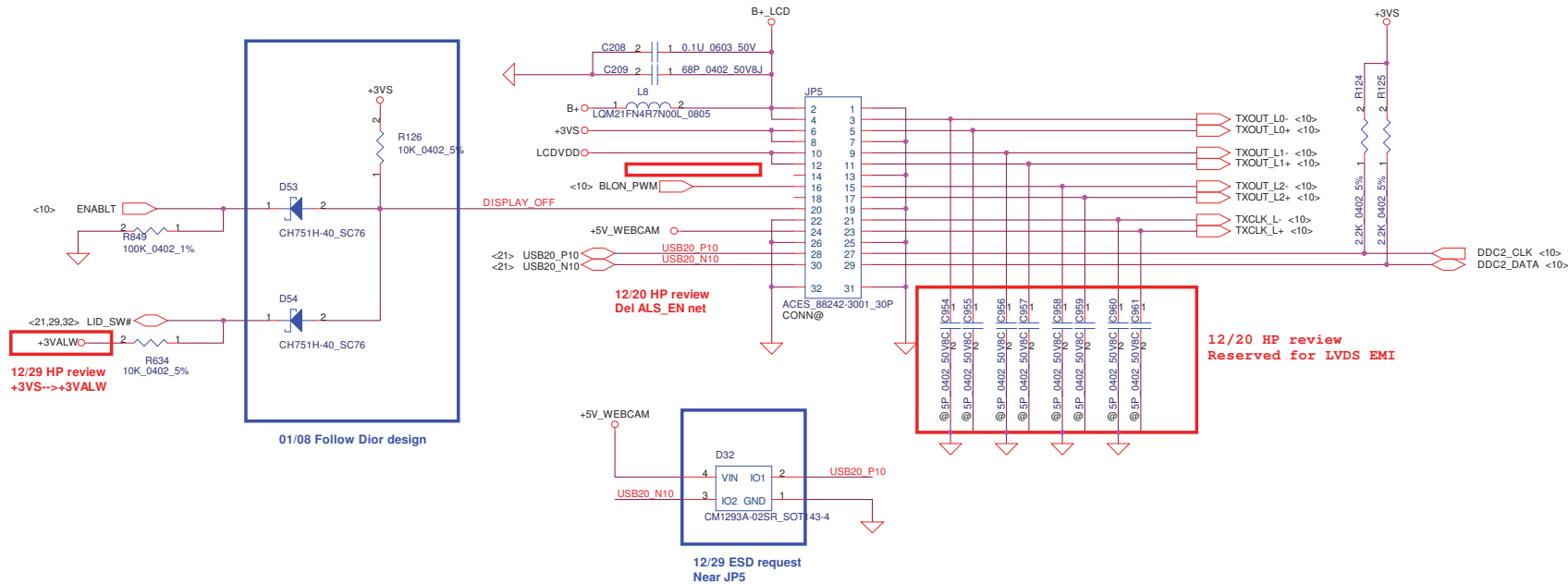
01/06
Del R115, support DP only
R116-->@



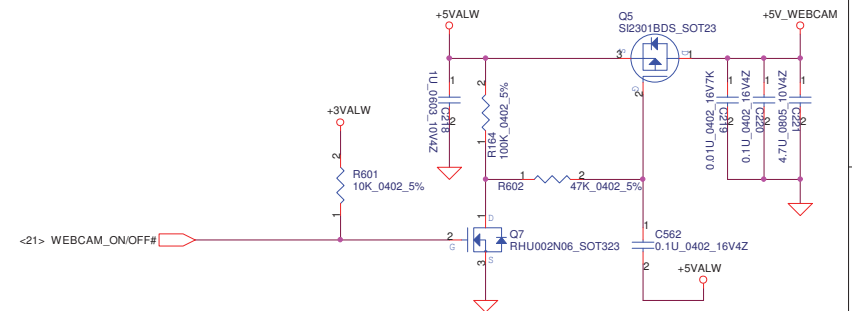
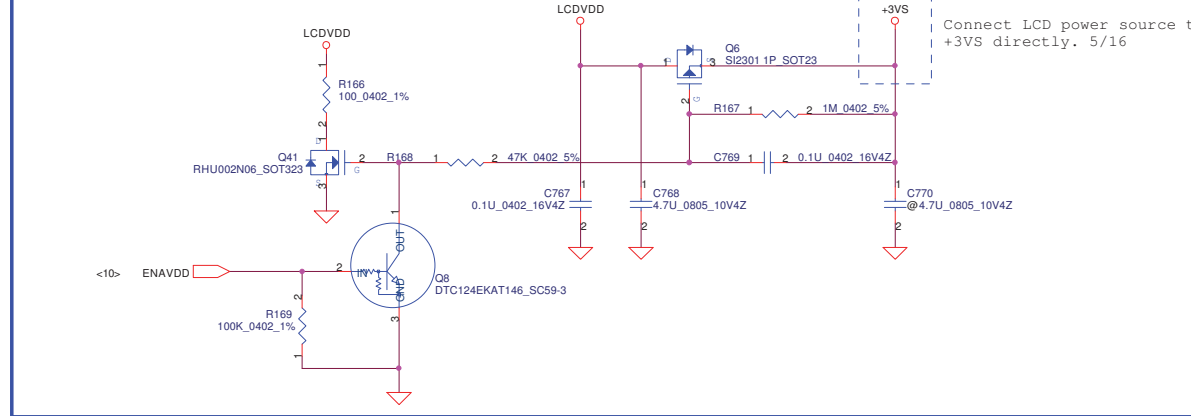
01/12 HP review
Follow intel DG REV2.1(20k-->100K)

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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	Display Port Connector
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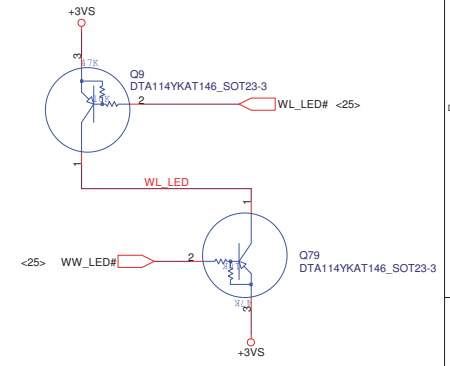
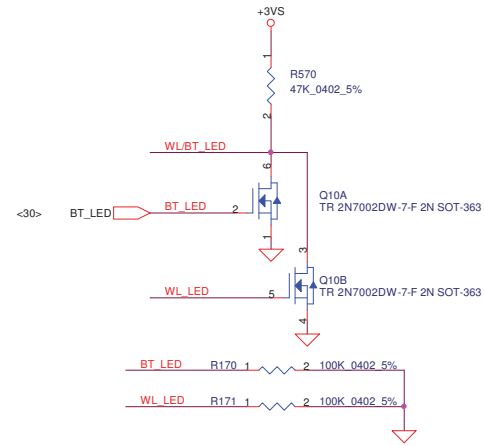
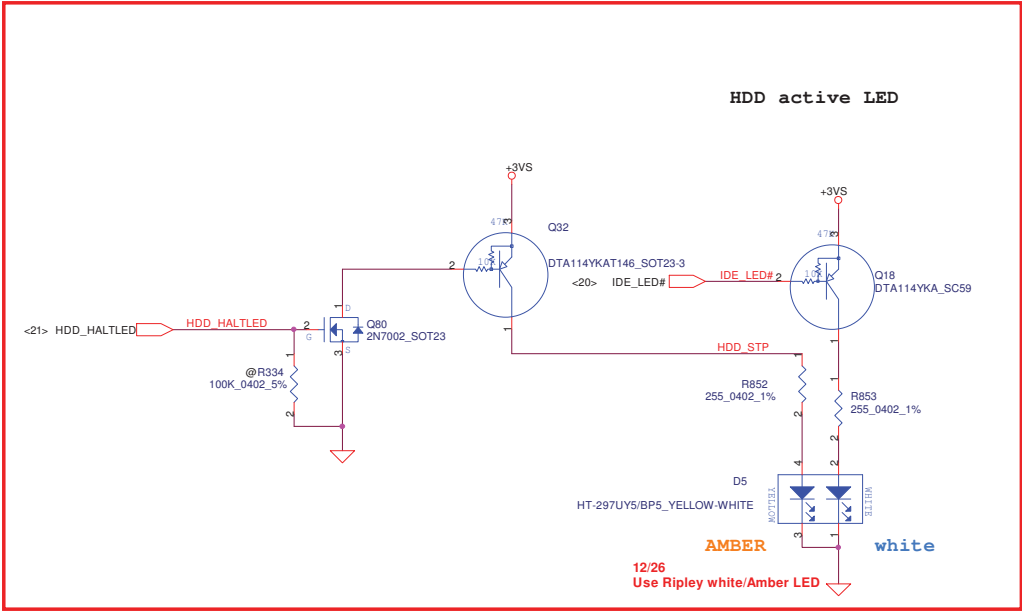
LED/PANEL BD. CONN.



LCD POWER CIRCUIT

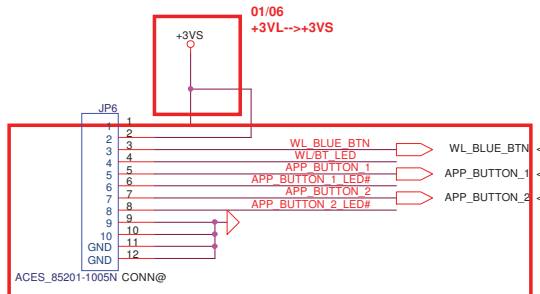


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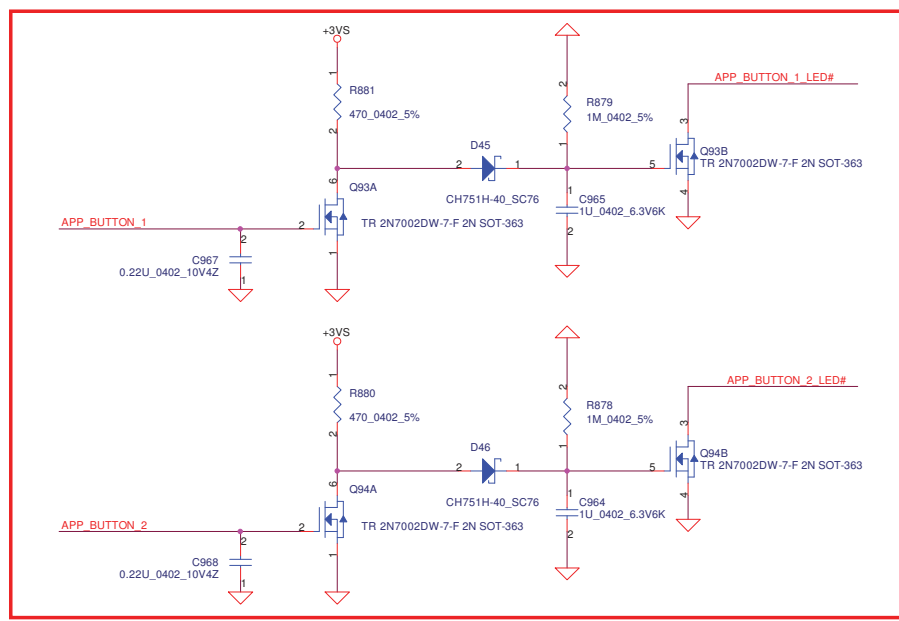
01/06
Small board no more space,so add circuit on main board

To LED small board



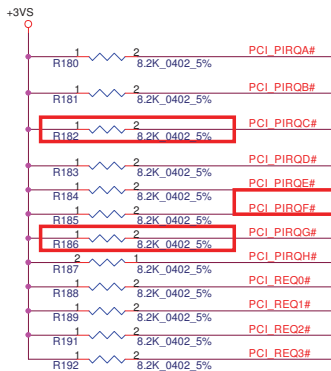
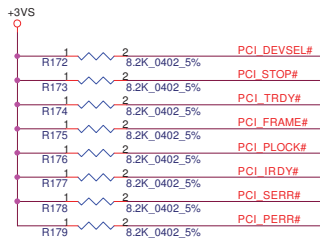
01/06
Confirm LED GPIO ok

12/26
Power LED on small board



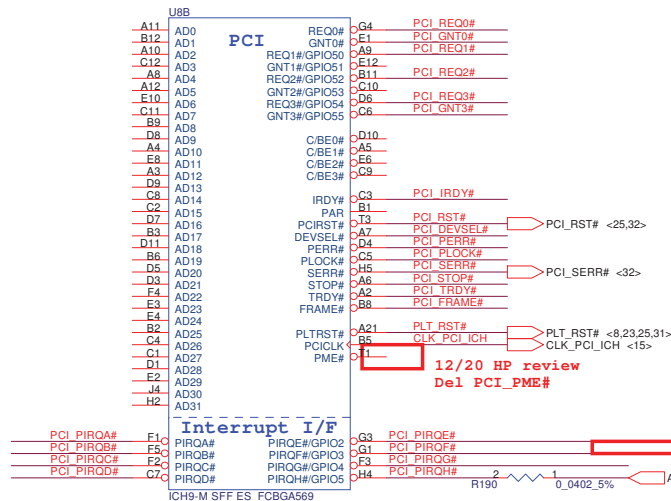
12/26
LID switch on small board

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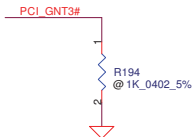
01/13 HP review
Add R182 and R186

12/20 HP review
Update net (No ODD_DET#)

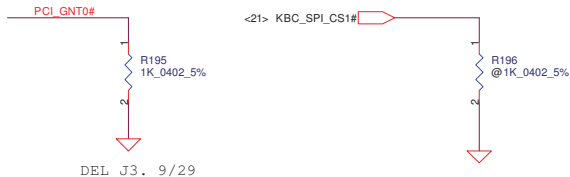


12/20 HP review
Update net (No ODD_DET#)

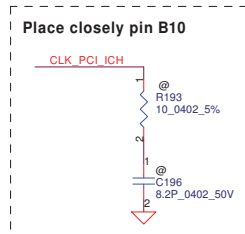
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

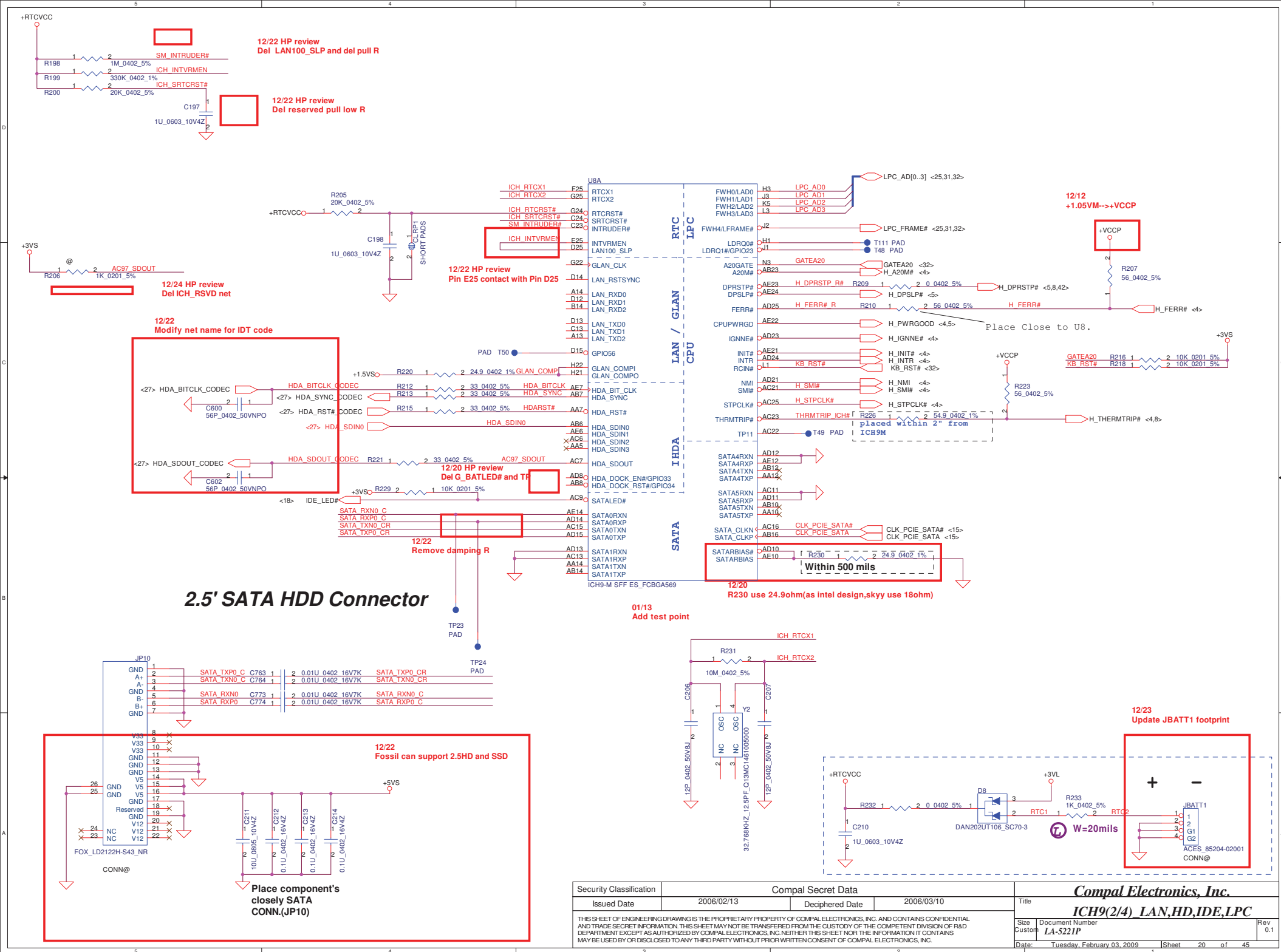


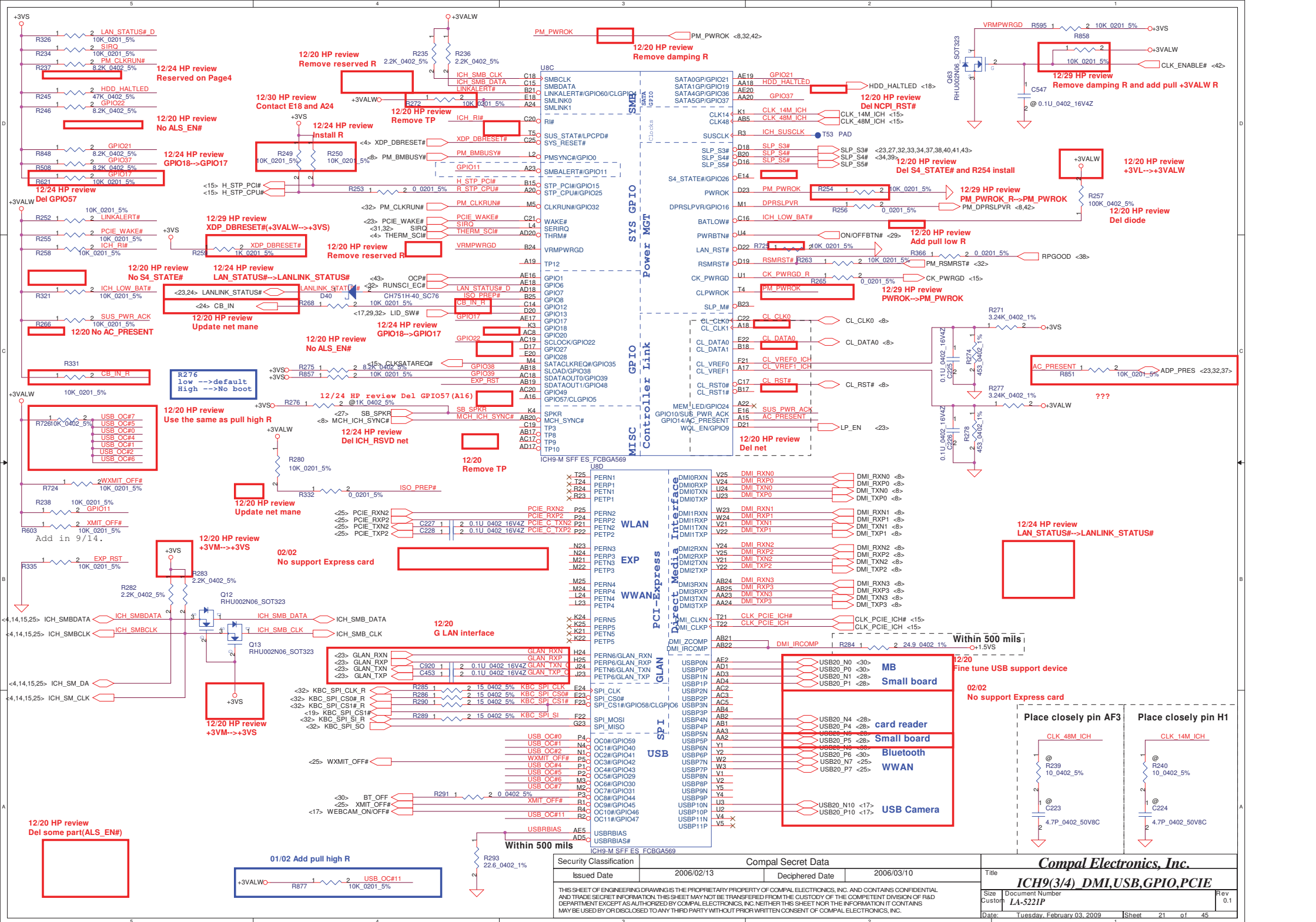
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

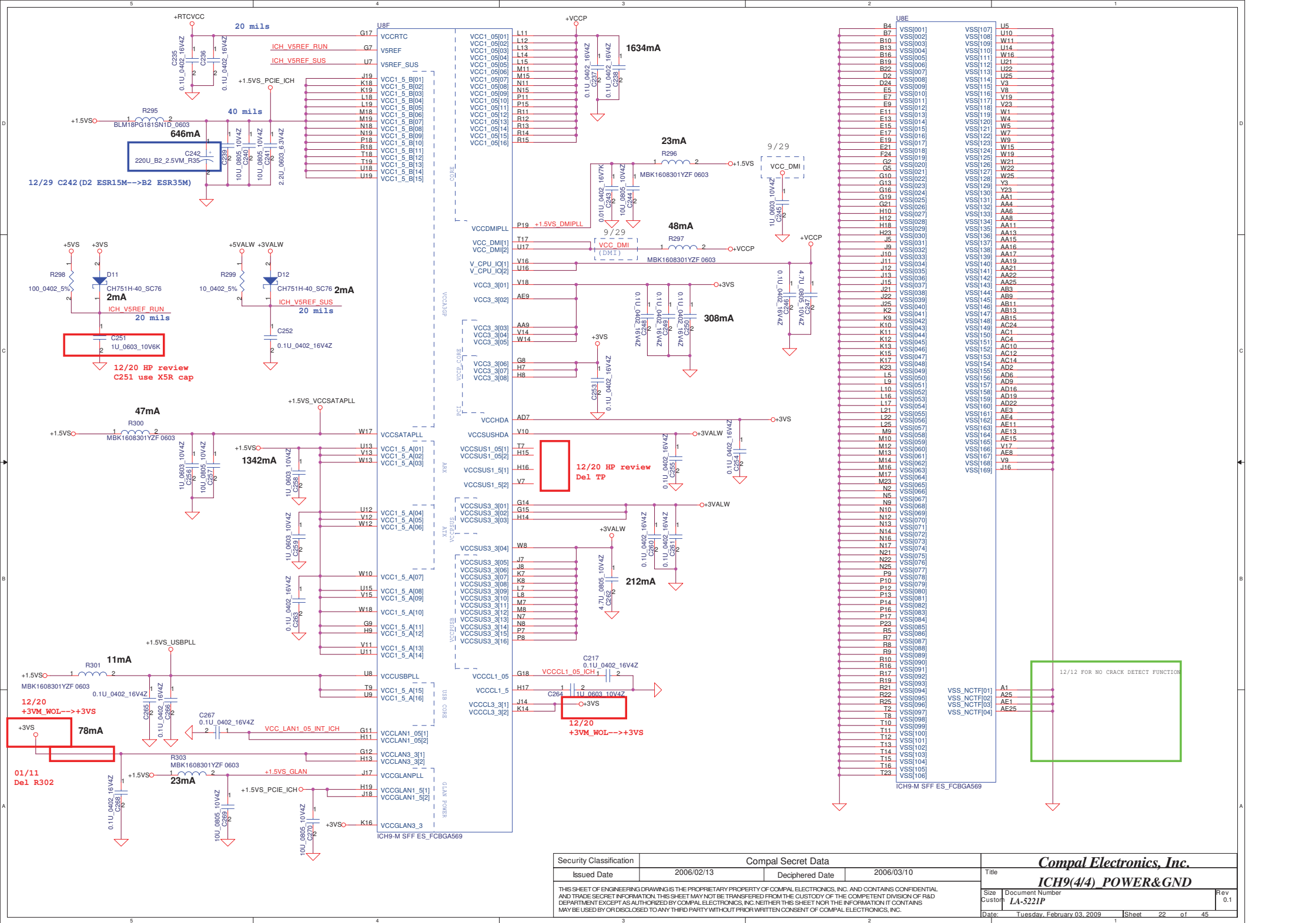


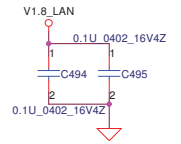
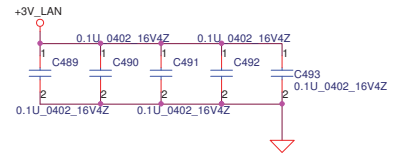
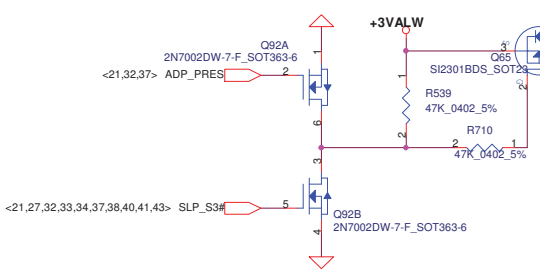
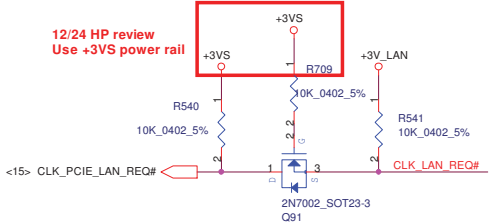
DEL J3. 9/29



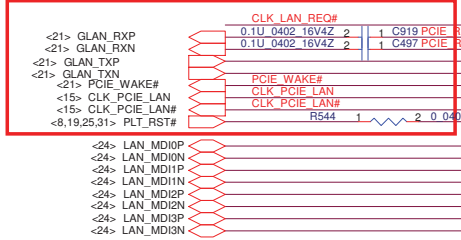








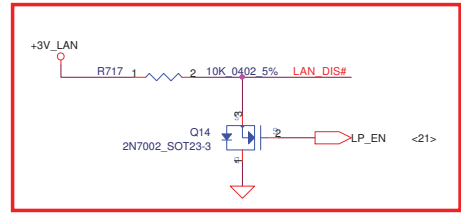
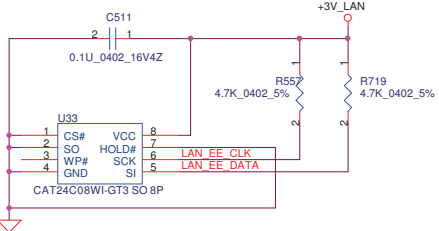
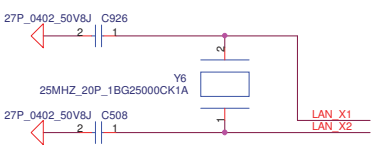
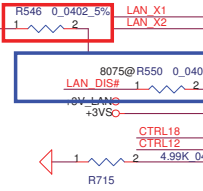
12/20
Update net



12/20
Del reserved SPI net

12/26
8072@-->install

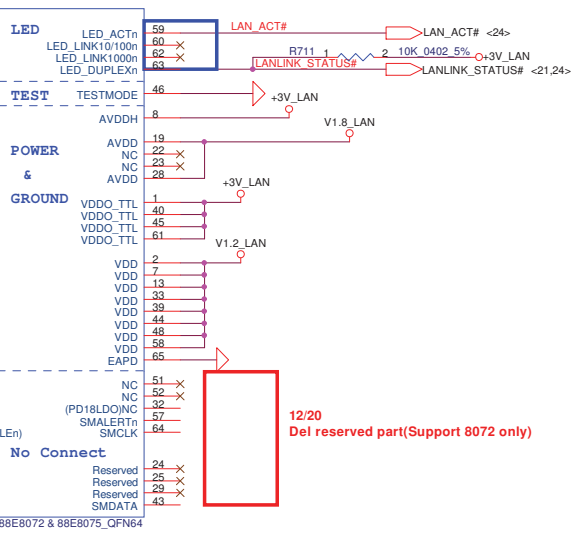
01/23
No support 8075



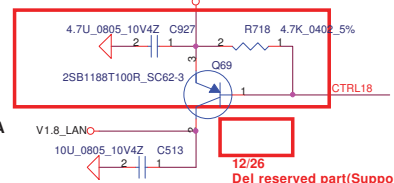
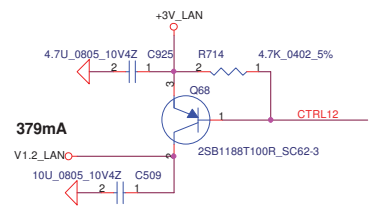
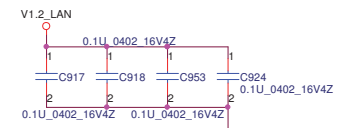
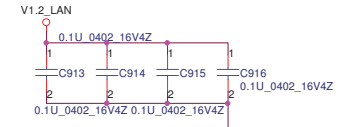
12/22 HP review
Add LP_EN

	88E8072	88E8075
Insert	R653	R654
	C533	R655
	R440	U36
	Q28	C694
		R659
		R658
		R656
		R652
	R660	

0115 Marvell
Open Pin62 Pin63



12/20
Del reserved part(Support 8072 only)



12/26
8072@-->install

151mA

12/26
Del reserved part(Support 8072 only)

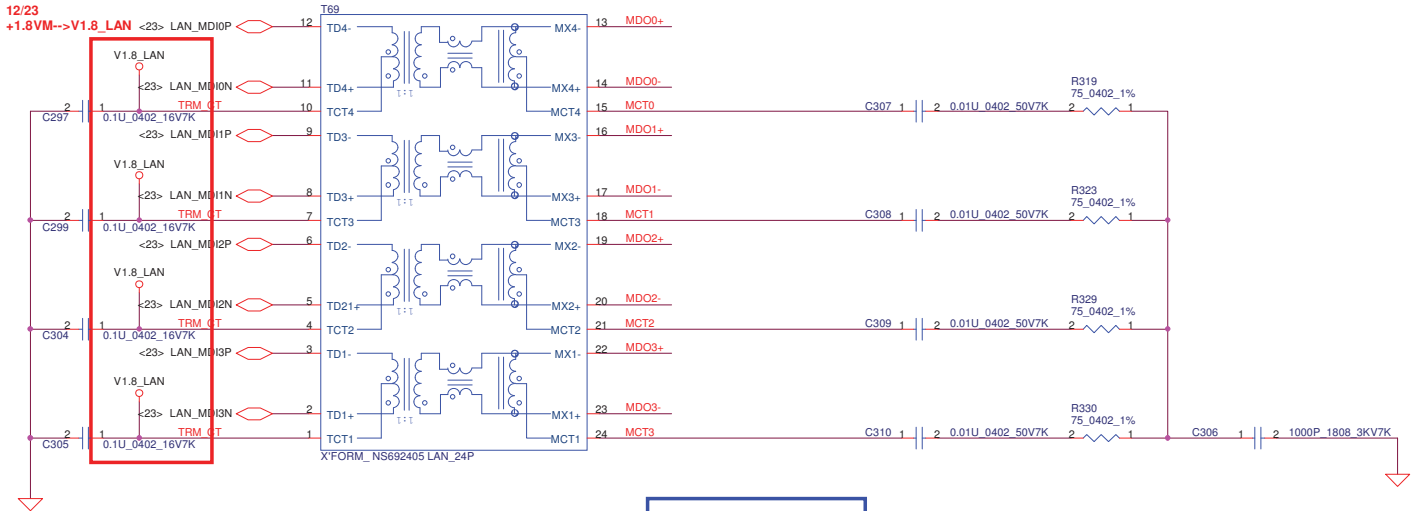


12/20
Del reserved SPI part

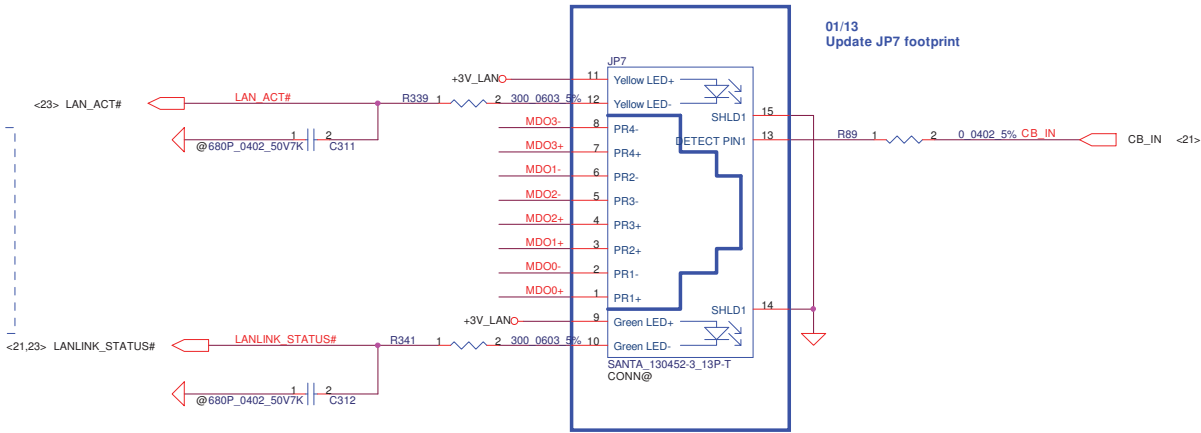
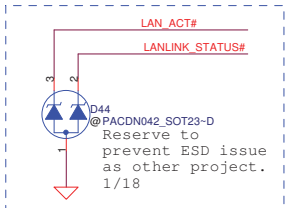


12/15 No support Docking

Delete all termination cause they are already inside BOAZMAN. 9/28

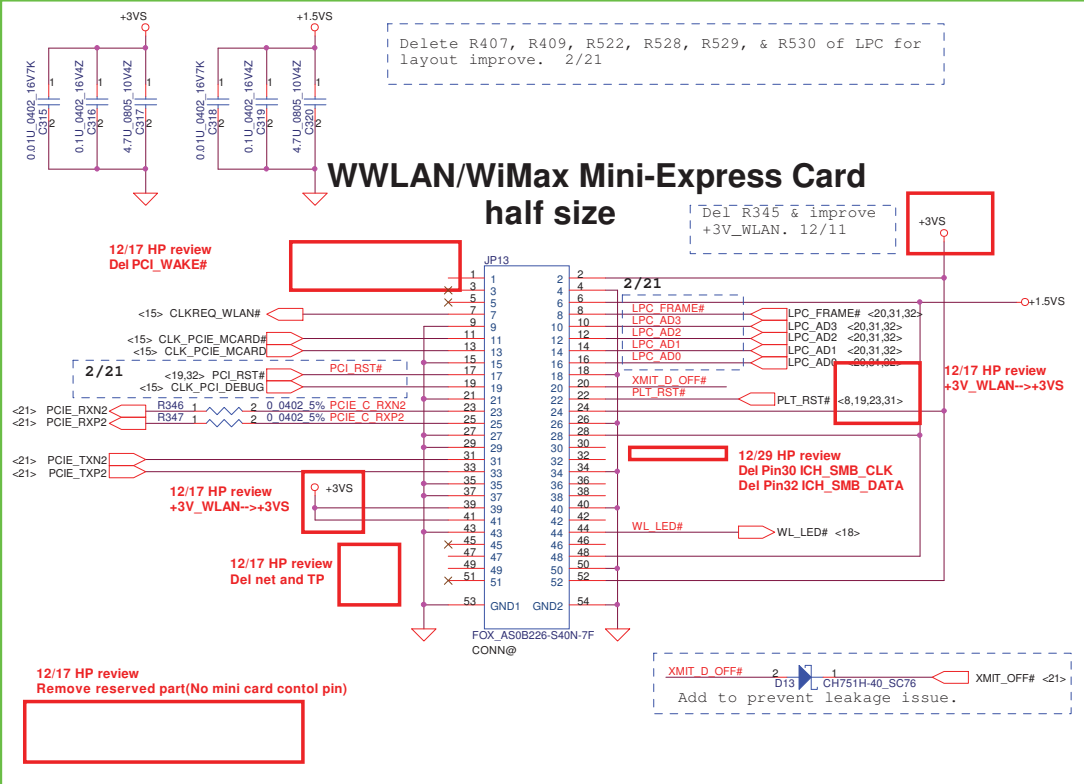


12/29 HP review
Del Q23 Q24



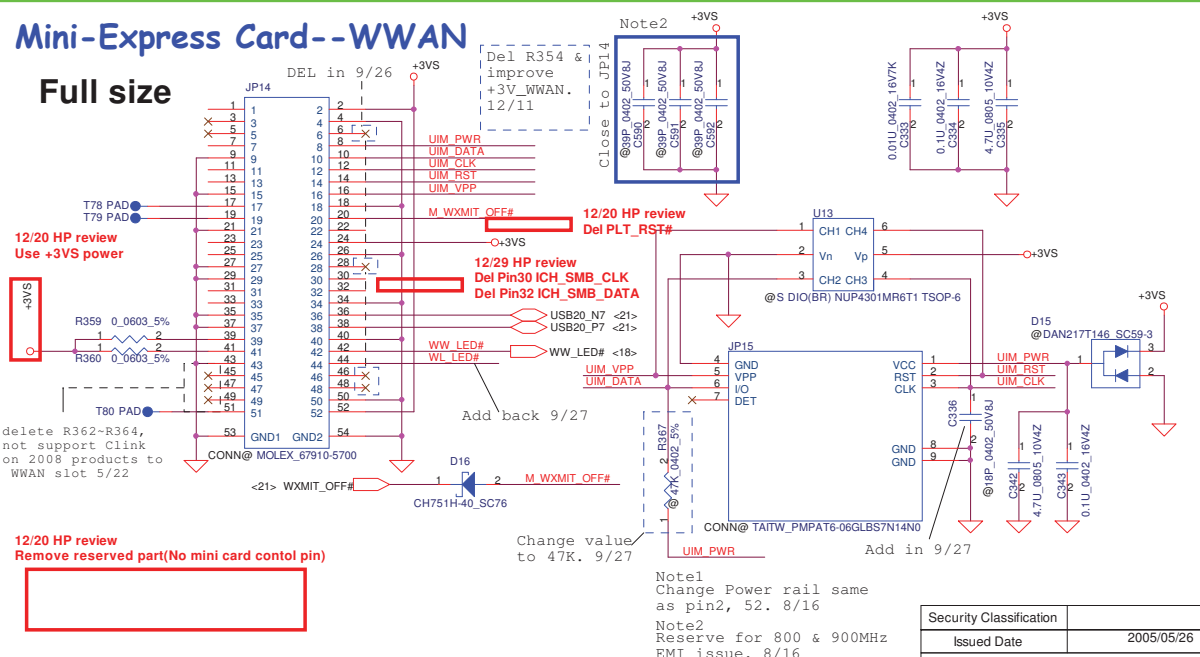
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				Date: Tuesday, February 03, 2009	Sheet 24 of 45

WWLAN/WiMax Mini-Express Card half size

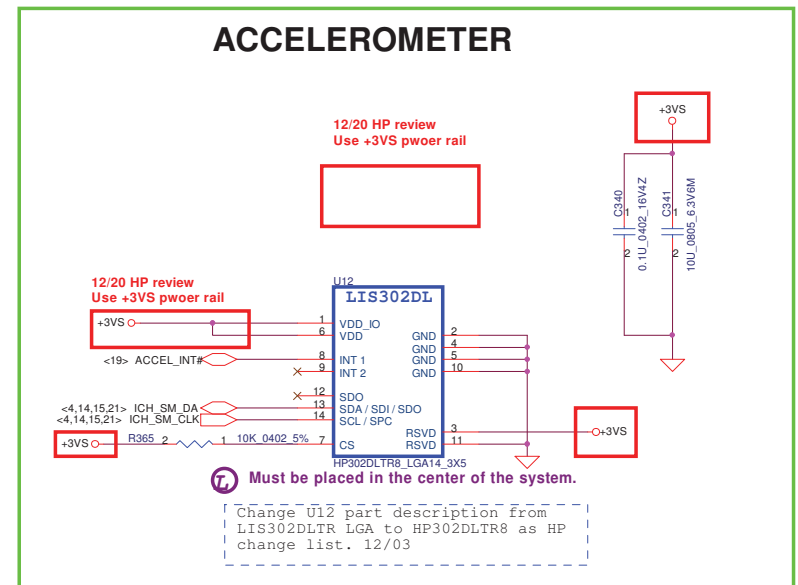


Mini-Express Card--WWAN

Full size



ACCELEROMETER

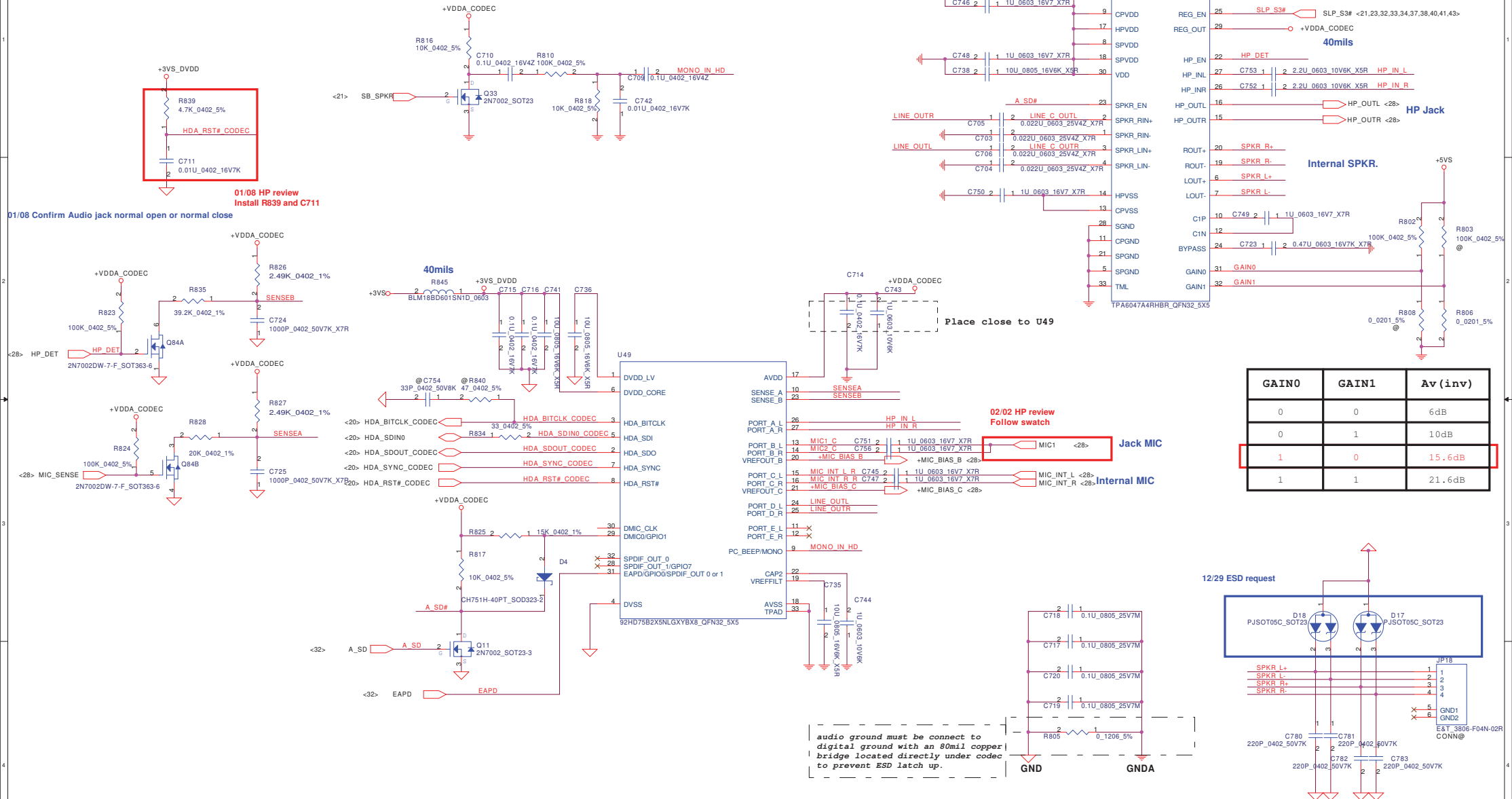


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12/17 Remove to small board

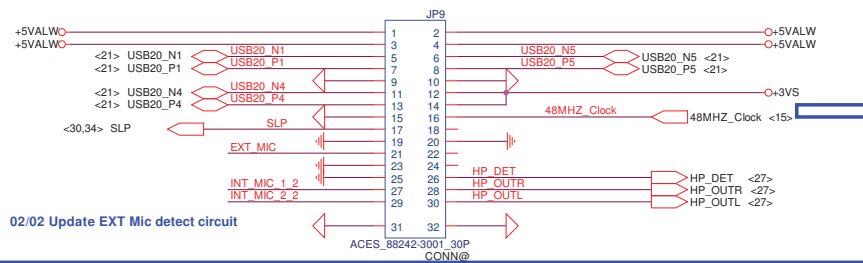
Title			
Card reader board			
Size	Document Number		Rev
	LA-5221P		0.1
Date:	Tuesday, February 03, 2009	Sheet	26 of 45

TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5



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Size	Document Number	Rev			
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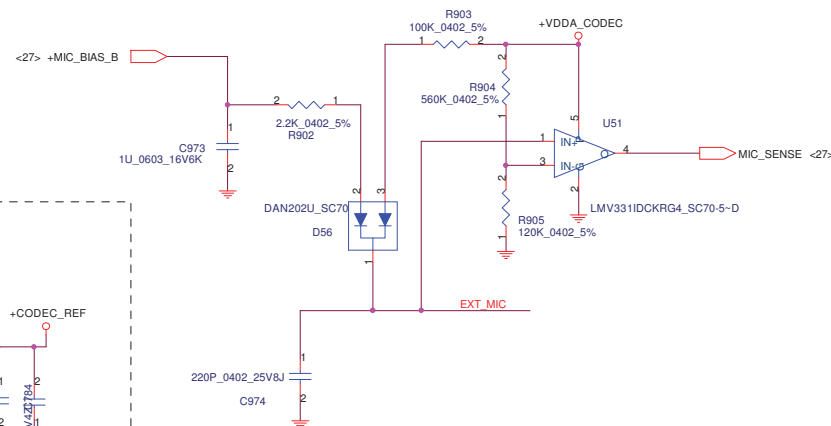
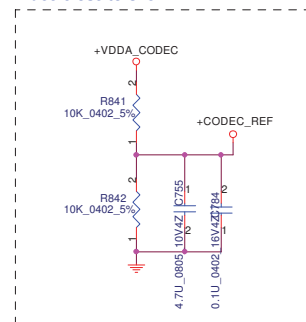
01/10 Fine tune pin define Use the same conn JP9



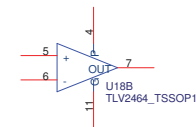
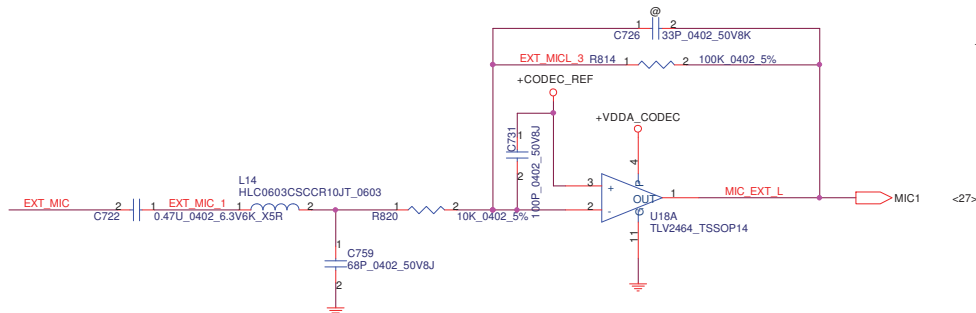
USB I/O connx2 , Aduio JACK
Card reader transfer conn

12/26 Reserved for card reader

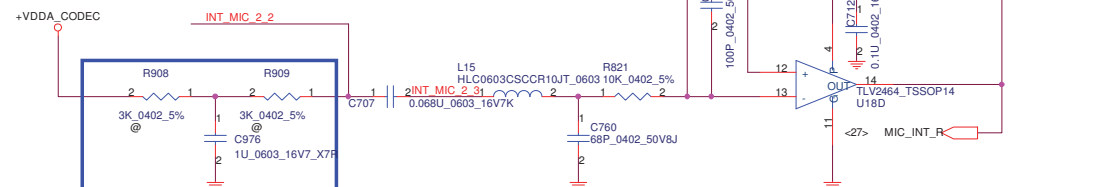
Place close to U18



AMP. FOR EXTERNAL MICROPHONE



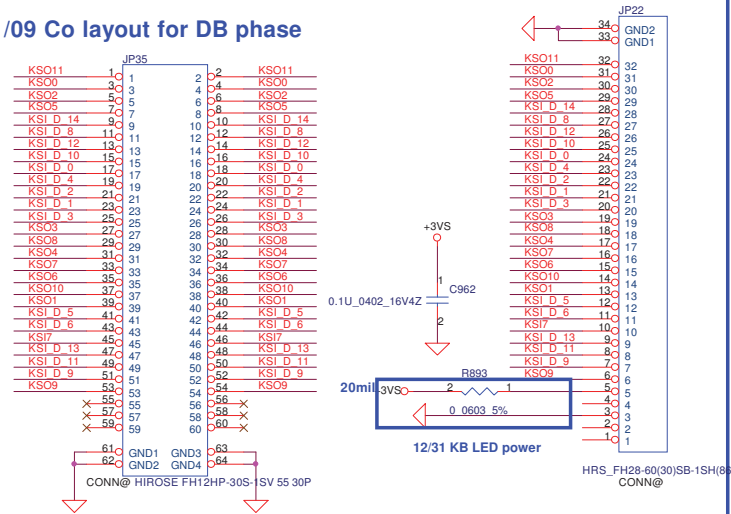
AMP. FOR INTERNAL MICROPHONE



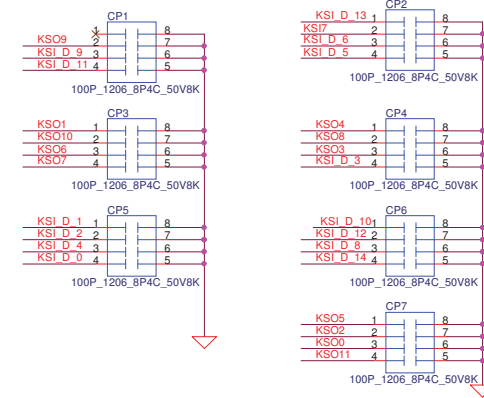
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INT_KBD CONN.

01/09 Co layout for DB phase



<32> KSO[0..11] KSO[0..11]
<32> KSI[0..7] KSI[0..7]

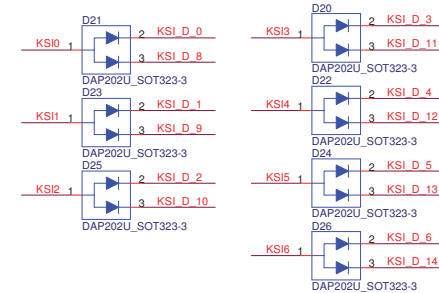


Dior KB up contact

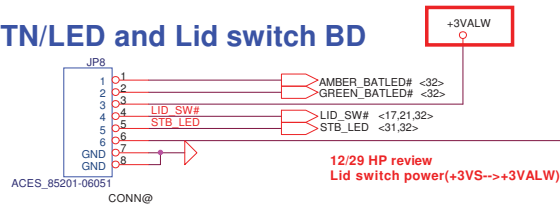


DB use

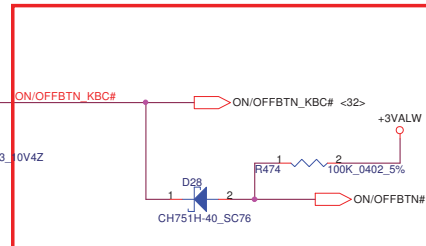
Pin1 reserve , so net name is reserve
for Fossil down contact



Power BTN/LED and Lid switch BD

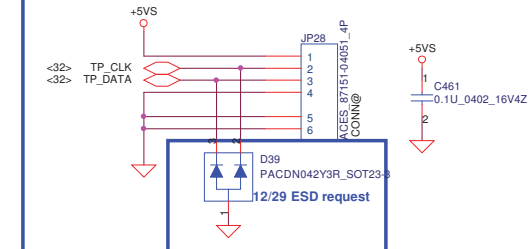


PS:GND use DC in jack GND

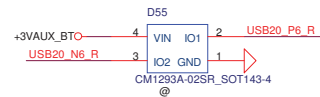


12/20 HP review
Modify ON/OFFBTN# circuit

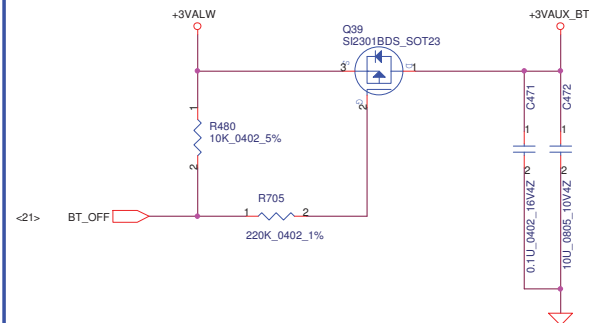
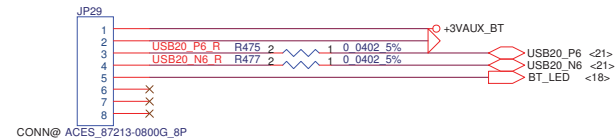
T/P BOARD.



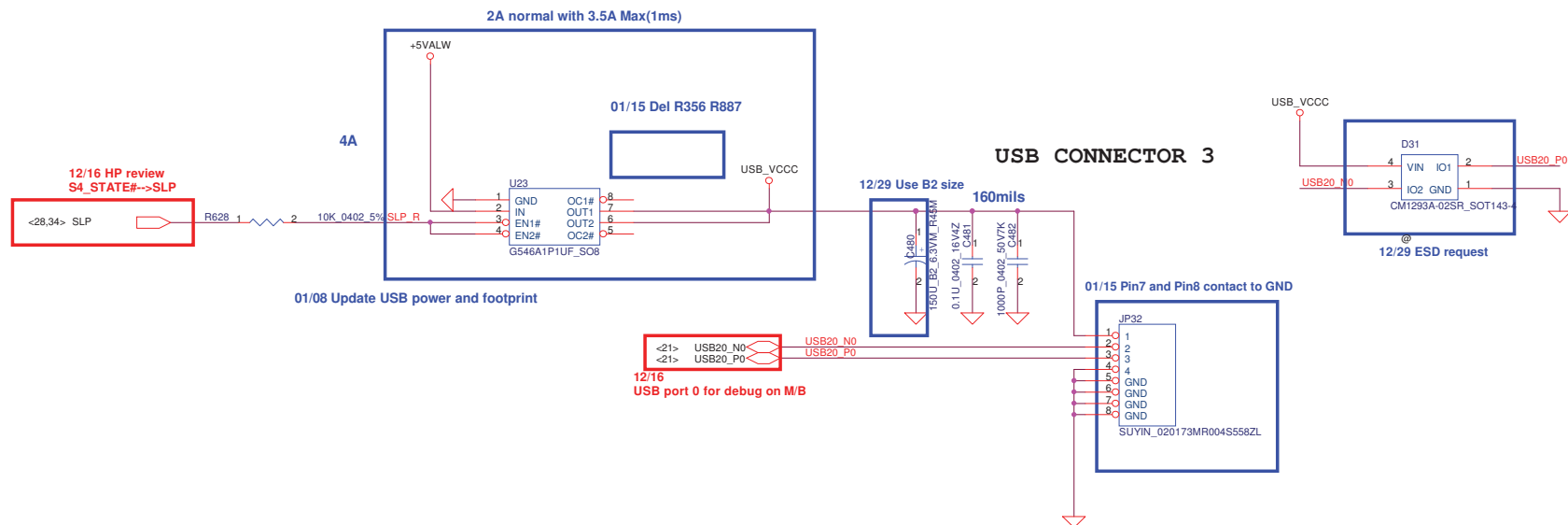
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BT (SoftBreeze) Connector



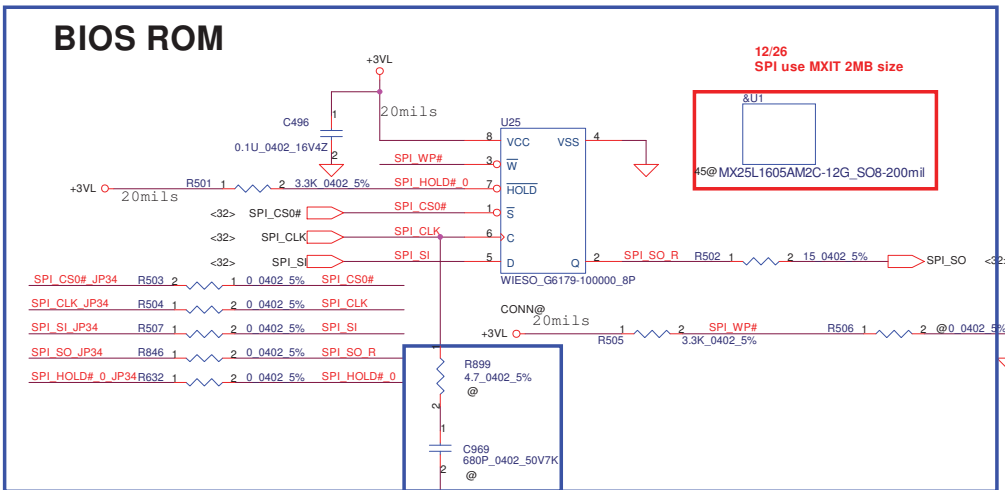
12/16 change to small board



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				LA-5221P	Rev 0.1
				Date	Tuesday, February 03, 2009
				Sheet	30 of 45

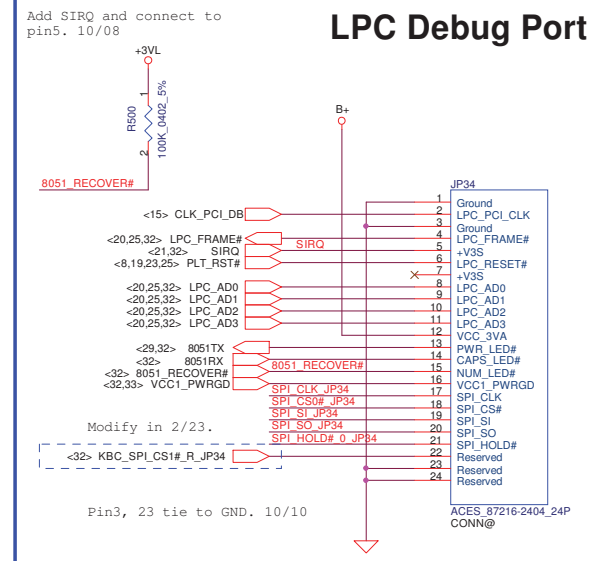
01/23
U25 is conn
&U1 is SPI ROM

BIOS ROM



01/13
Reserved for ESD

LPC Debug Port



Security Classification	Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	TCG/BIOS ROM/PS2/SW LPC DEBUG
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				LA-5221P 0.1
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01/15 HP review
Every +3VL share 0.1u cap for U26

01/14 HP review
Del R722

01/14 HP review
Del R511

01/15 HP review
C504 Y5V-->X5R

12/20 HP review
Del G_BATLED#

12/29 HP review
R523 @-->2.2k

12/20 HP review
Del reserved pull high R

12/20 HP review
Del reserved pull high R

12/20 HP review
Contact to +3VL

12/20 HP review
Contact to GND

12/20 HP review
Contact to GND

12/29 HP review
R543 2.2k-->1.2k

12/29 HP review
Contact Pin 115

12/29 HP review
Del D36

12/20 HP review
LANLINK_STATUS by ICH9

01/06 HP review
Add pull up R

SMSC_1091-NU_TQFP-128P

Keyboard/Mouse Interface

General Purpose I/O Interface

Access Bus Interface

Power Mgmt/SIRQ

Miscellaneous

LPC Bus

01/05 HP review
+3VS-->+3VL

01/15 BIOS review

01/19 SMSC review
Pin 68 +3VL-->RTCVCC

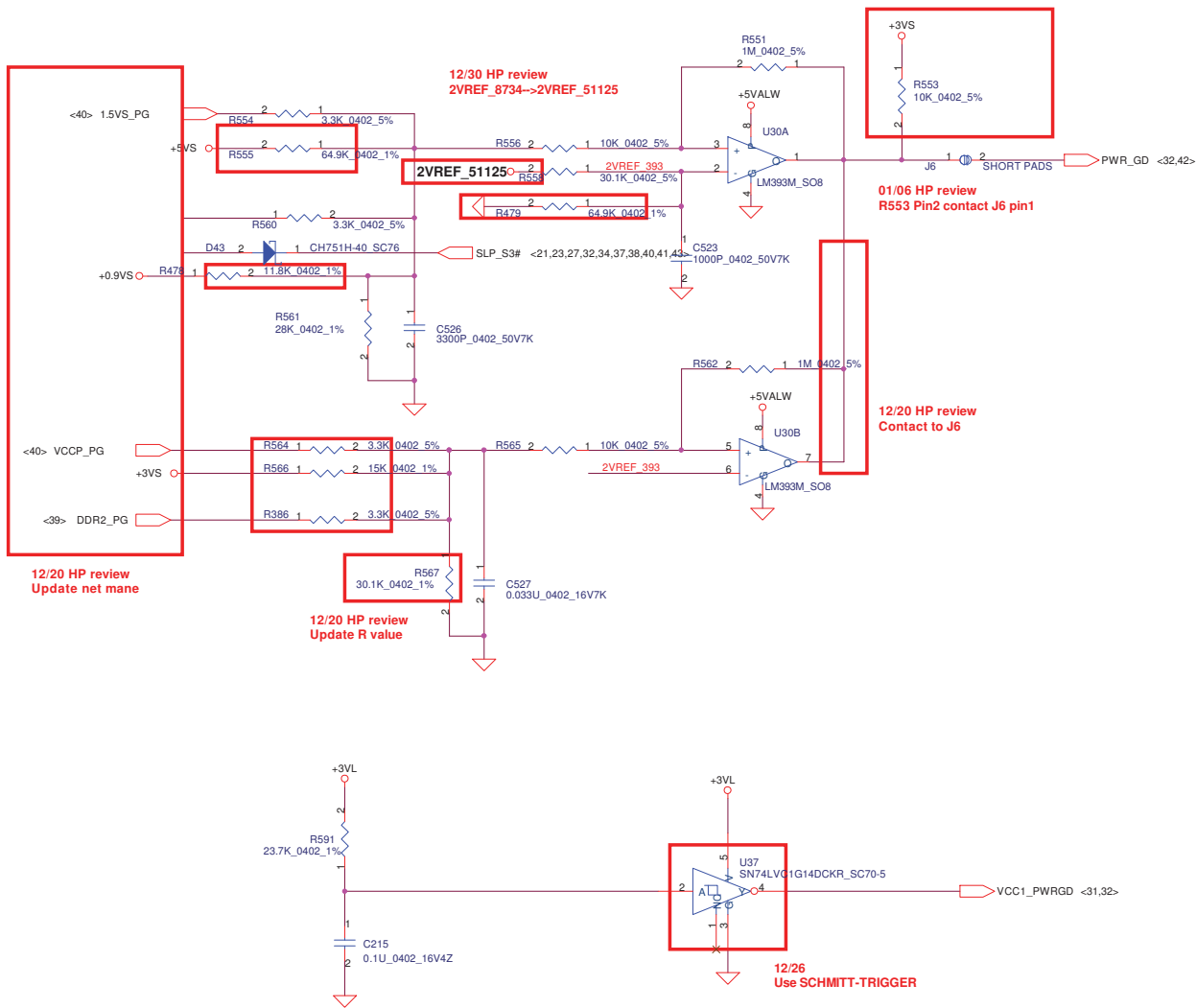
12/20 HP review
+VCC0-->+3VL and Del GPIO40

12/20 HP review
Del GPIO39(WLAN power control)
Del GPIO38(WLAN power control)
Del GPIO37(LAN_WOL_EN to ICH)

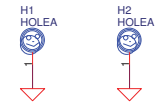
12/20 HP review
Contact DGND

12/20 HP review
No AGND filter

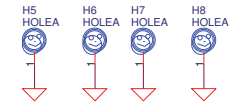
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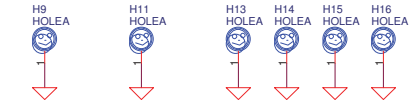
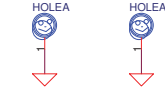
WWAN Card STANDOFF



CPU support



WWLAN Card STANDOFF



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				Document Number LA-522IP	0.1
				Date: Tuesday, February 03, 2009	Sheet 33 of 45

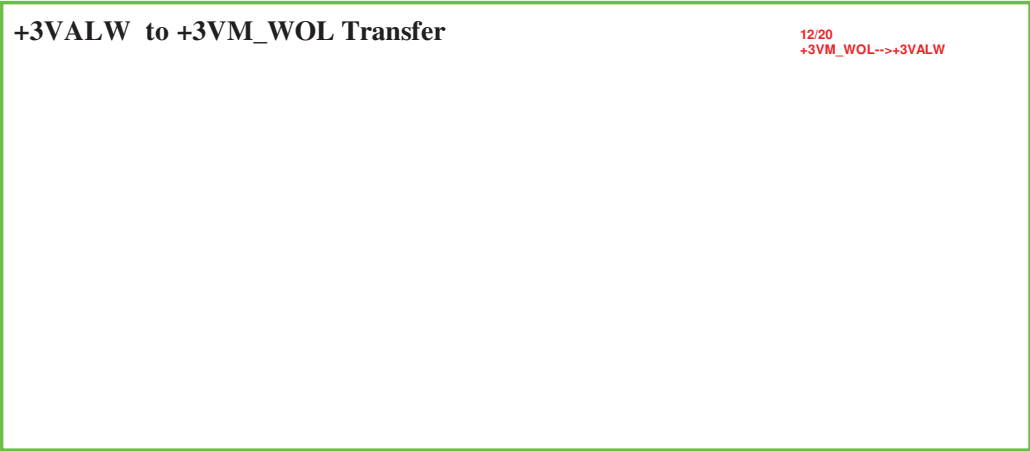
+1.05VM to +VCCP Transfer

12/12
+1.05VN-->+VCCP



+3VALW to +3VM_WOL Transfer

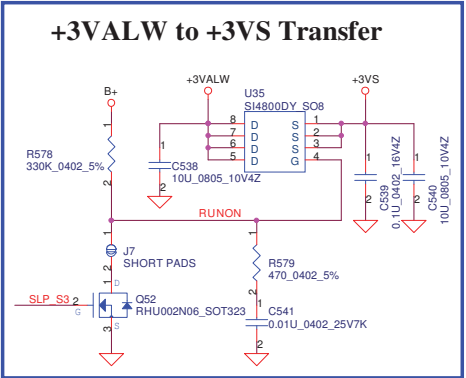
12/20
+3VM_WOL-->+3VALW



12/12 REMOVE

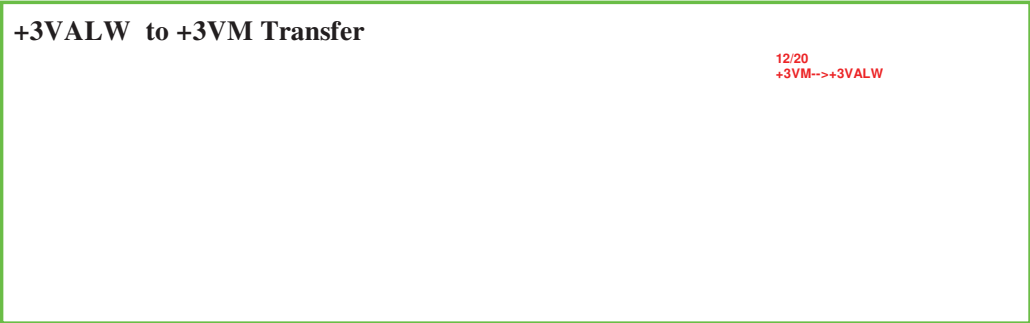


+3VALW to +3VS Transfer

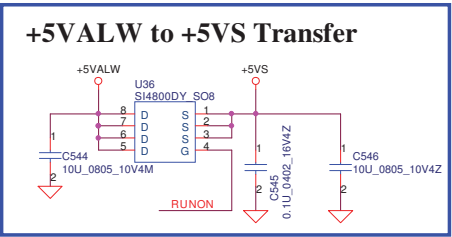


+3VALW to +3VM Transfer

12/20
+3VM-->+3VALW

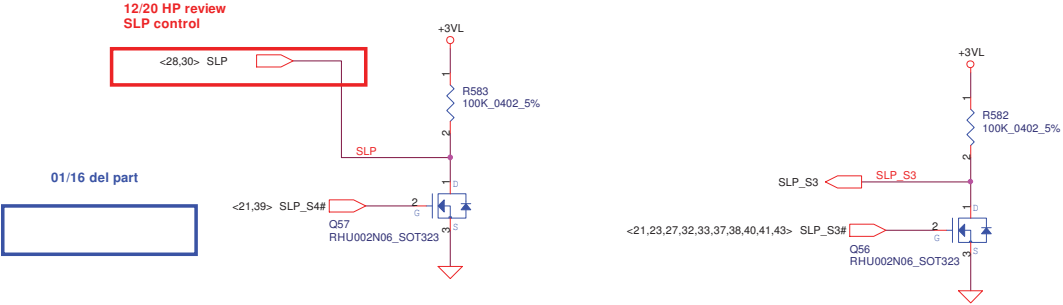


+5VALW to +5VS Transfer

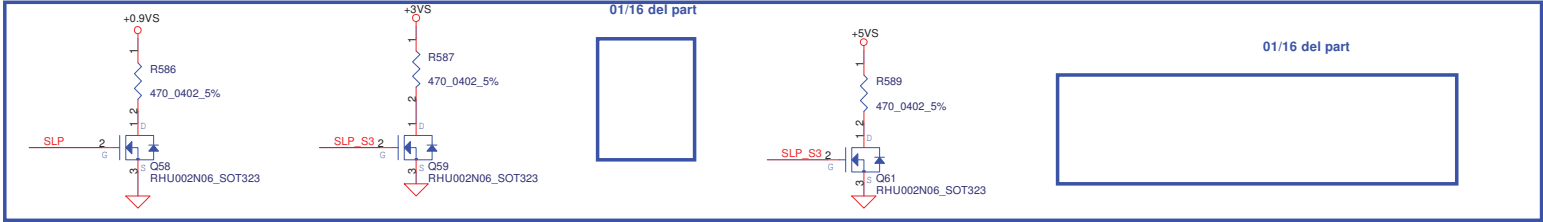


12/20 HP review
SLP control

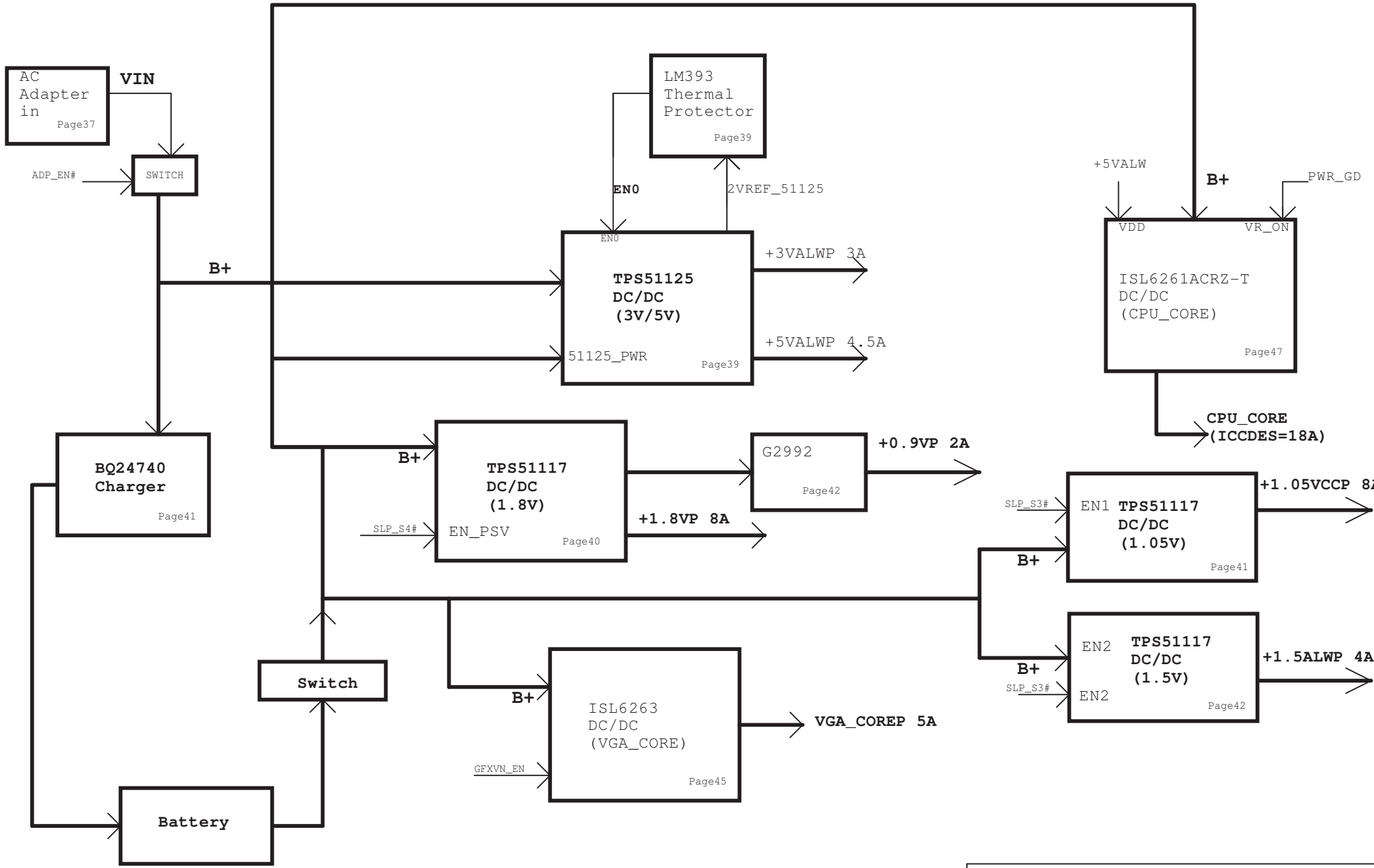
01/16 del part



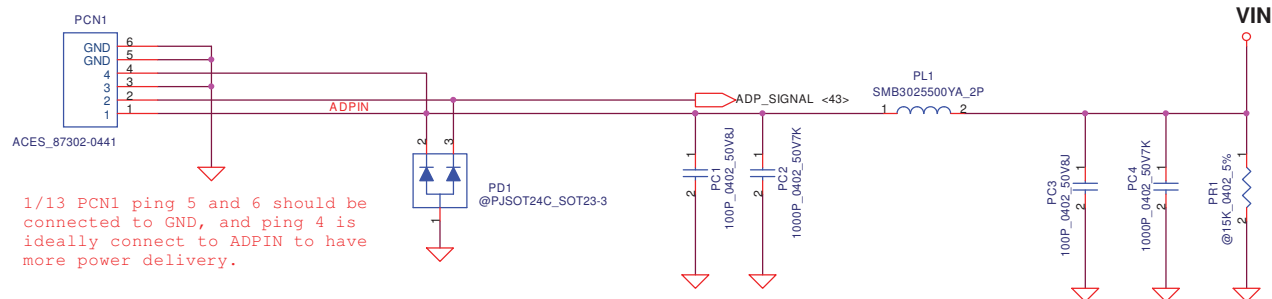
Discharge circuit-1



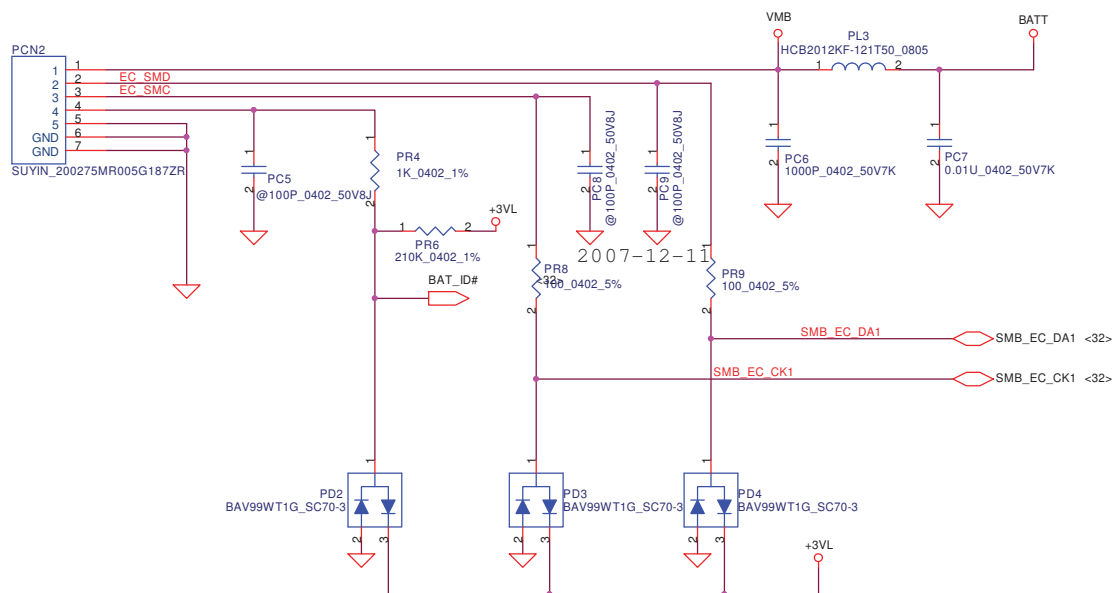
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				Size	Document Number	Rev
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Title		
POWER BLOCK DIAGRAM		
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PH1 under CPU bottom side :
 CPU thermal protection at 90 $\pm$ 3 degree C
 Recovery at 47 $\pm$ 3 degree C

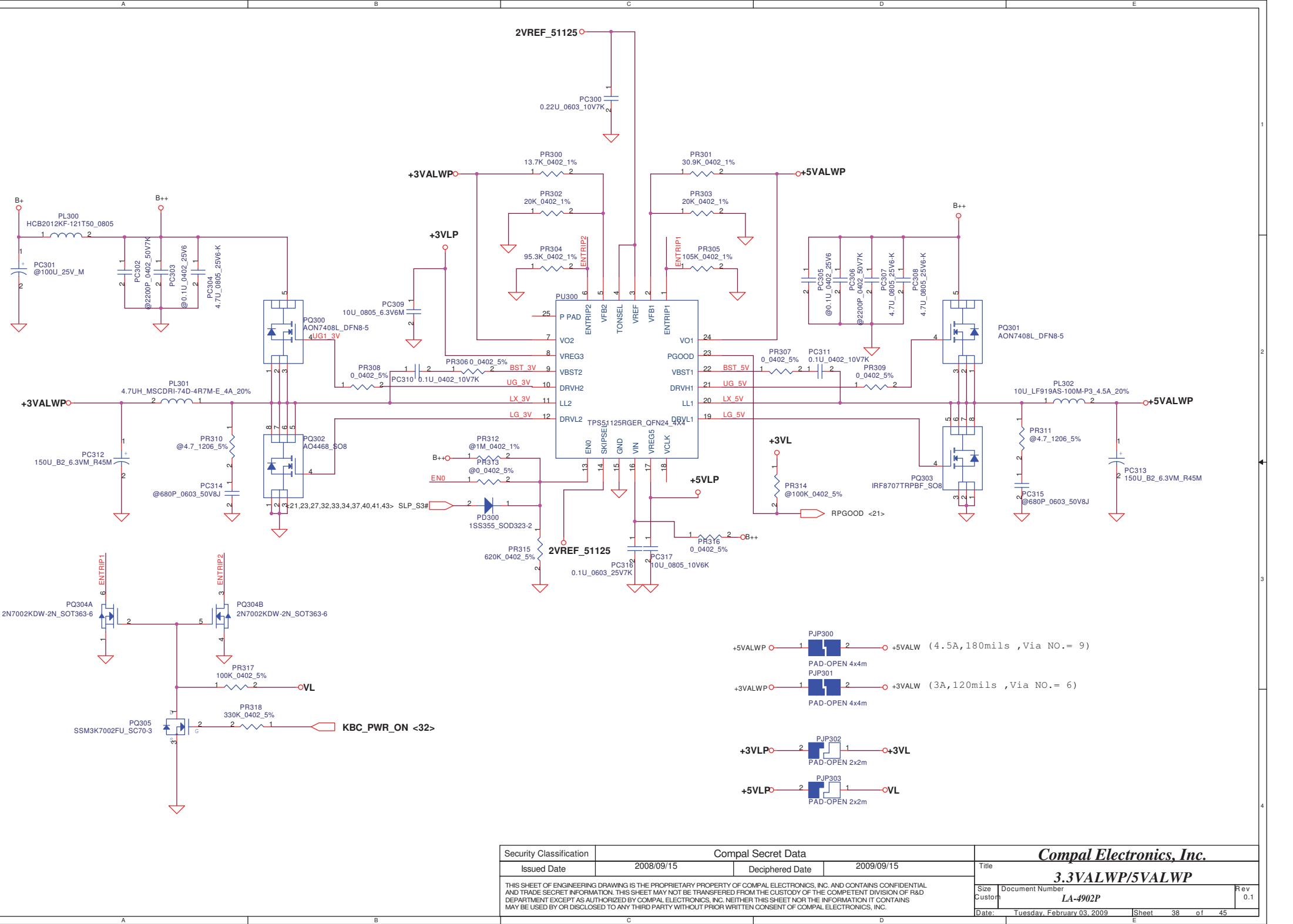


12/26 HP review
 Remove reserved PH1 circuit

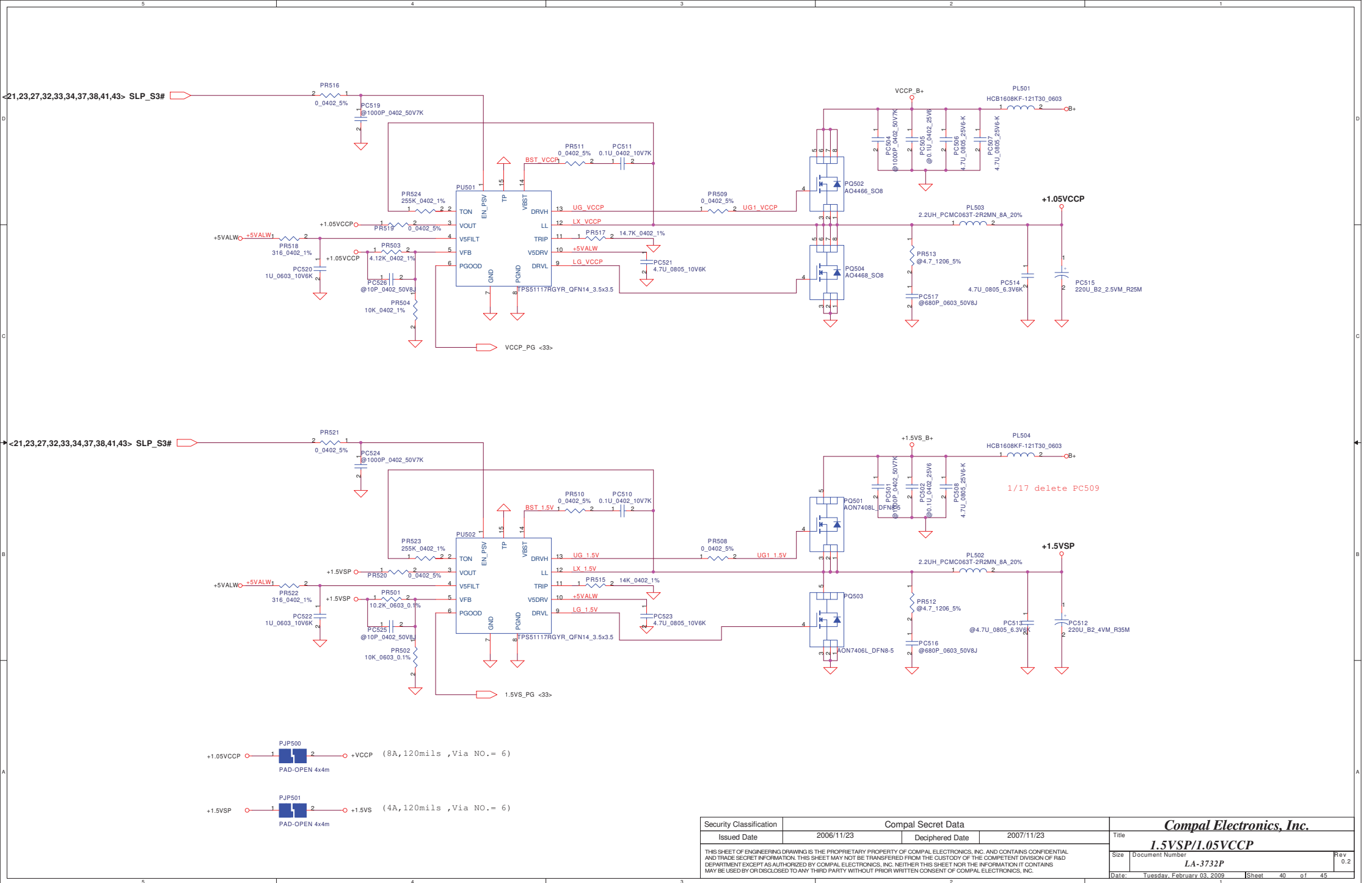
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				Date:	Tuesday, February 03, 2009
				Sheet	36 of 45



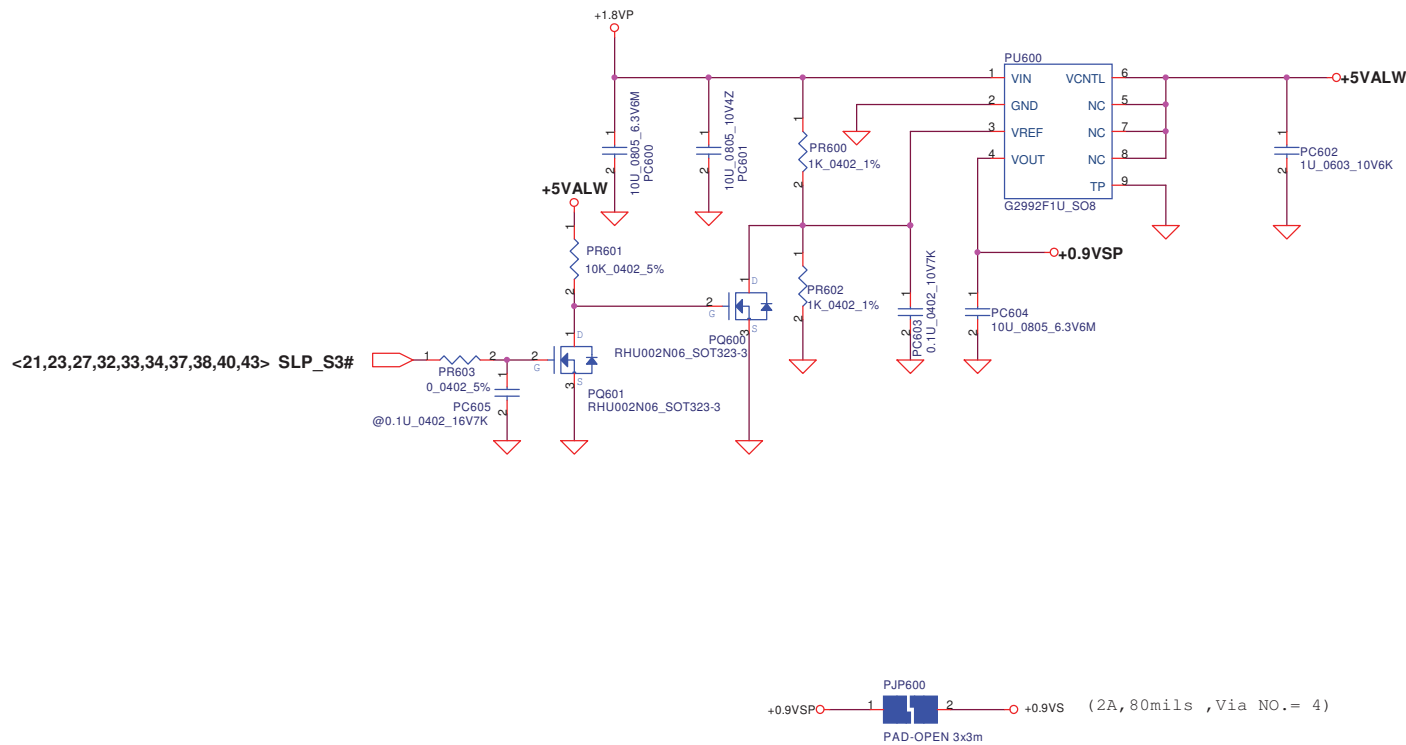
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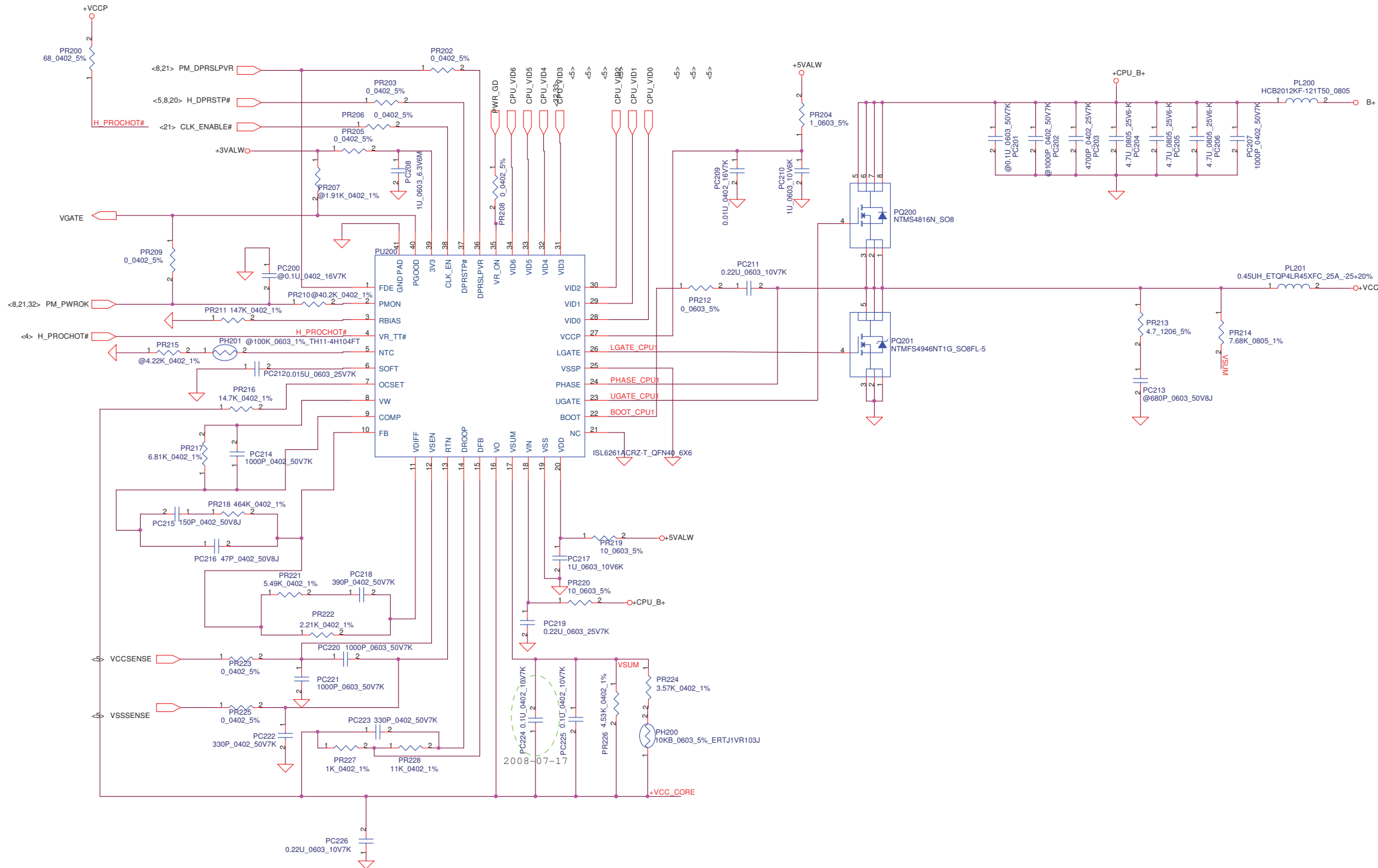
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Size	Custom	Document Number	LA-4902P	Rev	0.1
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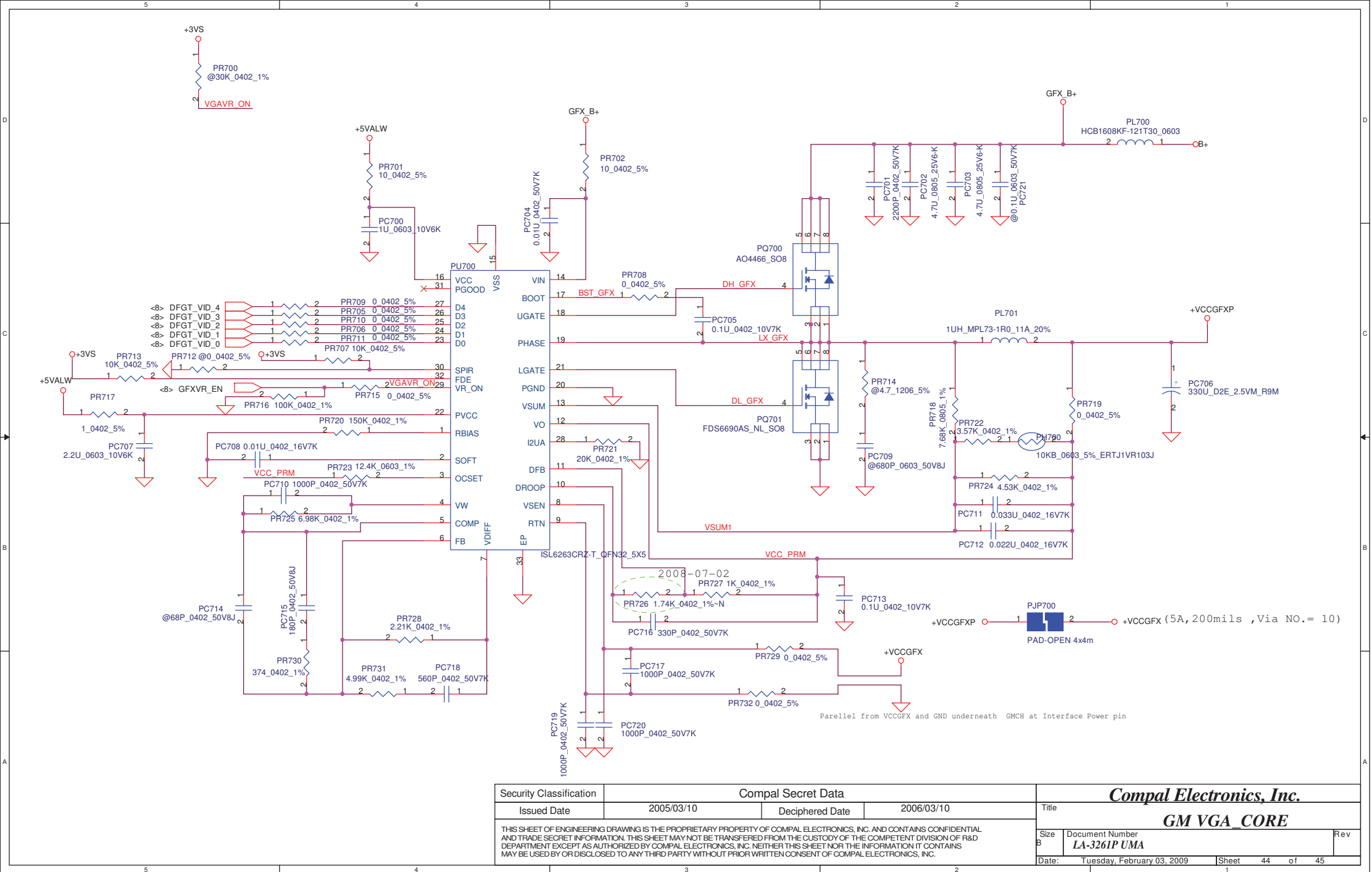
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				Size	Document Number	Rev
				LA-3732P		0.2
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