

COMPAL CONFIDENTIAL

MODEL NAME : JAZ00

PCB NO : LA-4291P

BOM P/N : 46155331L01



MINICOOPER

**uFCBGA Mobile Penryn SFF ULV
Intel Cantiga GS(High Performance) + ICH9M SFF**

12-07-2007

REV : 0.1(X00)

@ : Nopop Component

1@ : TAA board Used only

2@ : Without TAA board Used only

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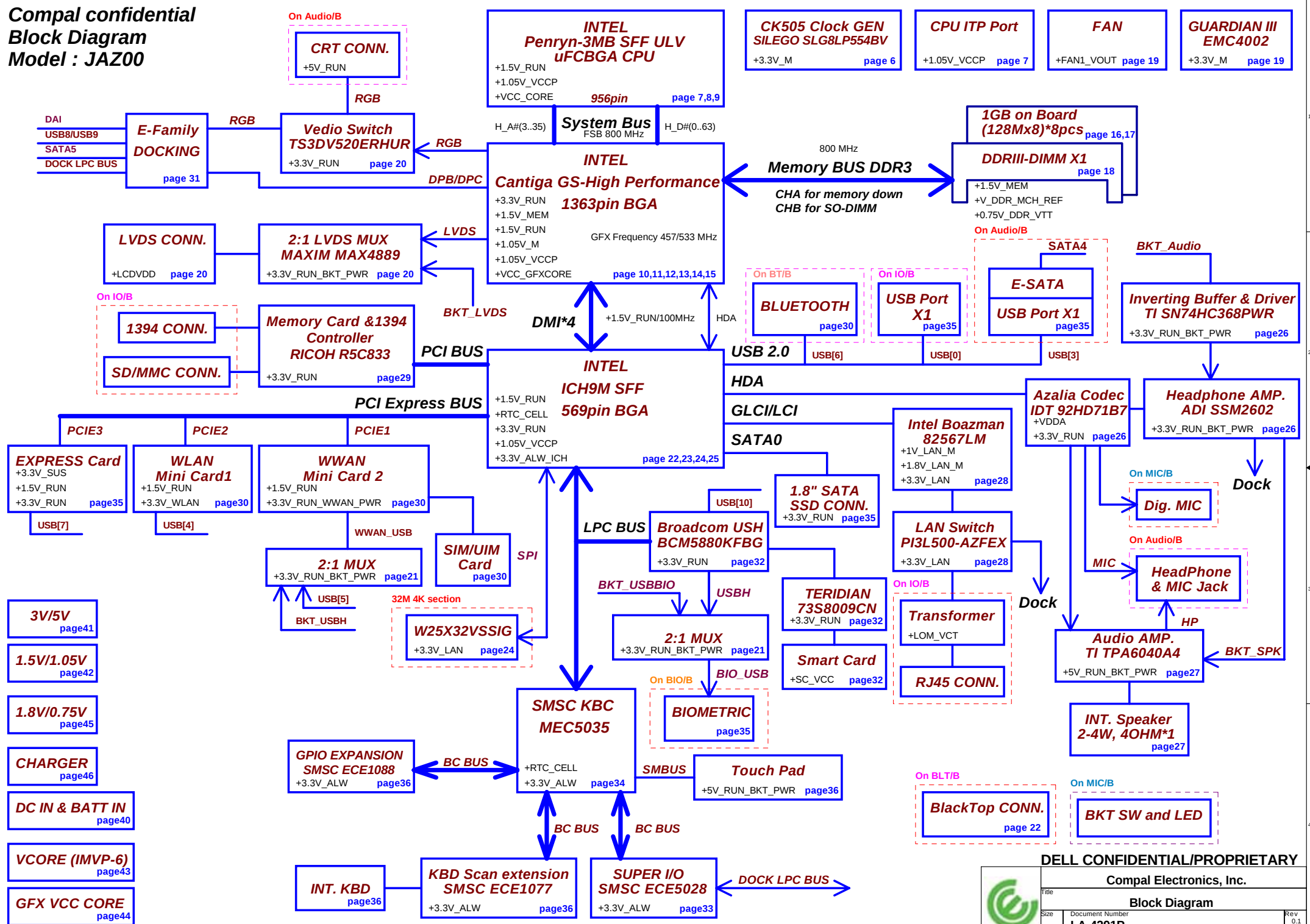
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Title			Rev 0.1
Cover sheet			
Size	Document Number		
	LA-4291P		
Date:	Friday, December 07, 2007	Sheet 1 of 49	

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Block Diagram
Model : JAZ00



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
0	JUSB (Ext Right Side)
1	NONE
2	NONE
3	JESATA (Ext Left Side)
4	WLAN
5	WWAN
6	BT
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	NONE

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO +1.5V_ALW_HDA	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)	+3.3V_RUN_BKT_PWR +5V_RUN_BKT_PWR +3.3V_RUN_WWAN_PWR +INV_PWR_SRC +LCDVDD	+3.3V_BKT_PWR
S0	ON	ON	ON	ON	ON	ON	OFF
S3	ON	ON	OFF	ON	OFF	OFF	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BLT mode	ON	OFF	OFF	OFF	OFF	ON	ON

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-2 WWAN
Lane 2	MINI CARD-1 WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	Giga LAN

PCI TABLE

PCI DEVICE	IDSEL	REQ#/IGNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQ[C..D]

SATA	DESTINATION
SATA0	SSD
SATA1	None
SATA4	ESATA
SATA5	DOCKING

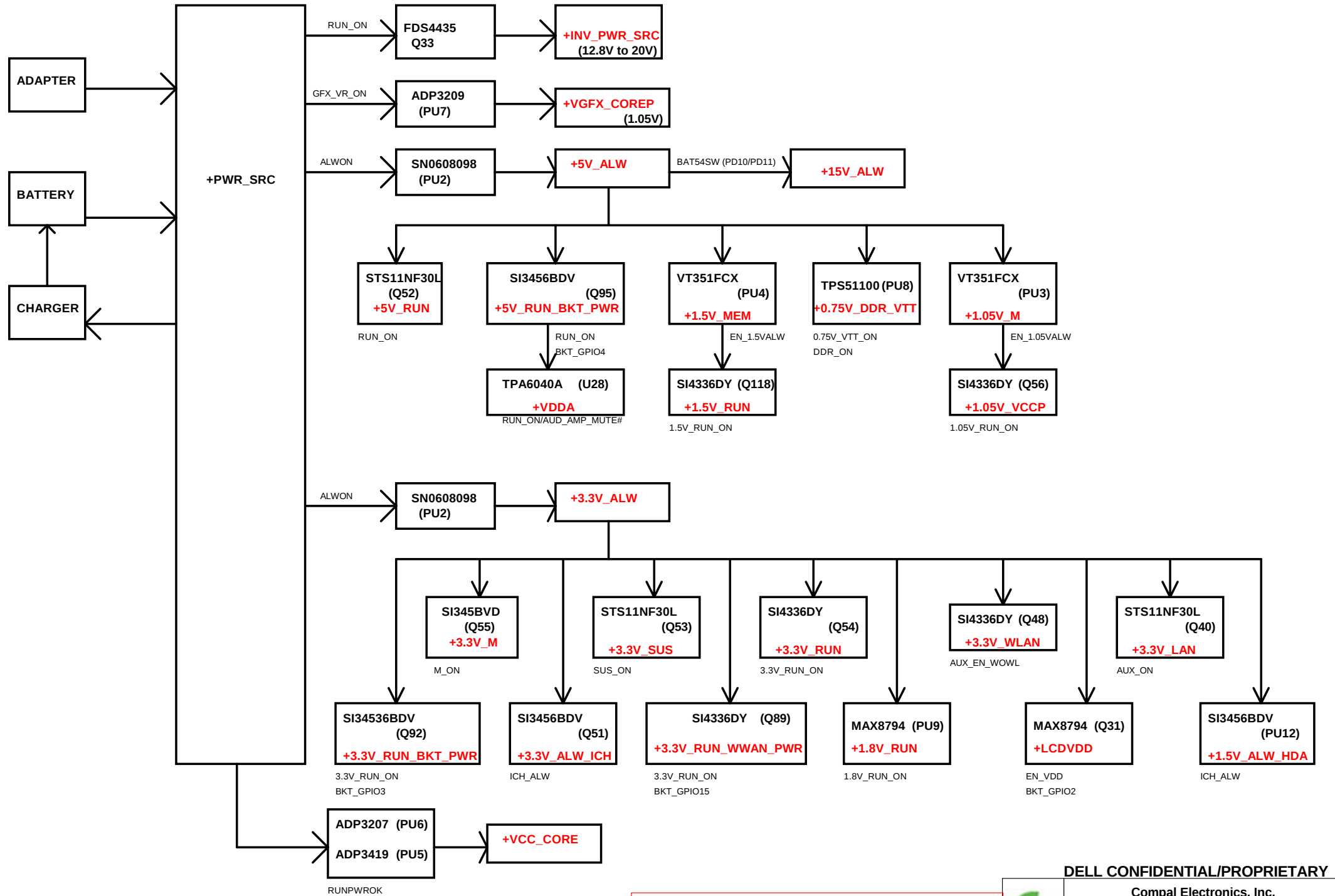
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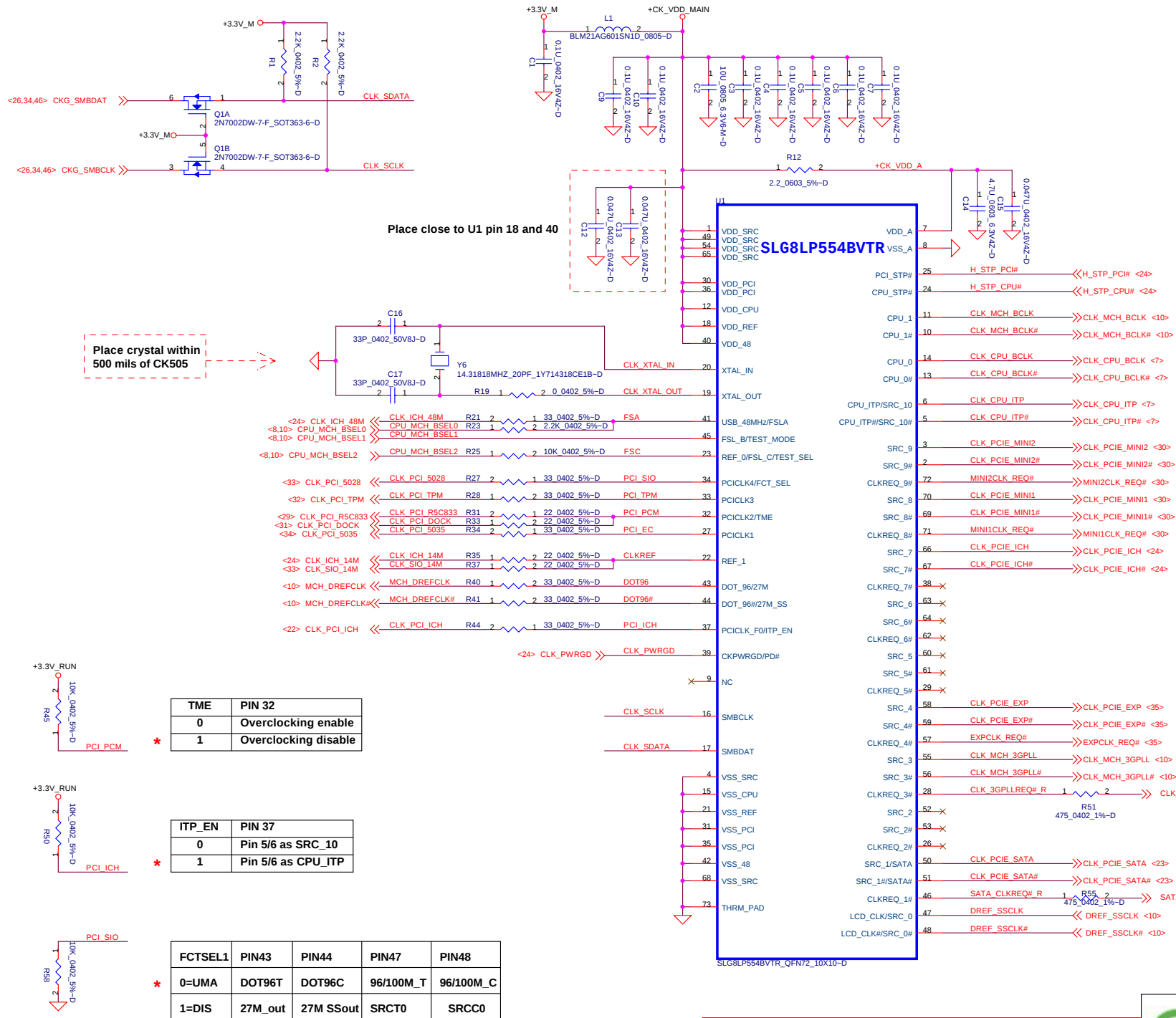
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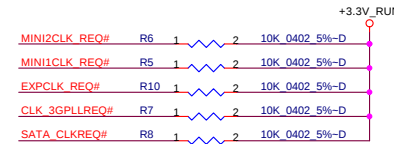




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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

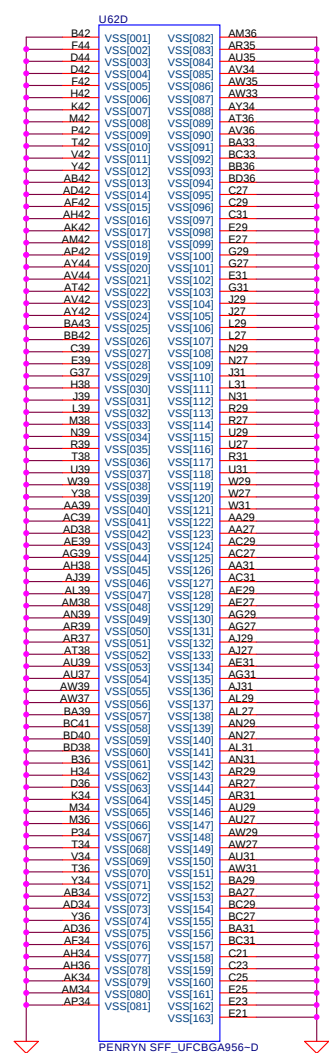


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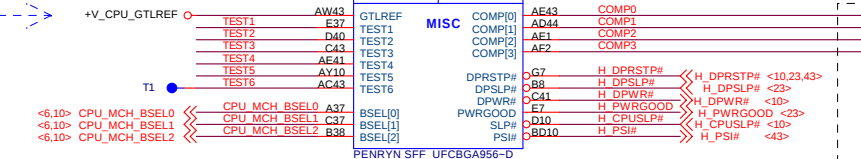
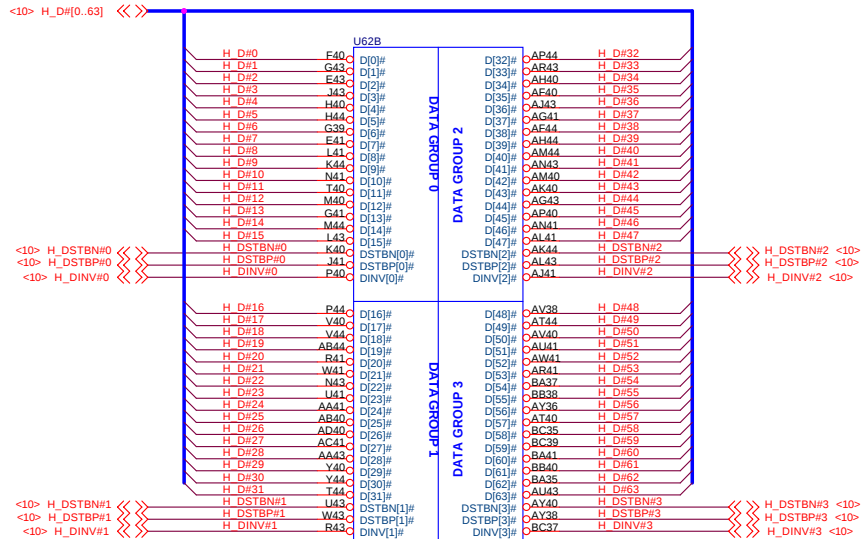


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Title	Clock GEN. with internal terminations
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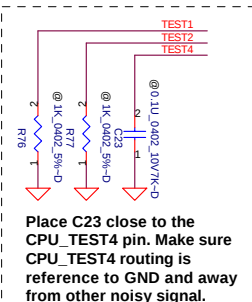
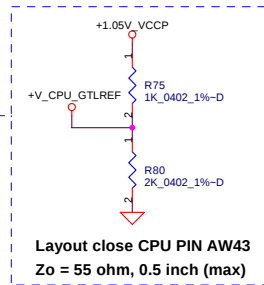


Place close to JITP within 200ps = 1000 mil

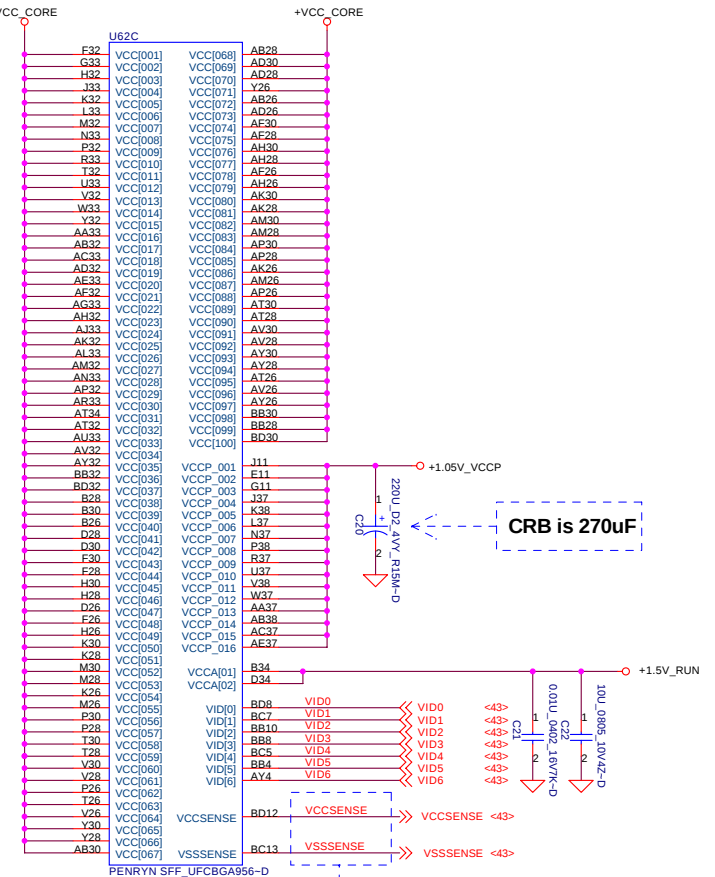


FSB	BCLK	BSEL2	BSEL1	BSEL0
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Route TEST3 and TEST5 signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via.

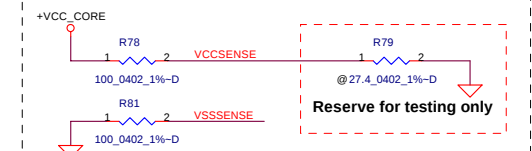


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55ohm.



Length match within 25 mils, Z0=27.4 ohm

Place R78 and R81 close to CPU within 1000 mil



Route VCCSENSE and VSSSENSE trace at 27.4 ohms with 7 mil spacing

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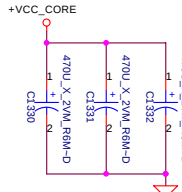
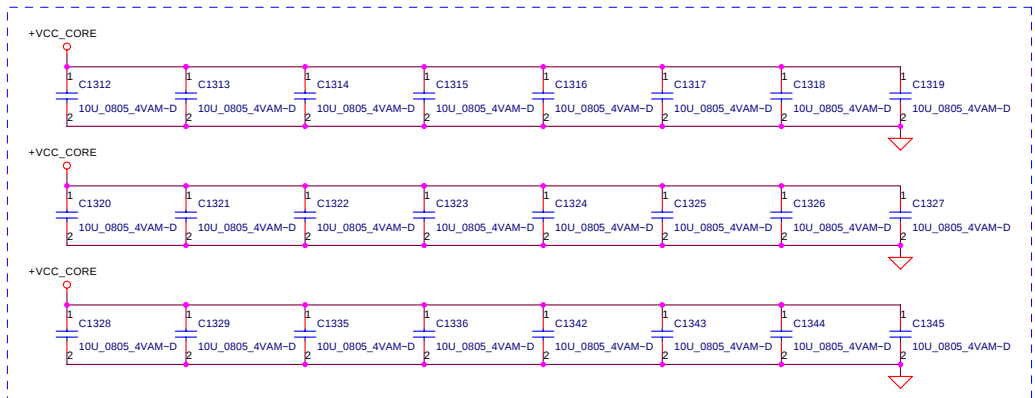
Penryn SFF ULV Processor(2/3)			
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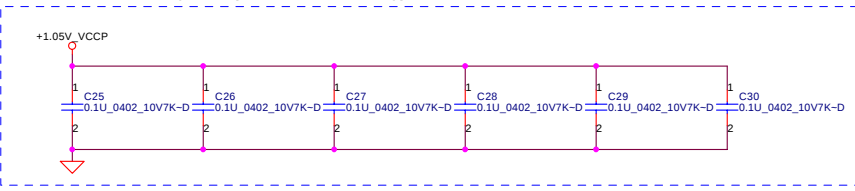
U62F			U62E		
+VCC_CORE	BD28	VCC_101	VCCP_021	AL37	+1.05V_VCCP
BB26	VCC_102	VCCP_022	AN37		
BD26	VCC_103	VCCP_023	AP38		
B22	VCC_104	VCCP_024	C33		
B24	VCC_105	VCCP_025	J25		
D22	VCC_106	VCCP_026	D32		
D24	VCC_107	VCCP_027	E35		
F22	VCC_108	VCCP_028	L23		
H24	VCC_109	VCCP_029	F34		
H22	VCC_110	VCCP_030	G35		
K24	VCC_111	VCCP_031	N23		
K22	VCC_112	VCCP_032	H36		
M24	VCC_113	VCCP_033	J35		
M22	VCC_114	VCCP_034	R23		
U24	VCC_115	VCCP_035	R21		
U22	VCC_116	VCCP_036	K36		
P22	VCC_117	VCCP_037	R35		
T24	VCC_118	VCCP_038	U23		
T22	VCC_119	VCCP_039	U21		
V24	VCC_120	VCCP_040	W23		
V22	VCC_121	VCCP_041	W35		
Y24	VCC_122	VCCP_042	AA25		
Y22	VCC_123	VCCP_043	AA23		
AB24	VCC_124	VCCP_044	AB36		
AB22	VCC_125	VCCP_045	AC25		
AD24	VCC_126	VCCP_046	AC23		
AD22	VCC_127	VCCP_047	AG35		
AE24	VCC_128	VCCP_048	AJ35		
AE22	VCC_129	VCCP_049	AE35		
AH24	VCC_130	VCCP_050	AE23		
AH22	VCC_131	VCCP_051	AG25		
AK24	VCC_132	VCCP_052	AG26		
AK22	VCC_133	VCCP_053	B12		
AM24	VCC_134	VCCP_054	B14		
AM22	VCC_135	VCCP_055	C13		
AP24	VCC_136	VCCP_056	AJ21		
AP22	VCC_137	VCCP_057	AL25		
AT24	VCC_138	VCCP_058	AL23		
AT22	VCC_139	VCCP_059	AL21		
AV24	VCC_140	VCCP_060	AN25		
AV22	VCC_141	VCCP_061	AN23		
AY24	VCC_142	VCCP_062	AN21		
AY22	VCC_143	VCCP_063	AR25		
BB24	VCC_144	VCCP_064	AR23		
BB22	VCC_145	VCCP_065	AR21		
BD24	VCC_146	VCCP_066	AU25		
BD22	VCC_147	VCCP_067	AU23		
B18	VCC_148	VCCP_068	AU21		
B20	VCC_149	VCCP_069	AW25		
D16	VCC_150	VCCP_070	AW23		
D18	VCC_151	VCCP_071	AW21		
F18	VCC_152	VCCP_072	BA25		
F16	VCC_153	VCCP_073	BA23		
H16	VCC_154	VCCP_074	BA21		
H18	VCC_155	VCCP_075	BC25		
D20	VCC_156	VCCP_076	BC23		
F20	VCC_157	VCCP_077	BC21		
H20	VCC_158	VCCP_078	C17		
K18	VCC_159	VCCP_079	C19		
K16	VCC_160	VCCP_080	E19		
M18	VCC_161	VCCP_081	E17		
M16	VCC_162	VCCP_082	G19		
P18	VCC_163	VCCP_083	G17		
P16	VCC_164	VCCP_084	G19		
T18	VCC_165	VCCP_085	H19		
T16	VCC_166	VCCP_086	I17		
V18	VCC_167	VCCP_087	I19		
V16	VCC_168	VCCP_088	L19		
T20	VCC_169	VCCP_089	L17		
V20	VCC_170	VCCP_090	N19		
Y18	VCC_171	VCCP_091	N17		
Y16	VCC_172	VCCP_092	R19		
AB18	VCC_173	VCCP_093	R17		
AB16	VCC_174	VCCP_094	U19		
AD18	VCC_175	VCCP_095	U17		
AD16	VCC_176	VCCP_096	W19		
AE18	VCC_177	VCCP_097	W17		
AH18	VCC_178	VCCP_098	Y19		
AH16	VCC_179	VCCP_099	Y17		
AK18	VCC_180	VCCP_100	AA19		
AK16	VCC_181	VCCP_101	AA17		
AM18	VCC_182	VCCP_102	AE19		
AM16	VCC_183	VCCP_103	AE17		
AP18	VCC_184	VCCP_104	AG19		
AP16	VCC_185	VCCP_105	AG17		
AK20	VCC_186	VCCP_106	AJ19		
AM20	VCC_187	VCCP_107	AJ17		
AP20	VCC_188	VCCP_108	AL19		
AT18	VCC_189	VCCP_109	AL17		
AT16	VCC_190	VCCP_110	AN19		
AV18	VCC_191	VCCP_111	AN17		
AV16	VCC_192	VCCP_112	AR19		
AY18	VCC_193	VCCP_113	AR17		
AY16	VCC_194	VCCP_114	AW19		
BB18	VCC_195	VCCP_115	AW17		
BB16	VCC_196	VCCP_116	BA19		
BD18	VCC_197	VCCP_117	BA17		
BD16	VCC_198	VCCP_118	BC19		
BD20	VCC_199	VCCP_119	BC17		
BD22	VCC_200	VCCP_120	C11		
BD24	VCC_201	VCCP_121	N7		
	VCC_202	VCCP_122	E15		
	VCC_203	VCCP_123	G15		
	VCC_204	VCCP_124	H10		
	VCC_205	VCCP_125	I15		
	VCC_206	VCCP_126	L15		
	VCC_207	VCCP_127	M10		
	VCC_208	VCCP_128	T12		
	VCC_209	VCCP_129	U15		
	VCC_210	VCCP_130	R15		
	VCC_211	VCCP_131	U15		
	VCC_212	VCCP_132	W15		
	VCC_213	VCCP_133	T10		
	VCC_214	VCCP_134	Y12		
	VCC_215	VCCP_135	AD12		
	VCC_216	VCCP_136			
	VCC_217	VCCP_137			
	VCC_218	VCCP_138			
	VCC_219	VCCP_139			
	VCC_220	VCCP_140			
		VCCP_141			
		VCCP_142			
		VCCP_143			
		VCCP_144			
		VCCP_145			

PENRYN SFF_UFCBGA956-D

+1.05V_VCCP



Place these inside cavity on L8(North side Secondary)

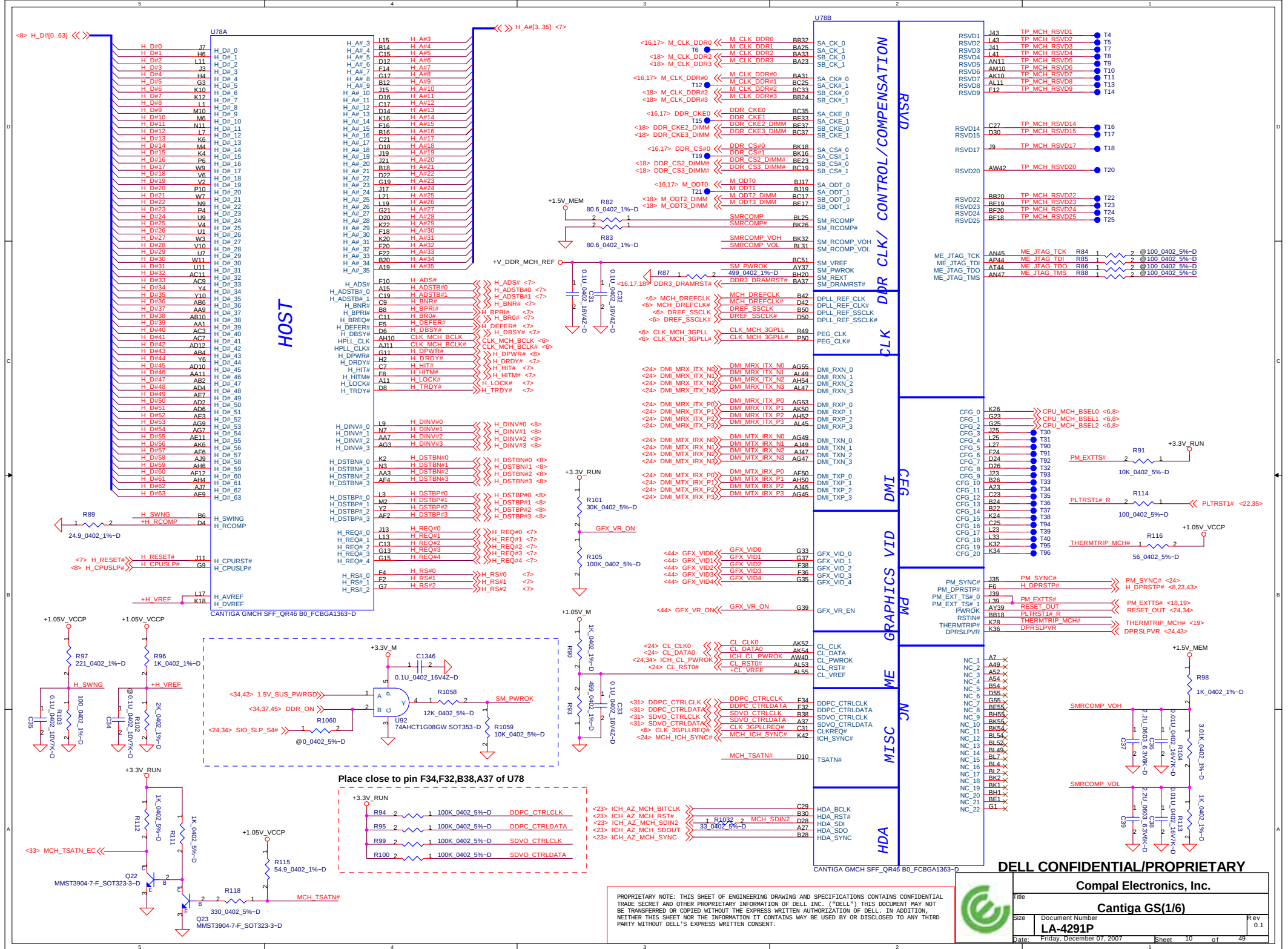


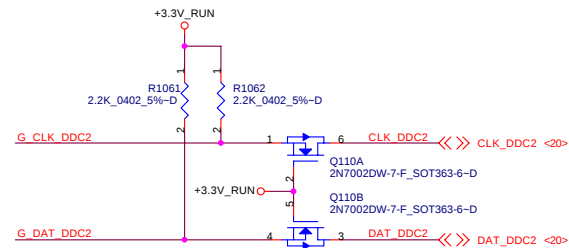
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CFG[5:16] have internal pullup CFG[19:20] have internal pulldown

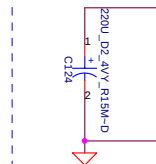
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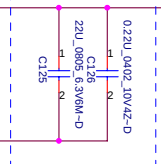
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Layout Note:
Place close to U78

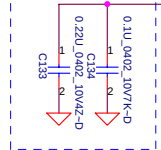
Layout Note:
Inside GMCH cavity



CRB 270uF



C125



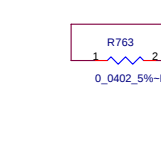
C125



C125



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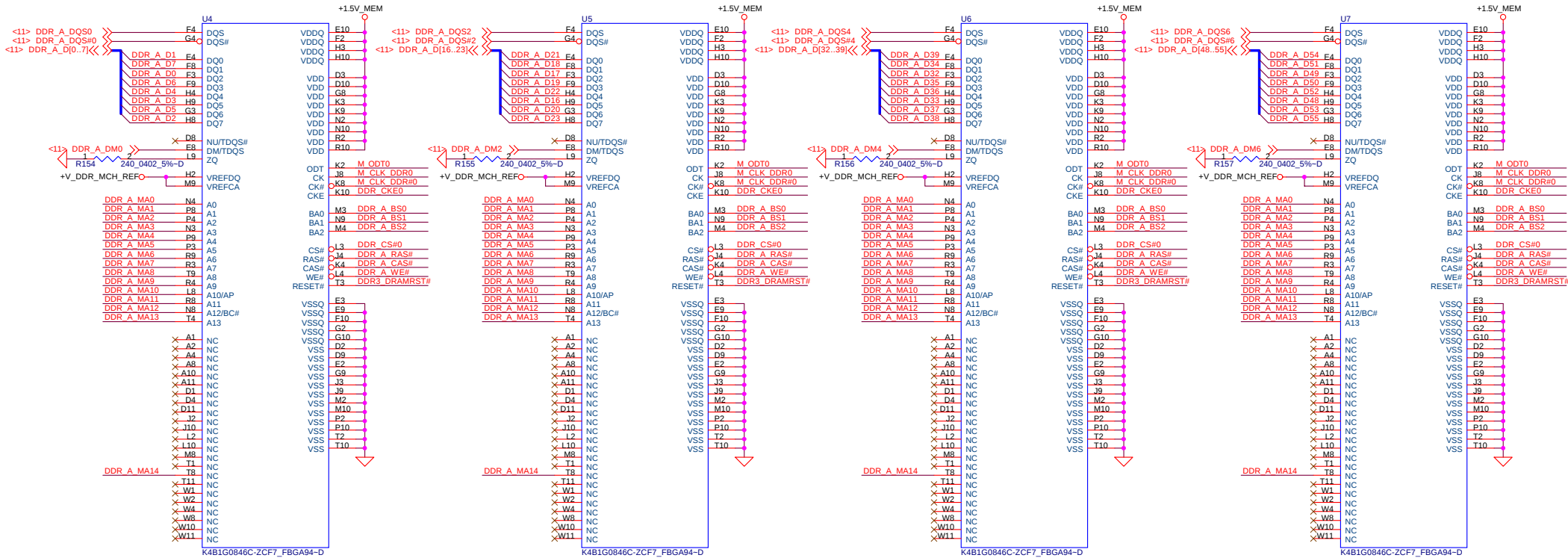
U78I

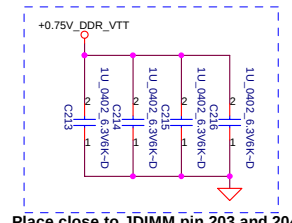
BA55	VSS_1	VSS_100	C43
AU55	VSS_2	VSS_101	A43
AN55	VSS_3	VSS_102	BD42
AJ55	VSS_4	VSS_103	H42
AE55	VSS_5	VSS_104	BG41
AA55	VSS_6	VSS_105	AY41
IJ55	VSS_7	VSS_106	AU41
BD54	VSS_8	VSS_107	AM41
BG53	VSS_9	VSS_108	AU41
AJ53	VSS_10	VSS_109	AG41
AE53	VSS_11	VSS_110	AE41
AA53	VSS_12	VSS_111	AA41
IJ53	VSS_13	VSS_112	R41
N53	VSS_14	VSS_113	M41
J53	VSS_15	VSS_114	E41
G53	VSS_16	VSS_115	BD40
E53	VSS_17	VSS_116	AU40
K52	VSS_18	VSS_117	AR40
BG51	VSS_19	VSS_118	AN40
AW51	VSS_20	VSS_119	W40
AU51	VSS_21	VSS_120	U40
AR51	VSS_22	VSS_121	T40
AN51	VSS_23	VSS_122	R40
AI51	VSS_24	VSS_123	K40
AJ51	VSS_25	VSS_124	H40
AG51	VSS_26	VSS_125	BL39
AE51	VSS_27	VSS_126	BG39
AA51	VSS_28	VSS_127	BA39
IJ51	VSS_29	VSS_128	E39
BD50	VSS_30	VSS_129	C39
BG49	VSS_31	VSS_130	A39
AJ49	VSS_32	VSS_131	BD38
AE49	VSS_33	VSS_132	AU38
AA49	VSS_34	VSS_133	H38
IJ49	VSS_35	VSS_134	BG37
N49	VSS_36	VSS_135	AU37
J49	VSS_37	VSS_136	M37
G49	VSS_38	VSS_137	E37
E49	VSS_39	VSS_138	BD36
K48	VSS_40	VSS_139	AW36
BG47	VSS_41	VSS_140	H36
AW47	VSS_42	VSS_141	BL35
AU47	VSS_43	VSS_142	BG35
AR47	VSS_44	VSS_143	AY35
AN47	VSS_45	VSS_144	AU35
AI47	VSS_46	VSS_145	AL35
AJ47	VSS_47	VSS_146	AG35
AG47	VSS_48	VSS_147	AE35
AE47	VSS_49	VSS_148	AA35
AA47	VSS_50	VSS_149	Y35
IJ47	VSS_51	VSS_150	M35
BD46	VSS_52	VSS_151	E35
BG45	VSS_53	VSS_152	A35
AJ45	VSS_54	VSS_153	BD34
AE45	VSS_55	VSS_154	AU34
AA45	VSS_56	VSS_155	AN34
IJ45	VSS_57	VSS_156	H34
N45	VSS_58	VSS_157	BL33
J45	VSS_59	VSS_158	BG33
G45	VSS_60	VSS_159	AY33
E45	VSS_61	VSS_160	E33
K44	VSS_62	VSS_161	BD32
BG43	VSS_63	VSS_162	AU32
AW43	VSS_64	VSS_163	AN32
AU43	VSS_65	VSS_164	AG32
AR43	VSS_66	VSS_165	AC32
AN43	VSS_67	VSS_166	Y32
AI43	VSS_68	VSS_167	H32
AJ43	VSS_69	VSS_168	B32
AG43	VSS_70	VSS_169	BL31
AE43	VSS_71	VSS_170	BG31
AA43	VSS_72	VSS_171	AY31
IJ43	VSS_73	VSS_172	U31
N43	VSS_74	VSS_173	M31
J43	VSS_75	VSS_174	E31
G43	VSS_76	VSS_175	N30
E43	VSS_77	VSS_176	H30
K42	VSS_78	VSS_177	AN29
BG41	VSS_79	VSS_178	AJ29
AW41	VSS_80	VSS_179	M29
AU41	VSS_81	VSS_180	AR29
AR41	VSS_82	VSS_181	AW28
AN41	VSS_83	VSS_182	AN28
AI41	VSS_84	VSS_183	AD28
AJ41	VSS_85	VSS_184	AC28
AG41	VSS_86	VSS_185	Y28
AE41	VSS_87	VSS_186	W28
AA41	VSS_88	VSS_187	H28
IJ41	VSS_89	VSS_188	F28
BD40	VSS_90	VSS_189	AN27
BG39	VSS_91	VSS_190	AJ27
AJ39	VSS_92	VSS_191	M27
AE39	VSS_93	VSS_192	BE26
AA39	VSS_94	VSS_193	BD26
IJ39	VSS_95	VSS_194	N26
N39	VSS_96	VSS_195	H26
J39	VSS_97	VSS_196	BJ25
G39	VSS_98	VSS_197	AY25
E39	VSS_99	VSS_198	AU25

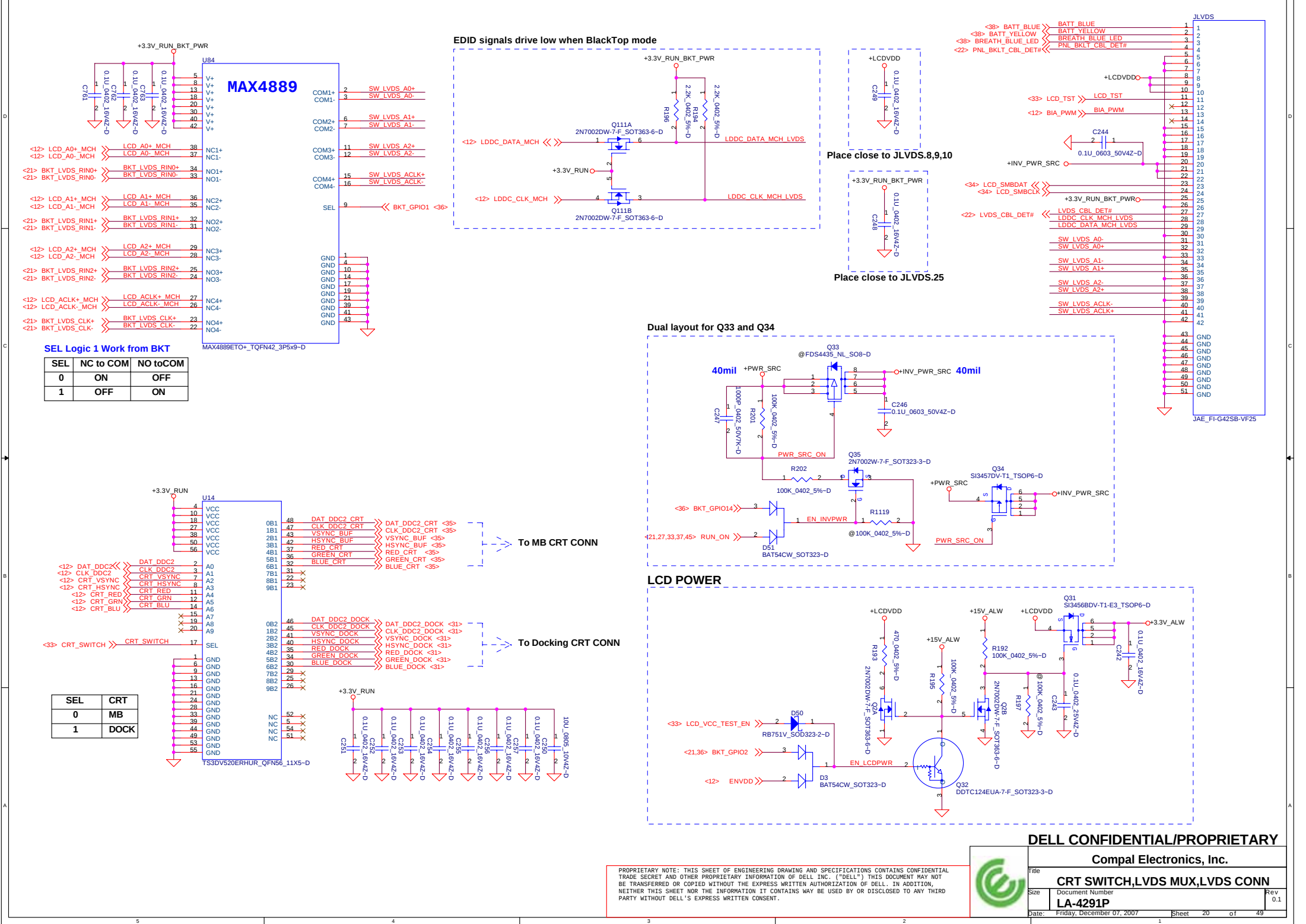
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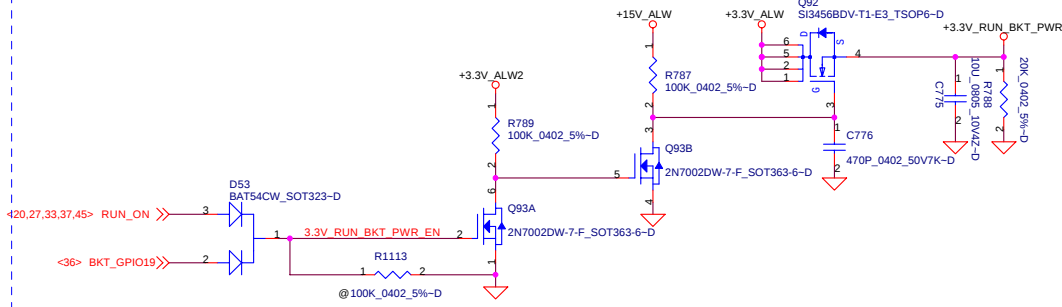
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AE25	VSS_201	VSS_302	AH8
AA25	VSS_202	VSS_303	AE8
IJ25	VSS_203	VSS_304	AD8
N25	VSS_204	VSS_305	AB8
J25	VSS_205	VSS_306	Y8
BD24	VSS_206	VSS_307	V8
BG23	VSS_207	VSS_308	P8
AJ23	VSS_208	VSS_309	M8
AE23	VSS_209	VSS_310	K8
AA23	VSS_210	VSS_311	H8
IJ23	VSS_211	VSS_312	B17
N22	VSS_212	VSS_313	E7
J22	VSS_213	VSS_314	BF6
G22	VSS_214	VSS_315	BC5
E22	VSS_215	VSS_316	BA5
K21	VSS_216	VSS_317	AW5
BG21	VSS_217	VSS_318	AU5
AW21	VSS_218	VSS_319	AR5
AU21	VSS_219	VSS_320	AN5
AG21	VSS_220	VSS_321	AL5
AE21	VSS_221	VSS_322	AG5
AA21	VSS_222	VSS_323	AE5
IJ21	VSS_223	VSS_324	AC5
N21	VSS_224	VSS_325	AA5
J21	VSS_225	VSS_326	W5
G21	VSS_226	VSS_327	U5
E21	VSS_227	VSS_328	N5
K20	VSS_228	VSS_329	L5
BG19	VSS_229	VSS_330	J5
AW19	VSS_230	VSS_331	G5
AU19	VSS_231	VSS_332	C5
AG19	VSS_232	VSS_333	BH4
AE19	VSS_233	VSS_334	BE3
AA19	VSS_234	VSS_335	U3
IJ18	VSS_235	VSS_336	E3
N18	VSS_236	VSS_337	BC1
J18	VSS_237	VSS_338	AW1
G17	VSS_238	VSS_339	AR1
E17	VSS_239	VSS_340	AL1
K17	VSS_240	VSS_341	AG1
BG16	VSS_241	VSS_342	AC1
AW16	VSS_242	VSS_343	W1
AU16	VSS_243	VSS_344	N1
AG16	VSS_244	VSS_345	J1
AE16	VSS_245	VSS_346	U1
AA16	VSS_246	VSS_347	AU43
IJ16	VSS_247	VSS_348	BB42
N16	VSS_248	VSS_349	AW38
J16	VSS_249	VSS_350	BA35
G15	VSS_250	VSS_351	L29
E15	VSS_251	VSS_352	N28
K15	VSS_252	VSS_353	N22
BG14	VSS_253	VSS_354	N20
AW14	VSS_254	VSS_355	N14
AU14	VSS_255	VSS_356	AL13
AG14	VSS_256	VSS_357	B10
AE14	VSS_257	VSS_358	AN13
AA14	VSS_258		
IJ14	VSS_259	VSS_359	N42
N14	VSS_260	VSS_360	N40
J14	VSS_261	VSS_361	N38
G13	VSS_262	VSS_362	M39
E13	VSS_263		
K13	VSS_264		
BG13	VSS_265		
AW13	VSS_266		
AU13	VSS_267		
AG13	VSS_268		
AE13	VSS_269		
AA13	VSS_270		
IJ13	VSS_271		
N13	VSS_272		
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G12	VSS_274		
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BG12	VSS_277		
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AU12	VSS_279		
AG12	VSS_280		
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AA12	VSS_282		
IJ12	VSS_283		
N12	VSS_284		
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J11	VSS_297		
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E10	VSS_299		
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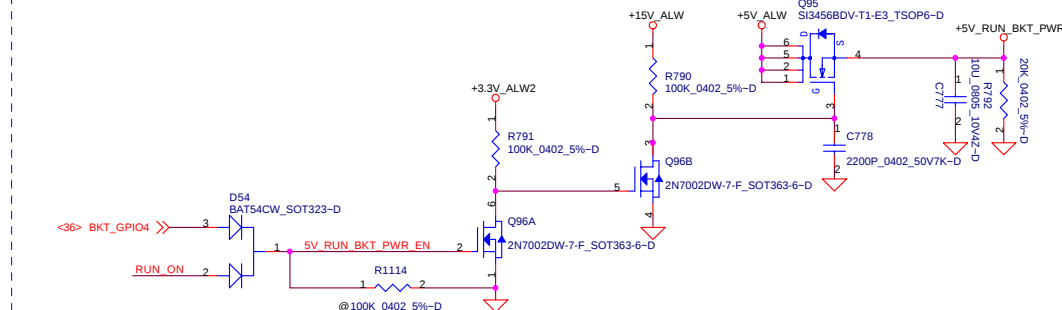




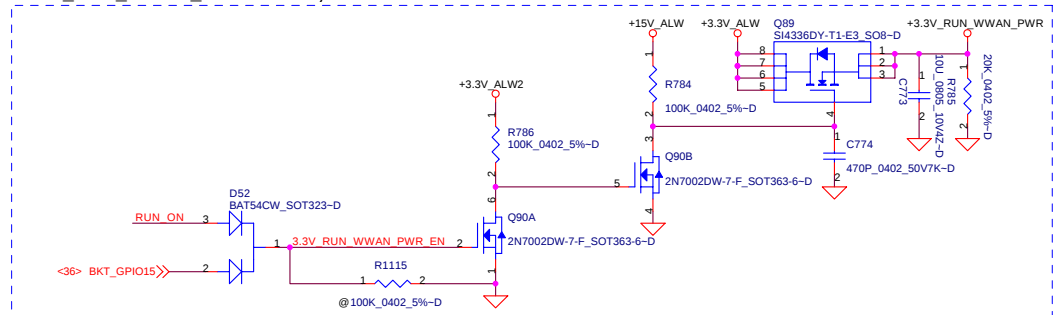
+3.3V_RUN_BKT_PWR Source



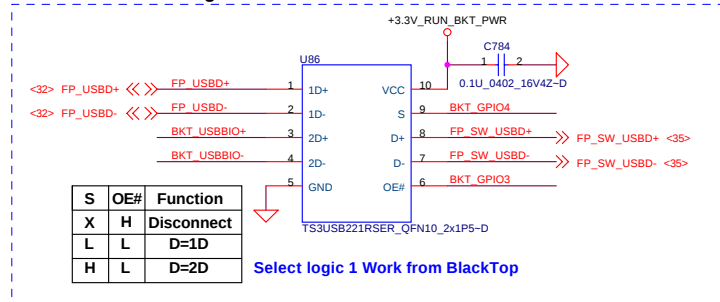
+5V_RUN_BKT_PWR Source, for Touch Pad and Audio Amplifier



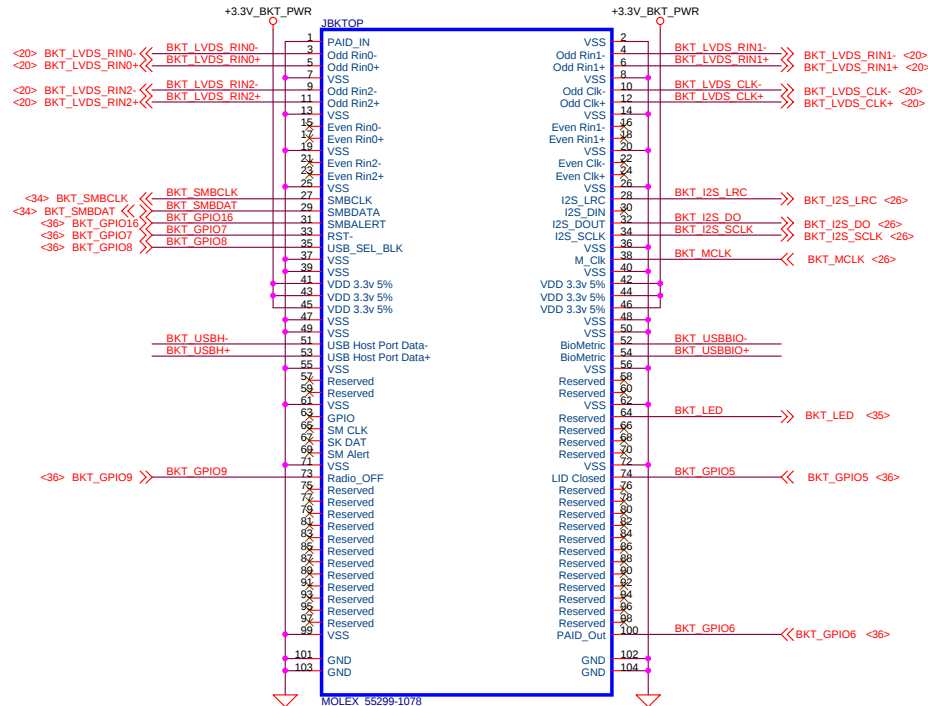
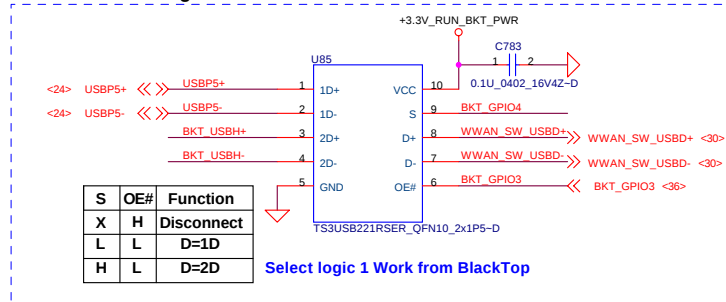
+3.3V_RUN_WWAN_PWR Source, for WWAN



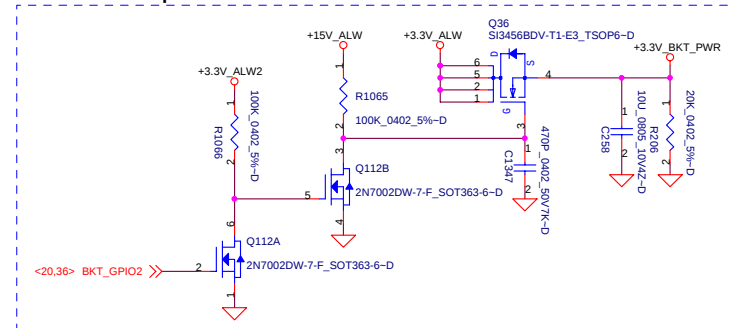
For Biometric USB signals isolation



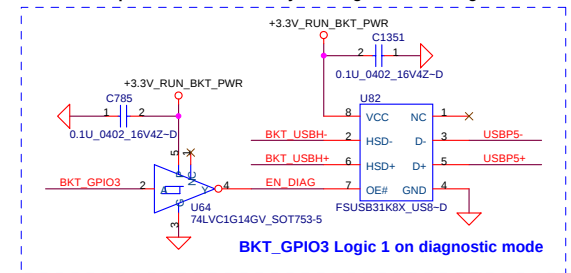
For WWAN USB signals isolation



Enable BlackTop POWER



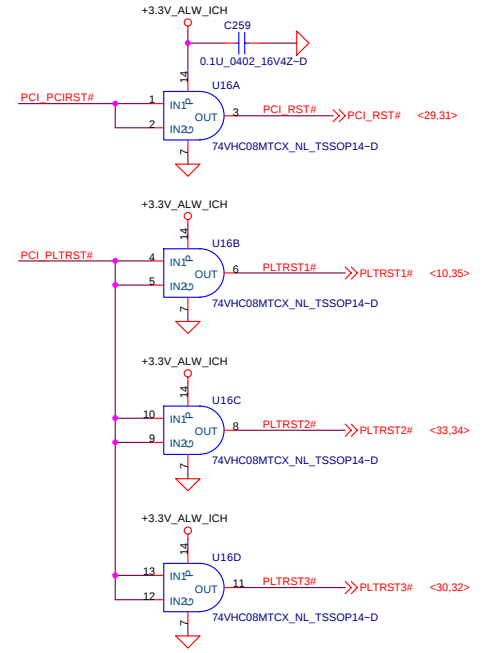
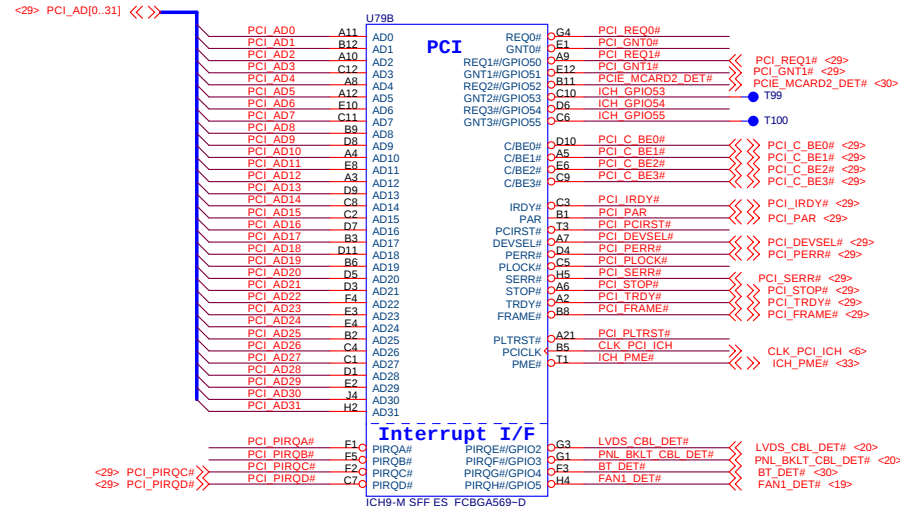
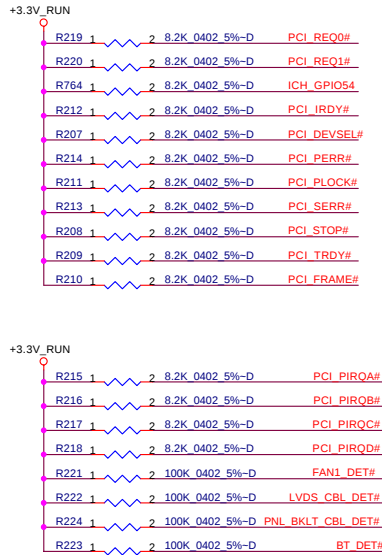
Add BlackTop to ICH9M interface by USB signals when diagnostic mode



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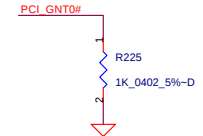
Compal Electronics, Inc.	
BlackTop POWER and CONN	
LA-4291P	Rev 0.1
Date: Friday, December 07, 2007	Sheet 21 of 49

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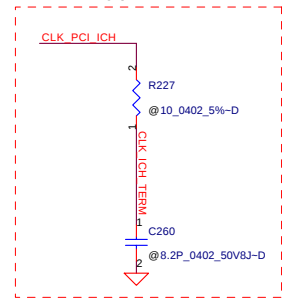


There is a weak integrated pull-up resistor on SPI_CS#1 pin

Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Destination
0	1	SPI
1	0	PCI
1	1	LPC



Place closely pin U79.B5



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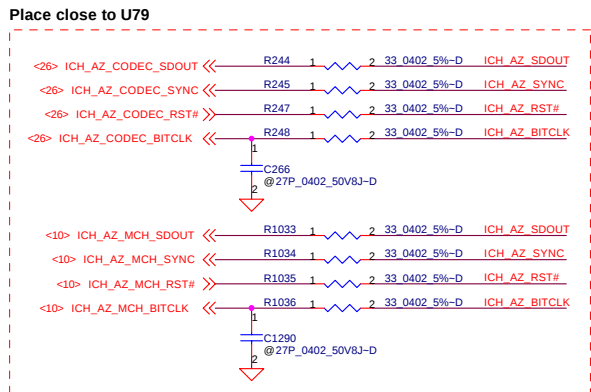
Compal Electronics, Inc.



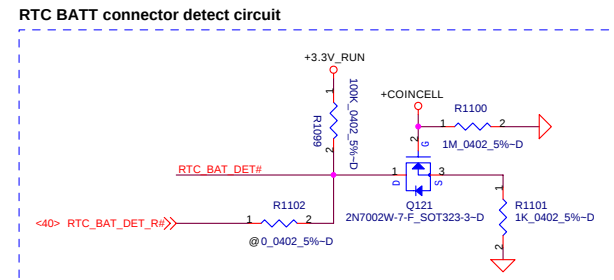
Title		
ICH9M SFF(1/4)		
Size	Document Number	Rev
	LA-4291P	0.1
Date	Friday, December 07, 2007	Sheet 22 of 49

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ME_CLR	TPM setting
Short	Clear ME RTC Registers
Open	Keep ME RTC Registers



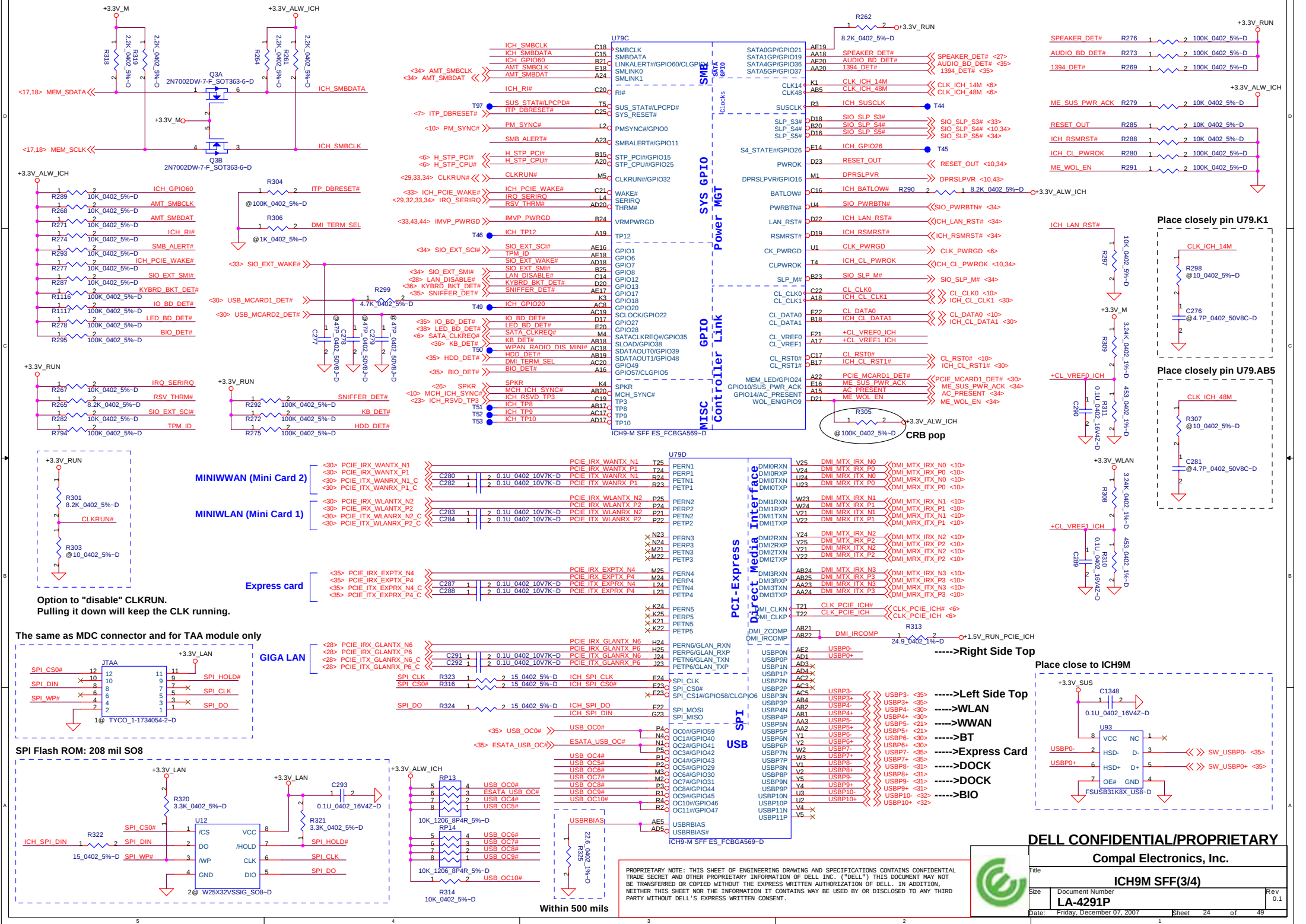
There is a weak integrated pull-up resistor on ICH_RSVD_TP3 pin
There is a weak integrated pull-down resistor on HDA_SDOUT pin

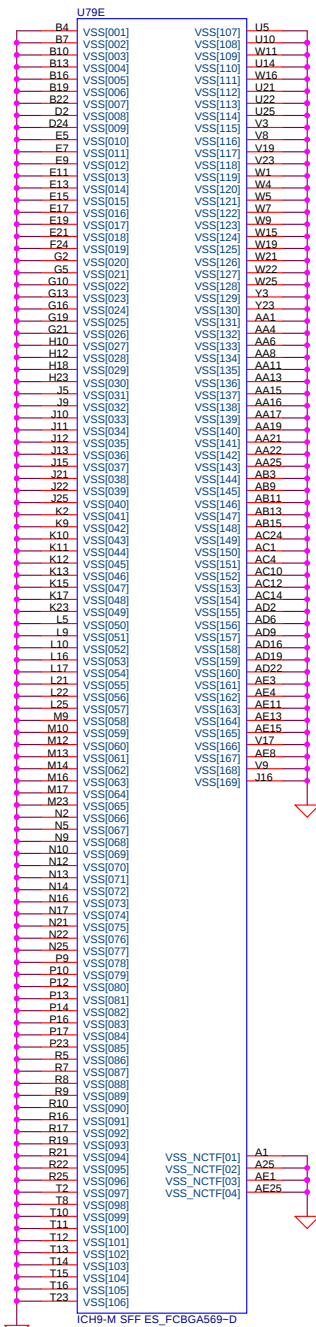


Size	Document Number LA-4291P	Rev. 0.
Date:	Friday, December 07, 2007	Sheet 23 of 49

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Compal Electronics, Inc.

Document Number
LA-4291P



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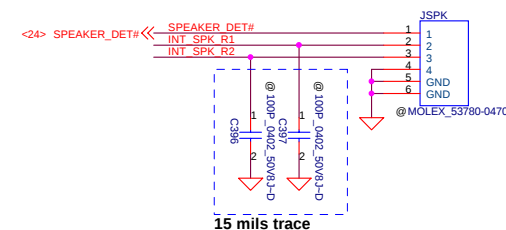
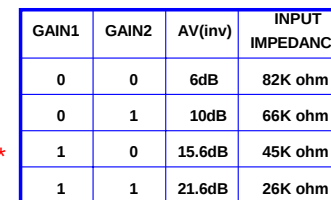
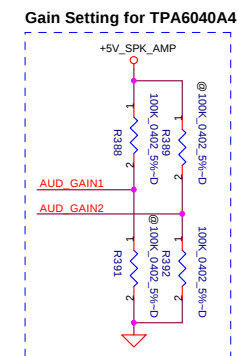
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Codec 92HD71B and I2C D/A A/D converters

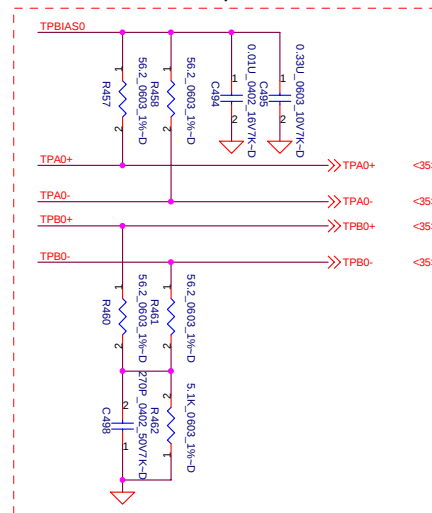
size	Document Number LA 4301B	Rev 0.1
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UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-down	Pull-down	Enable SD,MMC Card

Media I/F	SD Card	MMC Card
MDIO00	SDCD#	MMCCD#
MDIO01		
MDIO02		
MDIO03	SDWP#	
MDIO04	SDPWR0	MMCPWR
MDIO05	SDPWR1	
MDIO06	SDLED#	MMCLEd#
MDIO07	SDEXTCK	
MDIO08	SDCCMD	MMCCMD
MDIO09	SDCCLK	MMCCCLK
MDIO10	SDCDAT0	MMCDAT0
MDIO11	SDCDAT1	MMCDAT1
MDIO12	SDCDAT2	MMCDAT2
MDIO13	SDCDAT3	MMCDAT3
MDIO14		MMCDAT4
MDIO15		MMCDAT5
MDIO16		MMCDAT6
MDIO17		MMCDAT7
MDIO18		
MDIO19		



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Mini Card 2---WWAN



Title	Mini WLAN/WWAN, SIM card and BT
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Date:	Friday, December 07, 2007	Sheet	30 of 49

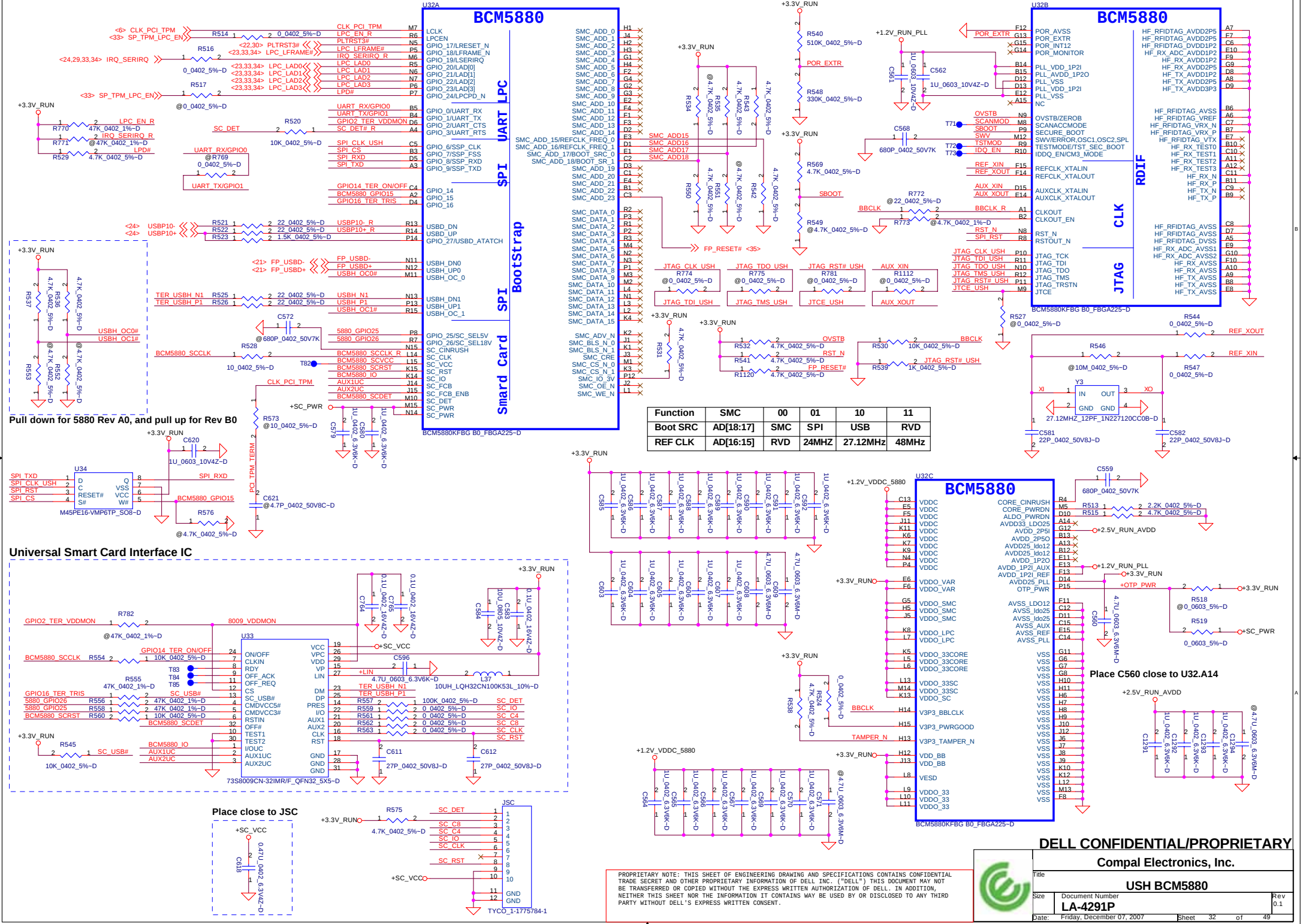
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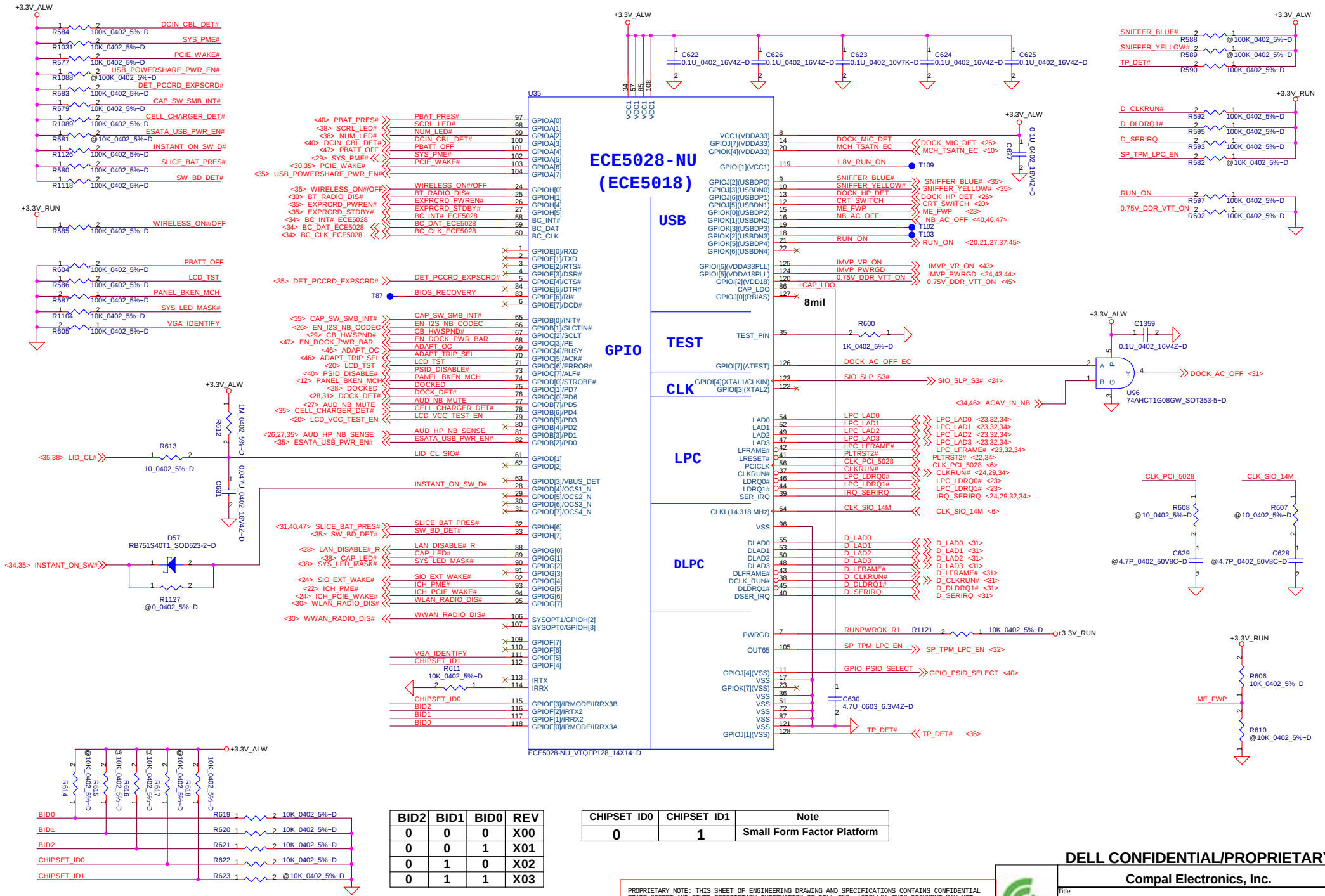
RCLAMP0524P.TCT-D									
DPB_LANE_P0_C	1		10	DPB_LANE_P0_C					
DPB_LANE_N0_C	2		9	DPB_LANE_N0_C					
DPB_LANE_P1_C	4		7	DPB_LANE_P1_C					
DPB_LANE_N1_C	5		6	DPB_LANE_N1_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DPB_LANE_P2_C	1		10	DPB_LANE_P2_C					
DPB_LANE_N2_C	2		9	DPB_LANE_N2_C					
DPB_LANE_P3_C	4		7	DPB_LANE_P3_C					
DPB_LANE_N3_C	5		6	DPB_LANE_N3_C					
	3								
	8								
RCLAMP0524P.TCT-D									
SDVO_CTRLCLK	1		10	SDVO_CTRLCLK					
SDVO_CTRLDATA	2		9	SDVO_CTRLDATA					
DPB_DOCK_HPD	4		7	DPB_DOCK_HPD					
DPB_CA_DET	5		6	DPB_CA_DET					
	3								
	8								
RCLAMP0524P.TCT-D									
DPC_LANE_P0_C	1		10	DPC_LANE_P0_C					
DPC_LANE_N0_C	2		9	DPC_LANE_N0_C					
DPC_LANE_P1_C	4		7	DPC_LANE_P1_C					
DPC_LANE_N1_C	5		6	DPC_LANE_N1_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DPC_LANE_P2_C	1		10	DPC_LANE_P2_C					
DPC_LANE_N2_C	2		9	DPC_LANE_N2_C					
DPC_LANE_P3_C	4		7	DPC_LANE_P3_C					
DPC_LANE_N3_C	5		6	DPC_LANE_N3_C					
	3								
	8								
RCLAMP0524P.TCT-D									
DDPC_CTRLCLK	1		10	DDPC_CTRLCLK					
DDPC_CTRLDATA	2		9	DDPC_CTRLDATA					
DPC_DOCK_HPD	4		7	DPC_DOCK_HPD					
DPC_CA_DET	5		6	DPC_CA_DET					
	3								
	8								
RCLAMP0524P.TCT-D									



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BID2	BID1	BID0	REV
0	0	0	X00
0	0	1	X01
0	1	0	X02
0	1	1	X03

CHIPSET_ID0	CHIPSET_ID1	Note
0	1	Small Form Factor Platform

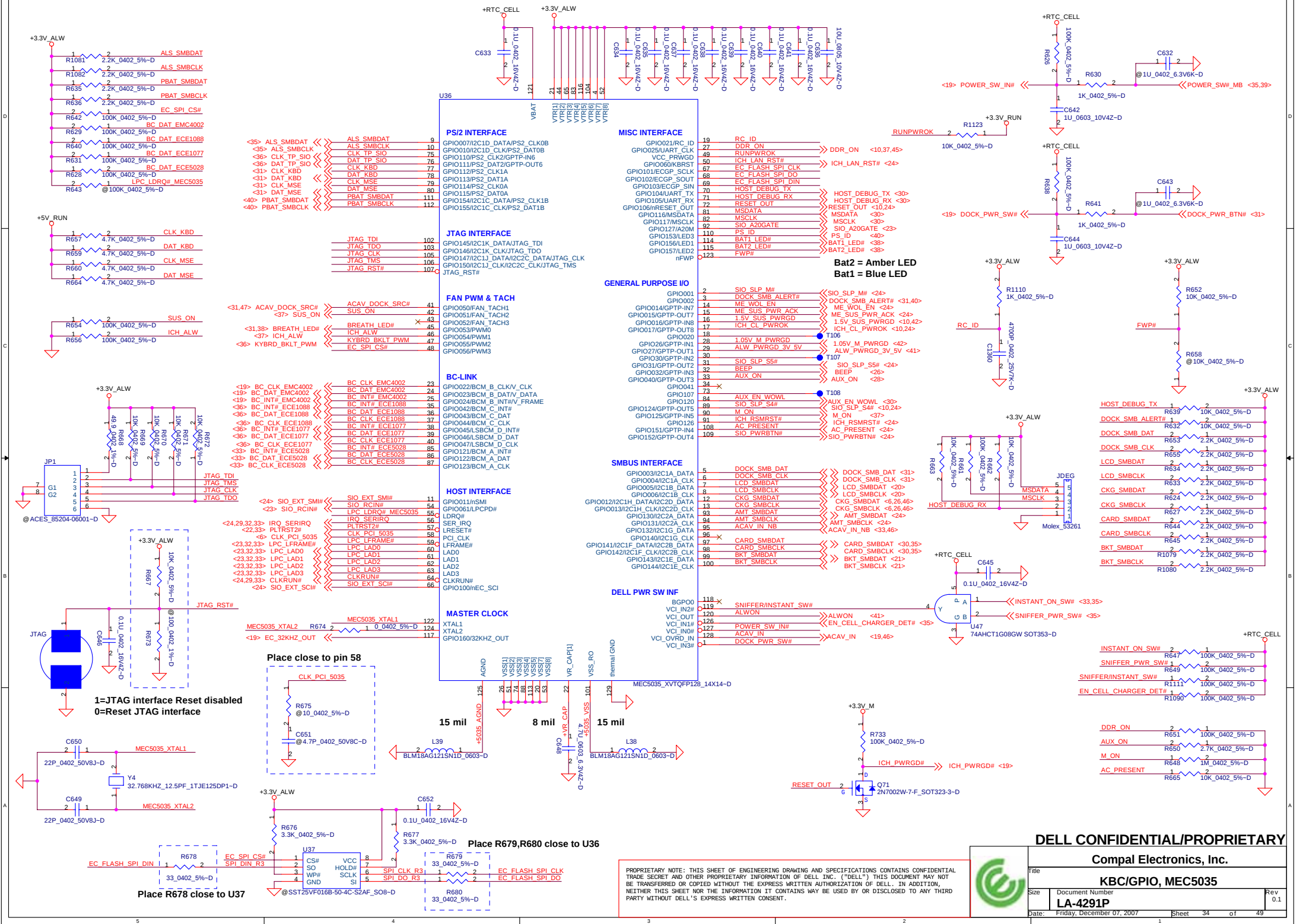
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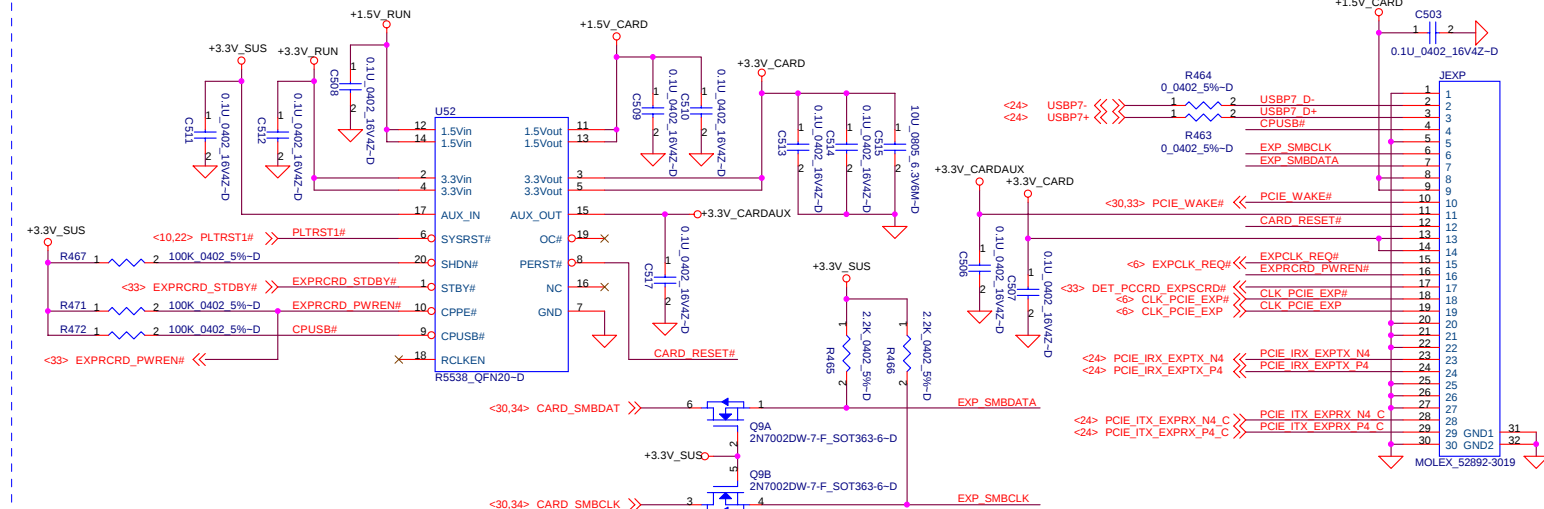
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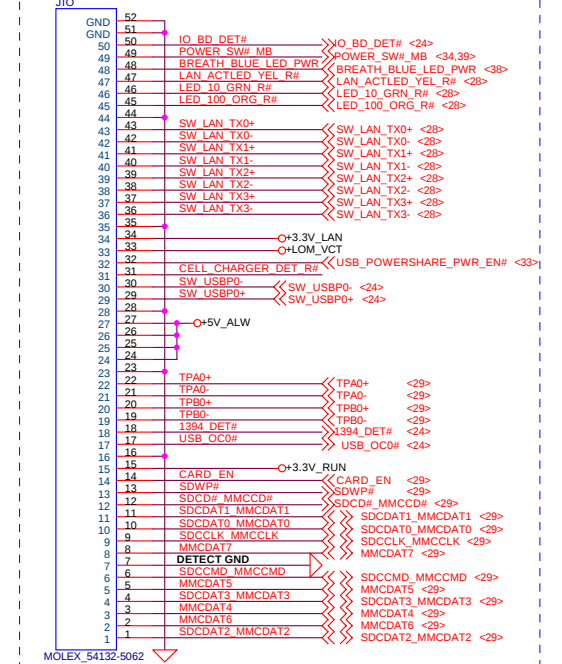
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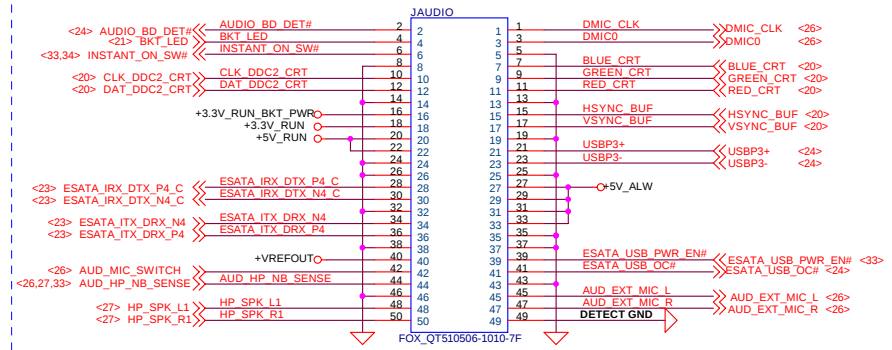
Express Card



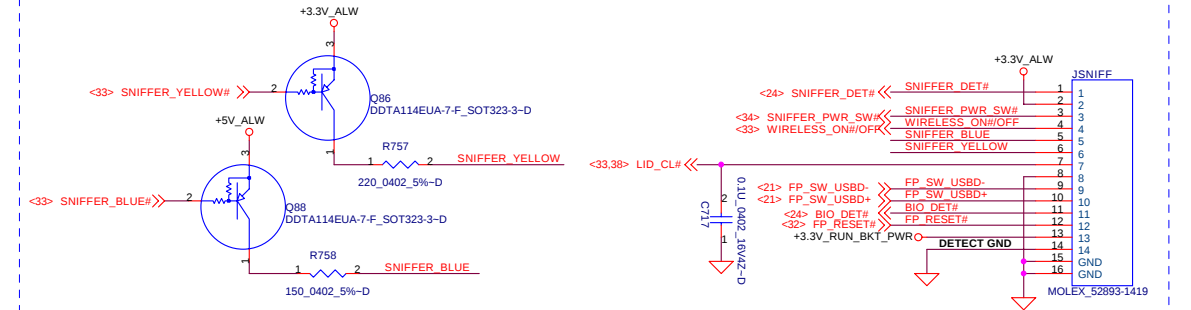
IO/B connector, Right side



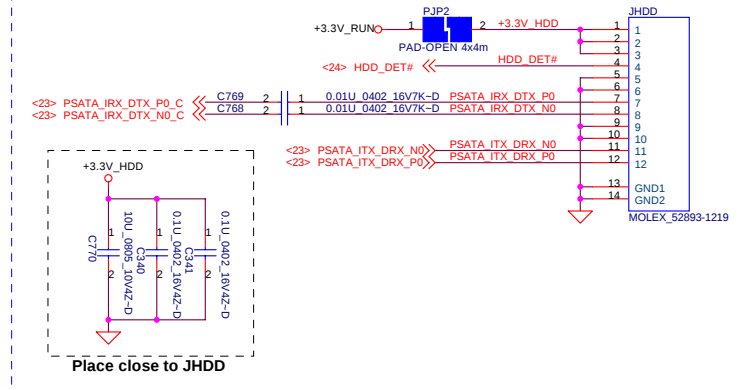
AUDIO/B BTB connector, Left side



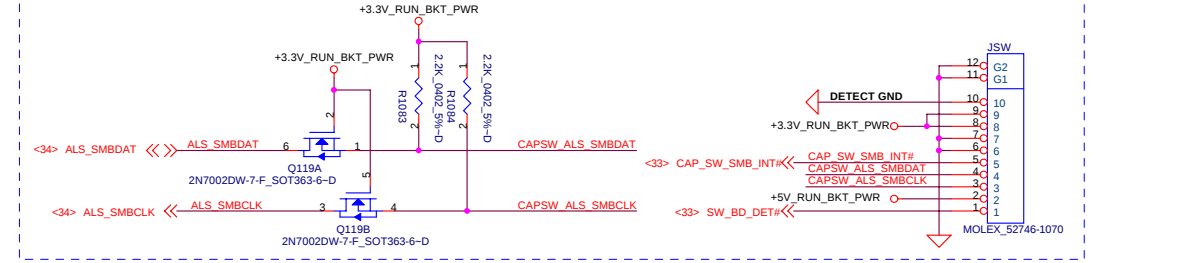
SNIFFER connector and LED



1.8" Micro SATA HDD connector



CAP Switch and ALS connector

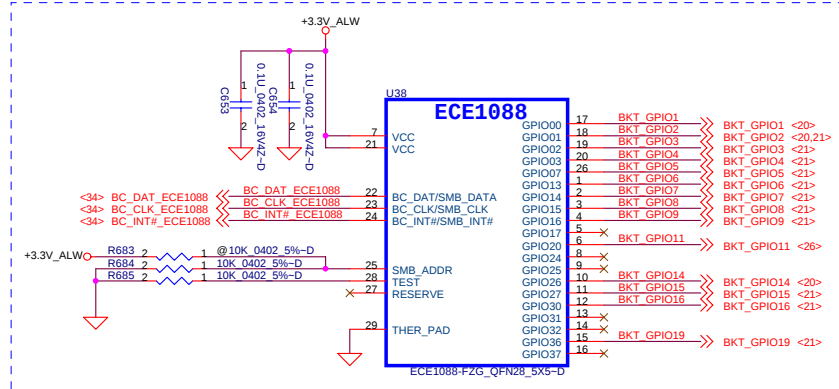


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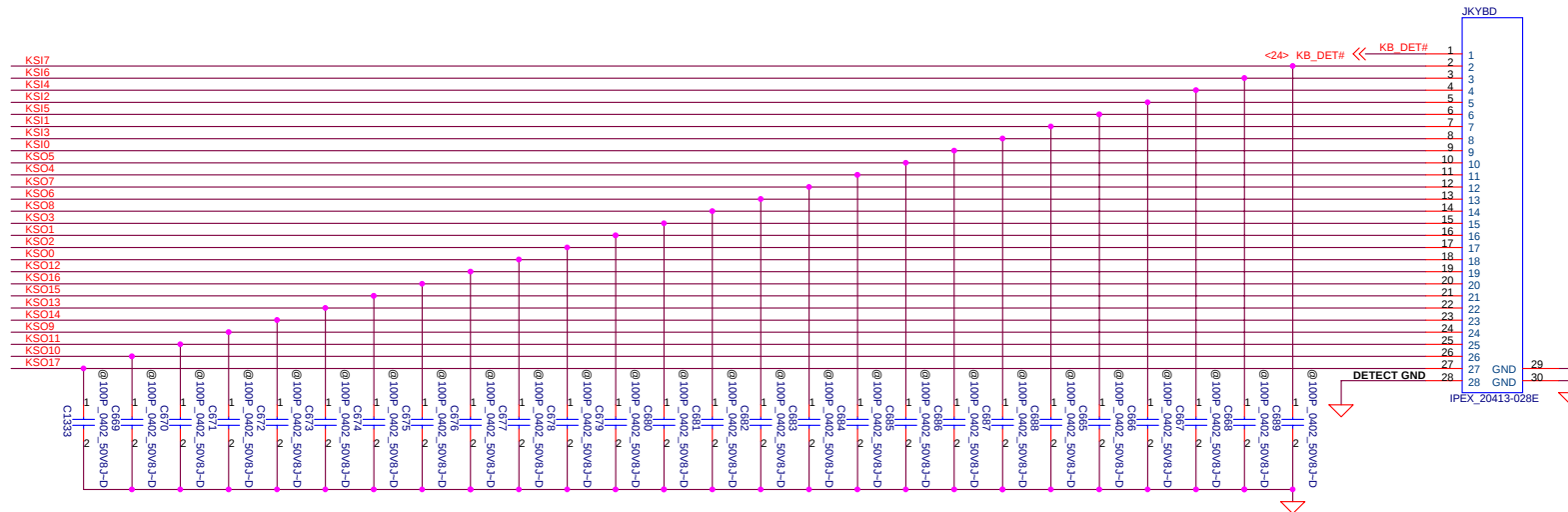
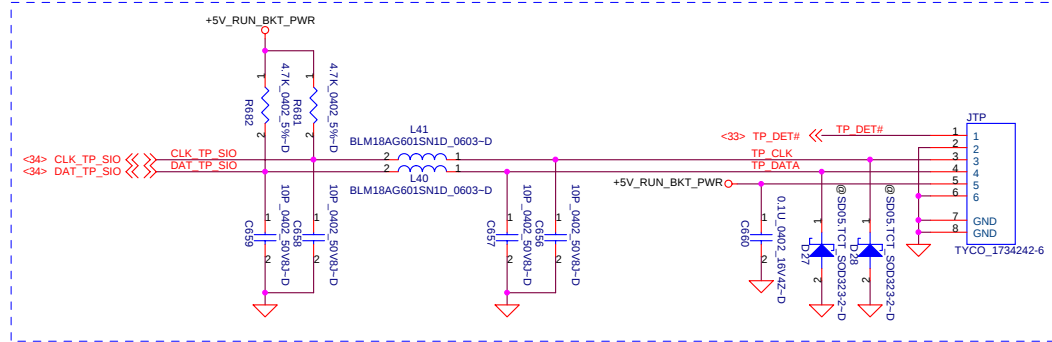
Compal Electronics, Inc.	
Title	Express Card, HDD, Sniffer, IO CONN
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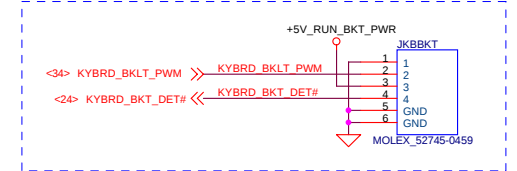
GPIO Expander for BlackTop



Touch Pad connector



Keyboard Backlight connector



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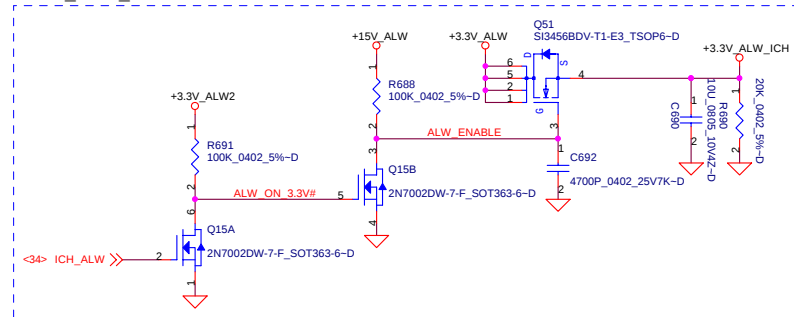
Compal Electronics, Inc.



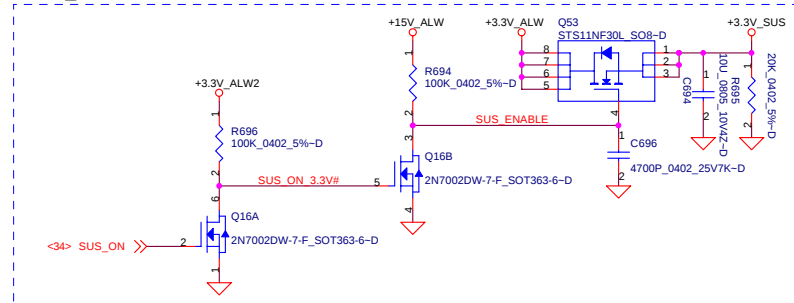
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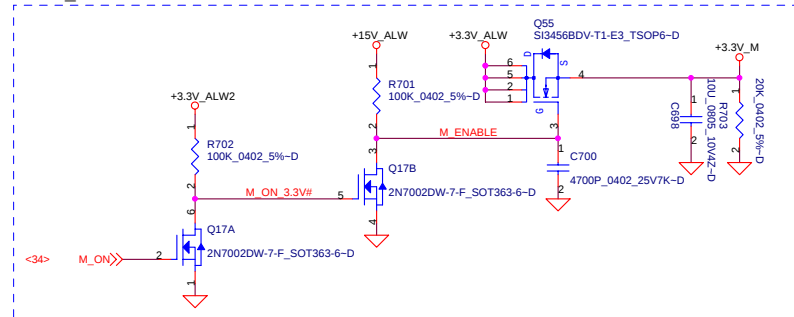
+3.3V_ALW_ICH Source



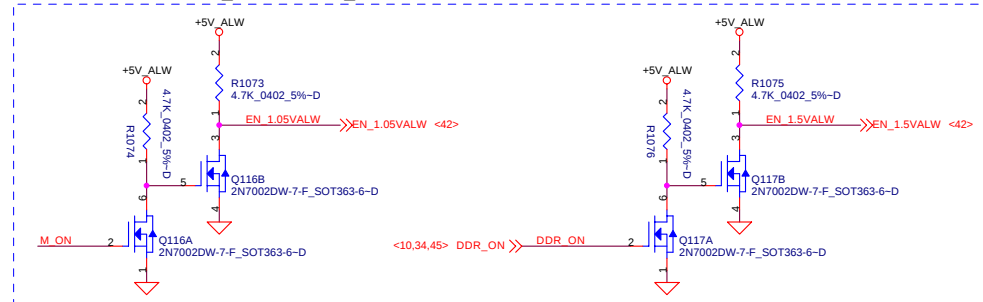
+3.3V_SUS Source



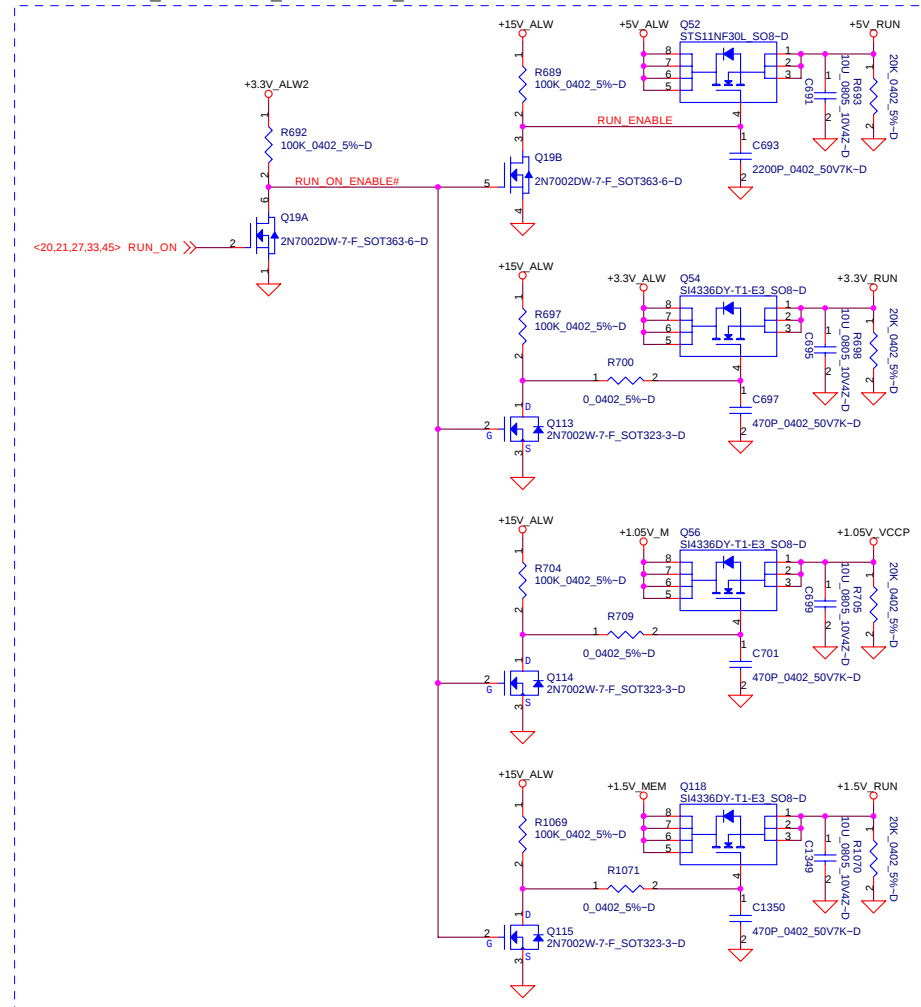
+3.3V_M Source



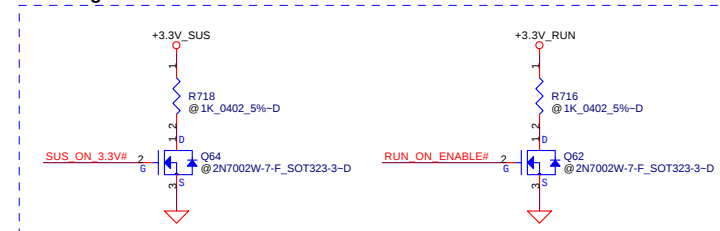
Level shifter for +1.05V_M and +1.5V_MEM PWM IC



+5V_RUN/+3.3V_RUN/+1.05V_VCCP/+1.5V_RUN Source



Discharg Circuit



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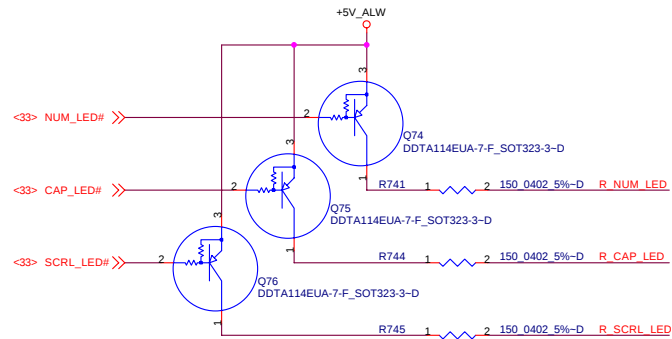
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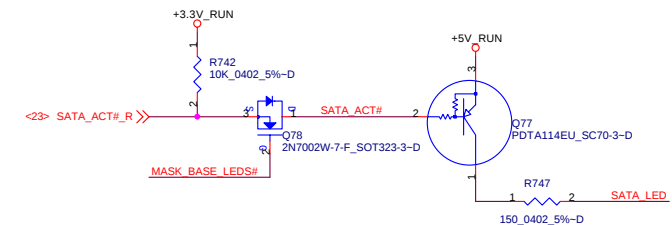
POWER CONTROL

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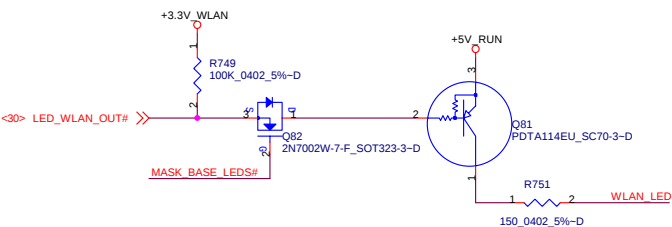
Keyboard Status, Num Lock/Caps Lock/Scroll Lock LEDs



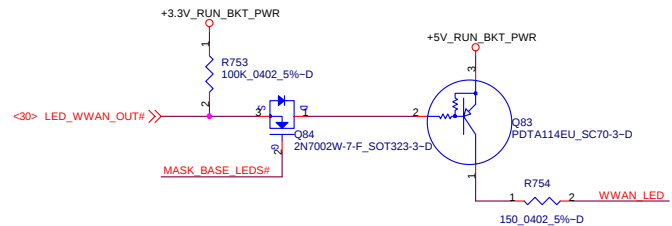
HDD LED



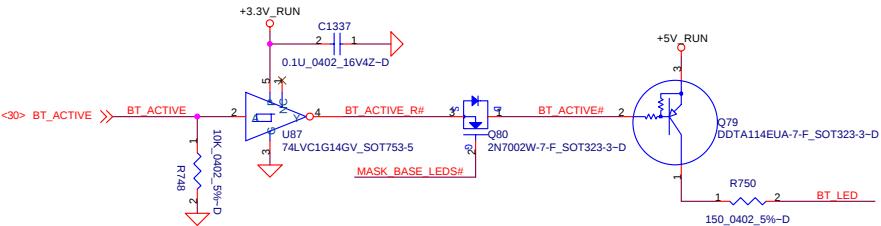
WLAN LED



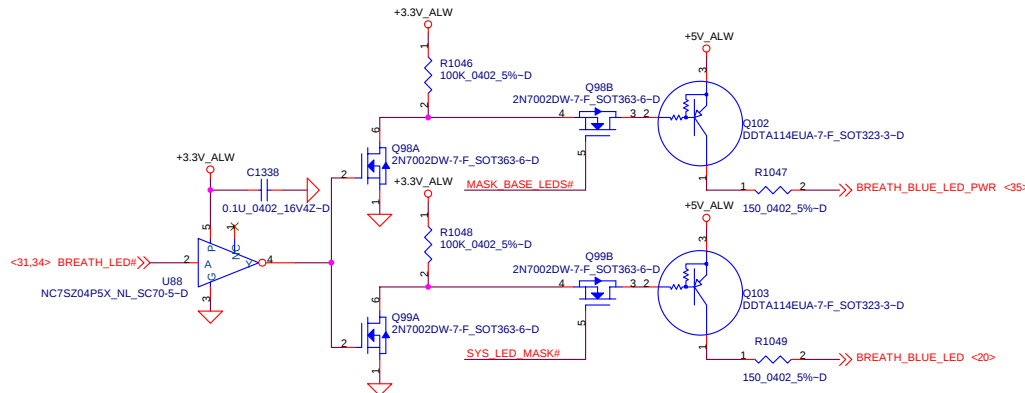
WWAN LED



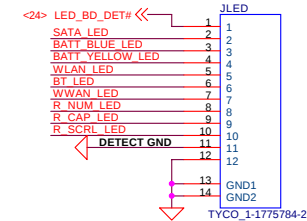
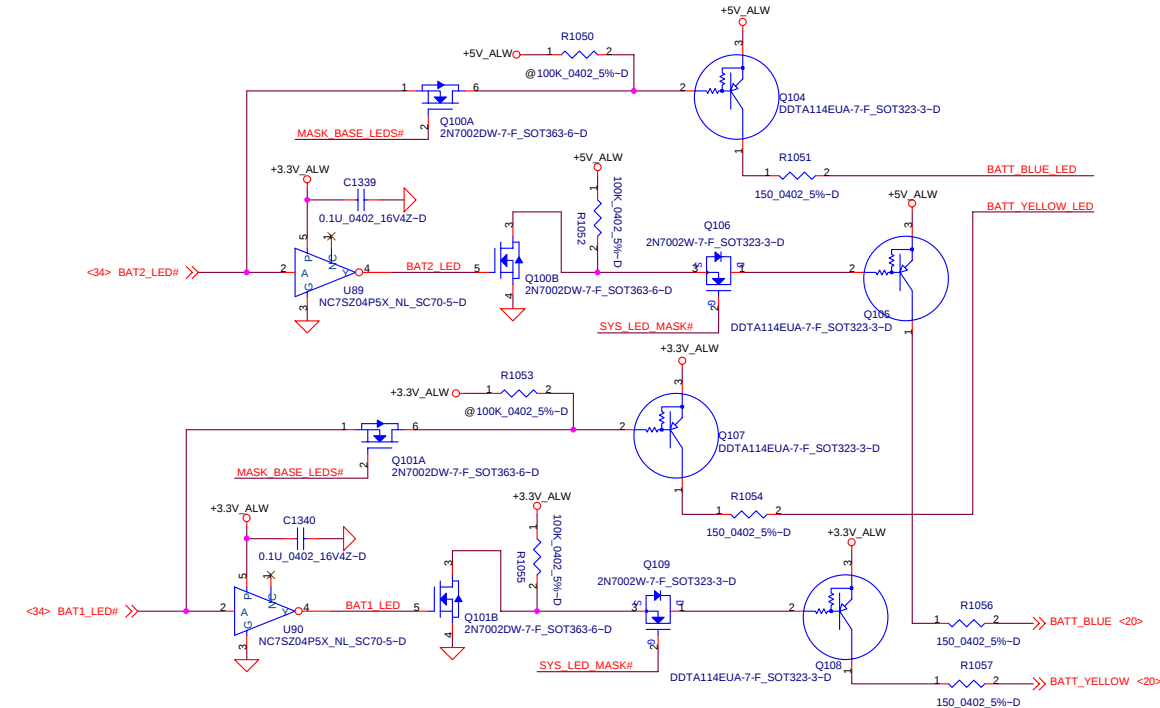
BLUETOOTH LED



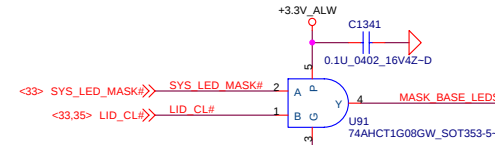
POWER/SUSPEND breathing LED



BATTERY LED



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

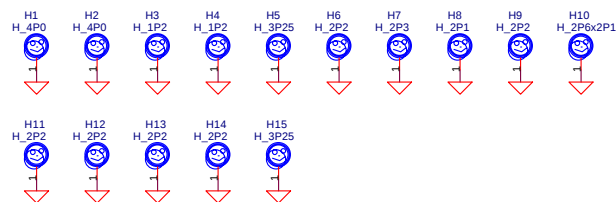
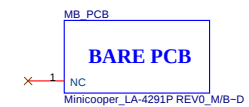
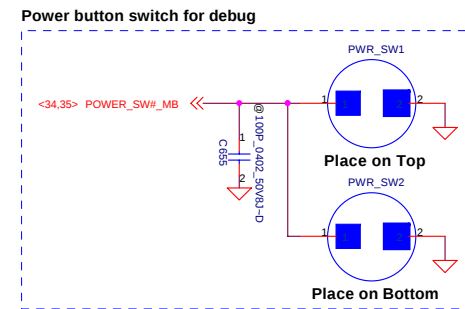
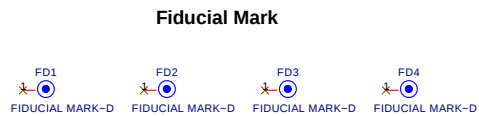


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System LEDs Control
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Standoff and EE Design Part				
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+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP

5 Volt +/-5%
Thermal Design Current:7.39A
Peak current: 10.55A
OCP min: 11A

3.3 Volt +/-5%
Thermal Design Current: 6.73A
Peak current: 9.62A
OCP min: 11A

VOUT1=5V
L=2.2uF
Fsw=400KHz
D=0.256
Output Ripple Current=4.23A
Output Ripple Voltage=4.23A*18mOhm=76.14mV

VOUT2=3.3V
L=2.2uF
Fsw=500KHz
D=0.169
Output Ripple Current=2.49A
Output Ripple Voltage=2.49A*25mOhm=62.25mV

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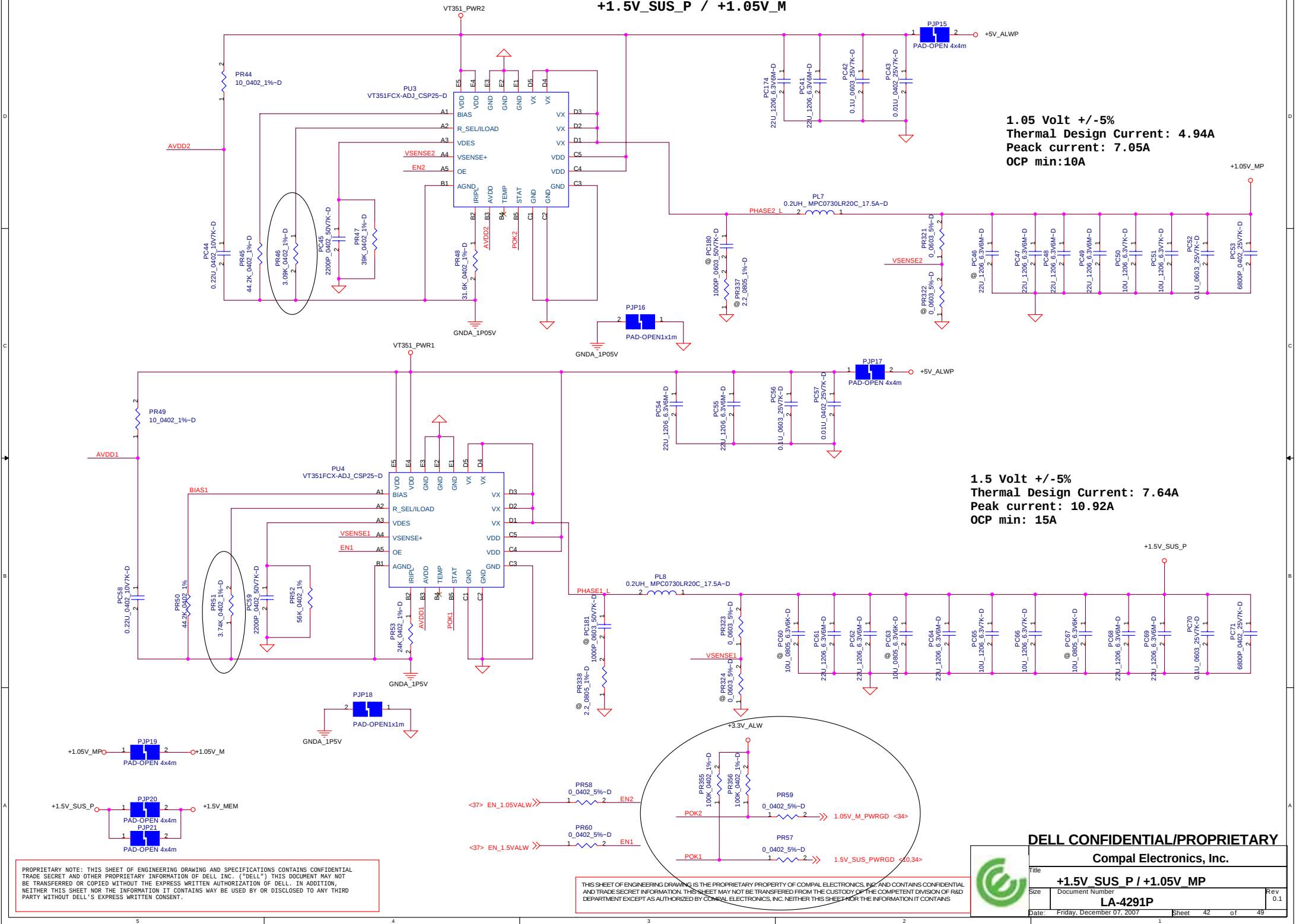
Compale Electronics, Inc.

DC/DC +3V/ +5V

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+1.5V_SUS_P / +1.05V_M



1.05 Volt +/-5%
Thermal Design Current: 4.94A
Peak current: 7.05A
OCp min:10A

1.5 Volt +/-5%
Thermal Design Current: 7.64A
Peak current: 10.92A
OCp min: 15A

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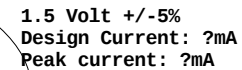
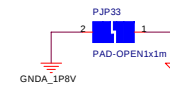
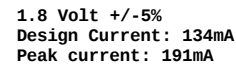
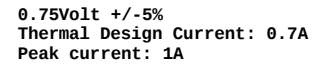
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+1.5V SUS P / +1.05V MP		
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DDR3 Termination



It's for layout first.

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+1.8VRUNP/ +0.75V_DDR_VT

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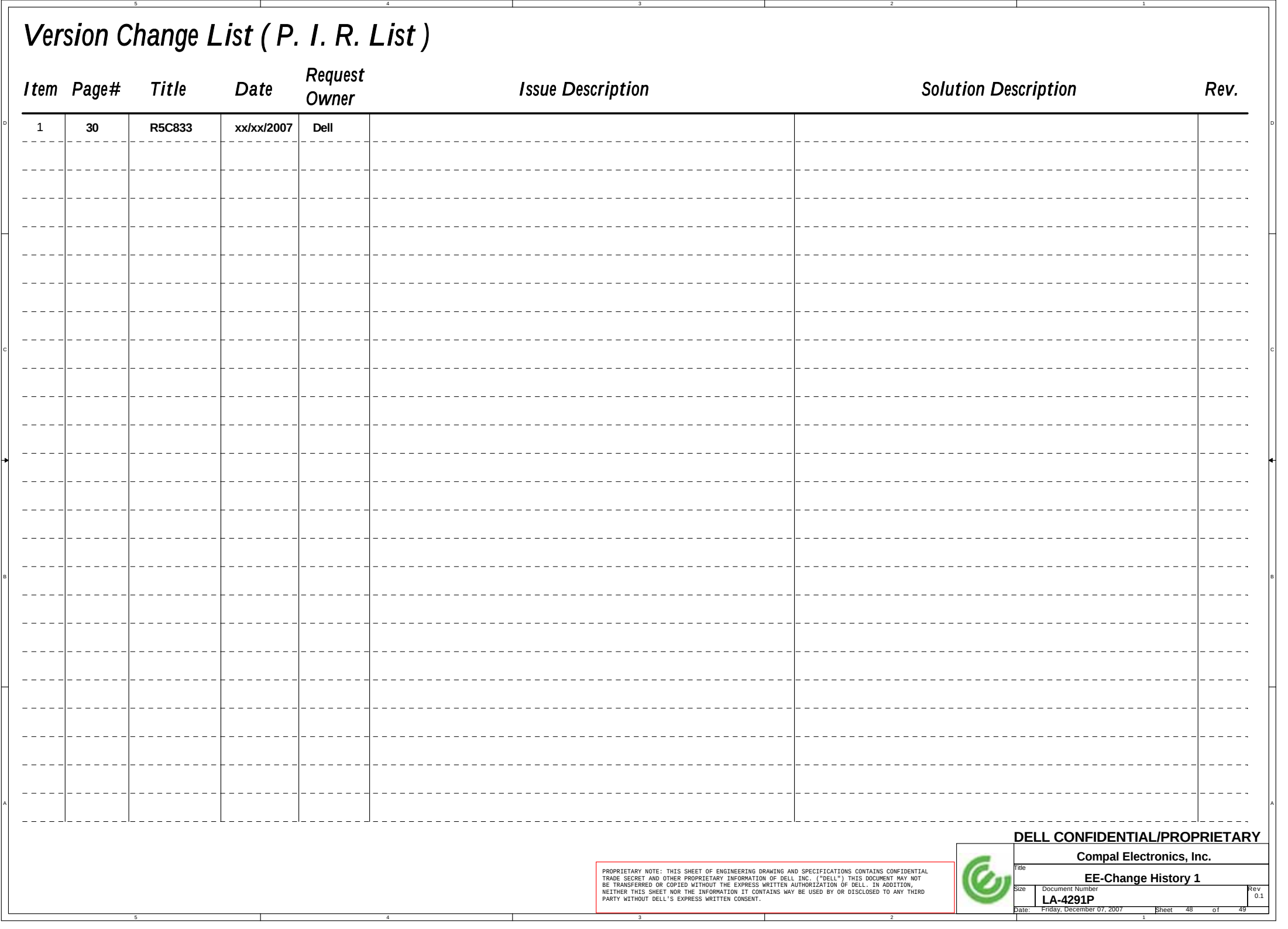
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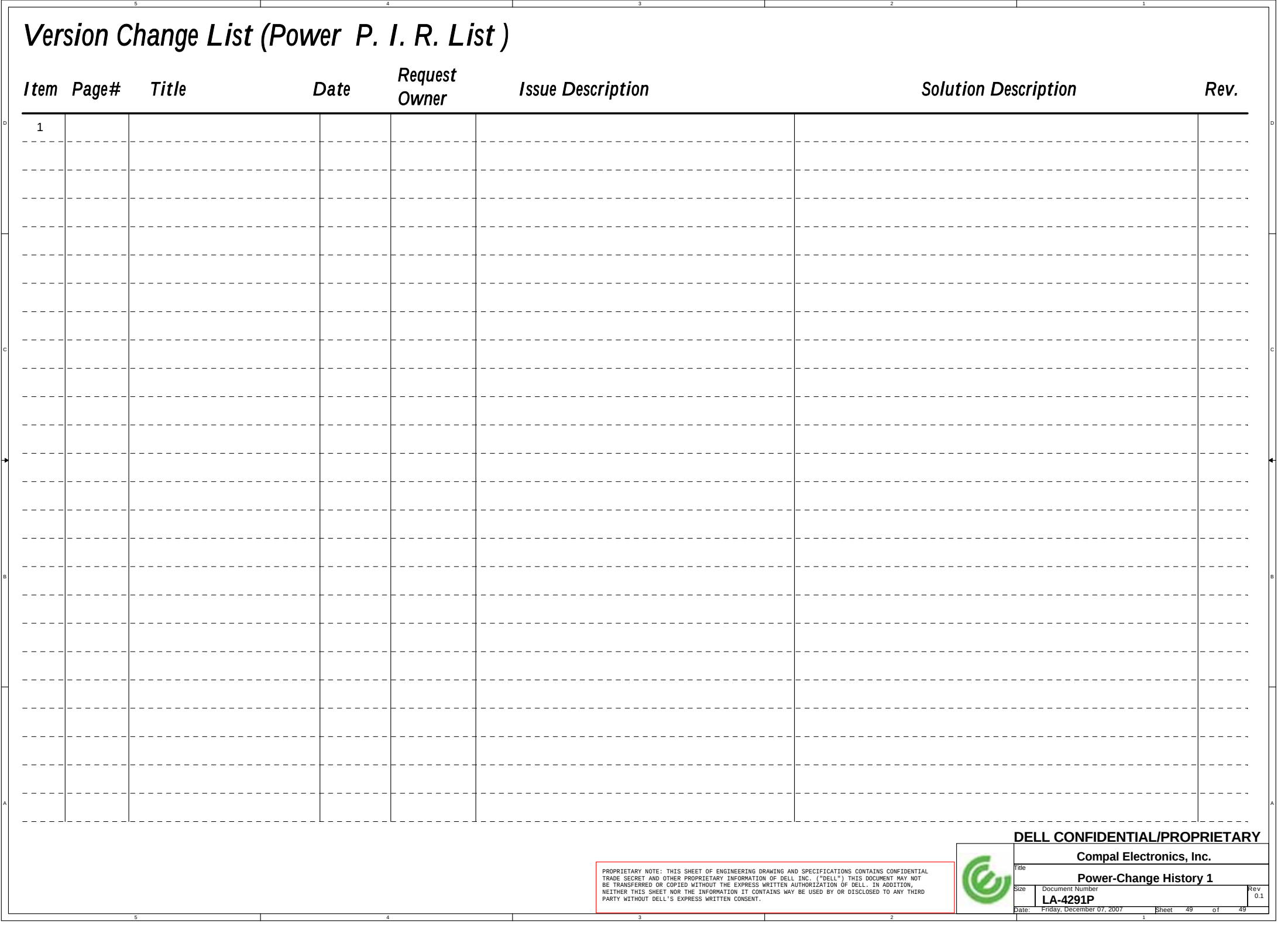


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Charger			
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