ZZZ1
DAZ

ZZZ2
12.1W_PCB_LA5191P
Part Number = DA80000EF10

ZZZ3
12.1W_PCB_LS5191P
Part Number = DA60000C410

ZZZ4
12.1W_PCB_LS5192P
Part Number = DA40000K110

ZZZ5
12.1W_PCB_LS5193P
Part Number = DA40000K010

ZZZ6
12.1W_PCB_LS5194P
Part Number = DA20000GH10

KIUE0

Schematics Document

Mobile Penryn PGA with Intel Cantiga_GM45+ICH9-M core logic

REV:1.0

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics,Ltd.

Title: **Cover Sheet**

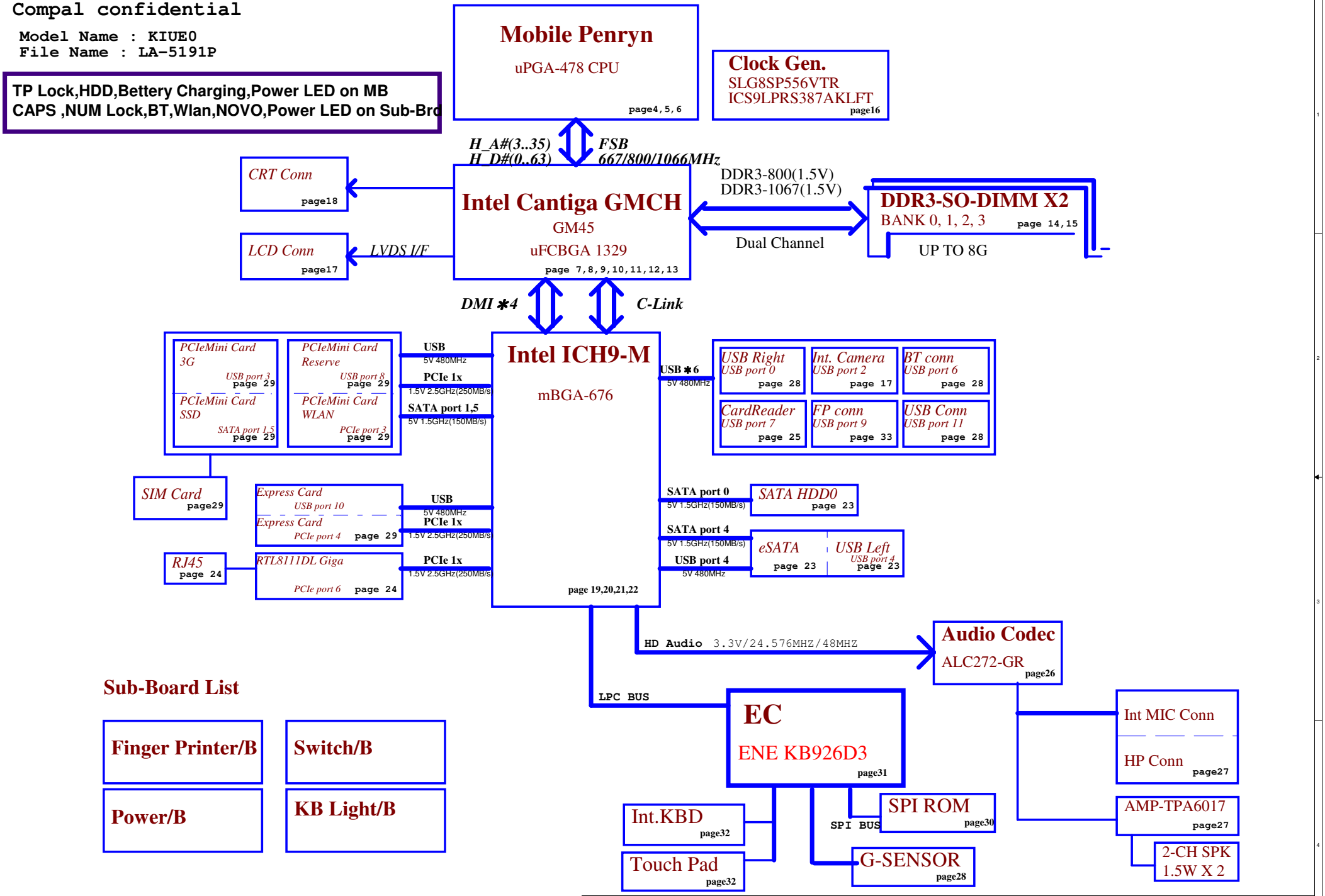
Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Thursday, June 25, 2009 Sheet 1 of 43

Compal confidential

Model Name : KIUE0
File Name : LA-5191P

TP Lock,HDD,Bettery Charging,Power LED on MB
CAPS ,NUM Lock,BT,Wlan,NOVO,Power LED on Sub-Brd



Sub-Board List

- Finger Printer/B
- Switch/B
- Power/B
- KB Light/B

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: MB Block Diagram

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 2 of 43

Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+GPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for NB	ON	OFF	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	CRT	LAN	Finger printer	BLUE TOOTH	3G SIM slot	Mini card
description	(Q)	(C)	(F)	(B)	(3)	(D2)
explain						
BTO						

External PCI Devices

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	Smart Battery	

EC SM Bus2 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	CPU THM Sen SMSC SMC1402	

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	
+3VS	DDR DIMM0	
+3VS	DDR DIMM1	
+3VS	Express	

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

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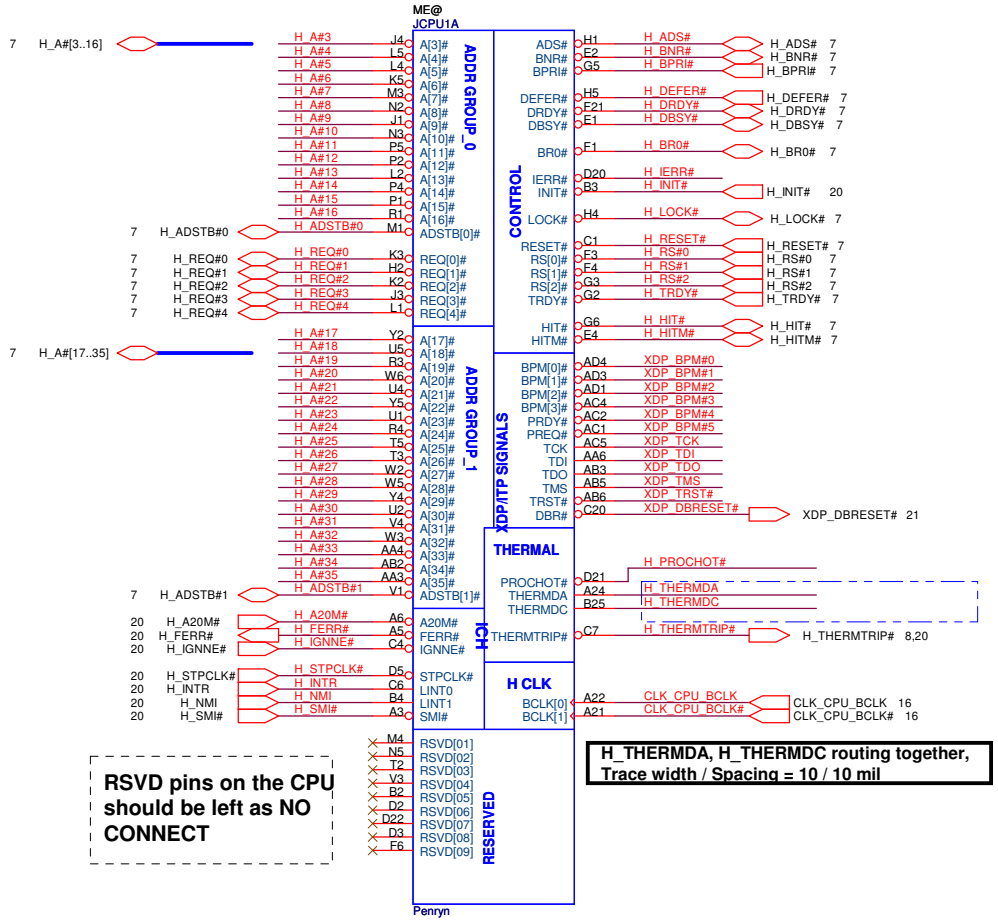
Title: MB Notes List

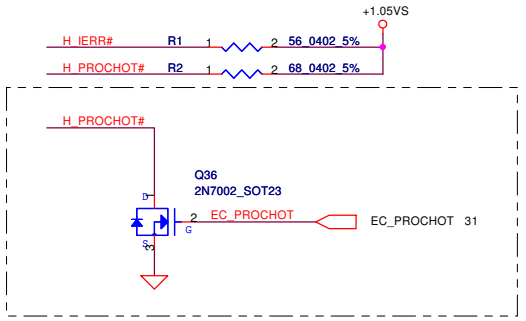
Size: B | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 3 of 43

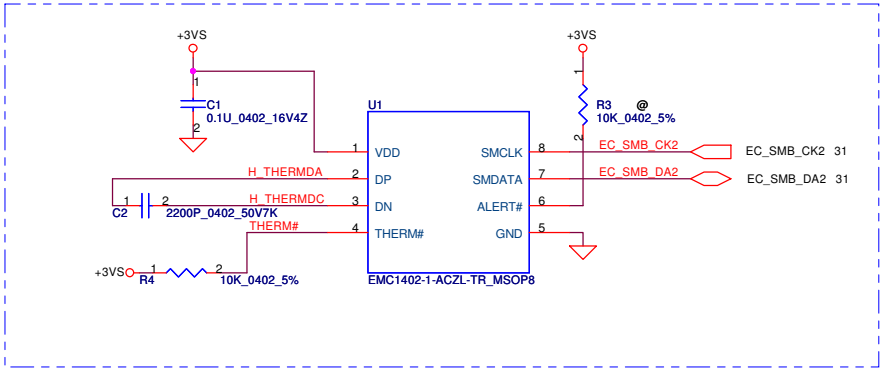


RSVD pins on the CPU should be left as NO CONNECT

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

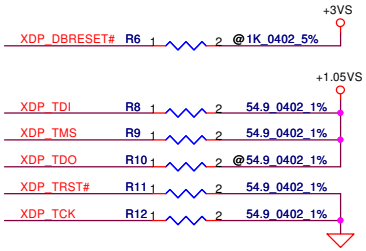


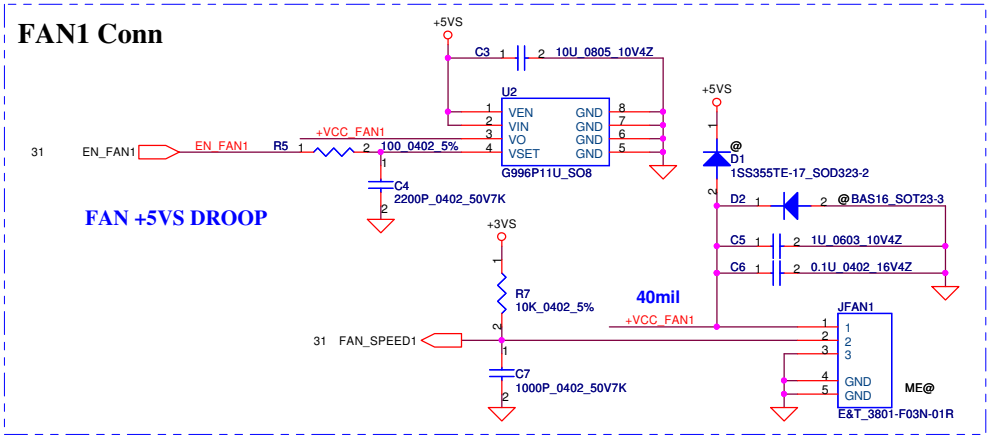
Hardware force mechanism for throttling



Address:100_1100

XDP Reserve for debug , Please close to CPU side





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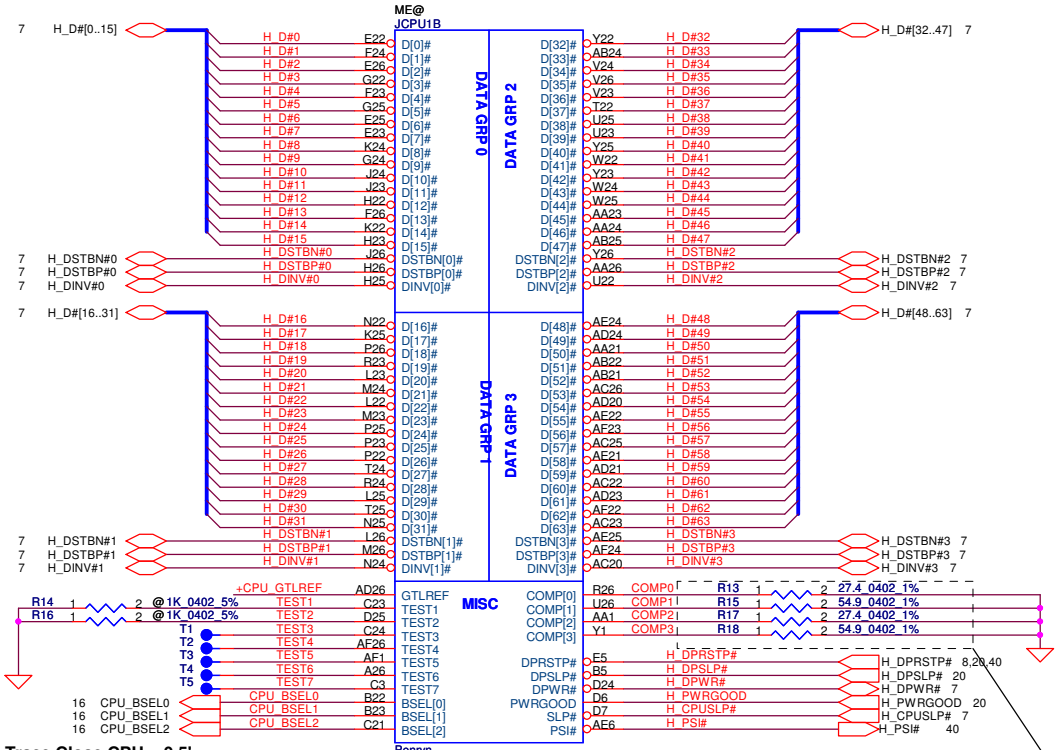
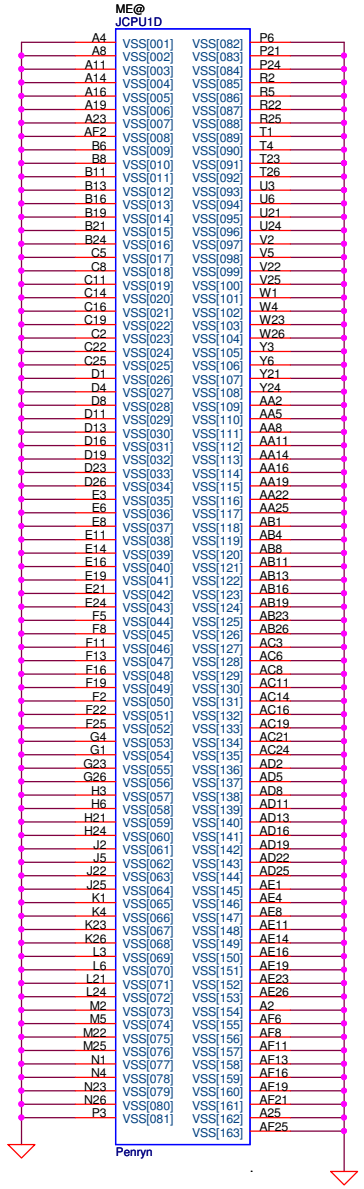
Title: Penryn(1/3)

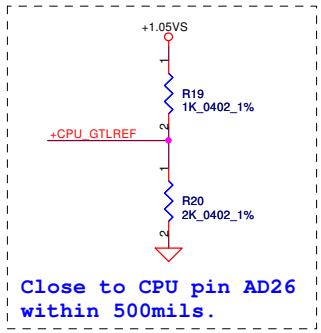
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 4 of 43





layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs



Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

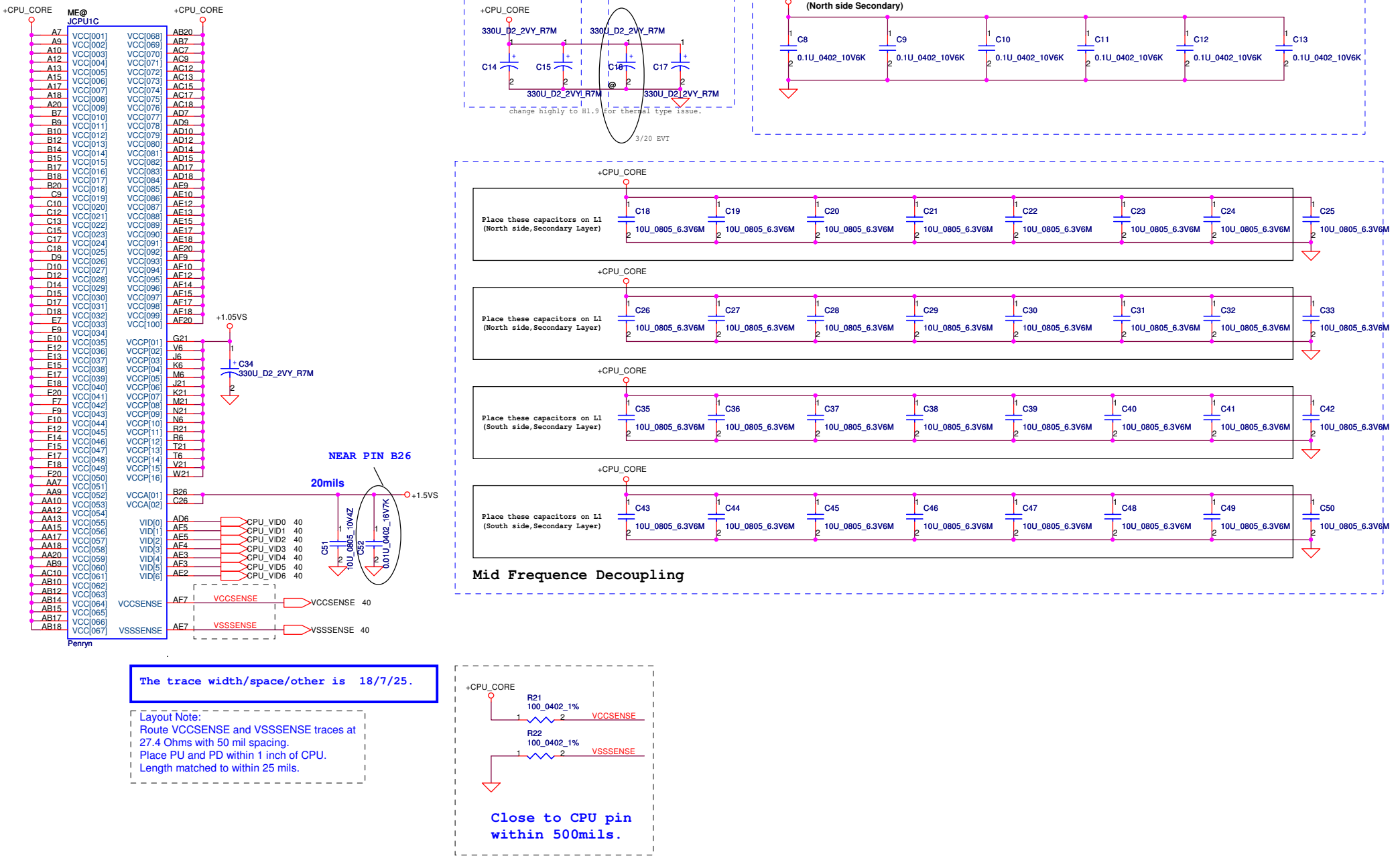
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Penryn (2/3)

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 5 of 43



The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

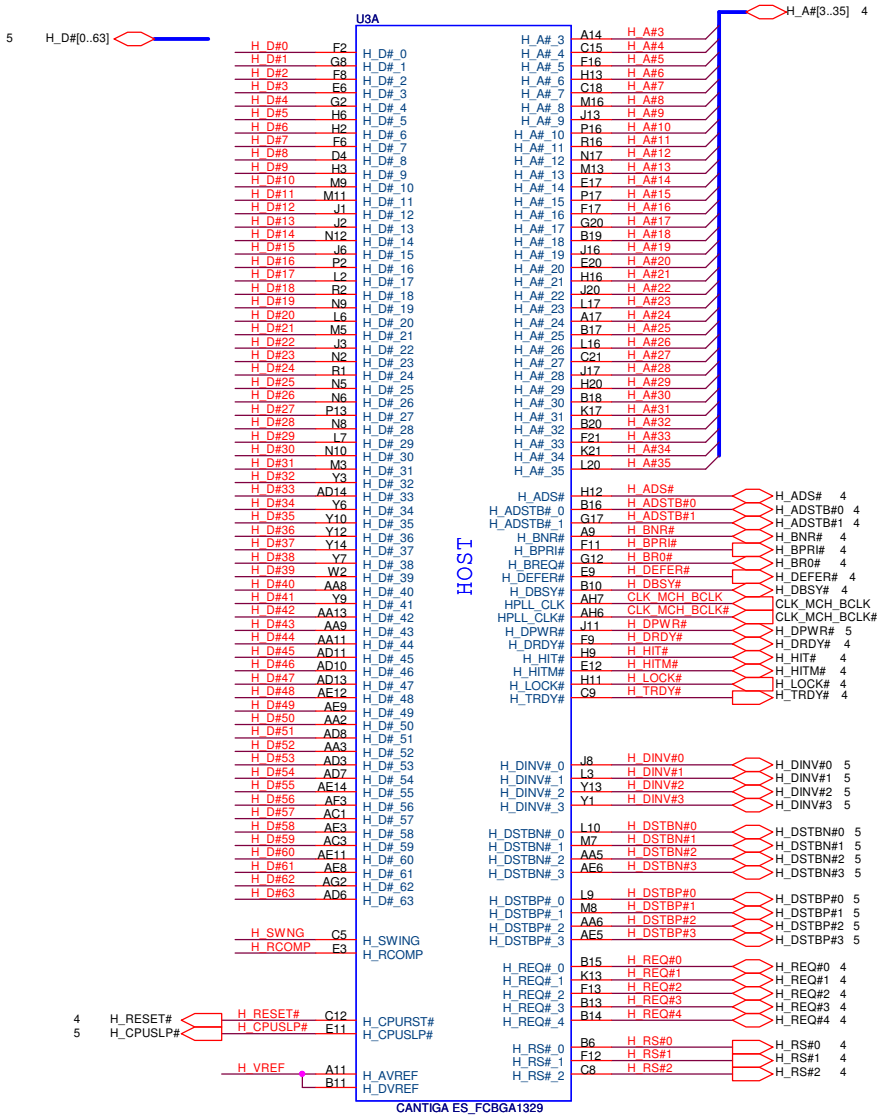
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

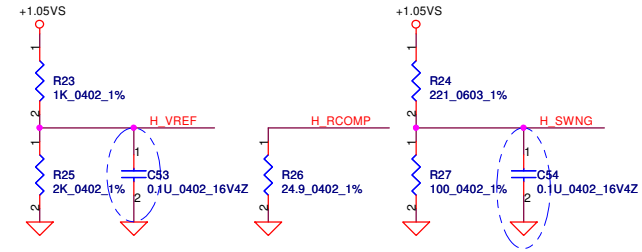
Title: Penryn (3/3)

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 6 of 43



Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20



within 100 mils from NB **Near B3 pin**

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Cantiga GMCH(1/6)-GTL

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 7 of 43

Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

U3B

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, AL34 RSVD10, AK34 RSVD11, AN35 RSVD12, AM35 RSVD13, T24 RSVD14, B31 RSVD15, B2 RSVD16, M1 RSVD17, AY21 RSVD20, BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

DDR CLK/ CONTROL/ COMPENSATION:
SA_CK_0 AP24 M_CLK_DDR0 → M_CLK_DDR0 14
SA_CK_1 AT21 M_CLK_DDR1 → M_CLK_DDR1 14
SB_CK_0 AY24 M_CLK_DDR2 → M_CLK_DDR2 15
SB_CK_1 AU20 M_CLK_DDR3 → M_CLK_DDR3 15
SA_CK#_0 AR24 M_CLK_DDR#0 → M_CLK_DDR#0 14
SA_CK#_1 AR21 M_CLK_DDR#1 → M_CLK_DDR#1 14
SB_CK#_0 AU24 M_CLK_DDR#2 → M_CLK_DDR#2 15
SB_CK#_1 AV20 M_CLK_DDR#3 → M_CLK_DDR#3 15
SA_CKE_0 BC28 DDR_CKE0_DIMMA → DDR_CKE0_DIMMA 14
SA_CKE_1 AY28 DDR_CKE1_DIMMA → DDR_CKE1_DIMMA 14
SB_CKE_0 AY36 DDR_CKE2_DIMMB → DDR_CKE2_DIMMB 15
SB_CKE_1 BB36 DDR_CKE3_DIMMB → DDR_CKE3_DIMMB 15
SA_CS#_0 BA17 DDR_CS0_DIMMA# → DDR_CS0_DIMMA# 14
SA_CS#_1 AY16 DDR_CS1_DIMMA# → DDR_CS1_DIMMA# 14
SB_CS#_0 AV16 DDR_CS2_DIMMB# → DDR_CS2_DIMMB# 15
SB_CS#_1 AR13 DDR_CS3_DIMMB# → DDR_CS3_DIMMB# 15
SA_ODT_0 BD17 M_ODT0 → M_ODT0 14
SA_ODT_1 AY17 M_ODT1 → M_ODT1 14
SB_ODT_O BF15 M_ODT2 → M_ODT2 15
SB_ODT_1 AY13 M_ODT3 → M_ODT3 15
SM_RCOMP BG22 SMRCOMP
SM_RCOMP# BH21 SMRCOMP# — R29 80.6_0402_1%
SM_RCOMP_VOH BF28 SMRCOMP_VOH
SM_RCOMP_VOL BH28 SMRCOMP_VOL — R30 0_0402_5% → 1.5V_PGOOD 39
SM_VREF AV42 +DDR_MCH_REF
SM_PWROK AR36 SM_PWROK — R31 @10K_0402_5%
SM_REXT BF17 SM_REXT — R32 499_0402_1%
SM_DRAMRST# BC36 SM_DRAMRST# → SM_DRAMRST# 14,15

For DDR3 : 1.5V power rail
For DDR2 : 1.8V power rail
+1.5V — R28 80.6_0402_1%
20mil
For Crestline: 20ohm
For Calero: 80.6ohm
For Cantiga: 80.6ohm
SM_DRAMRST# is only for DDR3.
DDR2 left it No Connect

CLK:
DPLL_REF_CLK B38 CLK_MCH_DREFCLK → CLK_MCH_DREFCLK 16
DPLL_REF_CLK# A38 CLK_MCH_DREFCLK# → CLK_MCH_DREFCLK# 16
DPLL_REF_SSCLK E41 MCH_CLKDREFSSC → MCH_CLKDREFSSC 16
DPLL_REF_SSCLK# F41 MCH_CLKDREFSSC# → MCH_CLKDREFSSC# 16
PEG_CLK F43 CLK_MCH_3GPLL → CLK_MCH_3GPLL 16
PEG_CLK# E43 CLK_MCH_3GPLL# → CLK_MCH_3GPLL# 16

DMI:
DMI_RXN_0 AE41 DMI_TXN0 → DMI_TXN0 21
DMI_RXN_1 AE37 DMI_TXN1 → DMI_TXN1 21
DMI_RXN_2 AE47 DMI_TXN2 → DMI_TXN2 21
DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN3 21
DMI_RXP_0 AE40 DMI_TXP0 → DMI_TXP0 21
DMI_RXP_1 AE38 DMI_TXP1 → DMI_TXP1 21
DMI_RXP_2 AE48 DMI_TXP2 → DMI_TXP2 21
DMI_RXP_3 AH40 DMI_TXP3 → DMI_TXP3 21
DMI_TXN_0 AE35 DMI_RXN0 → DMI_RXN0 21
DMI_TXN_1 AE43 DMI_RXN1 → DMI_RXN1 21
DMI_TXN_2 AE46 DMI_RXN2 → DMI_RXN2 21
DMI_TXN_3 AH42 DMI_RXN3 → DMI_RXN3 21
DMI_TXP_0 AD35 DMI_RXP0 → DMI_RXP0 21
DMI_TXP_1 AE44 DMI_RXP1 → DMI_RXP1 21
DMI_TXP_2 AF46 DMI_RXP2 → DMI_RXP2 21
DMI_TXP_3 AH43 DMI_RXP3 → DMI_RXP3 21

+1.5V — R34 1K_0402_1%
SMRCOMP_VOH — C55 0.01U_0402_25V7K — C56 2.2U_0603_6.3V4Z — R37 3.01K_0402_1%
SMRCOMP_VOL — C57 0.01U_0402_25V7K — C58 2.2U_0603_6.3V4Z — R43 1K_0402_1%

GRAPHICS VID:
GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 E33
GFX_VR_EN C34

For independent Power Rail : connect to PWM CORE VID
For Common Power Rail : left it No Connect
+1.05VS — R52 1K_0402_1% — C59 0.1U_0402_16V4Z — R55 499_0402_1%

ME:
CL_CLK AH37 CL_CLK0 → CL_CLK0 21
CL_DATA AH36 CL_DATA0 → CL_DATA0 21
CL_PWROK AN36 CL_PWROK → M_PWROK 21
CL_RST# AJ35 CL_RST# → CL_RST# 21
CL_VREF AH34 CL_VREF

For AMT function

MISC:
DDPC_CTRLCLK N28
DDPC_CTRLDATA M28 DP_DATA
SDVO_CTRLCLK G36 SDVO_SCLK
SDVO_CTRLDATA E36
CLKREQ# K36 MCH_CLKREQ# → MCH_CLKREQ# 16
ICH_SYNC# H36 MCH_ICH_SYNC# → MCH_ICH_SYNC# 21
TSATN# B12 MCH_TSATN# — R57 56_0402_5% → +1.05VS

HDA:
HDA_BCLK B28
HDA_RST# B30
HDA_SDI B29
HDA_SDO C29
HDA_SYNC A28

Notice: Please check HDA power rail to select HDA controller.

CFG:
16 MCH_CLKSEL0 → MCH_CLKSEL0 T25 → CFG_0
16 MCH_CLKSEL1 → MCH_CLKSEL1 R25 → CFG_1
16 MCH_CLKSEL2 → MCH_CLKSEL2 P25 → CFG_2
CFG_3 P20, CFG_4 P24, CFG_5 C25, CFG_6 N24, CFG_7 M24, CFG_8 E21, CFG_9 C23, CFG_10 C24, CFG_11 N21, CFG_12 P21, CFG_13 T21, CFG_14 R20, CFG_15 M20, CFG_16 L21, CFG_17 H21, CFG_18 P29, CFG_19 R28, CFG_20 T28

+1.05VS — R33 1K_0402_5% @ — R35 54.9_0402_1% @ — Q1 MMBT3904_SOT23-3 @ — +3VS — R36 1K_0402_5% @ — MCH_TSATN# — MCH_TSATN_EC#

R38 @2.21K_0402_1% MCH_CFG_5
R39 @2.21K_0402_1% MCH_CFG_6
R40 @2.21K_0402_1% MCH_CFG_7
R41 @2.21K_0402_1% MCH_CFG_9
R42 @2.21K_0402_1% MCH_CFG_10
R44 @2.21K_0402_1% MCH_CFG_12
R45 @2.21K_0402_1% MCH_CFG_13
R46 @2.21K_0402_1% MCH_CFG_16
R49 @4.02K_0402_1% MCH_CFG_19
R50 @4.02K_0402_1% MCH_CFG_20

+3VS — R47 10K_0402_5% — R48 10K_0402_5% — PM_EXTTS#0 — PM_EXTTS#1

21 ICH_POK — R51 0_0402_5% — PM_POK_R
21,40 VGATE — R53 @0_0402_5%
19,24,29 PLT_RST# — R54 100_0402_5% — PLT_RST#_R

PM:
21 PM_BMBUSY# → PM_BMBUSY# R29
5,20,40 H_DPRSTP# → H_DPRSTP# B7 → PM_SYNC#
14,15 PM_EXTTS#0 → PM_EXTTS#0 N33 → PM_DPRSTP#
PM_EXTTS#1 P32 → PM_EXT_TS#_0
PM_POK_R AT40 → PM_EXT_TS#_1
PLT_RST#_R AT11 → PWROK
4,20 H_THERMTRIP# → H_THERMTRIP# T20 → RSTIN#
21,40 DPRSLPVR → DPRSLPVR R32 → THERMTRIP#
DPRSLPVR

NC:
NC_1 BG48, NC_2 BF48, NC_3 BD48, NC_4 BC48, NC_5 BH47, NC_6 BG47, NC_7 BF47, NC_8 BH46, NC_9 BF46, NC_10 BG45, NC_11 BH44, NC_12 BH43, NC_13 BH6, NC_14 BH5, NC_15 BG4, NC_16 BH3, NC_17 BF3, NC_18 BH2, NC_19 BG2, NC_20 BF2, NC_21 BG1, NC_22 BF1, NC_23 BD1, NC_24 BC1, NC_25 F1, NC_26 A47

CANTIGA ES_FCBGA1329

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled (Default) 1 = Digital display (iHDMI/DP) interface enabled

+3VS — SDVO_SCLK — R56 @ 2.2K_0402_5%

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20. CLOSE TO PIN.AV21

+1.5V — R58 10K_0402_5% — +DDR_MCH_REF — C61 0.1U_0402_16V4Z — R64 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Cantiga(2/7)-DMI/DDR/STRP

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 8 of 43

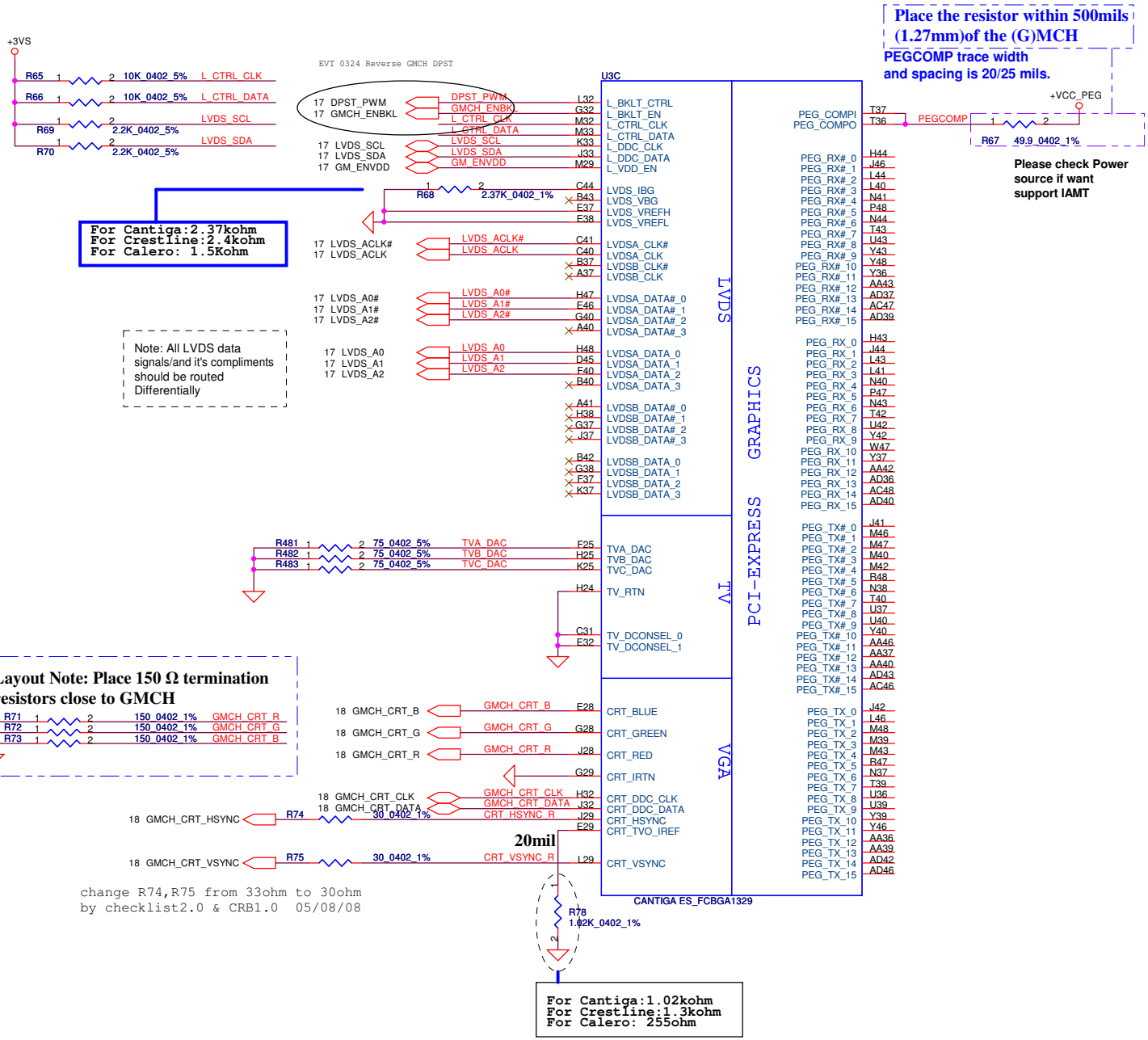
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 9 of 43



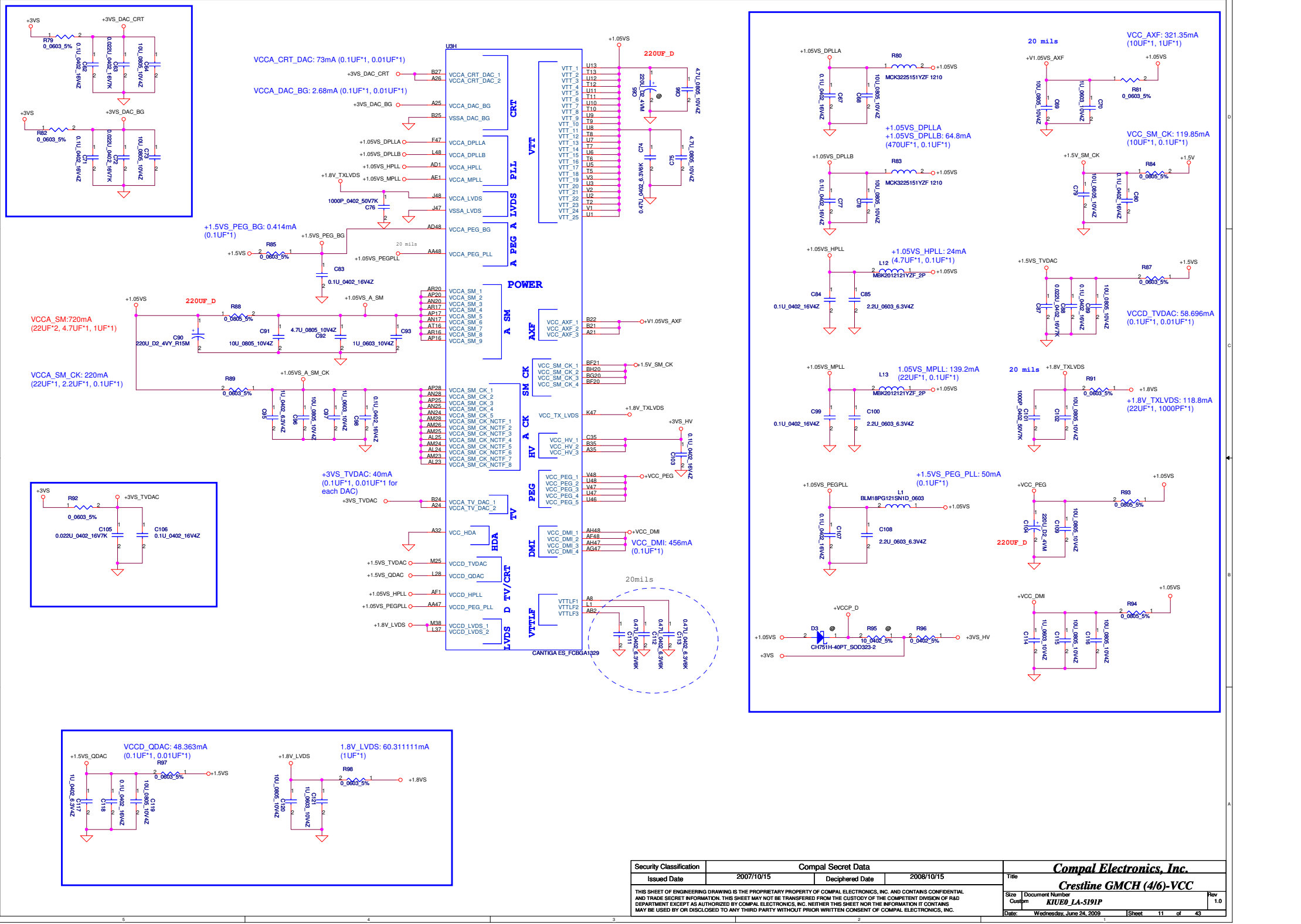
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: Cantiga(3/6)-VGA/LVDS/TV

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 10 of 43


VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
VCCA_SM:720mA (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCC_DMI: 456mA (0.1UF*1)
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
1.8V_LVDS: 60.311111mA (1UF*1)
+1.05VS_DPLLA +1.05VS_DPLLB: 64.8mA (470UF*1, 0.1UF*1)
+1.05VS_HPLL: 24mA (4.7UF*1, 0.1UF*1)
1.05VS_MPLL: 139.2mA (22UF*1, 0.1UF*1)
+1.5VS_PEG_PLL: 50mA (0.1UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
+1.8V_TXLVDS: 118.8mA (22UF*1, 1000PF*1)
U3H
CRT
PLL
LVDS
PEG
POWER
SM
AXF
SM CK
HV
PEG
TV
HDA
DMI
D TV/CRT
VTTLF
LVDS
VTT
CANTIGA ES_FCBGA1329
20mils
20 mils
MCK3225151YZF 1210
MBK2012121YZF_2P
BLM18PG121SN1D_0603
CH751H-40PT_SOD323-2
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
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Compal Electronics, Inc.
Title
Crestline GMCH (4/6)-VCC
Size
Custom
Document Number
KIUE0_LA-5191P
Rev
1.0
Date:
Wednesday, June 24, 2009
Sheet
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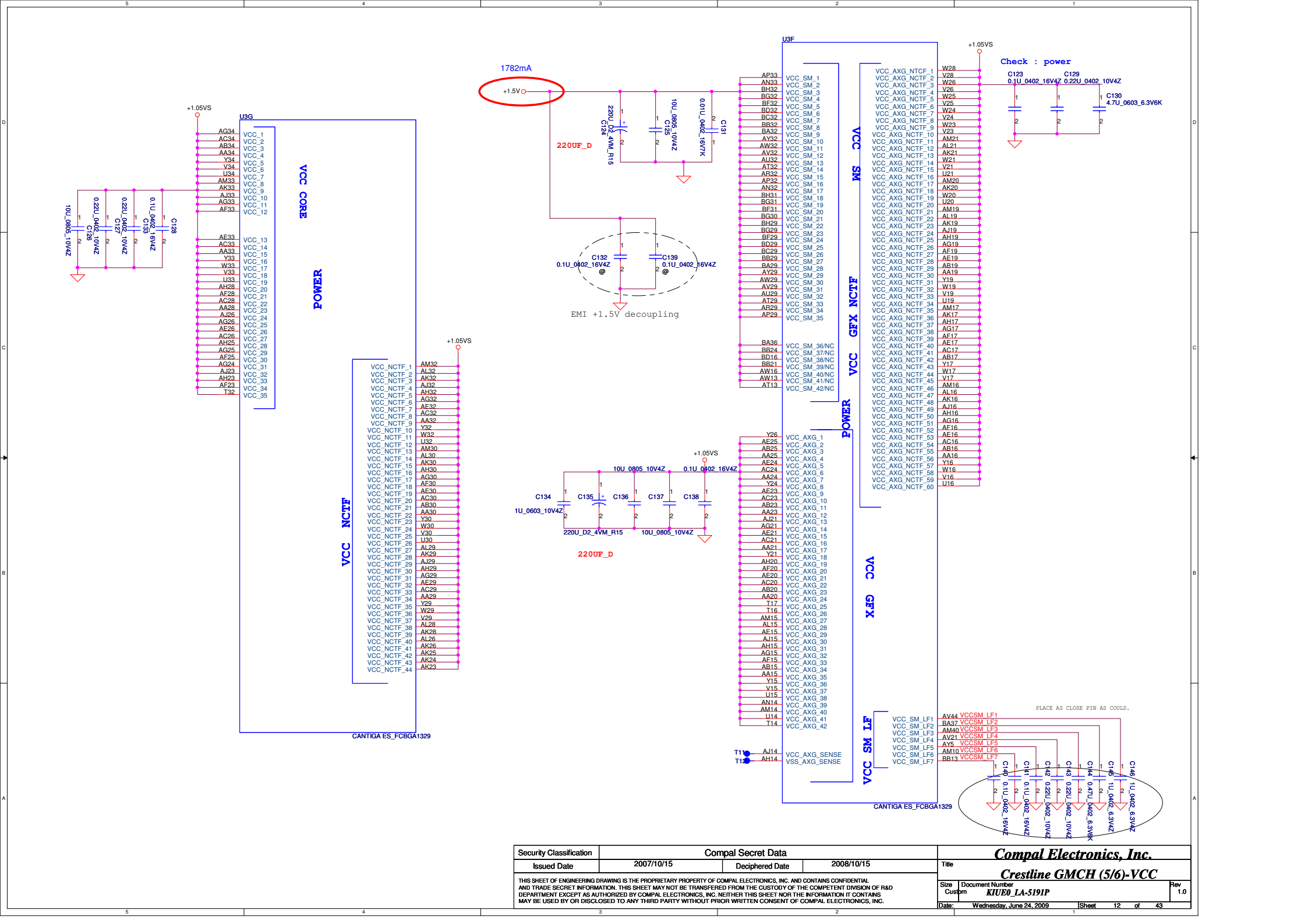
of
43



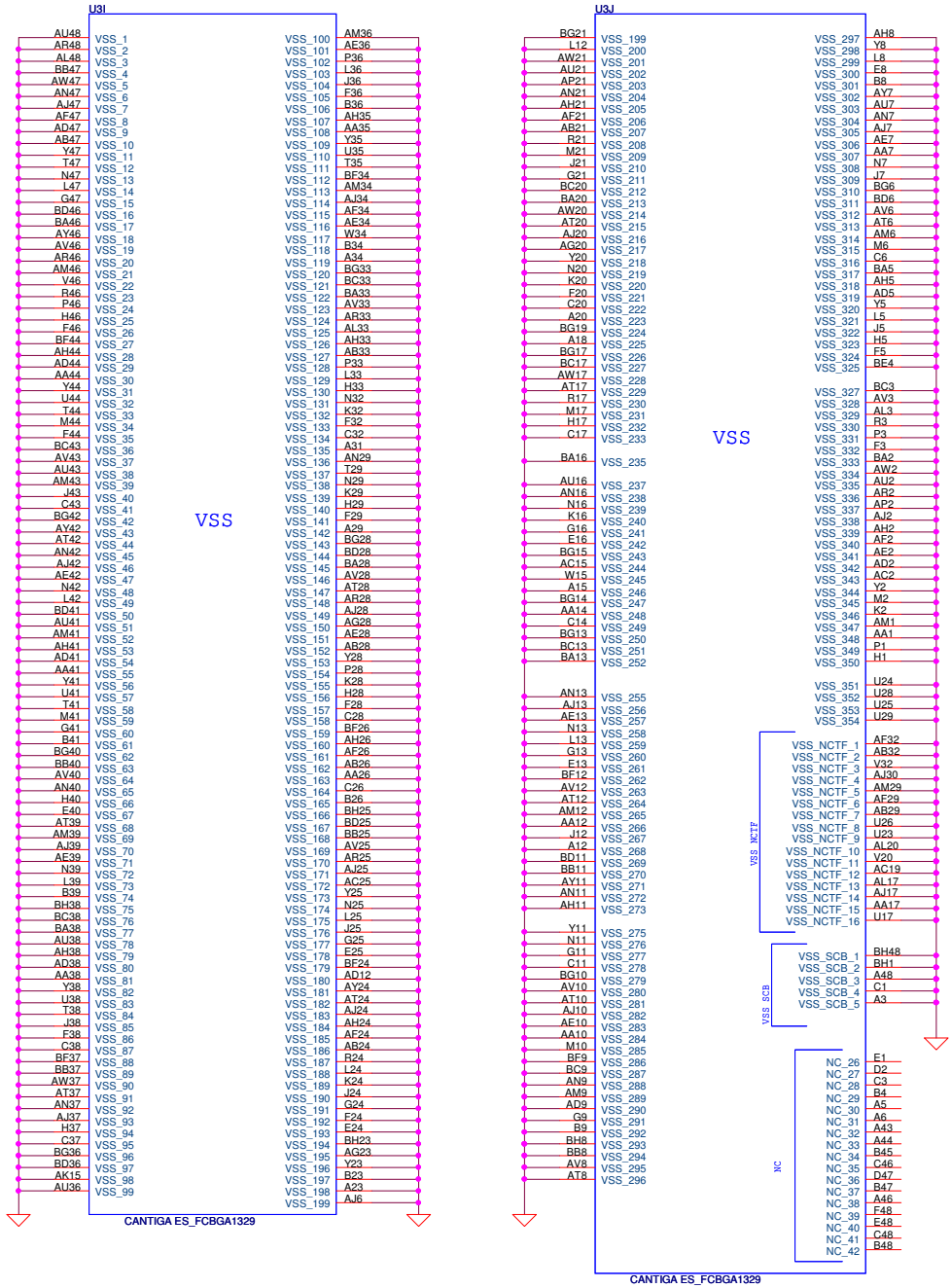
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 12 of 43



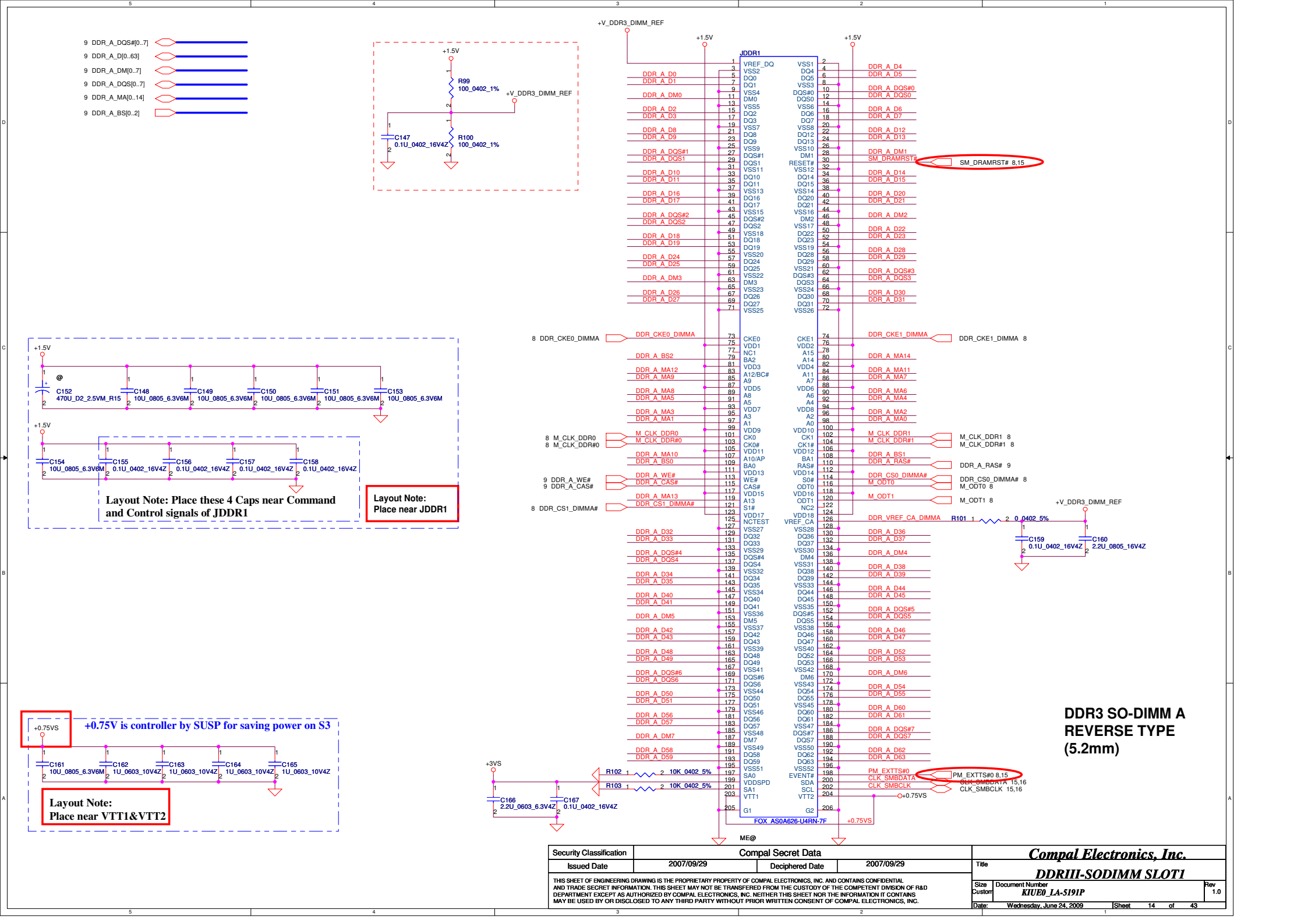
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Cantiga GMCH (6/6)-GND

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 13 of 43


9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]
9 DDR_A_BS[0..2]
+1.5V
R99
100_0402_1%
+V_DDR3_DIMM_REF
C147
0.1U_0402_16V4Z
R100
100_0402_1%
+V_DDR3_DIMM_REF
JDDR1
DDR_A_D0
DDR_A_D1
DDR_A_DM0
DDR_A_D2
DDR_A_D3
DDR_A_D8
DDR_A_D9
DDR_A_DQS#1
DDR_A_DQS1
DDR_A_D10
DDR_A_D11
DDR_A_D16
DDR_A_D17
DDR_A_DQS#2
DDR_A_DQS2
DDR_A_D18
DDR_A_D19
DDR_A_D24
DDR_A_D25
DDR_A_DM3
DDR_A_D26
DDR_A_D27
DDR_A_D4
DDR_A_D5
DDR_A_DQS#0
DDR_A_DQS0
DDR_A_D6
DDR_A_D7
DDR_A_D12
DDR_A_D13
DDR_A_DM1
SM_DRAMRST#
DDR_A_D14
DDR_A_D15
DDR_A_D20
DDR_A_D21
DDR_A_DM2
DDR_A_D22
DDR_A_D23
DDR_A_D28
DDR_A_D29
DDR_A_DQS#3
DDR_A_DQS3
DDR_A_D30
DDR_A_D31
SM_DRAMRST# 8,15
8 DDR_CKE0_DIMMA
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
DDR_CKE1_DIMMA 8
DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
8 M_CLK_DDR0
8 M_CLK_DDR#0
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_CLK_DDR1 8
M_CLK_DDR#1 8
DDR_A_MA10
DDR_A_BS0
DDR_A_BS1
DDR_A_RAS#
DDR_A_RAS# 9
9 DDR_A_WE#
9 DDR_A_CAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
M_ODT0
DDR_CS0_DIMMA# 8
M_ODT0 8
DDR_A_MA13
DDR_CS1_DIMMA#
M_ODT1
M_ODT1 8
8 DDR_CS1_DIMMA#
DDR_VREF_CA_DIMMA
R101
0_0402_5%
+V_DDR3_DIMM_REF
C159
0.1U_0402_16V4Z
C160
2.2U_0805_16V4Z
DDR_A_D32
DDR_A_D33
DDR_A_DQS#4
DDR_A_DQS4
DDR_A_D34
DDR_A_D35
DDR_A_D40
DDR_A_D41
DDR_A_DM5
DDR_A_D42
DDR_A_D43
DDR_A_D48
DDR_A_D49
DDR_A_DQS#6
DDR_A_DQS6
DDR_A_D50
DDR_A_D51
DDR_A_D56
DDR_A_D57
DDR_A_DM7
DDR_A_D58
DDR_A_D59
DDR_A_D36
DDR_A_D37
DDR_A_DM4
DDR_A_D38
DDR_A_D39
DDR_A_D44
DDR_A_D45
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D46
DDR_A_D47
DDR_A_D52
DDR_A_D53
DDR_A_DM6
DDR_A_D54
DDR_A_D55
DDR_A_D60
DDR_A_D61
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
PM_EXTTS#0
CLK_SMBDATA
CLK_SMBCLK
PM_EXTTS#0 8,15
CLK_SMBDATA 15,16
CLK_SMBCLK 15,16
+0.75VS
+3VS
R102
10K_0402_5%
R103
10K_0402_5%
C166
2.2U_0603_6.3V4Z
C167
0.1U_0402_16V4Z
FOX_AS0A626-U4RN-7F
ME@
+1.5V
C152
470U_D2_2.5VM_R15
C148
10U_0805_6.3V6M
C149
10U_0805_6.3V6M
C150
10U_0805_6.3V6M
C151
10U_0805_6.3V6M
C153
10U_0805_6.3V6M
C154
10U_0805_6.3V6M
C155
0.1U_0402_16V4Z
C156
0.1U_0402_16V4Z
C157
0.1U_0402_16V4Z
C158
0.1U_0402_16V4Z
Layout Note: Place these 4 Caps near Command and Control signals of JDDR1
Layout Note: Place near JDDR1
+0.75VS
+0.75VS is controller by SUSP for saving power on S3
C161
10U_0805_6.3V6M
C162
1U_0603_10V4Z
C163
1U_0603_10V4Z
C164
1U_0603_10V4Z
C165
1U_0603_10V4Z
Layout Note: Place near VTT1&VTT2
DDR3 SO-DIMM A
REVERSE TYPE
(5.2mm)
Security Classification
Compal Secret Data
Issued Date
2007/09/29
Deciphered Date
2007/09/29
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Compal Electronics, Inc.
Title
DDRIII-SODIMM SLOT1
Size
Custom
Document Number
KIUE0_LA-5191P
Rev
1.0
Date:
Wednesday, June 24, 2009
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of
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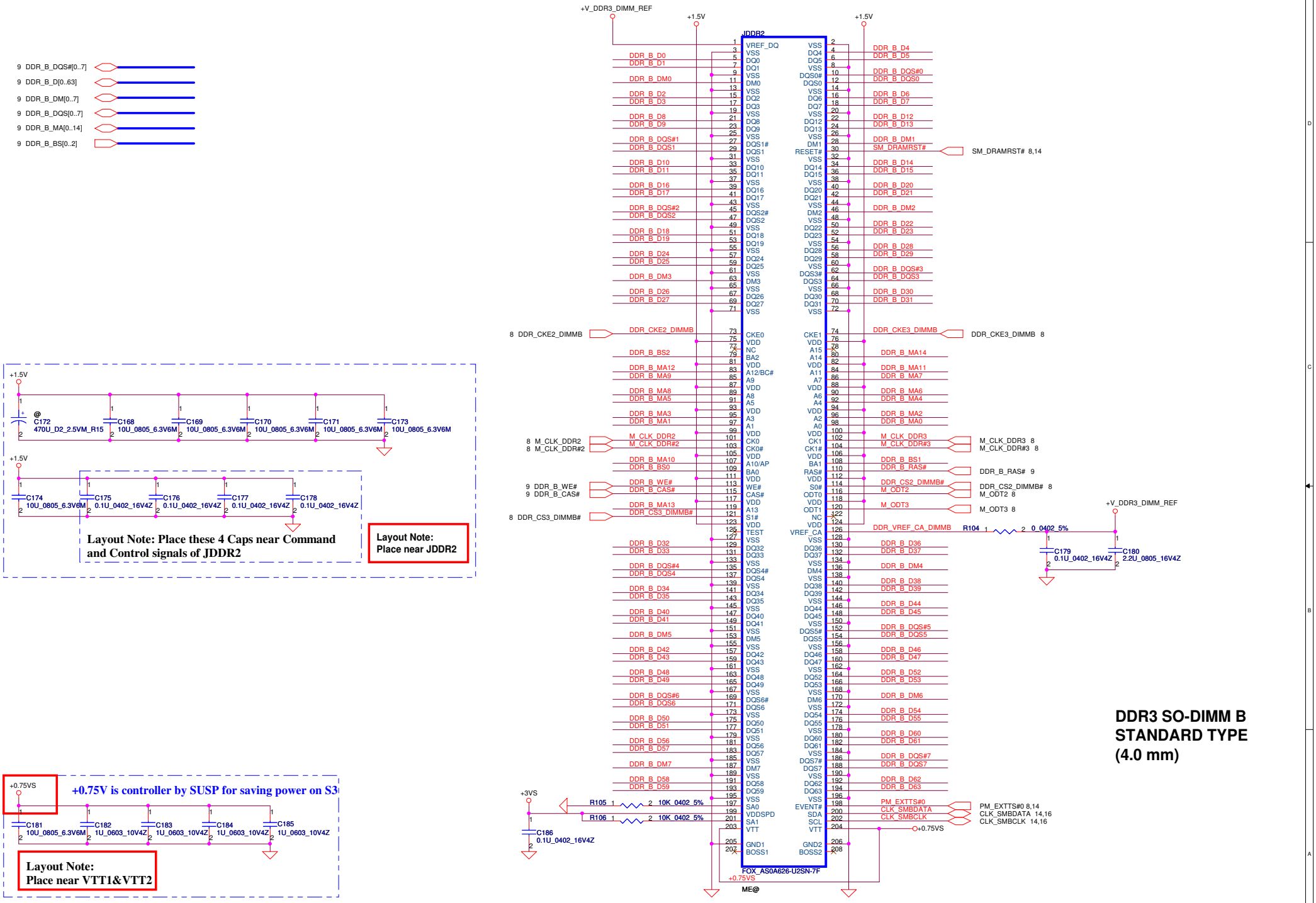


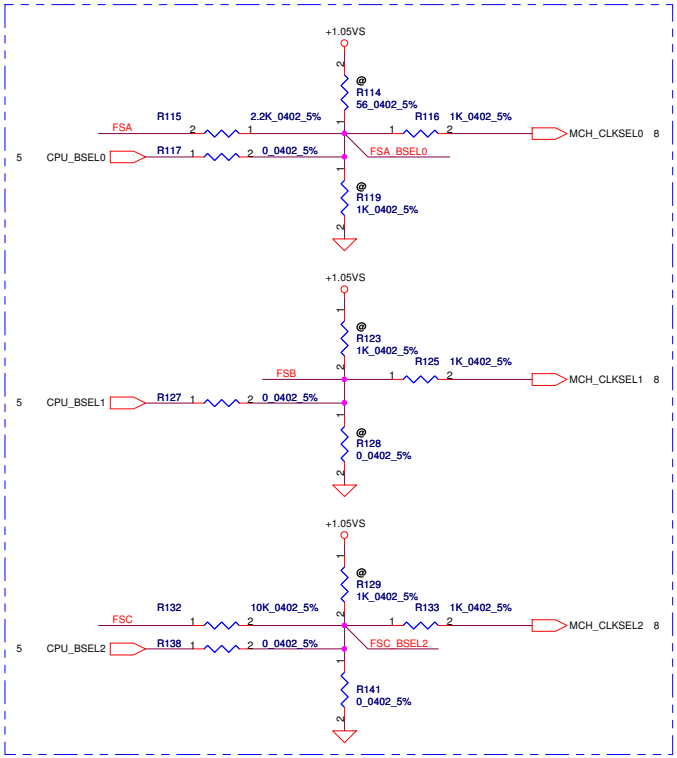
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

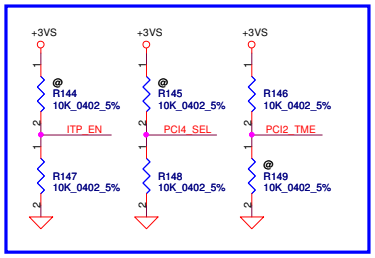
Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009	Sheet 15 of 43		

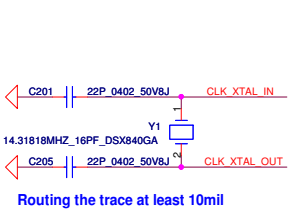
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

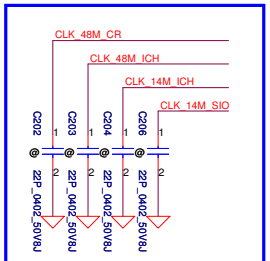
SA000020H00 (ICS : ICS9LPRS387AKLFT)







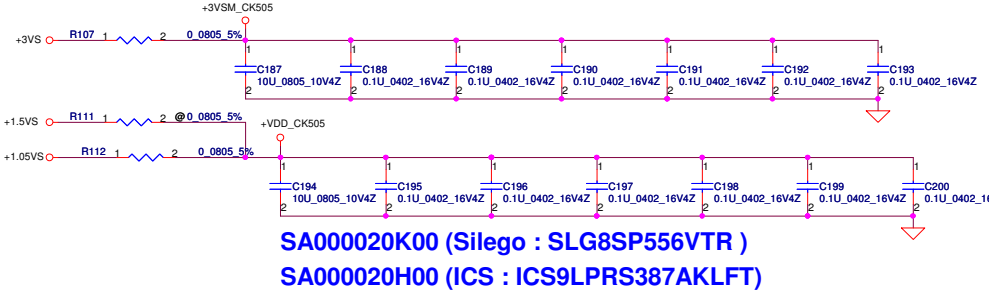
Routing the trace at least 10mil

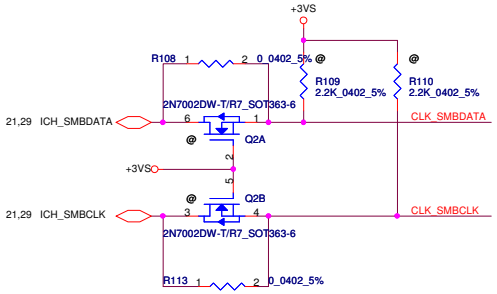


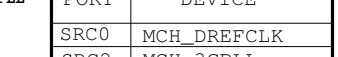
place CAPs near Resistors of U10
For 3G RF noise .

For ITP_EN, 0 =SRC8/SRC8#(100MHz); 1 = ITP/ITP#(266MHz)

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#(UMA)
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS(DISCRETE)







SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

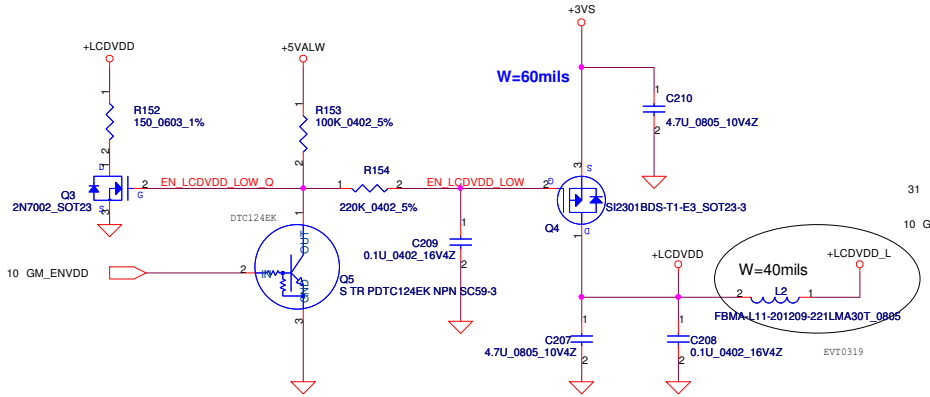
Compal Electronics,Ltd.

Title: Clock Generator CK505

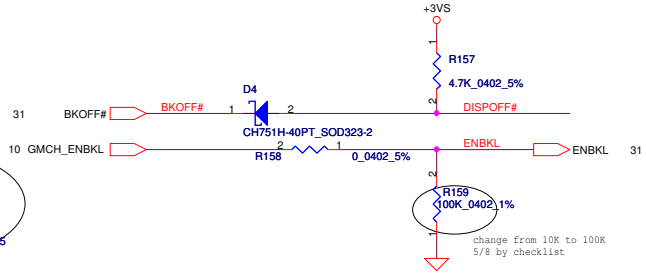
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

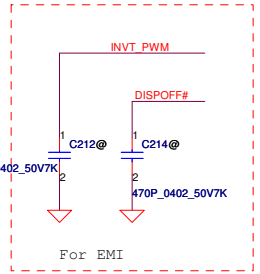
Date: Wednesday, June 24, 2009 | Sheet 16 of 43

LCD POWER CIRCUIT

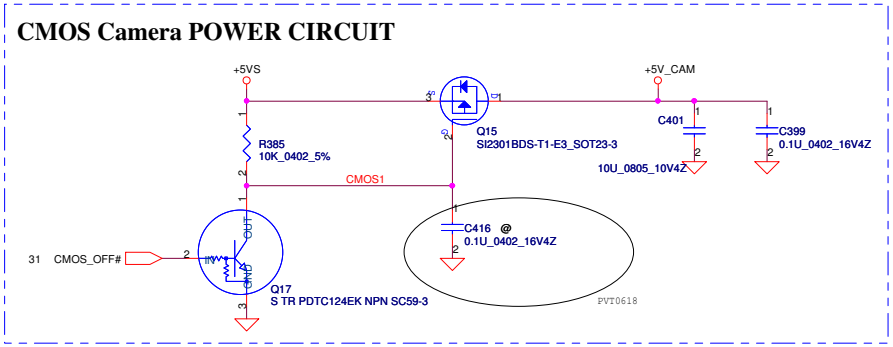


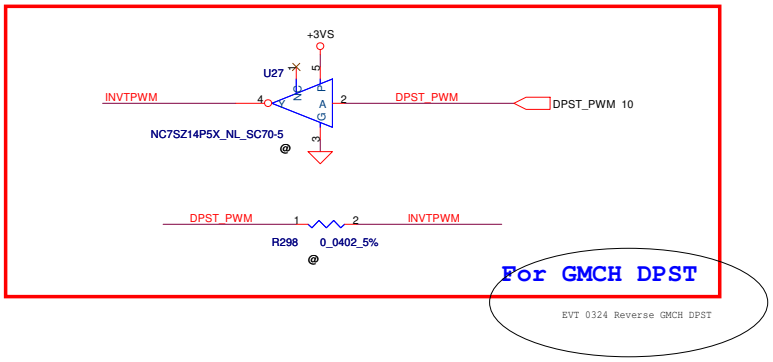
PANEL Logic Power 250mA (typ 3.15v)



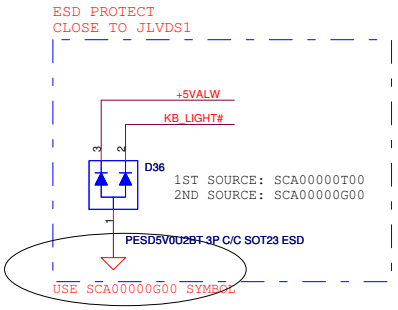


CMOS Camera POWER CIRCUIT





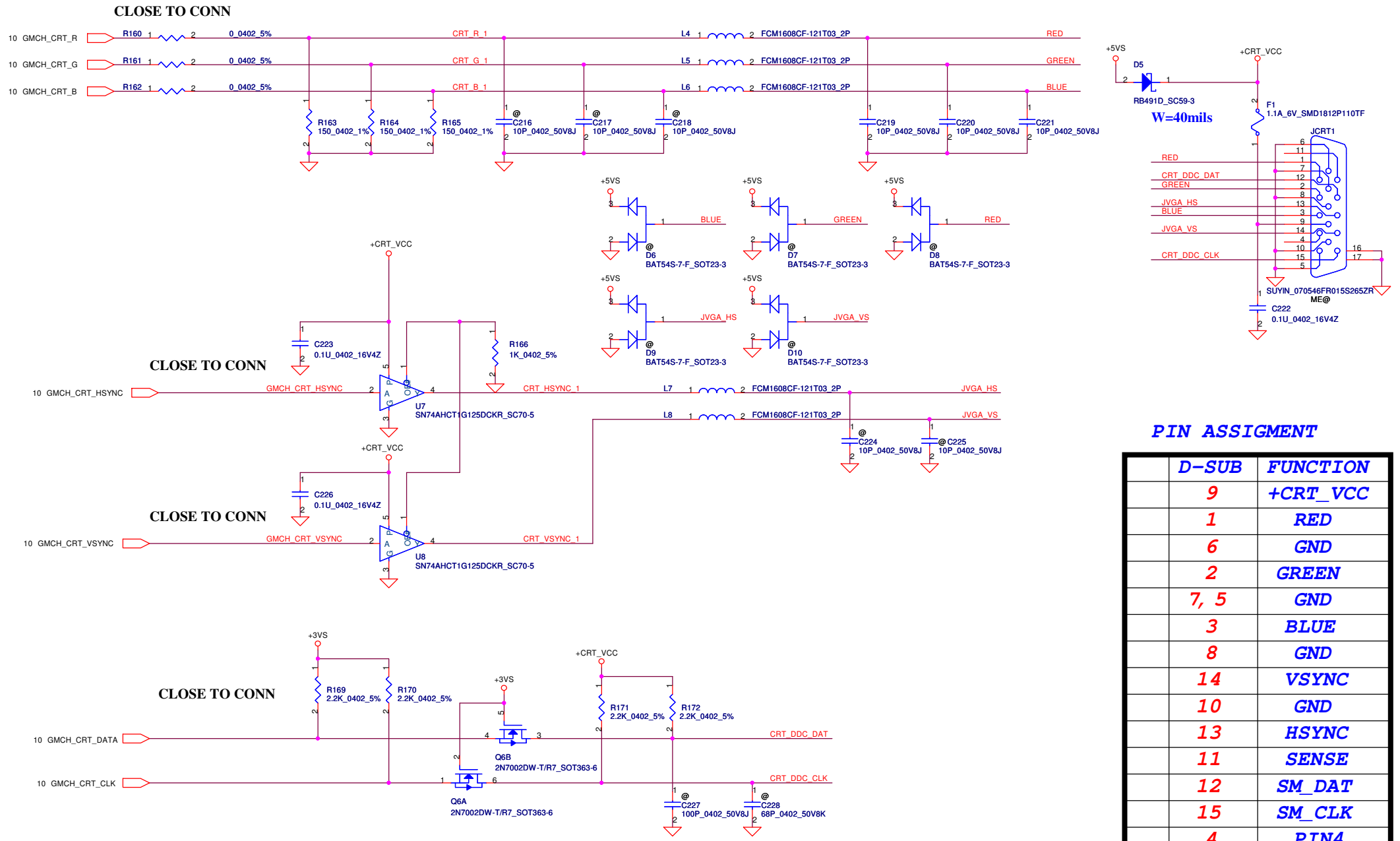
COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LVDS & DVI Connector		
Size B	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009	Sheet 17 of 43		

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

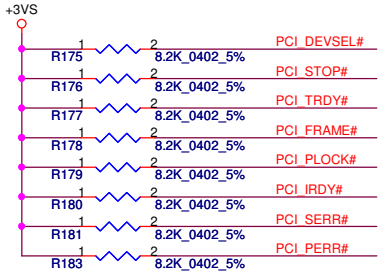
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

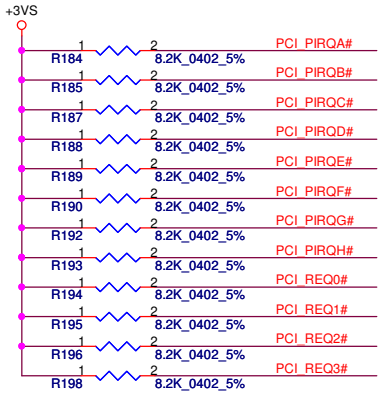
Compal Electronics, Inc.

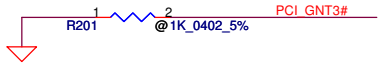
Title: CRT & TV-OUT Connector

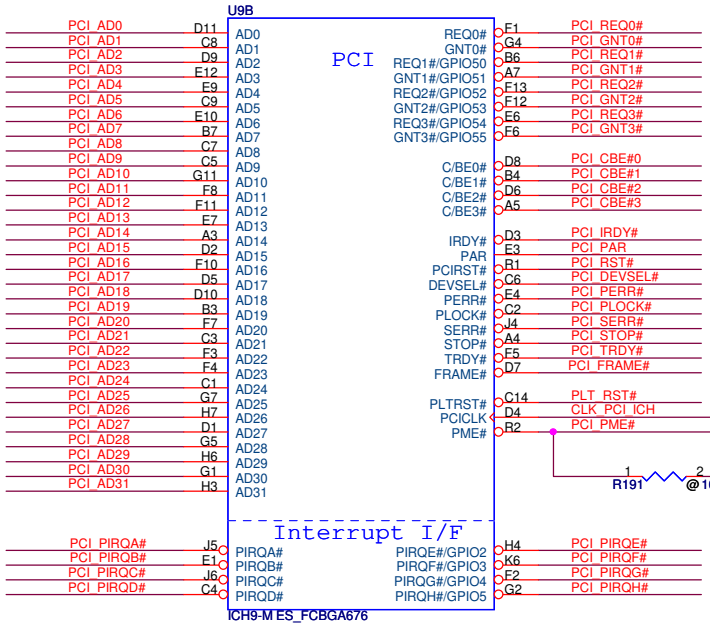
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

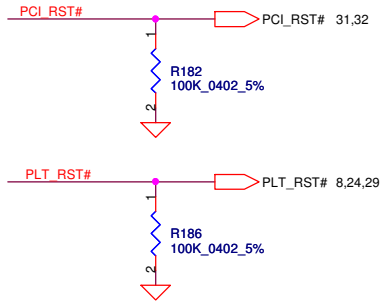
Date: Wednesday, June 24, 2009 | Sheet 18 of 43

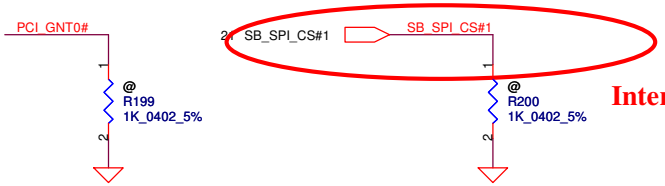


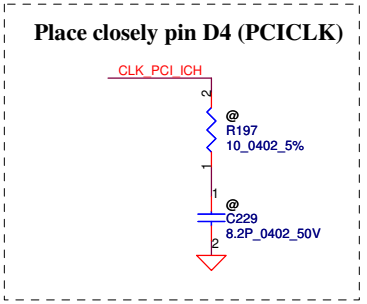










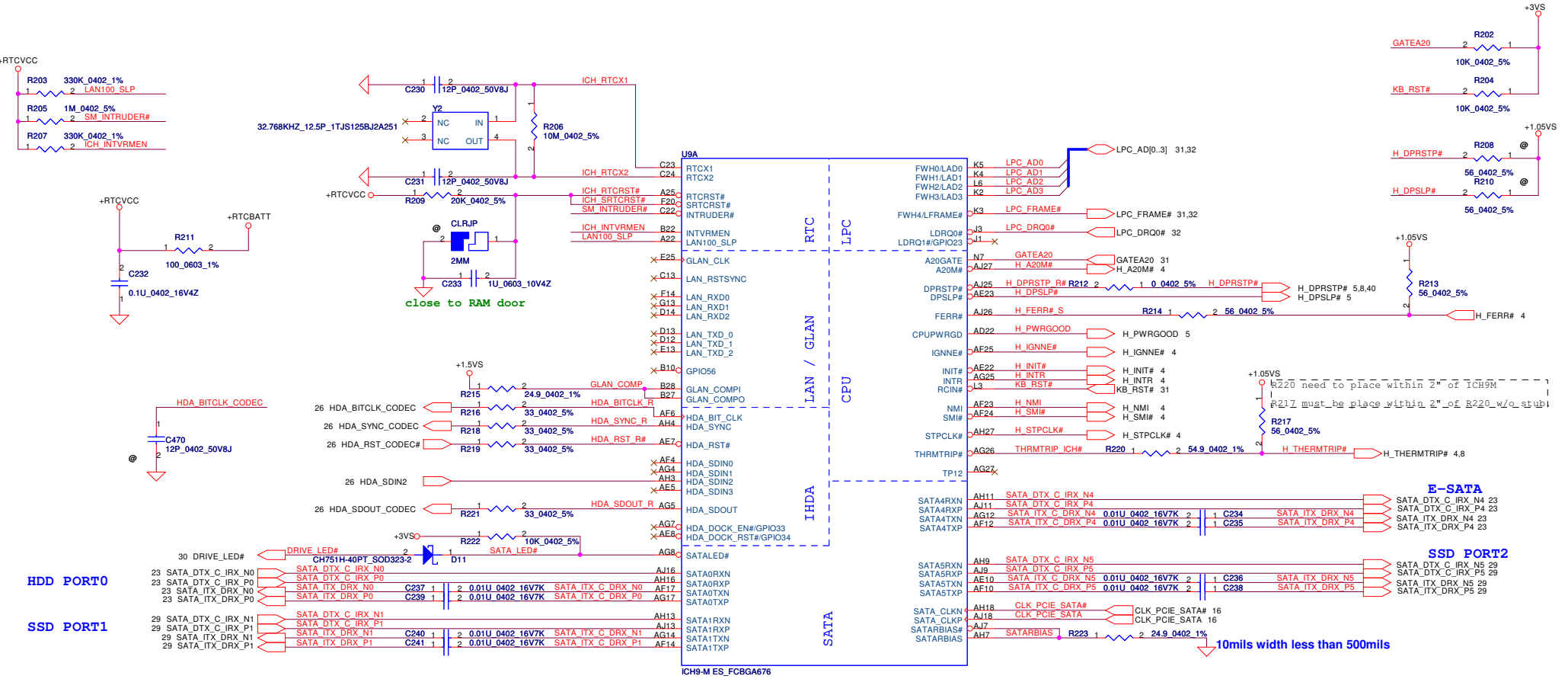


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(1/4)-PCI		
Size	Document Number		Rev
	KIUE0_LA-5191P		1.0
Date:	Wednesday, June 24, 2009	Sheet	19 of 43



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

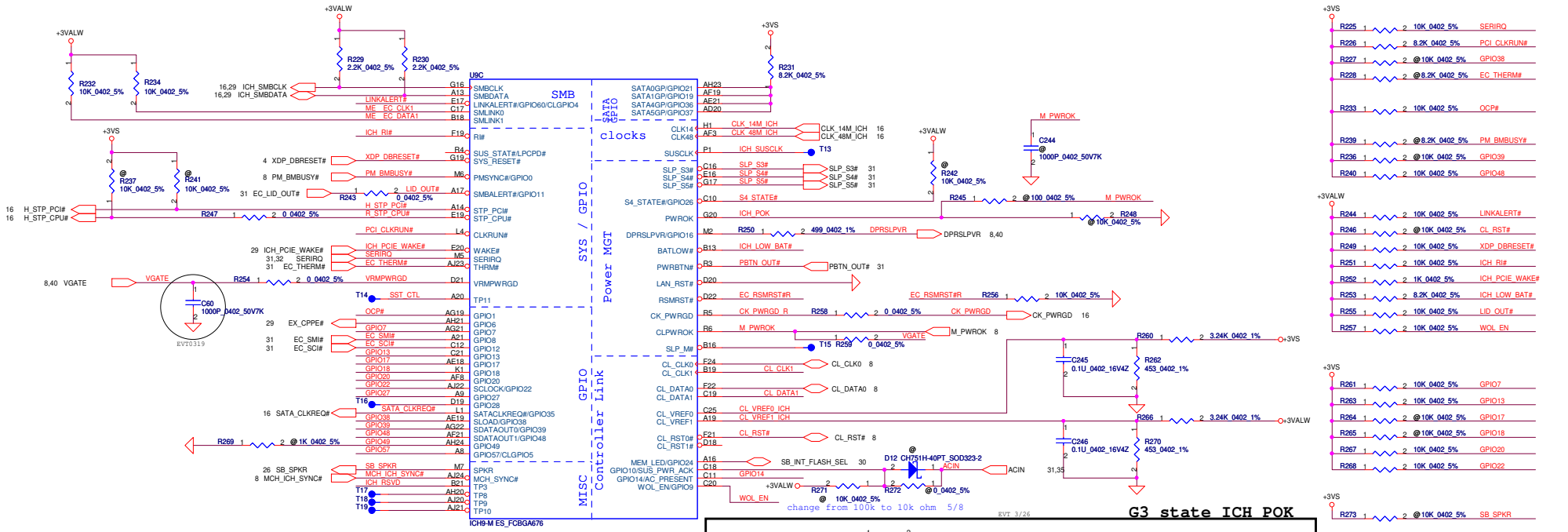
SATA PORT LIST	
PORT	DEVICE
0	HDD
1	Mini-Card SSD PORT1
4	E-SATA
5	Mini-Card SSD PORT2

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 20 of 43



USB PORT LIST

PORT	DEVICE
0	RIGHT USB
1	
2	CMOS
3	3G
4	LEFT USB/ESATA
5	
6	BT
7	CARD READER
8	WIRELESS
9	Finger Print
10	NEW CARD
11	RIGHT USB CONN

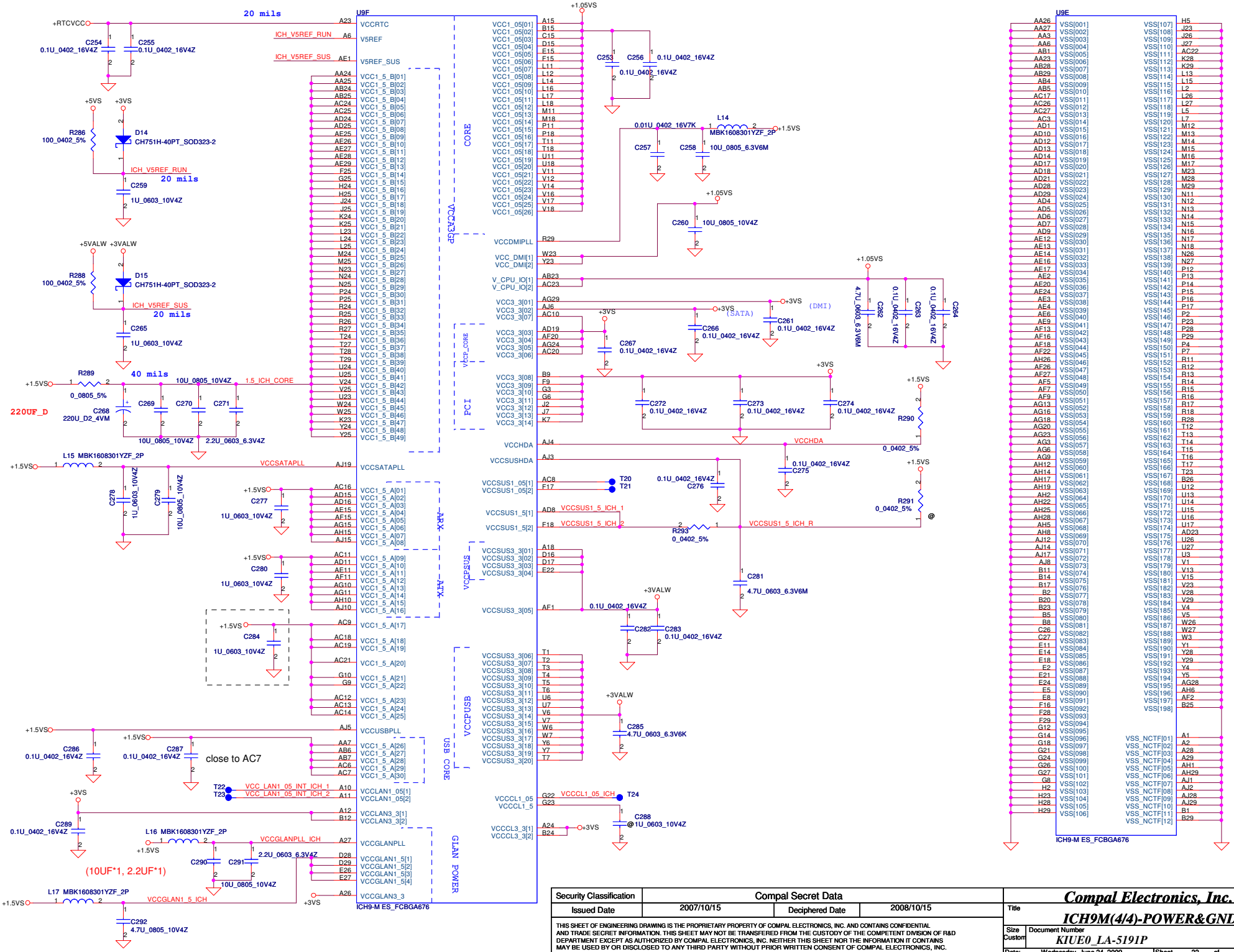
PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	
3	WLAN
4	
5	
6	LAN

EHCI#1	USB_OC#1	PORT0	PORT1
	USB_OC#2	PORT2	PORT3
	USB_OC#3	PORT4	PORT5
EHCI#2	USB_OC#4	PORT6	PORT7
	USB_OC#5	PORT8	PORT9
	USB_OC#6	PORT10	PORT11

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

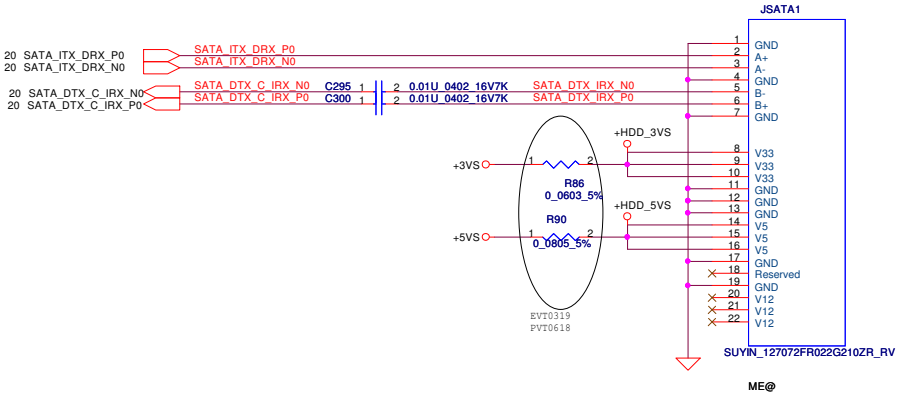
Compal Electronics, Inc.			
Title	ICH9M(3/4)-USB,GPIO,PCIE		
Size C	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009	Sheet 21 of 43		

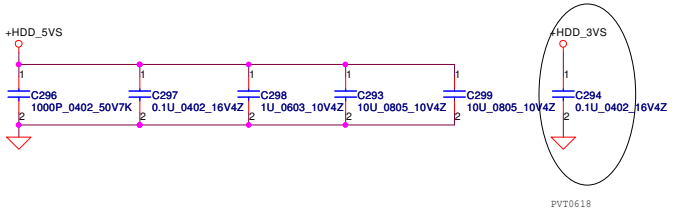


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

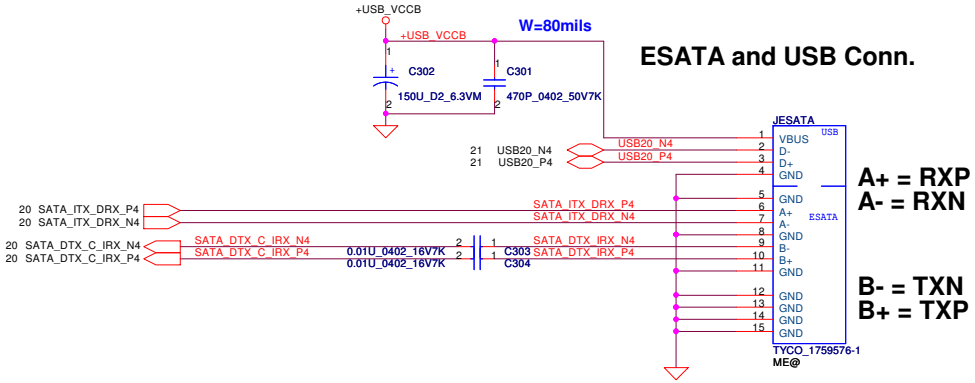
Compal Electronics, Inc.			
Title	ICH9M(4/4)-POWER&GND		
Size: Custom	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 22 of 43		

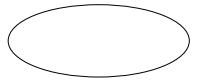
SATA HDD Conn.



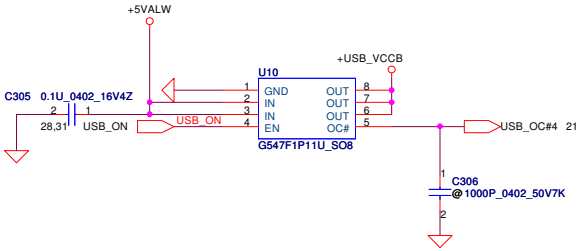


ESATA and USB Conn.



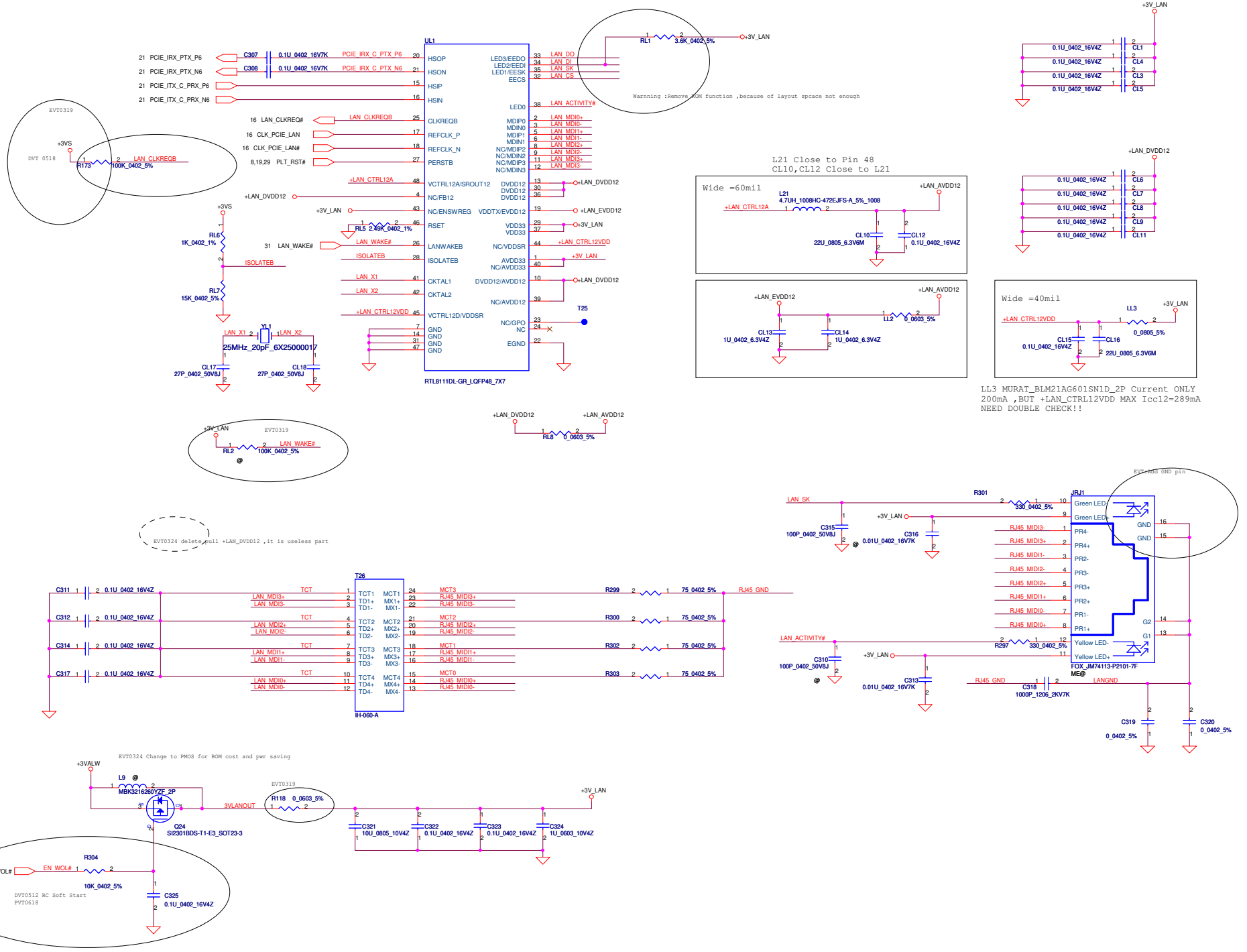


3/26 Remove ESD Diode ,by AndyYL



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 23 of 43		



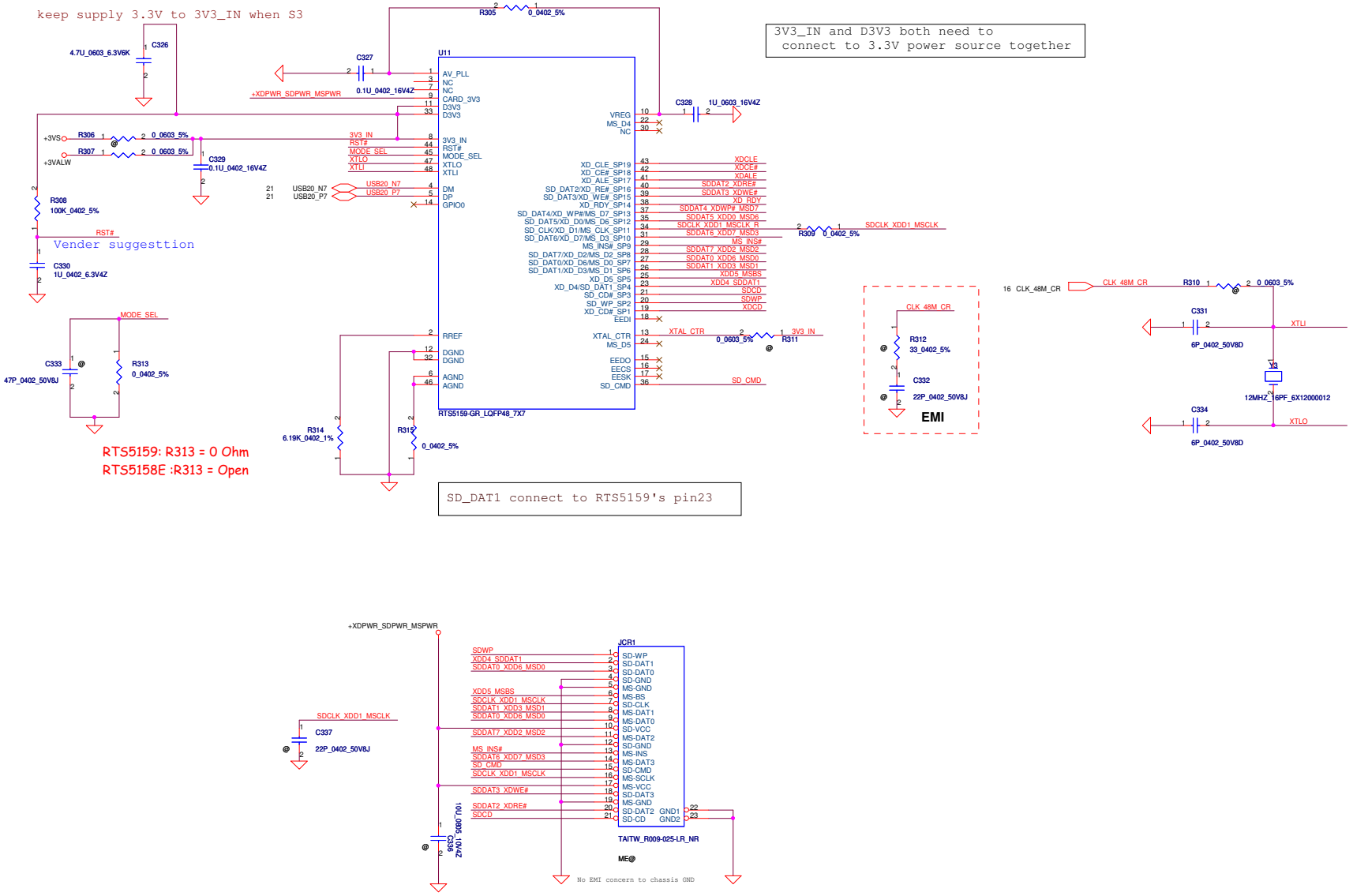
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: RTL8111DL-GR_LQFP48_7X7

Size	Document Number	Rev
C	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 24 of 43



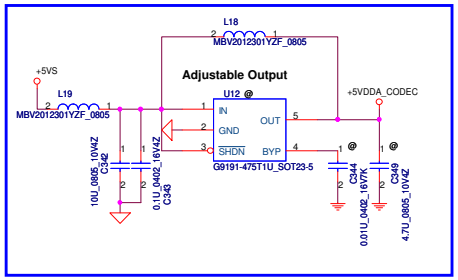
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

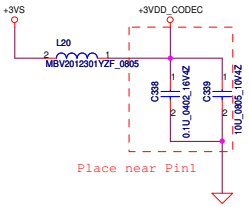
Compal Electronics,Ltd.

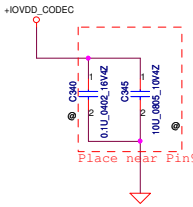
Title: RTS5159-VCC-GRT CARD READER

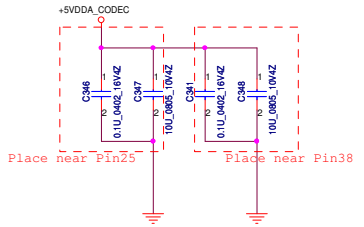
Size	Document Number	Rev
C	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 25 of 43

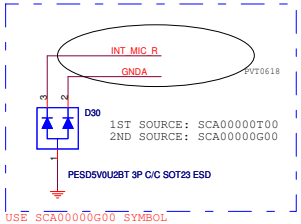




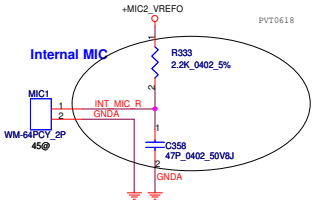


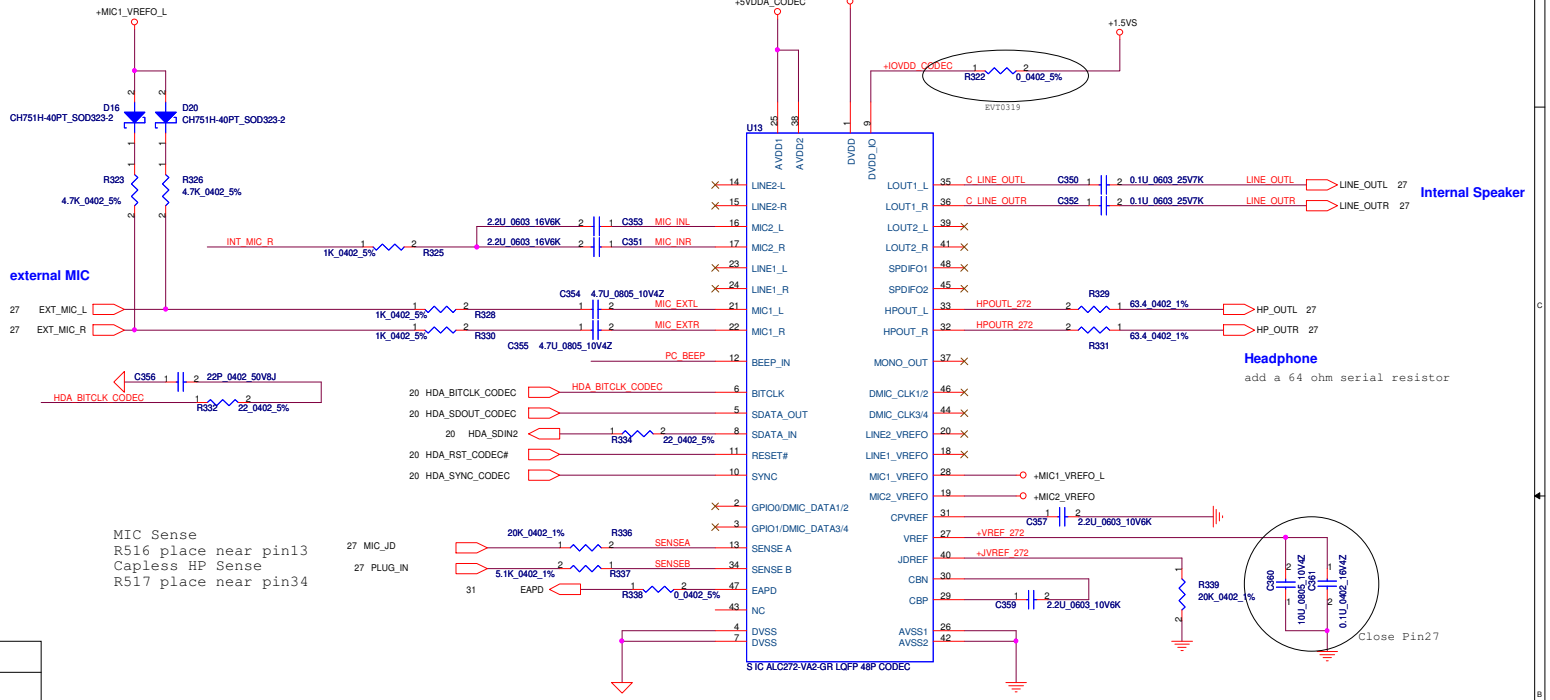


ESD PROTECT
CLOSE TO MIC1



USE SCA00000G00 SYMBOL

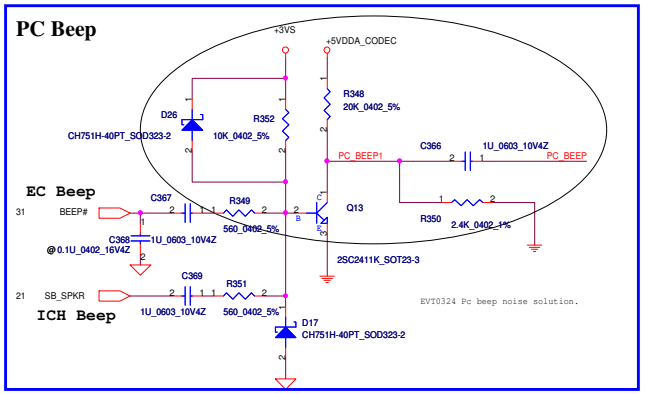


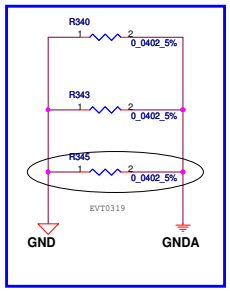


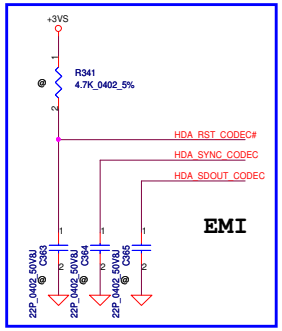
MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

27 MIC_JD
27 PLUG_IN
20K_0402_1% R336
5.1K_0402_1% R337
R338 0_0402_5%
SENSEA
SENSEB
EAPD

Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	NOT USE
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	NOT USE
MIC2(Pin16/17)	Internal	Internal Mic







Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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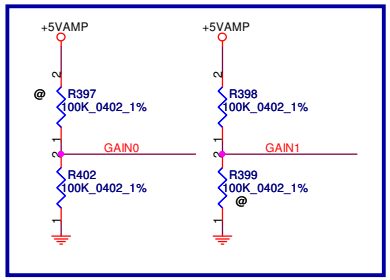
Compal Electronics,Ltd.

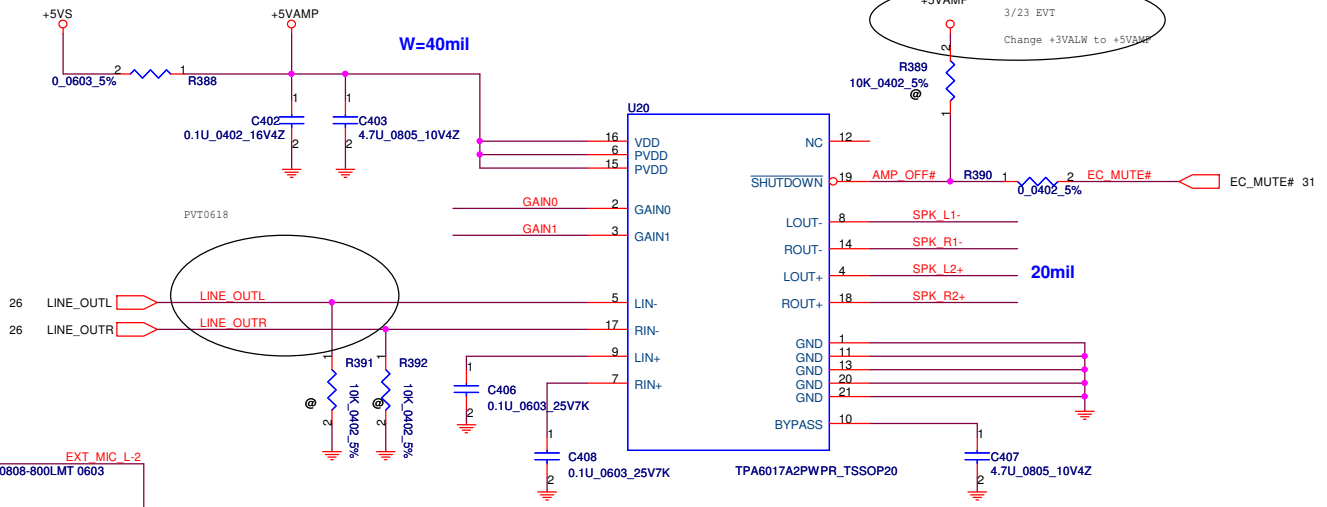
Title: HD Audio Codec_ALC272

Size: C | Document Number: KIUE0_LA-5191P | Rev: 1.0

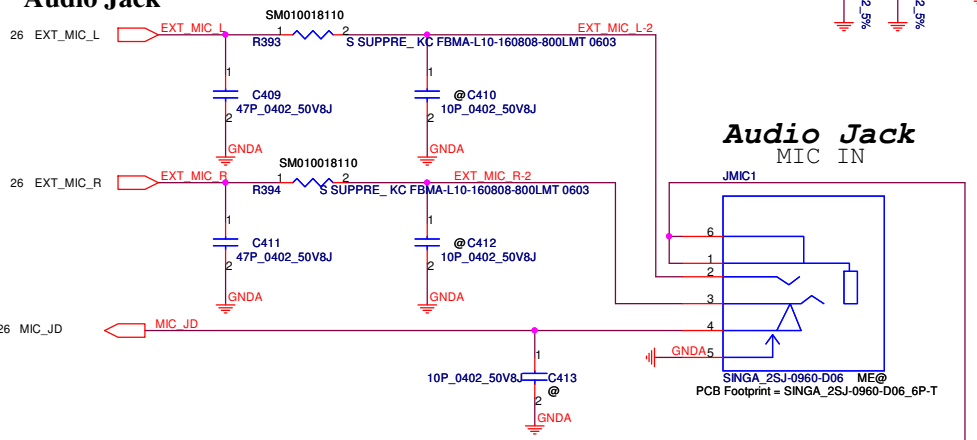
Date: Wednesday, June 24, 2009 | Sheet 26 of 43

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



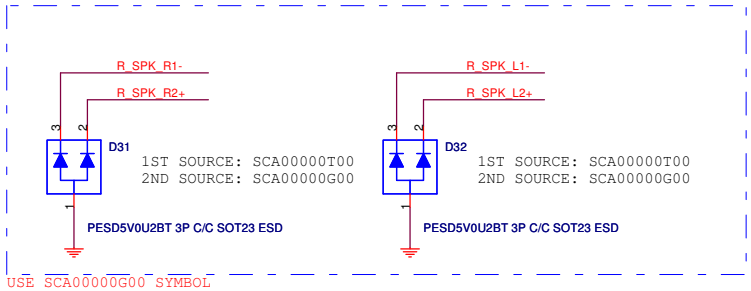


Audio Jack

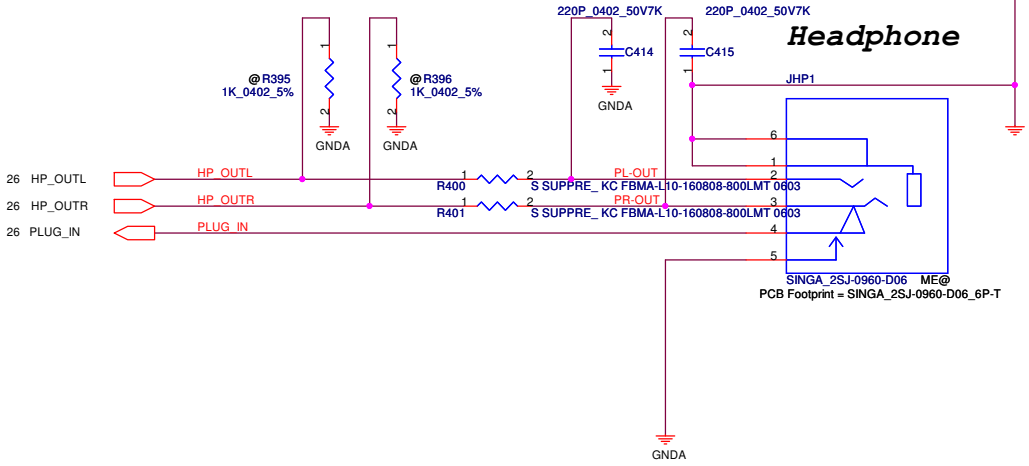


Audio Jack
MIC IN

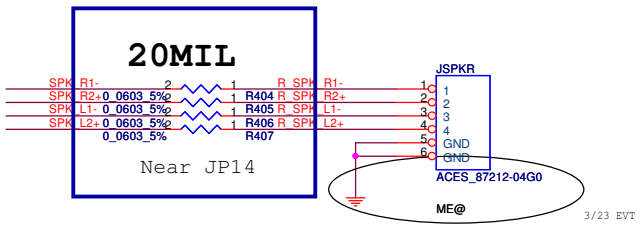
ESD PROTECT



Headphone



SPEAKER JACK



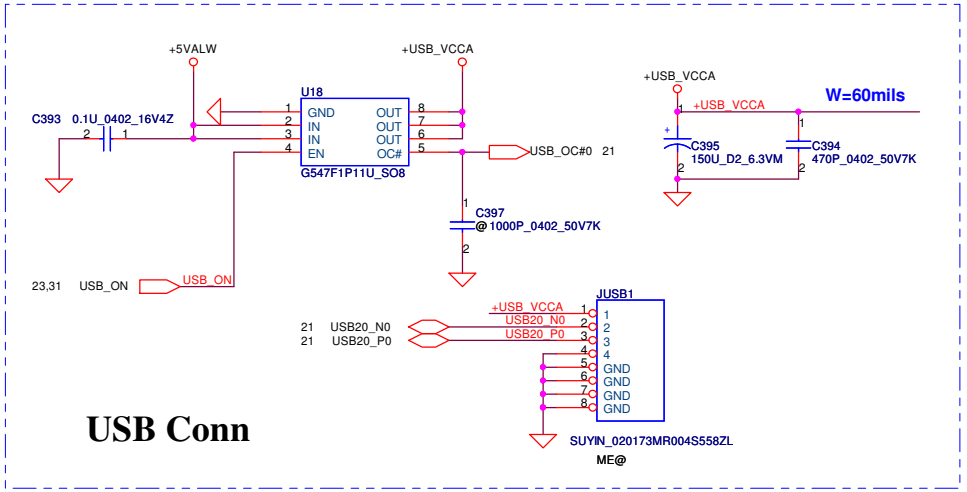
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

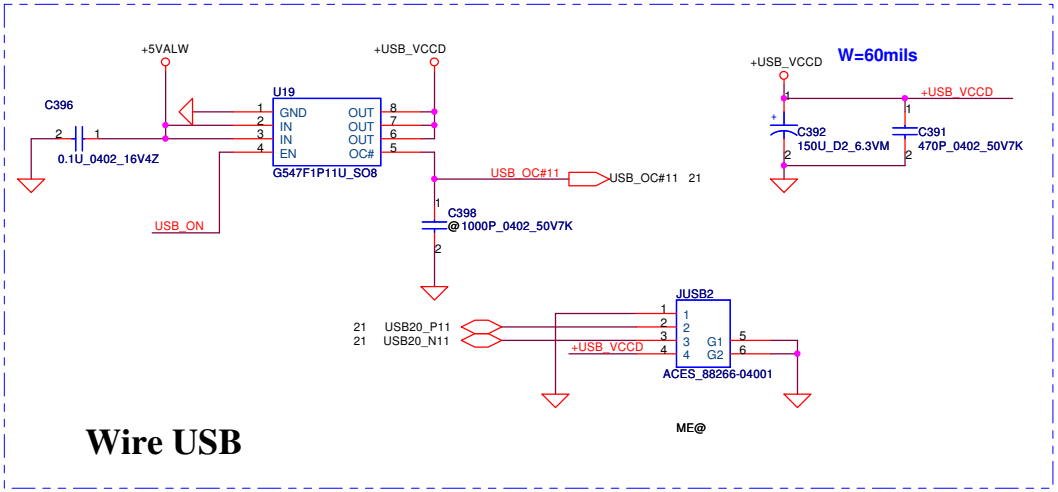
Compal Electronics,Ltd.

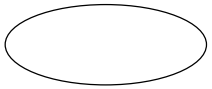
Title: AMP,Audio speaker CONN

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 27 of 43

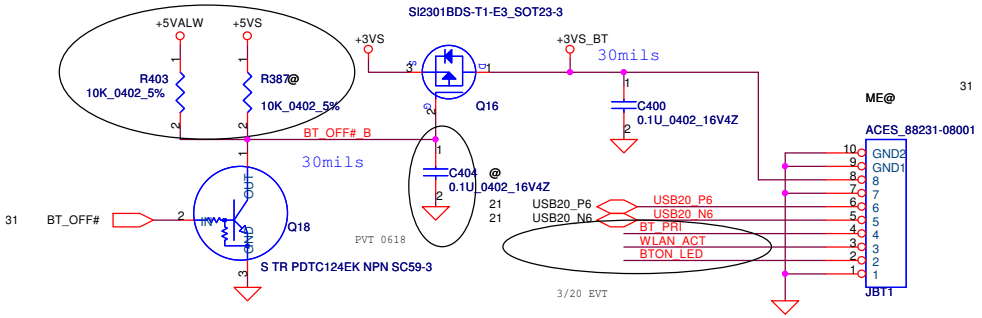


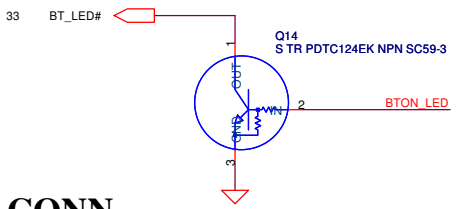




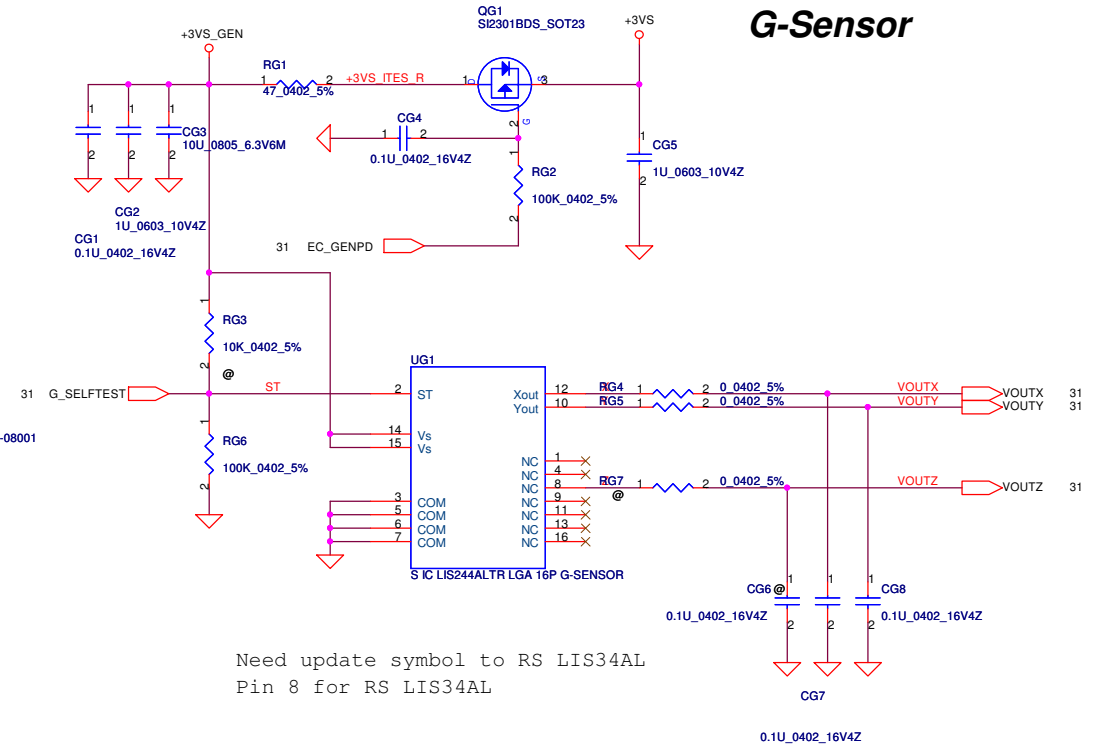
3/26 Remove ESD Diode ,by AndyYL

5/14 Change to +5VALW for floating





G-Sensor



Need update symbol to RS LIS34AL
Pin 8 for RS LIS34AL

BT MODULE CONN

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

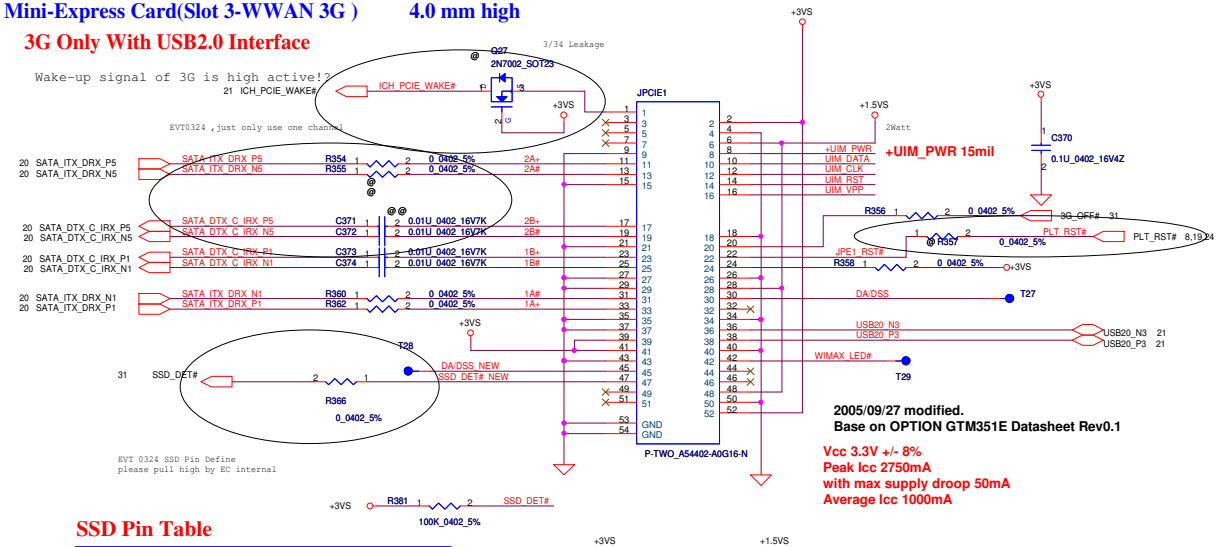
Title: USB/CMOS/BT/G-SENSOR

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 28 of 43

Mini-Express Card(Slot 3-WWAN 3G) 4.0 mm high

3G Only With USB2.0 Interface

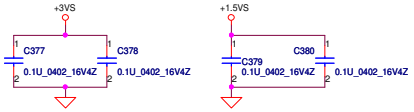


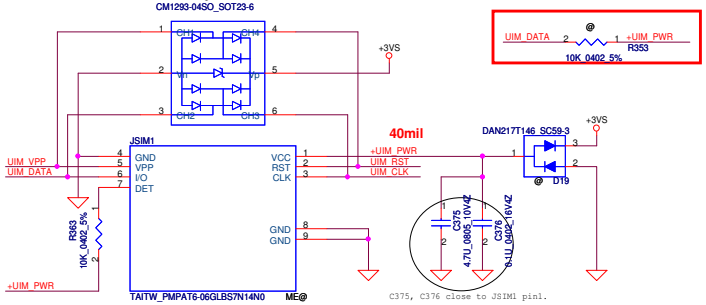
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

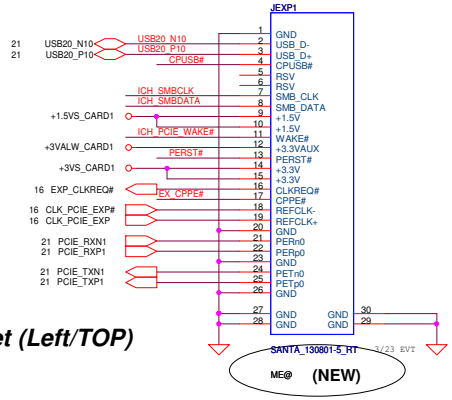
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

SSD Pin Table

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	DA/DSS
31	-A (port 1)
32	Presence Detection
33	+A (port 1)

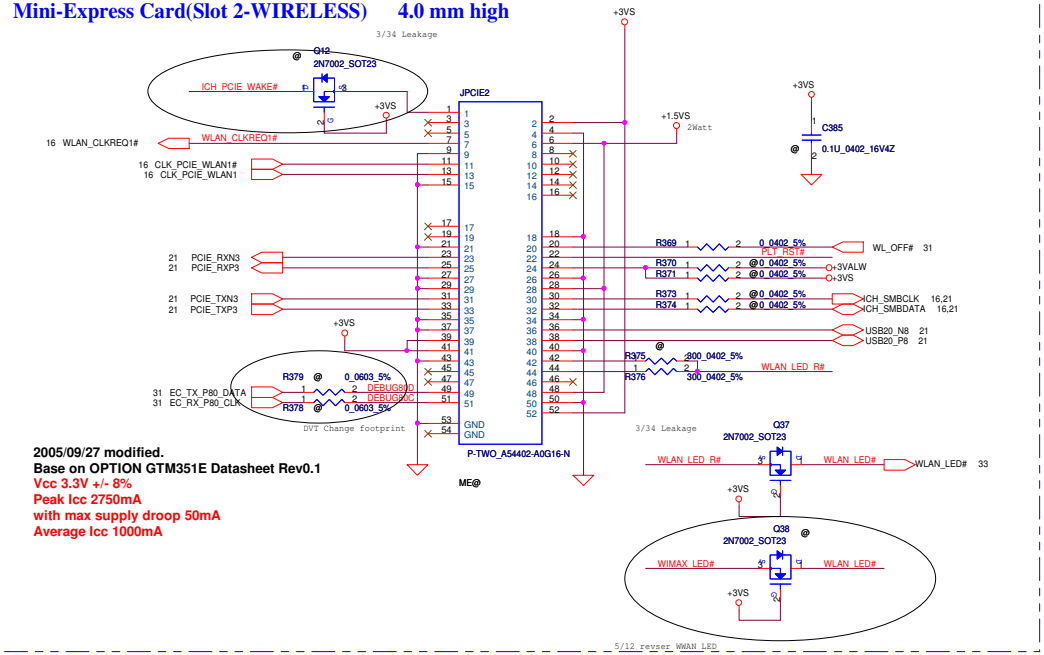






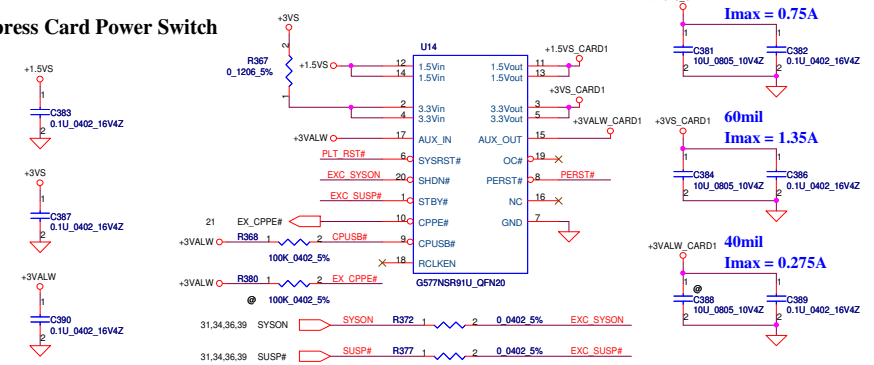
New Card 34mm Socket (Left/TOP)

Mini-Express Card(Slot 2-WIRELESS) 4.0 mm high



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

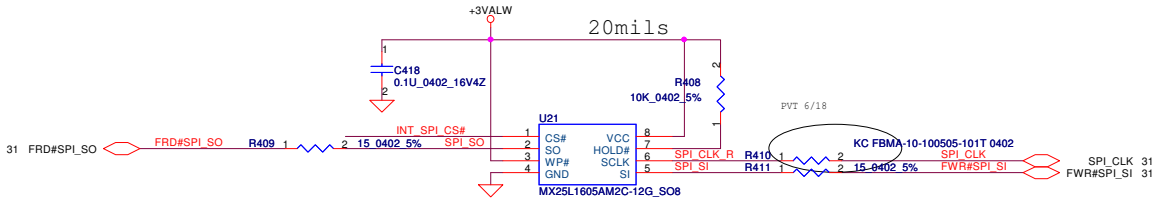
Express Card Power Switch

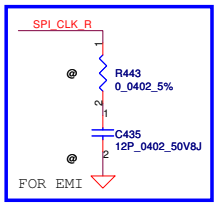


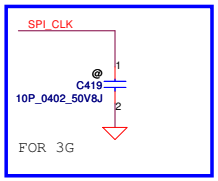
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	Mini-Card/3G/TV /BT		
Size	Document Number		Rev
	KIUE0_LA-5191P		1.0
Date:	Thursday, June 25, 2009	Sheet	29 of 43

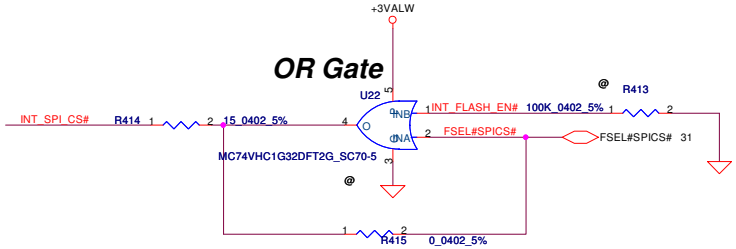
FOR EC 16M SPI ROM



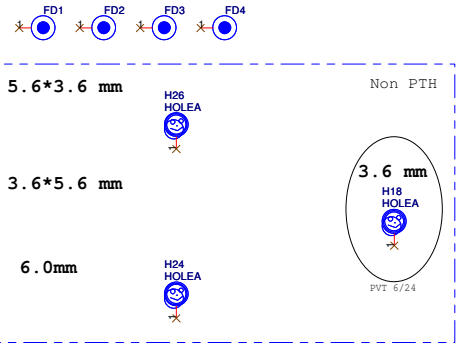


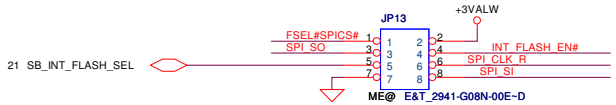


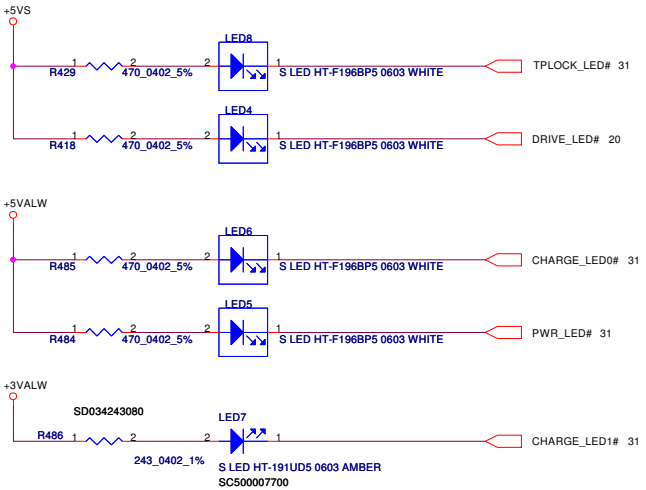
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



EVT 3/26 **Close EC Pin**

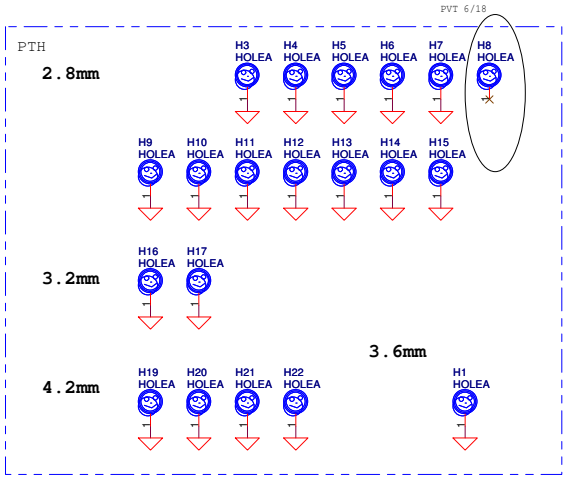






+5VLAW 470 ohm	typ	max
White LED(Vf)	2.8	3.15
current	4.6mA	3.9mA

+3.3 VALW 243 ohm	typ	max
Amber LED(Vf)	1.9	2.4
current	5.7mA	3.7mA

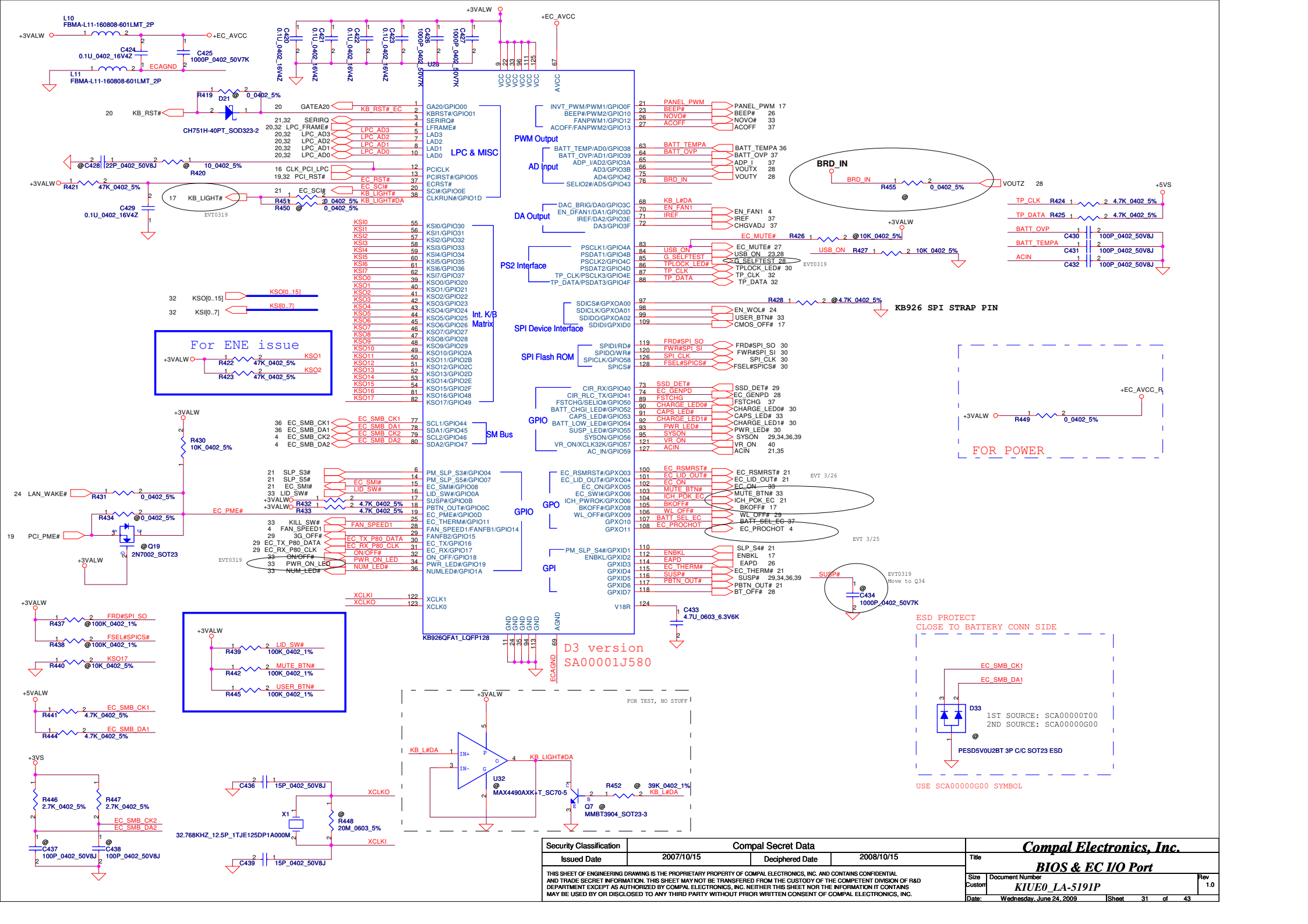


Compal Electronics, Inc.

Title: **LED/EC SPI ROM**

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 30 of 43



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

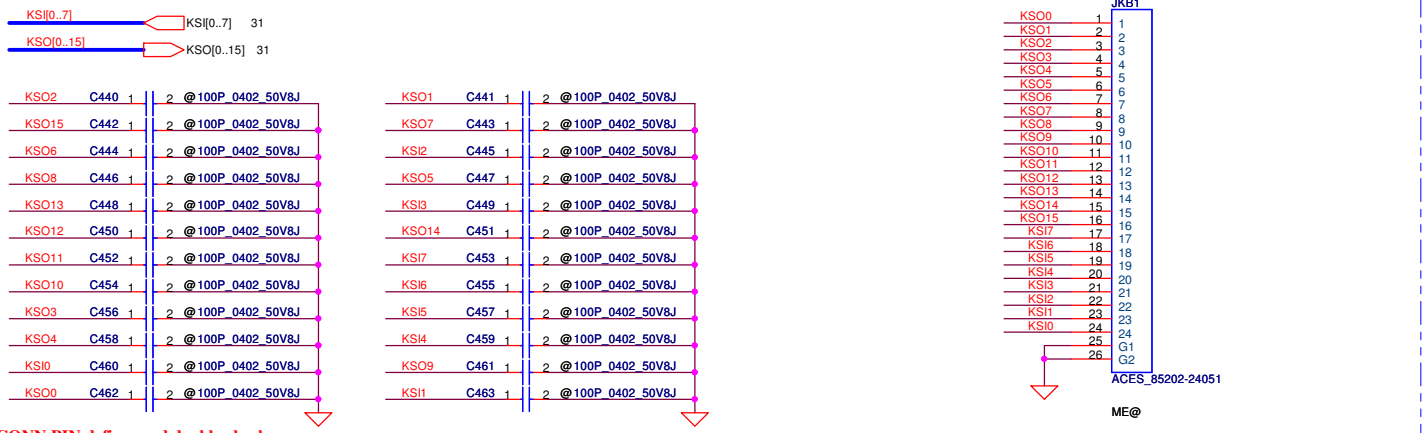
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

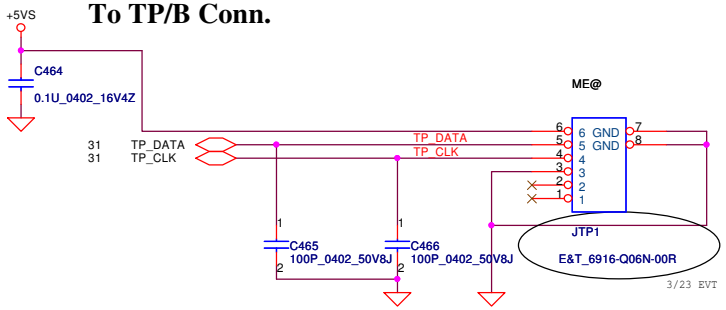
Date: Wednesday, June 24, 2009 Sheet 31 of 43

INT_KBD Conn.



CONN PIN define need double check

To TP/B Conn.

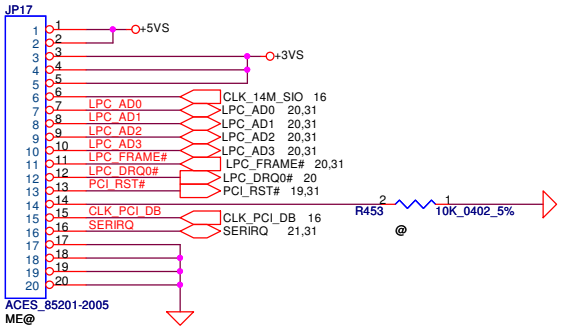


EC DEBUG PORT

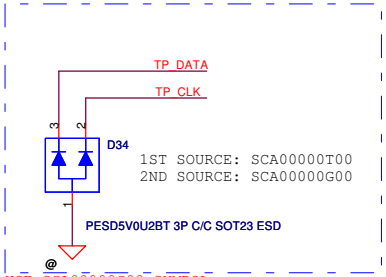
EVT0319

Delete this connector.
It same as MiniPCIE Debug Card.

FOR LPC SIO DEBUG PORT



ESD PROTECT
CLOSE TO JTP1

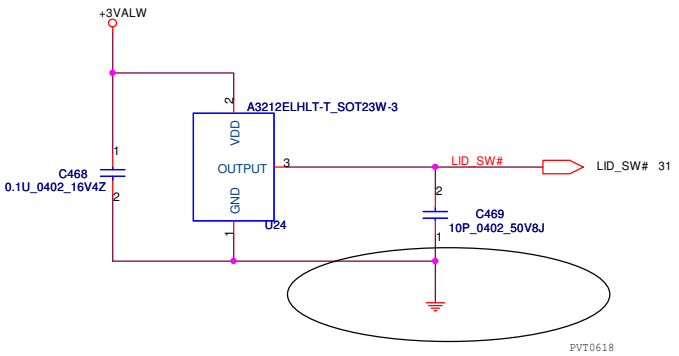


USE SCA00000G00 SYMBOL

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

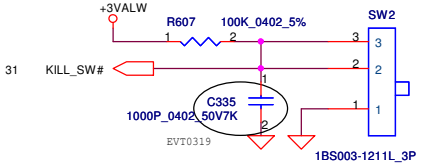
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 32 of 43		

Lid Switch

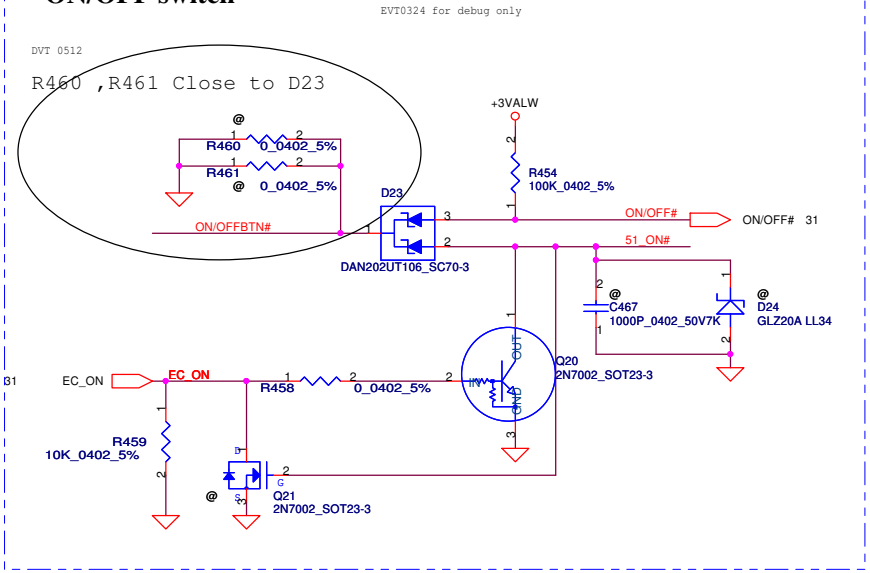


Kill Switch

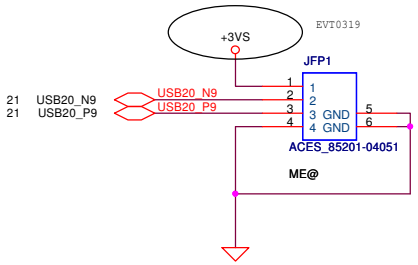
EE parts.
1st: DE100000100
2nd: DE100000I00

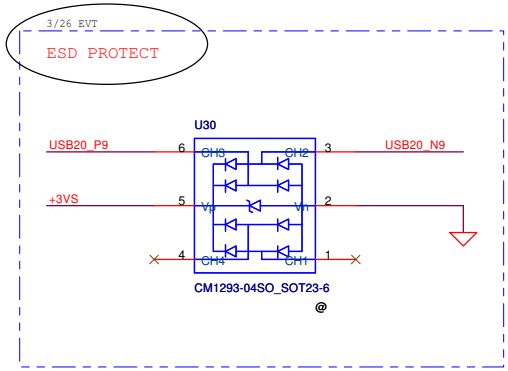


ON/OFF switch



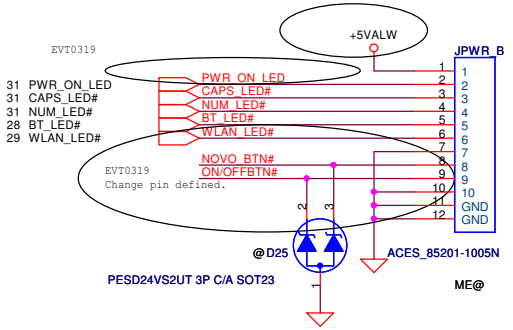
FP Board Conn 4 pin



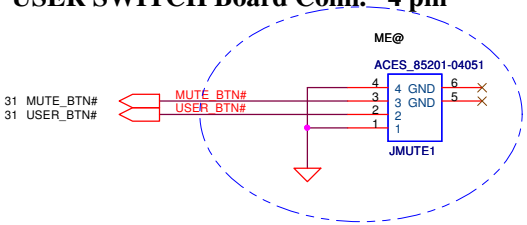


3/26 Please CLose JFP1

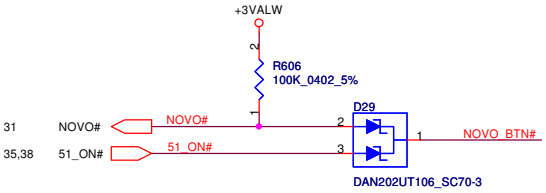
Power Board Conn. 10 pin



USER SWITCH Board Conn. 4 pin



Reverse for CABLE Pin define



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

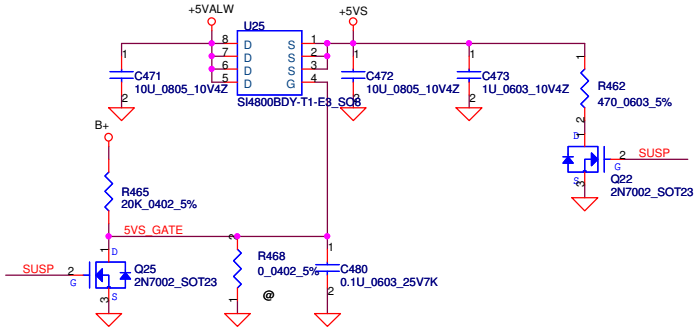
Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

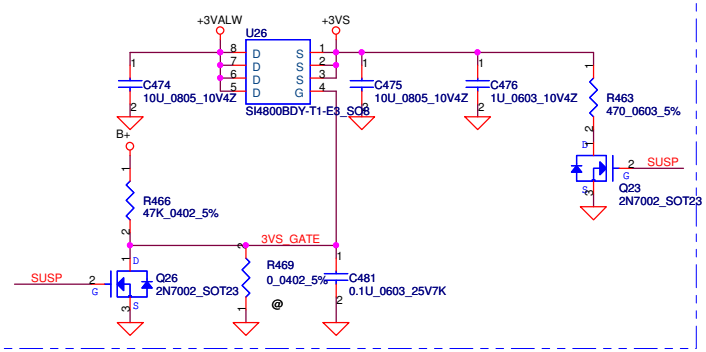
Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 33 of 43

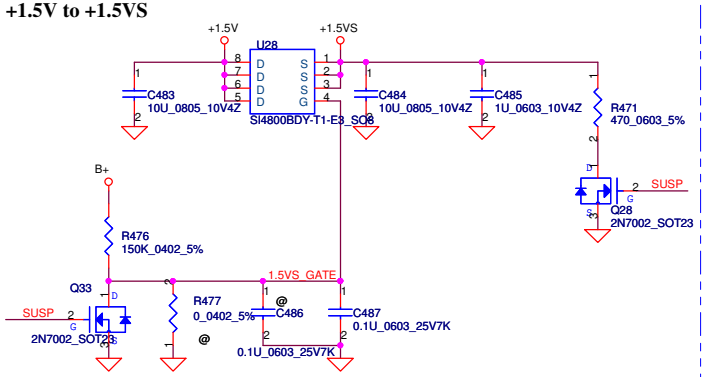
+5VALW TO +5VS

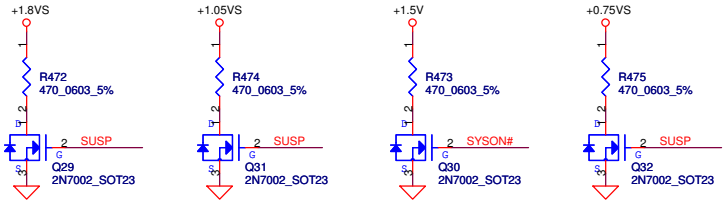


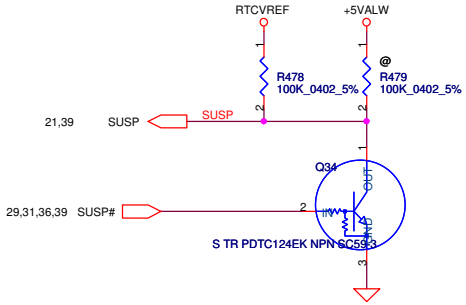
+3VALW TO +3VS

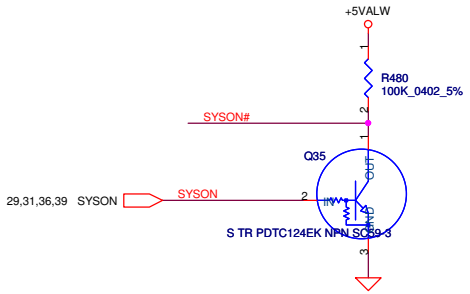


+1.5V to +1.5VS









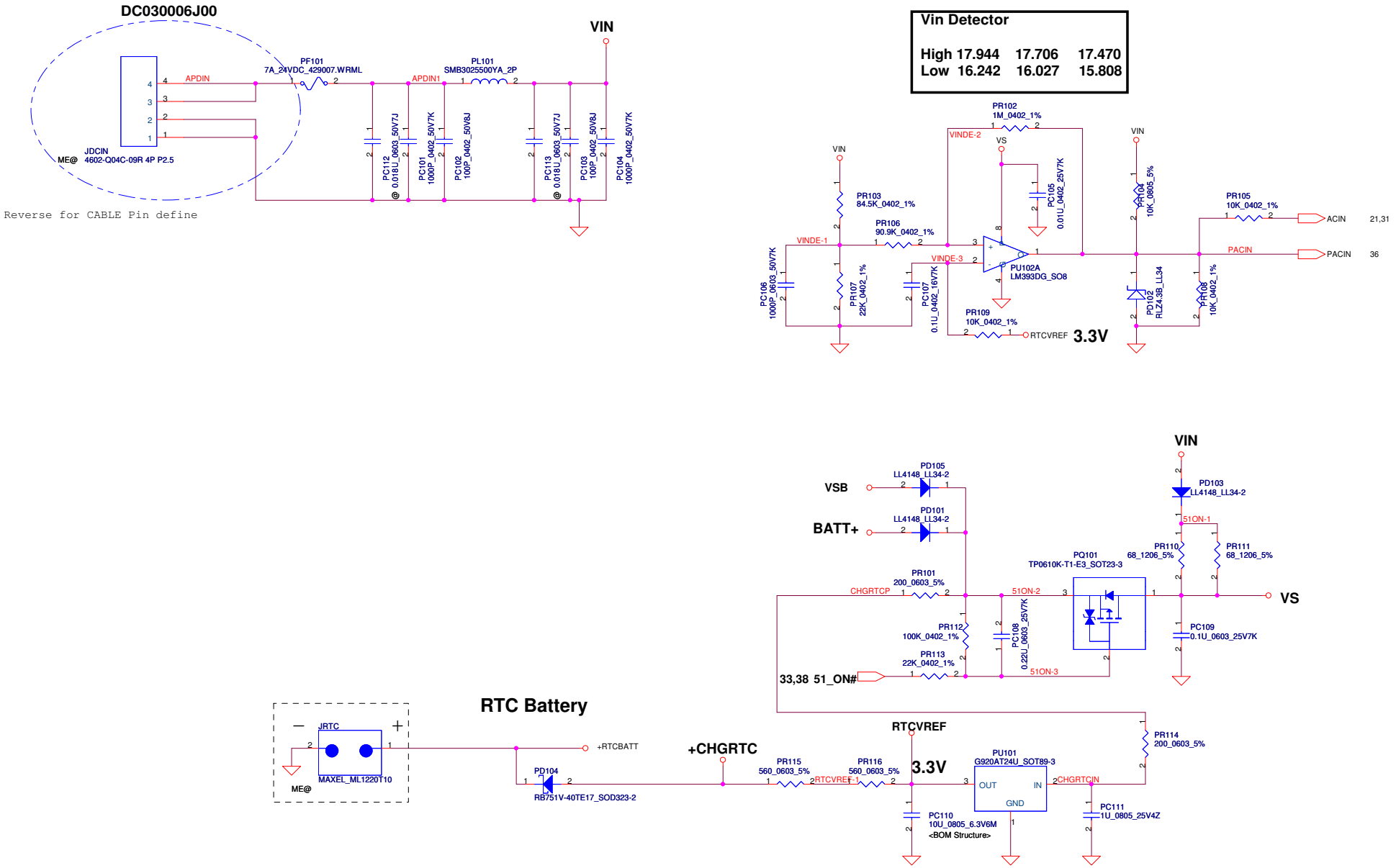
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 34 of 43



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

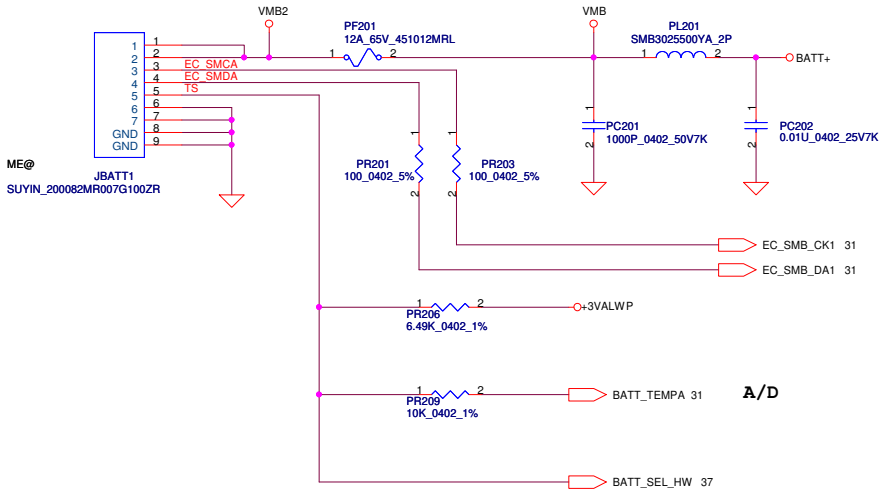
Compal Electronics, Inc.

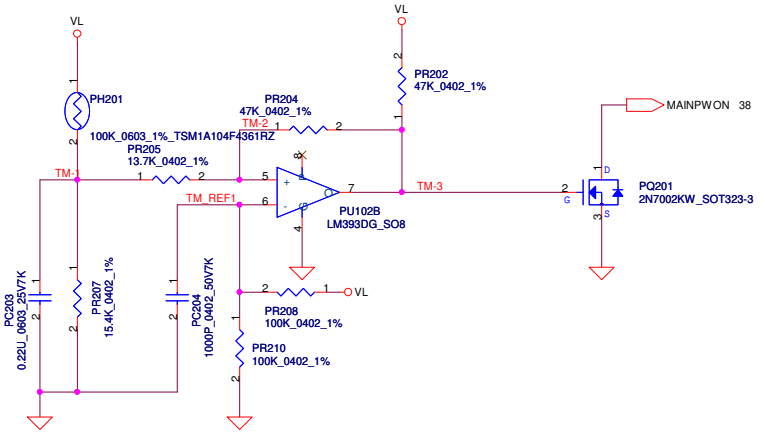
Title: DCIN & DETECTOR

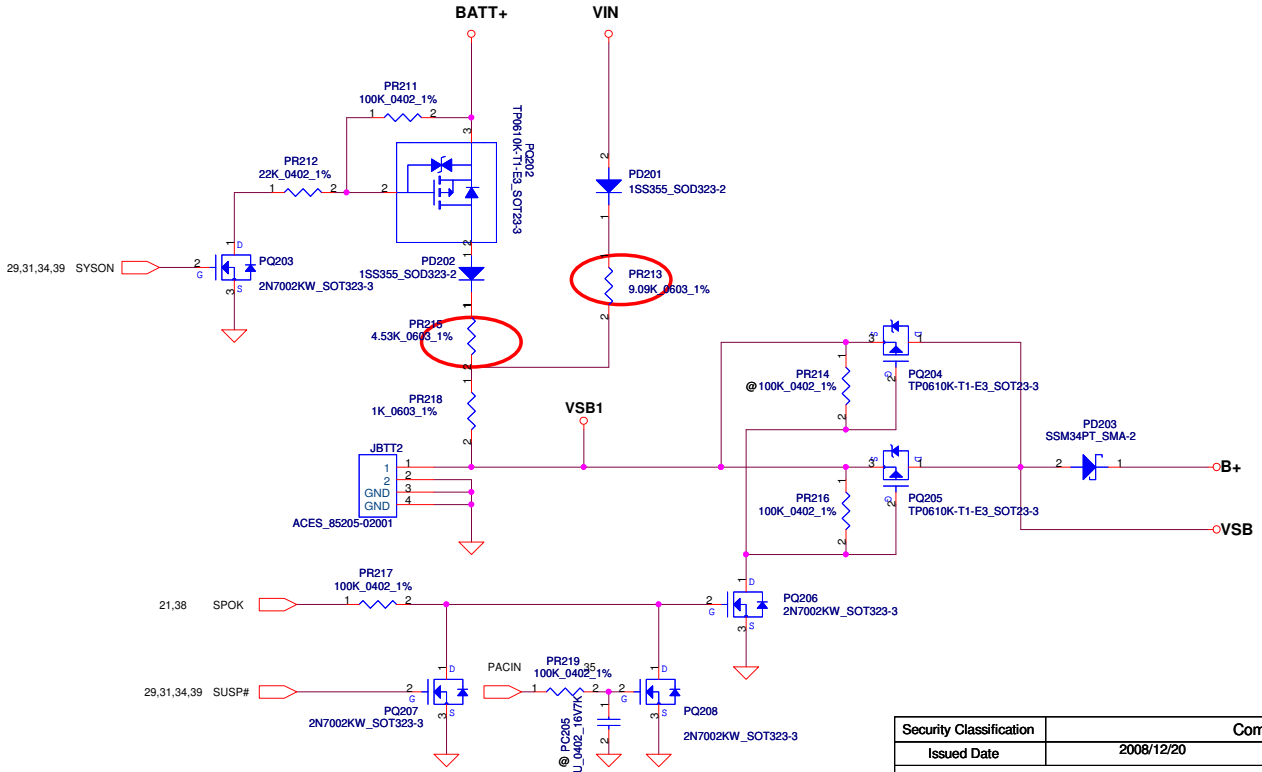
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 35 of 42

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C







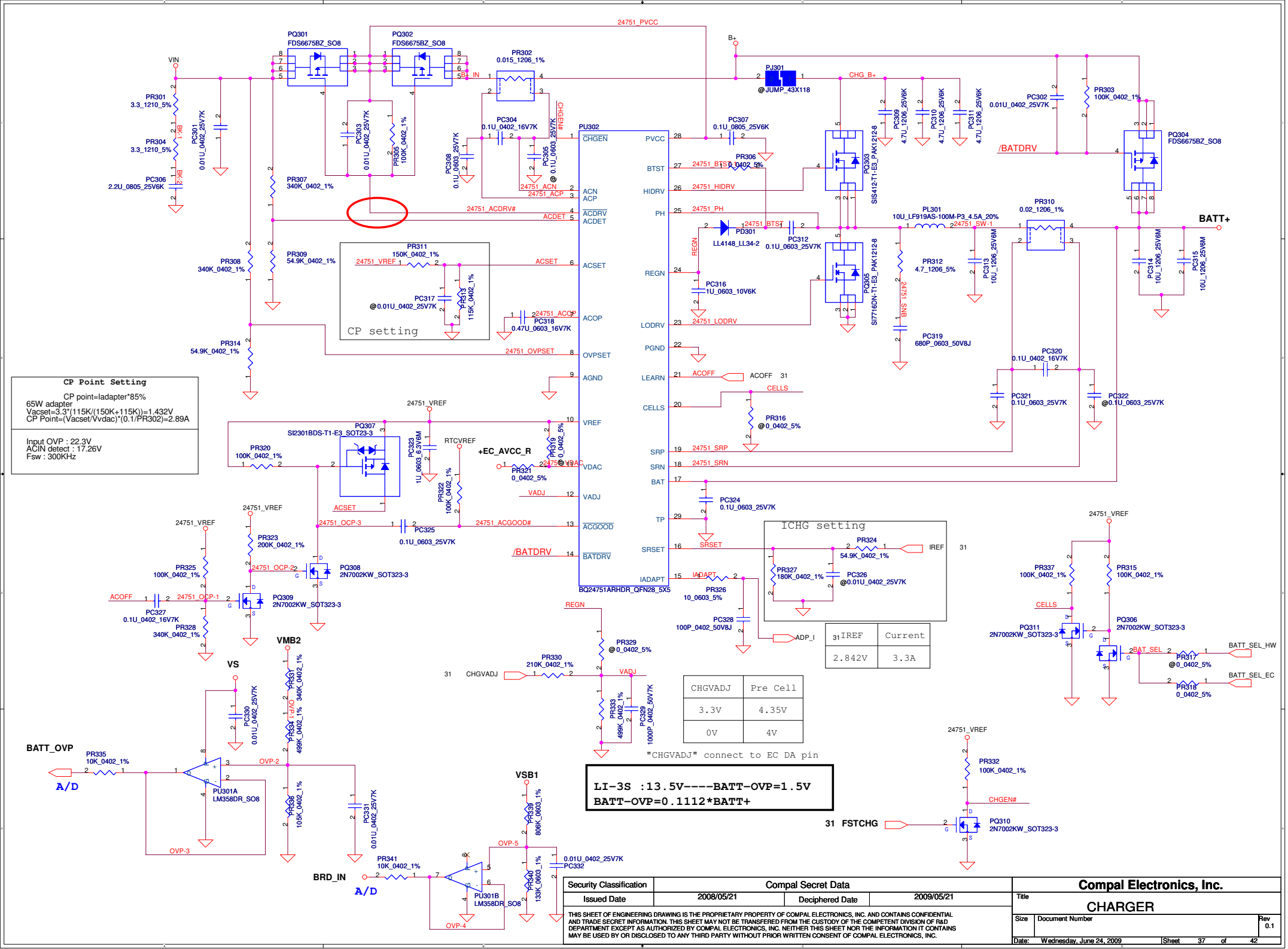
Security Classification	Compal Secret Data		
Issued Date	2008/12/20	Deciphered Date	2009/12/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Wednesday, June 24, 2009 | Sheet 36 of 42


CP Point Setting
CP point=Iadapter*85%
65W adapter
Vacset=3.3*(115K/(150K+115K))=1.432V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.89A
Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz
CP setting
ICHG setting
IREF | Current
2.842V | 3.3A
CHGVADJ | Pre Cell
3.3V | 4.35V
0V | 4V
"CHGVADJ" connect to EC DA pin
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+
BQ24751ARHDR_QFN28_5X5
PU301A LM358DR_SO8
PU301B LM358DR_SO8
A/D
Security Classification
Compal Secret Data
Issued Date
2008/05/21
Deciphered Date
2009/05/21
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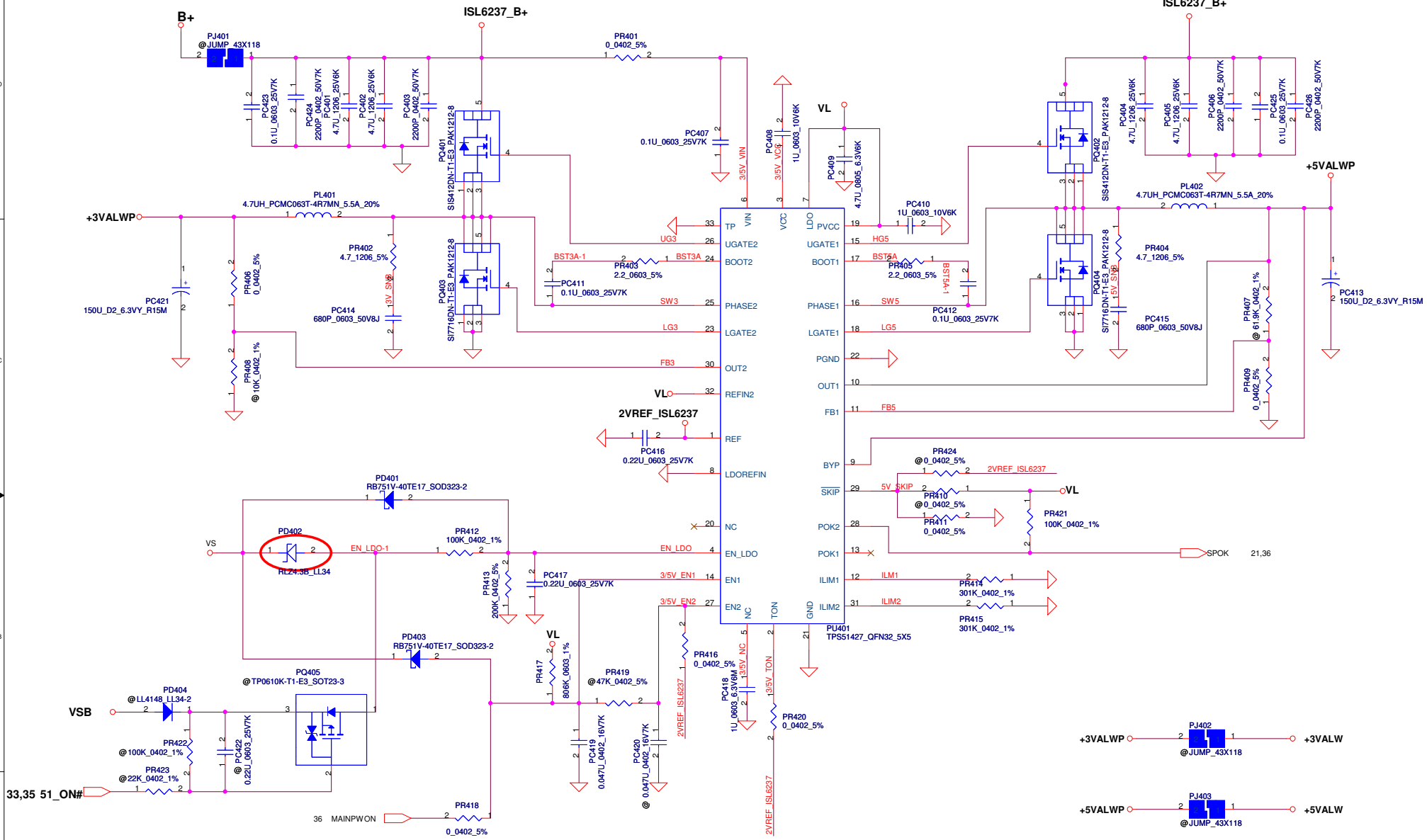
Compal Electronics, Inc.
Title
CHARGER
Size
Document Number
Rev
0.1
Date: Wednesday, June 24, 2009
Sheet 37 of 42



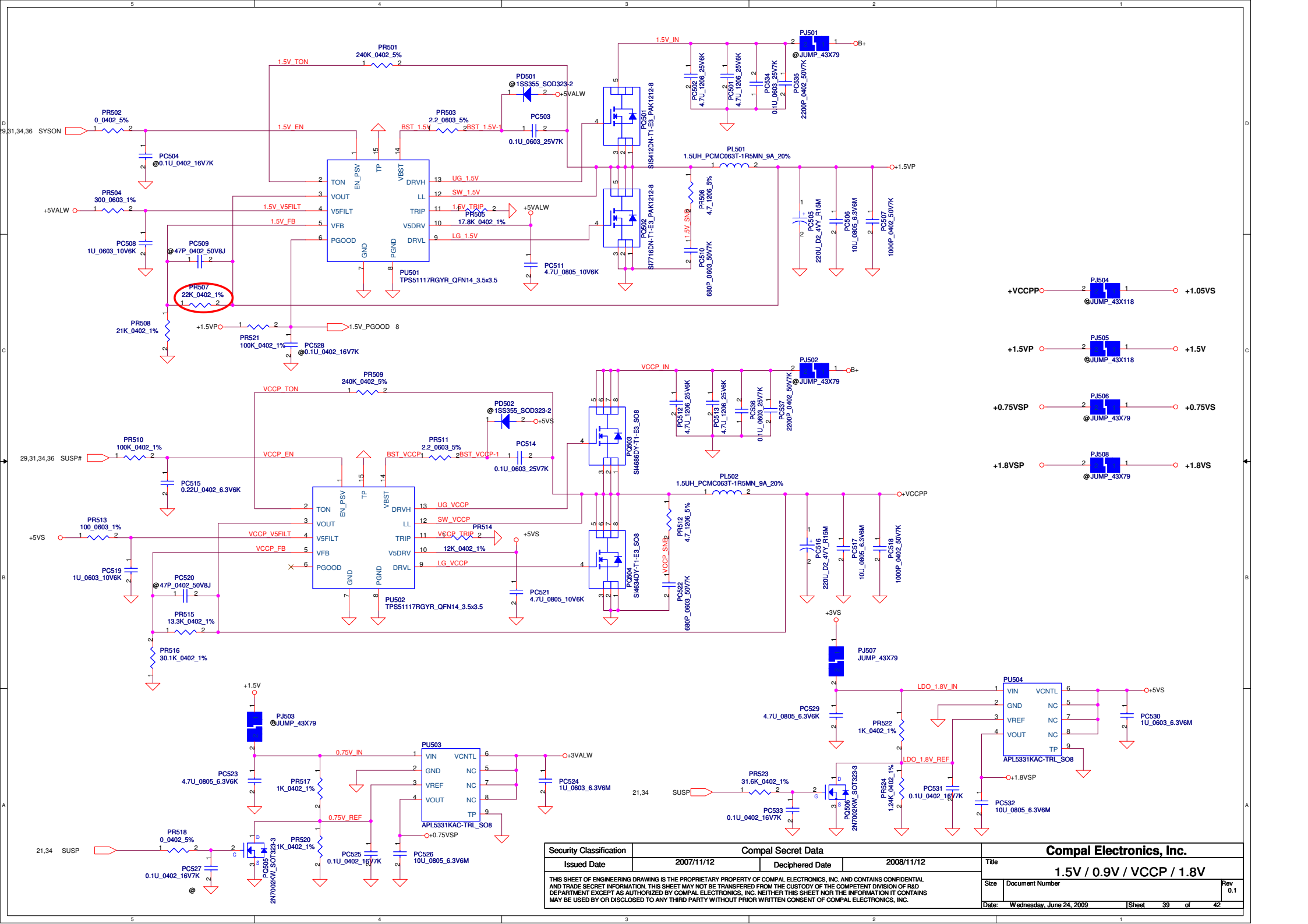
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 38 of 42



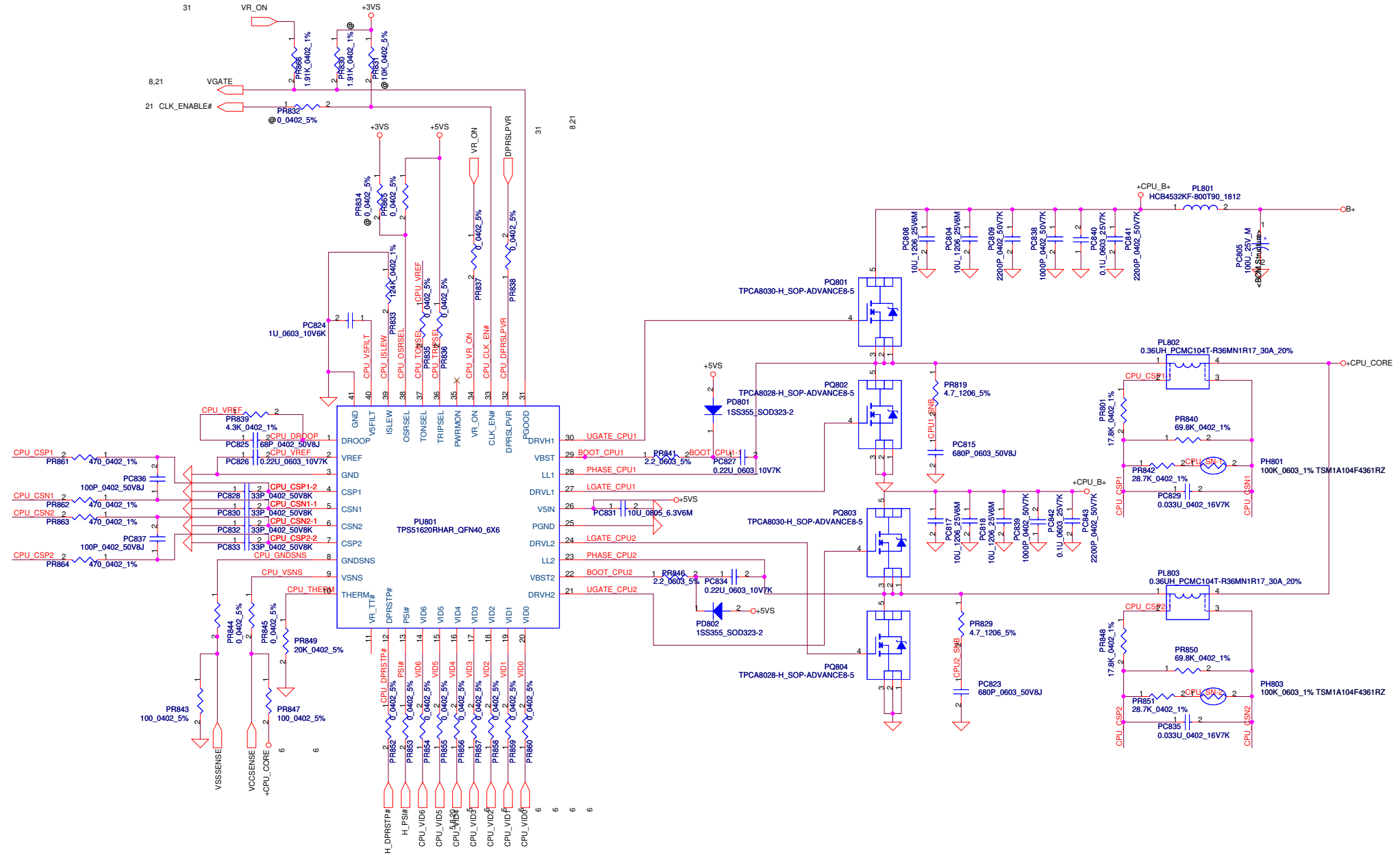
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP / 1.8V

Size	Document Number	Rev
		0.1

Date: Wednesday, June 24, 2009 | Sheet 39 of 42



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 40 of 42

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change design	add bridge battery charge circuit		P.37	add PR215 and PR218 and change PR213 from 2K to 2.2K	2009.3.20	DVT
2	Change design	Change design		P.36	JDCIN turn off 180 degree	2009.3.20	DVT
3	Change design	Change design		P.37	change JBTT2 from lie to stand	2009.3.24	DVT
4	Change design	Change design		P.37	add PR219 and PC205	2009.3.25	DVT
5	Change design	Change design		P.39	change PR403 and PR405 from 0 to 2.2 ohm	2009.3.25	DVT
6	Change design	Change design		P.40	change PR503 and PR511 from 0 to 2.2 ohm	2009.3.25	DVT
7	Change design	Change design		P.41	change PR841 and PR846 from 0 to 2.2 ohm	2009.3.25	DVT
8	Change design	Change design		P.40	change PR514 from 15.4K to 12K ohm	2009.3.25	DVT
9	Change design	Change design		P.38	add PR339 PR340 PR341 and PC332	2009.5.5	PVT
10	Change design	Change design		P.41	change PR839 from 5.76K to 4.3K ohm	2009.5.15	PVT
11	Change design	Change design		P.40	change PR504 and PR513 from 422 to 300 ohm	2009.5.15	PVT
12	Change design	Change design		P.38	delect PR338	2009.6.18	Pre_MP
13	Change design	Modify bridge battery charge current		P.37	change PR213 from 2.2k to 9.09k and PR215 from 1.21k to 4.53k	2009.6.18	Pre_MP
14	Change design	Modify 1.5V output voltage		P.40	change PR507 from 21k to 22k	2009.6.18	Pre_MP
15	Change design	For bridge battery can work in S3		P.39	change PD402 from RLZ5.1B to RLZ4.3B	2009.6.18	Pre_MP
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: KIWAX_LA-5081P | Rev: 0.1
Date: Wednesday, June 24, 2009 | Sheet 41 of 42

NO DATE PAGE MODIFICATION LIST PURPOSE

EVT modify 20090319

1. 03/19 P.17: Change EDID voltage to +3VS rail.
2. 03/19 P.23: HDD power +3VS +5VS add resistors for measure.
3. 03/19 P.24: LANREQB is low active. Don't need unnecessary circuit.
4. 03/19 P.24: Net LAN_WAKE# is double pull-up. del RL2.
5. 03/19 P.24: +3V_LAN add a resistor for measure.
6. 03/19 P.32: Del JP15, It same as MiniPCIE Debug Card.
7. 03/19 P.26: R322 add, R321 del. For HDA interface.
8. 03/19 P.33: Change Finger printer from Egis to Upek. Power rail is +3VS of Upek.
9. 03/19 P.16: Avoid glitch of H_STP_PCI#, pull-up PCI_STP# directly.
10. 03/19 P.29: For debug card issue. And add R378, R379, R295 100K.
11. 03/19 P.21: For Waveform add C60.
12. 03/19 P.26: For EMI R345.
13. 03/19 P.31: KB light change to pin38 GPIO1D.
14. 03/19 P.31: Add EC pin34 GPIO19 PWR_ON_LED to page.33 power board connector.
15. 03/19 P.31: Add EC pin85 GPIO4C G_SELFTEST to page.28 G-sensor ST pin.
16. 03/19 P.33: Add C335 for Kill-switch.
17. 03/19 P.33: Change JPWR_B conn Pin define

EVT modify 20090320

18. 03/20 P.6: C16 NC,for Pwr confirm
19. 03/20 P.28: Change JBT1 pin define for BT spec updated

EVT modify 20090323

20. 03/23 P.29: Change JEXP1 ;JLVDS1; JTP1 Conn by ME

EVT modify 20090324

21. 03/24 P.17: Reverse GMCH DPST function
22. 03/24 P.29: Reverse MINI CARD SATA Lane
23. 03/24 P.29: Change Pin Define for SSD
24. 03/24 P.29: Reveerse JPCIE1 PLT_RST#

EVT modify 20090325

25. 03/25 P.4 : Add thermal protection Circuit by lenvono
26. 03/25 P.21 : S0 to G3 state ,abnormal shudown
27. 03/25 P.21 : Change New CARD PCI-E port 4 to Port 1 for powr saving
28. 03/25 P.33 : ADD EMI&ESD solution
29. 03/25 P.24 : Delete Mac ROM Circuit ,Because of layout space not enough
30. 03/25 P.24 : Change Q24 to PMOS From NMOS,to saving bom cost
31. 03/25 P.26 : modify PC-BEEP circuit aviod Signal and Pwr noise

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number: *KIUE0_LA-5191P* | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 42 of 43

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Detect Bridge Bettery life	Can't detect Bridge bettery	0.3	31	ADD R455	5/5	DVT
2	Esay rework for PORT 80	Not easy debug with system builded	0.3	29	CHANGE R378,R379 SIZE From 0402 to 0603 (NC)	5/13	DVT
3	BT Pwer MOS Floating	BT Pwr MOS Floating	0.3	28	NC R387, ADD R403	5/13	DVT
4	WWAN Noise Solution	Reserve C470	0.3		ADD C470 (NC)	5/13	DVT
5	Material LT	LIS34ALTR LT more than 4 months	0.3	28	CHANGE UG1 From LIS34ALTR to LIS244ALTR	5/13	DVT
6	DFB Design	COST DOWN	0.3	17	DELETE R167,R168,R287,R361	5/13	DVT
7	WWLAN LED	Reverse WWAN LED SWITCH	0.3	29	ADD Q38 (NC)	5/13	DVT
8	ICH_POK Glitch	Glitch will cause abnormal Power sequence	0.3	21	ADD D35,Q39 (NC),R456 (NC)	5/13	DVT
9	EMI Solution	EMI issue	0.3	17	ADD D36	5/13	DVT
10	Soft Start circuit	OCP	0.3	24	ADD R304,C325 (NC),C122	5/13	DVT
11	Debug use only		0.3	33	DELETE J3,J4,SW1,ADD R460 (NC),R461(NC)	5/13	DVT
12	BOM Option	Reserve R121	0.3	16	CHANGE R122 From 12 Ohm to 33 Ohm	5/16	DVT
13	BOM Option	ALC272-GR EOL	0.3	20	CHANGE SA00002CI00 to SA00002CI10	5/25	DVT
14	BOM Option	DELETE ROHM MATERIAL FROM 1st BOM	0.3		CHANGE SBX01240010 to SB00000AG00	5/25	DVT
15	BOM Modify		1.0	23	CHANGE R90 SIZE From 0603 to 0805, DELETE R335,R342,R416	6/23	PVT
16	Stepping to V1.0	Update LA5191PR10 to Stepping to V1.0	1.0	01	Update DAZ P/N to V1.0 and ADD Sub-Bard P/N LS5191/LS5192/LS5193/LS5194	6/23	PVT
17	Soft START Circuit	OCP for LAN	1.0	24	Change R304 from 0 Ohm to 10K Ohm , Delete C122	6/23	PVT
18	Mic Pull high change		1.0	26	Change R333 From 4.7K Ohm to 2.2K Ohm	6/23	PVT
19	AUDIO LINE OUT CAP	Remove Duplicated Cap	1.0	27	DELETE C404,C405	6/23	PVT
20	EMI SOLUTION	SPI CLK	1.0	30	Change R410 From 15 Ohm to KC FBMA-10-100505-101T 0402	6/23	PVT
21	Soft START Circuit	OCP for Bluetooth	1.0	28	ADD C404 (NC)	6/23	PVT
21	Soft START Circuit	OCP for CAMERA	1.0	17	ADD C416 (NC)	6/23	PVT

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Thursday, June 25, 2009 | Sheet 43 of 43