

Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-06-18

REV:0.2

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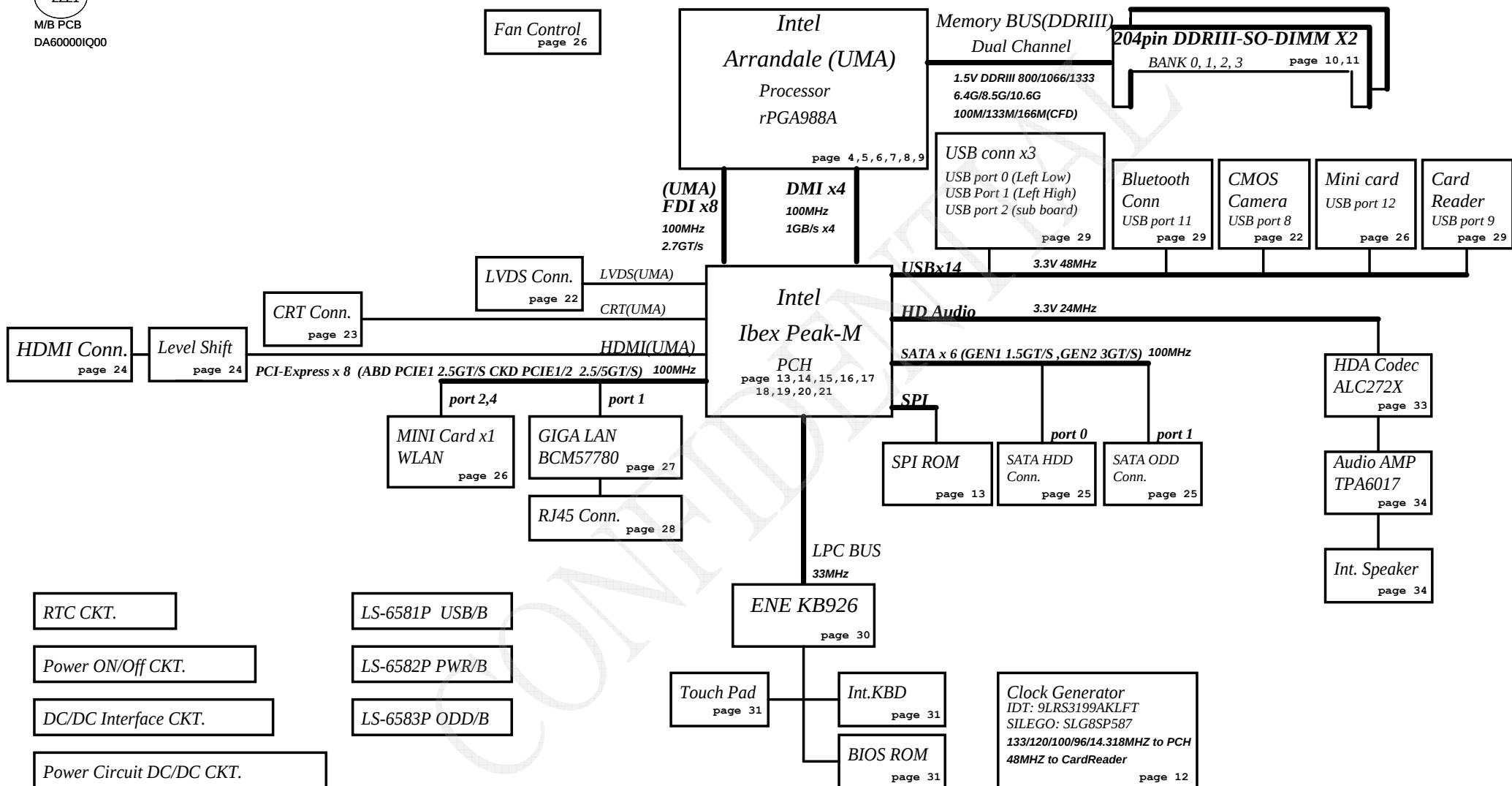
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Model Name PEW71_81 UMA

File Name : LA-6582P

ZZZ1

M/B PCB
DA60000IQ00



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

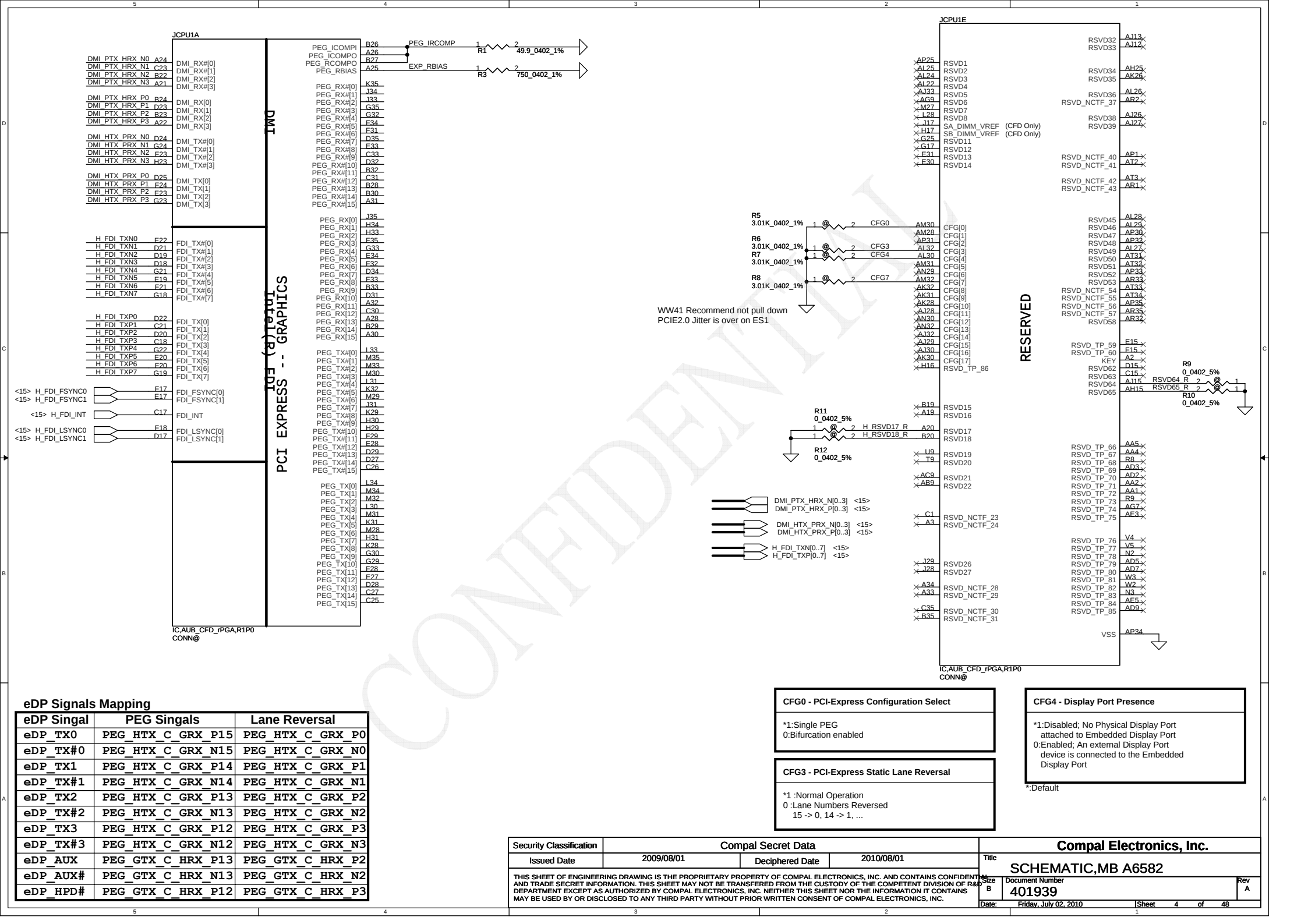
Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

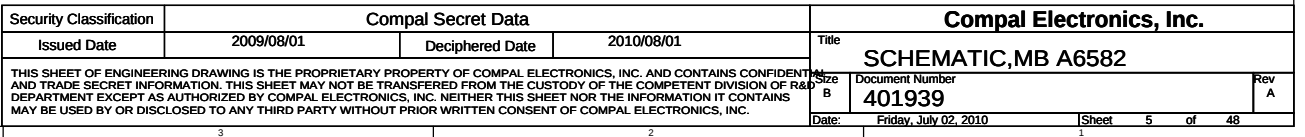
Project ID / Board ID Table for EC-AD channel

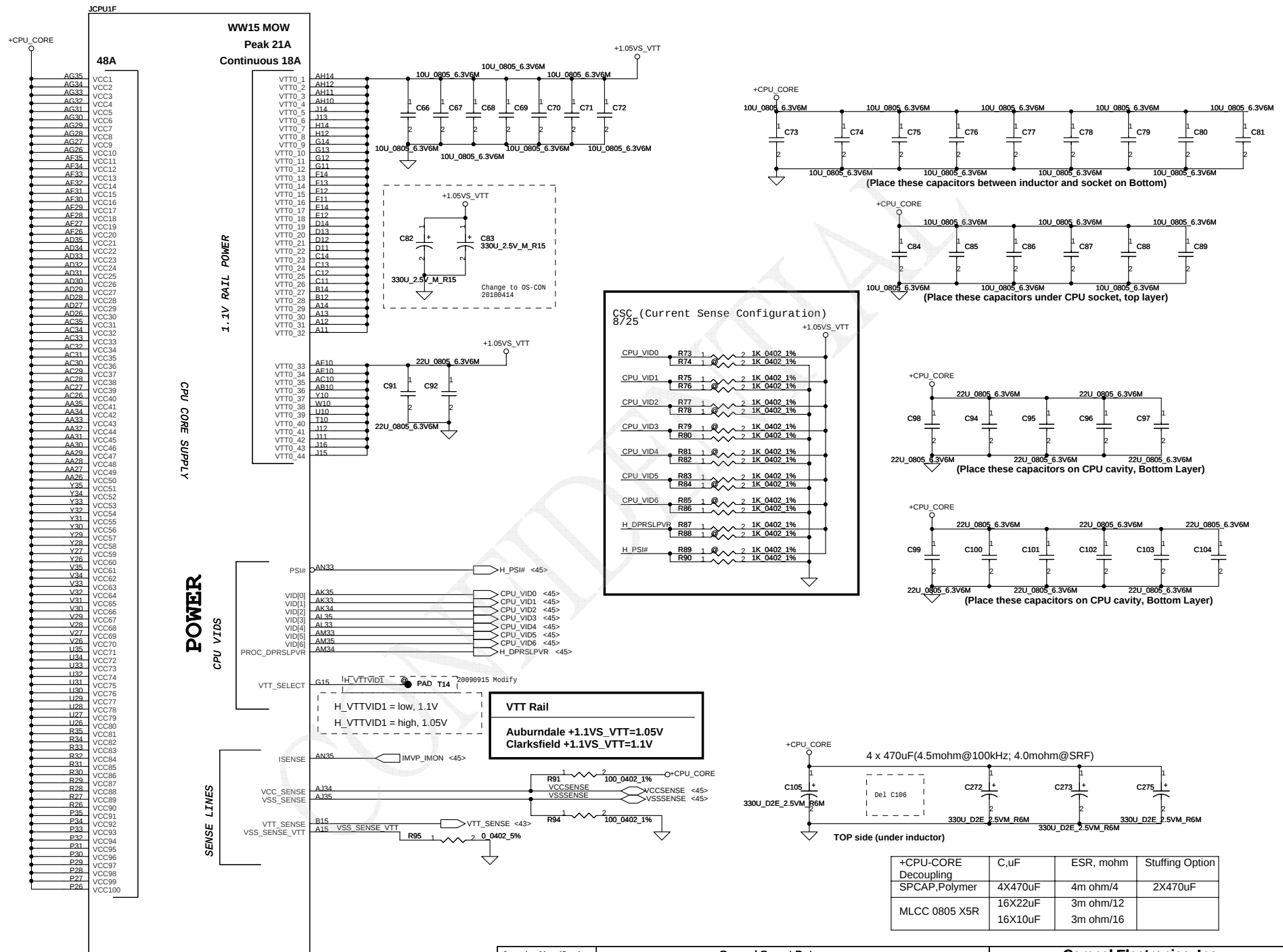
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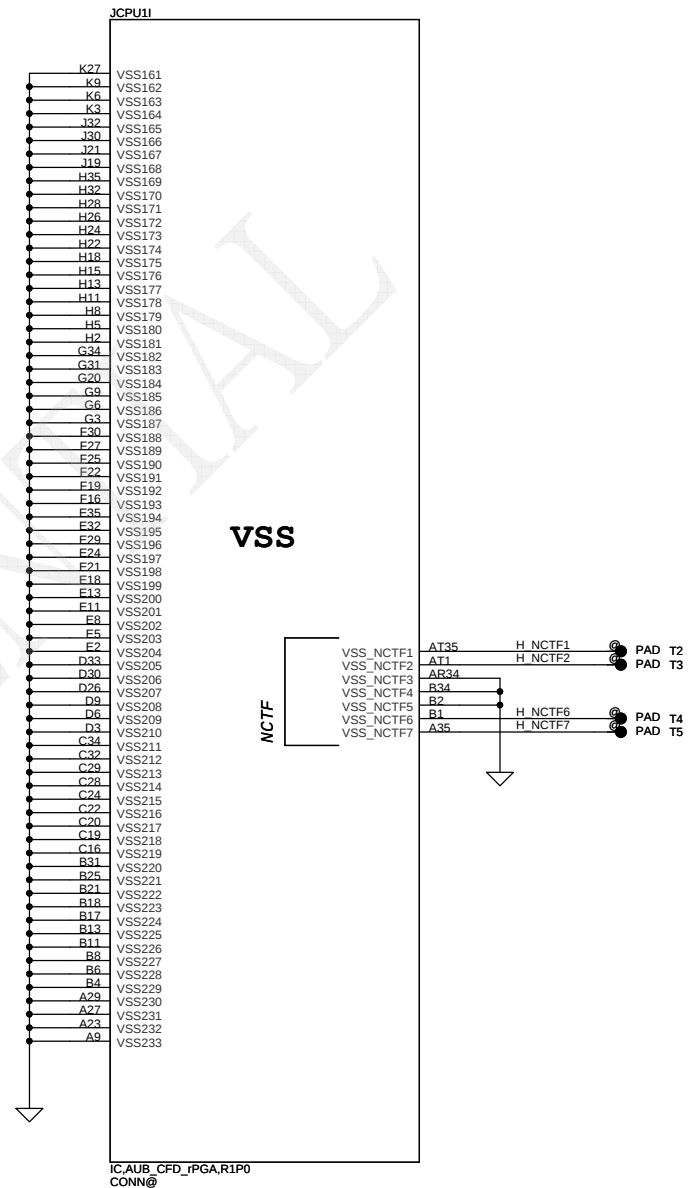
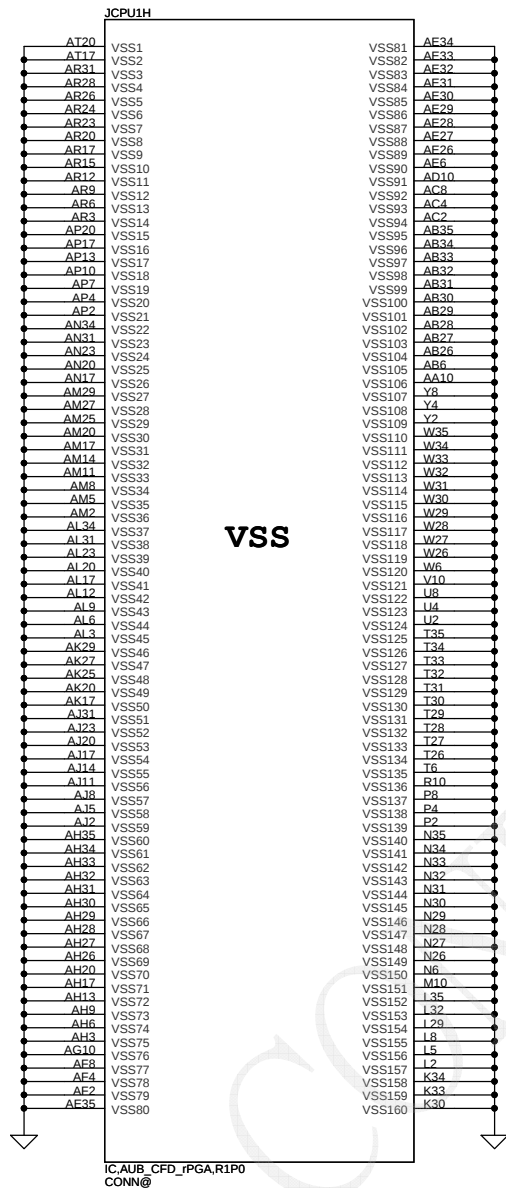
USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
		2	Ext3 Right USB	Ext3 Right USB
	UHCI1	3		
		4		
	UHCI2	5		
		6		
		7		
EHCI2	UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10		
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13		

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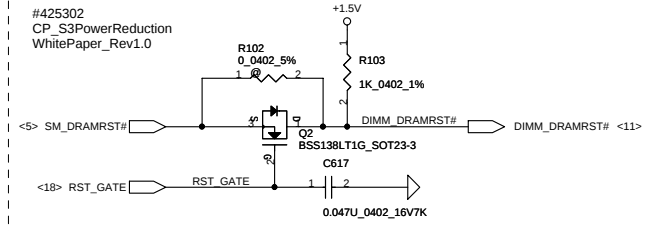
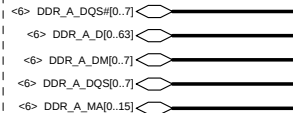








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Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

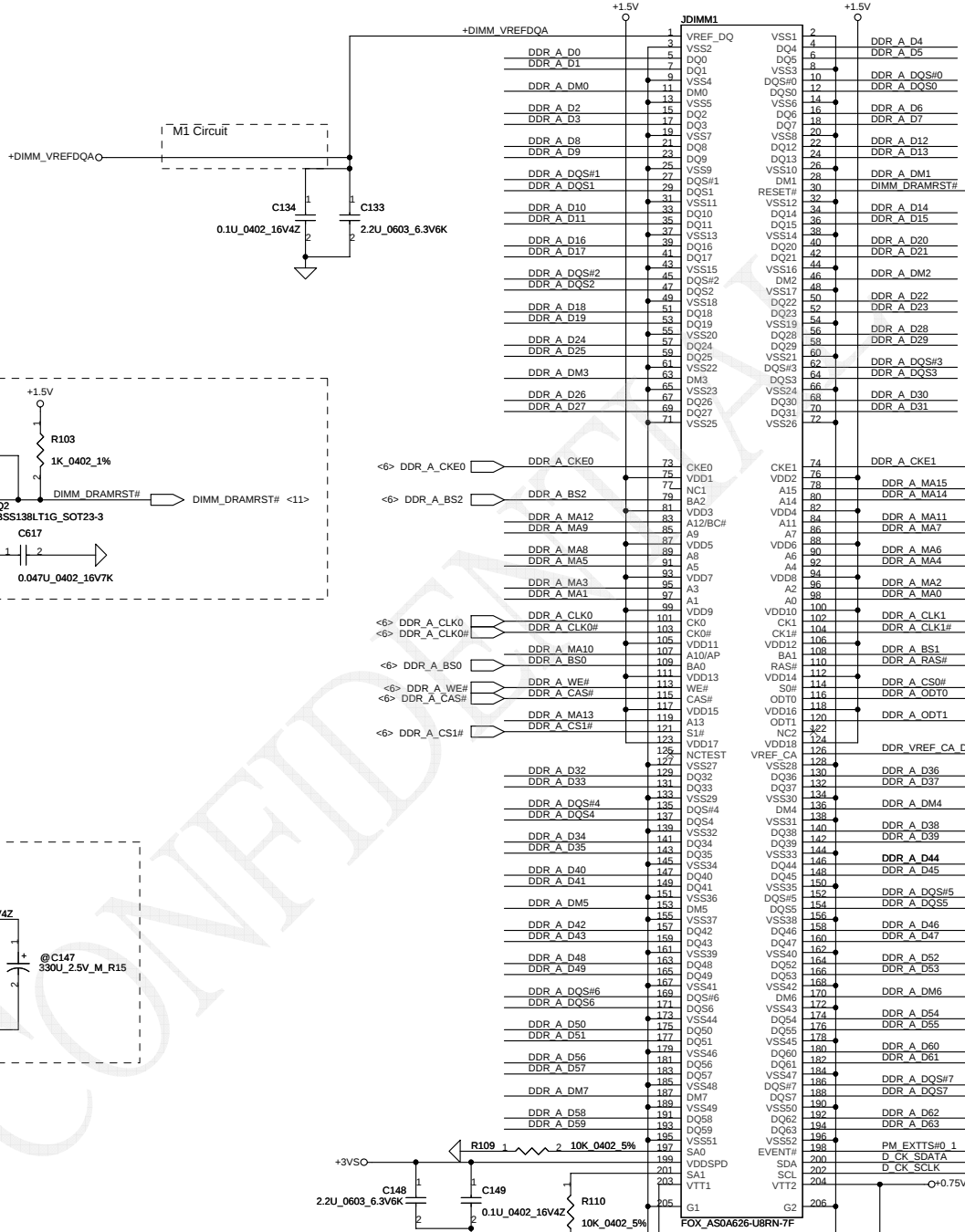
+15V

10U_0805_6.3V6M 10U_0805_6.3V6M 10U_0805_6.3V6M 0.1U_0402_16V4Z 0.1U_0402_16V4Z

C137 C138 C139 C140 C141 C142 C143 C144 C145 C146

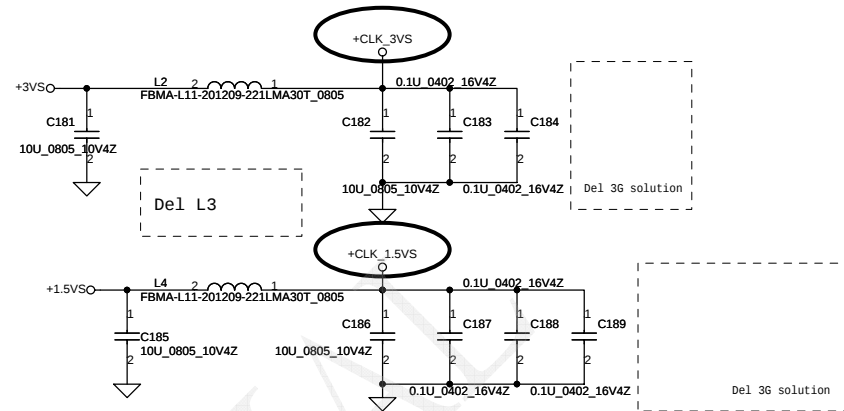
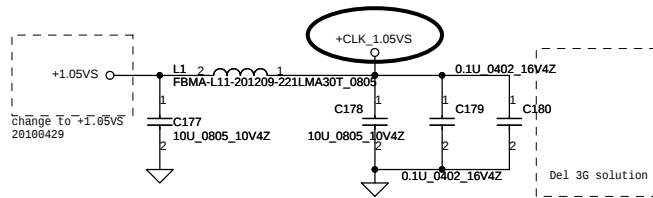
10U_0805_6.3V6M 10U_0805_6.3V6M 10U_0805_6.3V6M 0.1U_0402_16V4Z 0.1U_0402_16V4Z

@C147 330U_2.5V_M_R15

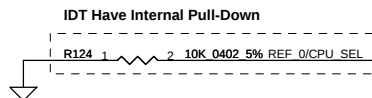
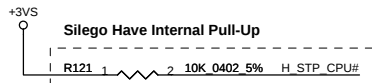
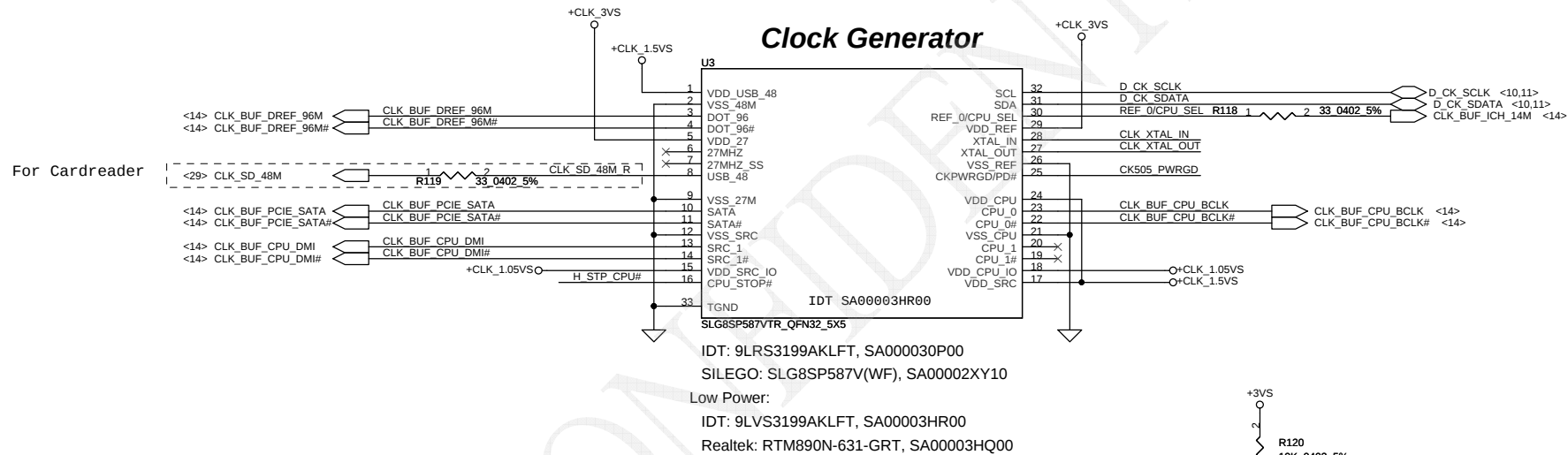


DDR3 SO-DIMM A Change to Reverse Type 8mm High

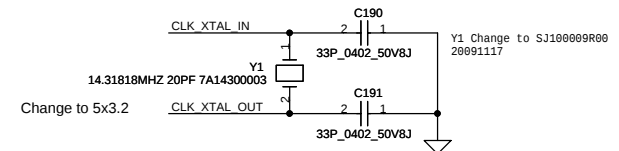
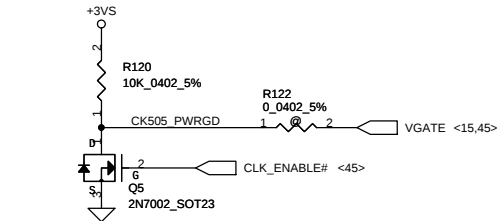
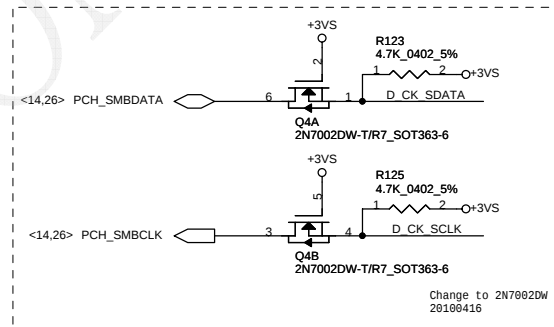
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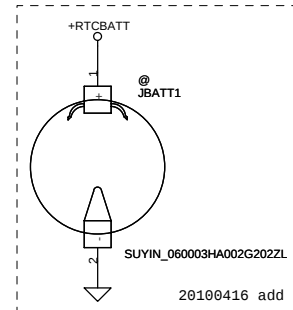
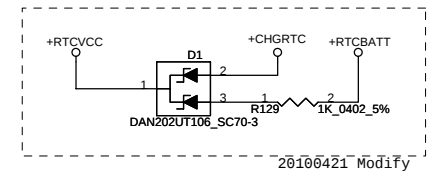
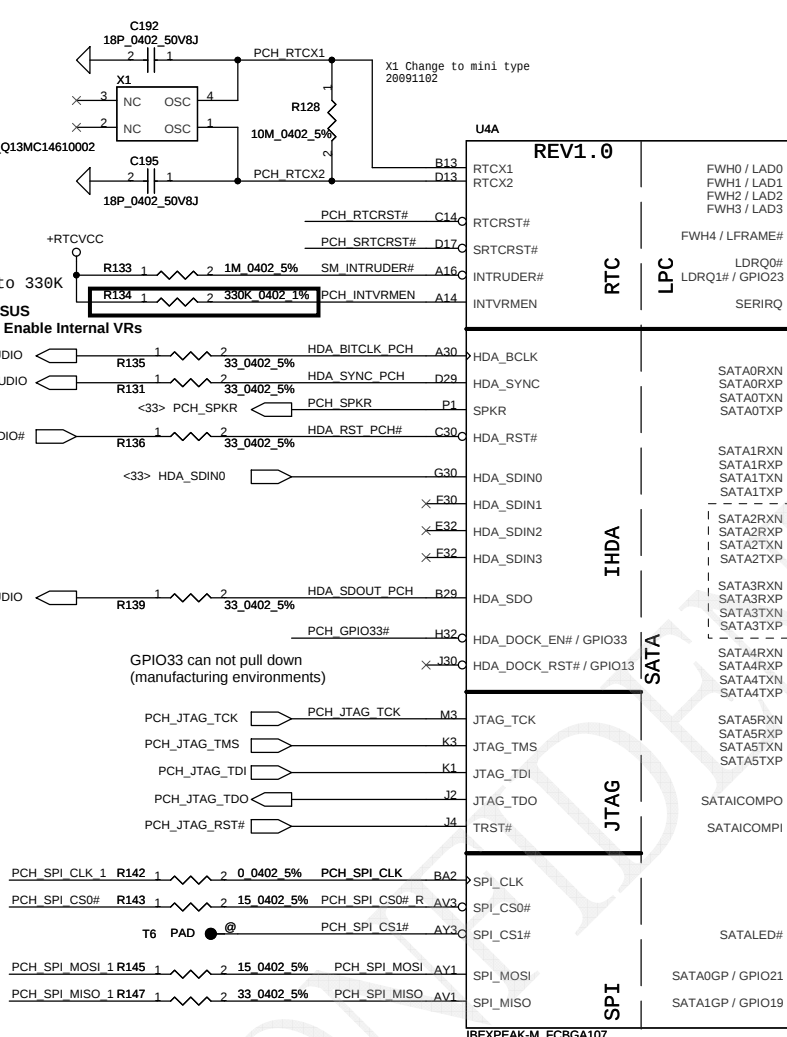
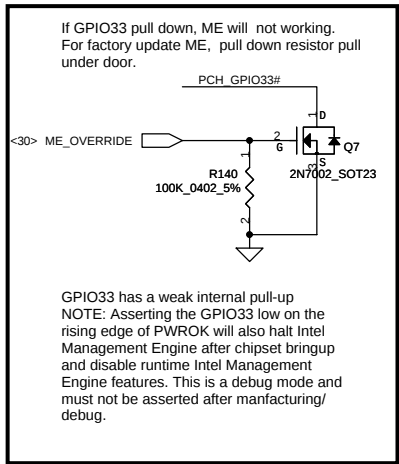
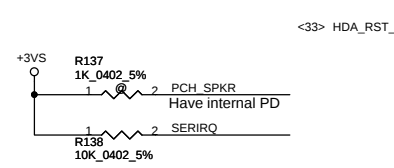
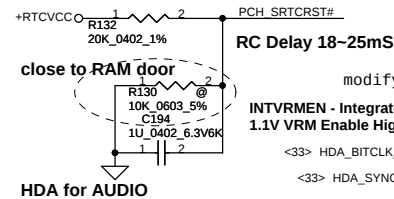
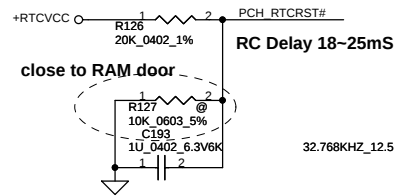
Clock Generator



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

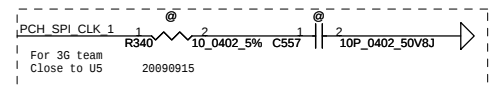
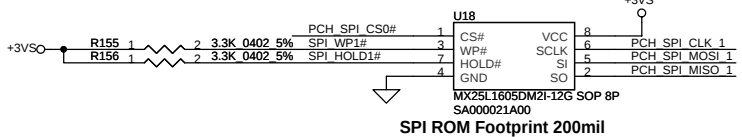
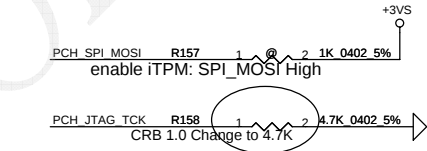
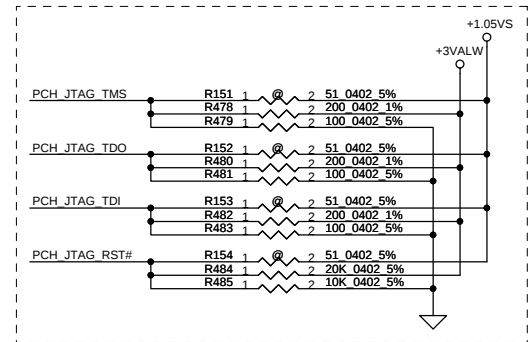
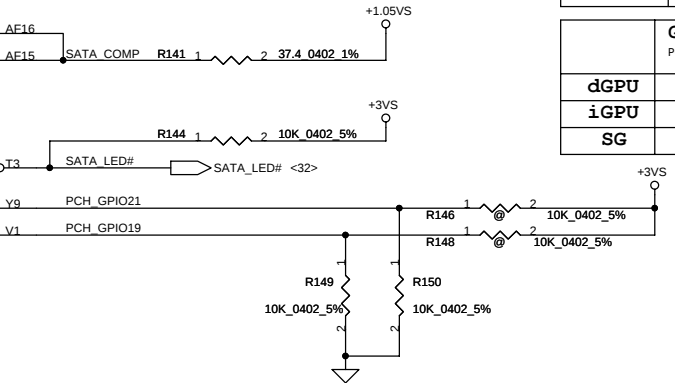


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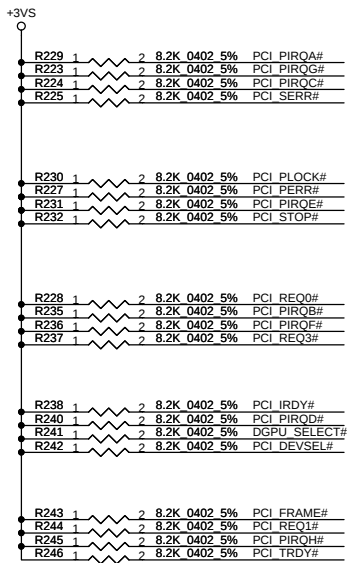


GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRST_L#
dGPU	0	0
iGPU	0	1
SG	1	X



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A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled High=Default *

T11 PAD

T12 PAD

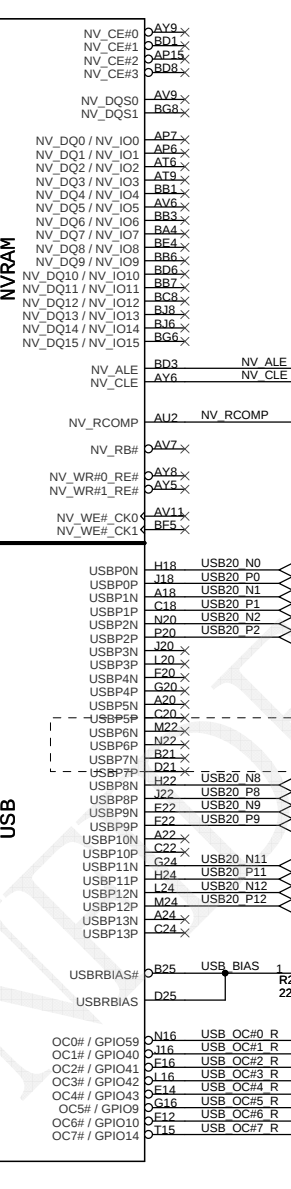
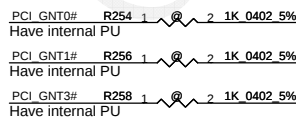
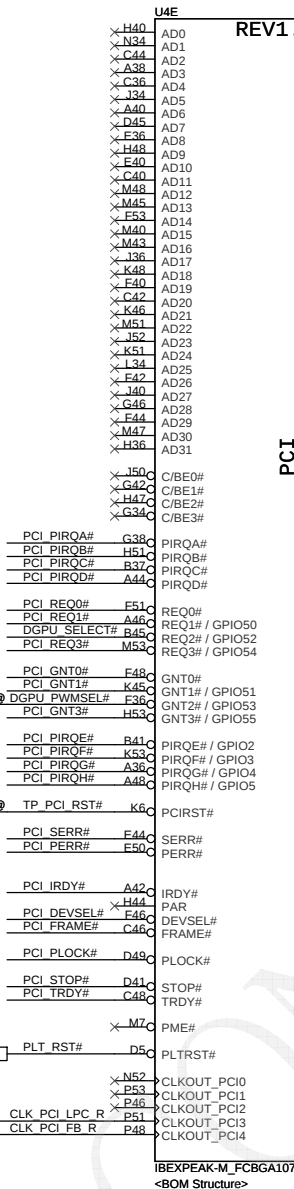
<30> CLK_PCI_LPC
<14> CLK_PCI_FB

2008/1/6 2009MOW01 change to 22 ohm

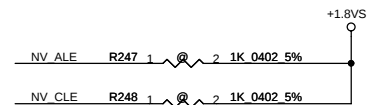
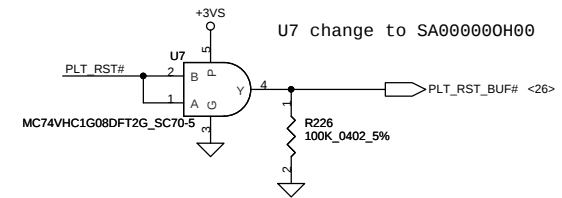
Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3 Low = A16 swap High = Default



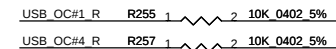
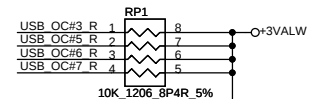
OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2



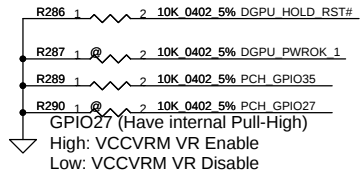
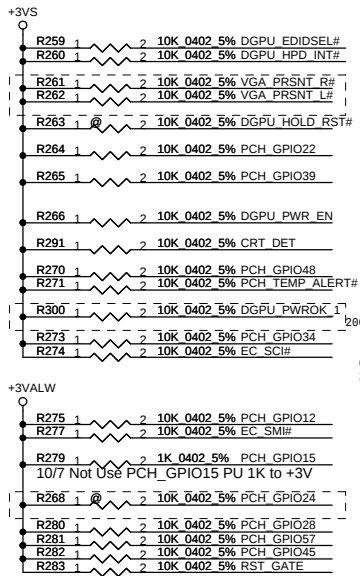
Intel Anti-Theft Techonlogy	
NV_ALE	High=Enabled Low=Disabale(floating)★

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3V5
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE
DMI termination voltage.
weak internal PU, don't PD



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	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO27

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

* H: On-Die voltage regulator enable

L: On-Die PLL Voltage Regulator disable

GPIO8

This signal has a weak internal pull up

can't Pull low

GPIO15

L: Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality

H: Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

it have weak internal PU 20K

GPIO24 change PU +3VS to +3VALW

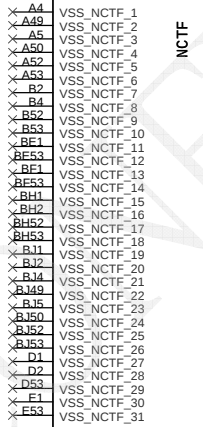
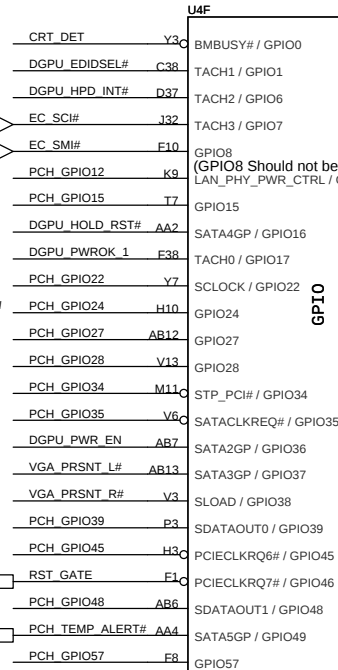
20090916

<30> EC_SCI#

<30> EC_SMI#

<10> RST_GATE

<30> PCH_TEMP_ALERT#



IBEXPEAK-M_FCBGA107

REV1.0

MTSC

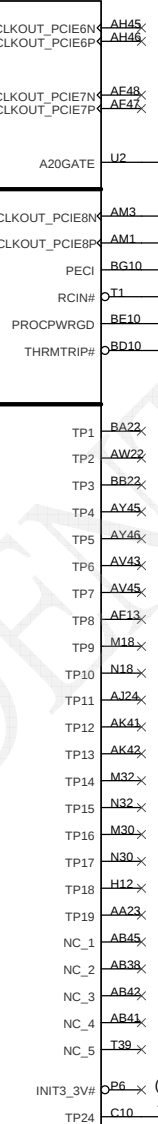
GPIO

CPU

NCTF

RSVD

REV1.0



AH45

AH46

AE48

AE41

AM3

AM1

BG10

T1

BE10

BD10

BA22

AW22

BB22

AY45

AY46

AV43

AV45

AF13

M18

N18

AJ24

AK41

AK42

M32

N32

M30

N30

H12

A23

AB45

AB38

AB42

AB41

T39

INIT3_3V#

TP24

C10

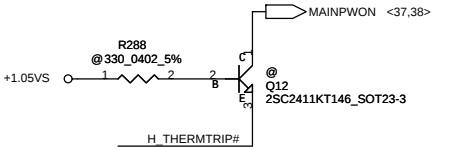
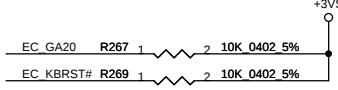
TP24

SST

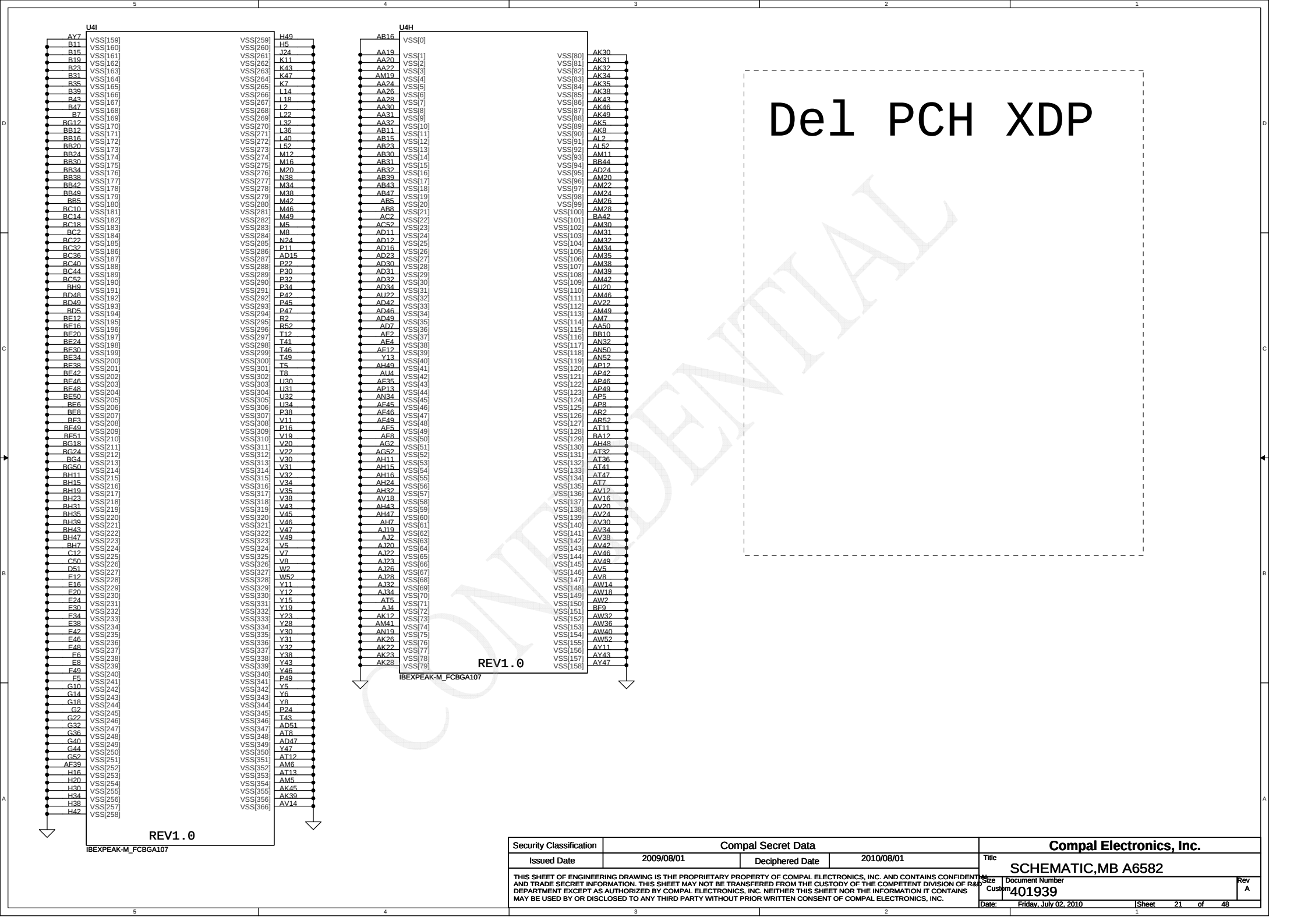
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PAD

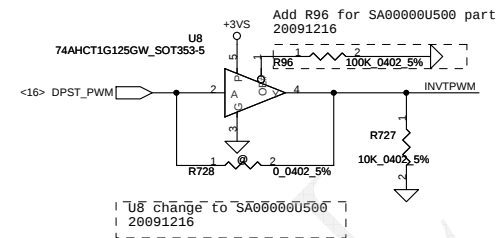
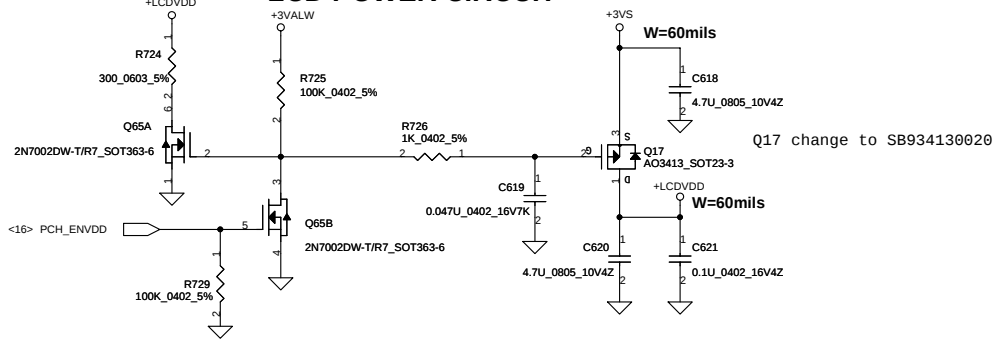
T13



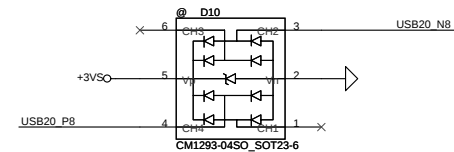
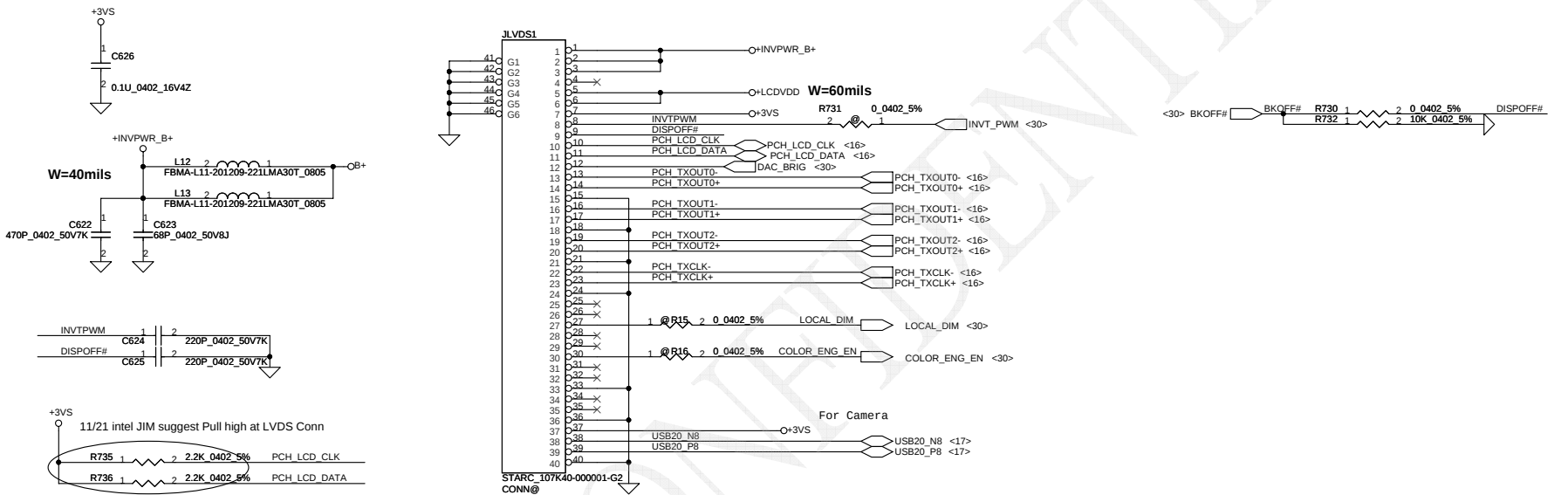
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LCD POWER CIRCUIT

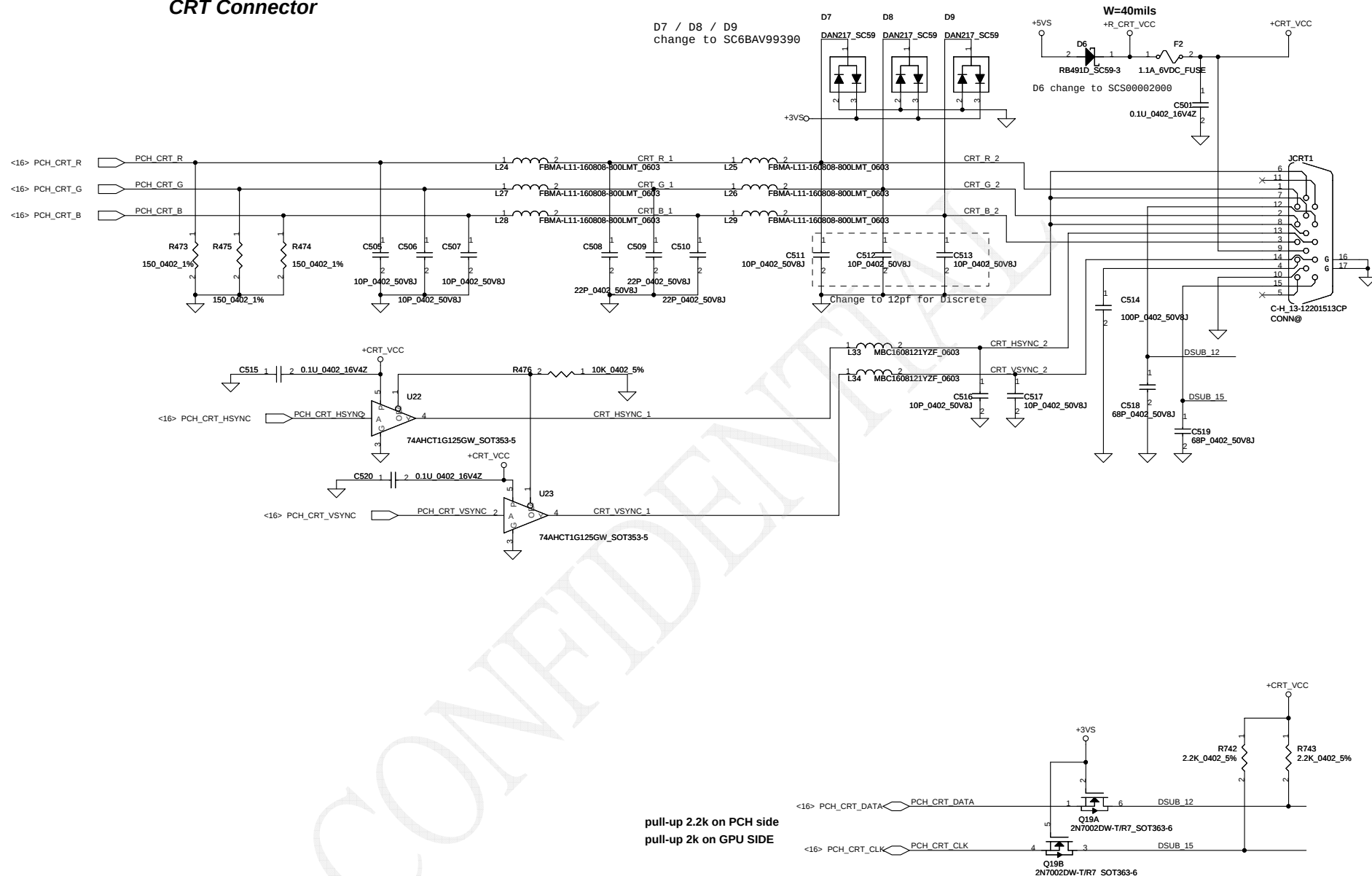


LED PANEL Conn.



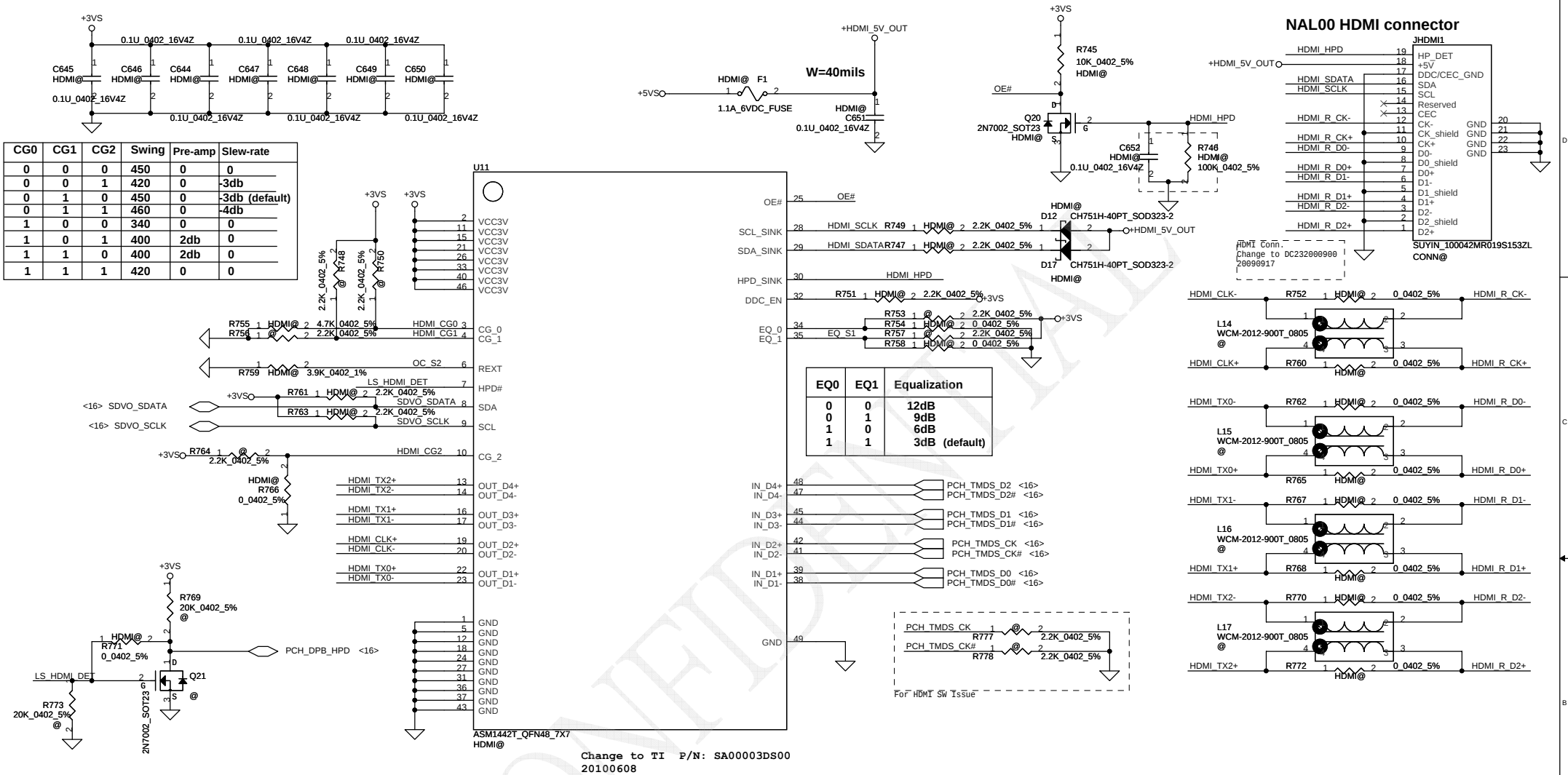
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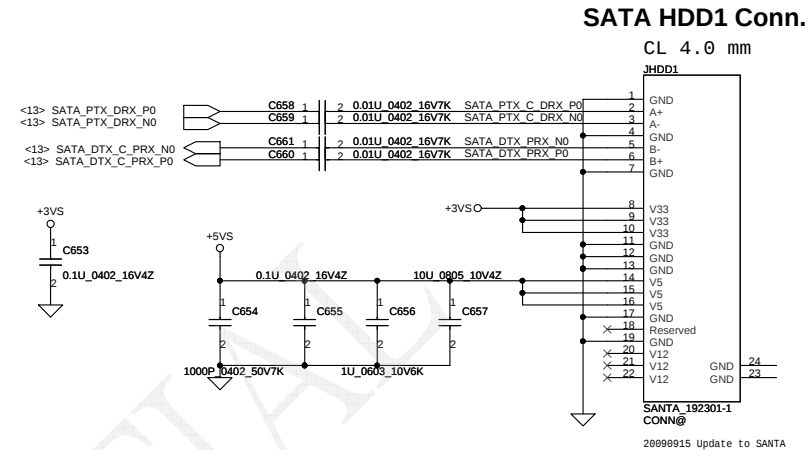
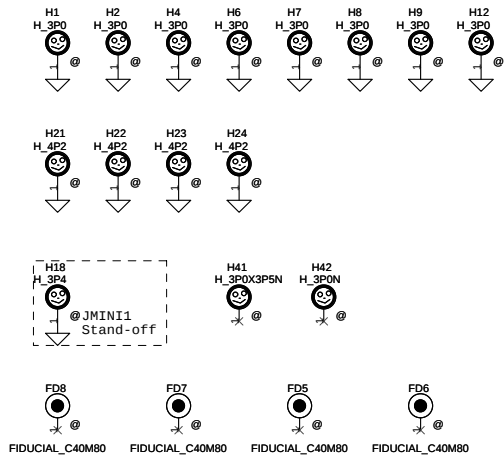
CRT Connector



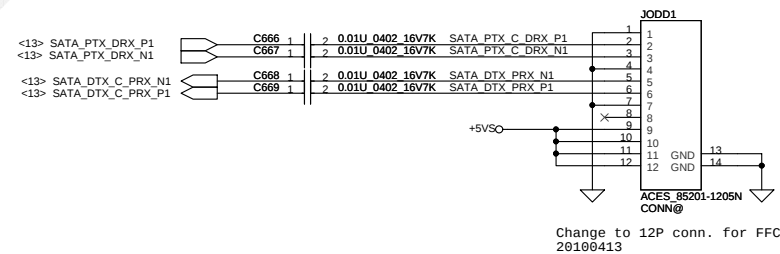
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CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0



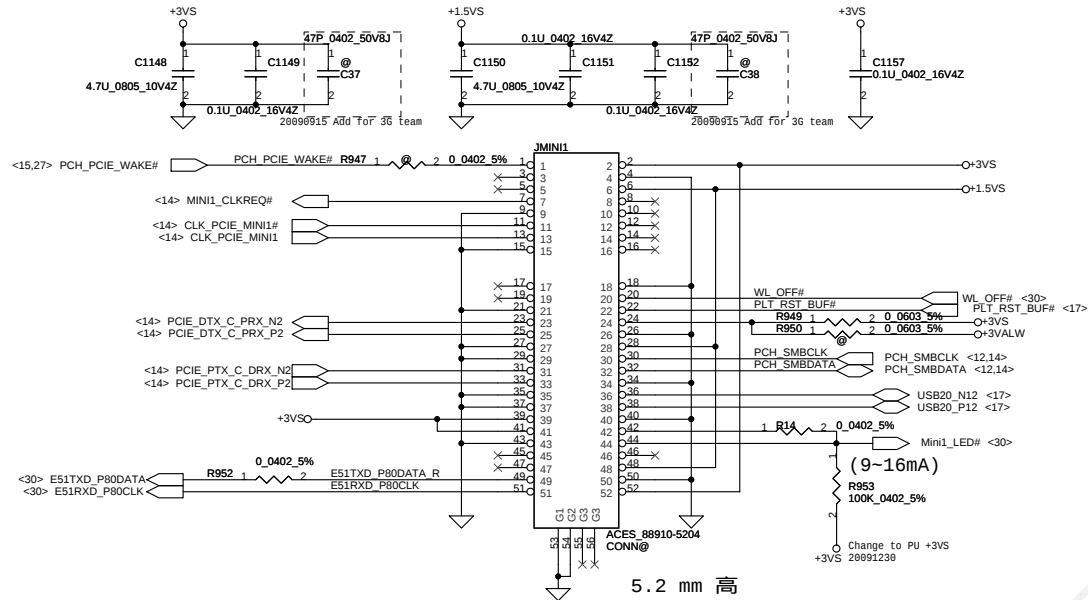


SATA ODD
FFC Conn.



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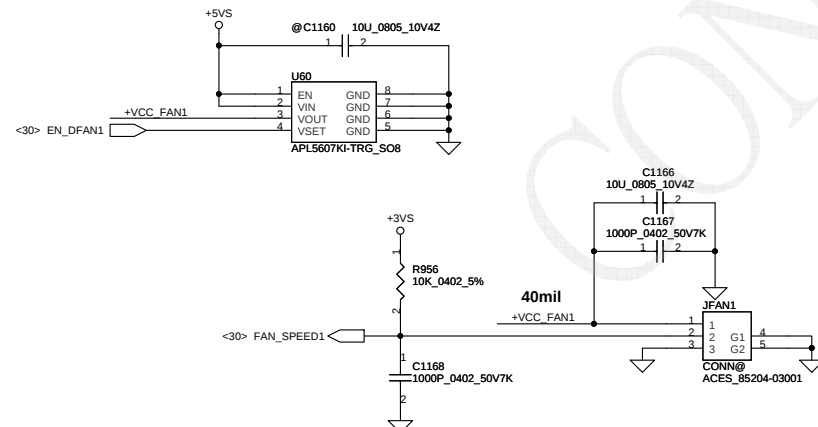
For Wireless LAN



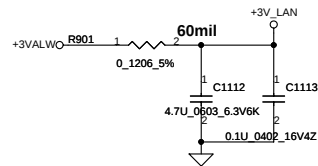
Del 3G / GPS Module Connect

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

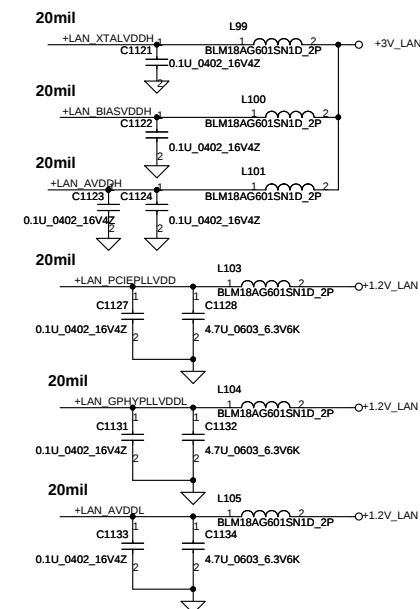
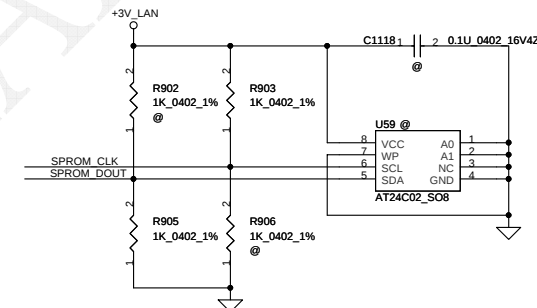
FAN1 Conn



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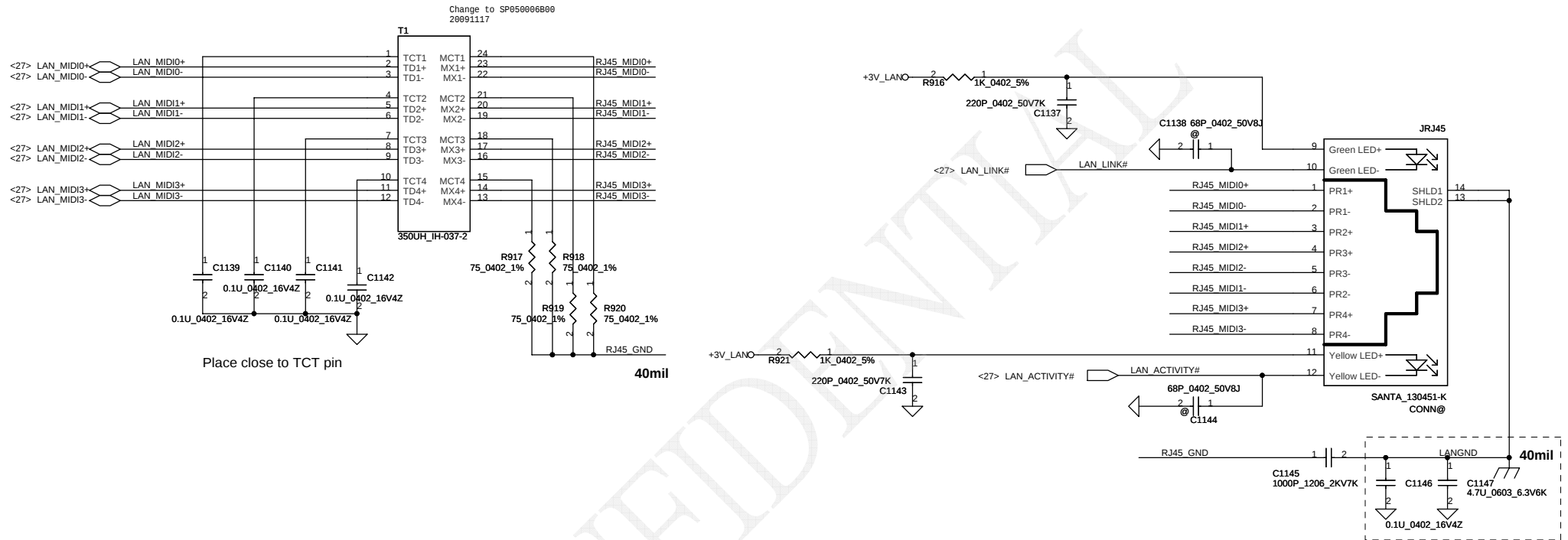


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



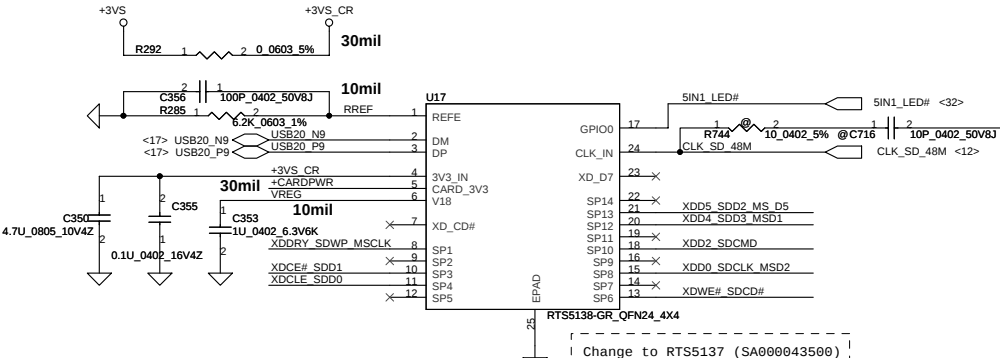
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LAN Connector

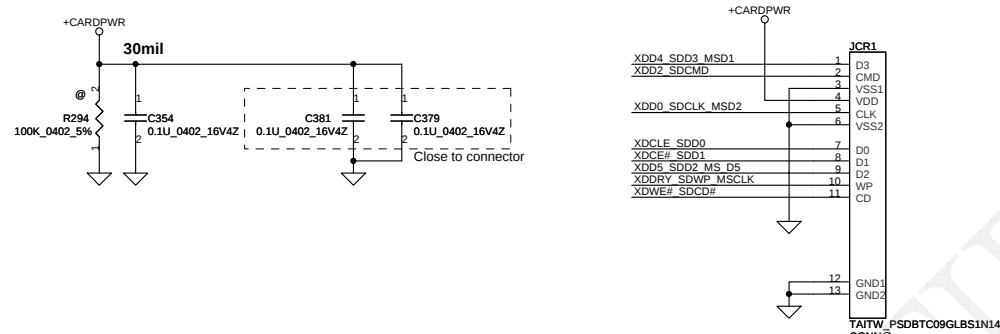


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Card Reader RTS5138 / RTS5137
(only SD+MMC function)

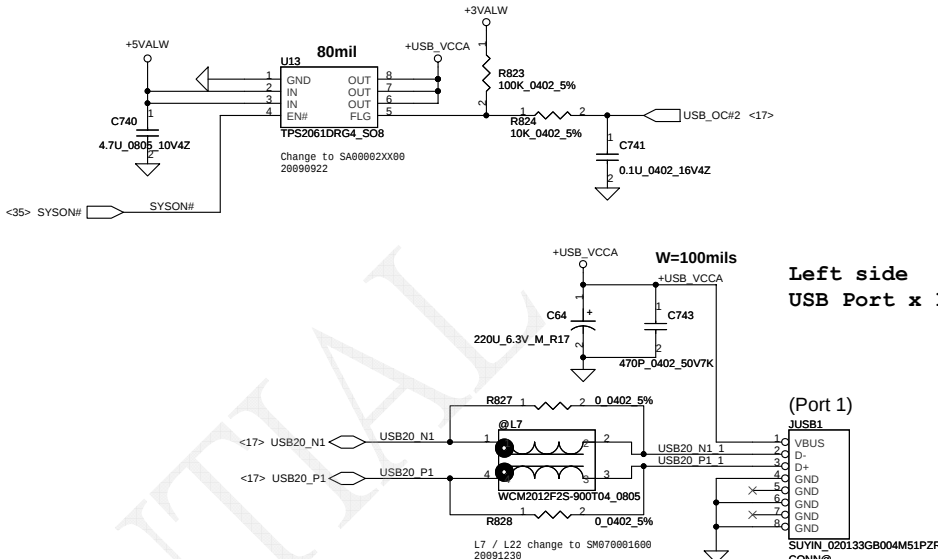
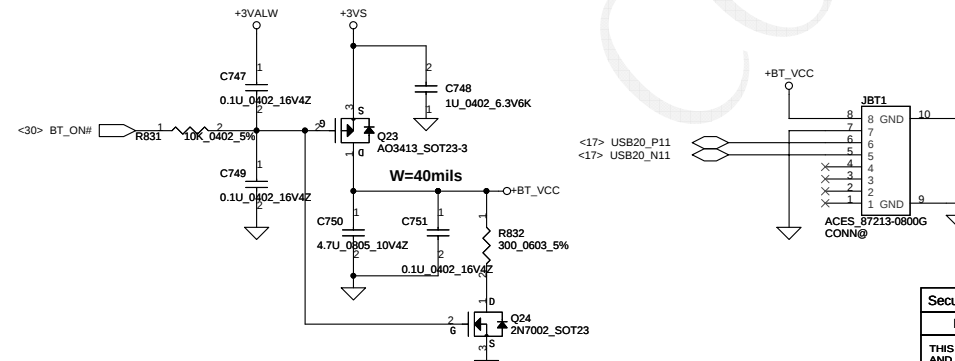


Card Reader Connector



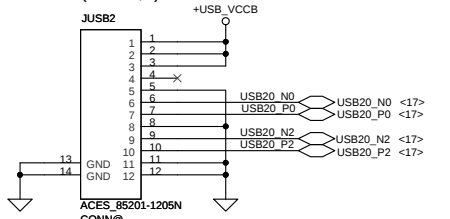
Bluetooth Conn.

Q23 change to SB934130020

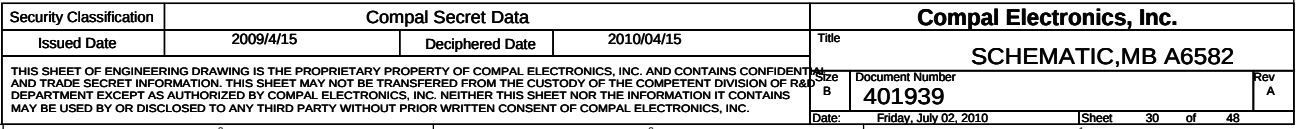


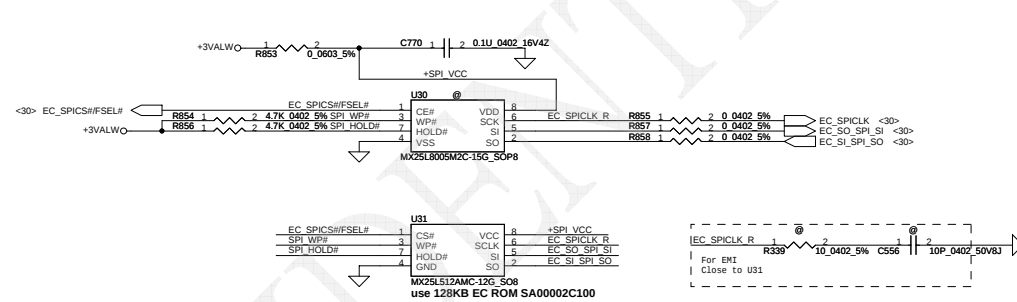
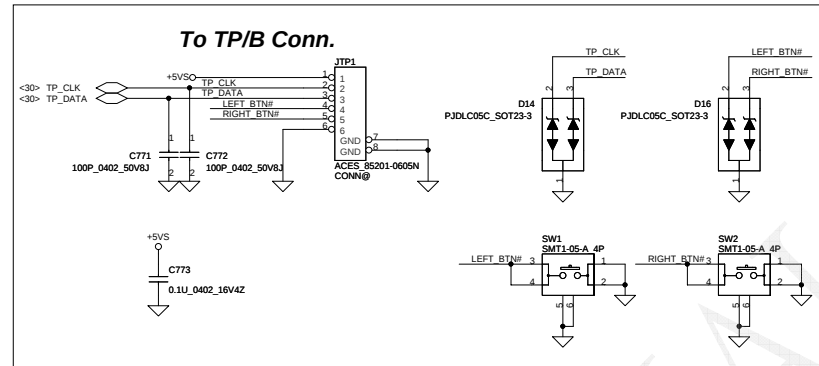
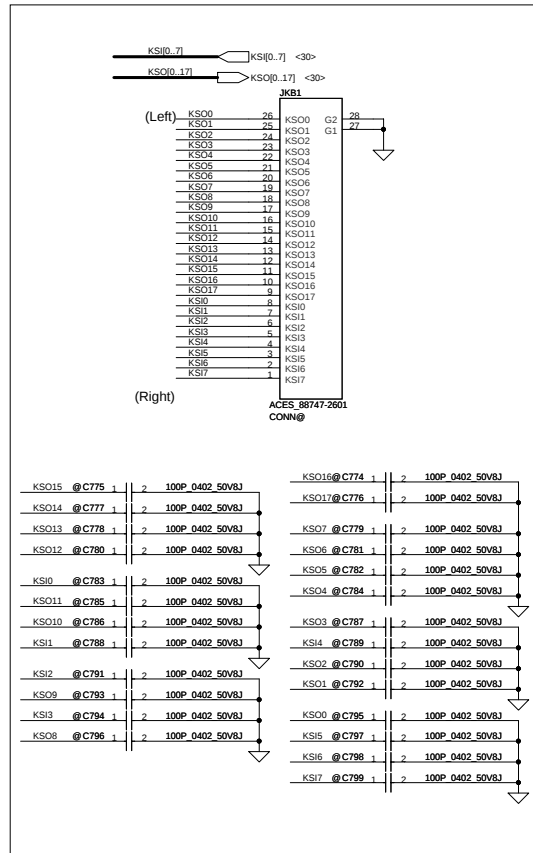
USB/B Conn.

(Port 0,2)



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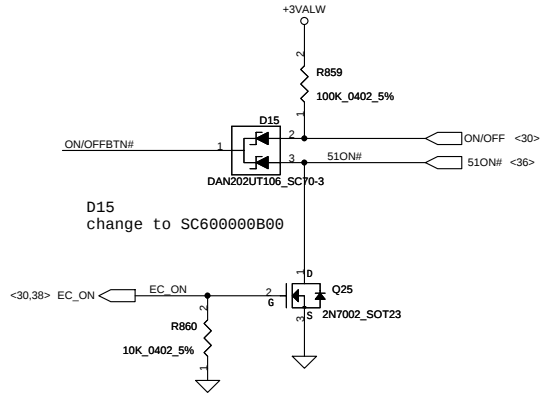


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

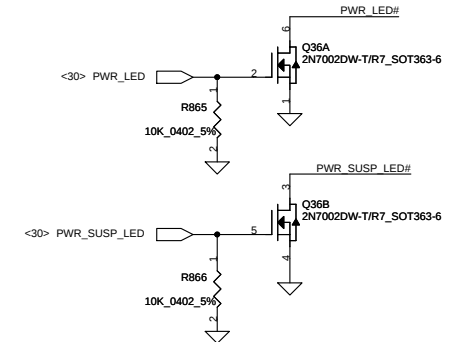
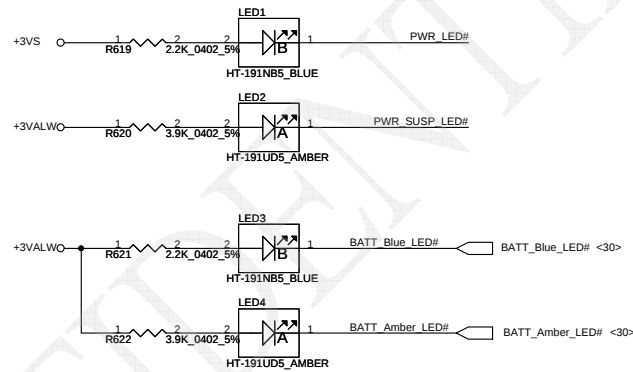
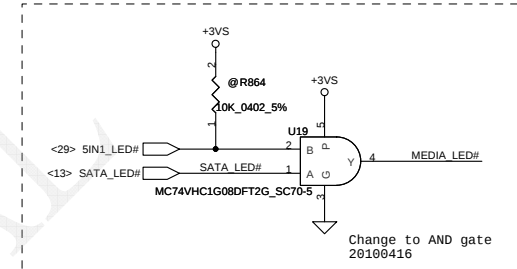
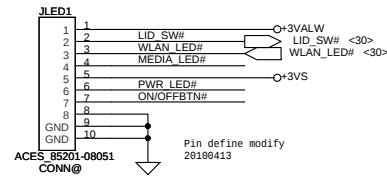
To BTN/B Conn.

KSO0	KSO3
KS11	WL_BTN#
KS12	T/P lock_BTN#
KS13	Back up_BTN#
KS14	BT_BTN#
KS15	Power save_BTN#
	Program_BTN#
	Volum up_BTN#
	Volum down_BTN#

Power Button

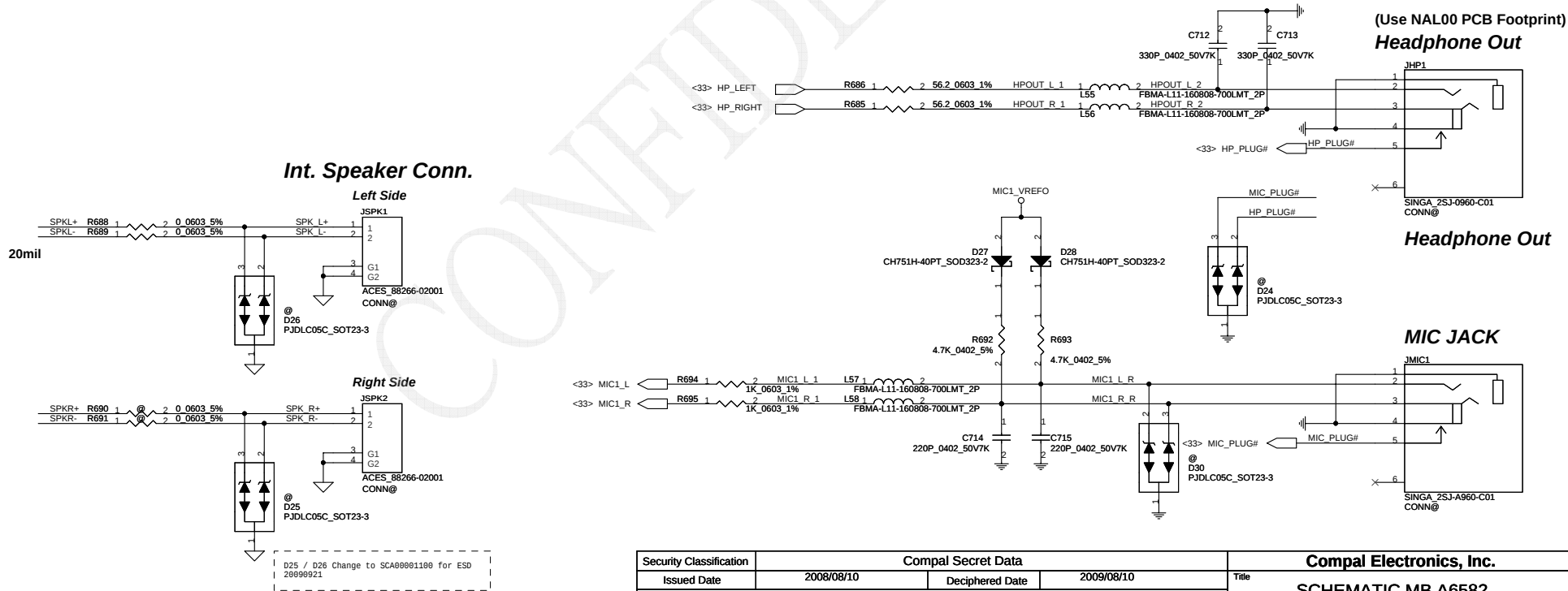
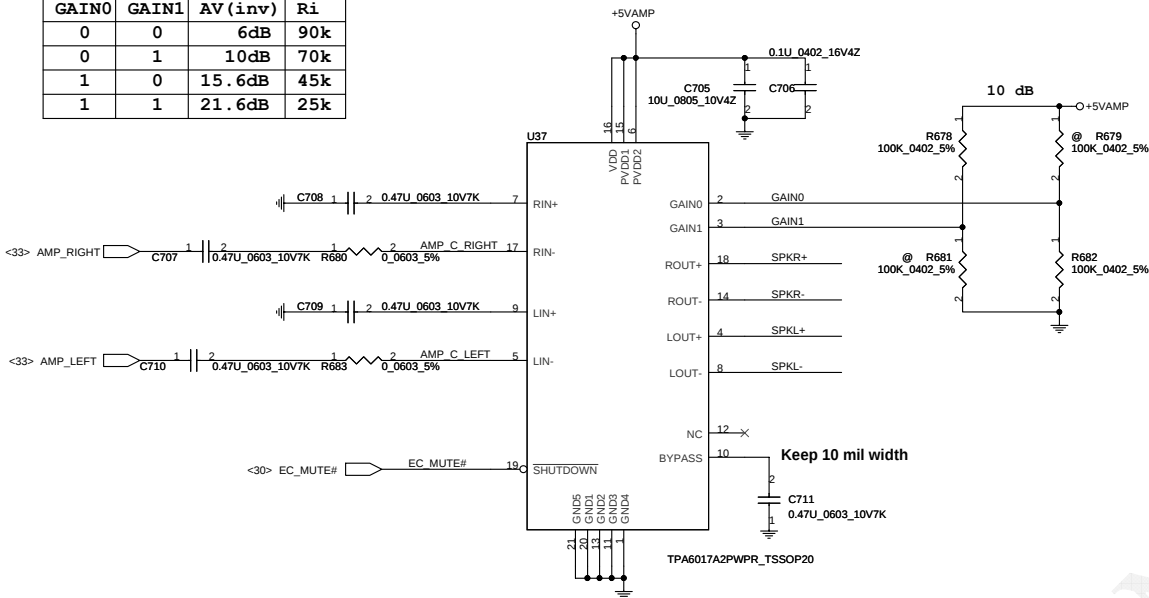


LED/B LEFT



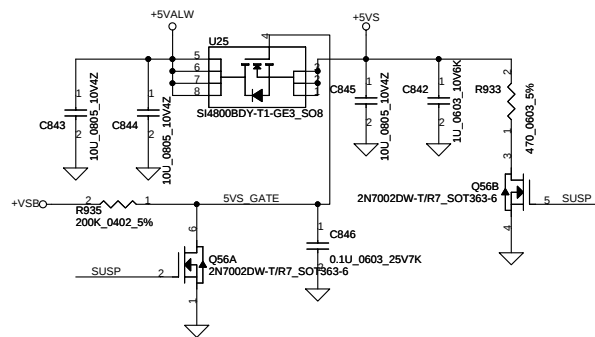
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GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

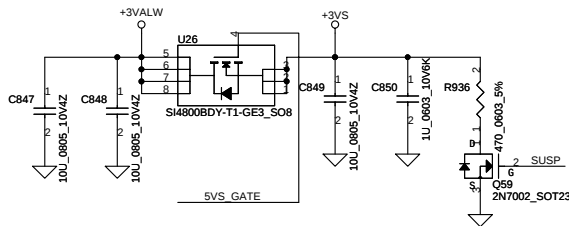


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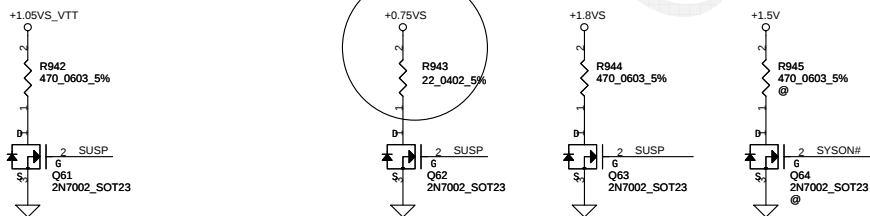
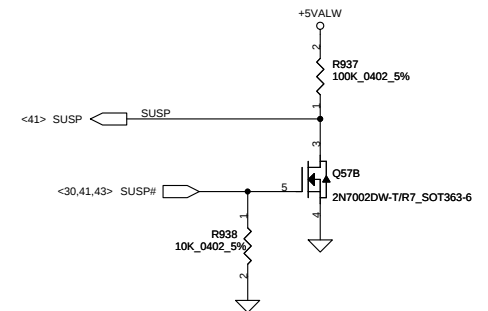
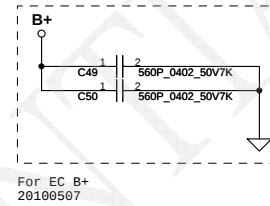
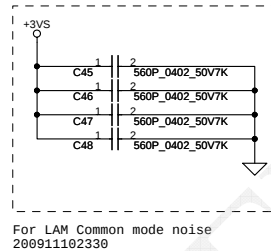
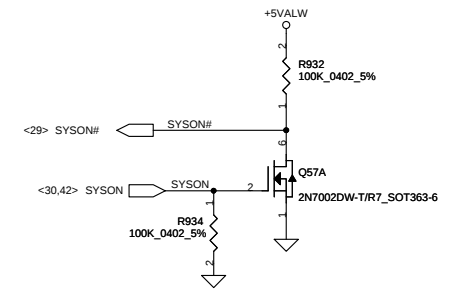
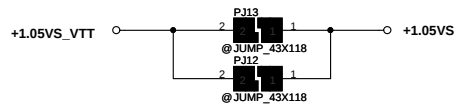
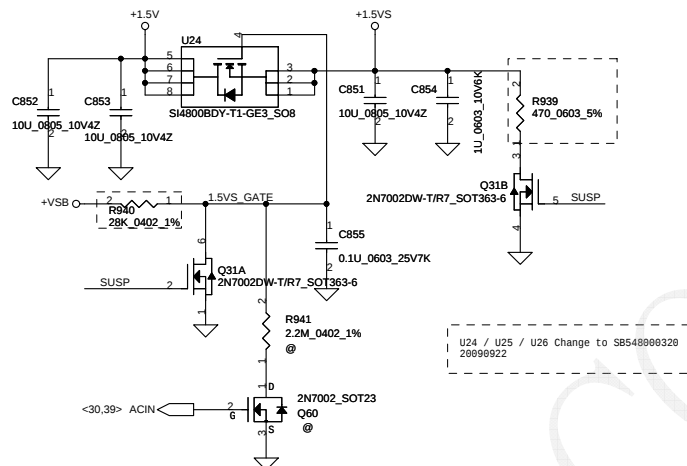
+5VALW TO +5VS



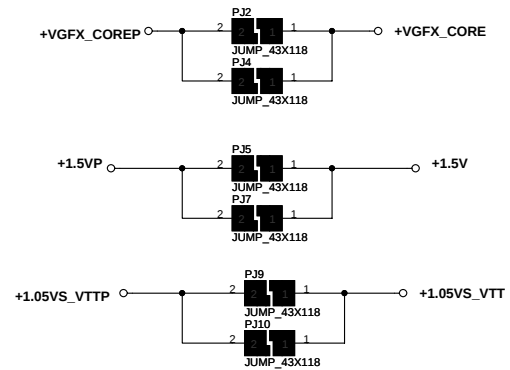
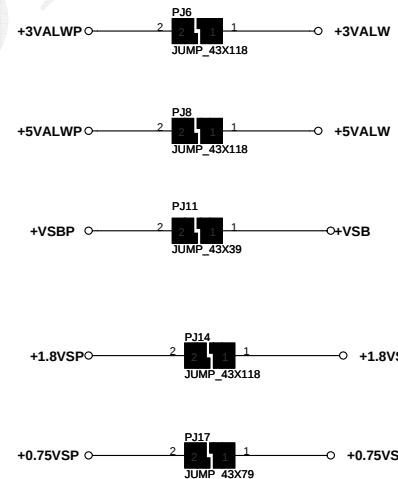
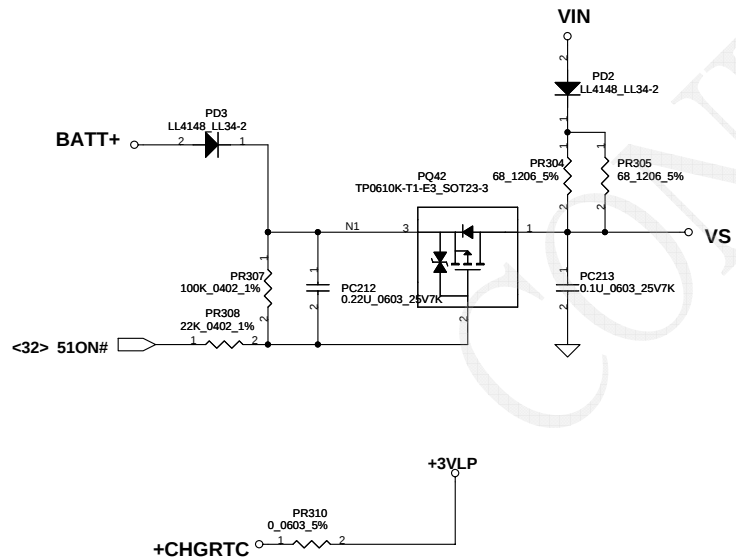
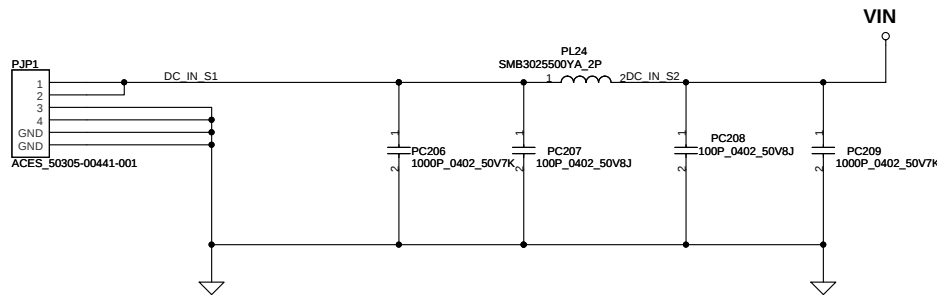
+3VALW TO +3VS



+1.5V to +1.5VS

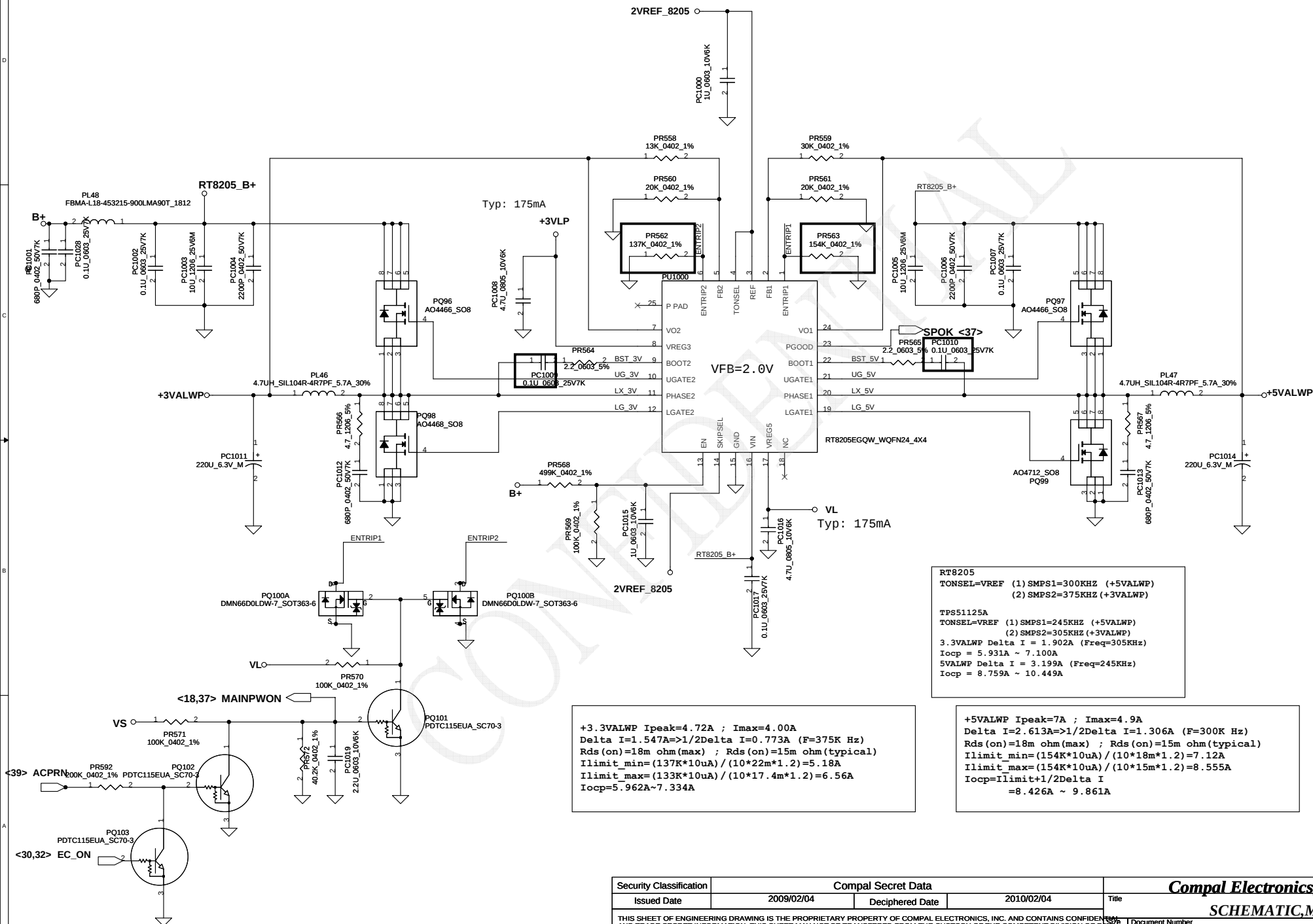


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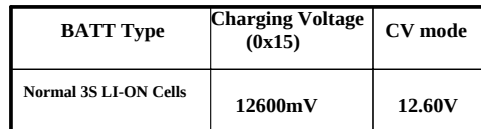


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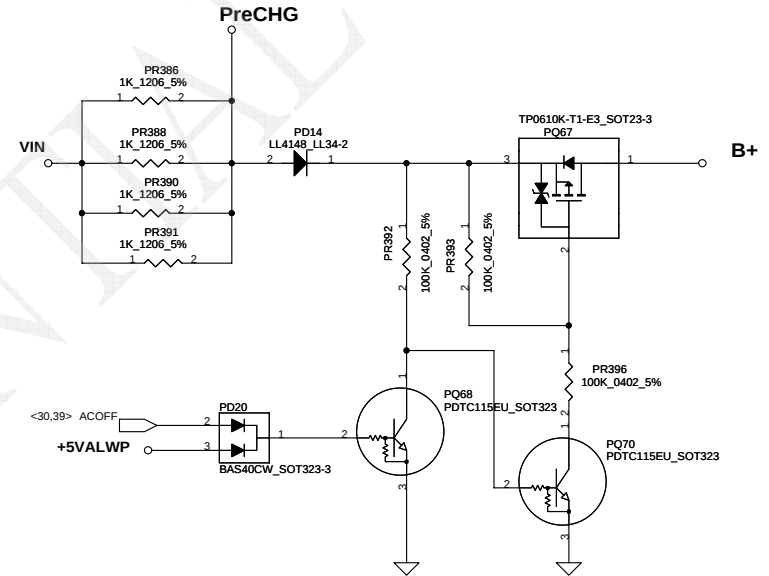
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



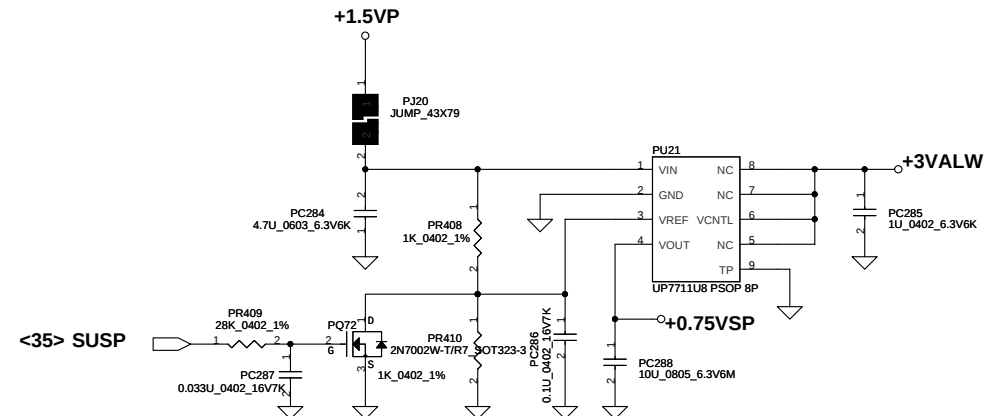
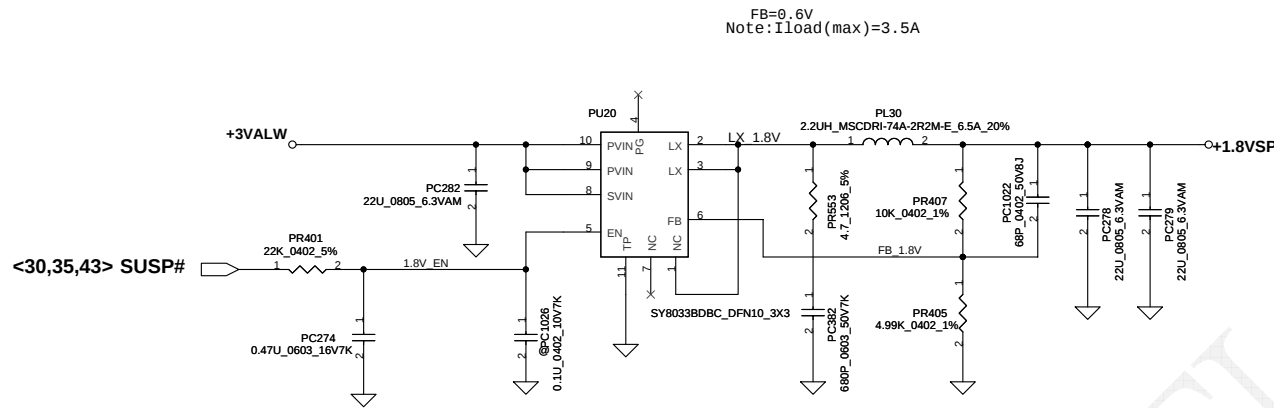
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$$\begin{aligned} \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 4.07\text{A} \\ \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 2.91\text{A} \end{aligned}$$


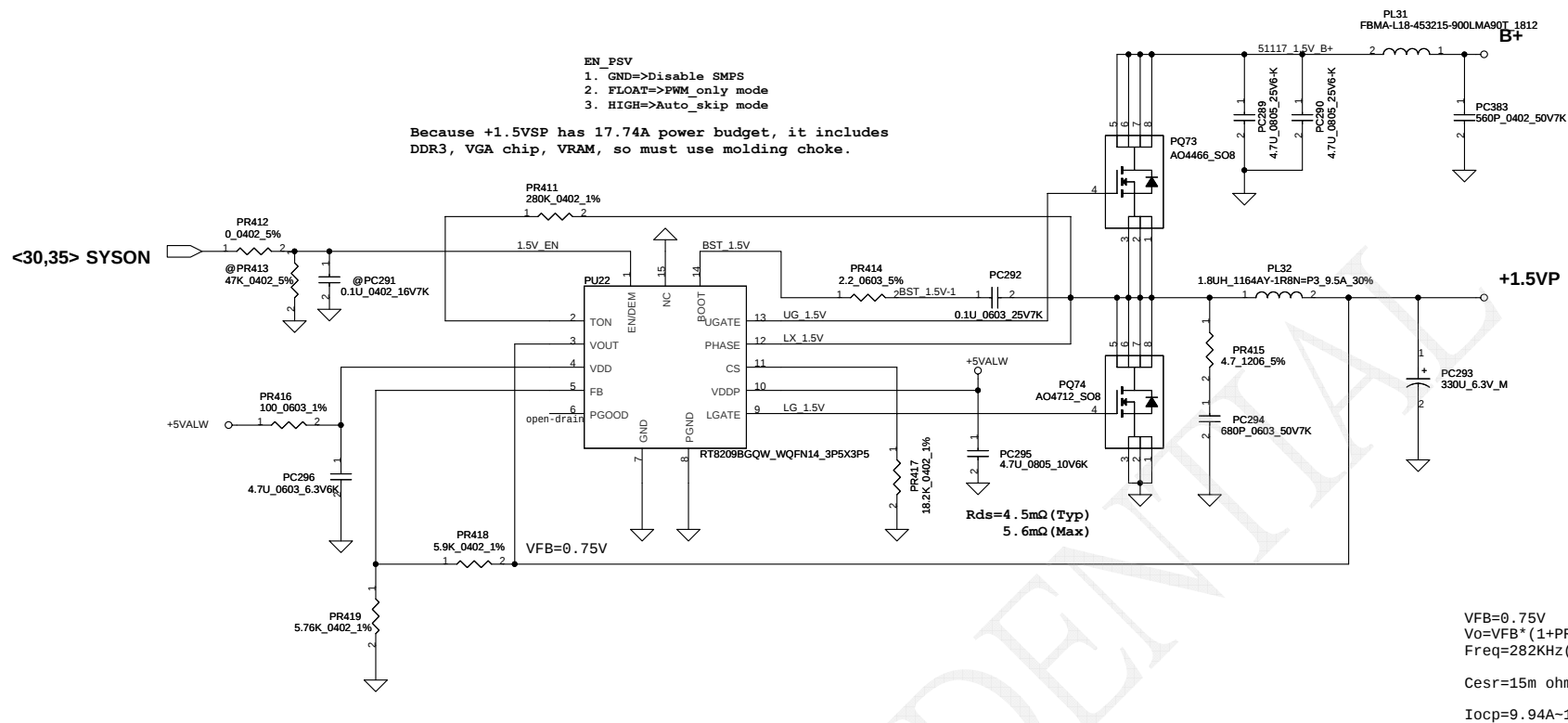
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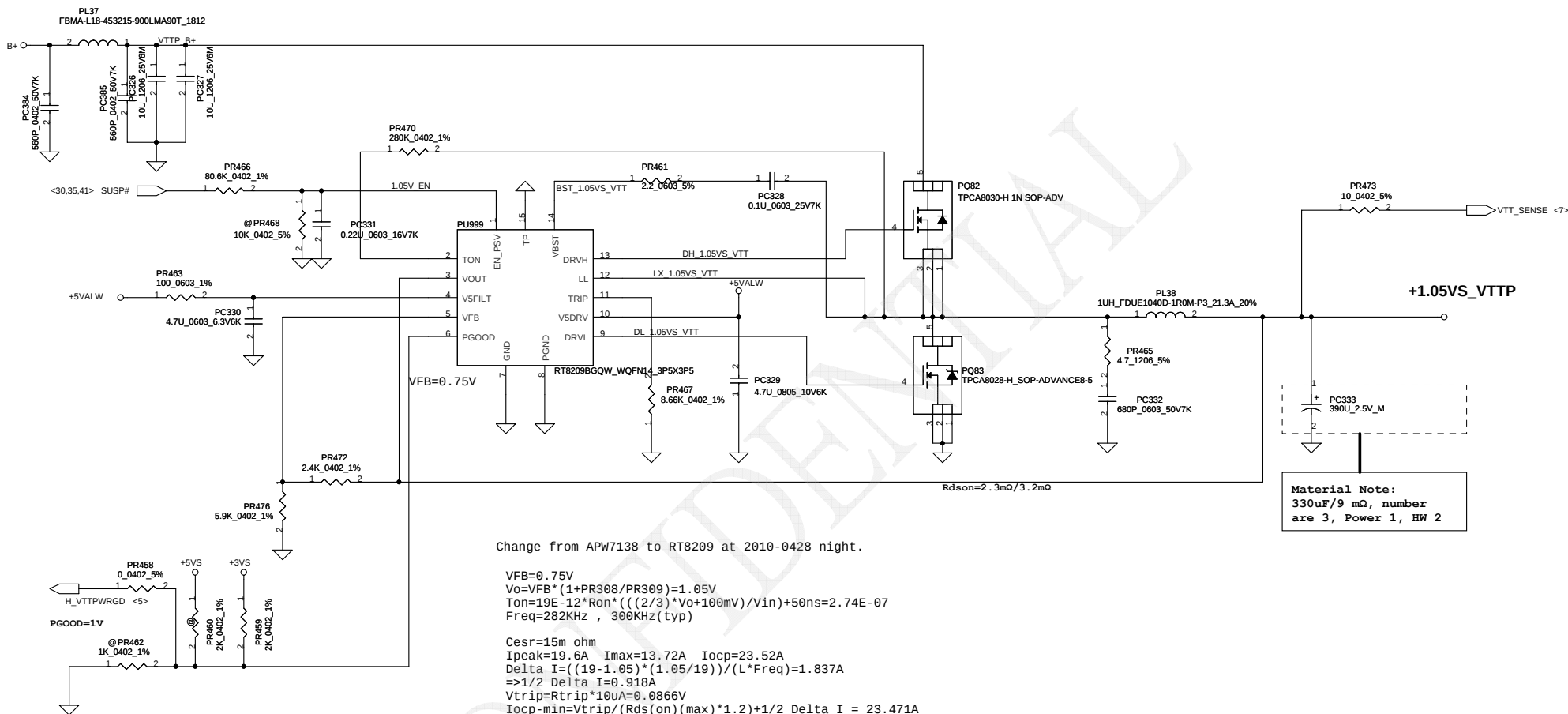
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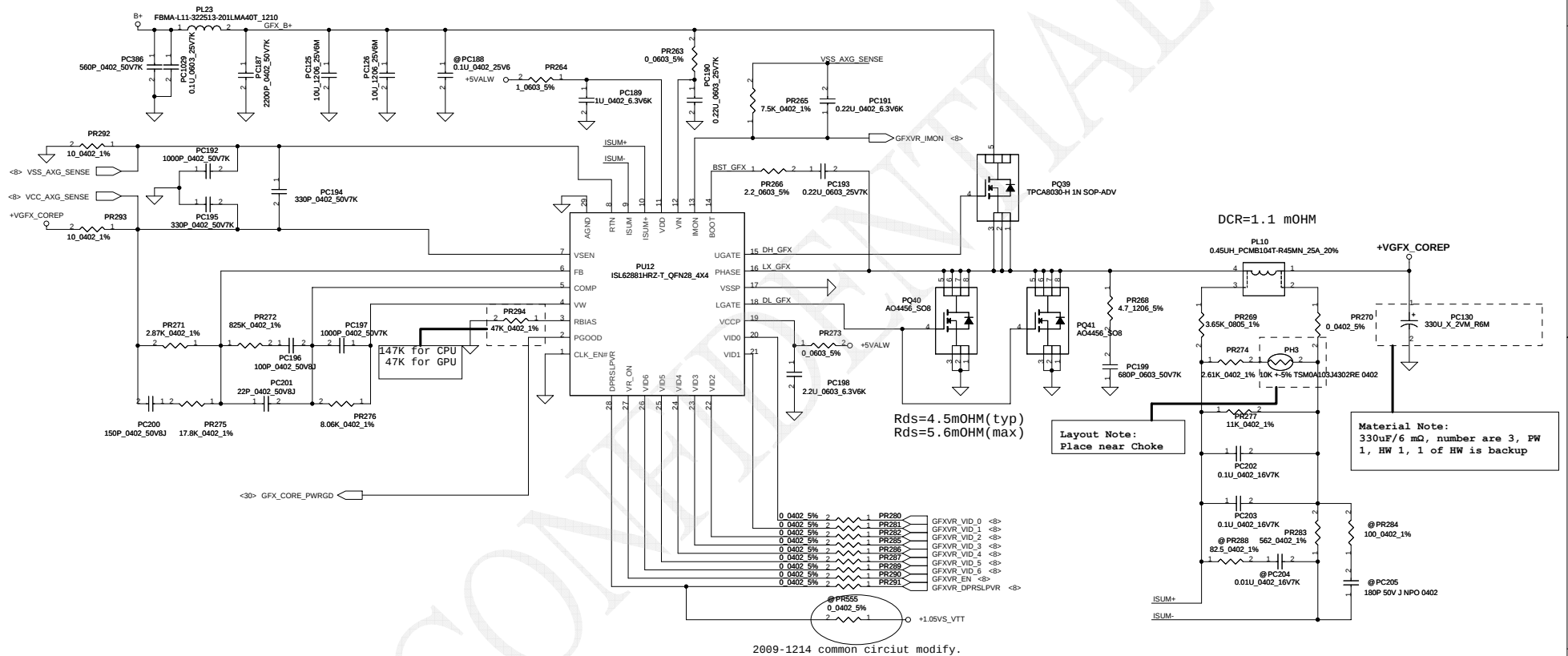


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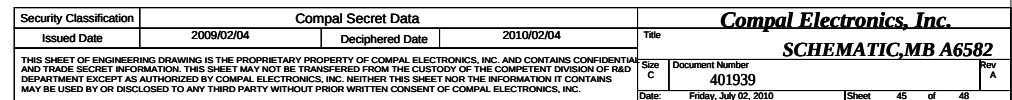
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Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k\ ohm$
 $Rsum=PR269=3.65k\ ohm$
 $LL=2*Rdroop*G1*DCR/Ri=6.96m\ V/A$
 where $Rdroop=PR271=8.66k\ ohm$, $Ri=PR283=1.69k\ ohm$
 $Iocp=OCP\ Threshold*Rdroop/LL=24.89A$



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	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dy
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Pre-Charge circuit update.	Pre-Charge circuit disable in EVT, now modify and enable it.	0.1	39	Change PR353 from SD034470280 to SD034200380.	2010/06/08	to PVT
2					Change PR371 from SD034220280 to SD034470280.		
3					Change PR587 from SD034100380 to SD034470280.		
4	Pre-Charge circuit update.	Pre-Charge circuit disable in EVT, now modify and enable it.	0.1	38	Change PR590 from SD034200280 to SD034143280.	2010/06/08	to PVT
5	Pre-Charge circuit update.	Pre-Charge circuit disable in EVT, now modify and enable it.	0.1	40	Change PR591 from SD028470280 to SD028100380.		
6	Pre-Charge circuit update.	Pre-Charge circuit disable in EVT, now modify and enable it.	0.1	40	Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K)		
7	EMI fail, add 3/5V snubber and Boost Resister to solve it.	EMI request to solve EMI issue.	0.1	38	Change PQ111 from SB000006800 to SB301150200	2010/06/08	to PVT
8	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Add PQ102 and PQ103 SB301150200.		
9	EMI fail, add 1.05V snubber and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PR592 SD034200380.		
10	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Change PR386 from SD011000080 to SD011100180.	2010/06/08	to PVT
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PR388, PR390, PR391 SD011100180.		
12	HW power sequence modify.	HW request.	0.1	43	Add PD14 SC100001Y80 LL4148_LL34-2		
13	BOM unique.	BOM unique.	0.1	38	Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5%	2010/06/08	to PVT
14	EMI request.	EMI request.	0.1	38	Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K		
15	EMI request.	EMI request.	0.1	44	Change PR564 and PR565 from SD013000080 to SD013220B80		
16	Sourcer request to change a common part.	Sourcer request.	0.1	38	Add PR415 SD001470B80 4.7 1206 5%.	2010/06/08	to PVT
17	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603		
18	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Add PR465 SD001470B80 4.7 1206 5%.		
19	Per sourcer request.	Per sourcer request.	0.1	43	Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
20	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38	Change PR461 from SD013000080 to SD013220B80		
21	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Add PR268 SD001470B80 4.7 1206 5%.		
22	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%)		
					Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402		
					chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
					Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
					Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
					Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
					change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
					Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
					chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
					Change PQ98 from SB00000AJ00 to SB000009580(A04468).	2010/06/08	to PVT
					Change PQ64 from SB00000CG00 to SB000009580(A04468).	2010/06/08	to PVT
					chnage PQ74 from SB000009F80 to SB00000AJ00(A04712).	2010/06/08	to PVT
					CHnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
					Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
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Version change list (P. I. R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08 04 / 16 04 / 21 04 / 26 04 / 27 04 / 29 04 / 29 05 / 03 05 / 03 05 / 06 05 / 07 05 / 10 05 / 11 05 / 12 05 / 13	N/A Modify RTC SCH Change LAN to AR8152 Update Power SCH Update AND Gate symbol - U1 / U2 / U6 / U7 / U19 Update Power MOS symbol - U24 / U25 / U26 C196 change to 1U for INTEL disign CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function) Q4+Q6 change to 2N7002DW Update U8 symbol Add DMIC function Modify USB define. Update Power SCH Add R17 for DMIC power Update Power SCH Change LAN to GIGA&10/100 co-lay Del R307 (LVDS conn.) Change +1.05VS_VTT to +1.05VS (CLK GEN) Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K Change R940 to 28K (S3 Power sequence) SW T1 pin define (LAN) Change R907 (0.0603) to 0.1206 5% Remove C40 / C41 / C42 / C43 / C44 Change FAN Conn. Update Power SCH Change LAN to BCM57780 GIGA Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO) Del DMIC Update Power SCH Update Power SCH Add C49 / C50 (EC B+) Update Power SCH C764 / C765 change to 18P_0402_50V8J (EC) Reserve D13 / D24 / D30 (ESD) U17 change to RTS5137 (SA000043500) Card reader Update Power SCH	
			06 / 01 06 / 02 06 / 03 06 / 04 06 / 10	Unpop L11 / C247 & Pop R304 for cost down Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal Pop R834 & R835 change to 200K for Project ID Unpop D24 / D30 Unpop R690 / R691 Pop C49 / C50 For HDMI Unpop R753 / R757 , Add R754 / R758 to 0 ohm. Change R759 to 3.9K. Change R755 to 4.7K ohm , Unpop R748. Unpop R778. R833 / R292 0.0805 change to 0.0603. C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report Unpop C774-C799 for EMI cost down. Update Power SCH Add T25 / T26 / T27	