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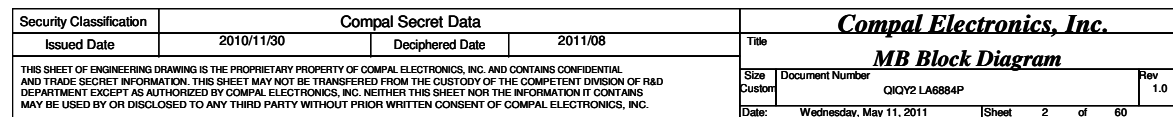
QIQY2 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATi Whistler XT+DDR3

2011-05-11

REV: 1.0

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Voltage Rails

power plane				
State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	✗	✗	✗	✗	✗	✗	✓ +3VS
SMBCLK SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✓ +3VS	✗	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VS	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb

EC SM Bus2 address

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	
Camera	CMOS@

VRAM BOM Config

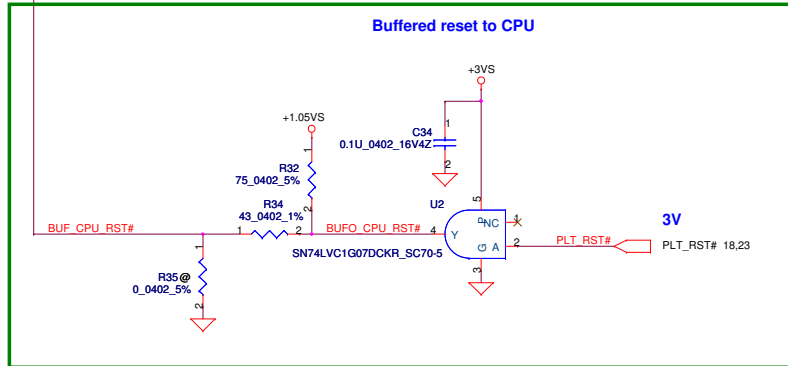
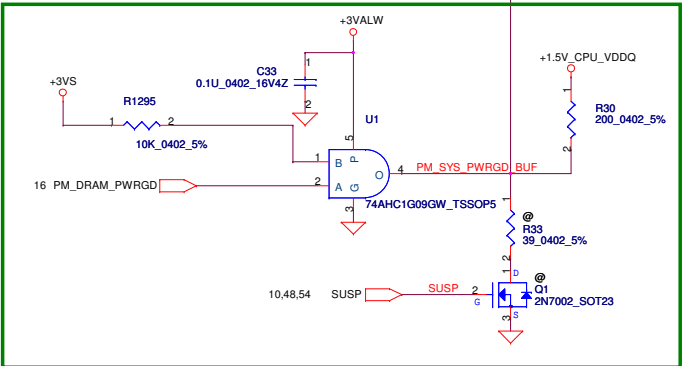
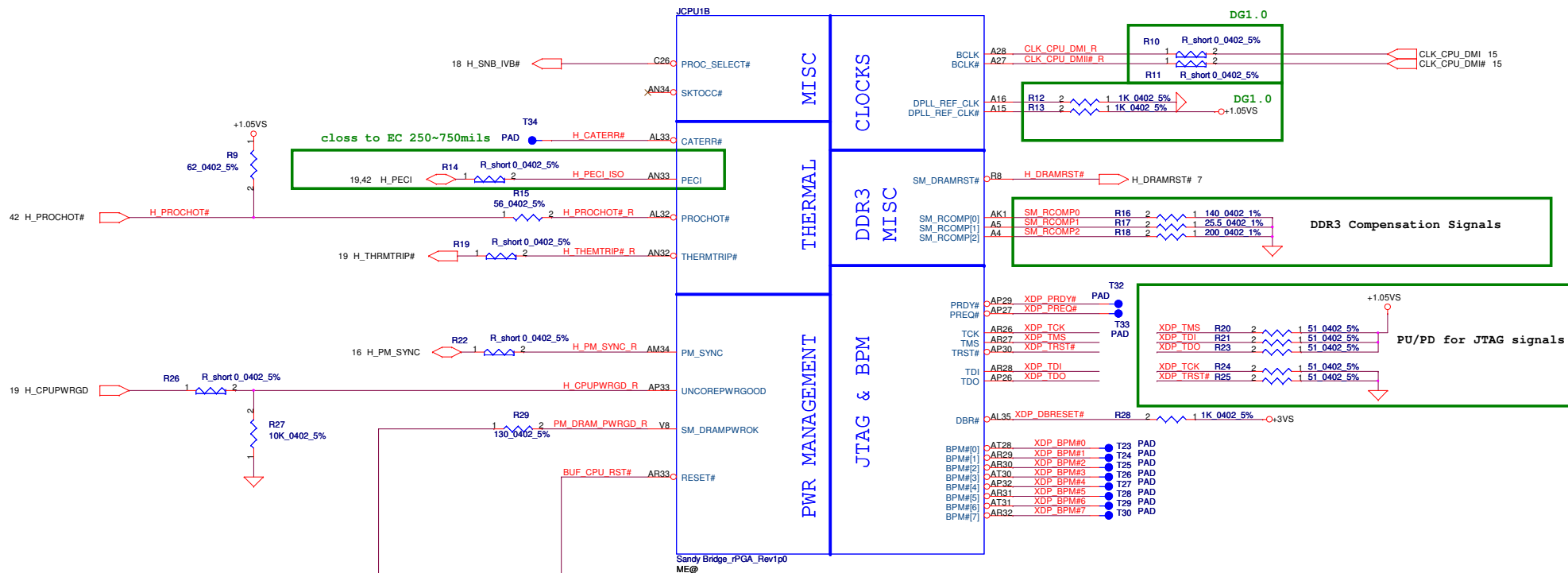
X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

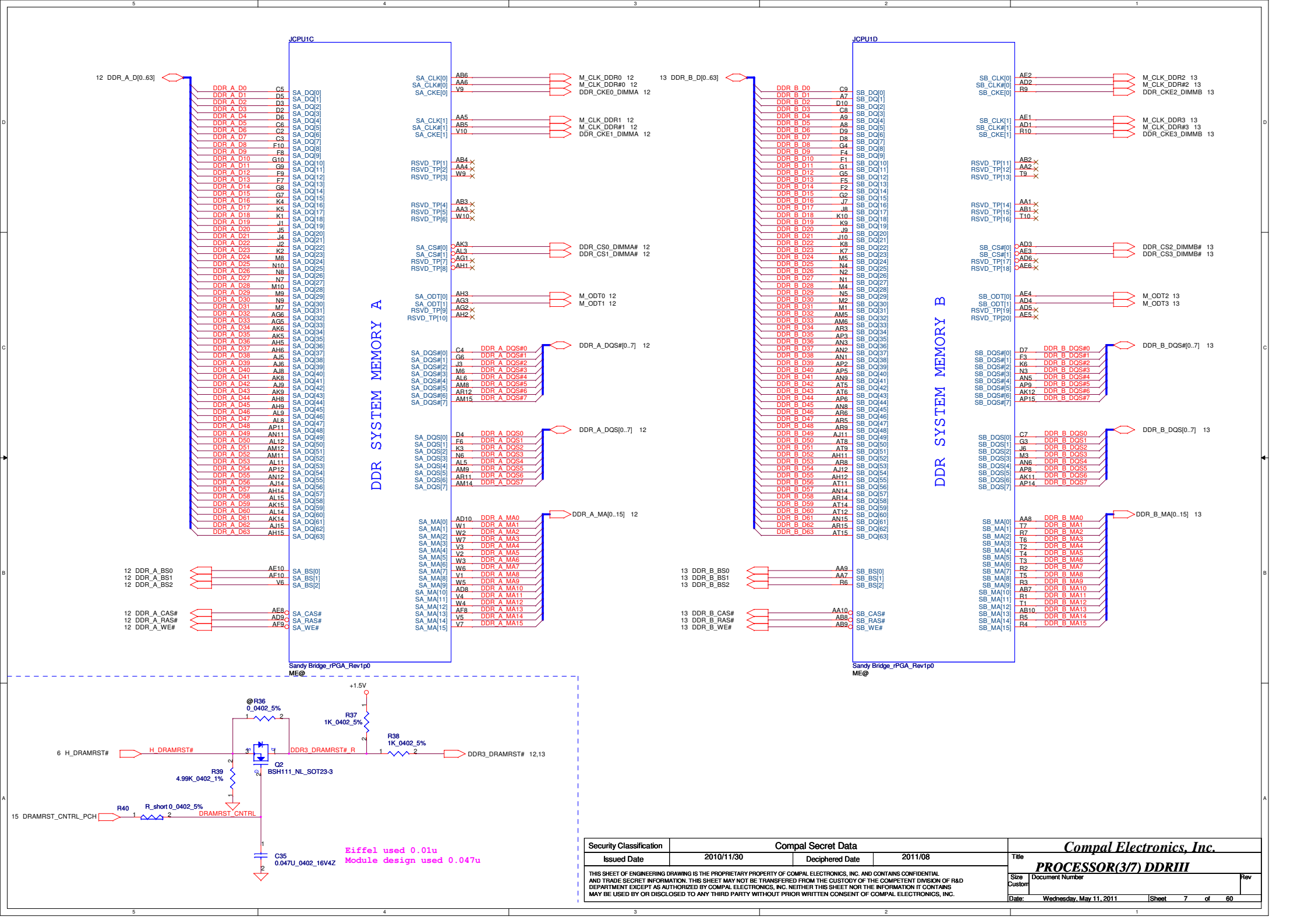
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Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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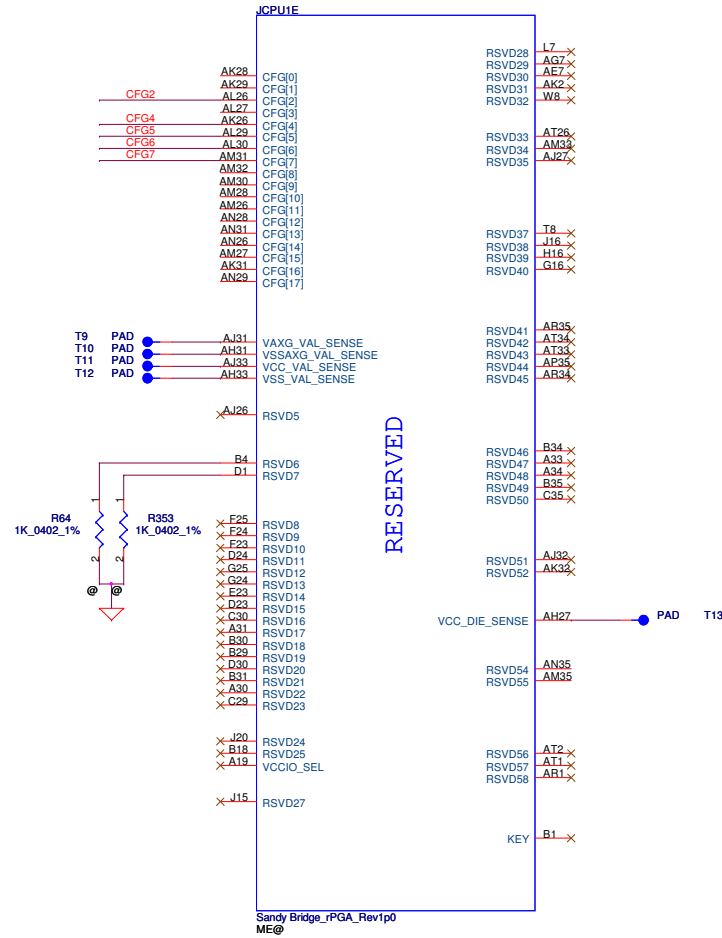
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Issued Date				2010/11/30				Title		
				Deciphered Date				PROCESSOR(2/7) PM,XDP,CLK		
				2011/08				Size		
								Document Number		
								QIQY2 LA6884P		
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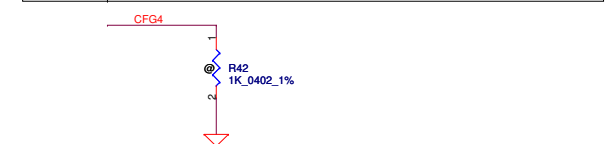


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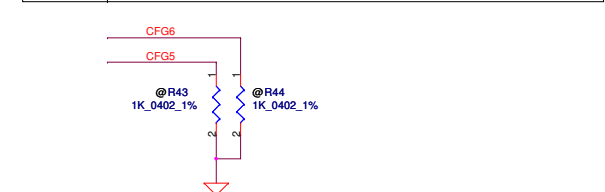
CFG Straps for Processor



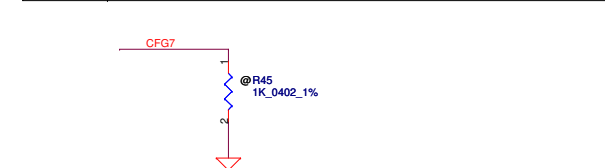
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

JCPU1H

AT35	VSS1	VSS81	AJ22
AT32	VSS2	VSS82	AJ19
AT29	VSS3	VSS83	AJ16
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	VSS86	AJ7
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AJ1
AT7	VSS11	VSS91	AH35
AT4	VSS12	VSS92	AH34
AT3	VSS13	VSS93	AH32
AR25	VSS14	VSS94	AH30
AR22	VSS15	VSS95	AH29
AR19	VSS16	VSS96	AH28
AR16	VSS17	VSS97	AH26
AR13	VSS18	VSS98	AH25
AR10	VSS19	VSS99	AH22
AR7	VSS20	VSS100	AH19
AR4	VSS21	VSS101	AH16
AR2	VSS22	VSS102	AH7
AP34	VSS23	VSS103	AH4
AP31	VSS24	VSS104	AG9
AP28	VSS25	VSS105	AG8
AP25	VSS26	VSS106	AG4
AP22	VSS27	VSS107	AF6
AP19	VSS28	VSS108	AF5
AP16	VSS29	VSS109	AF3
AP13	VSS30	VSS110	AF2
AP10	VSS31	VSS111	AE35
AP7	VSS32	VSS112	AE34
AP4	VSS33	VSS113	AE33
AN30	VSS34	VSS114	AE32
AN27	VSS35	VSS115	AE31
AN25	VSS36	VSS116	AE30
AN22	VSS37	VSS117	AE29
AN19	VSS38	VSS118	AE28
AN16	VSS39	VSS119	AE27
AN13	VSS40	VSS120	AE26
AN10	VSS41	VSS121	AE9
AN7	VSS42	VSS122	AD7
AN4	VSS43	VSS123	AC9
AM29	VSS44	VSS124	AC8
AM25	VSS45	VSS125	AC6
AM22	VSS46	VSS126	AC5
AM19	VSS47	VSS127	AC3
AM16	VSS48	VSS128	AC2
AM13	VSS49	VSS129	AB35
AM10	VSS50	VSS130	AB33
AM7	VSS51	VSS131	AB32
AM4	VSS52	VSS132	AB31
AM3	VSS53	VSS133	AB30
AM2	VSS54	VSS134	AB29
AM1	VSS55	VSS135	AB28
AL34	VSS56	VSS136	AB27
AL31	VSS57	VSS137	AB26
AL28	VSS58	VSS138	Y9
AL25	VSS59	VSS139	Y8
AL22	VSS60	VSS140	Y6
AL19	VSS61	VSS141	Y5
AL16	VSS62	VSS142	Y3
AL13	VSS63	VSS143	Y2
AL10	VSS64	VSS144	Y2
AL7	VSS65	VSS145	W35
AL4	VSS66	VSS146	W34
AL2	VSS67	VSS147	W33
AK33	VSS68	VSS148	W32
AK30	VSS69	VSS149	W31
AK27	VSS70	VSS150	W30
AK25	VSS71	VSS151	W29
AK22	VSS72	VSS152	W28
AK19	VSS73	VSS153	W27
AK16	VSS74	VSS154	W26
AK13	VSS75	VSS155	U9
AK10	VSS76	VSS156	U8
AK7	VSS77	VSS157	U6
AK4	VSS78	VSS158	U5
AJ25	VSS79	VSS159	U3
	VSS80	VSS160	U2

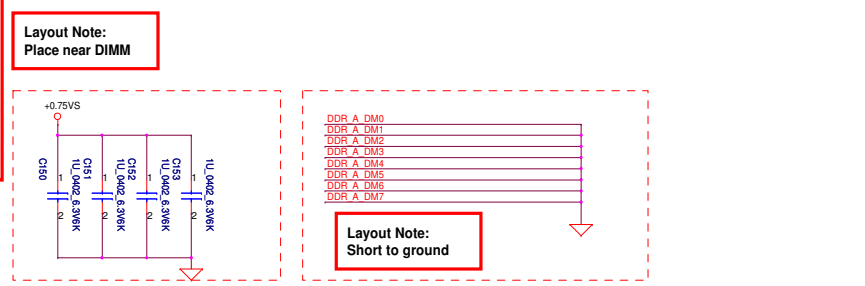
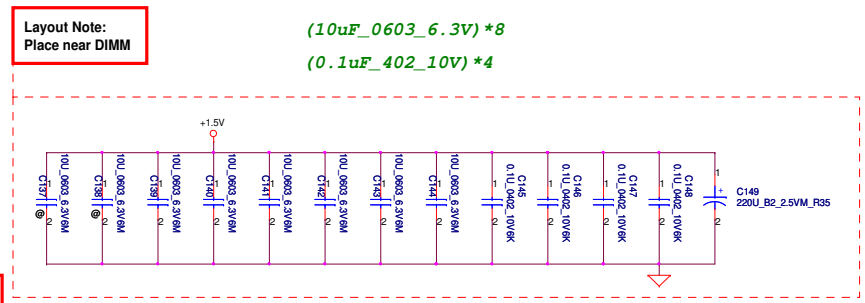
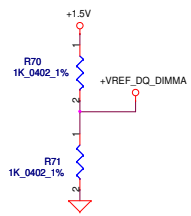
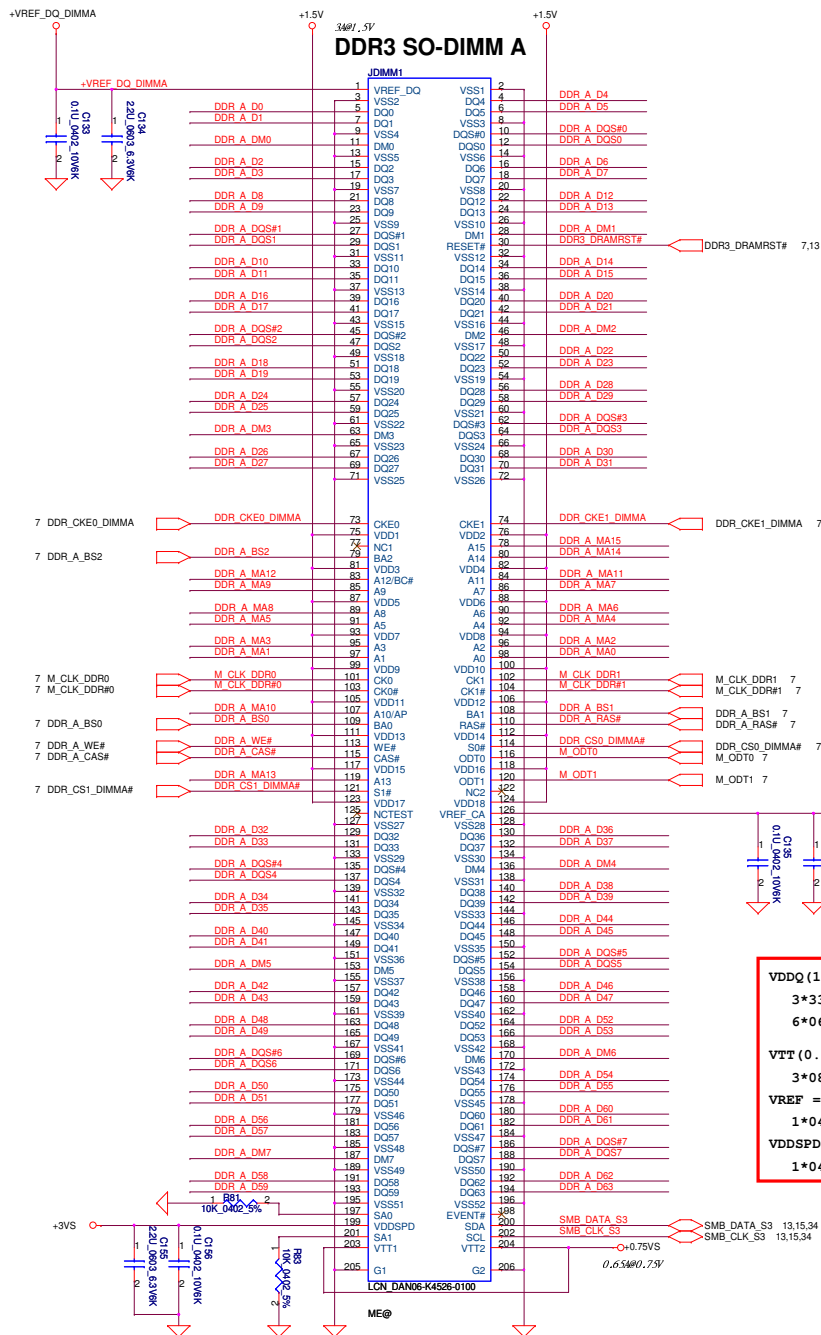
Sandy Bridge_rPGA_Rev1p0
ME@

JCPU1I

T35	VSS161	VSS234	F22
T34	VSS162	VSS235	F19
T33	VSS163	VSS236	E30
T32	VSS164	VSS237	E27
T31	VSS165	VSS238	E24
T29	VSS166	VSS239	E21
T28	VSS167	VSS240	E18
T27	VSS168	VSS241	E15
T26	VSS169	VSS242	E13
P9	VSS170	VSS243	E10
P8	VSS171	VSS244	E9
P6	VSS172	VSS245	E8
P5	VSS173	VSS246	E7
P3	VSS174	VSS247	E6
P2	VSS175	VSS248	E5
N35	VSS176	VSS249	E4
N34	VSS177	VSS250	E2
N33	VSS178	VSS251	E1
N32	VSS179	VSS252	D35
N31	VSS180	VSS253	D32
N30	VSS181	VSS254	D29
N29	VSS182	VSS255	D26
N28	VSS183	VSS256	D20
N27	VSS184	VSS257	D17
N26	VSS185	VSS258	D17
N25	VSS186	VSS259	C34
N24	VSS187	VSS260	C31
N23	VSS188	VSS261	C28
N22	VSS189	VSS262	C27
N21	VSS190	VSS263	C23
N20	VSS191	VSS264	C10
N19	VSS192	VSS265	C1
N18	VSS193	VSS266	B22
N17	VSS194	VSS267	B19
N16	VSS195	VSS268	B17
N15	VSS196	VSS269	B15
N14	VSS197	VSS270	B13
N13	VSS198	VSS271	B11
N12	VSS199	VSS272	B9
N11	VSS200	VSS273	B8
N10	VSS201	VSS274	B7
N9	VSS202	VSS275	B5
N8	VSS203	VSS276	B3
N7	VSS204	VSS277	B2
N6	VSS205	VSS278	A35
N5	VSS206	VSS279	A32
N4	VSS207	VSS280	A29
N3	VSS208	VSS281	A26
N2	VSS209	VSS282	A23
N1	VSS210	VSS283	A20
	VSS211	VSS284	A3
	VSS212	VSS285	
	VSS213		
	VSS214		
	VSS215		
	VSS216		
	VSS217		
	VSS218		
	VSS219		
	VSS220		
	VSS221		
	VSS222		
	VSS223		
	VSS224		
	VSS225		
	VSS226		
	VSS227		
	VSS228		
	VSS229		
	VSS230		
	VSS231		
	VSS232		
	VSS233		

Sandy Bridge_rPGA_Rev1p0
ME@

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VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

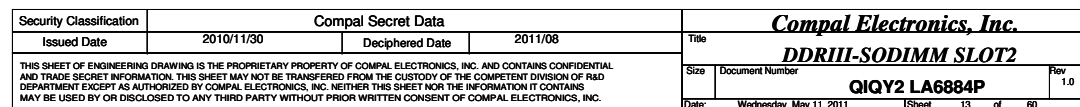
VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

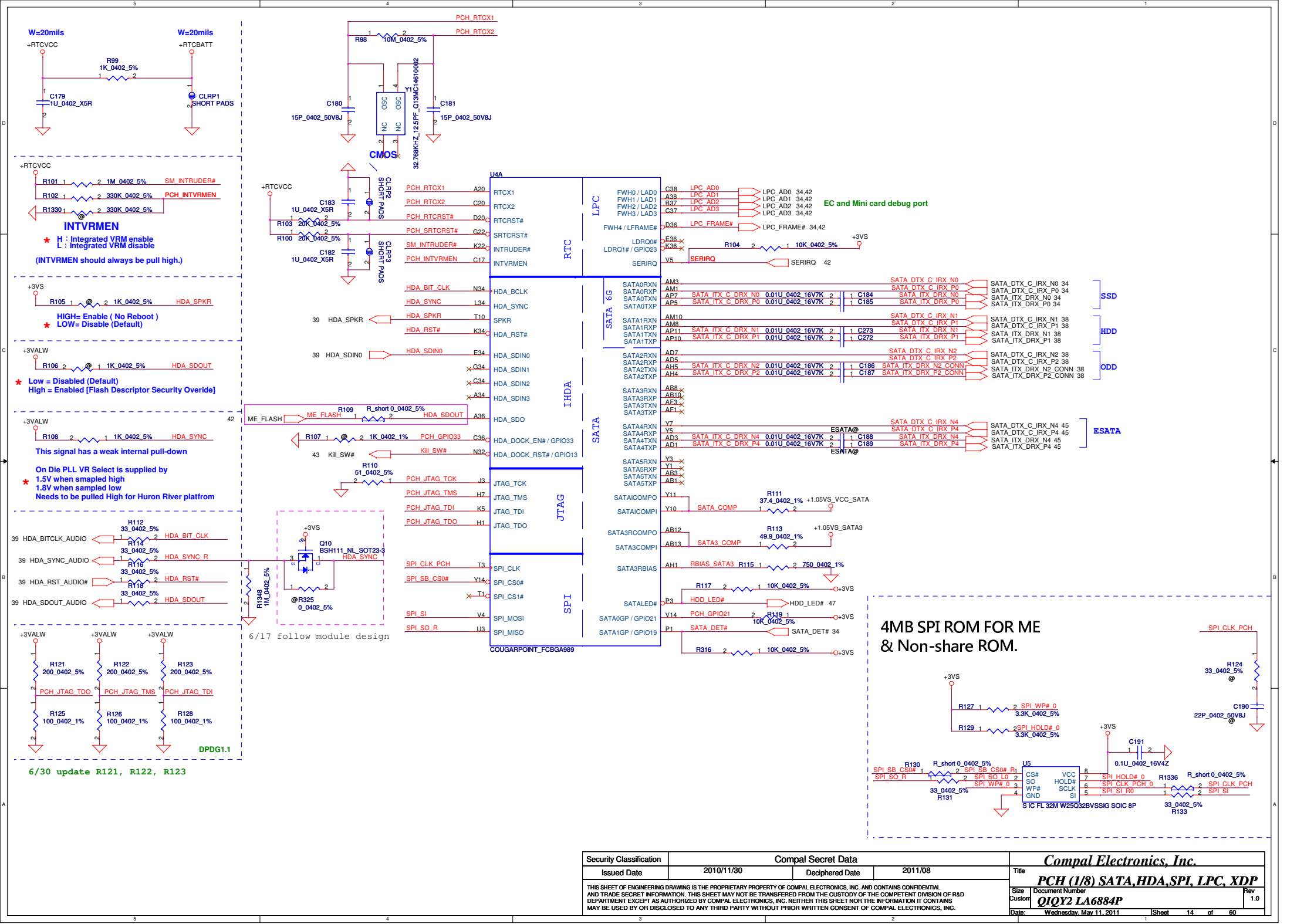
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Place near DIMM

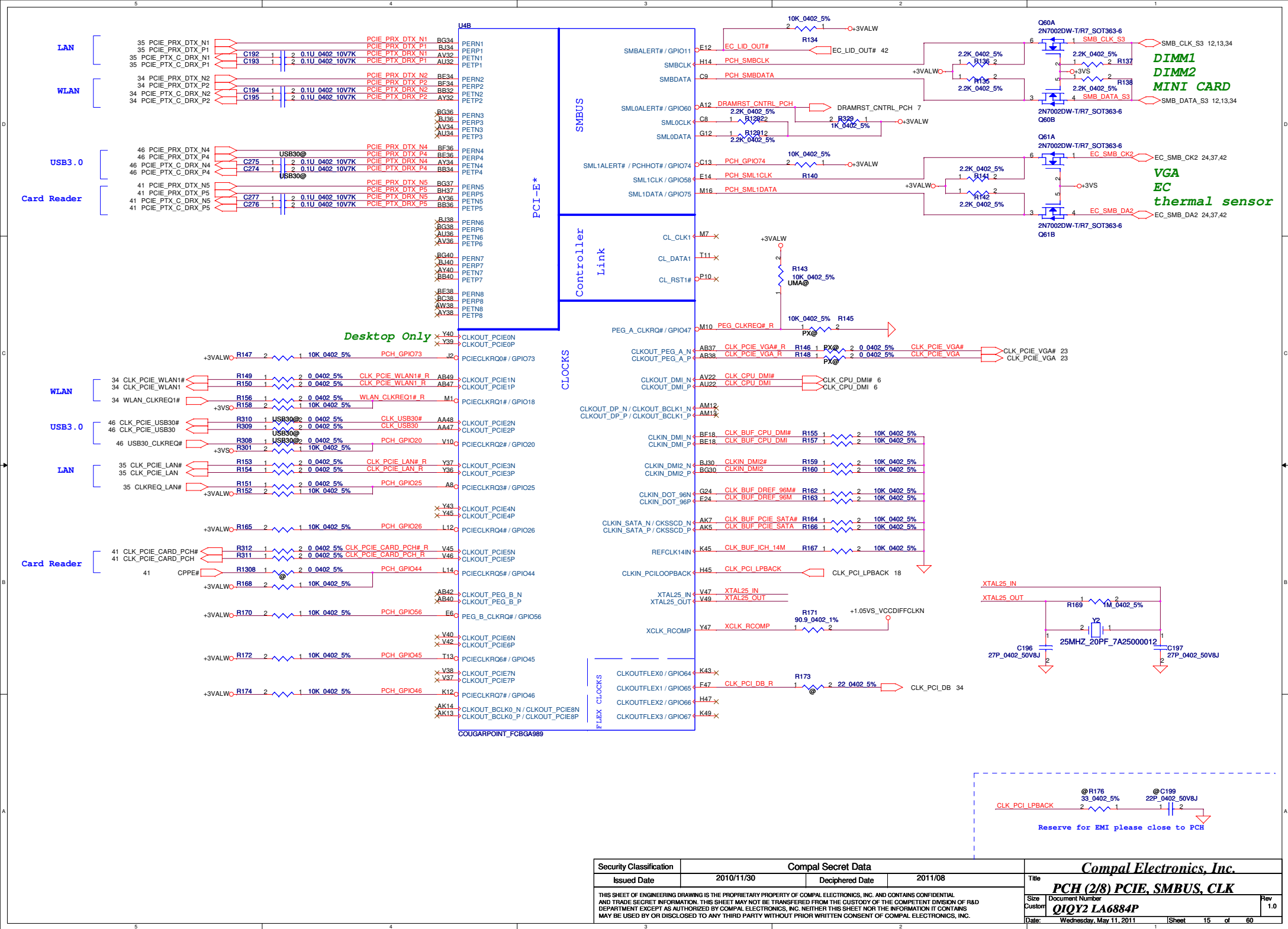
Layout Note:
Place near DIMM

Layout Note:
Short to ground

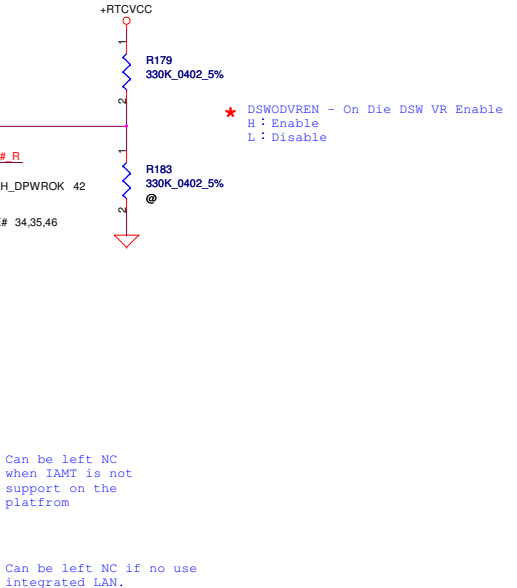
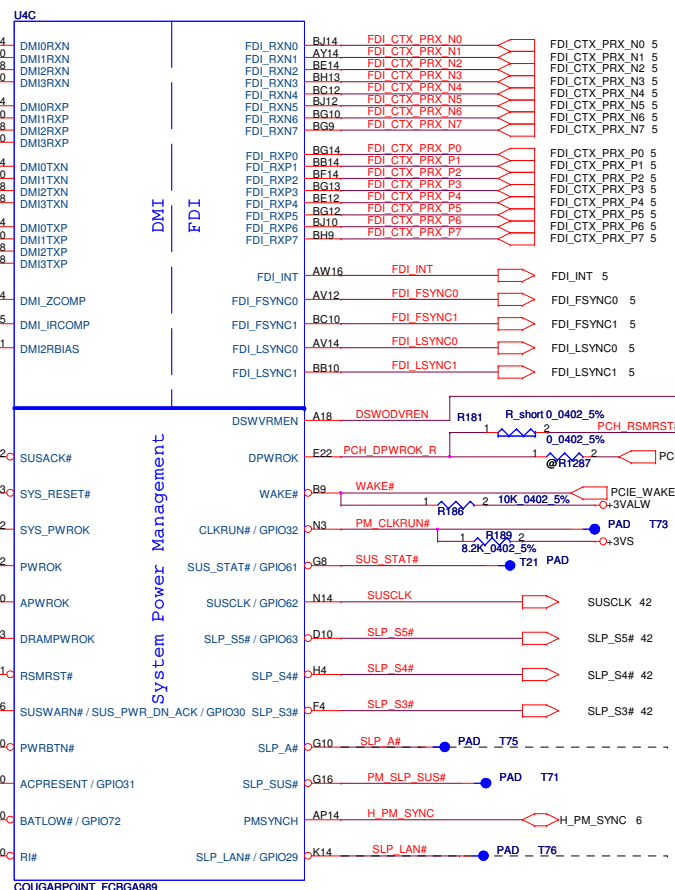
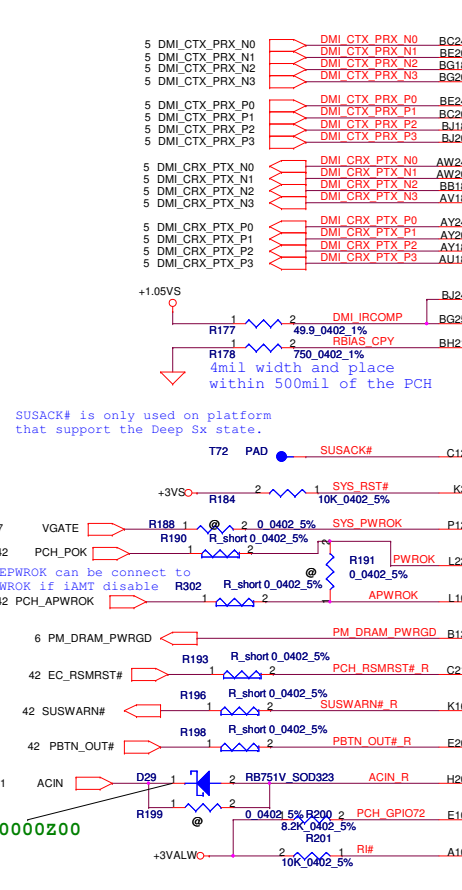
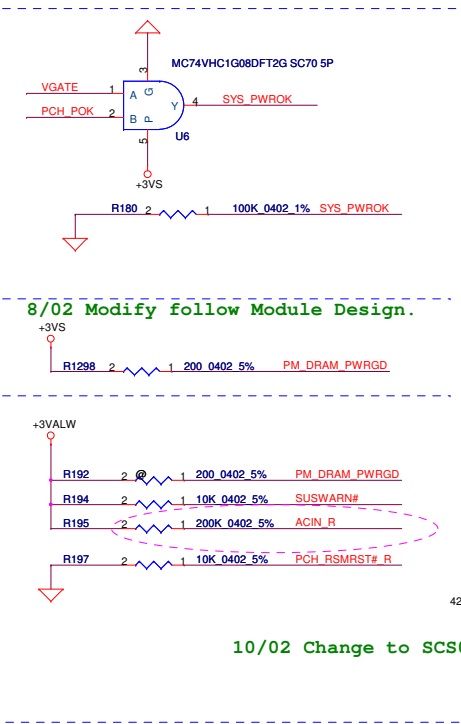
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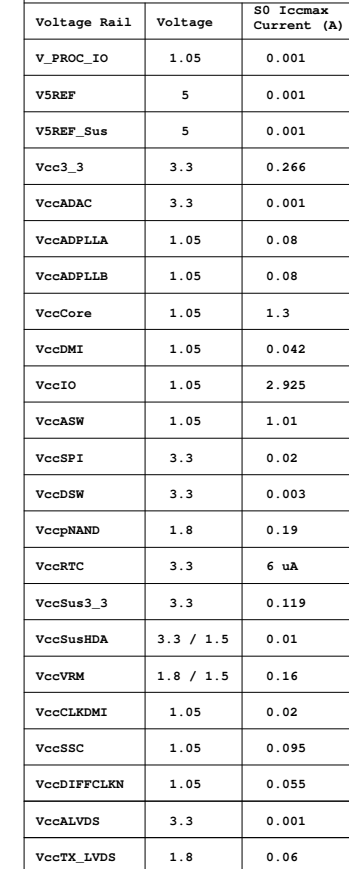




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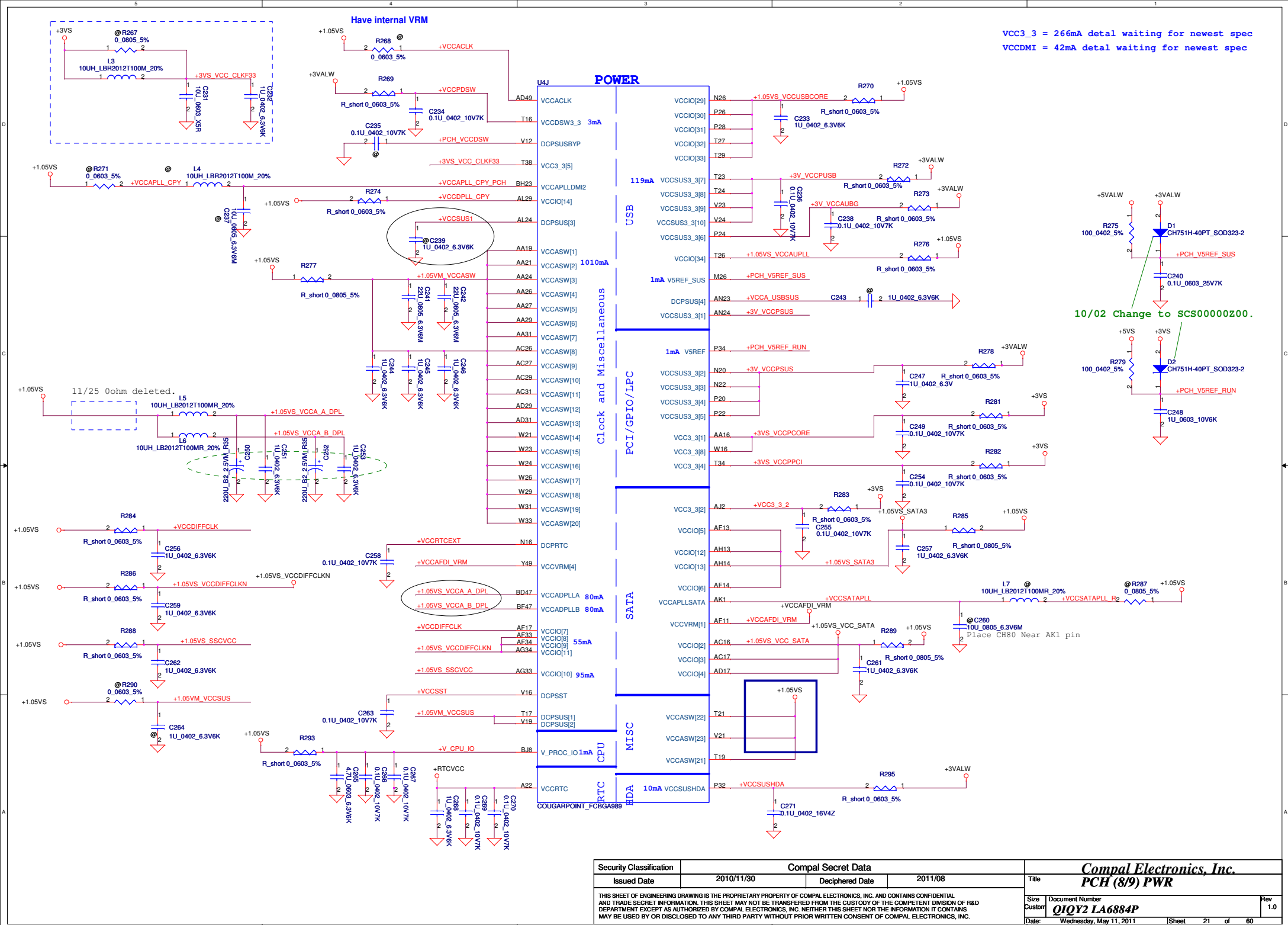
PCH Power Rail Table



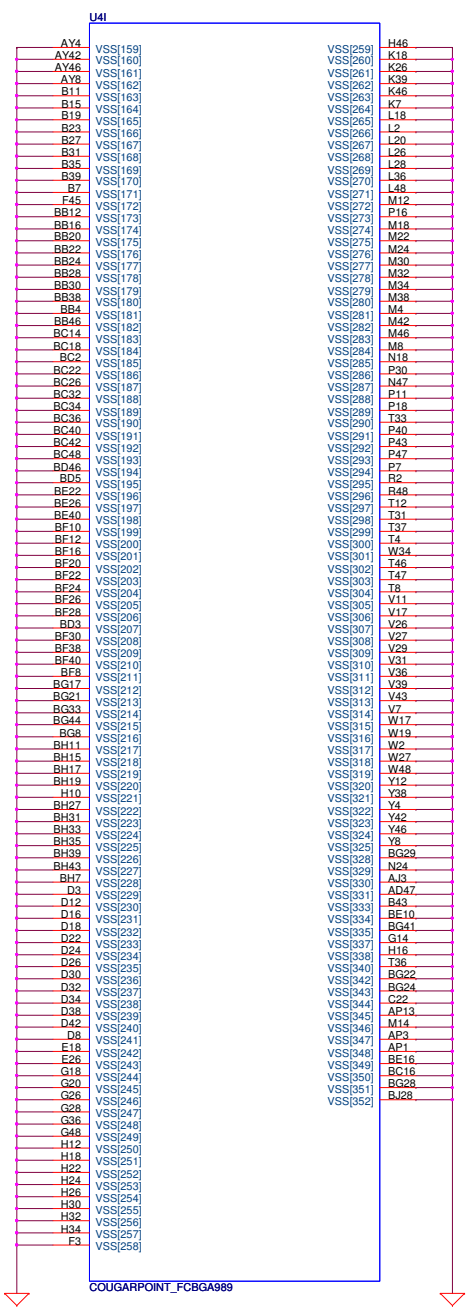
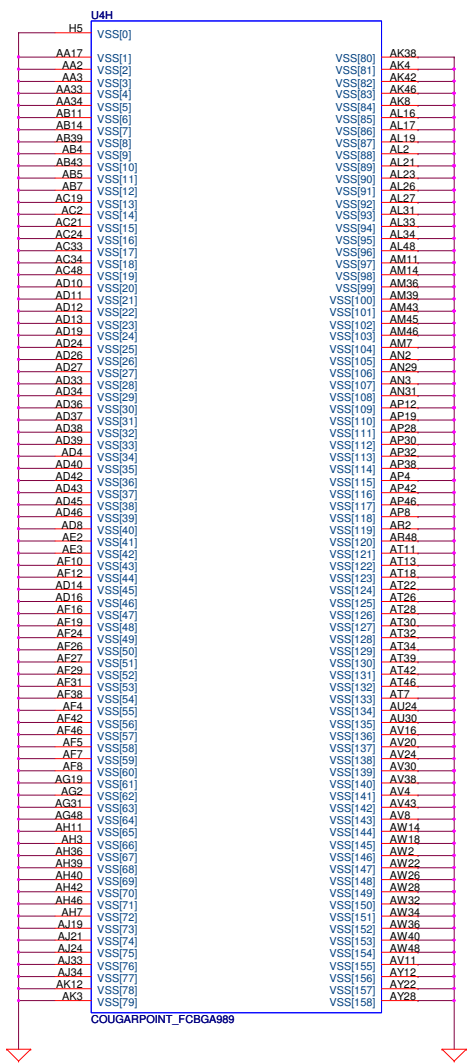
Intel HR_PDDG_1.21
1.5S rail. Default is to populate to enable VccVRM.

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PCH (7/9) PWR			
Size Custom	Document Number QIQY2 LA6884P		Rev 1.0
Date:	Wednesday, May 11, 2011	Sheet	20 of 60



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				Custom	1.0
				QIQY2 LA6884P	
Date:	Wednesday, May 11, 2011	Sheet	21	of	60



5 PCIE_CTX_GRX_P[15..0]
5 PCIE_CTX_GRX_N[15..0]

PCIE_CTX_GRX_P[15..0]
PCIE_CTX_GRX_N[15..0]

U8A PX@

PCIE_CRX_GTX_P[15..0]
PCIE_CRX_GTX_N[15..0]

PCIE_CRX_GTX_P[15..0] 5
PCIE_CRX_GTX_N[15..0] 5

LVDS Interface

PCIE_CTX_GRX_P0 AA38 PCIE_RX0P
PCIE_CTX_GRX_N0 Y37 PCIE_RX0N

PCIE_CTX_GRX_P1 Y35 PCIE_RX1P
PCIE_CTX_GRX_N1 W36 PCIE_RX1N

PCIE_CTX_GRX_P2 W38 PCIE_RX2P
PCIE_CTX_GRX_N2 V37 PCIE_RX2N

PCIE_CTX_GRX_P3 Y35 PCIE_RX3P
PCIE_CTX_GRX_N3 U36 PCIE_RX3N

PCIE_CTX_GRX_P4 U38 PCIE_RX4P
PCIE_CTX_GRX_N4 T37 PCIE_RX4N

PCIE_CTX_GRX_P5 T35 PCIE_RX5P
PCIE_CTX_GRX_N5 R36 PCIE_RX5N

PCIE_CTX_GRX_P6 R38 PCIE_RX6P
PCIE_CTX_GRX_N6 P37 PCIE_RX6N

PCIE_CTX_GRX_P7 P35 PCIE_RX7P
PCIE_CTX_GRX_N7 N36 PCIE_RX7N

PCIE_CTX_GRX_P8 N38 PCIE_RX8P
PCIE_CTX_GRX_N8 M37 PCIE_RX8N

PCIE_CTX_GRX_P9 M35 PCIE_RX9P
PCIE_CTX_GRX_N9 L36 PCIE_RX9N

PCIE_CTX_GRX_P10 L38 PCIE_RX10P
PCIE_CTX_GRX_N10 K37 PCIE_RX10N

PCIE_CTX_GRX_P11 K35 PCIE_RX11P
PCIE_CTX_GRX_N11 J36 PCIE_RX11N

PCIE_CTX_GRX_P12 J38 PCIE_RX12P
PCIE_CTX_GRX_N12 H37 PCIE_RX12N

PCIE_CTX_GRX_P13 H35 PCIE_RX13P
PCIE_CTX_GRX_N13 G36 PCIE_RX13N

PCIE_CTX_GRX_P14 G38 PCIE_RX14P
PCIE_CTX_GRX_N14 F37 PCIE_RX14N

PCIE_CTX_GRX_P15 F35 PCIE_RX15P
PCIE_CTX_GRX_N15 E37 PCIE_RX15N

PCI EXPRESS INTERFACE

15 CLK_PCIE_VGA
15 CLK_PCIE_VGA#

CLK_PCIE_VGA AB35
CLK_PCIE_VGA# AA36

PX@ R1355 10K_0402_5% AH16
VGA_RST# AA30

WHESTLERM2

CALIBRATION

PCIE_CALRP

PCIE_CALRN

PCIE_CALRP

PCIE_CALRN

PCIE_CALRP

PCIE_CALRN

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PCIE_CALRN

PCIE_CALRP

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PCIE_CALRP

PCIE_CALRN

PCIE_CALRP

PCIE_CALRN

PCIE_CALRP

PCIE_CALRN

PCIE_CALRP

PCIE_CALRN

PCIE_TX0P Y33 PCIE_CRX_C_GTX_P0 0.1U_0402_10V7K C930
PCIE_TX0N Y32 PCIE_CRX_C_GTX_N0 0.1U_0402_10V7K C931

PCIE_TX1P W33 PCIE_CRX_C_GTX_P1 0.1U_0402_10V7K C932
PCIE_TX1N W32 PCIE_CRX_C_GTX_N1 0.1U_0402_10V7K C933

PCIE_TX2P U33 PCIE_CRX_C_GTX_P2 0.1U_0402_10V7K C936
PCIE_TX2N U32 PCIE_CRX_C_GTX_N2 0.1U_0402_10V7K C934

PCIE_TX3P U30 PCIE_CRX_C_GTX_P3 0.1U_0402_10V7K C935
PCIE_TX3N U29 PCIE_CRX_C_GTX_N3 0.1U_0402_10V7K C937

PCIE_TX4P T33 PCIE_CRX_C_GTX_P4 0.1U_0402_10V7K C938
PCIE_TX4N T32 PCIE_CRX_C_GTX_N4 0.1U_0402_10V7K C939

PCIE_TX5P T30 PCIE_CRX_C_GTX_P5 0.1U_0402_10V7K C940
PCIE_TX5N T29 PCIE_CRX_C_GTX_N5 0.1U_0402_10V7K C941

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PCIE_TX6N P32 PCIE_CRX_C_GTX_N6 0.1U_0402_10V7K C943

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PCIE_TX8N N32 PCIE_CRX_C_GTX_N8 0.1U_0402_10V7K C947

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PCIE_TX9N N29 PCIE_CRX_C_GTX_N9 0.1U_0402_10V7K C949

PCIE_TX10P L33 PCIE_CRX_C_GTX_P10 0.1U_0402_10V7K C950
PCIE_TX10N L32 PCIE_CRX_C_GTX_N10 0.1U_0402_10V7K C951

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PCIE_TX12P K33 PCIE_CRX_C_GTX_P12 0.1U_0402_10V7K C954
PCIE_TX12N K32 PCIE_CRX_C_GTX_N12 0.1U_0402_10V7K C955

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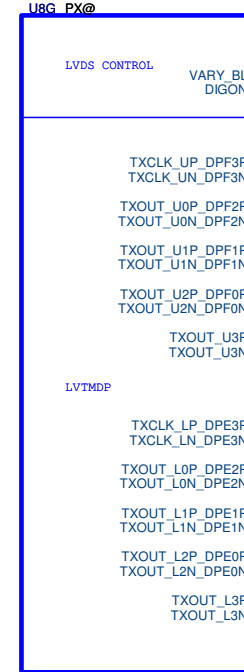
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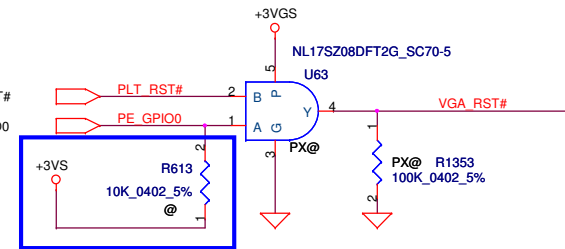
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modify 3/17

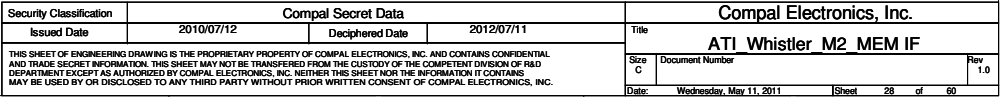
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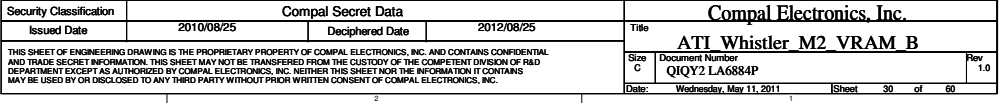


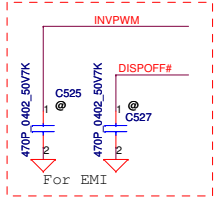
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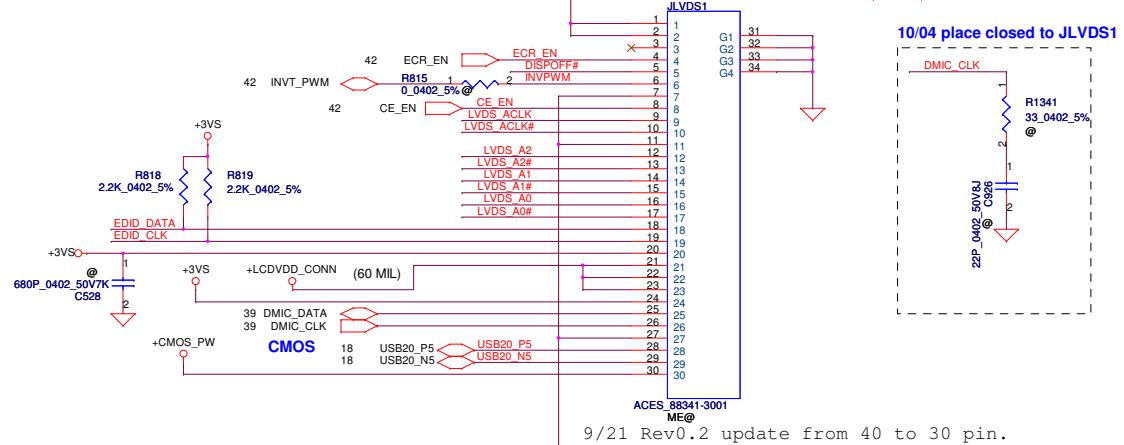
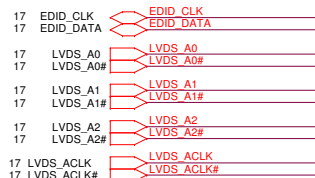
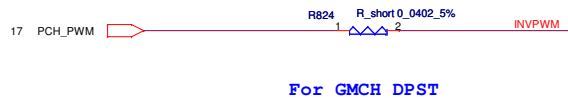
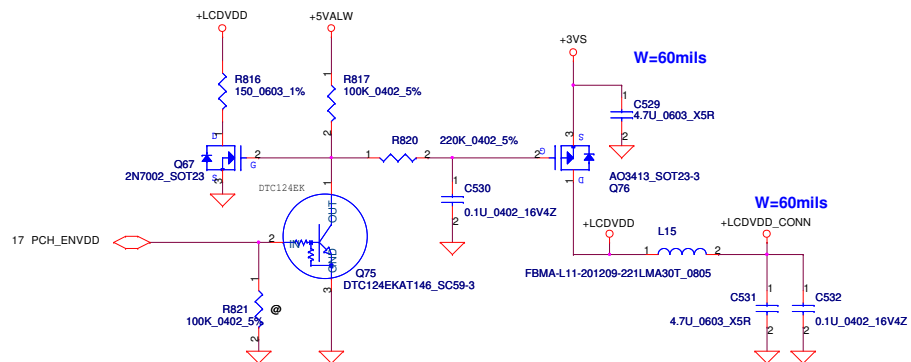
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						B				1.0	
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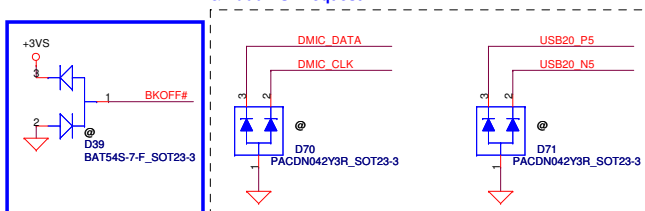




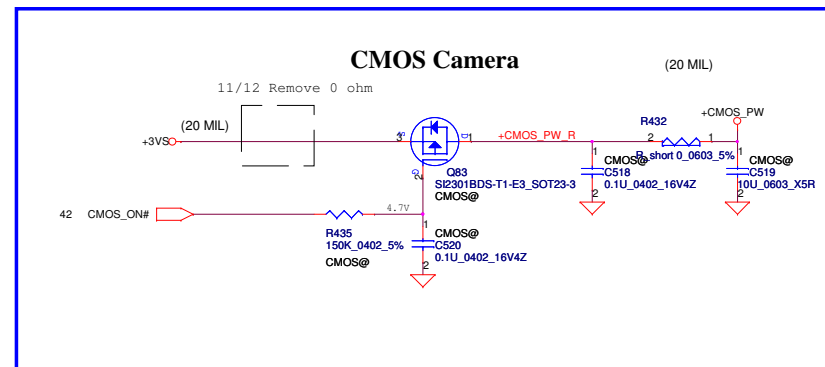
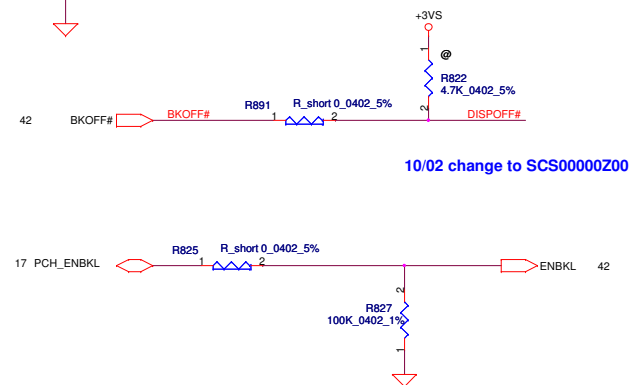
LCD POWER CIRCUIT



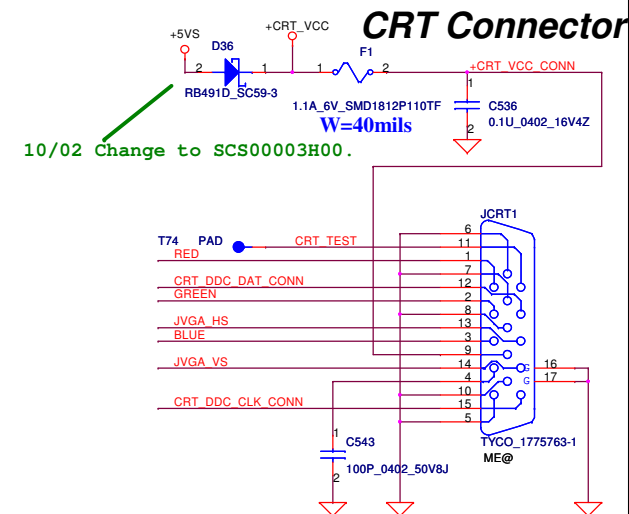
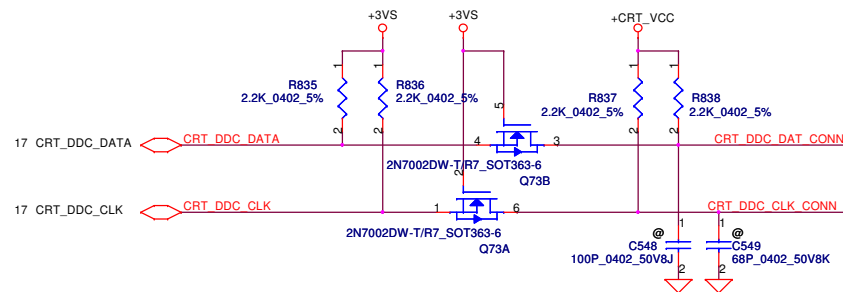
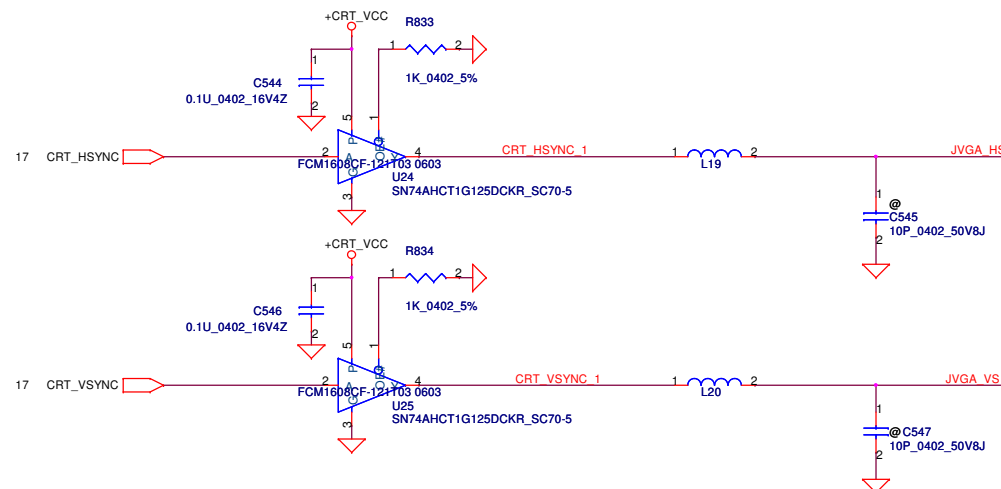
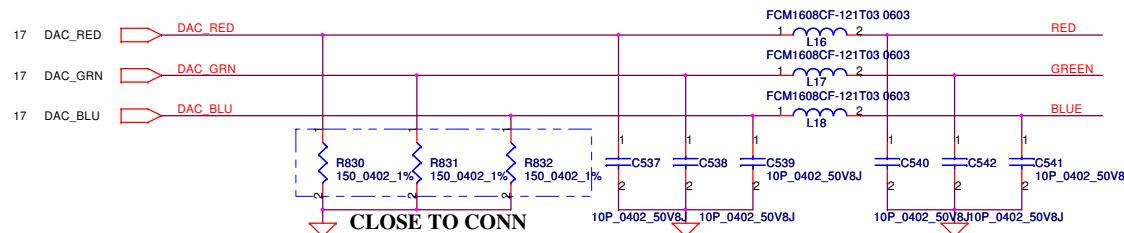
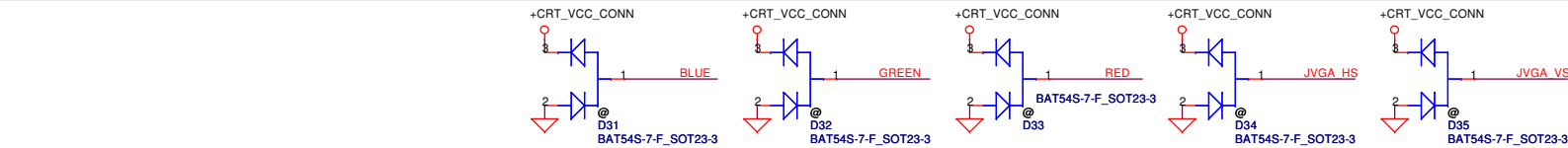
8/4 add ESD request



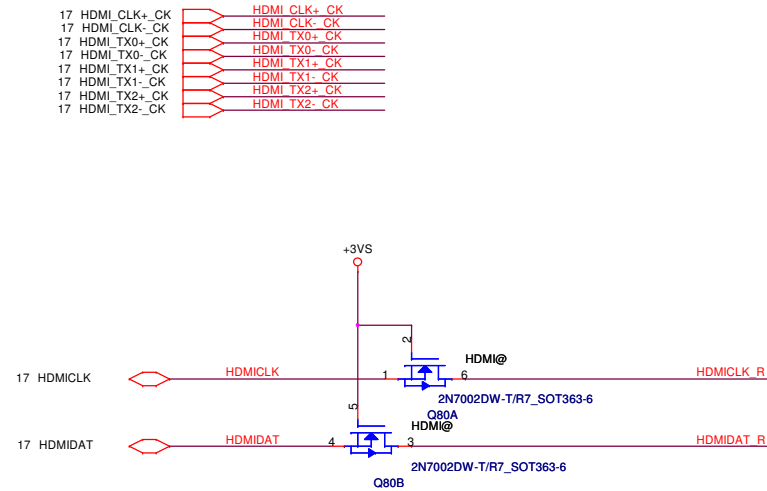
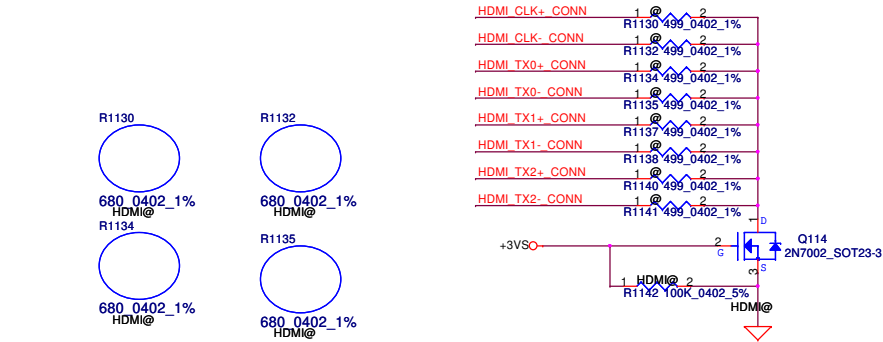
modify 4/20



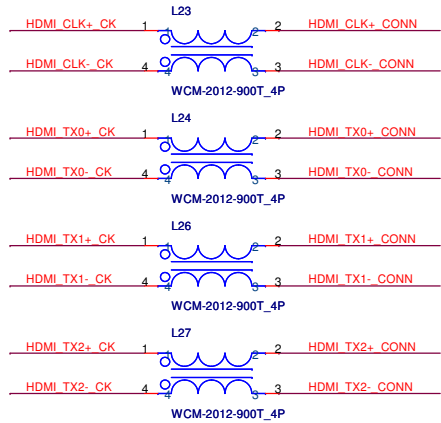
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				Size B	Document Number
				QIQY2 LA6884P	
Date: Wednesday, May 11, 2011				Sheet 31	Rev 1.0



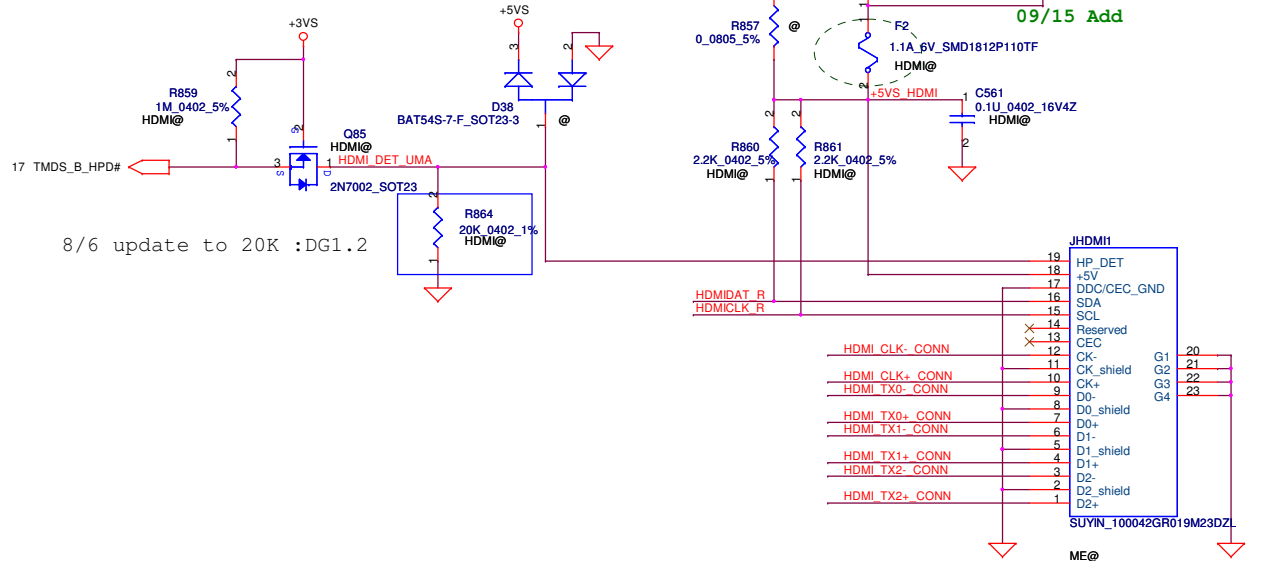
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DVT, Change to SM070000I00 for EMI request.



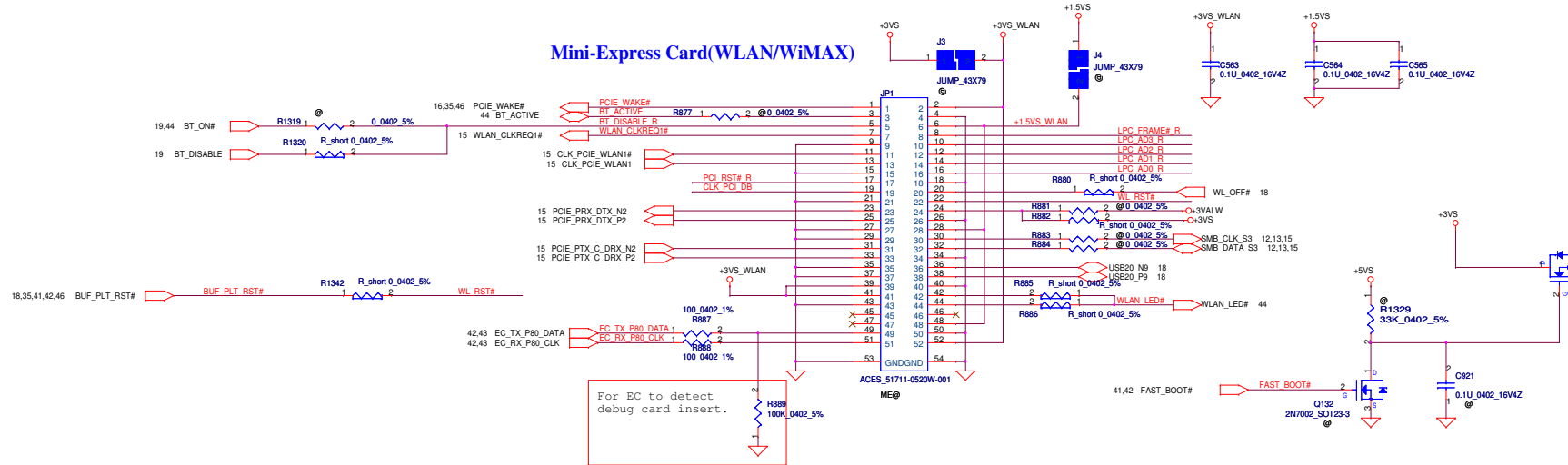
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HDMI CLK- CK	R886	1	0	0402_5%	HDMI CLK- CONN
HDMI TX0+ CK	R887	1	0	0402_5%	HDMI TX0+ CONN
HDMI TX0- CK	R888	1	0	0402_5%	HDMI TX0- CONN
HDMI TX1+ CK	R889	1	0	0402_5%	HDMI TX1+ CONN
HDMI TX1- CK	R890	1	0	0402_5%	HDMI TX1- CONN
HDMI TX2+ CK	R891	1	0	0402_5%	HDMI TX2+ CONN
HDMI TX2- CK	R892	1	0	0402_5%	HDMI TX2- CONN



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				Deciphered Date				HDMI CONN			
				2011/08				Size			
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								QIQY2 LA6884P			
								Date: Wednesday, May 11, 2011			
								Sheet 33 of 60			

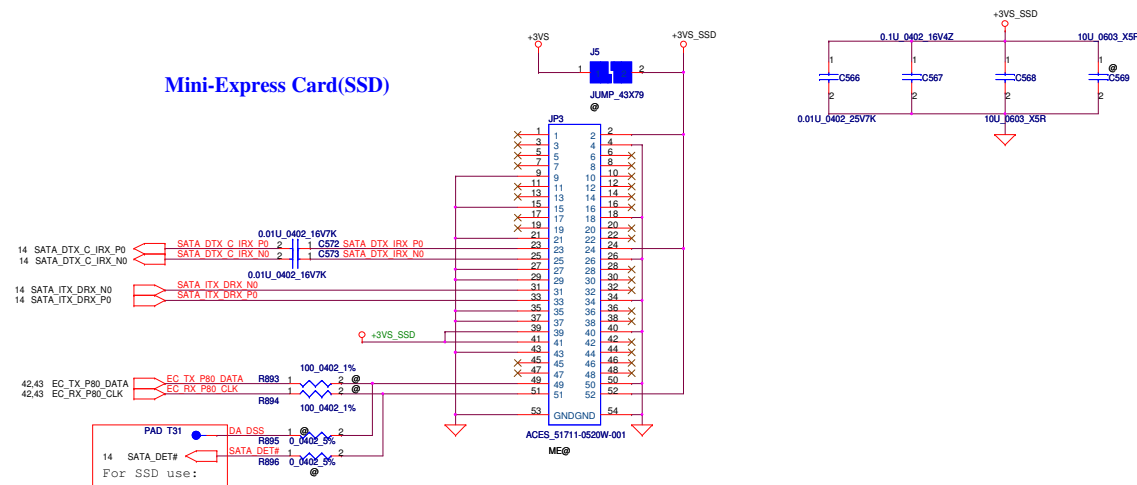
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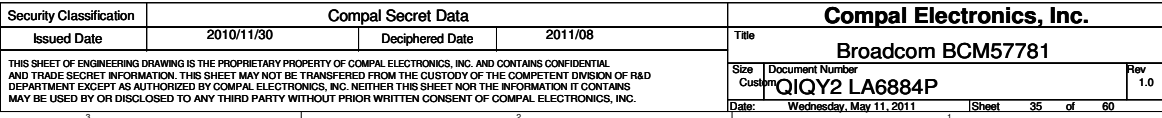
Mini-Express Card(WLAN/WiMAX)

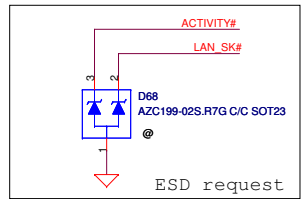
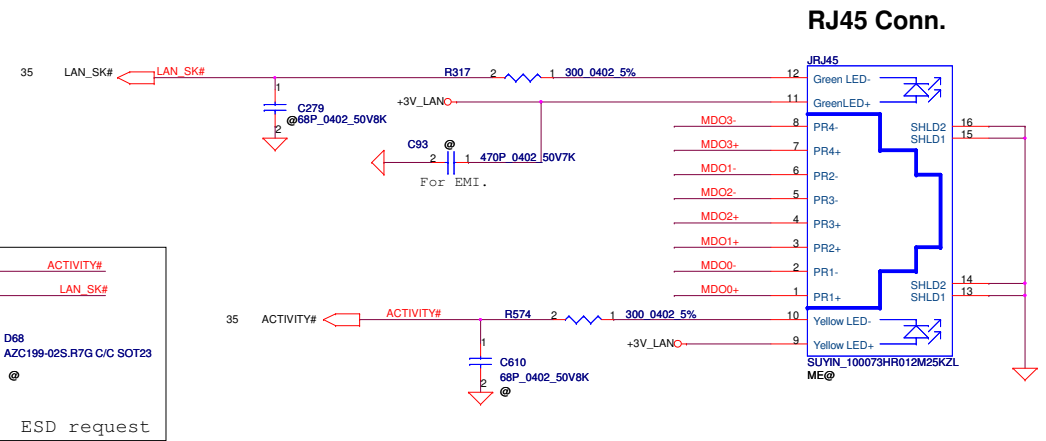
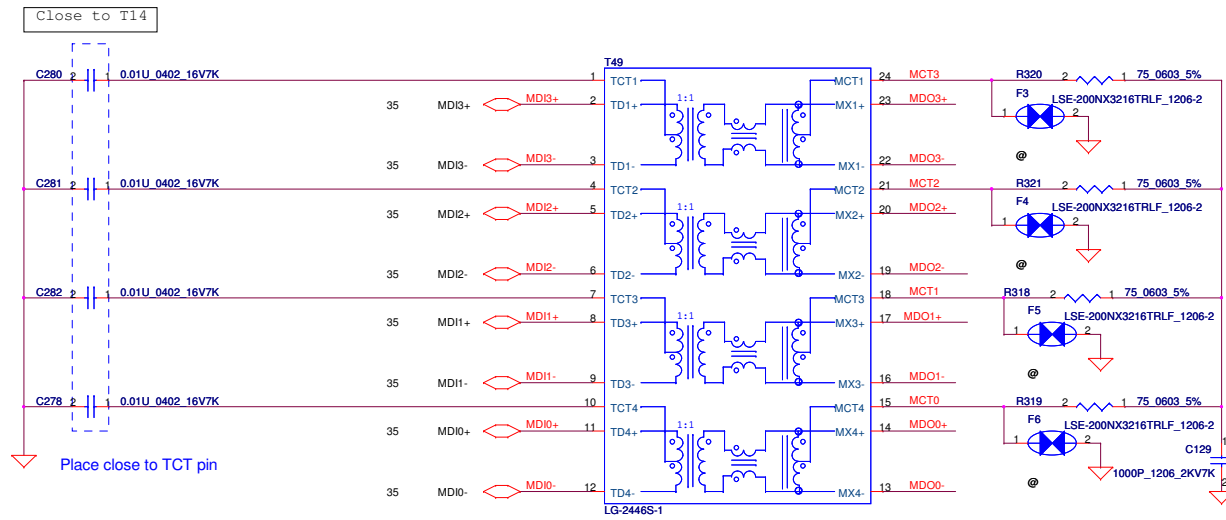


SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)

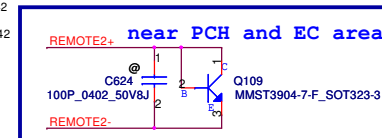
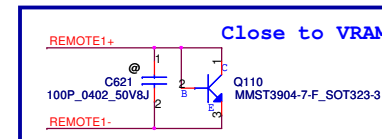
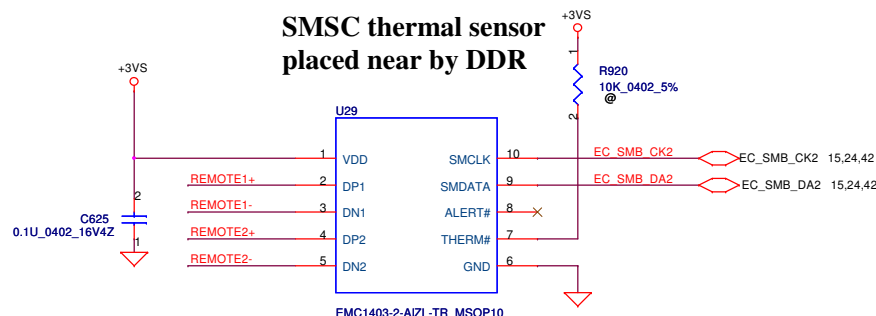
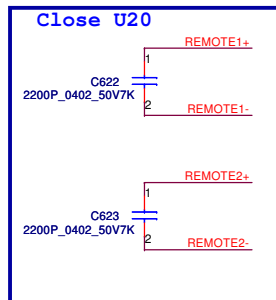




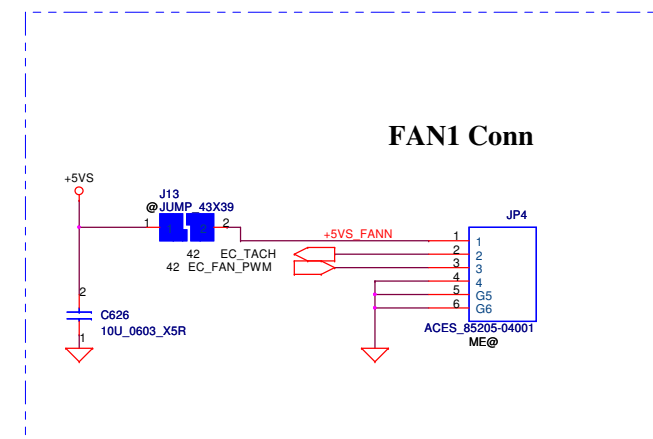


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										Rev	
										1.0	
										Date	
										Wednesday, May 11, 2011	
										Sheet	
										36 of 60	

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REMOTE1,2+/-:
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Issued Date	2010/11/30	Deciphered Date	2011/08	Title	EMC1403_ Thermal sensor/FAN
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[illegible]

SATA ODD Conn.

14 SATA_ITX_DRX_P2_CONN
14 SATA_ITX_DRX_N2_CONN
14 SATA_DTX_C_IRX_N2
14 SATA_DTX_C_IRX_P2

SATA ITX_DRX_P2_CONN
SATA ITX_DRX_N2_CONN
SATA DTX_C_IRX_N2
SATA DTX_C_IRX_P2

C629 1 2 0.01uF 0402 16V7K
C630 1 2 0.01uF 0402 16V7K

R921 1 2 +3VSO 10K_0402_5%
R922 1 2 +5V ODD 10K_0402_5%
R710 1 2 R_short 0_0402_5%
R711 1 2 R_short 0_0402_5%

18,42 ODD_DA#

ODD DA#

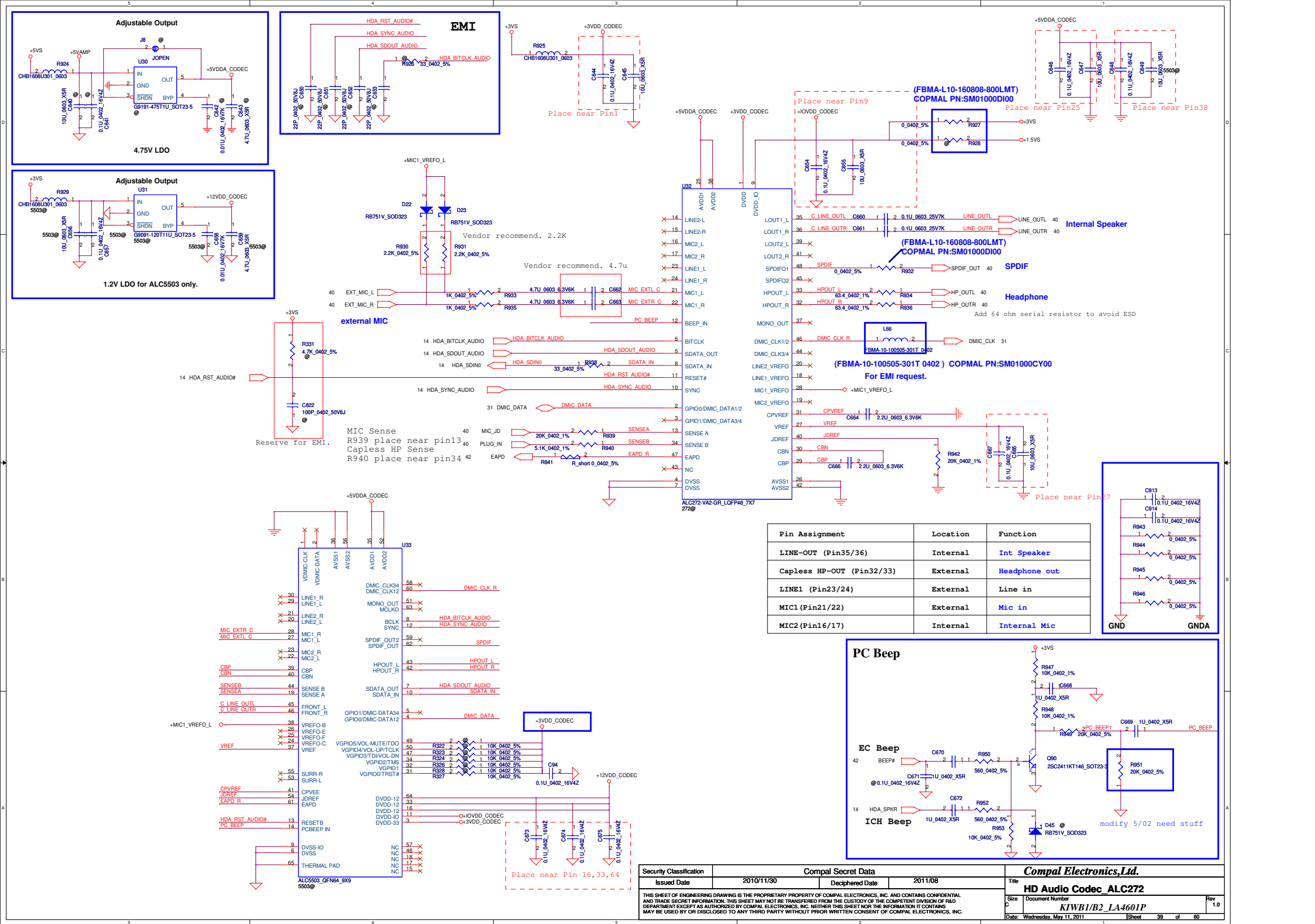
ODD1

1 GND
2 A+
3 A-
4 GND
5 B-
6 B+
7 GND
8 DP
9 +5V
10 +5V
11 MD
12 GND
13 GND
14 GND
15 GND

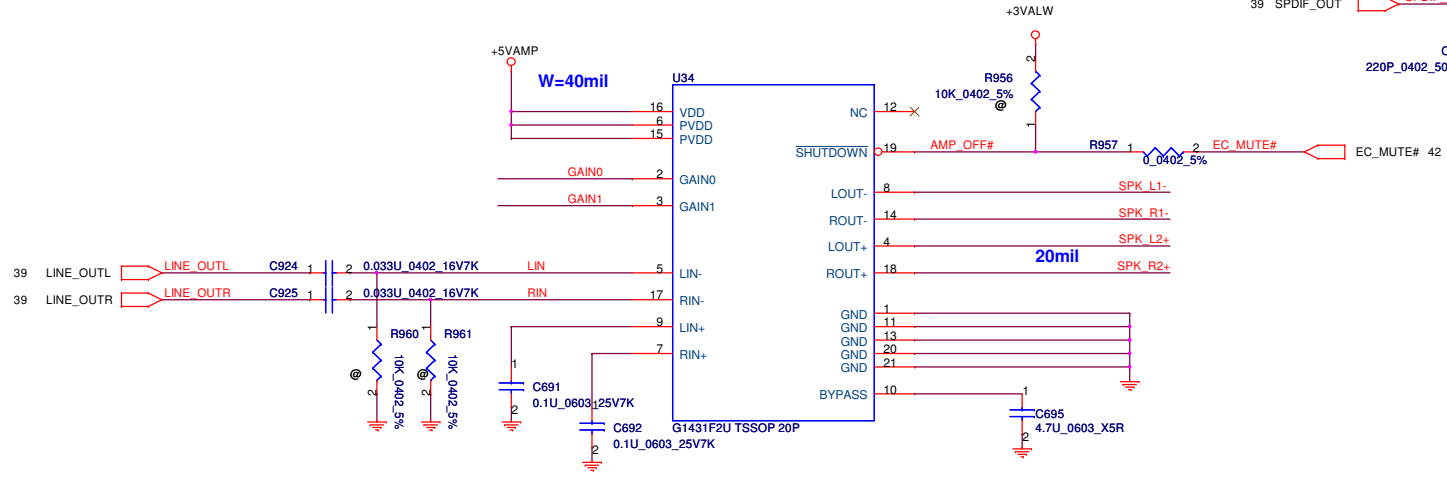
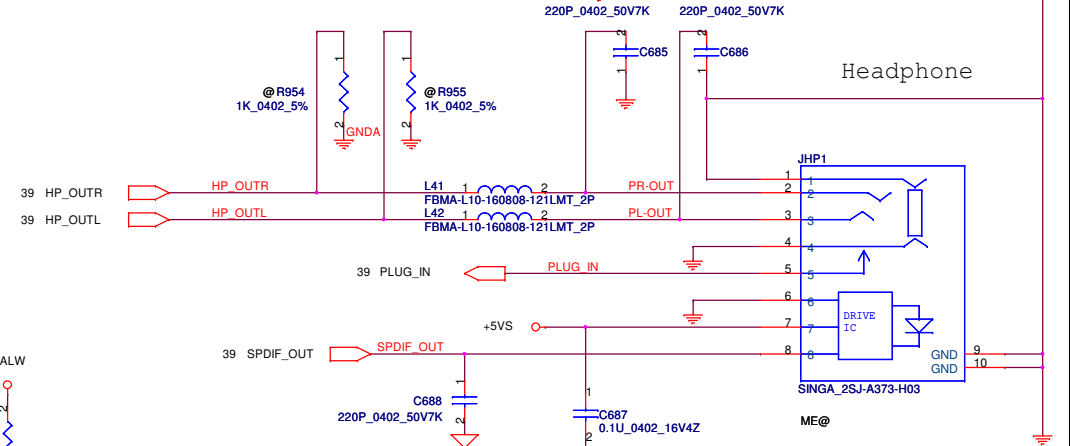
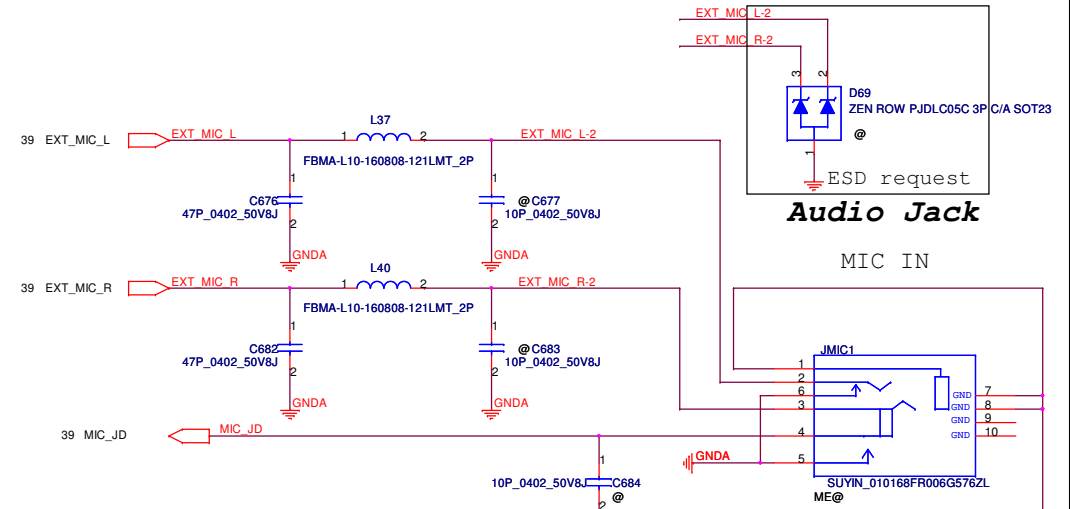
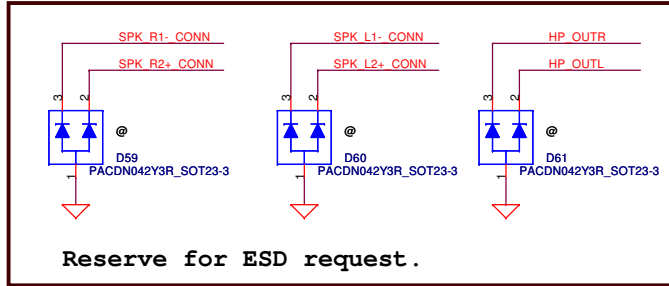
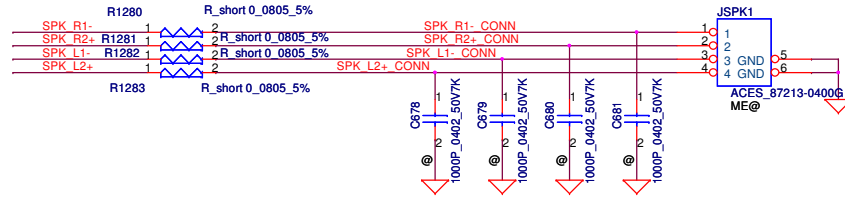
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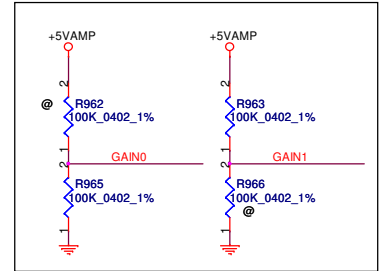
Security Classification		Compal Secret Data		Compal Electronics, Inc. HDD/ODD Connector	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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				B	1.0
				Document Number QIY2 LA6884P	
Date		Wednesday, May 11, 2011		Sheet	38 of 60



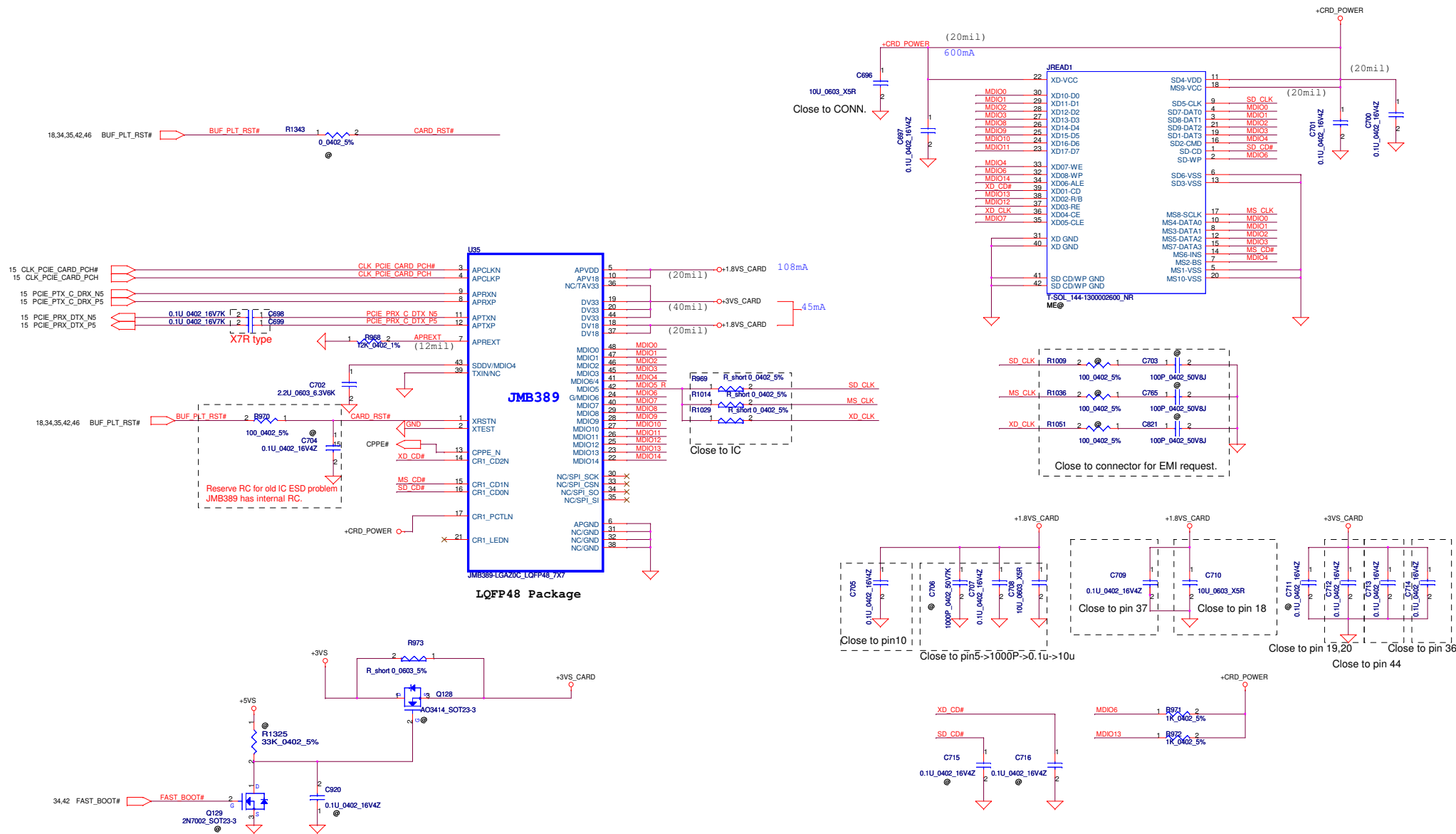
wide 20MIL



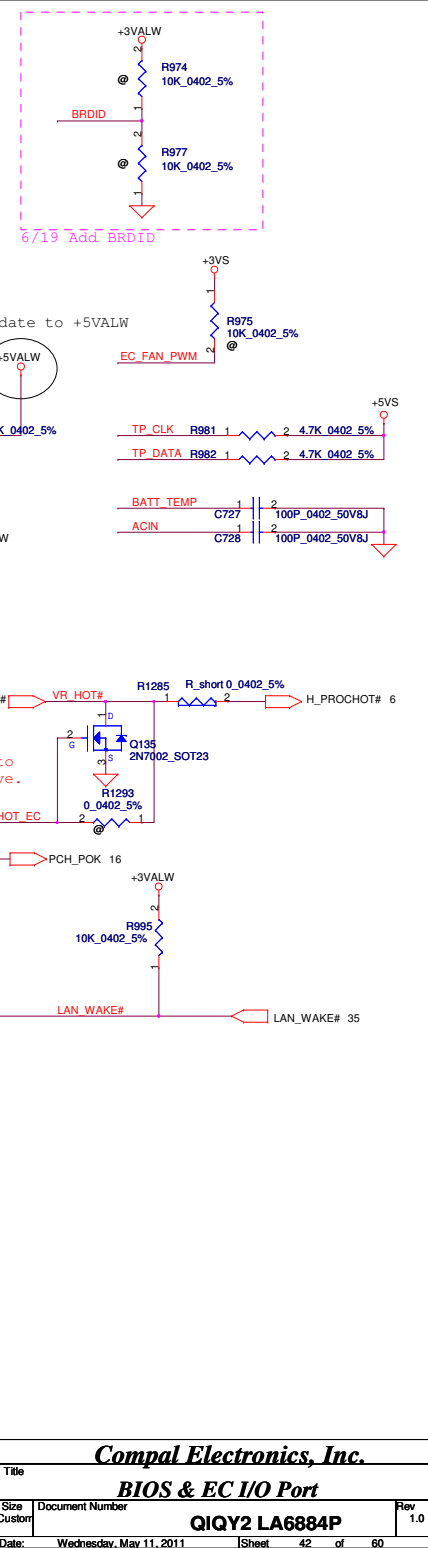
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	AMP Audio speaker CONN
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				KIWB1/B2_LA4601P	
				Date: Wednesday, May 11, 2011	Rev 1.0
				Sheet 40	of 60

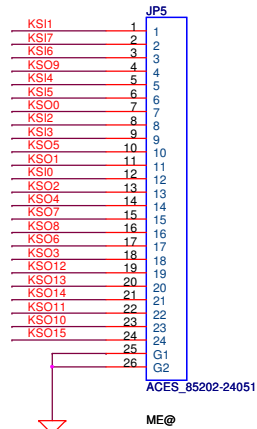
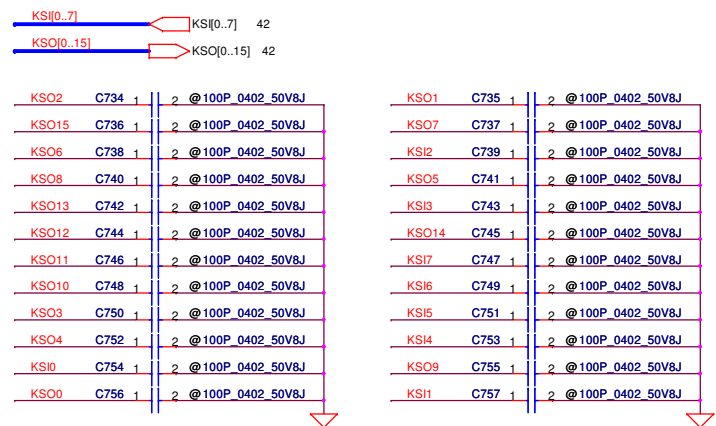


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Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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Size	Custom	Document Number	QIQY2 LA6884P	Rev	1.0
Date	Wednesday, May 11, 2011	Sheet	41	of	60

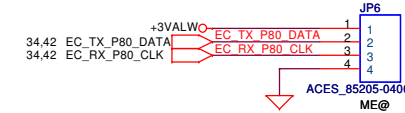


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Issued Date	2010/11/30	Deciphered Date	2011/08	Title		
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				Size	Document Number	Rev
				Custom	QIQY2 LA6884P	1.0
Date:				Wednesday, May 11, 2011	Sheet	42 of 60

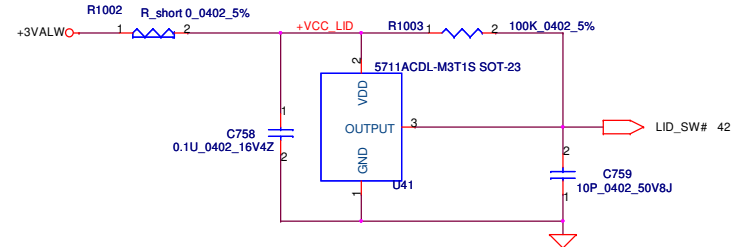
INT_KBD Conn.



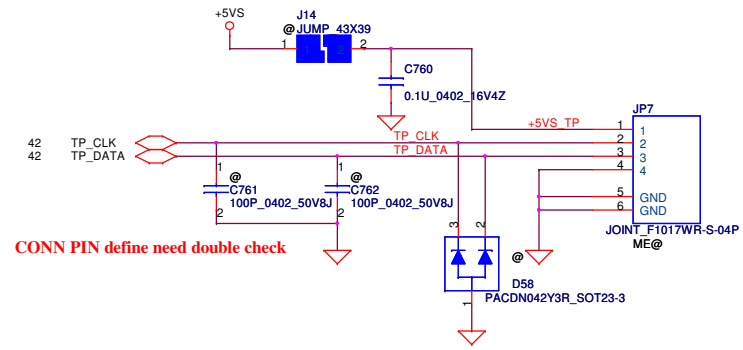
EC DEBUG PORT



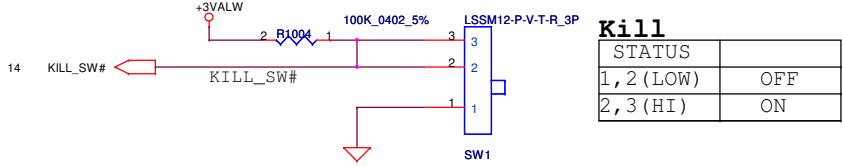
Lid Switch



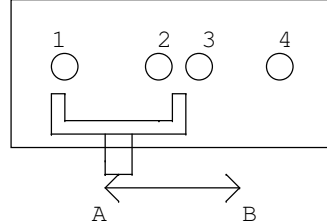
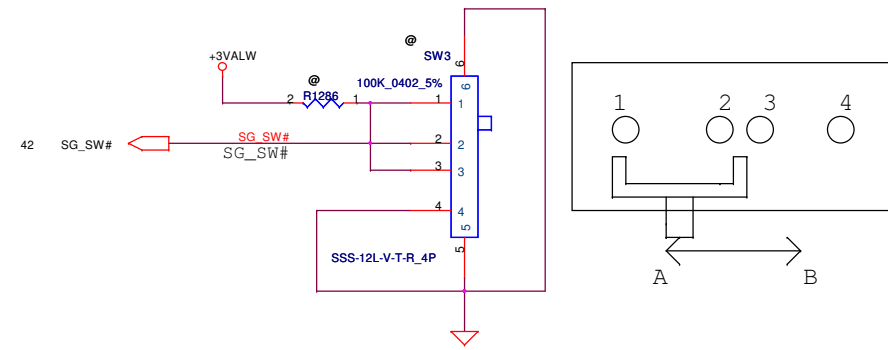
To TP/B Conn.



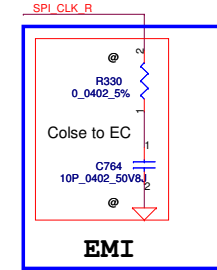
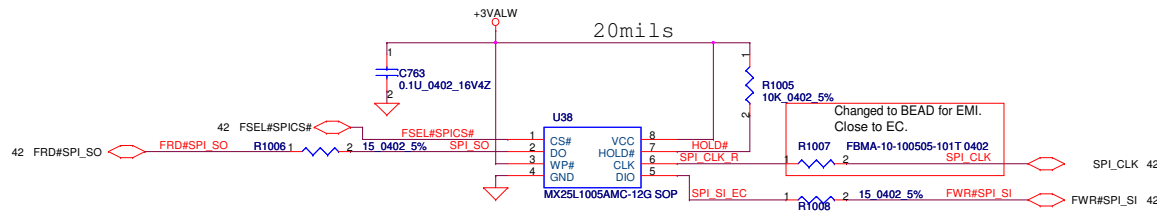
Kill Switch



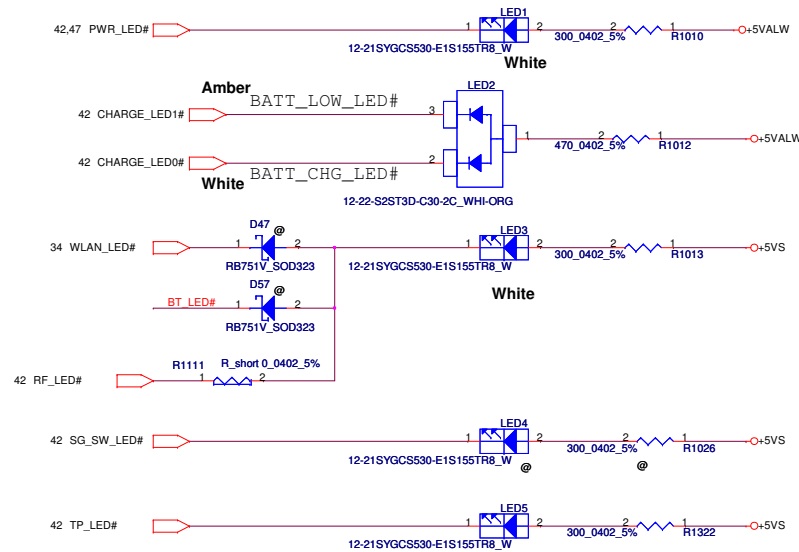
Kill	
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON



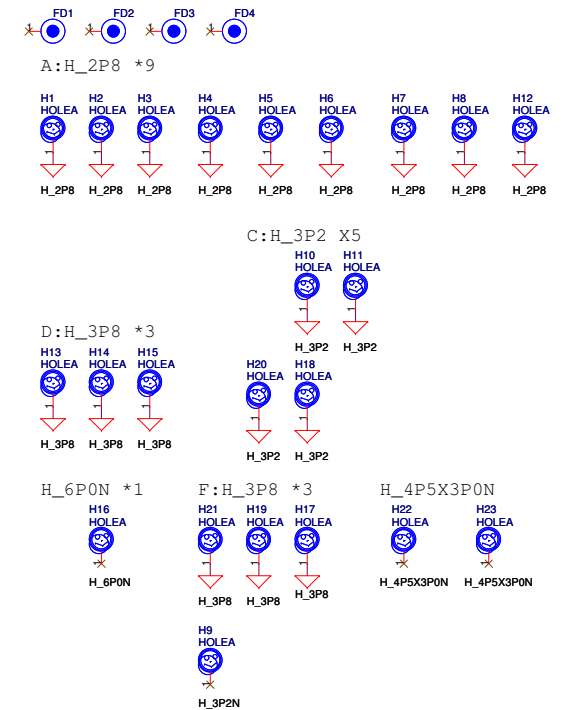
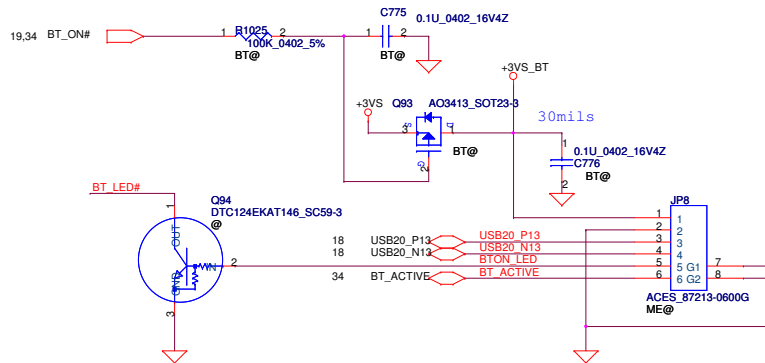
FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100



LED

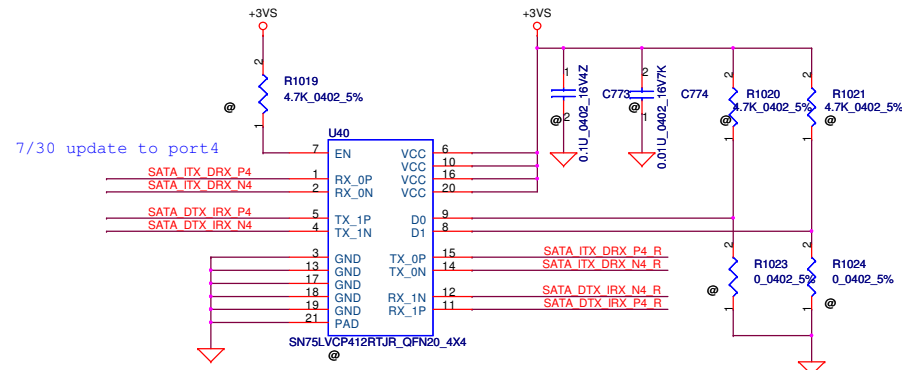
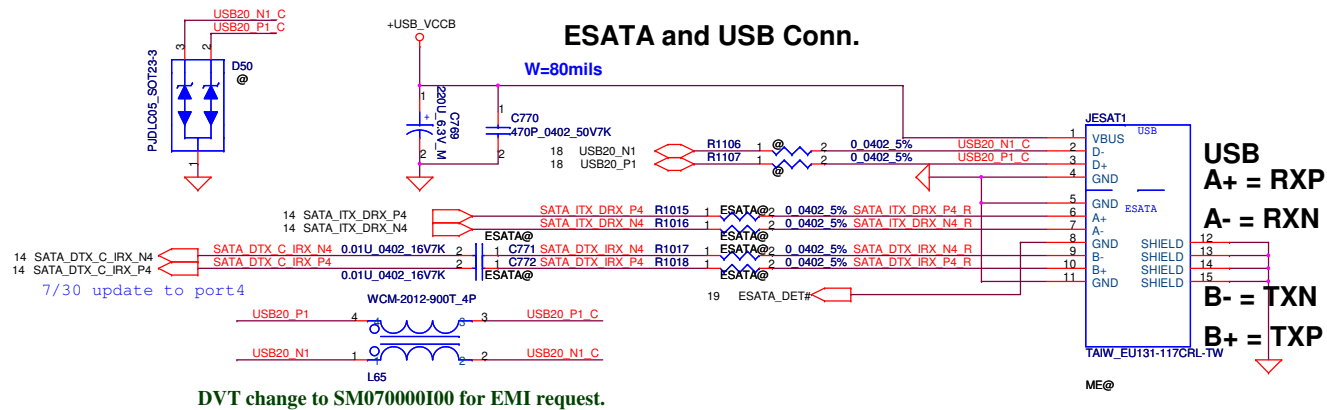
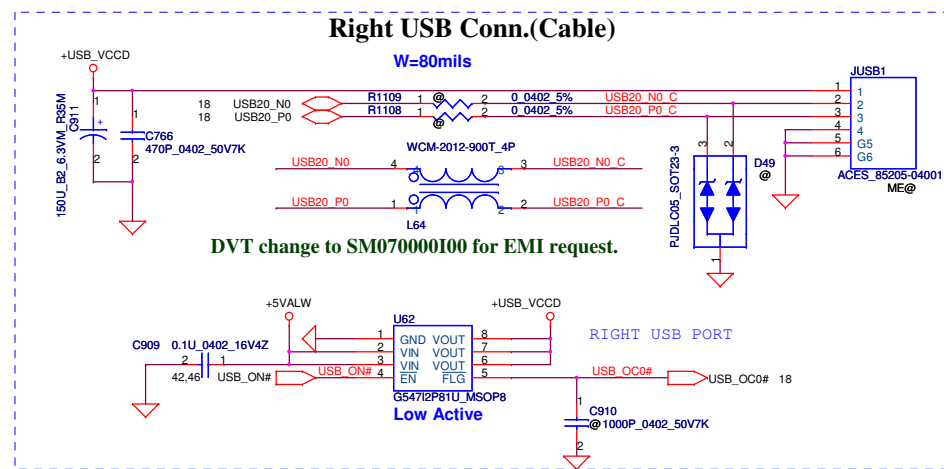
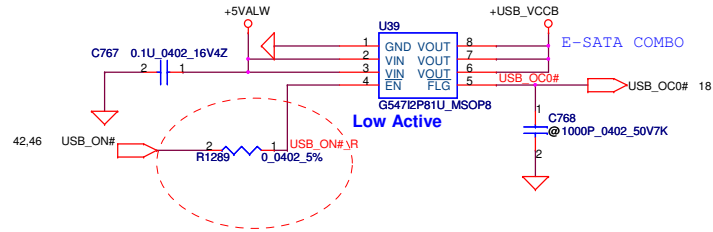


BT MODULE CONN

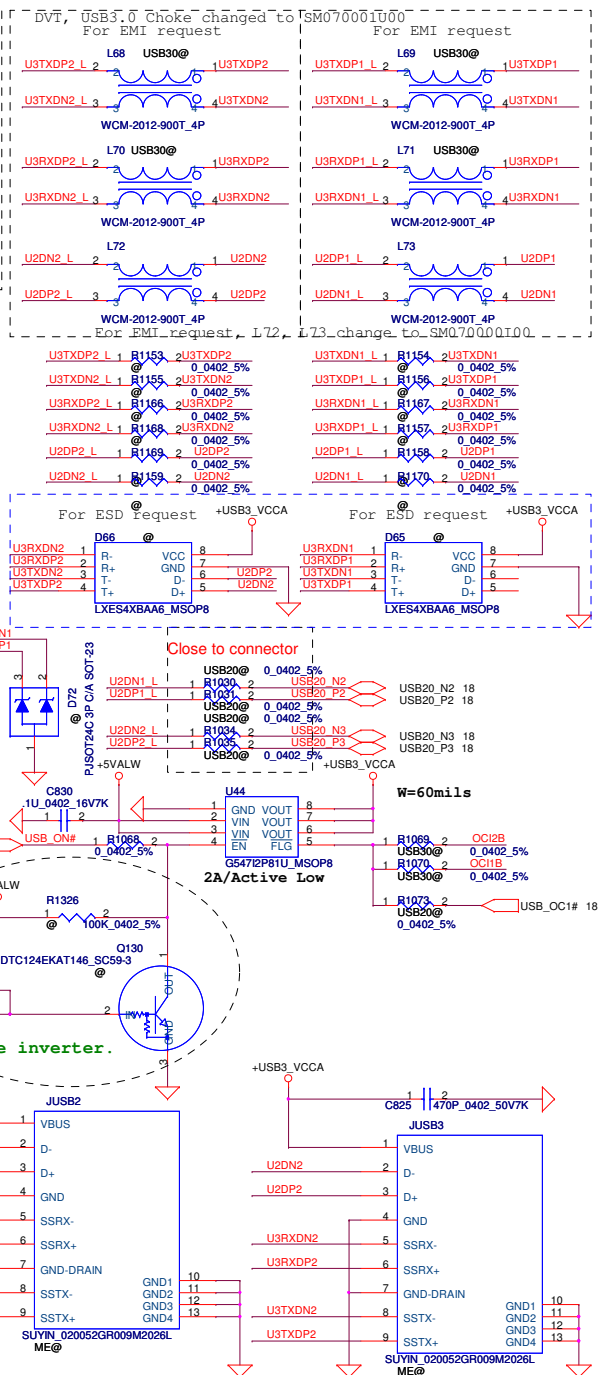
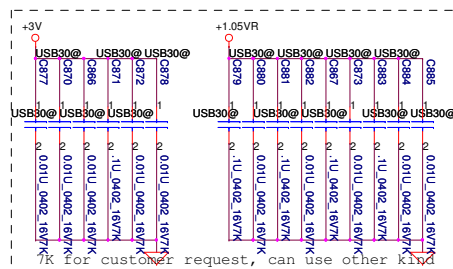
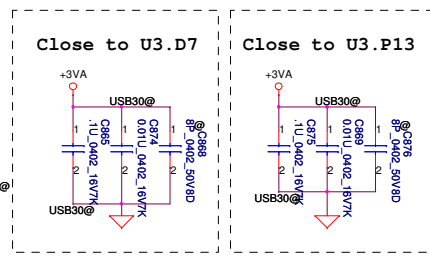
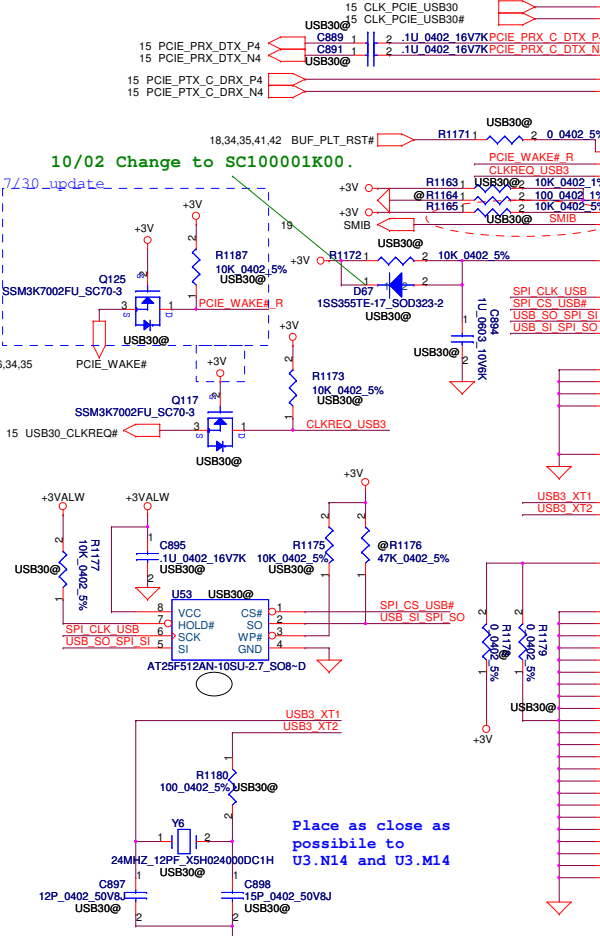
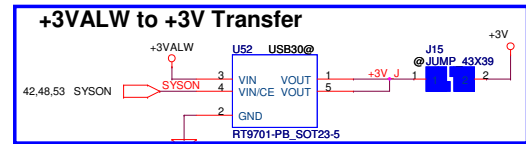
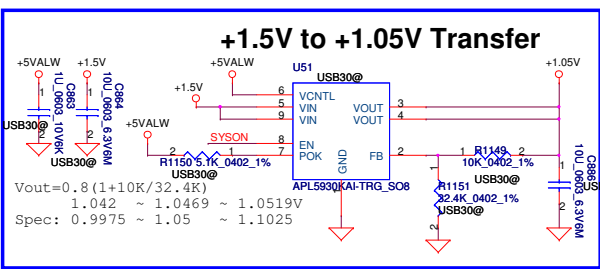


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/11/30		Deciphered Date		2011/08		Title	
										LED/EC SPI ROM/BT	
										Size B Document Number	
										QIQY2 LA6884P	
										Rev 1.0	
										Date: Wednesday, May 11, 2011	
										Sheet 44 of 60	

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				Size	Document Number	Rev			
				Custom	QIQY2 LA6884P	1.0			
Date:				Wednesday, May 11, 2011		Sheet	45	of	60



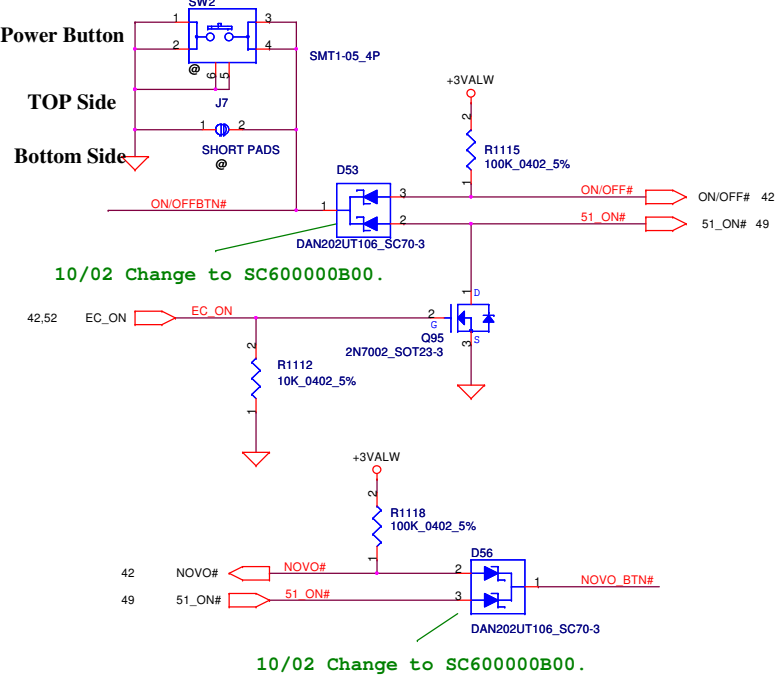
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

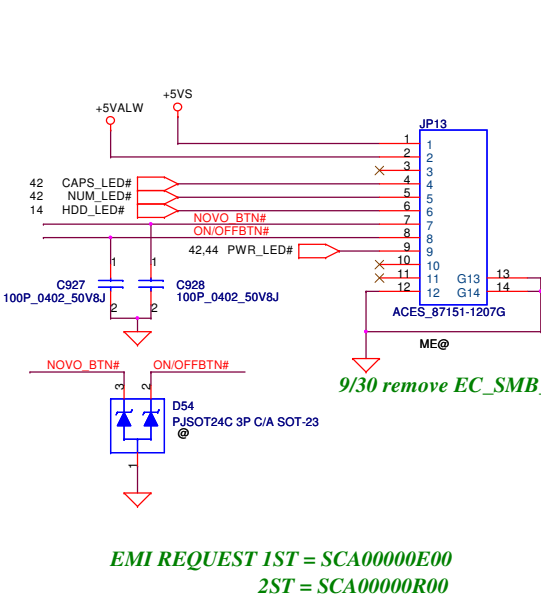
Security Classification	Compal Secret Data
Issued Date	2010/11/30
Deciphered Date	2011/08
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Title	USB3.0 PD270200
Size	Document Number
Customer	
Date	Wednesday, May 11, 2011
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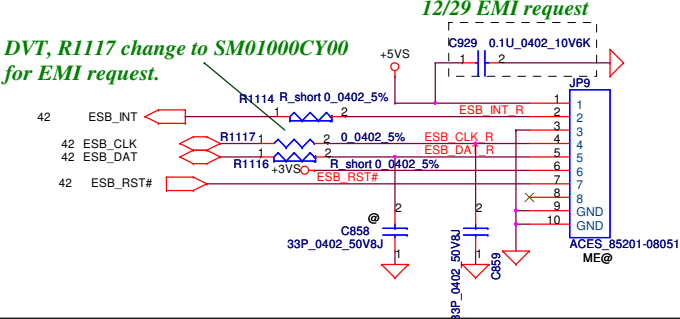
ON/OFF switch



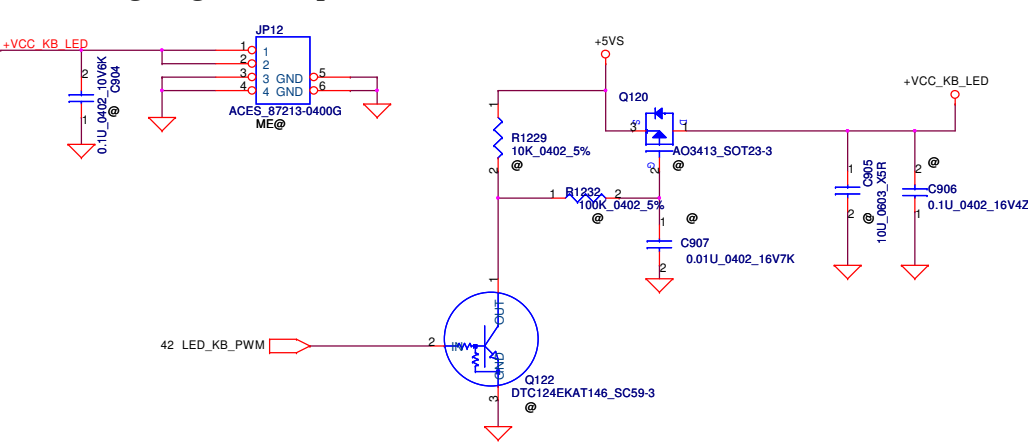
Power Bottom Board Conn. 10pin



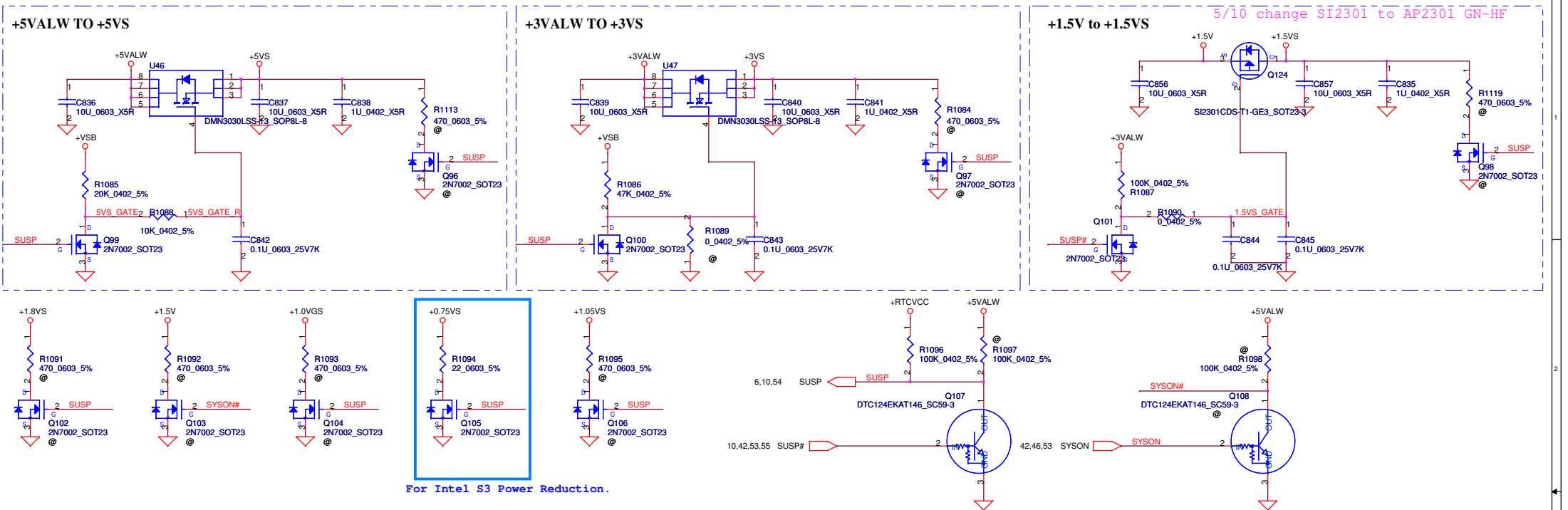
Silder Bar Board Mdule Conn. 6pin



KB Lighting CONN.4pin

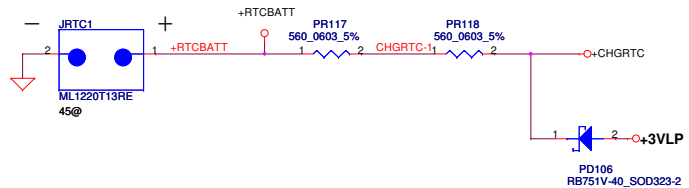
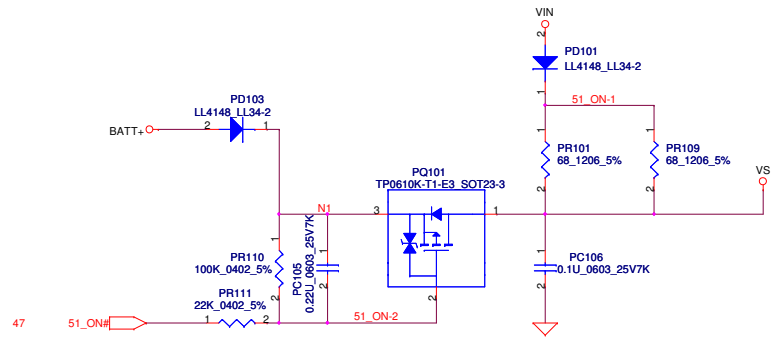
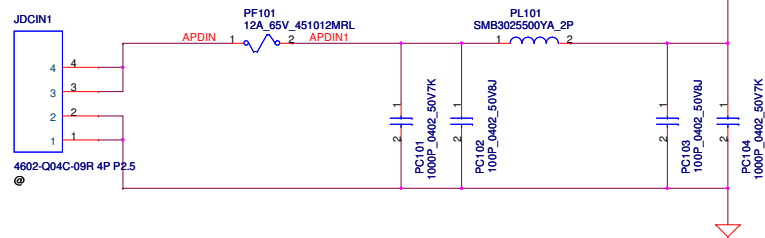


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Size Custom	Document Number	QIQY2 LA6884P		Rev 1.0
Date: Wednesday, May 11, 2011	Sheet	47	of	60

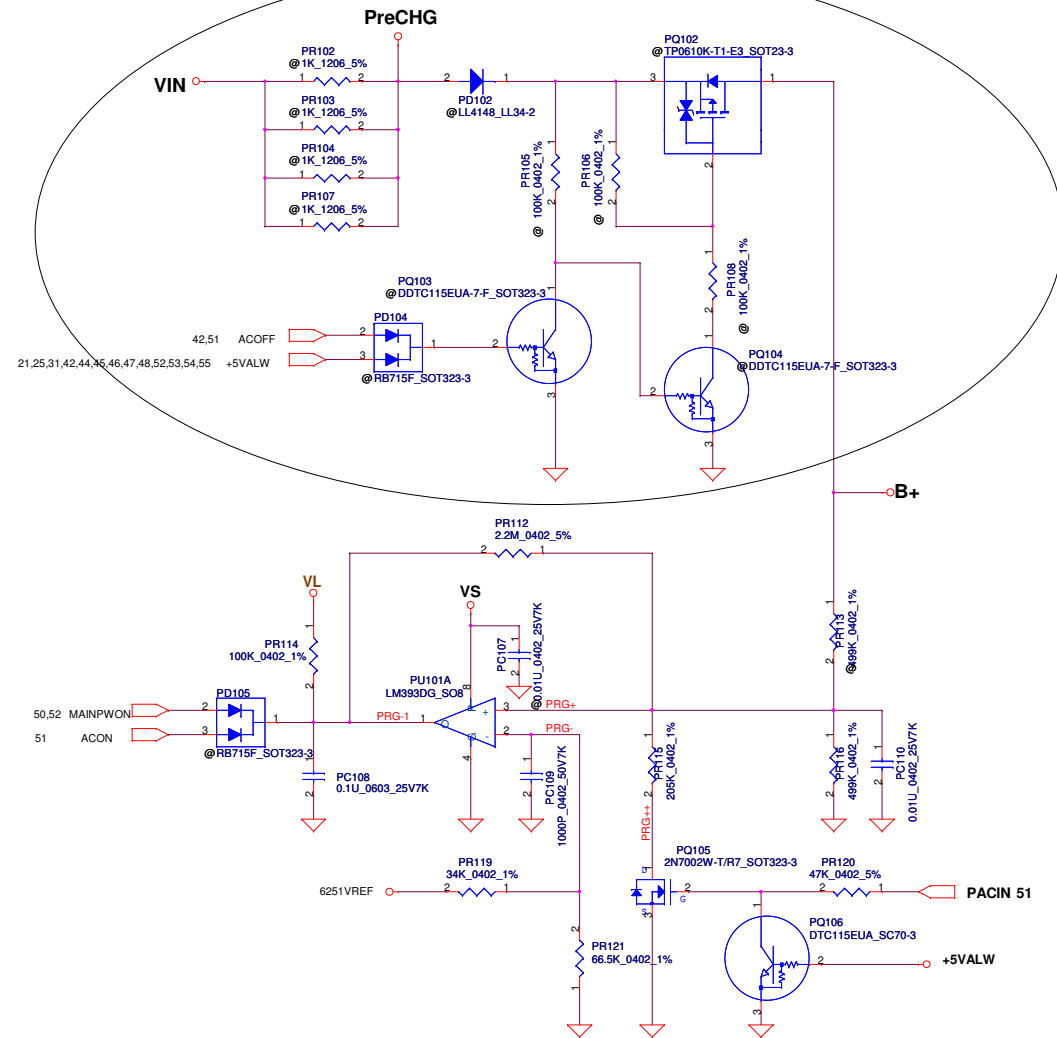


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2010/11/30	Deciphered Date	2011/08	Title
					DC Interface
		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size Custom
					Document Number QIQY2 LA6884P
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					Date: Wednesday, May 11, 2011
					Sheet 48 of 60

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector

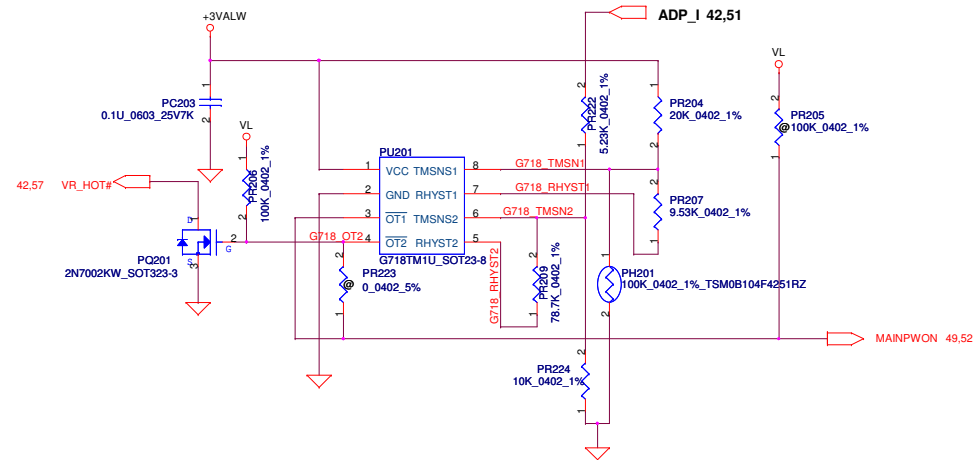
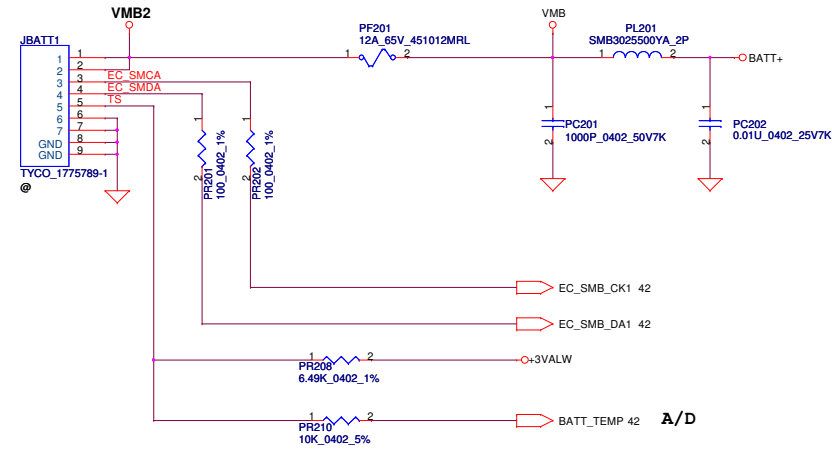
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

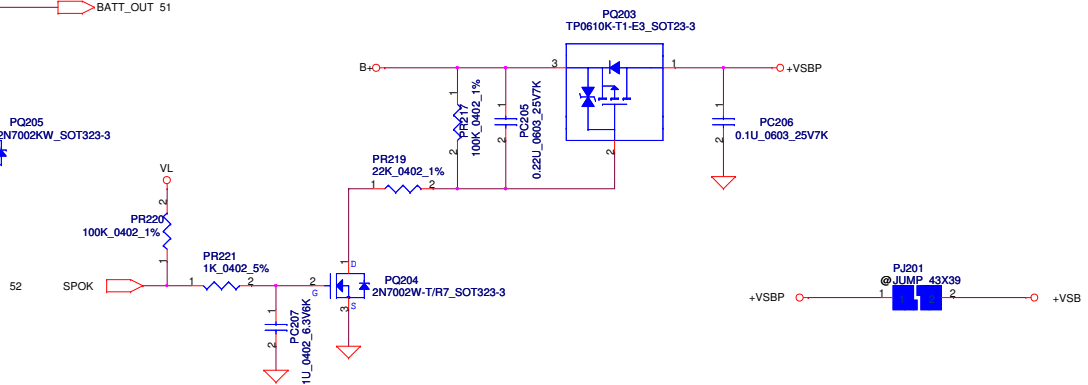
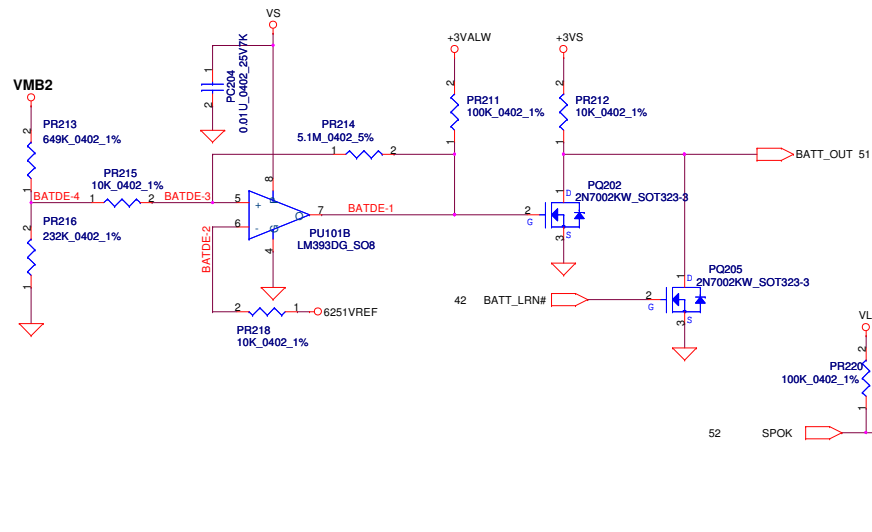
Precharge detector

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

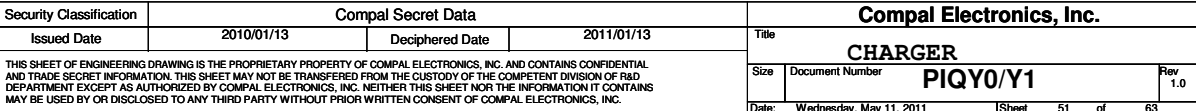
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title PWR DCIN / Vin Detector /Pre-charge		
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				Date Wednesday, May 11, 2011	Sheet 49	of 63



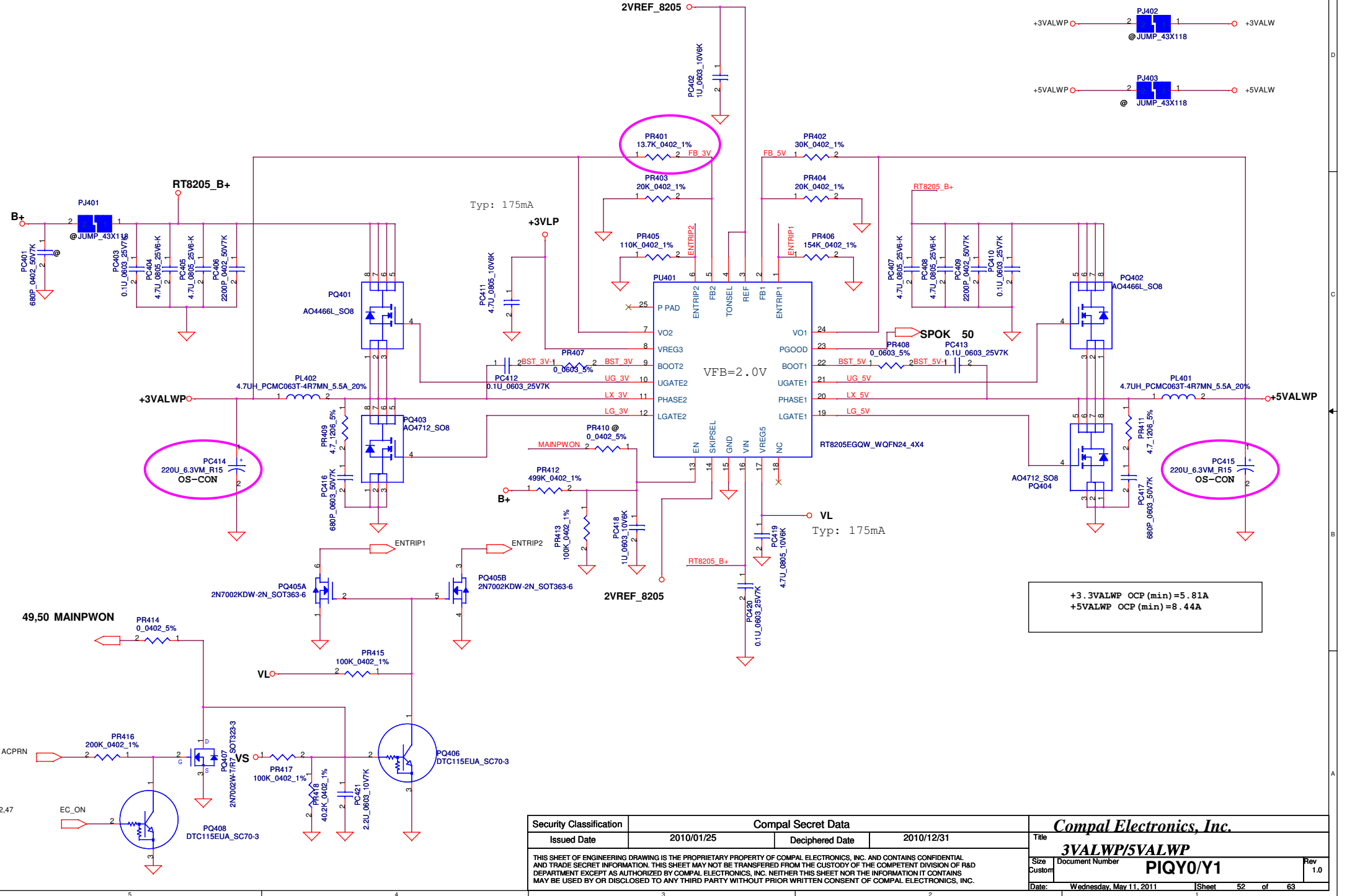
PR222
90W : 6.65K ohm
120W : 5.23K ohm



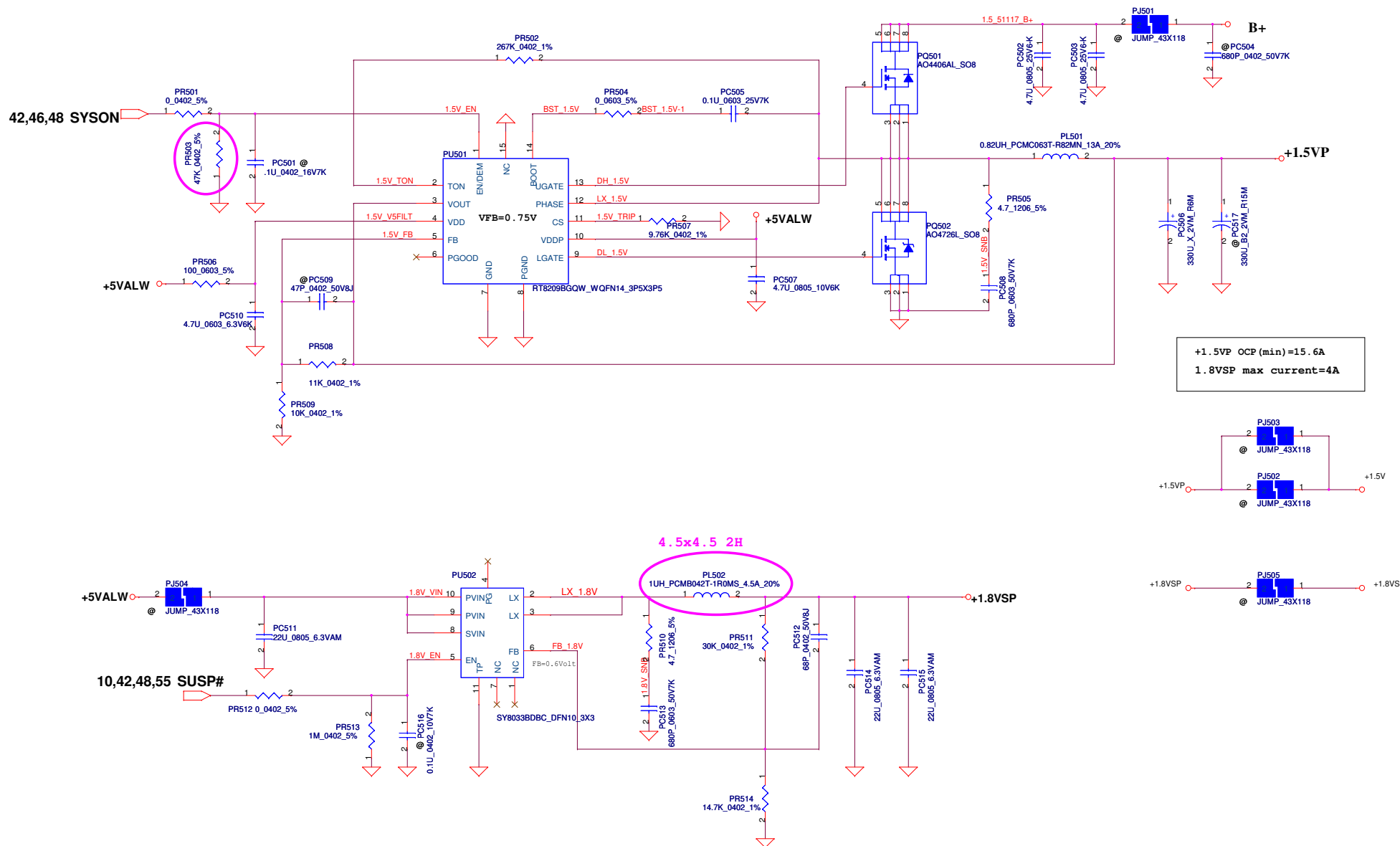
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-BATTERY CONN/OTP	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	
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				Customer	1.0
				Document Number	
				Date:	Wednesday, May 11, 2011
				Sheet	50 of 63



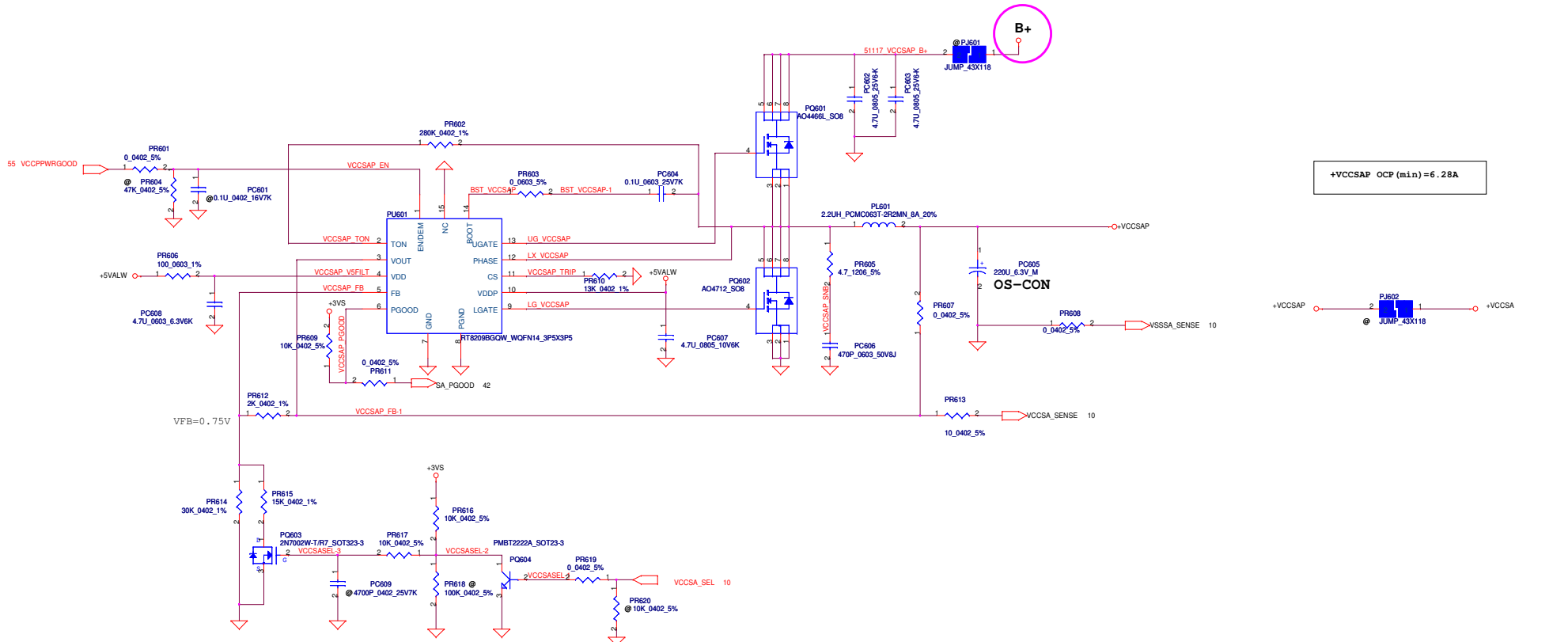
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	3VALWP/5VALWP
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				Date	Wednesday, May 11, 2011
				Sheet	52 of 63
				Rev	1.0

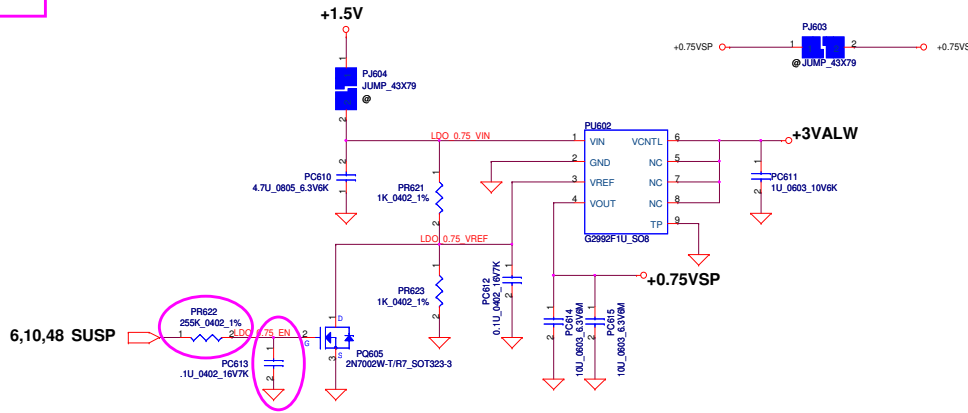


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+1.8VSP
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				Customer	Rev 1.0
				Date	Wednesday, May 11, 2011
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VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

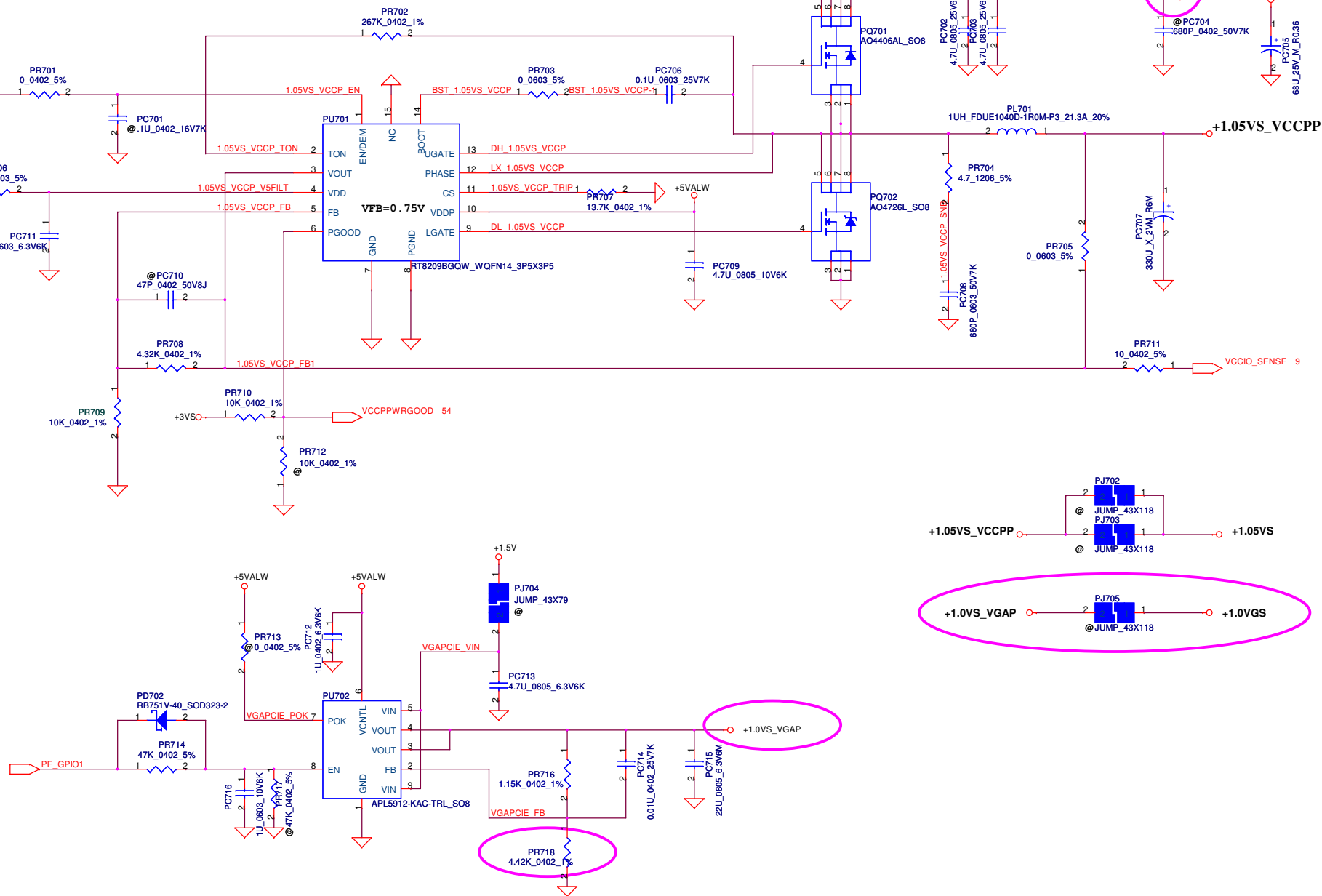
Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



10,42,48,53 SUSP#

+5VALW

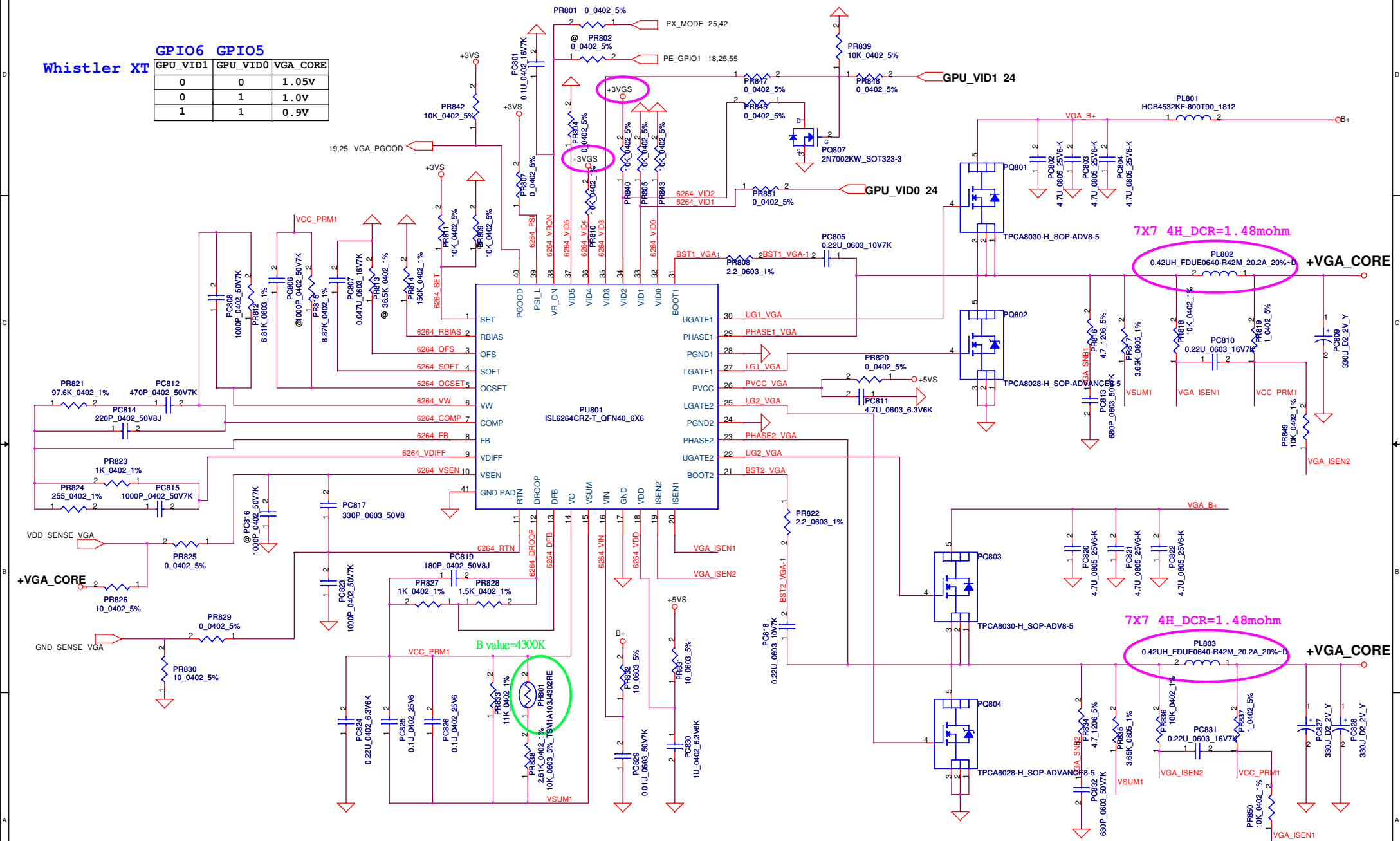
18,25,56 PE_GPIO1



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR +1.05VS VCCPP/1.0VS VGA
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				Date	Wednesday, May 11, 2011
				Sheet	55 of 63

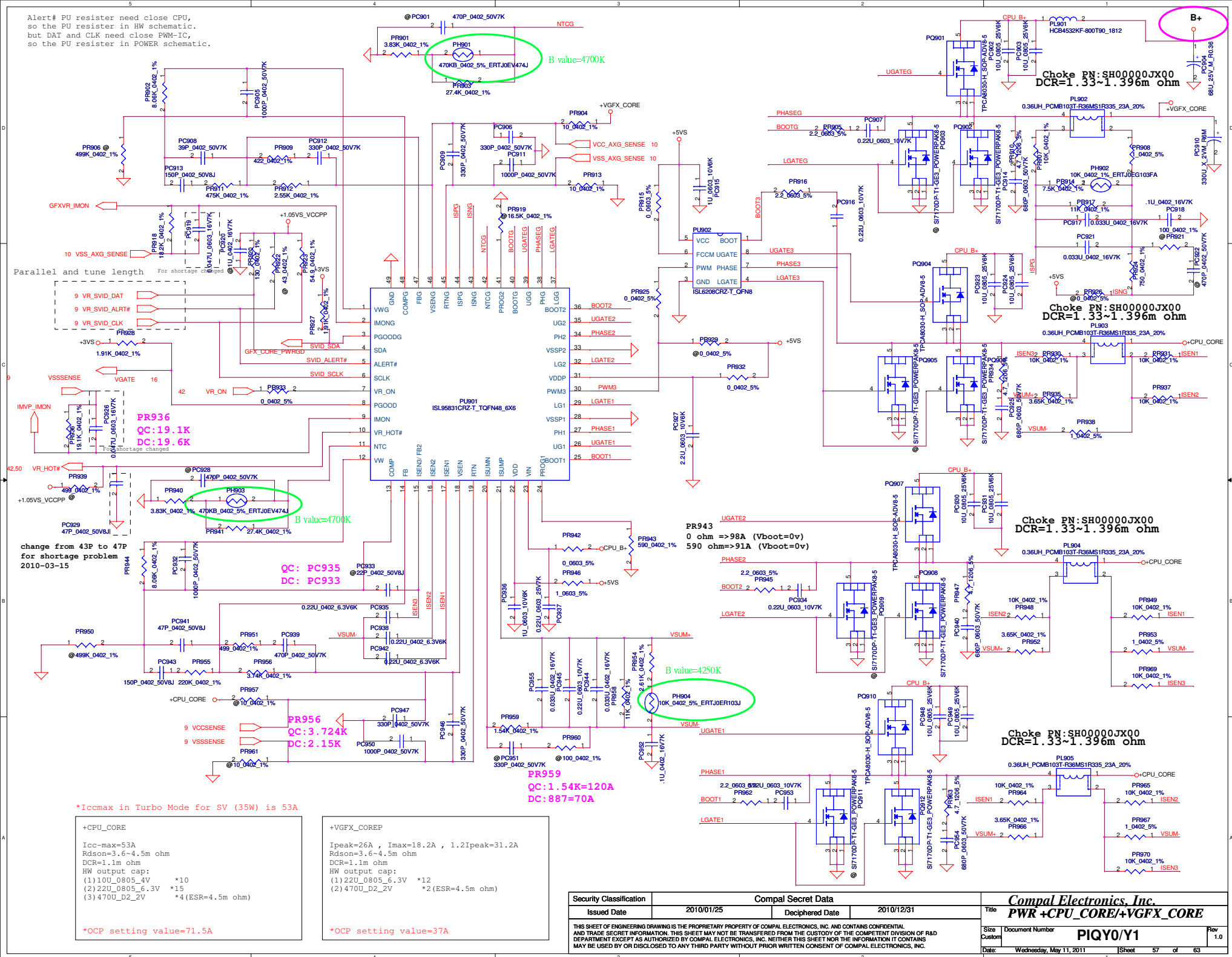
Whistler XT

GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
0	1	1.0V
1	1	0.9V



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/12/12	Deciphered Date	2007/12/12	Title Power-VGA_CORE		
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				Custom		
				Date:	Wednesday, May 11, 2011	

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

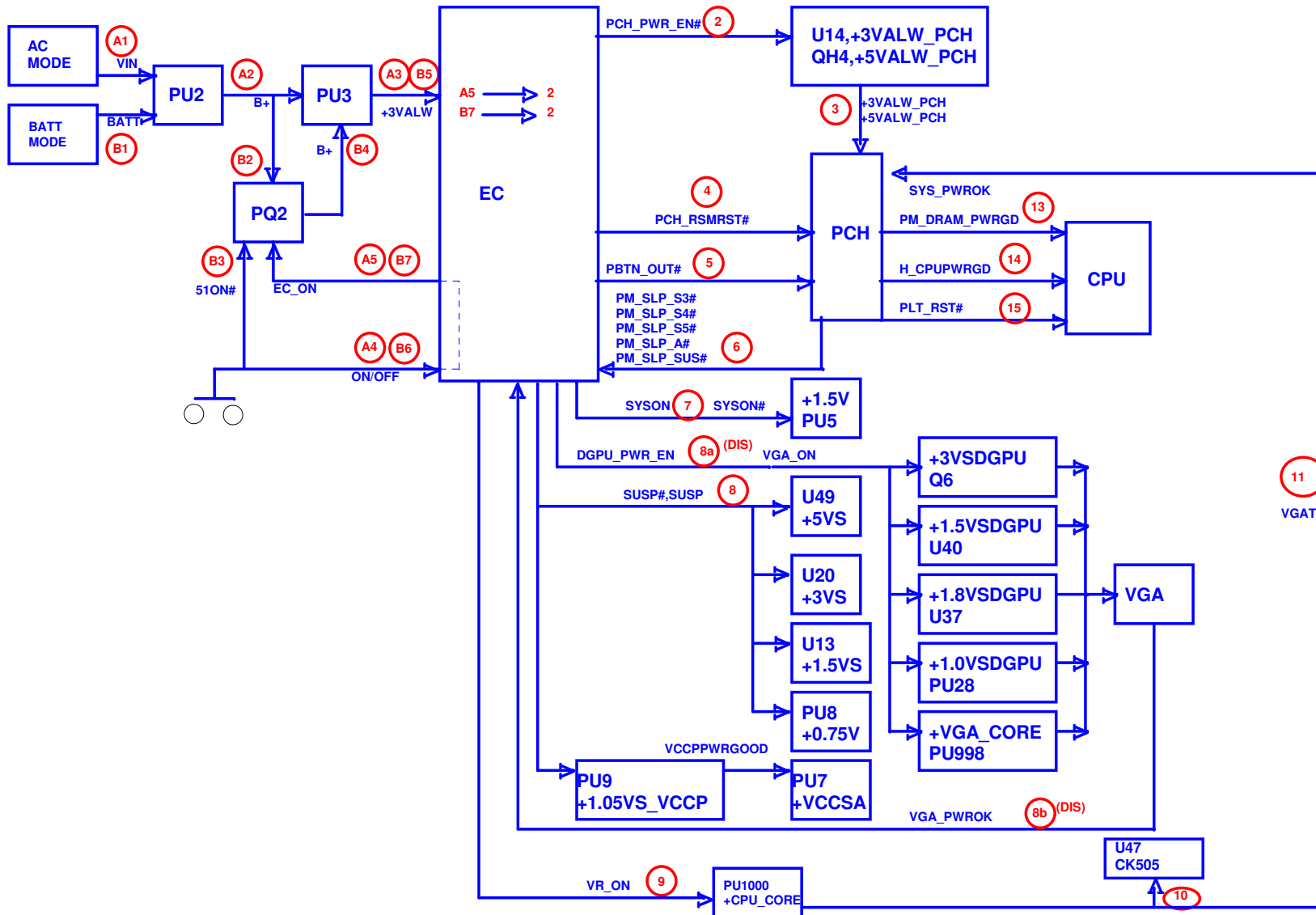


Item	Reason for change	PG#	Modify List	Date	Phase
1	Disable Pre-charge		PR102, PR103, PR104, PR107, PD102, PD104, PQ102, PQ103, PQ104		
2	Back to Back MOS change		PQ301, PQ302, PQ303		
3	Battery Learning function		PQ205		
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 QIQY2 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	
					SDV
1		P23	Change U8 to SA00004R500	Customer need to change	
2		P23	Del C998/ C1067/ C343/ C339/ C382/ C376/ C377/ R692	For VGA function	
3		P23	Change Q69 to Q75, Q68 to Q76, U56 to U62, U60 to U64, Q87 to Q109, Q86 to Q110, C732 to C777, U59 to U66, R872 to R890, U37 to U41	For VGA function	
4		P42	Del R994/ R999/ D46/ Q91	For EC function	
5		P15	Del PJP2/ R67/ R257/ R261	For PCH function	
6		P23	Del C386/ C732/ R1400/ R1360	For VGA function	
7		P33	Del R354/ R3461/ R1372/ R1373 Del R185/ R434/ Q84/ R1022/ Q92/ CV253-CV260/ Q115/R1144/ R1143/ L67/ R997/ R1321	For HDMI function	
8		P44	BT_OFF# change to BT_ON#	For BT function	
9		P35	EC_PME# change to LAN_WAKE#	For LAN wake funcion	
10		P32	CMOS_OFF# change to CMOS_ON#	For CMOS function	
11		P45	U11 from SB000007010 change to SB548000210	For +1.5VGS function	
12		P32	D31~D35 from +5VS change to +CRT_VCC_CONN	For CRT function	
13		P15	U4 from SA00004EEJ0 change to SA00004EEV0	PCH from rev.B2 change to rev.B3	
14		P14	R133 from 0 ohm change to 33 ohm	For BIOS ROM function	
					SIT
1		P23	Add C69 22uF_0805 cap for +BIF_VDDC.	For vendor feedback	
2		P23	Reserve R613 & R614 to pull up +3VS.	For VGA function	
3		P23	Change 0 ohm to R_short --- R10/R1002/R1014/R1029/R109/ R11/R1111/R1114/R1116/R1280/R1281/R1282/R1283/R1285/ R130/R1320/R1336/R1342/R1323/R14/R181R19/R190/R193/R196/ R198/R207/R22/R222/R254R256/R258/R26/R260/R263/R265/R269 /R270/R272R273/R274/R276/R277/R278/R281/R282/R283/R284/ R285/R286/R288/R289/R293/R295/R302/R303/R313/R40/R432/ R52/R53/R668/R710/R824/R825/R880/R882/R885/R886/R891/ R922/R941/R969/R973/R993/R996.	For IO/ PCH/ VGA function	
4		P45	U39/ U62 /U44 from SA000039E00 change to SA00003TV00.	For USB function	
5		P18	Del net name PCH_GPI051 connect to RP1 pin2.	For VGA function	
6		P25	C351 from 0.1uF_0603 change to 0.047uF_0402.	For VGA function	
7		P10	ADD PJP2 jump.	For PCH function	
8		P43	U41 from SA000031C00 change to SA00001TC00.	For LID function	
9		P25	R352 from 0 ohm change to 330K ohm.	For VGA function	
10		P25	Add C343 & C346 for reserve.	For VGA function	
11		P25	Q121 from SBX01240010 change to SB000008J10.	For VGA function	

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