VNKAE

Rosetta 10AN/10ANG

LA-9868P REV 1.0 Schematic

AMD KABINI Quad Core 25W only for UMA
AMD KABINI Quad Core 15W for DIS&UMA
2013-03-18 Rev 1.0

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: *Cover Page*		
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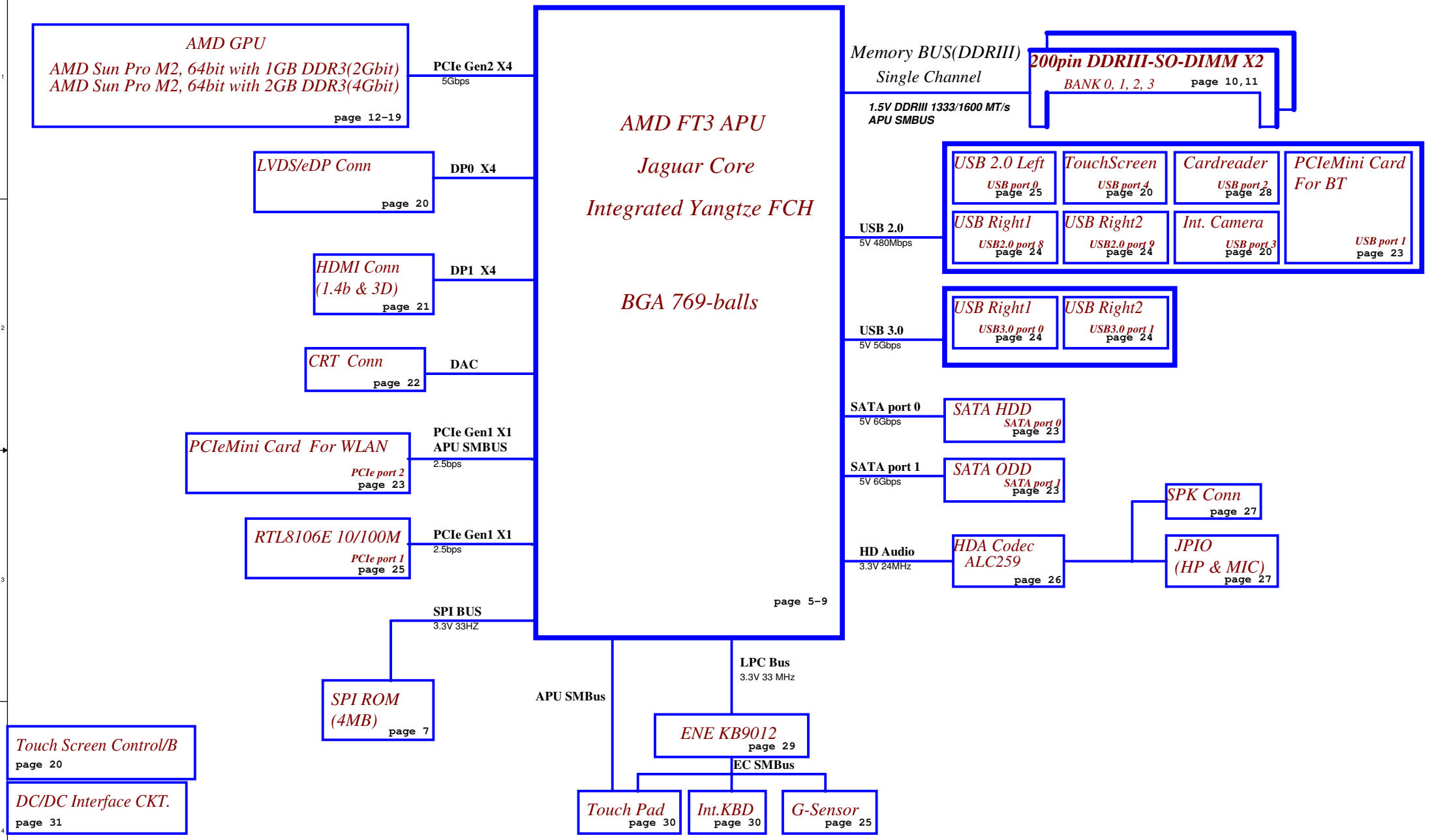

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Title	Block Diagram		
Size	Document Number	LA-9868P	Rev 1.0
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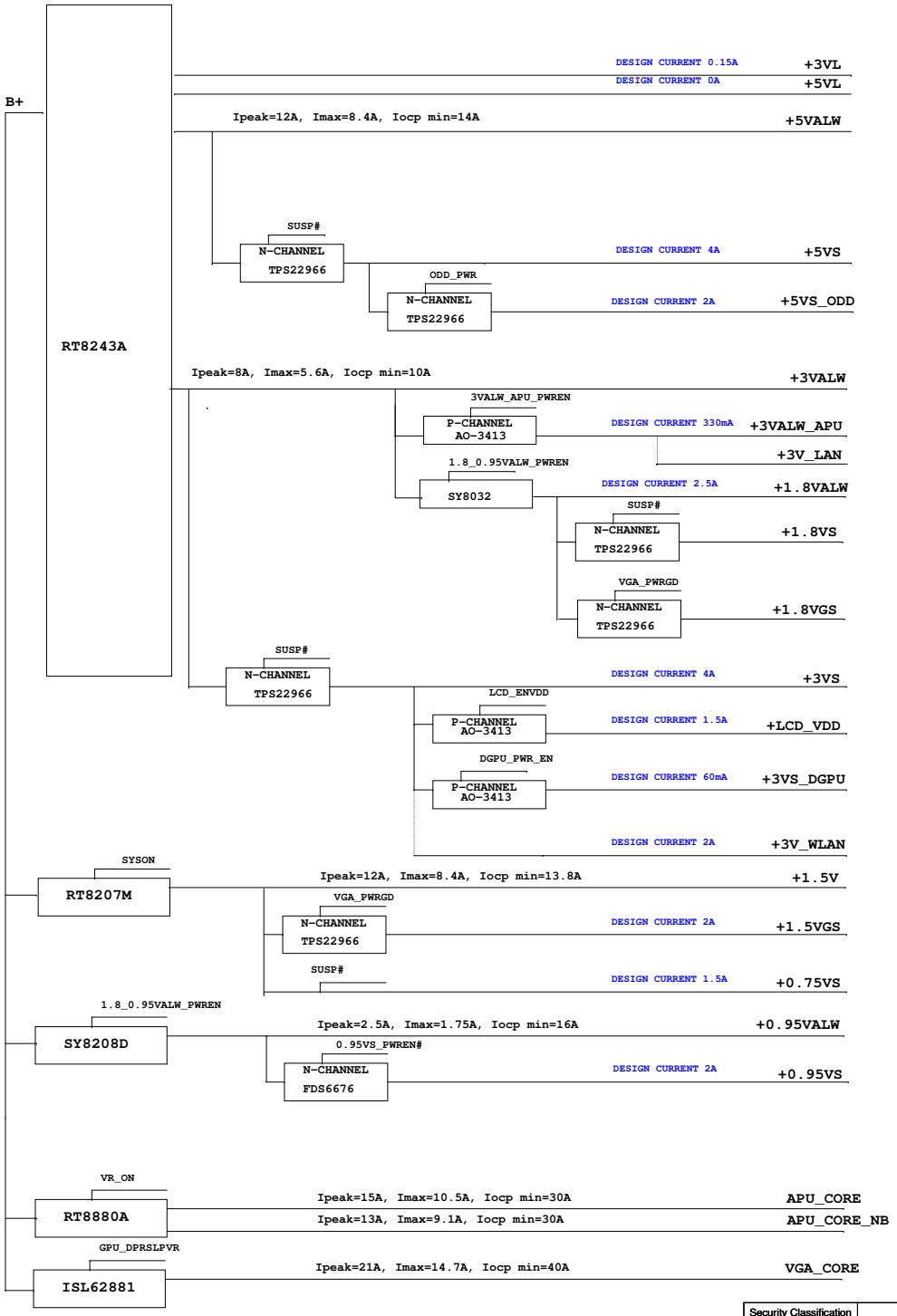

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Title: **Power Tree**

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Voltage Rails

(O MEANS ON X MEANS OFF)

UMA

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function									
description									
explain									
BTO									

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX Address
+3VS	DDR SO-DIMM A	A0H 1010 0000 b
+3VS	DDR SO-DIMM B	A2H 1010 0010 b
+3VS	WLAN	

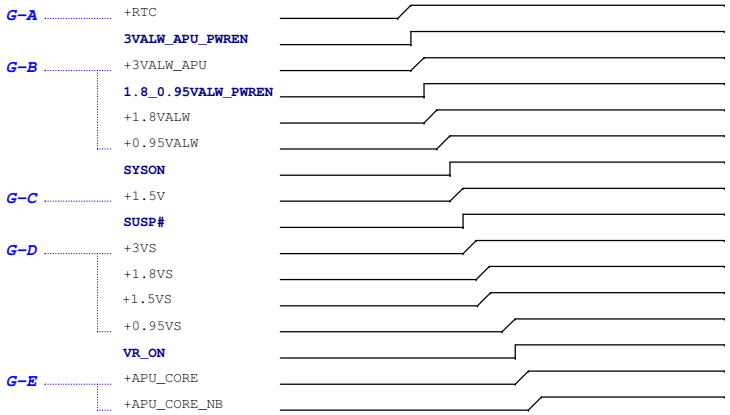
EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b
+3VL	Charger	12H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	G-Sensor	40H	0100 0000 b
+3VS	VGA thermal	82H	1000 0010 b
+3VS	APU thermal	98H	1001 1000 b

APU POWER SEQUENCE



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Title	Notes List		
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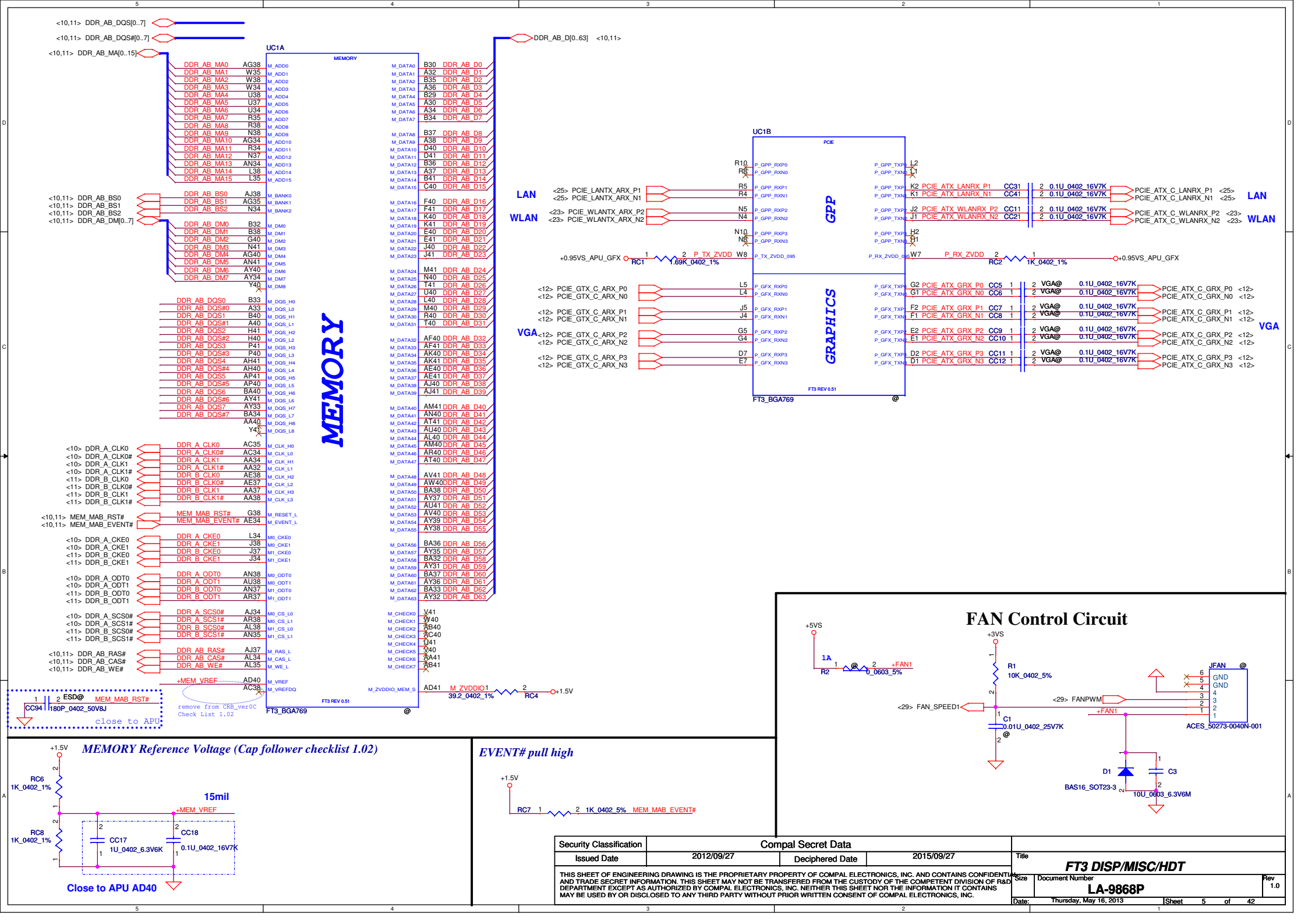
MEMORY
UC1A
UC1B
PCIE
GPP
GRAPHICS
FT3_BGA769
FT3 REV 0.51
LAN
WLAN
VGA
FAN Control Circuit
MEMORY Reference Voltage (Cap follower checklist 1.02)
EVENT# pull high
Close to APU AD40
close to APU
15mil
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Compal Secret Data
Issued Date
2012/09/27
Deciphered Date
2015/09/27
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Title
FT3 DISP/MISC/HDT
Size
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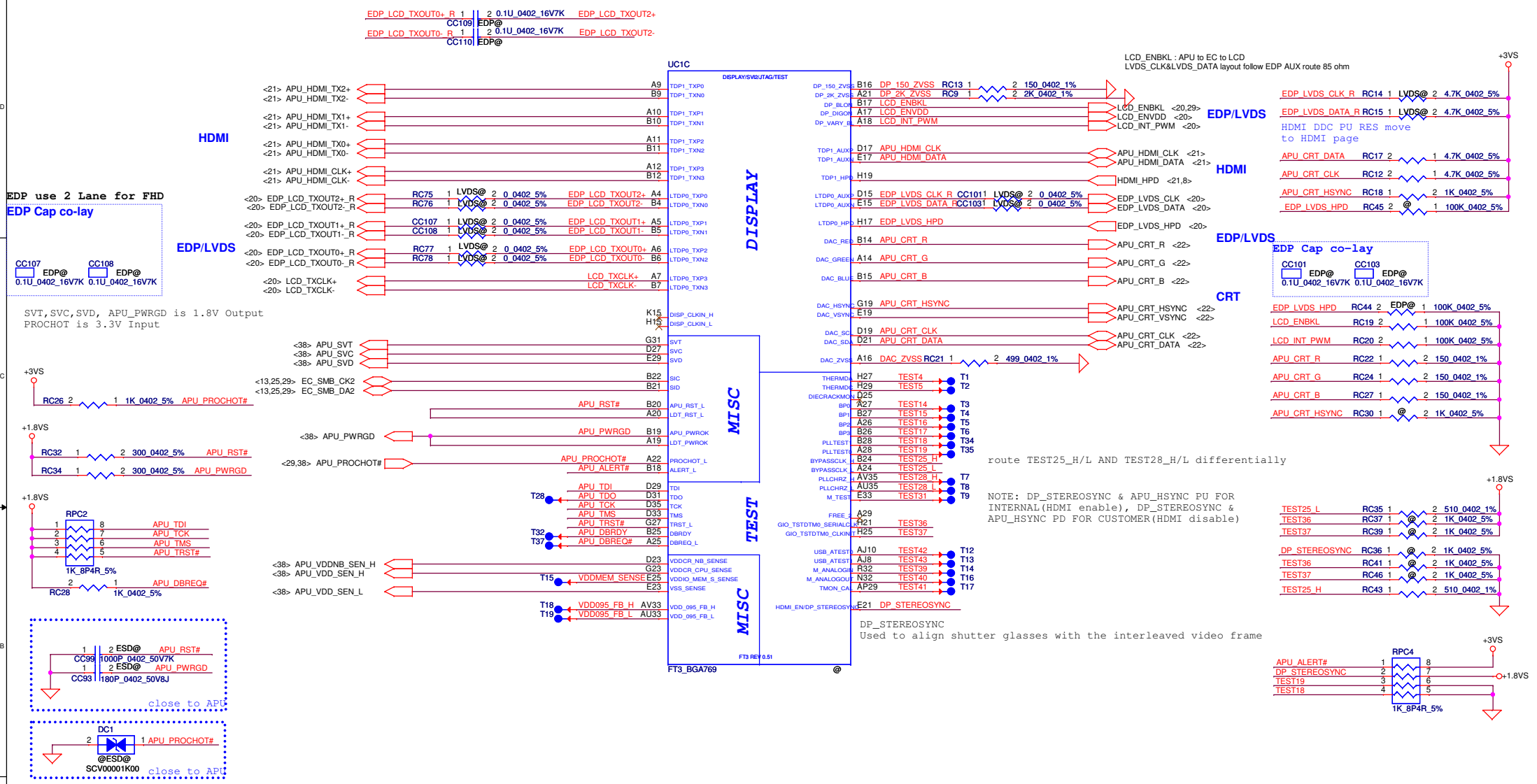

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Title	FT3 DISP/MISC/HDT		
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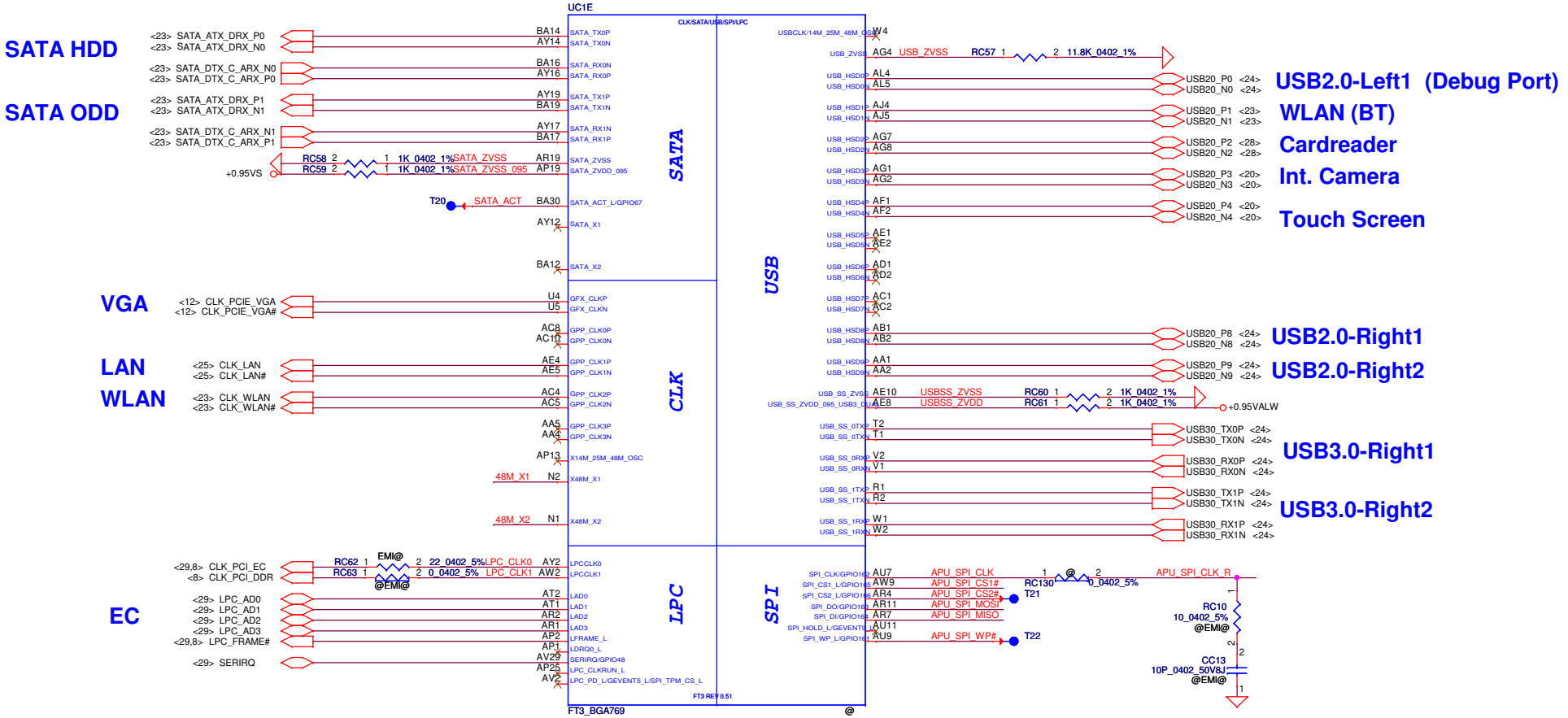
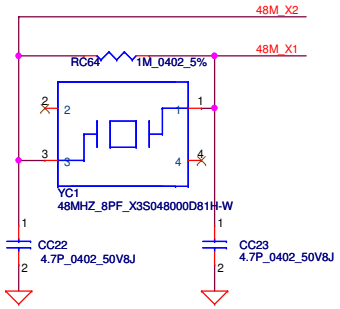
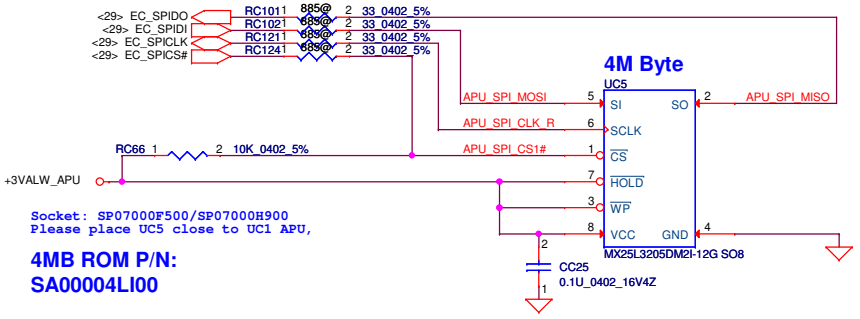


48KMHz CRYSTAL



SPI ROM



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Title	FT3-SATA/CLK/USB/SPI/LPC		
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Follow check list & ORB_0C
design 10 ms RC delay circuit
on +1.8-V S5 power rail.

close to APU

AMD G3-S5 clock issue

SLP_S3#, SLP_S5# PU reserve

UC1D

ACPI/SD/AZ/GPIO/RTC/MISC

Sequence

SD

IR

GPIO

MSIC

HDA

RTC CLK

FT3_BGA769

FT3 REV 0.51

PCIE_RST# is for PCIE devices on APU

A_RST# is for LPC devices

APU SMBus0 for S0 , SMBus1 for S5
If APU_SMBUS no use pull high 10K

GPIO174 PD CHK1.03

SW request

VRAM_SEL
Control by X76

Place at GPU

For DIS

close to APU

STRAP PINS

	CLK_PCI_EC	CLK_PCI_DDR	LPC_FRAME#	GEVENT2	RTC_CLK
PULL HIGH	BOOT FAIL TIMER	CLKGEN ENABLE DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT	FAST POWER UP/RESET TIMING FOR SIMULATION

PANEL_SEL	H	L
	eDP panel	LVDS panel

TOUCH_SEL	H	L
	Touch Panel	Non Touch Panel (turn off EHCI)

SM_EN	H	L
	Sleep& PlayMusic (ALC269)	ALC259

Board Conf.	Board_ID0	Board_ID1
PX5	0	0
Reserved	0	1
DIS	1	0
UMA	1	1

SPK_DET	Onkyo	No Brand
	0	1

ODD DA#

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Title: FT3 GPIO/AZ/MISC

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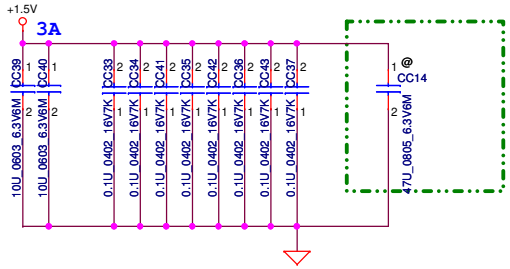
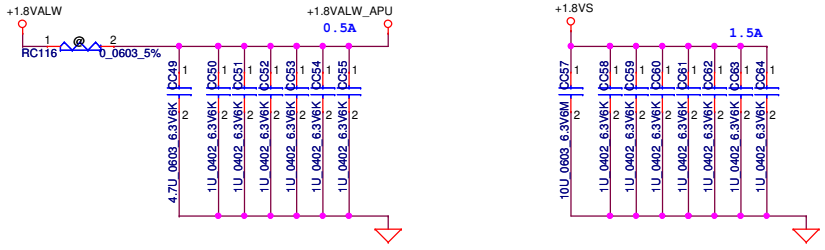
1.5V OF APU

AMD CKL v1.01	10uF	0.1uF	180pF
VDDIO_MEM_S	2	8	4

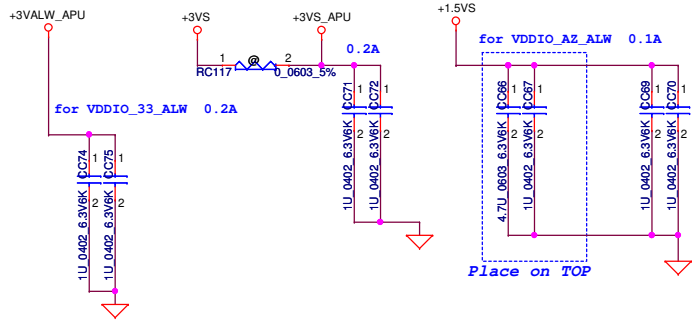


1.8VALW & 1.8VS OF APU

AMD CKL v1.01	10uF	4.7uF	1uF	180pF
VDD_18	1		7	1
VDD_18_ALW		1	6	1

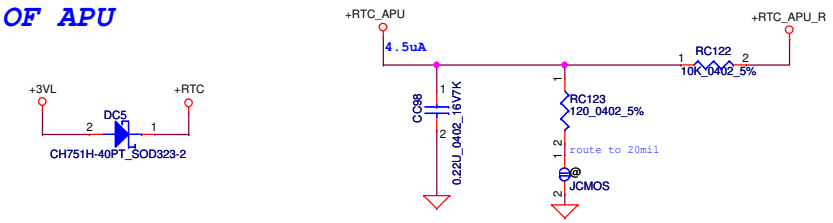


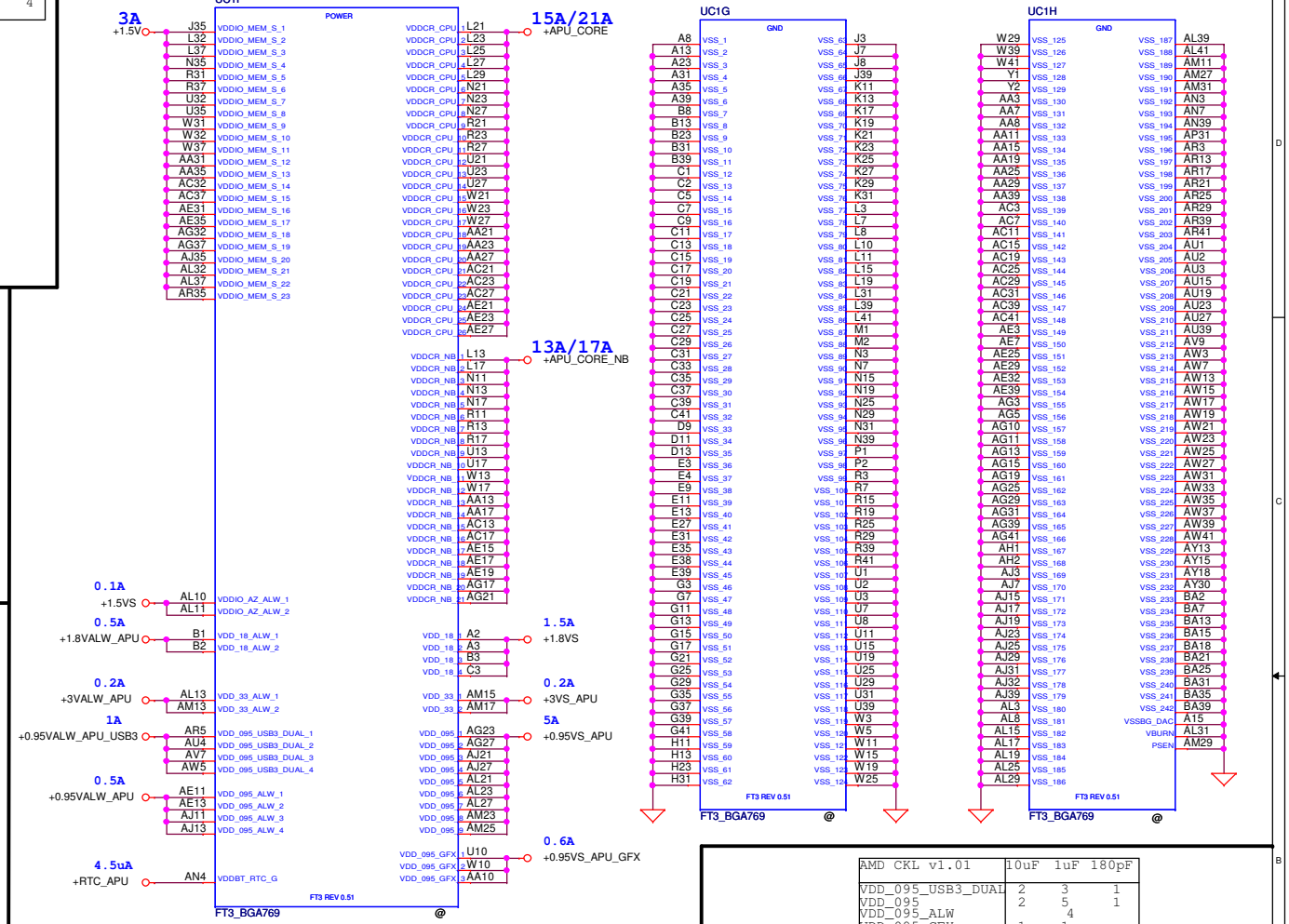
3.3VALW & 3.3VS OF APU



AMD CKL v1.01	4.7uF	1uF	180pF
VDDIO_AZ_ALW	1	3	1
VDDIO_33_ALW		2	
VDDIO_33		2	1

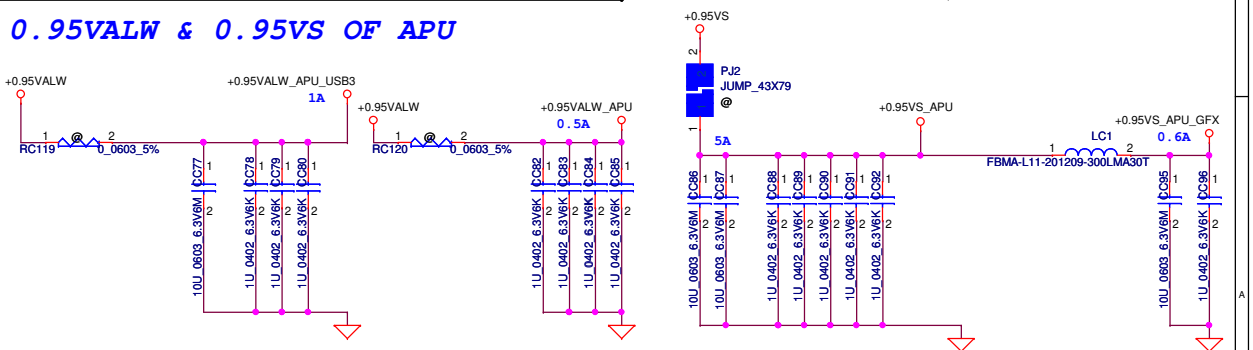
RTC OF APU





AMD CKL v1.01	10uF	1uF	180pF
VDD_095_USB3_DUAL	2	3	1
VDD_095	2	5	1
VDD_095_ALW		4	
VDD_095_GFX	1	1	

0.95VALW & 0.95VS OF APU



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Title: **FT3 PWR/GND**

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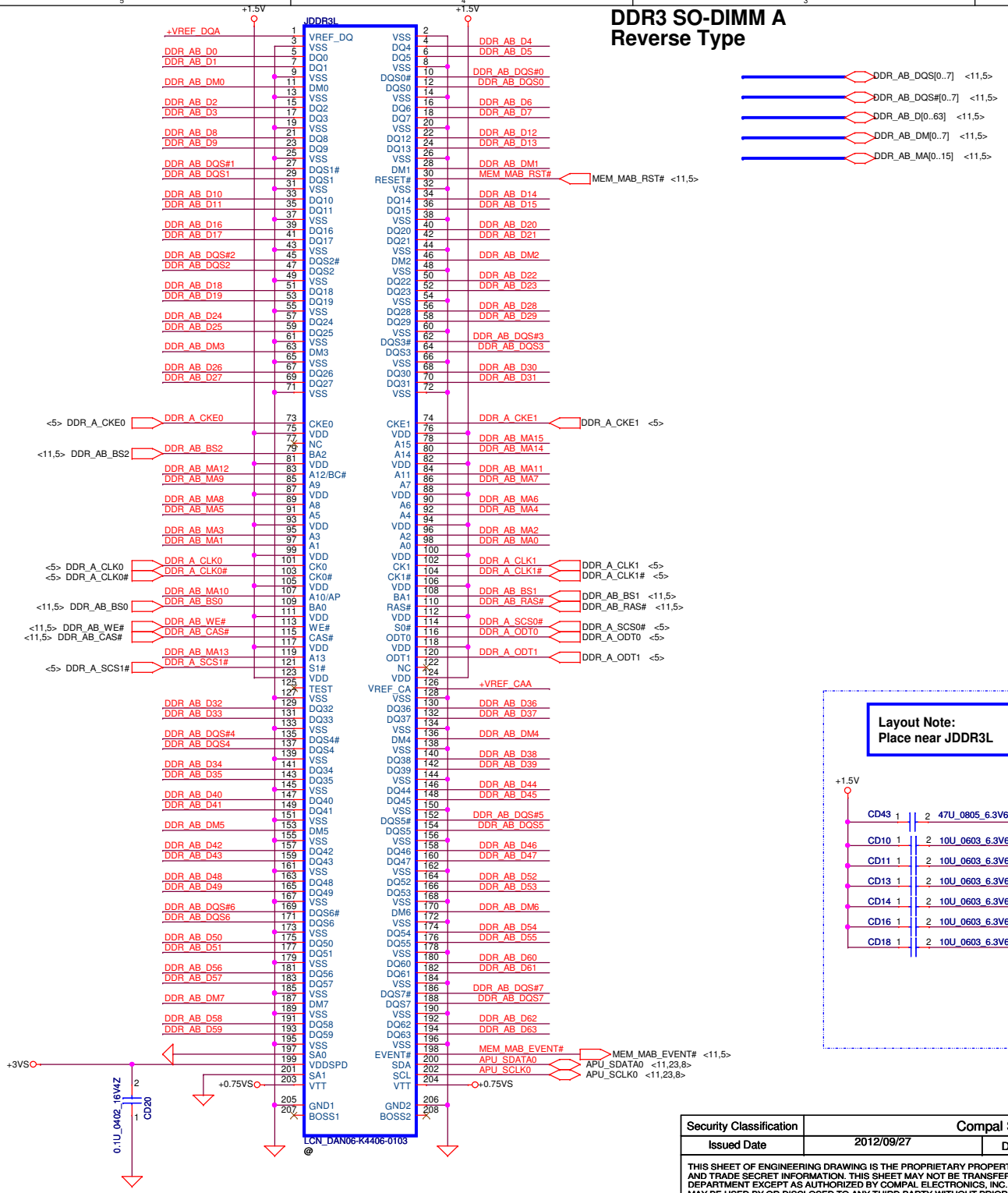
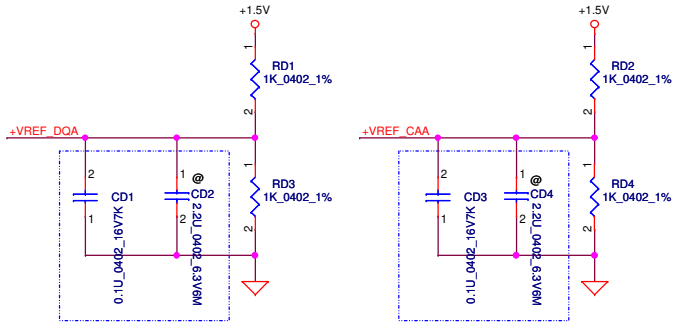
DDR3 SO-DIMM A
Reverse Type



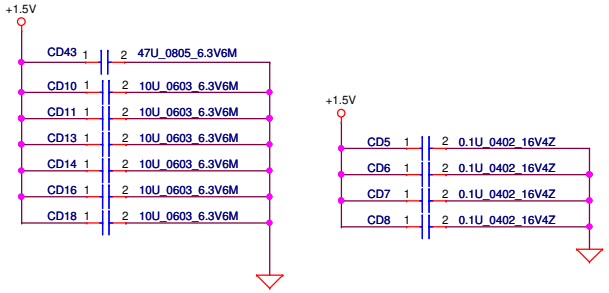
DDR_AB_DQS[0..7] <11,5>
DDR_AB_DQS#[0..7] <11,5>
DDR_AB_D[0..63] <11,5>
DDR_AB_DM[0..7] <11,5>
DDR_AB_MA[0..15] <11,5>

SO-DIMM VREF

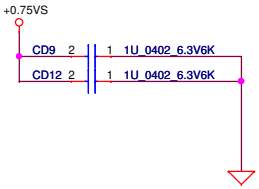


Layout Note:
Place near JDDR3L

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDDR3L.203 and 204



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Title: ***DDRIII-SODIMMA***

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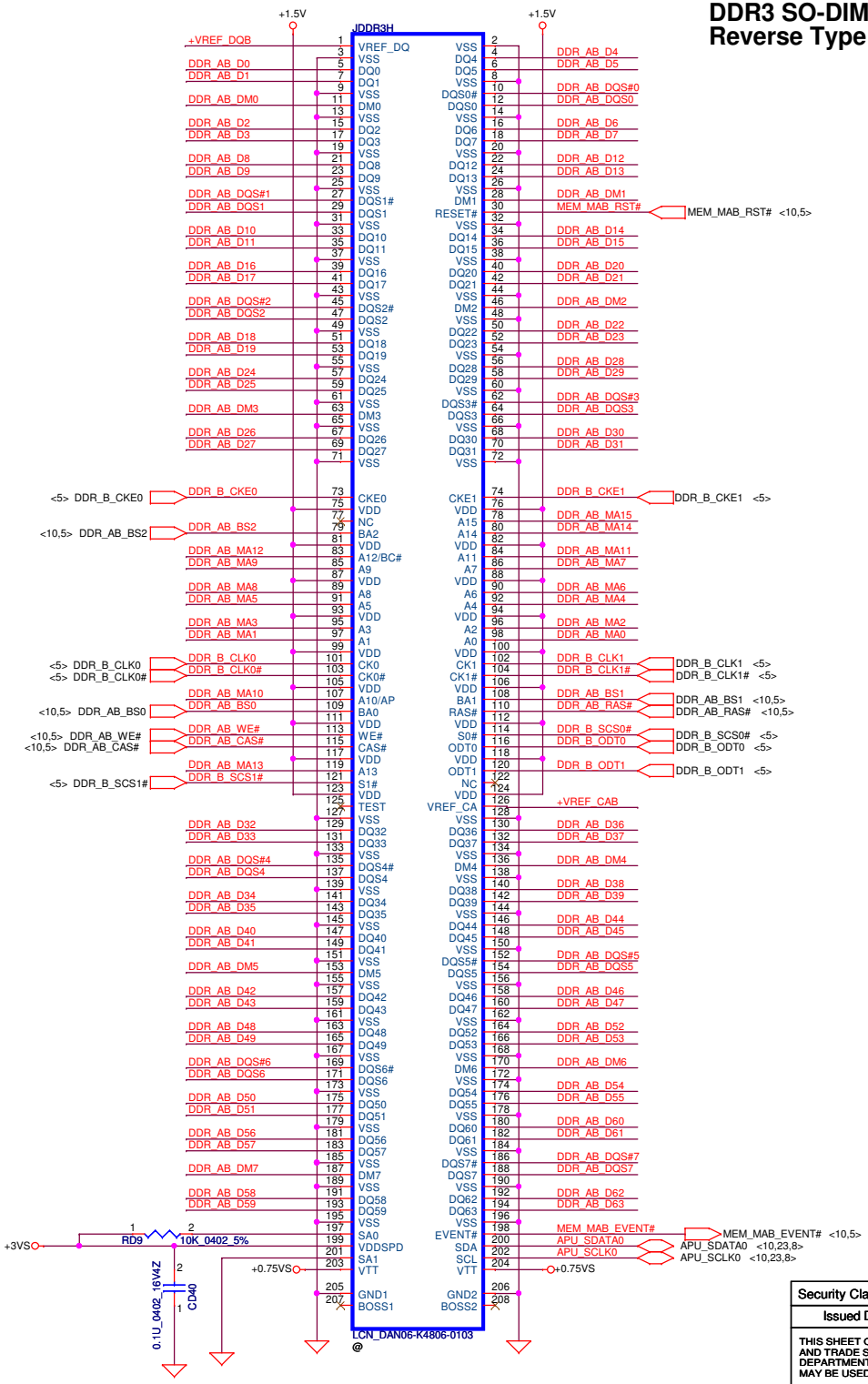
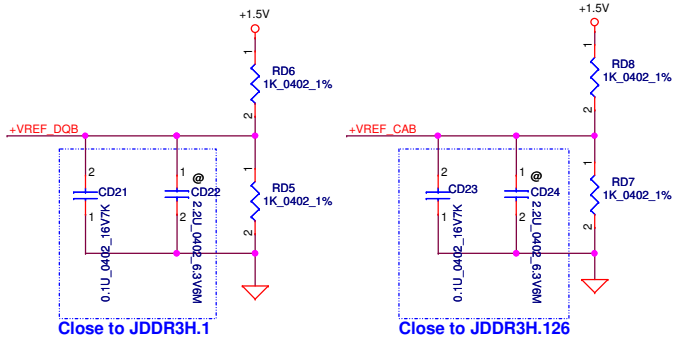
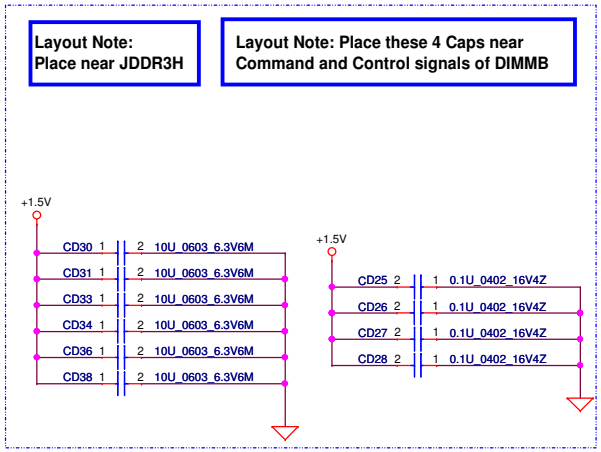
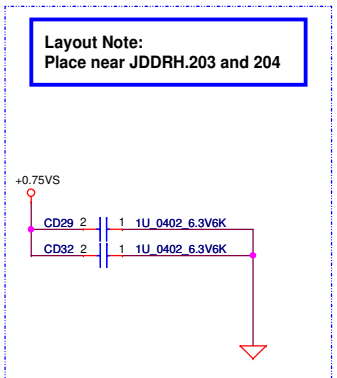
DDR3 SO-DIMM B
Reverse Type



SO-DIMM VREF







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Title: ***DDRIII-SODIMMB***

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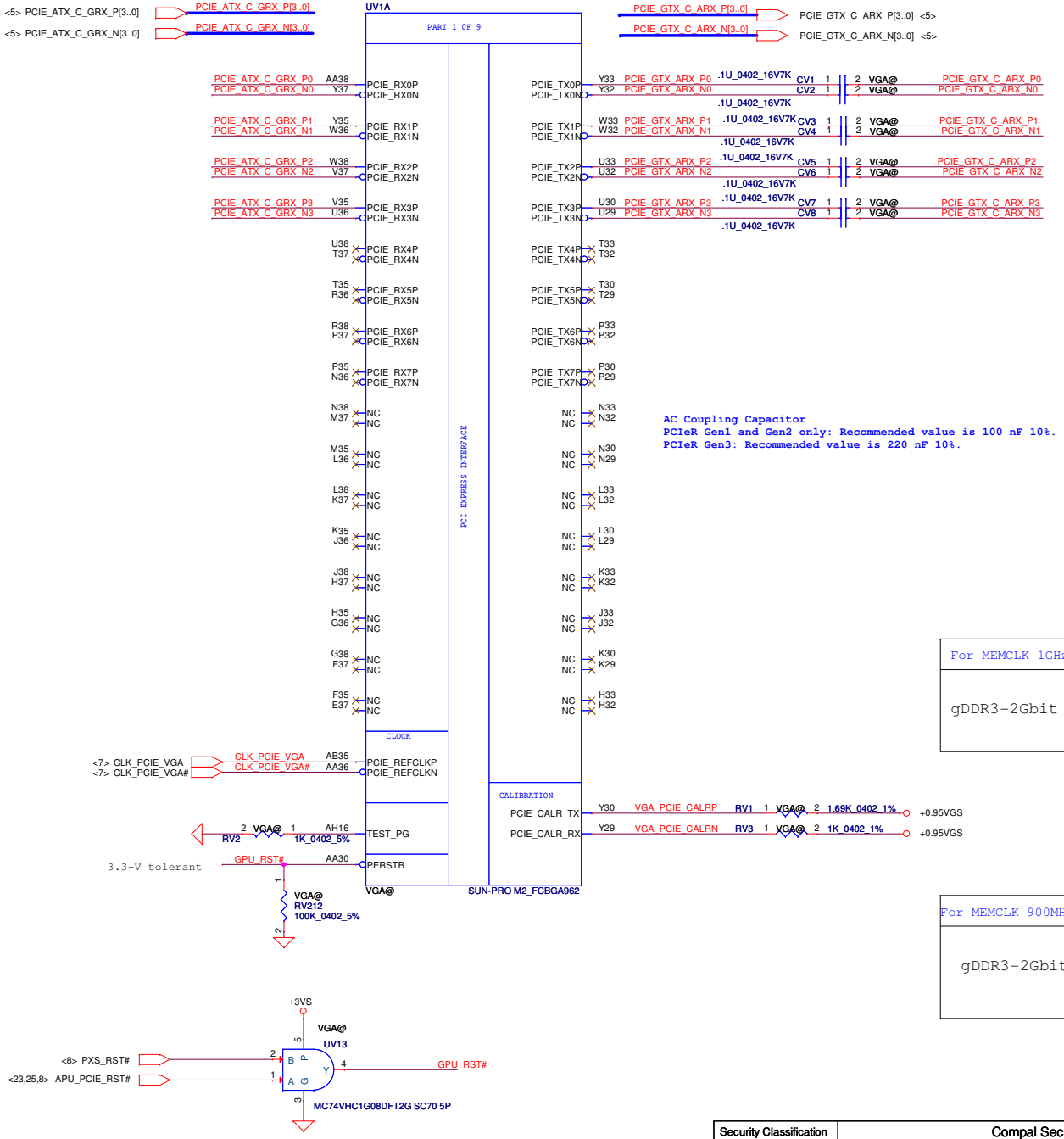
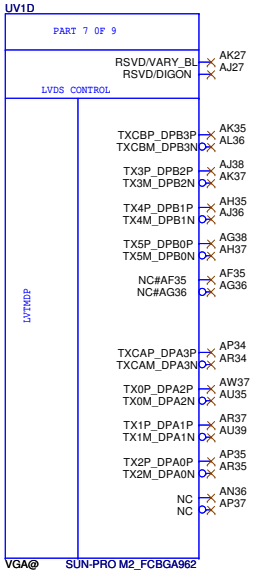


LVDS Interface



For MEMCLK 1GHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V/900MHz 1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

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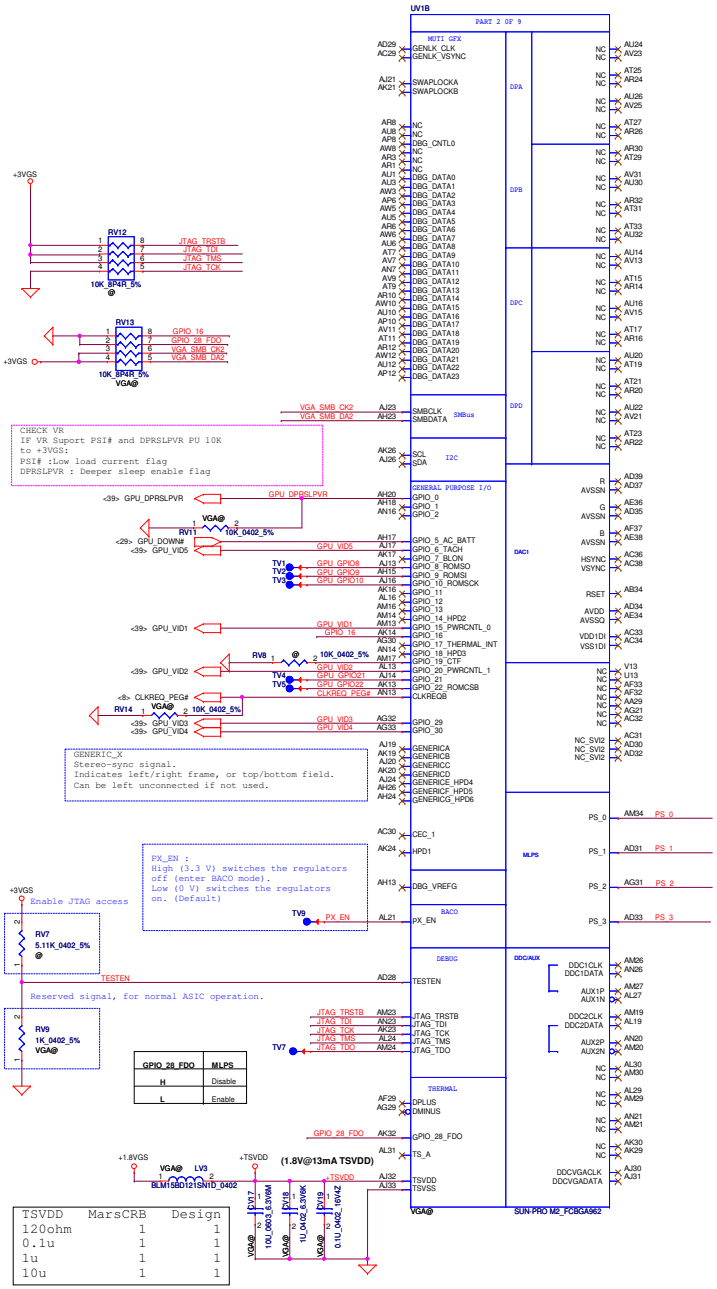


Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Suport PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point.
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109℃ by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

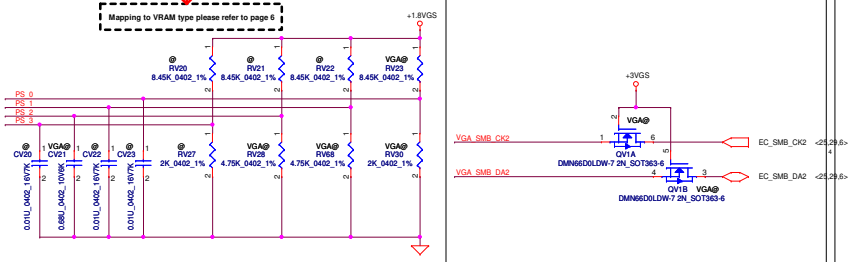
MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 6



Compal Electronics, Inc.

Title: Main_MSIC

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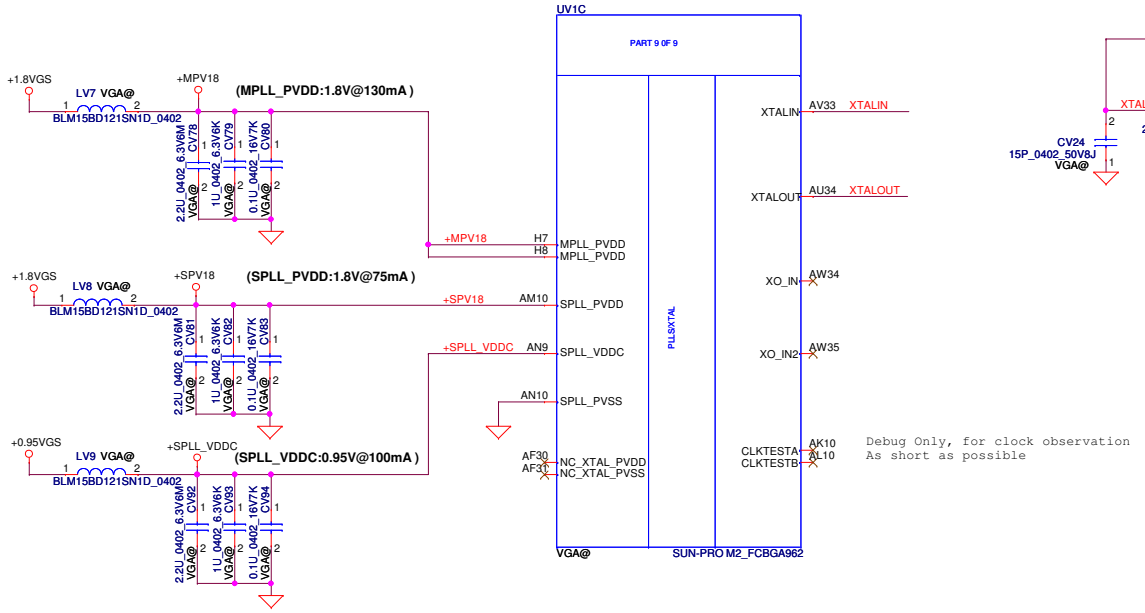
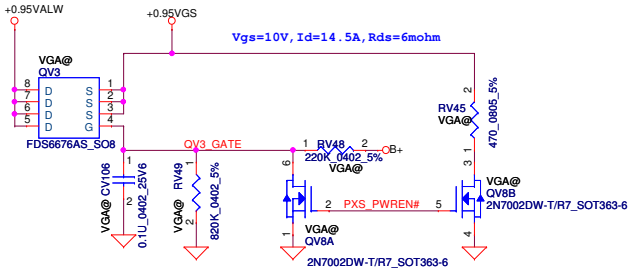
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

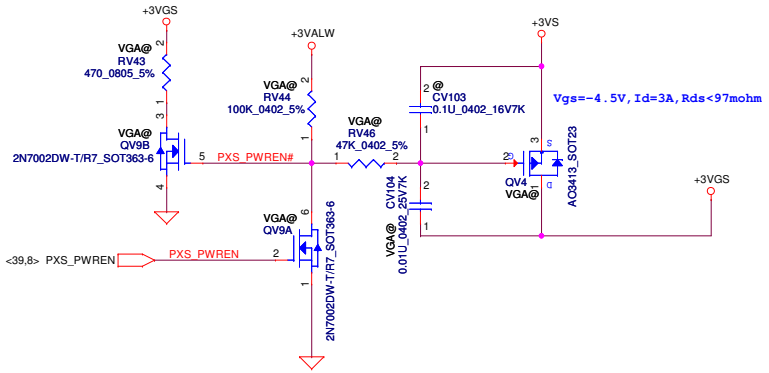
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1



+0.95VS to +0.95VGS



+3VS to +3VGS



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Title: BACO POWER

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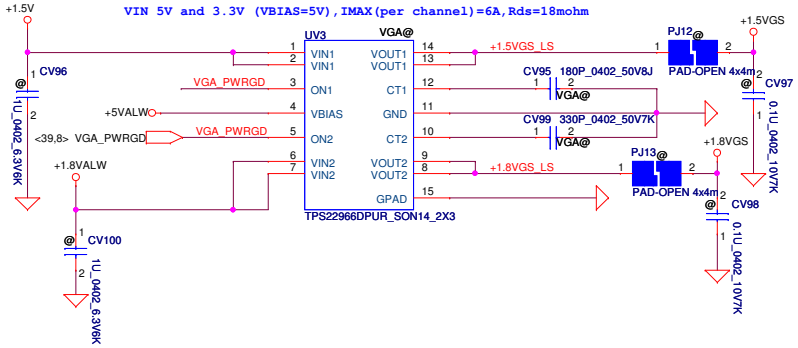
Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/27	Deciphered Date 2015/09/27	Title: BACO POWER

Size: Custom	Document Number: LA-9868P		Rev: 1.0
Date: Thursday, May 16, 2013	Sheet 15 of 42		

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	0
2.2u	5	5
10u	3	3

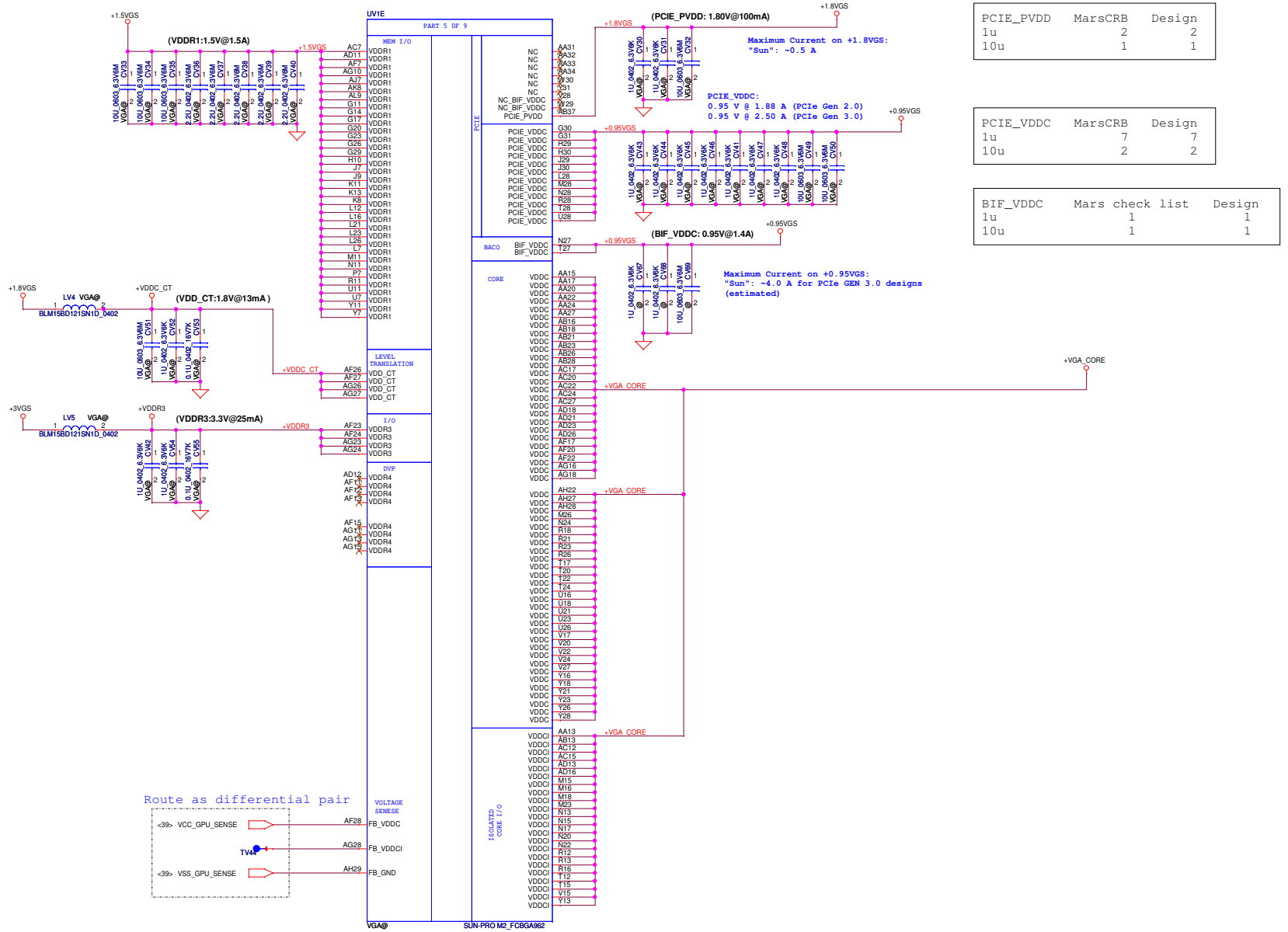
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDDR3	Mars check list	Design
120ohm	1	1
1u	3	2
10u	1	0
0.1u	0	1

PCIE_PVDD	MarsCRB	Design
1u	2	2
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	7
10u	2	2

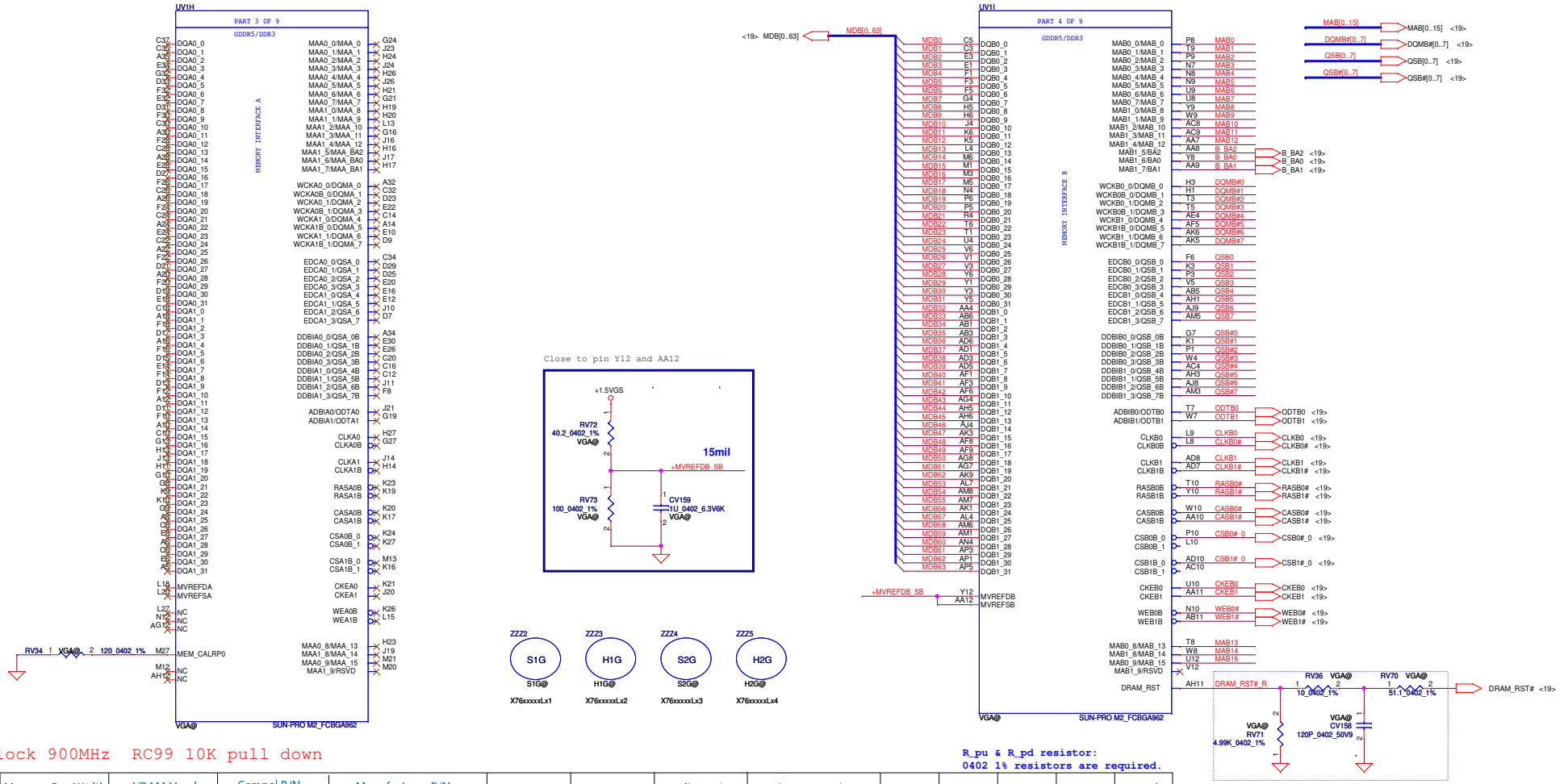
BIF_VDDC	Mars check list	Design
1u	1	1
10u	1	1



Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Title	Power		
Size C	Document Number LA-9868P		Rev 1.0
Date: Thursday, May 16, 2013	Sheet 16 of 42		



Memory clock 900MHz RC99 10K pull down

R_pu & R_pd resistor:
0402 1% resistors are required.

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA00003YO70	H5TQ2G63DFR-11C	X7648051L01	2Gbit	128M*16	1GB/4pcs	0	0	0	RV20 NC	RV27 4.75K
SUN PRO-M2	64bit	Micron	SA00005XB00	MT41K128M16JT-107G:K	X7648051L03	2Gbit	128M*16	1GB/4pcs	0	0	1	RV20 8.45K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA00005SH00	K4W2G1646E-BC11	X7648051L04	2Gbit	128M*16	1GB/4pcs	1	1	1	RV20 4.75K	RV27 NC

Memory clock 1GHz RC95 10K pull high

GPU Type	Memory Bus Width	VRAM Vendor	Compal P/N	Manufacturer P/N	X76 P/N	Size per part	Configuration	Total Memory Size/Qty	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
SUN PRO-M2	64bit	Hynix	SA000065300	H5TQ2G63DFR-N0C	X7648051L02	2Gbit	128M*16	1GB/4pcs	0	1	0	RV20 4.53K	RV27 2K
SUN PRO-M2	64bit	Samsung	SA000068U20	K4W2G1646E-BC1A	X7648051L05	2Gbit	128M*16	1GB/4pcs	1	1	0	RV20 3.4K	RV27 10K

Place all these components close to GPU (Within 25mm) and keep all component close to each other

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: MEM Interface

Size	Document Number	Rev
C	LA-9868P	1.0

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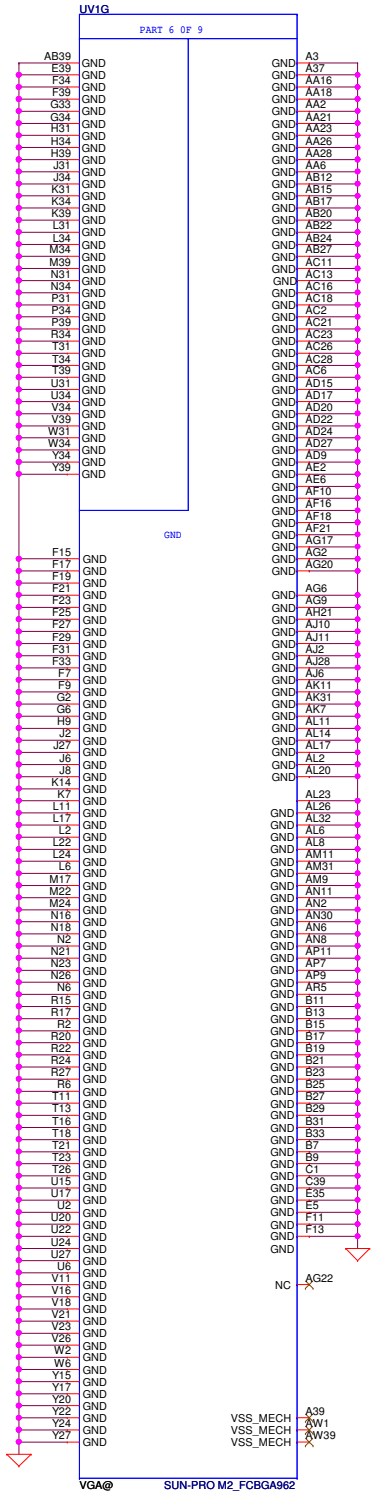

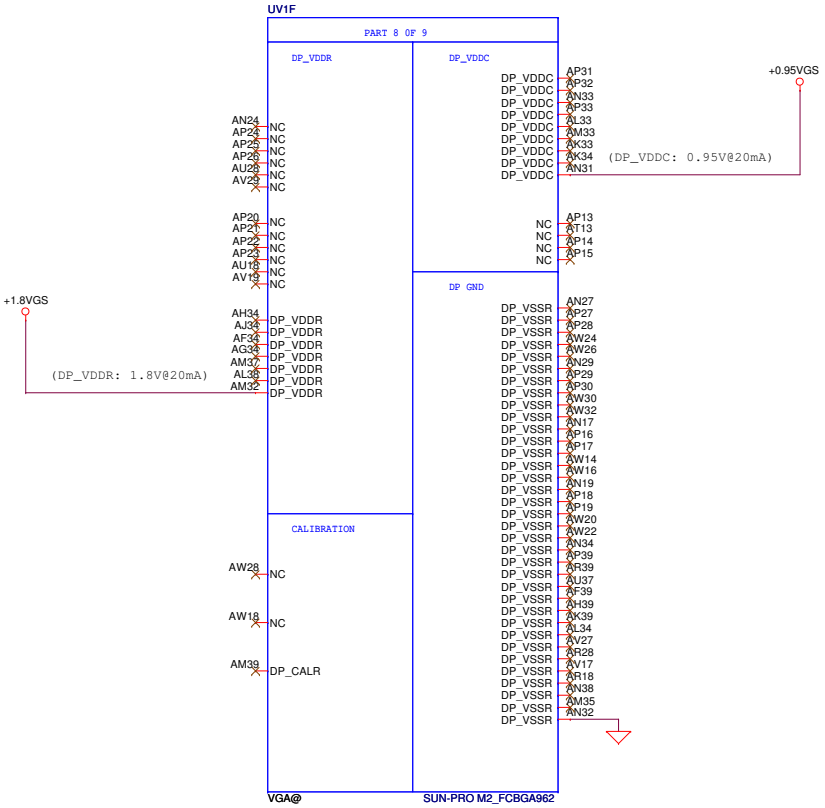

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Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: PWR_GND

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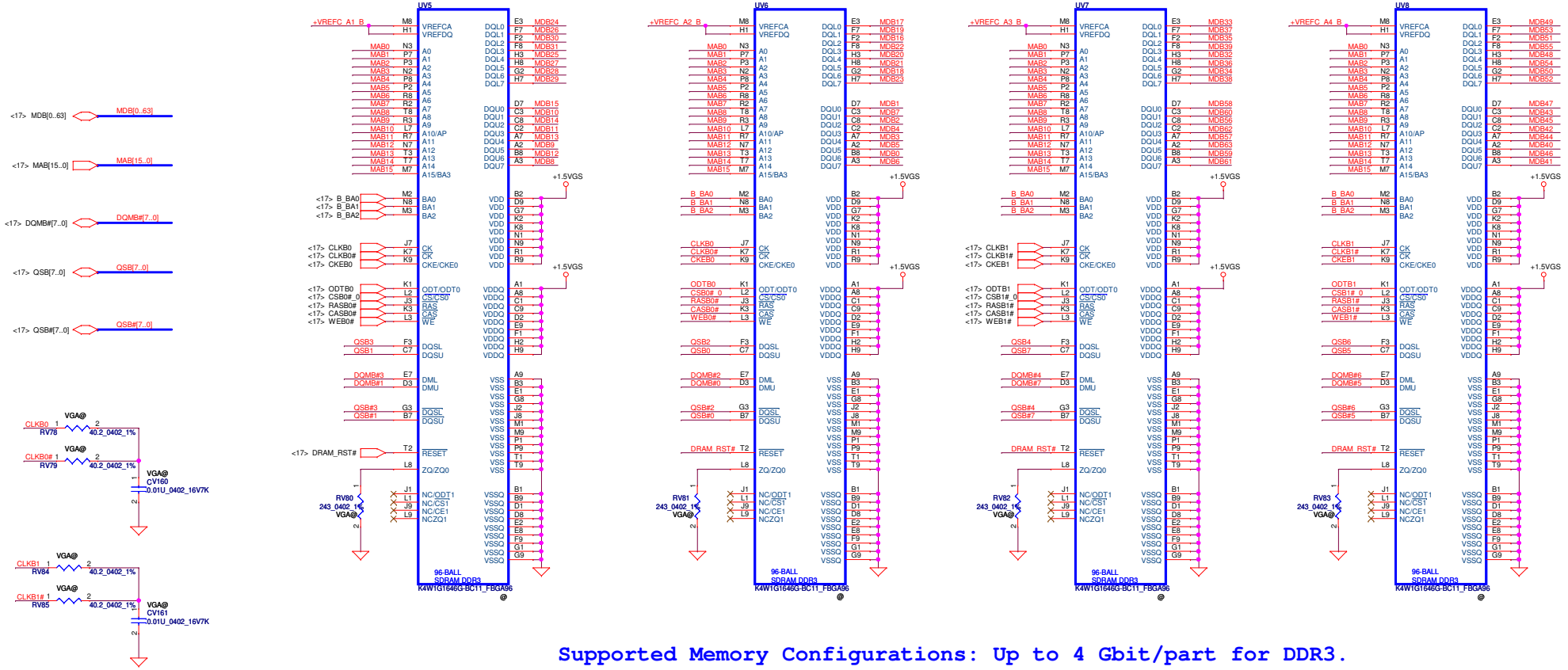
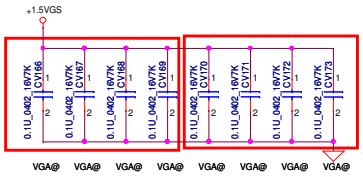
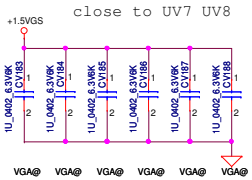
CHANNEL B: 512MB/1024MB DDR3



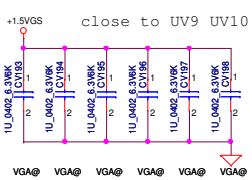
Supported Memory Configurations: Up to 4 Gbit/part for DDR3.



close to UV9 UV10



close to UV7 UV8



close to UV9 UV10

close to UV7 UV8

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: VRAM Channel B

Size	Document Number	Rev
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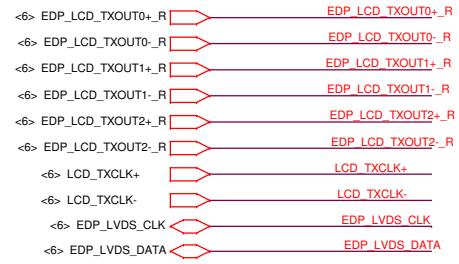
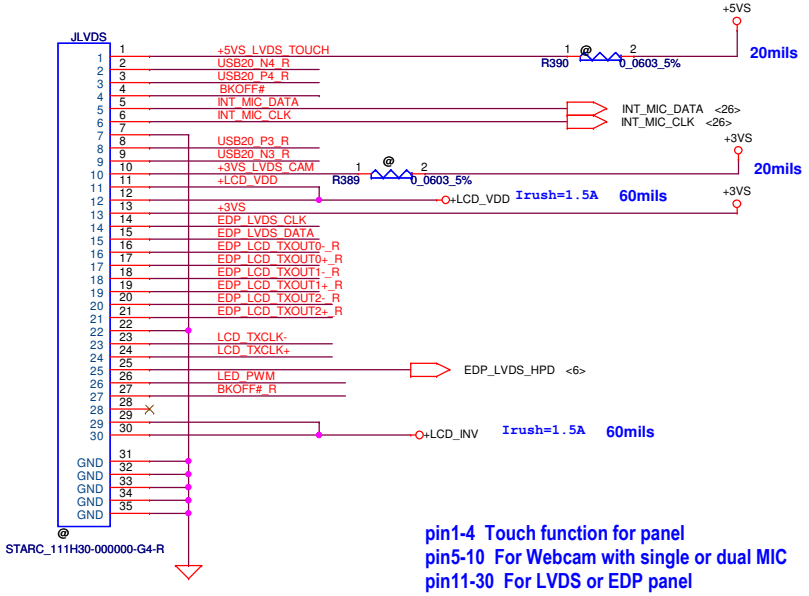
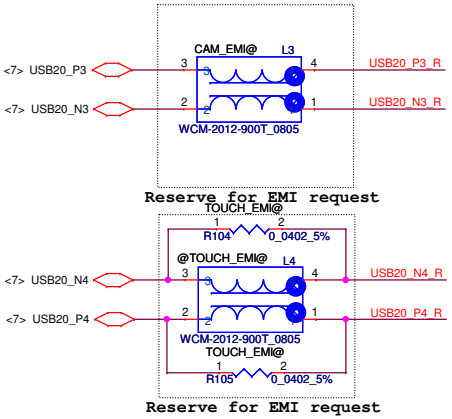


If it's EPD, they're become
LCD_TXOUT2+_R = EDP_TX0+
LCD_TXOUT2-_R = EDP_TX0-
LCD_TXOUT1+_R = EDP_TX1+
LCD_TXOUT1-_R = EDP_TX1-
LVDS_CLK = EDP_AUXP
LVDS_DATA = EDP_AUXN



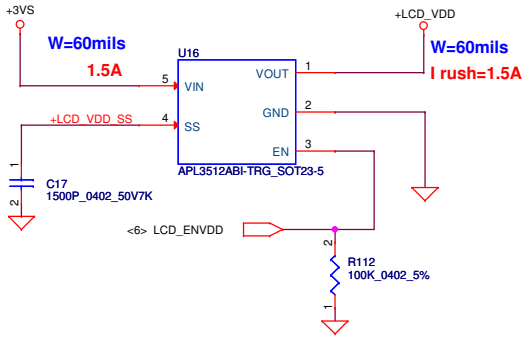
pin1-4 Touch function for panel
pin5-10 For Webcam with single or dual MIC
pin11-30 For LVDS or EDP panel

Carmera & Touch Screen

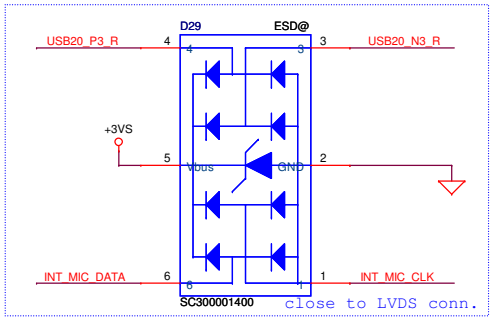


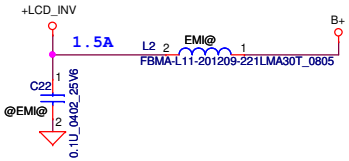
LCD_VDD

Need check eDP&LVDS both 3V power rail.

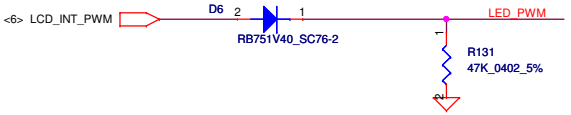


LCD_INV

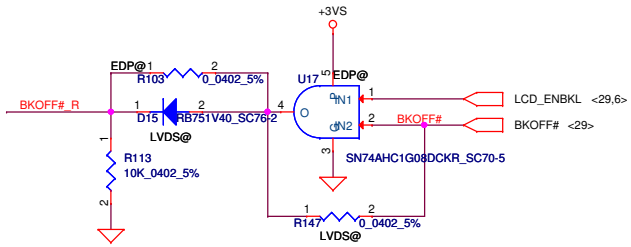




LCD Control



Reserve for eDP panel potential issue



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.	
Title	LVDS/EDP W/ CAMERA
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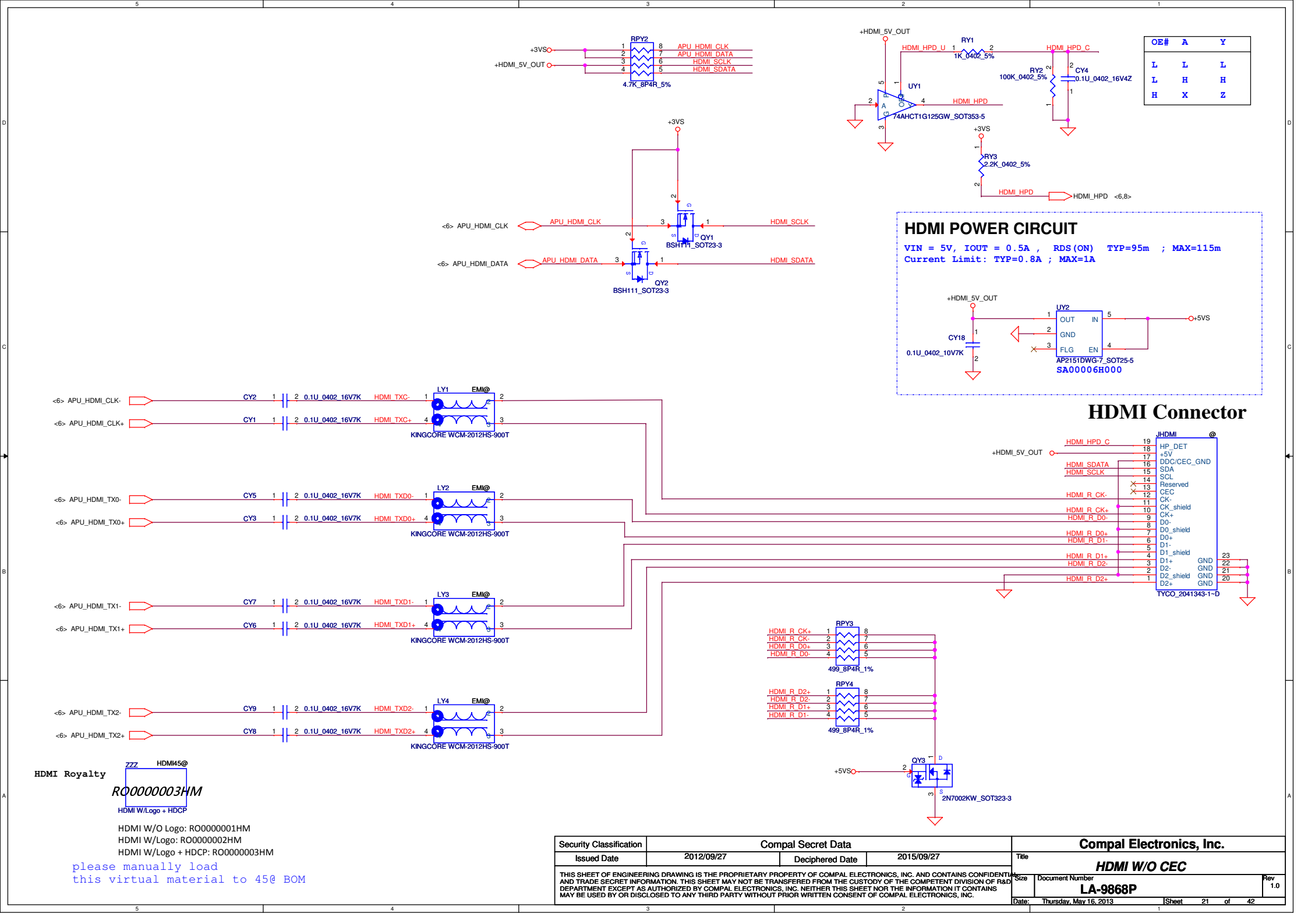
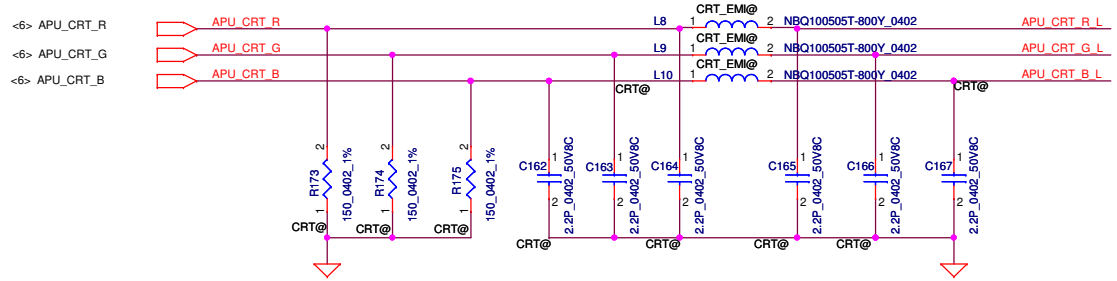
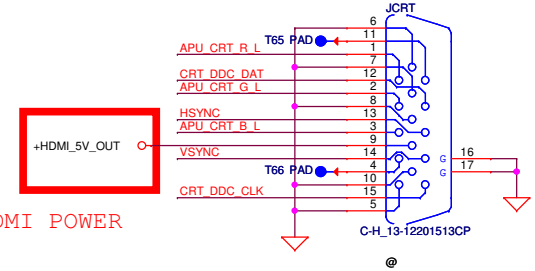


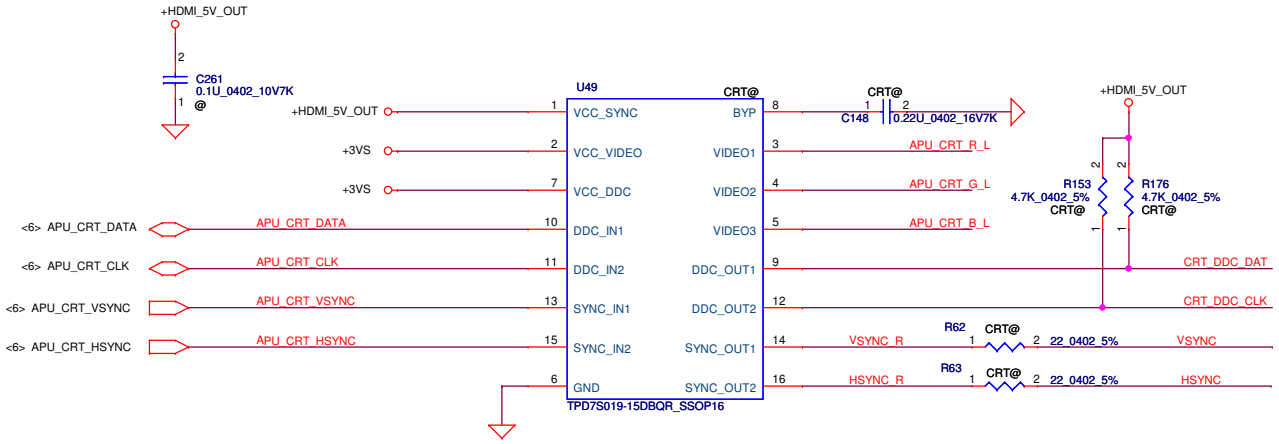
Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.		
Title: HDMI W/O CEC		
Size	Document Number: LA-9868P	Rev: 1.0
Date: Thursday, May 16, 2013	Sheet 21 of 42	





USE HDMI POWER



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: ***CRT***

Size	Document Number	Rev
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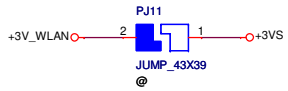
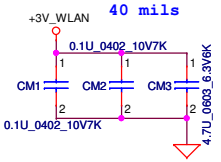
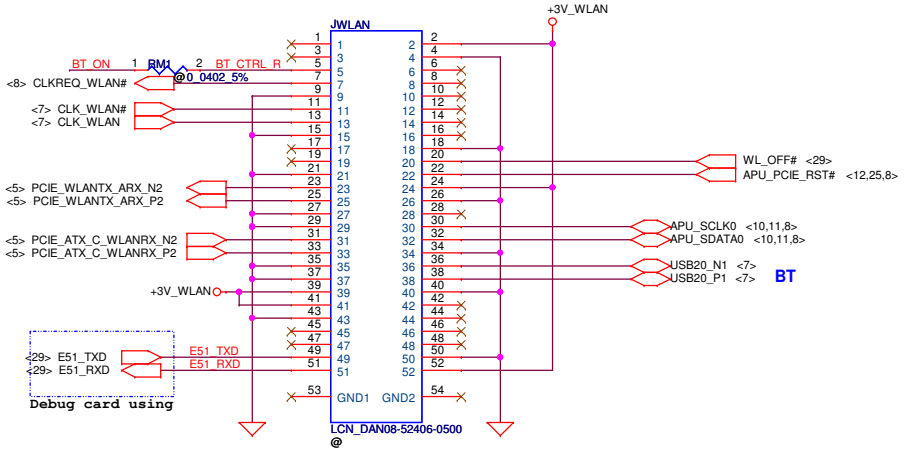
Slot 1 Half PCIe Mini Card-WLAN

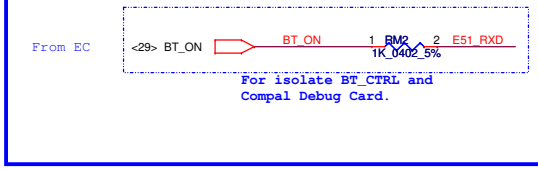




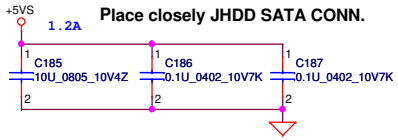


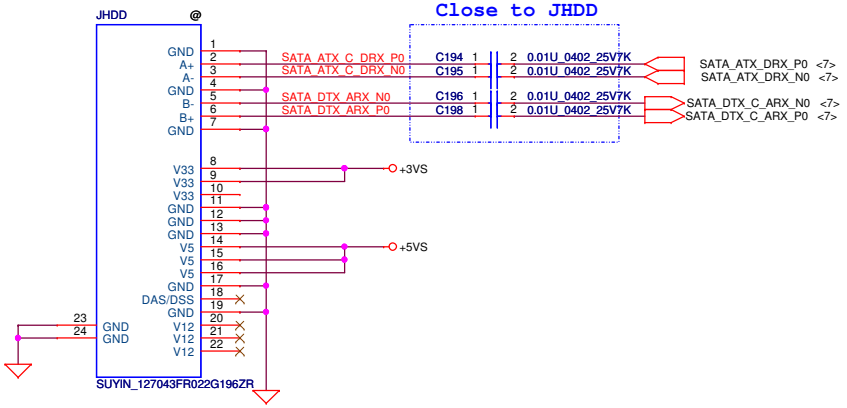
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

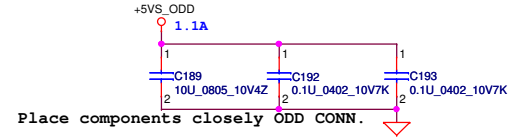


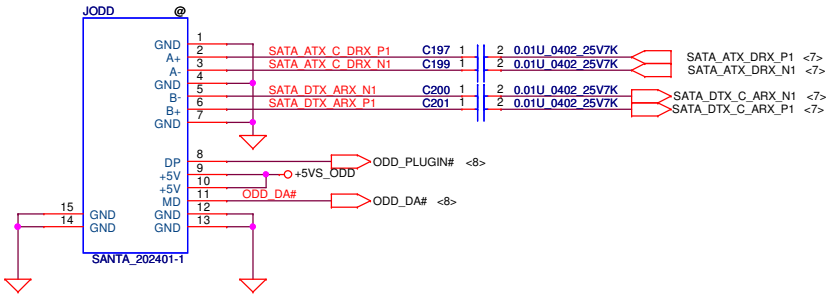
SATA HDD Conn.





SATA ODD Conn





Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: ***WLAN/SATA HDD&ODD***

Size | Document Number: **LA-9868P** | Rev: 1.0

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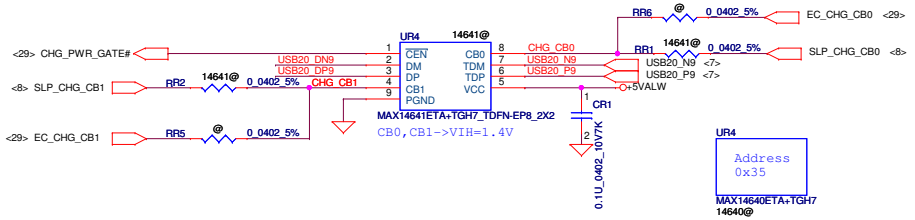
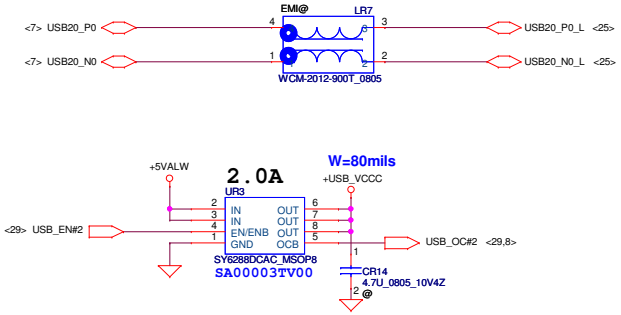
USB Sleep & Charge

Right side USB 3.0 x 2/ Sleep&Charge

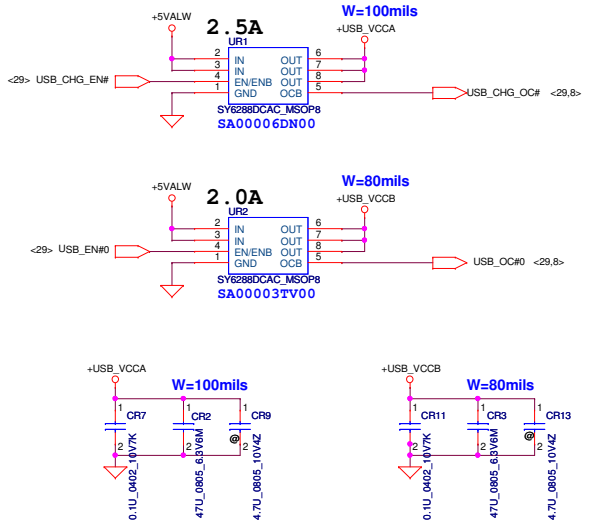
State table for MAX14641			
CB0	**CB1**	**Mode**	**STATUS**
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

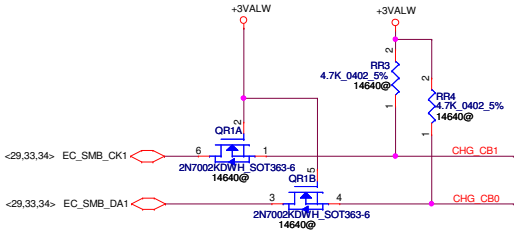


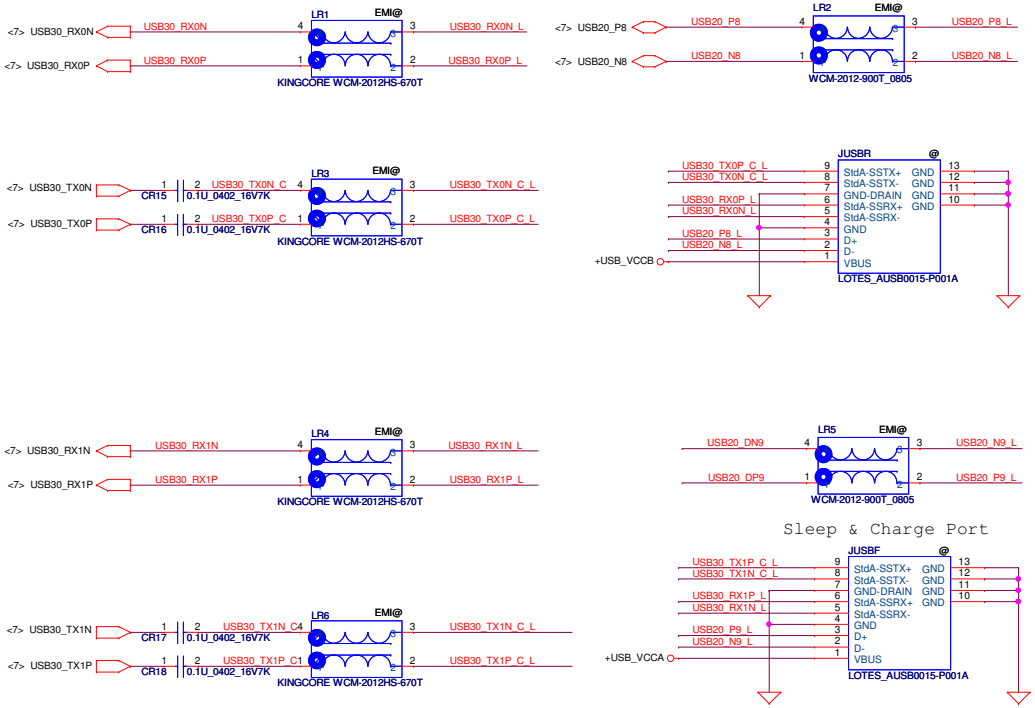
Left Side USB Port

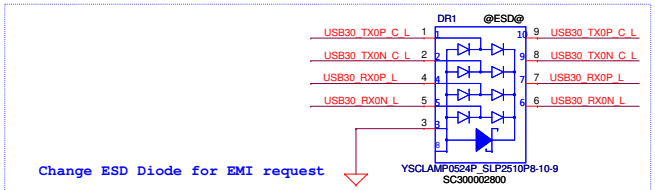


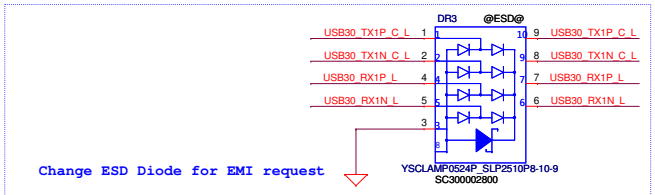
USB POWER SWITH











Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.			
Title	***LUSB/RUSB/S&C***		
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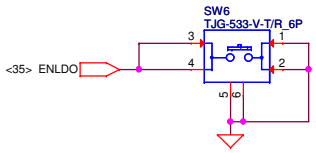
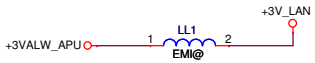
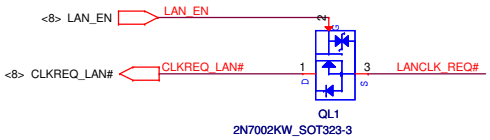
Battery Reset

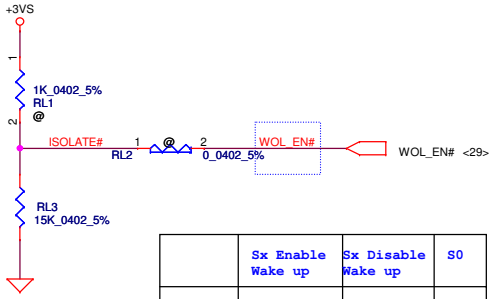


LAN Conn

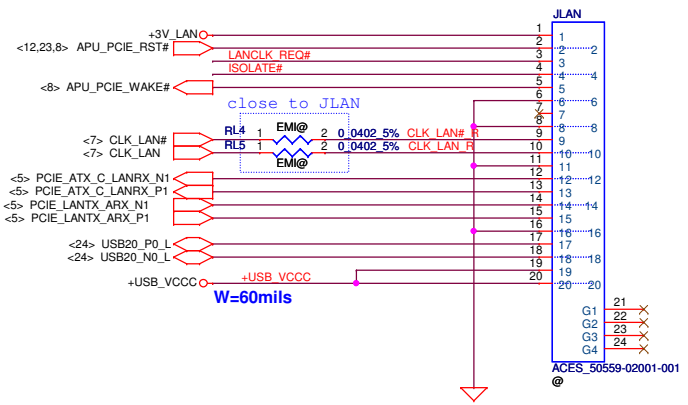


For LAN function

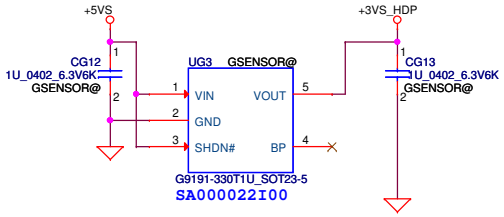


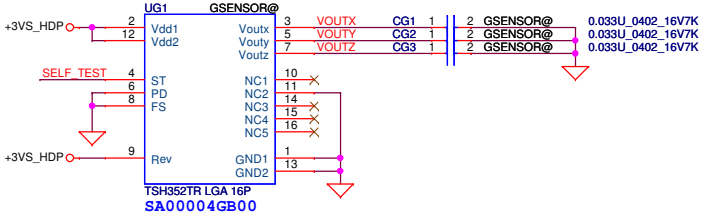


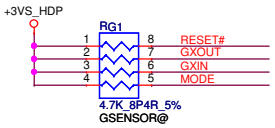
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

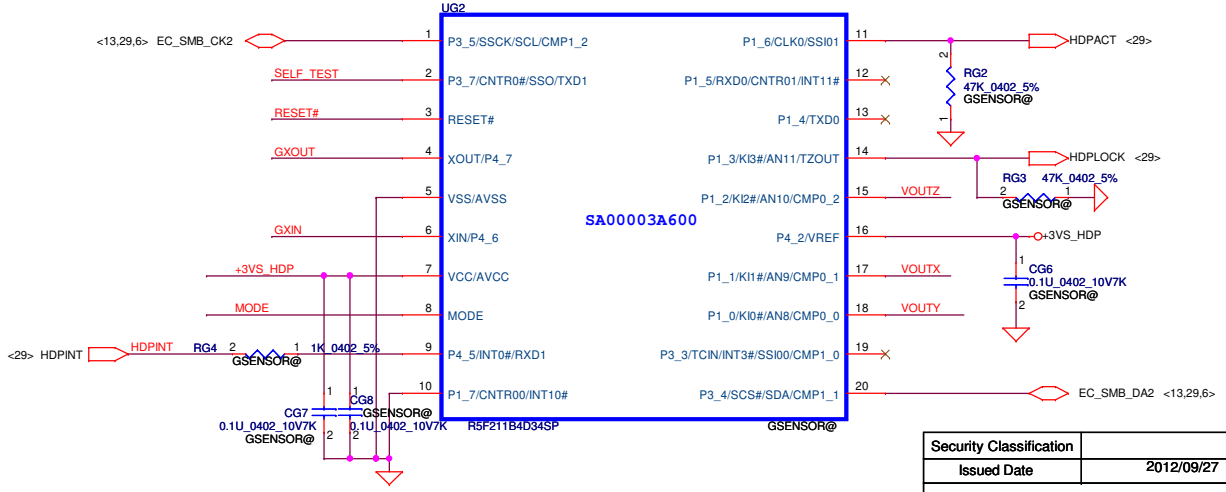


G-SENSOR



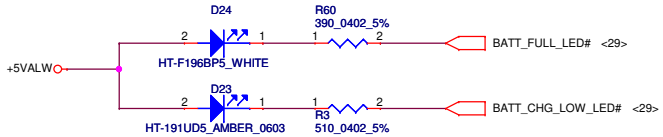






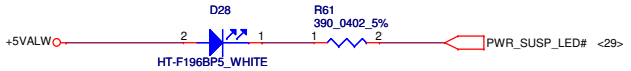
LED

BATT CHARGE /FULL LED



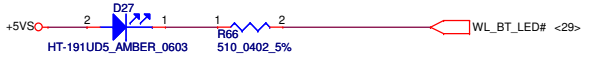
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED (AMD NO WIMAX)



Amber LED bright while Wireless and/or WiMAX turns on.

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.	
Title	LAN/G-SENSOR/LED/B_RES
Size	Document Number: LA-9868P
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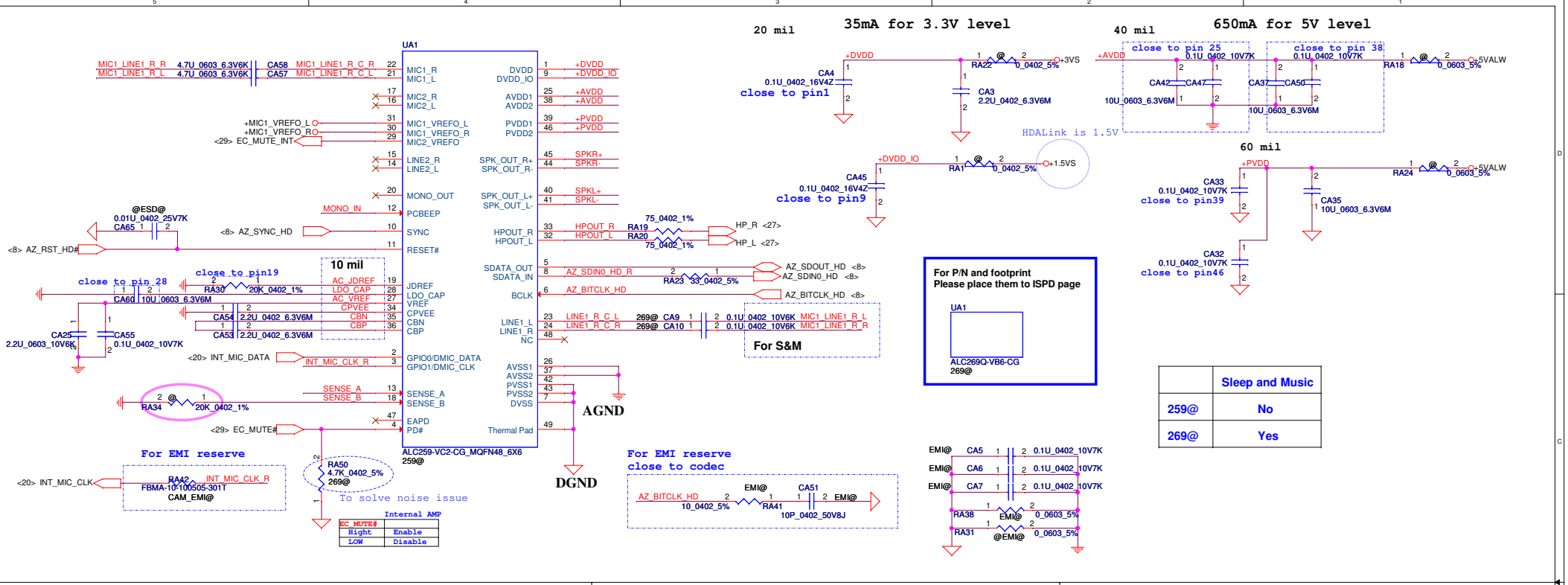
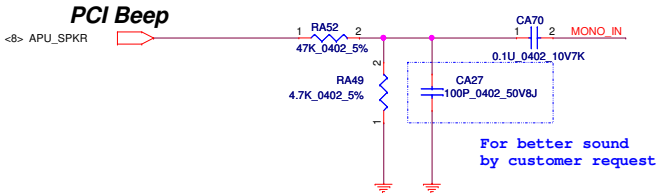
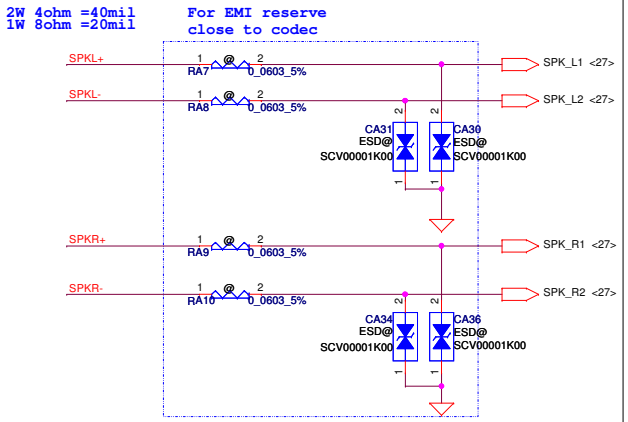


Beep sound

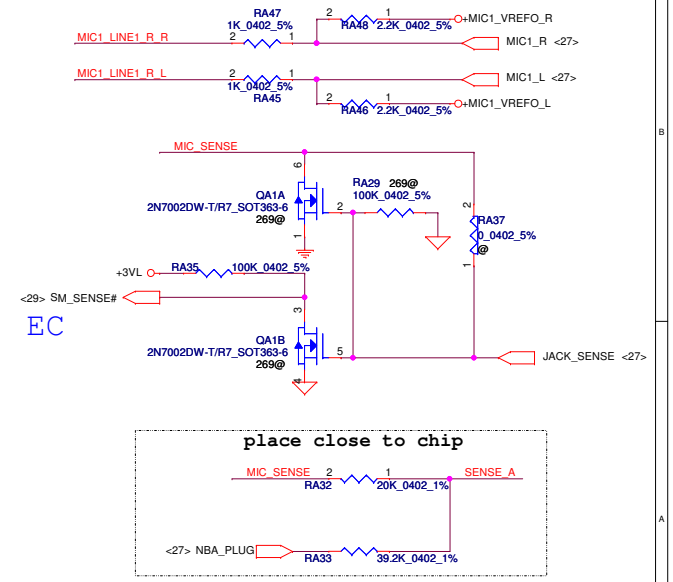


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

SPK



MIC/LINE IN



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: Cover Sheet

Size	Document Number	Rev
Custom		1.0

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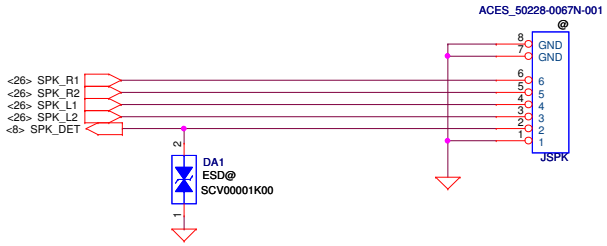
SPK Conn.

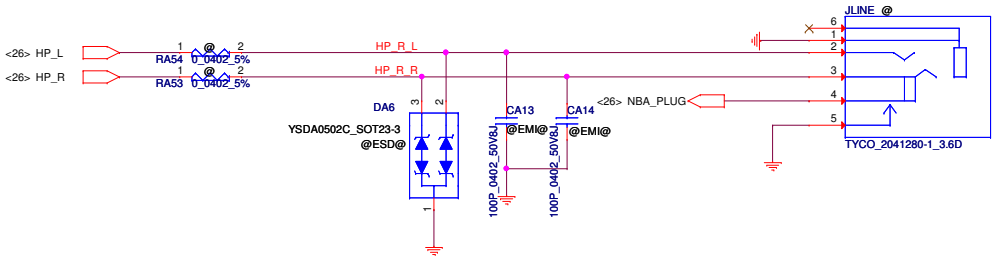
For common design,
pull-high resistor should be placed at connector side.



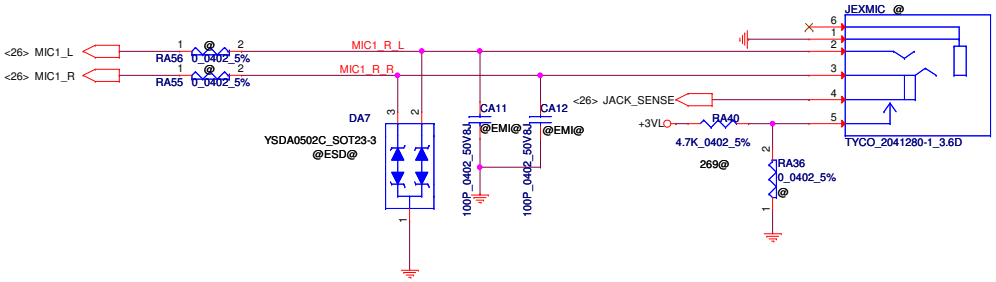
SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK



MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: Conn

Size: Custom | Document Number | Rev: 1.0

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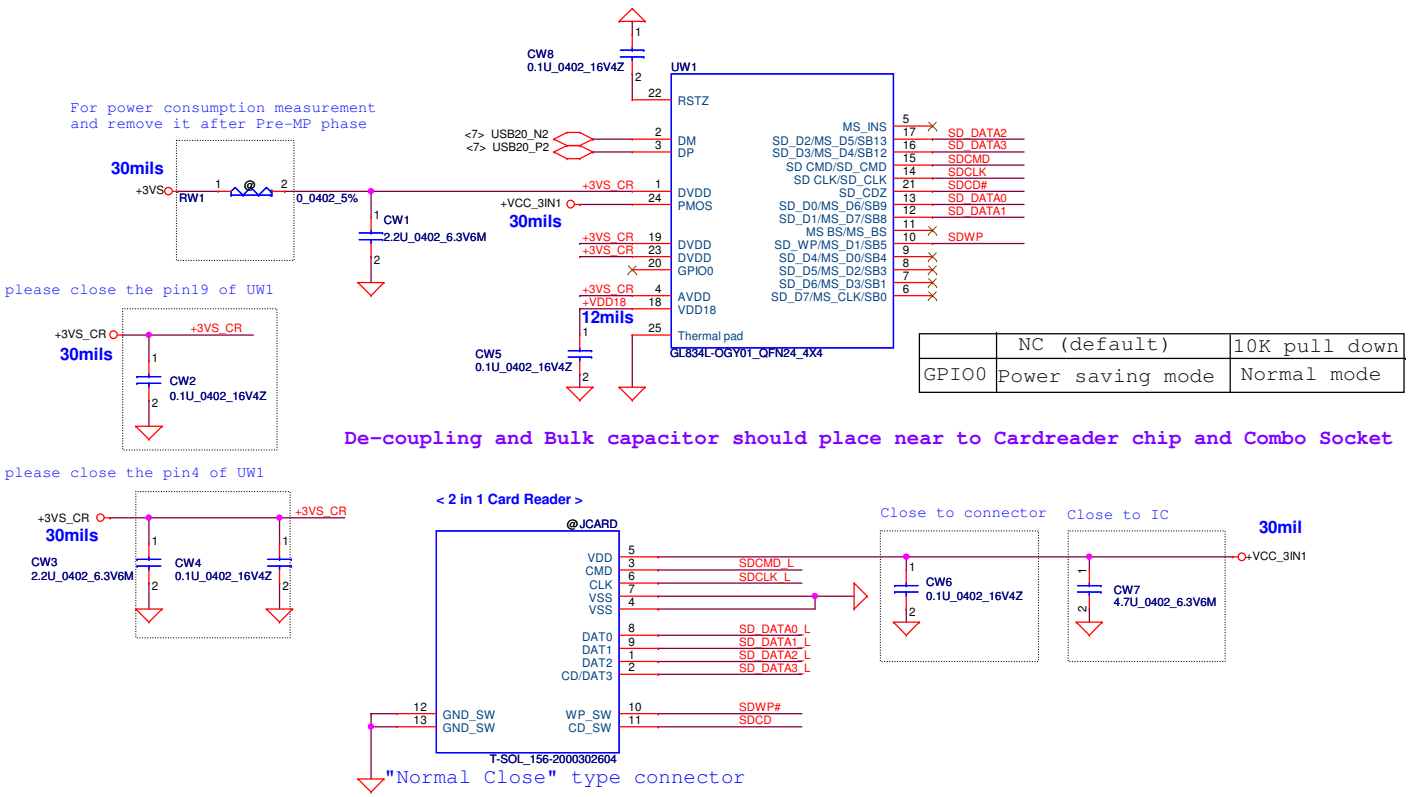
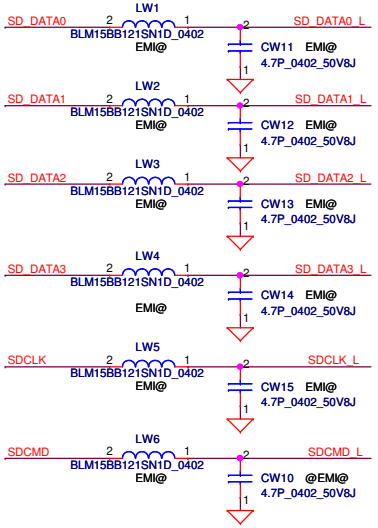


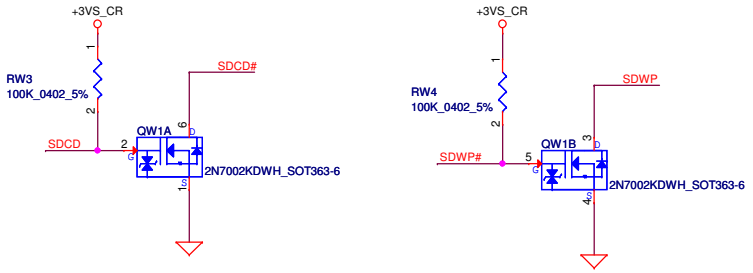
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/27	Deciphered Date	2015/09/27
Title	CardReader GL834L		
Size	Document Number LA-9868P		Rev 1.0
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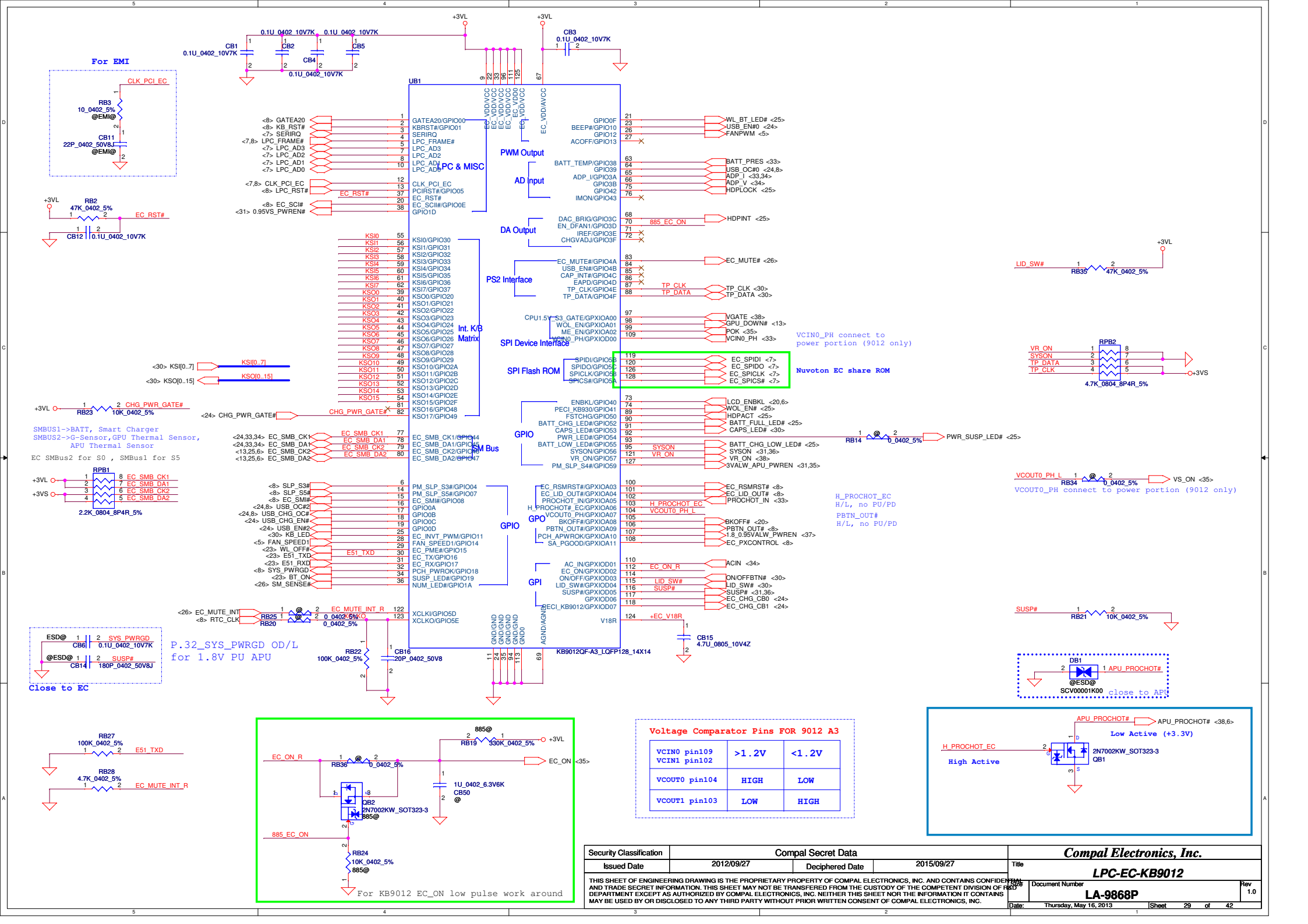

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.			
Title	LPC-EC-KB9012		
Size	Document Number	LA-9868P	Rev 1.0
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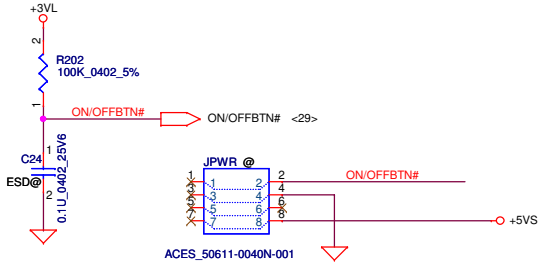
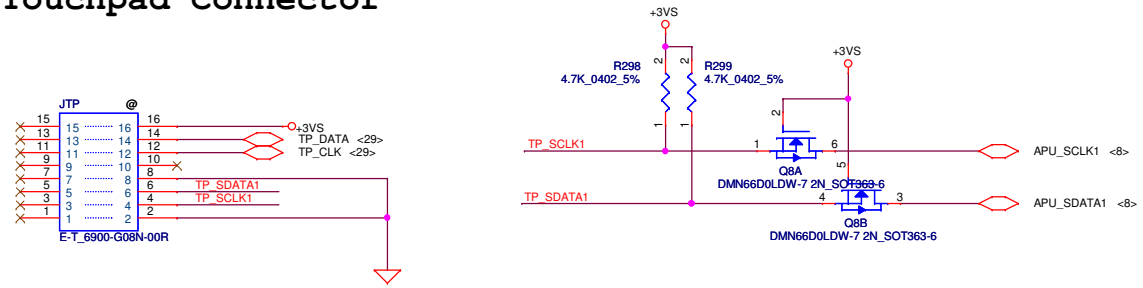
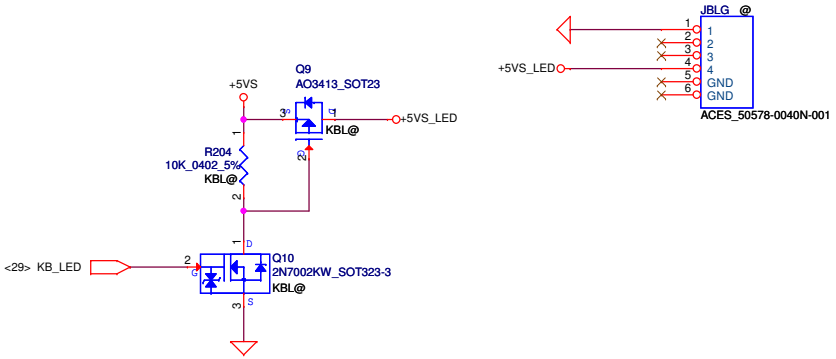
Power Button



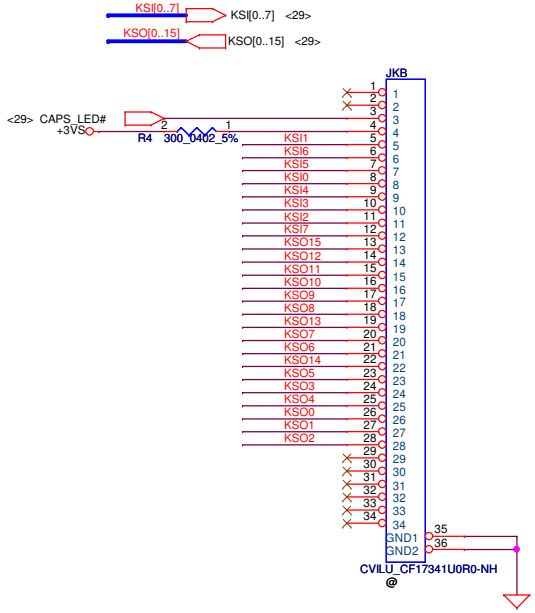
Touchpad Connector



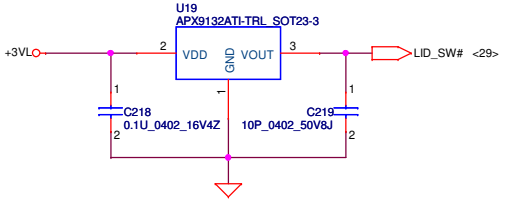
Keyboard LED



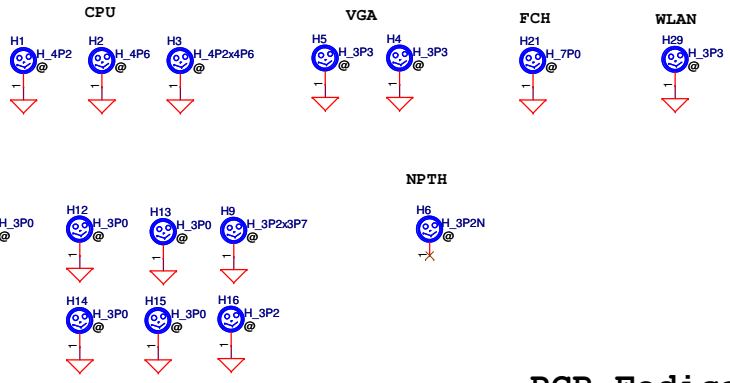
NEW KEYBOARD CONN.



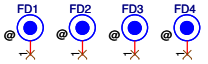
Lid SW



Screw Hole



PCB Fedical Mark PAD



ISPD

ZZZ1
DAZ0WJ00100
PCB LA-9868P

UC1 @
SA00006KR40
A4-5000 15W 4C

UC1 X4@ SA00006R430 CPU A4-5000 15W 4C

UC1 X4NPI@ SA00006R400 CPU A4-5000 15W 4C

UC1 X4R1@ SA00006R410 CPU A4-5000 15W 4C

UC1 X5@ SA00006R330 CPU A6-5200 25W 4C

UC1 X5NPI@ SA00006R300 CPU A6-5200 25W 4C

UC1 X5R1@ SA00006R310 CPU A6-5200 25W 4C

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.	
Title	KB/TP/LED/LID/DEBUG/ISPD
Size	Document Number: LA-9868P
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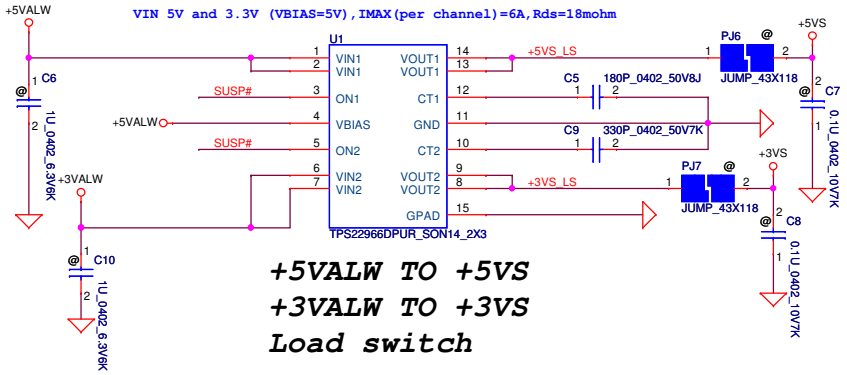
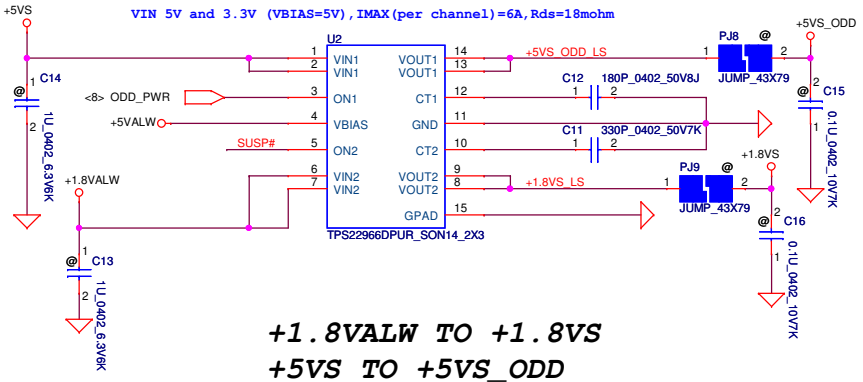
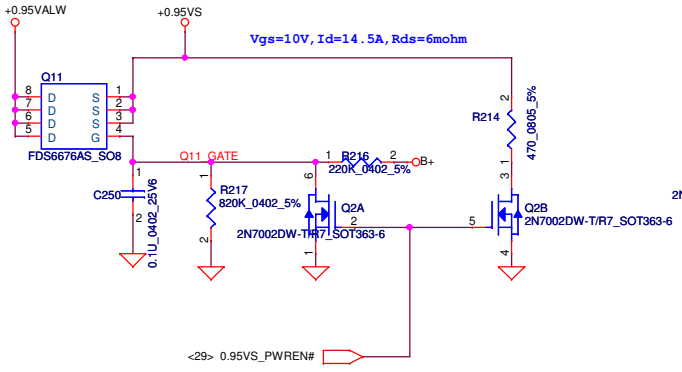


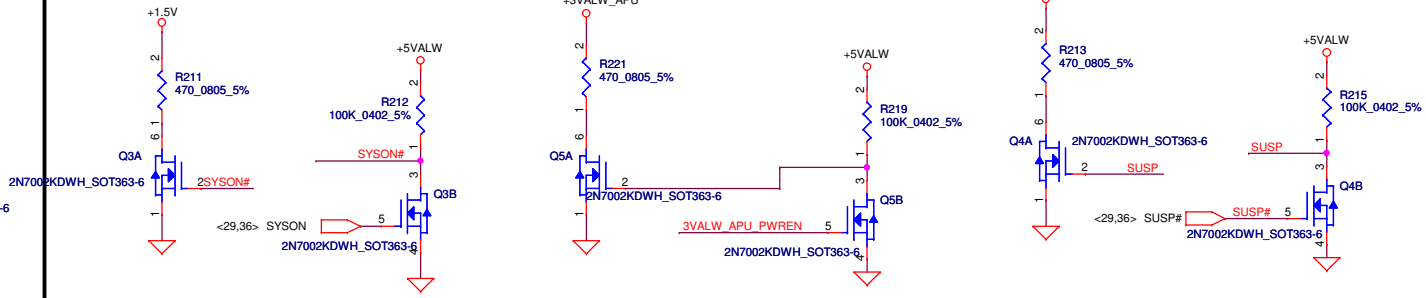
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



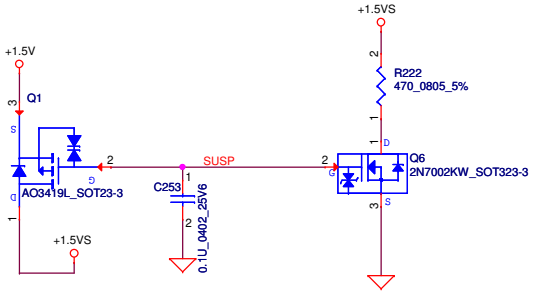
+1.8VALW TO +1.8VS
+5VS TO +5VS_ODD
Load switch

+0.95VALW to +0.95VS

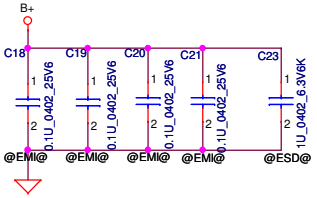




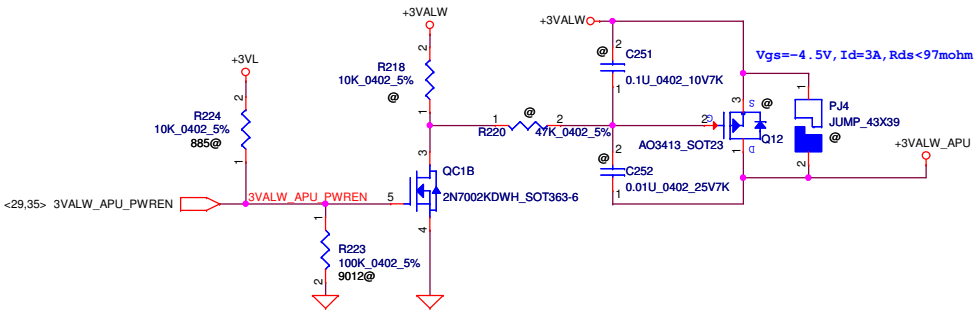
+1.5V to +1.5VS



EMI Cap.
Please check location



+3VALW to +3VALW_FCH



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: ***DC TO DC INTERFACE***

Size	Document Number	Rev
	LA-9868P	1.0

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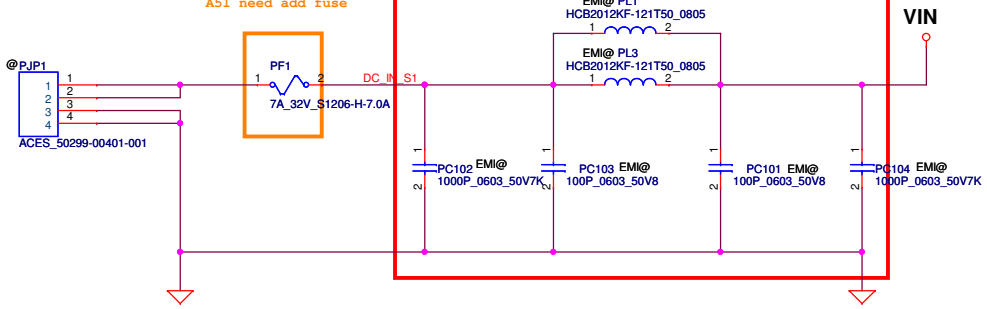
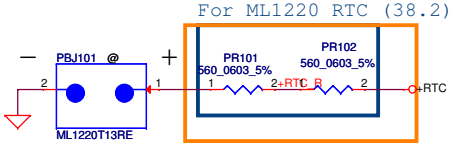
EMI Part (47.1)

Other component (37.1)

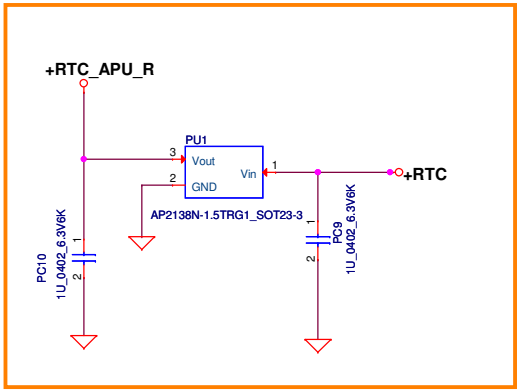
A51 need add fuse



For ML1220 RTC (38.2)



For RTC (38.2)



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: *DCIN/PRECHARGE*

Size	Document Number	Rev
Custom	*LA-9868P*	1.0

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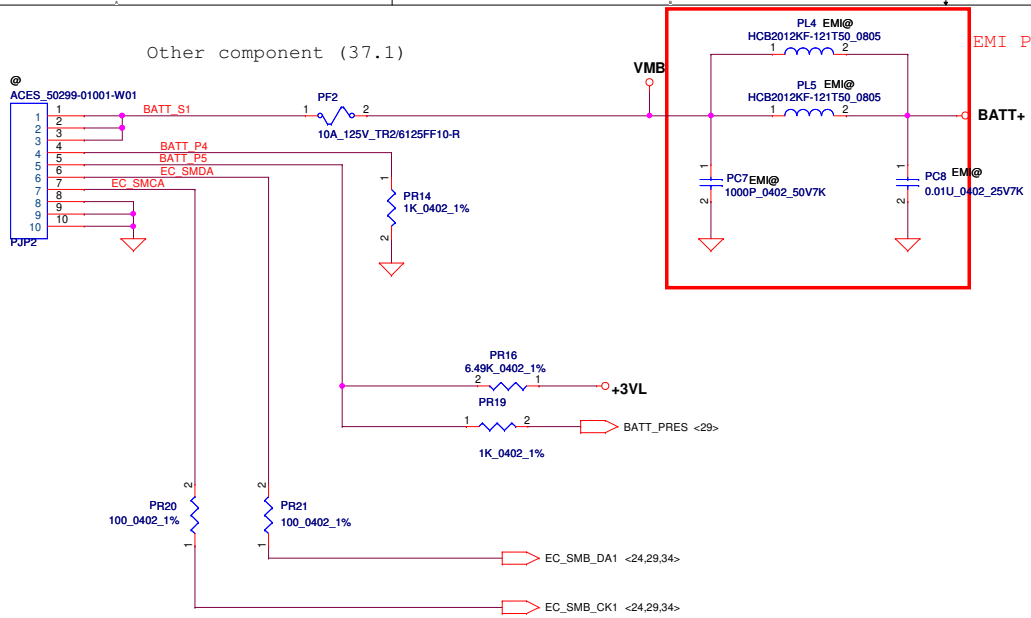
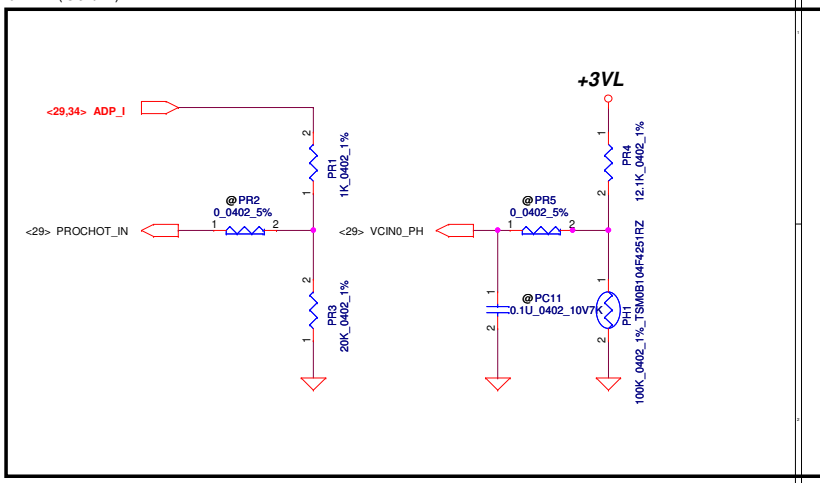
Other component (37.1)

EMI Part (47.1)



OTP (39.7)



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size: Custom | Document Number: *LA-9868P* | Rev: 1.0

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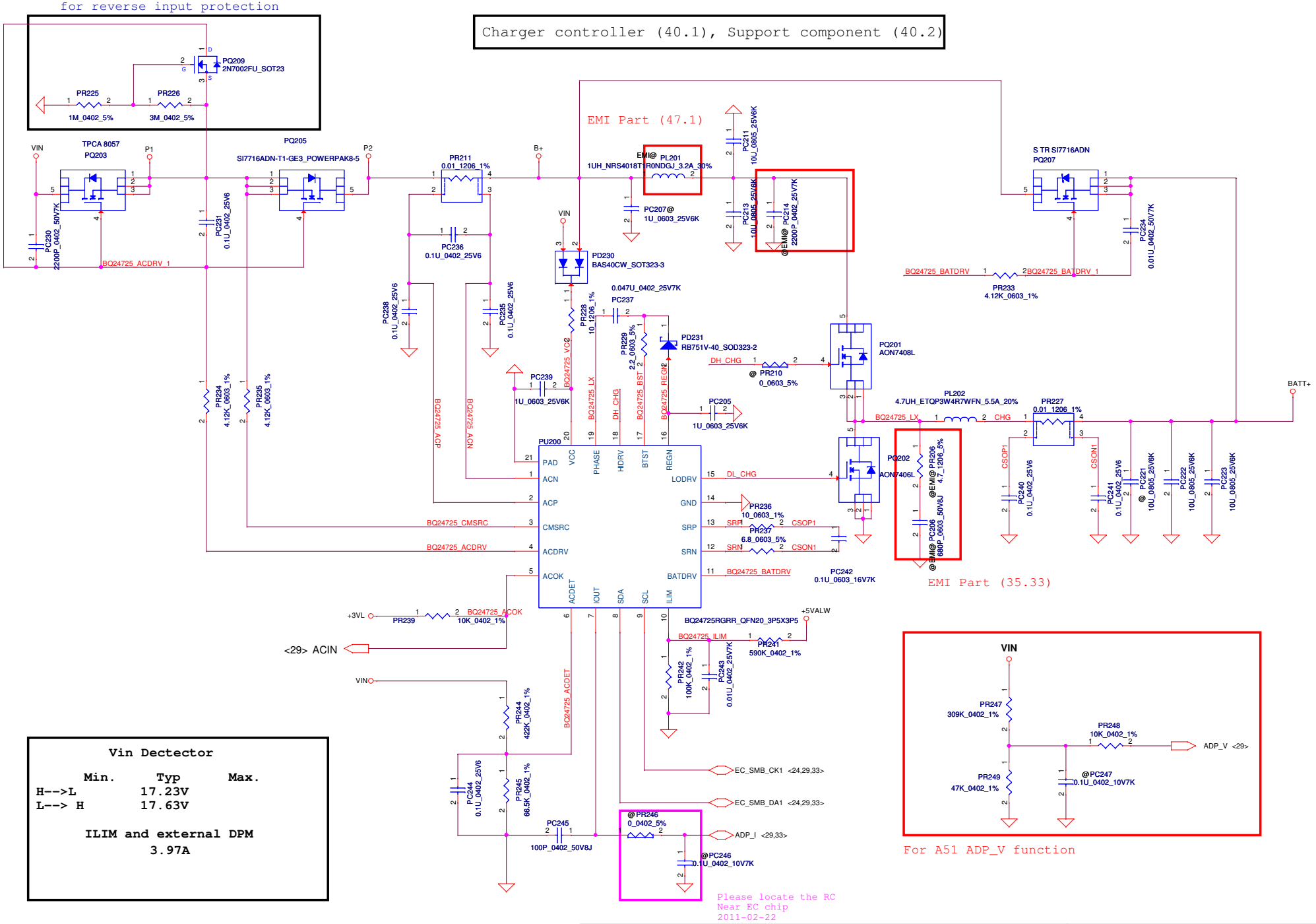
for reverse input protection

Charger controller (40.1), Support component (40.2)



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

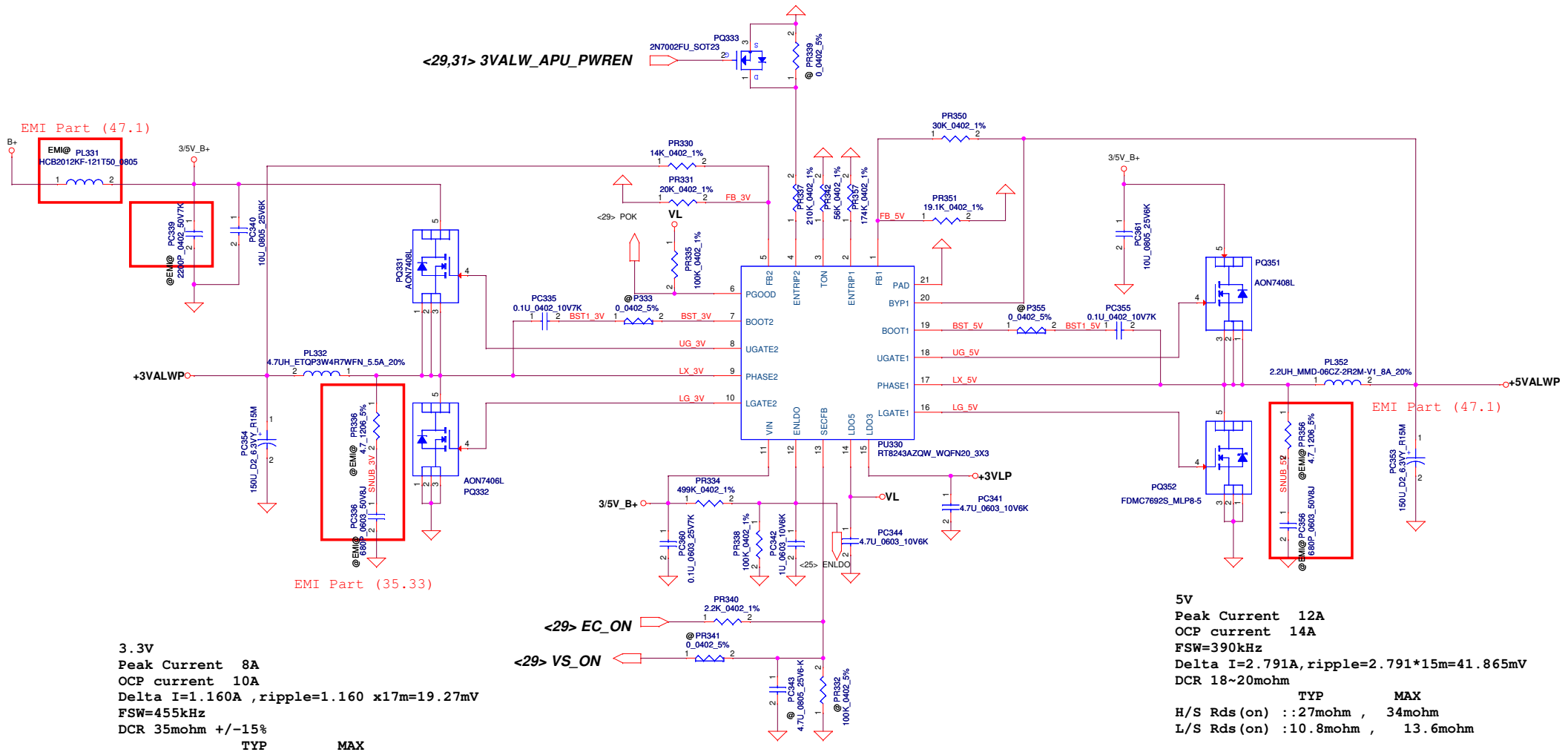
Compal Electronics, Inc.

Title: **CHARGER**

Size: Custom | Document Number: LA-9868P | Rev: 1.0

Date: | Sheet 34 of 42

3/5VALW controller (35.1), Support component (35.2)



3.3V
Peak Current 8A
OCP current 10A
Delta I=1.160A ,ripple=1.160 x17m=19.27mV
FSW=455kHz
DCR 35mohm +/-15%

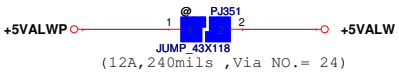
	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:19mohm ,	23.5mohm

5V
Peak Current 12A
OCP current 14A
FSW=390kHz
Delta I=2.791A,ripple=2.791*15m=41.865mV
DCR 18~20mohm

	TYP	MAX
H/S Rds(on)	::27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

(100mA,20mils ,Via NO.= 1)

(8A,160mils ,Via NO.= 16)



(12A,240mils ,Via NO.= 24)

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.	
Title	3VALW/5VALW
Size	Custom
Document Number	
Rev	1.0
Date:	
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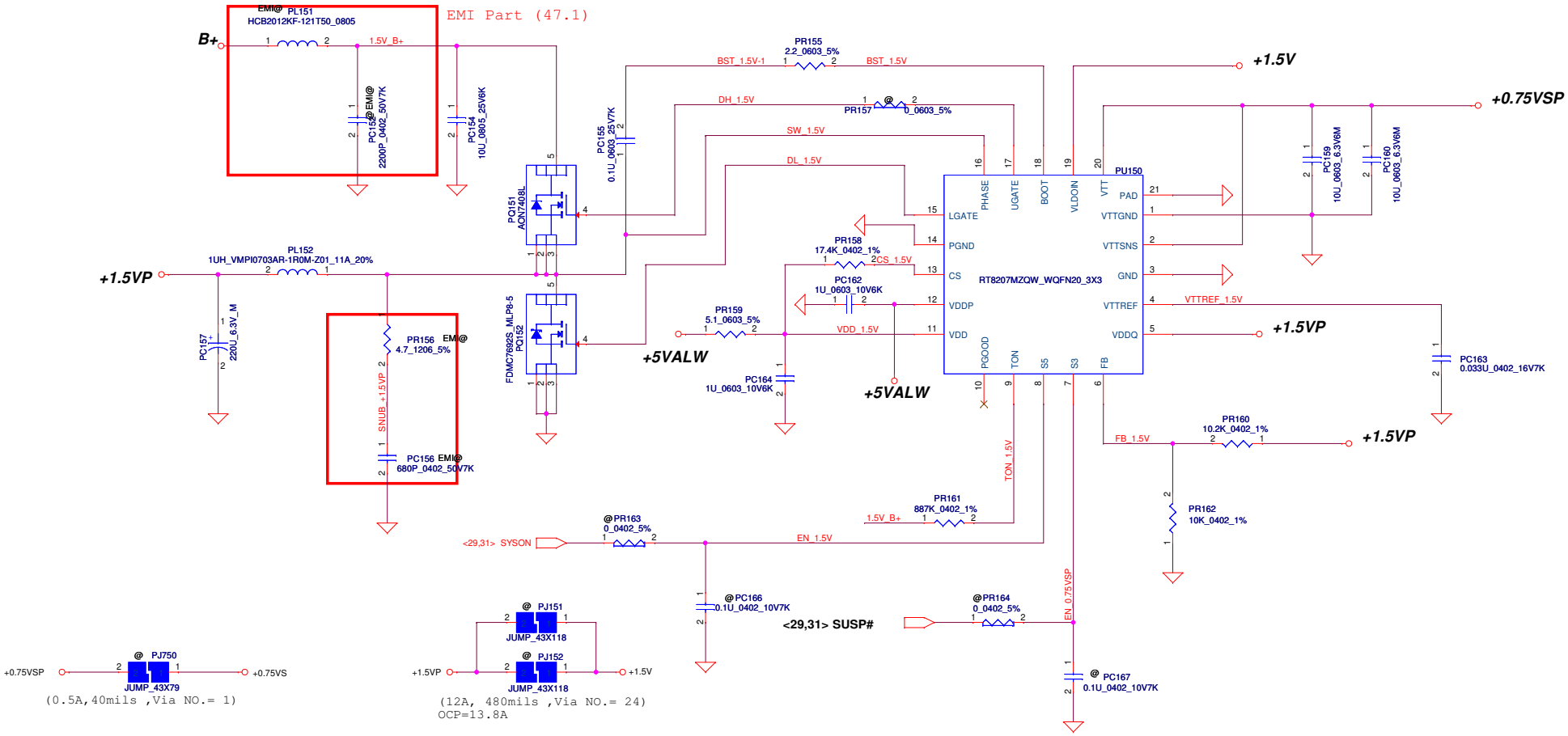
DDR controller (35.3), Support component (35.4)



1.5V
Peak Current 12A
OCP current 13.82A
FSW=500kHz
DCR 8.3 ~ 10mohm

	TYP	MAX
H/S Rds(on)	**:27mohm ,**	**34mohm**
L/S Rds(on)	**:10.8mohm ,**	**13.6mohm**

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

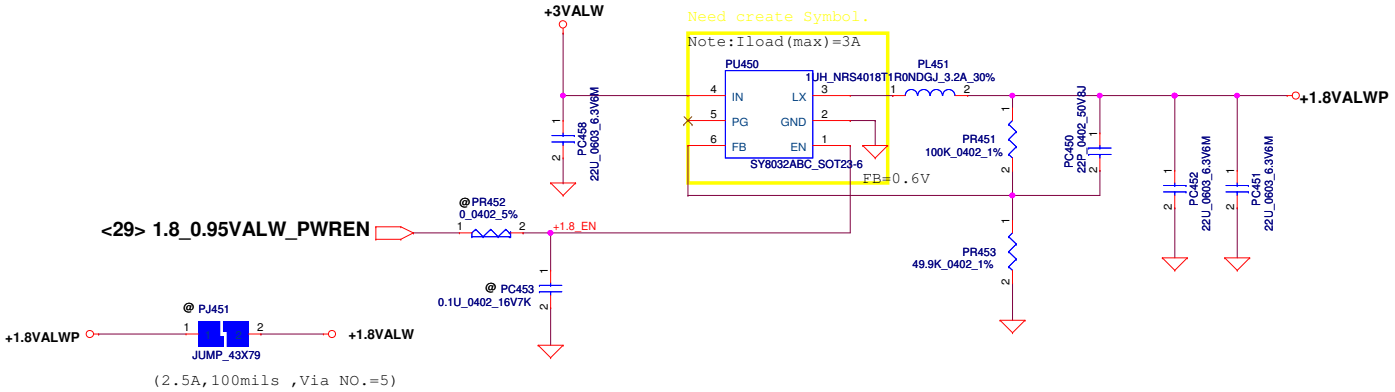
Compal Electronics, Inc.

Title: *1.5VP/0.75VSP/1.8VSP*

Size: Custom | Document Number: *LA-9869P* | Rev: 1.0

Date: | Sheet 36 of 42

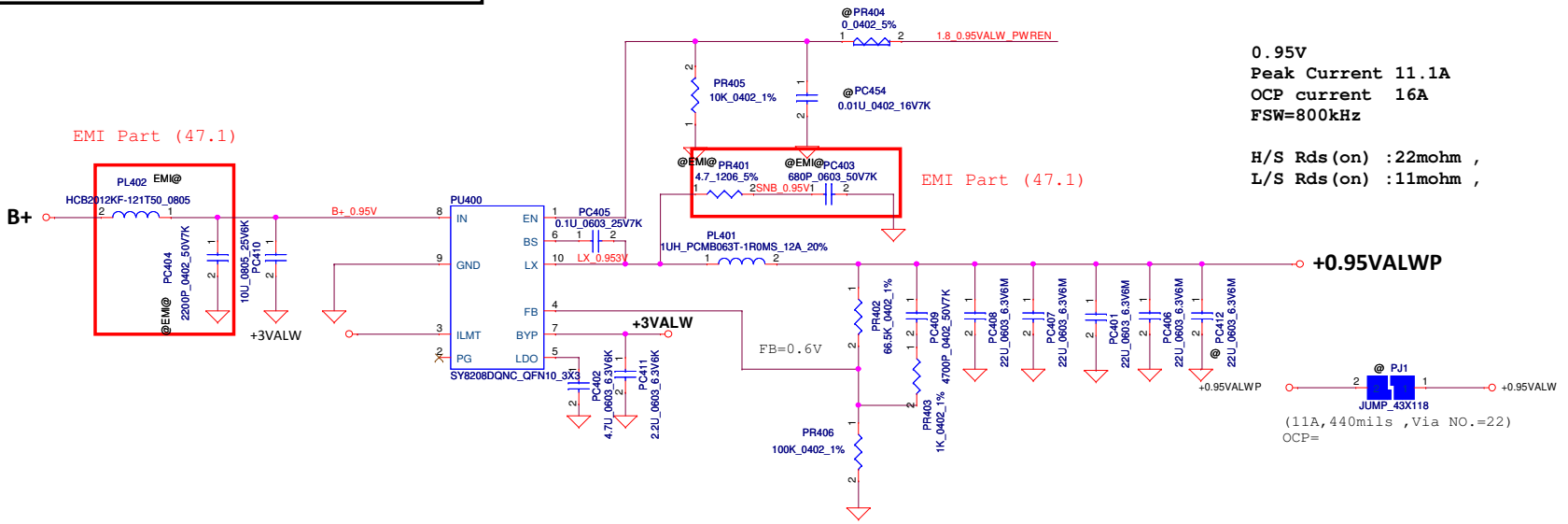
1.8V controller (35.15), Support component (35.16)



1.8V
Peak Current 2.5A
OCP current 3.5A
FSW=800kHz

H/S Rds(on) :100mohm ,
L/S Rds(on) :80mohm ,

0.95V controller (35.5), Support component (35.6)



0.95V
Peak Current 11.1A
OCP current 16A
FSW=800kHz

H/S Rds(on) :22mohm ,
L/S Rds(on) :11mohm ,

Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

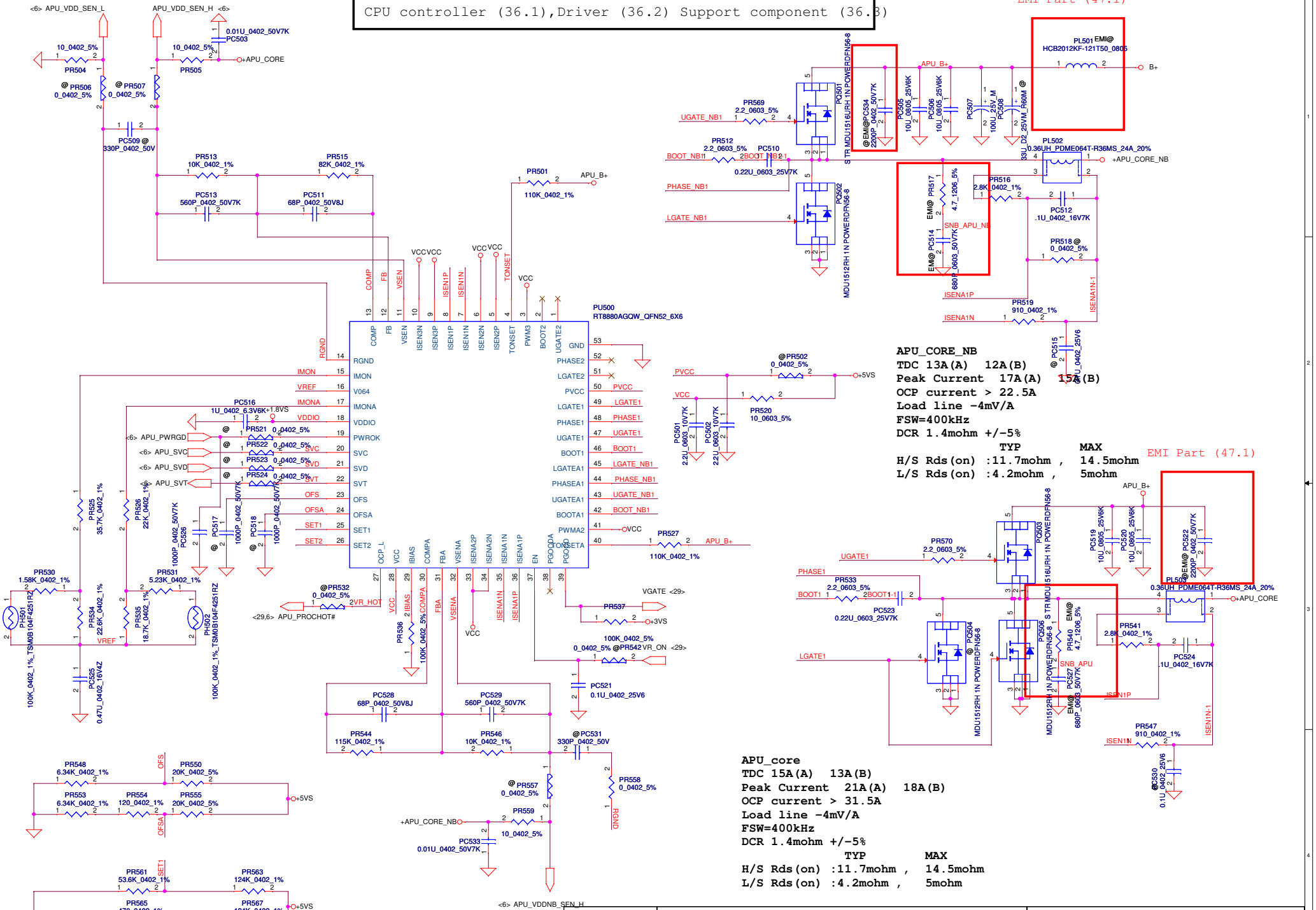
Title: *+1.8VALWP/+0.95VALWP*

Size: Custom | Document Number: *LA-9868P* | Rev: 1.0

Date: Thursday, May 16, 2013 | Sheet 37 of 42

CPU controller (36.1),Driver (36.2) Support component (36.3)

EMI Part (47.1)



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	

Compal Electronics, Inc.

Title: +CPU_CORE/VDDNBP

Size	Document Number	Rev
Custom	LA9868P	1.0

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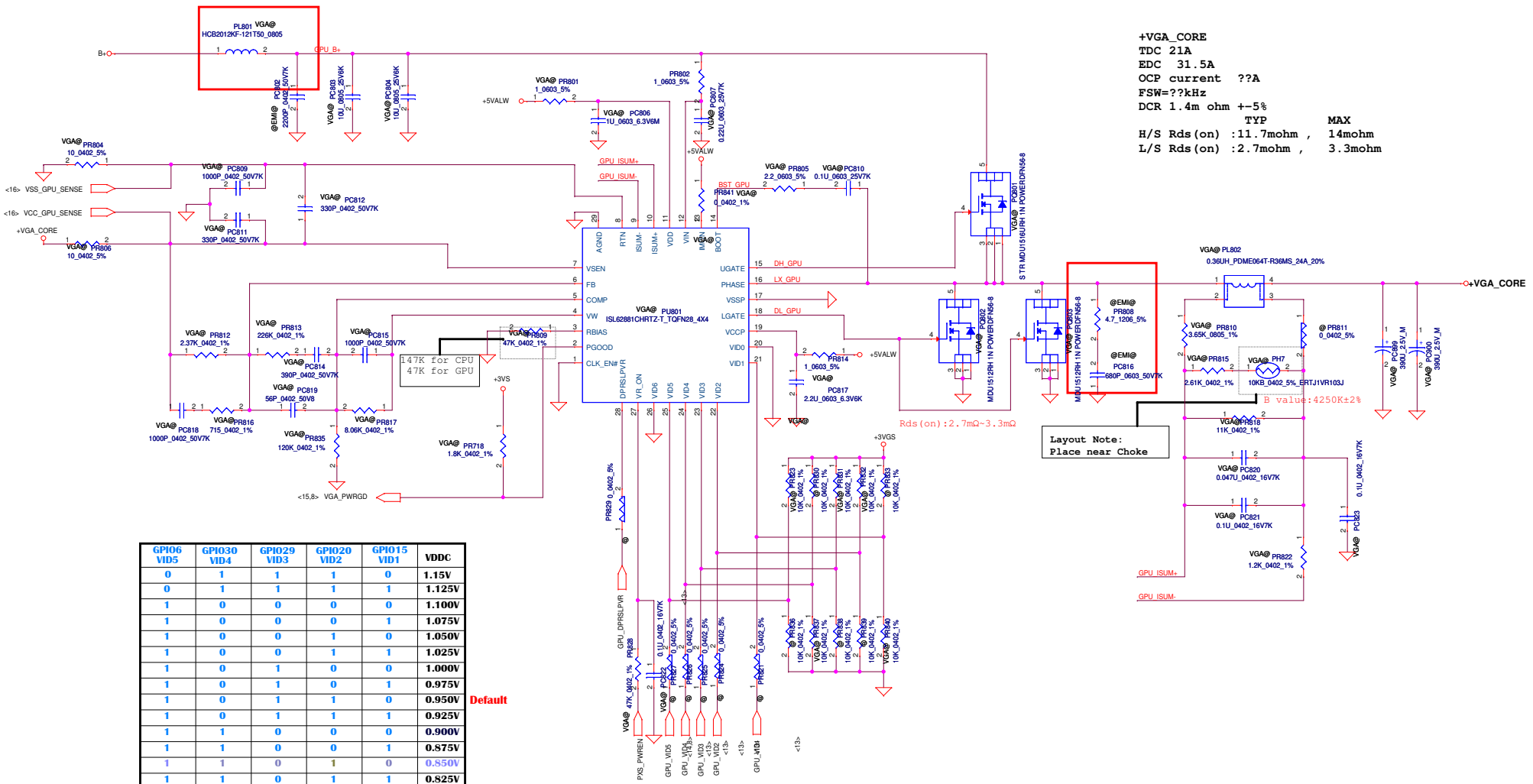
VGA controller (43.1),Driver (43.2) Support component (43.3)

EMI Part (47.1)



GPIO6 VID5	GPIO30 VID4	GPIO29 VID3	GPIO20 VID2	GPIO15 VID1	VDDC	
0	1	1	1	0	1.15V	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	Default
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	
1	1	1	0	1	0.775V	

Compal Electronics, Inc.

Title: +VPU_COREP

Size	Document Number	Rev
C	LA-9868P	1.0

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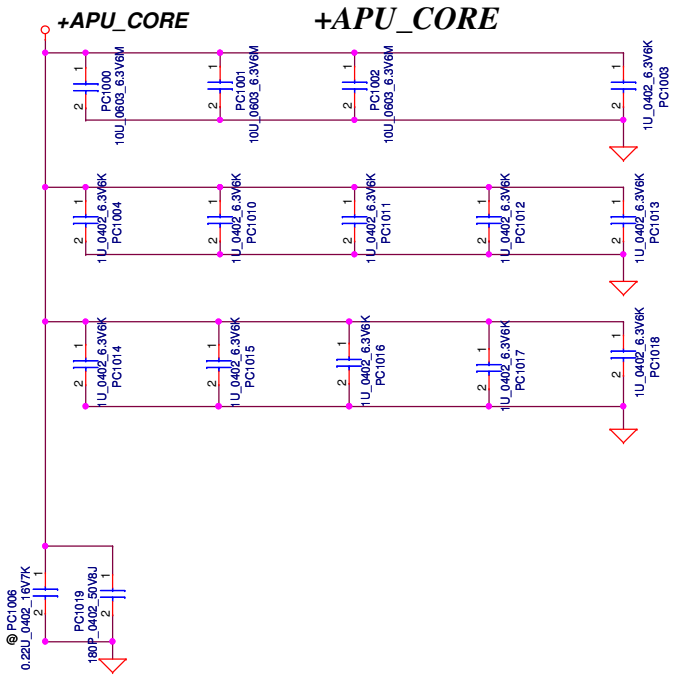
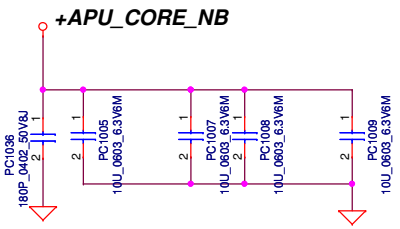
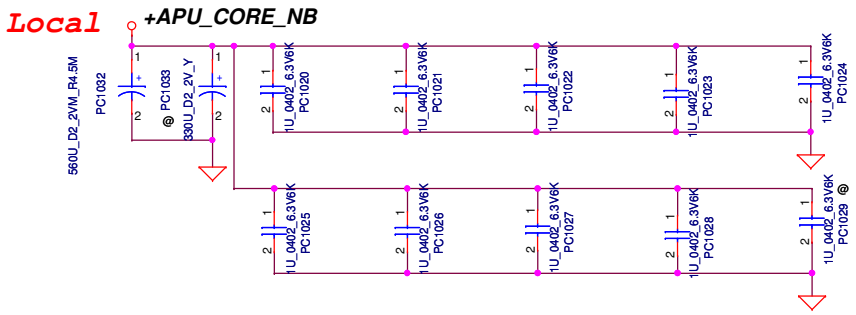
CPU_Core output CAP (Including MLCC) 36.4



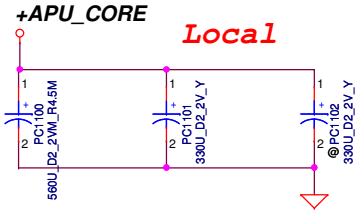


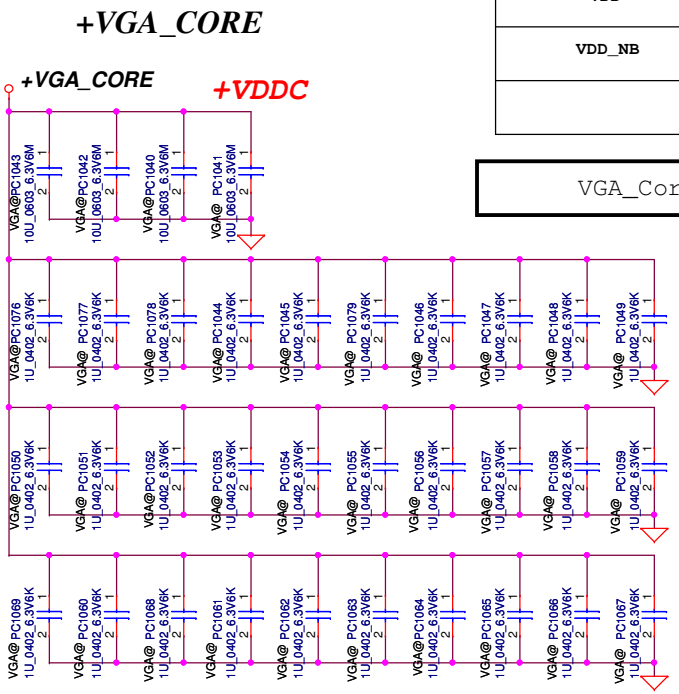
GFX output CAP (Including MLCC) 36.5



kabini	560uF*4.5m	10uF (0603)	1u (0402)	0.22uF	180P (0402)
VDD	2	3	11		1
VDD_NB	1	4	9		1

VGA_Core output CAP (Including MLCC 43.9)





Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	

Compal Electronics, Inc.

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
A3	LA-9868P	1.0

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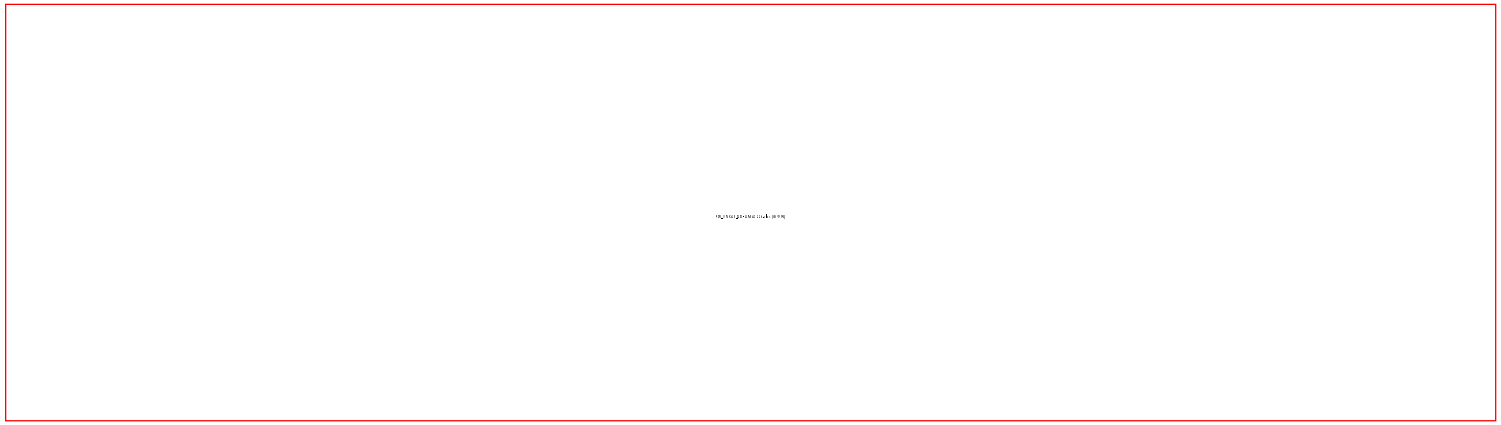
Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase



Security Classification	Compal Secret Data		
Issued Date	2012/09/27	Deciphered Date	2015/09/27

Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number: VCUAA	Rev: 1.0
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HW PIR (Product Improve Record)

VNKAE LA-9868P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

Item	Page	Date	Request	Solution
1		2013/03/5a	Change APU to PR sample	PR sample PN SA00006R300, SKU 4519NL51L03
2	P30	2013/03/5a	PCB cut outline	Remove SW1
3	P06	2013/03/5a	co-lay eDP & LVDS	Due to common eDP cable, swap Lane0 and Lane2 to follow common design; replace CC106, CC102 with RC75, RC76; add RC77, RC78, CC109, CC110.
4	P30	2013/03/06a	no need power button	Remove SW2
5	P30	2013/03/06a		Add C24(0.1uF) to ON/OFFBTN# and set to ESD@
6	P06	2013/03/06a		Add CC99(1000pF) to APU_RST# and set to ESD@
7		2013/03/06a		Change CC93, CC94, CC97, CB6 to ESD@
8	P07	2013/03/06a	BIOS ROM	Change UC5 to always mount on 43-level
9	P07	2013/03/06a	For vendor recommand	Change CC22, CC23 from 5.6pF to 4.7pF(SE07147AC80)
10	P28	2013/03/07a	co-lay card reader for EMI request	Update card reader schematic for co-lay GL834L and RT5117
11	P09	2013/03/07b	Remove 0ohm res	Change RC116, RC117, RC119, RC120 to short pad symbol
12	P26	2013/03/07b	Remove 0ohm res	Change RA18, RA24, RA22, RA36, RA37 to short pad symbol
13	P05	2013/03/07b	Remove 0ohm res	Change R2 to short pad symbol
14	P20	2013/03/07b	Remove 0ohm res	Remove R106
15	P29	2013/03/07b	Remove 0ohm res	Change RB36 to short pad symbol
16		2013/03/11a	Update power schematic	
17	P28	2013/03/12a	Remove co-lay RT5117	Update card reader schematic
18	P30	2013/03/18a	Change PCB PN	Change PCB PN to DAZ0WJ00100
19	P30	2013/03/18a		Remove DC-IN JACK PN due to BOM structure changed
20	P24	2013/03/18a	Remove 0ohm res	Change RR1, RR2 to short pad symbol
21	P08	2013/03/18a	For power consumption improve	Change VRAM_SEL to TOUCH_SEL for BTO to improve battery life.
22	P26	2013/03/25a	ESD request	Change DA1, CA30, CA31, CA34, CA36 to varistor(SCV00001K00)
23	P08	2013/03/25a	vendor recommand	Change CC31 to 8pF(SE00000DB80)
24	P24	2013/03/25a	Remove 0ohm res	Change RR1, RR2 to 0 ohm

Title: HW PIR			
Size: B	Document Number: LA-9868P		Rev: 1.0
Date: Thursday, May 16, 2013		Sheet 42 of 42	