Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2009-07-15

Blade 1.4 MV

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Title: Cover Sheet		
Size: Custom	Document Number: Montevina Blade UMA LA4105P	Rev: 1.0
Date: Saturday, July 18, 2009	Sheet 1 of 45	

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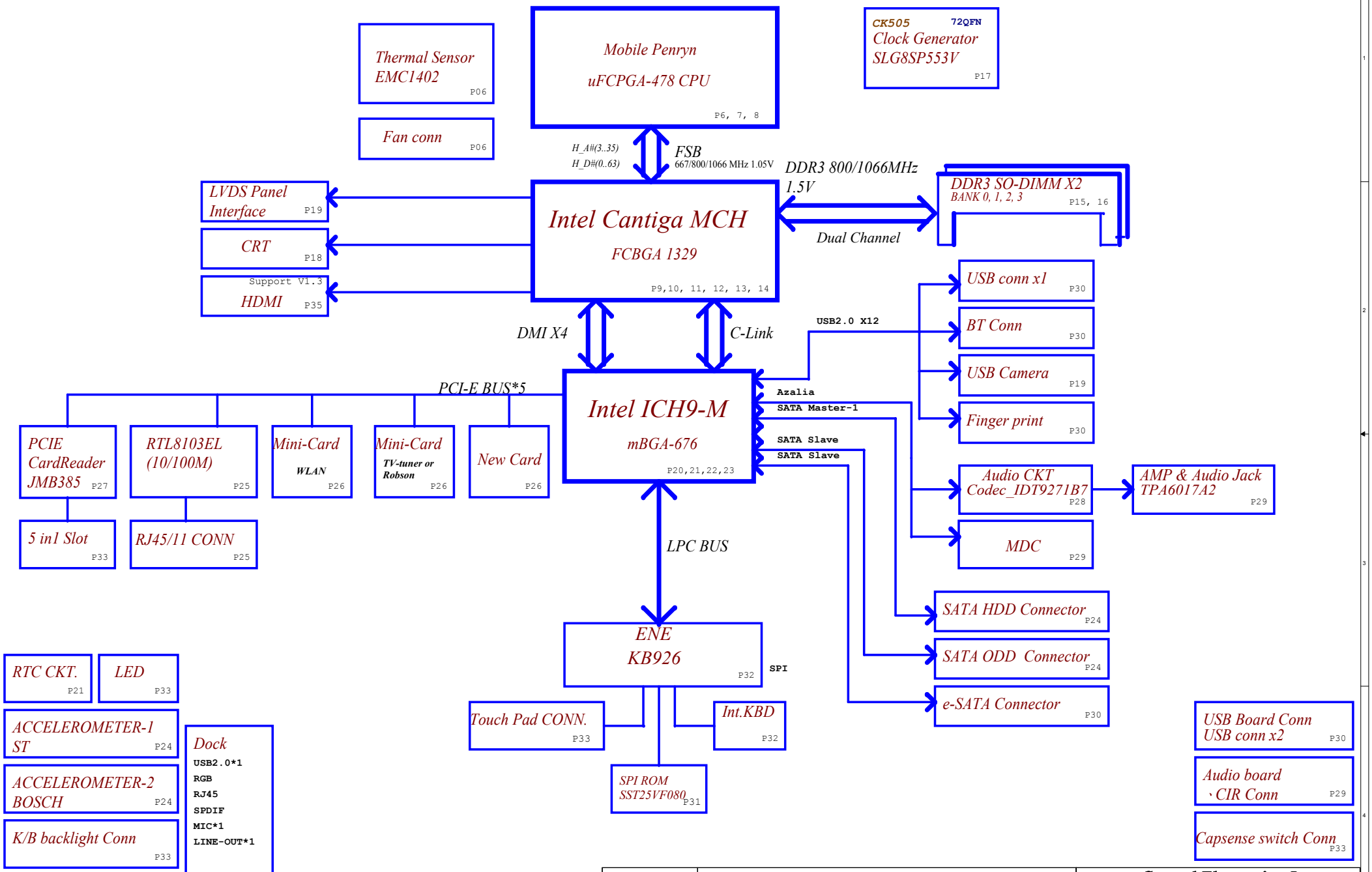
Montevina Consumer 14" UMA



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Title: **Block Diagram**

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Date: Saturday, July 18, 2009 Sheet 2 of 45

Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@/PA@
43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/PR@
43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/PR@
43154432L04 : OPP@/DEBUG@/PR@
43154432L05 : OPP@/DEBUG@/PR@

43154432L01 : UMA GM PA FF (V)
43154432L02 : UMA GM PR FF (V)
43154432L03 : UMA GL PR FF-
43154432L04 : UMA GM OPP (V)
43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930 (SI-1、SI-2)
ICH9M A2 ES2 Base : SA00002AN10 (SI-1、SI-2)
Cantiga GM45 B-2 QS QT62 : SA00002JT10 (PV-1)
Cantiga GM45 B-3 QS QU36 : SA00002JT50 (PV-2)
ICH9M A-3 QS - BASE QT09 : SA00002JH00 (PV-1、PV-2)
Cantiga GM45 B-3 QS SLB97 : SA00002JJE0 (MV-1、MV-2)
ICH9M A-3 QS -BASE SLB8Q : SA00002JHB0 (MV-1、MV-2)

PCB : DA600007110 --->M/B
DAZ03V00200 --->Main
DAZ03V00101 --->OPP

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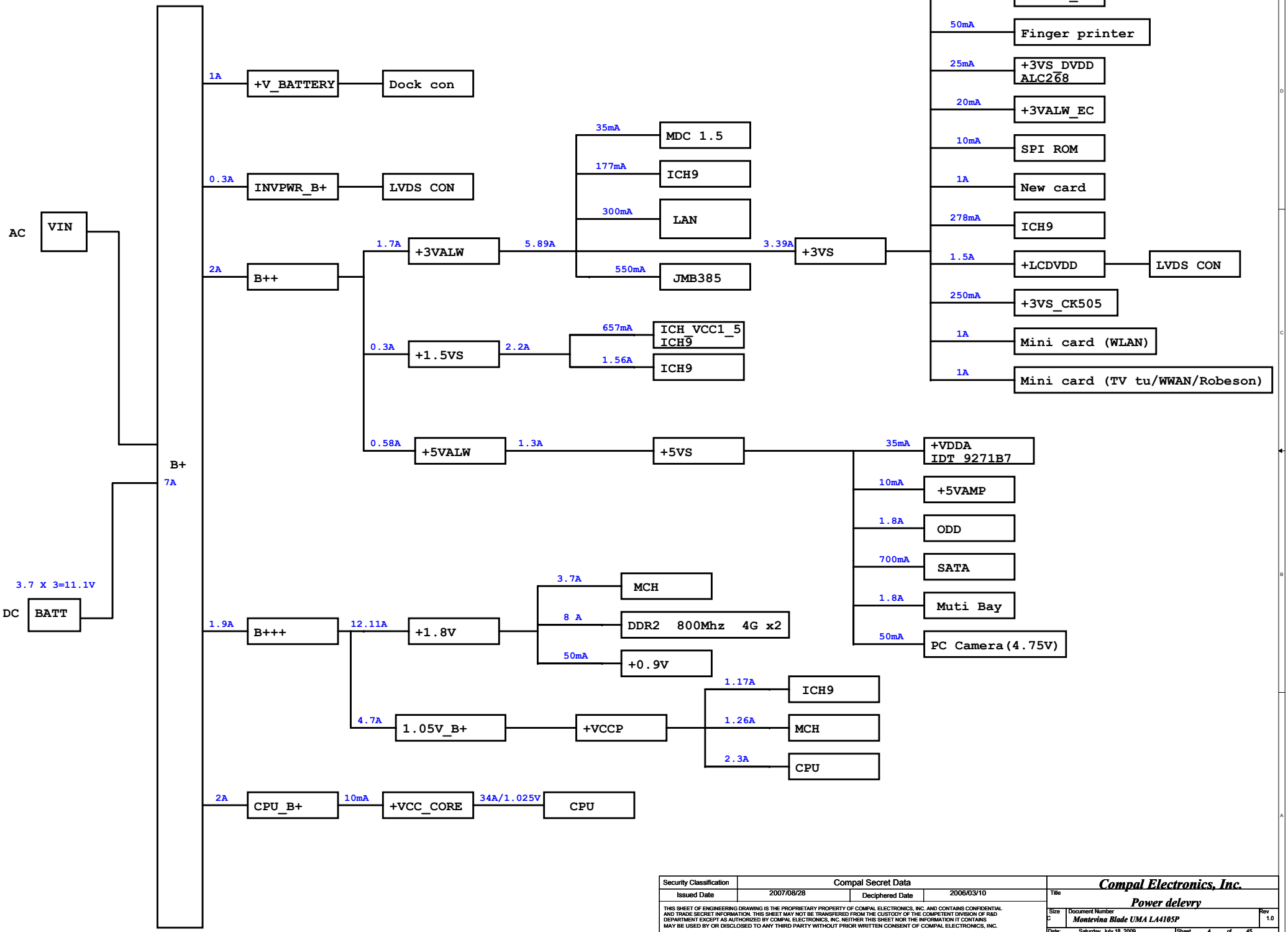
Title: Notes List

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 3 of 45



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Title: Power delevry

Size	Document Number	Rev
C	Montevina Blade UMA LA4105P	1.0

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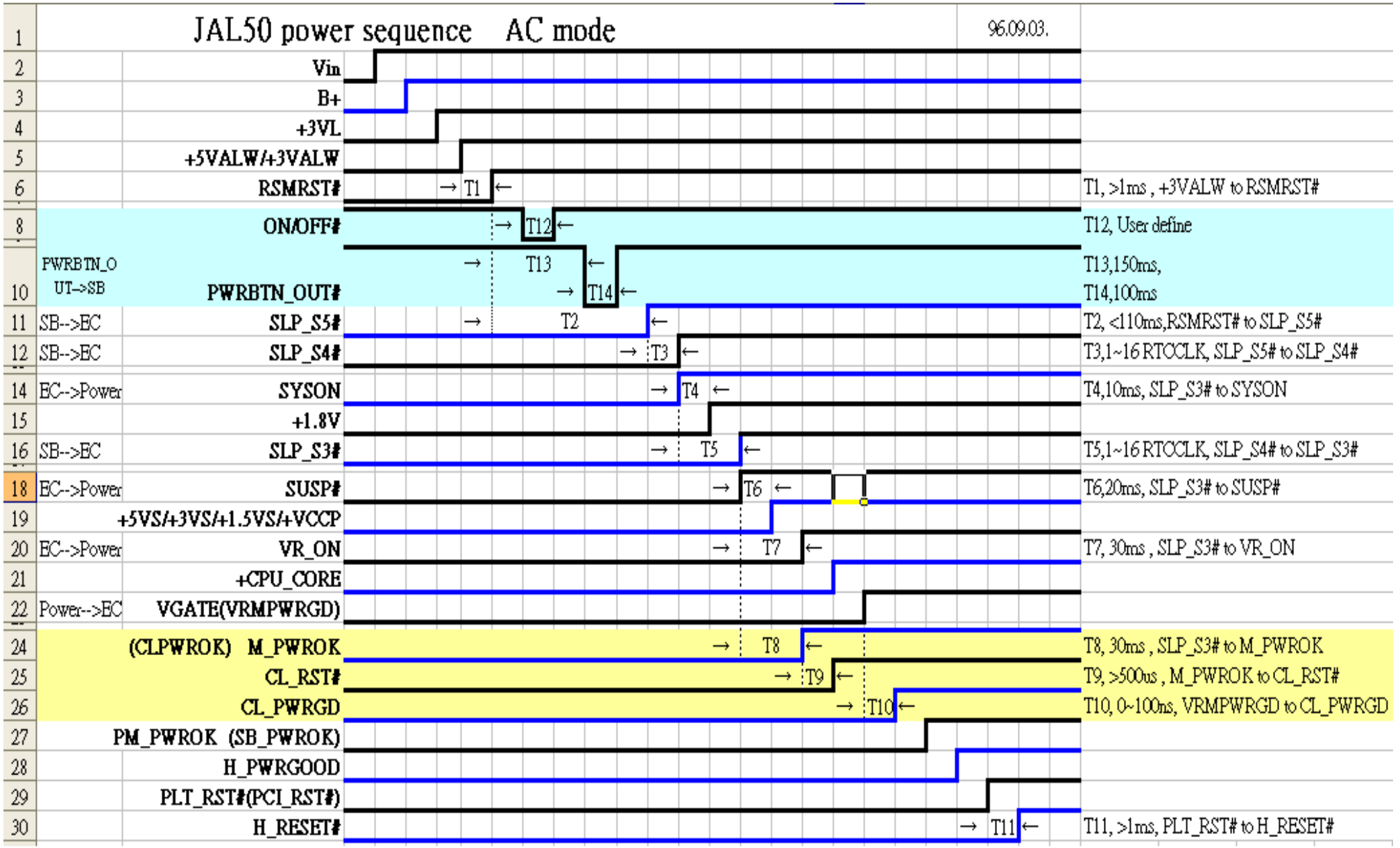

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Title: **Notes List**

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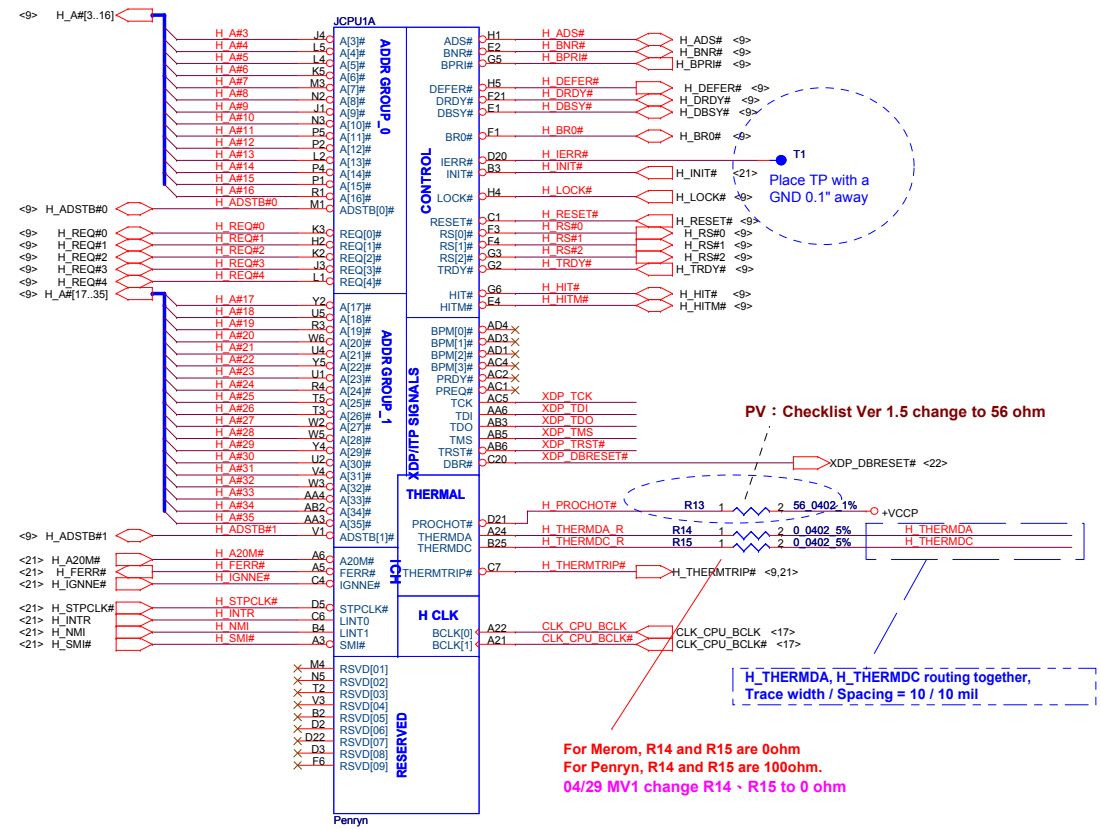
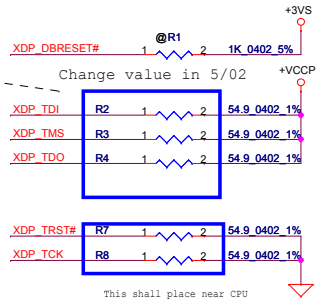


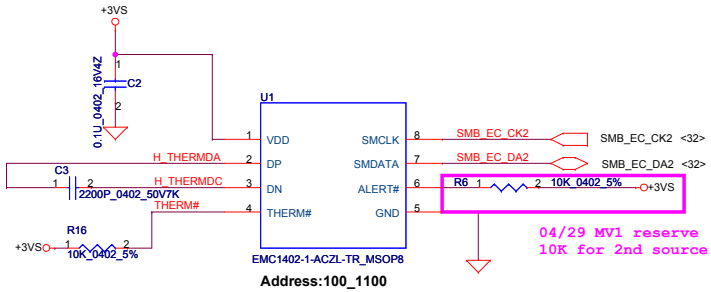
ITP-XDP Connector

PV： follow check list ver:1.5 change to 51 ohm

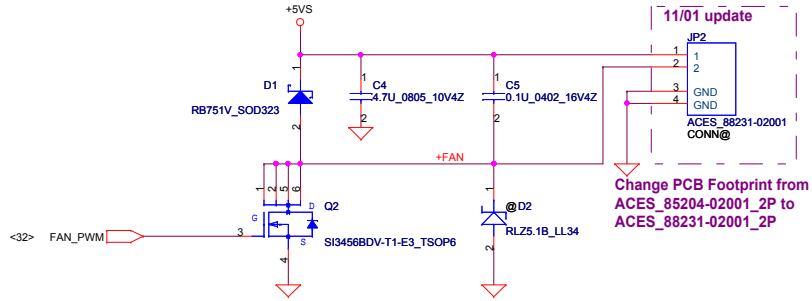
04/29 MV1 R2~R8 change to 54.9 Ohm, follow checklist 2.0



03/18 PV：Delete XDP connector



PWM Fan Control circuit



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Title: Penryn(1/3)-AGTL+/ITP-XDP

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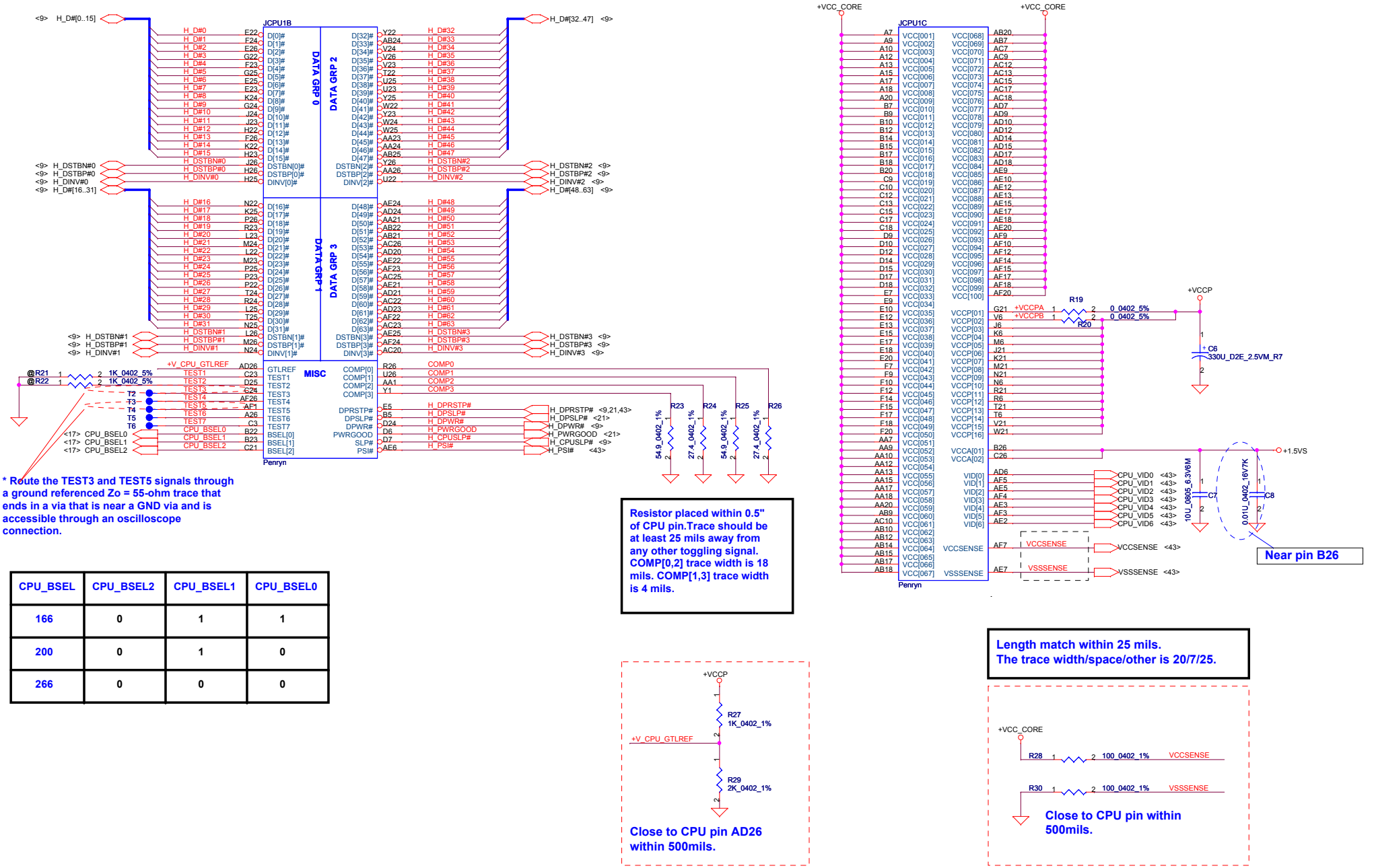
Date: Saturday, July 18, 2009 | Sheet 6 of 45



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26 within 500mils.

Length match within 25 mils.
The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/ITP-XDP

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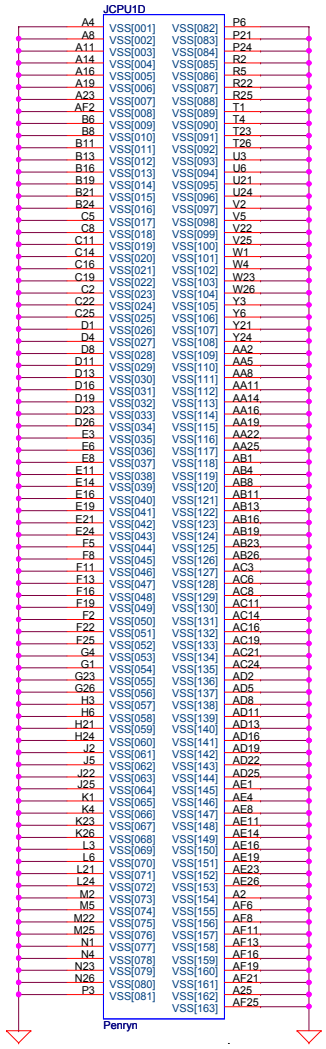
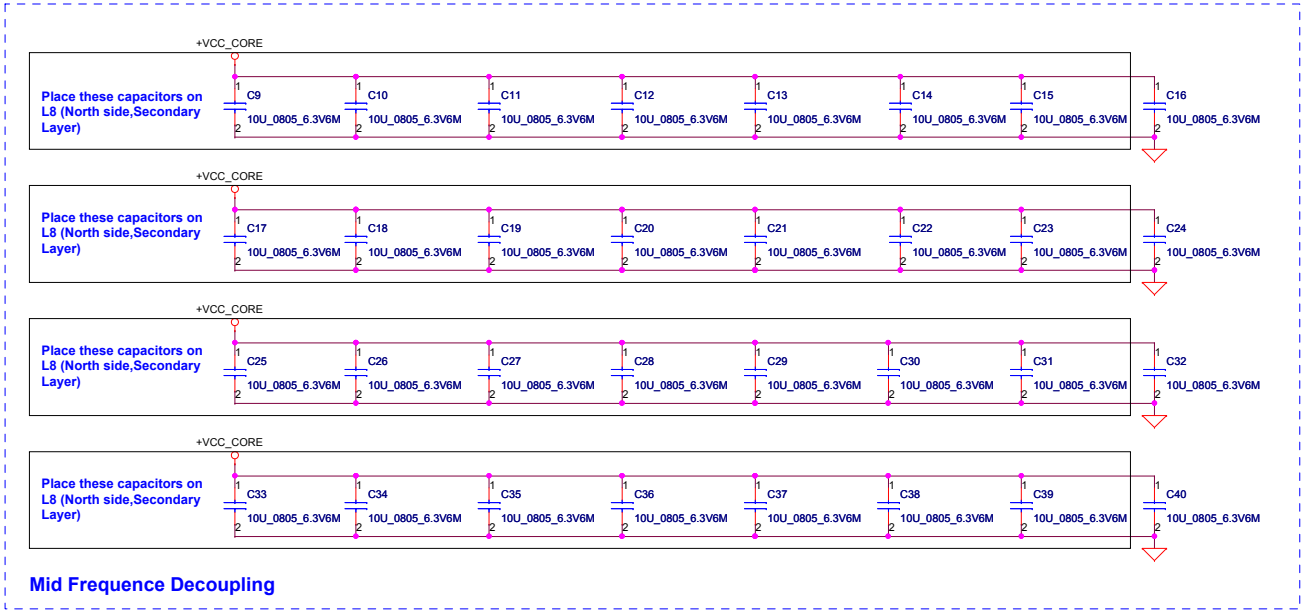
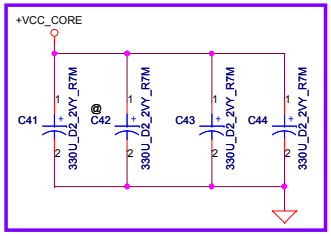


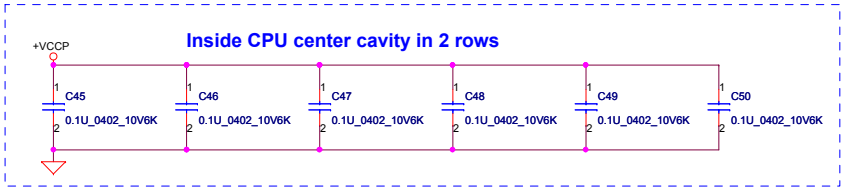


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



11/21 Change ESR=7m ohm



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Title	Penryn(3/3)-AGTL+/ITP-XDP
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Rev	1.0
Date: Saturday, July 18, 2009	Sheet 8 of 45

Layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note: V_DDR_MCH_REF
trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

PV : follow check list ver:1.5 change to 10K ohm

Follow Design Guide
For Cantiga: 80.6ohm

0621 add CLK and DAT for DVI

*R44*Follow Intel feedback

0830 Add pull-up and pull-down resistor.

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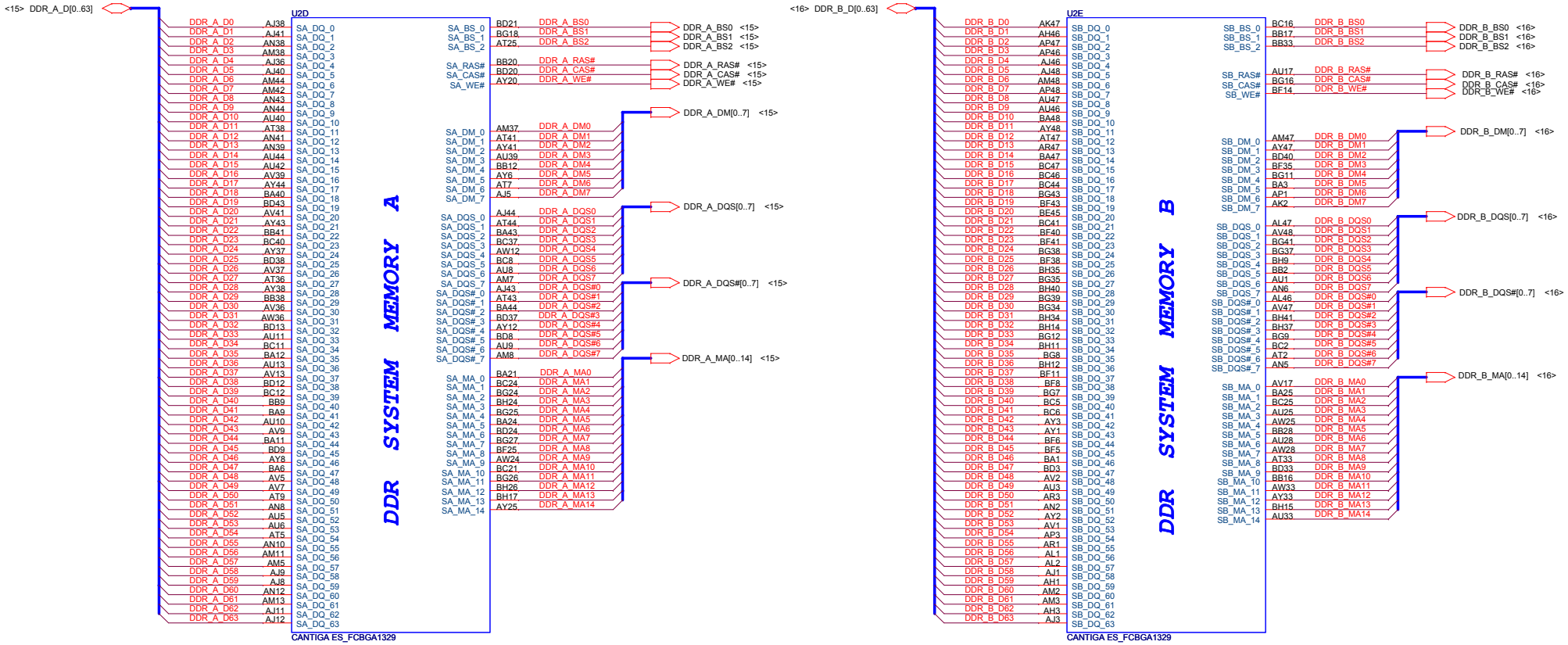
Title: Cantiga(1/6)-AGTL/DMI/DDR

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 9 of 45



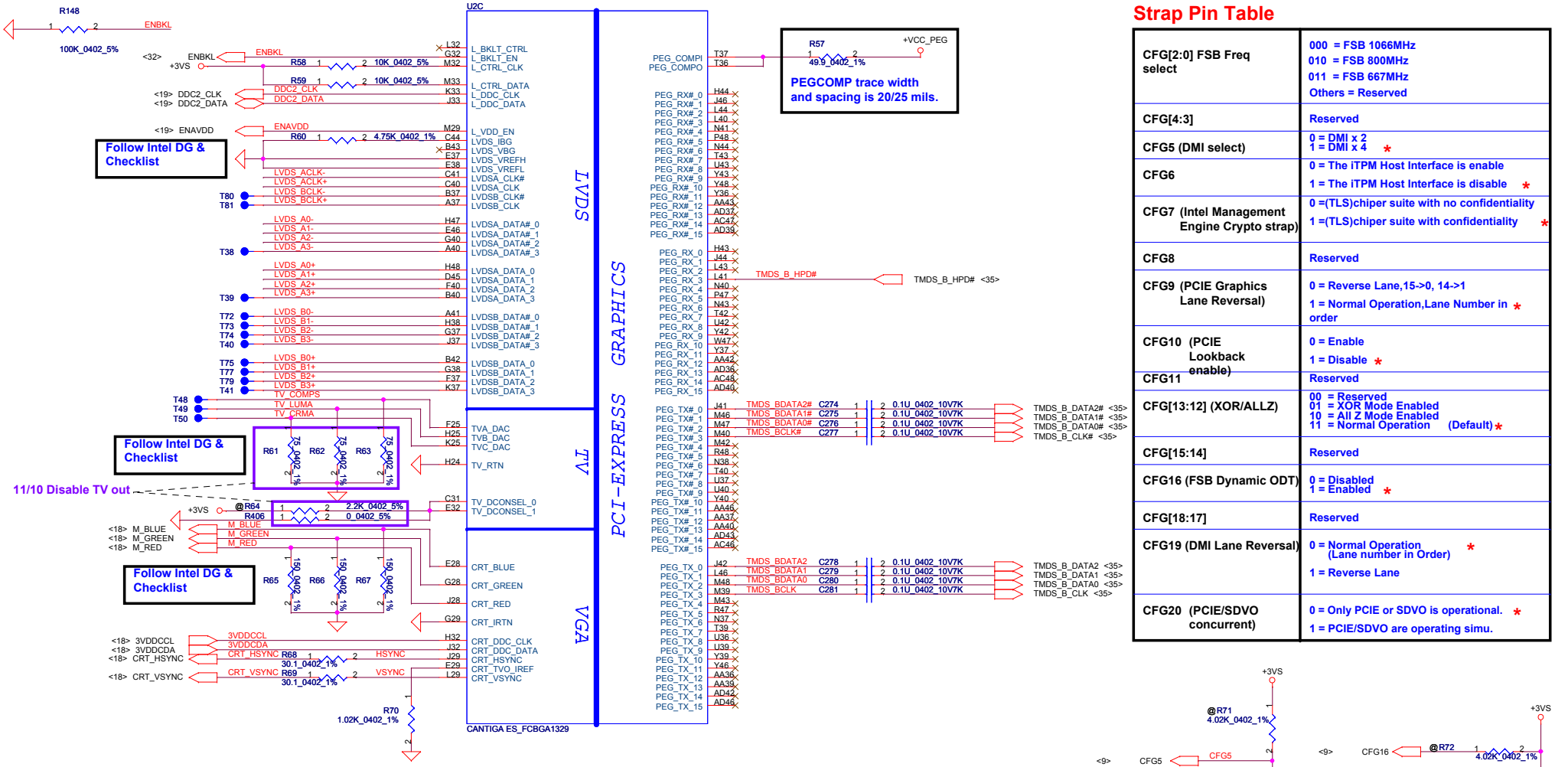
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 10 of 45

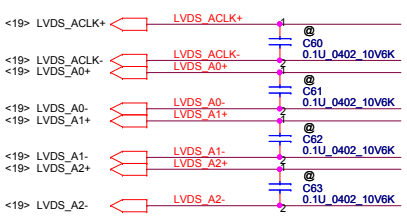


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

04/29 MV-1 Delete CFG5、CFG7、CFG12、CFG13、CFG16

Solve 3G WWAN issue



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Title: Cantiga(3/6)-VGA/LVDS/TV

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Date: Saturday, July 18, 2009 | Sheet 11 of 45

RED Mark: Means UMA & dis@ Power select
~It check by INTEL Graphics Disable Guidelines~

Check Again!!!

POWER

CANTIGA ES_FCBGA1329

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Title: Cantiga(4/6)-PWR

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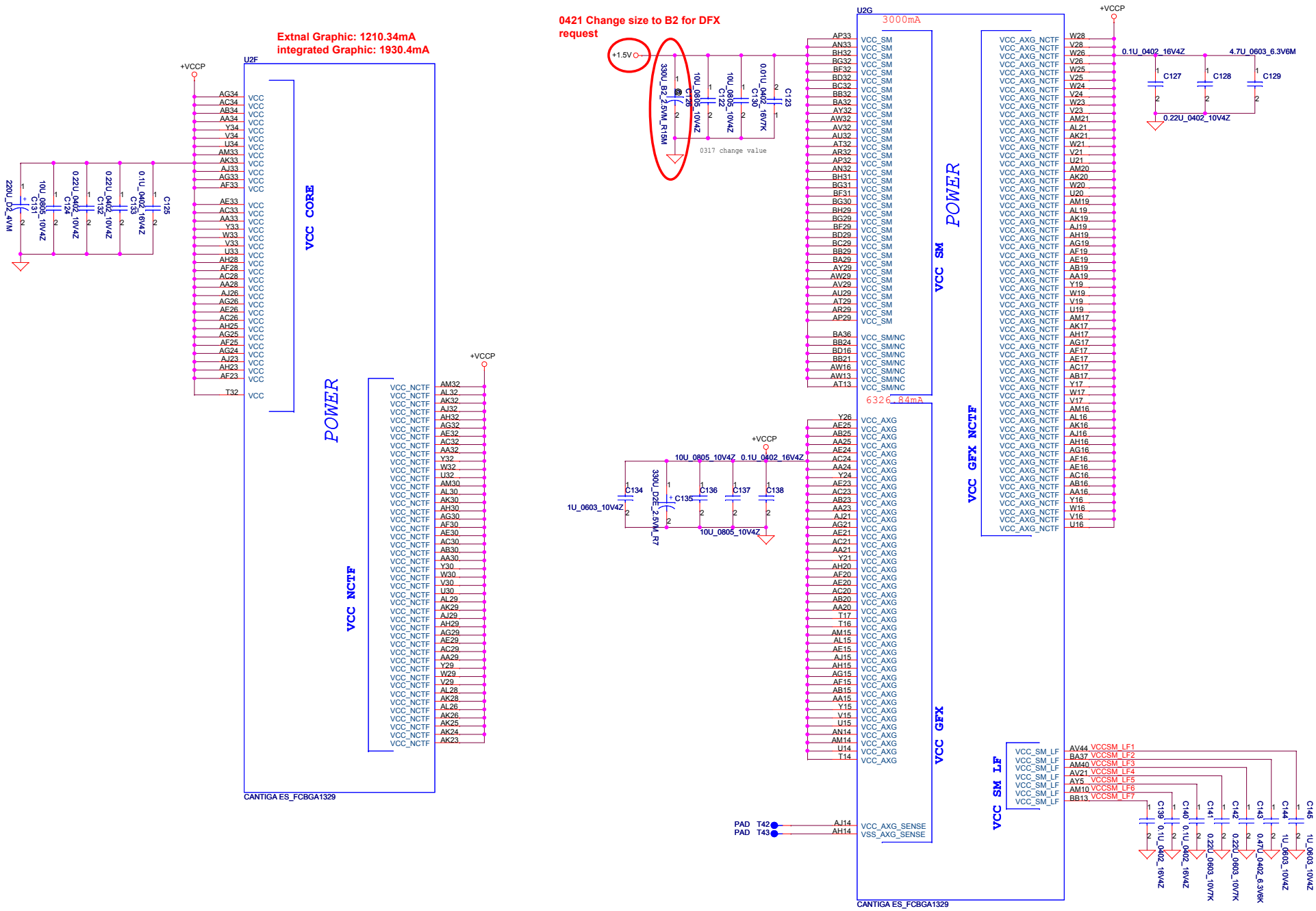

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Title: **Cantiga(5/6)-PWR/GND**

Size	Document Number	Rev
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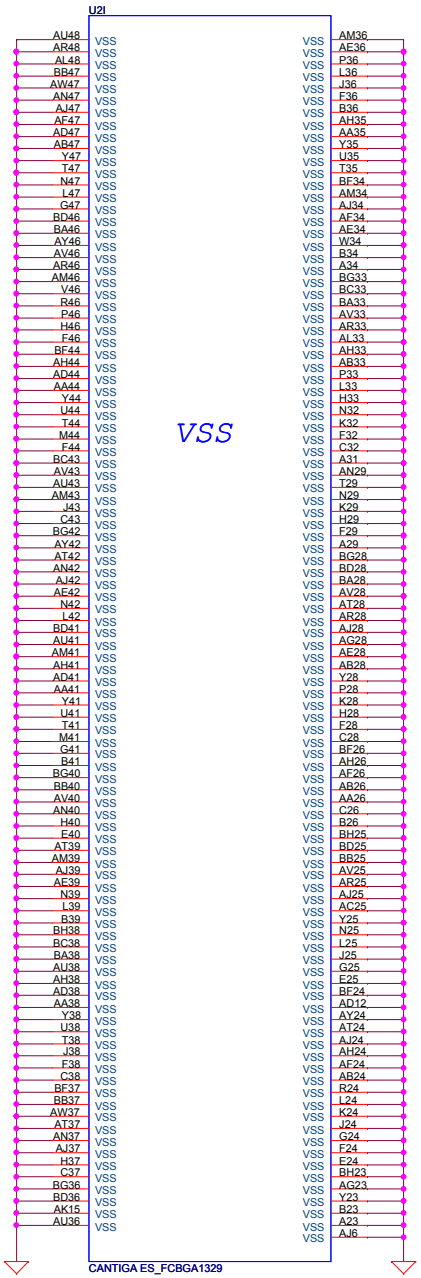
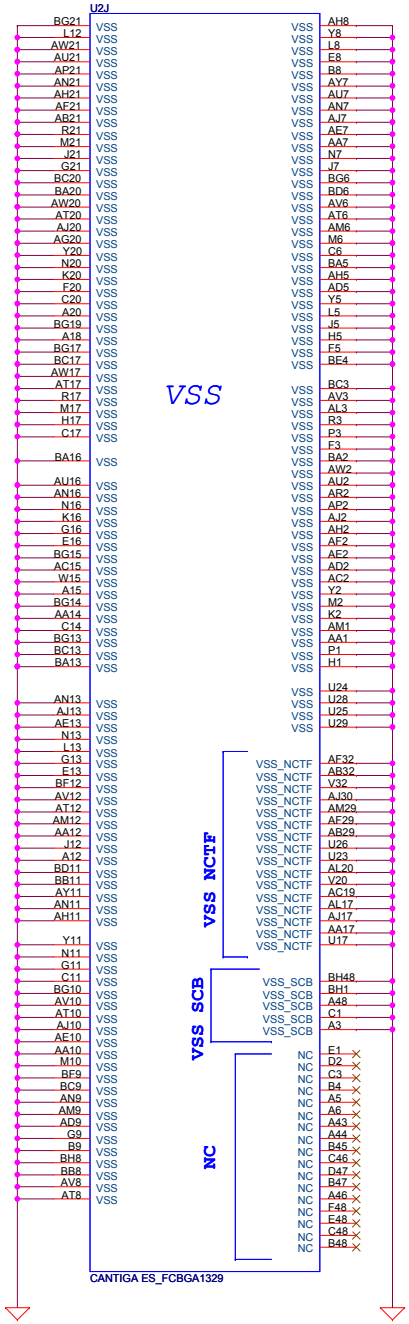
Date: Saturday, July 18, 2009 Sheet 13 of 45





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Title: **Cantiga(6/6)-PWR/GND**

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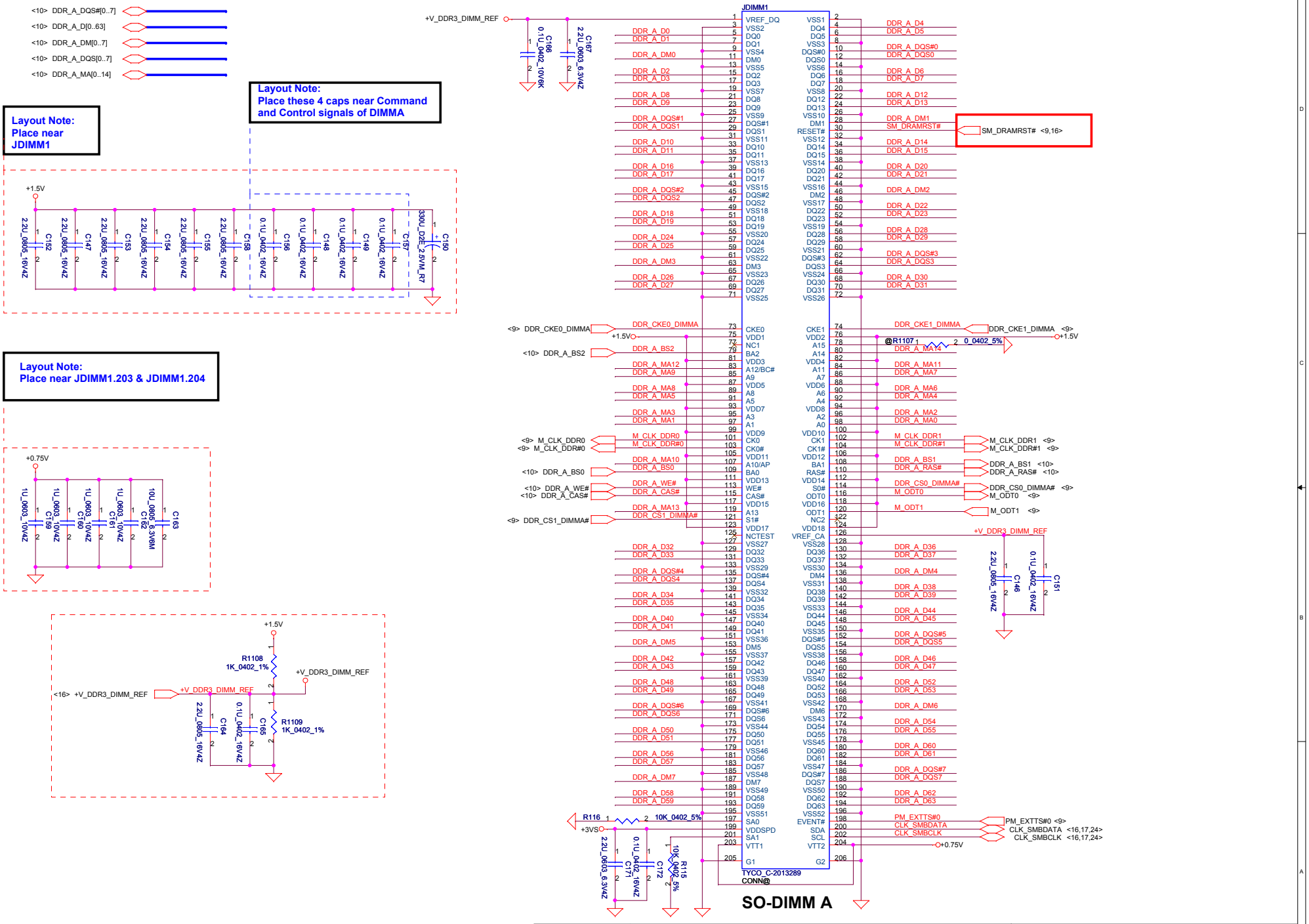
Date: Saturday, July 18, 2009 | Sheet 14 of 45



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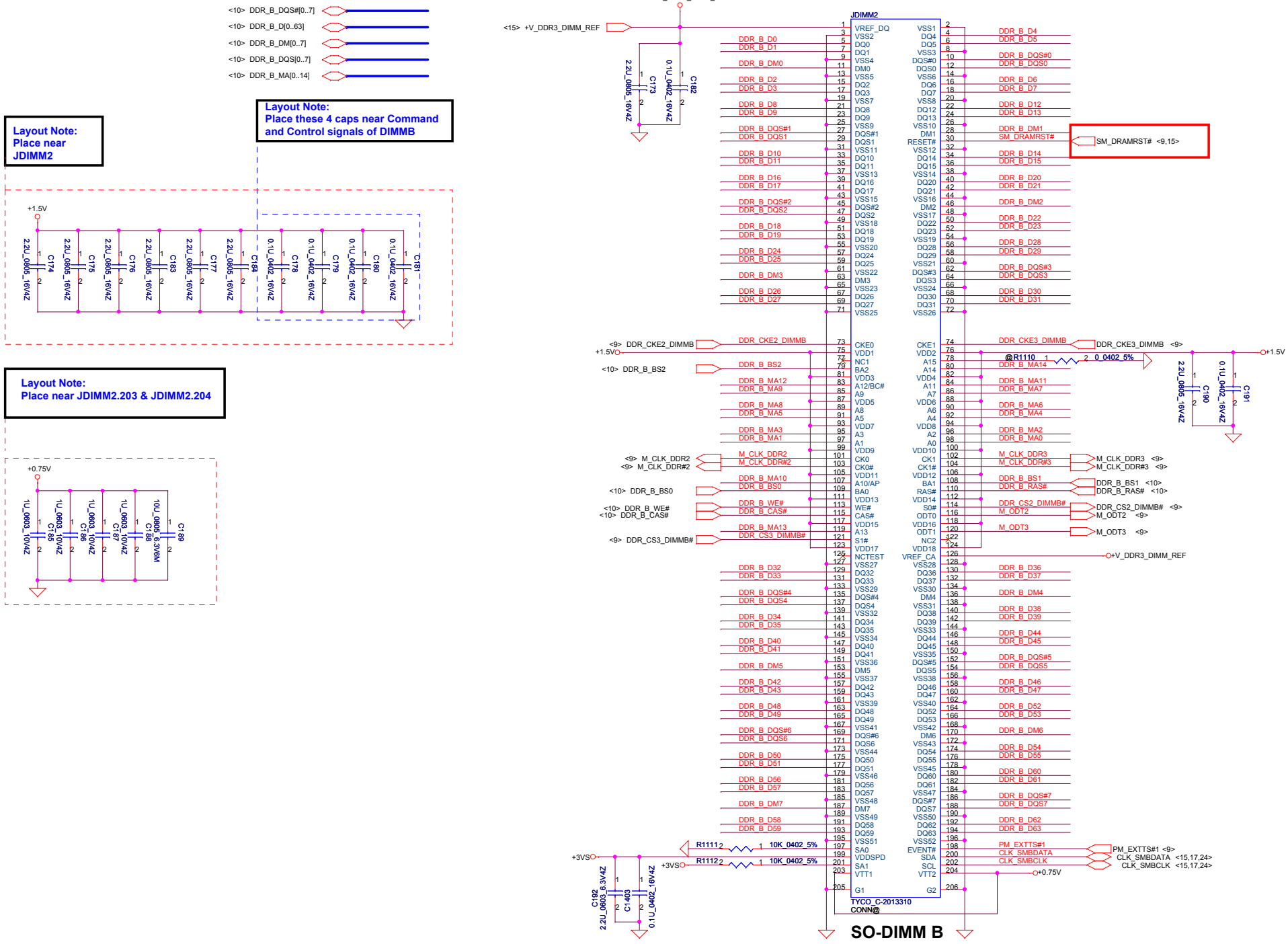
Title	DDRIII-SODIMM SLOT1
Size: Custom	Document Number: Montevina Blade UMA LA4105P
Rev	1.0
Date: Saturday, July 18, 2009	Sheet 15 of 45



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Title	*Compal Electronics, Inc.*	
	DDRIII-SODIMM SLOT2	
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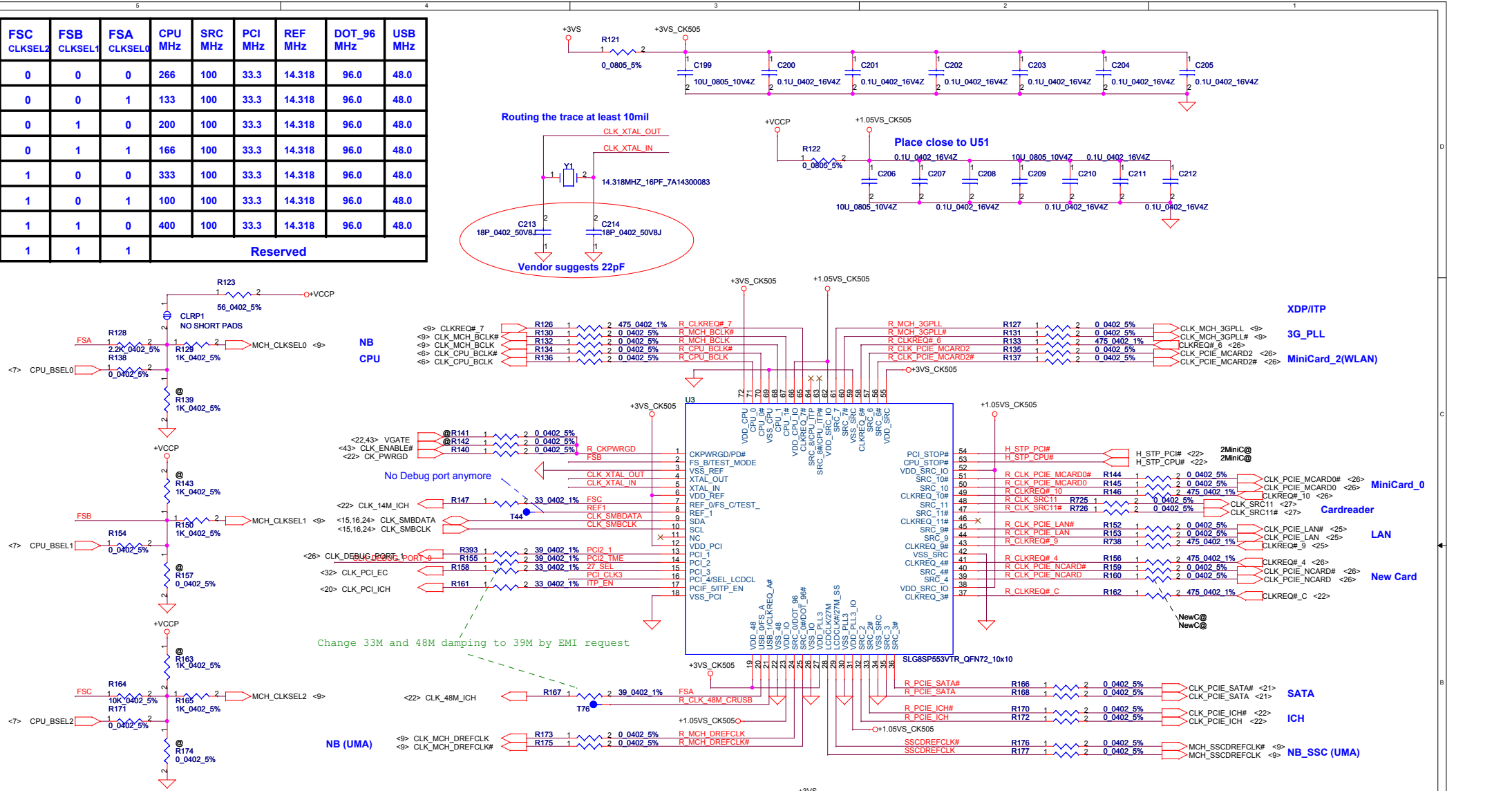
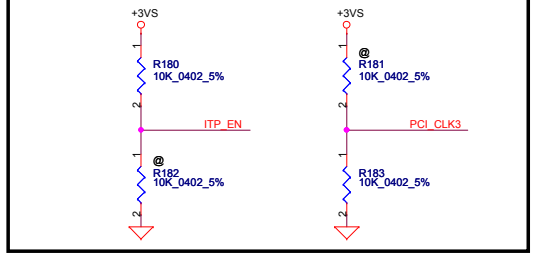
Date: Saturday, July 18, 2009	Sheet 16 of 45	

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



SB, MINI PCI

<BOM Structure>

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Title: Clock Generator CK505

Size	Document Number	Rev
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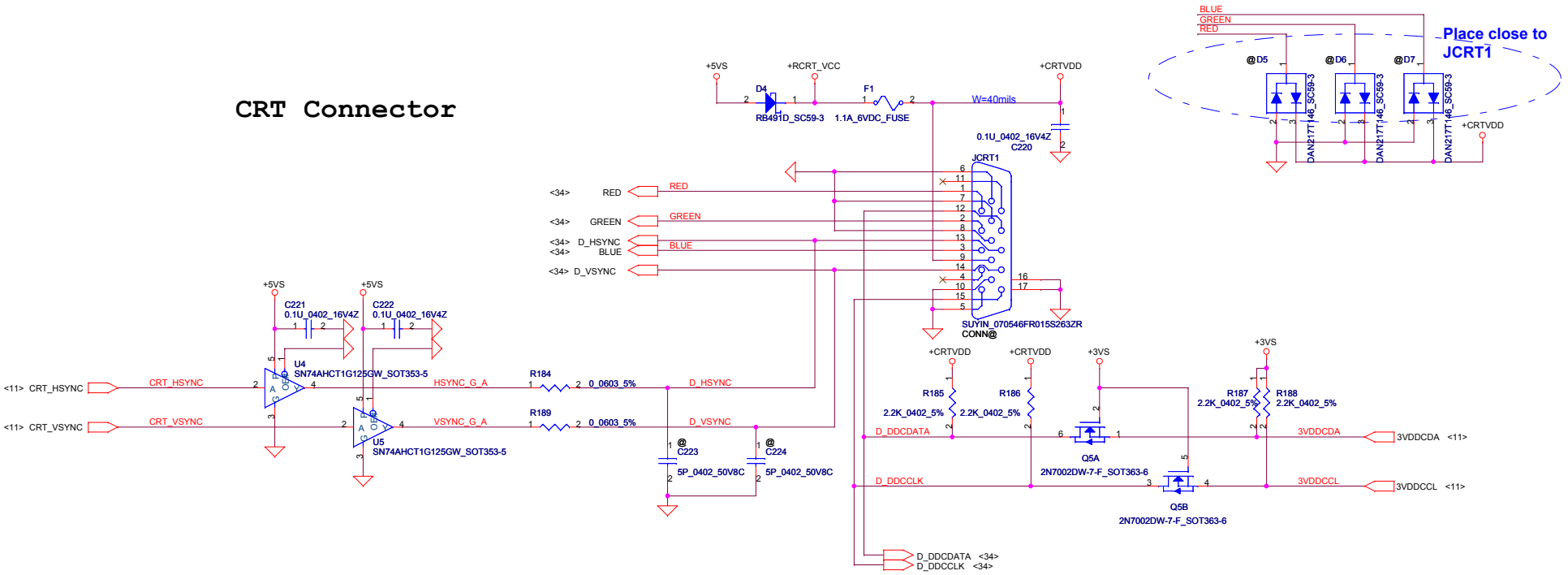
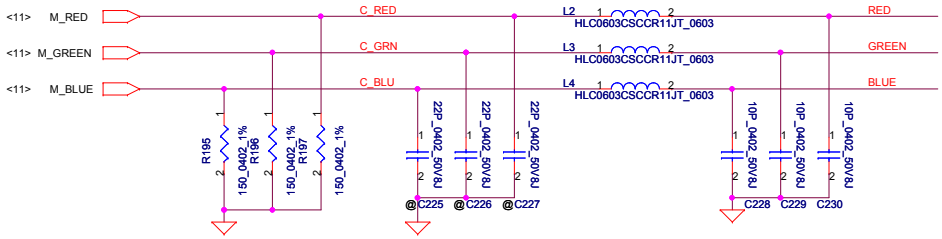
Date: Saturday, July 18, 2009 Sheet 17 of 45

CRT Connector



CRT Termination/EMI Filter

11/07 Change CRT lounting NB-->Docking-->CRT connector



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
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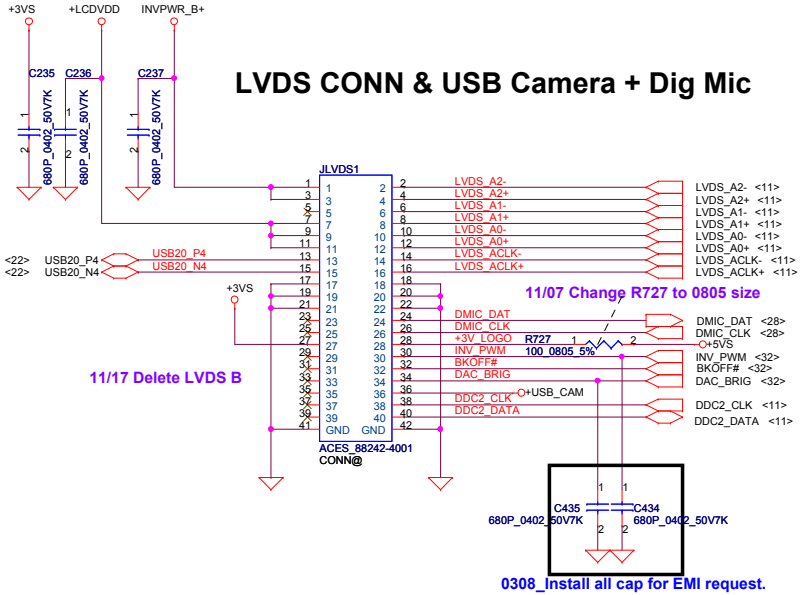
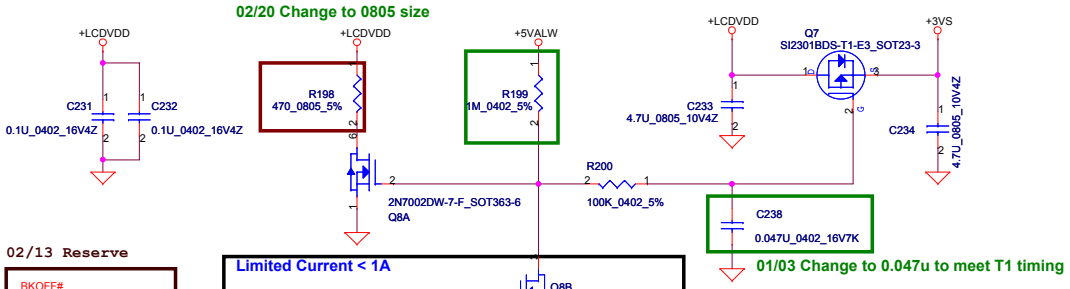
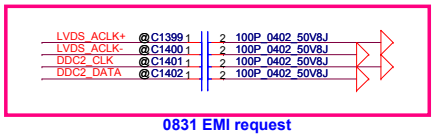
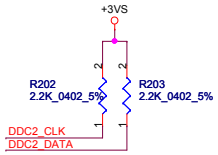
Date: Saturday, July 18, 2009 Sheet 18 of 45

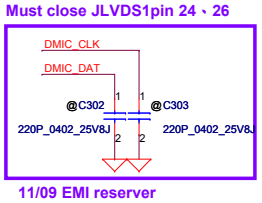
LVDS CONN & USB Camera + Dig Mic

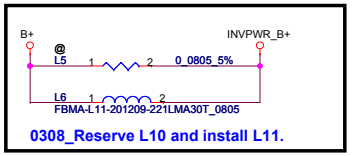




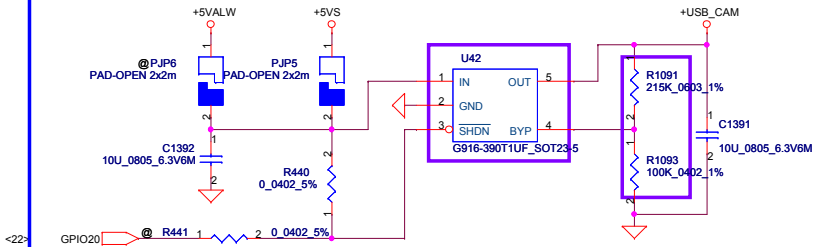






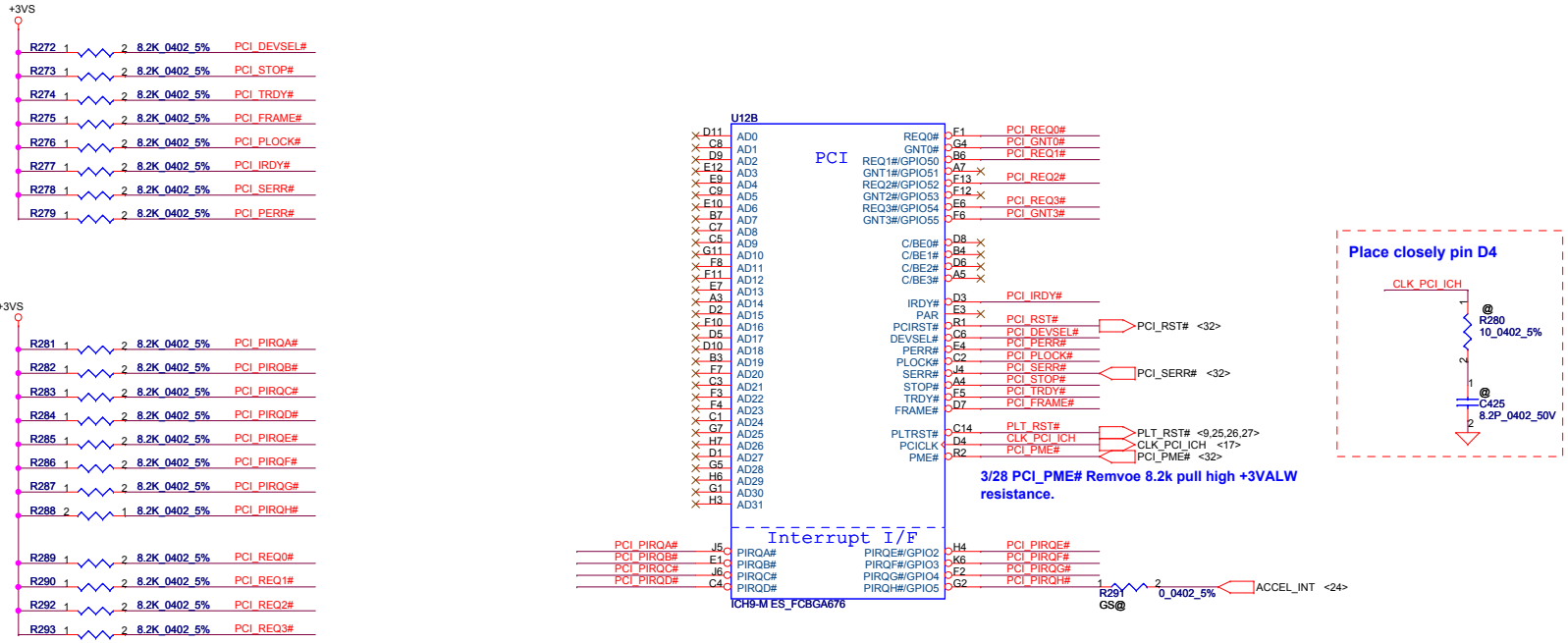


USB Camera



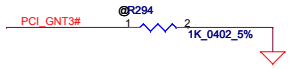
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: LCD CONN.			
Size	Document Number: Montevina Blade UMA LA4105P		Rev: 1.0
Date: Saturday, July 18, 2009	Sheet 19 of 45		



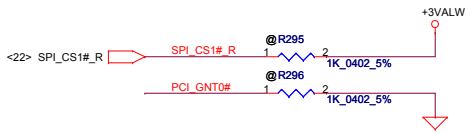
A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= ~~Default~~ *



Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	ICH9(1/4)-PCI/INT
Size	Document Number: Montevina Blade UMA LA4105P
Rev	1.0
Date: Saturday, July 18, 2009	Sheet 20 of 45

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

PV : follow check list ver:1.5 change to 8.2K ohm

U12A

ICH9-M ES_FCBGA676

P- HDD

ODD

e-SATA
De-feature disable

3/28 add 56ohm

within 2" from R379

placed within 2" from ICH9M

Within 500 mils

Add 12p on HDA_SDOUT and HDA_SDOUT

XOR CHAIN ENTRANCE STRAP:RSVD

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

03/18 Reserve SSC for EMI

02/13 Reserve cap on HDA_BITCLK for WWAN noise issue

0821 Change C436 and C437 to 15PF

@ CR2032 RTC BATTERY

Place near ICH9

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(2/4) LAN,HD,IDE,LPC

Size: Custom | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 21 of 45

04/29 MV-1 add R337 clock REQ pull high

11/09 Change Gsensor control from SB

Place closely pin AF3

Place closely pin H1

11/17 Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue

11/17 Swap PCIE LAN and New card

05/08 MV-1 Delete R739

R366 Low High ->No default boot

TV Tuner

WLAN

LAN

Card Reader

New Card

11/20 Add HDCP ROM for ICH9M

01/03 Change HDCP ROM to +3VS

Board ID

#PV PWROK sequence issue

Within 500 mils

USB-0 Right side

USB-1 Right side

USB-2 Left side(with ESATA)

USB-3 Dock

USB-4 Camera

USB-5 WLAN

USB-6 Bluetooth

USB-7 Finger Printer

USB-8 MiniCard(WWAN/TV)

USB-9 Express card

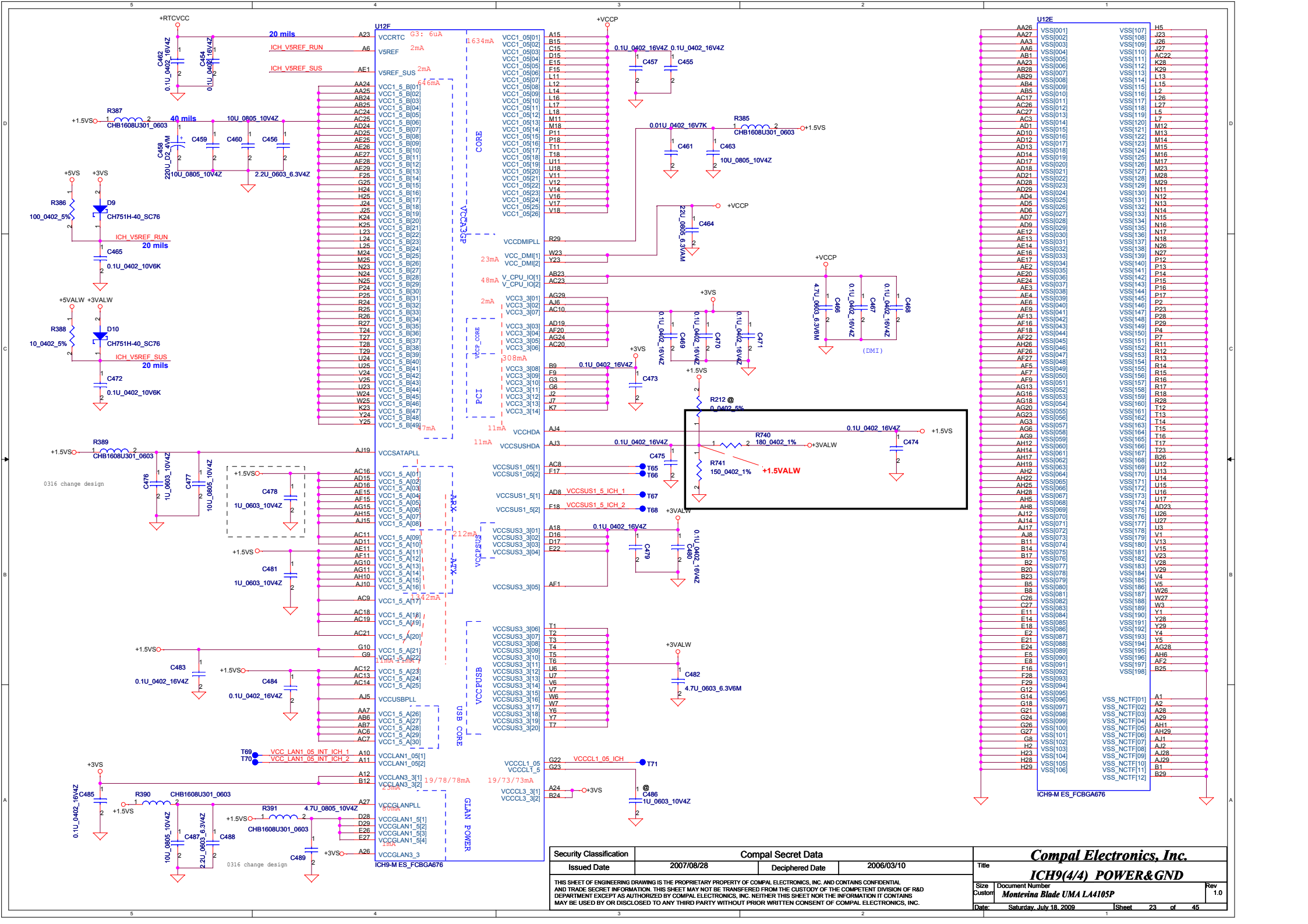
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(3/4) DMI,USB,GPIO,PCIE

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 22 of 45


U12F
ICH9-M ES_FCBGA676
U12E
ICH9-M ES_FCBGA676
CORE
VCCA3GP
PCI
VCCP_CORE
ATX
VCCPSUS
USB CORE
VCCPUSB
GLAN POWER
(DMI)
0316 change design
R212 @ 0_0402_5%
+1.5VALW
Security Classification
Compal Secret Data
Issued Date
2007/08/28
Deciphered Date
2006/03/10
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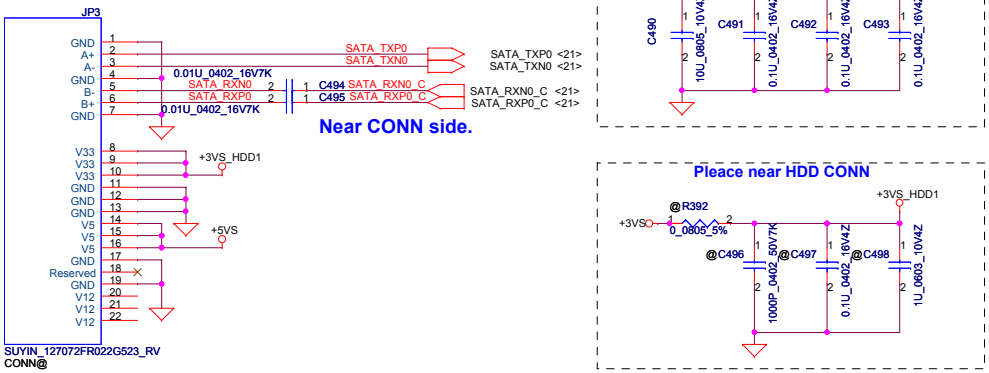
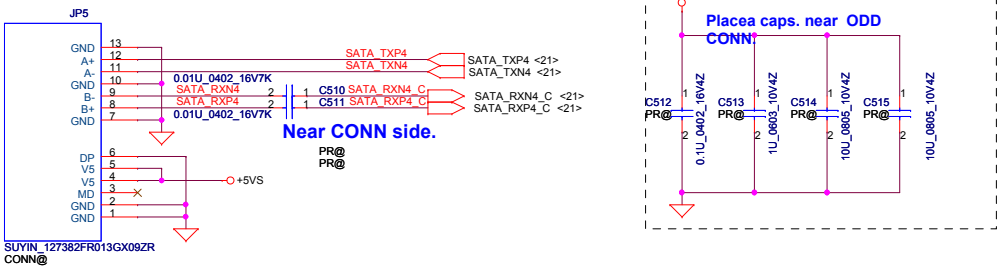
Compal Electronics, Inc.
Title
ICH9(4/4) POWER&GND
Size
Custom
Document Number
Montevina Blade UMA LA4105P
Rev
1.0
Date:
Saturday, July 18, 2009
Sheet
23
of
45

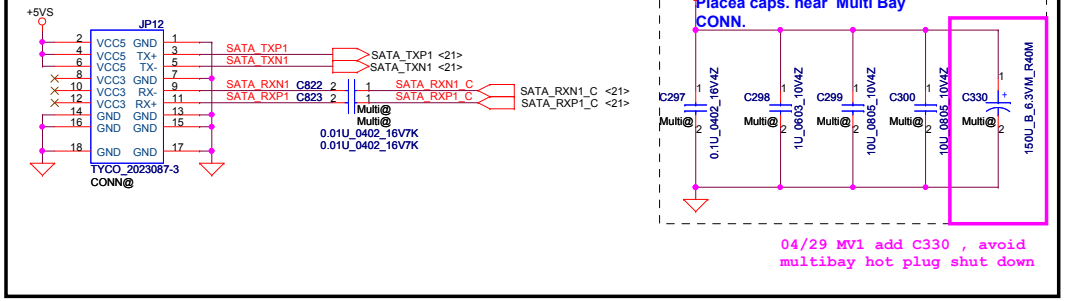
HDD Connector



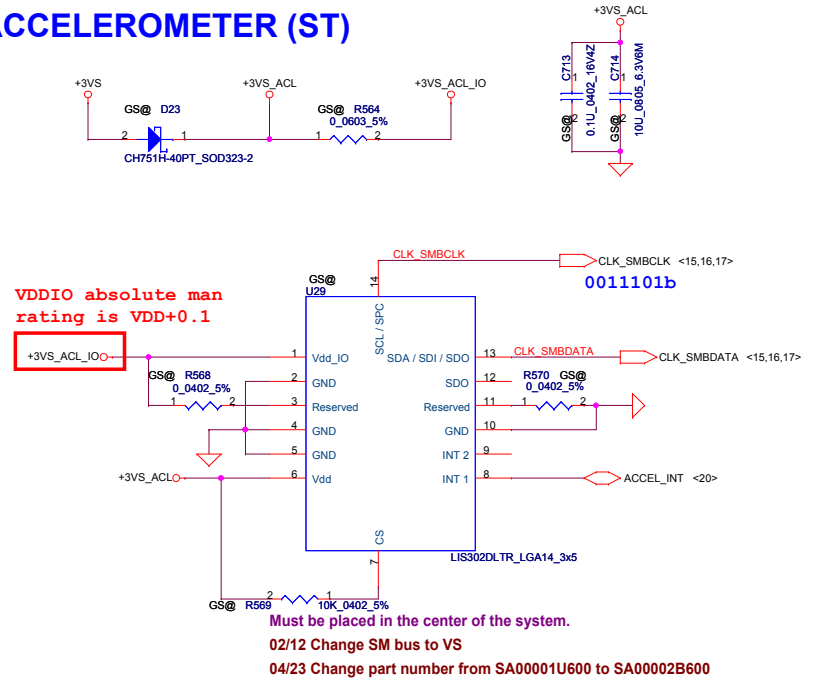
CD-ROM Connector



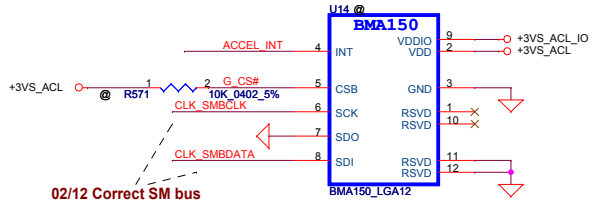
Multi Bay



ACCELEROMETER (ST)



ACCELEROMETER (Bosch)



ZZZ2
PCB-MB

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

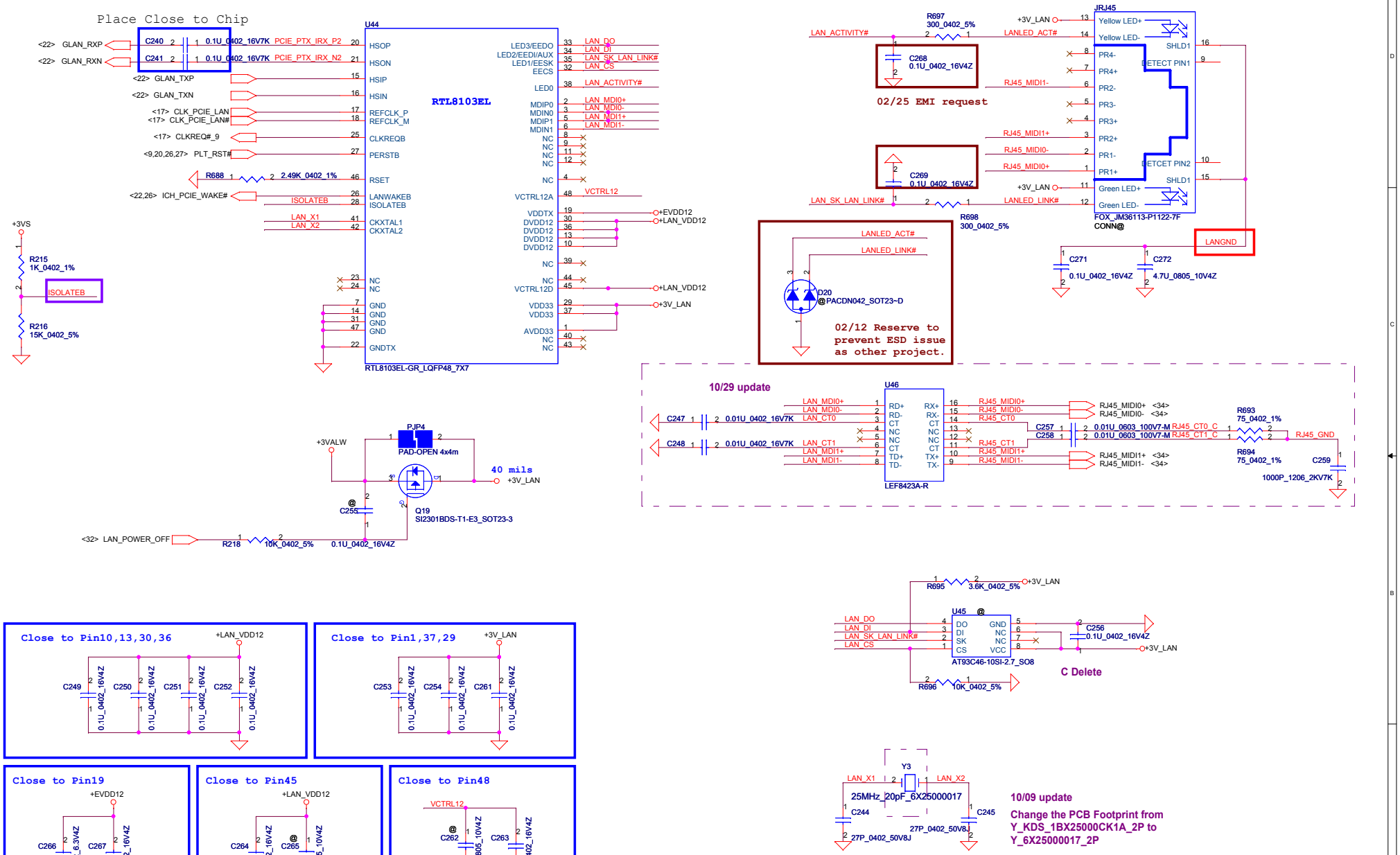
Compal Electronics, Inc.

Title: HDD & CDROM

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 24 of 45

LAN Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2007/06/30

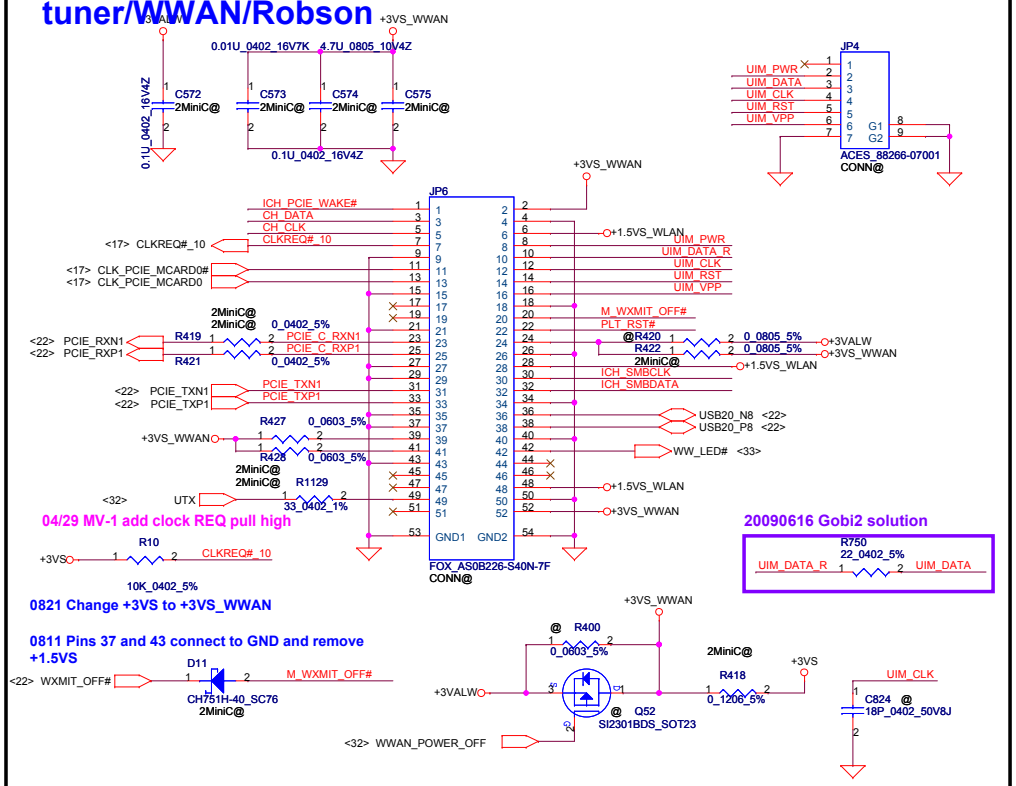
Compal Electronics, Inc.

Title: RTL8103EL LAN

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 25 of 45

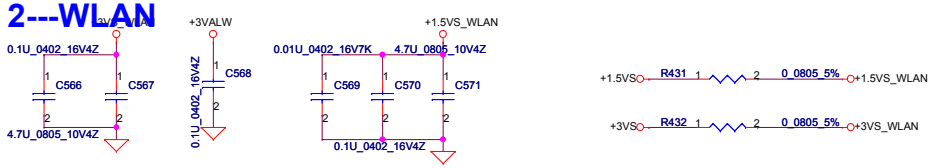
Mini Card 0--TV tuner/WWAN/Robson



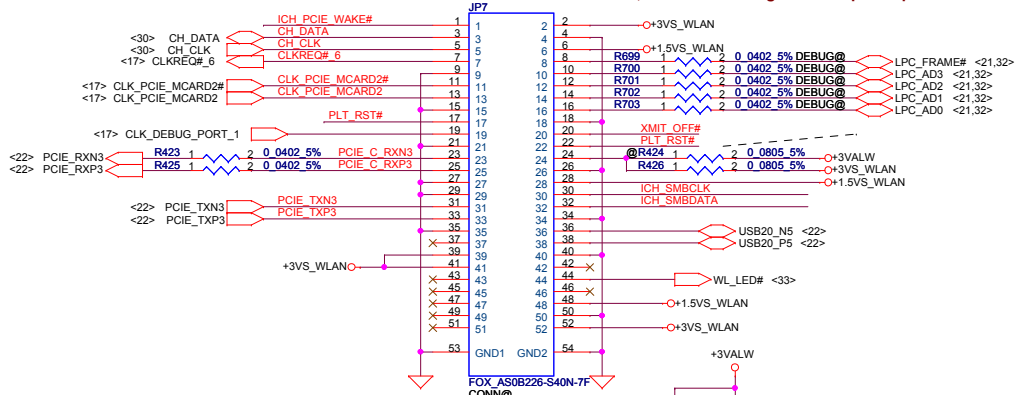
SIM card Connector

20090616 Gobi2 solution

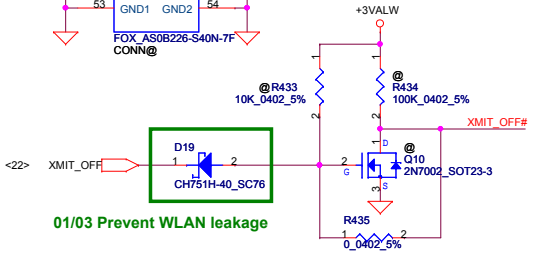
Mini Card 2---WLAN



02/13 Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane



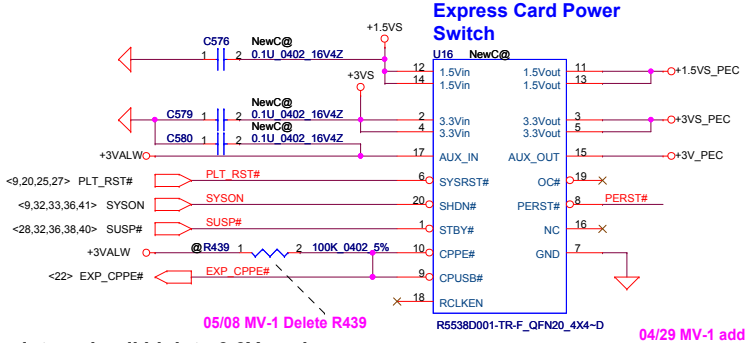
04/29 MV-1 add clock REQ pull high



01/03 Prevent WLAN leakage

New Card

Express Card Power Switch

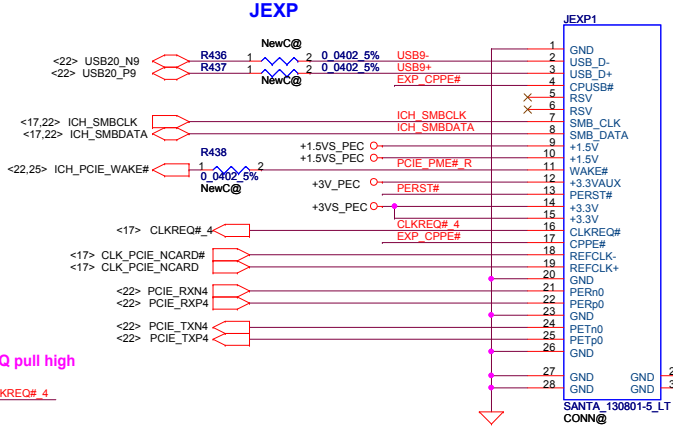


05/08 MV-1 Delete R439

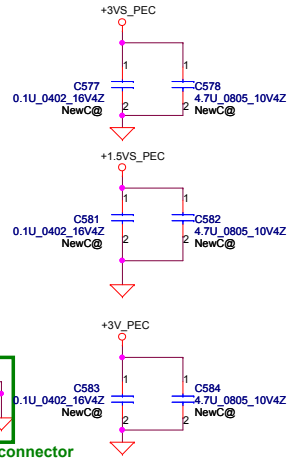
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

04/29 MV-1 add clock REQ pull high

Close to JEXP



Near to Express Card slot.



01/03 New card PTH connector

GND

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: WLAN, WWAN, New Card

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 26 of 45

09/26 (JMicron) recommend C1328/1000pF close to U36 pin5
09/26 (JMicron) recommend place C1329/0.1uF near by C1328
09/26 (JMicron) recommend (APVDD, 20 mil width, less than 120mil long)

11/07 Stuff for JMB385 internal LDO

Use 0603 type and over 20 mils trace width on both side

09/26 (JMicron) recommend change to 0805 Size

09/26 (JMicron) recommend +VCC_OUT >30mil

11/07 Change to 10K(vender)

01/03 Change Cardreader LED control

02/13 XD_ALE Change to LED low active

09/26 (JMicron) recommend width/length: 12mil / <250mil for PREXT signal (pin 7)

11/07 Change to 8.2K(vender)

09/26 (JMicron) recommend add a test point for pin 13、14

11/09 Reserve D18 for cardreader wake up

02/13 Add D18

use for PWR_EN#

8mA sink current

JMB385

JMB385-LGEZ0A_LQFP48_7X7

reserved power circuit

11/07 Change U37 correct PCBFootprint SOT23

11/07 BOM delete for JMB385 internal LDO

delete +1.8VS_CR R

White LED: VF=3V, IF = 5mA, Res = 56ohm

11/09 don't support DIM function

01/03 Change Cardreader LED control

02/13 Direct driver LED

Card Reader Connector

7 IN 1 CONN

TAITW_R015-B10-LM

CONN@

11/17 Update CIS library

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

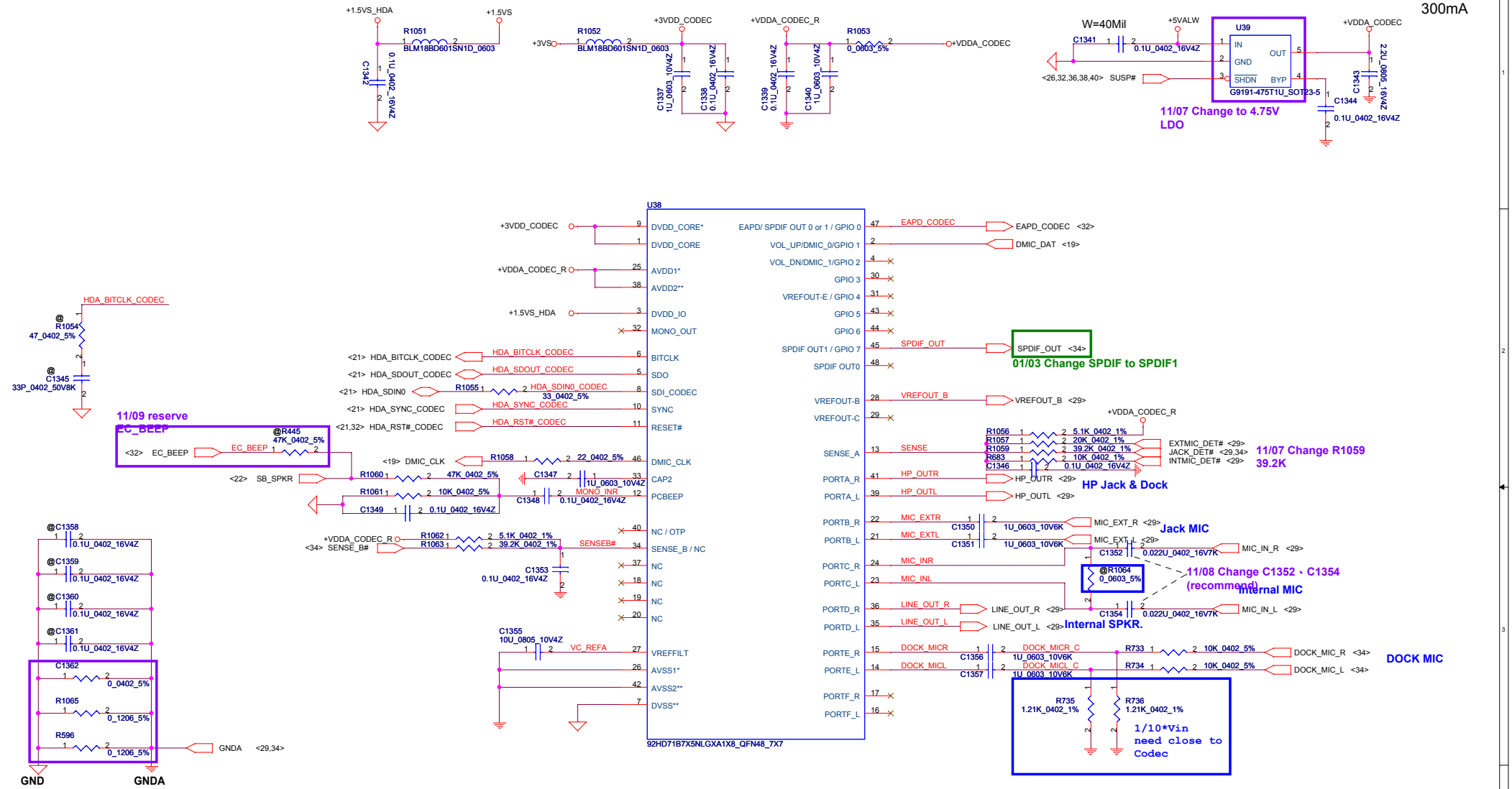
Title: USB CardReader&CONN

Size: Custom | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 27 of 45

CODEC POWER

(4.75V(4.56~4.94V))
300mA



SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	Codec_IDT9271B7		
Size: Custom	Document Number: Montevina Blade UMA LA4105P		Rev: 1.0
Date: Saturday, July 18, 2009	Sheet 28 of 45		

GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

11/17 Change to15.6 dB

15.6 dB

Keep 10 mil width

12/18 Shut down pop noise

11/07 Add 10K PU

04/29 MV-1 add 2 2N7002 for Docking issue

11/07Change JP60 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P

8/31EMI request

11/07 Add Capacitor avoid DC lever to Docking audio

Audio/B & CIR

HP OUT

HP OUT For Docking

HP OUT For M/B

EXTMIC IN

INTMIC IN

SPEAKER

TPA6017A2_TSSOP20

ACES_88231-04001 CONN@

ACES_87213-1400G CONN@

ACES_88018-124G

ACES_85231-04001 CONN@

MDC 1.5 Conn.

Connector for MDC Rev1.5

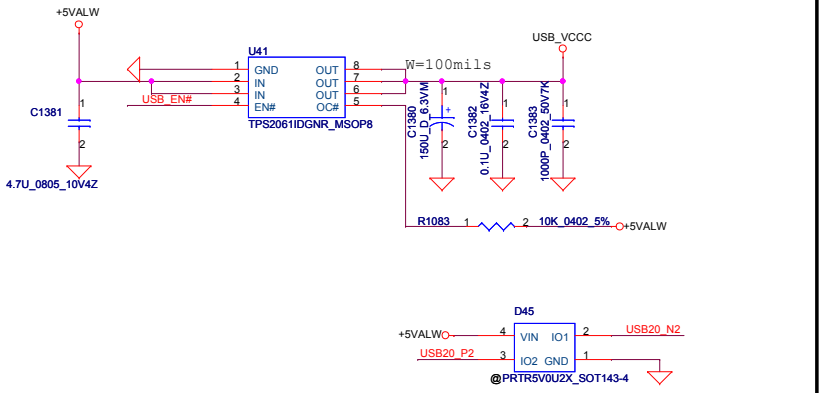
CONN@

MDC Standoff

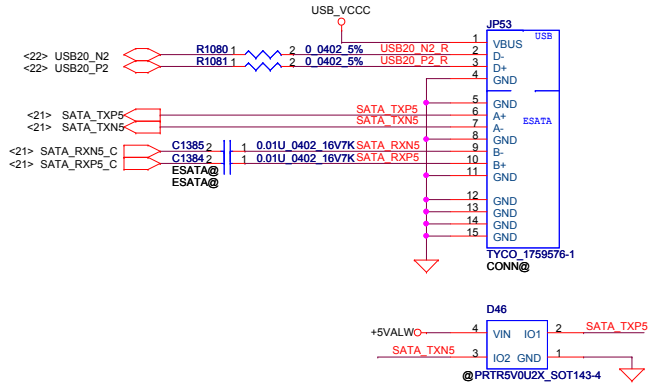
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size	Custom	Document Number	Montevina Blade UMA LA4105P
Rev	1.0		
Date:	Saturday, July 18, 2009	Sheet	29 of 45

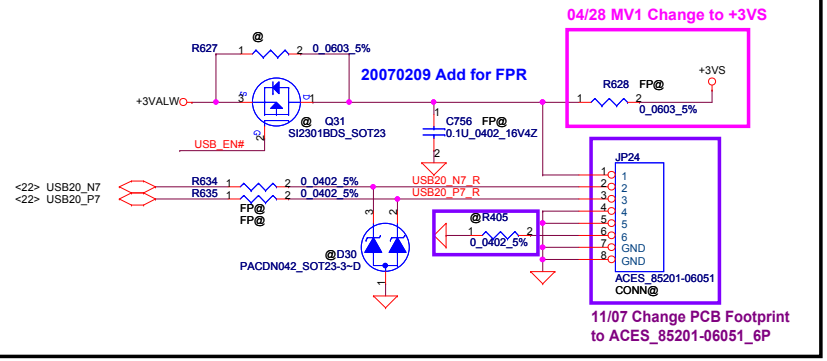
Left side USB Power Switch



Left side ESATA/USB combination Connector

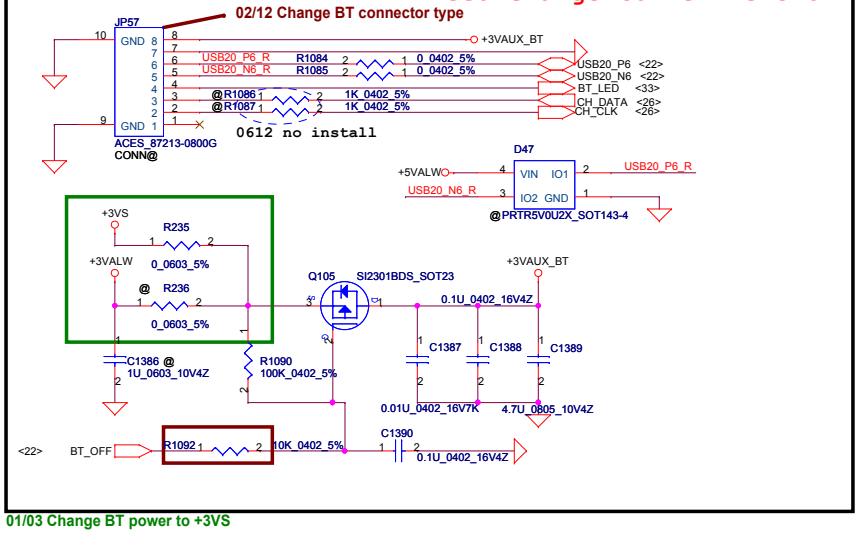


Finger printer



BT Connector

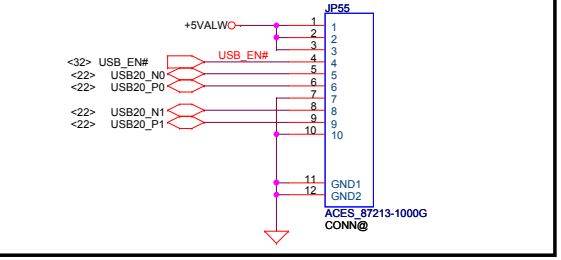
Need change to New version



01/03 Change BT power to +3VS

02/12 Change to 10K

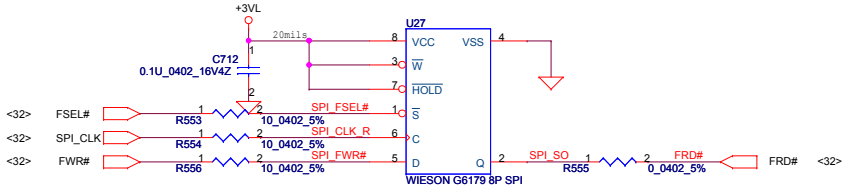
USB cable connector for Right side



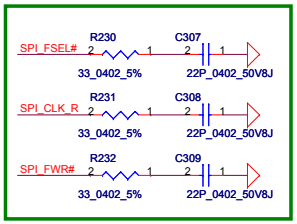
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size	Document Number: Montevina Blade UMA LA4105P		Rev: 1.0
Date: Saturday, July 18, 2009		Sheet 30 of 45	

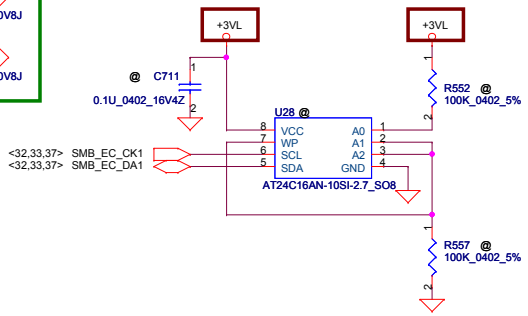
SPI ROM



SP07000F500 S SOCKET WIESON G6179-100000 8P
SPIFLASH
WIESO_G6179-100000_8P

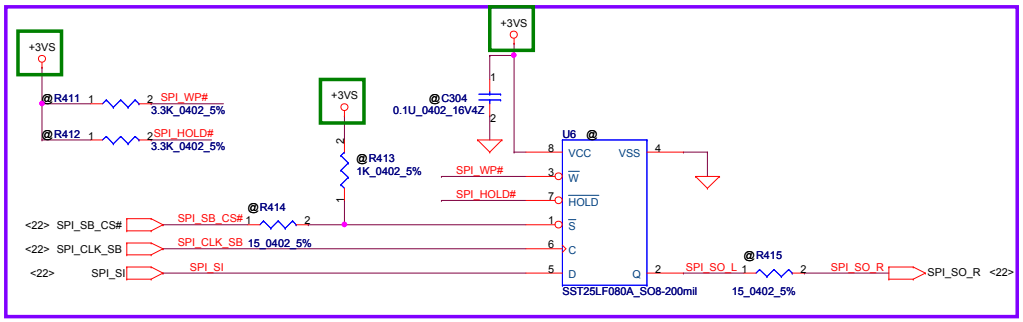


12/27EMI request



11/16 Change TO +3VALW
02/18 Change TO +3VL
02/18 Delete KBC EEPROM

HDCP ROM

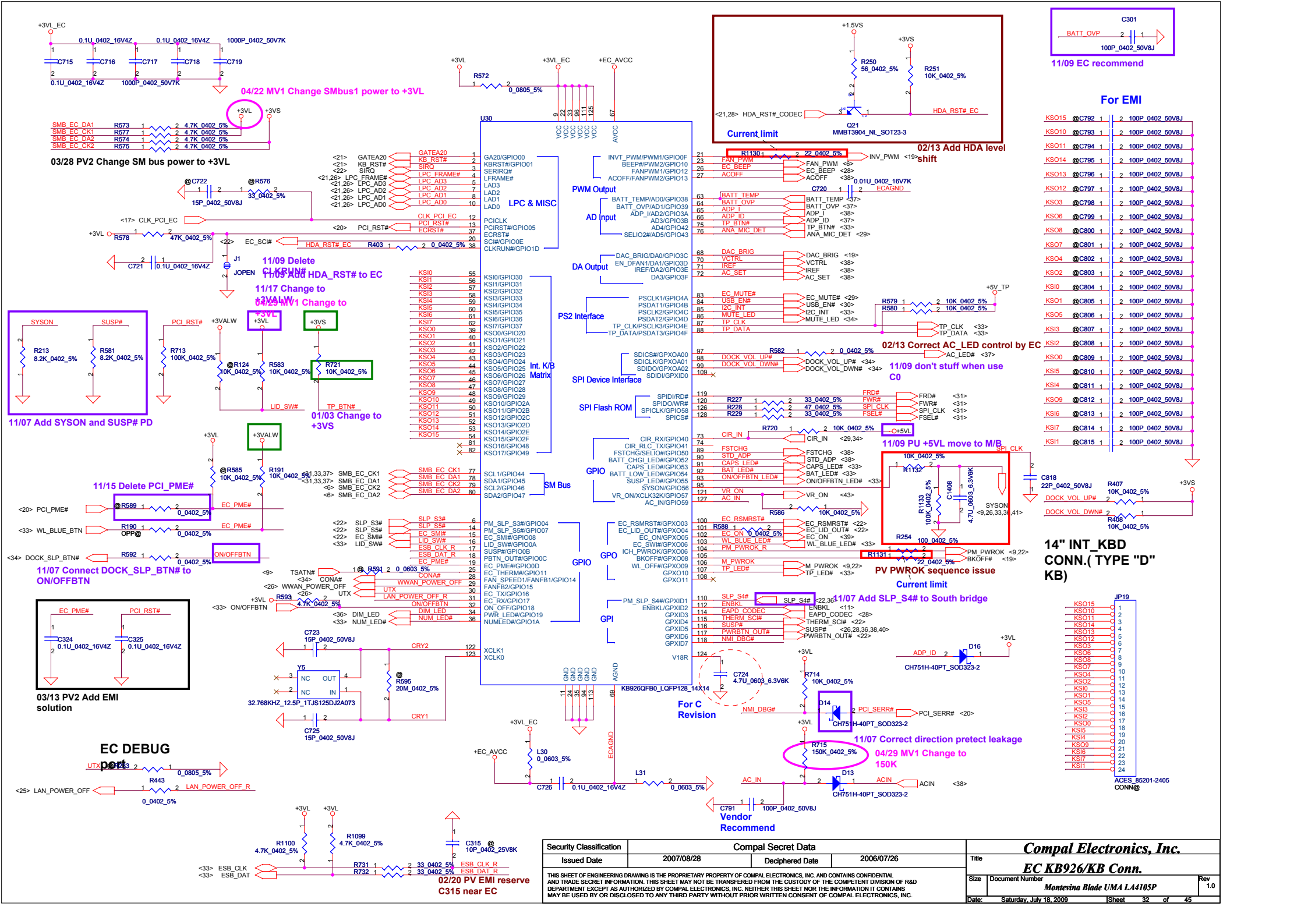


11/17 Add SB HDCP ROM
01/03 Change HDCP ROM to +3VS
02/13 Sparate SPI_CLK between SB and EC

Remove LPC Debug Port
20090618

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: BIOS ROM			
Size	Document Number: Montevina Blade UMA LA4105P		Rev: 1.0
Date: Saturday, July 18, 2009		Sheet 31 of 45	



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

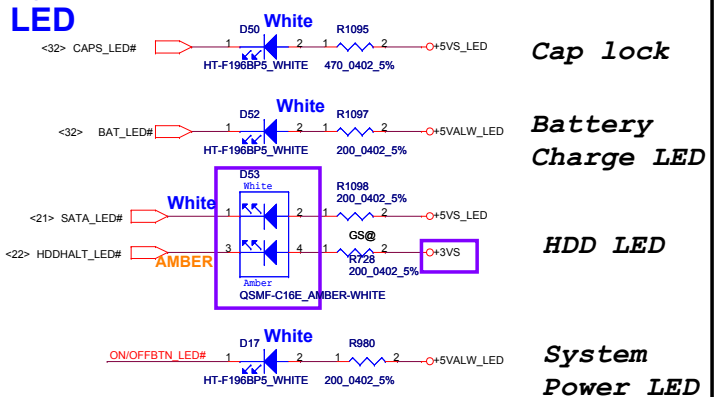
Compal Electronics, Inc.

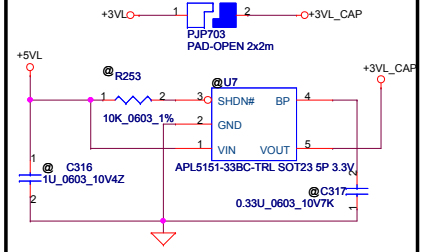
Title: **EC KB926/KB Conn.**

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 32 of 45

System LED





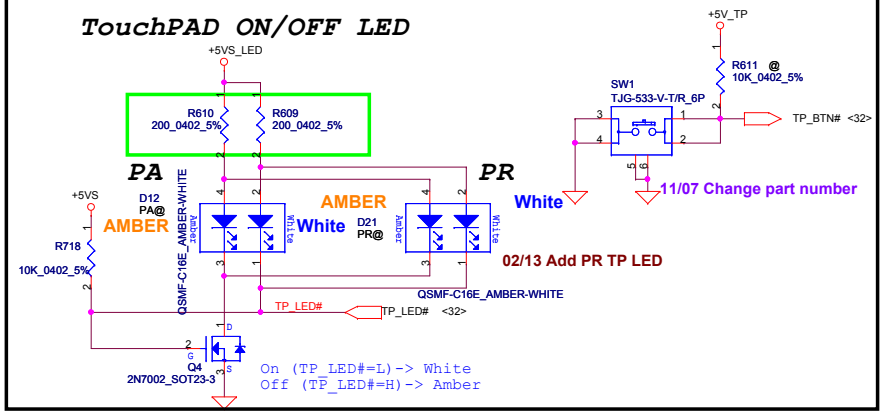
#PV reserve LDO for capacitor sensor board

03/28 PV2 Delete LDO

T/P Board (Inculde T/P_ON/OFF)

TouchPAD ON/OFF LED

TP ON/OFF

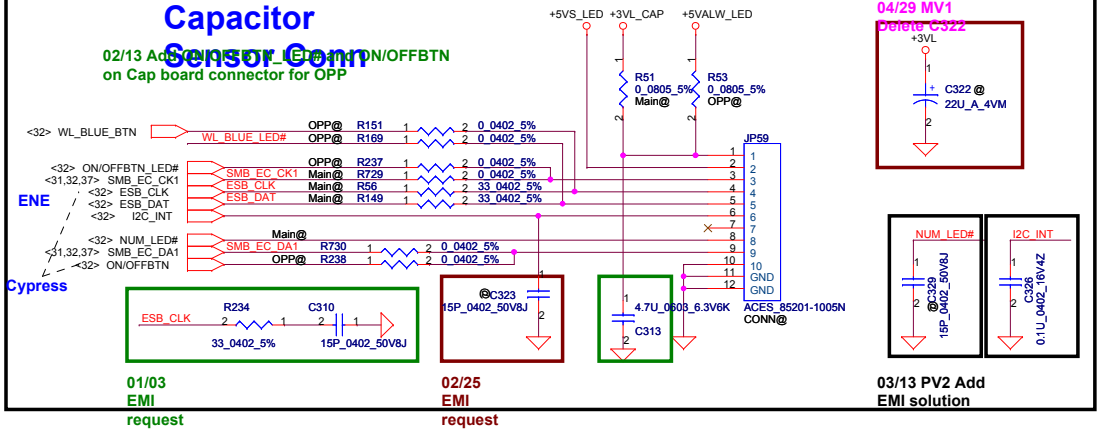


Capacitor Conn

02/13 Add [illegible] on ON/OFFBTN on Cap board connector for OPP

02/22 Add C on +3VL

04/29 MV1 Delete C322

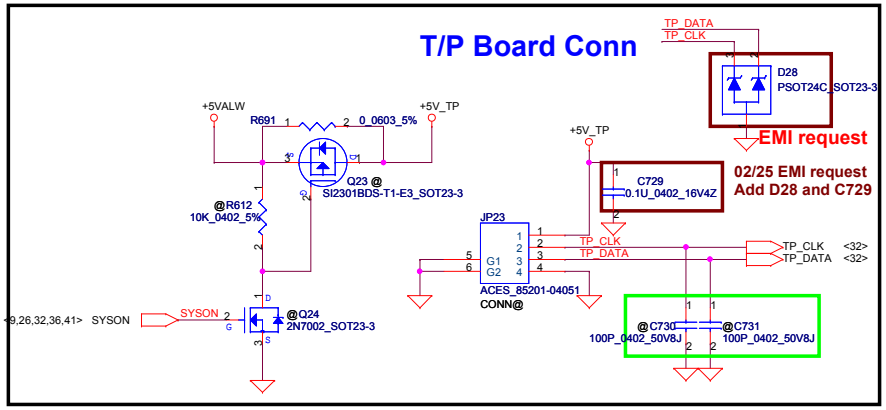


01/03 EMI request

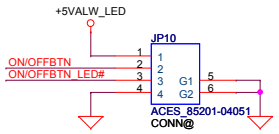
02/25 EMI request

03/13 PV2 Add EMI solution

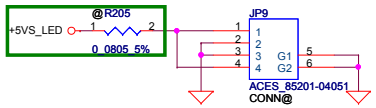
T/P Board Conn



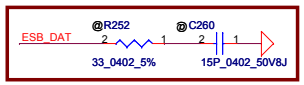
ON/OFF Button Connector



Keyboard backlight Conn

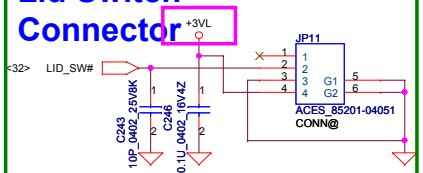


01/03 Keyboard backlight reserve a 0805 size resistor



02/20 EMI request

Lid Switch Connector



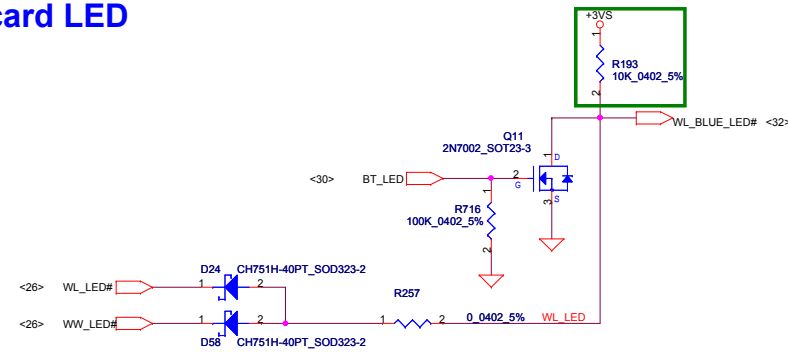
01/03 Change Lid switch connector type

02/18 Support Hall sensor module, move C243、C246 to M/B

03/18 Delete Lid switch pin 1

04/29 MV1 Change LID switch power to +3VL

Mini card LED



02/20 PV change to doide

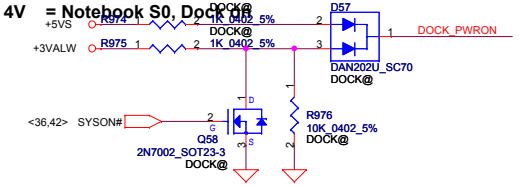
11/20 Reserve WW_LED function

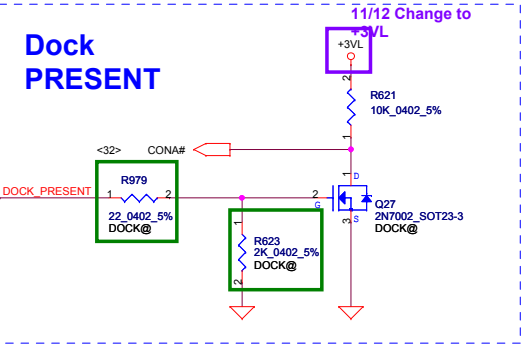
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

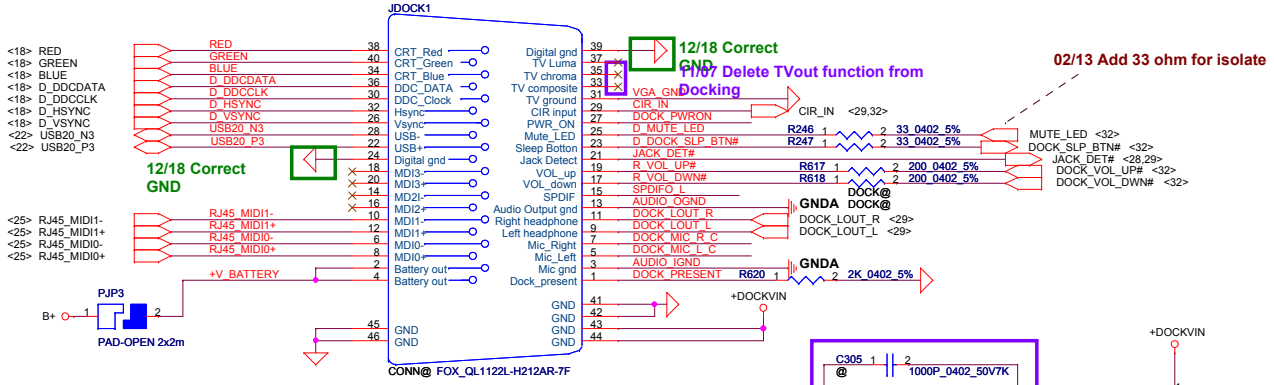
Compal Electronics, Inc.	
Title	KBD, ON/OFF, SW, CIR
Size	Document Number: Montevina Blade UMA LA4105P
Rev	1.0
Date: Saturday, July 18, 2009	Sheet 33 of 45

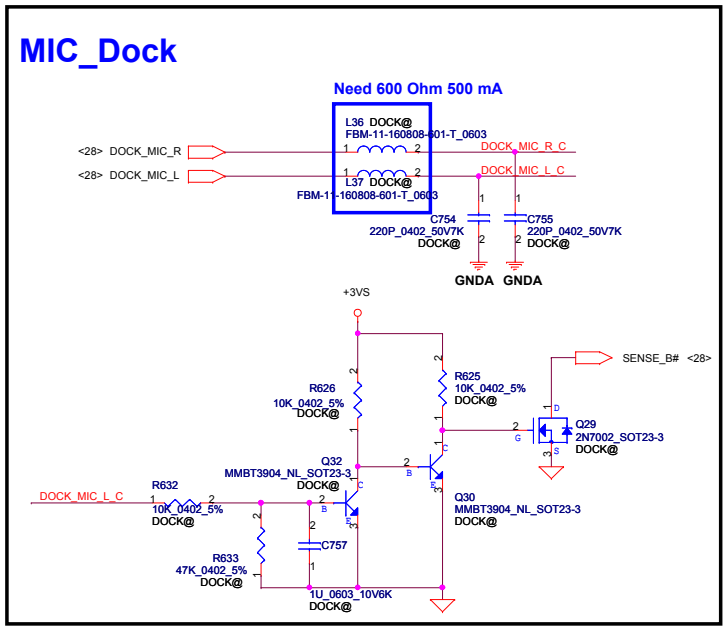
Atlas/ Saturn Dock

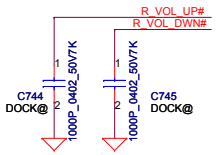
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

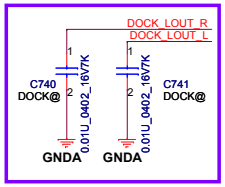


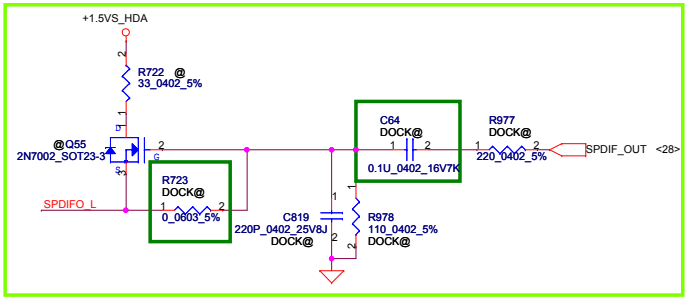












Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: DOCK CONN.

Size: Custom | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 34 of 45

EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommanded)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB

PV 02/20 follow datasheet

Follow Intel Feedback putting 2.2K ohm

11/07 Enable DDC_EN pin

PV 02/20 follow datasheet

Follow Vendor Feedback

11/07 correct TMDS_B_HPD# connection to North bridge

02/20 PV EMI request add C273、C314

HDMI Connector

Vendor suggests 4K PU
11/07 Follow recommend change to 3.9K

01/03 Reserver 0 ohm co lay with common choke

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

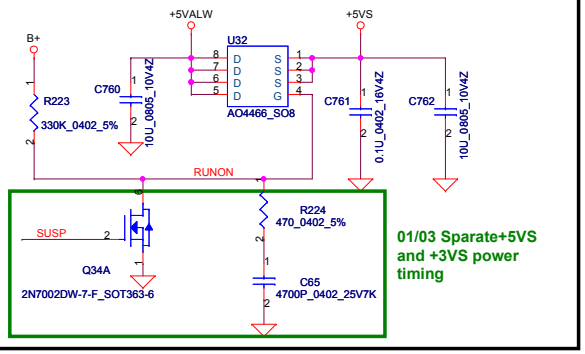
Compal Electronics, Inc.

Title: HDMI LS & Conn.

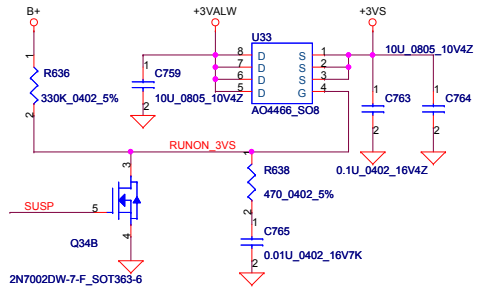
Size: Custom | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 35 of 45

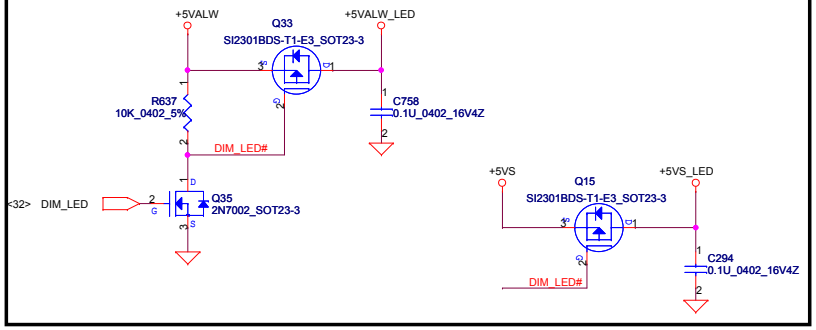
+5VALW to +5VS Transfer



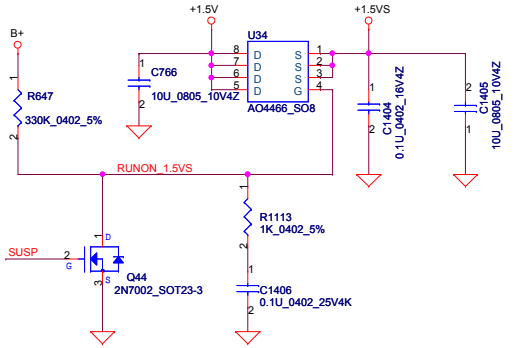
+3VALW to +3VS Transfer

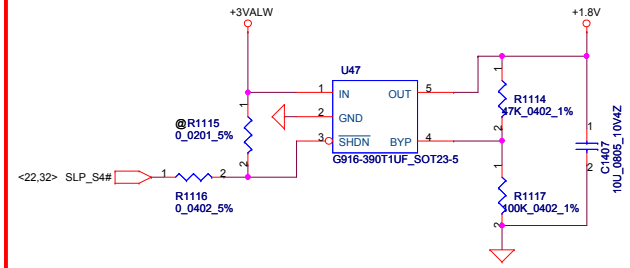


DIM LED

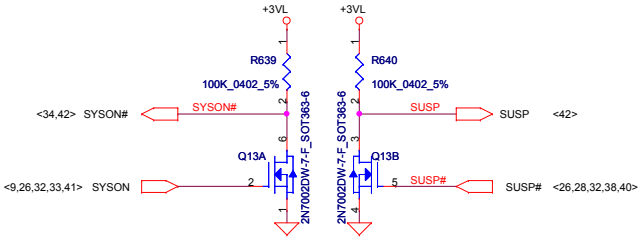


+1.5V to +1.5VS Transfer

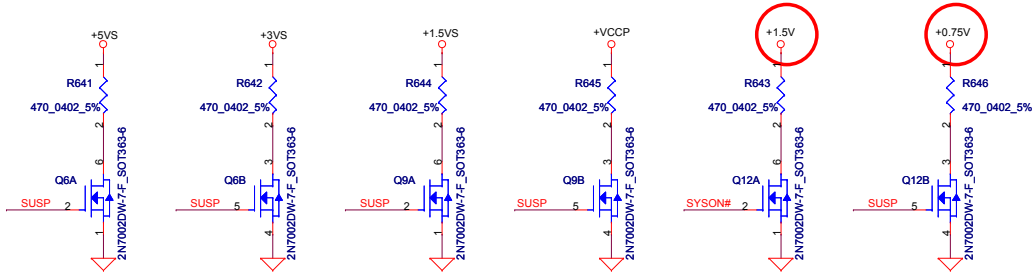


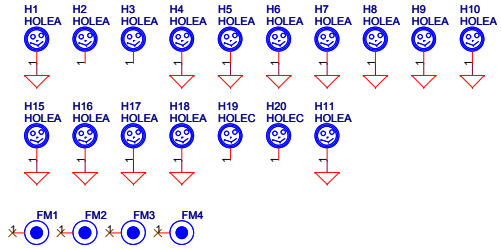


VOUT=1.25(1+R912/R913)
VOUT=1.25(1+100k/215k)=1.83V



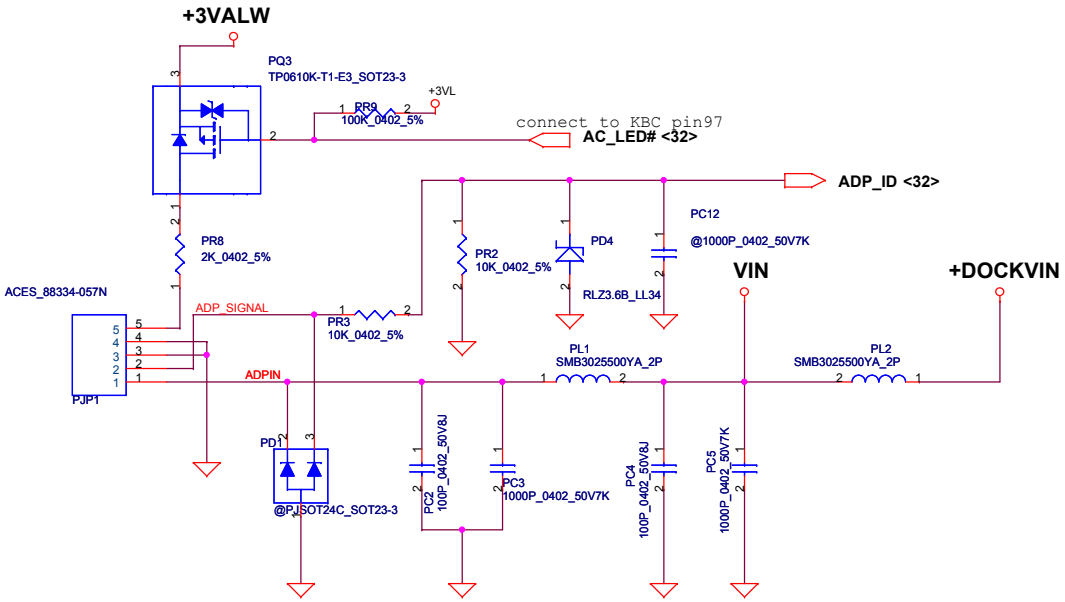
Discharge circuit

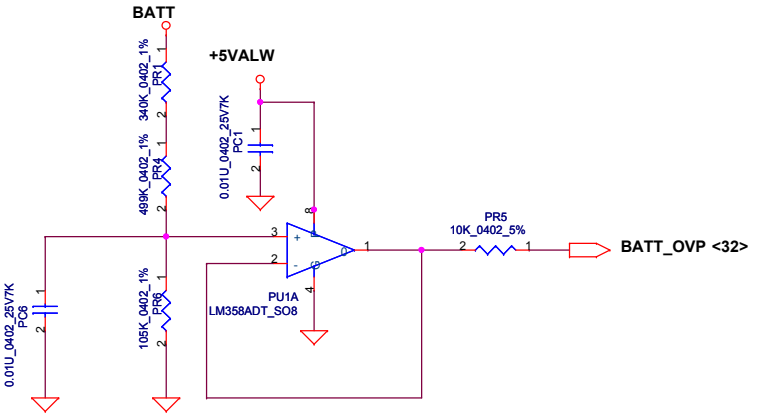


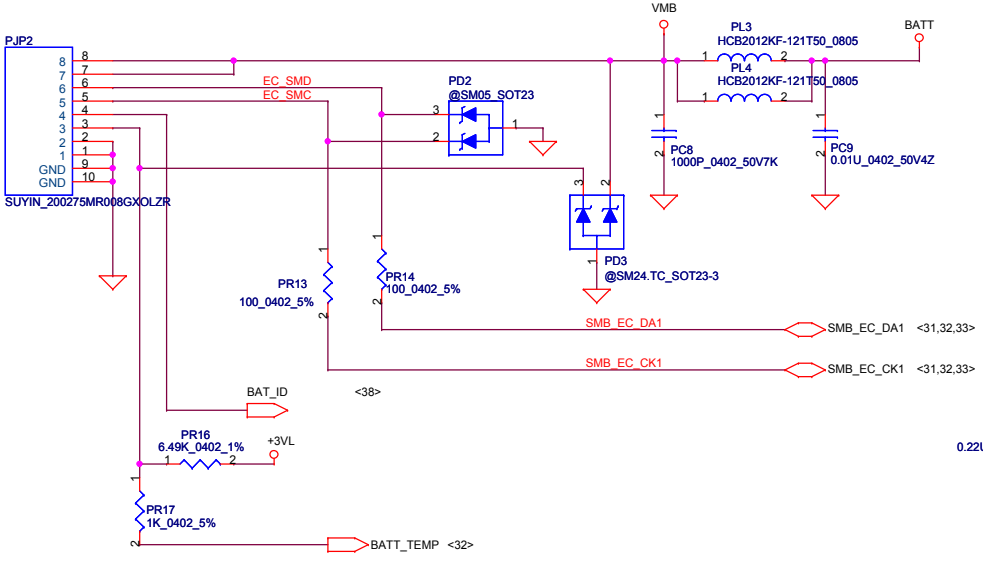


Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

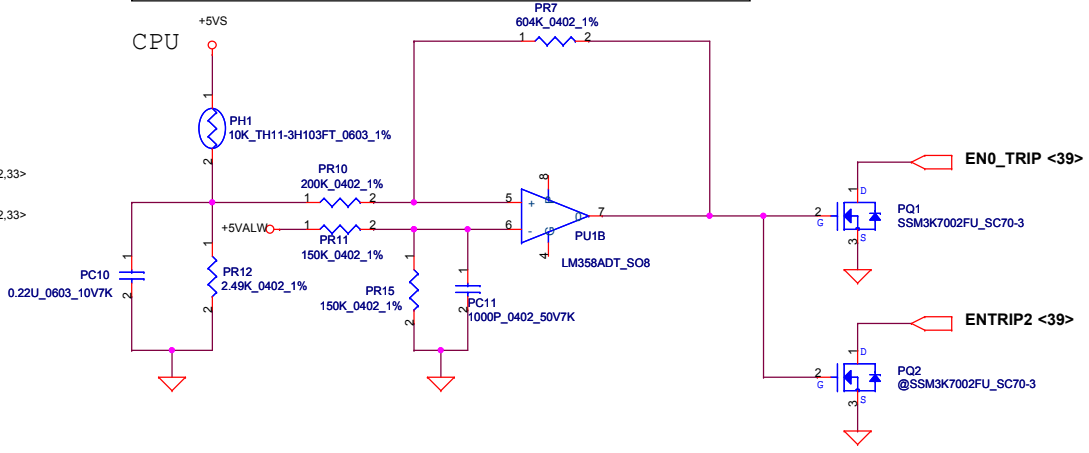
Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: Montevina Blade UMA LA4105P		Rev: 1.0
Date: Saturday, July 18, 2009		Sheet 36 of 45	





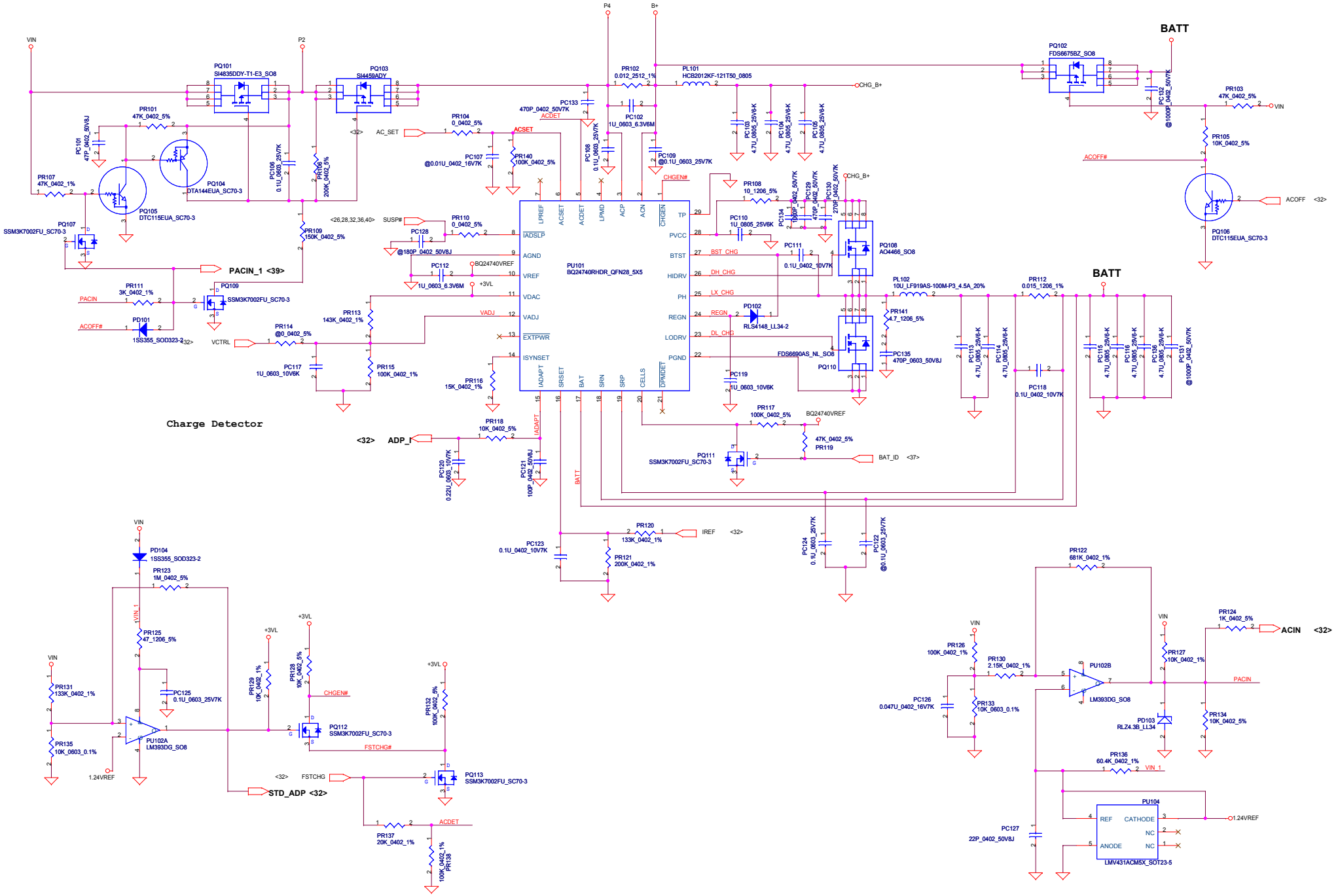


PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title	DC Connector/CPU_OTP		
Size	Document Number	Montevina Blade UMA LA4105P	Rev 1.0
Date: Saturday, July 18, 2009	Sheet 37 of 45		



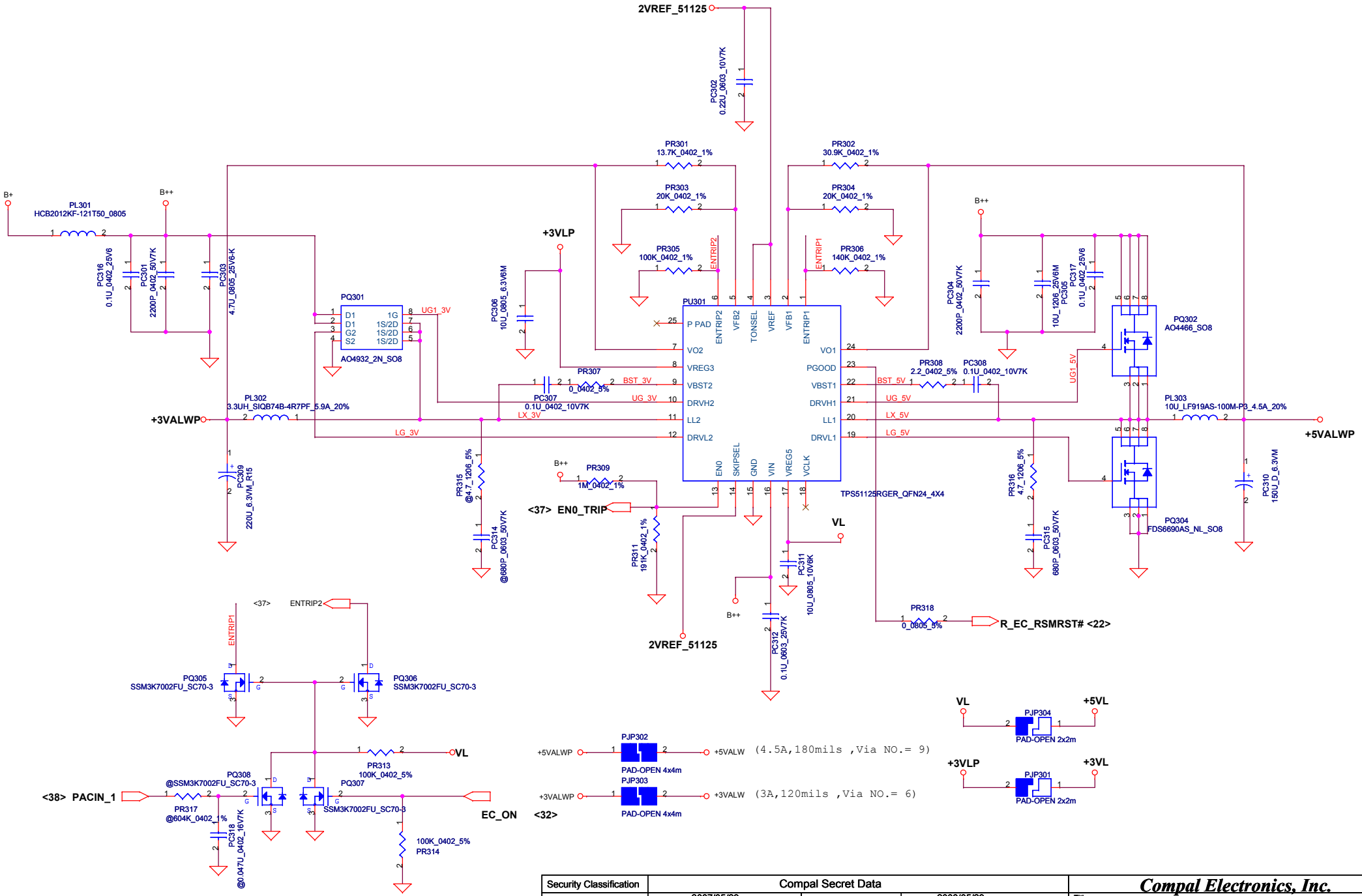
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 | Sheet 38 of 45



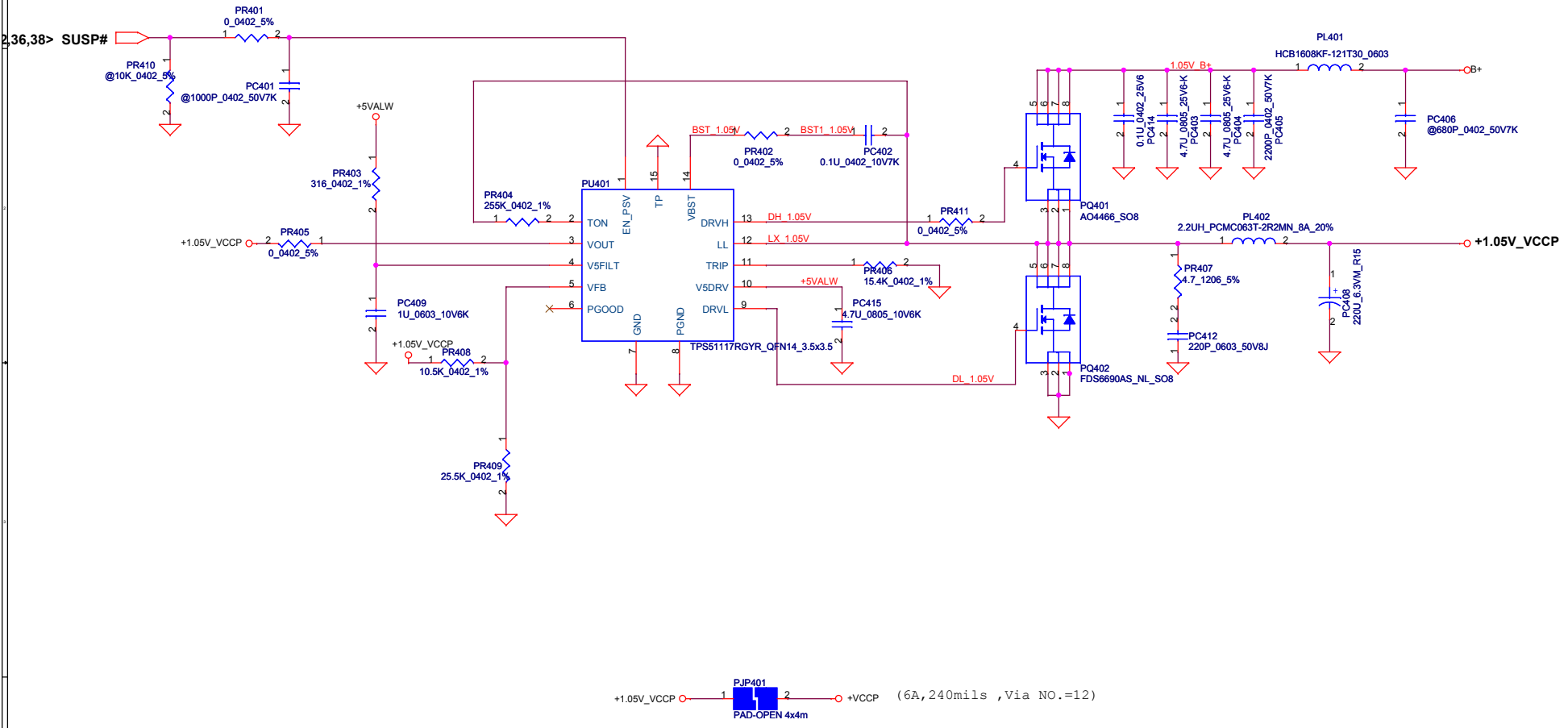
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 Sheet 39 of 45



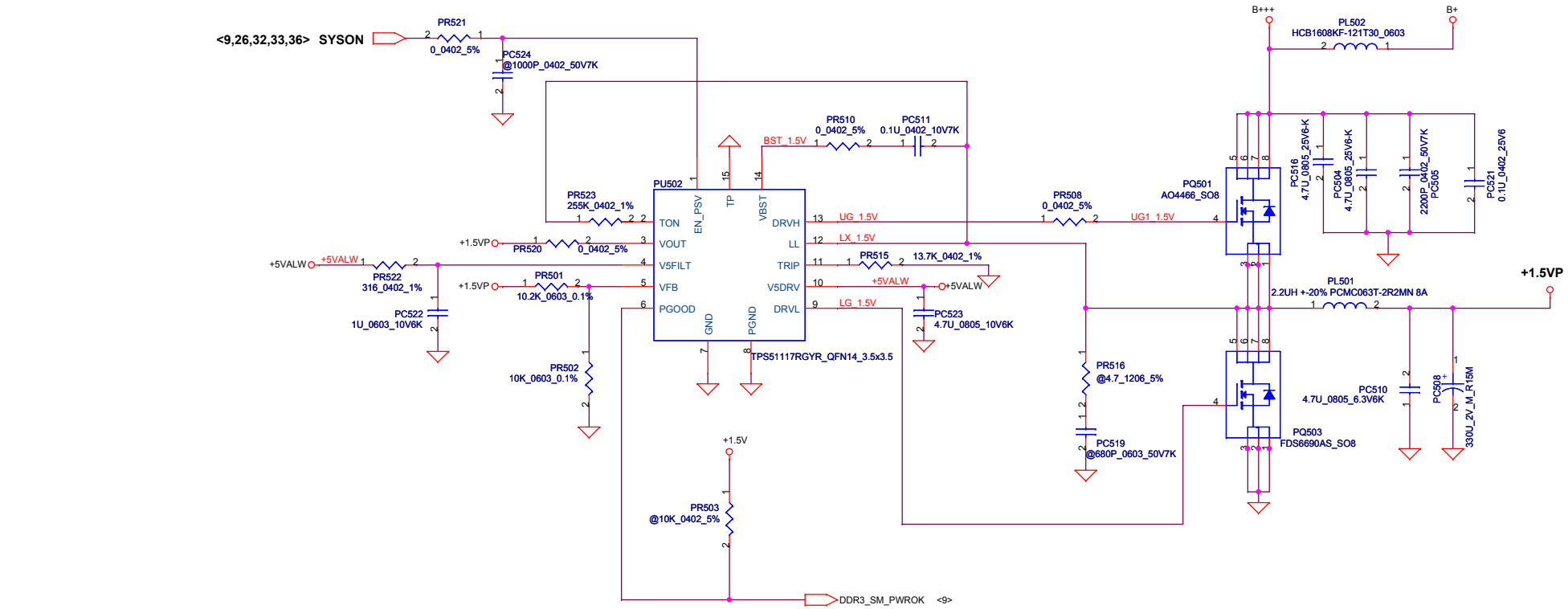
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: *1.05V_VCCP*

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 | Sheet 40 of 45



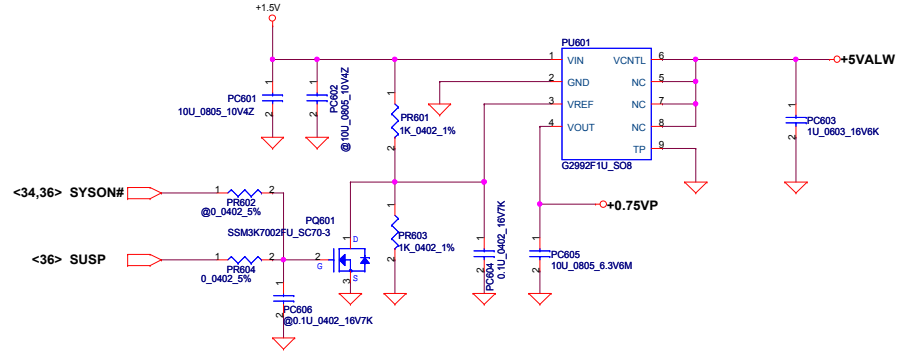
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VP**

Size	Document Number	Rev
	Montevina Blade UMA LA4105P	1.0

Date: Saturday, July 18, 2009 | Sheet 41 of 45



(2A,80mils ,Via NO.= 4)

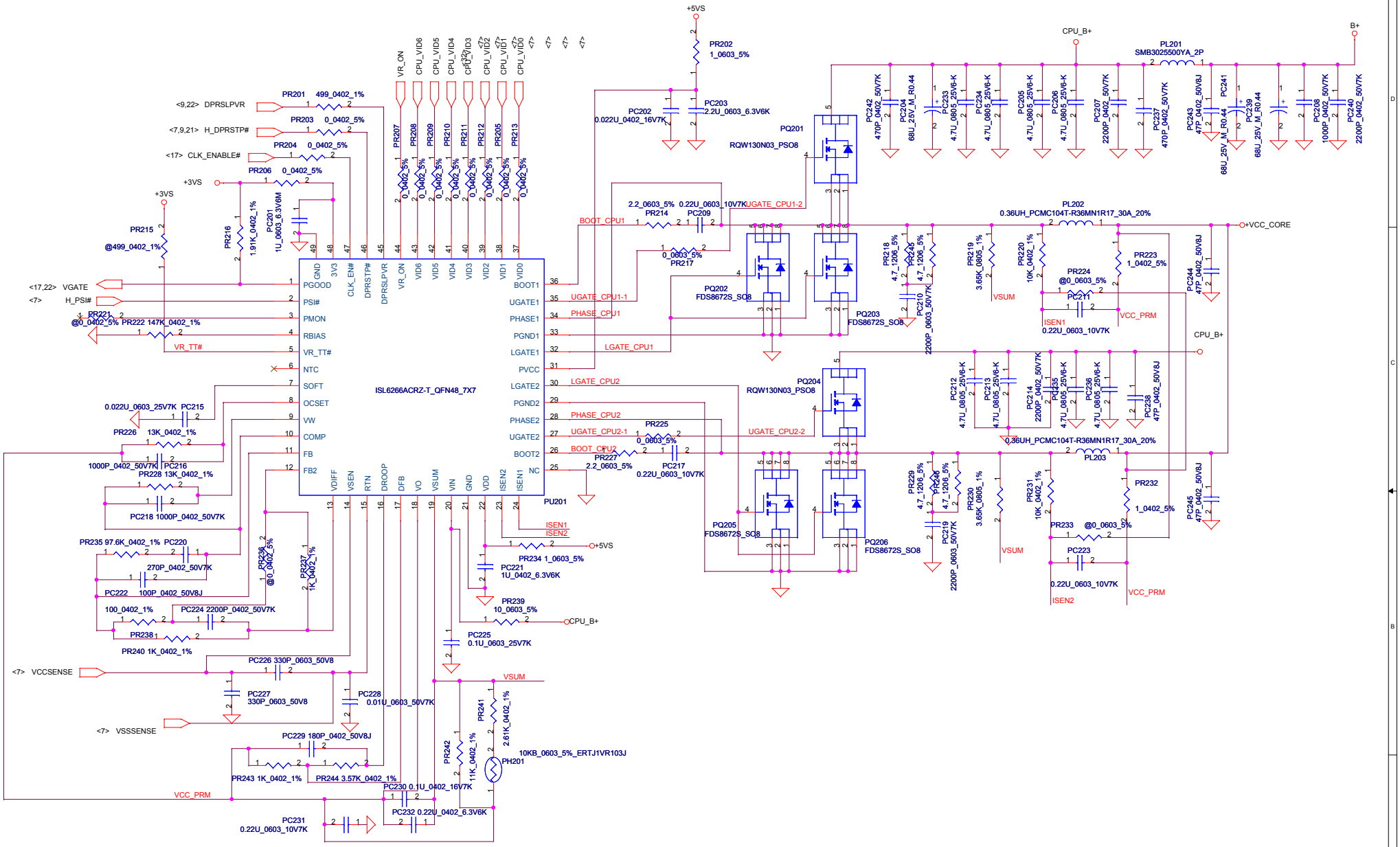
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: 0.75VP

Size | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 42 of 45



Compal Electronics, Inc.	
Title	+CPU_CORE
Size: Custom	Document Number:
Rev	1.0
Date: Saturday, July 18, 2009	Sheet 43 of 45

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	3.3VALWP/5VALWP	5/4	Compal	RF solution	Add PC316, PC317	
2	40	+1.05V_VCCP	5/4	Compal	RF solution	Add PC414	
3	41	+1.5VP	5/4	Compal	RF solution	Add PC521	

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
85	DDR2 change to DDR3	09	V_DDR_MCH_REF change to +1.5V	03/31	1.4DB
86	DDR2 change to DDR3	09	SMRCOMP_VOH change to +1.5V	03/31	1.4DB
87	DDR2 change to DDR3	09	SMRCOMP change to +1.5V	03/31	1.4DB
88	DDR2 change to DDR3	09、41	Add AND gate (U48) and R1119~R1120, C1408 for SM_RWOK	03/31	1.4DB
89	DDR2 change to DDR3	12	VCC_SM_CK change to +1.5V	03/31	1.4DB
90	DDR2 change to DDR3	13	VCC_SM change to +1.5V	03/31	1.4DB
91	DDR2 change to DDR3	15、16	Change to DDR3 SODIMM	03/31	1.4DB
92	DDR2 change to DDR3	36	Delete reserve +1.8V DC-DC, and add +1.5V DC-DC	03/31	1.4DB
93	DDR2 change to DDR3	36	Add LDO for +1.8V_LVDS	03/31	1.4DB
94	DDR2 change to DDR3	27	delete +1.8VS_CR, card reader internal LDO can provide +1.8VS	03/31	1.4DB
	Gobi RF test and UTX for debug card.	26	modify R750 netname trace, add R1129 for UTX.	06/19	1.4PVR
	EMI solution for ENE cap. board.	32	modify R731 and R732 to 33 ohm. BOM change.	06/19	1.4PVR
	EMI solution for ENE cap. board.	33	modify R234 ,R56 and R149 to 33 ohm , C310 to 15pF. BOM change.	06/19	1.4PVR

Compal Electronics, Inc.

Title: HW PIR 3

Size | Document Number: Montevina Blade UMA LA4105P | Rev: 1.0

Date: Saturday, July 18, 2009 | Sheet 45 of 45