Compal Confidential

JAQ10 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2008-04-21

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

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Montevina Commercial UMA

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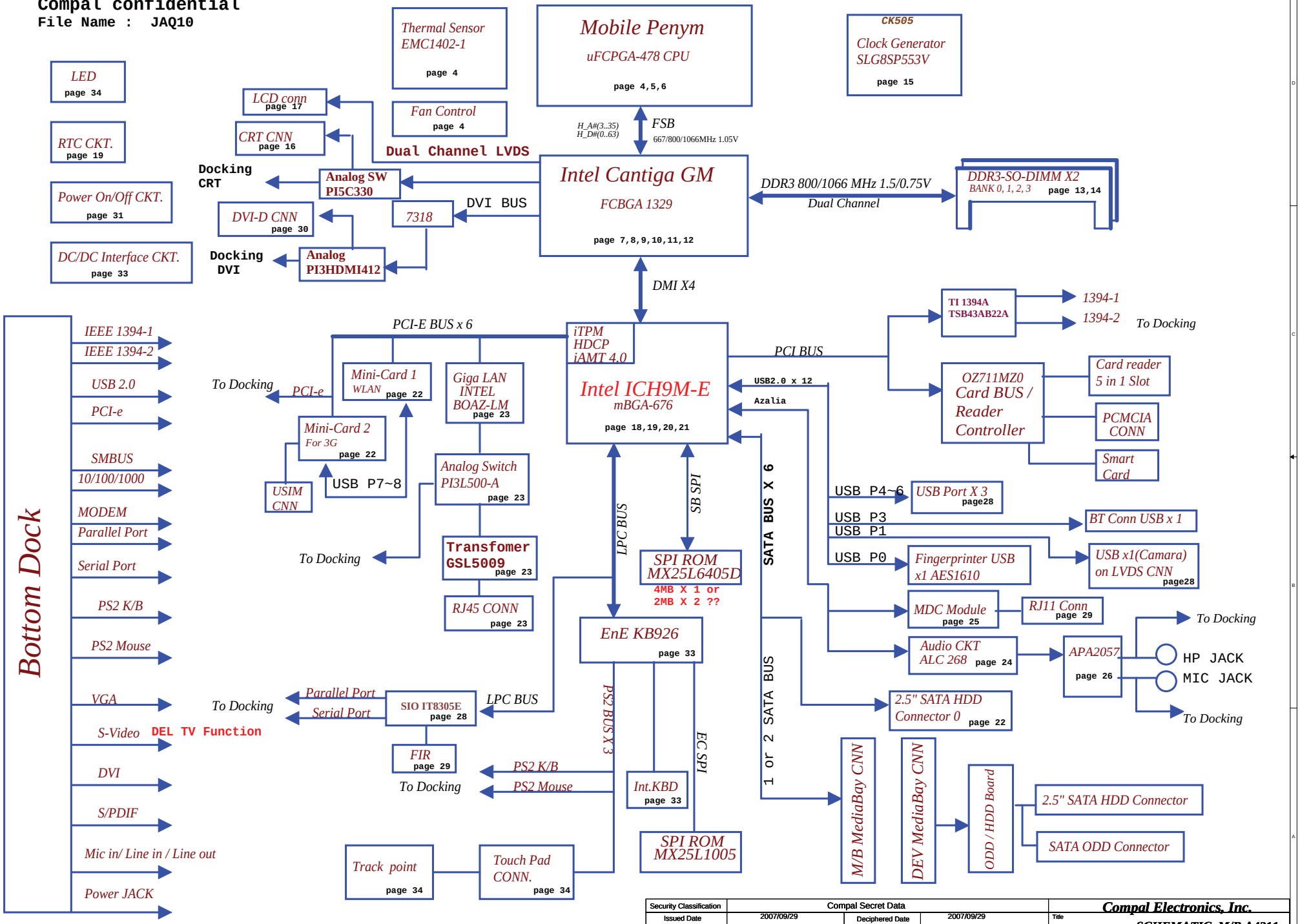

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Voltage Rails

Power Plane	Description	S1	S3/M1	S5/M1
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF/ON	OFF/ON
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.05VM	1.05VM switched power rail	ON	OFF/ON	OFF/ON
+1.5V	1.5V power rail for HDA	ON	ON	OFF/ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	OFF/ON	OFF/ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394 TI	AD21	3	PIRQ-F
PCMCIA + Card Reader + Small Card	AD22	2	PIRQ-E

External PCI-e Devices

Device	PORT NO.	Interrupts
MINI CARD1 WLAN	P1	??
MINI CARD2 3G	P2	??
DOCKING PCI-E	P5	??
INTEL GIGA LAN	P6	??

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
GMT G781-1	1001 101X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
HDMI Analog S/W	1100 000Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
CIR	CIR@
8111C	8111C@
8102E	8102E@
ALC888VC	888VC@
ALC888VB	888VB@
ALC268	268@

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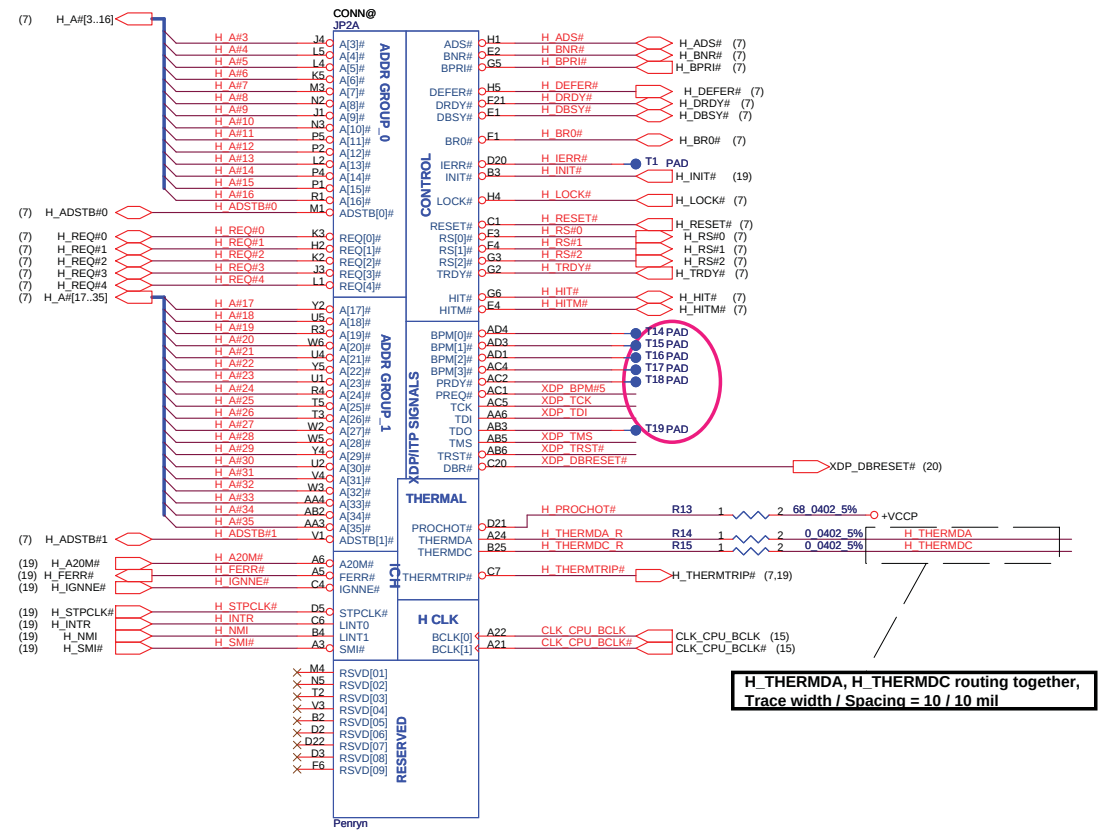
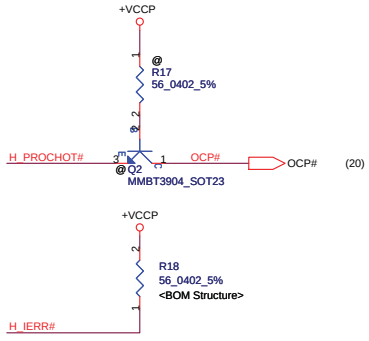
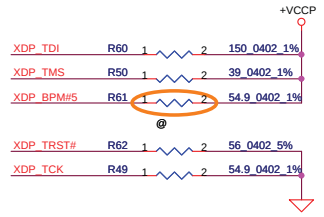
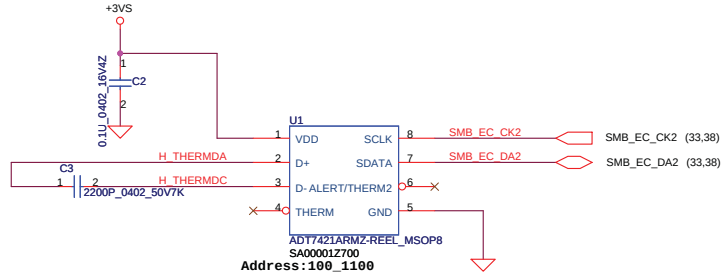
			Date: Friday, July 04, 2008; Sheet 3 of 44

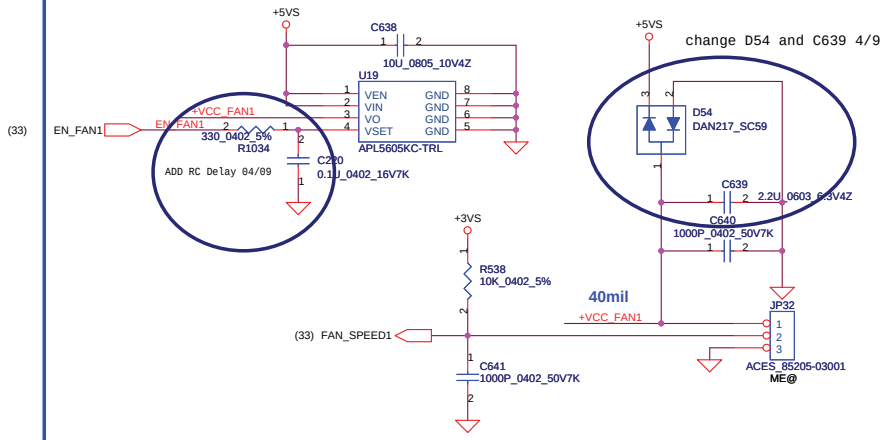


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil









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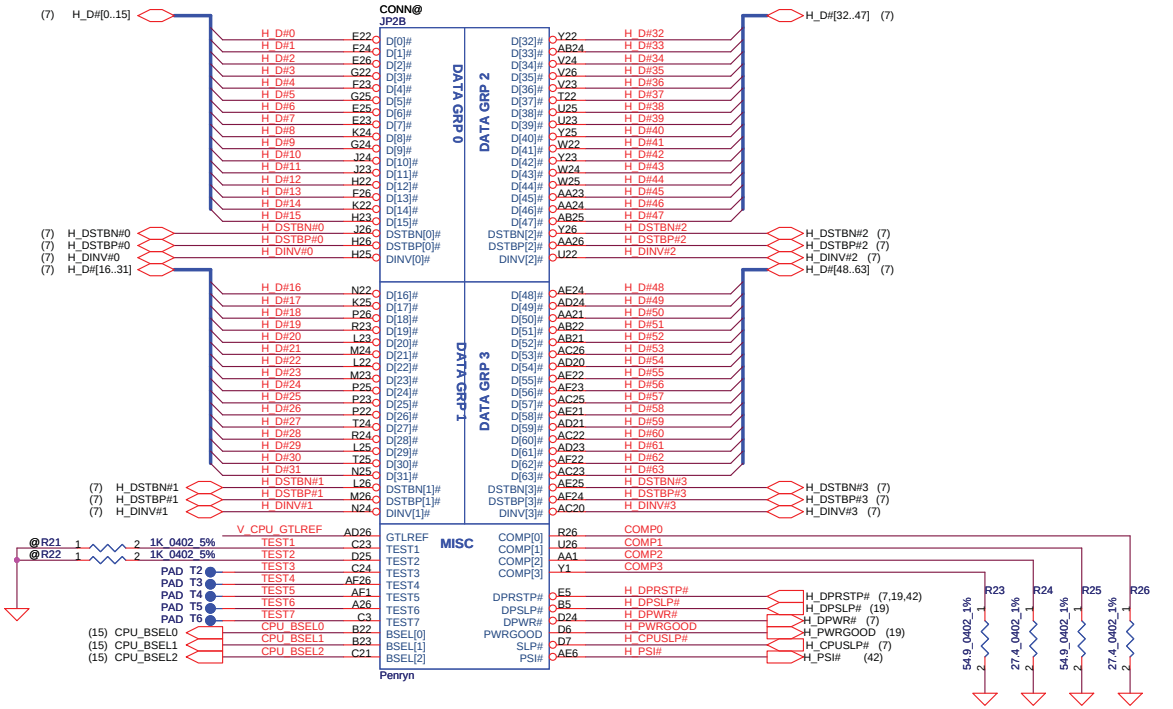
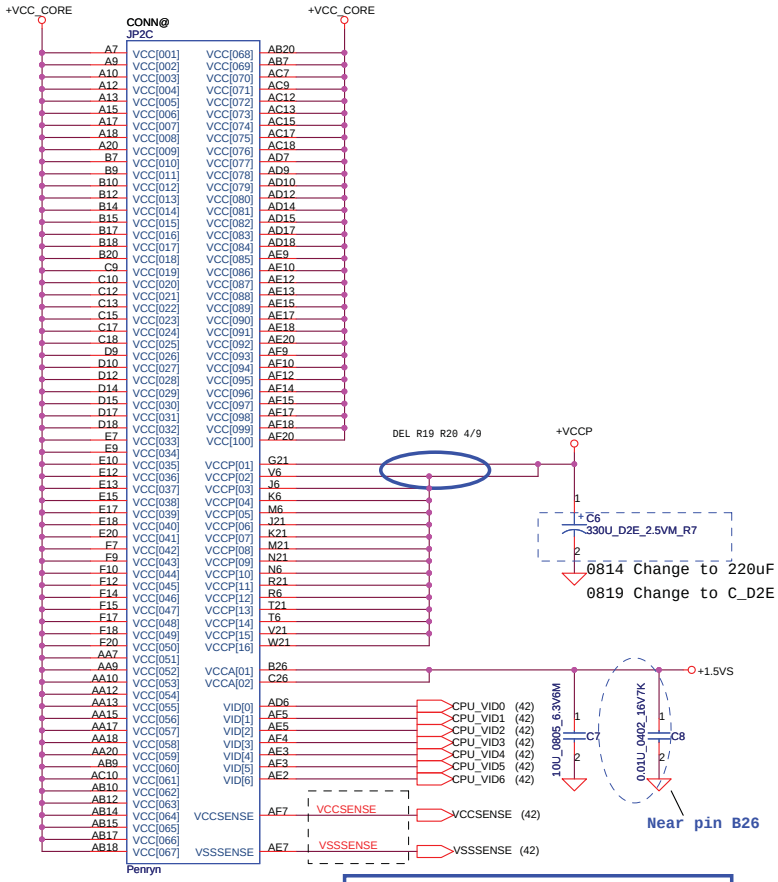


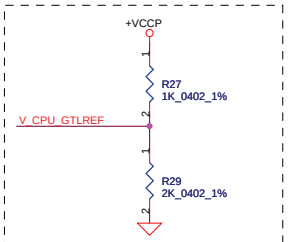


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

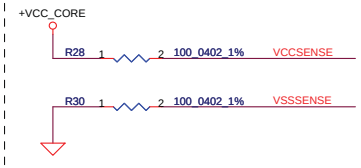
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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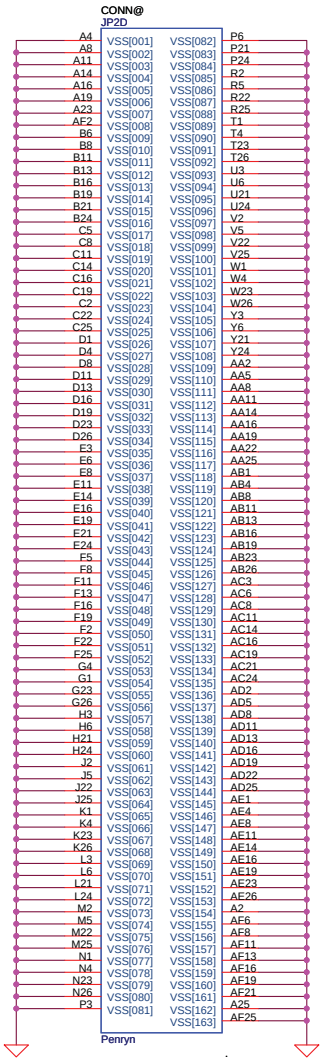
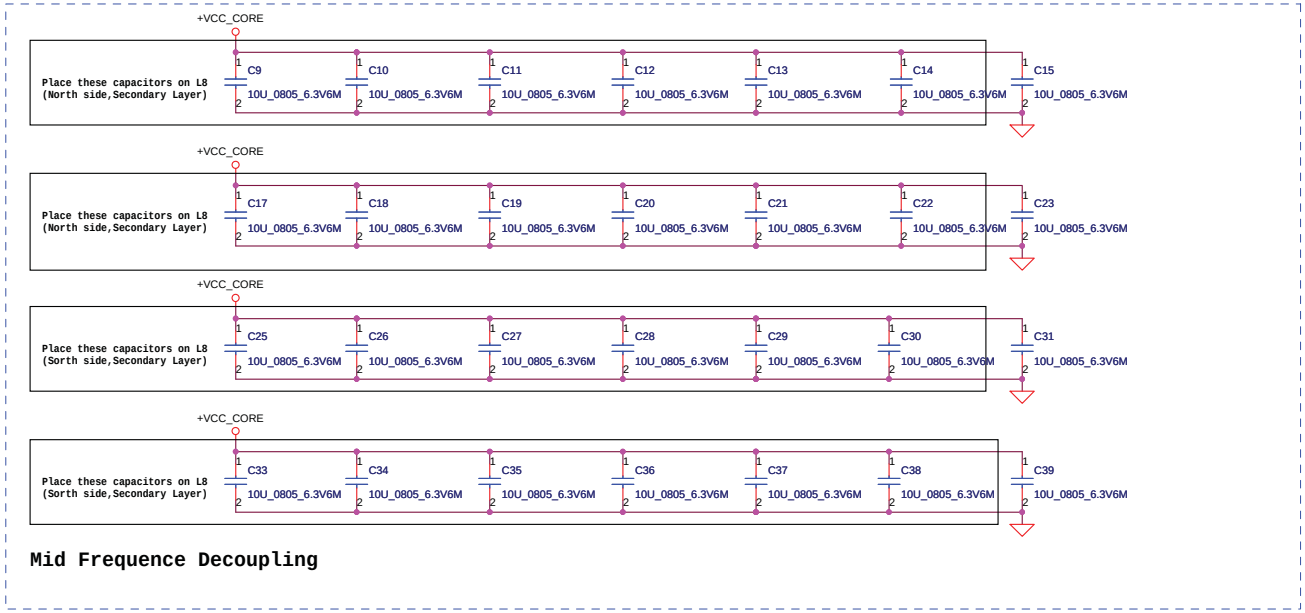
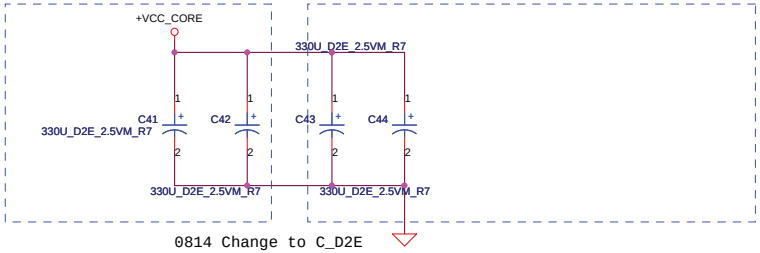




Mid Frequence Decoupling

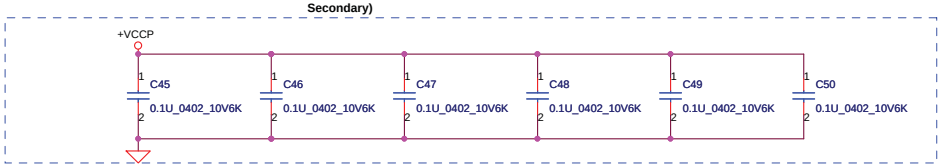
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



0814 Change to C_D2E

Place these inside socket cavity on L8 (North side Secondary)



DEL 330U 1017

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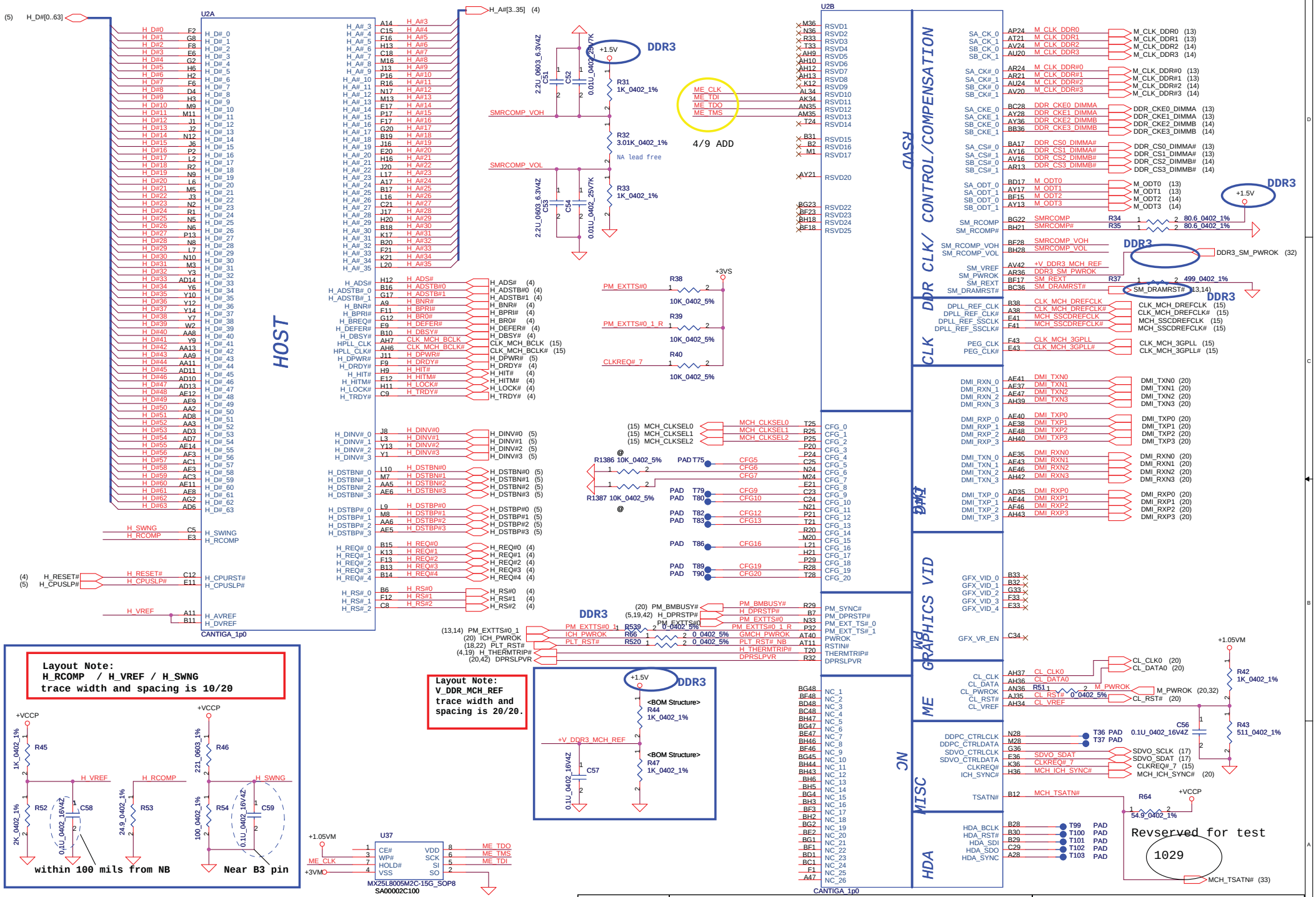

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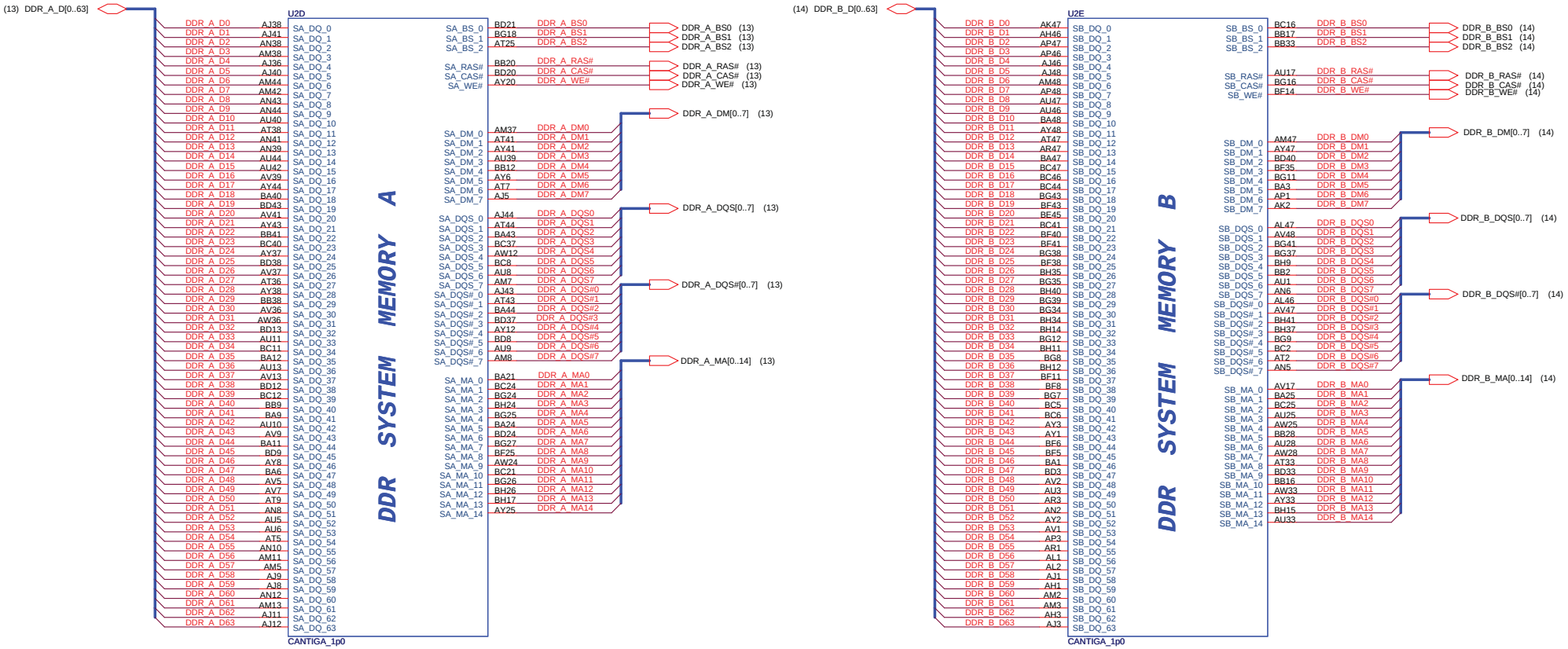

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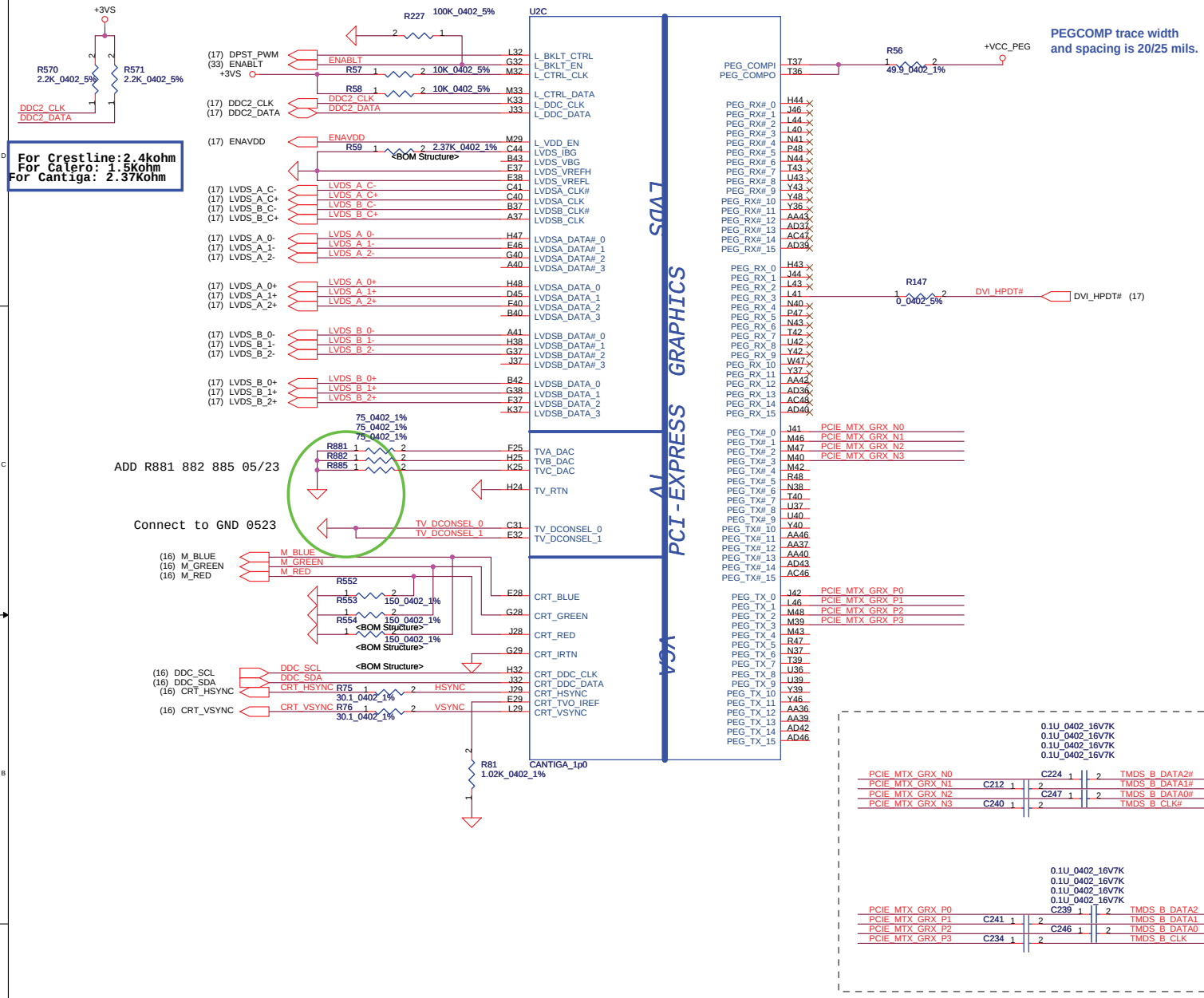

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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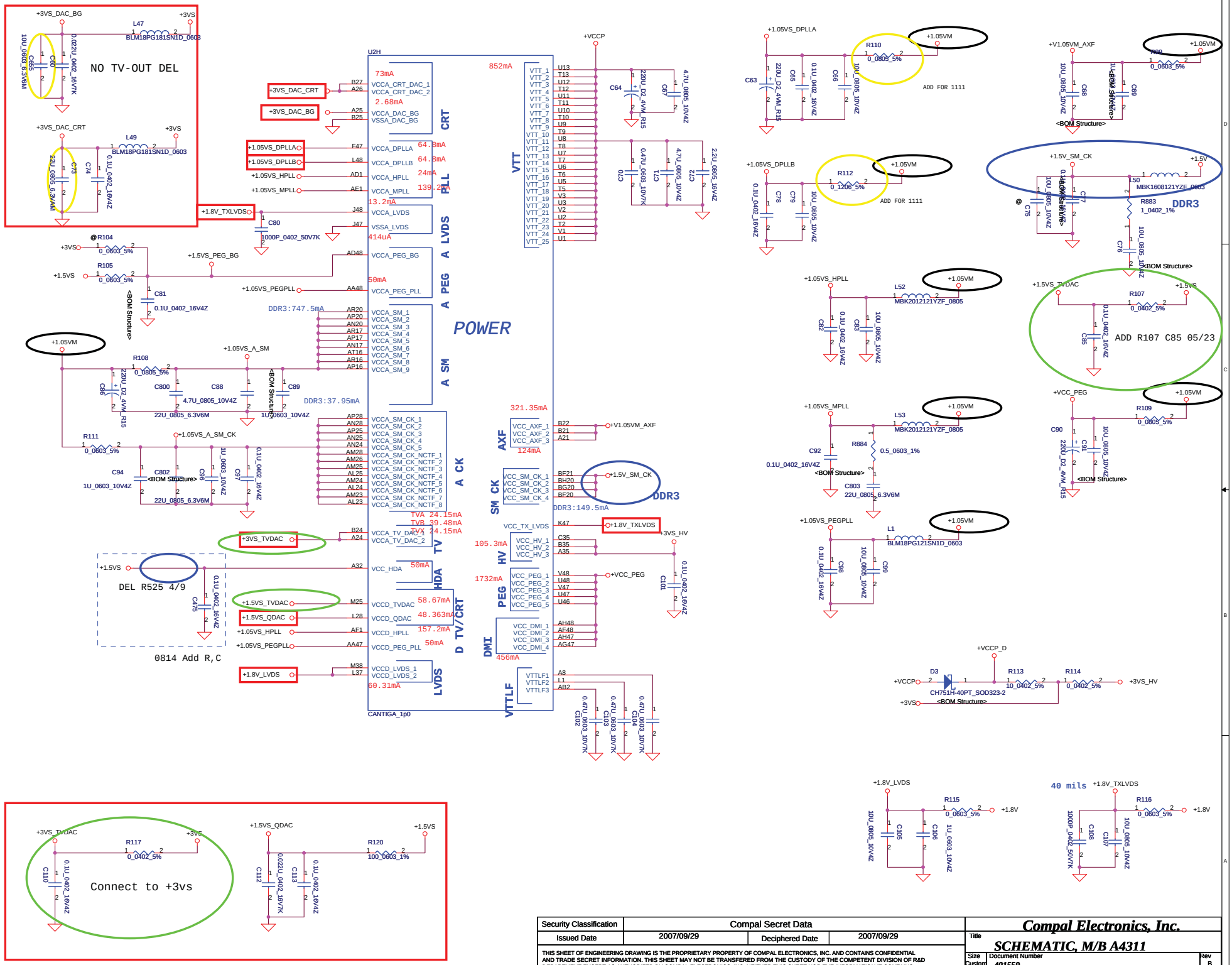

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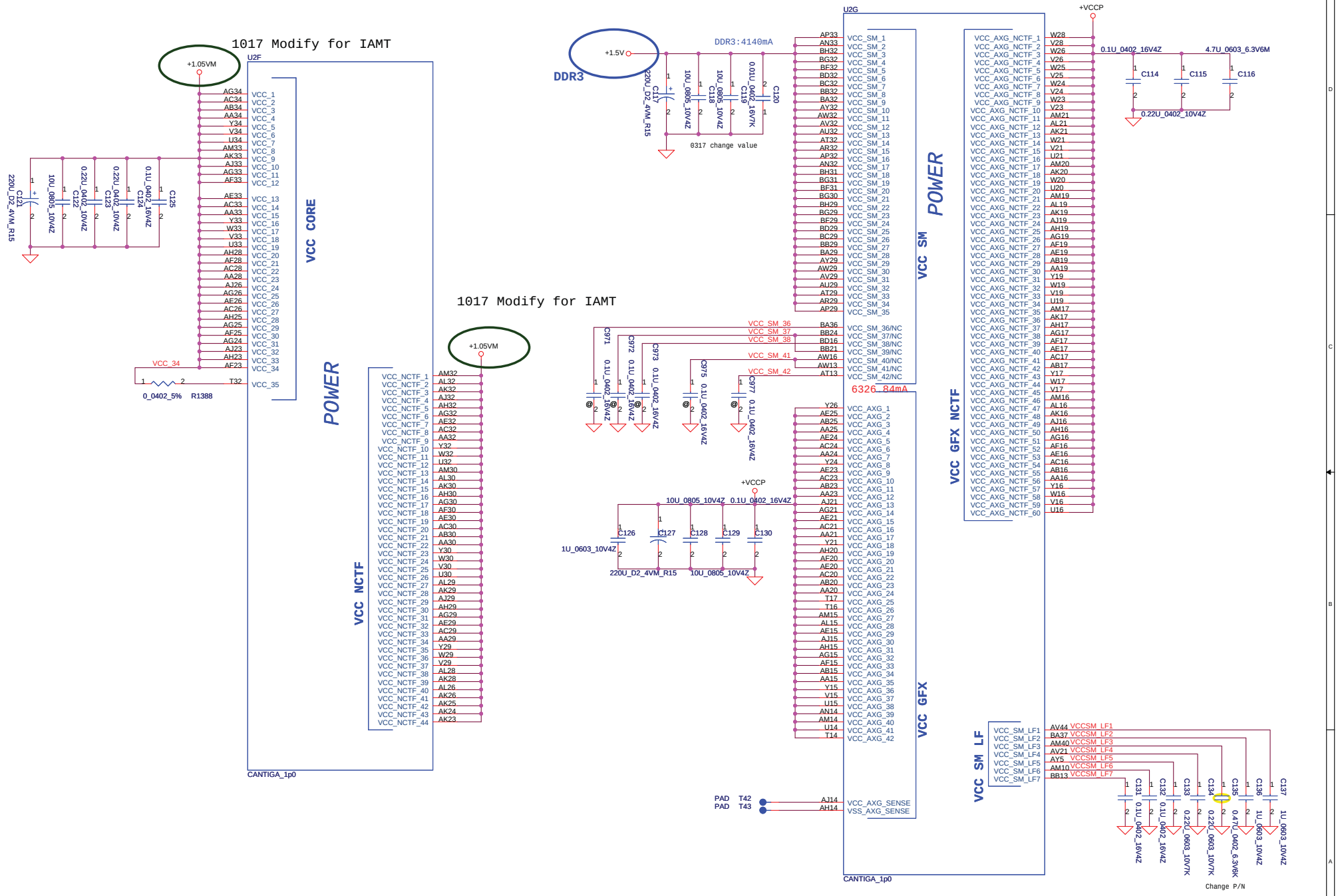

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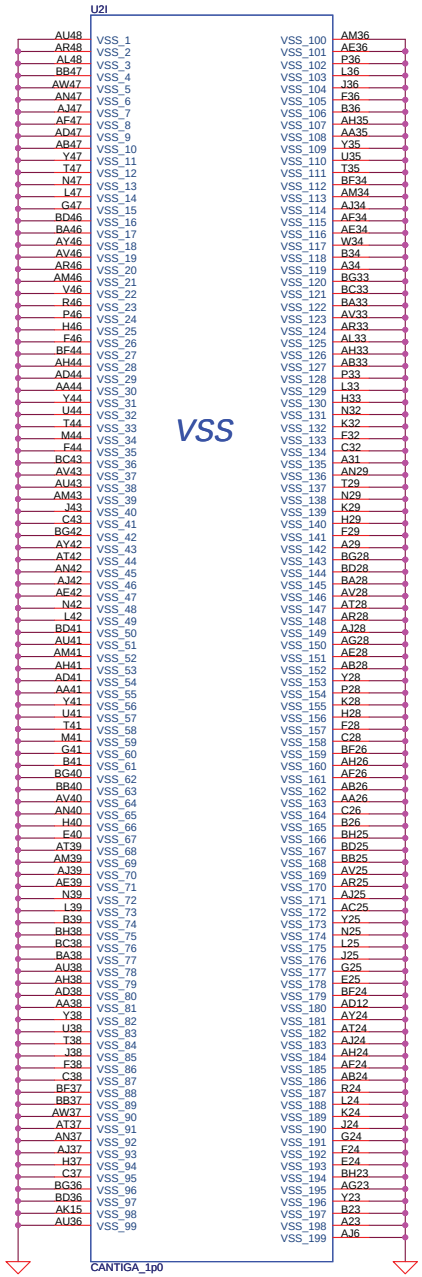

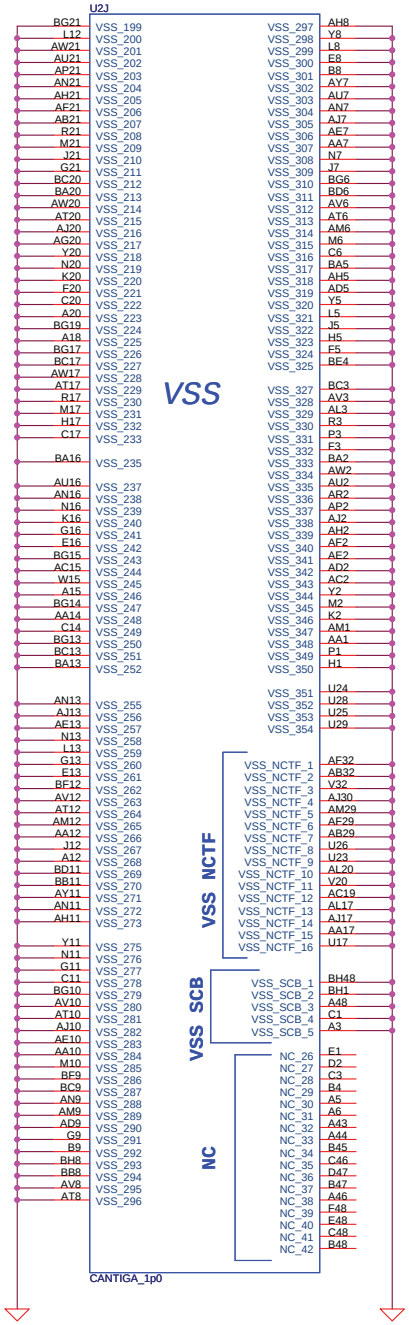

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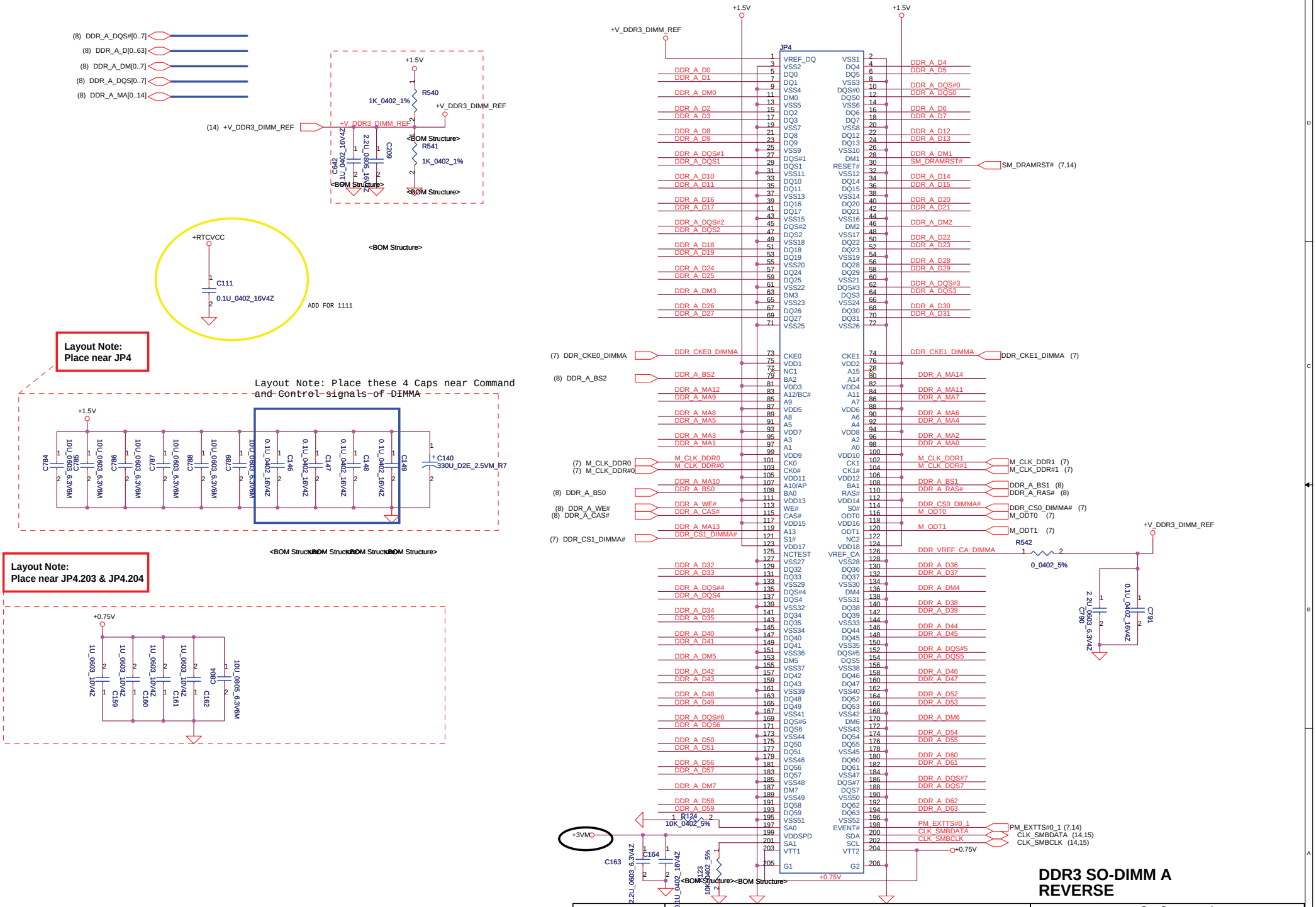

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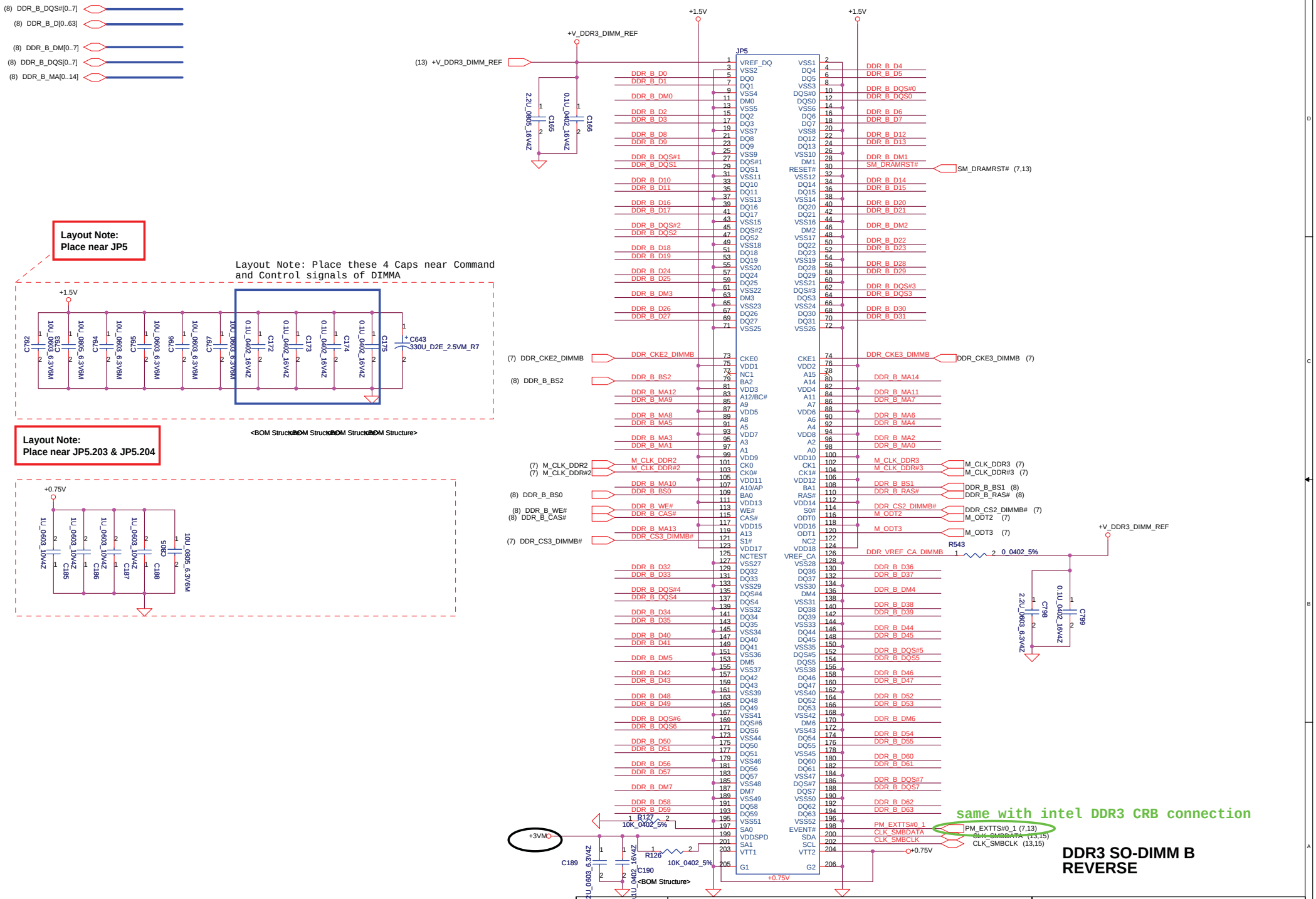
(8) DDR_B_DQS#[0..7]
(8) DDR_B_D[0..63]
(8) DDR_B_DM[0..7]
(8) DDR_B_DQS[0..7]
(8) DDR_B_MA[0..14]
Layout Note: Place near JP5
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
Layout Note: Place near JP5.203 & JP5.204
+1.5V
+0.75V
+V_DDR3_DIMM_REF
(13) +V_DDR3_DIMM_REF
JP5
(7) DDR_CKE2_DIMMB
(8) DDR_B_BS2
(7) M_CLK_DDR2
(7) M_CLK_DDR#2
(8) DDR_B_BS0
(8) DDR_B_WE#
(8) DDR_B_CAS#
(7) DDR_CS3_DIMMB#
DDR_CKE3_DIMMB (7)
M_CLK_DDR3 (7)
M_CLK_DDR#3 (7)
DDR_B_BS1 (8)
DDR_B_RAS# (8)
DDR_CS2_DIMMB# (7)
M_ODT2 (7)
M_ODT3 (7)
SM_DRAMRST# (7,13)
PM_EXTTS#0_1 (7,13)
CLK_SMBDATA (13,15)
CLK_SMBCLK (13,15)
+3VM
same with intel DDR3 CRB connection
DDR3 SO-DIMM B
REVERSE
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SCHEMATIC, M/B A4311
Security Classification
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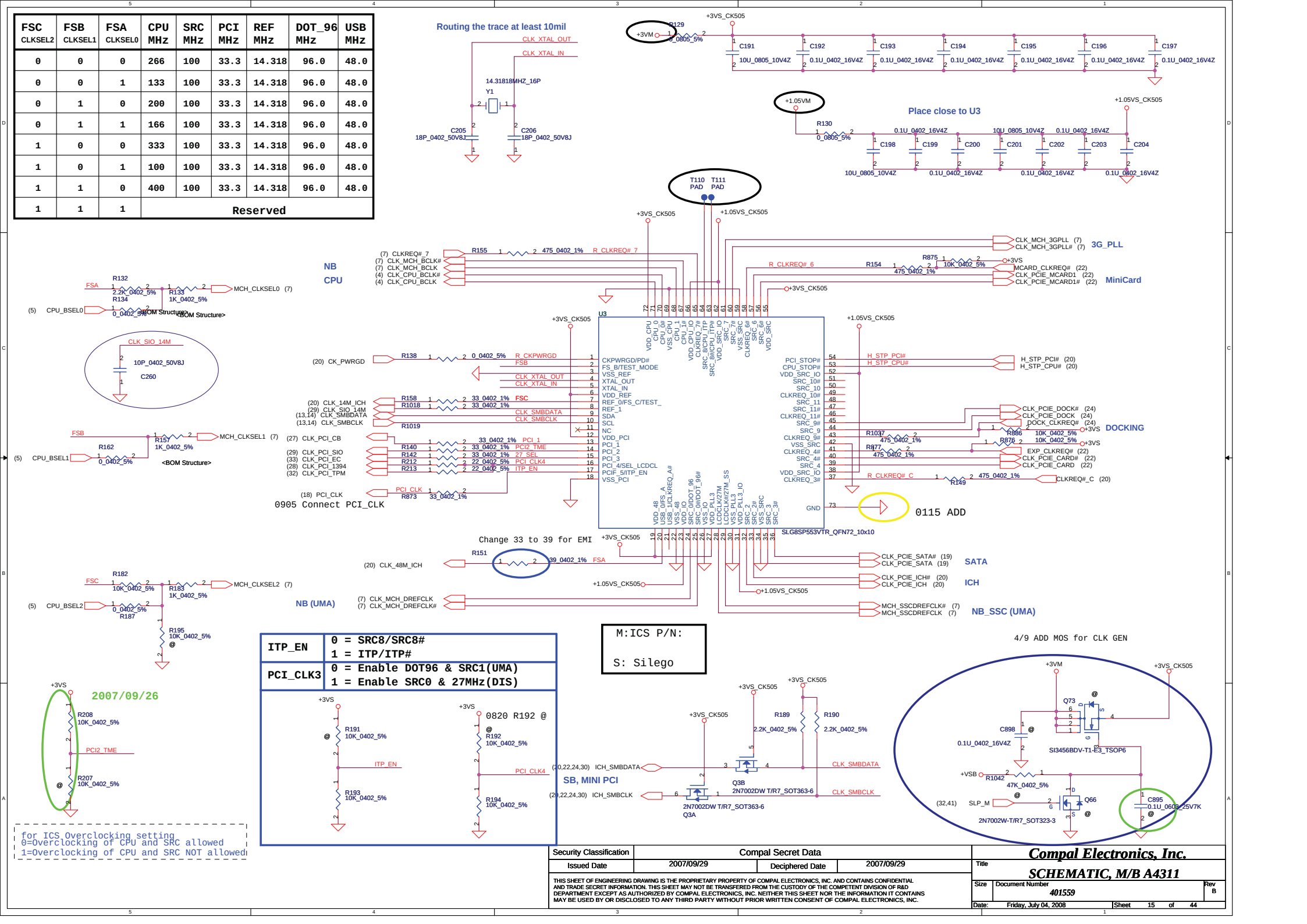
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



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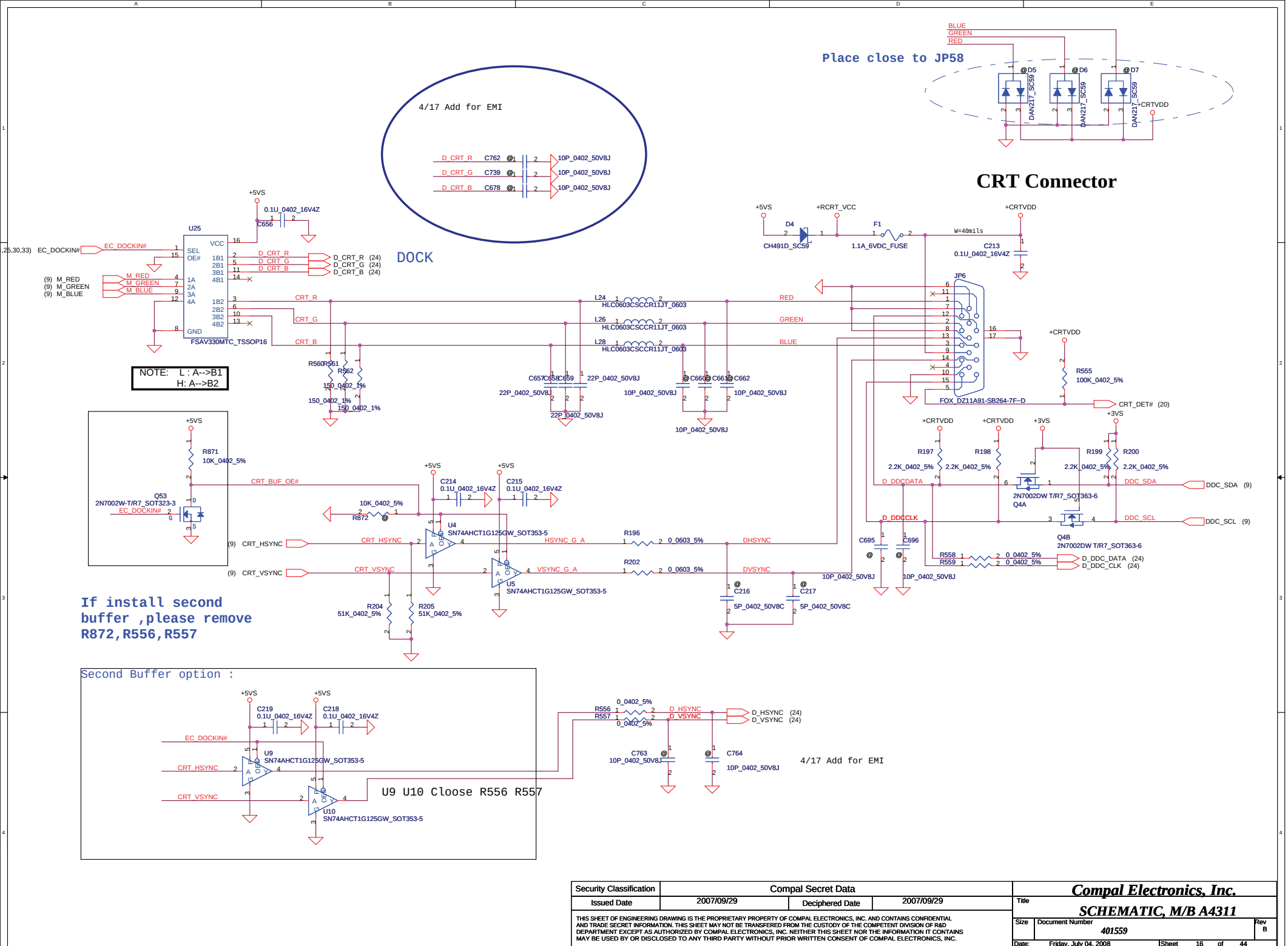

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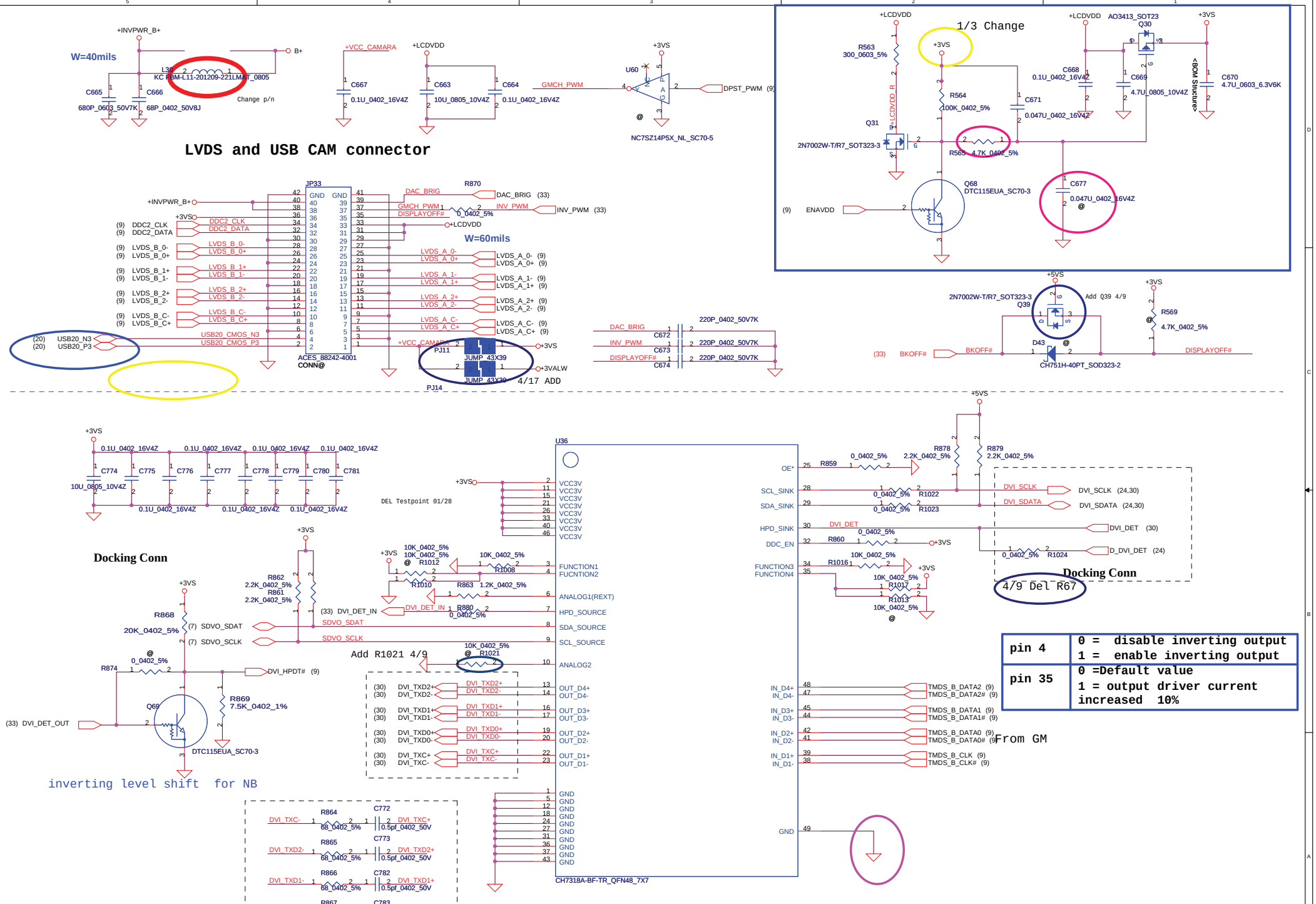

pin 4	0 = disable inverting output 1 = enable inverting output
pin 35	0 =Default value 1 = output driver current increased 10%

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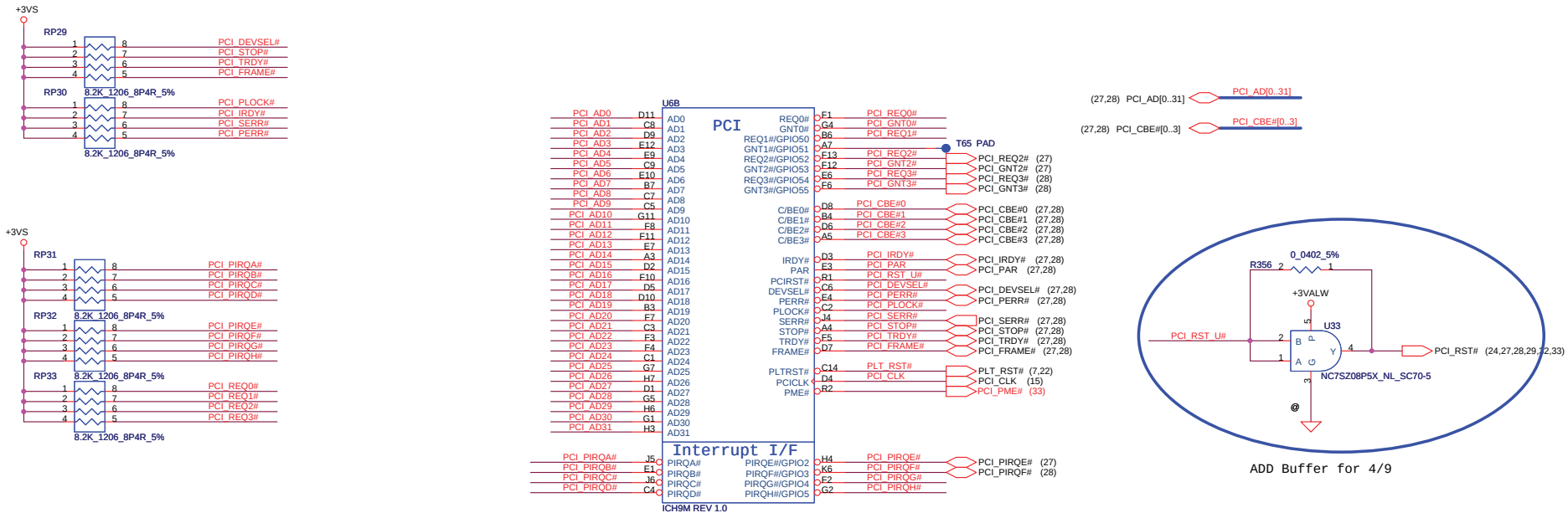
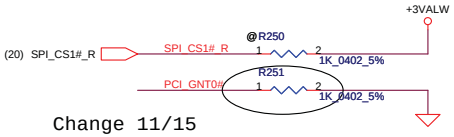


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Change 11/15

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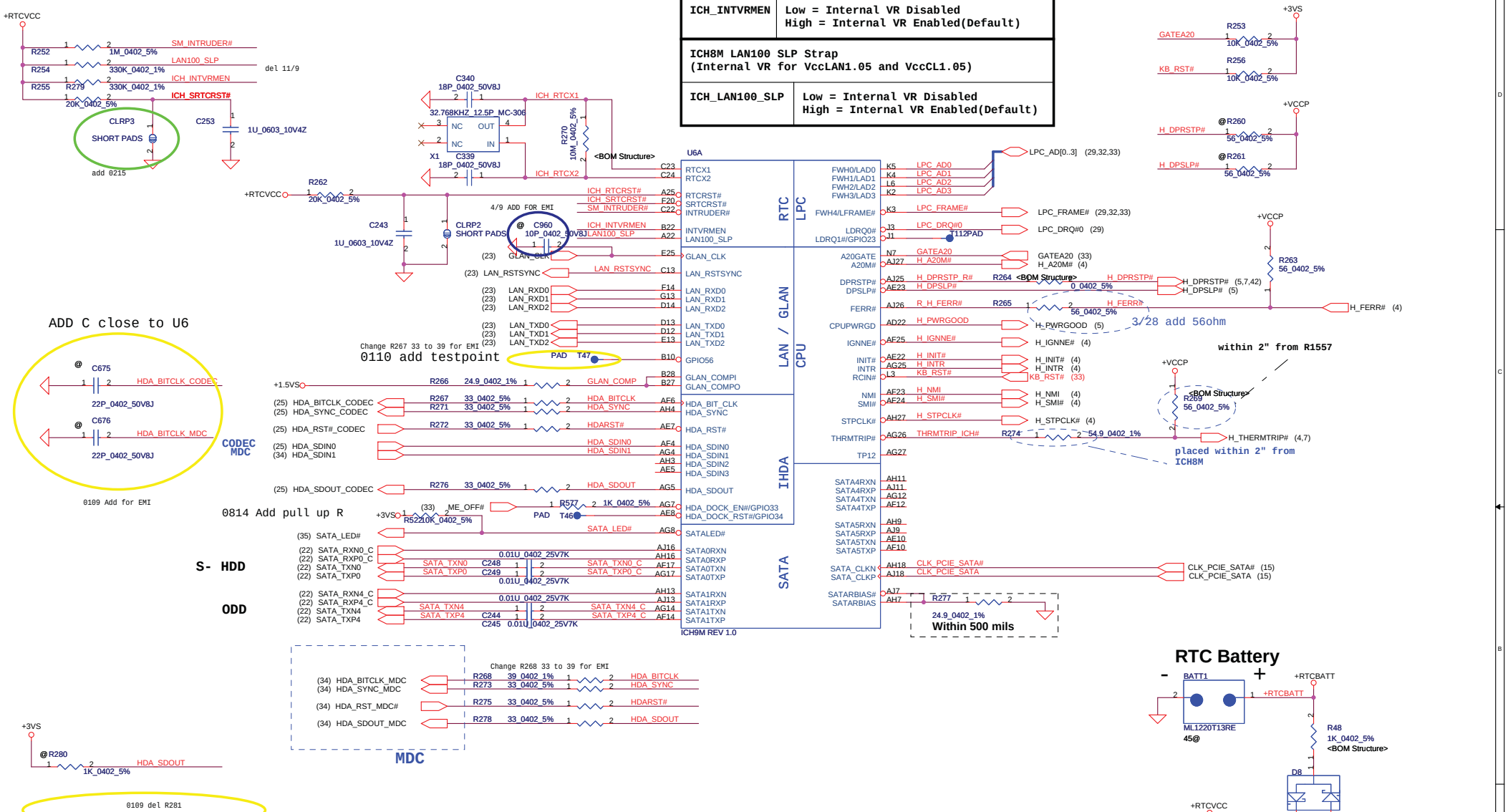
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



XOR CHAIN ENTRANCE STRAP:RSVD

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

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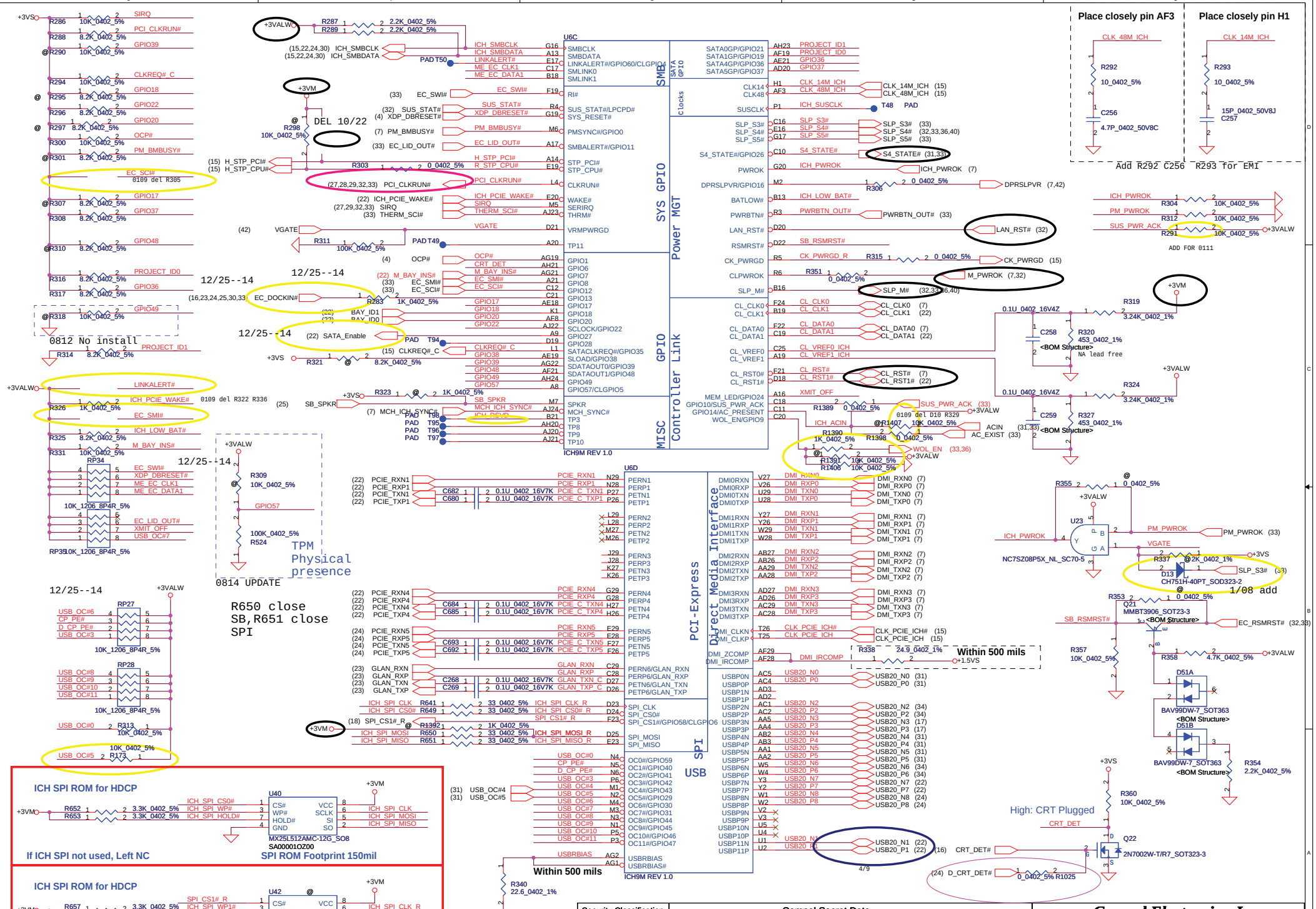

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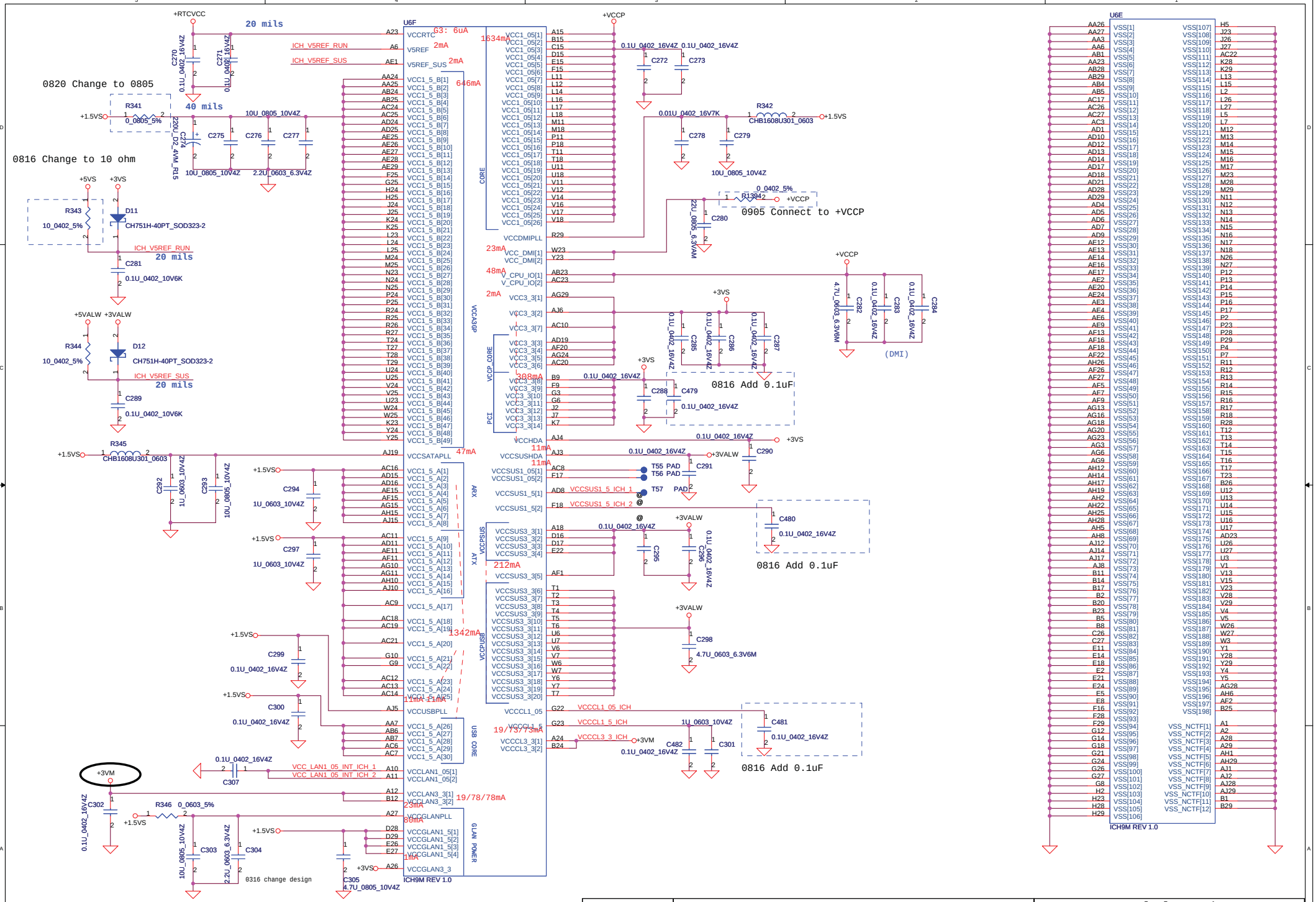

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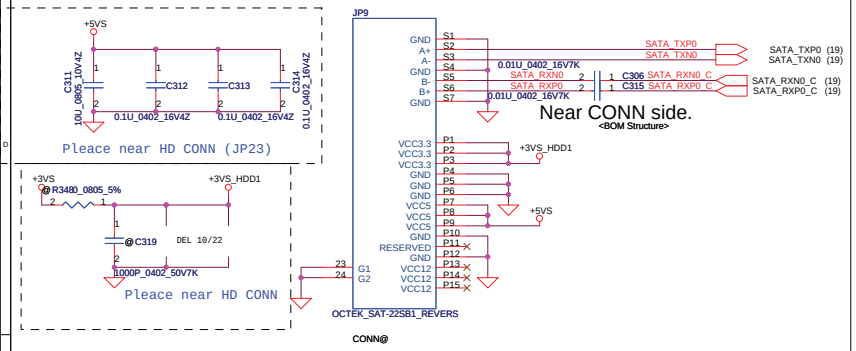
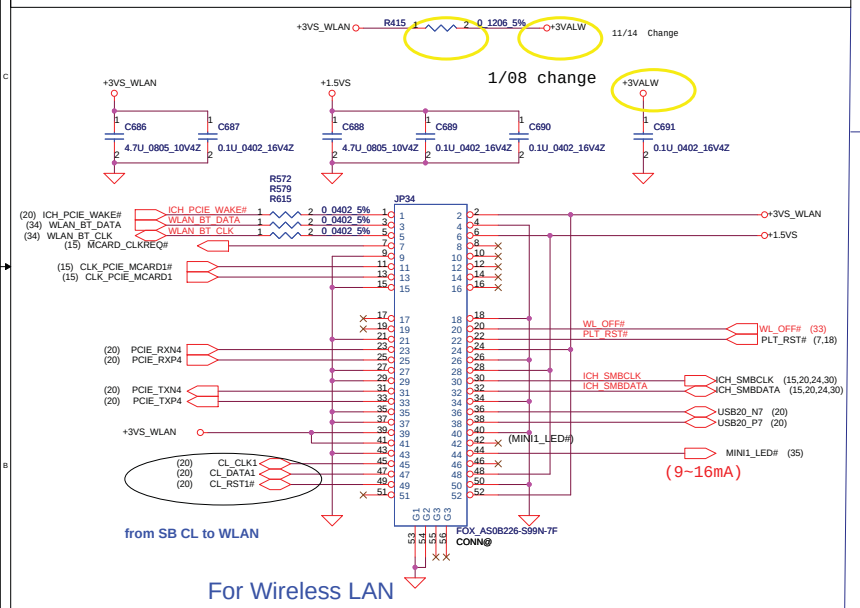
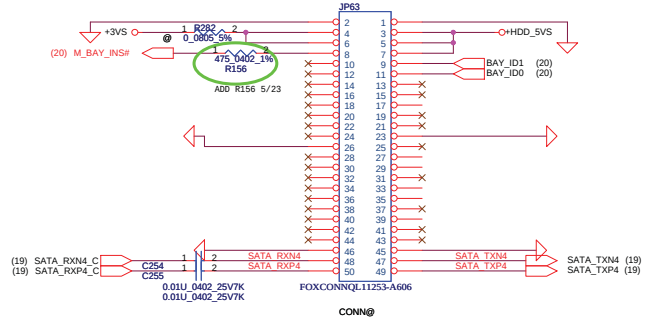
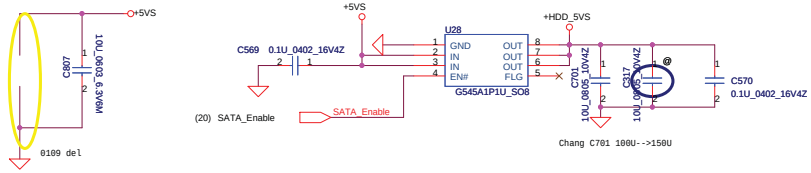
HDD Connector

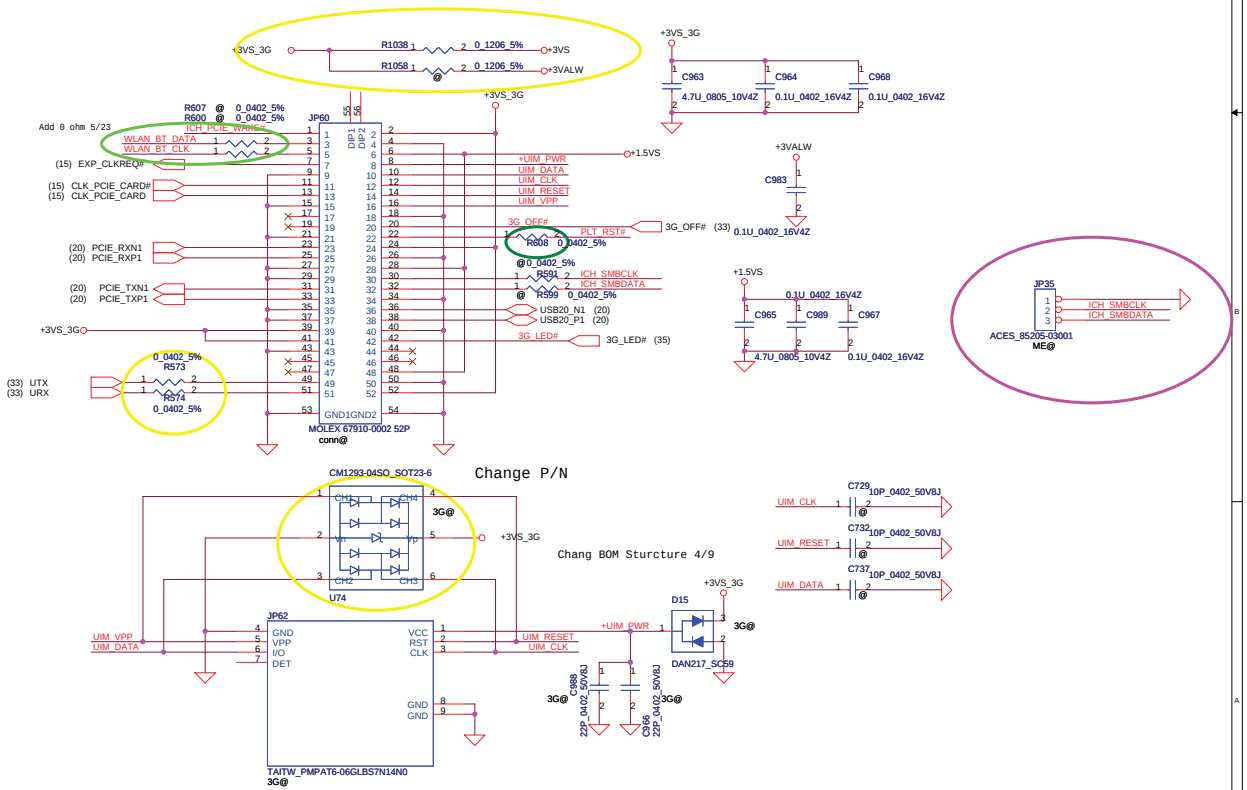




Media BAY for 2ND HDD BATT







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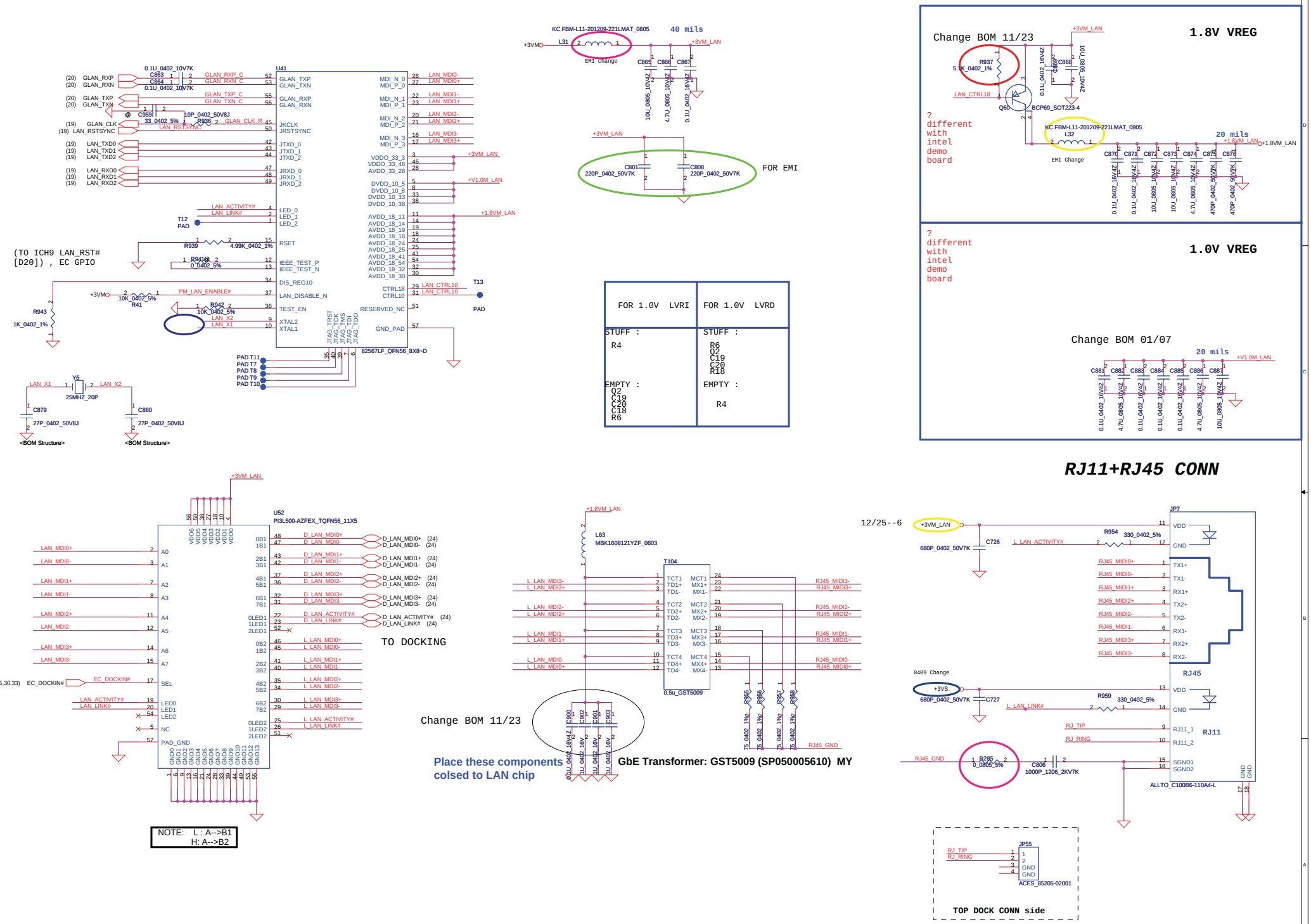

FOR 1.0V LVRI	FOR 1.0V LVRD
STUFF : R4	STUFF : R6 Q2 C19 C20 R18
EMPTY : Q2 C19 C20 C18 R6	EMPTY : R4

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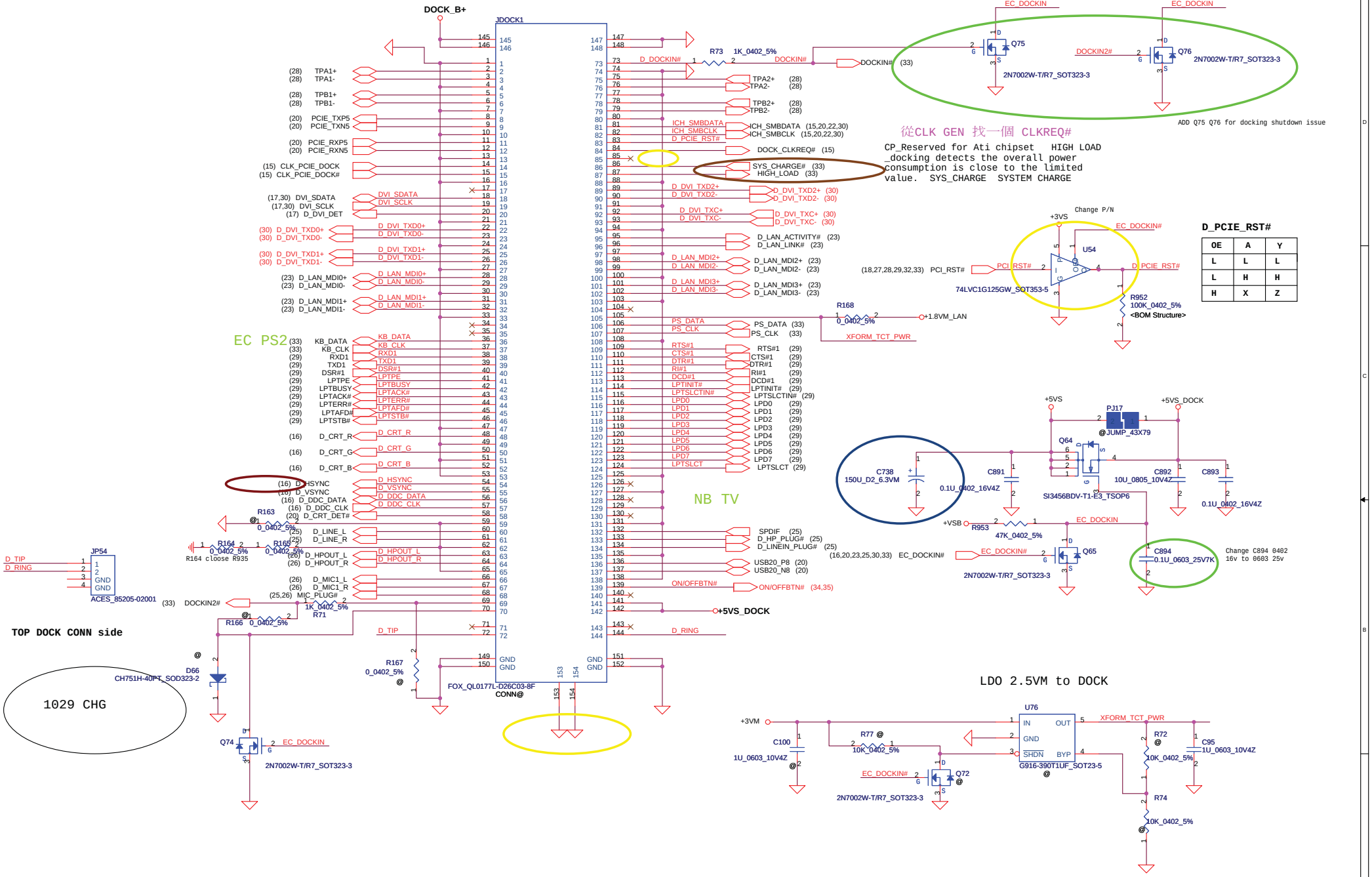

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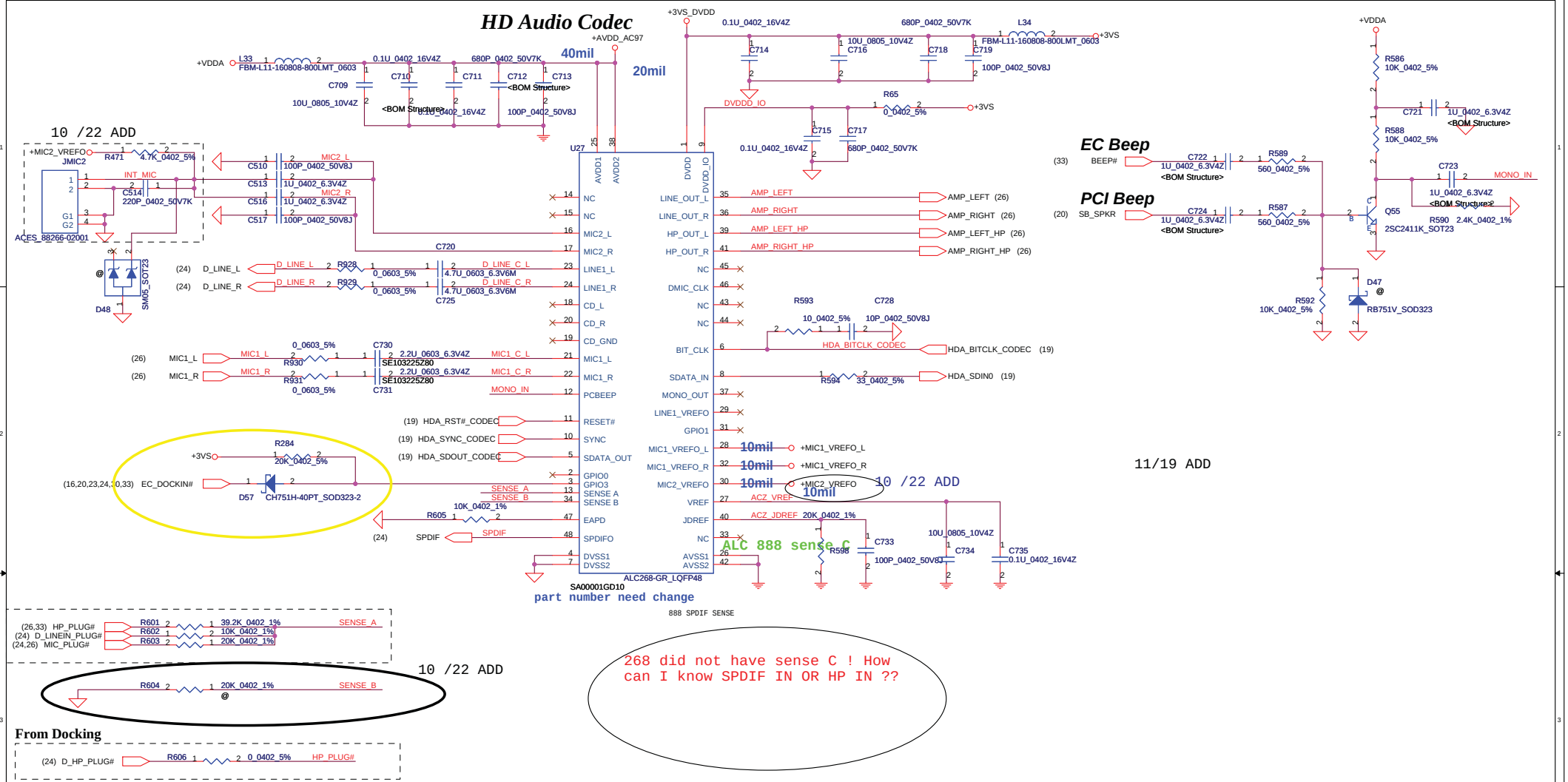
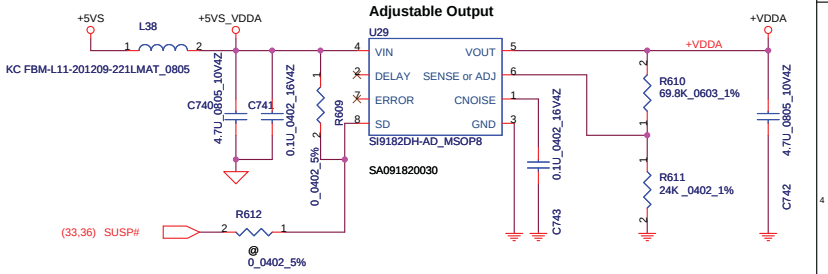
HD Audio Codec



268 did not have sense C ! How can I know SPDIF IN OR HP IN ??

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)
SENSE C	39.2K	CD
	20K	1st S/PDIF Out
	10K	2nd S/PDIF Out
	5.1K	S/PDIF-IN

Regulator for CODEC



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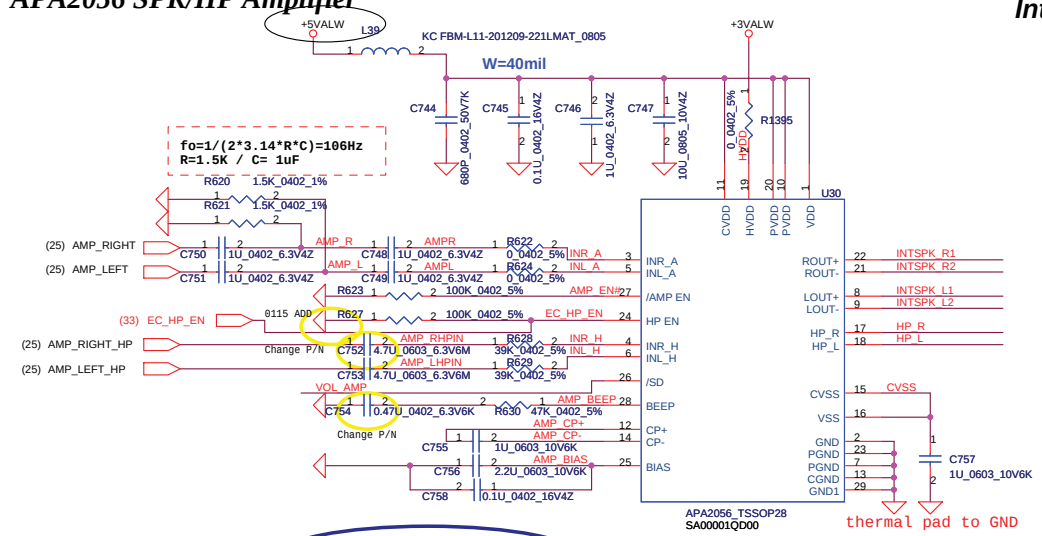
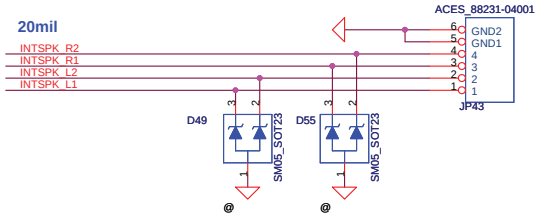
APA2056 SPK/HP Amplifier



Int. Speaker Conn.

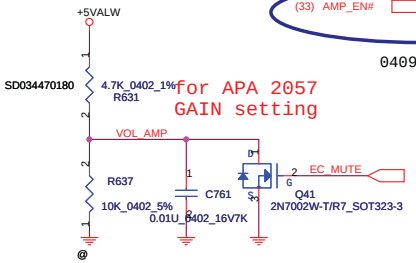


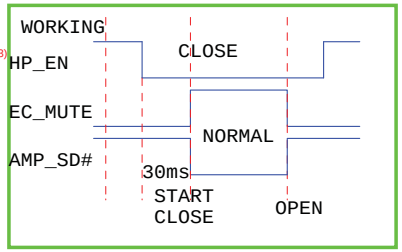
DEL SPDIF POWER 11/20

(33) AMP_EN# AMP_EN#

0409 ADD

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)





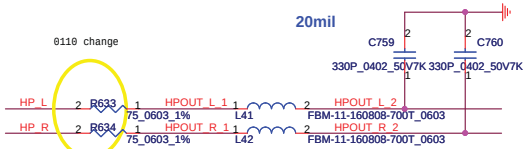
APA2057 gain setting table

gain \ V	V(low)	V(high)
8	3.21	3.27
9	3.33	3.39
10	3.45	3.51

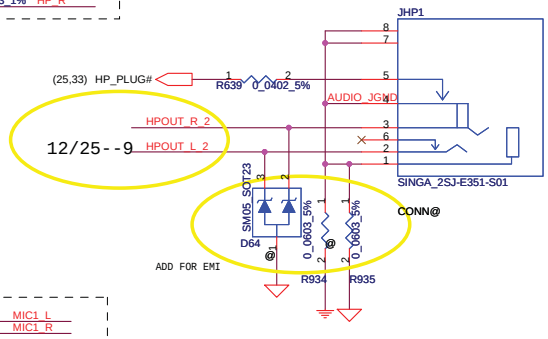
(dB)

current setting(3.48V)

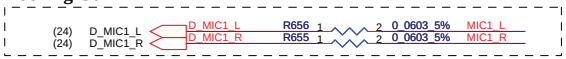
LINE Out/Headphone Out S/PDIF Out JACK



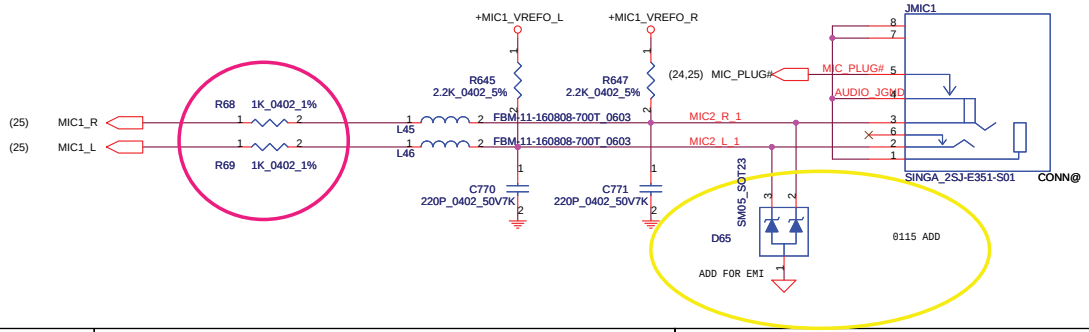
Docking Conn



Docking Conn



MIC JACK



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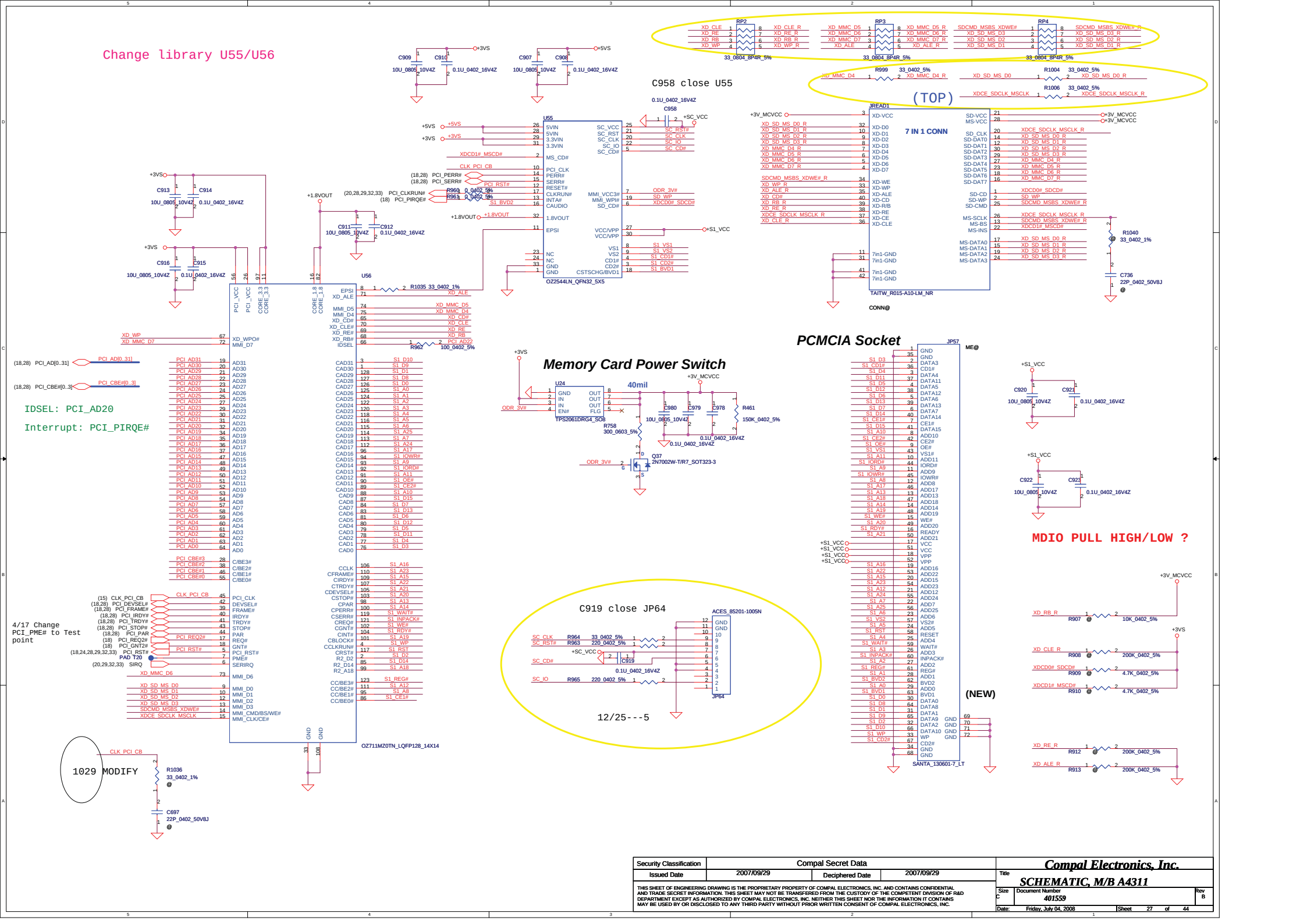

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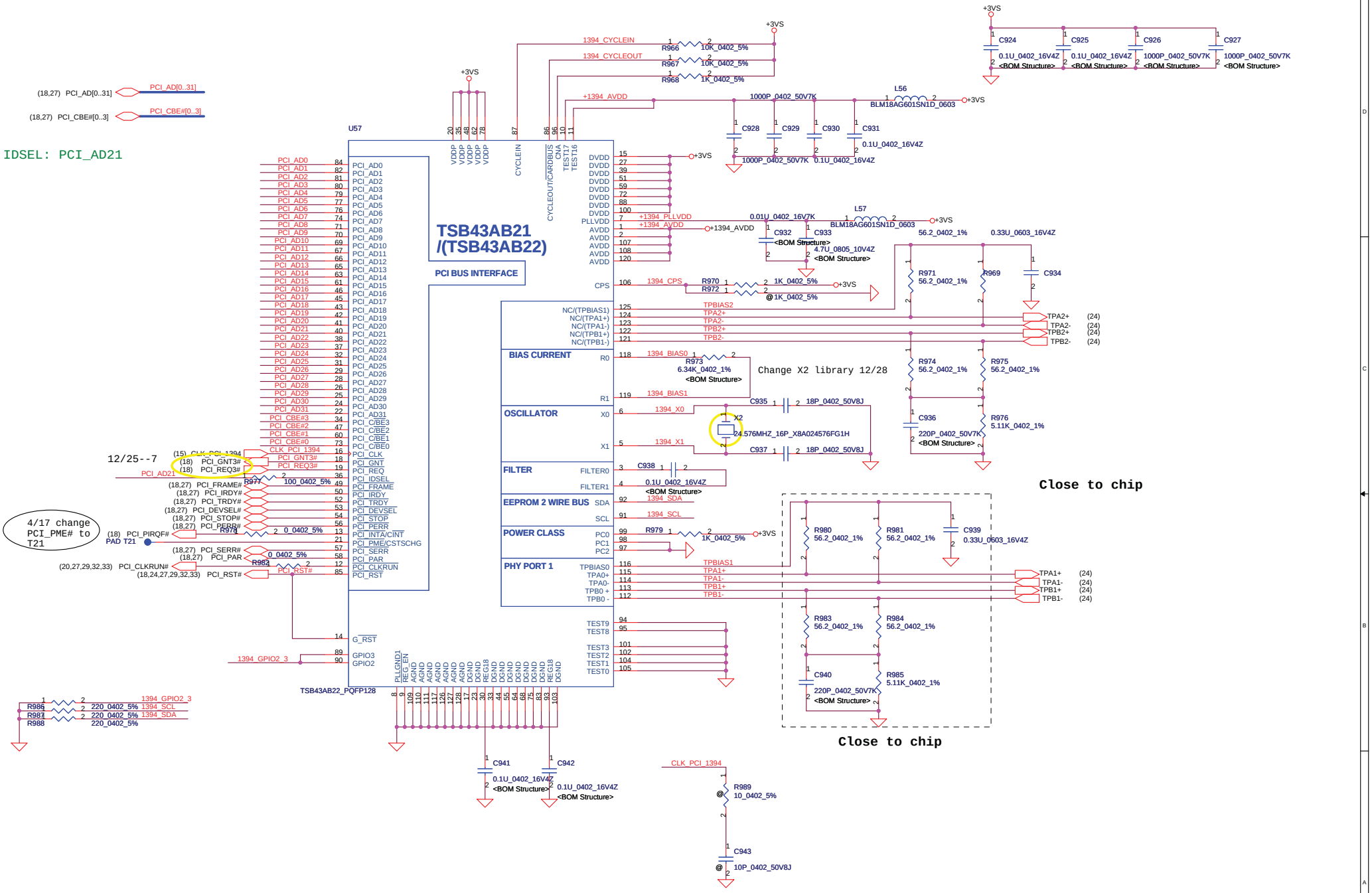

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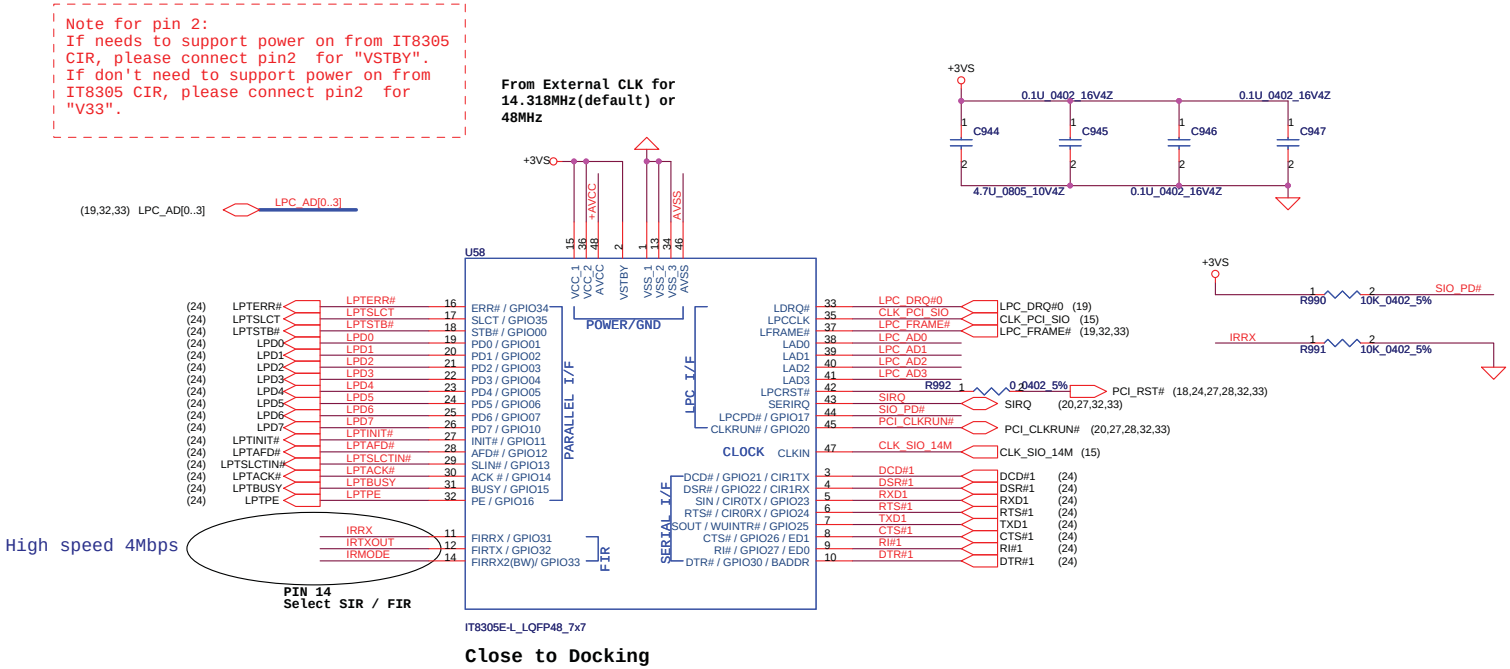
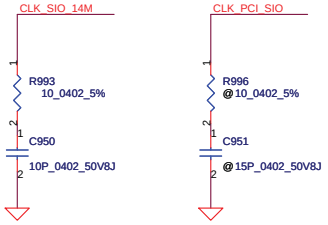
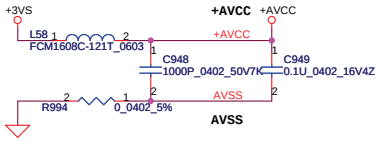
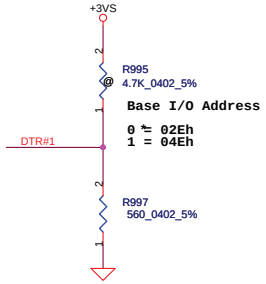
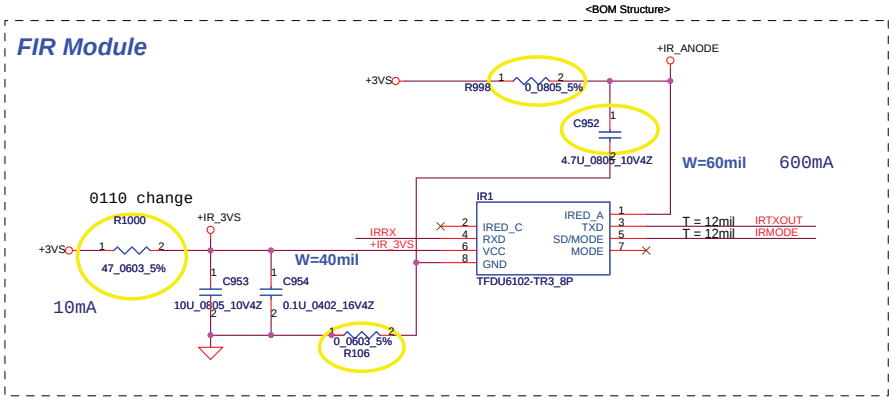
SUPER I/O ITE IT8305E











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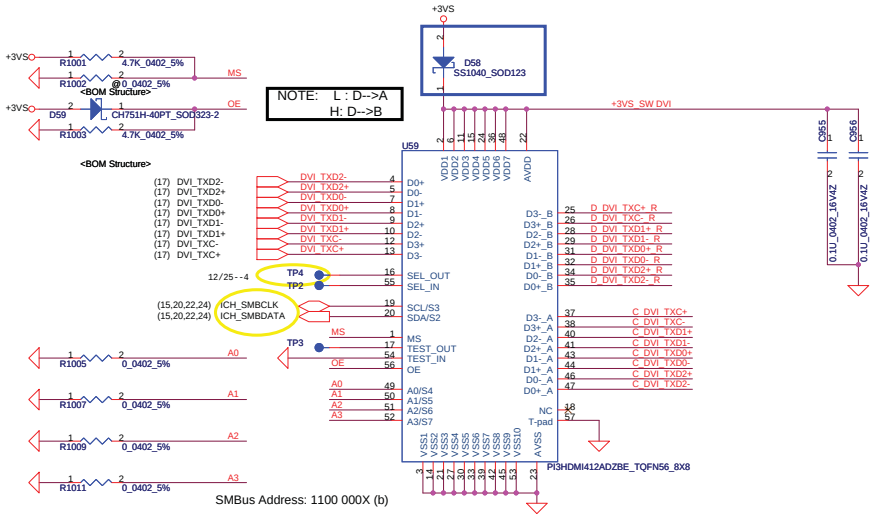
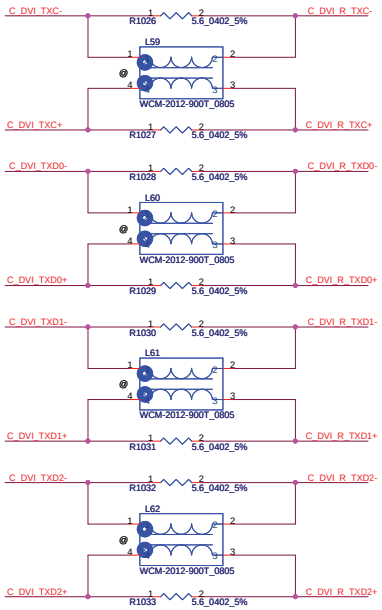
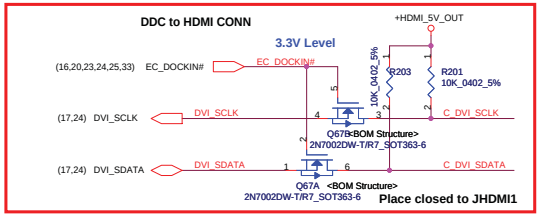
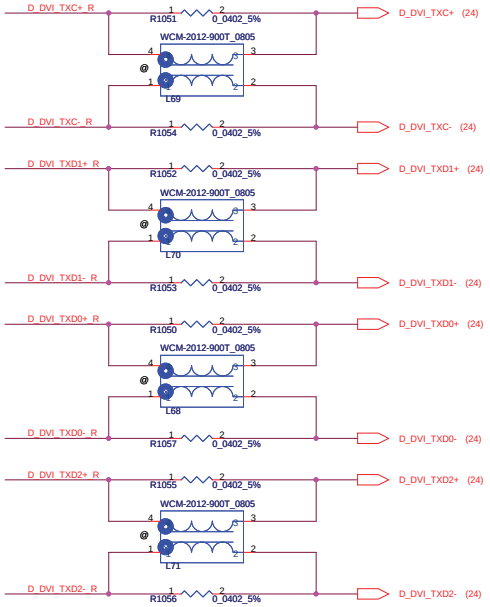
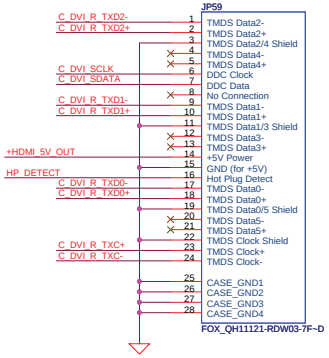


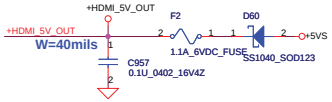


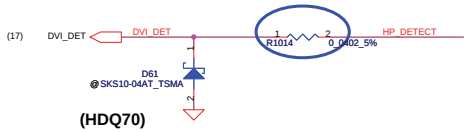




DVI-D Connector







(HDQ70)

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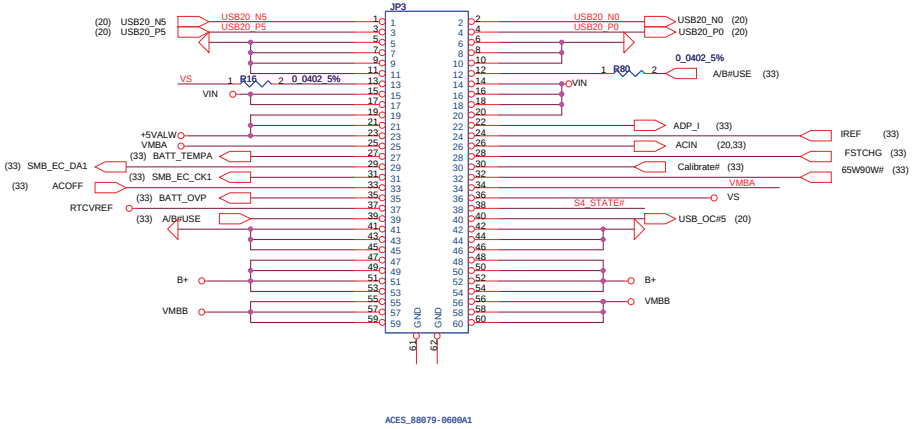

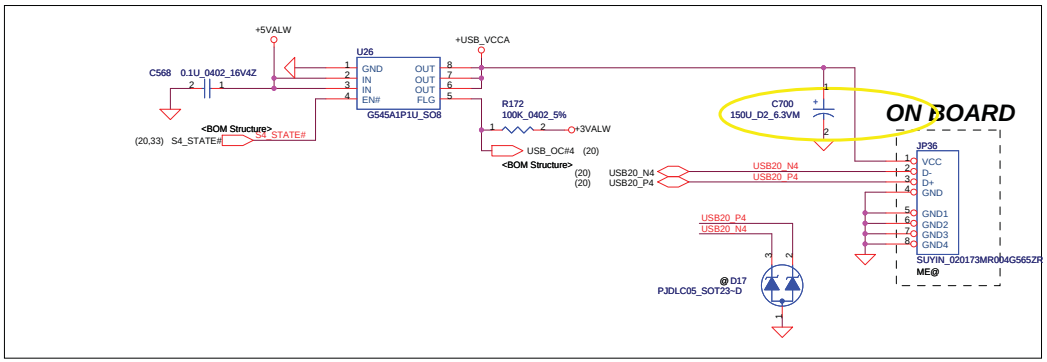

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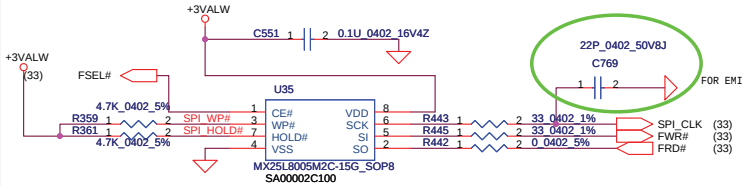
BIOS

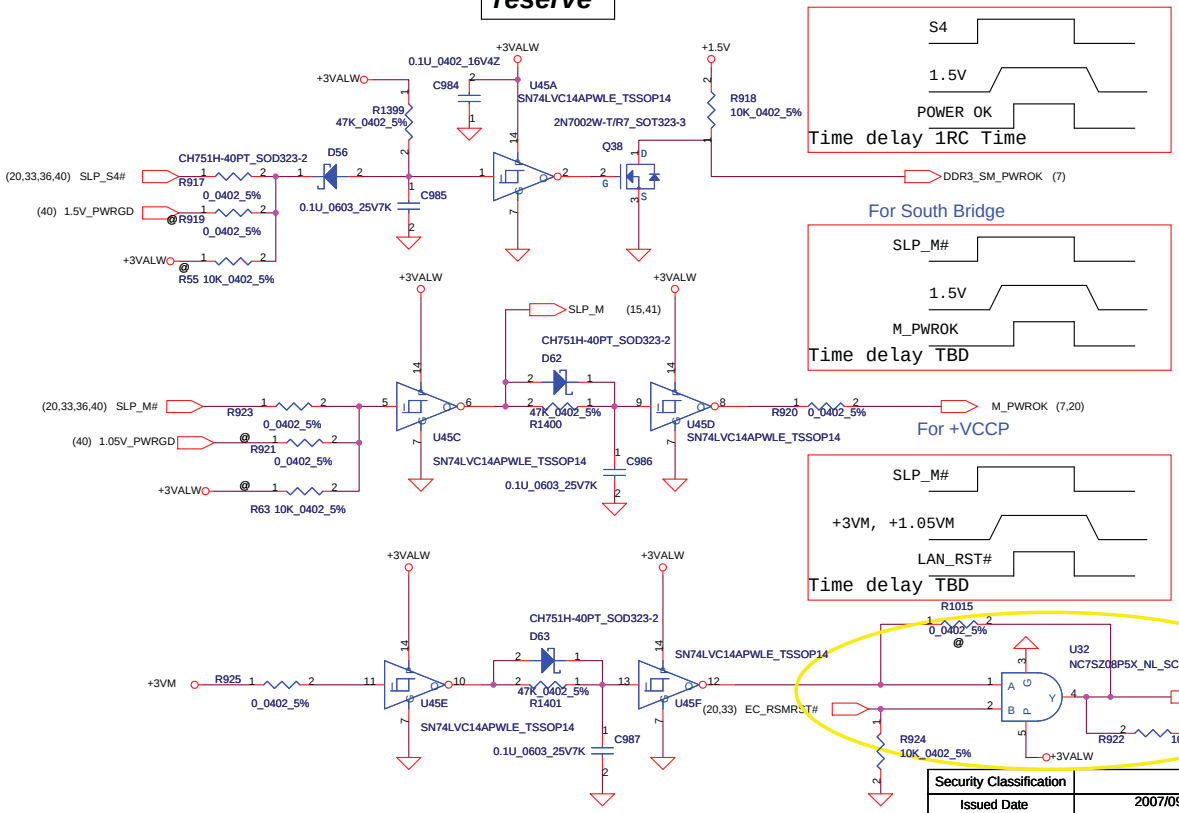


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

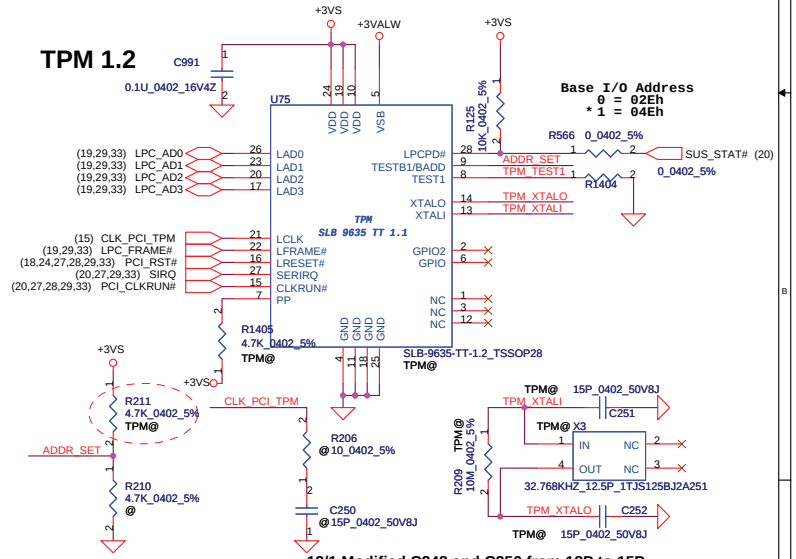
0115 DEL

Power ON Circuit

reserve



TPM 1.2



12/1 Modified C248 and C250 from 18P to 15P

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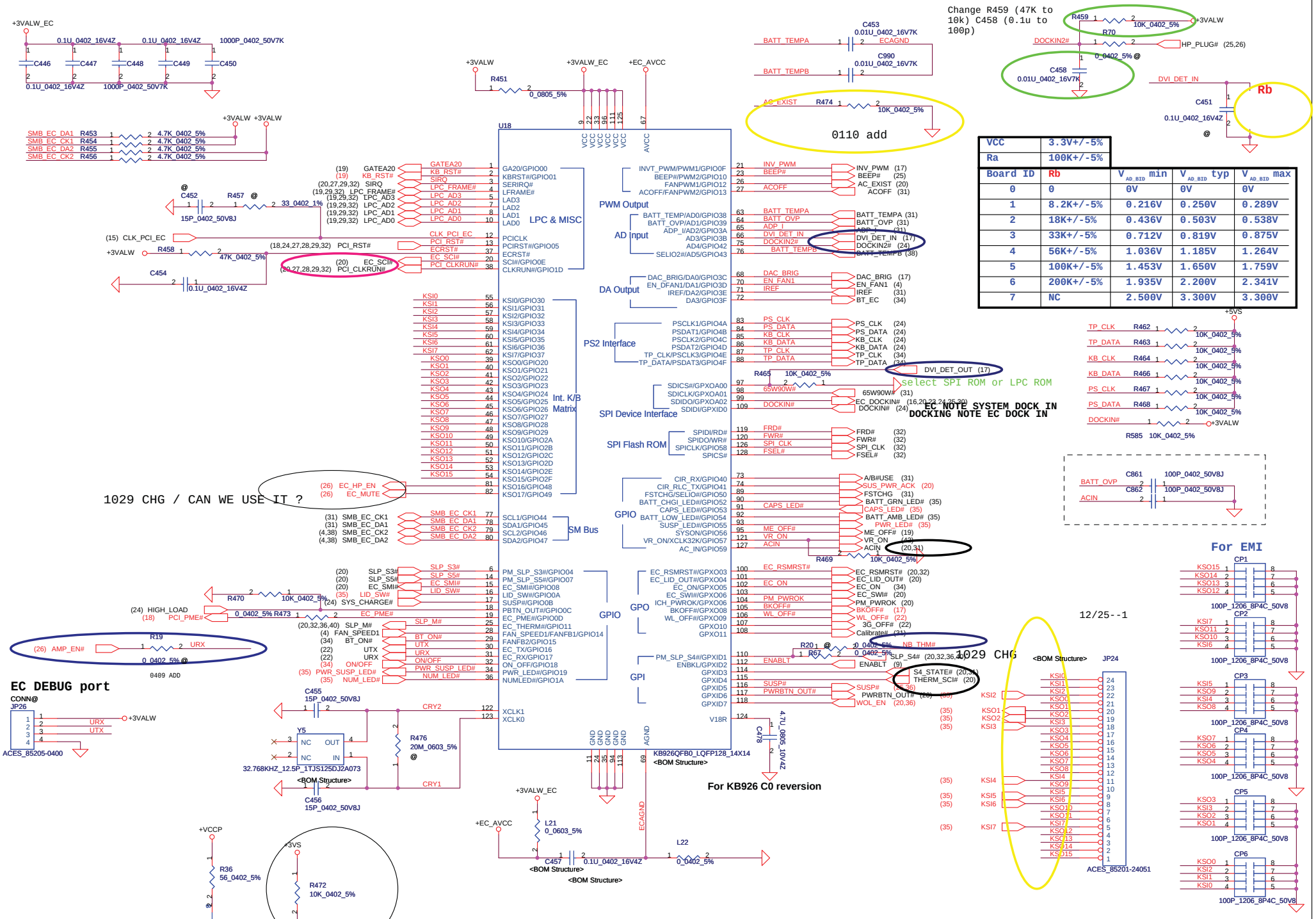

VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

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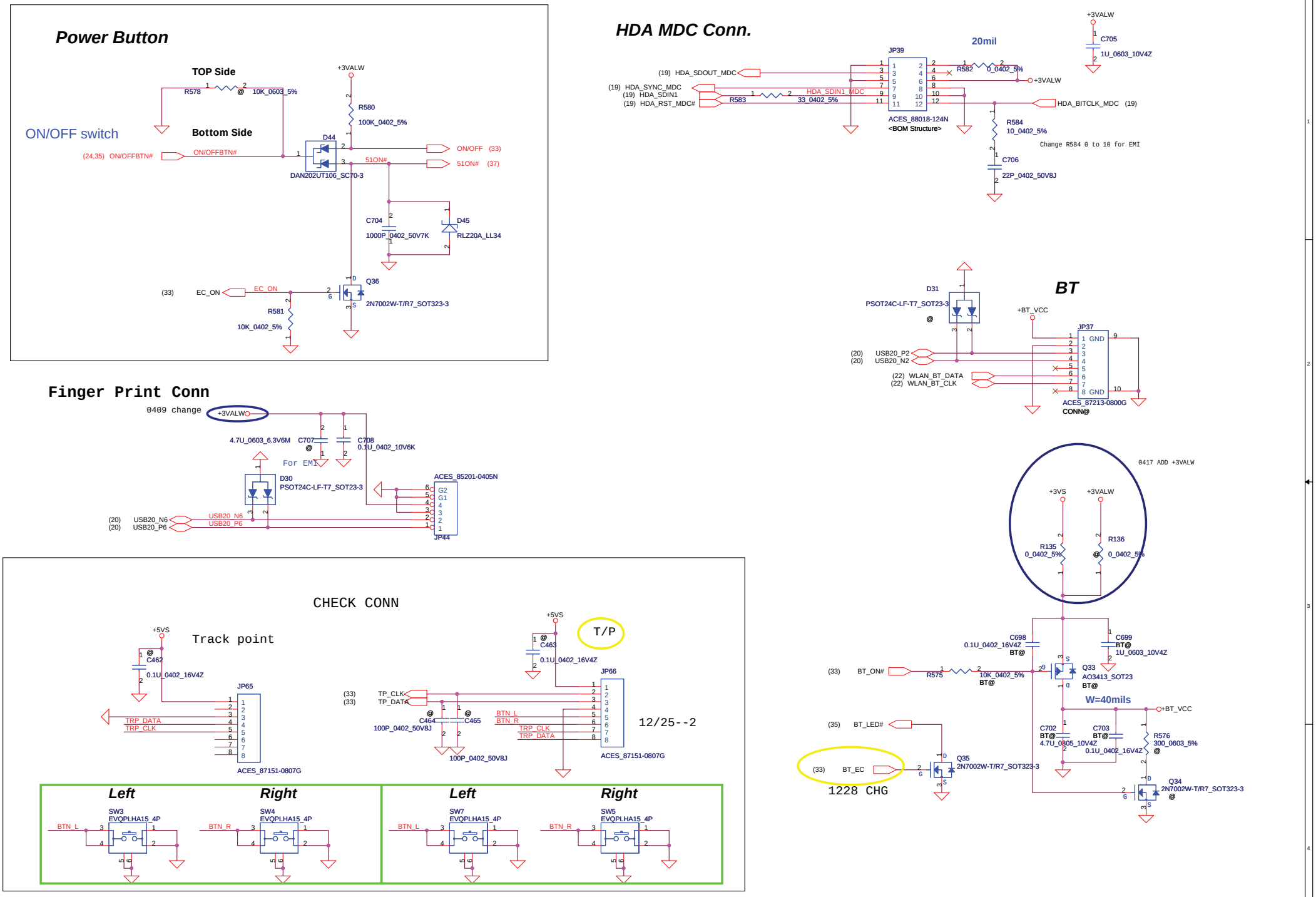

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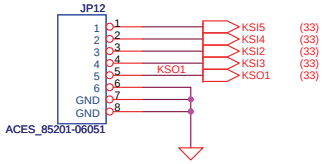
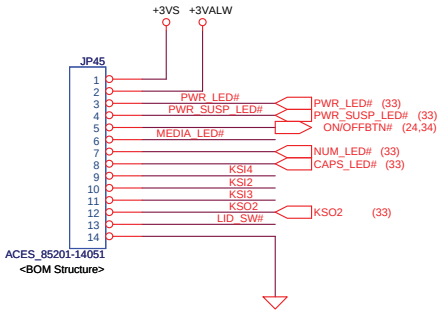
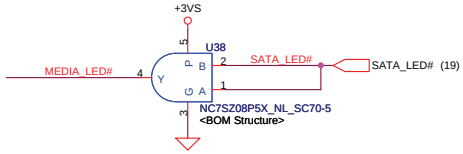
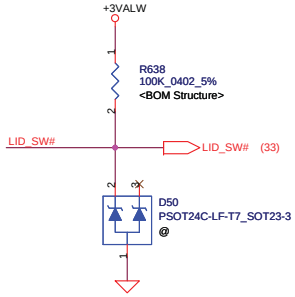
TO S/W B



TO POWER BTN/B







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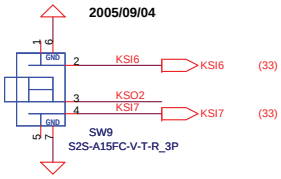
KSI2	SYNC_BTN#	EMAIL_BTN#
KSI3	BRIEF_BTN#	PROGRAM_BTN#
KSI4	LOCK_BTN#	IE_BTN#
KSI5	E-KEY_BTN#	
KSI6		3G ON#
KSI7	WL ON#	BT ON#

0103 Changel

Change +3vs to +3valw

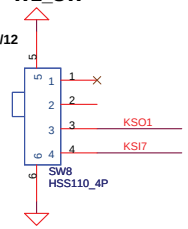
BT_SW & 3G_SW

2005/09/04

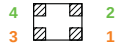


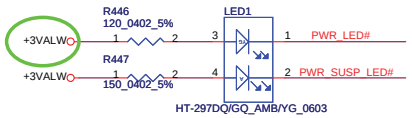
WL_SW

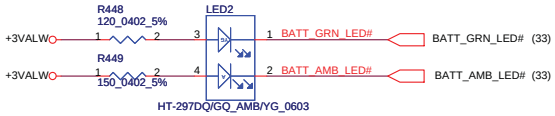
2005/09/12

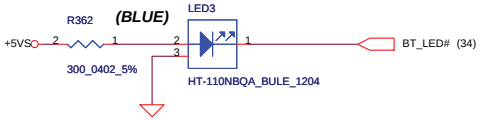


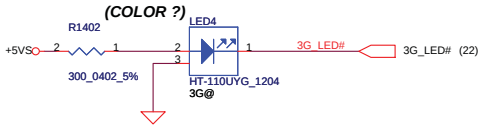
Compal Footprint

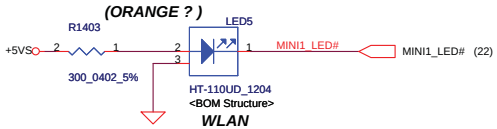


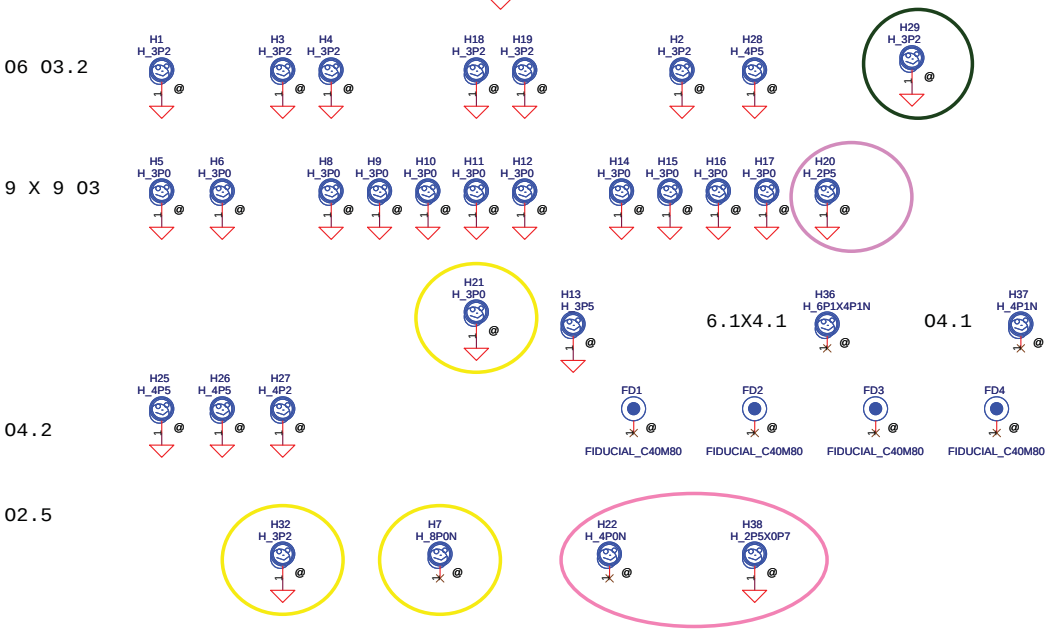












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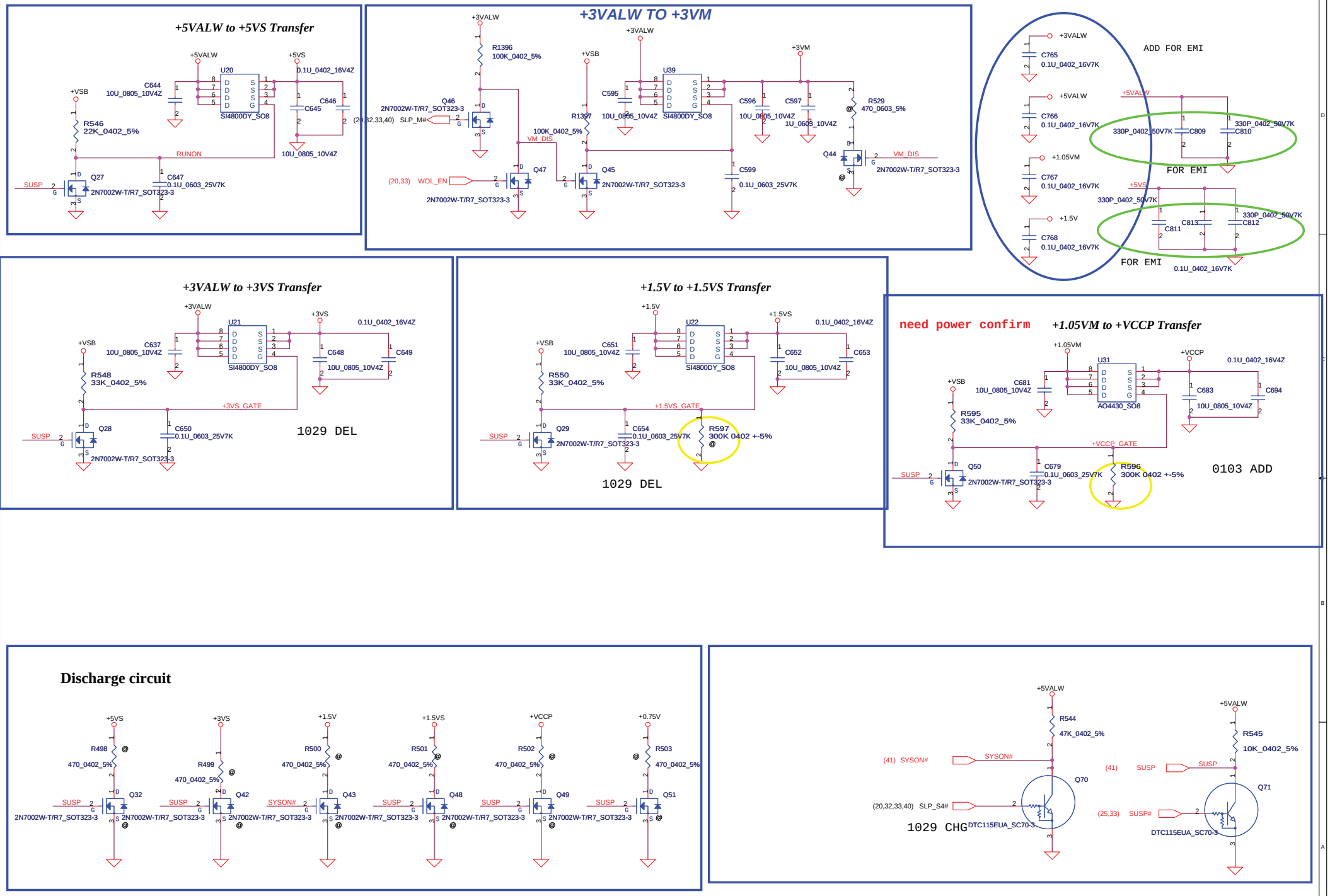

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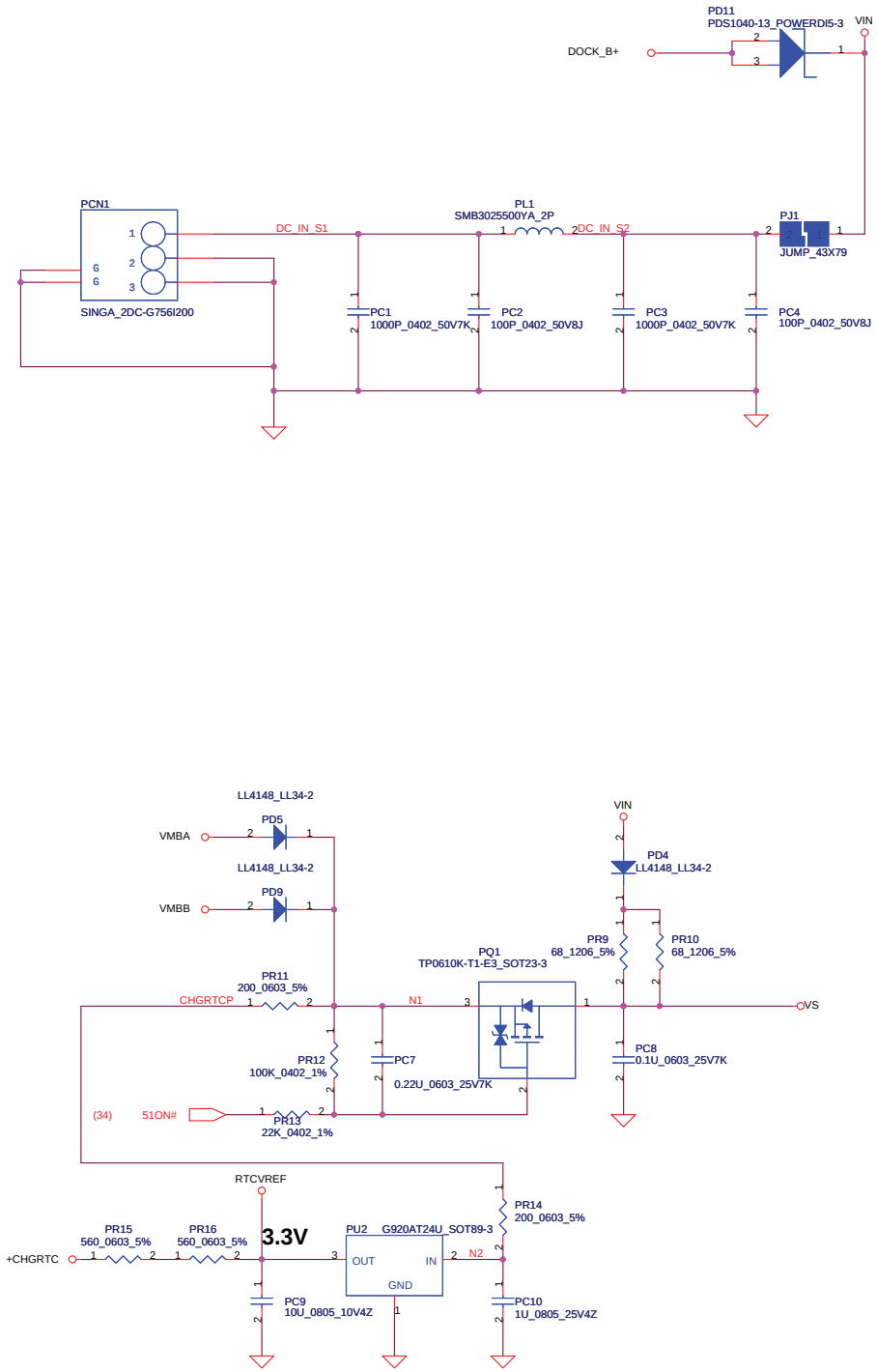

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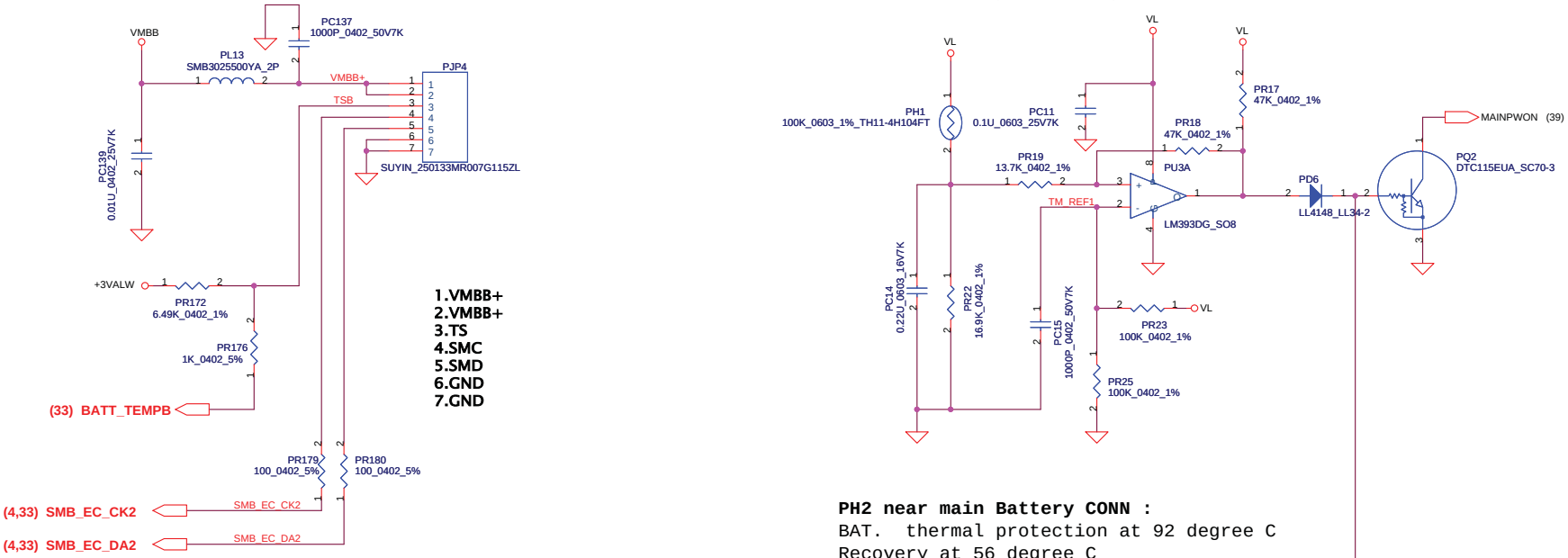
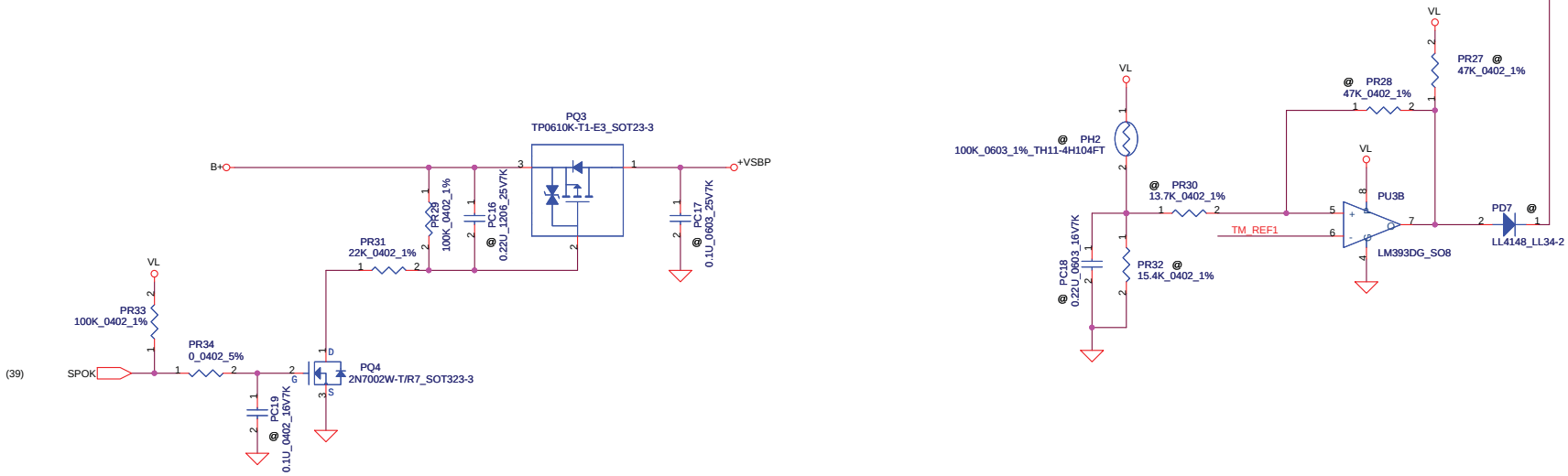
PH1 under CPU botten side :
CPU thermal protection at 86 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title: SCHEMATIC, M/B A4311
				Size: Document Number: 401559 Rev: B
				Date: Friday, July 04, 2008 Sheet 38 of 44

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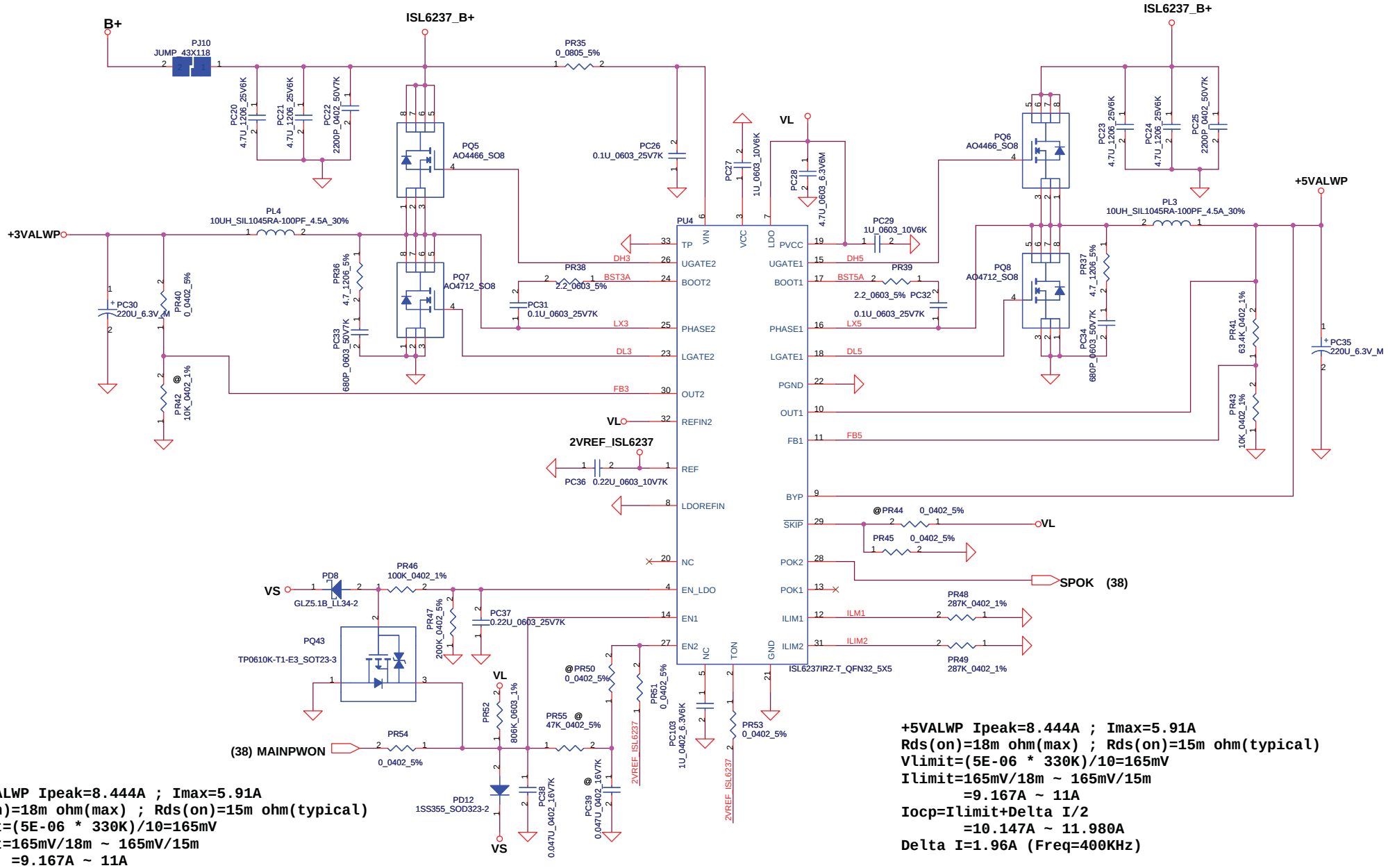

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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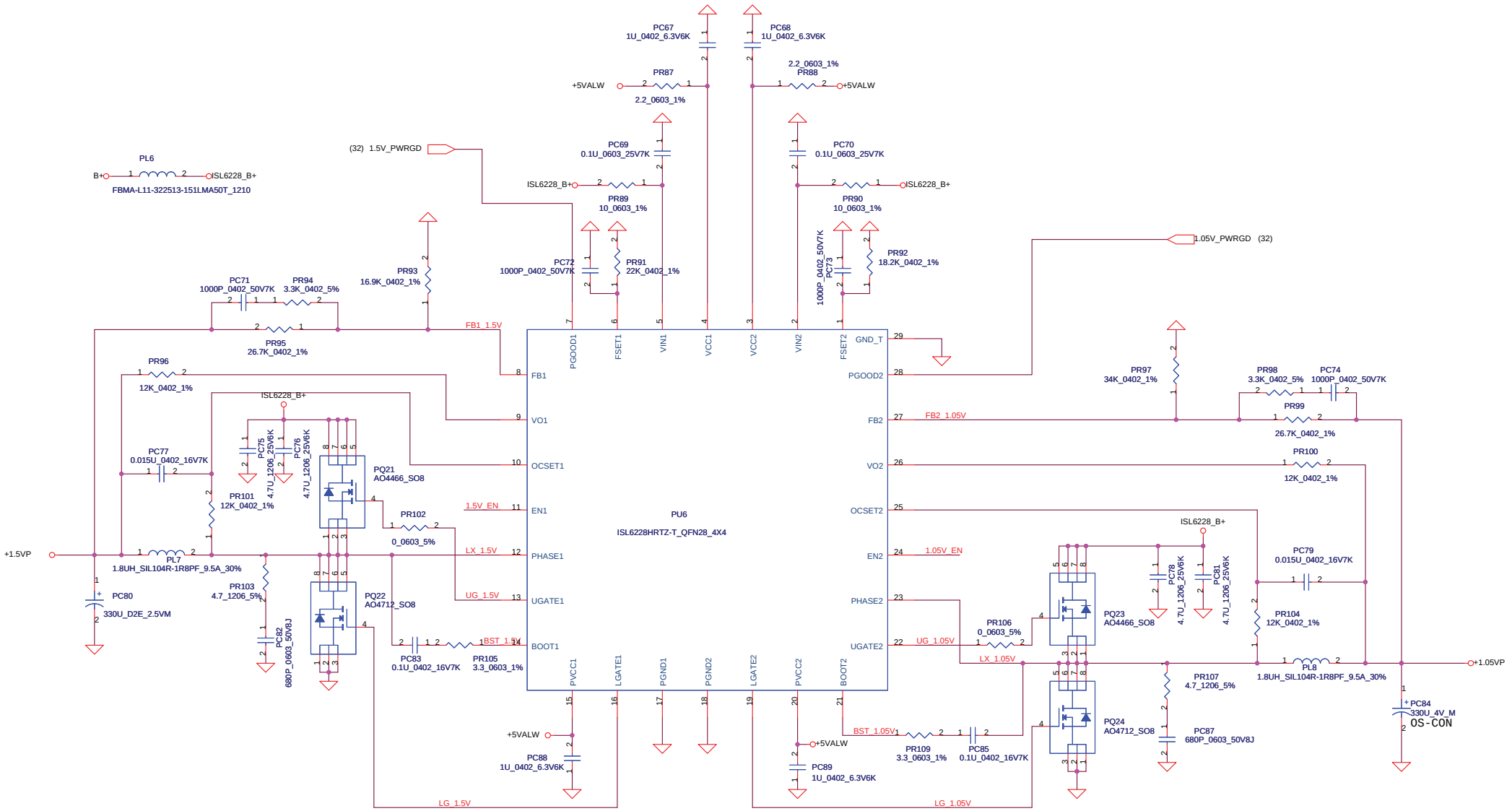

1.05VP Ipeak=8.8A ; Imax=6.16A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=12K ohm
Iocp=12A
Csen=L/(Rocset*DCR)=0.015uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

1.5VP Ipeak=9.45A ; Imax=6.615A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=12K ohm
Iocp=12A
Csen=L/(Rocset*DCR)=0.015uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

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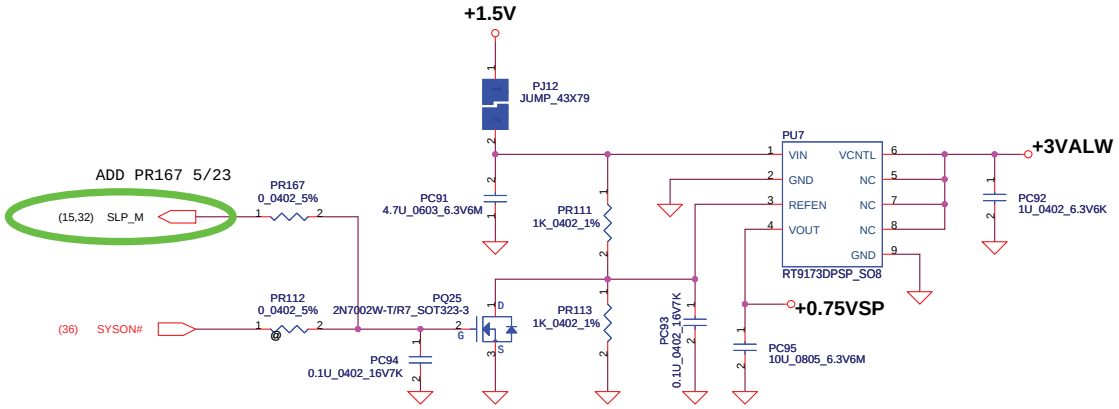

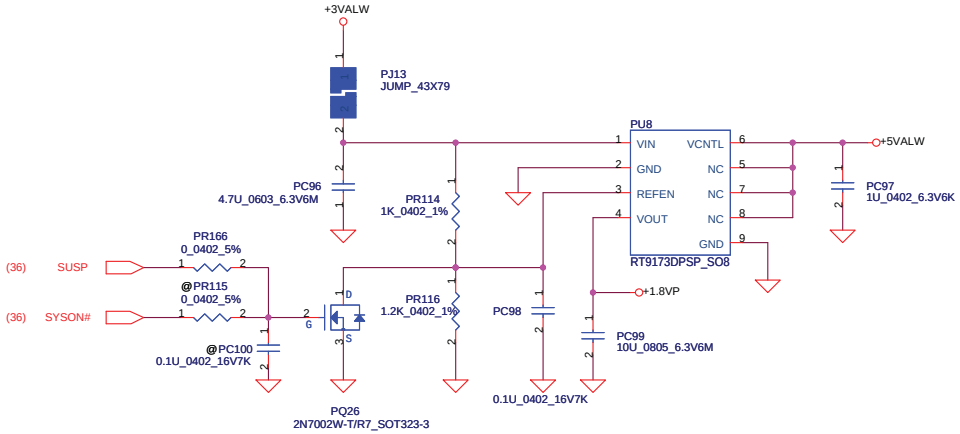

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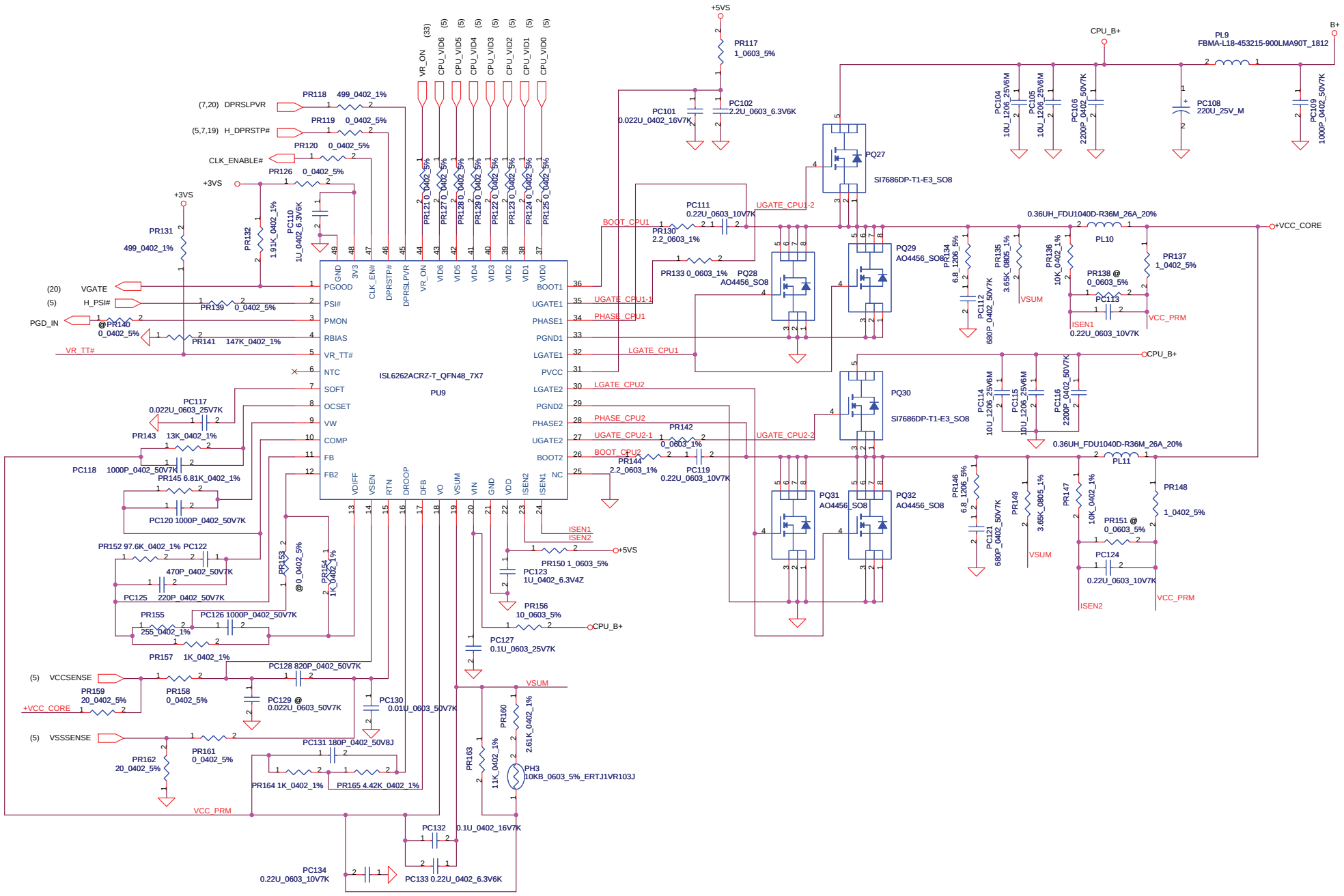

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For 2nd source of ISL6237		39	Add PC103 SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on Pin5 of PU4 to GND	2007 12/26	EVT
2		For EN function of PU4		39	Add PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K)on pin 3 of PQ43 to VS	2007 12/26	EVT
3		Down size		39	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/26	EVT
4		Down size		39	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
5		Down size		37	Change PC7 from 1206 to 0603(SE000005Z80)	2007 12/26	EVT
6		For more current		37	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
7		For more current		37	Change PD1 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
8		Down size		41	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
9		Down size		41	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
10		Down size		41	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
11		Down size		41	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
12		Down size		42	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
13		Down size		42	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
14		Down size		42	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
15		Down size		42	Change PC128 from 0603 to 0402(SE000003W00)	2007 12/26	EVT
16		Down size		38	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
17		Down size		38	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
18		Sourcer request		40	Change PC71、PC74 from NPO to X7R (SE074102K80)	2008 01/14	EVT
19		DFX		37	Delete PD1	2008 01/14	EVT
20		OCP adjust		39	Change PL3、PL4 from 4.7uH to 10uH (SH000002L80)	2008 01/14	EVT
21		OCP adjust		39	Change PR48、PR49 from 330K to 287K (SD000005D80)	2008 01/14	EVT
22	HW request	Set 1.5V==>1.54V, 1.05V==>1.07V		40	Change PR95、PR99 from 25.5K to 26.7K (SD034267280)	2008 01/14	EVT
23	HW request	Set 5V==>5.138V		39	Change PR41 from 61.9K to 63.4K (SD03463K280)	2008 04/17	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Thermal request	Change protect point from 92 to 86 degree C		38	Change PR22 from 15.4K to 16.9K (SD034169280)	2008 04/17	DVT
25		3G EMI request			Delete PR36、PR37、PR103、PR107、PC33、PC34、PC82、PC87 "@" mark	2008 04/22	DVT
26					Change PR105、PR109、PR130、PR144 from 0 to 2.2		
27		3G EMI request		40	Change PR105、PR109 from 2.2 to 3.3	2008 05/21	PVT
28	EPA power	HW request		41	Add PR167, mark "@" PR112	2008 05/27	PVT
29		~~EMI request~~		~~37~~	~~Delete PJ4, add PL12 (SM010020720)~~	~~2008 05/27~~	~~PVT~~ 2008 06/06 delete
30		3G EMI request		39	Change PR38、PR39 from 0 to 2.2	2008 05/29	PVT
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