

Compal Confidential

Model Name :
File Name : LA-8671P

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TN-Note Schematic Document

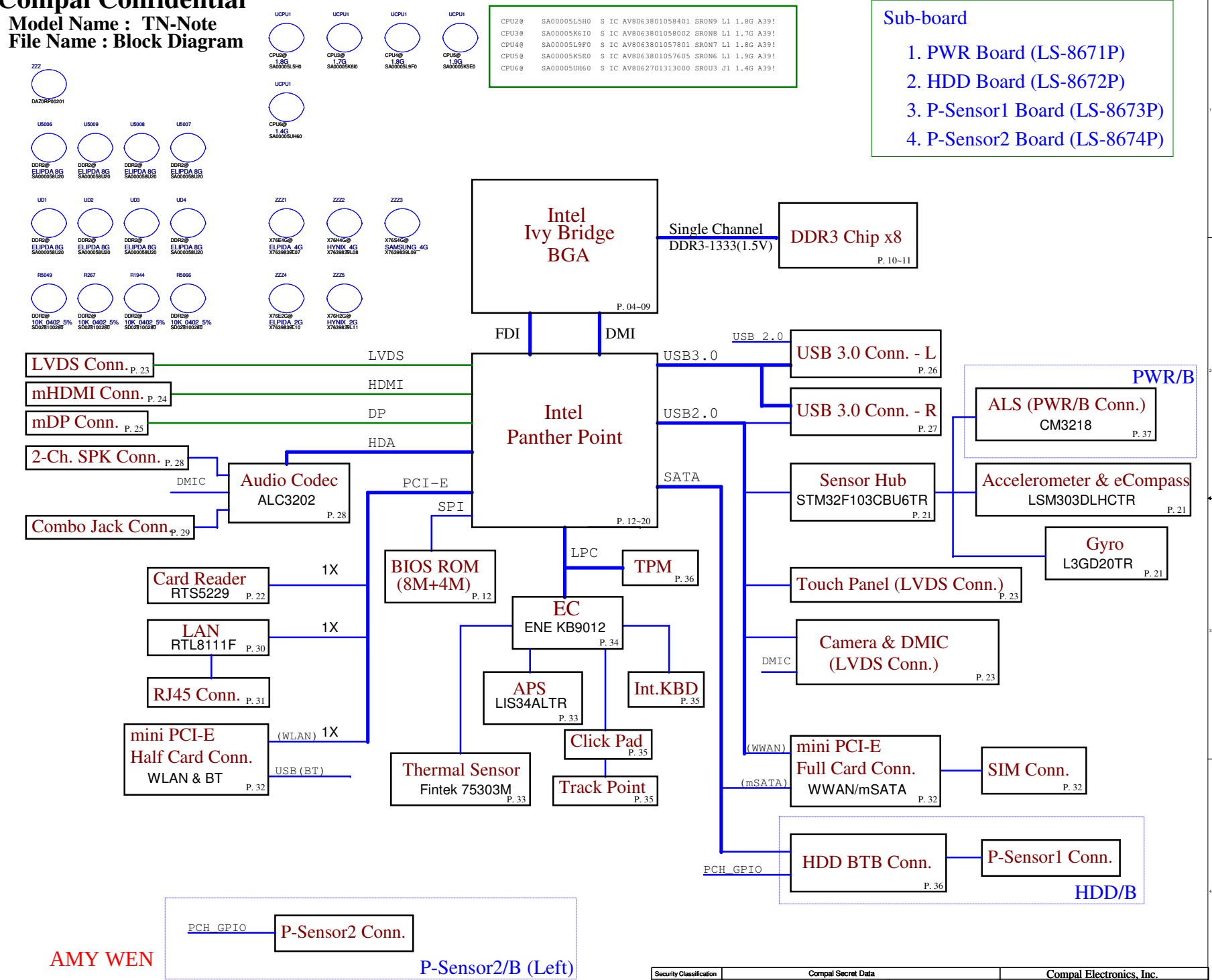
2012-10-04

REV:1A_1004A

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								Size	Document Number	Rev
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Compal Confidential
Model Name : TN-Note
File Name : Block Diagram



Voltage Rails

Power plane					
State	+B	+5VALW +3VALW	+1.5V	+3VM +1.05VM	+5VS +3VS +1.8VS +1.5VS +1.05VS +VCC_GFXCORE_AXG +CPU_CORE +VCCSA +0.75VS
S0	○	○	○	○	○
S3	○	○	○	○	✗
M3	○	○	○	○	✗
S4/S5 - AC	○	○	✗	✗	✗
S4/S5 - BATT ONLY	○	✗	✗	✗	✗
S4/S5 - NO AC & BATT	✗	✗	✗	✗	✗

BOM Structure

	SDV	FVT	SIT	SVT	SOVP
@ : No Stuff					
ME@ : ME components					
CPUx@ : CPU SKU	V	V	V	V	V
DDRx@ : RAM SKU	V	V	V	V	V
SBA@ : SBA	V	V	V	V	V
NOSBA@ : NO SBA					
ID4@ : Intel Deep S4	V				
AOAC@ : AOAC	V	V	V	V	V
TPM@ : TPM		V	V	V	V
Short@ : 0ohm short pad					

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BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON	H	H	H	ON	ON	ON
S3 (Suspend to RAM)	L	H	H	ON	ON	OFF
S4 (Suspend to Disk)	L	L	H	ON	OFF	OFF
S5 (Soft OFF)	L	L	L	ON	OFF	OFF

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	Thermal sensor	1001-101xb	9AH
Charger	0001-0010b	12H	PCH (SML1DATA / GPIO75)	1001-0110 b	96H

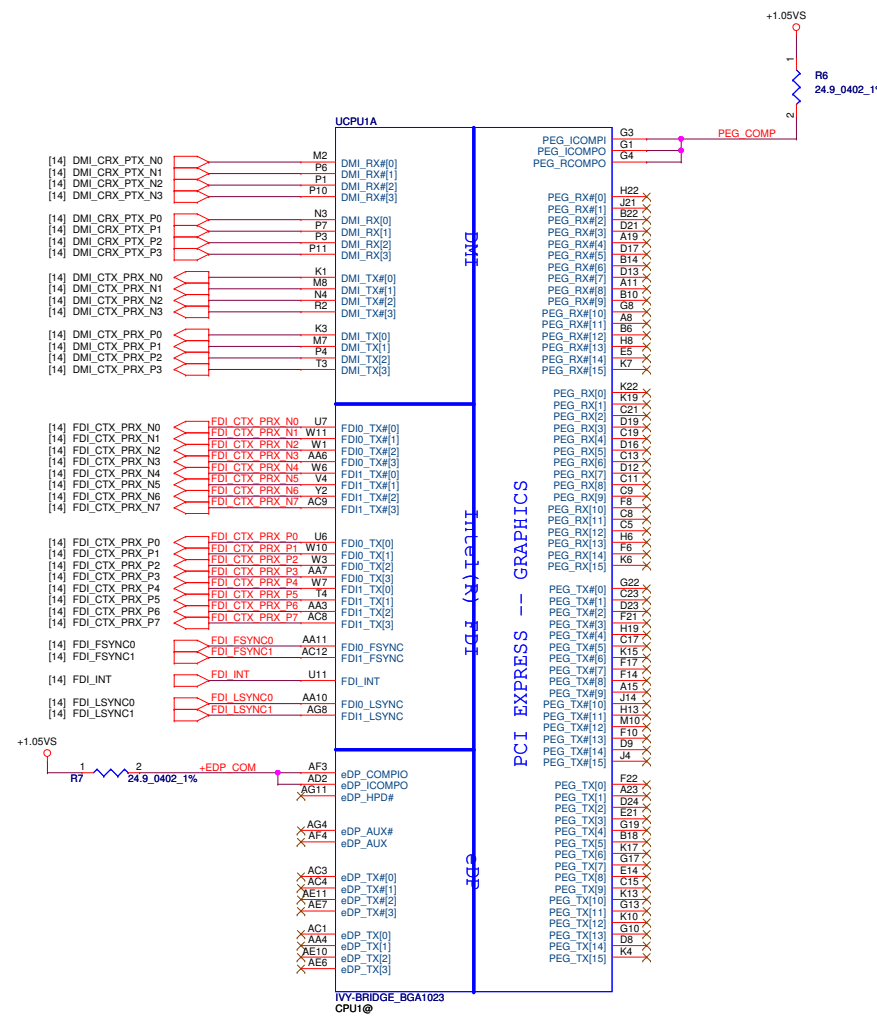
Device	Address	HEX
Security Rom	1010-100xb	A8 H
DDR DIMMO	1010-000xb	A0 H

Device	Address	HEX
No-use	No-use	No-use

Device	Address	HEX
ALS	0100-100xb	48h
APS	0011-001xb	32h
Gyroscope	0110-101xb	6Ah
e-Compass	0011-110xb	3Ch

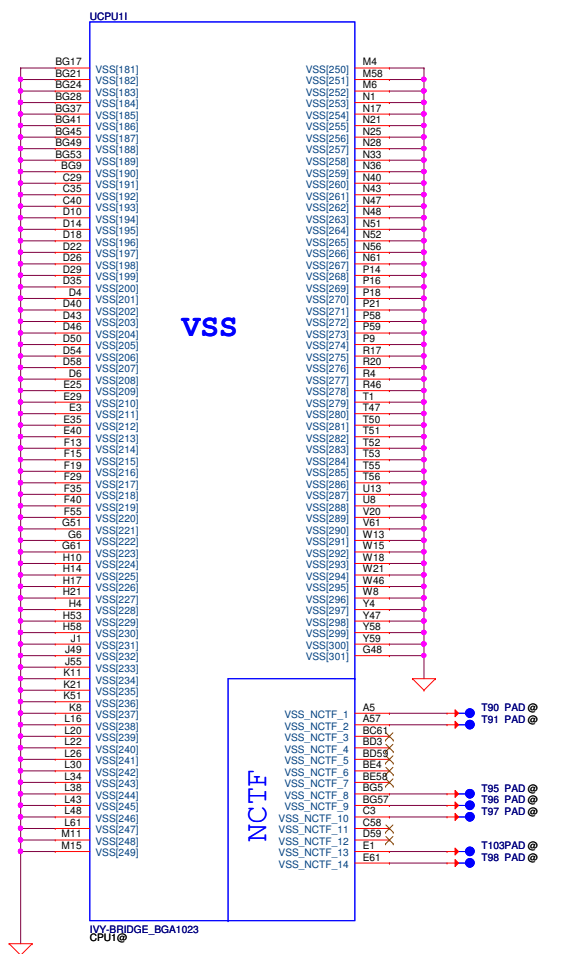
USB3.0	USB2.0	NOTE
1	0	
2	1 *	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	✗
	7	✗
	8	Touch Panel
	9 *	WWAN
	10	WLAN
	11	Finger Printer**
	12	
	13	Bluetooth**

* Debug Port
** Not Use



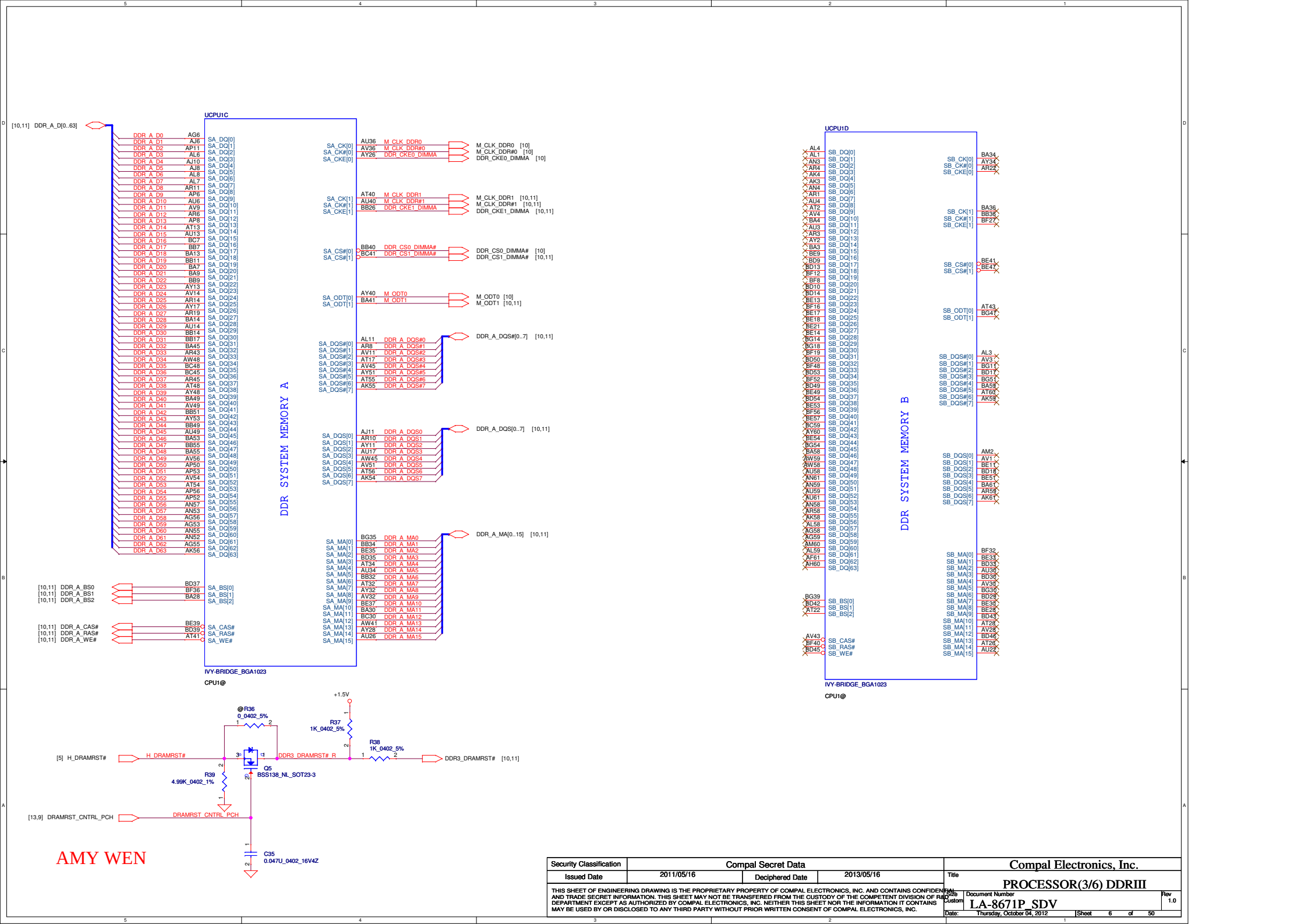
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

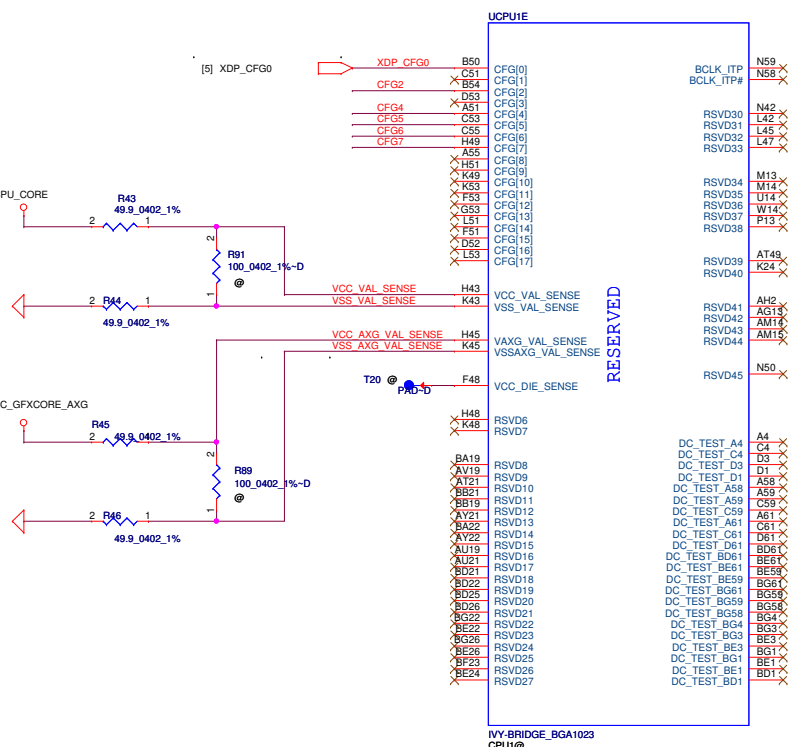
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--



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								Size	Document Number	Rev
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								Date:	Thursday, October 04, 2012	Sheet





CFG Straps for Processor

CFG2

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map 0: Lane Reversed
------	--

CFG4

Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

CFG6

PCIE Port Bifurcation Straps

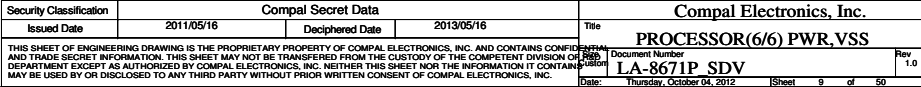
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	---

CFG7

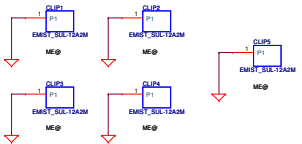
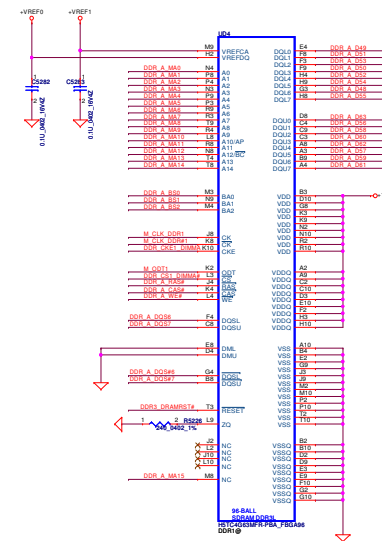
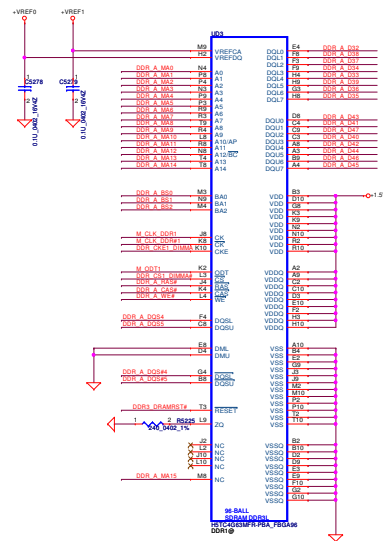
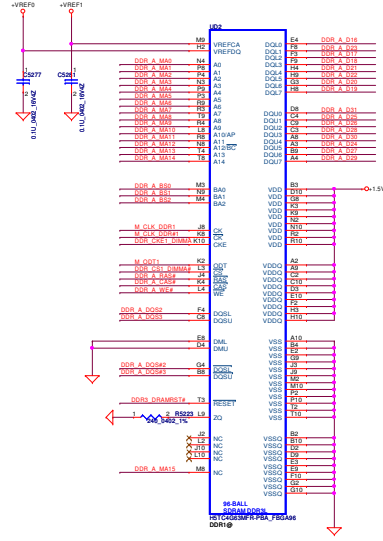
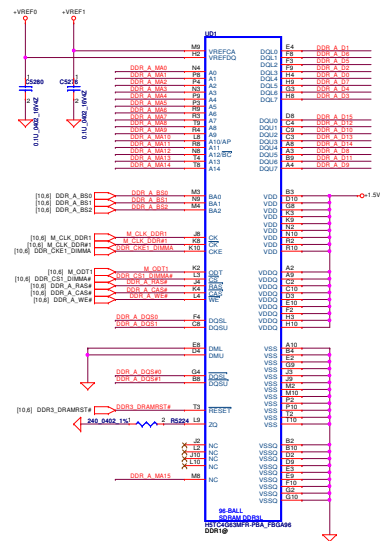
PEG DEFER TRAINING

CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	--

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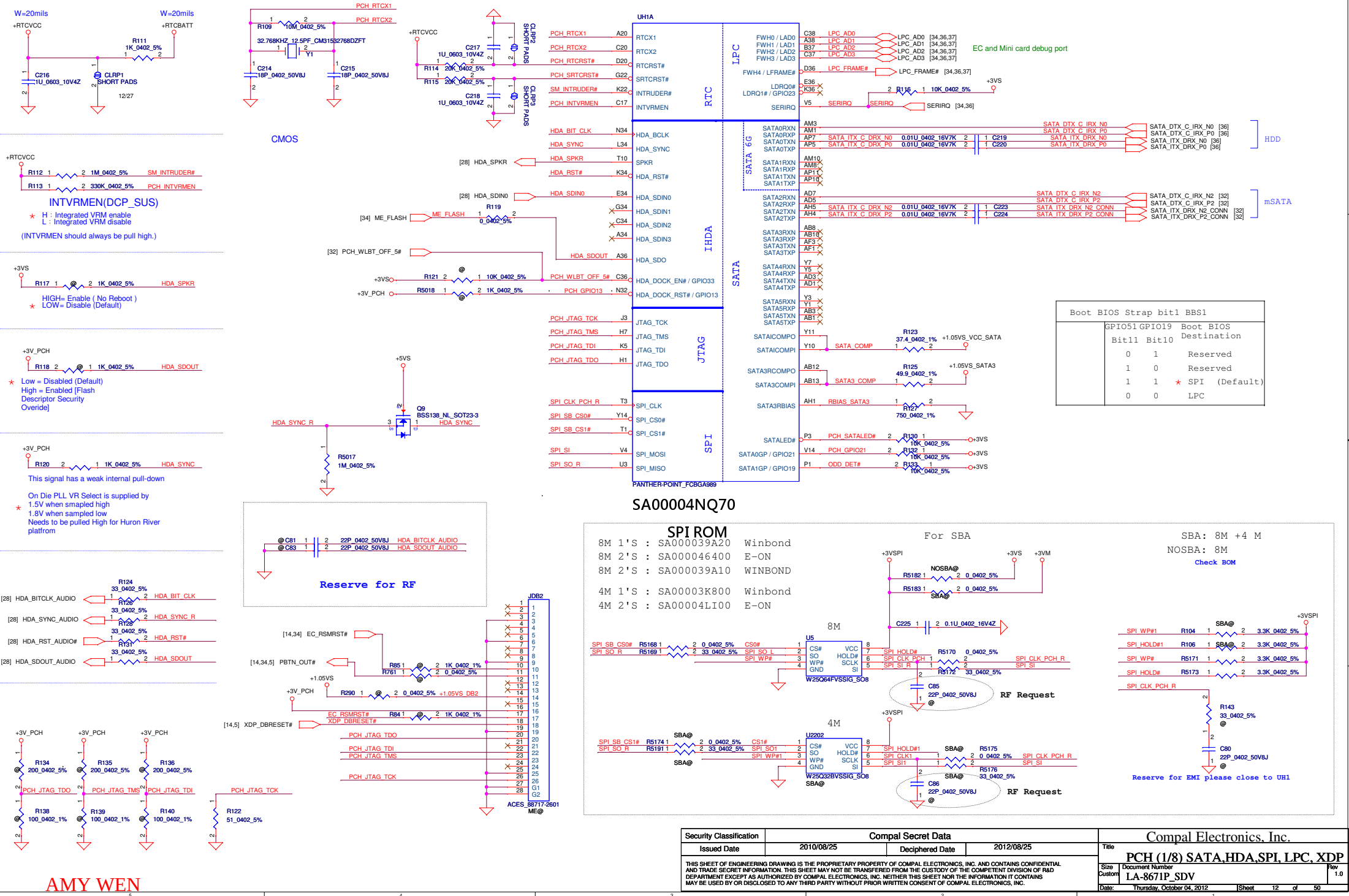


[16A] DDR_A_M0D_15
 [16A] DDR_A_DQ60-7
 [16A] DDR_A_DQ60-7
 [16A] DDR_A_DQ60-7
 [16A] DDR_A_DQ60-7



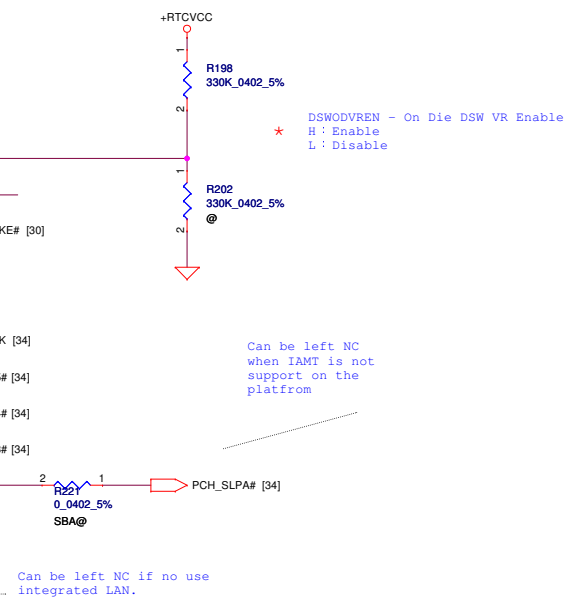
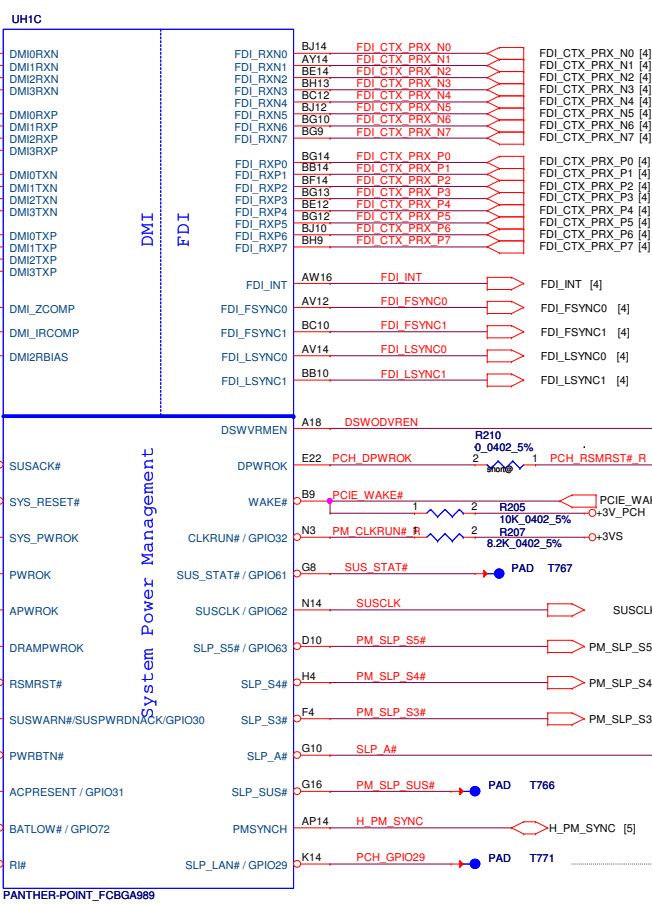
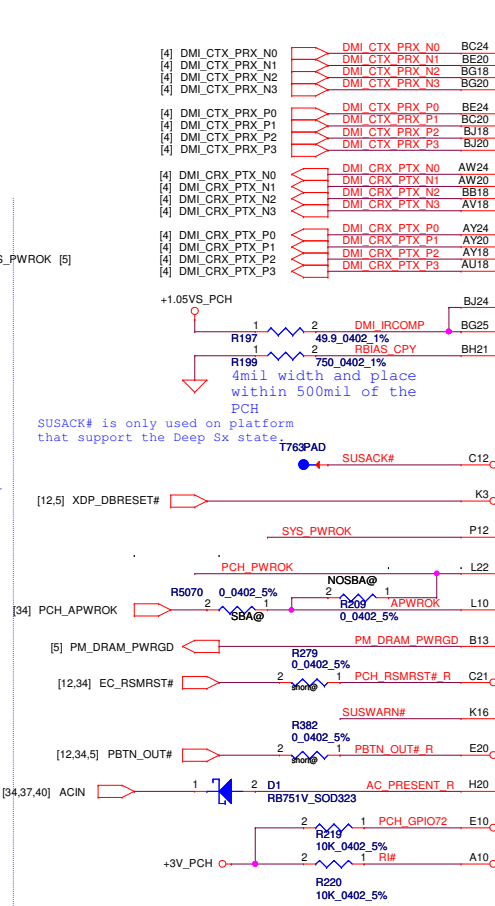
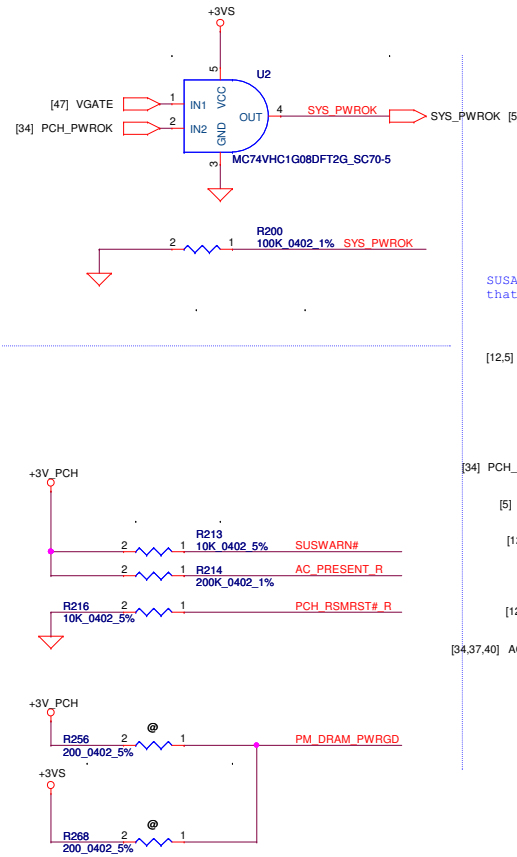
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2013/05/16		
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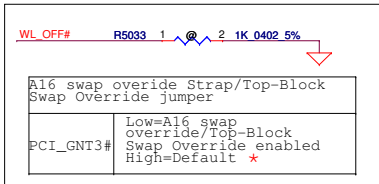
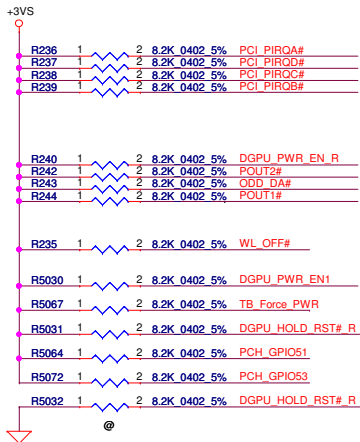
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		Deciphered Date		PCH (1/8) SATA,HDA,SPI, LPC, XDP	
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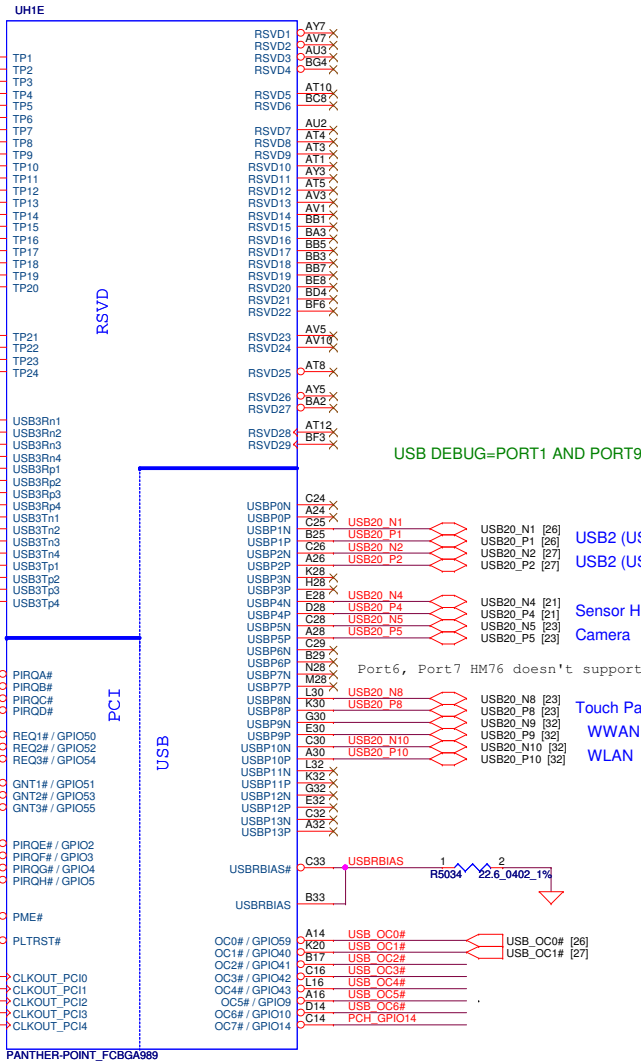
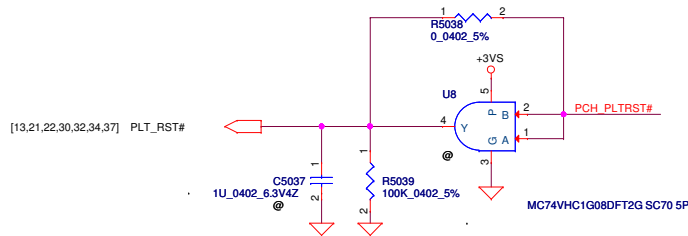
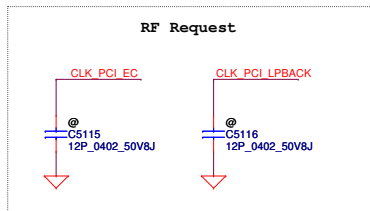
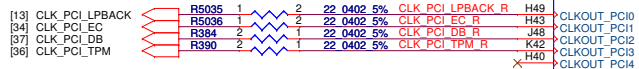
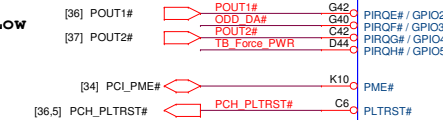


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Default: Active Low



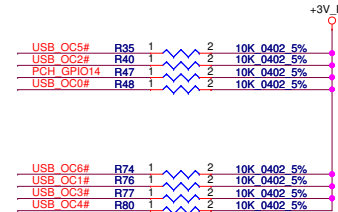
USB DEBUG=PORT1 AND PORT9

Port6, Port7 HM76 doesn't support

Touch Panel
WWAN
WLAN

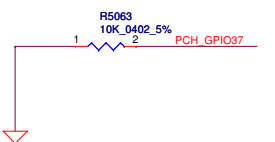
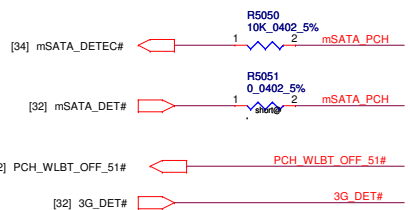
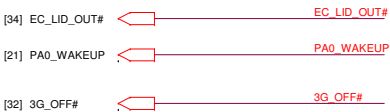
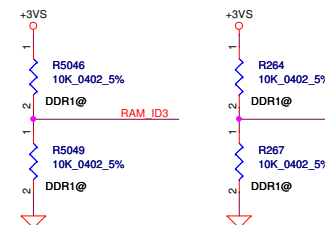
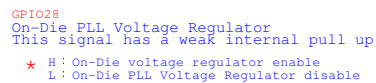
USB3.0	USB2.0	NOTE
1	0	
2	1 *	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	X
	7	X
	8	Touch Panel
	9 *	WWAN
	10	WLAN
	11	Finger Printer**
	12	
	13	Bluetooth**

* Debug Port
** Not Use

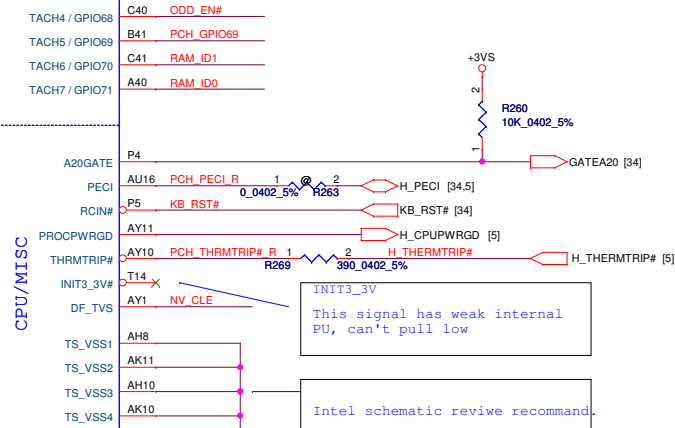
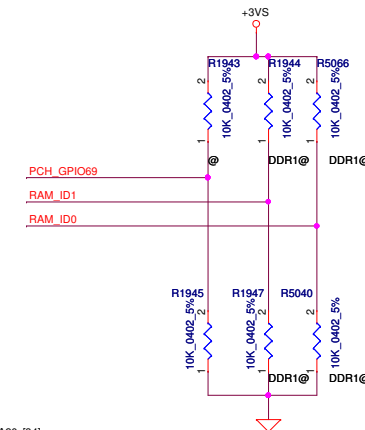
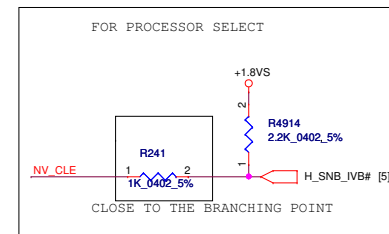
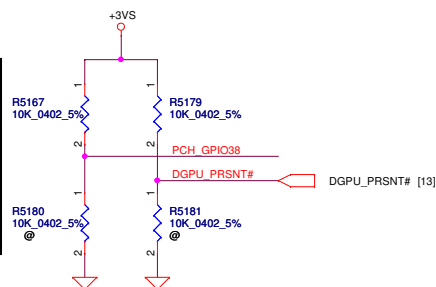
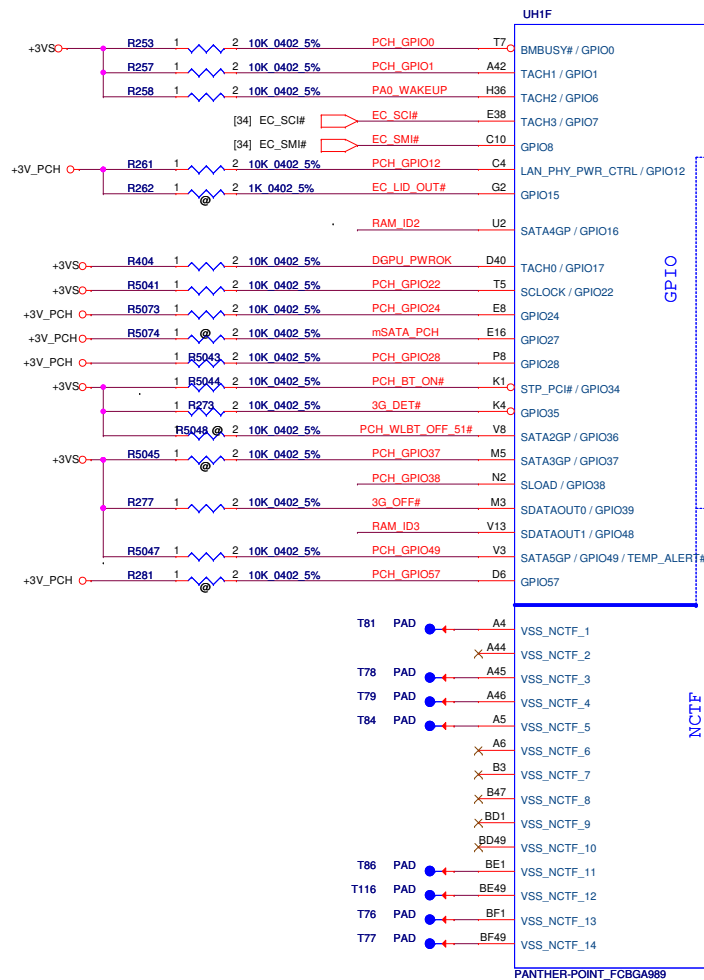


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								PCH (5/9) PCI, USB					
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						Date		LA-8671P_SDV				1.0	
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PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function	GPU_ID
0	0	0	PX4.0	0
0	0	1	Reserved	1
0	1	0	DIS	2
0	1	1	UMA	3



RAM_ID3 <i>GPI048</i>	RAM_ID2 <i>GPI016</i>	RAM_ID1 <i>GPI070</i>	RAM_ID0 <i>GPI071</i>	RAM
0	0	0	0	ELPIDA 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	HYNIX 4GB
0	0	1	1	ELPIDA 8GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	HYNIX 8GB
0	1	1	0	ELPIDA 2GB
0	1	1	1	SAMSUNG 2GB
1	0	0	0	HYNIX 2GB
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

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				Rev	1.0

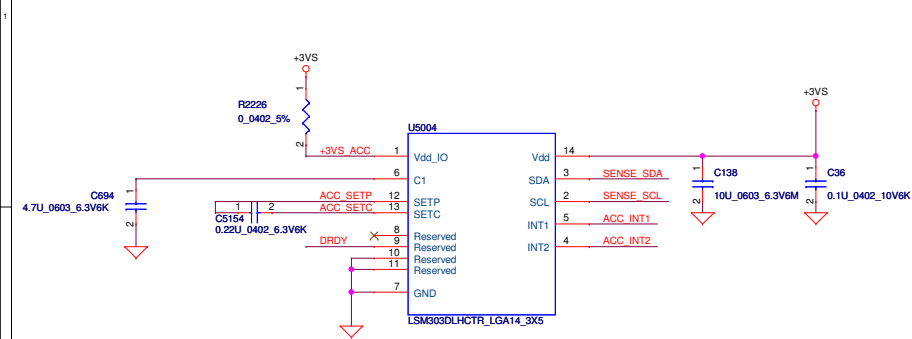


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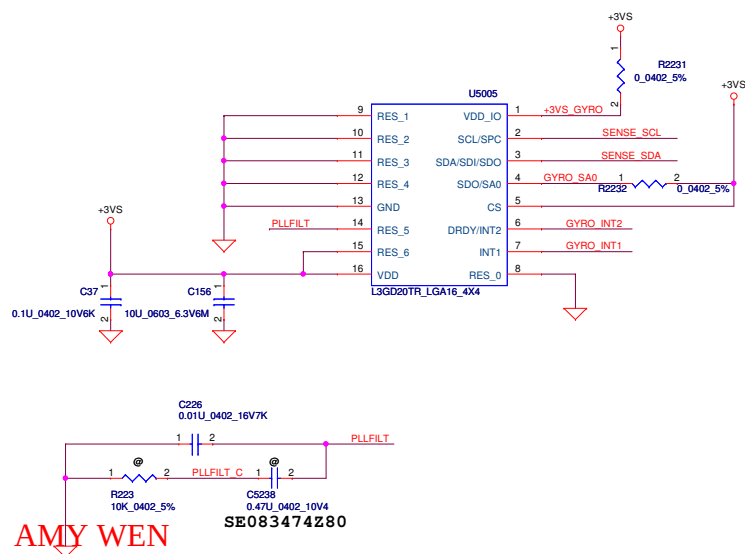
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		2012/08/25		Title	
				PCH (9/9) VSS	
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Accelerometer + eCompass



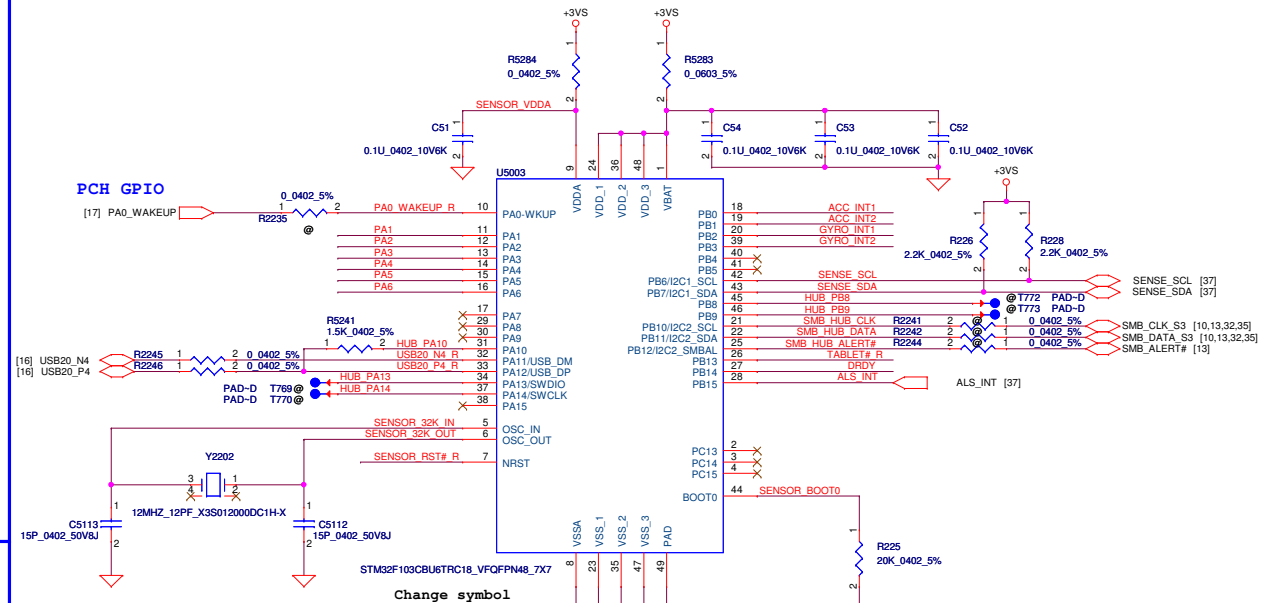
Gyro



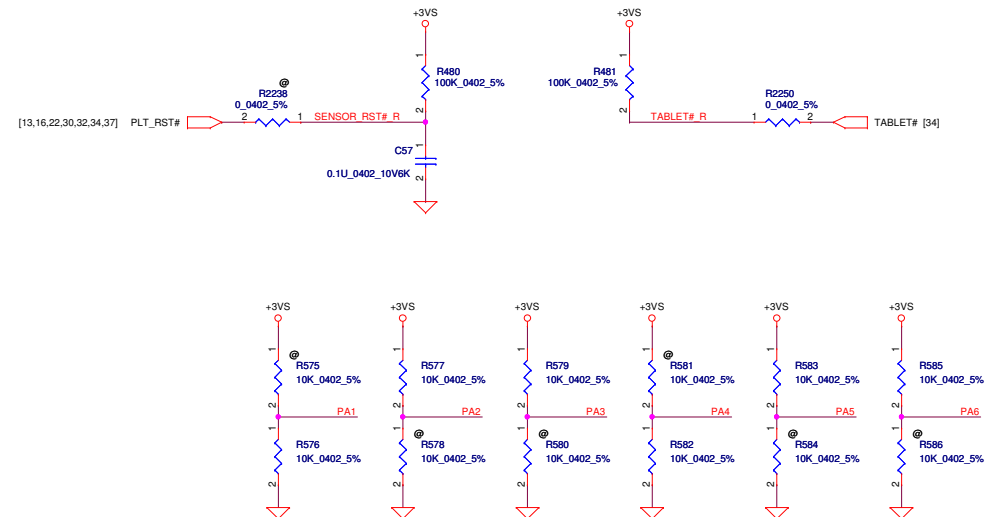
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SE083474Z80

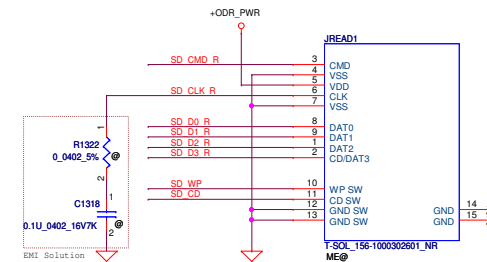
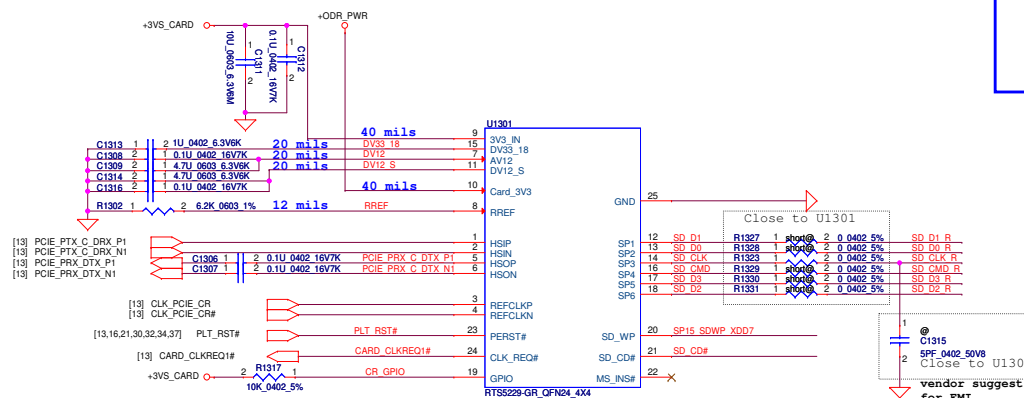
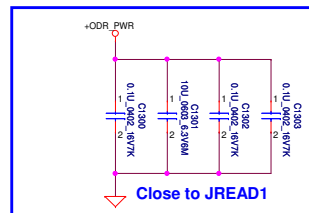
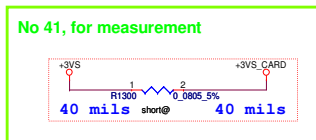
Sensor Hub



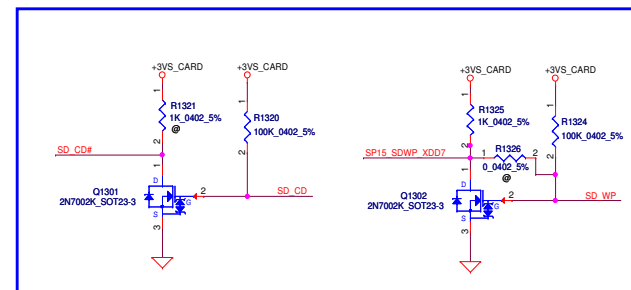
Change symbol



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	SD_CD	SD_WP
CARD UNINSERTION	Close (Low)	Close (Low)
CARD HALF INSERTION	Close (Low)	Open (High)
CARD INSERTION	Open (High)	Close (Low)



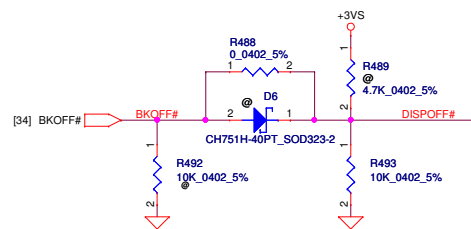
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Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2011/05/16	Card Reader
Deciphered Date	2013/05/16	Size
Document Number	LA-8671P_SDV	Rev
Date	Thursday, October 04, 2012	1.0
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W=60mils

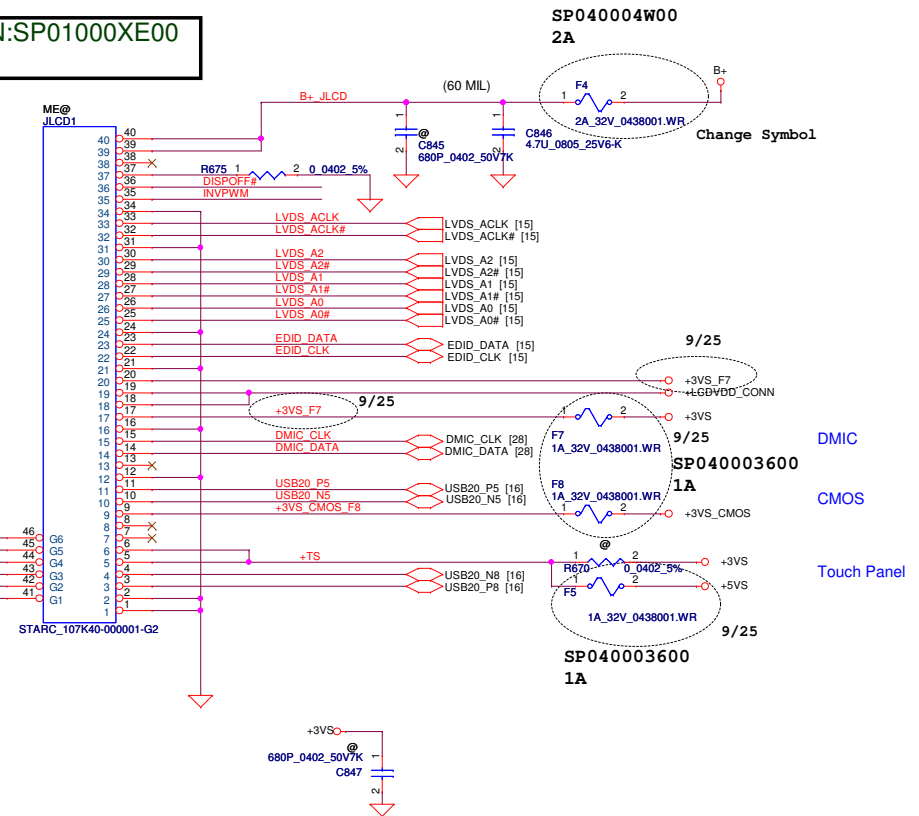
LCD POWER CIRCUIT

For GMCH DPST

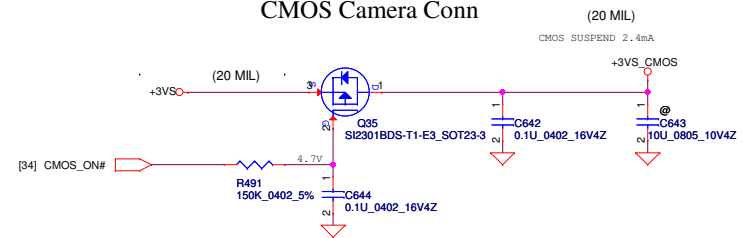


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PN:SP01000XE00

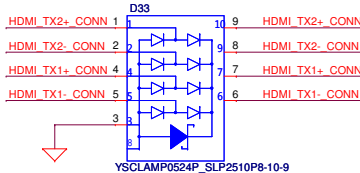
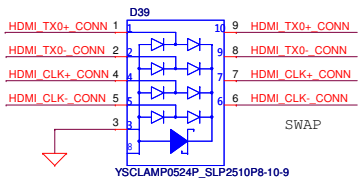
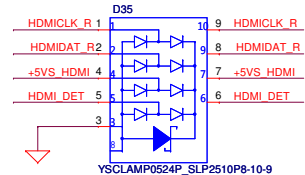
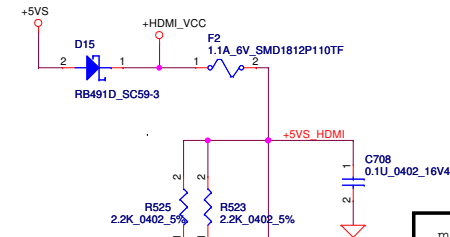
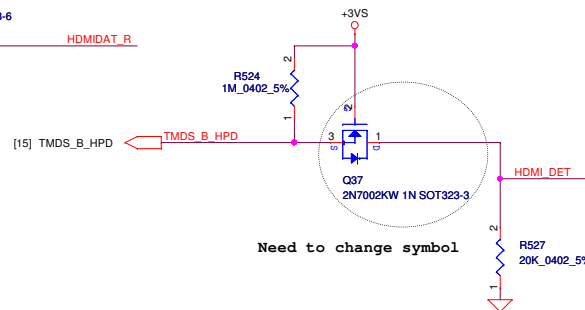
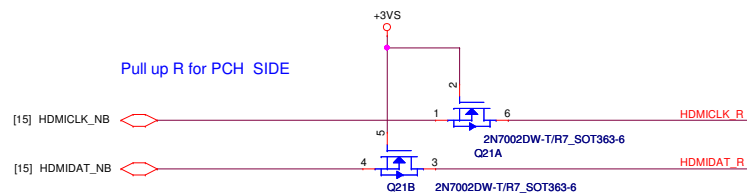
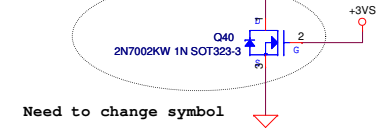
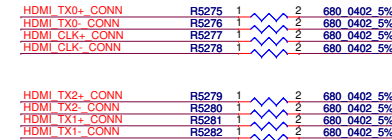
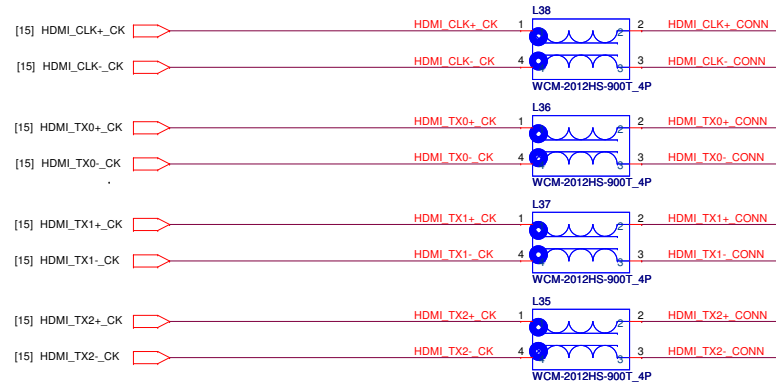


CMOS Camera Conn



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				Document Number	1A
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PN:SM070001S00x 4

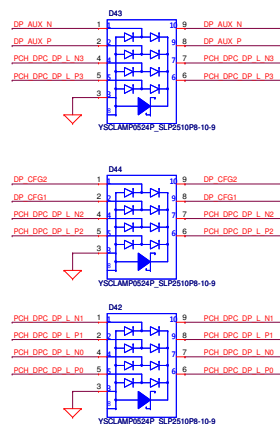
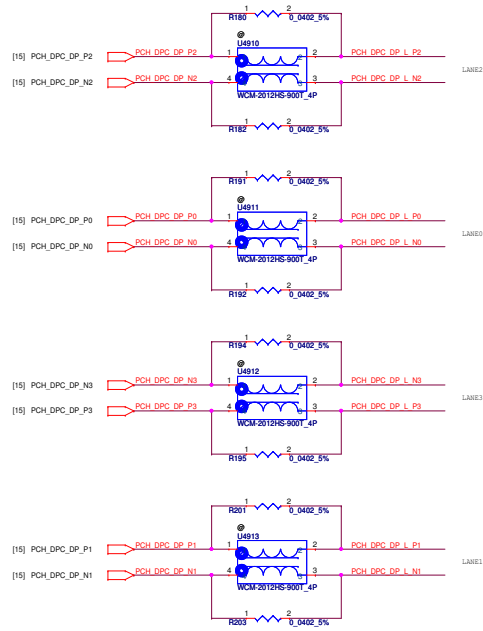


1'SPN: SC300001Y00
2'SPN: SC300002800

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				Size	Document Number	Rev
				Custom	LA-8671P_SDV	1.0
				Date:	Thursday, October 04, 2012	Sheet 24 of 50

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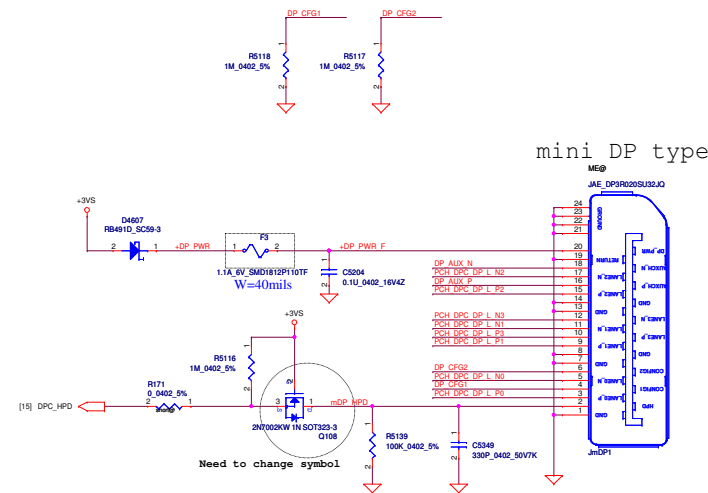
Close to JmDP1



The schematic diagram illustrates the HDMI interface circuit for the T1000. It features several MOSFETs (Q2306A, Q2306B, Q2308A, Q2308B, Q2307A, Q2307B) and resistors (R5137, R5158, R5146, R5162) connected to various signals. The circuit is powered by +3VS and +5VS. The signals are labeled as [15] PCH_DPC_DAT, [15] PCH_DPC_CLK, [15] PCH_DPC_AUXN_C, [15] PCH_DPC_AUXP_C, and DP_AUX_N. The output signals are DP_AUX_N, DP_AUX_P, and DP_CFG1.

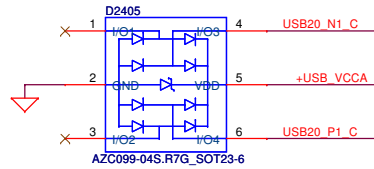
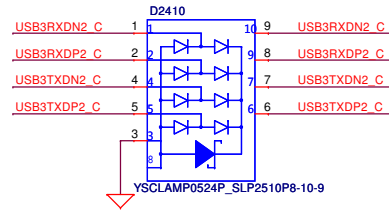
TBT, HDMI, DP mode table

HPD	CFG1	CFG2	LSRX	Mode
1	0	0	X	DP
1	1	X	X	HDMI
0	0	1	1	TBT



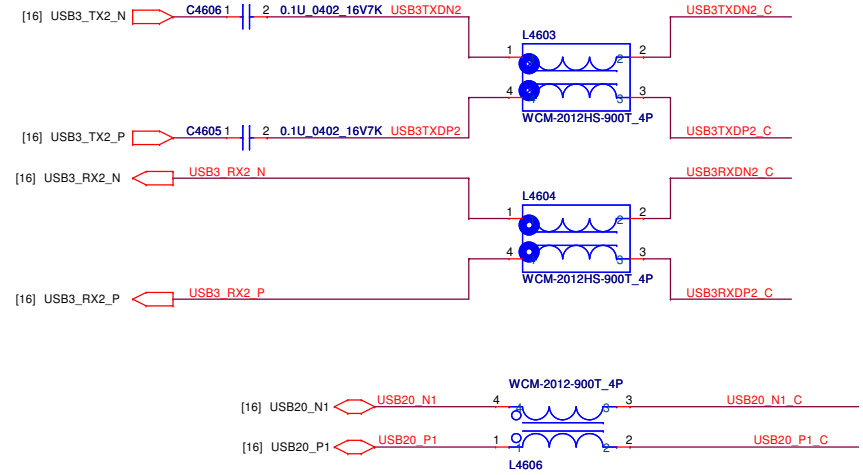
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2'SPN: SC300002800

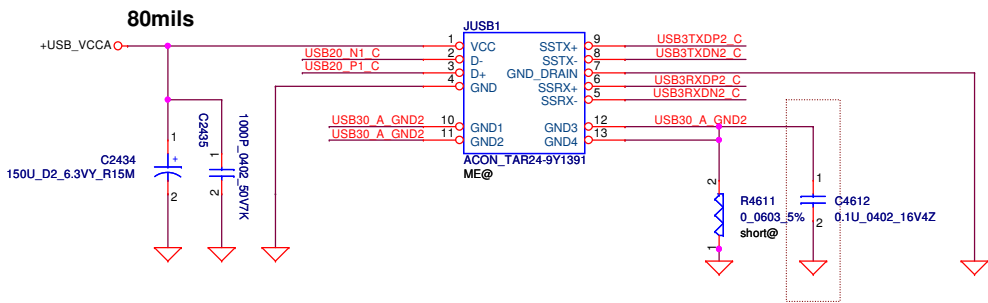
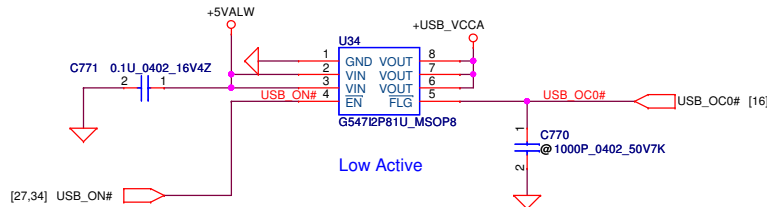


1'S PN: SC300001G00
2'S PN: SC300002E00

JUSB1USB3.0/USB2.0



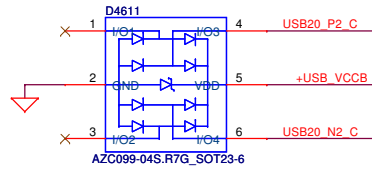
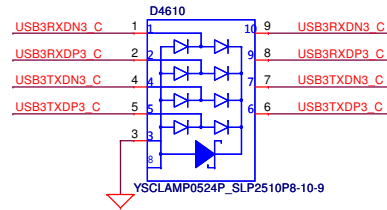
DC23300A410



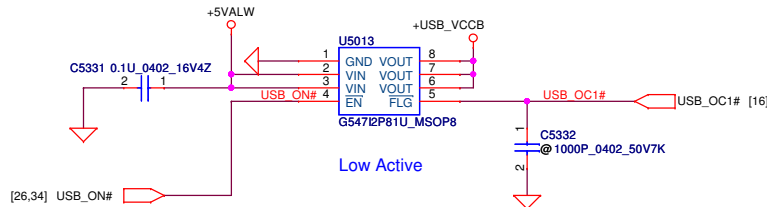
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Size	Custom	Document Number	LA-8671P_SDV	Rev	1.0
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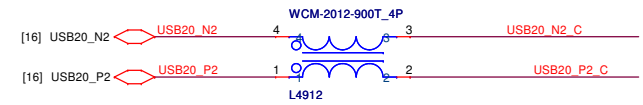
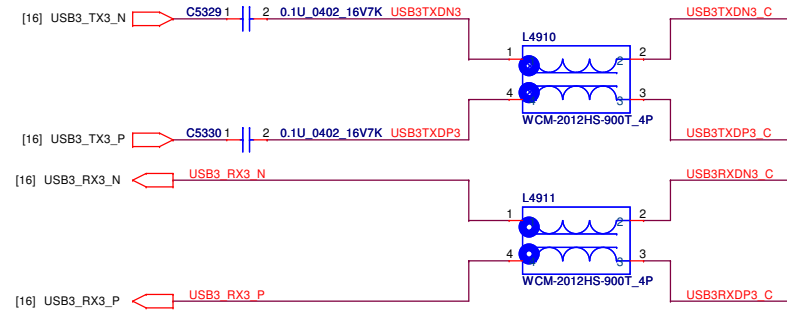
1'SPN: SC300001Y00
2'SPN: SC300002800



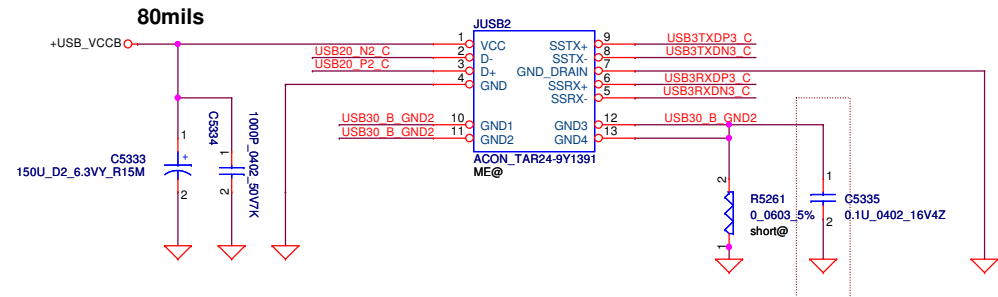
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2'S PN: SC300002E00



JUSB1USB3.0/USB2.0



DC23300A410

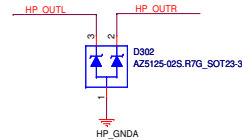
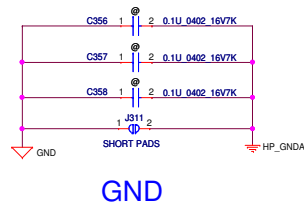
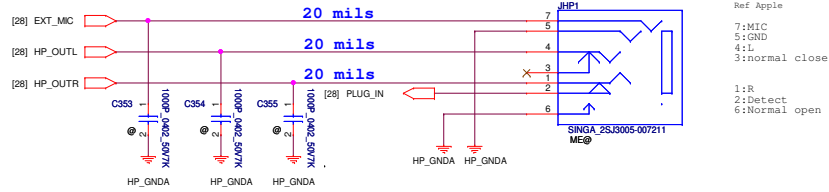


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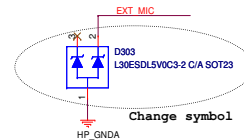
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Size	Custom	Document Number	LA-8671P_SDV	Rev	1.0
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PN:DC230008E00

Choose normal-open type!



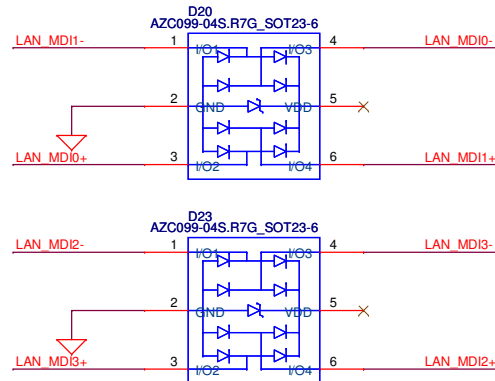
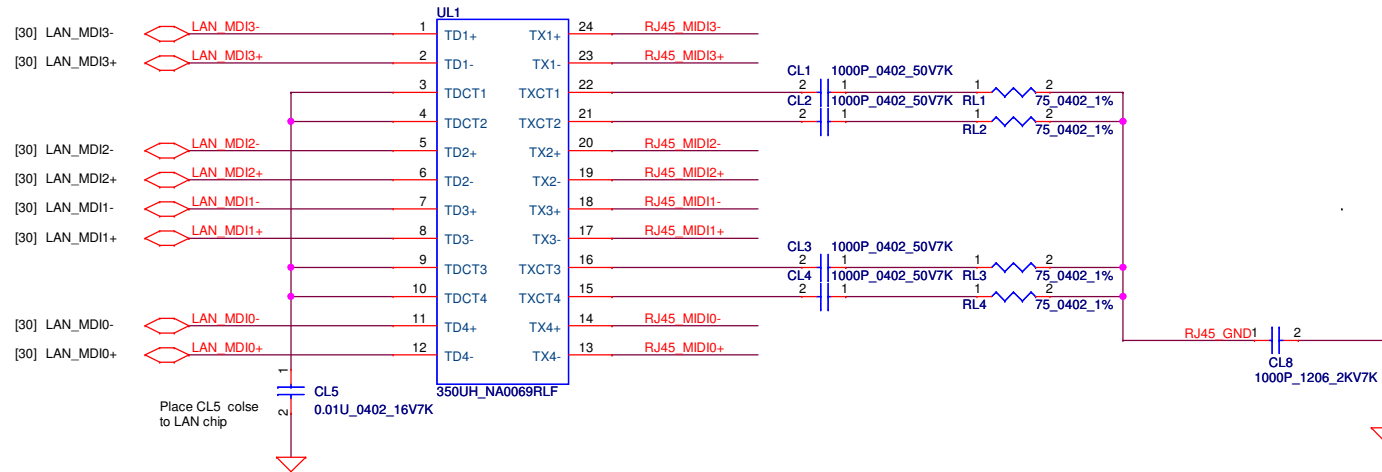
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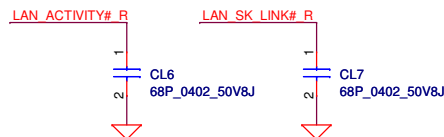
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				Date: Thursday, October 04, 2012	Sheet 29 of 50



D20/D23
1'S PN:SC300001G00
2'S PN:SC300002E00

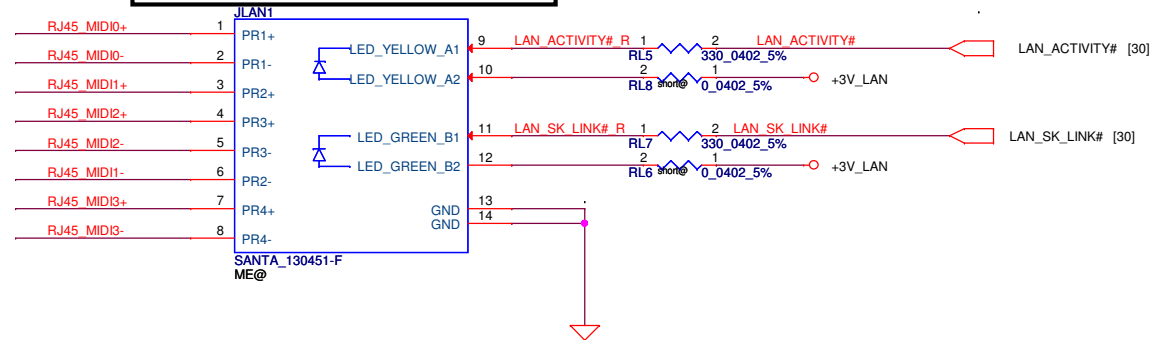
For EMI's request



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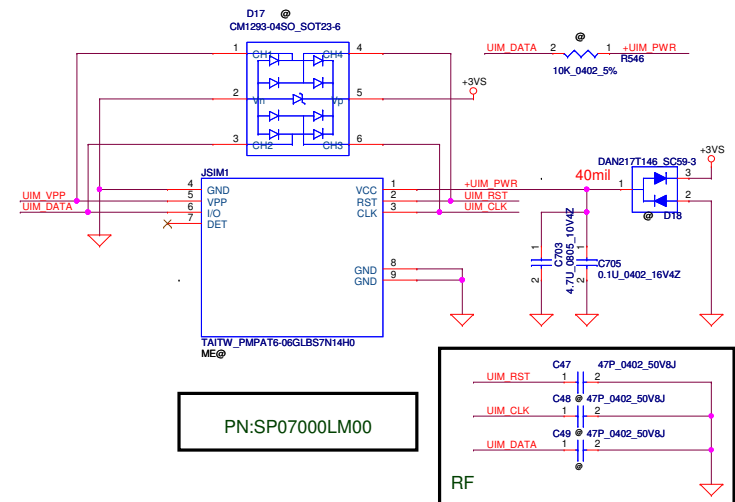
DC234005300
LAN Conn.

RL5,RL7 Vendor recommend 510 ohm

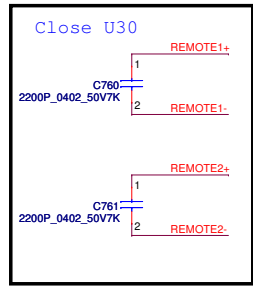


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				Size Custom	Document Number
				LA-8671P_SDV	
Date: Thursday, October 04, 2012		Sheet 31 of 50		Rev 1.0	

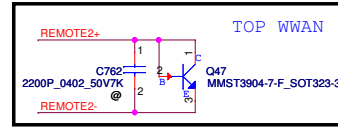
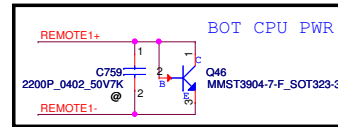
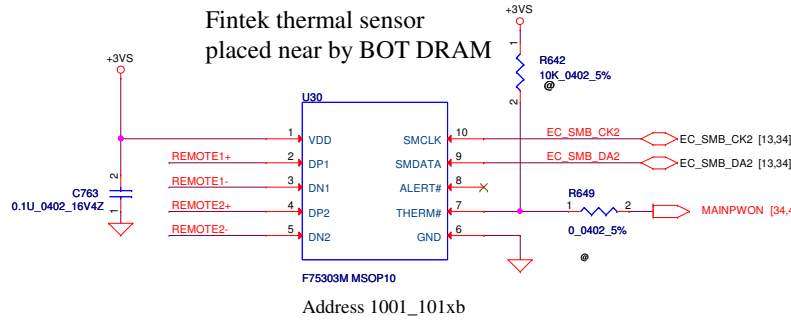
Mini-Express Card(WLAN/BT Combo)



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Date:	Thursday, October 04, 2012	Sheet	32	of	50

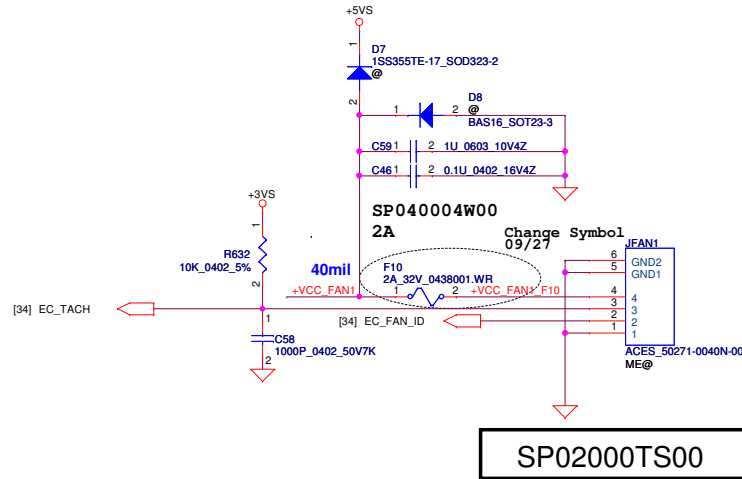
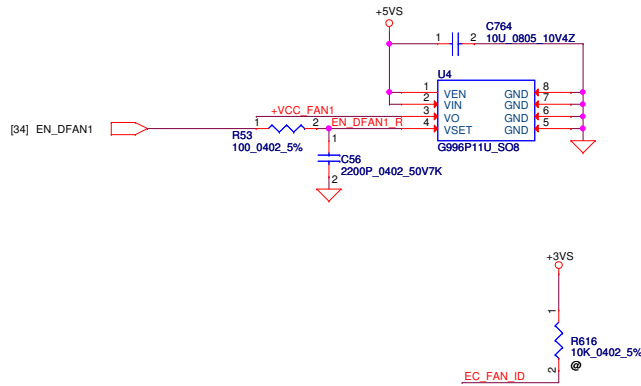


Fintek thermal sensor
placed near by BOT DRAM

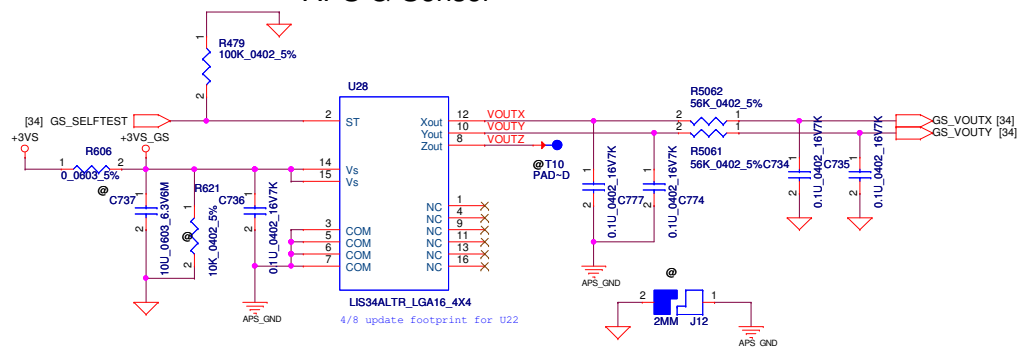
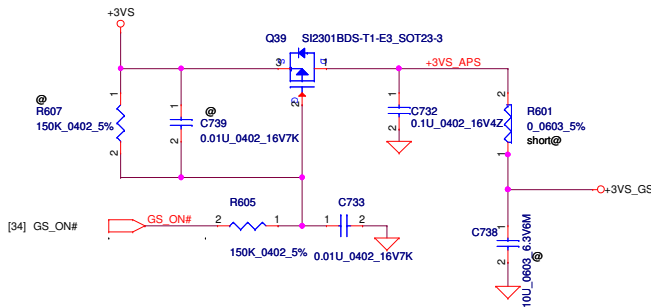


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN +5VS DROOP



APS G-Sensor



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KSO	C778	C780	C782	C784	C786	C788	C790	C792	C794	C796	C798	C800
KSO2	1	2	@100P_0402_50V8J									
KSO15	1	2	@100P_0402_50V8J									
KSO6	1	2	@100P_0402_50V8J									
KSO8	1	2	@100P_0402_50V8J									
KSO13	1	2	@100P_0402_50V8J									
KSO12	1	2	@100P_0402_50V8J									
KSO11	1	2	@100P_0402_50V8J									
KSO10	1	2	@100P_0402_50V8J									
KSO3	1	2	@100P_0402_50V8J									
KSO4	1	2	@100P_0402_50V8J									
KSO10	1	2	@100P_0402_50V8J									
KSO0	1	2	@100P_0402_50V8J									

CONN PIN define need double check

IPD_LEFT	C814	1	2	@ 100P_0402_50V8J
IPD_MIDDLE	C819	1	2	@ 100P_0402_50V8J
IPD_RIGHT	C805	1	2	@ 100P_0402_50V8J
KSO1	C779	1	2	@ 100P_0402_50V8J
KSO7	C781	1	2	@ 100P_0402_50V8J
KSI2	C783	1	2	@ 100P_0402_50V8J
KSO5	C785	1	2	@ 100P_0402_50V8J
KSI3	C787	1	2	@ 100P_0402_50V8J
KSO14	C789	1	2	@ 100P_0402_50V8J
KSI7	C791	1	2	@ 100P_0402_50V8J
KSI6	C793	1	2	@ 100P_0402_50V8J
KSI5	C795	1	2	@ 100P_0402_50V8J
KSI4	C797	1	2	@ 100P_0402_50V8J
KSO9	C799	1	2	@ 100P_0402_50V8J
KSI1	C801	1	2	@ 100P_0402_50V8J

Reserve for ESD.

JAE FL45030HA3R3000A-DT

ME@

JKB1

Pin	Function
1	KS11
2	KS17
3	KS16
4	KSO9
5	KS14
6	KS15
7	KSO0
8	KS12
9	KS13
10	KSO5
11	KSO1
12	KS10
13	KSO2
14	KSO4
15	KSO7
16	KSO8
17	KSO6
18	KSO3
19	KSO12
20	KSO13
21	KSO14
22	KSO11
23	KSO10
24	KSO15
25	
26	IPD LEFT
27	IPD MIDDLE
28	IPD RIGHT
29	
30	
31	GND1
32	GND2

Track point

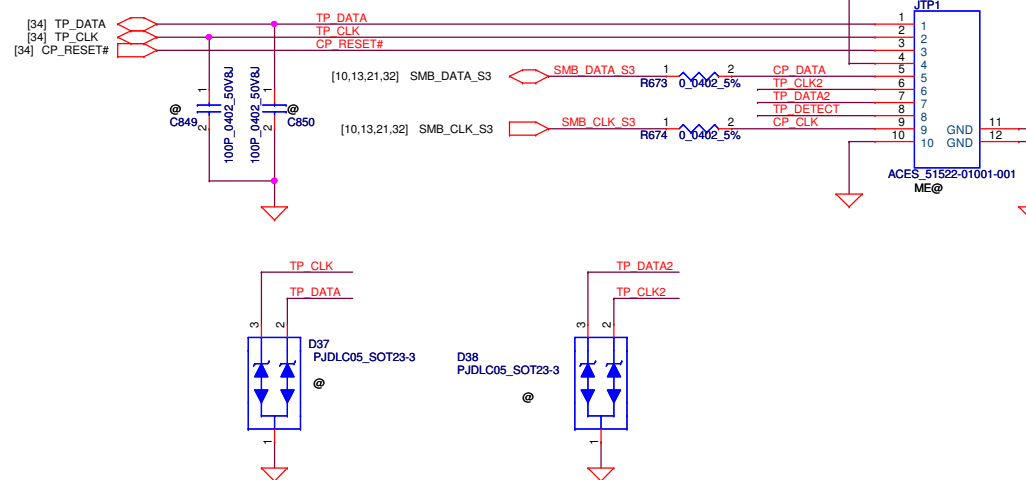
PN:SP01001CH00

Diagram illustrating the pin connections for the ACES 50524-0100N-001 MEQ. The diagram shows a 12-pin connector with pins 1 through 12. Pin 1 is labeled F9 1A_32V_0438001.WR and is connected to +5VSO. Pin 2 is labeled +5VS F9. Pin 3 is labeled JTP2. Pin 4 is labeled TP_CLK2. Pin 5 is labeled IPD LEFT. Pin 6 is labeled IPD RIGHT. Pin 7 is labeled IPD MIDDLE. Pin 8 is labeled TP_RESET. Pin 9 is labeled TP_DATA2. Pin 10 is labeled GND. Pin 11 is labeled GND. Pin 12 is labeled GND. A note indicates that pins 1, 2, and 3 are not to be connected to the device.

Click pad 10PIN

SP01001AL00

09/27

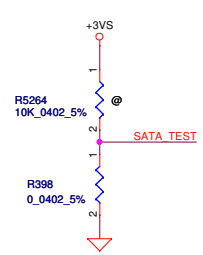
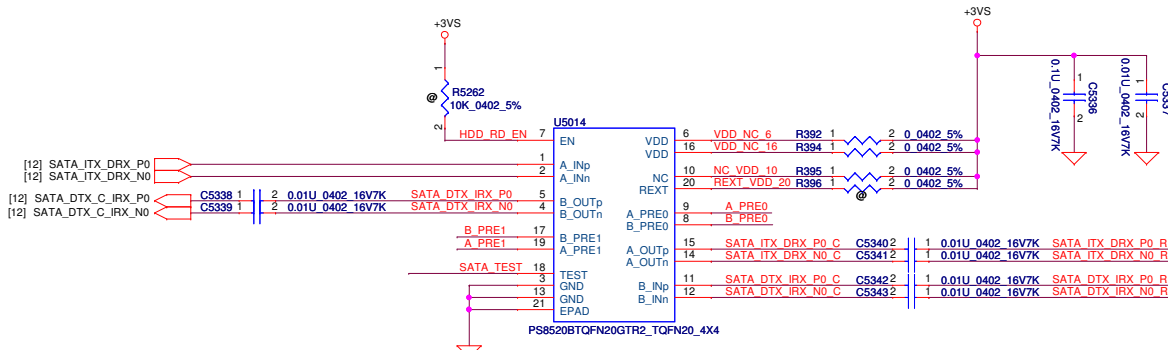


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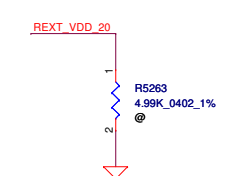
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				Date Thursday, October 04, 2012	Isheet 35 of 50

Compal Electronics, Inc.
KB /SW .

Size Custom	Document Number	Rev
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Date:	Thursday, October 04, 2012	Sheet 35 of 50

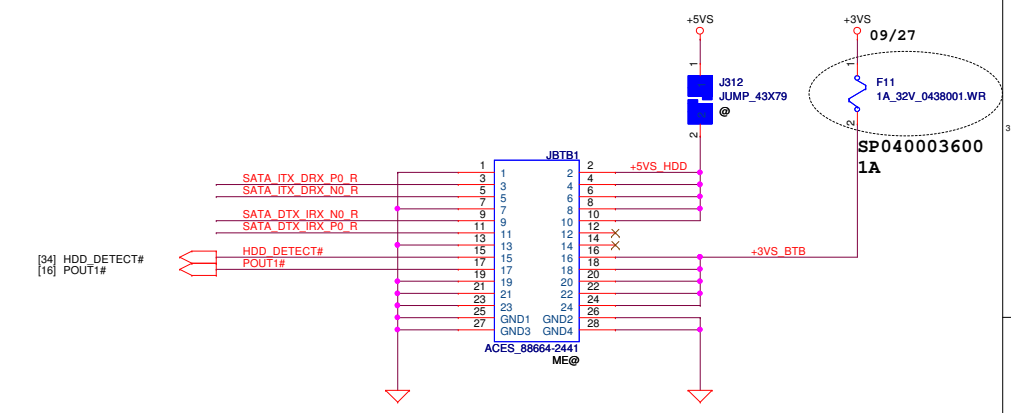
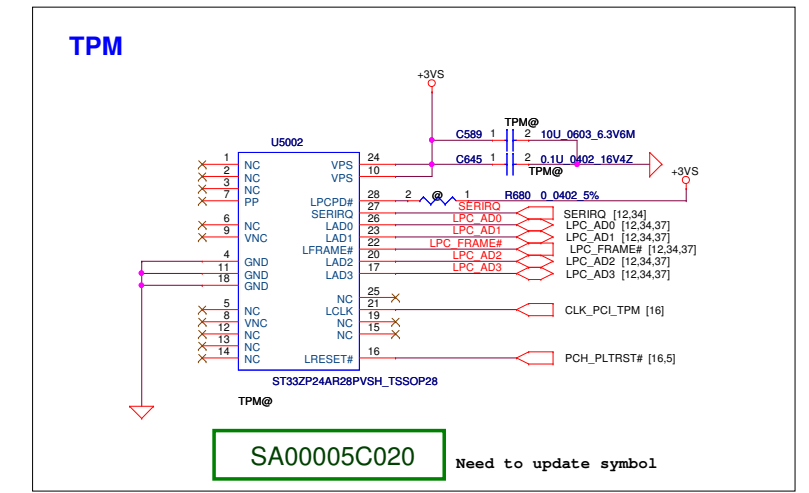


	TEST (Internal Low)
Normal Mode (Default)	LOW
Test Mode	HIGH



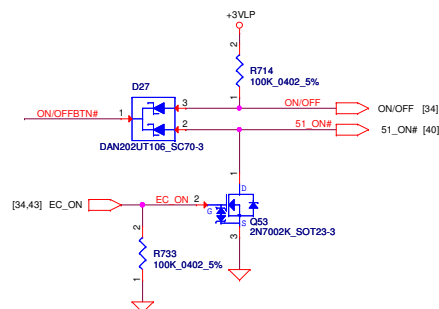
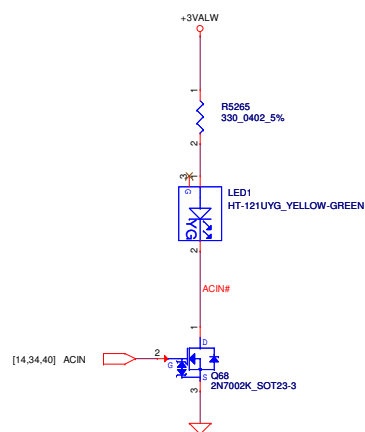
Remove pull-low

	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High

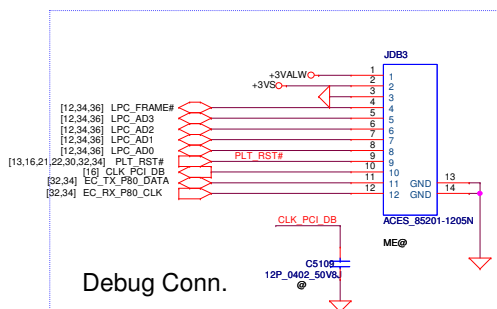
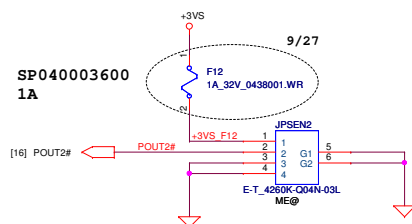


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AC-IN LED (Color : Green)

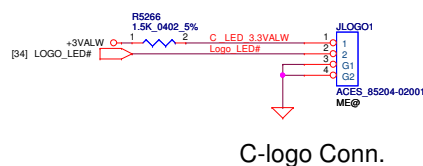


SP040003600
1A

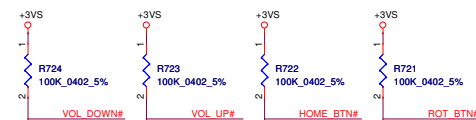


Debug Conn.

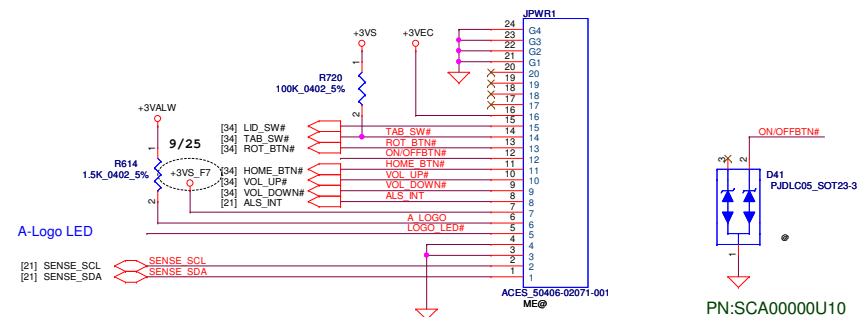
AMY WEN



C-logo Conn.

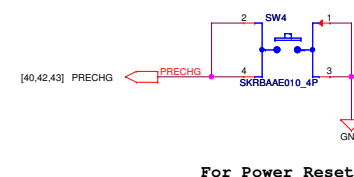


SP010016L00



Power Board connector

BOTTOM SIDE
SN111005800 by ME drawing

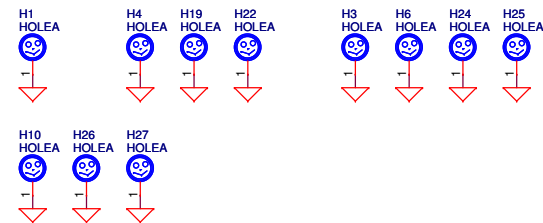


For Power Reset

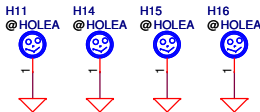
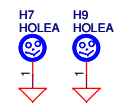
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Size	Document Number	LA-8671P_SDV		Rev 1A	
Date:	Thursday, October 04, 2012	Sheet	37	of 50	

PT-H 20 SCREW HOLE

H_2P3



H_3P3



H_6P0



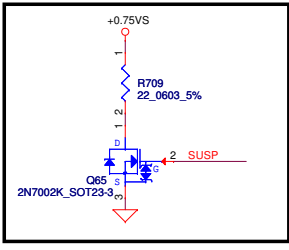
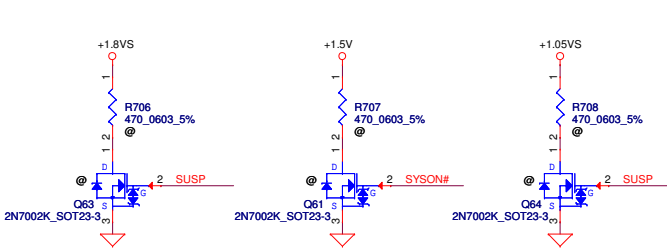
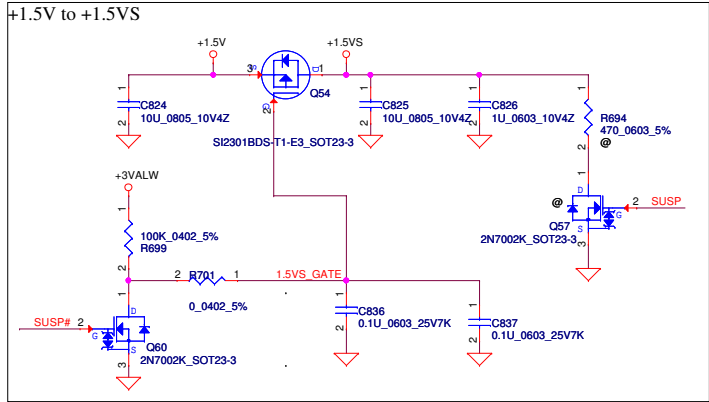
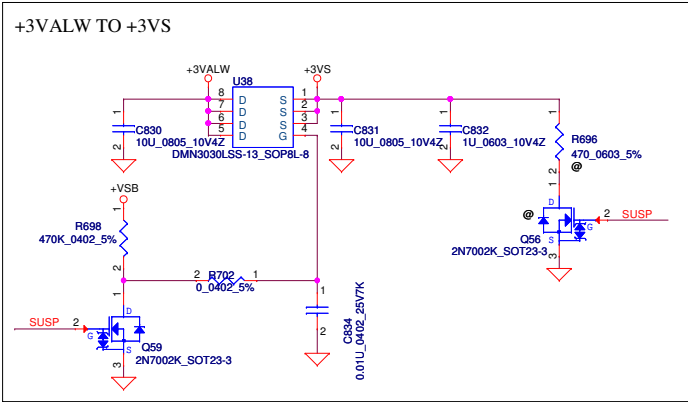
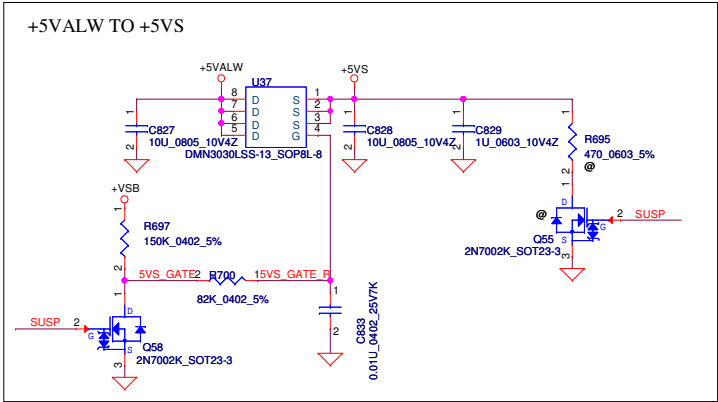
NON-PT-H 1 SCREW HOLE

H_2P4N

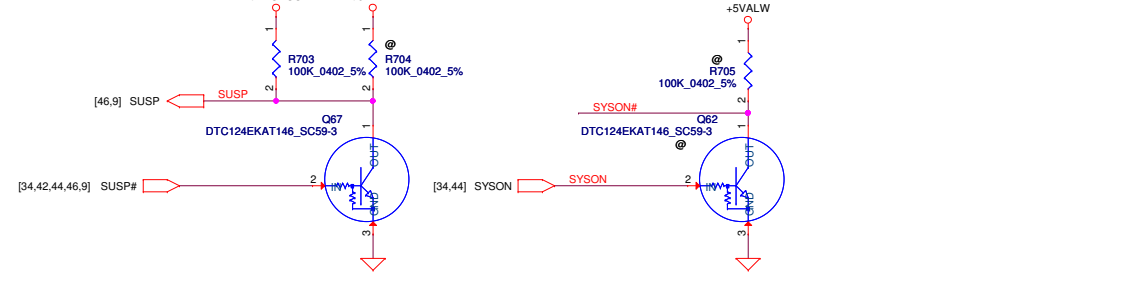


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				Custom	LA-8671P_SDV	1.0
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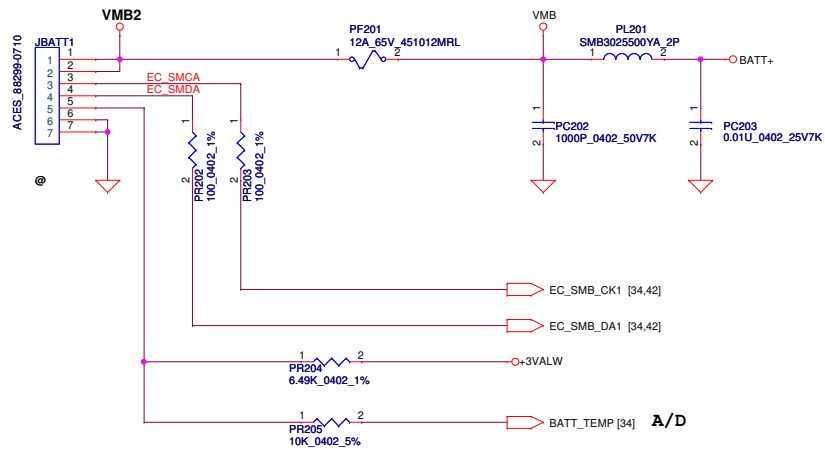


For Intel S3 Power Reduction.



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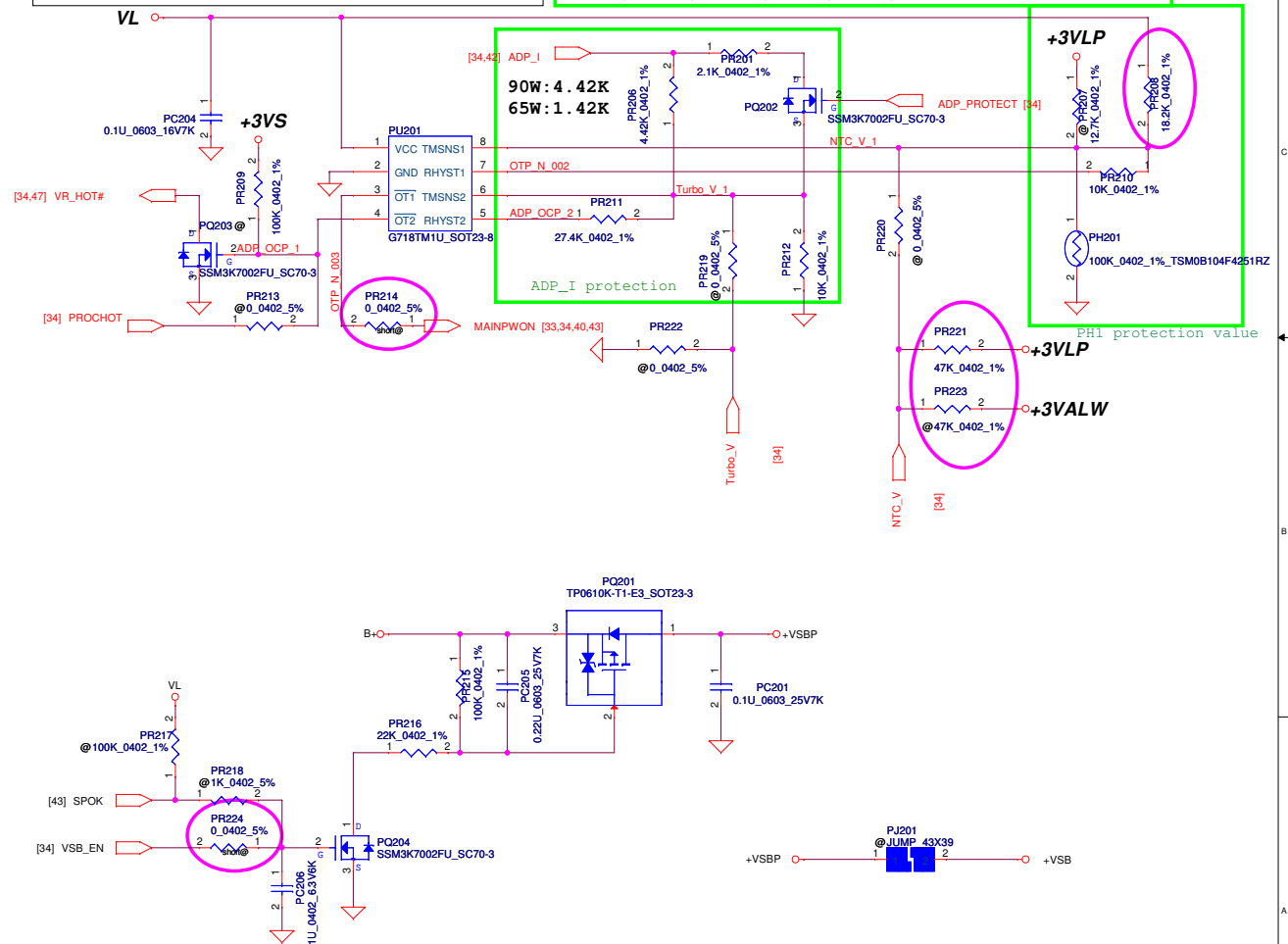
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/25	Deciphered Date	2012/08/25	Title	
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PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)

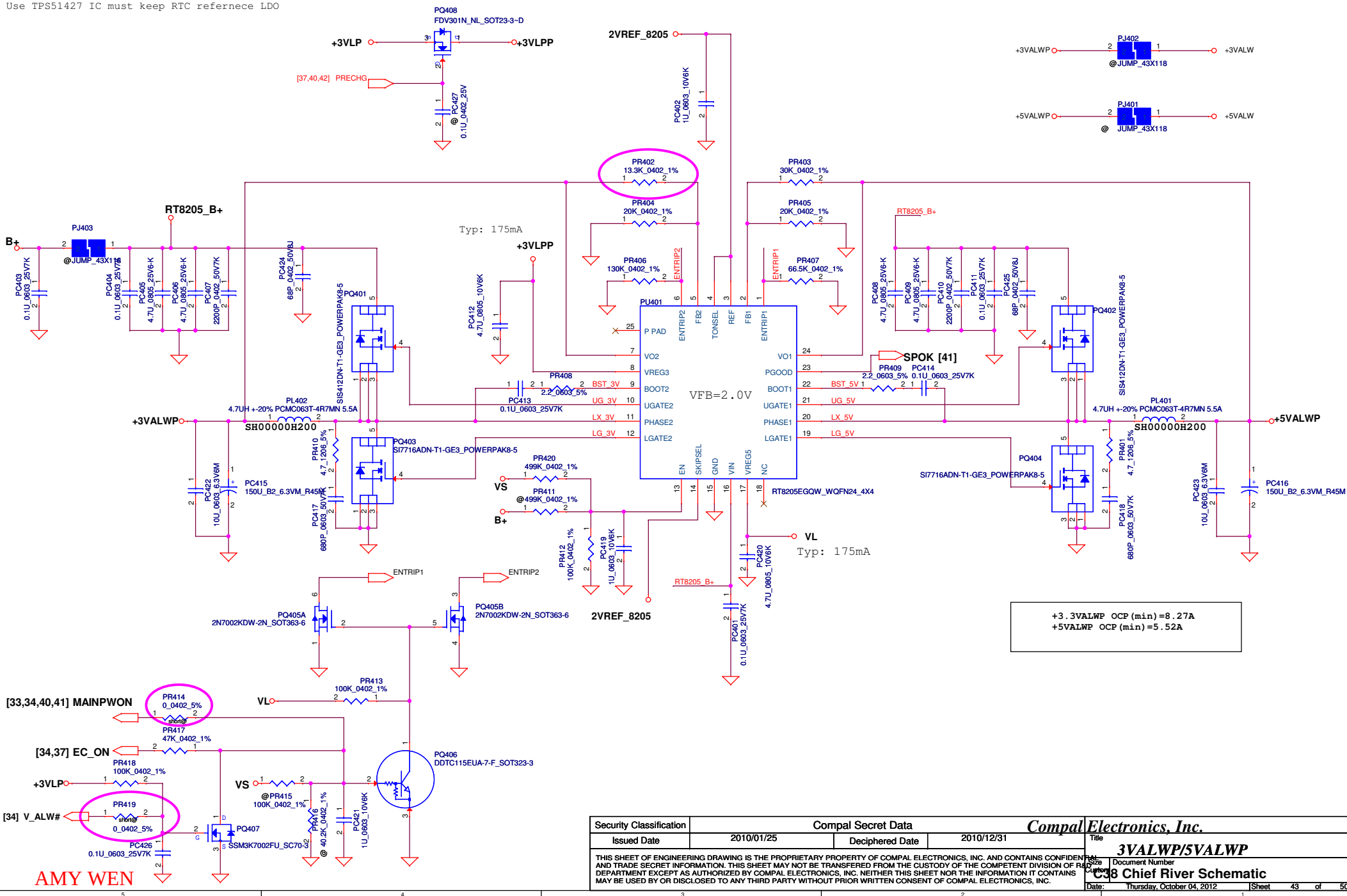
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



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				Date	Thursday, October 04, 2012
				Sheet	41 of 50

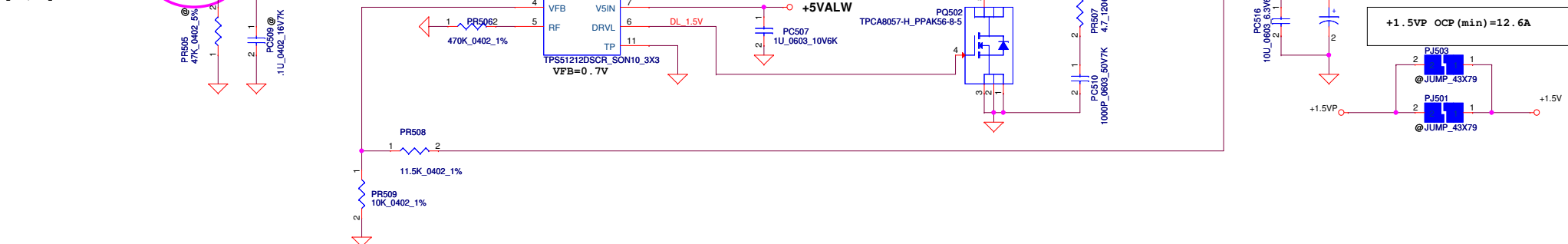
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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				Issue	038 Chief River Schematic	1.0
				Date:	Thursday, October 04, 2012	Sheet 43 of 50

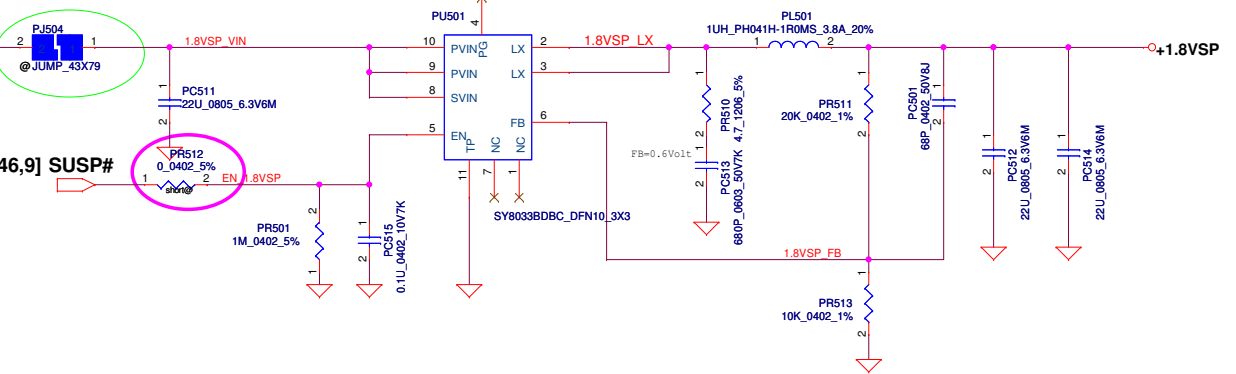
[34,39] SYSON



2011_0801 JP504 form
43x118 change to 43x79

+5VALW

[34,39,42,46,9] SUSP#



2011_0801 JP505 form
43x118 change to 43x79

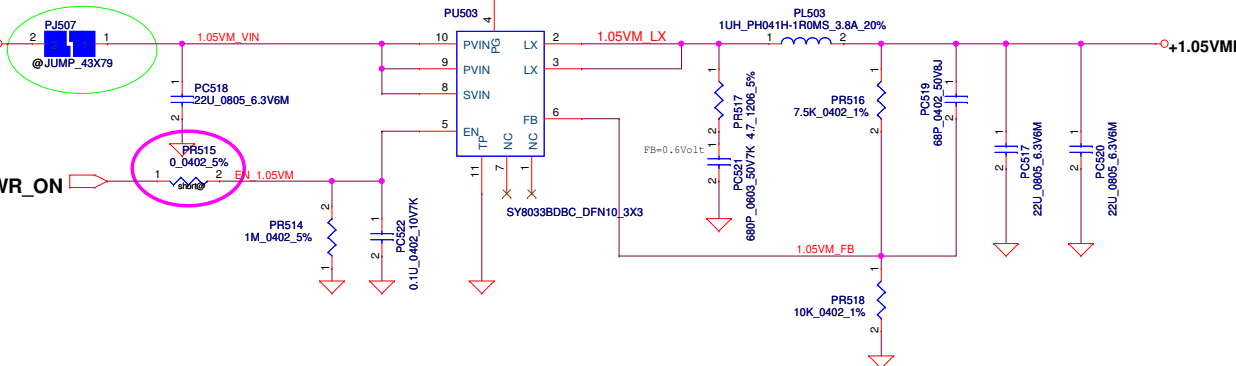
+1.8VSP

1.8VSP max current=4A

2011_0801 JP504 form
43x118 change to 43x79

+5VALW

[19,34] M_PWR_ON



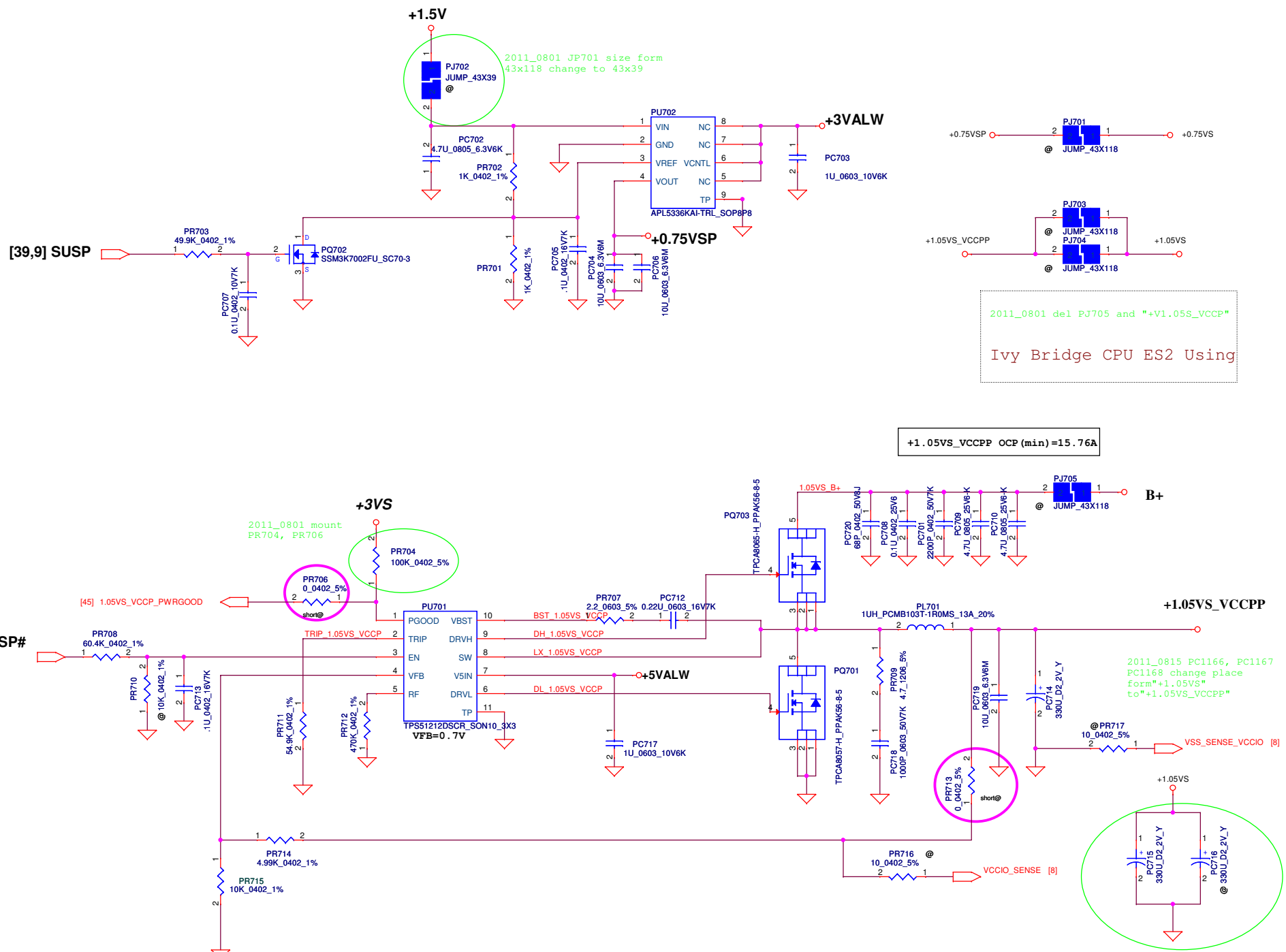
2011_0801 JP505 form
43x118 change to 43x79

+1.05VMP

1.05VMP max current=4A

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Date:	Thursday, October 04, 2012	Sheet	44	of	50

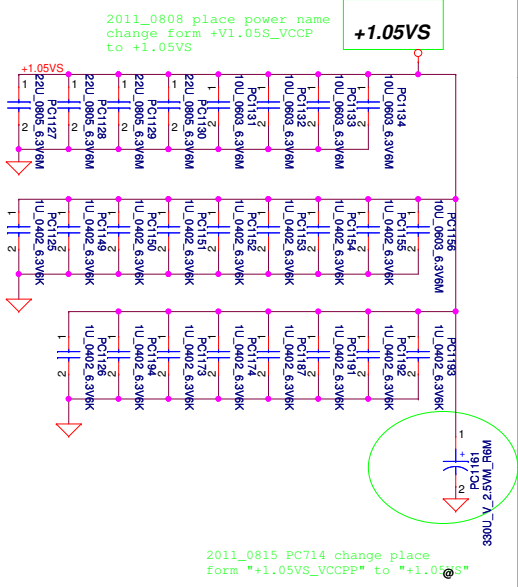
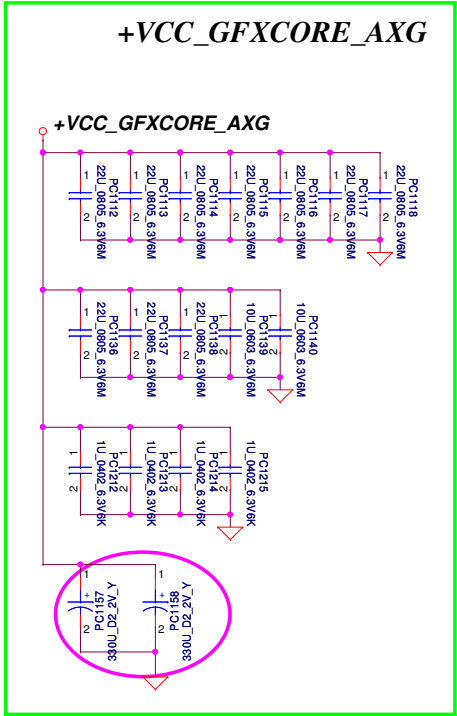
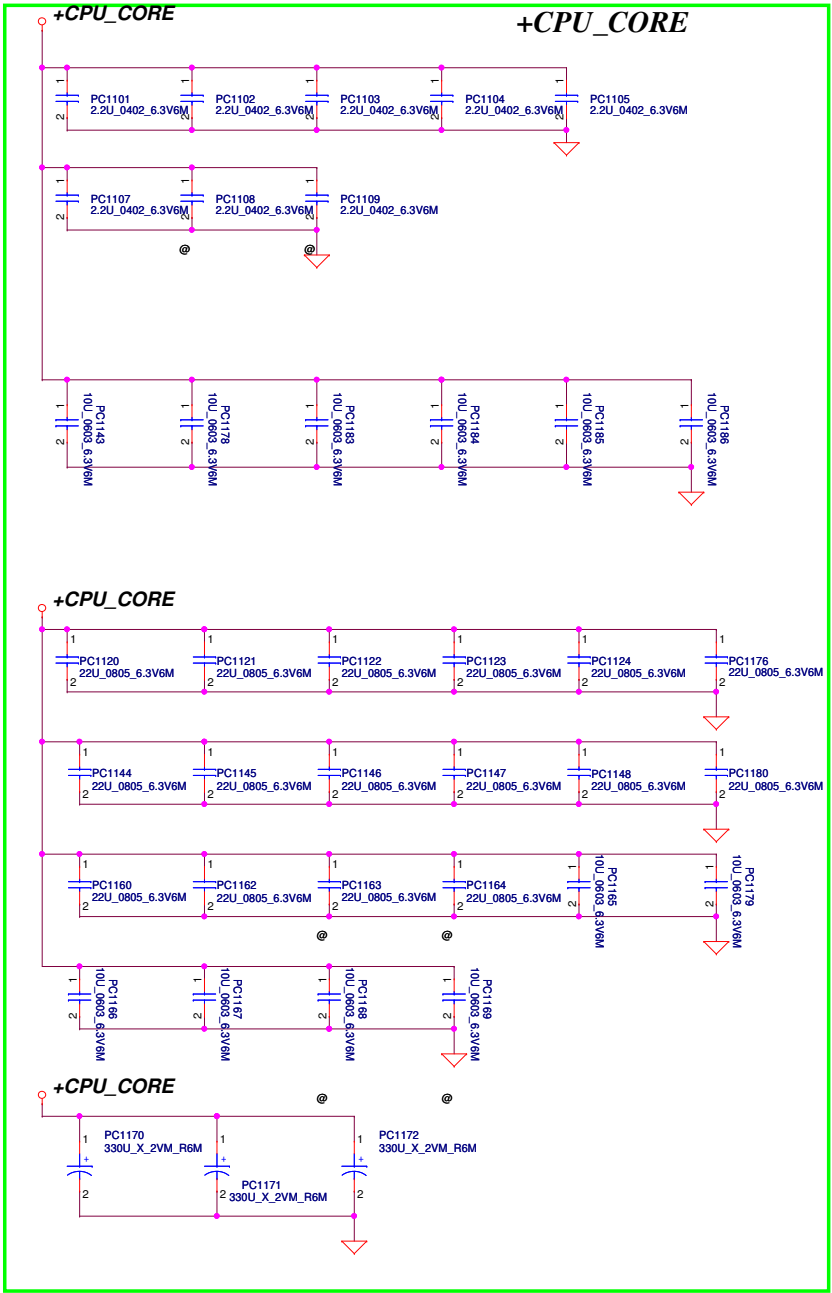


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				Document Number	Rev 1.0
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								Document Number		Rev	
								C38 Chief River Schematic		1.0	
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				LA-826IP_SDV	
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				Rev	1.0

Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	NCP6132A update SPEC	P47	Remove PR916, PR945	2012/06/05	
2	Thermal verify PH1 setting point	P41	Change PR208 value to 18.2K	2012/06/08	
3	ME demand : Keyboard assembly issue	P44	Change PL401, PL402 to High=2.4mm (SH000000H200)	2012/06/08	
4	Noise is PASS, Don't need 33u CAP	P48	Remove PC1023, PC1024	2012/06/08	
5					
6					
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				C38 Chief River Schematic	
Date: Thursday, October 04, 2012				Sheet	50 of 50
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