

MOLOKAI Block Diagram

SPR.01.2004

Project Code:91.43E01.001

03249-SC

PCB LAYER

- L1: COMPONENT
- L2: GND
- L3: SIGNAL1
- L4: SIGNAL2
- L5: VCC
- L6: GND
- L7: SIGNAL3
- L8: COMPONENT

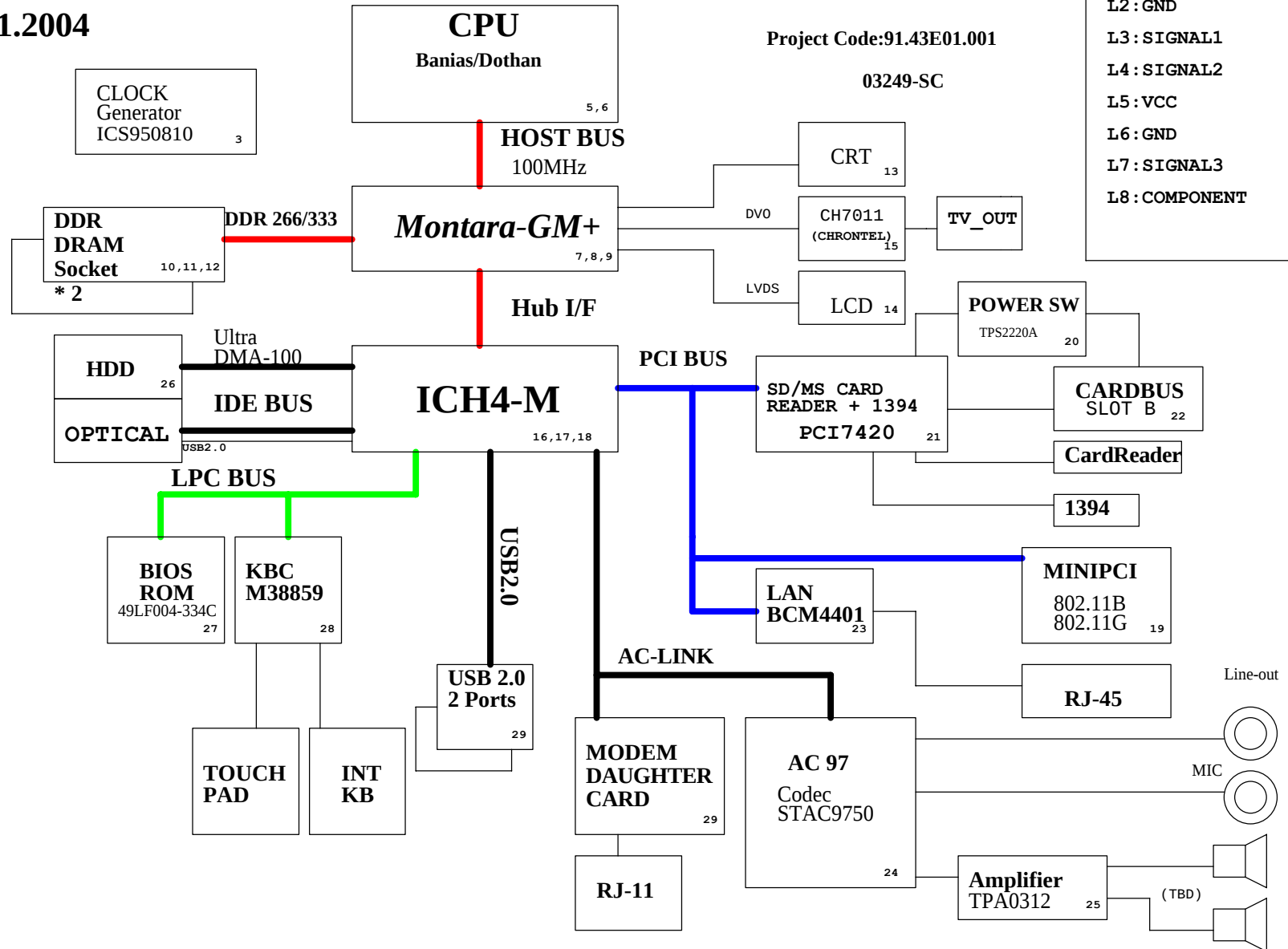
DC/DC IMVP4 Switching Power ISL6218 32	
INPUTS	OUTPUT
DCBATOUT	VCC_CORE

SYSTEM DC/DC MAX1715 34	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S0 2D5V_S3

DC/DC&CHARGER MAX1645 35	
INPUTS	OUTPUTS
AD+	BT+

DC/DC MAX1999 33	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

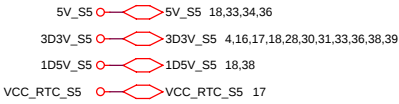
G913C/APL1085 APL5331kAC/G1211X 38	
INPUTS	OUTPUTS
3D3V_S0	1D8V_VCCA_S0
3D3V_S5	1D5V_S5
3D3V_S0	1D5V_S0
2D5V_S3	1D25V_S0
1D35V_S0	VCC_IO_S0



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Title: BLOCK DIAGRAM			
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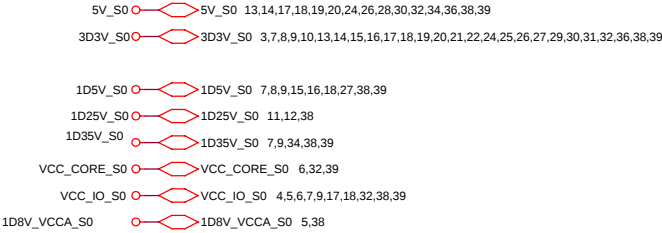
S5



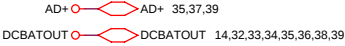
S3



S0



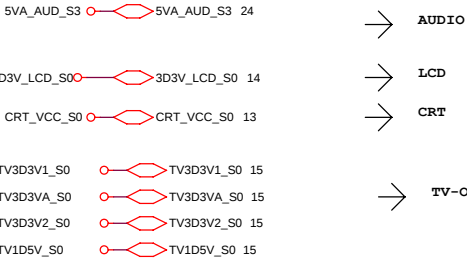
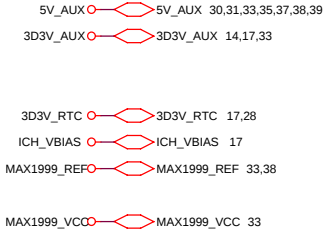
AC-IN / BAT-IN



LAN-AC



OTHERS



PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
SD/MS CARD READER+1394 PCI7420	AD20	PIRQB# PIROC# PIRQF#	REQ#1 / GNT#1
MINI PCI 802.11B/G	AD17	PIRQE# PIRQG#	REQ#0 / GNT#0
LAN BCM4401	AD21	PIRQD#	REQ#4 / GNT#4



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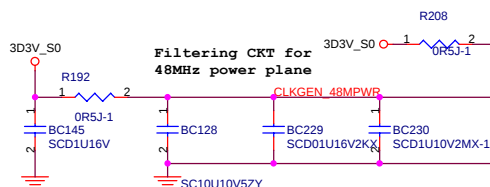
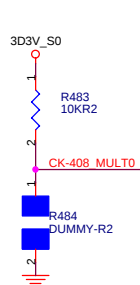
Host Freq. Setting

FS1/0 = 00 166MHz
 FS1/0 = 01 100MHz
 FS1/0 = 10 200MHz
 FS1/0 = 11 133MHz

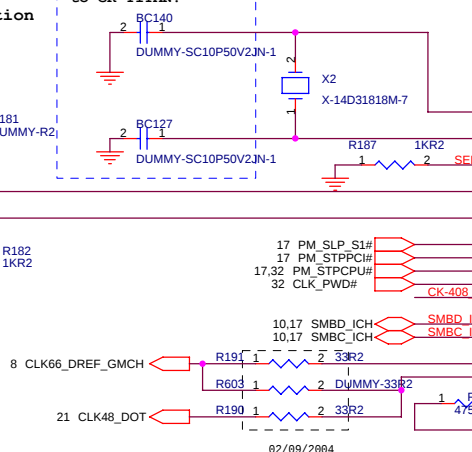
FS2 = 0 unbuffer mode (disable 66MHz-IN)
 FS2 = 1 buffer mode

Mult0 = 0 Rr=221,Iref=5mA =>Vswing=1.0V@50ohm
 Mult0 = 1 Rr=475,Iref=2.32mA =>Vswing=0.7V@50ohm

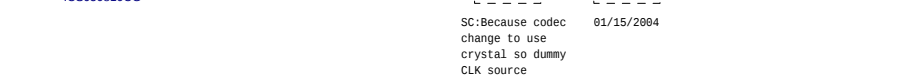
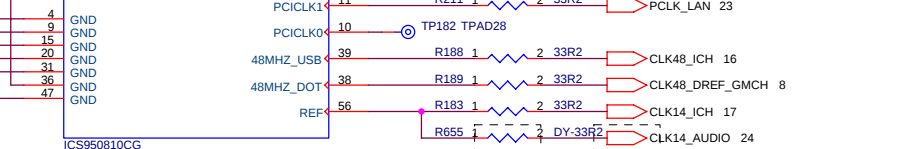
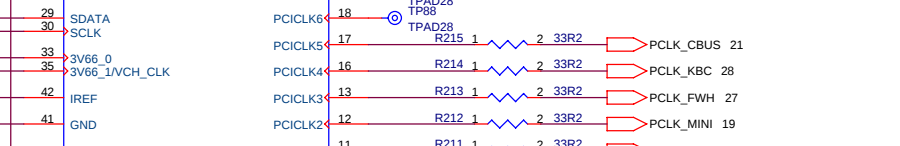
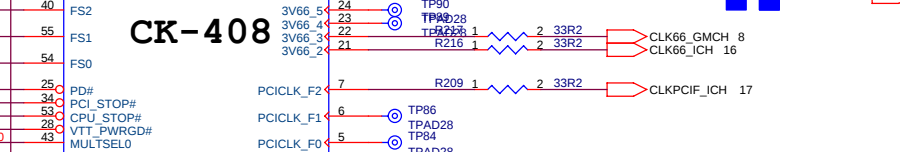
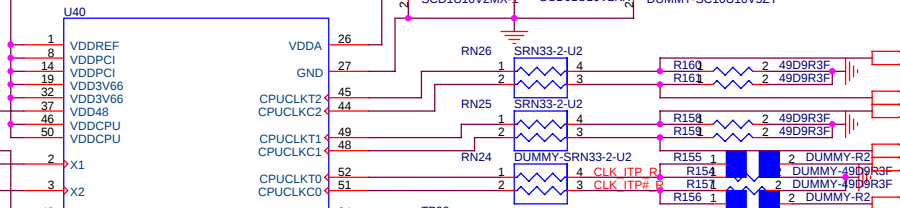
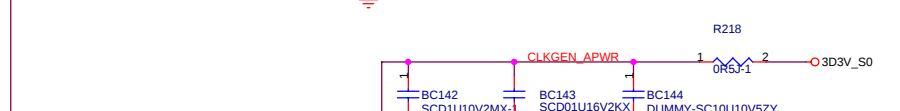
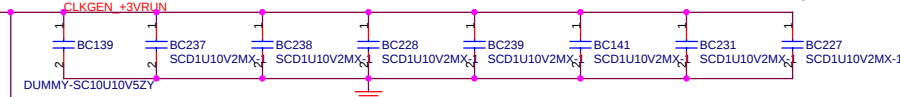
CPU & MEMORY Freq. Selection



No stuff:
 caps are internal
 to CK-TITAN.



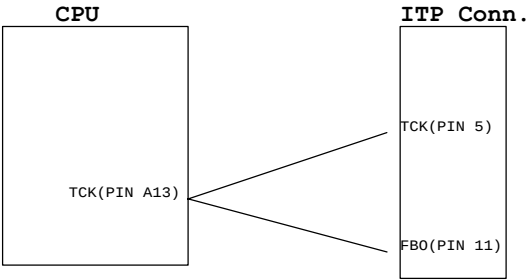
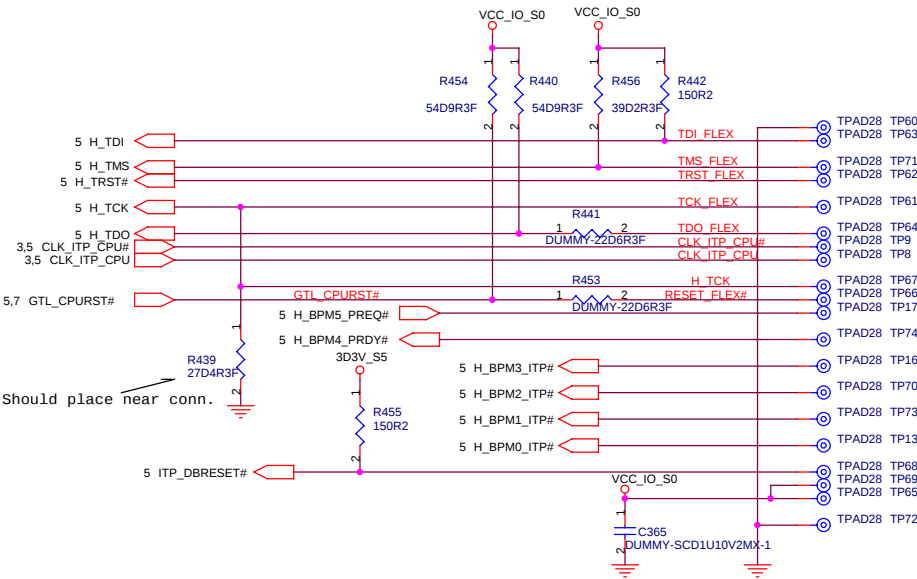
PLACE NEAR EACH PIN



CK-408

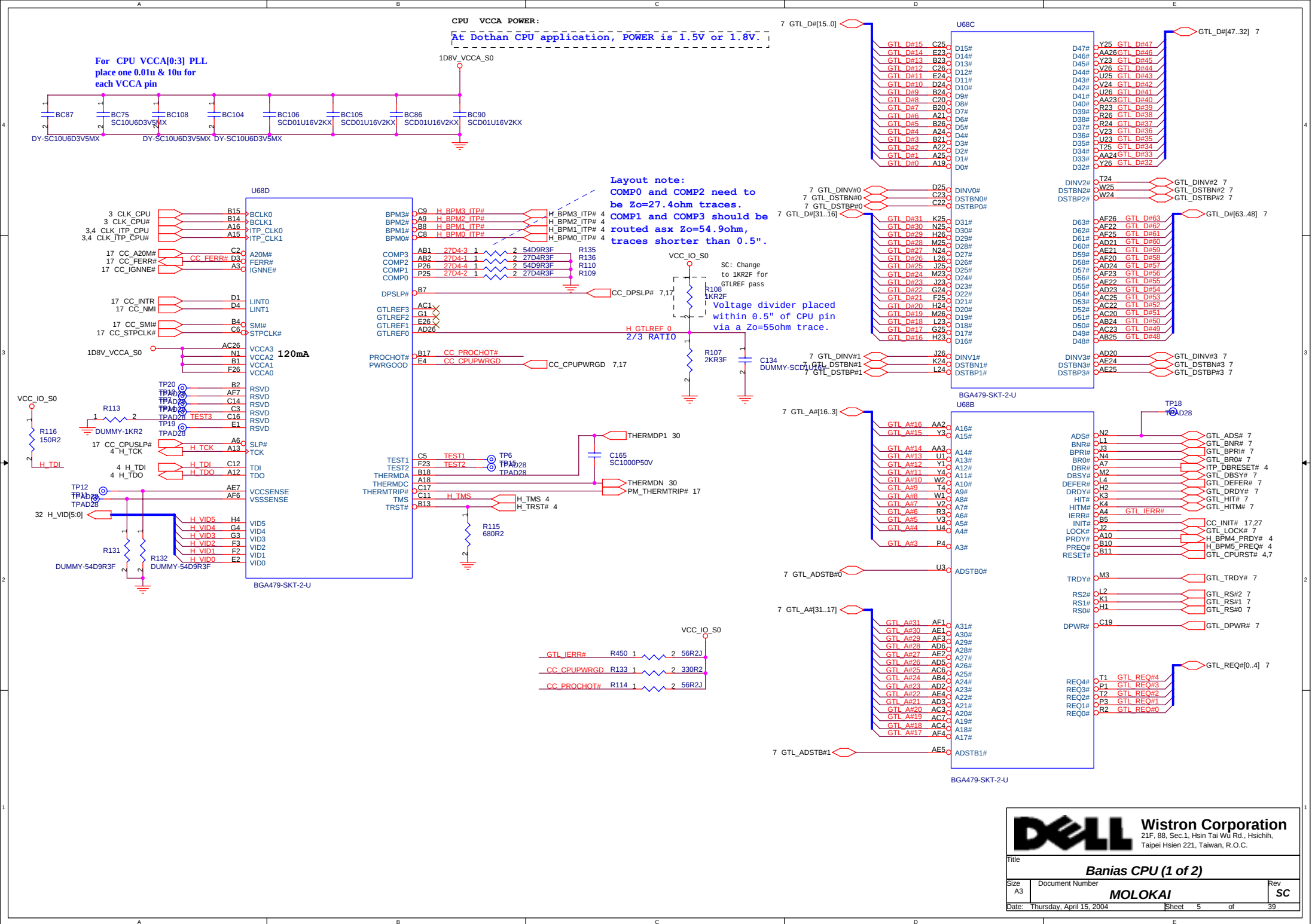
SC:Because codec
 change to use
 crystal so dummy
 CLK source

ITP Debug Pad

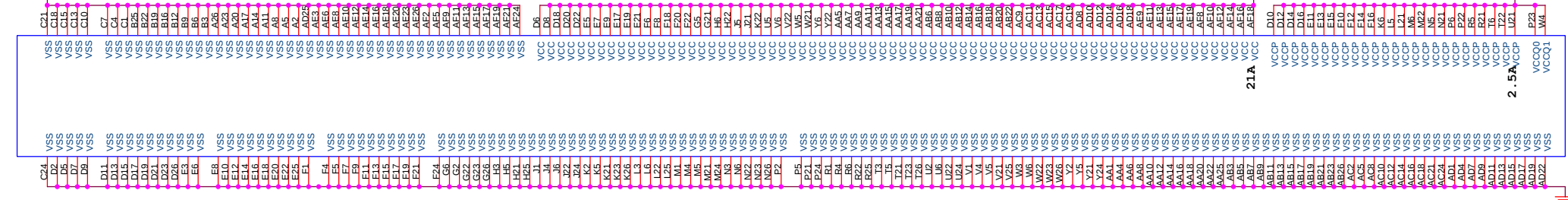


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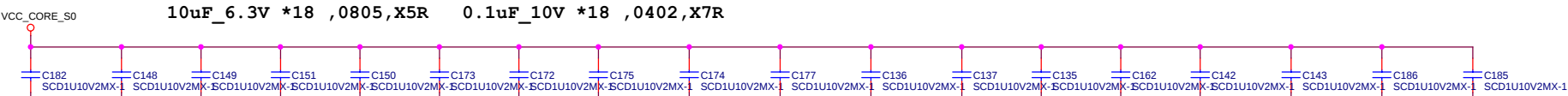
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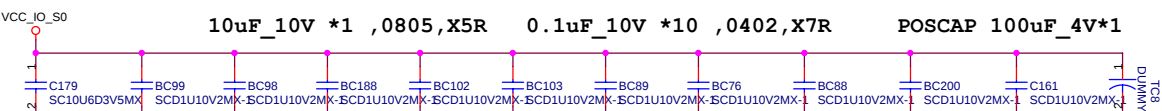
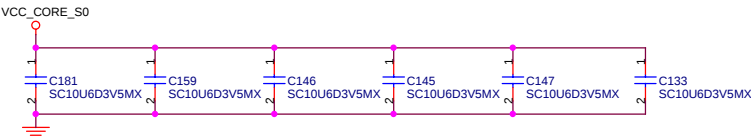
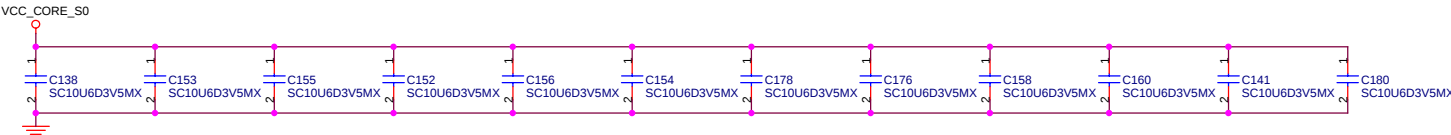
U68A



BGA479-SKT-2-U



Place near CPU



Place near CPU



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Document Number

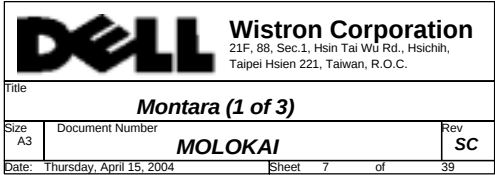
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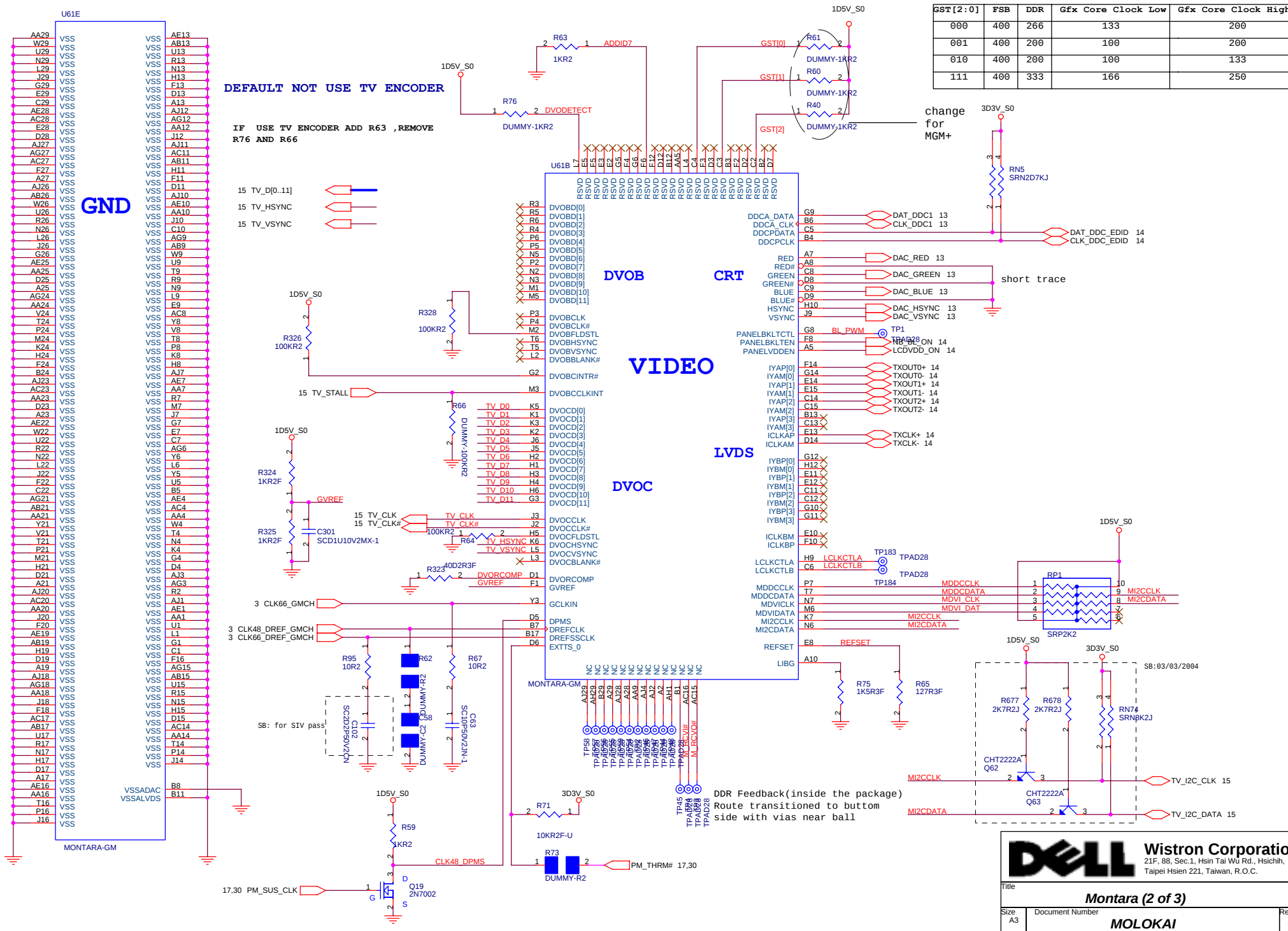
Rev

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FOR MGM+		internal pull down			
GST[2:0]	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High	
000	400	266	133	200	
001	400	200	100	200	
010	400	200	100	133	
111	400	333	166	250	



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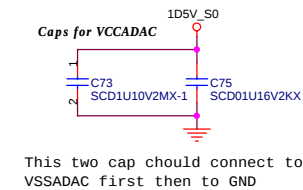
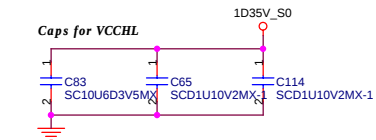
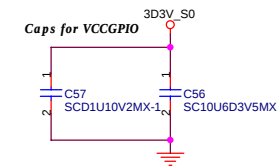
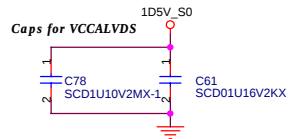
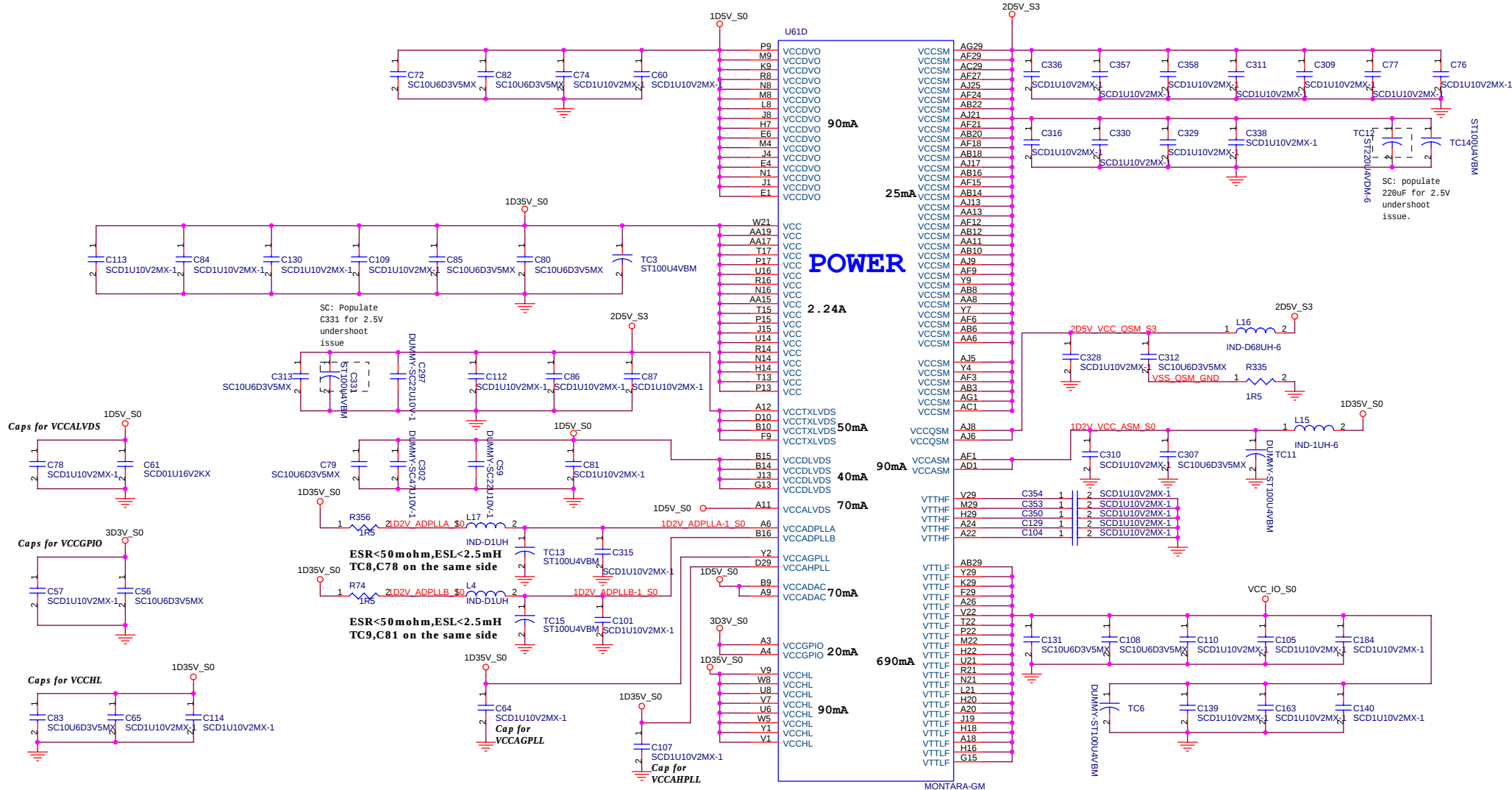
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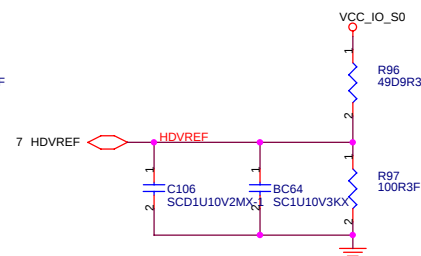
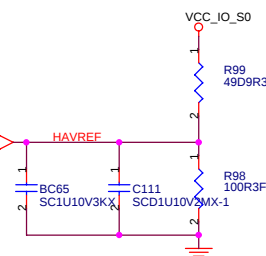
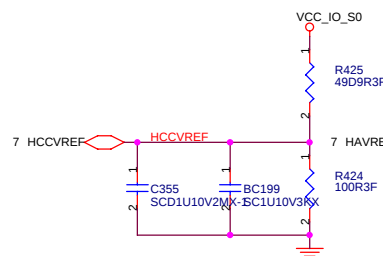
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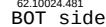
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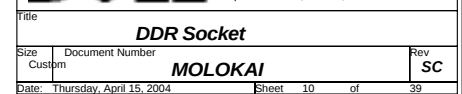


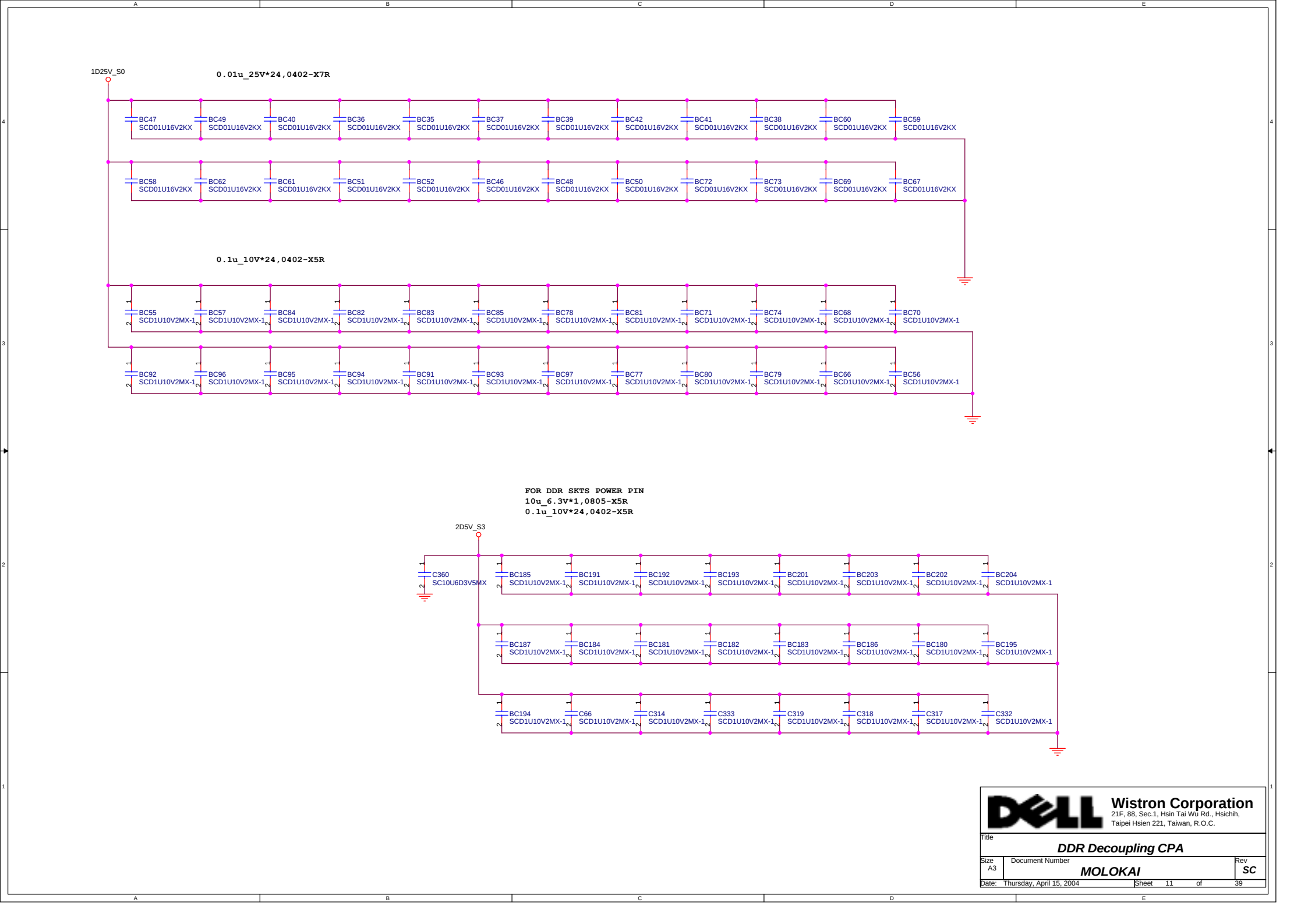
Reference Voltage: 2/3 Vcc_IO_S0



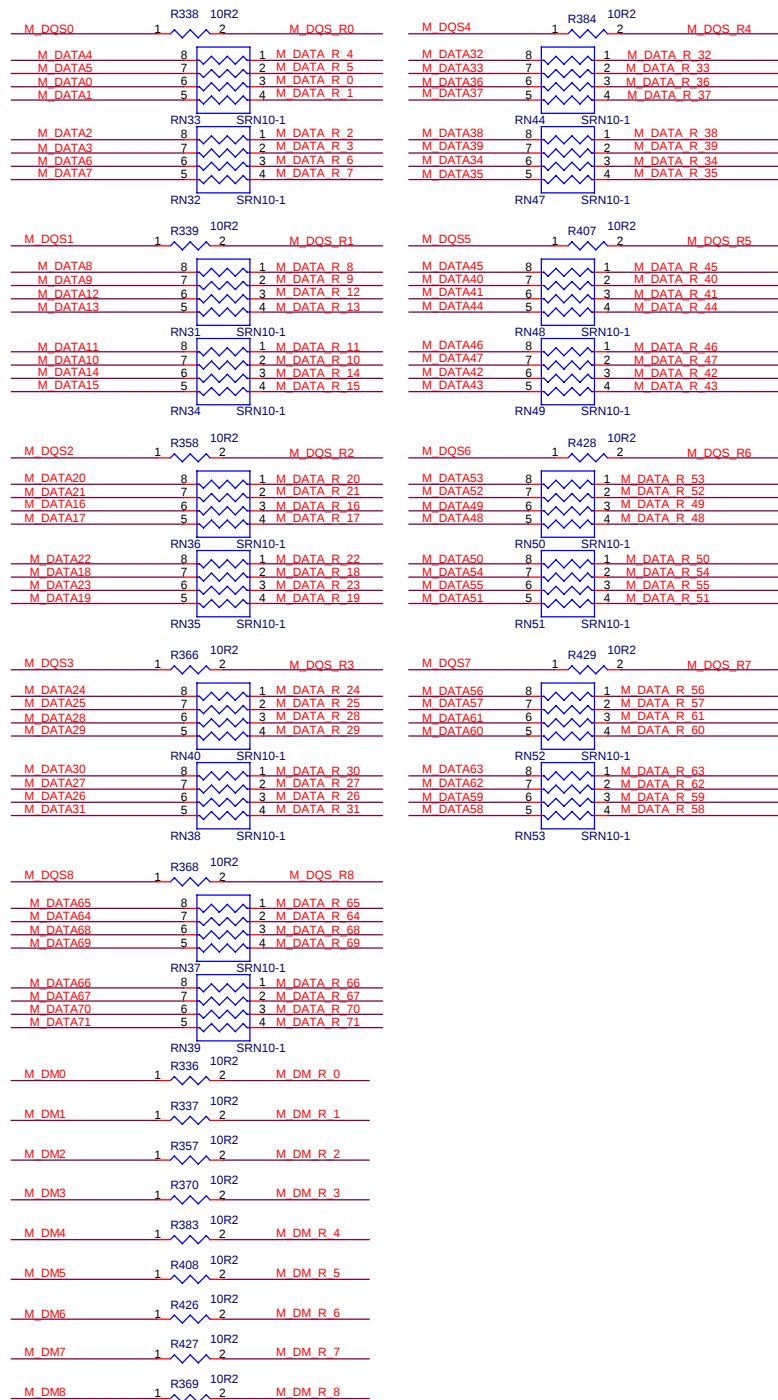


Montara-GM+
(BOT side)



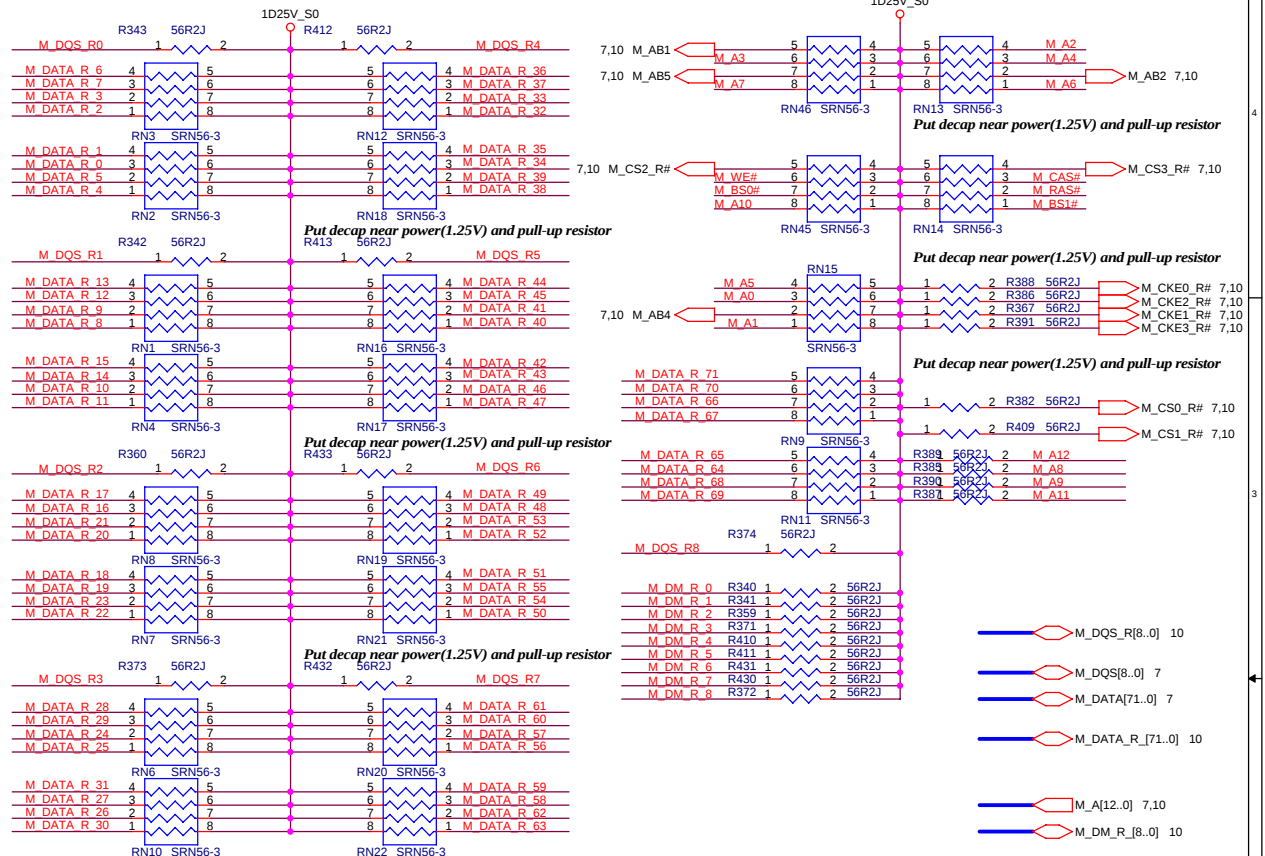


SERIES DAMPING

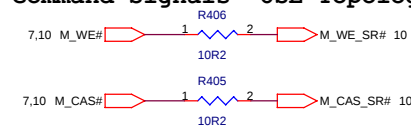


PARALLEL TERMINATION

Put decap near power(1.25V) and pull-up resistor

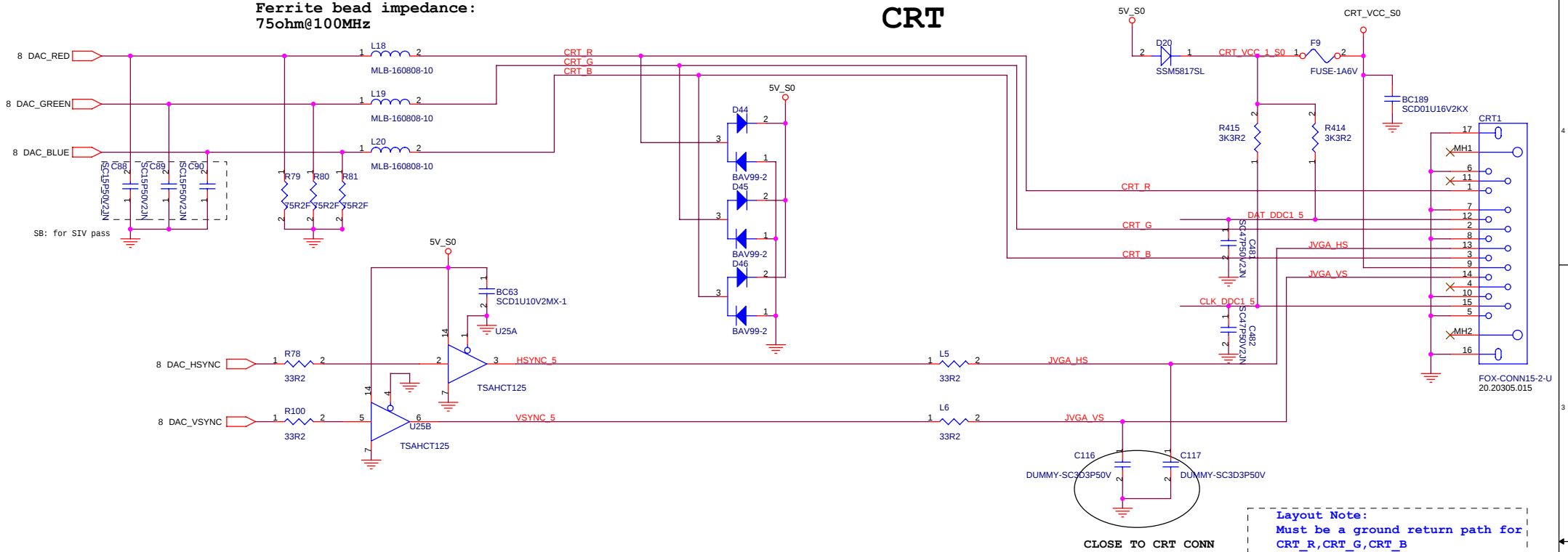


Command Signals USE Topology 2

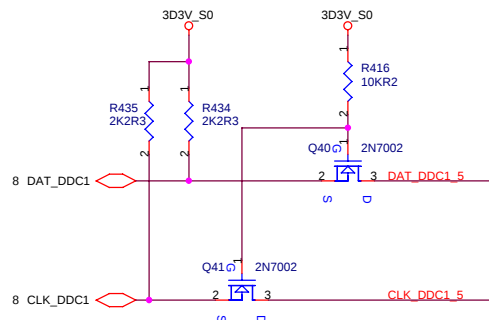


Ferrite bead impedance:
75ohm@100MHz

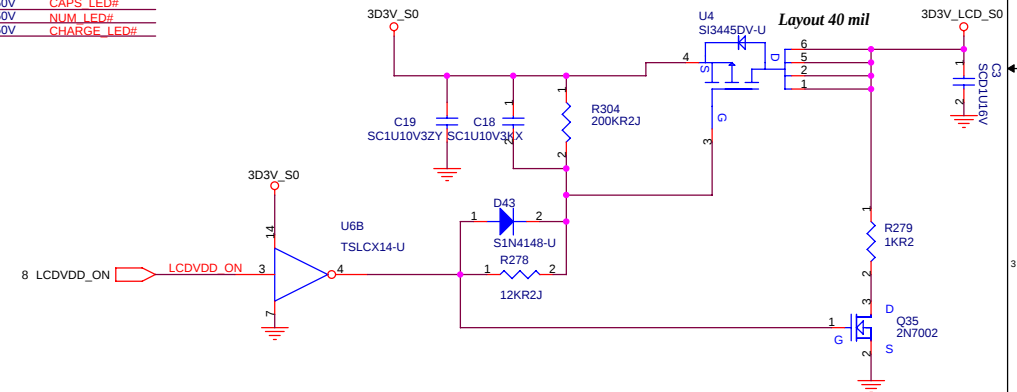
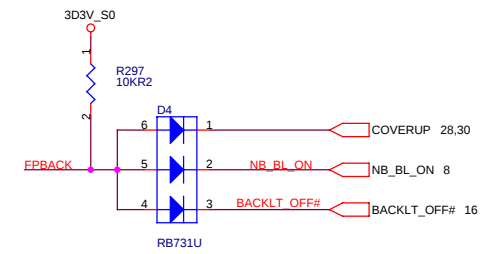
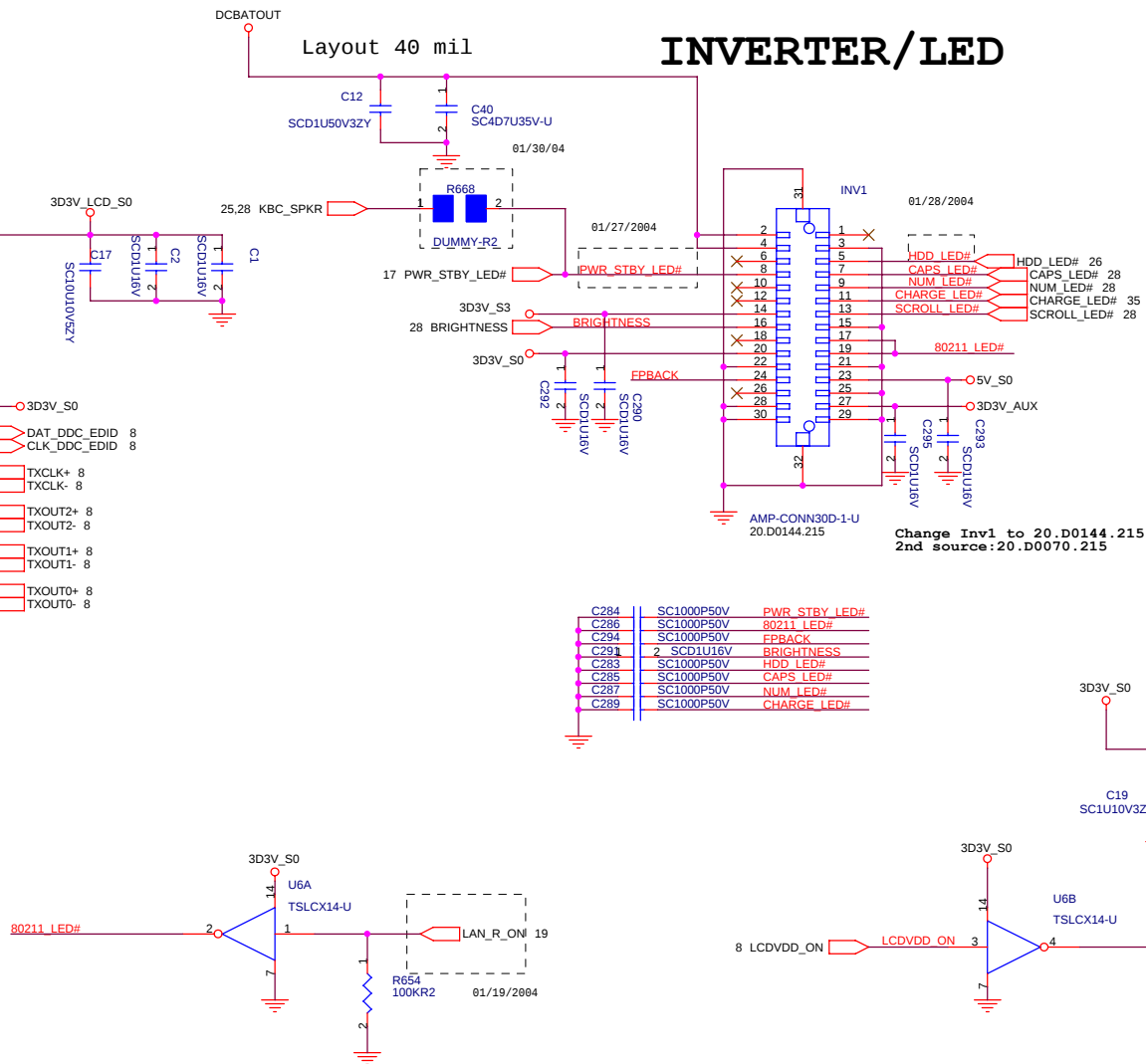
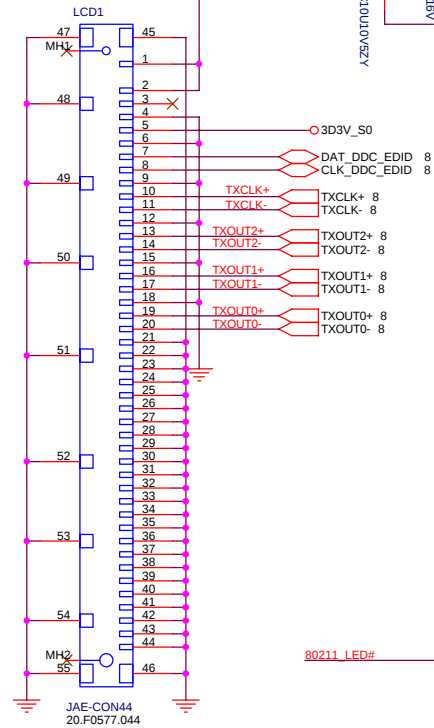
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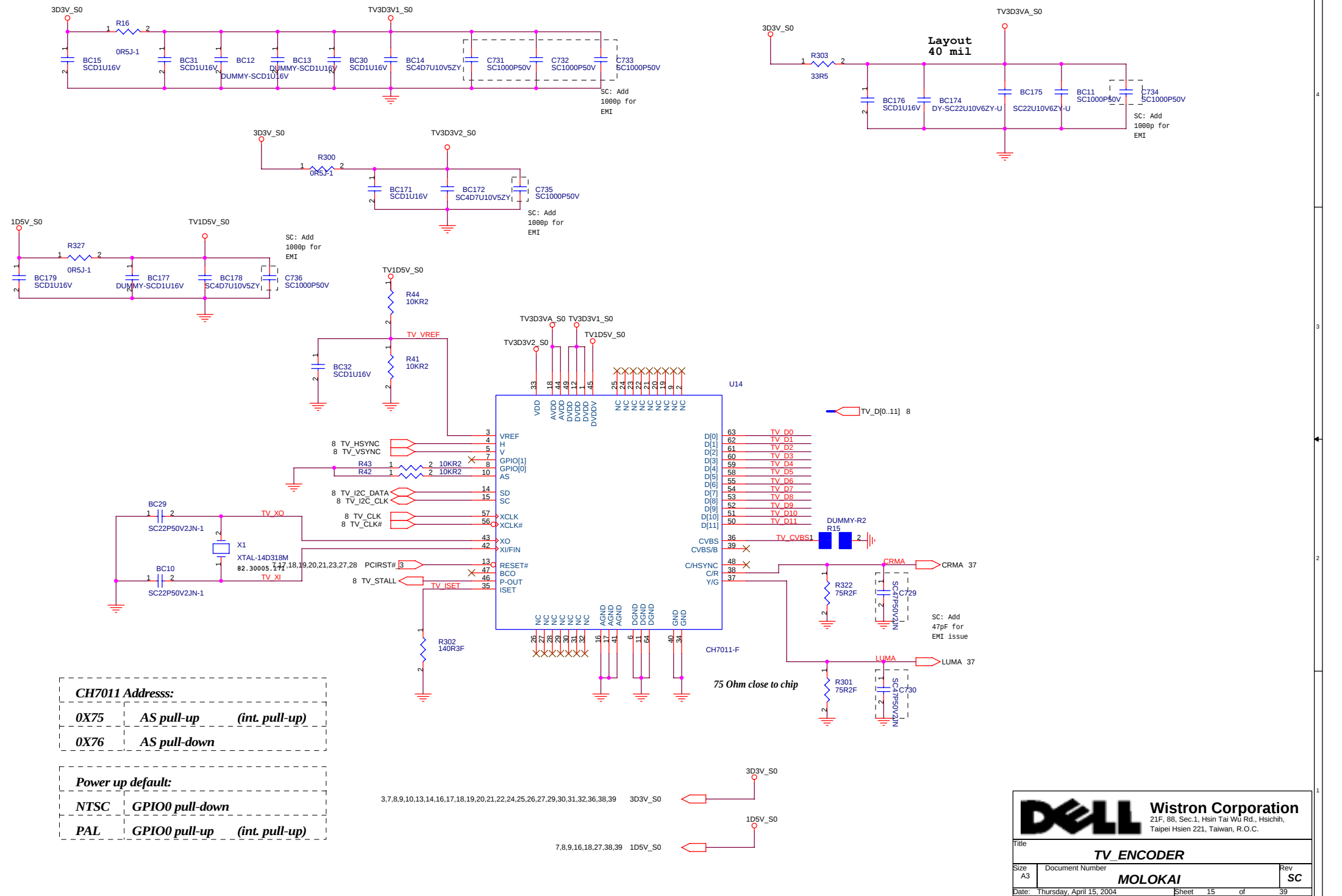
DDC_CLK & DATE LEVEL SHIFT



DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT CONN.			
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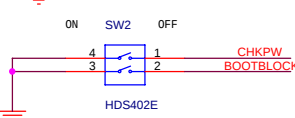
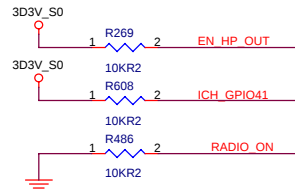
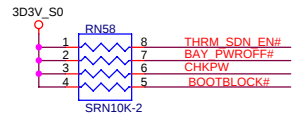
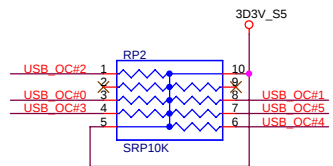


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Title			
LCD CONN & INVERTER			
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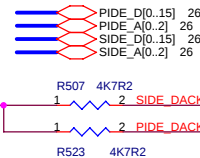
CH7011 Address:		
0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:		
NTSC	GPIO0 pull-down	
PAL	GPIO0 pull-up	(int. pull-up)



	SW1-4	SW2-3
CHKPW ENABLE	ON	X
BOOTBLOCK ENABLE	X	ON

Place R220 near S/B

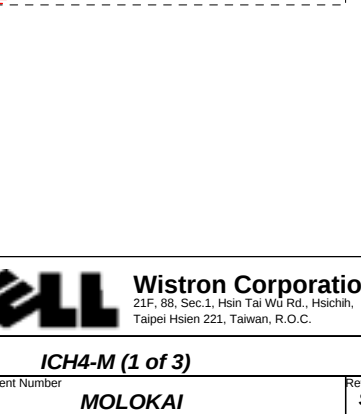
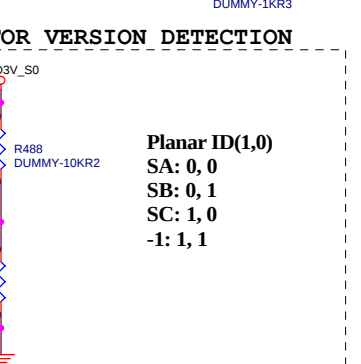
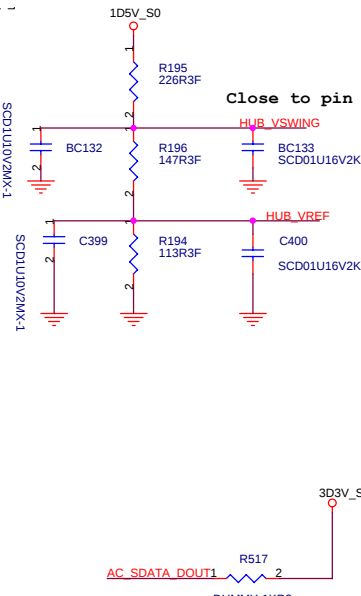
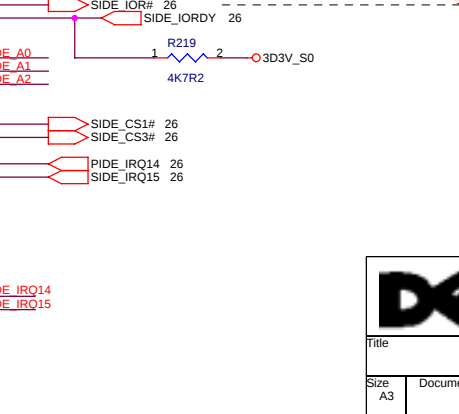
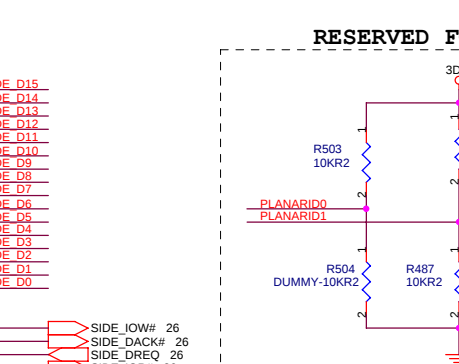
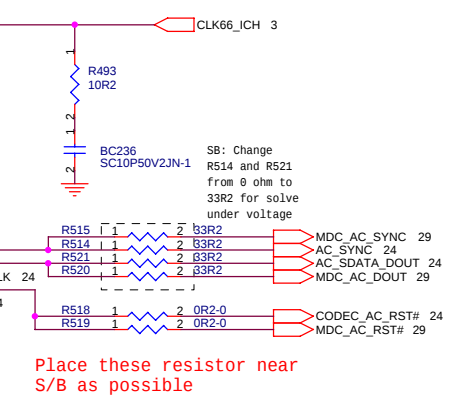
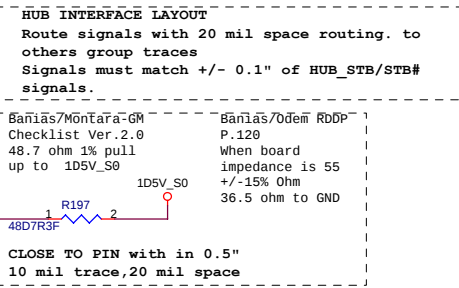
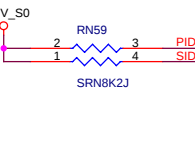
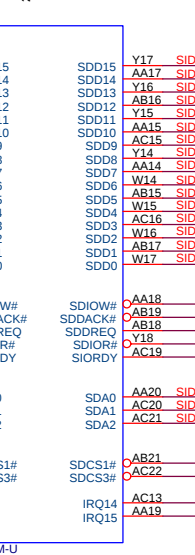
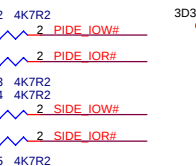
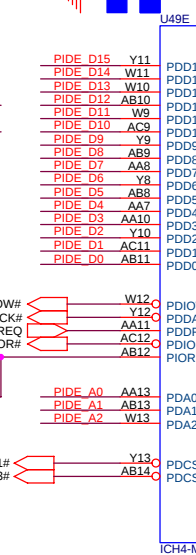
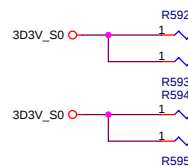
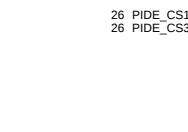
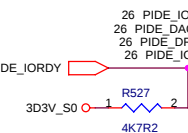


ICH4 Integrated Pull-up and Pull-down Resistors

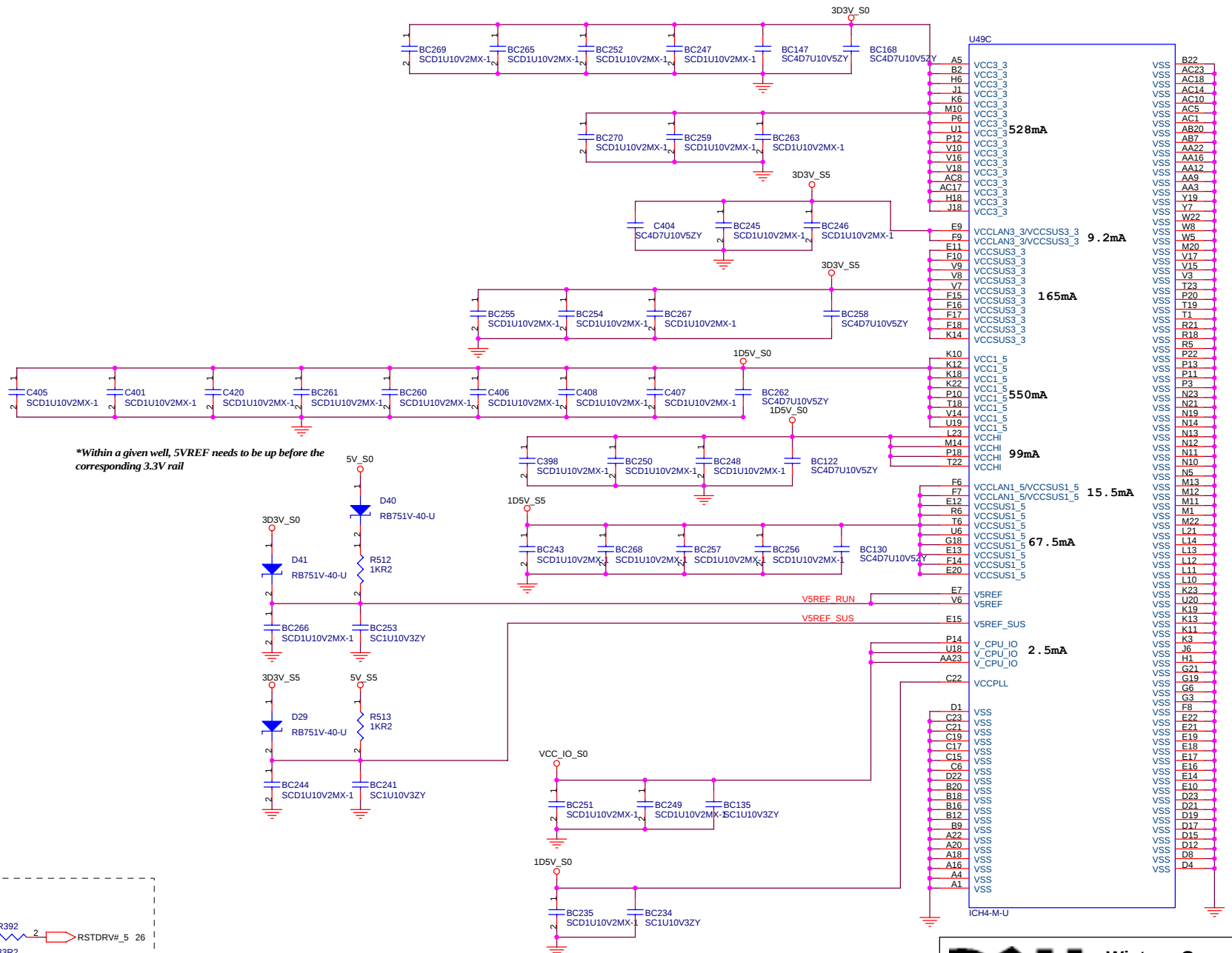
EE_DIN, EE_DOUT, PME#, PWRBTN#	ICH4 internal 20K pull-ups
GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

ICH4 IDE Integrated Series Termination Resistors

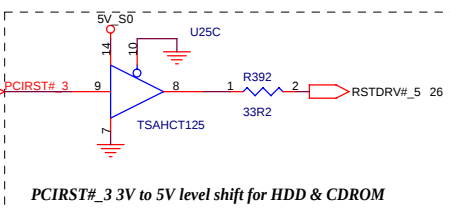
PDD[15:0], SDD[15:0], PDIOW#, SDIOW#, PDIOR#, PDIOW#, PDREQ, SDREQ, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15,	approximately 33 ohm
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**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



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Title: **ICH4-M (3 of 3)**

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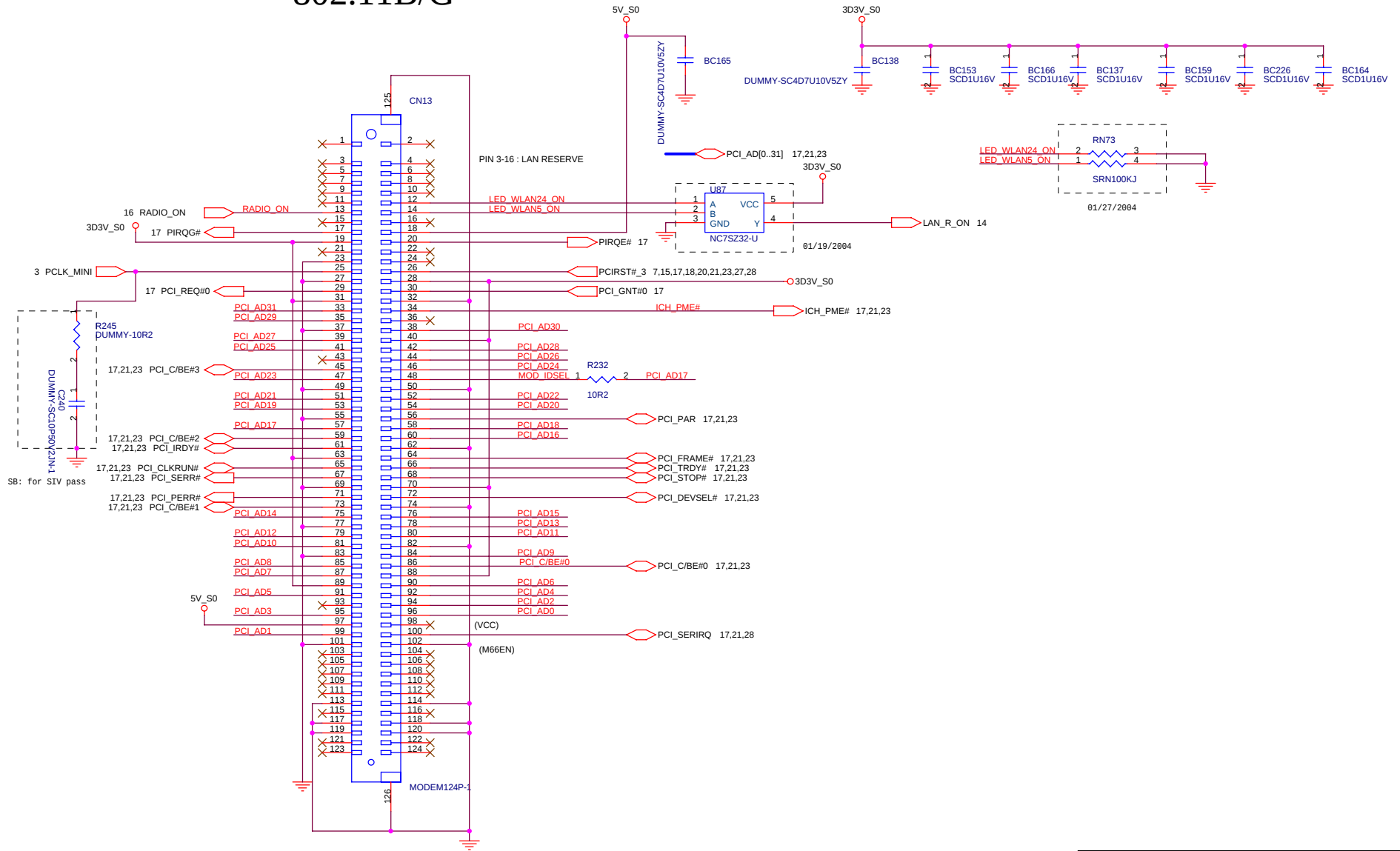
Date: Thursday, April 15, 2004

Document Number: **MOLOKAI**

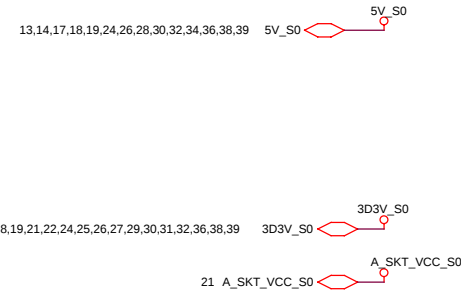
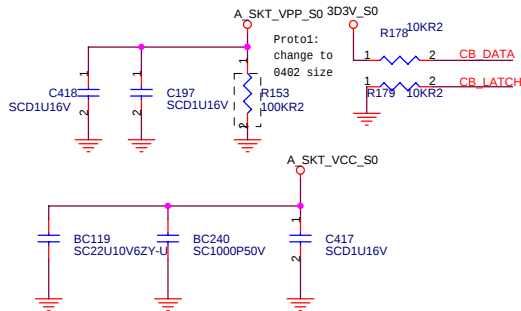
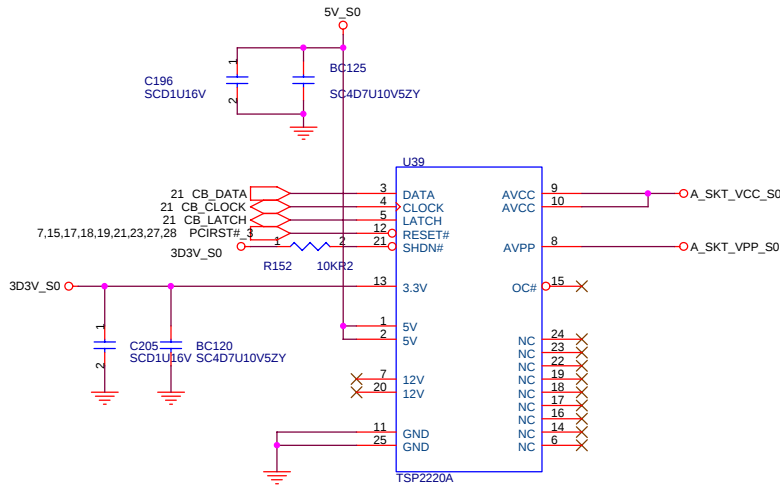
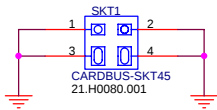
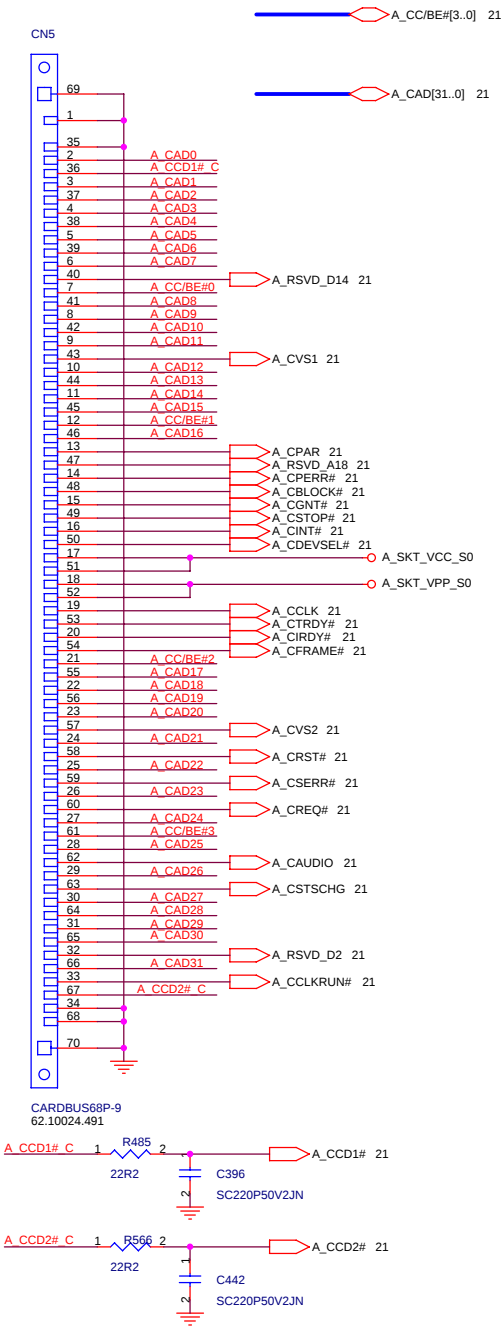
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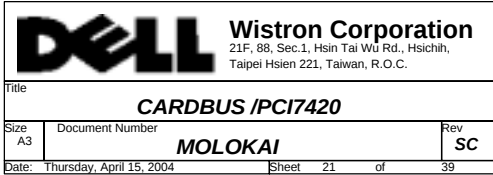
Mini PCI 802.11B/G

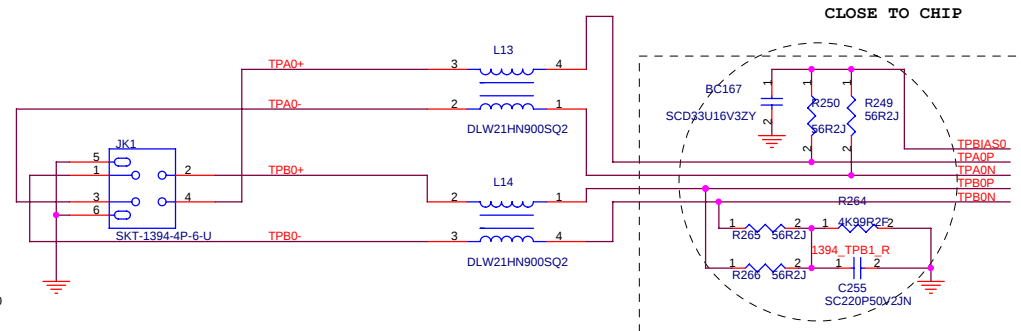
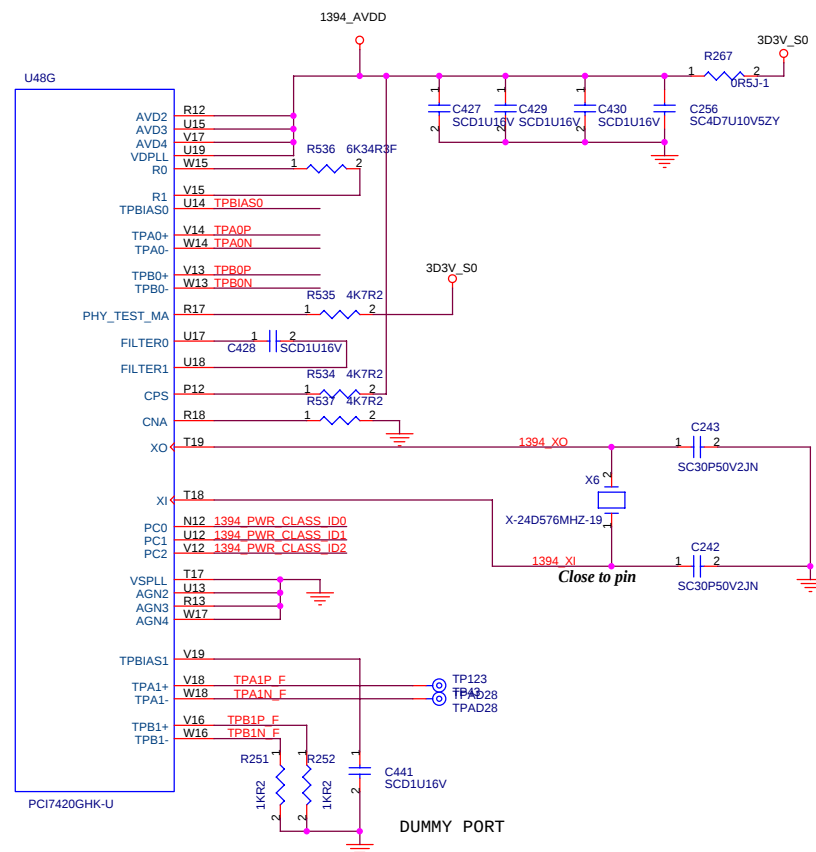
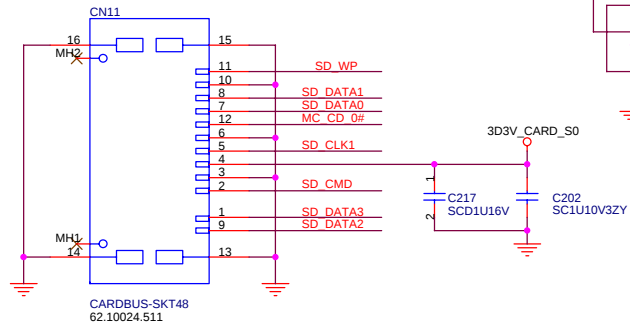
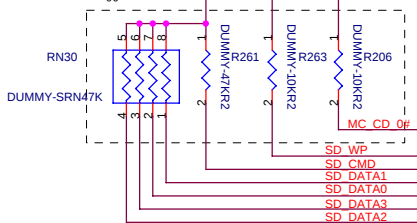
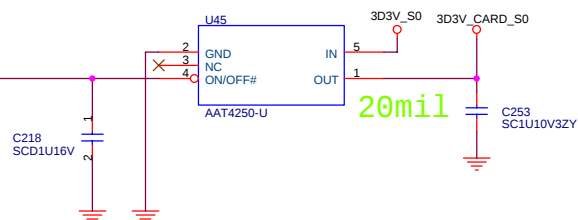
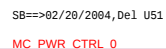
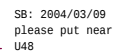
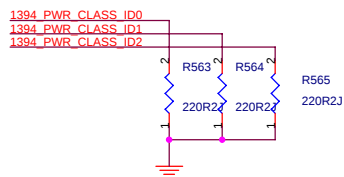


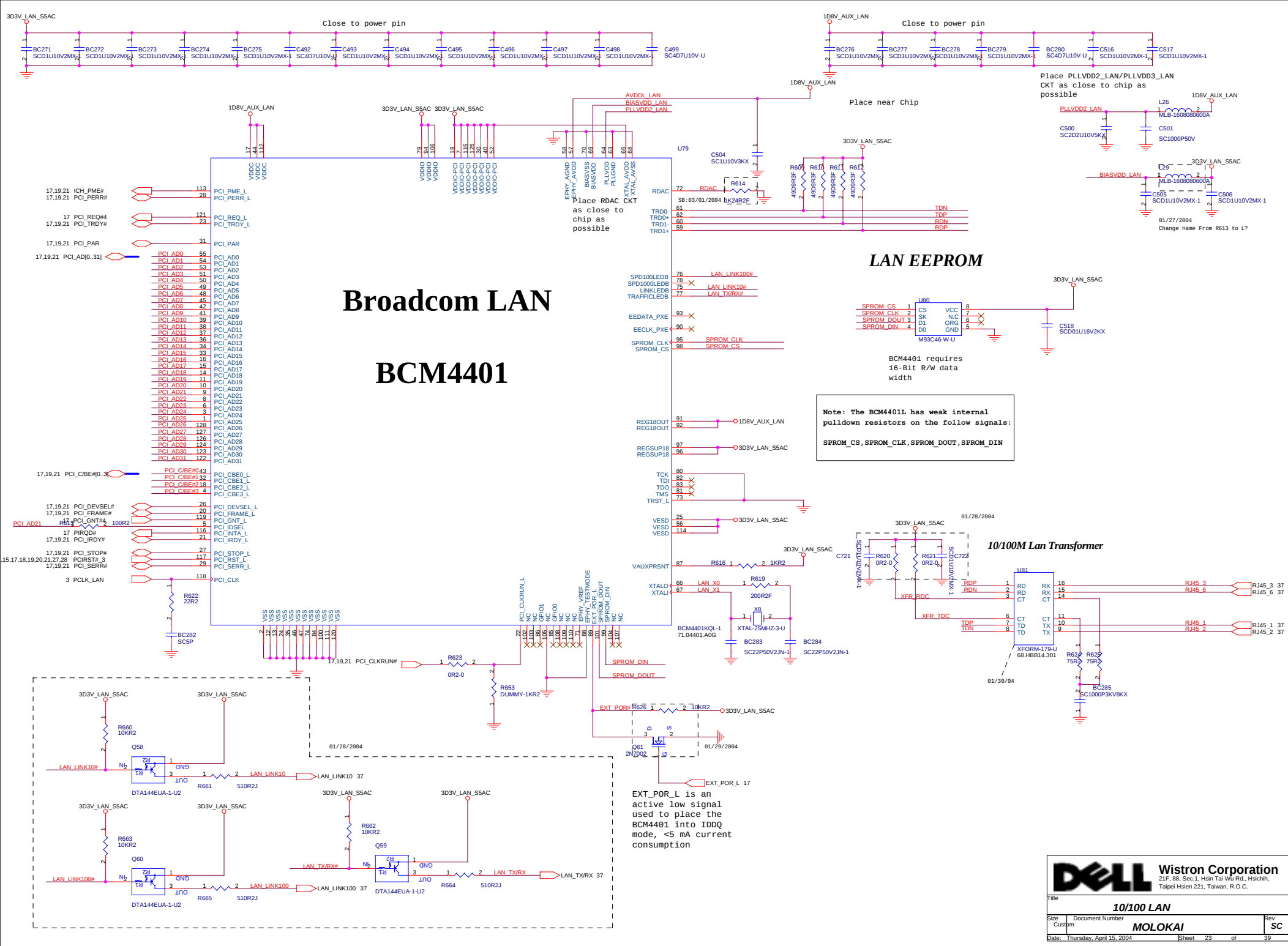
PCMCIA socket

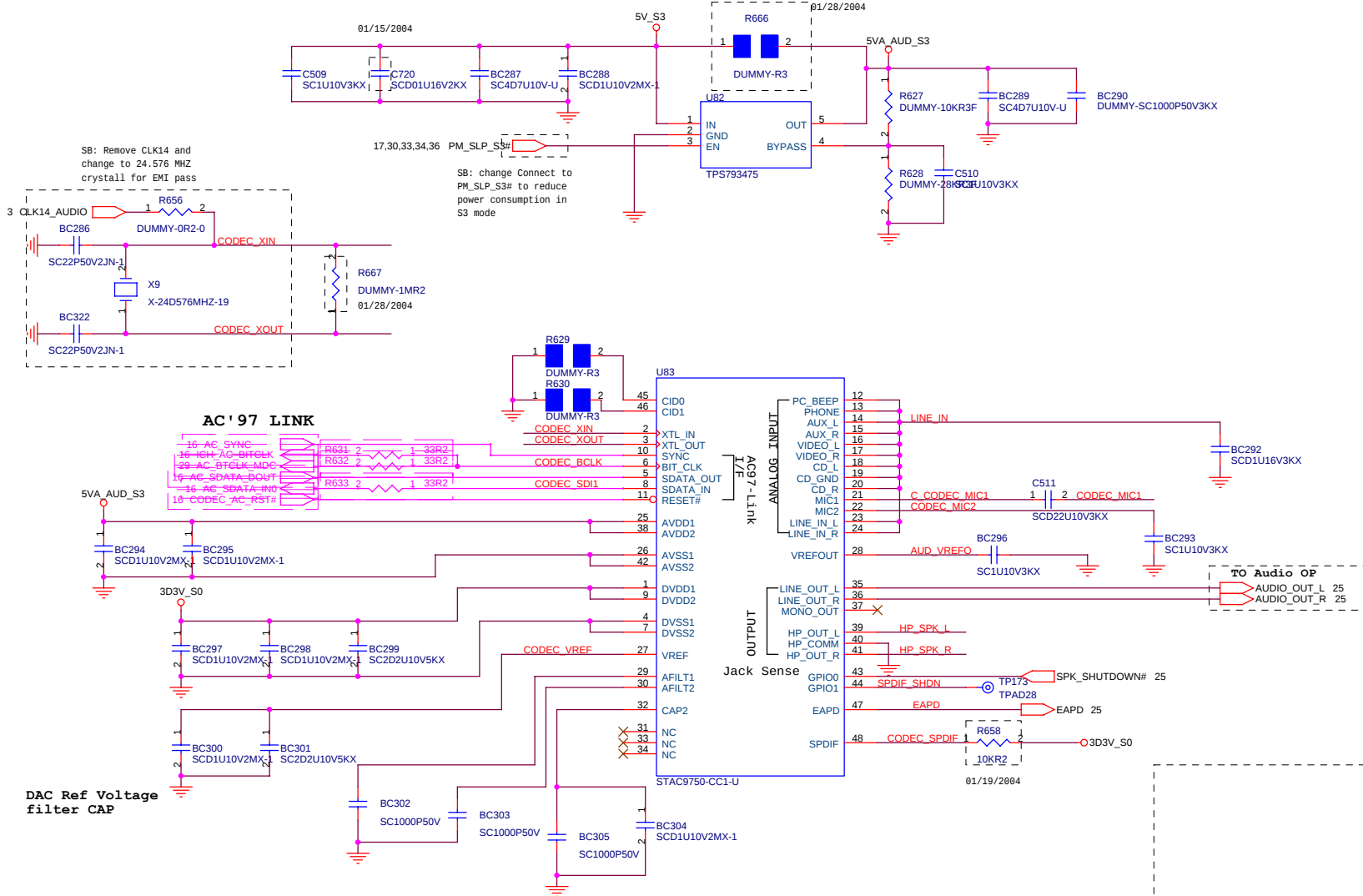


DELL		Wistron Corporation	
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Title CARDBUS CONN / PWR SW			
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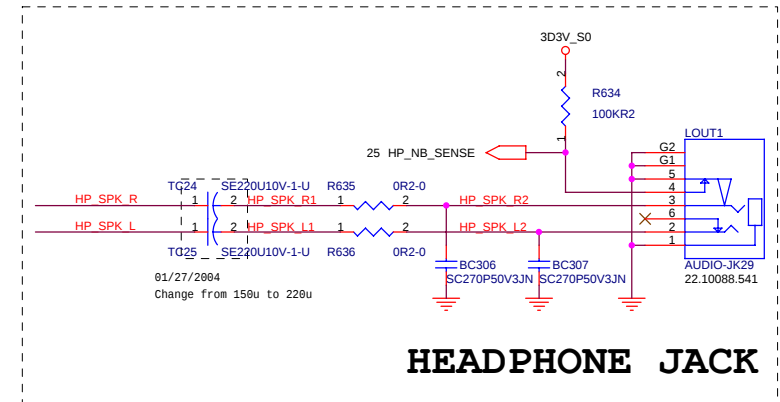
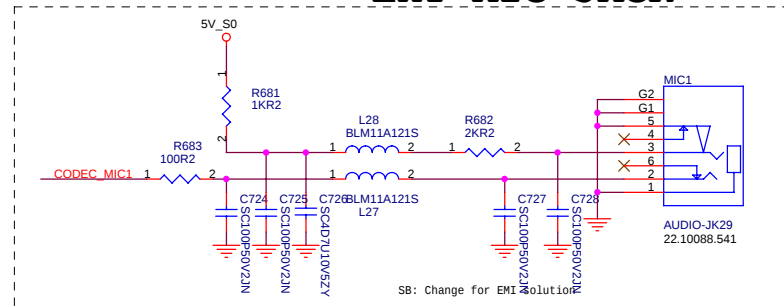






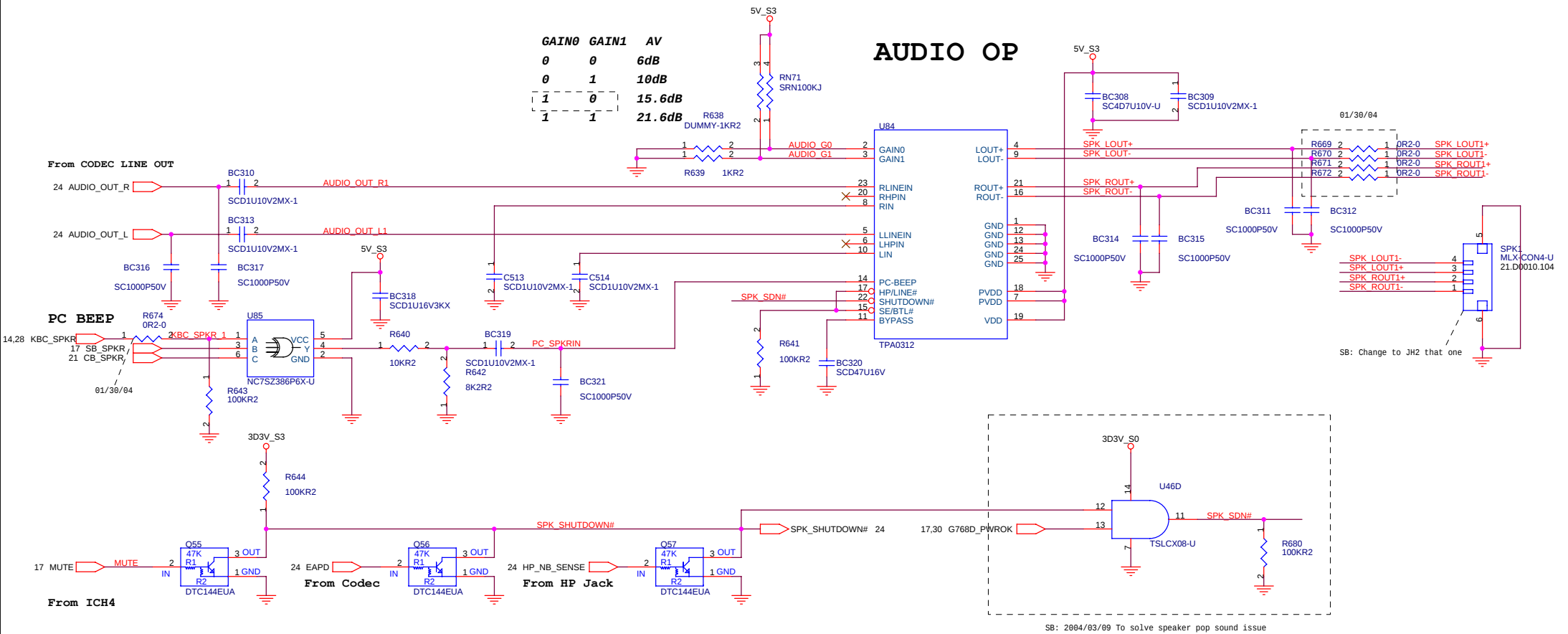


EXT MIC JACK

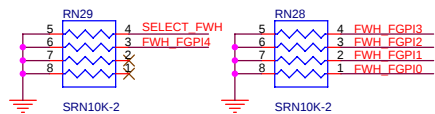


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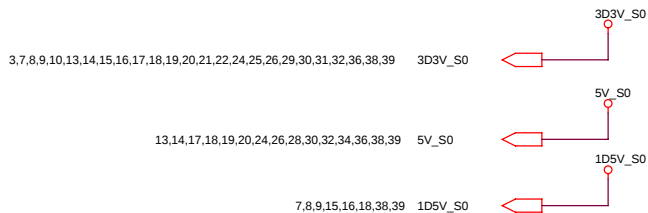
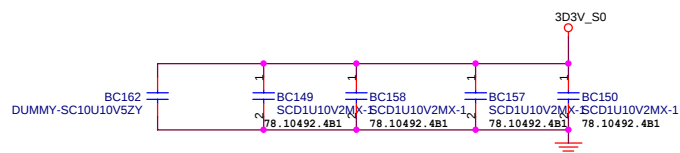
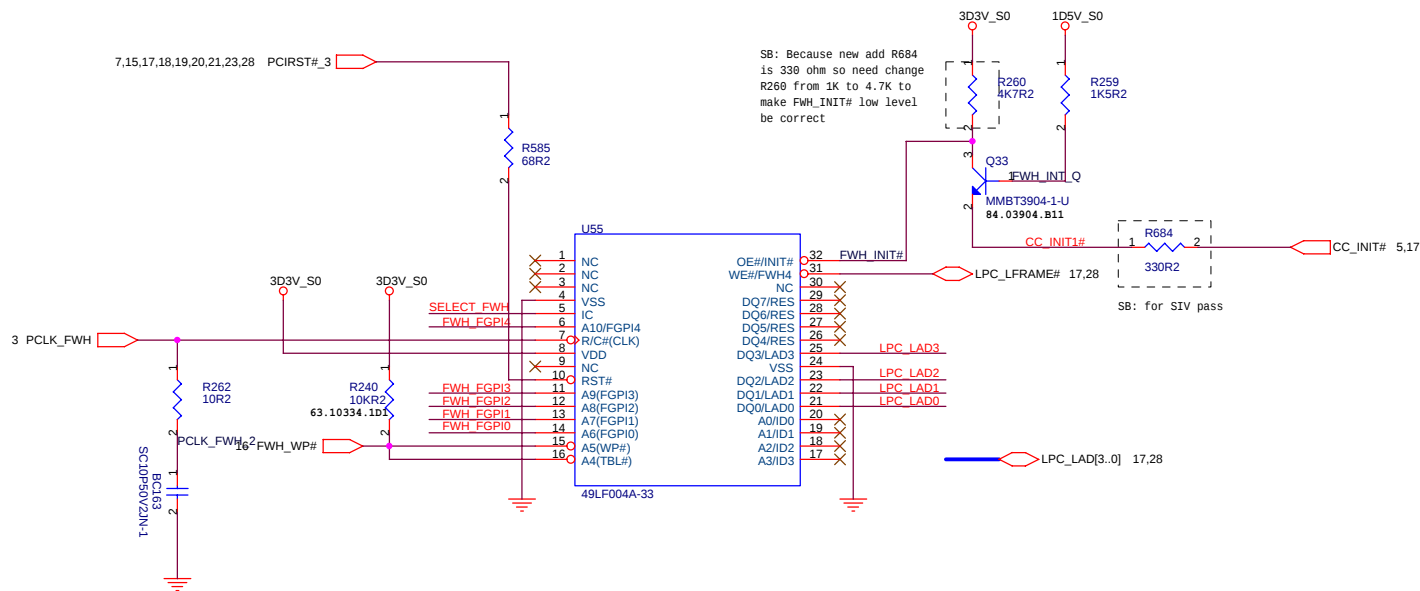
Title			
AUDIO (1 of 2) -- Codec			
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Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

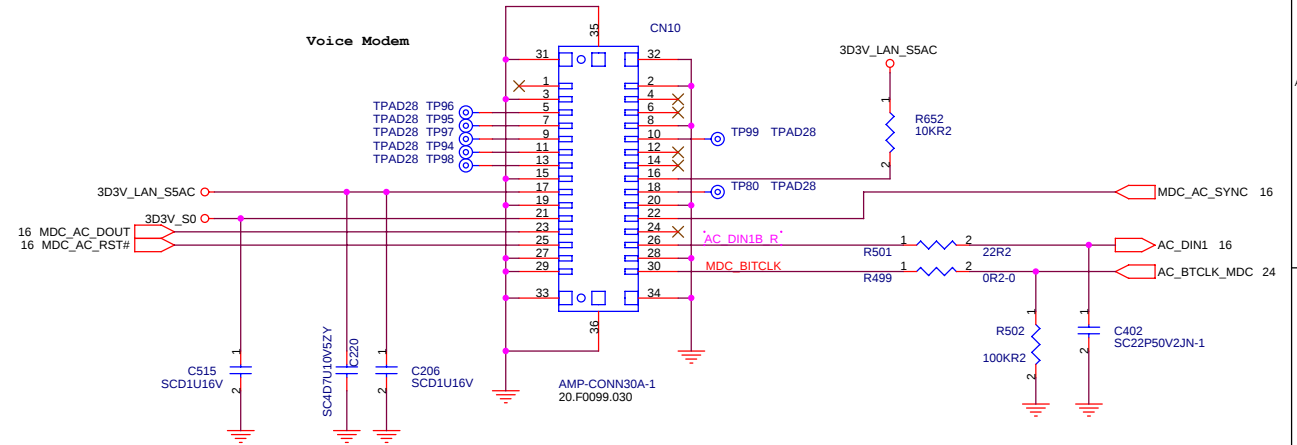


Unused FGPI pins must not be float

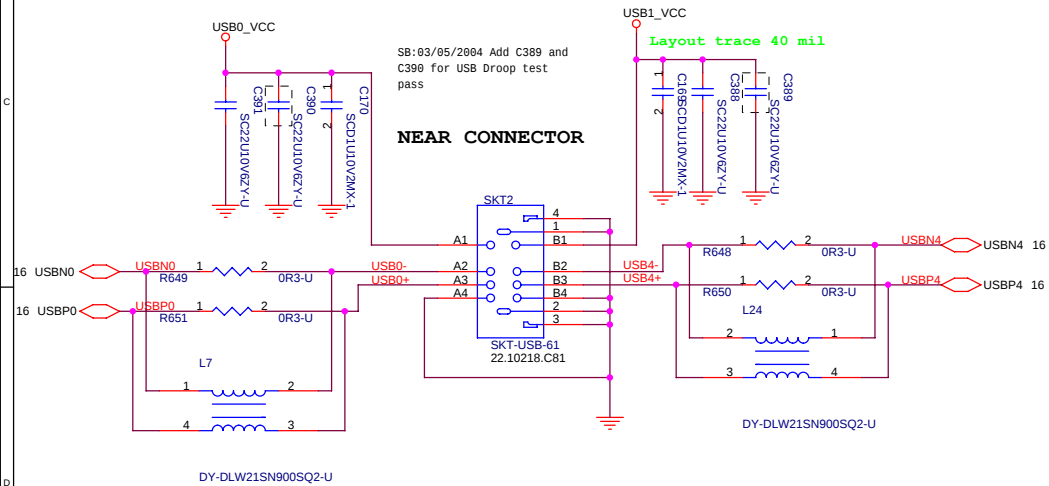




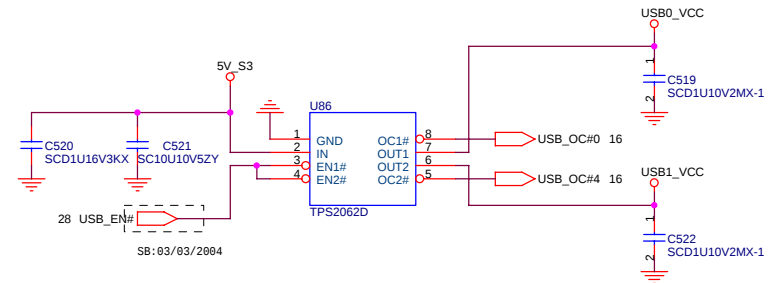
MDC CONN



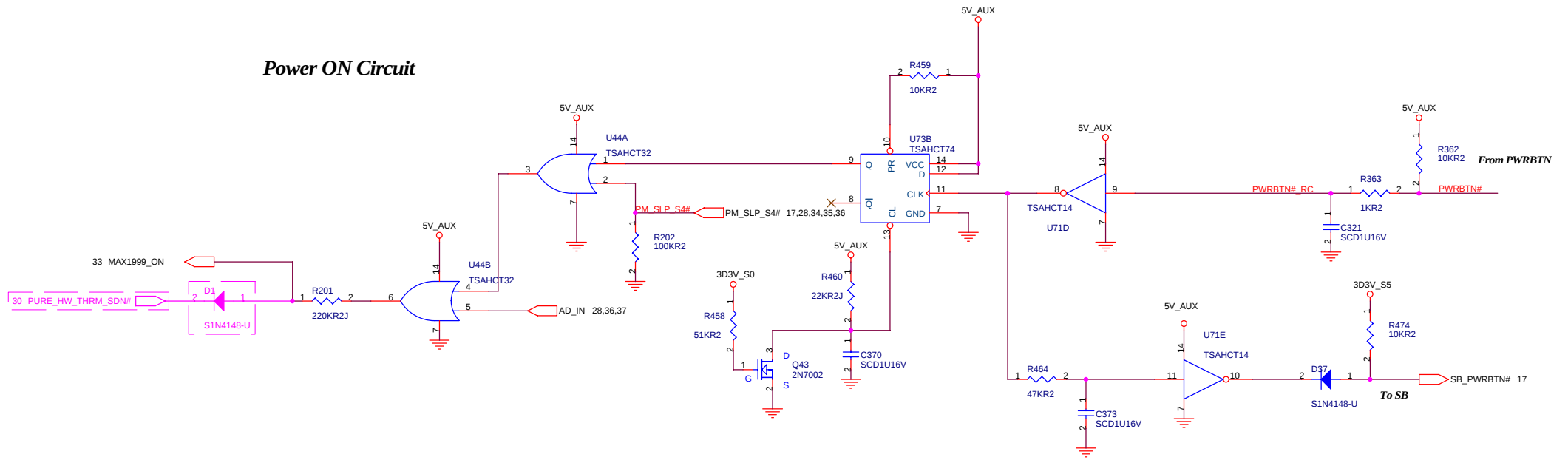
USB PORT



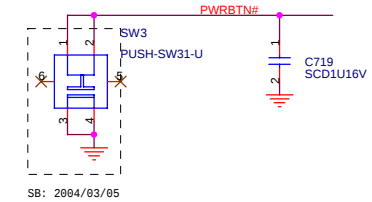
Dual USB switch



Power ON Circuit



PWRBTN



Title			
POWER ON CIRCUIT			
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	Active	Deep	Deeper
DPRSLPVR	0	0	1
STP CPU#	1	0	0

```
Active Mode:
1.Highest Frequency:
VID=1.484V/1.00V
2.Lowest Frequency:
VID=0.956V/0.85V

Deep Sleep Mode:
1.Highest Frequency: VID=1.484V,Offset=-1.2%>VID=1.466
2.Lowest Frequency: VID=0.956V,Offset=-1.2%>VID=0.945

Deeper Sleep Mode:
VID=0.748V
```

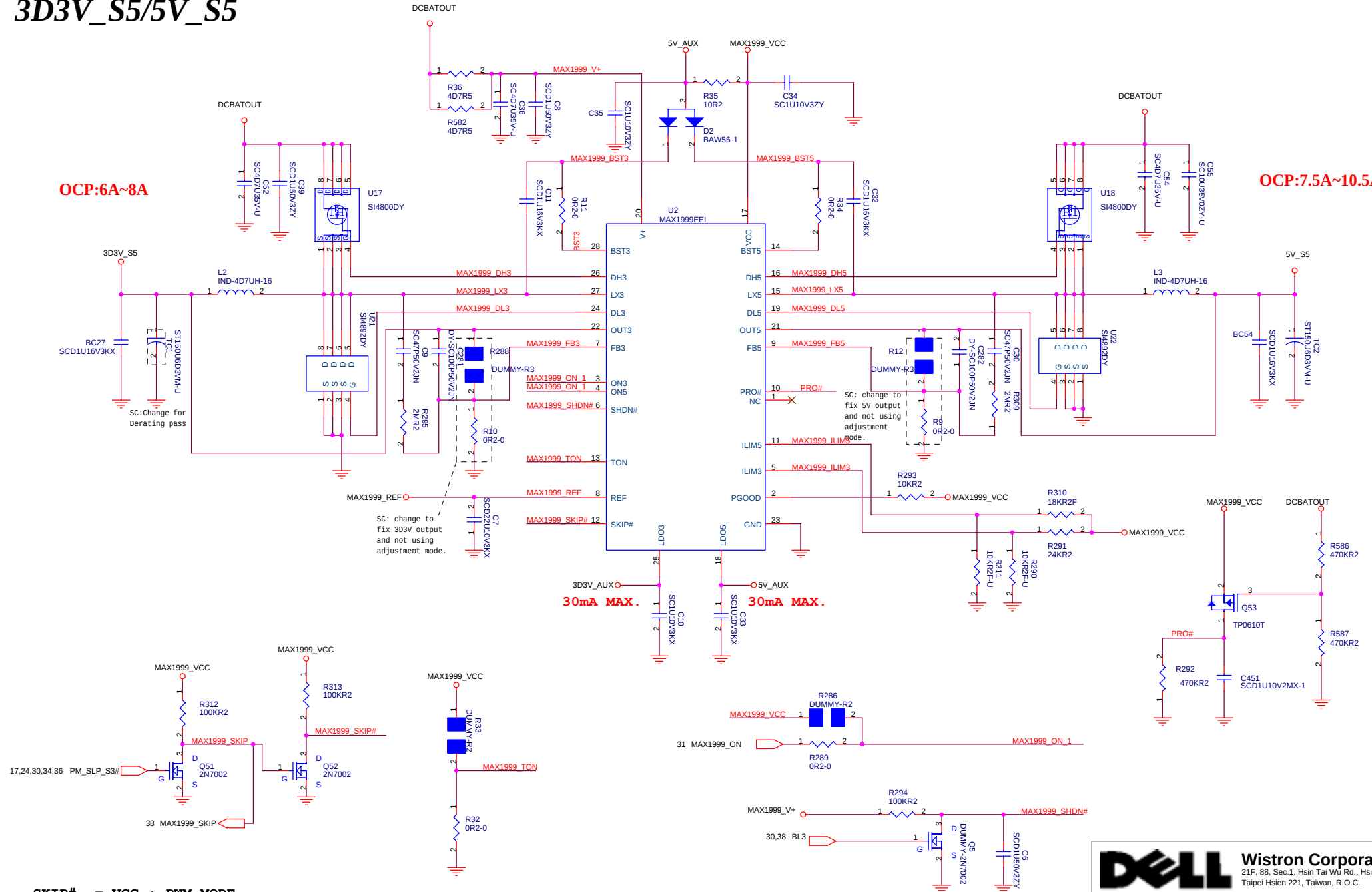
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IMVP IV-CPU POWER-ISL6218			
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SYSTEM DC/DC

3D3V_S5/5V_S5

OCP:6A~8A

OCP:7.5A~10.5A



SKIP# = VCC : PWM MODE
 SKIP# = GND : SKIP MODE
 SKIP# = REF/Floating : Ultrasonic MODE
 (25KHz min)

Ton = VCC : 200KHz/300KHz
 Ton = GND : 400KHz/500KHz
 (5V/3D3V)

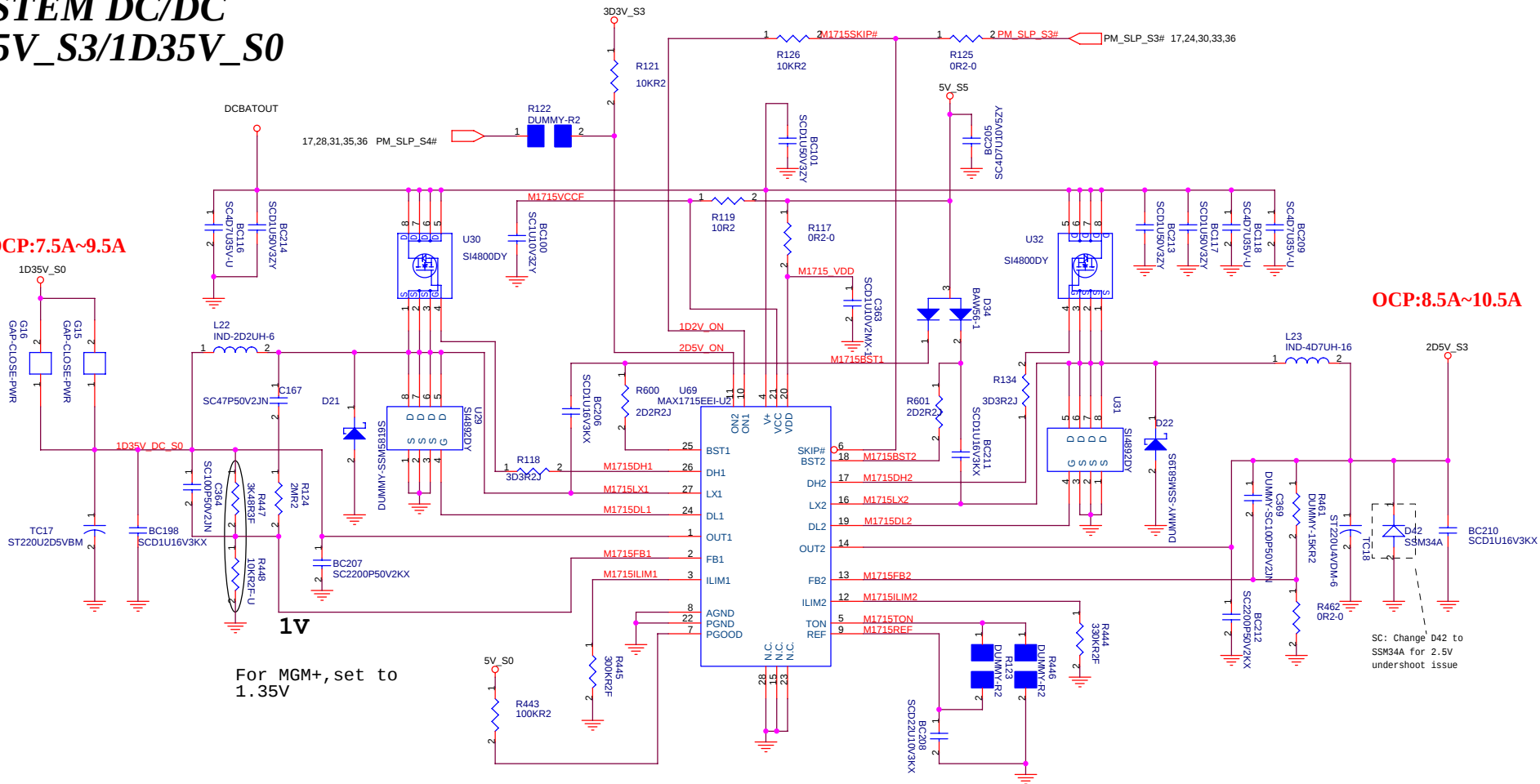
Wistron Corporation
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Title MAX1999/3D3V_S5/5V_S5		
Size A3	Document Number MOLOKAI	Rev SC
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SYSTEM DC/DC 2D5V_S3/1D35V_S0

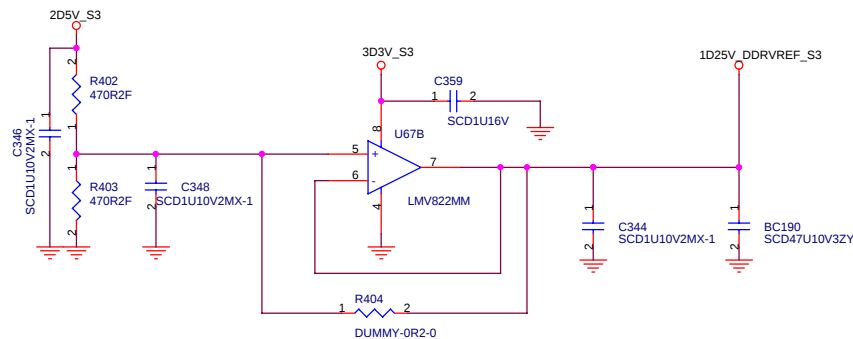
OCP:7.5A~9.5A

OCP:8.5A~10.5A



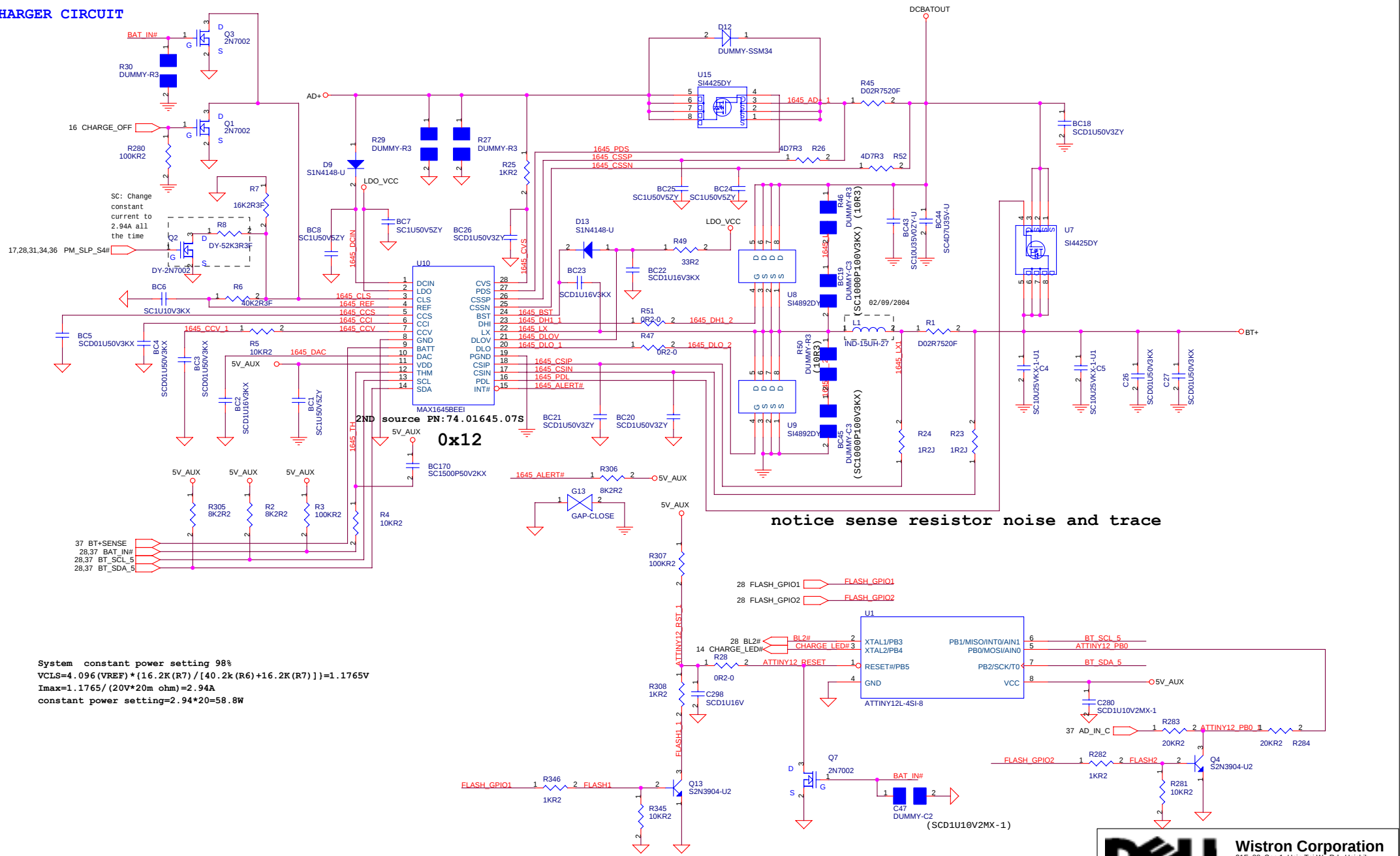
For MGM+, set to 1.35V

1D25V_DDRVREF_S3 need 10 mil and must near NB/DIMM



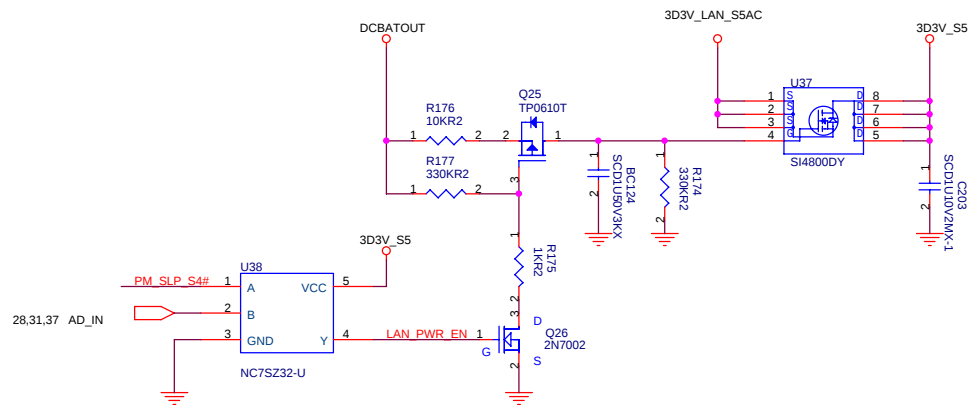
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Title: MAX1715/2D5V_S3/1D35V_S0			
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CHARGER CIRCUIT

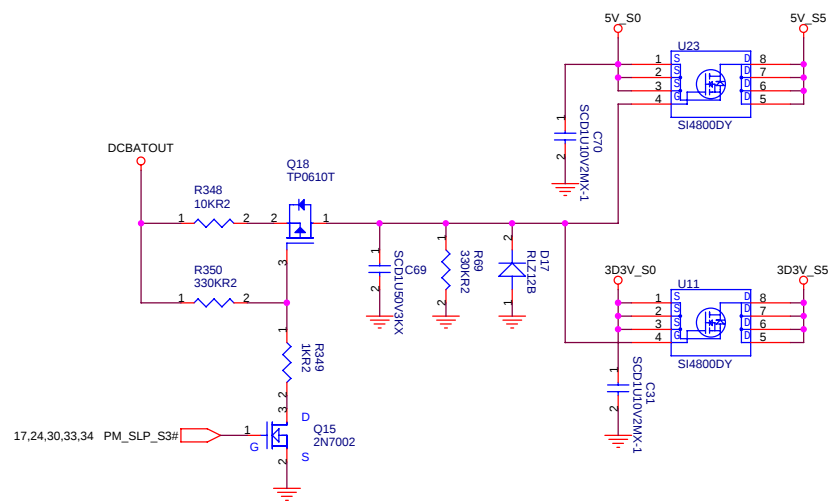


System constant power setting 98%
 $V_{CLS}=4.096(V_{REF}) * \{16.2K(R7) / [40.2k(R6)+16.2K(R7)]\}=1.1765V$
 $I_{max}=1.1765 / (20V*20m\ ohm)=2.94A$
constant power setting=2.94*20=58.8W

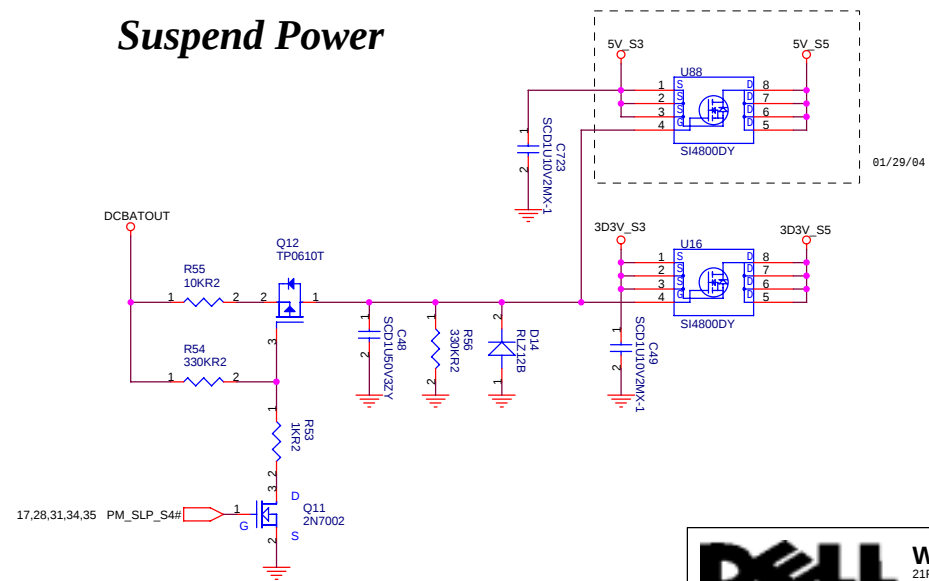
LAN Power



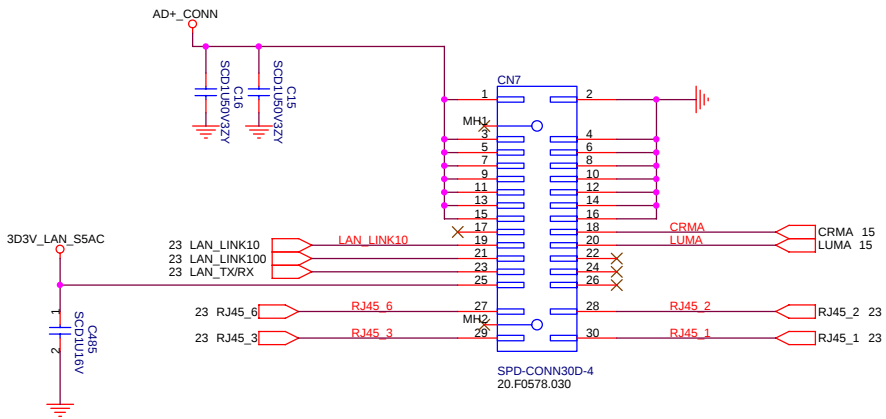
Run Power



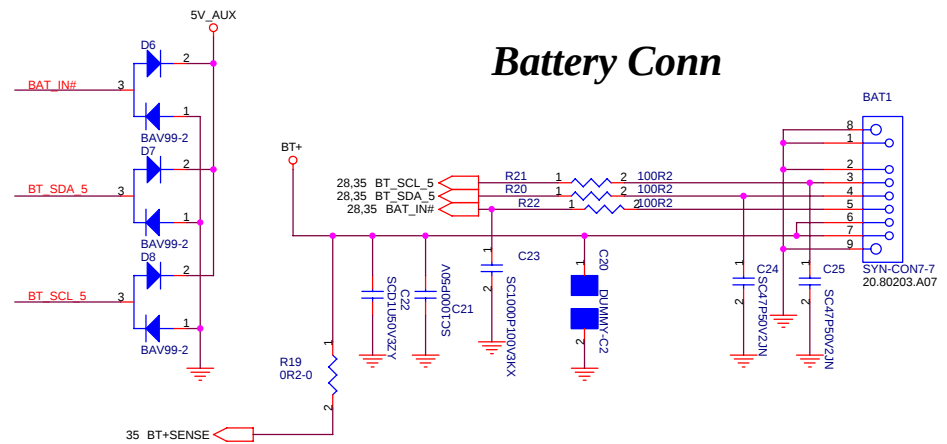
Suspend Power



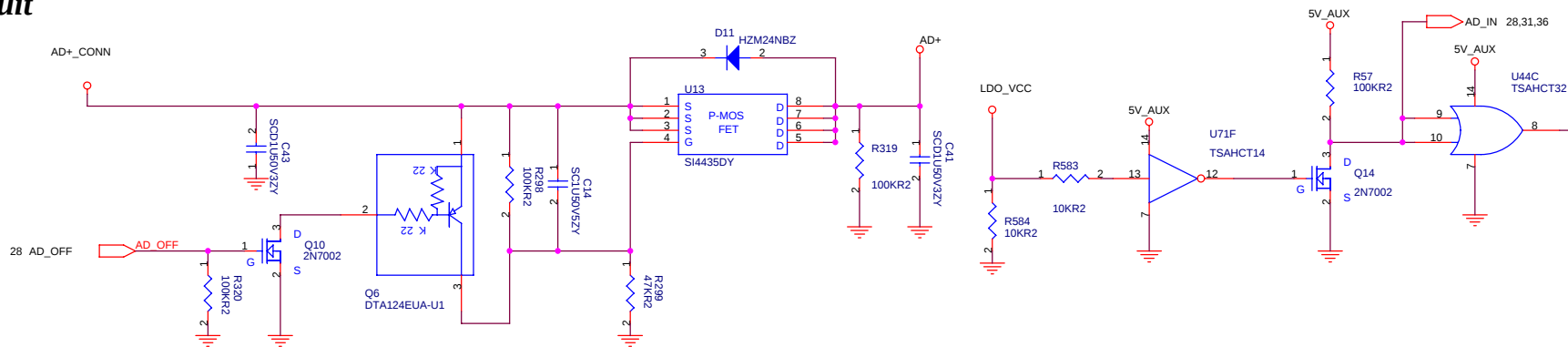
TV BD Conn



Battery Conn



Adaptor In Circuit



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Title

Battery Conn/TV BD Conn/Adaptor In Circuit

Size	Document Number
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MOLOKAI

Rev

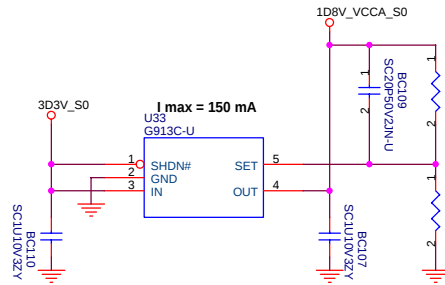
SC

Date: Thursday, April 15, 2004

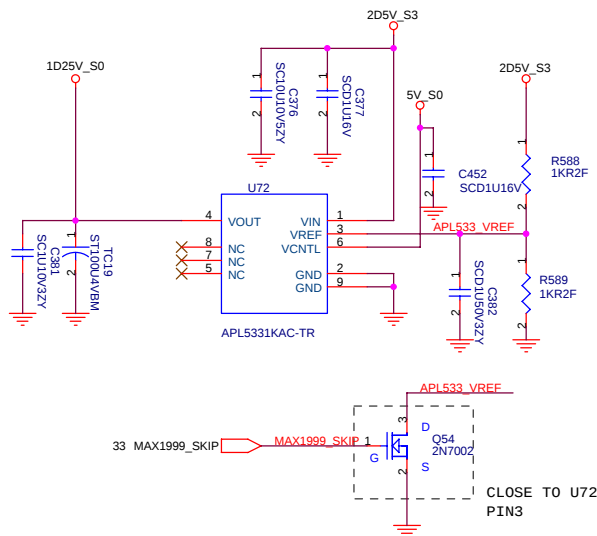
Sheet 37 of 39

At Dothan CPU application, POWER is 1.5V or 1.8V.

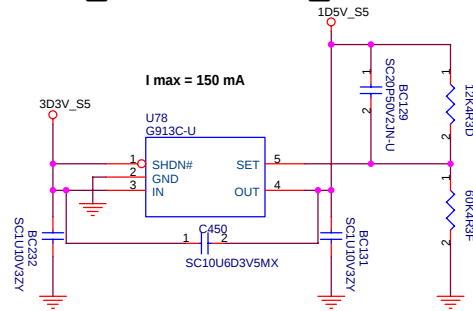
3D3V_S0 --> 1D8V_VCCA_S0
(For CPU VCCA)



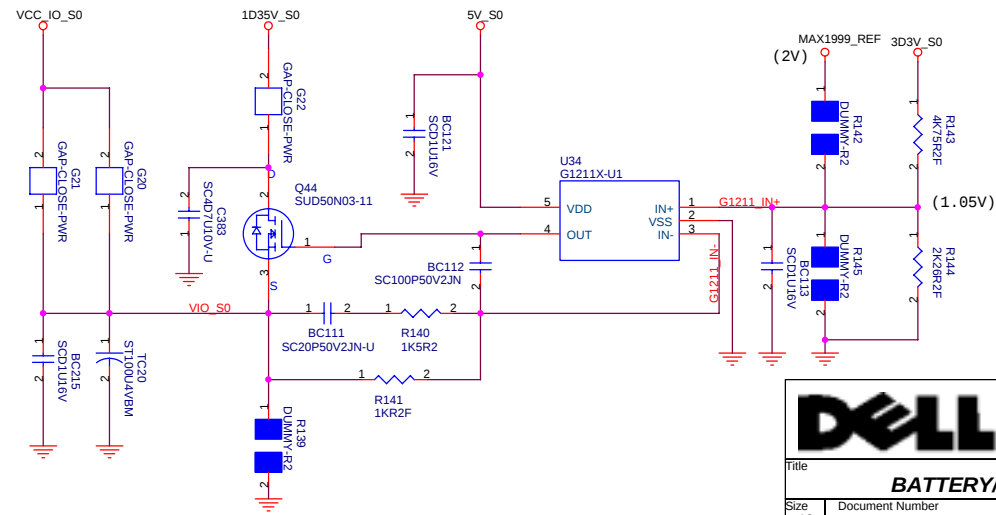
2D5V_S3 → 1D25V_S0



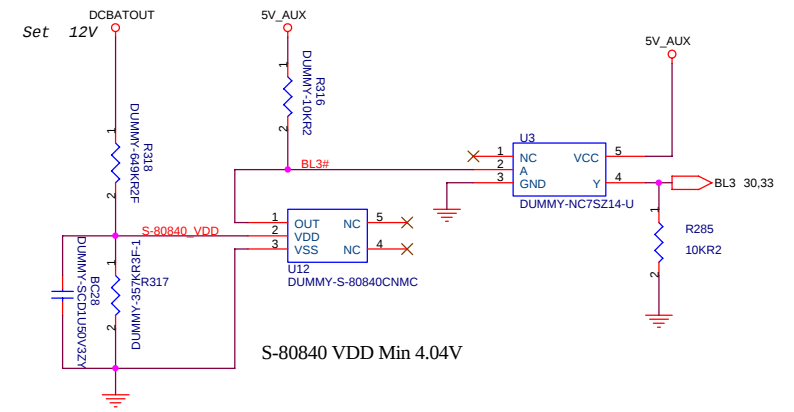
3D3V_S5 --> 1D5V_S5



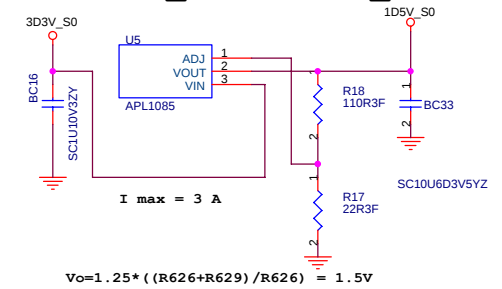
1D35V_S0 → VCC_IO_S0 (1.05V)



BATTERY LOW3 DETECTOR

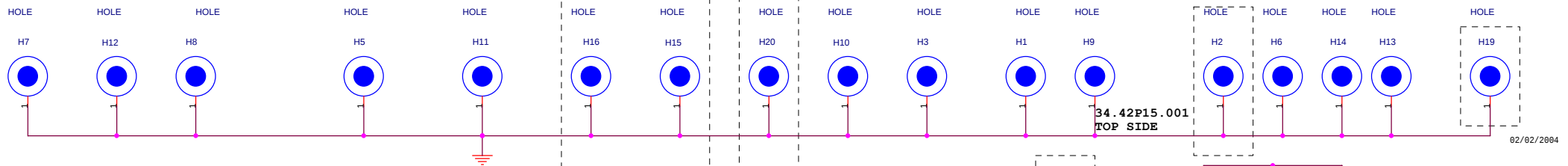
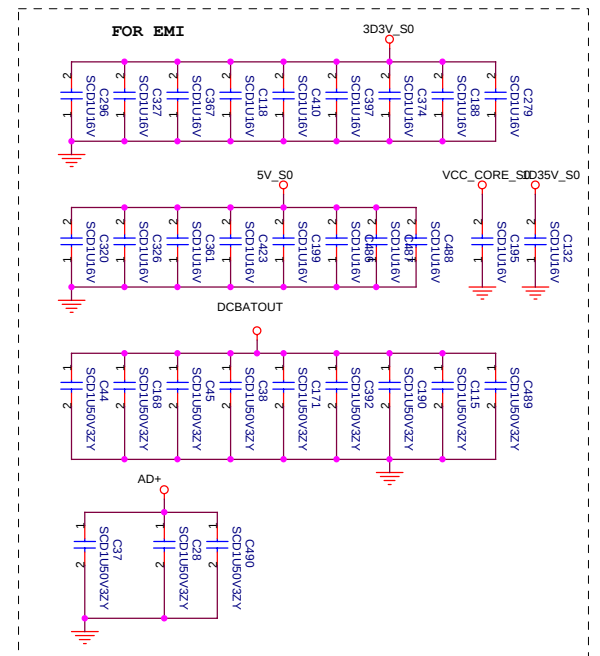
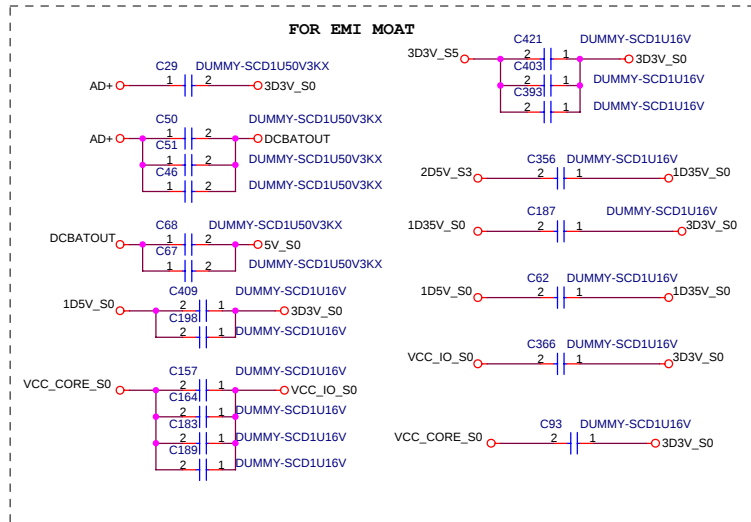
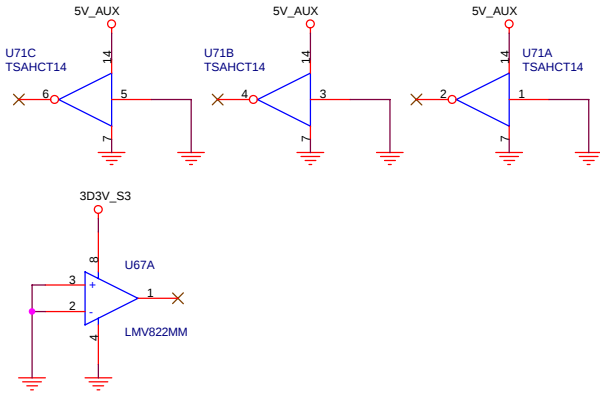
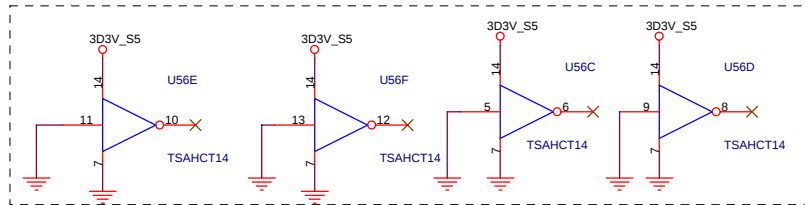
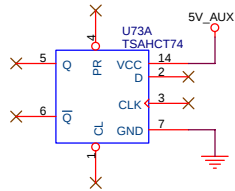
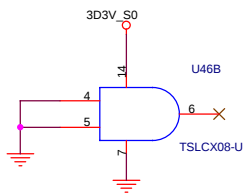


3D3V_S0 → 1D5V_S0



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34.41Q08.001
BOT SIDE

34.41P25.001
TOP SIDE

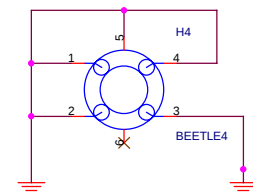
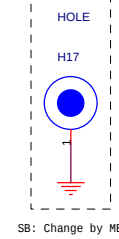
34.34S02.001
BOT SIDE

34.41P23.001
BOT SIDE

34.41D14.001
TOP SIDE

34.41P18.001
TOP SIDE

34.45V04.001
BOT SIDE



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Title		
MISC		
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