UL20A SCHEMATIC Revision 2.0

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5	CPU-CAPACITORS
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9	DIM-DDR3 VREF & TERMINATION
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11	NB_-GS45-DMI (2)
12	NB_-GS45-DISPLAY (3)
13	NB_-GS45-DDR2 BUS (4)
14	NB_-GS45-POWER (5)
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29	CLK-RTM875T-336-GRT
30	KBC-ITE8512
31	ROM-FLASH ROM,TOUCH PAD,KB
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46	CRT-LVDS CONN
49	VID CONTROLLER
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51	XDD-SATA HDD CONN
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56	LED- PWR,LED,FPC CONN
57	DSG-DISCHARGE CIRCUIT
60	DC_-DC, BATT CONN
65	ME_-SCREW HOLE, SMT NUT
67	CMO-CMOS CAMERA
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96	History
97	Power On Sequence

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	POWER PAGE REF.
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81	81_POWER_SYSTEM
82	82_POWER_I/O_+1.05VO
83	83_POWER_I/O_DDR & VTT
84	84_POWER_I/O_ +1.8V
88	88_POWER_CHARGER
90	90_POWER_DETECT
91	91_POWER_LOAD SWITCH
92	92_POWER_PROTECT
93	93_POWER_SIGNAL
94	94_POWER_FLOWCHART
95	95_POWER_LED_VCC BOOST

<Variant Name>

ASUSTeK COMPUTER INC

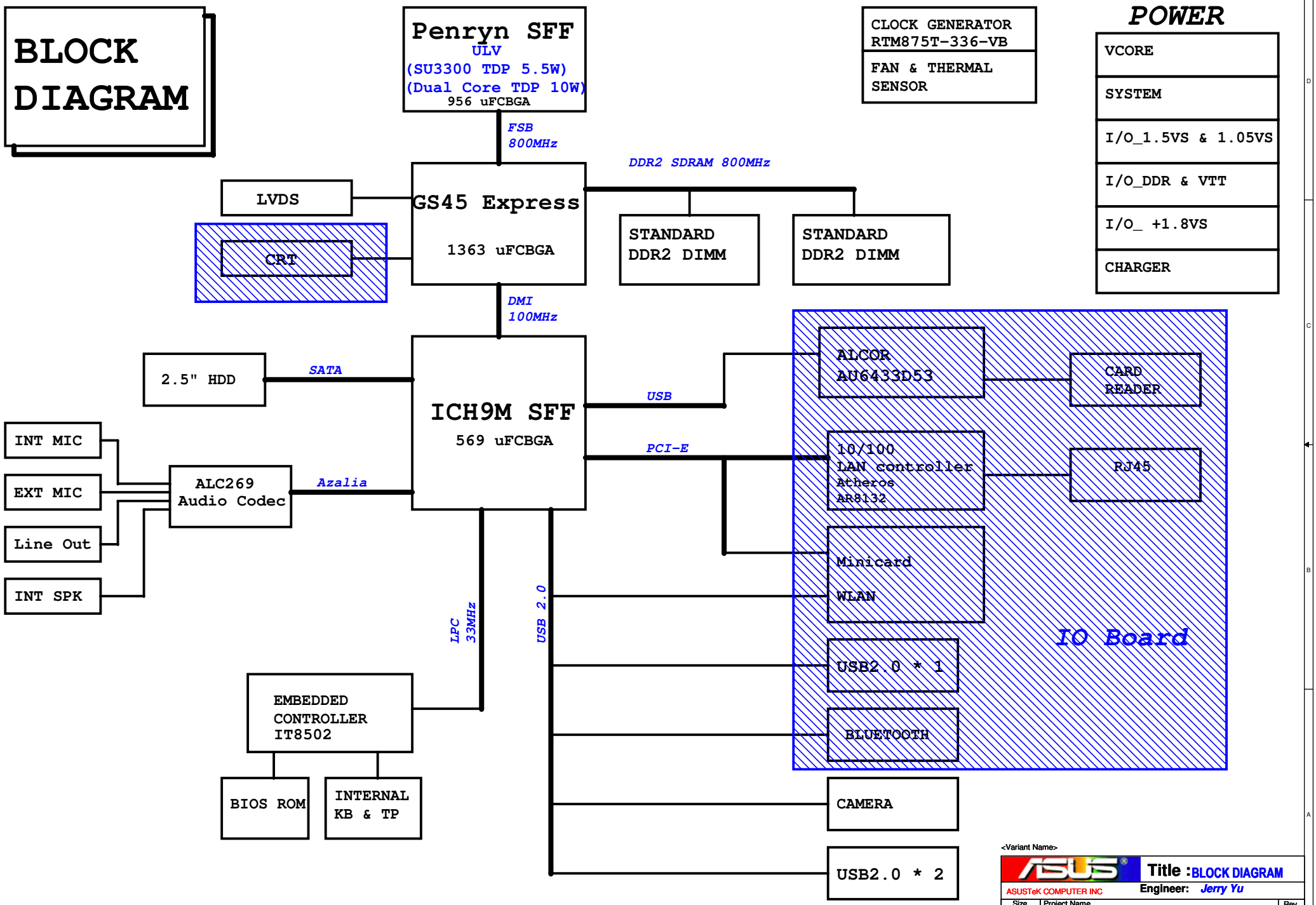
Title : PAGE REF.

Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0

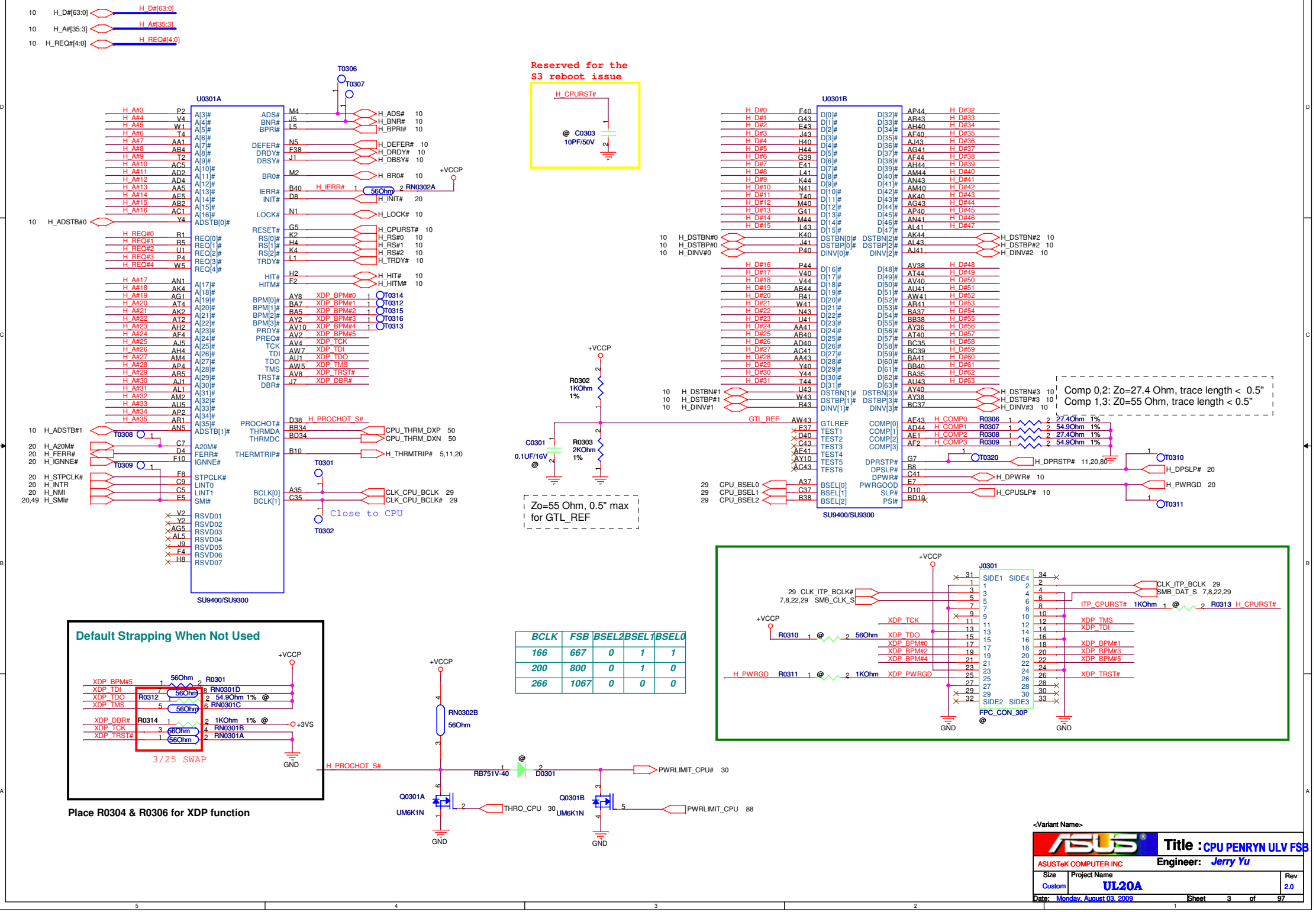
Date: Wednesday, July 29, 2009 Sheet 1 of 97

BLOCK DIAGRAM

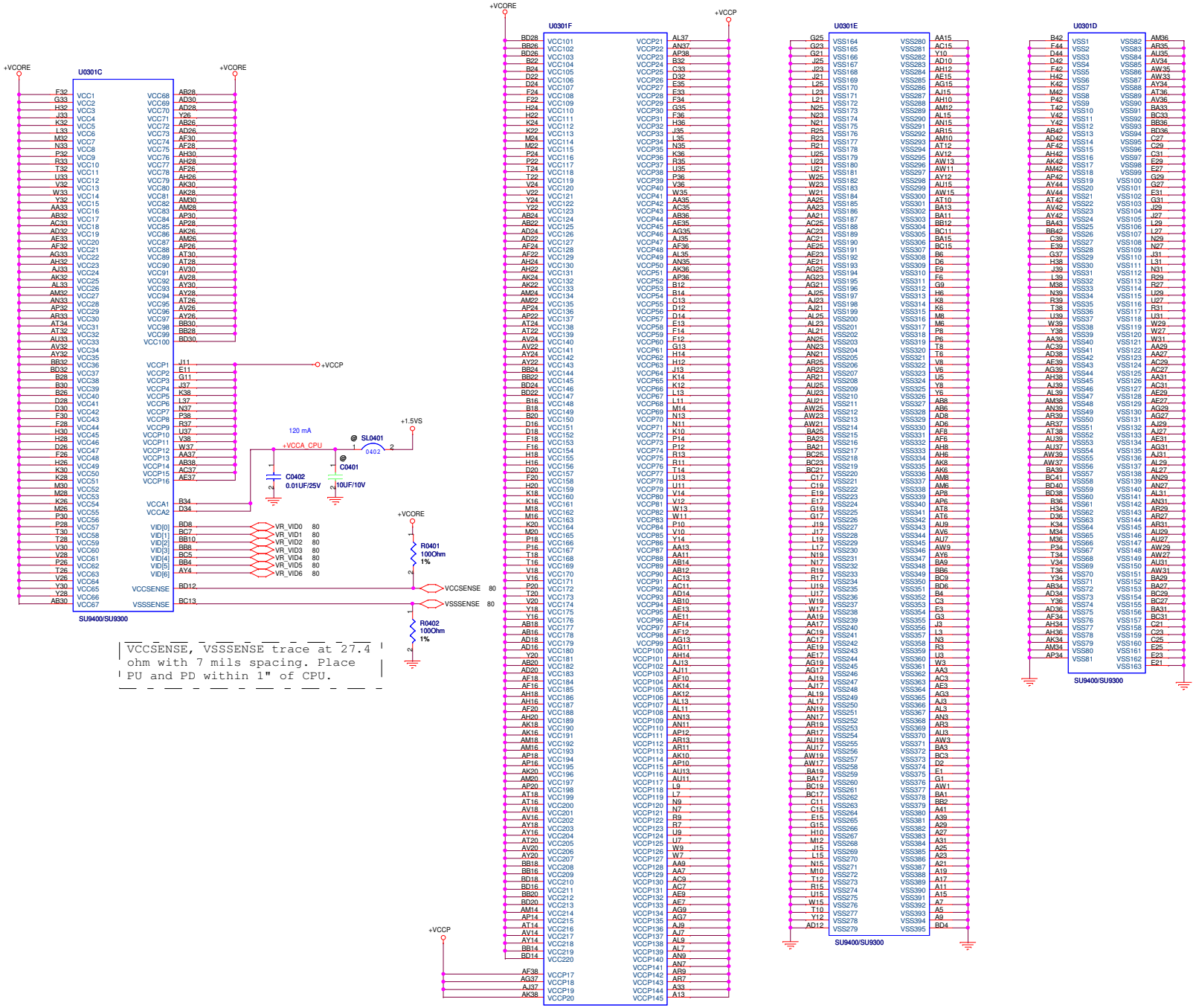


<Variant Name>

ASUS	Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 2 of 97	



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0



<Variant Name>

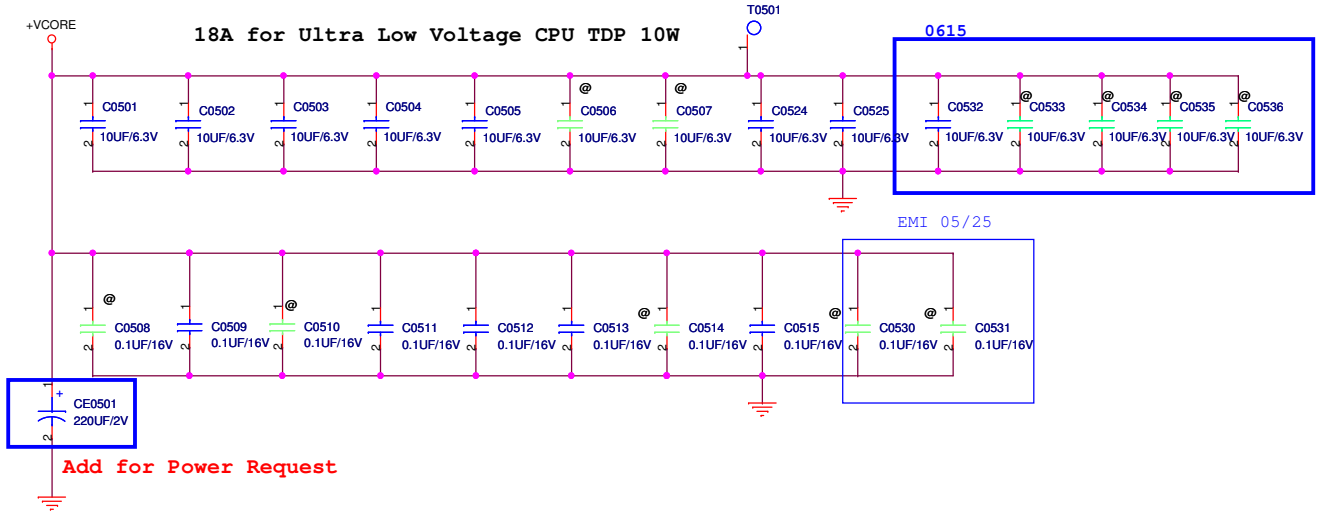
ASUSTeK COMPUTER INC

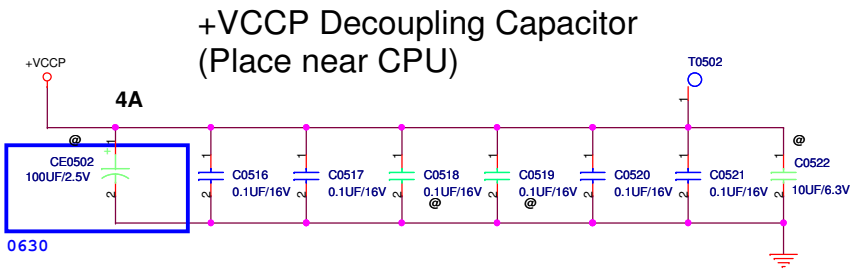
Title : CPU PENRYN ULV POWER

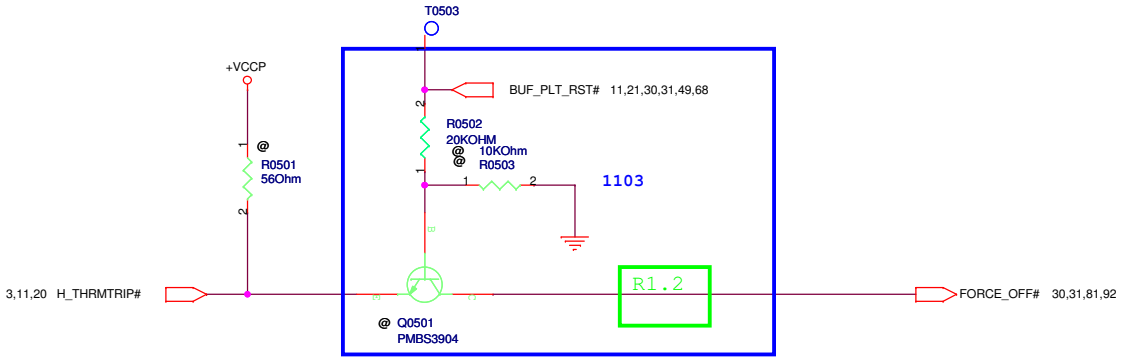
Engineer: Jerry Yu

Size	Project Name	Rev
C	UL20A	2.0

Date: Monday, August 03, 2009 Sheet 4 of 97







Thermal Trip signal (From CPU to ICH-9M and sequence)

Decoupling guide from Intel

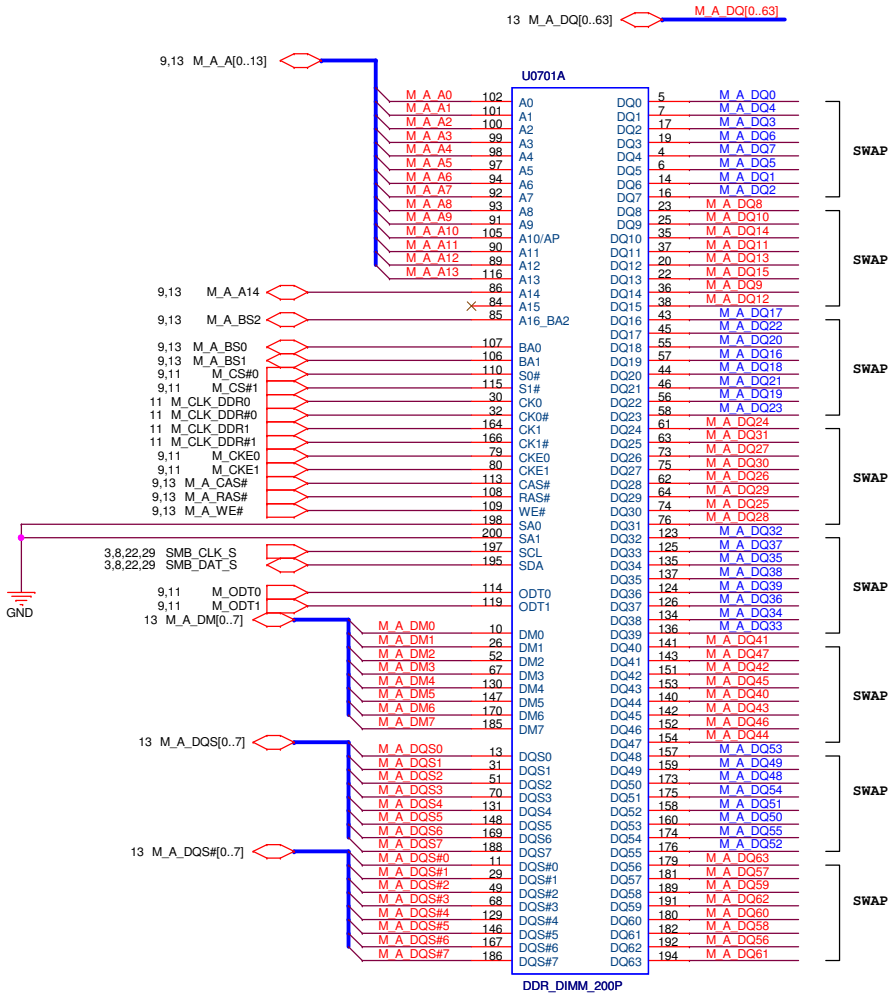
VCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	* 12pcs
	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

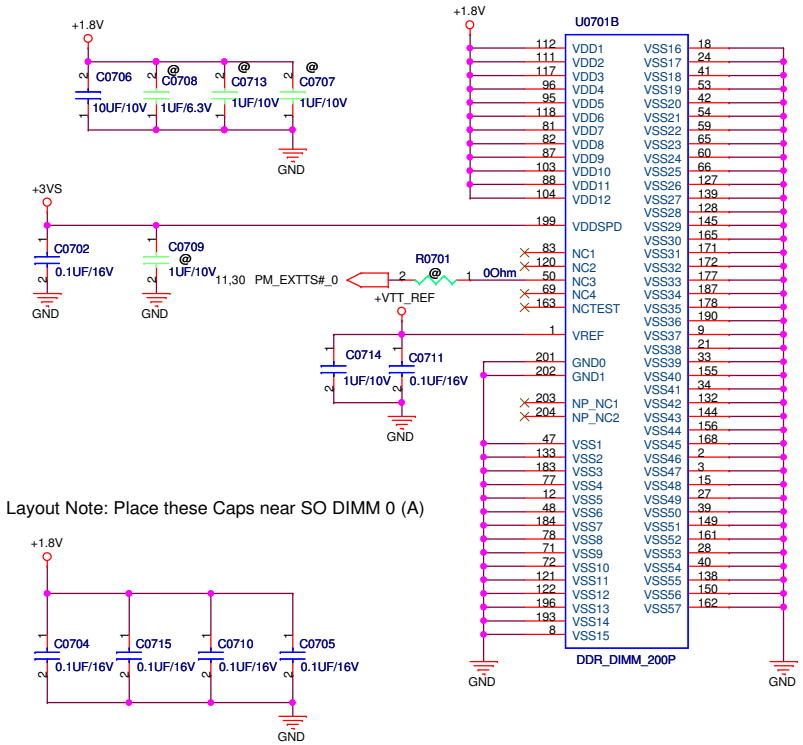
<Variant Name>

ASUSTeK COMPUTER INC	Title : CPU CAPACITORS	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 5 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 6 of 97	



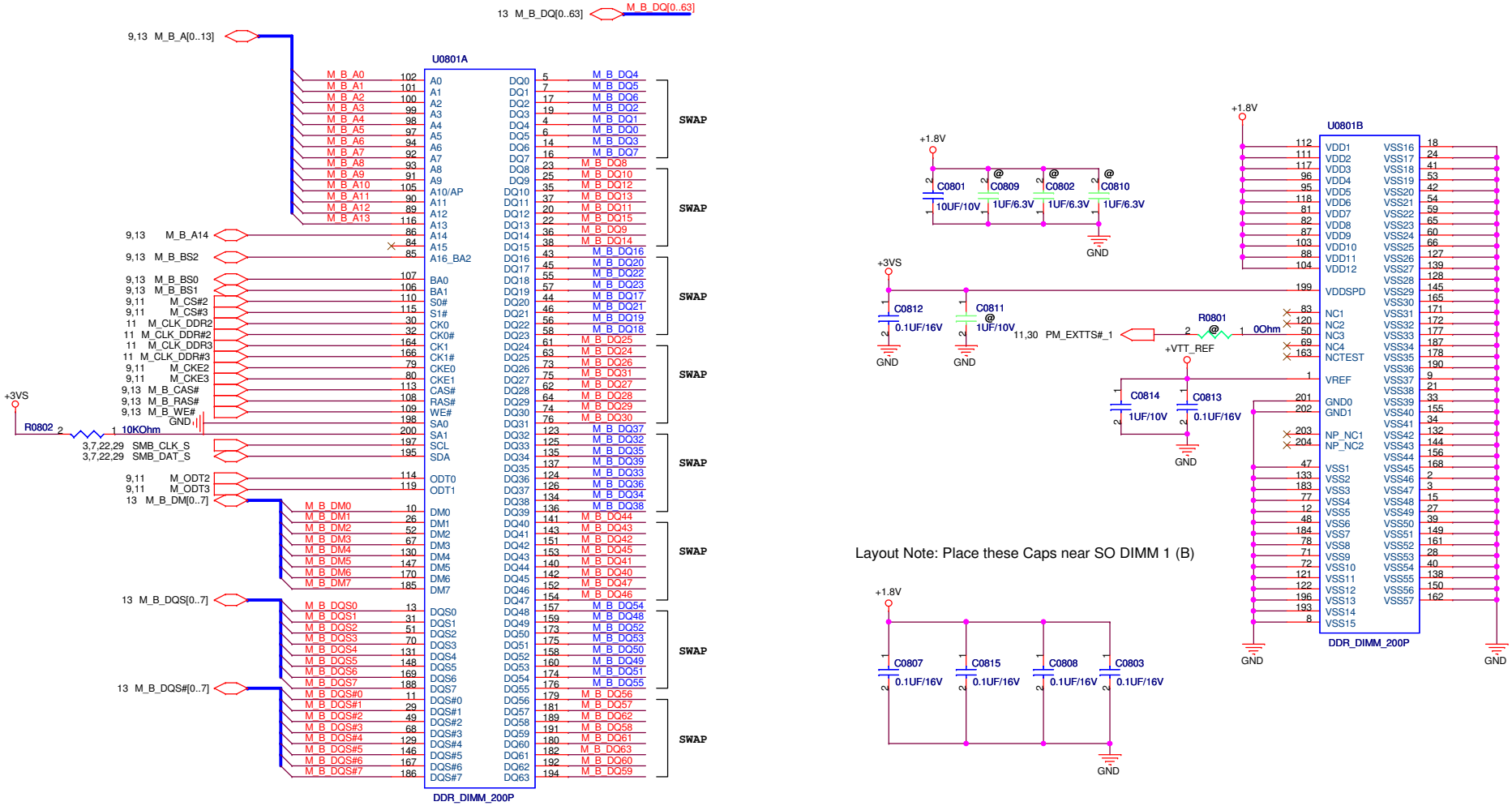


PN : 12G02533200E

STD

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR3 SO-DIMM CHANNEL A		
	Engineer: Jerry Yu		
Size: Custom	Project Name: UL20A		Rev: 2.0
Date: Monday, August 03, 2009	Sheet 7 of 97		

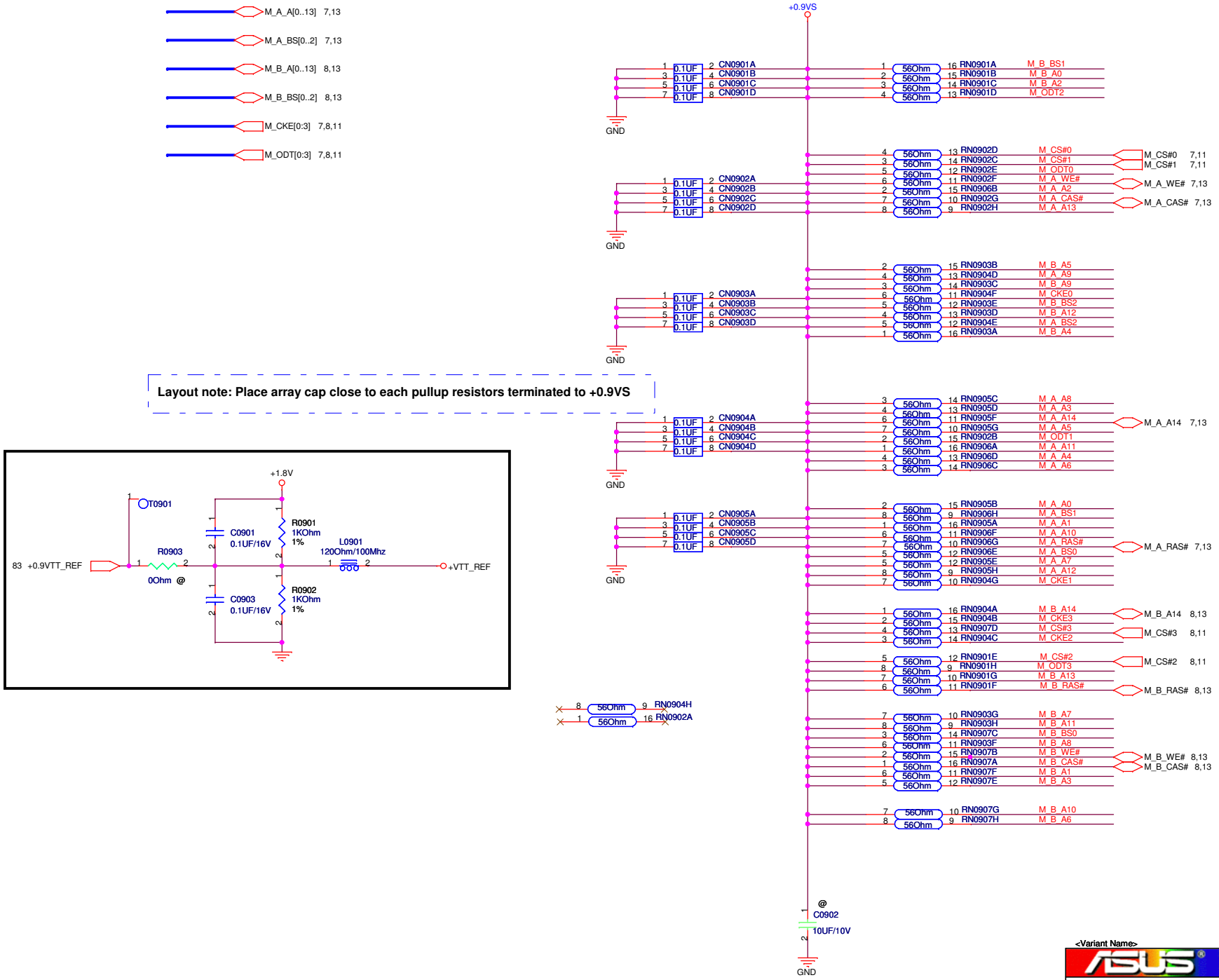


PN : 12G02533200D

REV

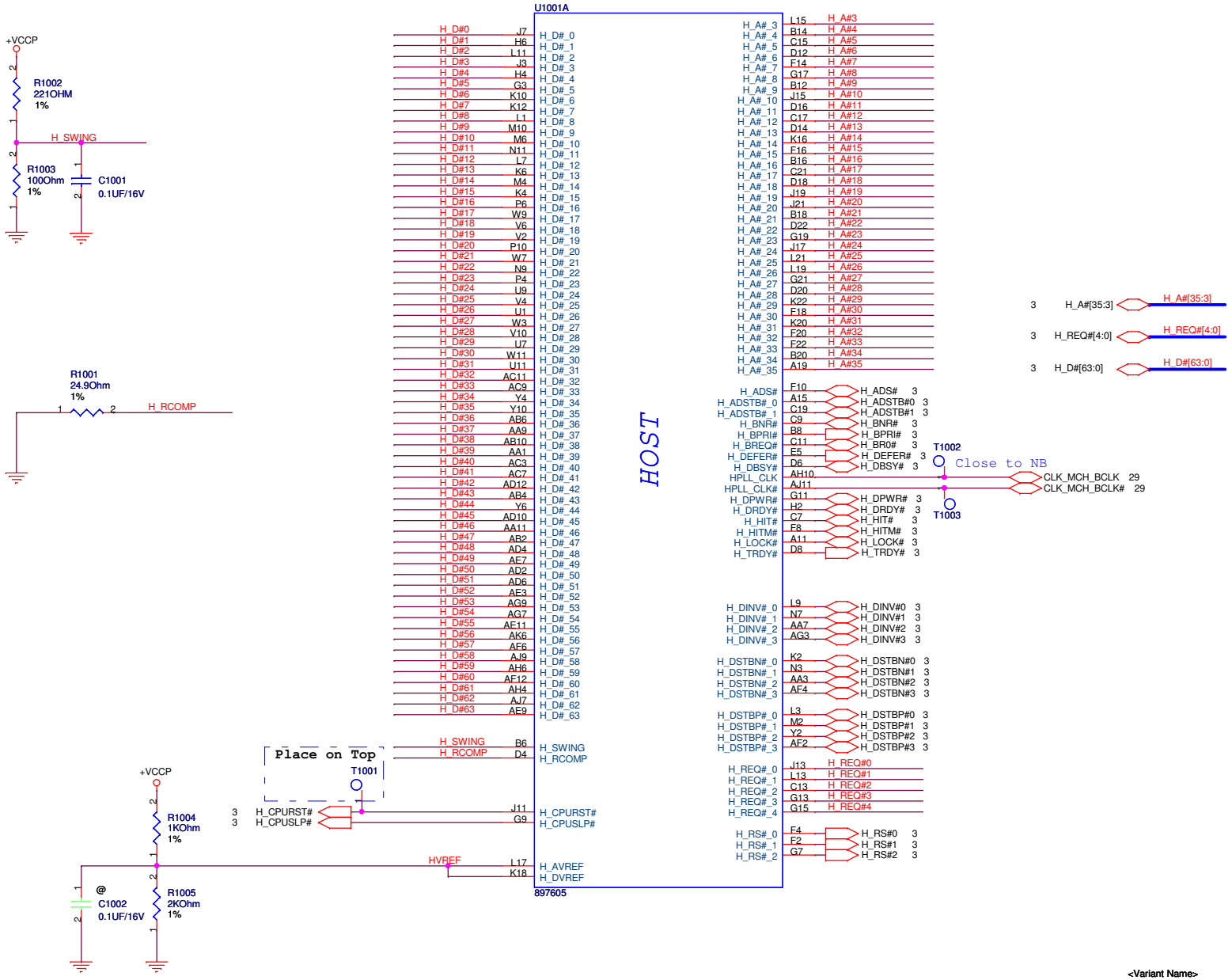
<Variant Name>

ASUSTeK COMPUTER INC	Title : M-DDR3 SO-DIMM CHANNEL B	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 8 of 97	



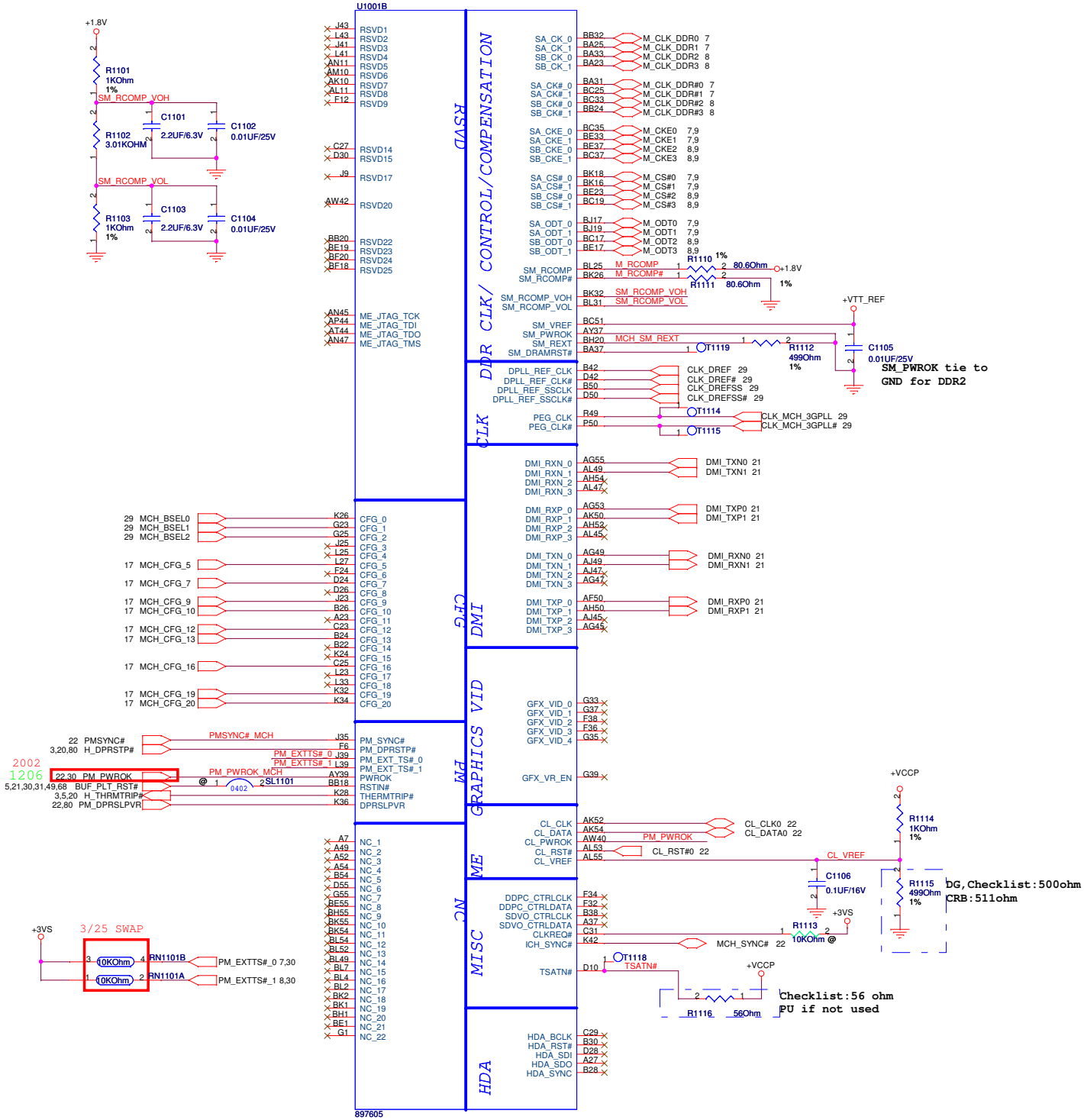
<Variant Name>

ASUSTeK COMPUTER INC	Title : DIM DDR2 VREF	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 9 of 97	



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 HOST	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 10 of 97	



<Variant Name>

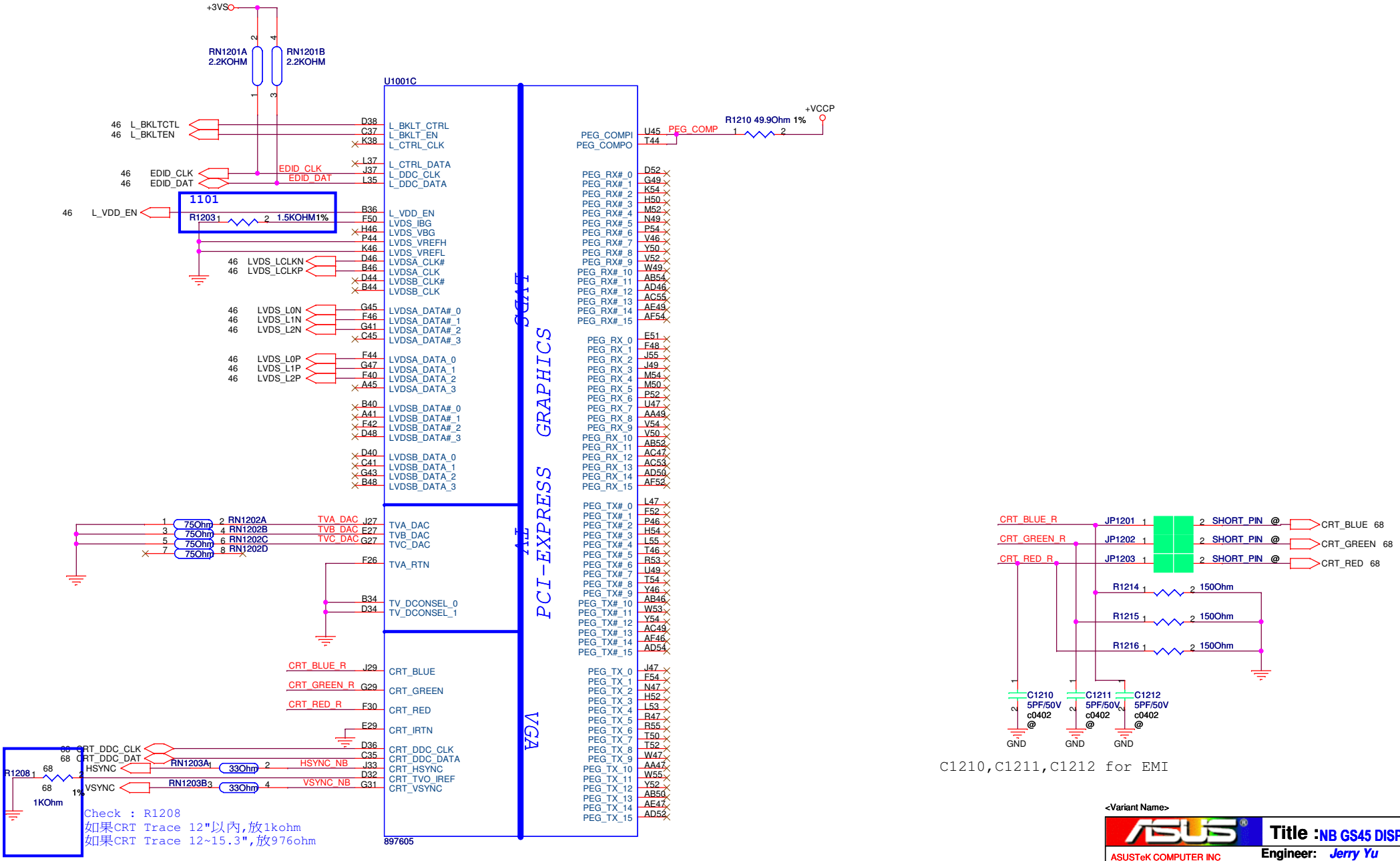
Title : NB GS45 DMI

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0

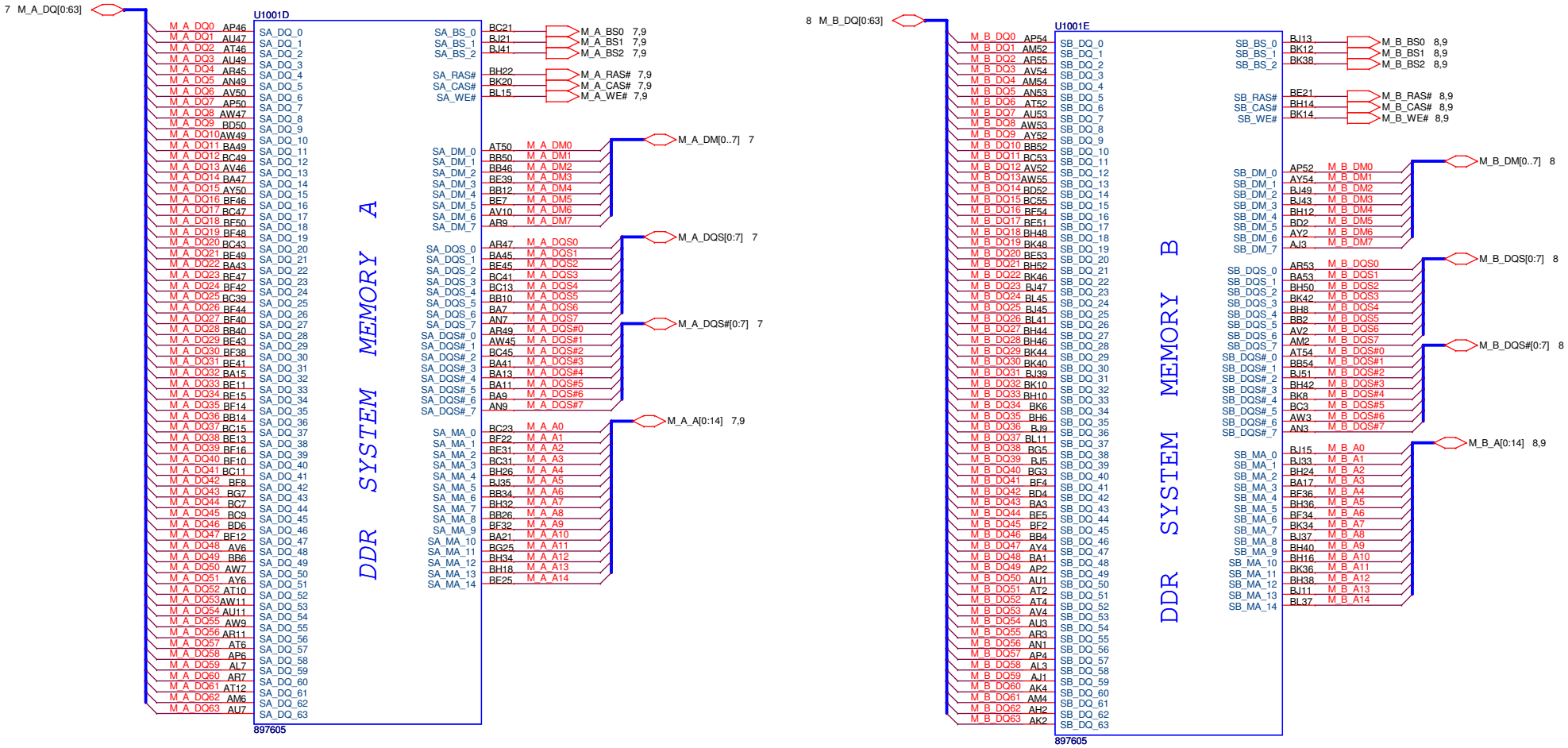
Date: Monday, August 03, 2009 Sheet 11 of 97



C1210,C1211,C1212 for EMI

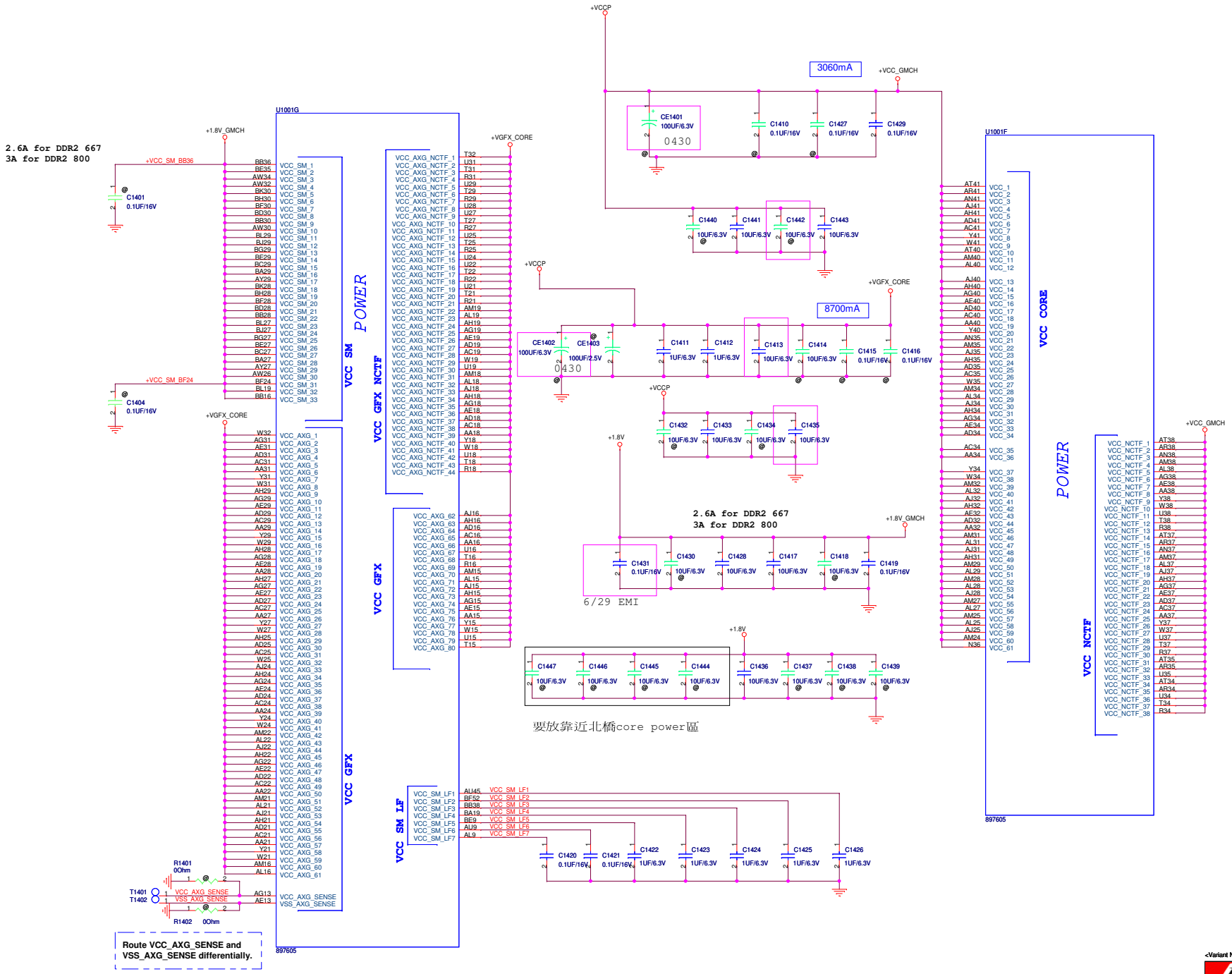
<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 DISPLAY	
	Engineer: Jerry Yu	
Size: B	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 12 of 97	



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 DDR3 BUS	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 13 of 97	



<Variant Name>

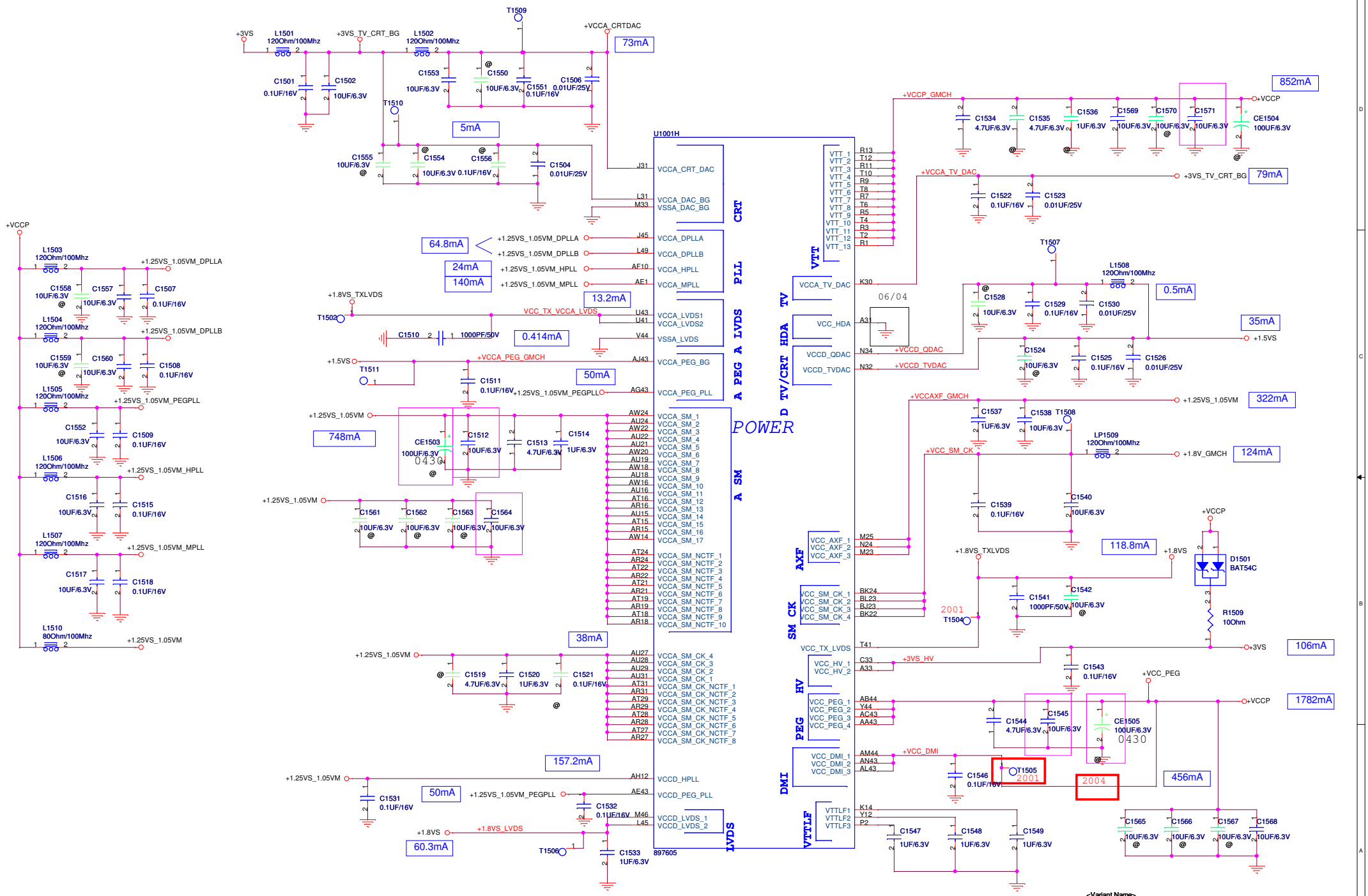
ASUSTeK COMPUTER INC

Title : NB GS45 POWER

Engineer: Jerry Yu

Size	Project Name	Rev
C	UL20A	2.0

Date: Wednesday, July 29, 2009 Sheet 14 of 97



<Variant Name>

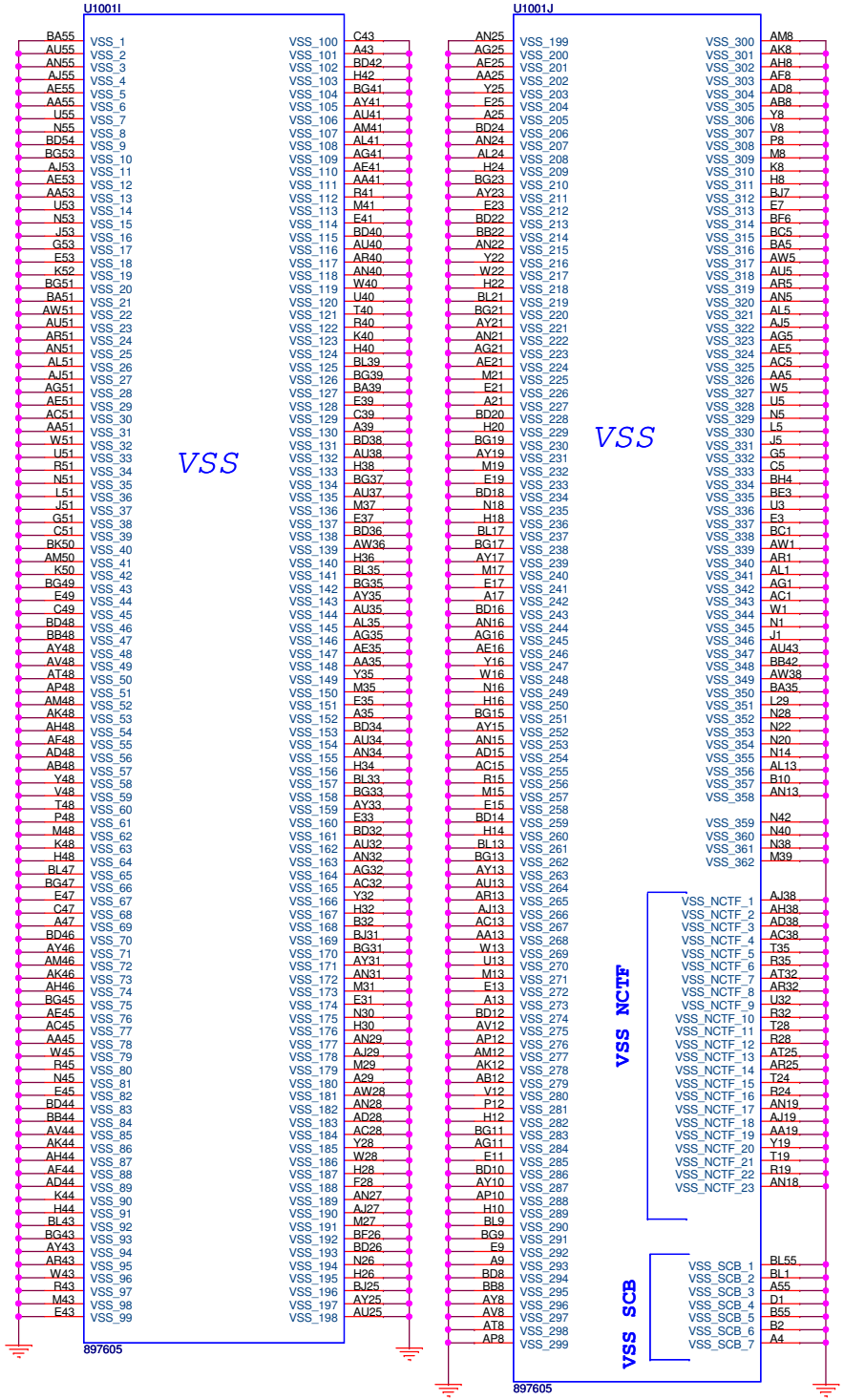
ASUSTeK COMPUTER INC

Title : NB GS45 POWER

Engineer: Jerry Yu

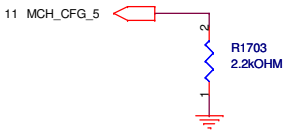
Size	Project Name	Rev
Custom	UL20A	2.0

Date: Wednesday, July 29, 2009 Sheet 15 of 97



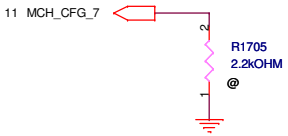
<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 GND	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 16 of 97	

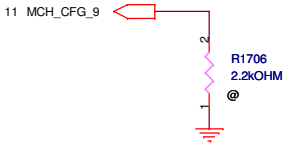


CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

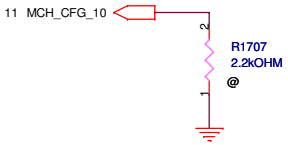
CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)



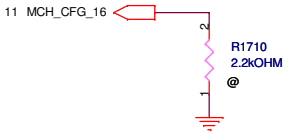
CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality



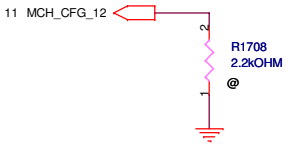
CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse



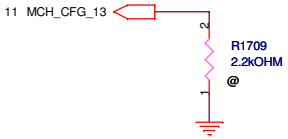
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable



CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

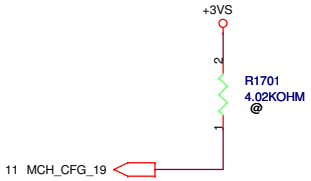


CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

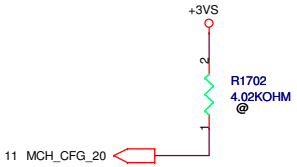


CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: C	Project Name: UL20A	Rev: 2.0
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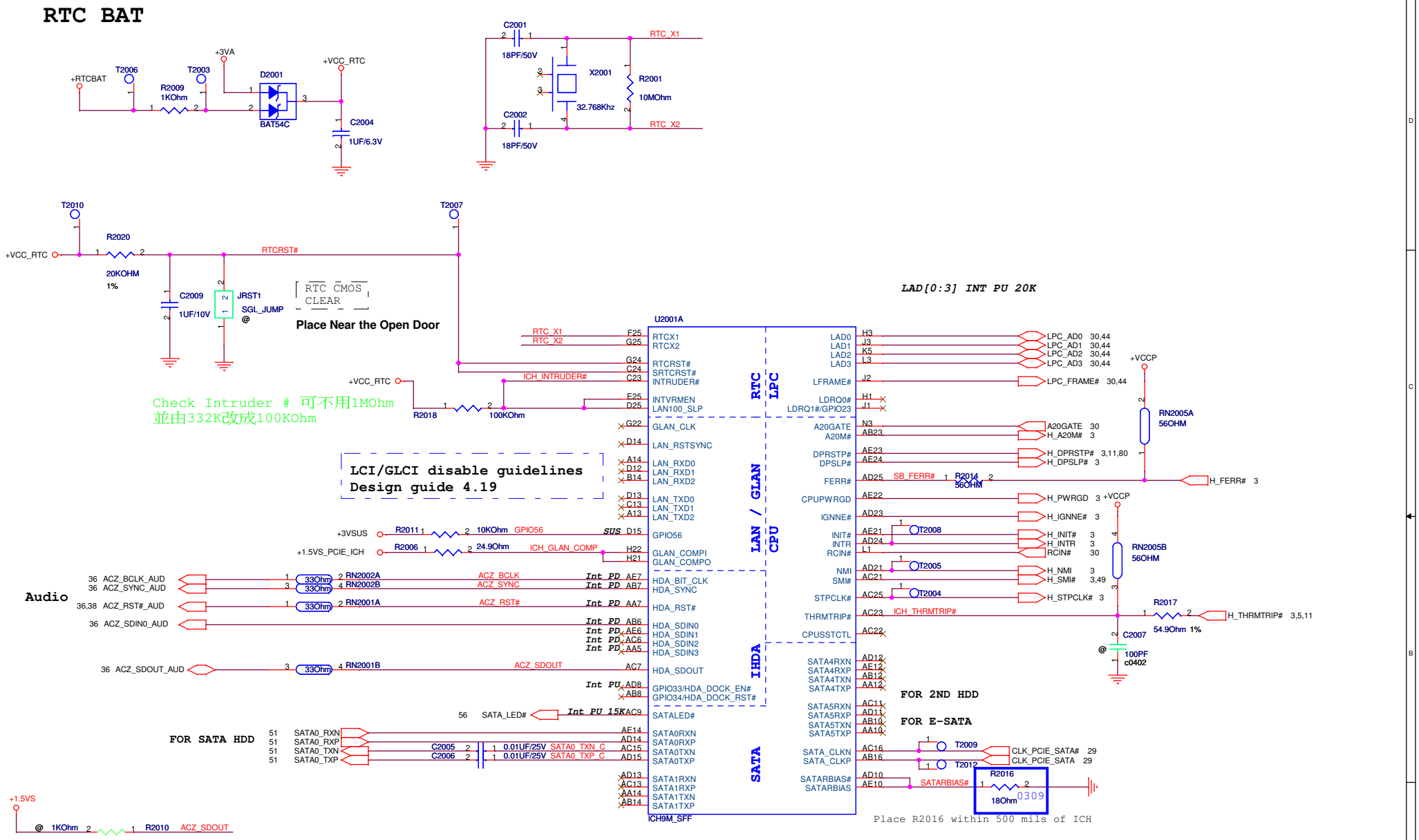
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 19 of 97	

RTC BAT



[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1

GPIO33:Flash Descriptor Security Override

High = Enable (Default)
Low = Overridden

<Variant Name>

ASUSTeK COMPUTER INC

Title : SB ICH9M PCI PCIE DMI USB

Engineer: *Jerry Yu*

Size	Project Name	Rev
Custom	UL20A	2.0

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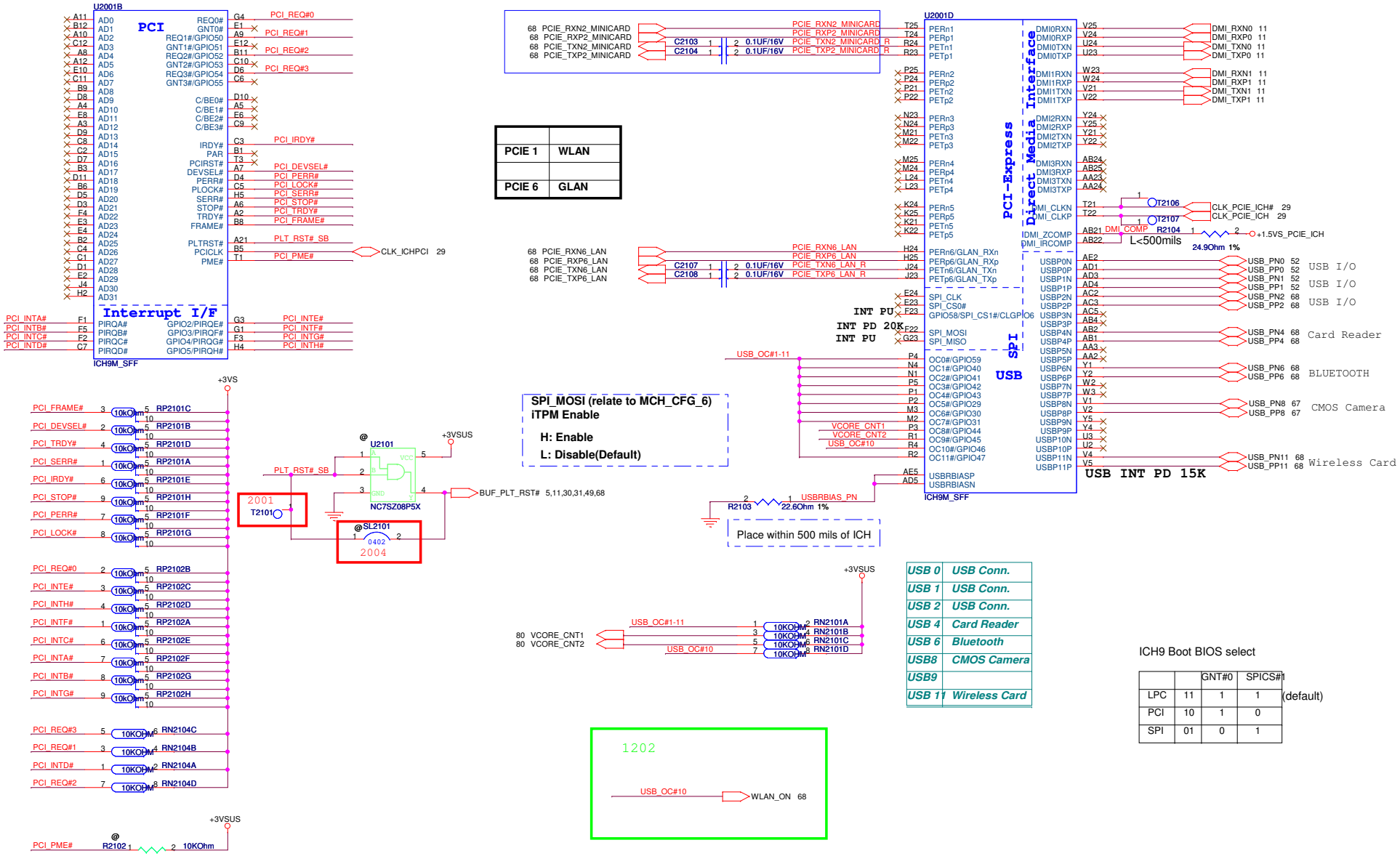
U2001B
PCI
Interrupt I/F
ICH9M_SFF
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_IRDY#
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PLT_RST#_SB
PCI_PME#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
CLK_ICHPCI 29
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
68 PCIE_RXN2_MINICARD
68 PCIE_RXP2_MINICARD
68 PCIE_TXN2_MINICARD
68 PCIE_TXP2_MINICARD
C2103 0.1UF/16V
C2104 0.1UF/16V
PCIE_RXN2_MINICARD
PCIE_RXP2_MINICARD
PCIE_TXN2_MINICARD_R
PCIE_TXP2_MINICARD_R
68 PCIE_RXN6_LAN
68 PCIE_RXP6_LAN
68 PCIE_TXN6_LAN
68 PCIE_TXP6_LAN
C2107 0.1UF/16V
C2108 0.1UF/16V
PCIE_RXN6_LAN
PCIE_RXP6_LAN
PCIE_TXN6_LAN_R
PCIE_TXP6_LAN_R
U2001D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M_SFF
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_RXN0 11
DMI_RXP0 11
DMI_TXN0 11
DMI_TXP0 11
DMI_RXN1 11
DMI_RXP1 11
DMI_TXN1 11
DMI_TXP1 11
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
T2106
T2107
CLK_PCIE_ICH# 29
CLK_PCIE_ICH 29
DMI_COMP
R2104
24.9Ohm 1%
+1.5VS_PCIE_ICH
L<500mils
SPI_CLK
SPI_CS0#
GPIO58/SPI_CS1#/CLGPIO6
SPI_MOSI
SPI_MISO
INT PU
INT PD 20K
INT PU
USB_OC#1-11
VCORE_CNT1
VCORE_CNT2
USB_OC#10
USBRBIASP
USBRBIASN
USBRBIAS_PN
R2103
22.6Ohm 1%
USB I/O
USB I/O
Card Reader
BLUETOOTH
CMOS Camera
Wireless Card
USB INT PD 15K
SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable
H: Enable
L: Disable(Default)
Place within 500 mils of ICH
PCIE 1 WLAN
PCIE 6 GLAN
+3VS
RP2101C
RP2101B
RP2101D
RP2101A
RP2101E
RP2101H
RP2101F
RP2101G
RP2102B
RP2102C
RP2102D
RP2102A
RP2102E
RP2102F
RP2102G
RP2102H
RN2104C
RN2104B
RN2104A
RN2104D
10KOhm
U2101
NC7SZ08P5X
+3VSUS
BUF_PLT_RST# 5,11,30,31,49,68
2001
T2101
SL2101
0402
2004
R2102
10KOhm
80 VCORE_CNT1
80 VCORE_CNT2
RN2101A
RN2101B
RN2101C
RN2101D
1202
USB_OC#10
WLAN_ON 68
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 4 Card Reader
USB 6 Bluetooth
USB8 CMOS Camera
USB9
USB 11 Wireless Card
ICH9 Boot BIOS select
GNT#0
SPICS#1
LPC 11 1 1 (default)
PCI 10 1 0
SPI 01 0 1
<Variant Name>
SB ICH9M PCI PCIE DMI USB
Title :
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size Custom
Project Name UL20A
Rev 2.0
Date: Monday, August 03, 2009
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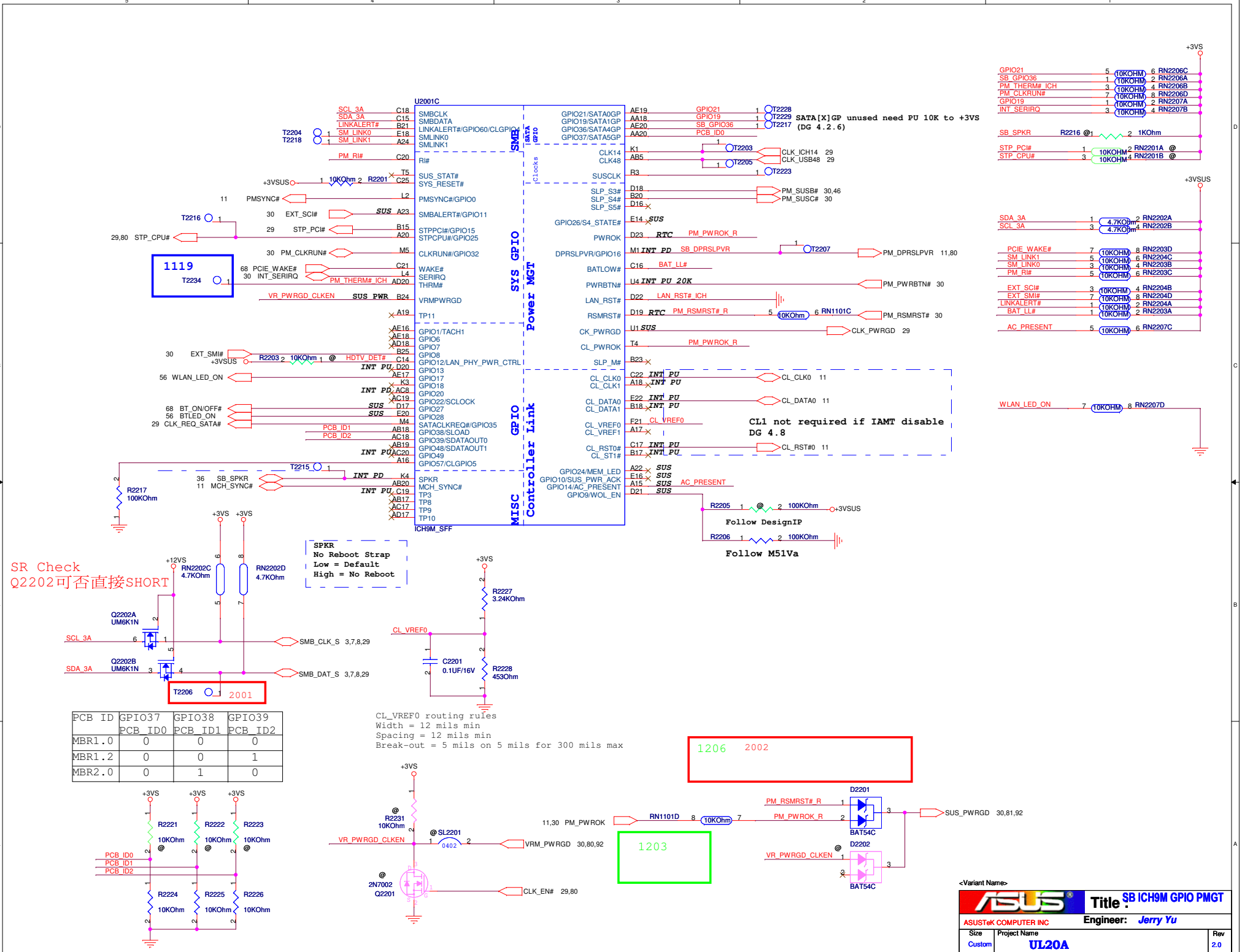
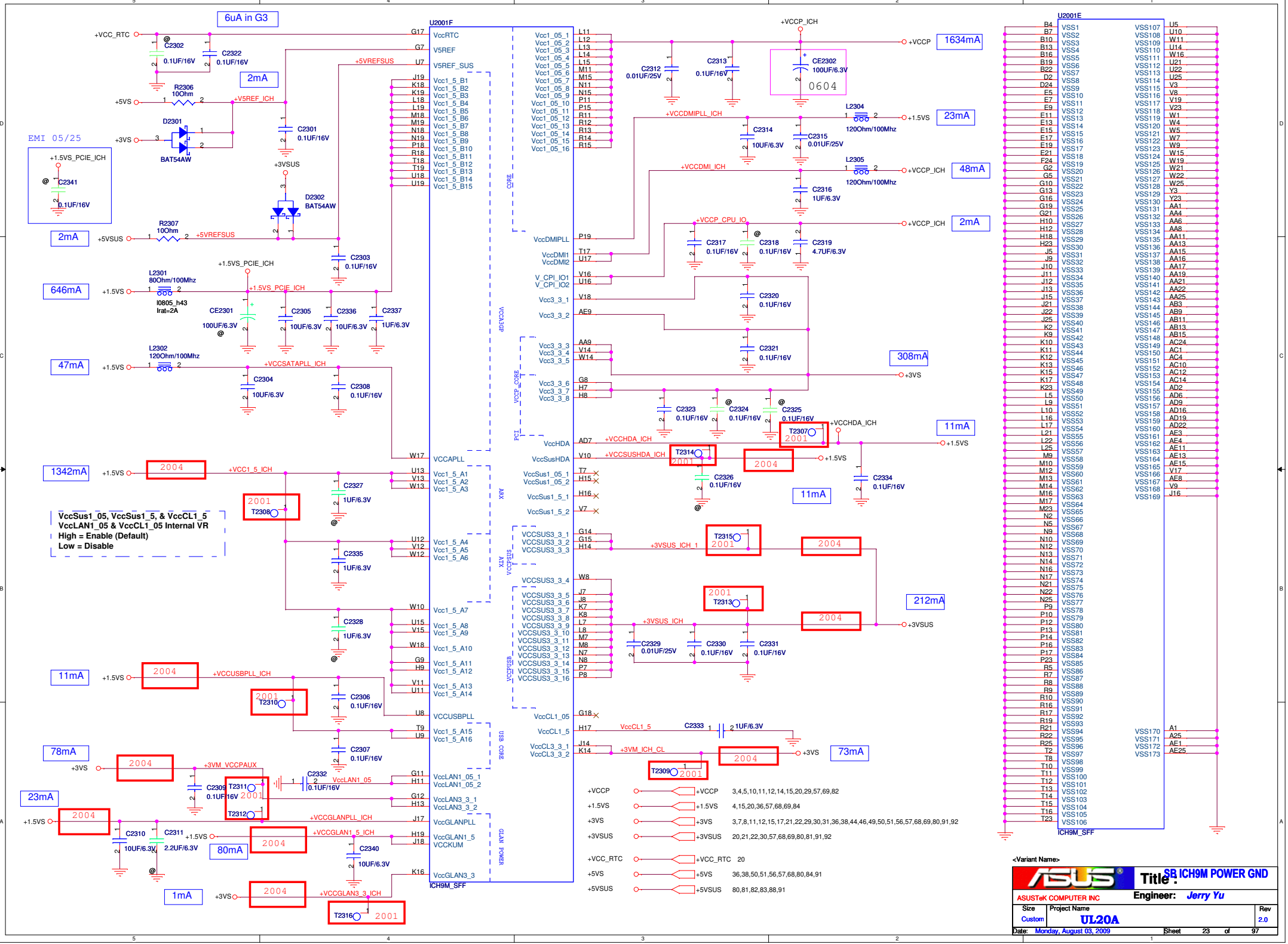


PCB ID	GPIO37 PCB_ID0	GPIO38 PCB_ID1	GPIO39 PCB_ID2
MBR1.0	0	0	0
MBR1.2	0	0	1
MBR2.0	0	1	0


6uA in G3
U2001F
ICH9M_SFF
U2001E
ICH9M_SFF
EMI 05/25
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
+VCCP 3,4,5,10,11,12,14,15,20,29,57,69,82
+1.5VS 4,15,20,36,57,68,69,84
+3VS 3,7,8,11,12,15,17,21,22,29,30,31,36,38,44,46,49,50,51,56,57,68,69,80,91,92
+3VSUS 20,21,22,30,57,68,69,80,81,91,92
+VCC_RTC 20
+5VS 36,38,50,51,56,57,68,80,84,91
+5VSUS 80,81,82,83,88,91
<Variant Name>
Title : SB ICH9M POWER GND
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size Custom
Project Name UL20A
Rev 2.0
Date: Monday, August 03, 2009
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<Variant Name>

Title : SB ICH9M SPI ROM & HDCP

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0

Date: Wednesday, July 29, 2009 Sheet 24 of 97

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 25 of 97	

<Variant Name>

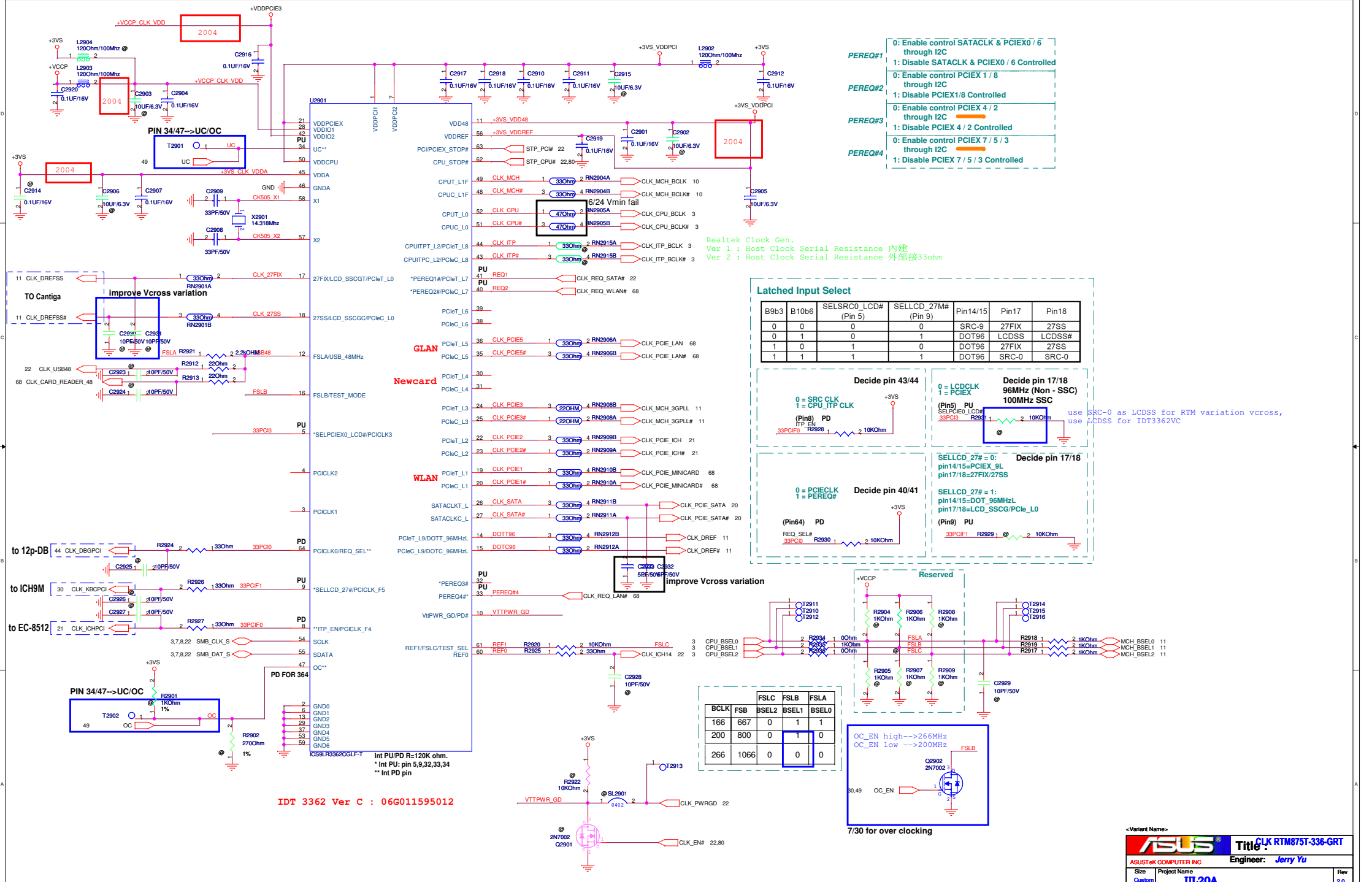
ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 26 of 97	

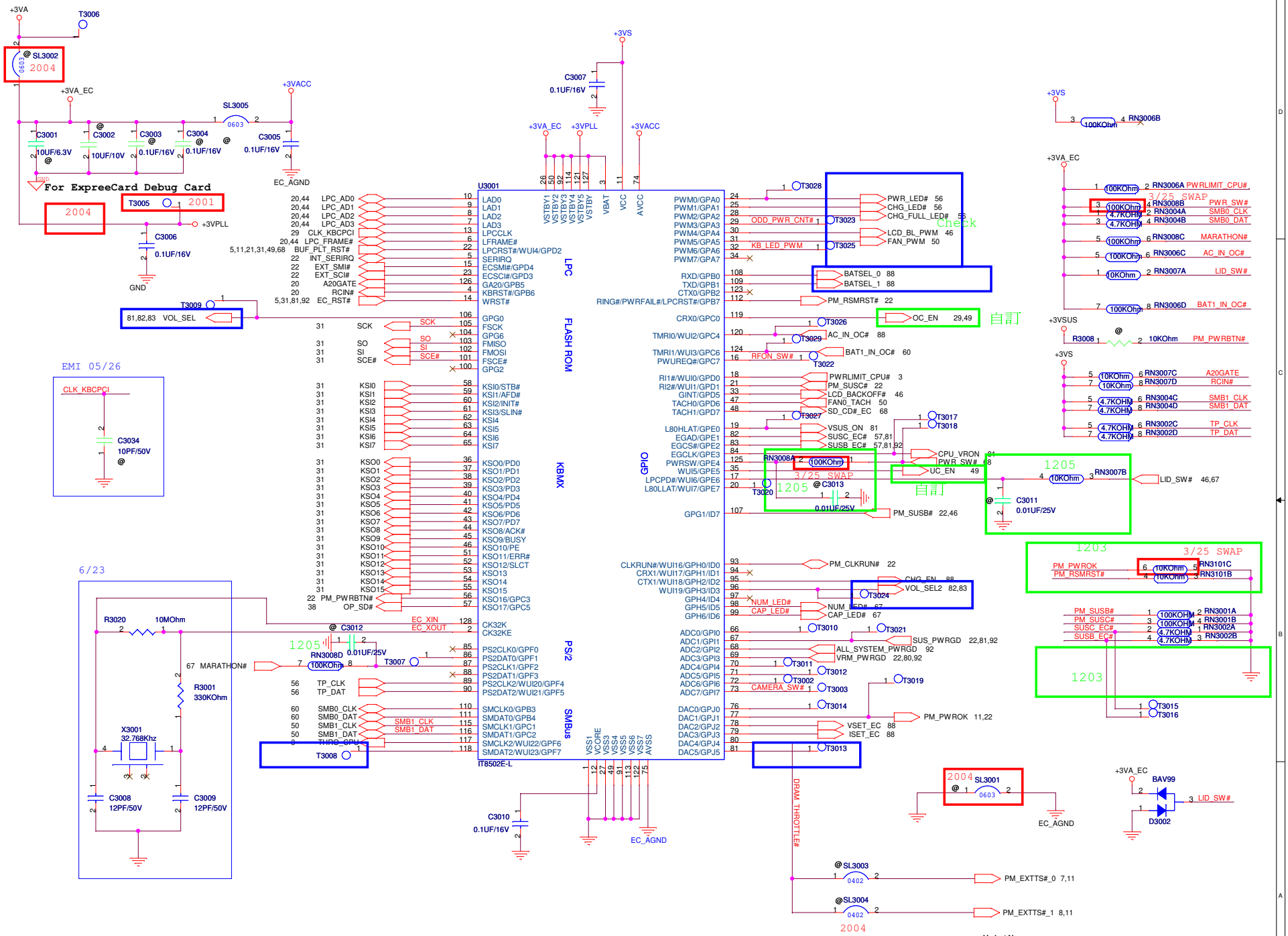
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 27 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 28 of 97	


PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled
PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled
PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled
PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled
PIN 34/47-->UC/OC
6/24 Vmin fail
Realtek Clock Gen.
Ver 1 : Host Clock Serial Resistance 內建
Ver 2 : Host Clock Serial Resistance 外部接33ohm
TO Cantiga
improve Vcross variation
GLAN
Newcard
WLAN
to 12p-DB
to ICH9M
to EC-8512
PD FOR 364
Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin
IDT 3362 Ver C : 06G011595012
Latched Input Select
Decide pin 43/44
Decide pin 17/18
96MHz (Non - SSC)
100MHz SSC
use SRC-0 as LCDSS for RTM variation vcross,
use LCDSS for IDT3362VC
Decide pin 40/41
Decide pin 17/18
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
Reserved
improve Vcross variation
OC_EN high-->266MHz
OC_EN low -->200MHz
7/30 for over clocking
Title : CLK RTM875T-336-GRT
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Project Name UL20A
Date: Monday, August 03, 2009
Sheet 29 of 97


U3001
IT8502E-L
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
For ExpreeCard Debug Card
EMI 05/26
6/23
3/25 SWAP
1205
1203
自訂
Check
DRAM_THROTTLE#
Title : KBC ITE8512
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size Custom
Project Name UL20A
Rev 2.0
Date: Monday, August 03, 2009
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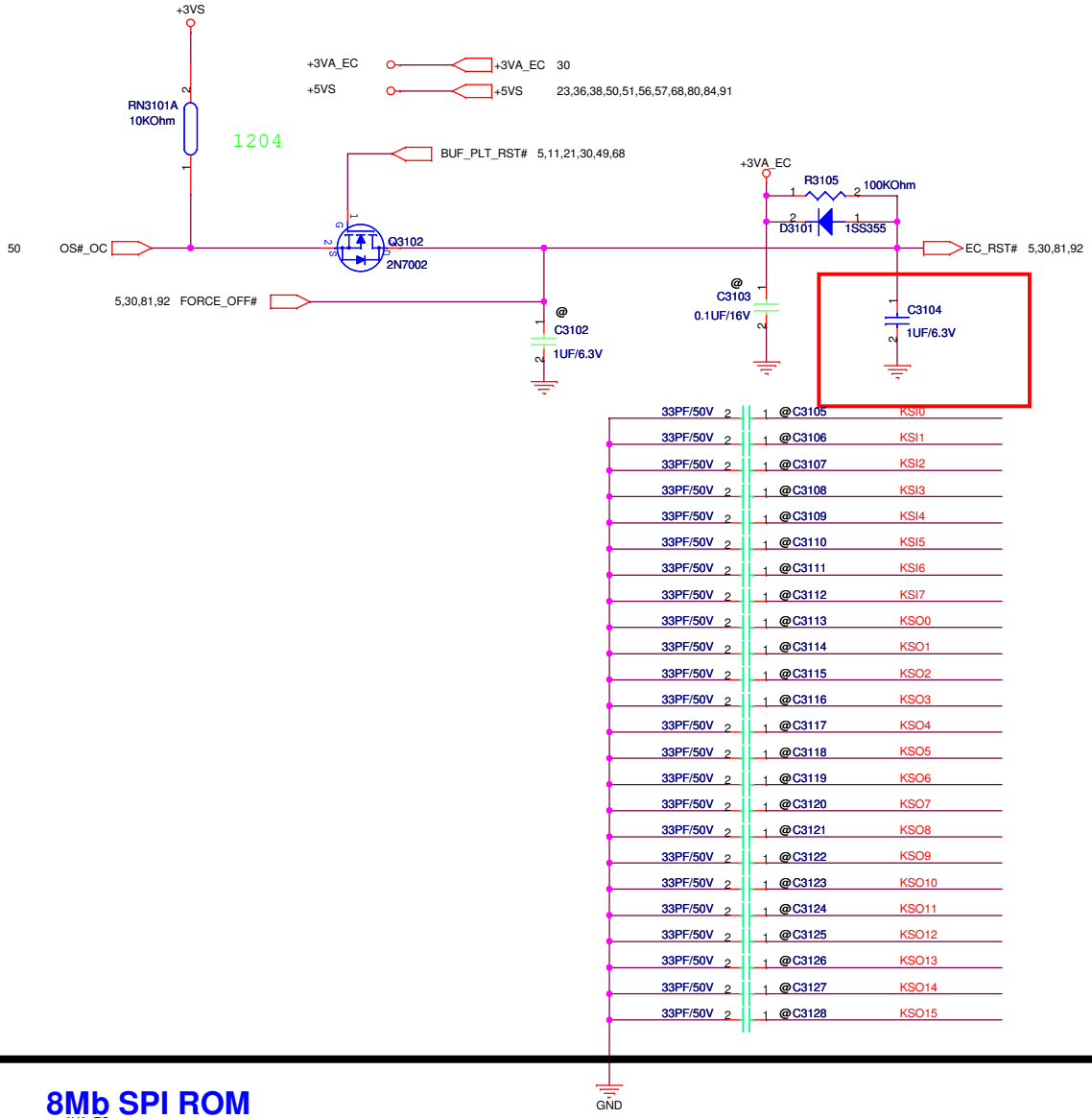
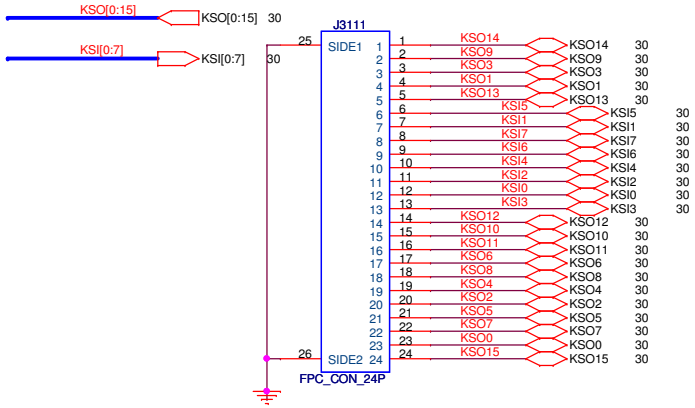
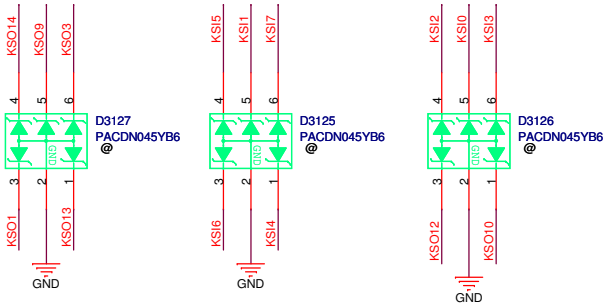
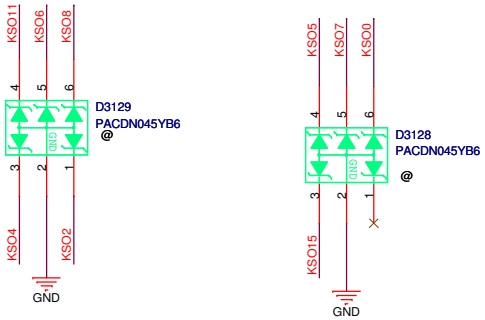
Internal Keyboard

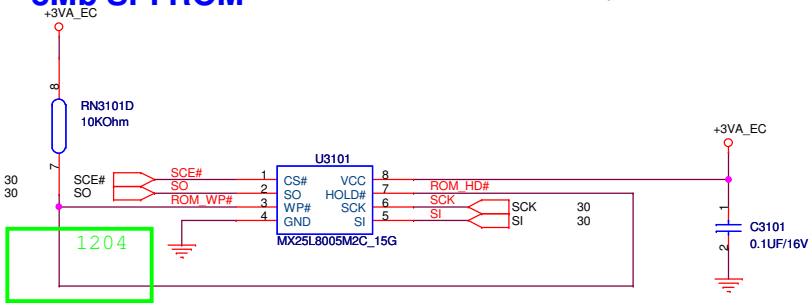








8Mb SPI ROM



<Variant Name> ROM FLASH ROM TOUCH PAD KB

ASUSTeK COMPUTER INC	Title :		
	Engineer: Jerry Yu		
Size: Custom	Project Name: UL20A		Rev: 2.0
Date: Monday, August 03, 2009	Sheet 31 of 97		

Parade PS8101T: Optional /PS
Stuff: R3216 R3219 R3201 R3215
No stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202 R3210 R3208 R3209 R3206 Q3201.

PERICOM PI3VDP411LSZDE: Optional /PI
No stuff: R3216 R3219 R3201 R3215
Stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202 R3210 R3208 R3209 R3206 Q3201.

<Variant Name>

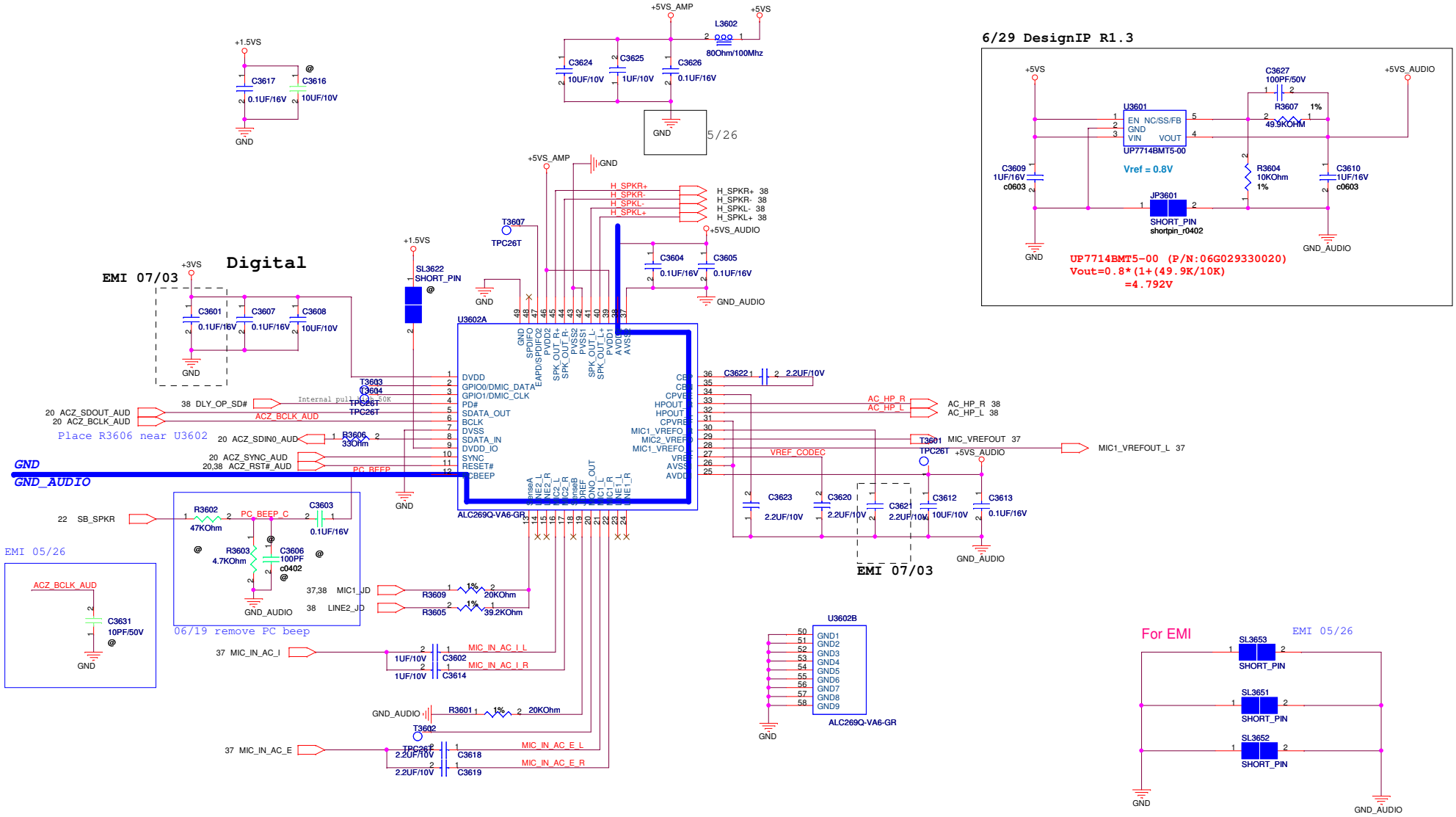
ASUS	Title : AR8131 LAN	
ASUSTeK COMPUTER INC	Engineer: Jerry Yu	
Size: B	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 33 of 97	

<Variant Name>

ASUS	Title : LAN RJ45 CONN	
ASUSTeK COMPUTER INC	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 34 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 35 of 97	



<Variant Name>

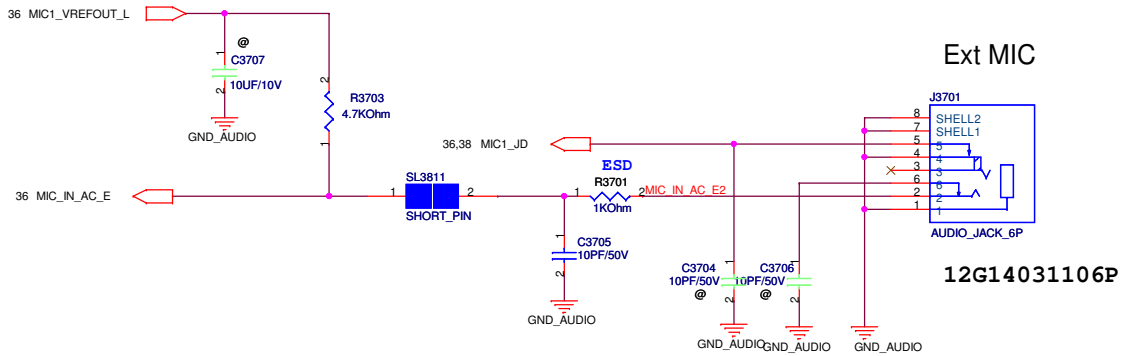
ASUSTeK COMPUTER INC

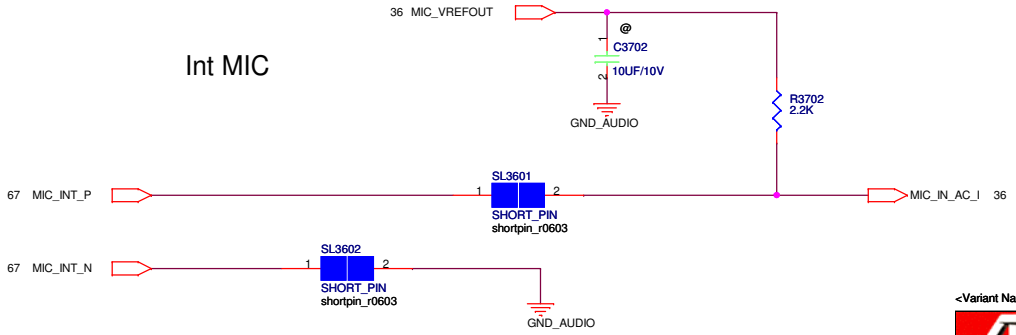
Title : AUD ALC269

Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0

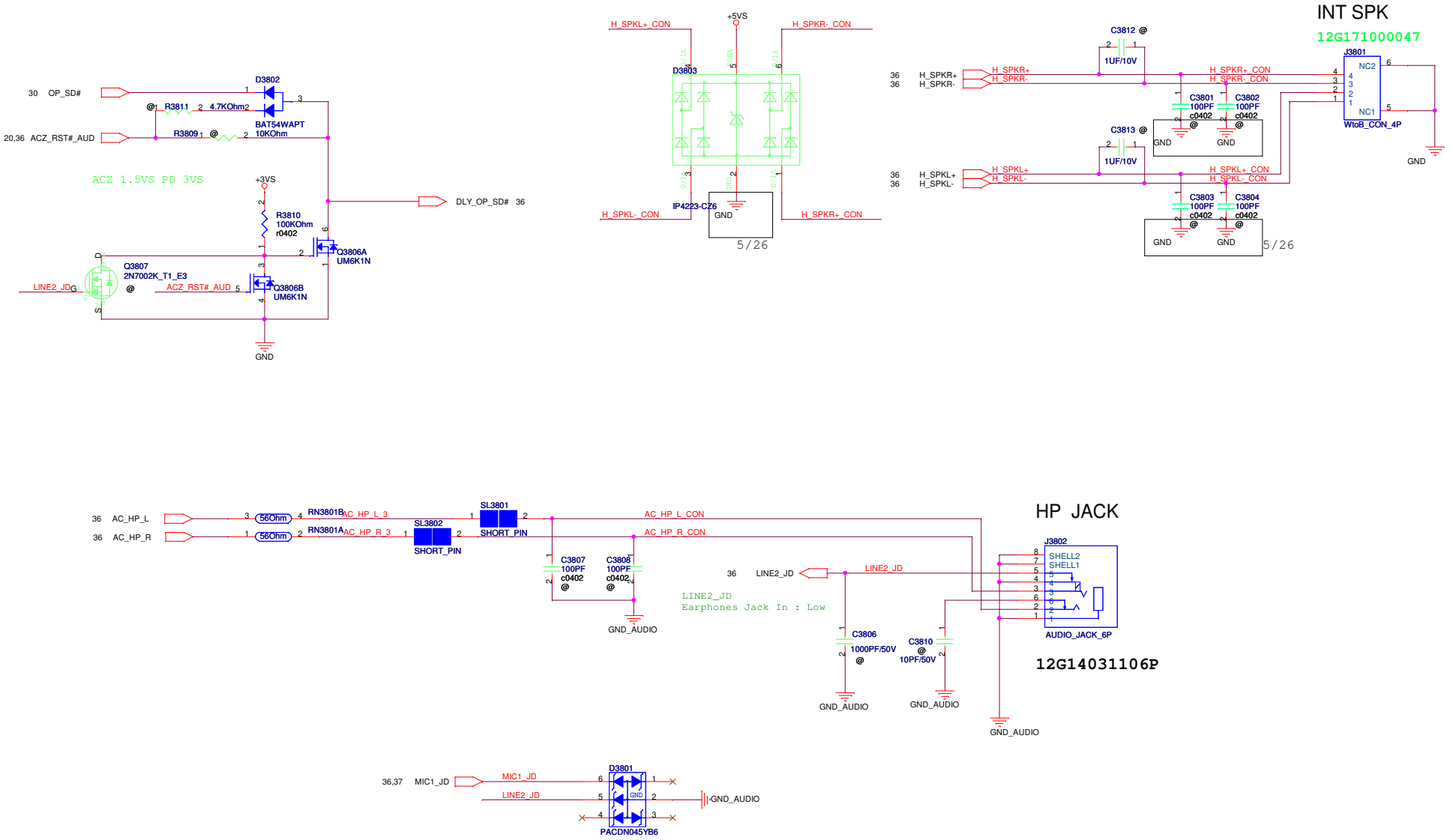
Date: Monday, August 03, 2009 Sheet 36 of 97





<Variant Name>

ASUSTeK COMPUTER INC	Title : AUD MIC CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 37 of 97	



<Variant Name>

ASUSTeK COMPUTER INC	Title : AUD HP&SPK CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 38 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 39 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 40 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 41 of 97	

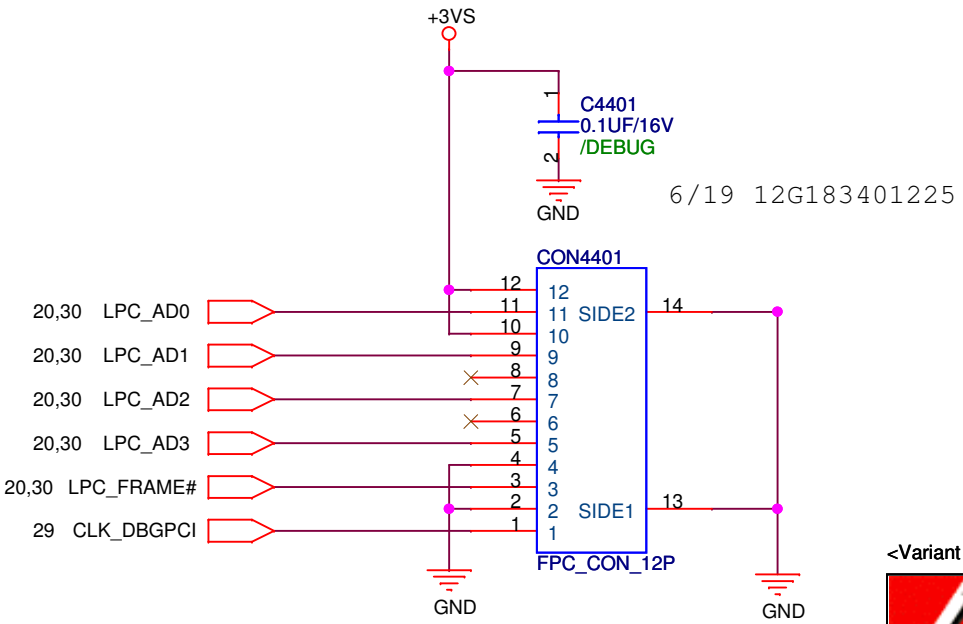
<Variant Name>

ASUSTeK COMPUTER INC	Title : CARD READER AU6371	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 42 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : CR EXPRESS CARD CONN	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 43 of 97	

LPC DEBUG PORT



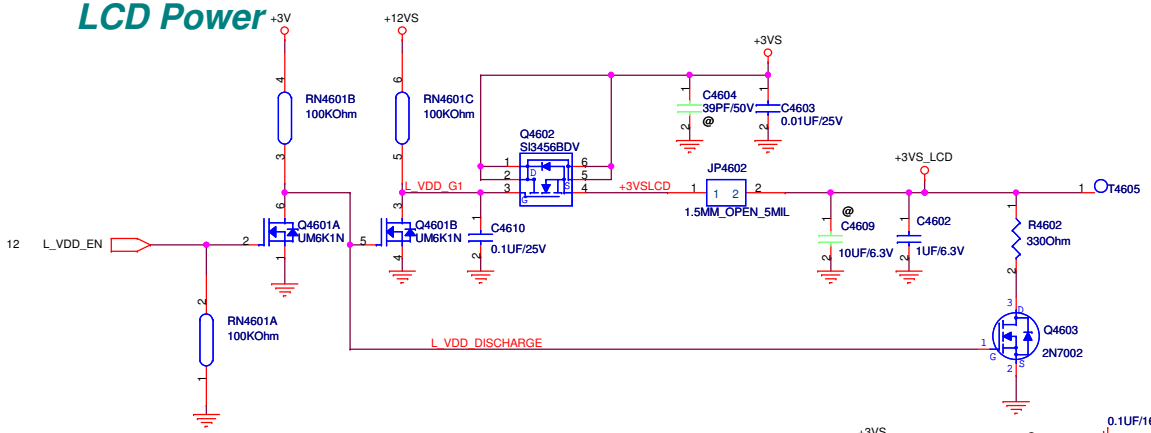
<Variant Name>

ASUSTeK COMPUTER INC	Title : BUG DEBUG PORT	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 44 of 97	

<Variant Name>

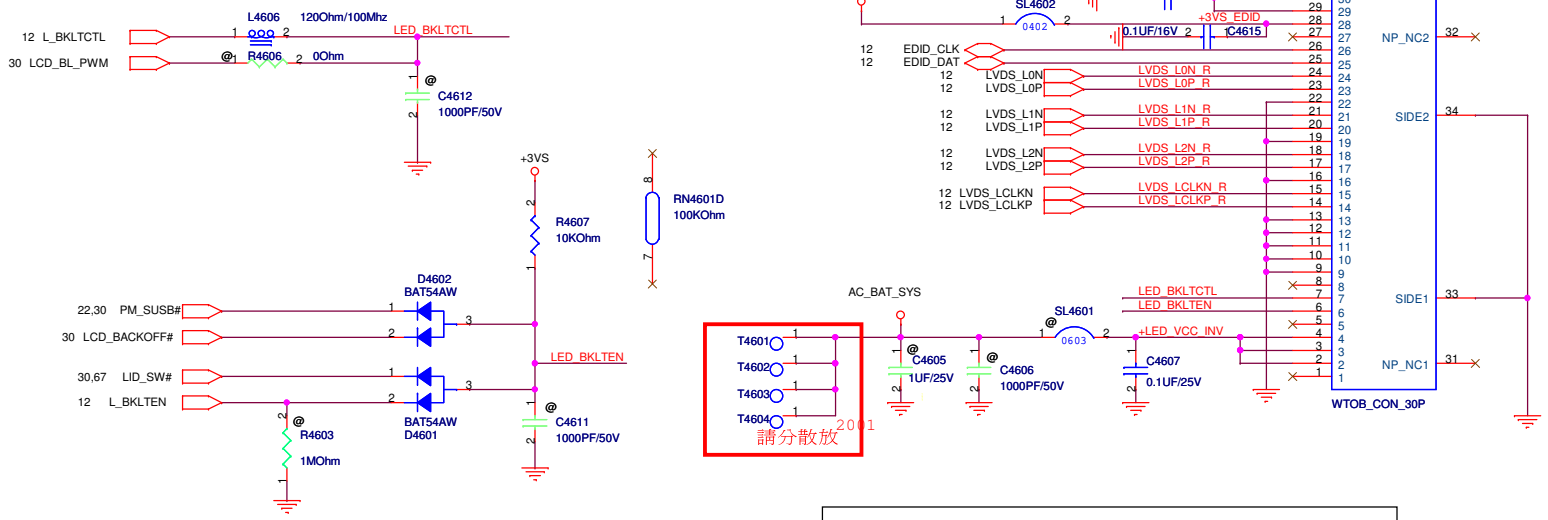
ASUSTeK COMPUTER INC	Title : HDMI CONN	
	Engineer: Jerry Yu	
Size: C	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 45 of 97	

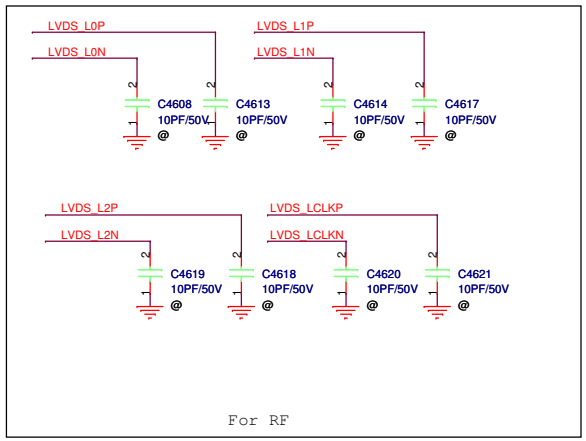
LCD Power



LVDS CONN

12G171040309 5/19





<Variant Name>

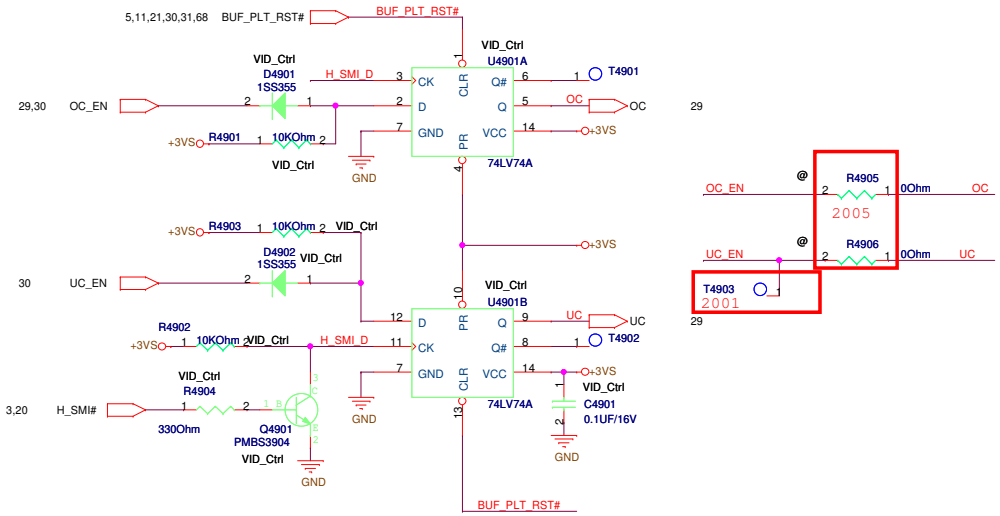
ASUSTeK COMPUTER INC	Title : LVDS CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 46 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT D-SUB CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 47 of 97	

<Variant Name>

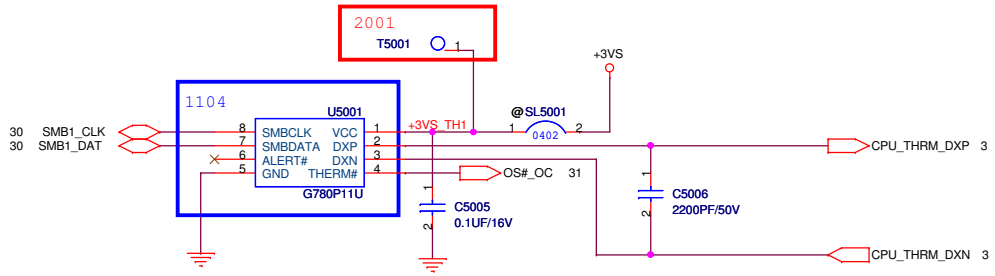
ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 48 of 97	



<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT D-SUB CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 49 of 97	

Thermal Seneor



U5001 Close to CPU

SMBus Address: G780 98H

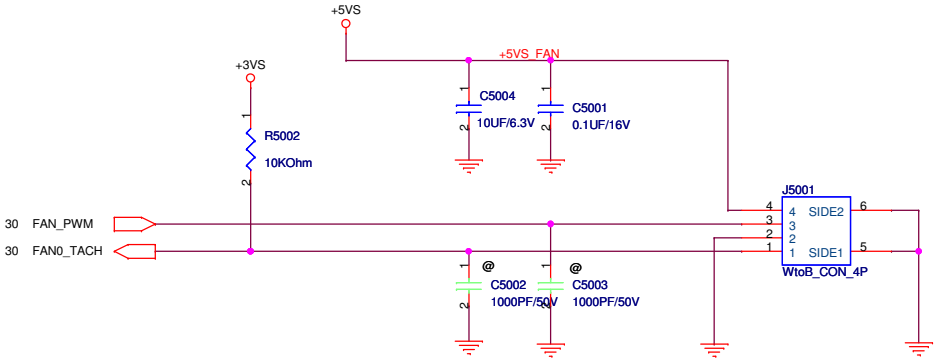
+3VS	+3VS	3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,51,56,57,68,69,80,91,92
+VCORE	+VCORE	4,5,69,80
+5VS	+5VS	23,36,38,51,56,57,68,80,84,91

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

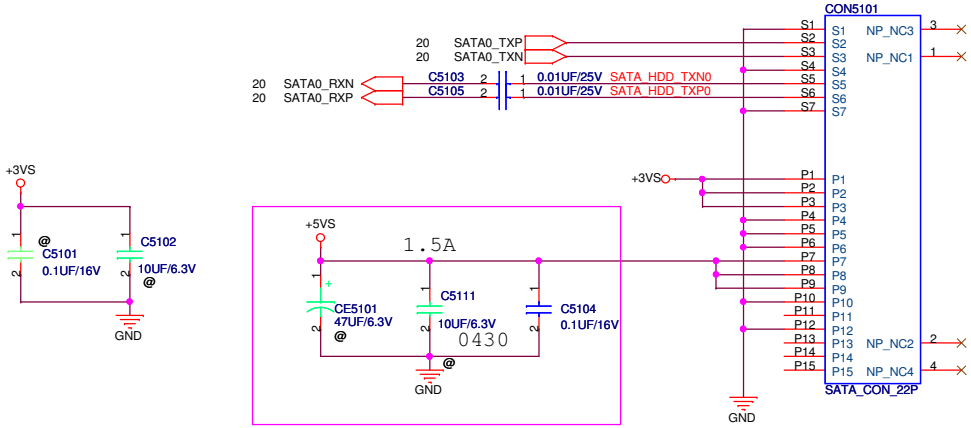
FAN CONN



<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN THERMAL SENSOR FAN CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 50 of 97	

SATA HDD

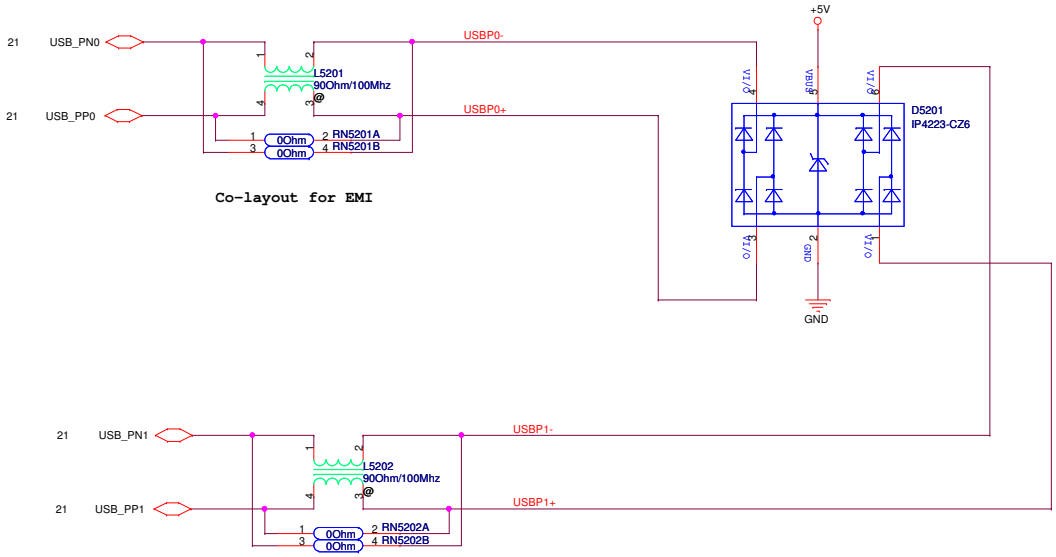


<Variant Name>

ASUSTeK COMPUTER INC	Title : XDD SATA HDD CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 51 of 97	

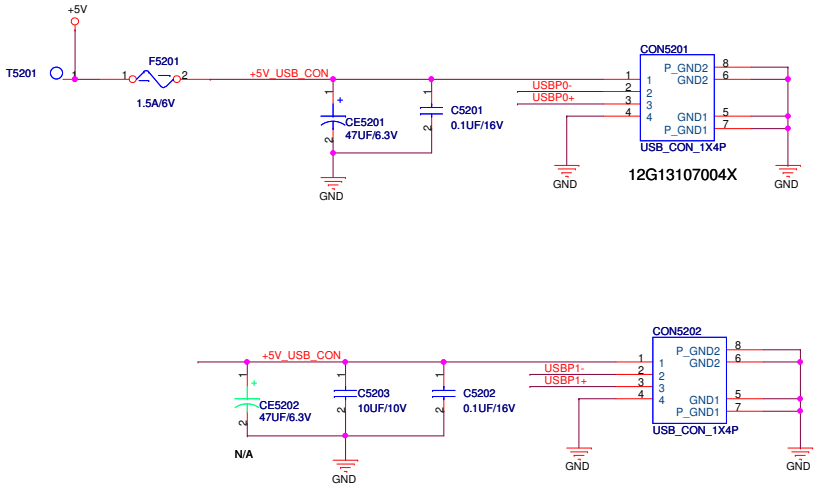
USB CONN *2

USB : MB



Co-layout for EMI

Co-layout for EMI



<Variant Name>

ASUSTeK COMPUTER INC	Title : USB 2.0 CONN*2	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 52 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : PCI MINICARD CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 53 of 97	

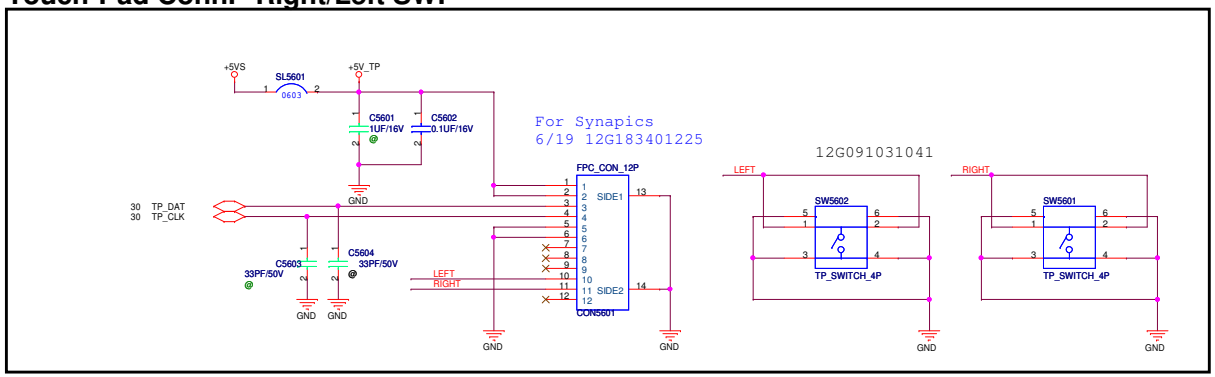
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 54 of 97	

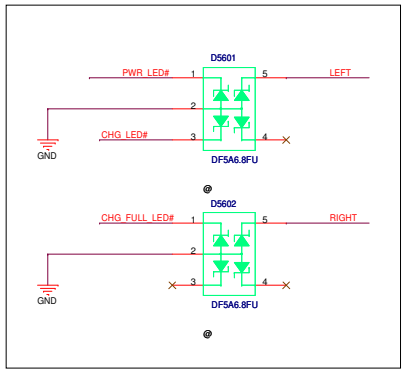
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 55 of 97	

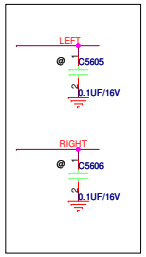
Touch-Pad Conn. Right/Left SW.



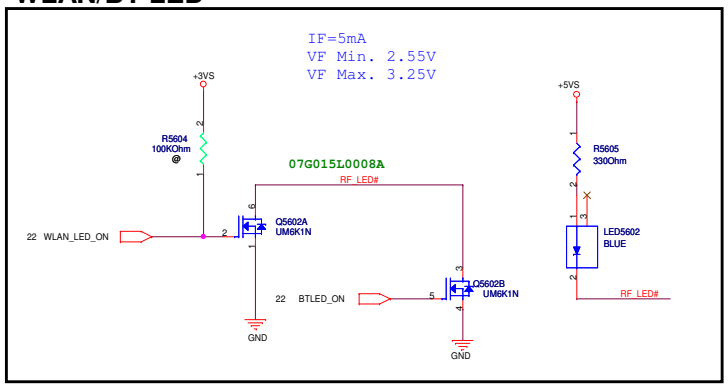
6/22 for ESD



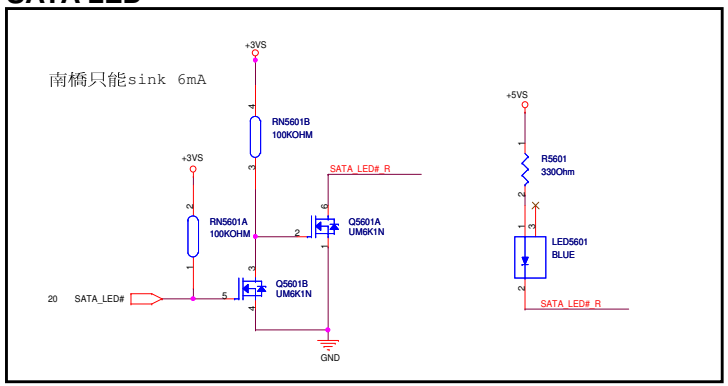
6/30 EMI near BTN



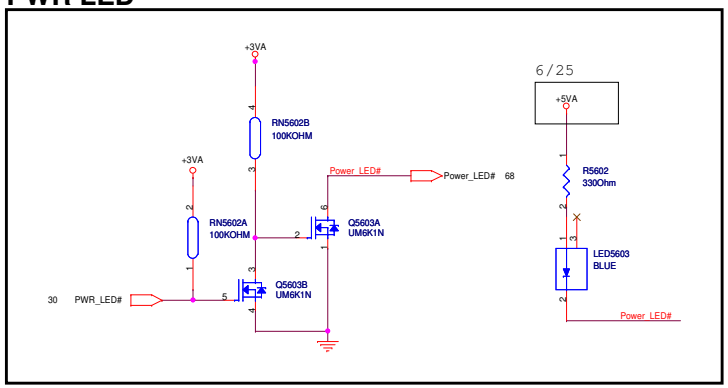
WLAN/BT LED



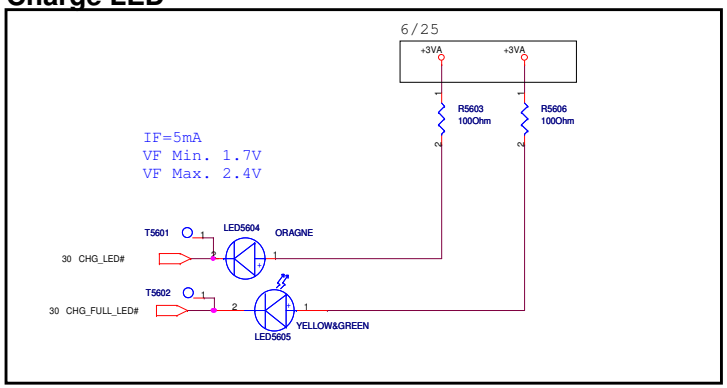
SATA LED



PWR LED

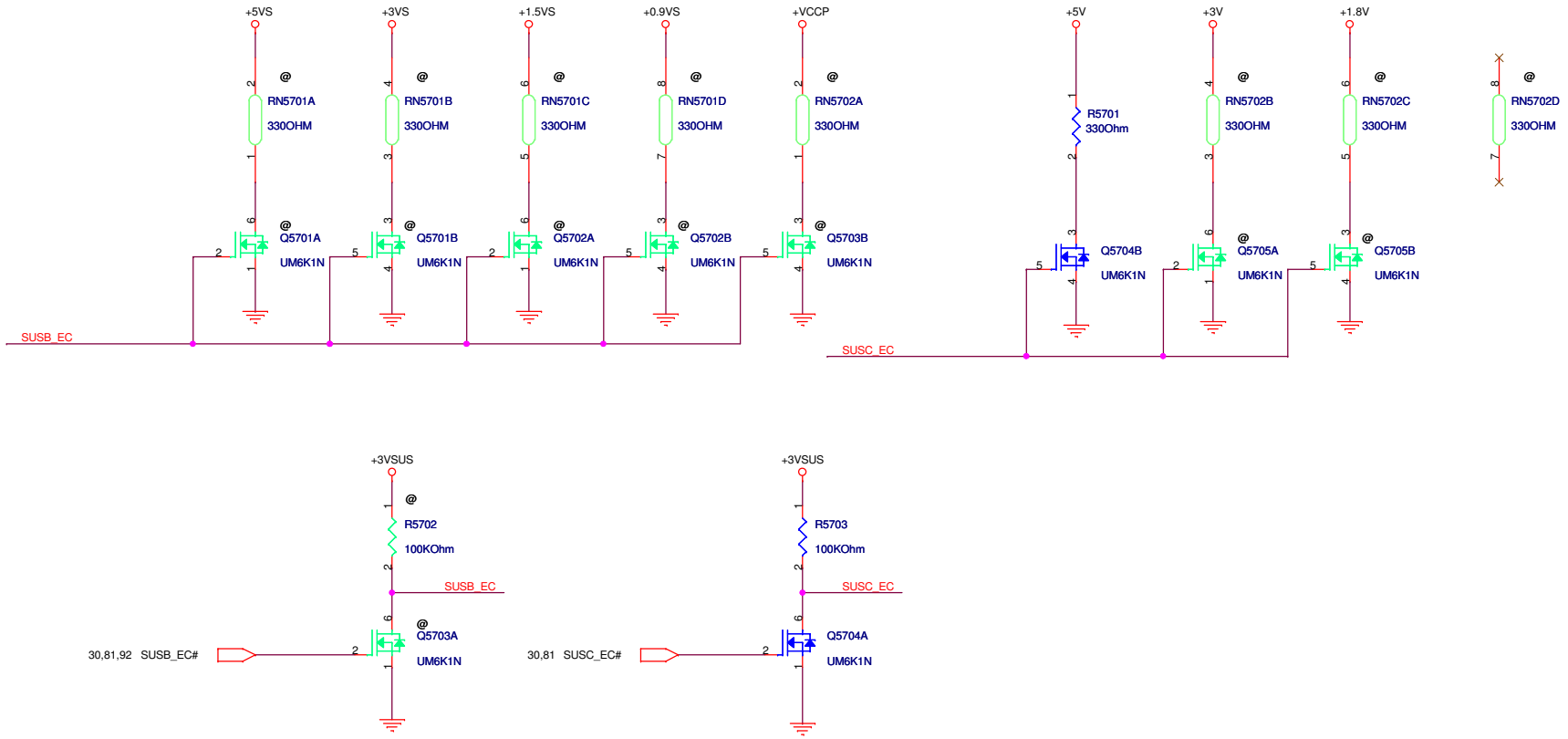


Charge LED



Discharge Circuit

+5VS	+5VS	23,36,38,50,51,56,68,80,84,91
+3VS	+3VS	3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,68,69,80,91,92
+1.5VS	+1.5VS	4,15,20,23,36,68,69,84
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,69,82
+5V	+5V	52,67,68,91
+3V	+3V	46,68,91
+1.8V	+1.8V	7,8,9,11,14,15,83,84,91
+0.9VS	+0.9VS	9,83
+3VSUS	+3VSUS	20,21,22,23,30,68,69,80,81,91,92



<Variant Name>

DSG DISCHARHE CIRCUIT

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0

Date: Monday, August 03, 2009 Sheet 57 of 97

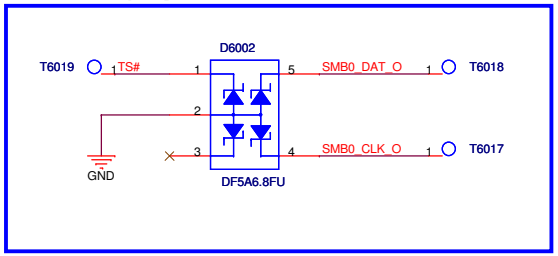
<Variant Name>

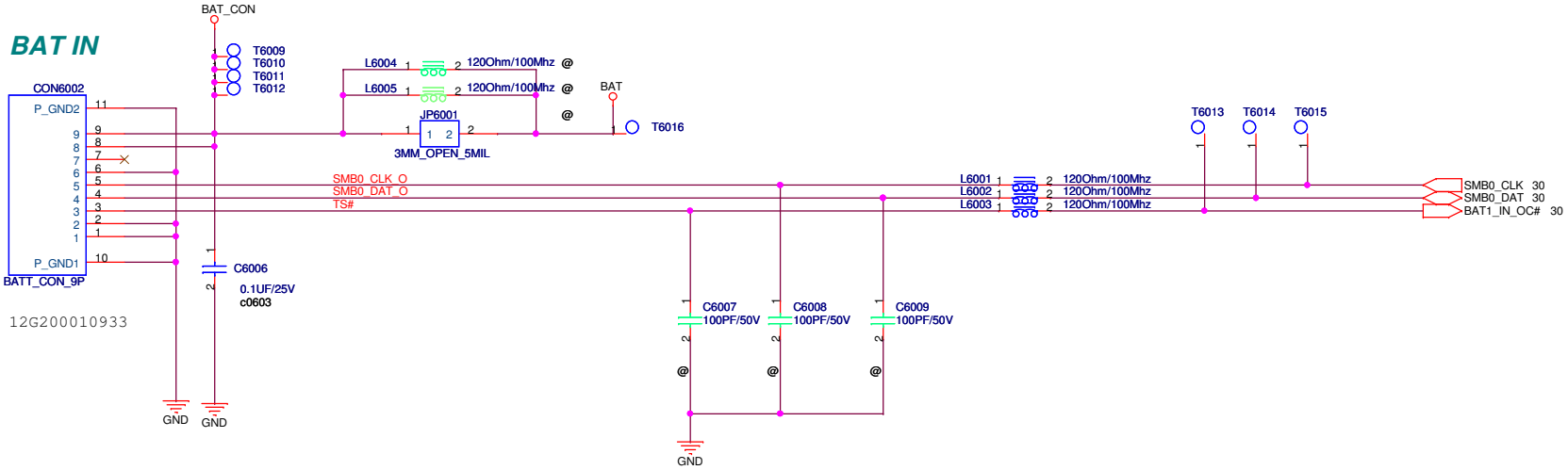
ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 58 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 59 of 97	

6/22 change part





12G200010933

<Variant Name>

ASUSTeK COMPUTER INC	Title : DC DC&BATT CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 60 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : BT BLUETOOTH CONN	
	Engineer: *Jerry Yu*	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 61 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 62 of 97	

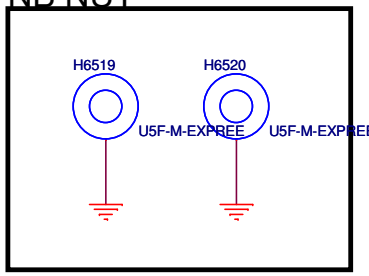
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 63 of 97	

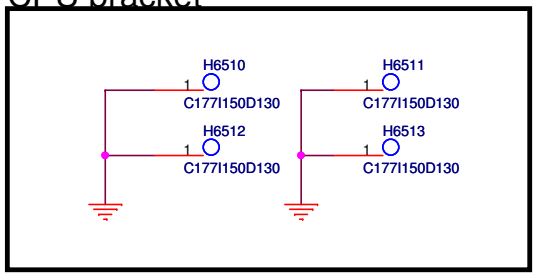
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 64 of 97	

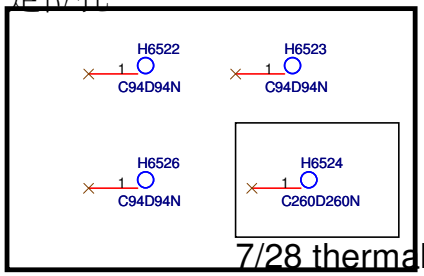
NB NUT



CPU bracket



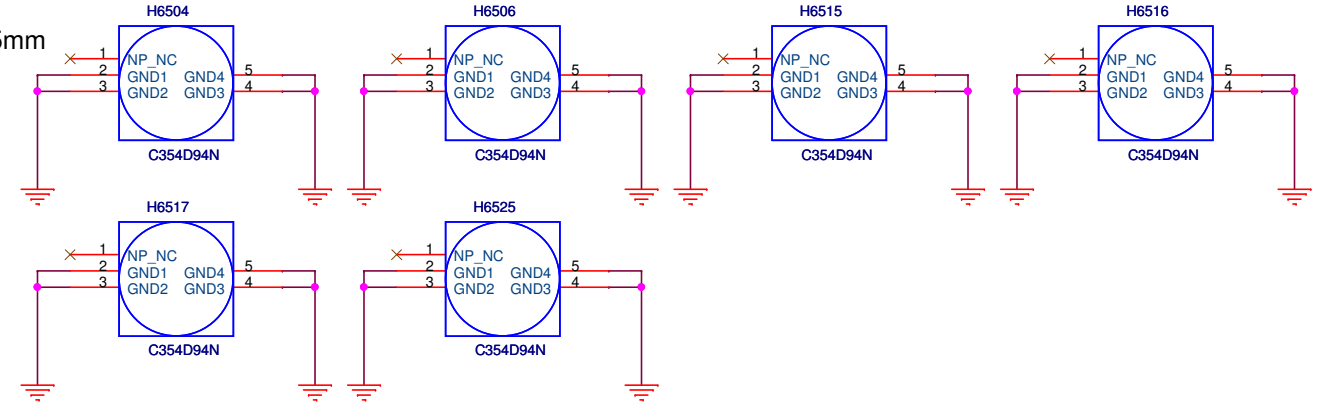
定位孔



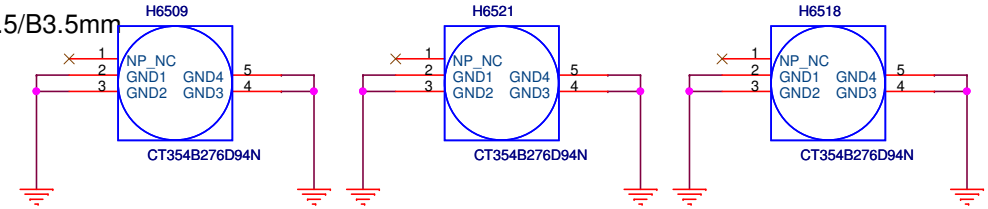
7/28 thermal request

Screw Holes

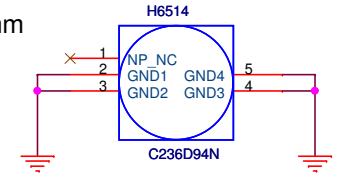
1.2/4.5mm

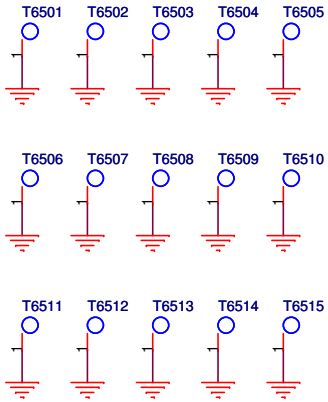


1.2/T4.5/B3.5mm



1.2/3mm





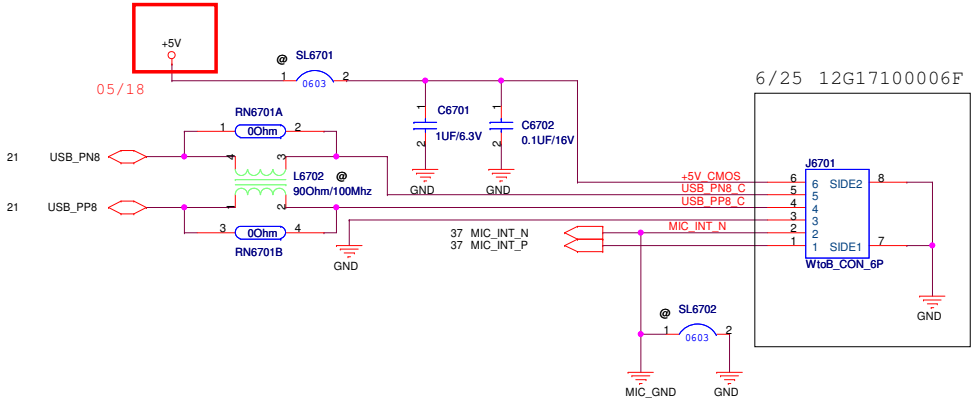
<Variant Name>

ASUSTeK COMPUTER INC	Title : ME SCREW HOLE AMT NUT	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 65 of 97	

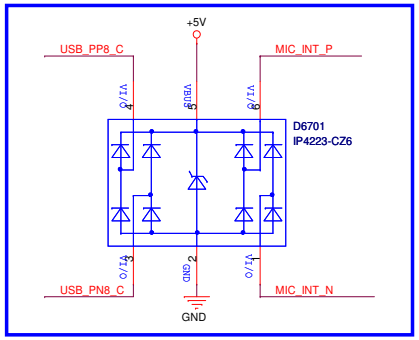
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 66 of 97	

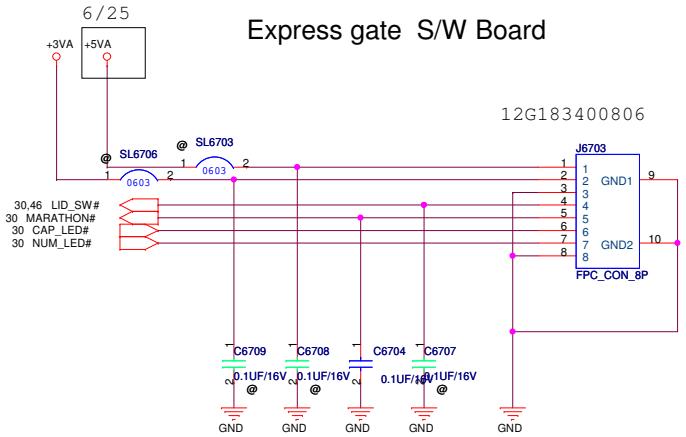
Camera Module & Mic.



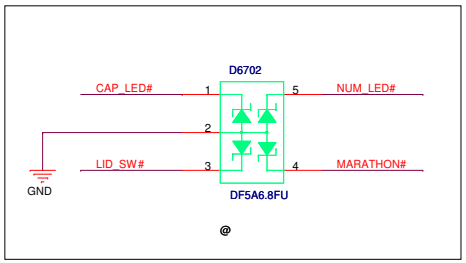
D6701 Close to J6701



Express gate S/W Board

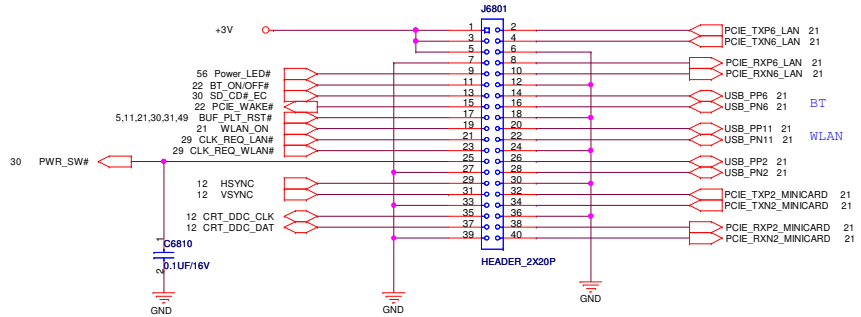


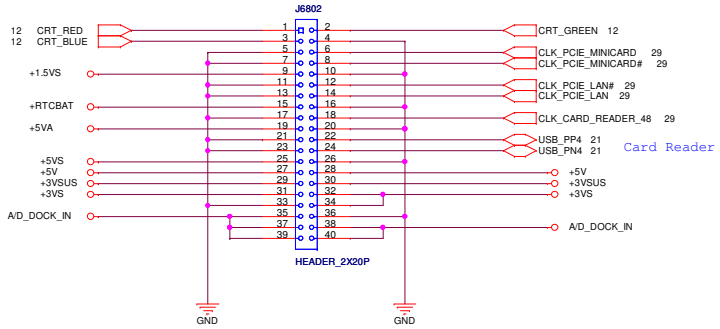
6/22 for ESD



<Variant Name>

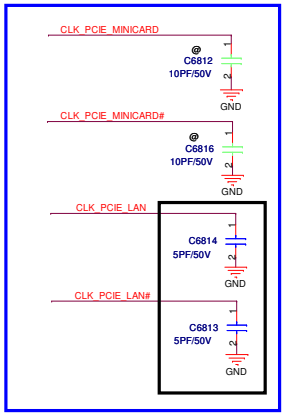
ASUS	Title :	CMO CMOS CAMERA
ASUSTeK COMPUTER INC	Engineer:	Jerry Yu
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 67 of 97	



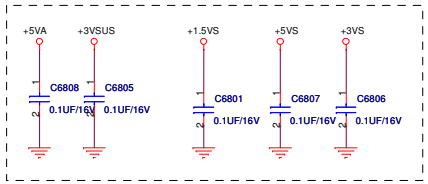


每一根估0.5A,connector spec 1A

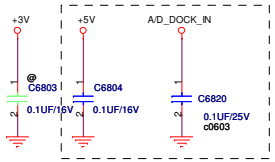
For Clock signal quality



EMI 07/03



EMI 05/25



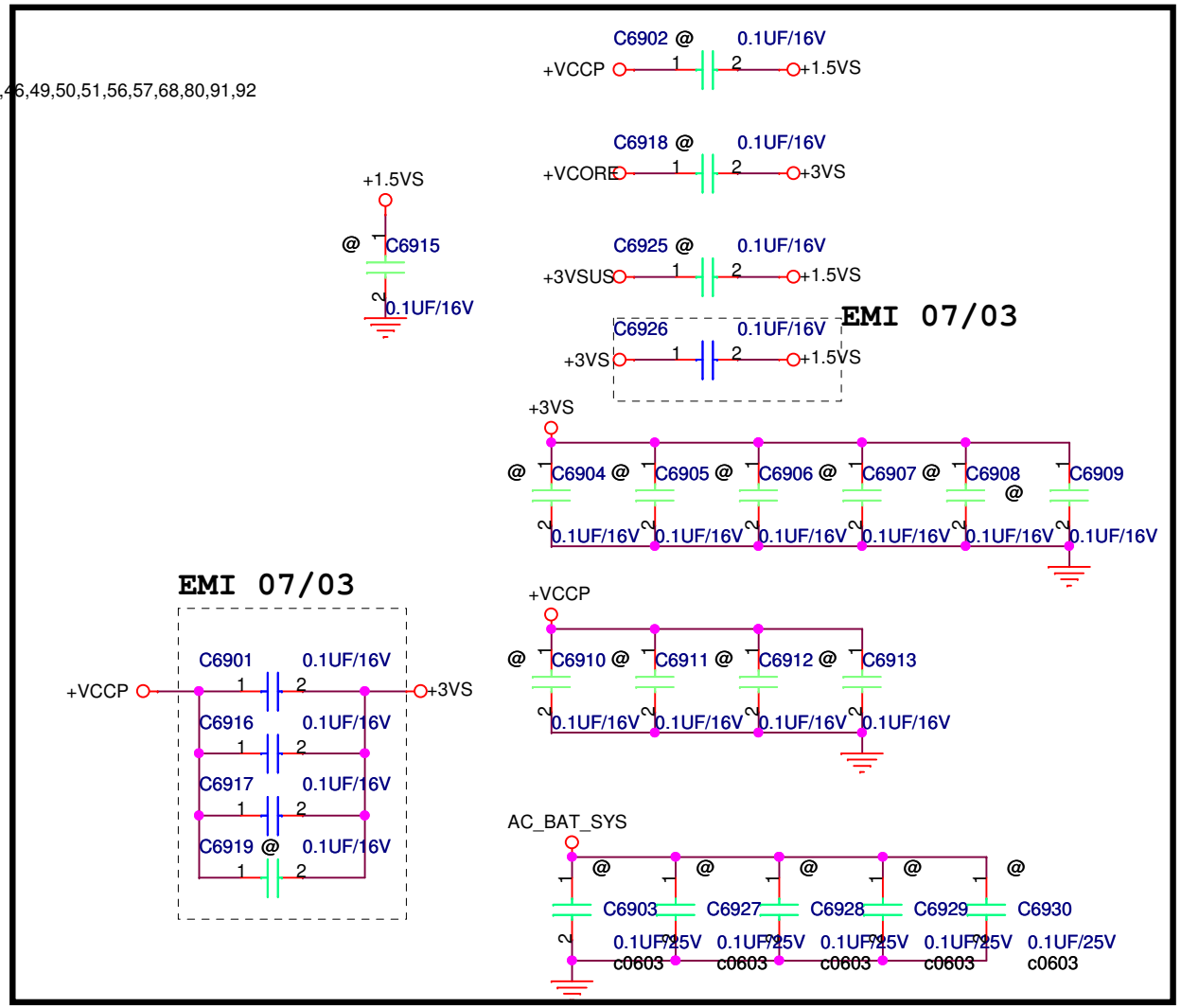
<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN	
	Engineer: Jerry Yu	
Size: Custom	Project Name: UL20A	Rev: 2.0
Date: Monday, August 03, 2009	Sheet 68 of 97	

SYSTEM

+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,82
+VCC_GMCH	+VCC_GMCH	3,4,5,10,11,12,14,15,20,23,29,57,82
+VGFX_CORE	+VGFX_CORE	3,4,5,10,11,12,14,15,20,23,29,57,82
+3VS	+3VS	3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,57,68,80,91,92
+VCORE	+VCORE	4,5,80
+1.5VS	+1.5VS	4,15,20,23,36,57,68,84
+1.8V	+1.8V	7,8,9,11,14,15,57,83,84,91
+5V	+5V	52,57,67,68,91
+5VS	+5VS	23,36,38,50,51,56,57,68,80,84,91
+3VA	+3VA	20,30,56,67,81,88
+VCC_RTC	+VCC_RTC	20,23
+3V	+3V	46,57,68,91
+3VSUS	+3VSUS	20,21,22,23,30,57,68,80,81,91,92
+5VSUS	+5VSUS	23,80,81,82,83,88,91
+3VPLL	+3VPLL	30,31
+3VACC	+3VACC	30
+3VA_EC	+3VA_EC	30,31
+5VS_AMP	+5VS_AMP	36
+12V	+12V	91
+12VS	+12VS	22,46,91
AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,88
+5VA	+5VA	56,67,68,81

EMI 05/25



<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size A	Project Name UL20A	Rev 2.0
Date: Monday, August 03, 2009	Sheet 69 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 70 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 71 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 72 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 73 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 74 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 75 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 76 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 77 of 97	

<Variant Name>

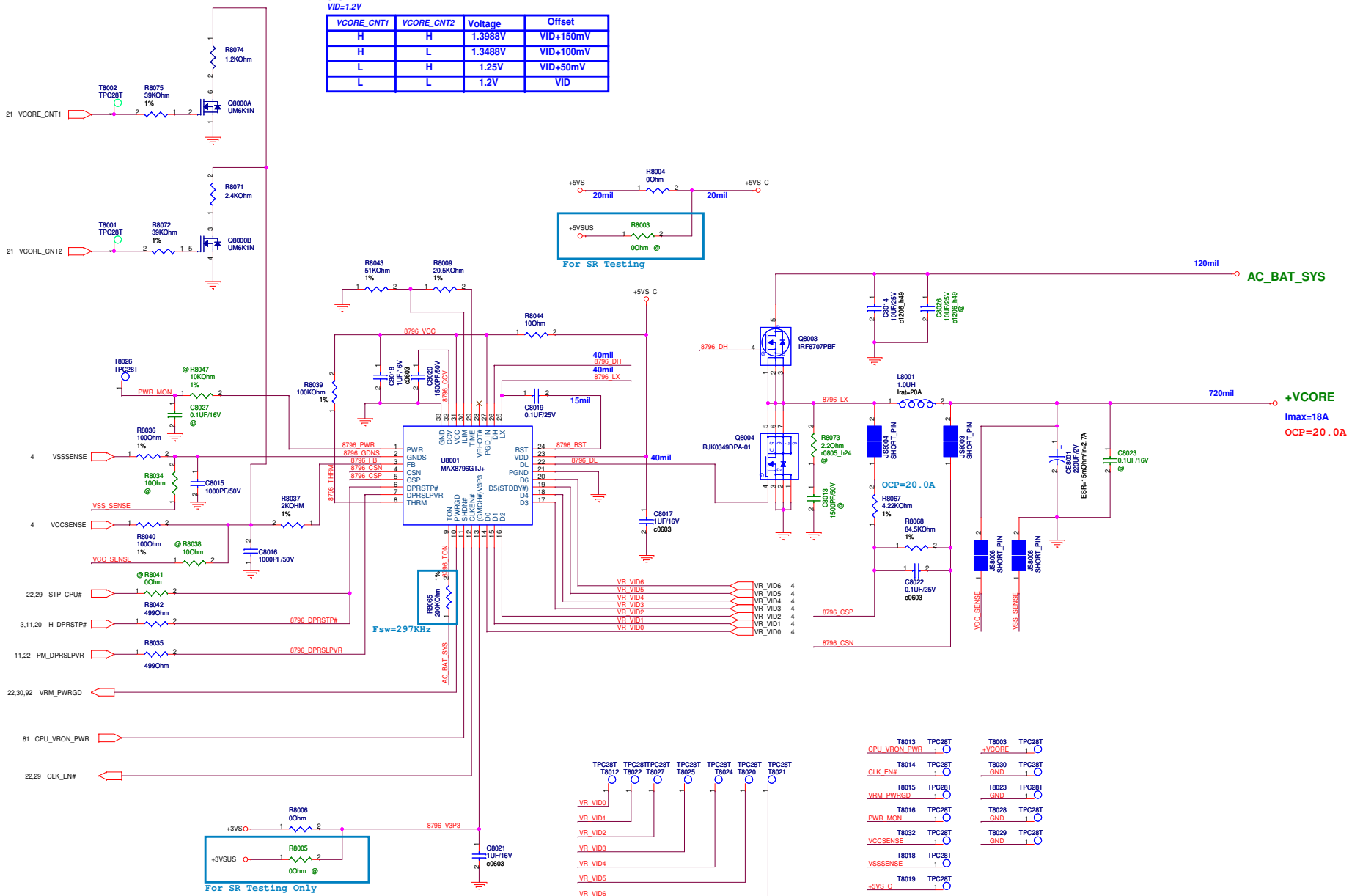
ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 78 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Jerry Yu	
Size: A	Project Name: UL20A	Rev: 2.0
Date: Wednesday, July 29, 2009	Sheet 79 of 97	

CPU
VID=1.2V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset
H	H	1.3988V	VID+150mV
H	L	1.3488V	VID+100mV
L	H	1.25V	VID+50mV
L	L	1.2V	VID



TOTAL COUNT : 29 PCS

<Variant Name>

ASUS

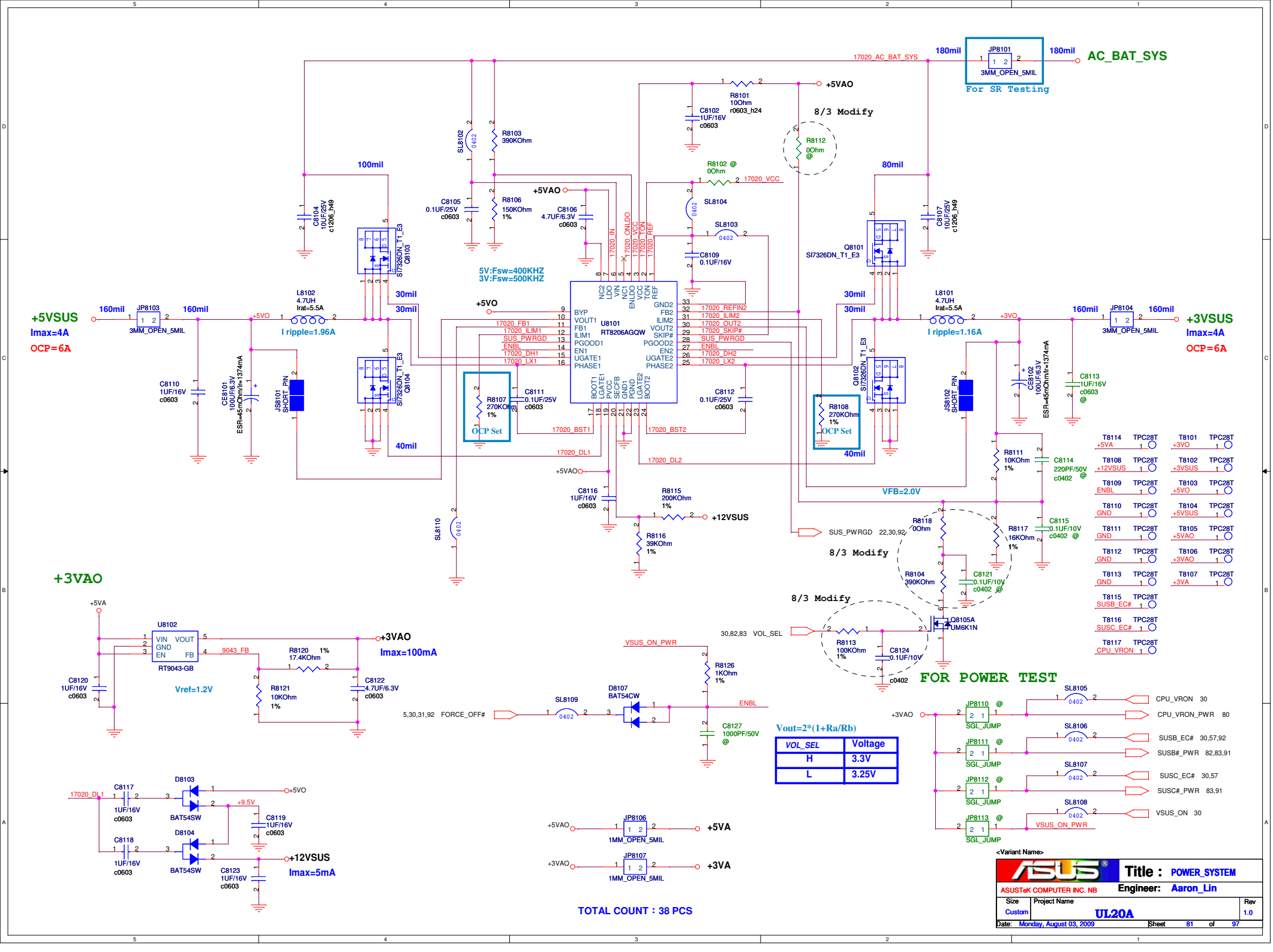
Title : POWER_VCORE

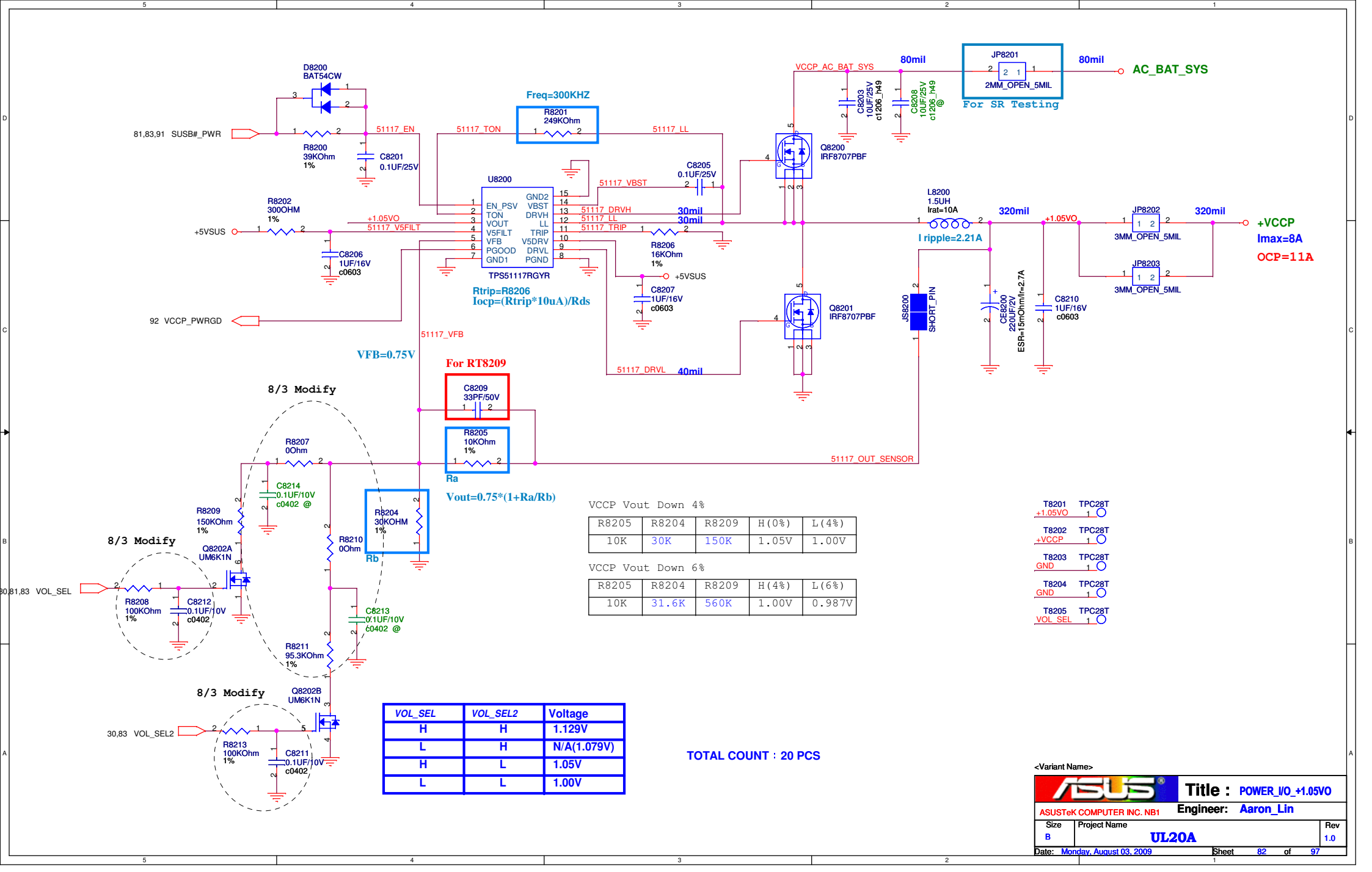
ASUSTeK COMPUTER INC. NB

Engineer: Aaron_Lin

Size	Project Name	Rev
C	UL20A	1.0

Date: Monday, August 03, 2009 Sheet 80 of 97


AC_BAT_SYS
JP8101
3MM_OPEN_5MIL
For SR Testing
180mil
17020_AC_BAT_SYS
+5VAO
R8101
10Ohm
r0603_h24
C8102
1UF/16V
c0603
8/3 Modify
R8112
0Ohm
R8102 @
0Ohm
17020_VCC
SL8104
SL8103
C8109
0.1UF/16V
SL8102
R8103
390KOhm
100mil
80mil
C8104
10UF/25V
c1206_h49
C8105
0.1UF/25V
c0603
R8106
150KOhm
1%
C8106
4.7UF/6.3V
c0603
C8107
10UF/25V
c1206_h49
Q8101
SI7326DN_T1_E3
Q8103
SI7326DN_T1_E3
5V:Fsw=400KHZ
3V:Fsw=500KHZ
+5VSUS
Imax=4A
OCP=6A
160mil
JP8103
3MM_OPEN_5MIL
+5VO
L8102
4.7UH
Irat=5.5A
I ripple=1.96A
30mil
40mil
C8110
1UF/16V
c0603
CE8101
100UF/6.3V
ESR=45mOhm/Ir=1374mA
JS8101
SHORT_PIN
Q8104
SI7326DN_T1_E3
U8101
RT8206AGQW
BYP
VOUT1
FB1
ILIM1
PGOOD1
EN1
UGATE1
PHASE1
NC2
LDO
VIN
NC1
ENLDO
VCC
TON
REF
GND2
FB2
ILIM2
VOUT2
SKIP#
PGOOD2
EN2
UGATE2
PHASE2
BOOT1
LGATE1
PVCC
SECFB
GND1
PGND
LGATE2
BOOT2
17020_FB1
17020_ILIM1
SUS_PWRGD
ENBL
17020_DH1
17020_LX1
17020_BST1
17020_DL1
17020_REFIN2
17020_ILIM2
17020_OUT2
17020_SKIP#
SUS_PWRGD
ENBL
17020_DH2
17020_LX2
17020_BST2
17020_DL2
17020_ONLDO
17020_IN
17020_VCC
17020_TON
17020_REF
R8107
270KOhm
1%
OCP Set
C8111
0.1UF/25V
c0603
C8112
0.1UF/25V
c0603
R8108
270KOhm
1%
OCP Set
+3VSUS
Imax=4A
OCP=6A
160mil
JP8104
3MM_OPEN_5MIL
L8101
4.7UH
Irat=5.5A
I ripple=1.16A
+3VO
JS8102
SHORT_PIN
CE8102
100UF/63V
ESR=45mOhm/Ir=1374mA
C8113
1UF/16V
c0603
@
R8111
10KOhm
1%
C8114
220PF/50V
c0402
@
VFB=2.0V
C8116
1UF/16V
c0603
R8115
200KOhm
1%
+12VSUS
R8116
39KOhm
1%
SL8110
SUS_PWRGD 22,30,92
R8118
0Ohm
R8117
16KOhm
1%
C8115
0.1UF/10V
c0402 @
8/3 Modify
R8104
390KOhm
C8121
0.1UF/10V
c0402 @
8/3 Modify
30,82,83 VOL_SEL
Q8105A
UM6K1N
R8113
100KOhm
1%
C8124
0.1UF/10V
c0402
FOR POWER TEST
T8114 TPC28T +5VA
T8108 TPC28T +12VSUS
T8109 TPC28T ENBL
T8110 TPC28T GND
T8111 TPC28T GND
T8112 TPC28T GND
T8113 TPC28T GND
T8115 TPC28T SUSB_EC#
T8116 TPC28T SUSC_EC#
T8117 TPC28T CPU_VRON
T8101 TPC28T +3VO
T8102 TPC28T +3VSUS
T8103 TPC28T +5VO
T8104 TPC28T +5VSUS
T8105 TPC28T +5VAO
T8106 TPC28T +3VAO
T8107 TPC28T +3VA
+3VAO
+5VA
U8102
RT9043-GB
VIN VOUT
GND
EN FB
9043_FB
R8120 1%
17.4KOhm
+3VAO
Imax=100mA
C8120
1UF/16V
c0603
Vref=1.2V
R8121
10KOhm
1%
C8122
4.7UF/6.3V
c0603
VSUS_ON_PWR
R8126
1KOhm
1%
5,30,31,92 FORCE_OFF#
SL8109
D8107
BAT54CW
ENBL
C8127
1000PF/50V
@
Vout=2*(1+Ra/Rb)
VOL_SEL | Voltage
H | 3.3V
L | 3.25V
+3VAO
JP8110 @
SGL_JUMP
SL8105
CPU_VRON 30
CPU_VRON_PWR 80
JP8111 @
SGL_JUMP
SL8106
SUSB_EC# 30,57,92
SUSB#_PWR 82,83,91
JP8112 @
SGL_JUMP
SL8107
SUSC_EC# 30,57
SUSC#_PWR 83,91
JP8113 @
SGL_JUMP
SL8108
VSUS_ON 30
VSUS_ON_PWR
17020_DL1
C8117
1UF/16V
c0603
D8103
BAT54SW
+5VO
+9.5V
C8119
1UF/16V
c0603
C8118
1UF/16V
c0603
D8104
BAT54SW
+12VSUS
Imax=5mA
C8123
1UF/16V
c0603
+5VAO
JP8106
1MM_OPEN_5MIL
+5VA
+3VAO
JP8107
1MM_OPEN_5MIL
+3VA
TOTAL COUNT : 38 PCS
<Variant Name>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Aaron_Lin
Size Custom
Project Name UL20A
Rev 1.0
Date: Monday, August 03, 2009
Sheet 81 of 97



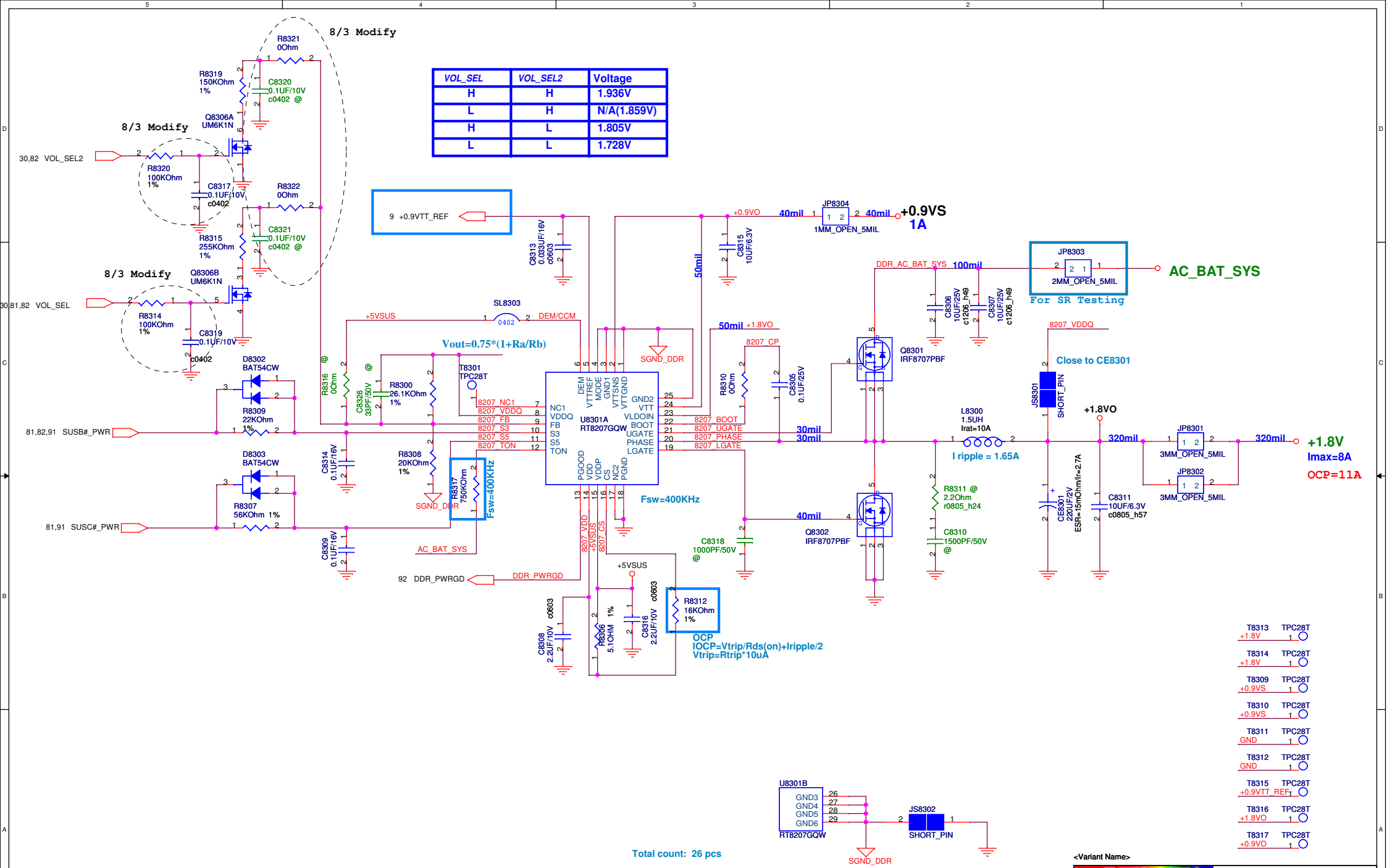
VCCP Vout Down 4%

R8205	R8204	R8209	H(0%)	L(4%)
10K	30K	150K	1.05V	1.00V

VCCP Vout Down 6%

R8205	R8204	R8209	H(4%)	L(6%)
10K	31.6K	560K	1.00V	0.987V

VOL_SEL	VOL_SEL2	Voltage
H	H	1.129V
L	H	N/A(1.079V)
H	L	1.05V
L	L	1.00V



VOL_SEL	VOL_SEL2	Voltage
H	H	1.936V
L	H	N/A(1.859V)
H	L	1.805V
L	L	1.728V

<Variant Name>

ASUSTeK COMPUTER INC. NB

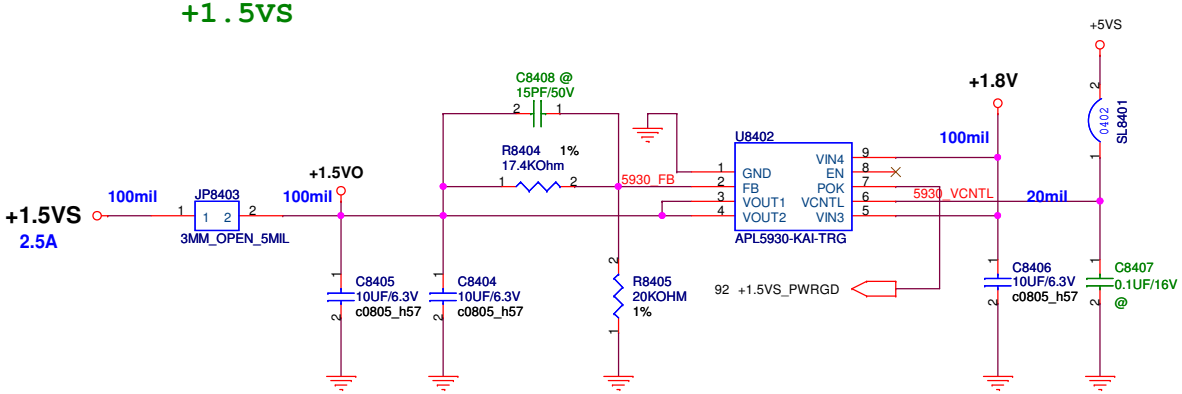
Title : POWER_I/O_DDR & VTT

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UL20A	1.0

Date: Monday, August 03, 2009 Sheet 83 of 97

+1.5VS



T8405	+1.5VO	TPC28T
T8406	+1.5VS	TPC28T
T8407	GND	TPC28T
T8408	GND	TPC28T

Total count: 6 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_ +1.8VS	
	Engineer: Aaron_Lin	
Size: B	Project Name: UL20A	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : +MCP_VDD_CORE	
	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : N/A	
	Engineer: Aaron_Lin	
Size B	Project Name UL20A	Rev 1.0
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<Variant Name>

ASUS	Title : N/A	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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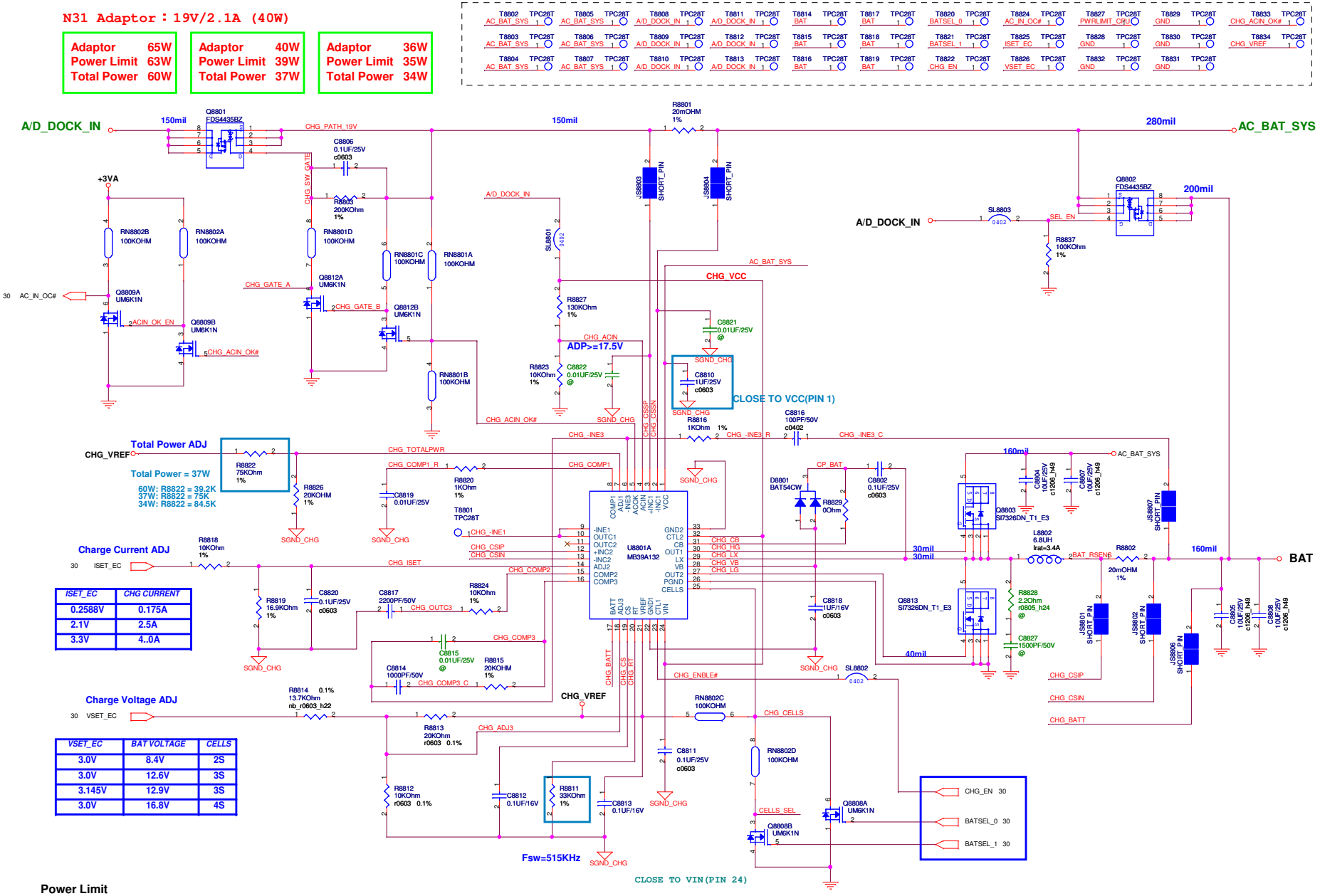
N31 Adaptor：19V/2.1A (40W)

Adaptor	65W
Power Limit	63W
Total Power	60W

Adaptor	40W
Power Limit	39W
Total Power	37W

Adaptor	36W
Power Limit	35W
Total Power	34W

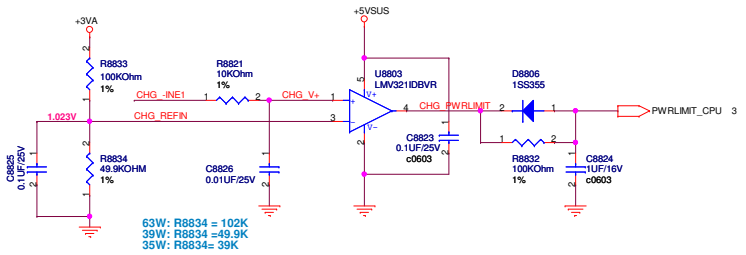


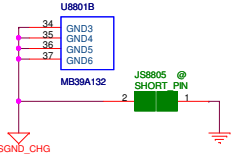
ISET_EC	CHG CURRENT
0.2588V	0.175A
2.1V	2.5A
3.3V	4..0A

VSET_EC	BAT VOLTAGE	CELLS
3.0V	8.4V	2S
3.0V	12.6V	3S
3.145V	12.9V	3S
3.0V	16.8V	4S

Power Limit

Power Limit = 39W





TOTAL COUNT：58 PCS

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet：
Charger MAX8725 => EC CODE：200
Charger MAX17015 => EC CODE：201
Charger MB39A132 => EC CODE：202

ASUSTeK COMPUTER INC. NB3

Title : CHARGER_202

Engineer: Aaron_Lin

Size: Custom | Project Name: UL20A | Rev: 1.0

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<Variant Name>

ASUS	Title : N/A	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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BATTERY IN DETECT

ADAPTER IN DETECT

<Variant Name>

ASUS	Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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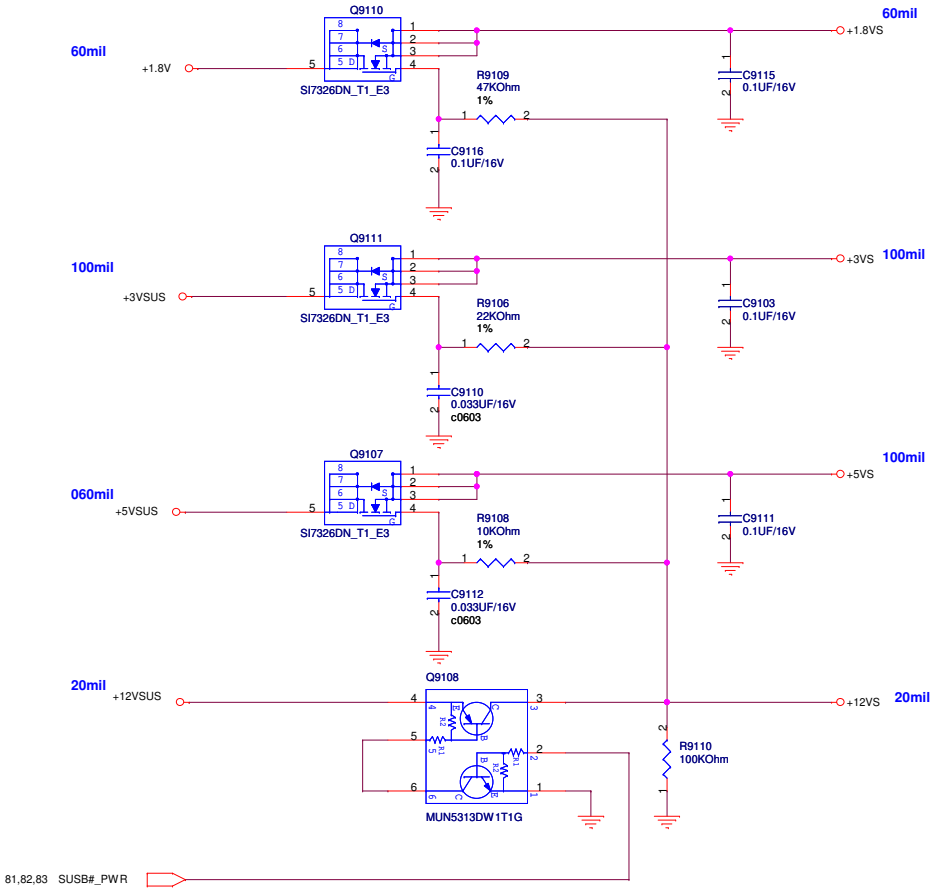
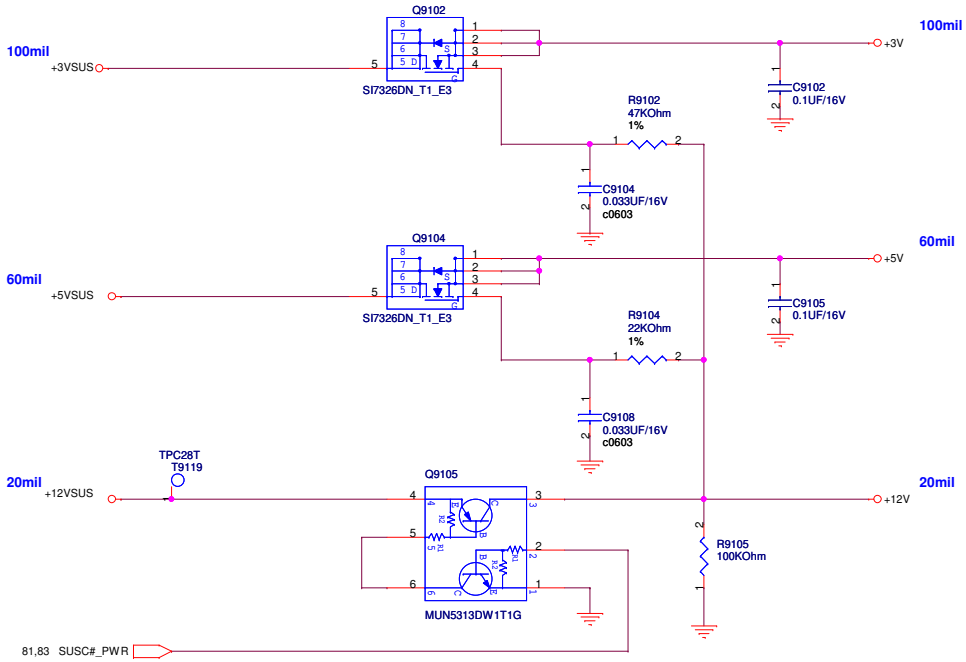
SUSB#_PWR POWER



SUSC#_PWR POWER



T9101 +12VSUS	TPC28T	T9111 +3VSUS	TPC28T
T9102 +12VS	TPC28T	T9113 +3VS	TPC28T
T9103 +12V	TPC28T	T9115 +3V	TPC28T
T9104 +5VSUS	TPC28T	T9120 +1.8V	TPC28T
T9106 +5VS	TPC28T	T9121 +1.8VS	TPC28T
T9110 +5V	TPC28T	T9123 SUSB# PWR	TPC28T
		T9114 SUSC# PWR	TPC28T

TOTAL COUNT : 19 PCS

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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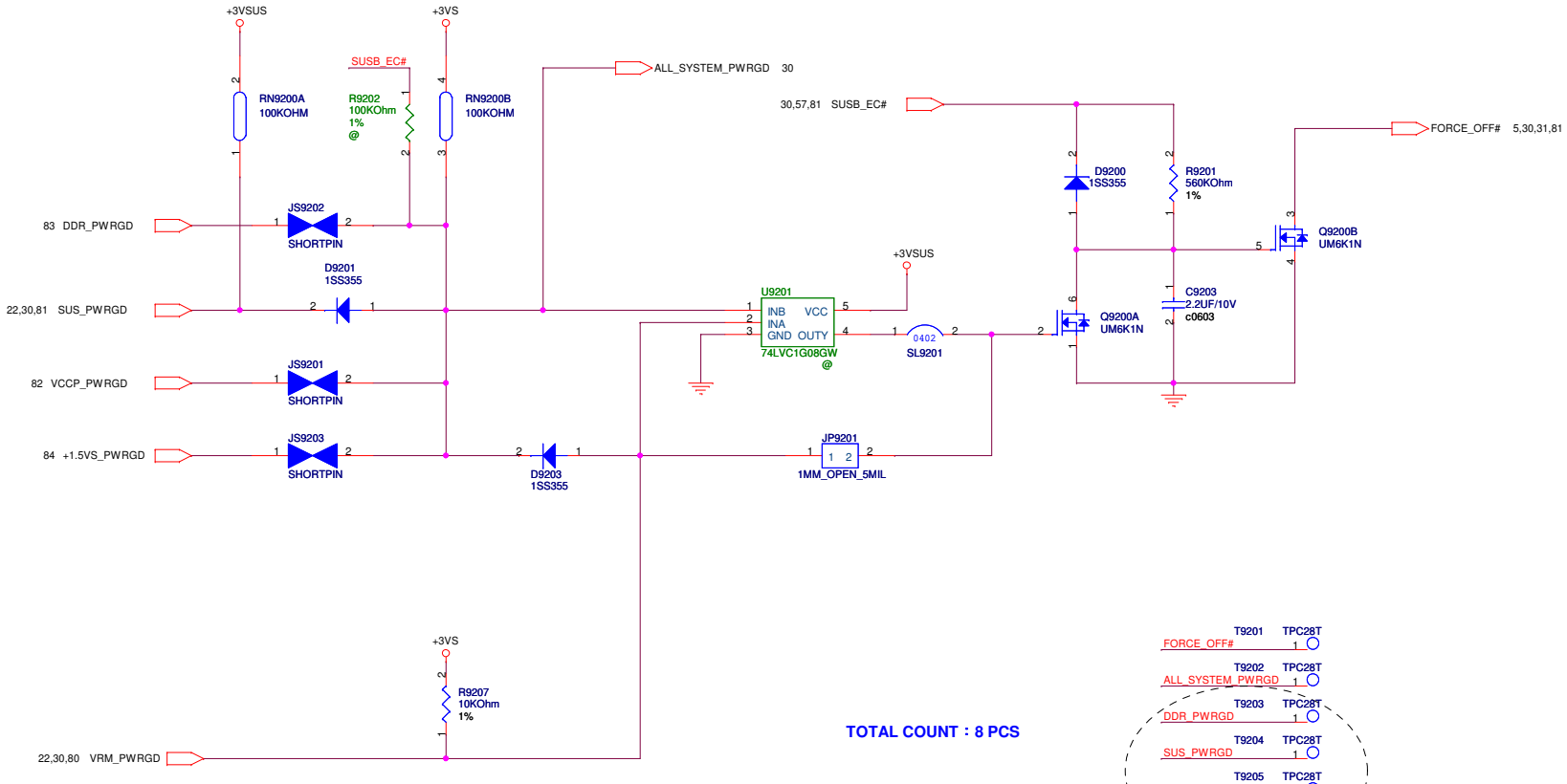
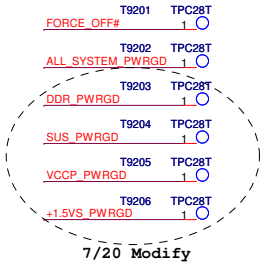
POWER GOOD DETECTER



TOTAL COUNT : 8 PCS



7/20 Modify

<Variant Name>

ASUS	Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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AC_BAT_SYS	AC_BAT_SYS	46,69,80,81,82,83,88
+5VAO	+5VAO	81
+5VA	+5VA	56,67,68,81
+3VAO	+3VAO	81
+3VA	+3VA	20,30,56,67,81,88
+12VSUS	+12VSUS	81,91
+5VSUS	+5VSUS	23,80,81,82,83,88,91
+3VSUS	+3VSUS	20,21,22,23,30,57,68,69,80,81,91,92
+12V	+12V	91
+5V	+5V	52,57,67,68,91
+3V	+3V	46,57,68,91
+1.8V	+1.8V	7,8,9,11,14,15,57,83,84,91
+0.9VS	+0.9VS	9,57,83
+12VS	+12VS	22,46,91
+5VS	+5VS	23,36,38,50,51,56,57,68,80,84,91
+3VS	+3VS	3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,57,68,69,80,91,92
+1.8VS	+1.8VS	15,91
+1.5VS	+1.5VS	4,15,20,23,36,57,68,69,84
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,69,82
+VCORE	+VCORE	4,5,69,80

<Variant Name>

ASUS	Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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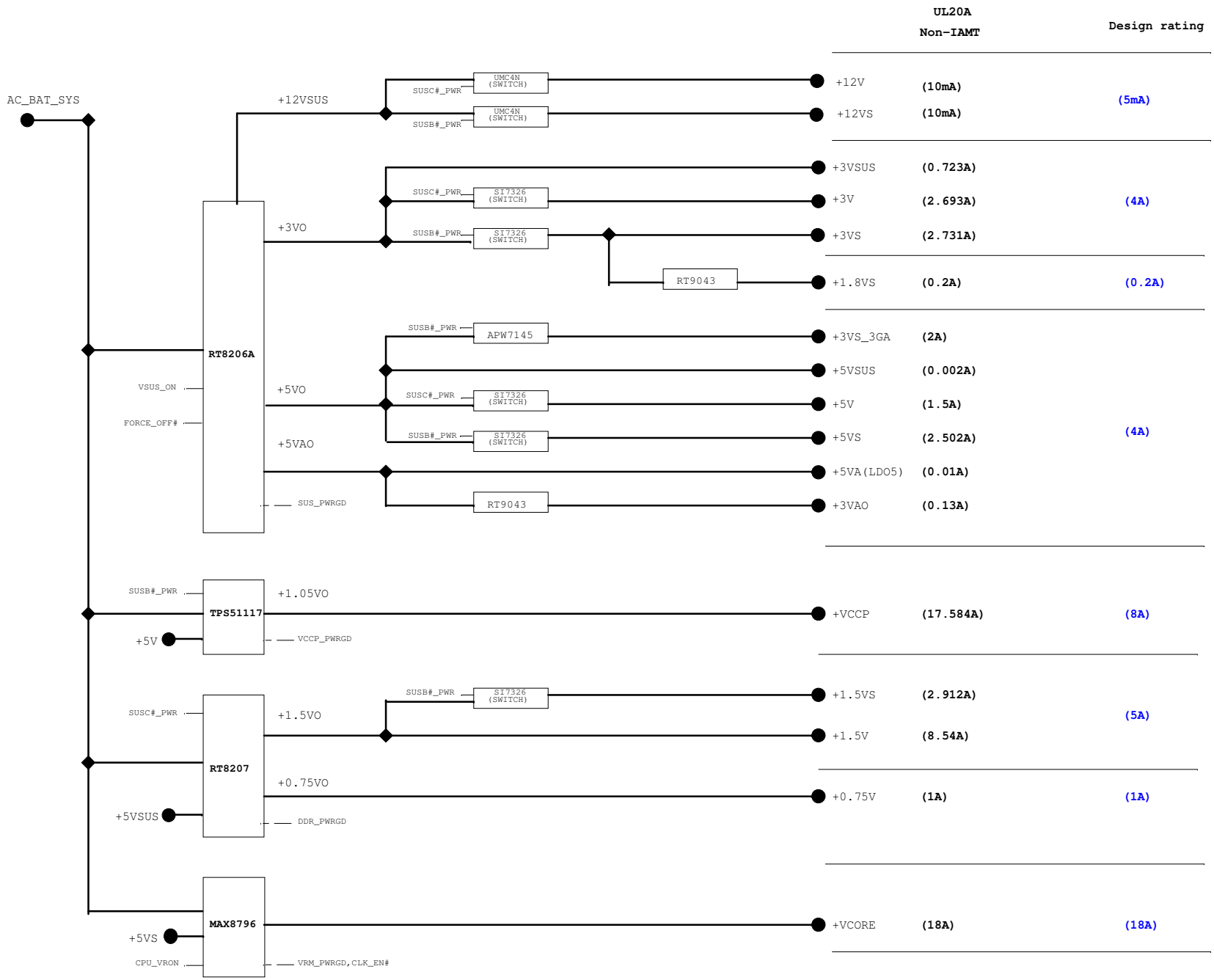

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UL20A	1.0

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<Variant Name>

ASUS	Title : POWER_LED_VCC BOOST	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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Rev	Date	Description
1.2a	2009/06/15	Item 1 remove CE0502 220uF, C0501,C0503,C0504 10uF/10V (0805) add C0532,C0533,C0534,C0535,C0536,C0501,C0503,C0504 10uF/6.3V(0603) Item 2 connect SW5601,SW5602 pin5&6 to GND Item 3 change TP/DeBUG conn to 12G183401225 ME request Item 4 unmount R3602,R3603,C3603 disable PC beep function
1.2b	2009/06/22	Item 1 change D6002 to 07G001023010 Item 2 add D5601,D5602,D6702 for ESD Item 3 add R3001 to reduce xtal DL Item 4 EA CLK: RN2905->47ohm, C2932=C2933=C6813=C6814->5pF Item 5 EA CRT: R1208->1k ohm Item 6 change Camera conn to 12G17100006F for cost down Item 7 charge/PWR LED connect from VSUS to VA (P.56), cap/num lock LED connect from VS to VA (P.67)
1.2c	2009/06/29	Item 1 update PWR schematic 0701 Item 2 change audio 5V LDO 06G029330020 by designIP (P.36) Item 3 restore CE0502 220uF Item 4 EMI: add C5605, C5606 0.1uF on Left/Right Item 5 Thermal: change H6524 to 2.4mm hole
1.2	2009/07/03	Item 1 EMI: mount C6801,C6804,C6805,C6806,C6807,C6808,C6820,C6901,C6916,C6917, C6926,C1431,C3601,C3621
2.0a	2009/07/20	Item 1 change J6802.19 to +5VA
2.0b	2009/07/28	Item 1 Thermal: change H6524 to 6.6mm hole Item 2 update PWR circuit: 1.8V low voltage circuit
	2009/07/30	Item 3 add vol_sel2 on EC GPH3 Item 4 update PWR circuit: Vcore/Vccp/1.8V/3.3V voltage control Item 5 add BSEL strap Q2902 circuit for over clocking (P.29)
2.0	2009/08/03	Item 1 PWR: update 3.3V/VCCP/DDR power control circuit

Rev	Date	Description

ASUS	Title : HISTORY	
<OrgName>	Engineer: Aaron_Lin	
Size: Custom	Project Name: UL20A	Rev: 1.0
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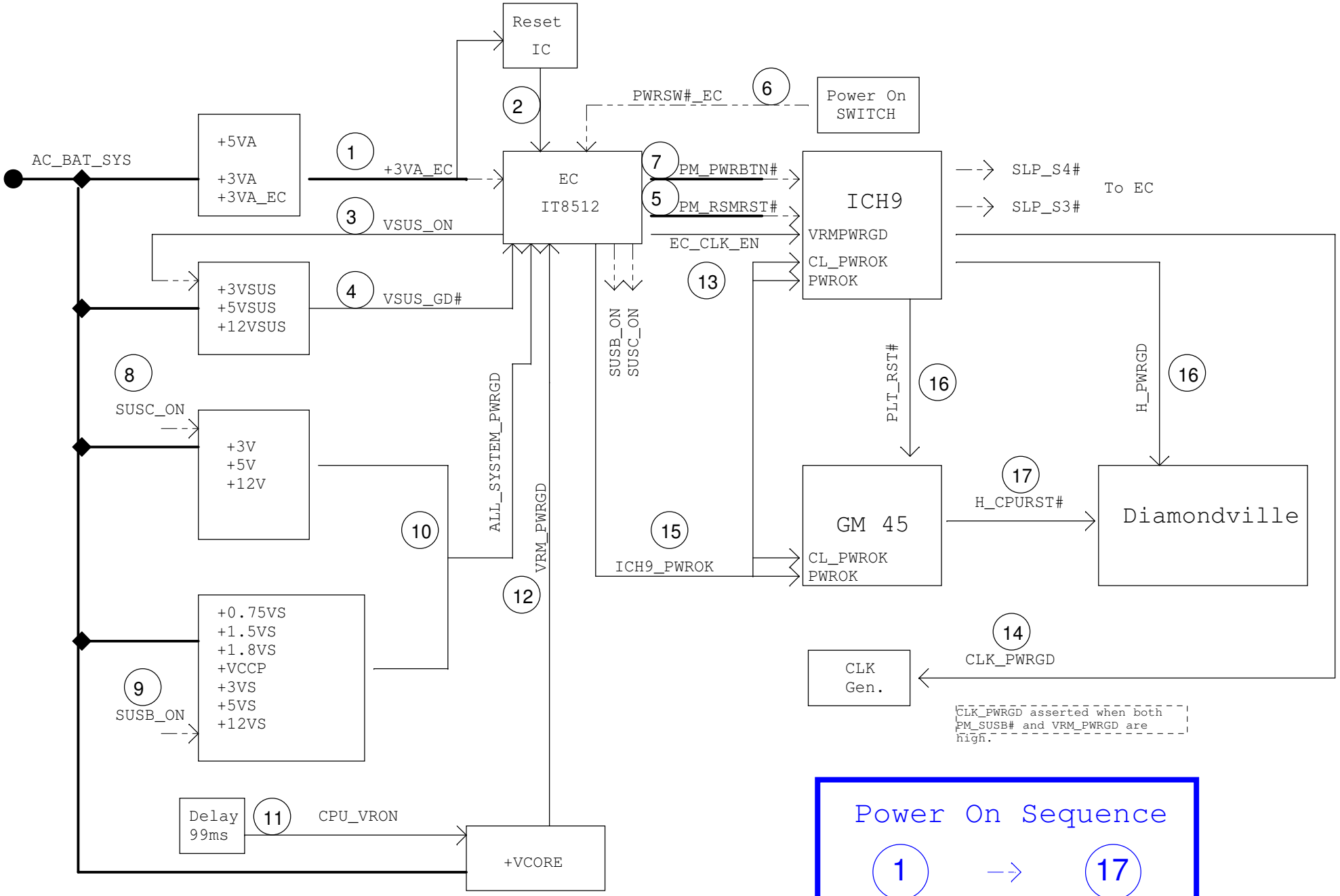

ASUS	Title : POWER SEQUENCE		
<OrgName>	Engineer: Aaron_Lin		
Size: Custom	Project Name: UL20A		Rev: 1.0
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