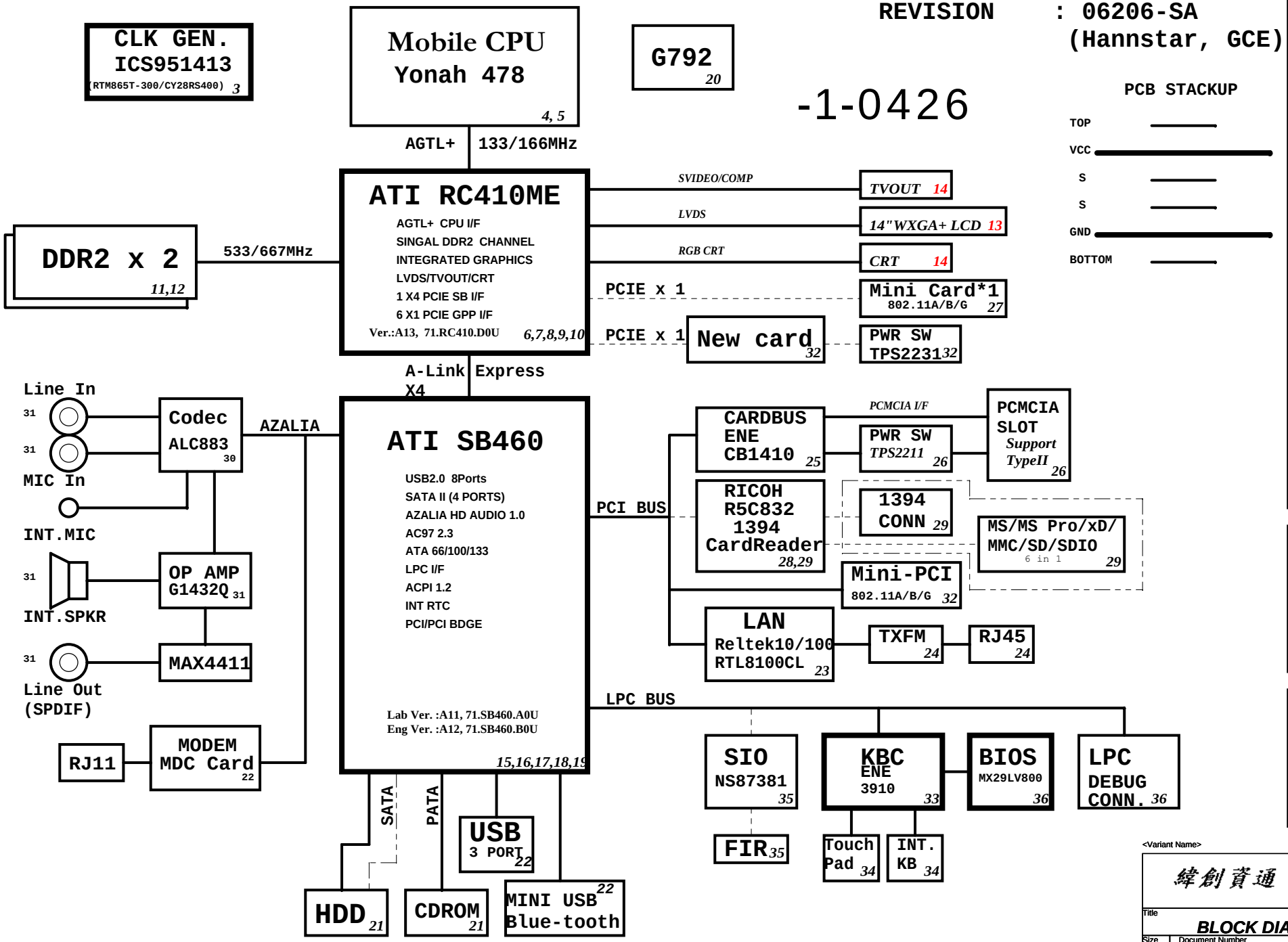
Garda-5 Block Diagram

Project code: 91.4Q201.001
PCB P/N : 55.4Q201.XXX
REVISION : 06206-SA
(Hannstar, GCE)

-1-0426



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124RGER 42	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0
APL5312 120mA	
3D3V_S0	1D5V_CPU_S0 43
APL5332 1A	
3D3V_S0	1D5V_NEW_MINI_S0 43
APL5912 3A	
1D2V_S0	1D05V_S0 43
TPS51100 1A	
1D8V_S3	DDR_VREF_S3 DDR_VREF_S0 43
APL5308 300mA	
3D3V_S5	1D8V_S5 43

MAXIM CHARGER MAX8725 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 39,40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 48A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Garda-5 | Rev: -1

Date: Wednesday, April 26, 2006 | Sheet 1 of 46

USB	
Pair	Device
0	USB1
1	BT
2	USB2
3	NEW C
4	USB3
5	CCD
6	MINIC1
7	NC

PCI_CLK0	PCM
PCI_CLK1	IEEE1394
PCI_CLK2	LAN
PCI_CLK3	MINI
PCI_CLK4	KBC
PCI_CLK5	FWH
PCI_CLK6	SIO
PCI_CLK7	SPDIFOUT

PCI ROUTING TABLE

DEVICE	IDSEL	IRQ(Default)	REQ# / GNT#
MiniPCI	AD22	H	REQ#1/ GNT#1
R5C832	AD20	F : 1394 H : 6 in 1	REQ#3/ GNT#3
LAN(RTL8100CL)	AD17	E	REQ#2/ GNT#2
CARDBUS CB1410	AD16	G	REQ#0 / GNT#0
USB UHCI	AD29	A, B, C, D	
USB 2.0 EHCI	AD29	A	
DMI-to-PCI AC97 Modem AC97 Audio	AD30	B A	REQ#1 / GNT#1
LPC Bridge IDE SATA SMBus	AD31	A B B	
PCI Express	AD28	A, B, C, D	
Azalia Controller	AD27	A	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

History

```
==========================================================
2006/04/26 (-1 Modify)
1. page 27, change R8/R226 to 100 ohm due to power/email to dark.
2. page 15, change C286/C287 from 18pf to 15pf due to frequence shift(from -6.7 to 4ppm).
3. page 23, change C295/C294 from 15p to 12p due to frequence shift(from -23.3 to 7.9ppm).
4. EMI Solution for USB/MDC
        a. Change L23, L24, L31, L32 to "69.10084.071".
        b. del R353,R354,R356,R360,R445,R446.
        c. Change L1, L2 to "68.00331.011".
5. Page 44, change C12/C14 to 78.10699.43L due to 78.10699.42L Obsoleted.
==========================================================
2006/04/13 (-1 Modify)
1. Page 31, R447/R448 tp 33ohm.
2. Page 45, Add D4:83.P4SSM.0AM.
3. Page 44, Change C321 from 78.10492.4BL to 78.10224.2BL(1000P, 50V, K0603).
4. Page 23, change R209 from 5.6K to 5.37K.
5. Page 24, change XF1 from 68.68161.30A to 68.01201.30A.
6. Page 46, Mini card stand-off(銅柱) need to be changed from 34.4P401.001 to 34.4A907.001.
7. change 84.27002.L04 to 84.27002.F31.
==========================================================
2006/04/10 (-1 Modify)
1. Page 8, add "LVDS_DIGON" solution from ATI PA note.
2. Page 31, Add R to GND and serial R for U60 pin13/15.
==========================================================
2006/04/03 (SB Modify)
1. Page 40,  Dummy C593.
2. Page 44, Del C32.
3. Page 41, DCBATOUT_51120 change to DCBATOUT (Del G4,G5,G6,G7,G8)
4. Page 4/5, updae CPU symbol.
5. Page 15, Change X5 to same as X1 due to ME high limit issue, Cap. the same as X1 but should fine-tune.
6. Page 39/41/42, change "GAP-CLOSE-PWR" to 0 ohm PAD due to layout concern.
==========================================================
2006/03/31 (SB Modify)
1. Page 3, change R139 to bead and C211 to 2.2u for CRT Jitter.
2. Page 6, change R105 from 1.8K to 4.7K.
3. Page 8, change C165 to 2.2u for ATI recommend.
4. Page 8, SIV EDID_CLK/DAT issue, change RN53 to 4.7K.
5. Page 14, SIV RBG fail:
6. Page 15,
        a. PCIRST1#(1394) shoulder: Add 33 ohm @ SB.
        b. PLT_RST1# overshot : change R144 to 33ohm & R141 to 100P.
        c. Add 0ohm for RTC power for ATI recommend.
7. Page 40 , add 10U Cap.
8. Page 13/27, change Green LED4/LED5/LED1 to 83.00190.L70.
       (manual change yellow LED6/LED3/LED8/LED2 to 83.00190.S70).
9. EMI request:
        a. Page 13, USB_PP5,USB_PN5 add COMMON CHOKE.
        b. EC28,EC34,C208 add O.1µCap.
        c. CLK48_ICH( near CLK GEN.),SB_CLK33_FWH(near R177) add 20p Cap..
==========================================================
2006/03/28 (SB Modify)
1. Page 14, change Q15/Q14 to 2N7002 for SIV CRT SMBus bug.
2. Page 15, Change C248/C261/C264/C263/C252 from 78.10491.4FL to 78.10523.5F1,
        and C262 from 78.10693.41L to 78.10623.51L.
3. Page 8, Add "LCDVDD_ON" PL 100K.
4. Page 41, change U7 to AO4406(84.04406.A37).
5. Page 33, KBC GPIO09 for 1394.
6. Page 33, add 1u Cap. for ENE ECRST# spec. 2ms.
7. Page 31, add audio popo noise solution.
8. Page 25, change C520 to 1U for "GBRST#".
9. Page 28, change "GBUS_GRST#_1" timing.
==========================================================
```

<Variant Name>

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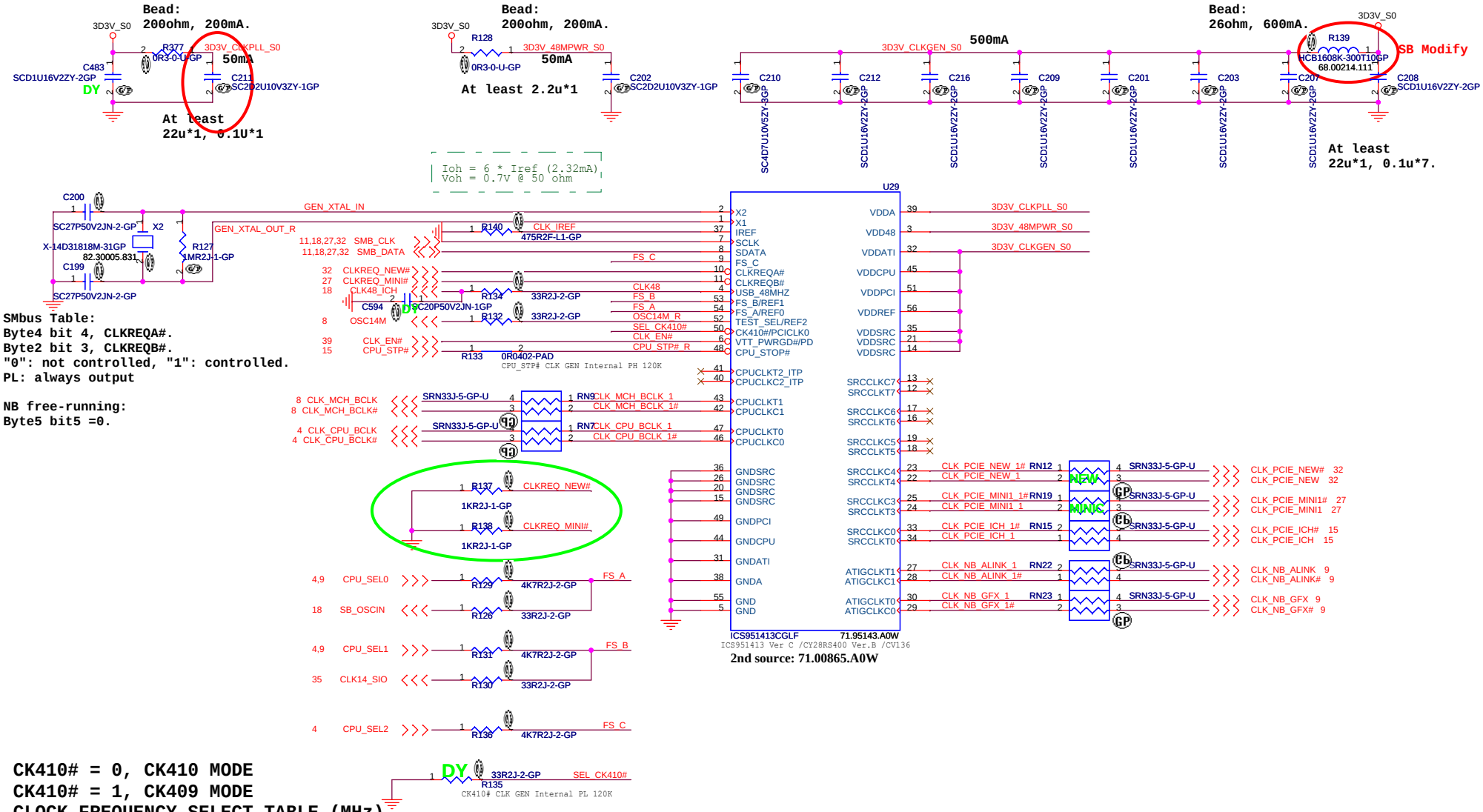
Title: Reference		
Size: A3	Document Number: Garda-5	Rev: -1
Date: Wednesday, April 26, 2006	Sheet 2 of 46	



FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	RESV	100	33	14.31

<Variant Name>

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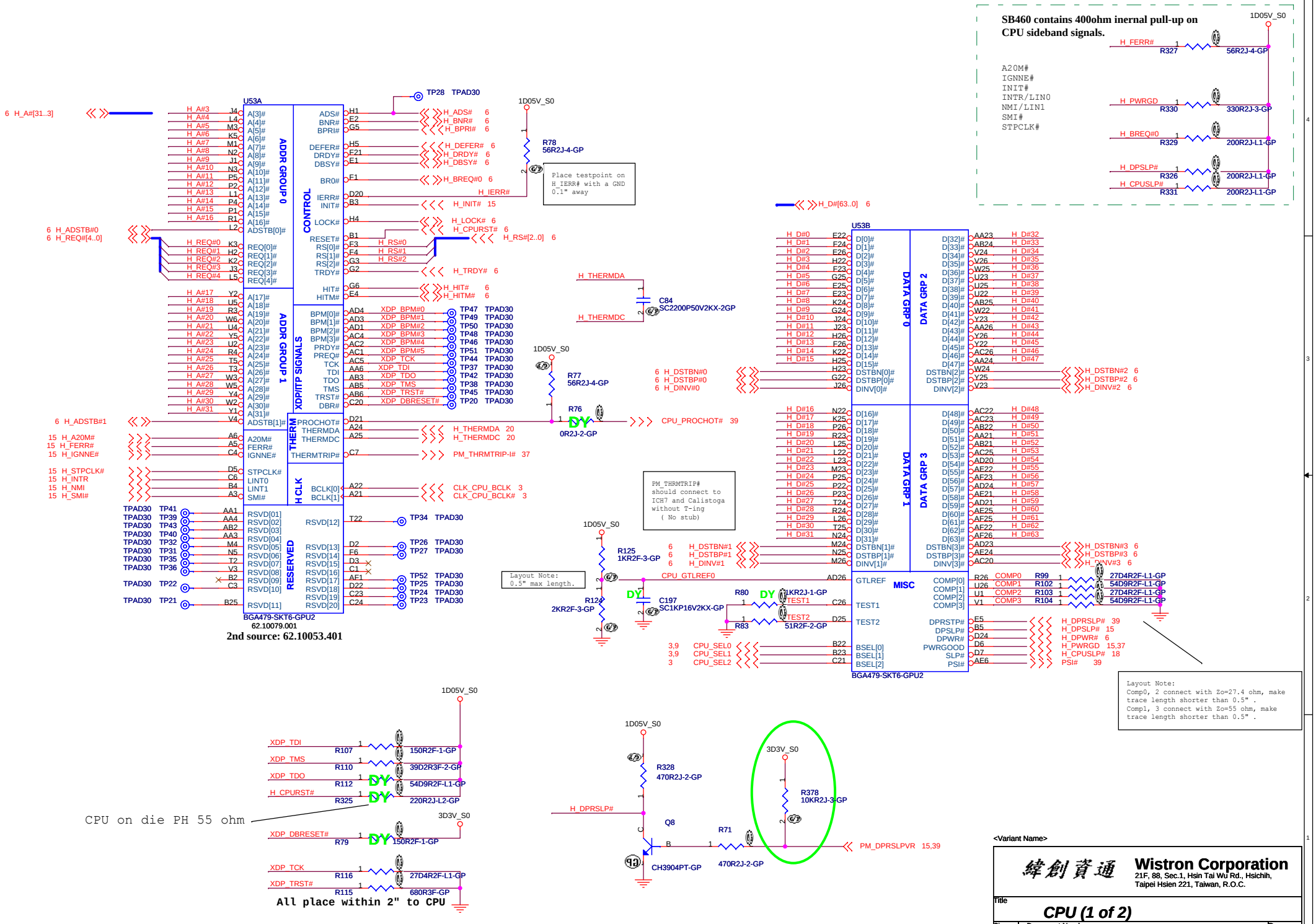
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator -ICS951413**

Size: A3 | Document Number: **Garda-5** | Rev: **SB**

Date: Wednesday, April 26, 2006 | Sheet 3 of 46



<Variant Name>

Wistron Corporation
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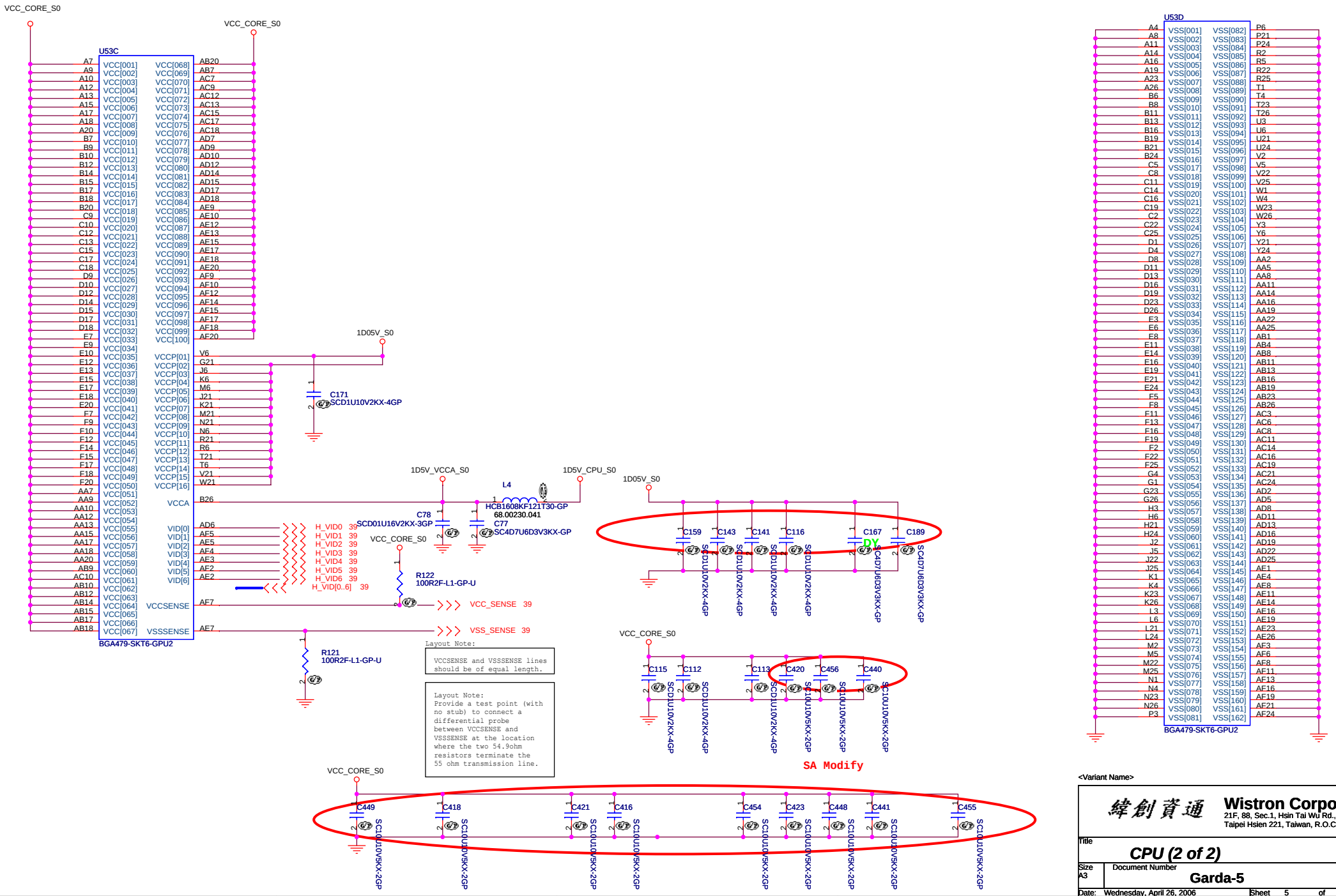
Title: CPU (1 of 2)

Size: A3 | Document Number: Garda-5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 4 of 46



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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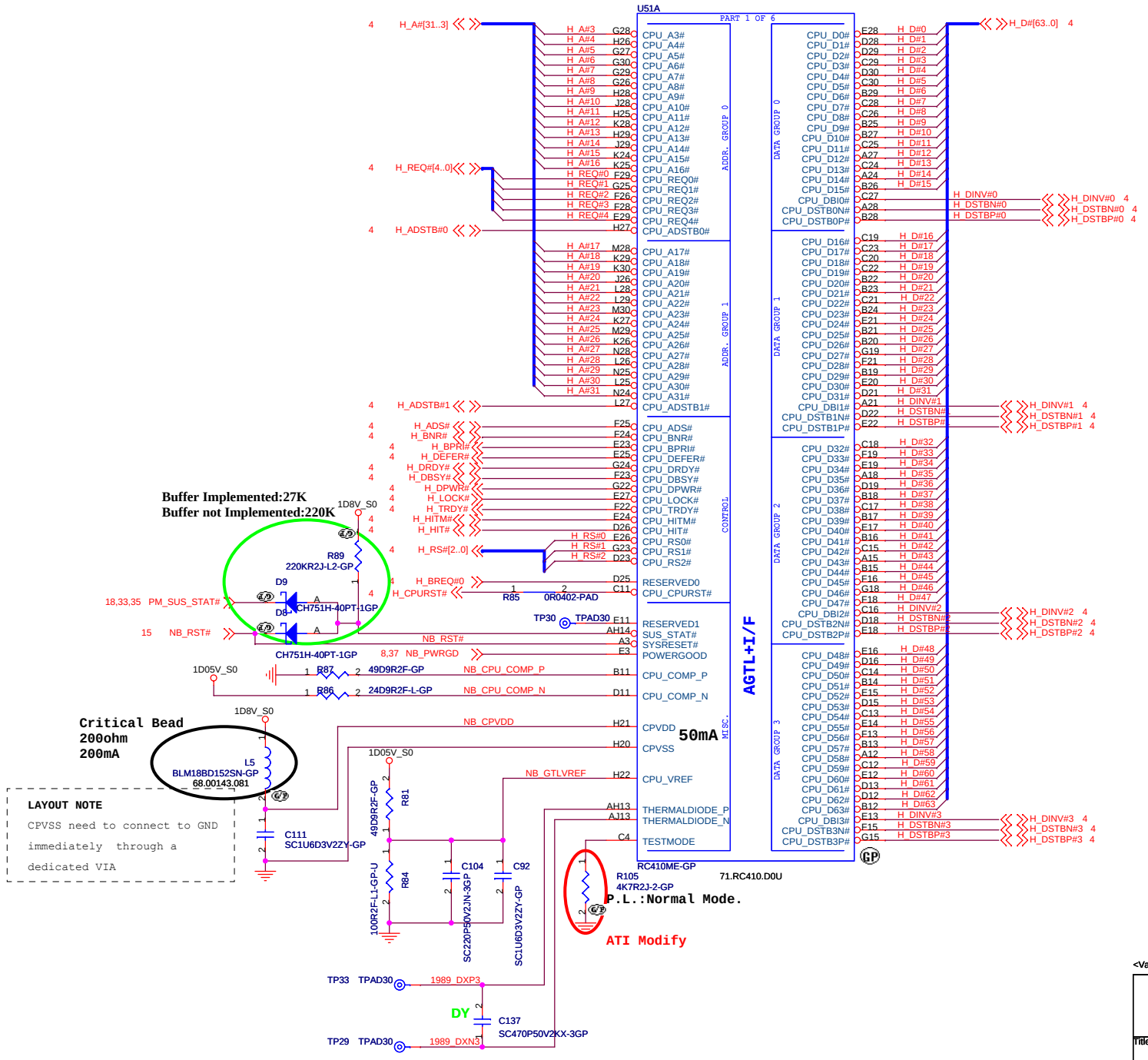
Title: **CPU (2 of 2)**

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 5 of 46



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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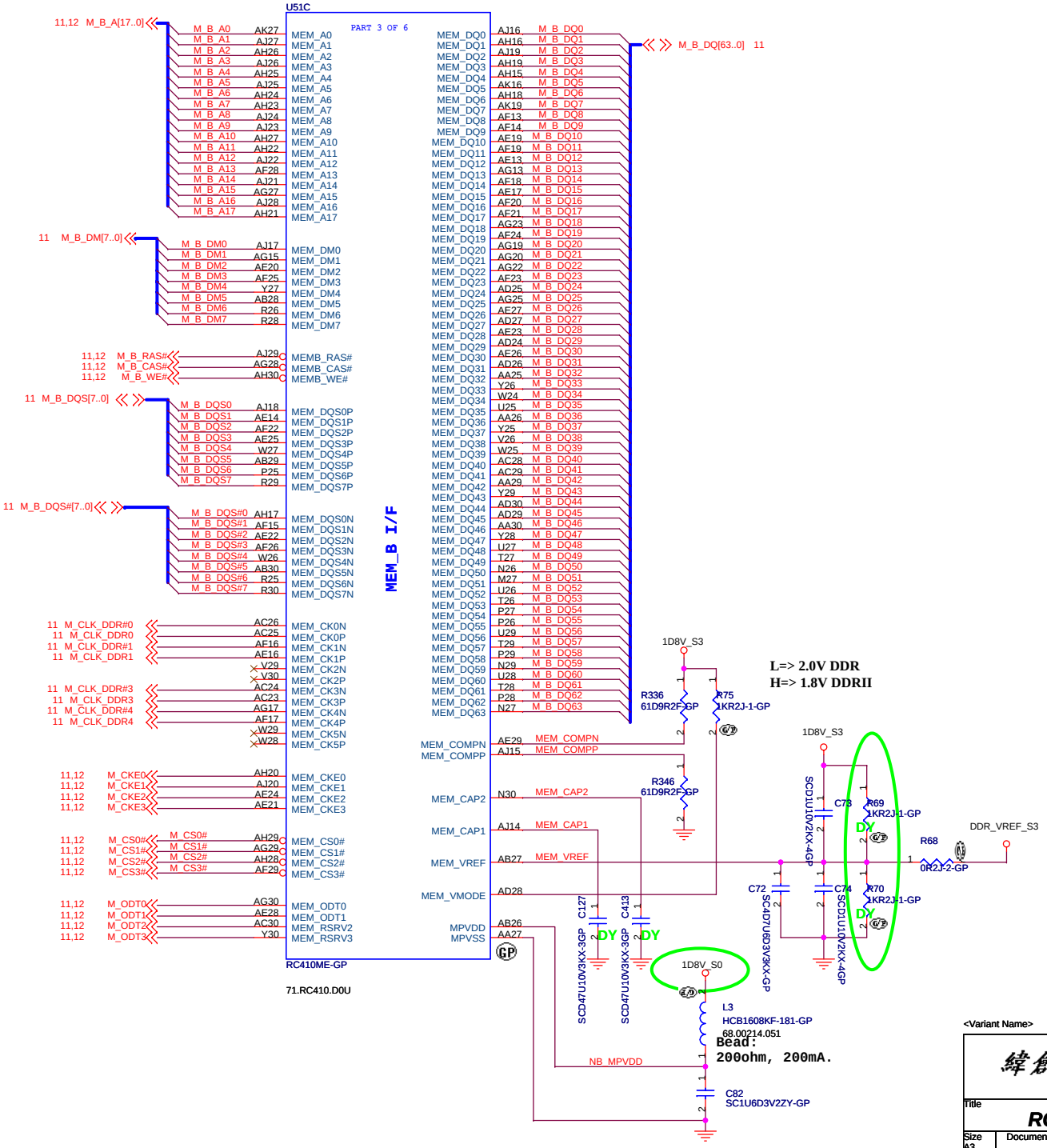
Title: ***RC410ME (1 of 5) Host I/F***

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 6 of 46



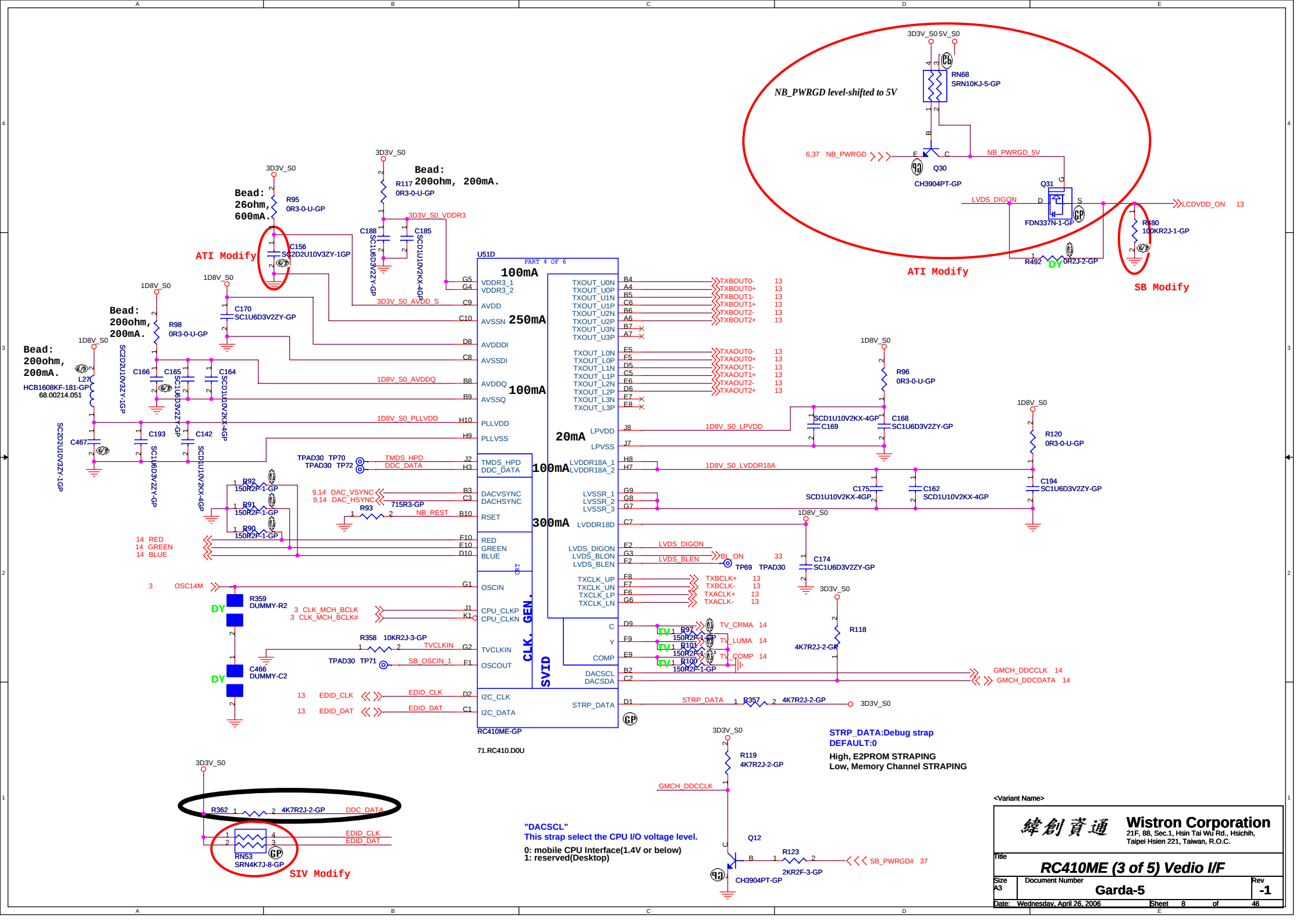
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RC410ME (2 of 5) Memory I/F***

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 7 of 46



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

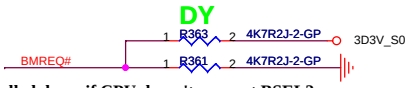
Title: **RC410ME (3 of 5) Vedio I/F**

Size	Document Number	Rev
A3	Garda-5	-1

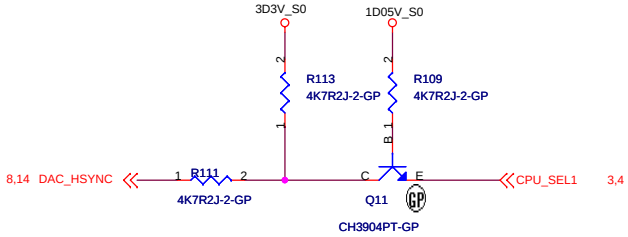
Date: Wednesday, April 26, 2006 Sheet 8 of 46

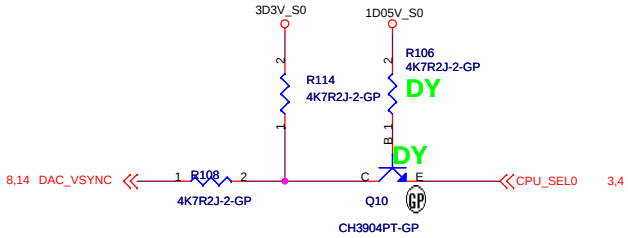
NB Strap pins

All pull-up and pull-down resistors are 4.7kohm.



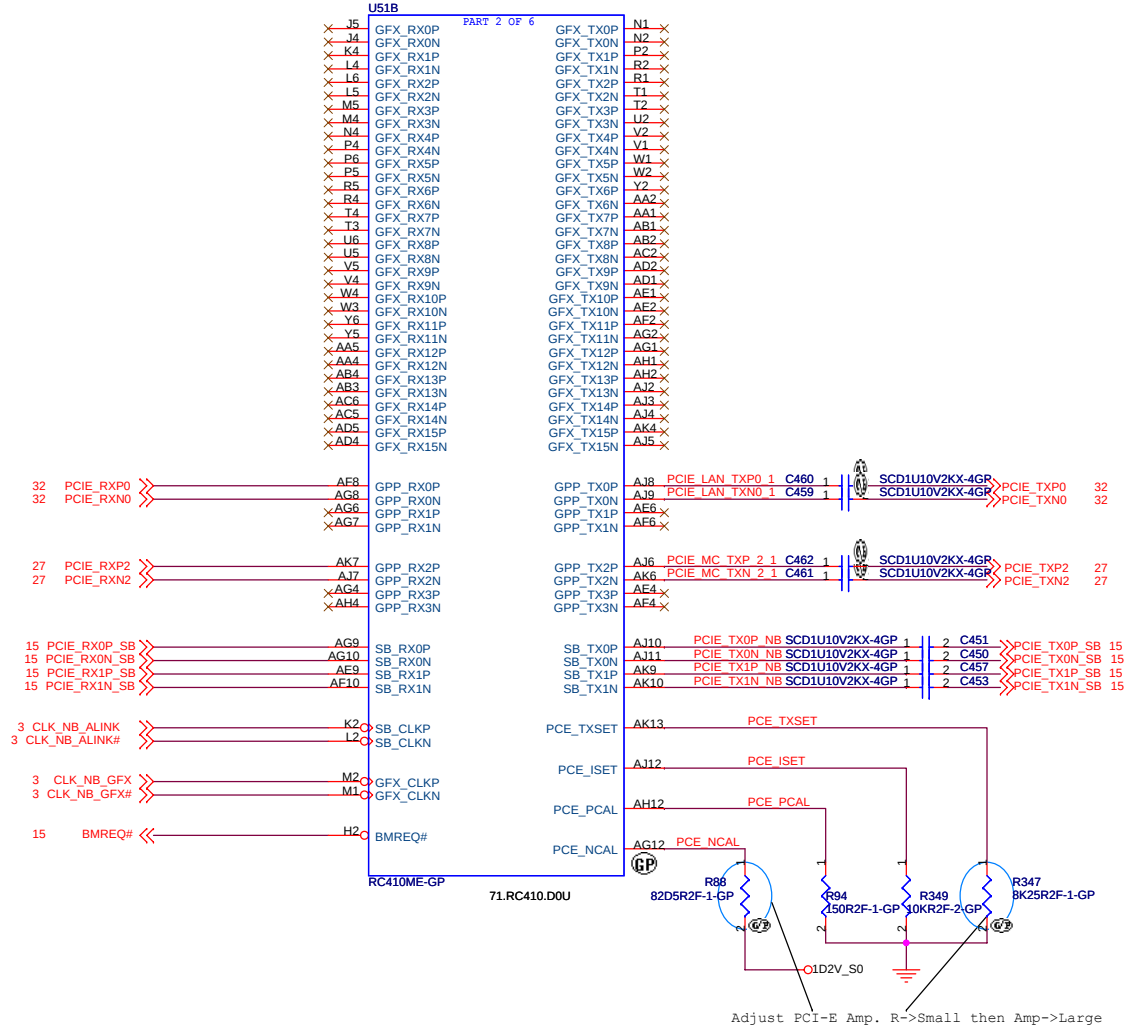
BMREQ# pulled down if CPU doesn't support BSEL2.





Select the FSB SPEED

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	------
0	1	1	166MHZ
1	0	0	100MHZ
1	0	1	100MHZ
1	1	0	------
1	1	1	------



<Variant Name>

緯創資通 Wistron Corporation
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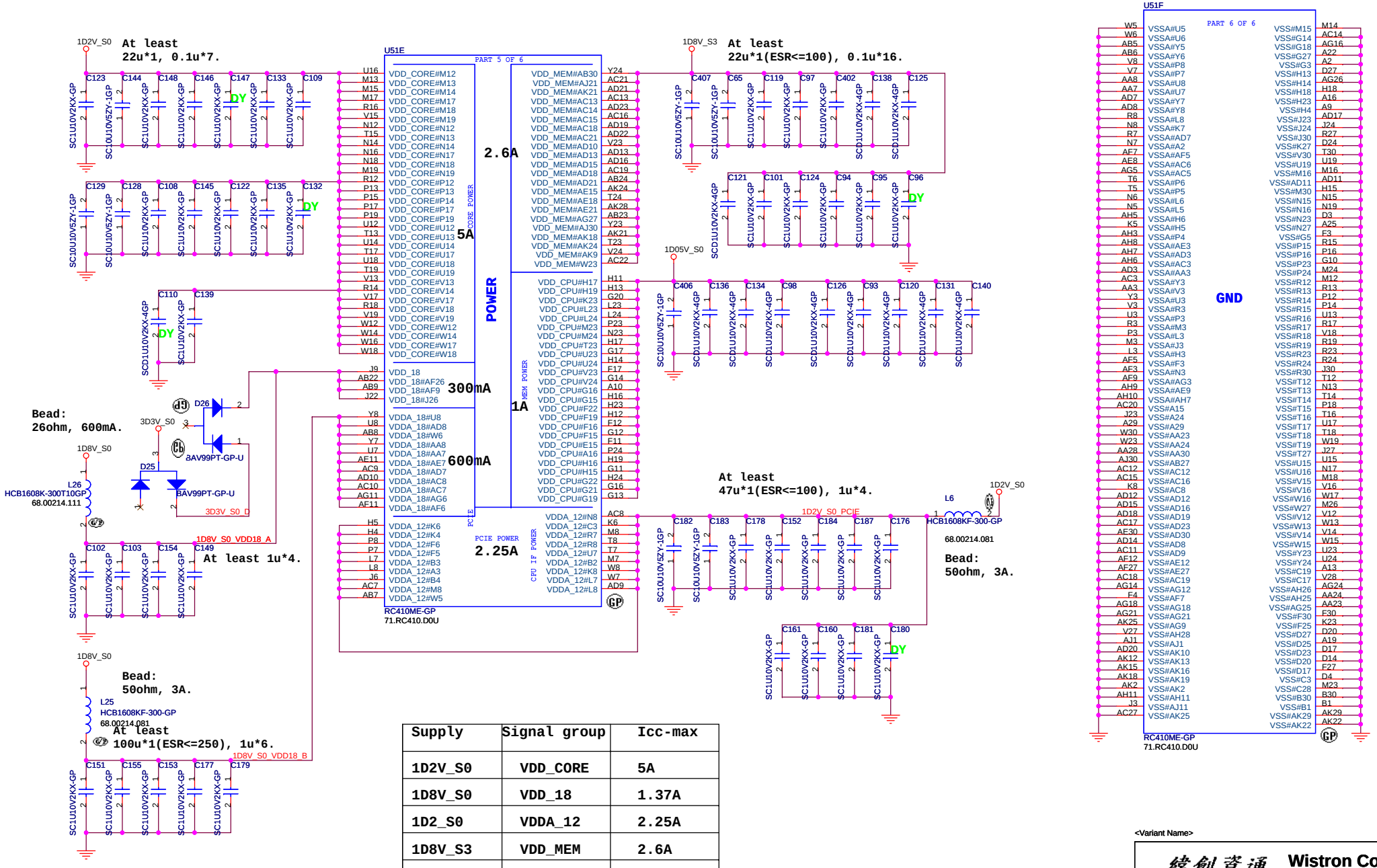
Title: **RC410ME (4 of 5) PCI-E & Strap**

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 9 of 46



Supply	Signal group	Icc-max
1D2V_S0	VDD_CORE	5A
1D8V_S0	VDD_18	1.37A
1D2_S0	VDDA_12	2.25A
1D8V_S3	VDD_MEM	2.6A
1D05V_S0	VDD_CPU	1A

<Variant Name>

緯創資通 Wistron Corporation
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Title: RC410ME (5 of 5) Power

Size: A3 | Document Number: Garda-5 | Rev: SA

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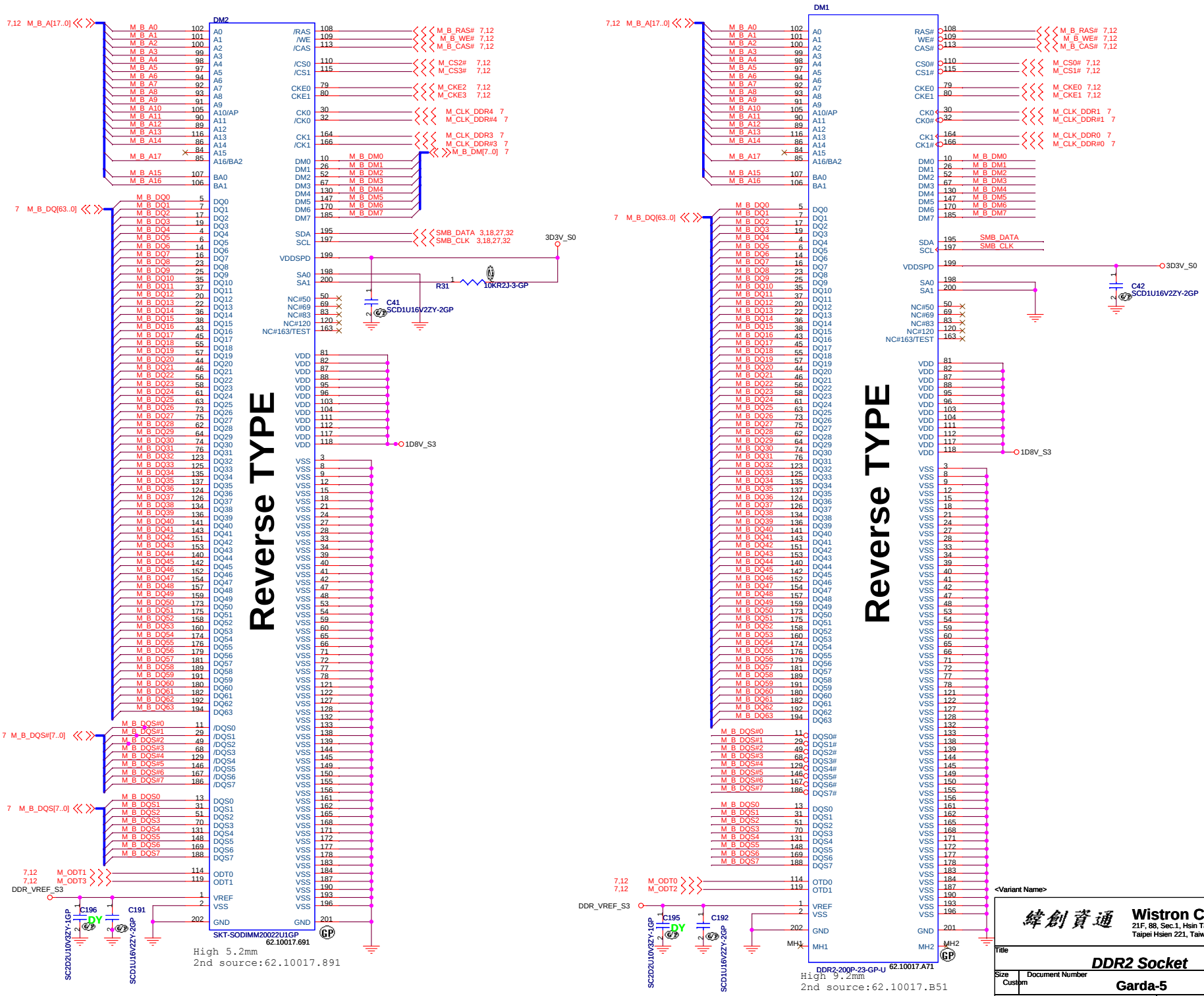

<Variant Name>

Wistron Corporation
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Title: DDR2 Socket

Size: Custom | Document Number: Garda-5 | Rev: SA

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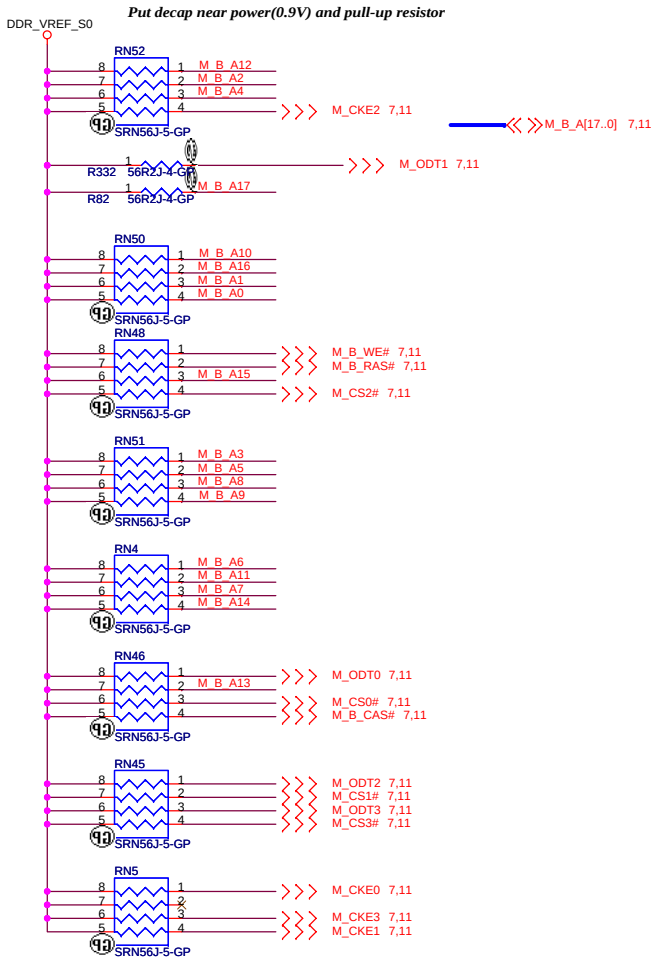
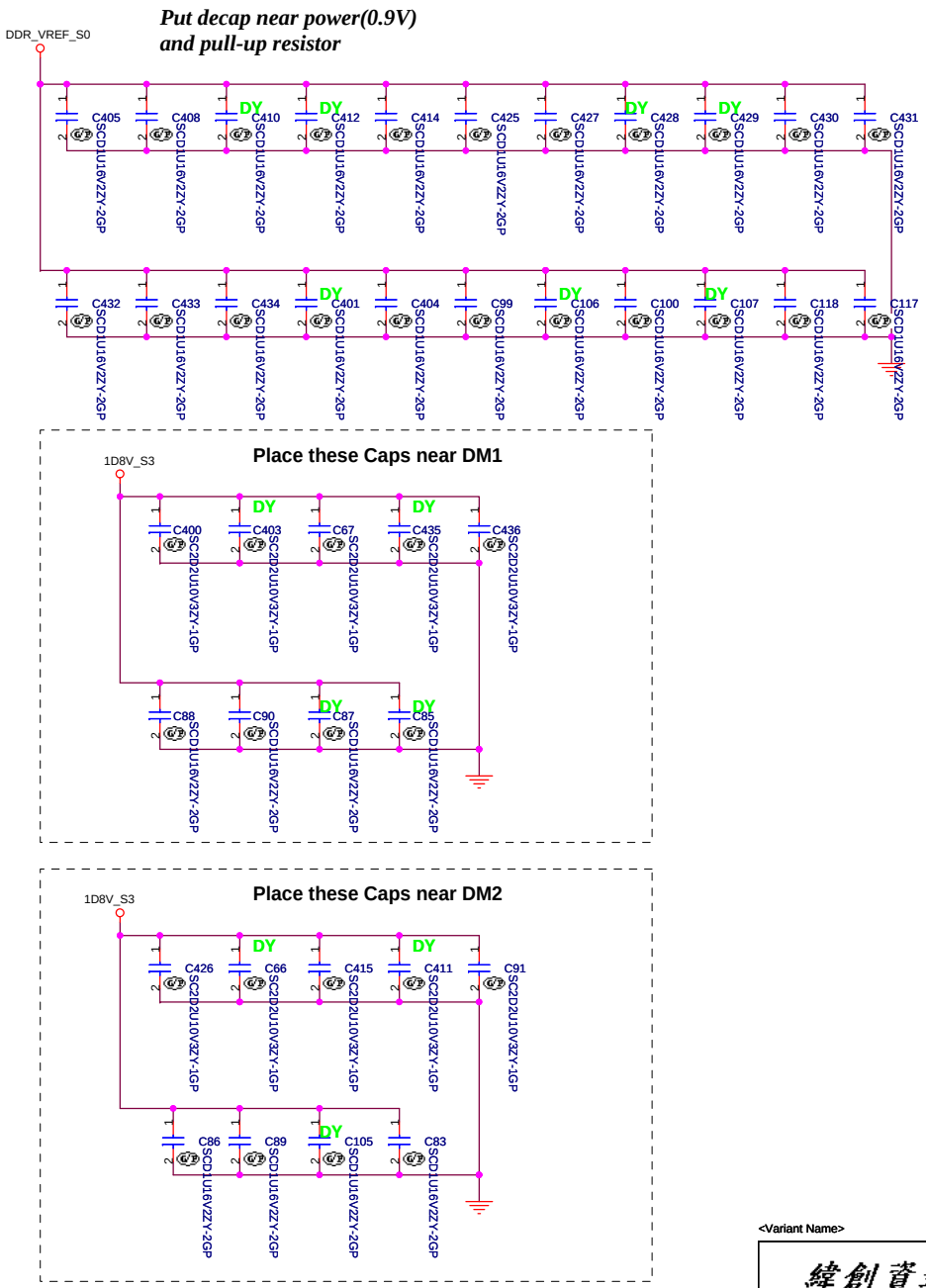
PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

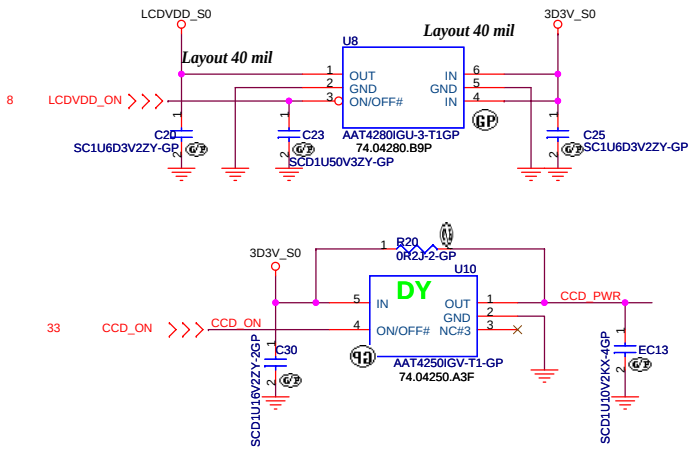
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR2 Termination Resistor***	
Size A3	Document Number **Garda-5**	Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 12 of 46	

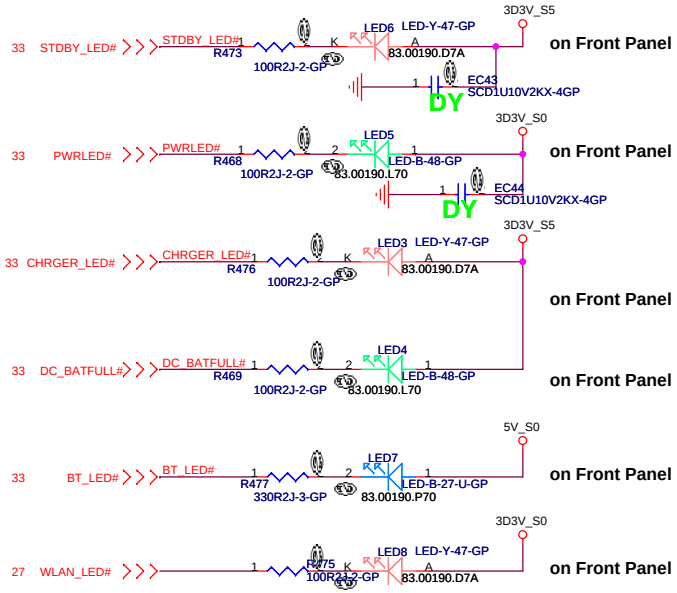
LCD/INVERTER/CCD CONN

CCD Pin	
Pin	Symbol
1	3.3V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN



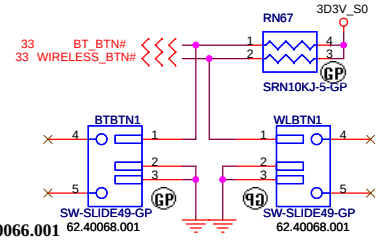


Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2



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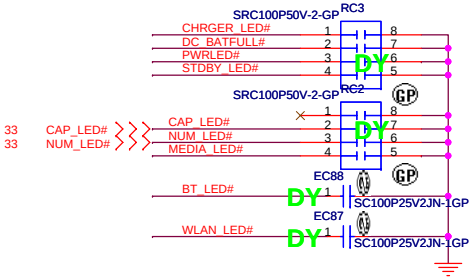
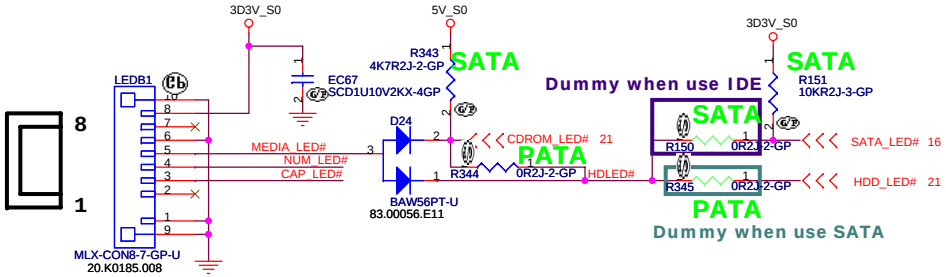
Edge Trigger



LED BD CONN



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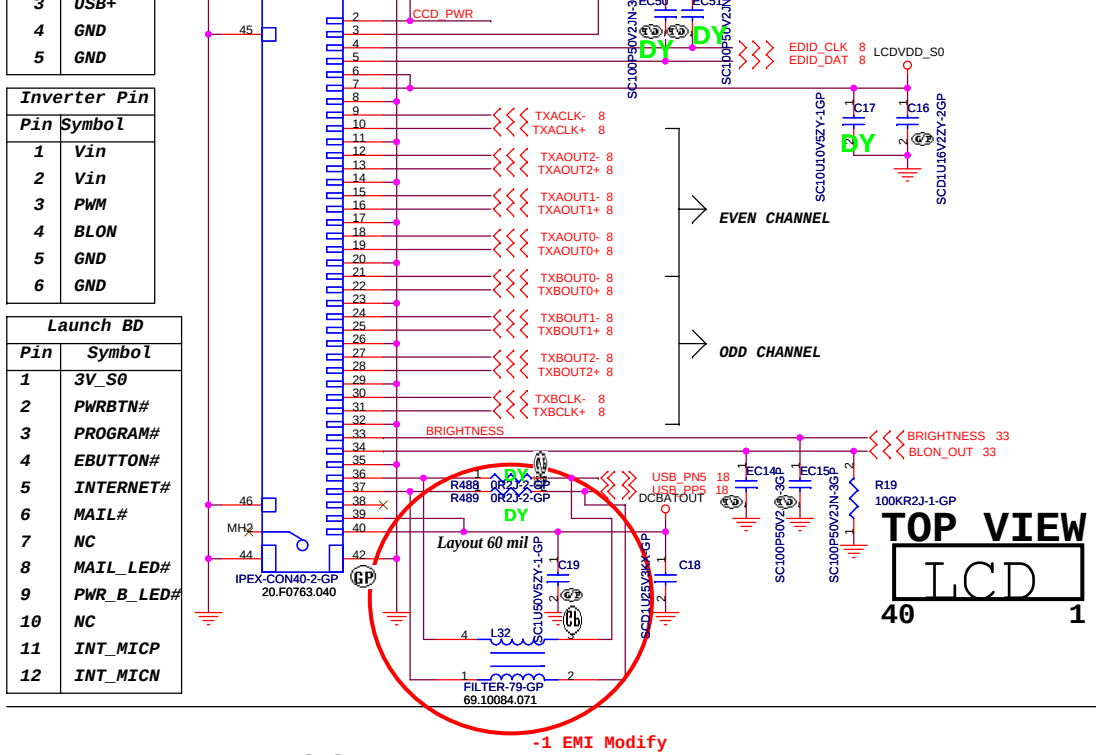

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<Variant Name>

Title: LCD / LAUNCH / LEDs

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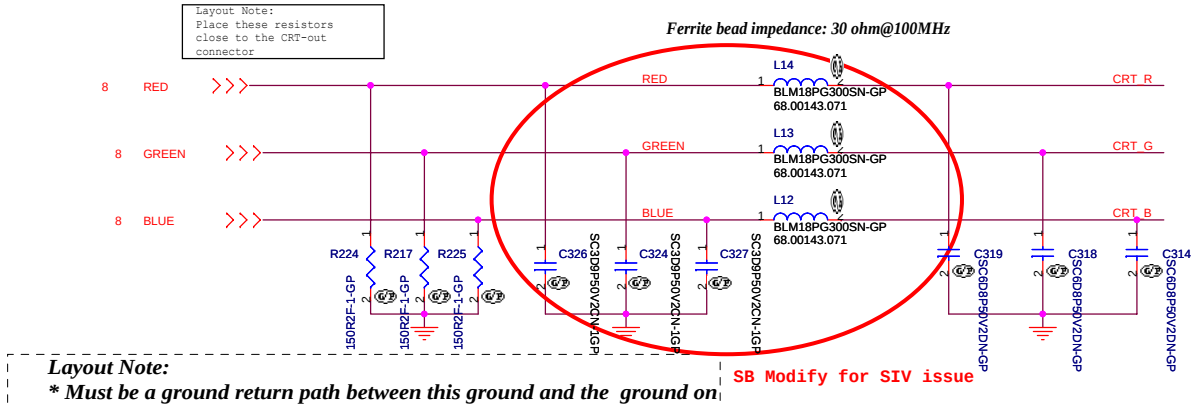
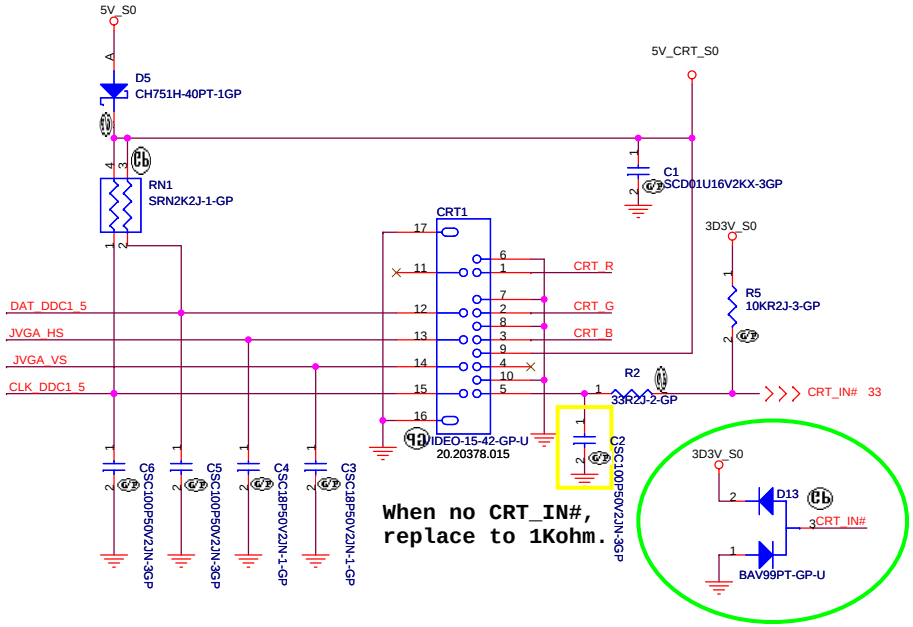
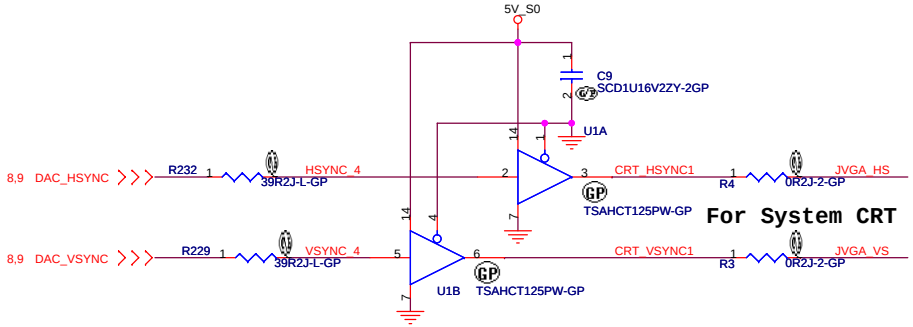
CRT I/F & CONNECTOR



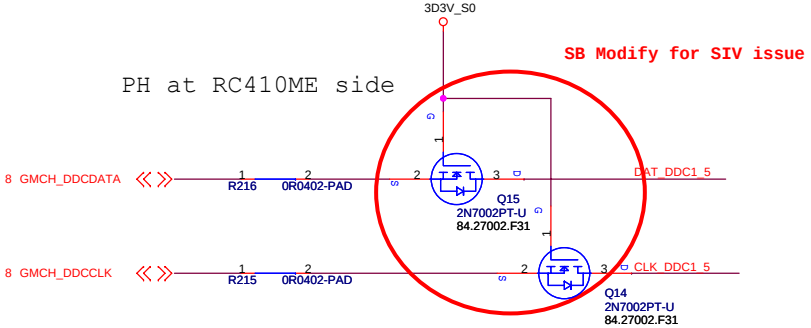
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



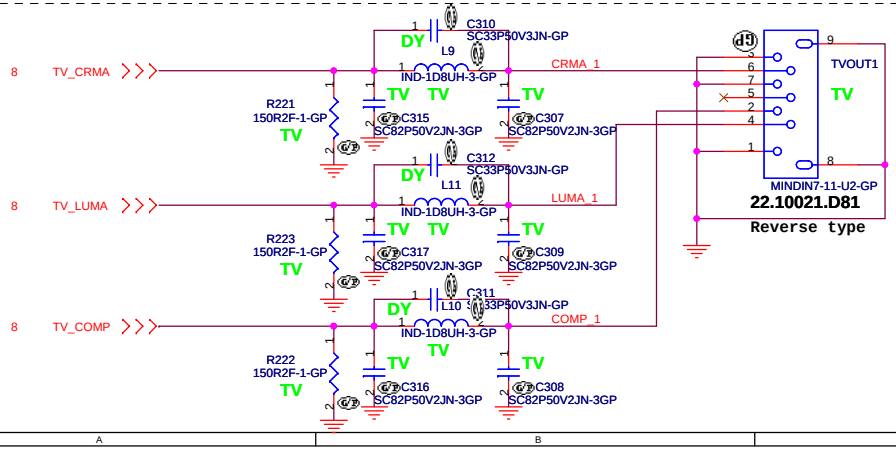
Hsync & Vsync level shift

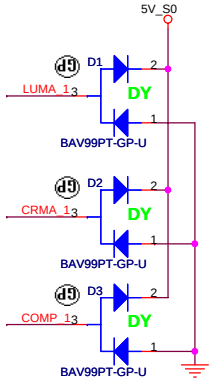


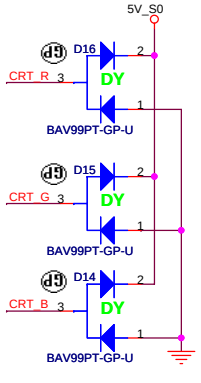
DDC_CLK & DATA level shift

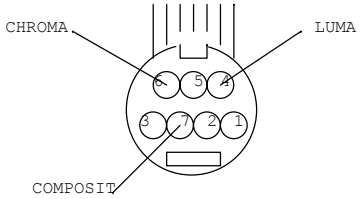


TV OUT CONN



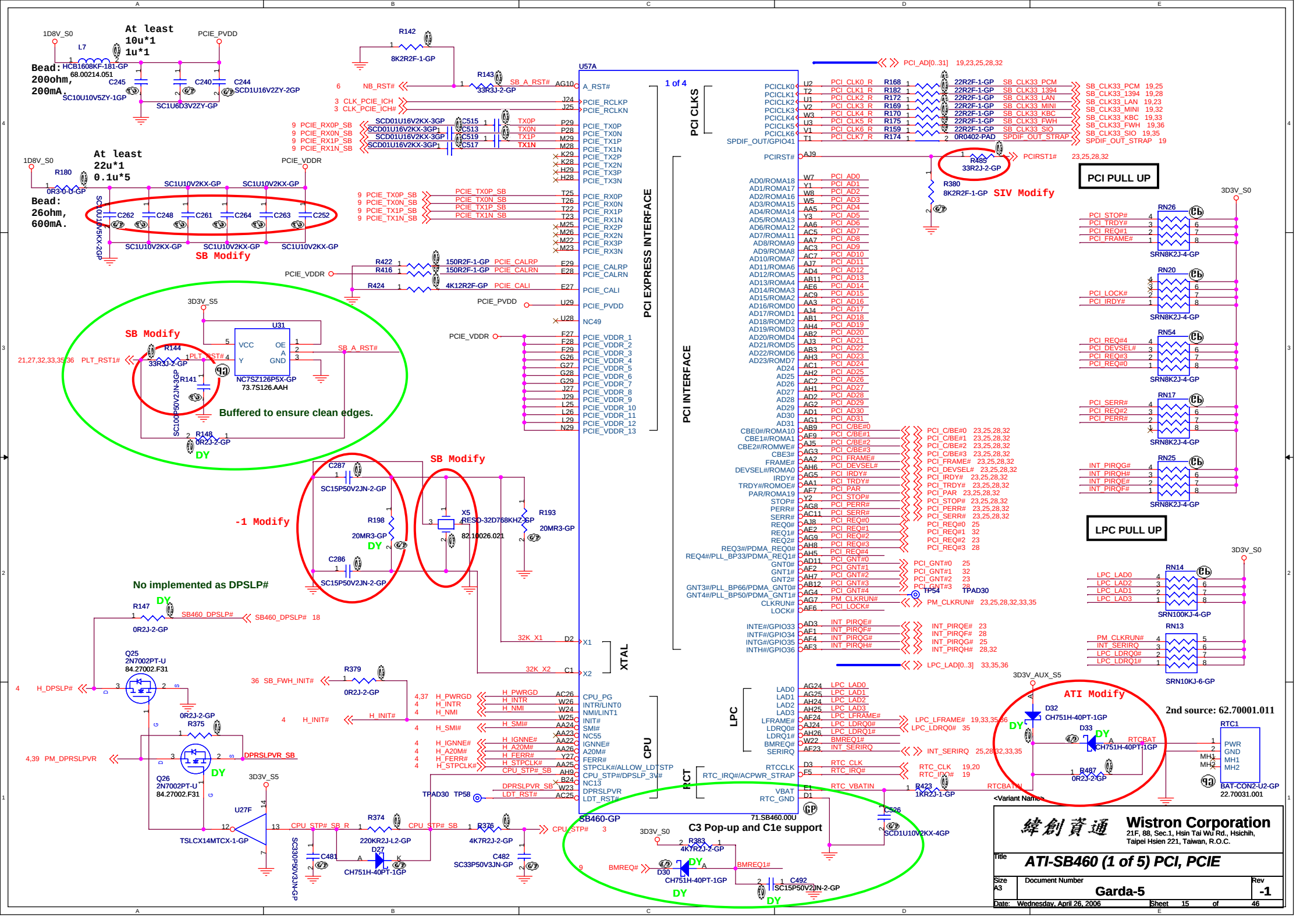




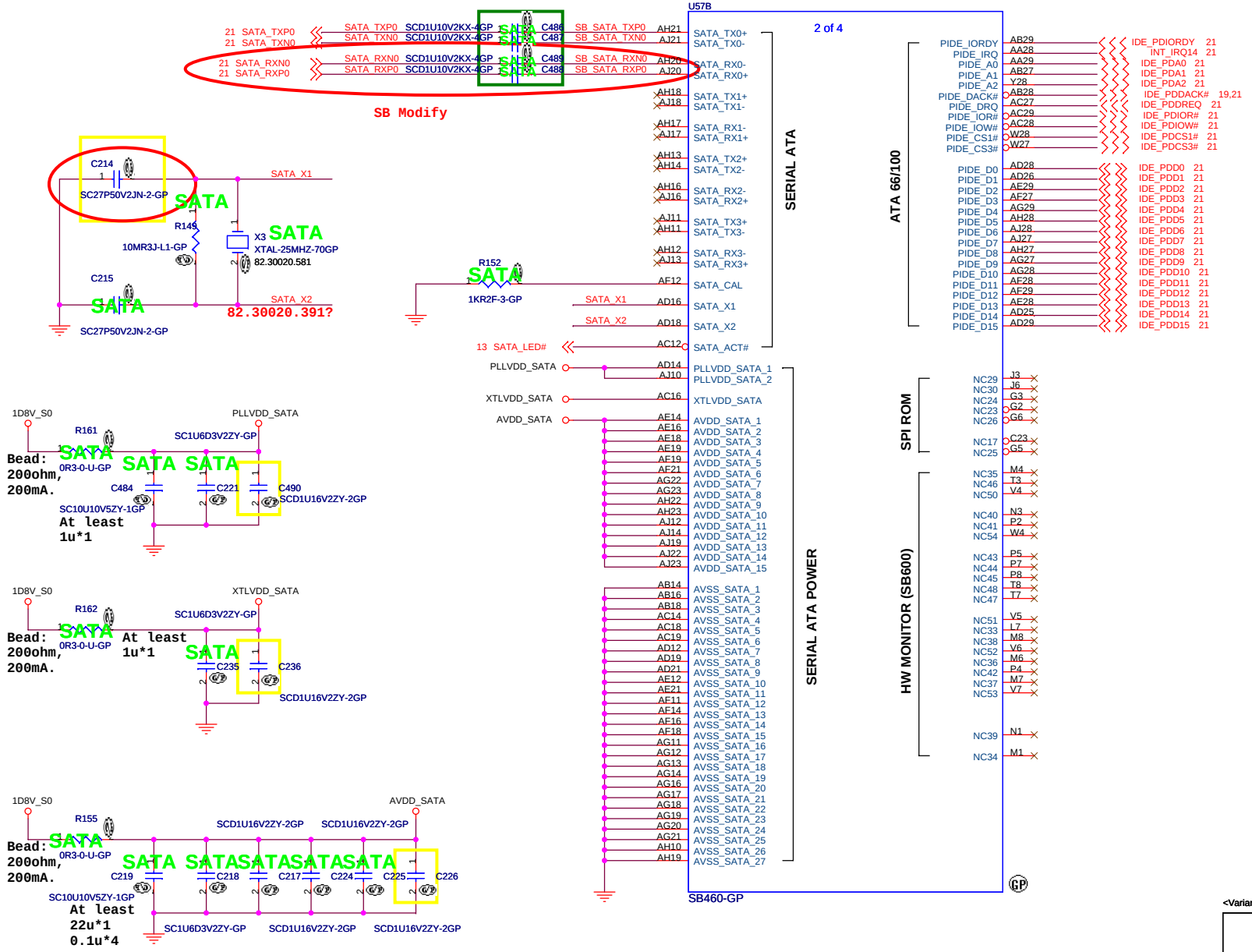


<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV Connector	
Size A3	Document Number Garda-5	Rev SB
Date: Wednesday, April 26, 2006	Sheet 14 of 46	


At least 10u*1 1u*1
Bead: 200ohm, 200mA
At least 22u*1 0.1u*5
Bead: 26ohm, 600mA.
SB Modify
Buffered to ensure clean edges.
-1 Modify
No implemented as DPSLP#
U57A
1 of 4
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
CPU
RCT
LPC
SB460-GP
71.SB460.00U
C3 Pop-up and C1e support
PCI PULL UP
LPC PULL UP
SIV Modify
ATI Modify
2nd source: 62.70001.011
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-SB460 (1 of 5) PCI, PCIE
Size A3
Document Number
Garda-5
Rev -1
Date: Wednesday, April 26, 2006
Sheet 15 of 46

When no SATA replace to 0 ohm.



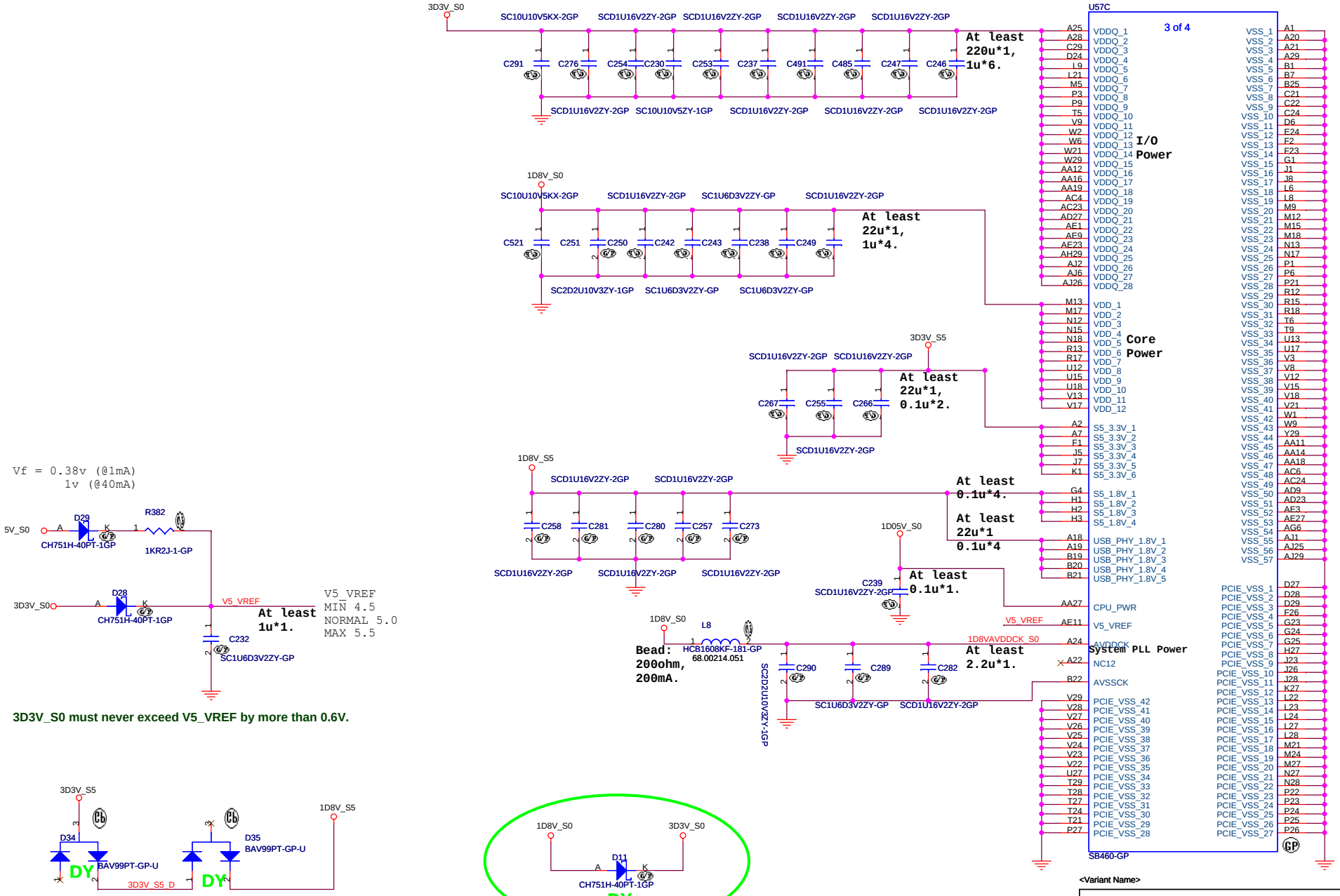
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATI-SB460 (2 of 5) IDE/SATA***

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 16 of 46



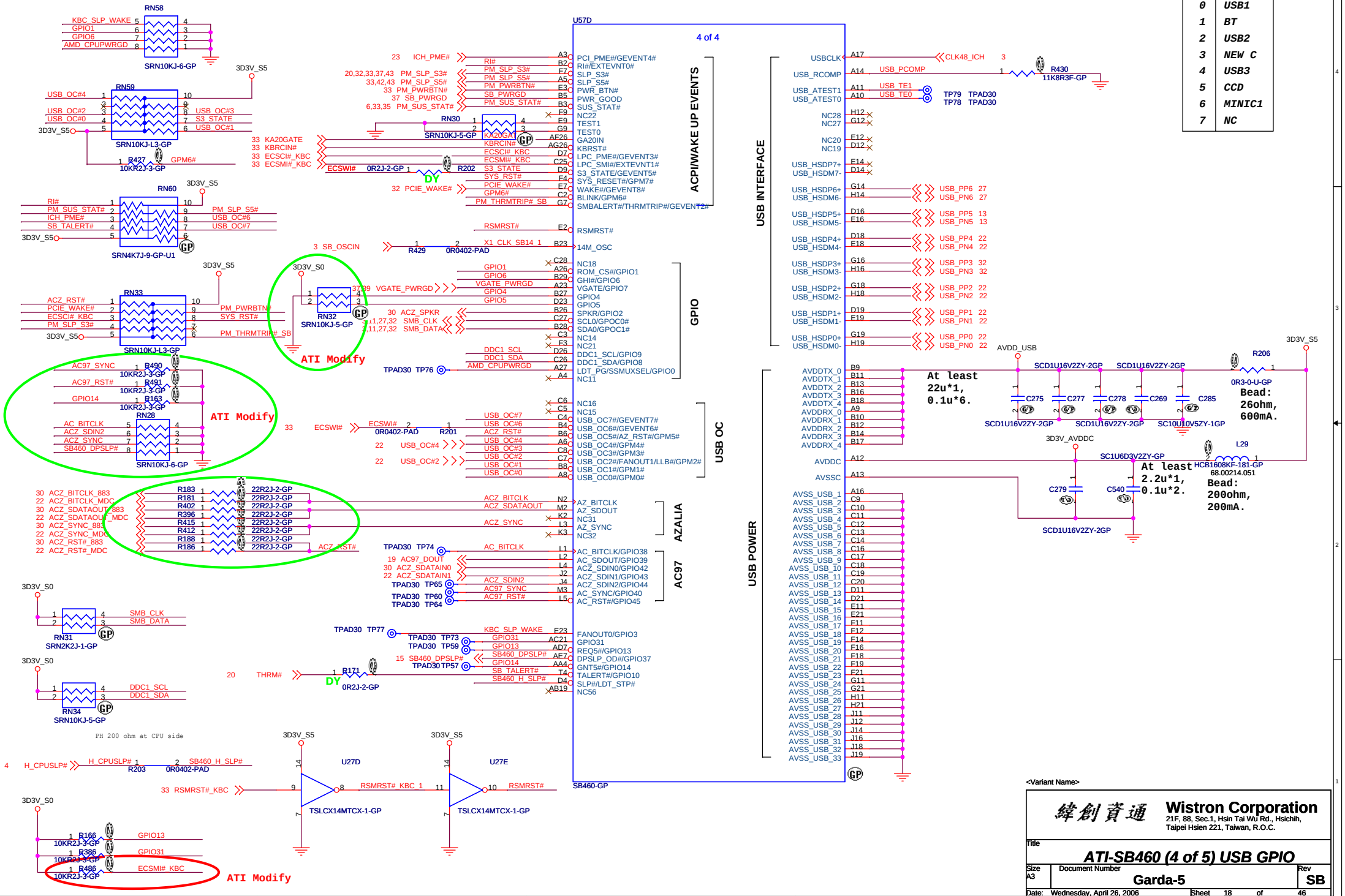
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATI-SB460 (3 of 5) POWER***

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 17 of 46



USB	
Pair	Device
0	USB1
1	BT
2	USB2
3	NEW C
4	USB3
5	CCD
6	MINIC1
7	NC

<Variant Name>

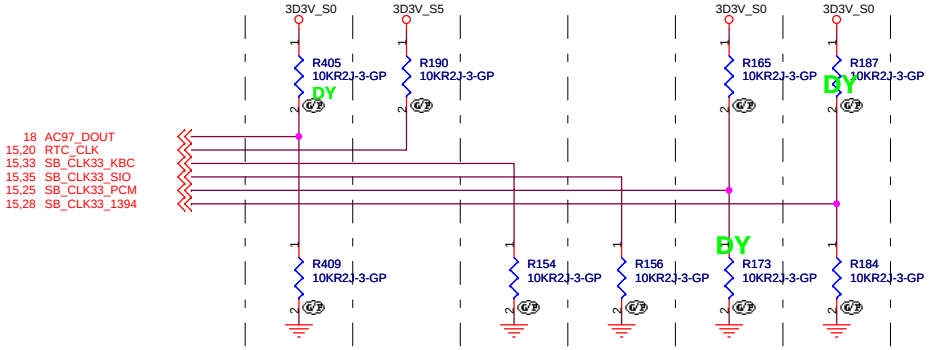
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

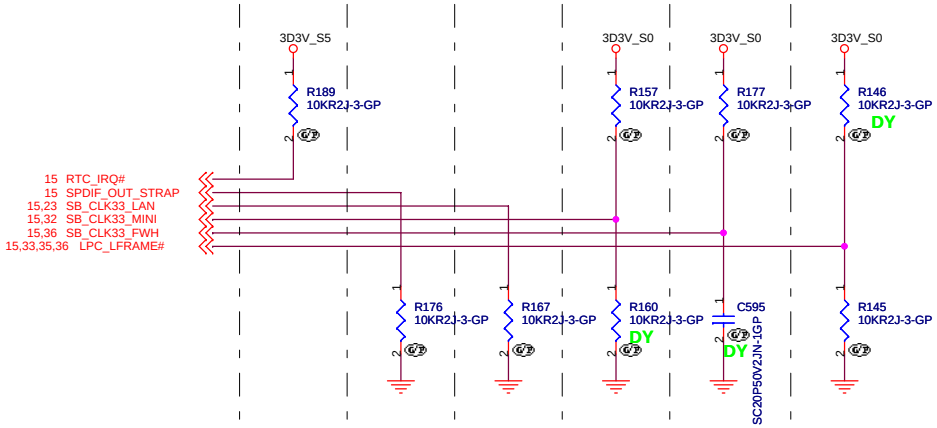
Title: ATI-SB460 (4 of 5) USB GPIO

Size: A3 | Document Number: Garda-5 | Rev: SB

Date: Wednesday, April 26, 2006 | Sheet 18 of 46

REQUIRED STRAPS





PCI_CLK0	PCM
PCI_CLK1	IEEE1394
PCI_CLK2	LAN
PCI_CLK3	MINI
PCI_CLK4	KBC
PCI_CLK5	FWH
PCI_CLK6	SIO
PCI_CLK7	SPDIFOUT

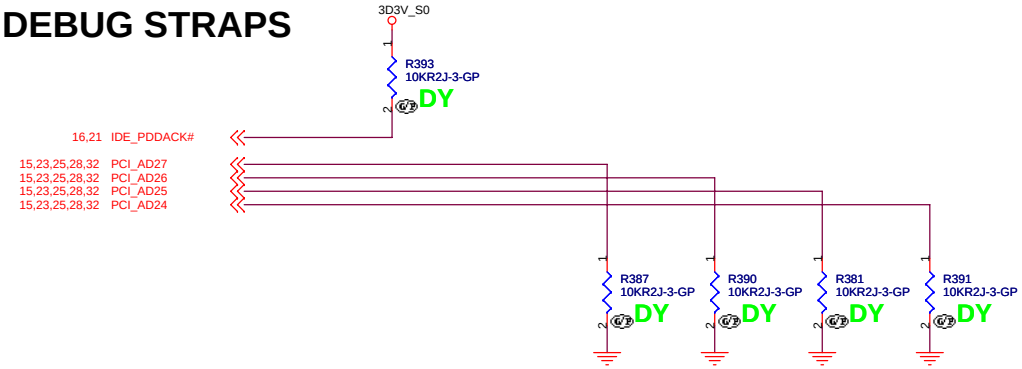
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB460 PCI_CLK0	SB460 PCI_CLK1	SB600 PCI_CLK0	SB600 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. USB PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM DEFAULT; L, H = LPC II ROM; L, L = FWH ROM; NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]		ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM	
PULL LOW	DISABLE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. USB 48MHZ SOURCE DEFAULT	CPU IF=P4 DEFAULT				

Require upper 12 addr bits set to "1".

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	48M XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE LANE AUTO DETECT DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE LANE FORCING TO 2 LANES DEBUG ONLY	DISABLE THERMTRIP#

USB wake from S5 supported.

DEBUG STRAPS



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY SB600 ONLY SB600 ONLY

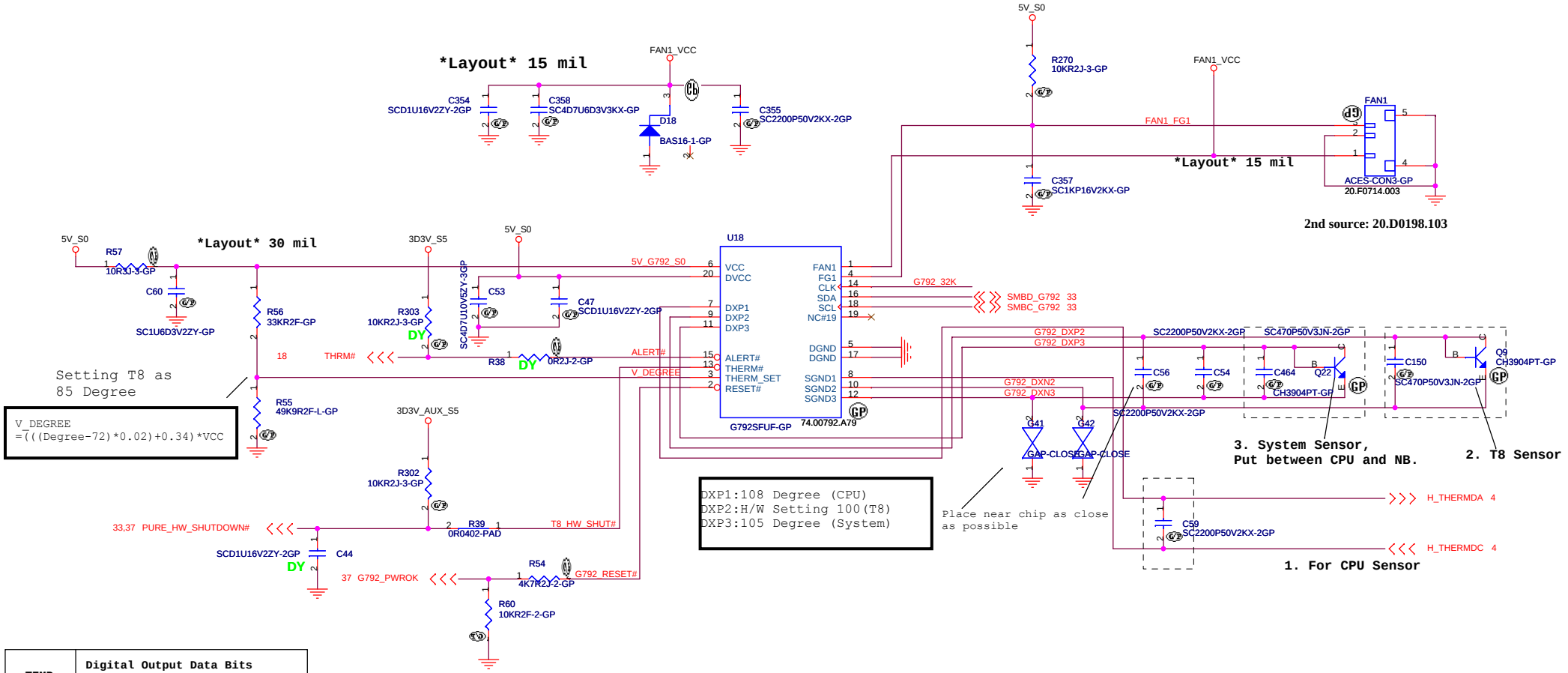
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB460 (5 of 5) STRAPPING

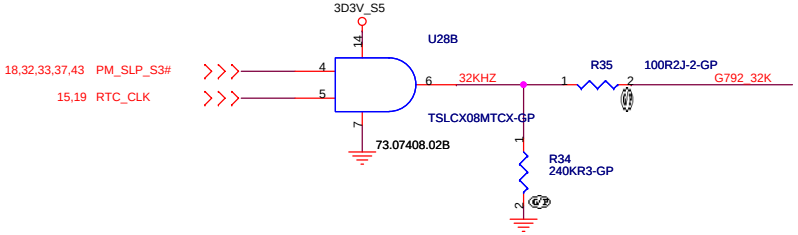
Size: A3 | Document Number: Garda5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 19 of 46



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

32K suspend clock output



<Variant Name>

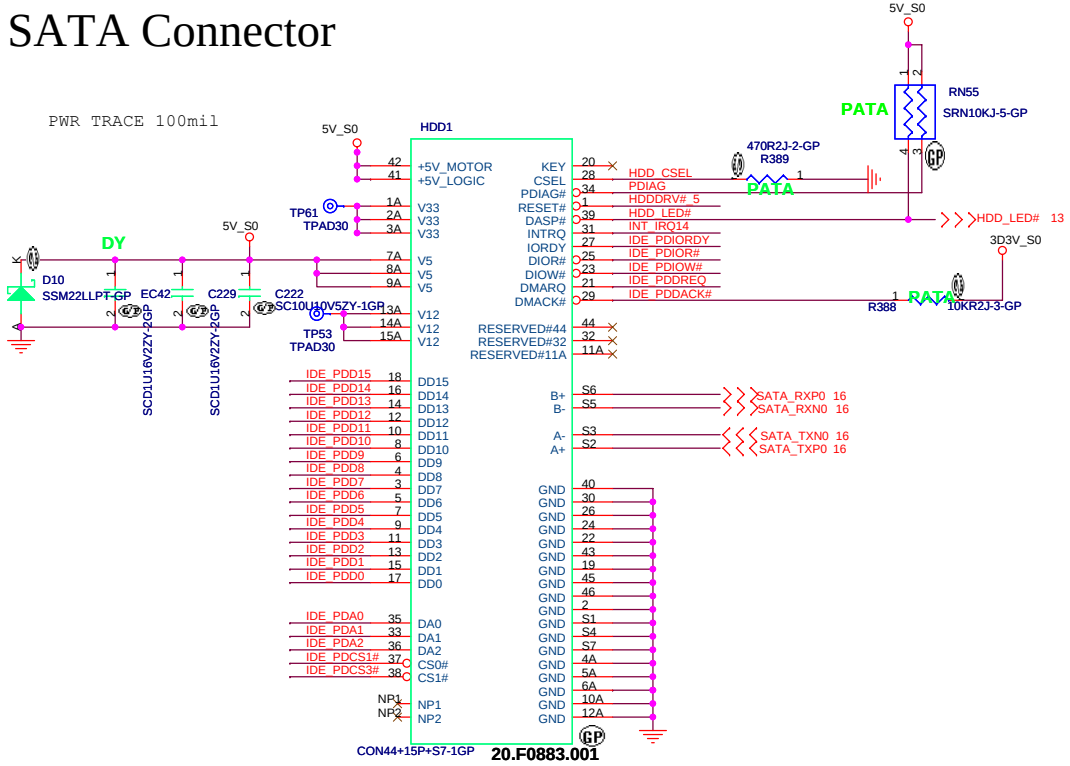
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controllor G792**

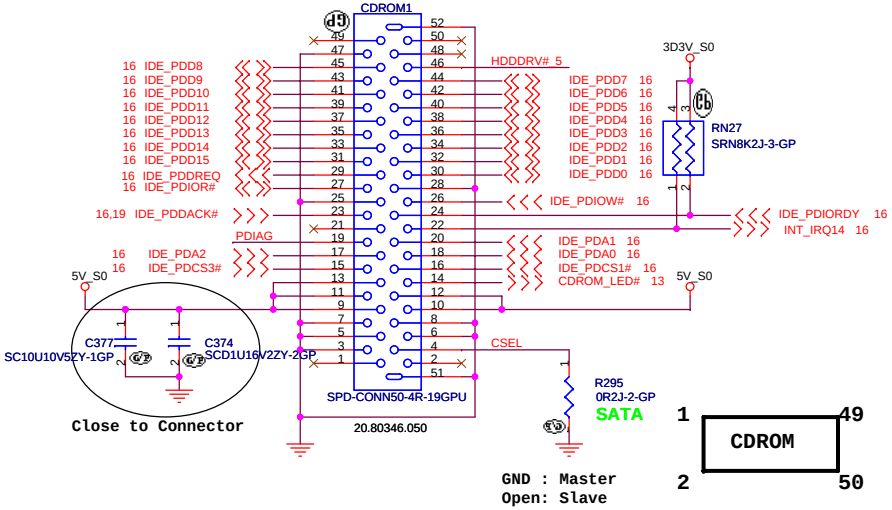
Size: Custom | Document Number: Garda-5 | Rev: SA

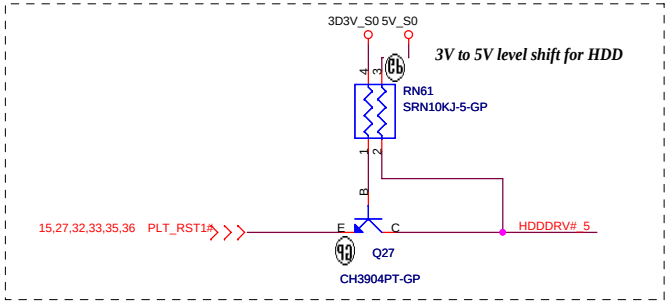
Date: Wednesday, April 26, 2006 | Sheet 20 of 46

SATA Connector



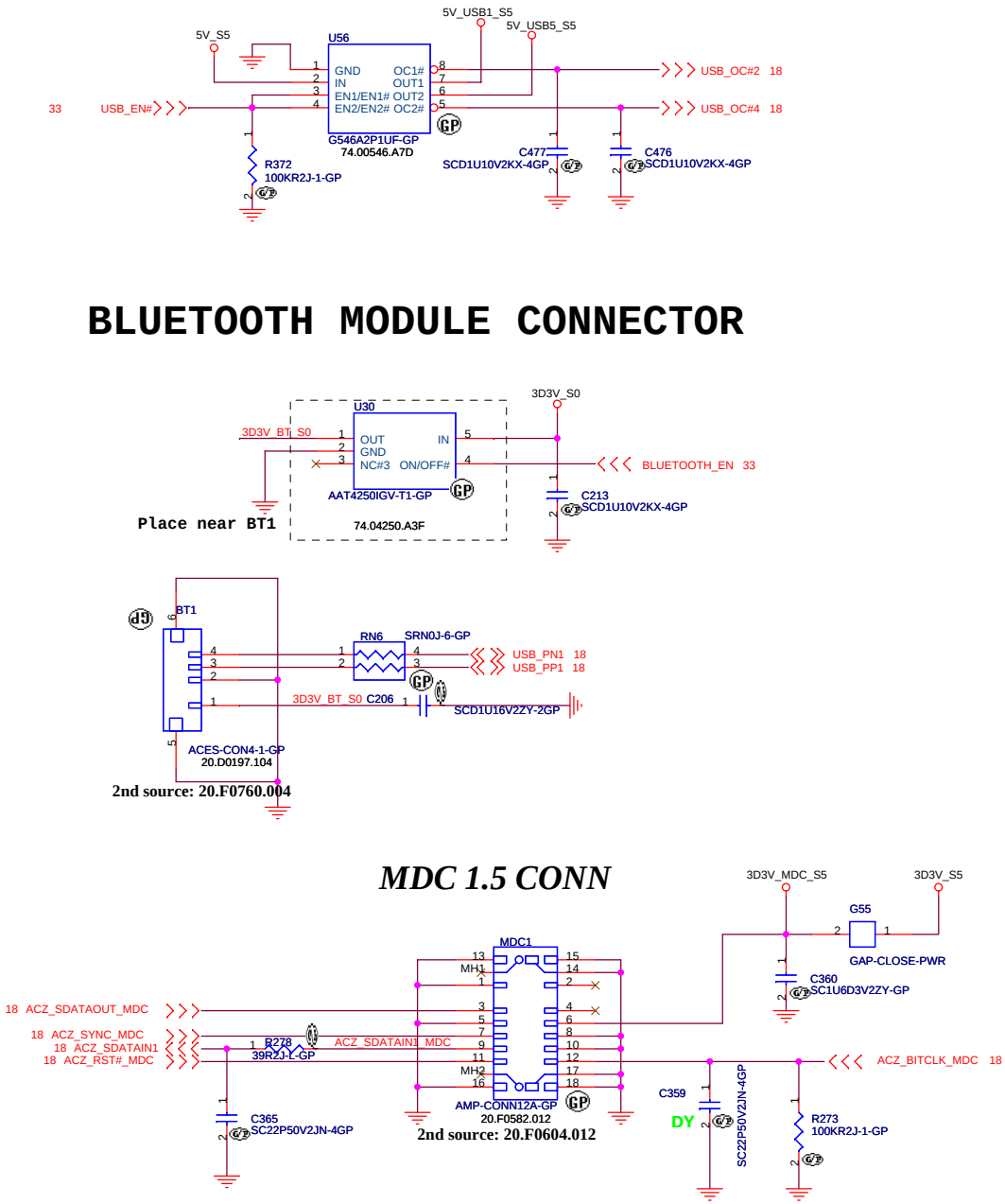
CDROM Connector





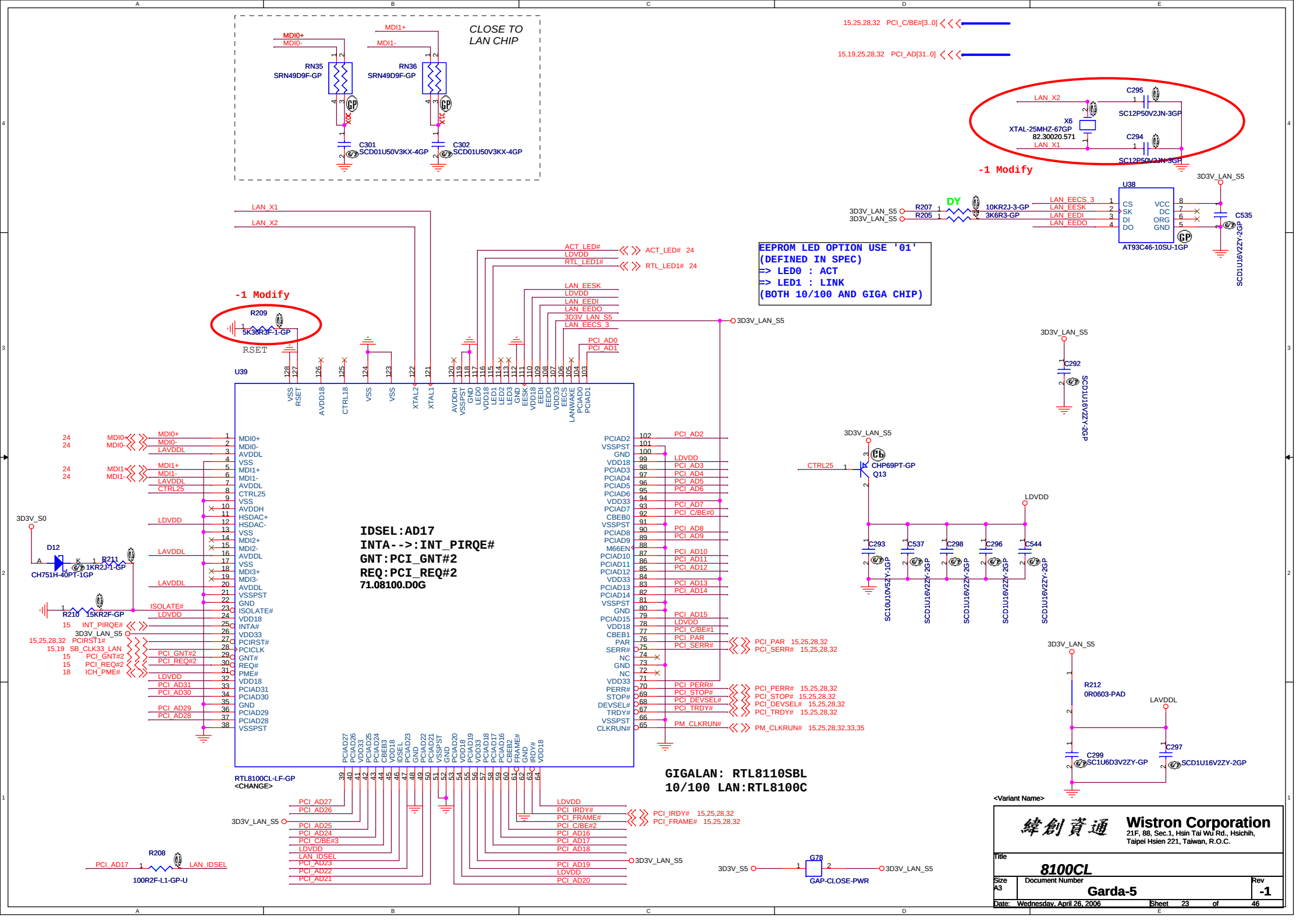
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SATA/PATA HDD / ODD	
Size A3	Document Number Garda-5	Rev SA
Date: Wednesday, April 26, 2006	Sheet 21 of 46	

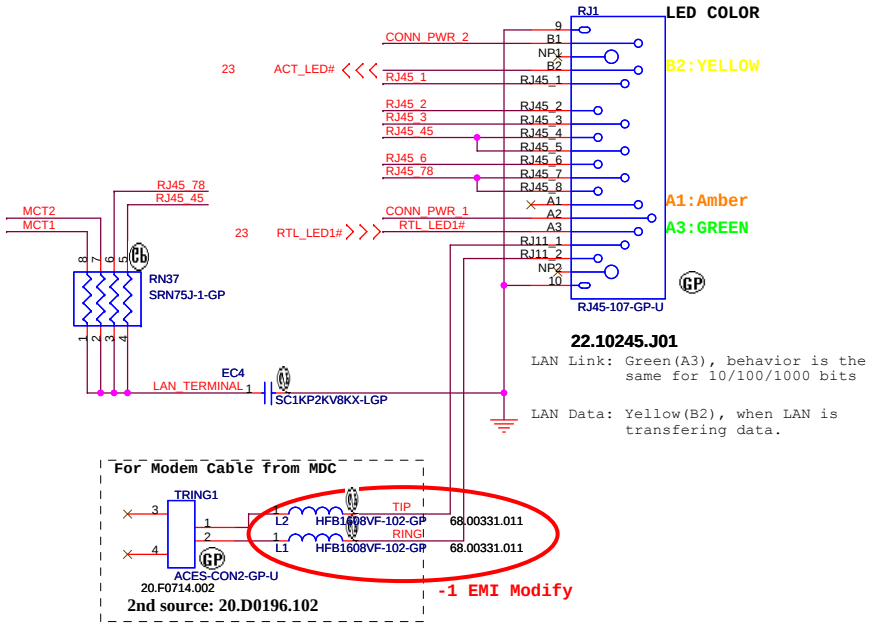


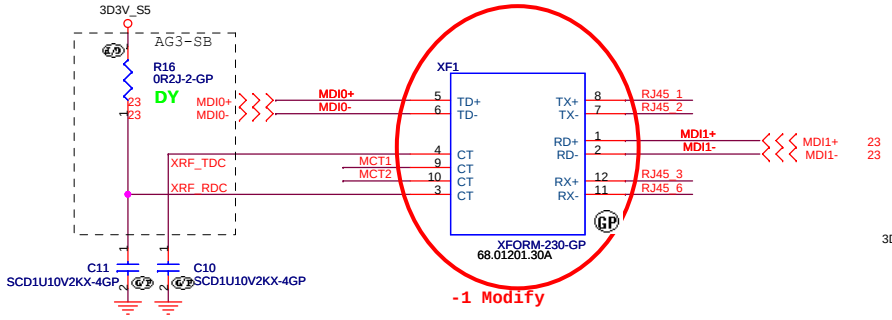
<Variant Name>

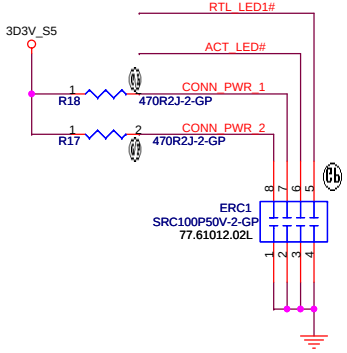
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB and MDC I/F***	
Size A3	Document Number **Garda-5**	Rev **-1**
Date: Wednesday, April 26, 2006	Sheet 22 of 46	


CLOSE TO LAN CHIP
RN35 SRN49D9F-GP
RN36 SRN49D9F-GP
C301 SCD01U50V3KX-4GP
C302 SCD01U50V3KX-4GP
15,25,28,32 PCI_C/BE#[3..0]
15,19,25,28,32 PCI_AD[31..0]
X6 XTAL-25MHZ-67GP 82.30020.571
C295 SC12P50V2JN-3GP
C294 SC12P50V2JN-3GP
-1 Modify
U38 AT93C46-10SU-1GP
R207 10KR2J-3-GP
R205 3K6R3-GP
DY
C535 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
-1 Modify
R209 5K36R3F-1-GP
RSET
U39
IDSEL:AD17
INTA-->:INT_PIRQE#
GNT:PCI_GNT#2
REQ:PCI_REQ#2
71.08100.D0G
RTL8100CL-LF-GP
<CHANGE>
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
C292 SCD1U16V2ZY-2GP
Q13 CHP69PT-GP
C293 SC10U10V5ZY-1GP
C537 SCD1U16V2ZY-2GP
C298 SCD1U16V2ZY-2GP
C296 SCD1U16V2ZY-2GP
C544 SCD1U16V2ZY-2GP
D12 CH751H-40PT-1GP
R211 1KR2J-1-GP
R210 15KR2F-GP
R212 0R0603-PAD
C299 SC1U6D3V2ZY-GP
C297 SCD1U16V2ZY-2GP
R208 100R2F-L1-GP-U
G78 GAP-CLOSE-PWR
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 8100CL
Size A3
Document Number Garda-5
Rev -1
Date: Wednesday, April 26, 2006
Sheet 23 of 46

LAN Connector







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

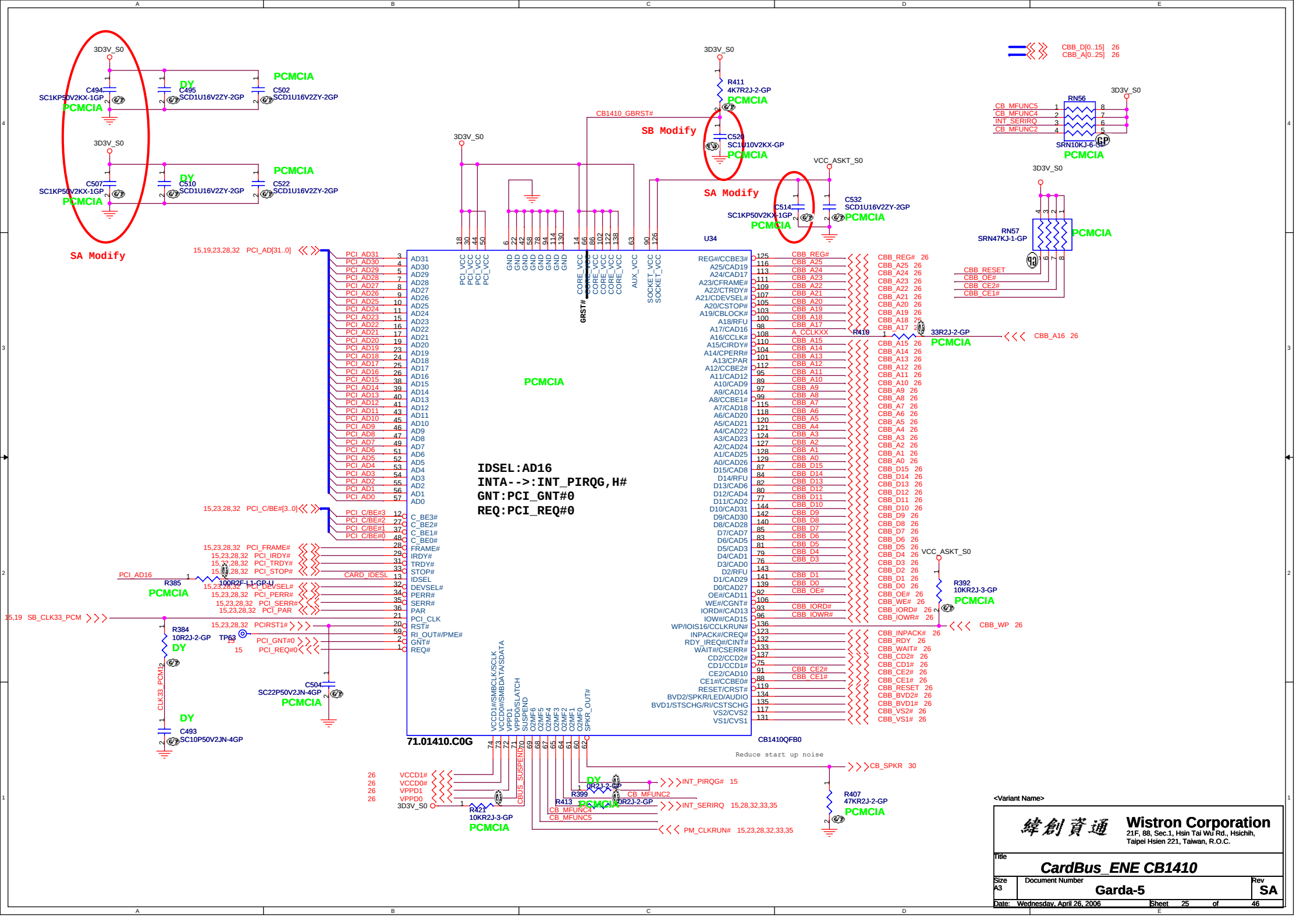
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

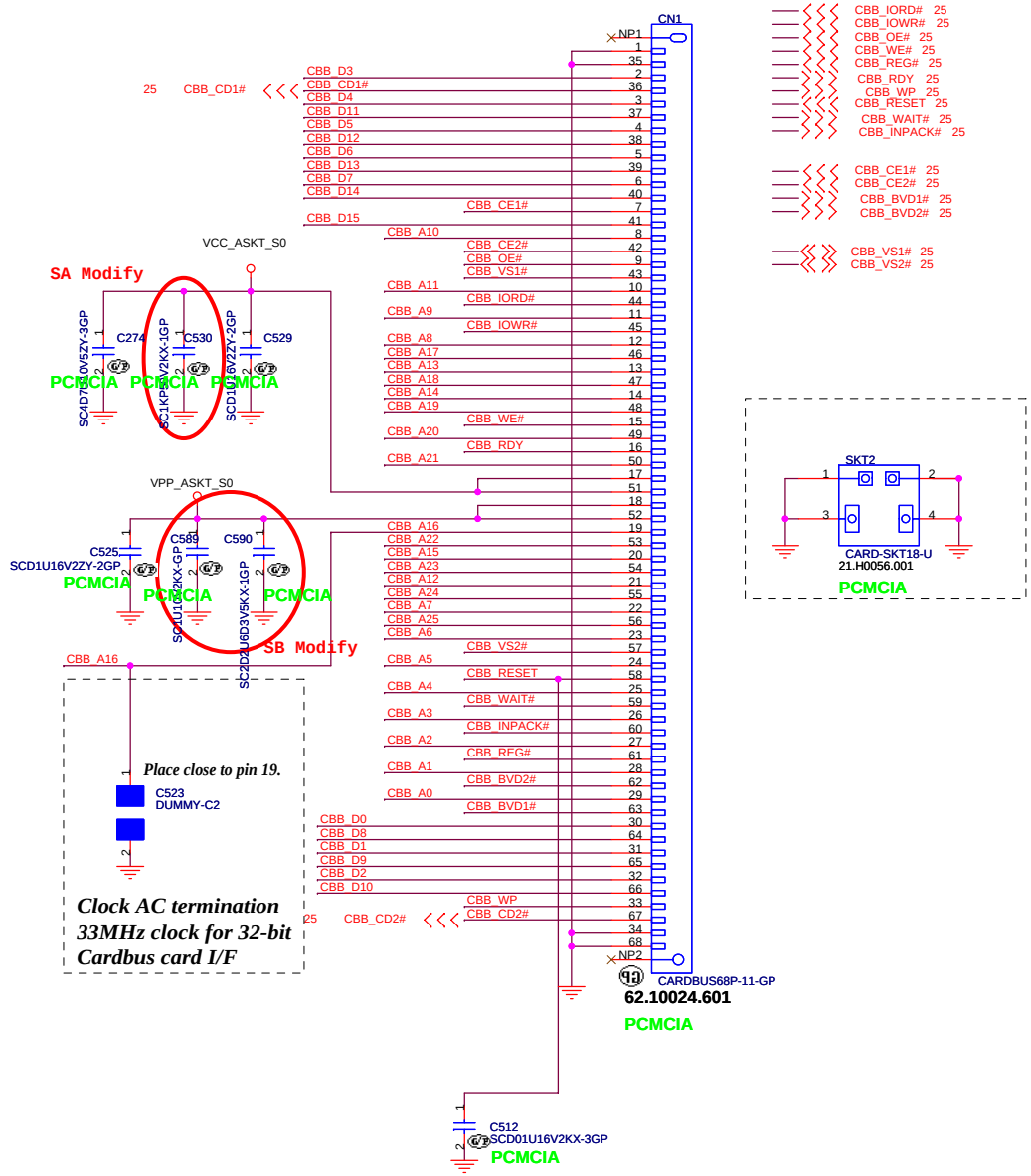
Title: LAN Connector

Size: A3 | Document Number: Garda-5 | Rev: -1

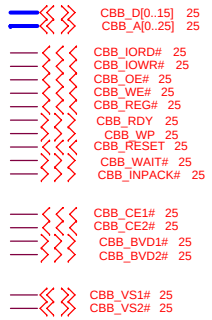
Date: Wednesday, April 26, 2006 | Sheet 24 of 46


3D3V_S0
C494
SC1KP50V2KX-1GP
PCMCIA
DY
C495
SCD1U16V2ZY-2GP
PCMCIA
C502
SCD1U16V2ZY-2GP
C507
SC1KP50V2KX-1GP
C510
SCD1U16V2ZY-2GP
C522
SCD1U16V2ZY-2GP
SA Modify
CB1410_GBRST#
SB Modify
R411
4K7R2J-2-GP
C520
SC1U10V2KX-GP
VCC_ASKT_S0
C514
SC1KP50V2KX-1GP
C532
SCD1U16V2ZY-2GP
CBB_D[0..15] 26
CBB_A[0..25] 26
RN56
SRN10KJ-6-GP
CB_MFUNC5
CB_MFUNC4
INT_SERIRQ
CB_MFUNC2
RN57
SRN47KJ-1-GP
CBB_RESET
CBB_OE#
CBB_CE2#
CBB_CE1#
15,19,23,28,32 PCI_AD[31..0]
15,23,28,32 PCI_C/BE#[3..0]
15,23,28,32 PCI_FRAME#
15,23,28,32 PCI_IRDY#
15,23,28,32 PCI_TRDY#
15,23,28,32 PCI_STOP#
15,23,28,32 PCI_DEVSEL#
15,23,28,32 PCI_PERR#
15,23,28,32 PCI_SERR#
15,23,28,32 PCI_PAR
15,23,28,32 PCIRST1#
PCI_GNT#0
PCI_REQ#0
PCI_AD16
R385
100R2F-L1-GP-U
CARD_IDESL
15,19 SB_CLK33_PCM
R384
10R2J-2-GP
TP63
CLK33_PCM12
C504
SC22P50V2JN-4GP
C493
SC10P50V2JN-4GP
U34
PCMCIA
IDSEL:AD16
INTA-->:INT_PIRQG,H#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
71.01410.C0G
CB1410QFB0
R410
33R2J-2-GP
CBB_A16 26
R392
10KR2J-3-GP
CBB_WP 26
Reduce start up noise
CB_SPKR 30
R407
47KR2J-2-GP
INT_PIRQG# 15
INT_SERIRQ 15,28,32,33,35
PM_CLKRUN# 15,23,28,32,33,35
VCCD1#
VCCD0#
VPPD1
VPPD0
R421
10KR2J-3-GP
R399
R413
CB_MFUNC4
CB_MFUNC5
CBUS_SUSPEND
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number
Garda-5
Rev SA
Date: Wednesday, April 26, 2006
Sheet 25 of 46

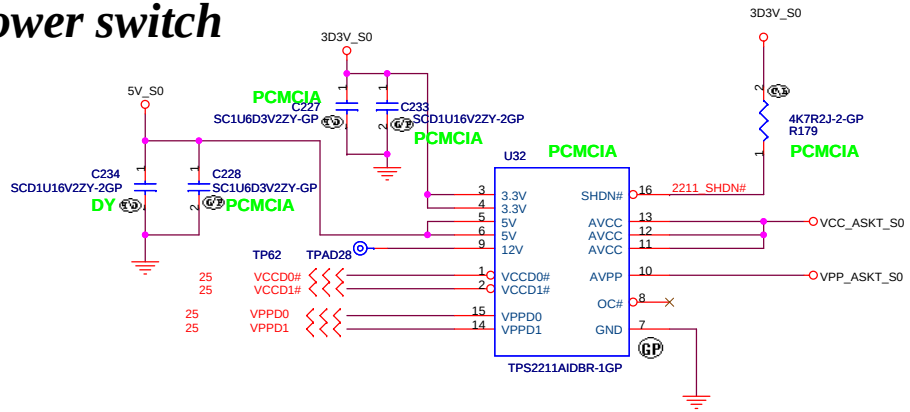
PCMCIA Socket



Cardbus I/F



Power switch



<Variant Name>

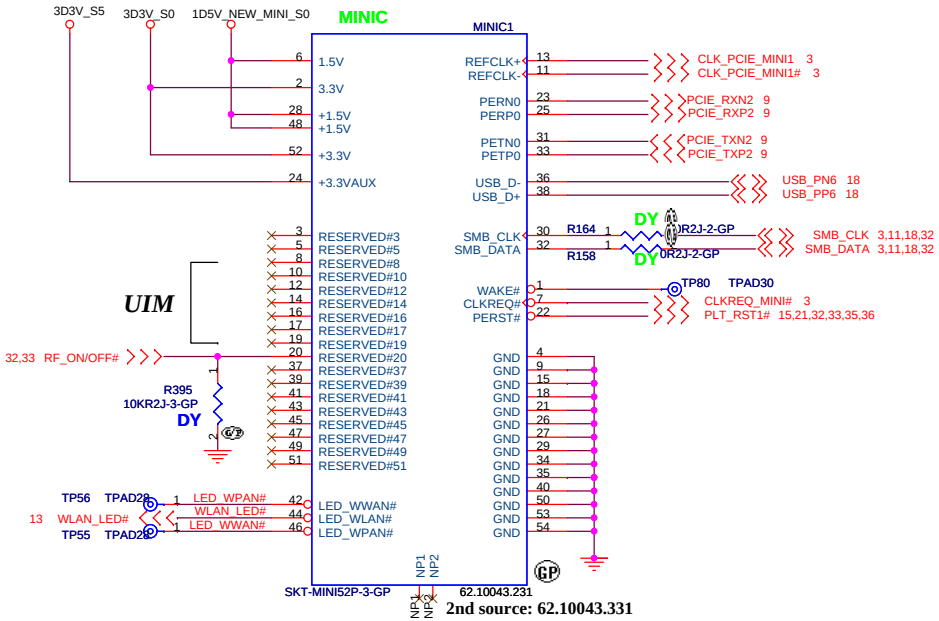
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

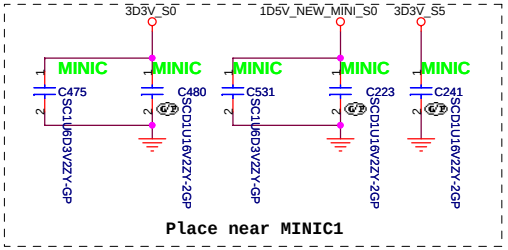
Title: PCMCIA

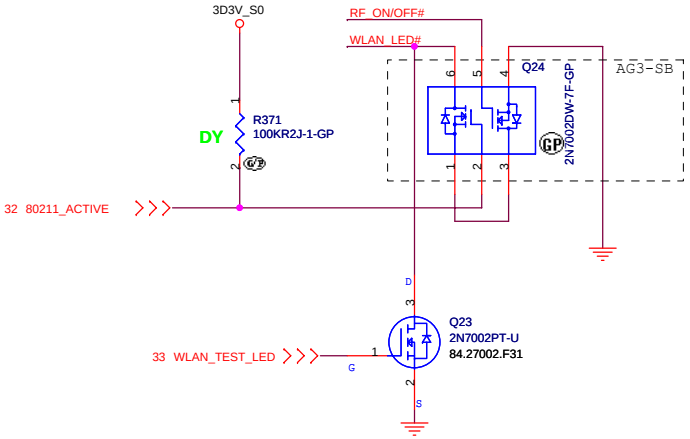
Size: A3 | Document Number: Garda-5 | Rev: SB

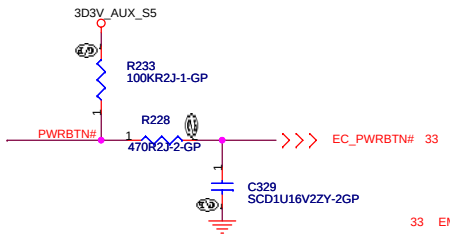
Date: Wednesday, April 26, 2006 | Sheet 26 of 46

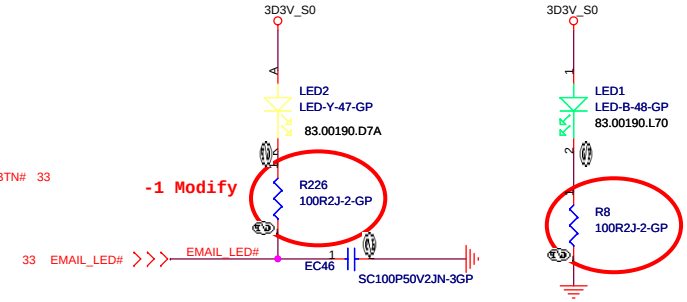
Mini Card Connector



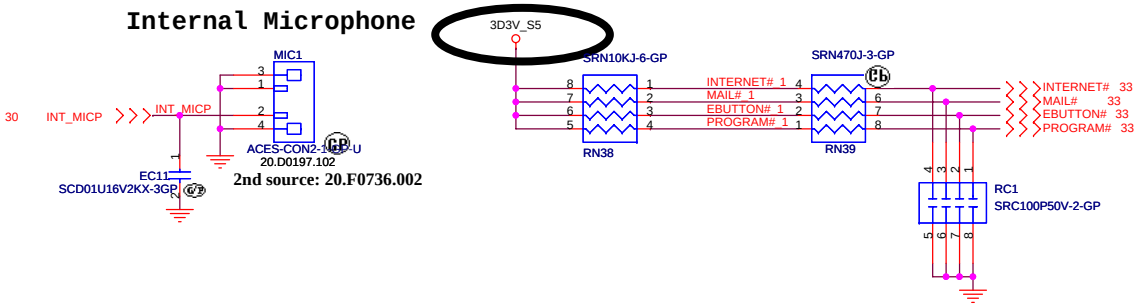






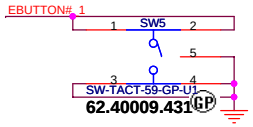


Internal Microphone



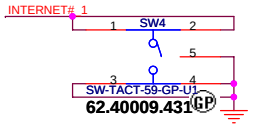
E-Button

TOP VIEW RIGHT 4



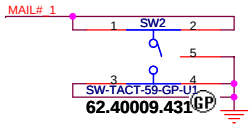
Internet Button

TOP VIEW RIGHT 3



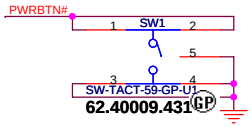
Mail Button

TOP VIEW RIGHT 2



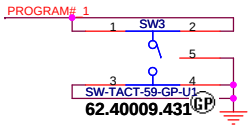
Power Button

TOP VIEW RIGHT 1



Program Button

TOP VIEW RIGHT 5

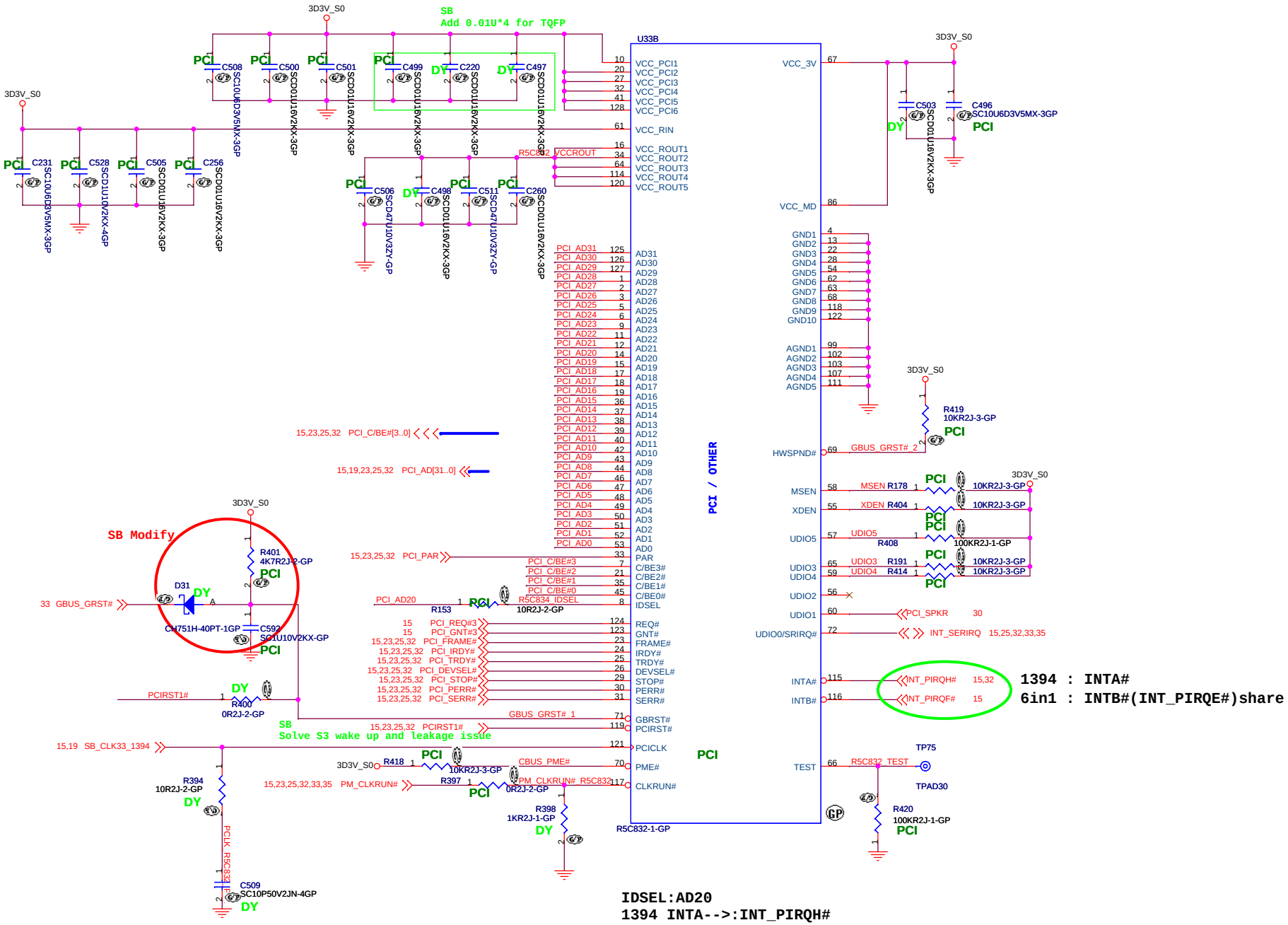


LED				V	V
Button	V	V	V	V	V
	Program Button	E-Button	Internet Button	Mail Button	Power Button

<Variant Name>

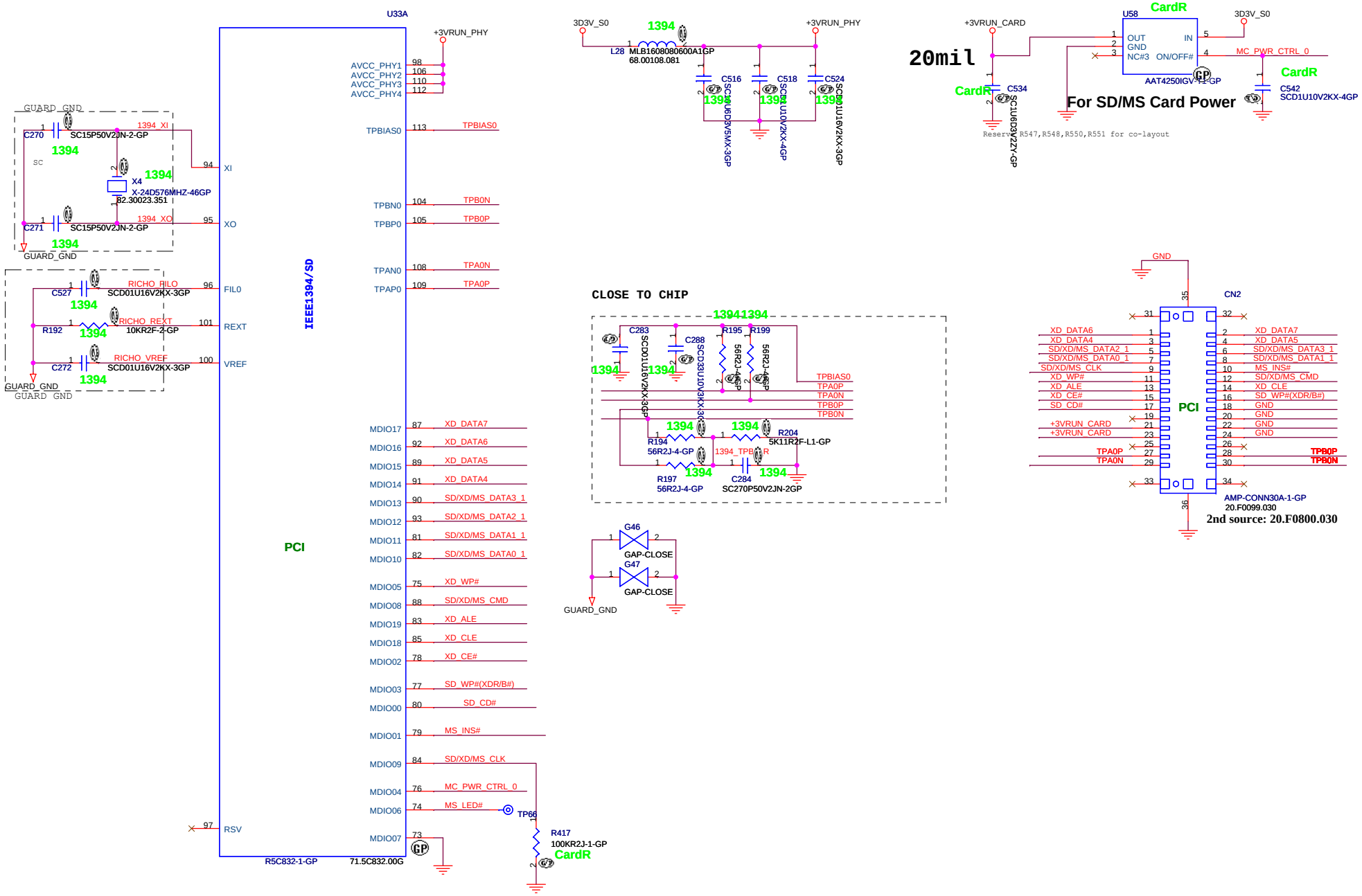
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MINI CARD / Launch Button***	
Size A3	Document Number **Garda-5**	Rev **-1**
Date: Wednesday, April 26, 2006	Sheet 27 of 46	



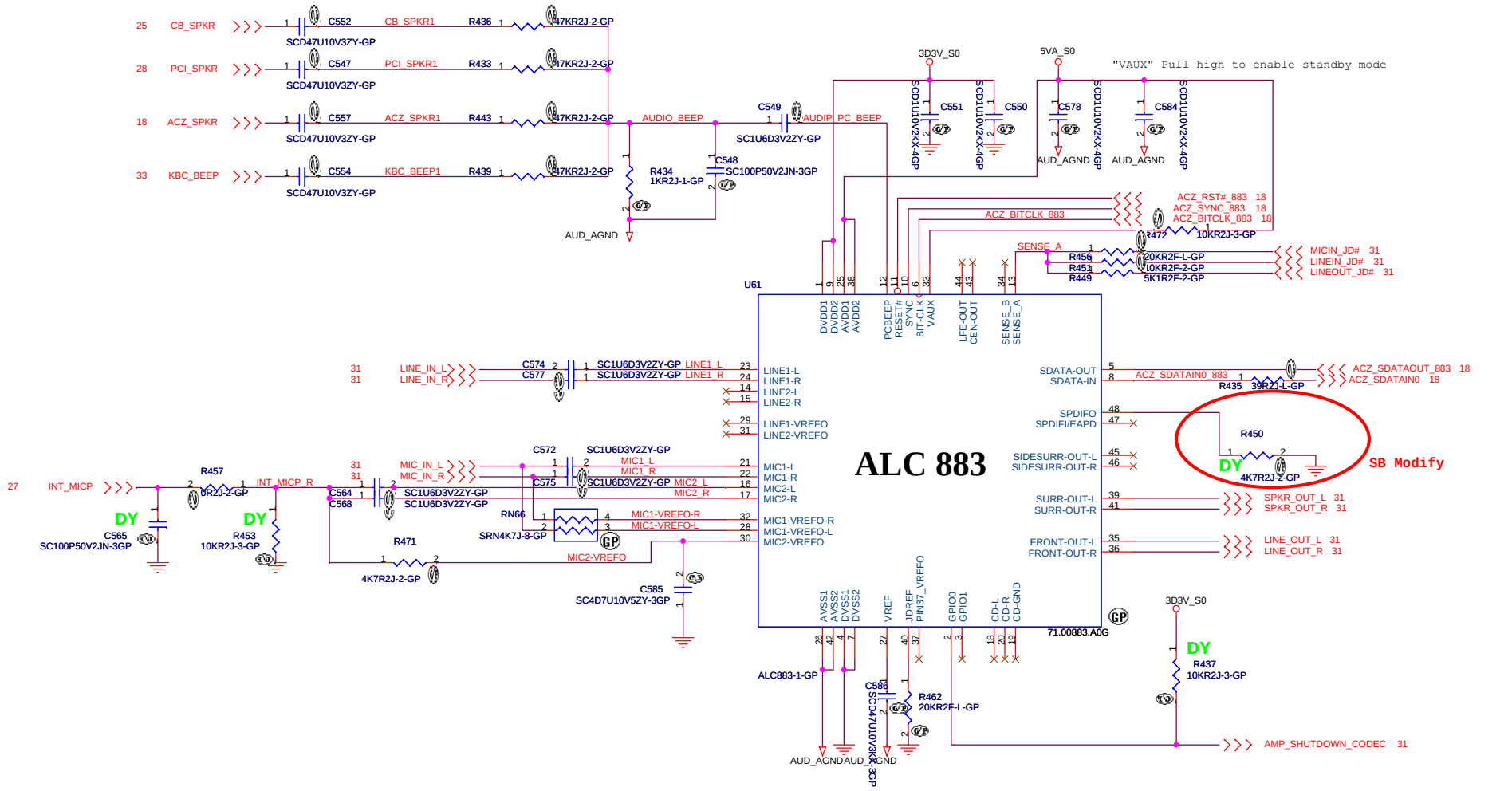
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	R5C832_1394_7IN1(1/2)	
Size A3	Document Number Garda5	Rev SB
Date: Wednesday, April 26, 2006	Sheet 28 of 46	



<Variant Name>

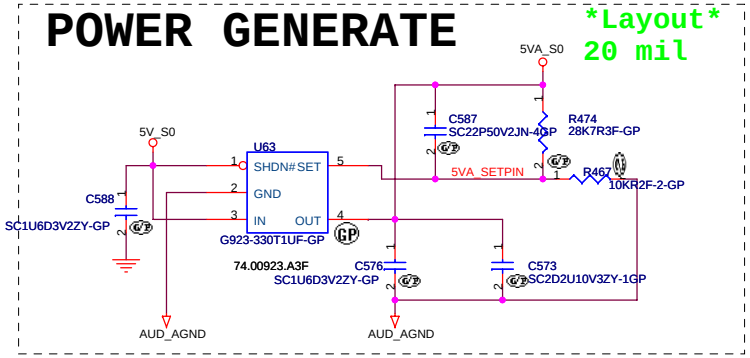
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***R5C832_1394_7IN1(2/2)***
Size A3	Document Number **Garda-5** Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 29 of 46

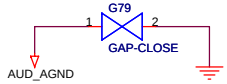


1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input





<Variant Name>

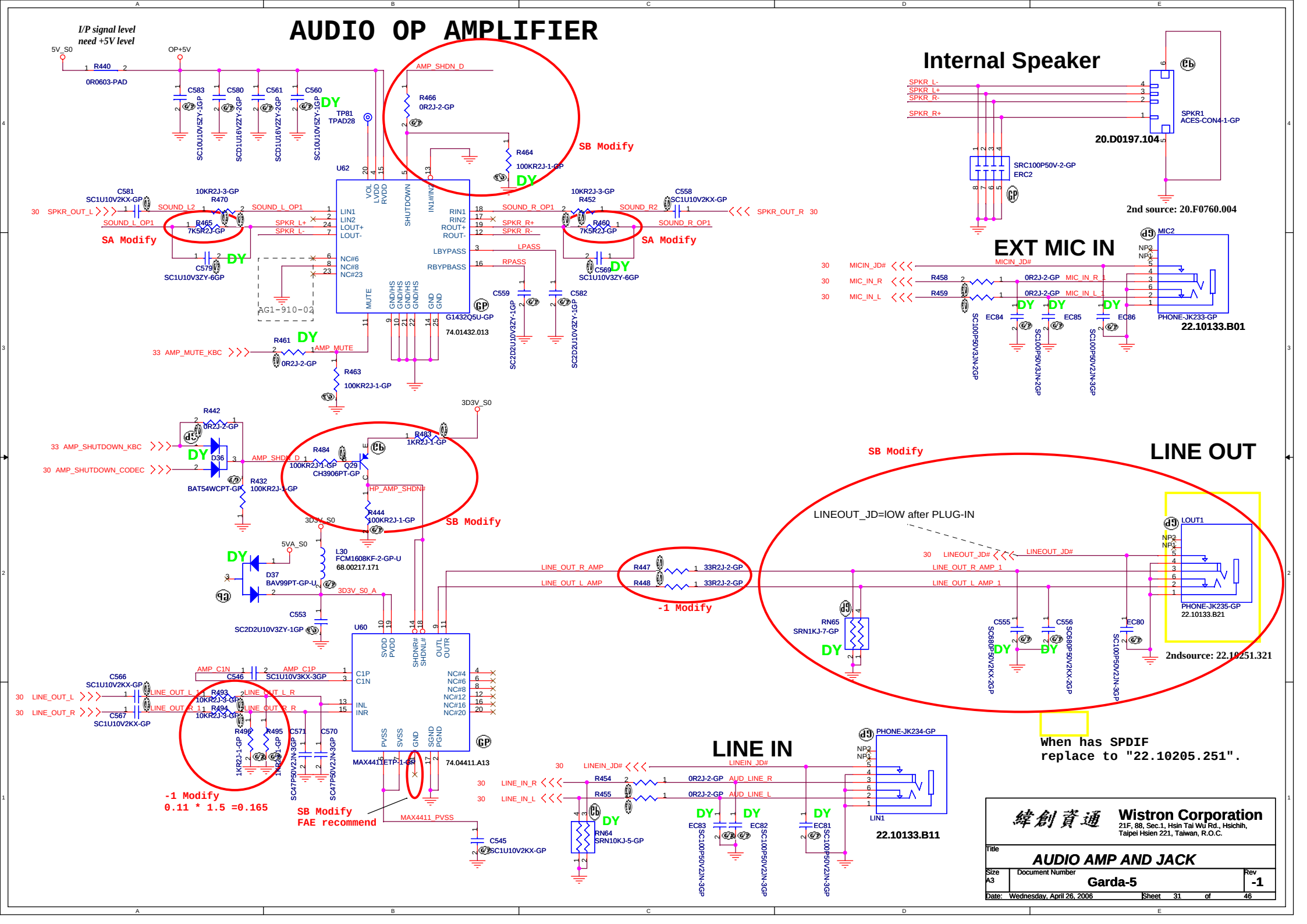
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC883***

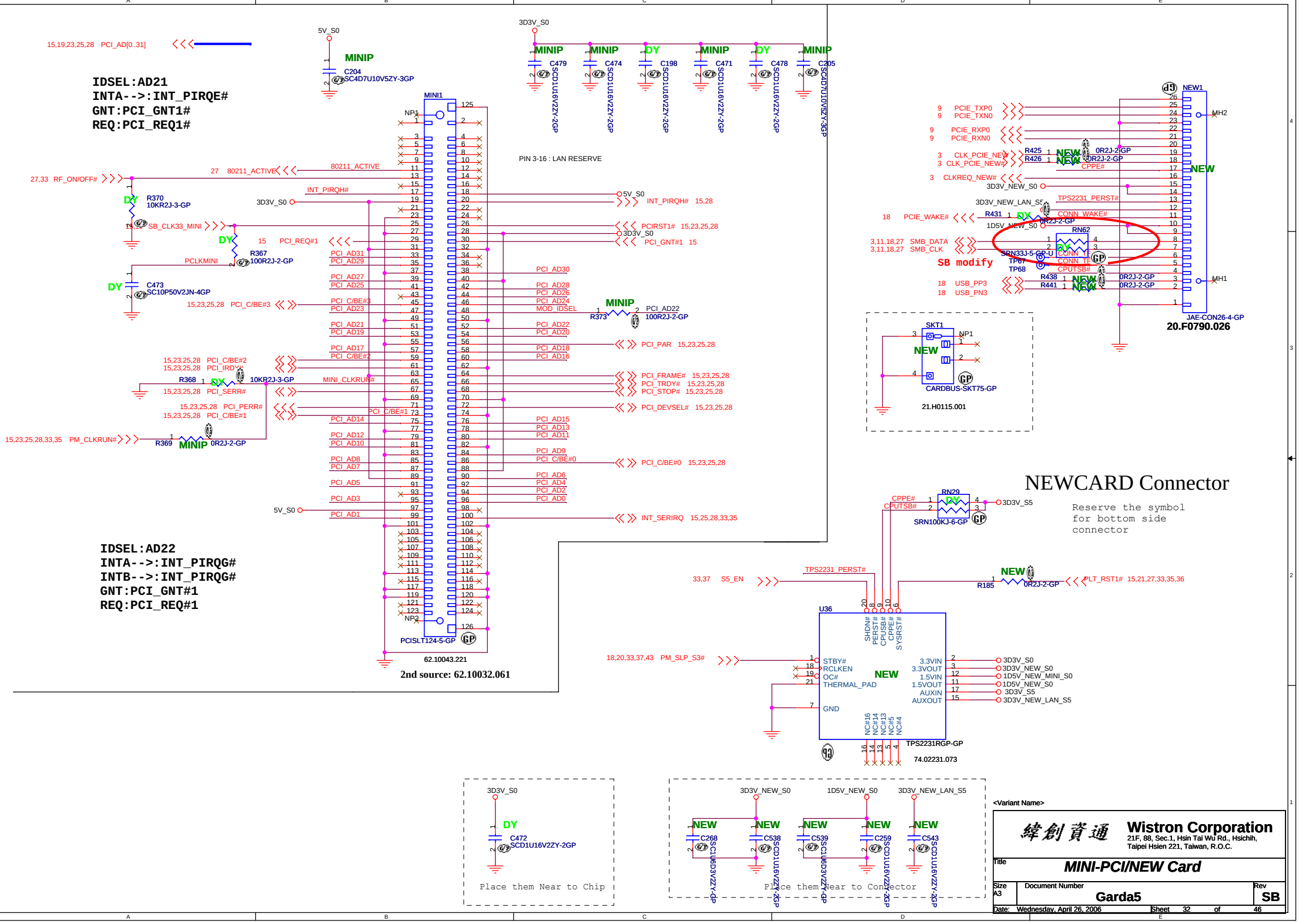
Size: A3 | Document Number: **Garda-5** | Rev: **SB**

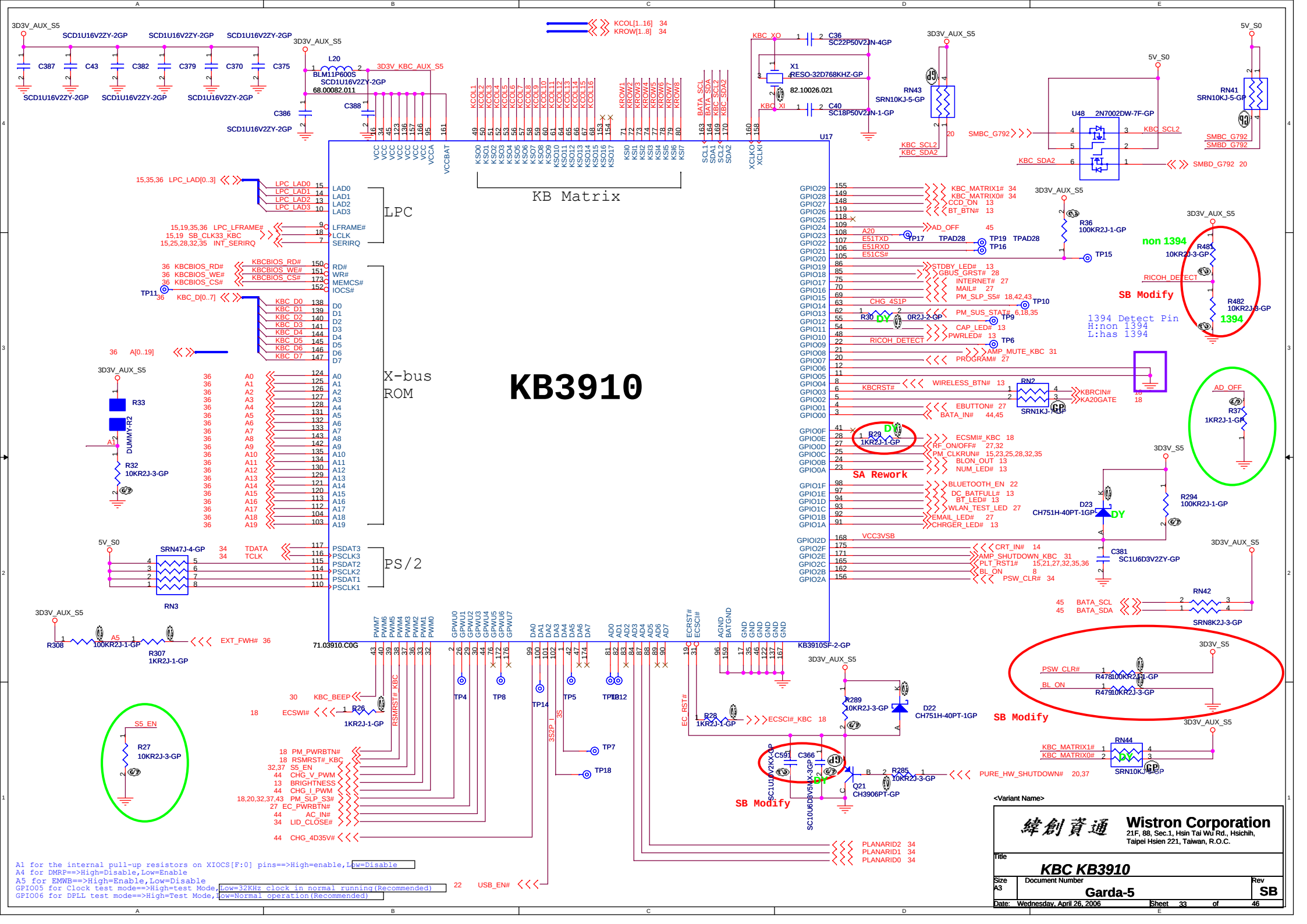
Date: Wednesday, April 26, 2006 | Sheet 30 of 46

AUDIO OP AMPLIFIER

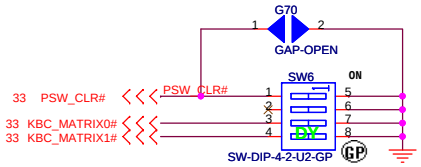


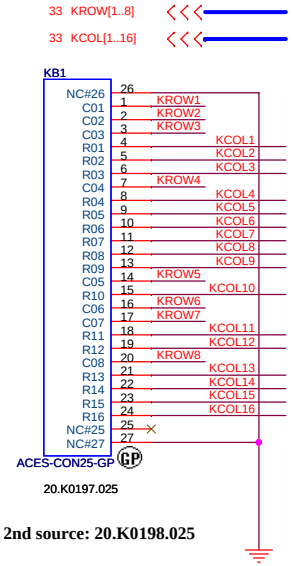
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size A3	Document Number Garda-5	Rev -1
Date: Wednesday, April 26, 2006	Sheet 31 of 46	


IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQG#
GNT:PCI_GNT#1
REQ:PCI_REQ#1
MINI1
PCISLT124-5-GP
62.10043.221
2nd source: 62.10032.061
PIN 3-16 : LAN RESERVE
NEW1
JAE-CON26-4-GP
20.F0790.026
SB modify
SKT1
CARDBUS-SKT75-GP
21.H0115.001
NEWCARD Connector
Reserve the symbol for bottom side connector
U36
TPS2231RGP-GP
74.02231.073
Place them Near to Chip
Place them Near to Connector
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MINI-PCI/NEW Card
Garda5
SB
Wednesday, April 26, 2006
Sheet 32 of 46


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U17
KB3910SF-2-GP
71.03910.C0G
SA Rework
SB Modify
non 1394
1394 Detect Pin
H:non 1394
L:has 1394
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommend)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC KB3910
Size A3
Document Number
Garda-5
Rev SB
Date: Wednesday, April 26, 2006
Sheet 33 of 46

Internal KeyBoard Connector



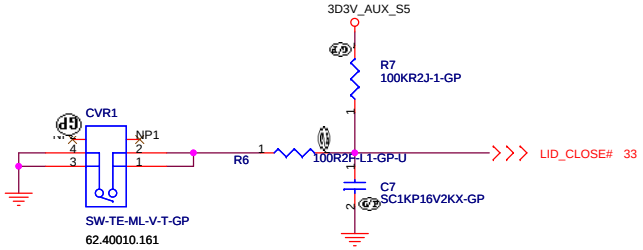


Keyboard matrix (from vendor)

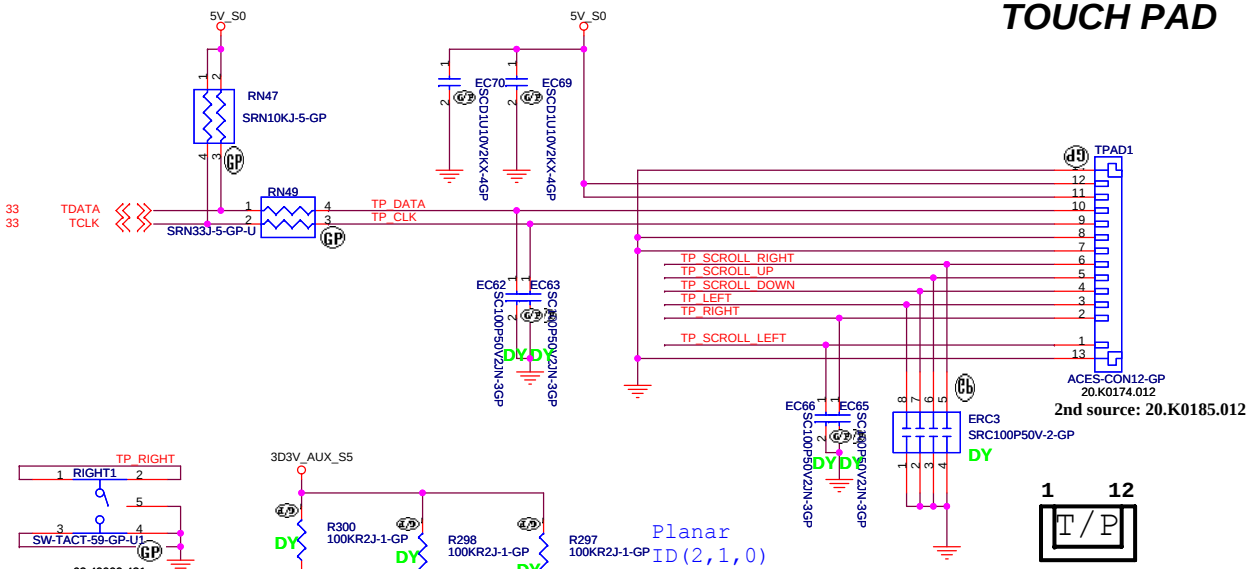
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

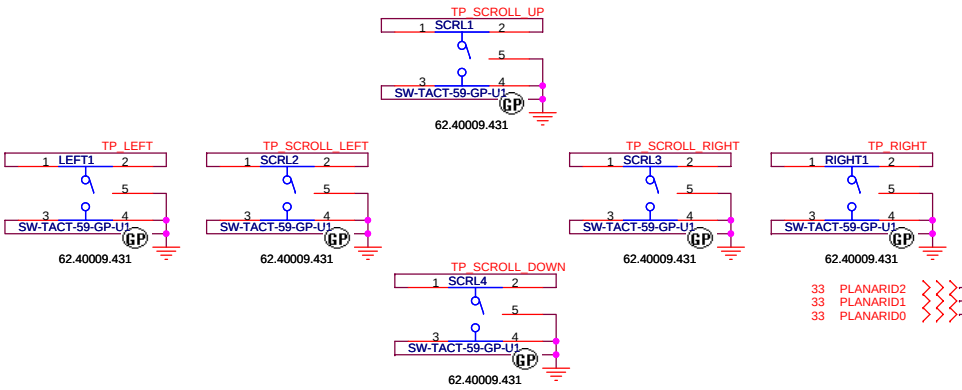
COVER SWITCH

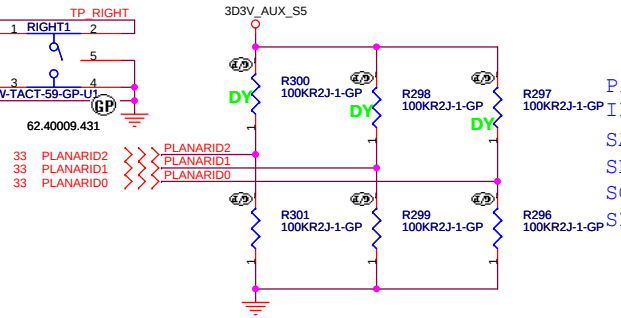


TOUCH PAD



SCROLL KEY





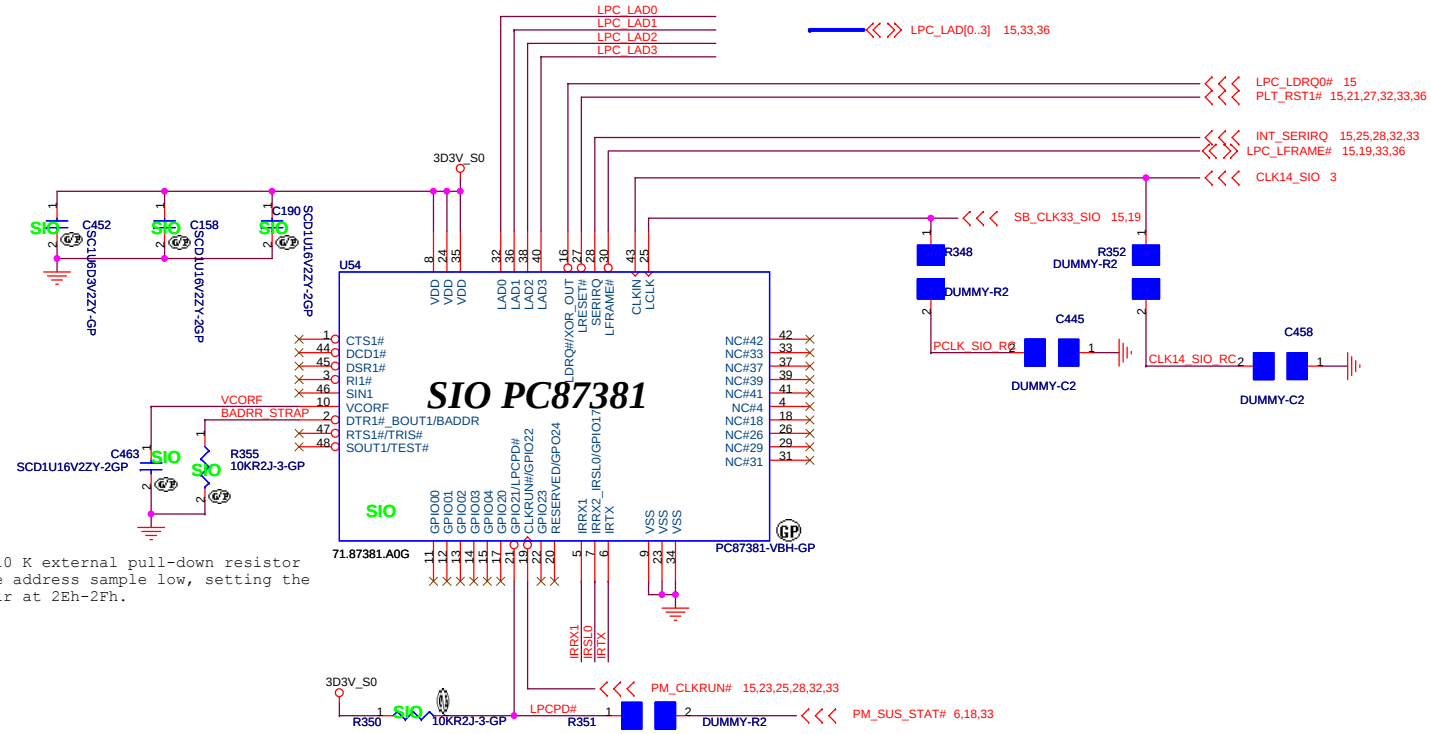
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1

<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCHPAD

Size: A3 | Document Number: Garda-5 | Rev: SA

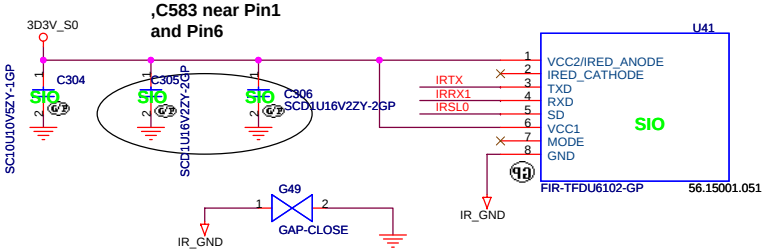
Date: Wednesday, April 26, 2006 | Sheet 34 of 46



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

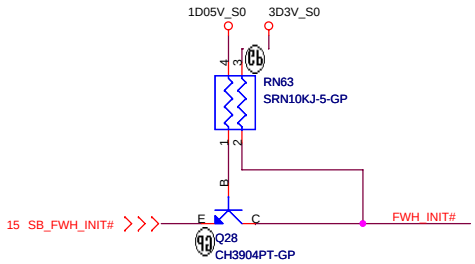
Place C581 ,C583 near Pin1 and Pin6

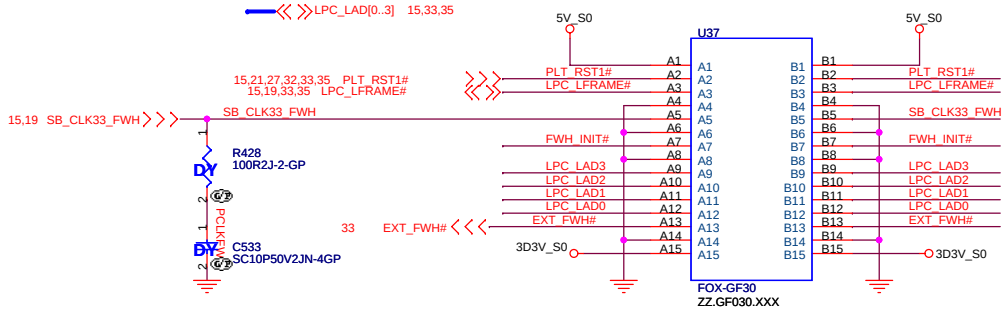


<Variant Name>

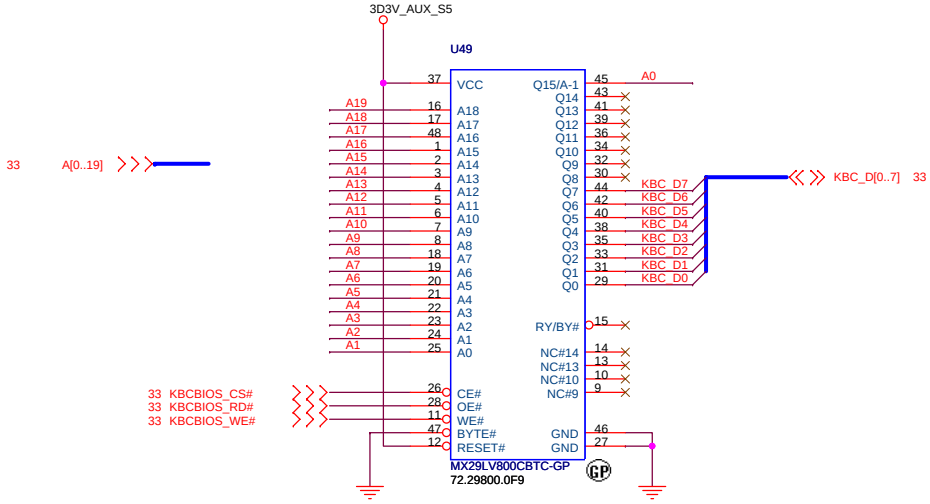
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIO 87381 / FIR***	
Size A3	Document Number **Garda-5**	Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 35 of 46	

GOLDEN FINGER FOR DEBUG BOARD





Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

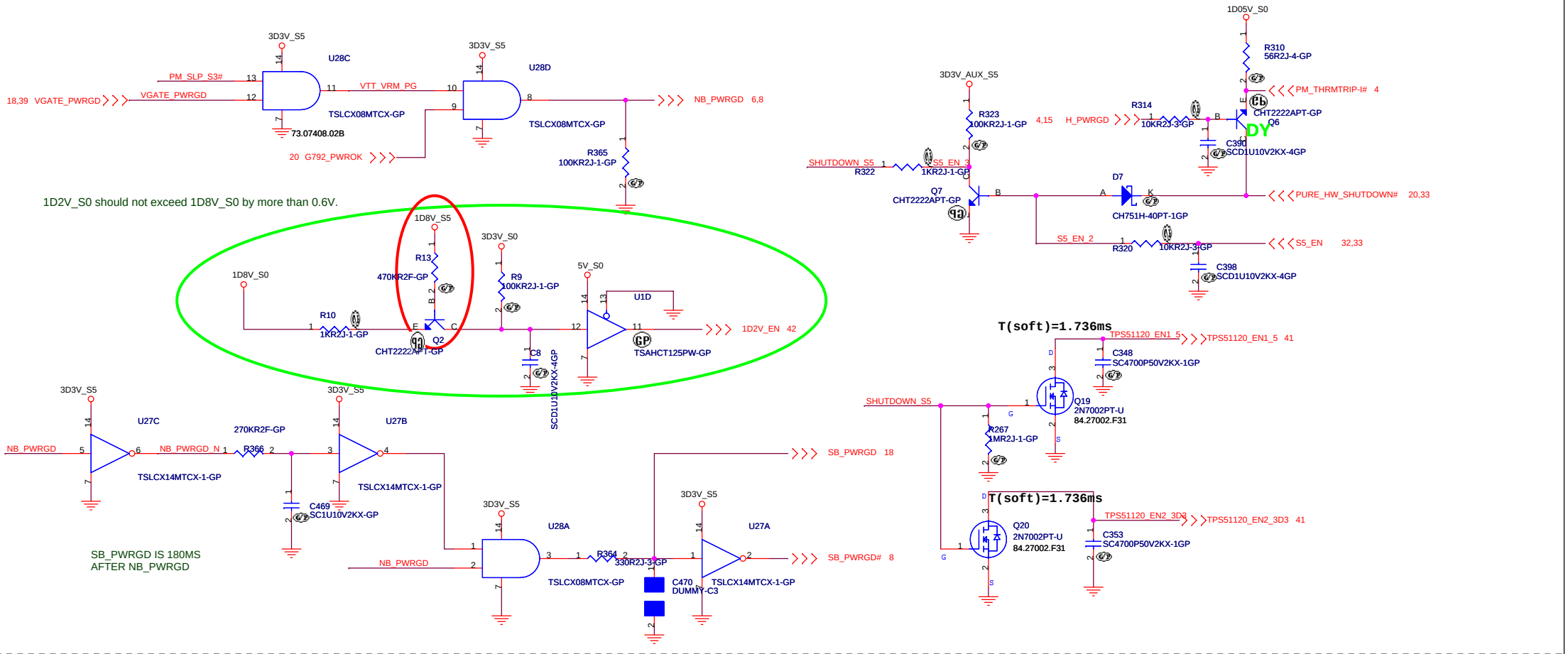
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

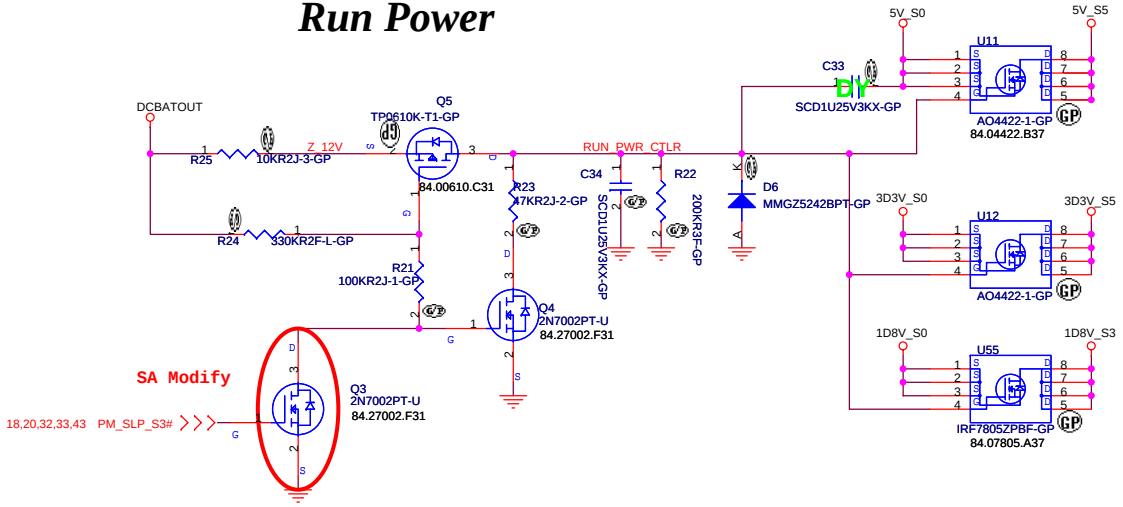
Title: ***BIOS ROM***

Size: A3 | Document Number: **Garda-5** | Rev: **SA**

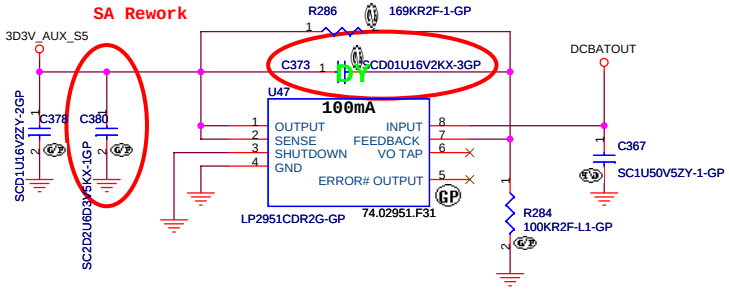
Date: Wednesday, April 26, 2006 | Sheet 36 of 46



Run Power



Aux Power



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RUN and AUX POWER**	
Size A3	Document Number **Garda-5**	Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 37 of 46	

CPU_CORE
Intersil ISL6262

VID Setting
- VID0(I / 1.05V)
- VID1(I / 1.05V)
- VID2(I / 1.05V)
- VID3(I / 1.05V)
- VID4(I / 1.05V)
- VID5(I / 1.05V)
- VID6(I / 1.05V)

Input Signal
- PSI# (I / 3.3V)
- PGD_IN (I / 3.3V)
- DPRSLPVR (I / 3.3V)
- DPRSTP# (I / 3.3V)

Voltage Sense
- VSEN(I / Vcore)
- RTN(I / Vcore)

Input Power
- VCC(I)
- VCC(I)
- VCC(I)

Output Signal
- PGOOD(OD / 3.3V)
- CLK_EN#(O)

Output Power
- VCC_CORE_PWR(O)

H_VID0, H_VID1, H_VID2, H_VID3, H_VID4, H_VID5, H_VID6

PSI#, CPUCORE_ON, PM_DPRSLPVR, H_DPRSTP#

VCC_SENSE, VSS_SENSE

DCBATOUT_6262, 5V_S0, 3D3V_S0

6262_PWRGOOD, CLK_EN#, VCC_CORE_S0(Imax=48A)

TPS51124
1D8V/1D05V

Input Power
- VCC
- VIN

Input Signal
- EN1
- EN2

Output Signal
- PGOOD1
- PGOOD2

Output Power
- 1D8V (O)
- 1D05V(O)

5V_S5, DCBATOUT_TPS51124, TPS51124_EN1, TPS51124_EN2, CPUCORE_ON, CPUCORE_ON

1D8V_S0 (7A), 1D05V_S0 (7A)

CHARGER MAX8725

Input Signal
- ICTL
- PKPRES

Input Power
- ACIN

Output Signal
- BATT
- ACOK

Output Power
- VOUT (O)
- VOUT (O)

CHGON#/OFF, BT_TH, AD+

BT+SENSE, AC_IN, BT+, DCBATOUT

TPS51120
5V/3D3V

Input Signal
- EN1
- EN2

Input Power
- VIN

Output Signal
- PGOOD1(OD / 5V)
- PGOOD2(OD / 5V)

Output Power
- 5V(O)
- 3D3V(O)

TPS51120_EN1_5, TPS51120_EN2_3D3, DCBATOUT_TPS51120

CPUCORE_ON, CPUCORE_ON, 5V_DC_S5 (6A), 3D3V_DC_S5 (5A)

Adapter

Input Signal (I)

Output Signal (O)

Input Power
- VCC(I)
- VCC(I)

Output Power
- VCC(O)

AD_OFF, AD_JK, 5V_AUX_S5

AD_IN, AD+

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D8V_S5

APL5308-18DC-GP

1D5V_S0

3D3V_S5 → INPUT / OUT → 1D5V_CPU_S0

APL5312

1D5V_S0

3D3V_S5 → INPUT / OUT → 1D5V_NEW_MINI_S0

APL5332

1D05V_S0

1D2V_S3 → INPUT / OUT → 1D05V_S0

APL5912-KAC-GP

DDR_VREF_S0

5V_S5 → INPUT / OUT → DDR_VREF_S0

TPS51100DGQR-GP

3D3V_AUX_S5

DCBATOUT → INPUT / OUT → 3D3V_AUX_S5

LP2951ACM

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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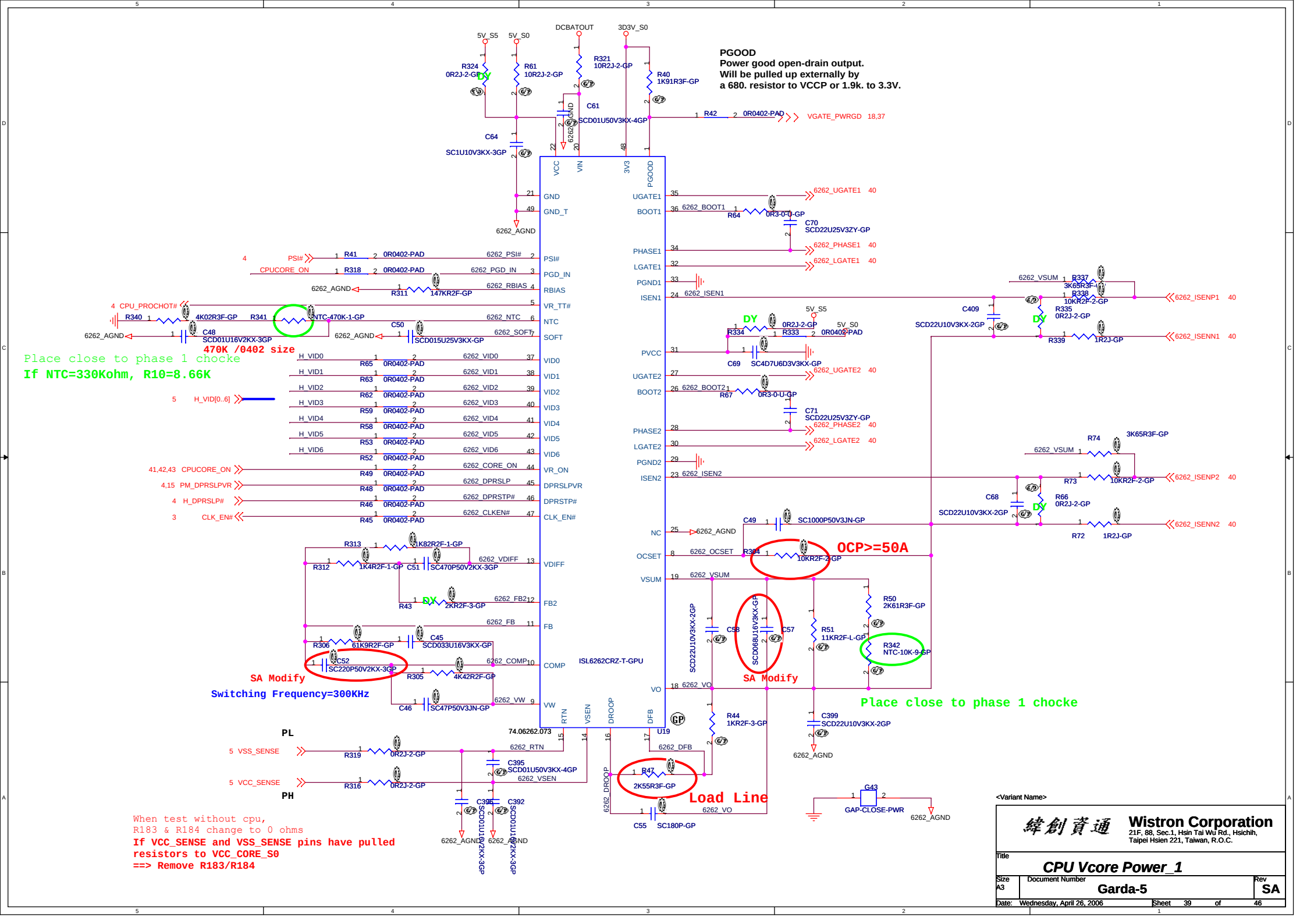
PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
ISL6262CRZ-T-GPU
U19
470K /0402 size
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
OCP>=50A
SA Modify
Switching Frequency=300KHz
Load Line
Place close to phase 1 chocke
PL
PH
When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184
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Title
CPU Vcore Power_1
Size A3
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Date: Wednesday, April 26, 2006
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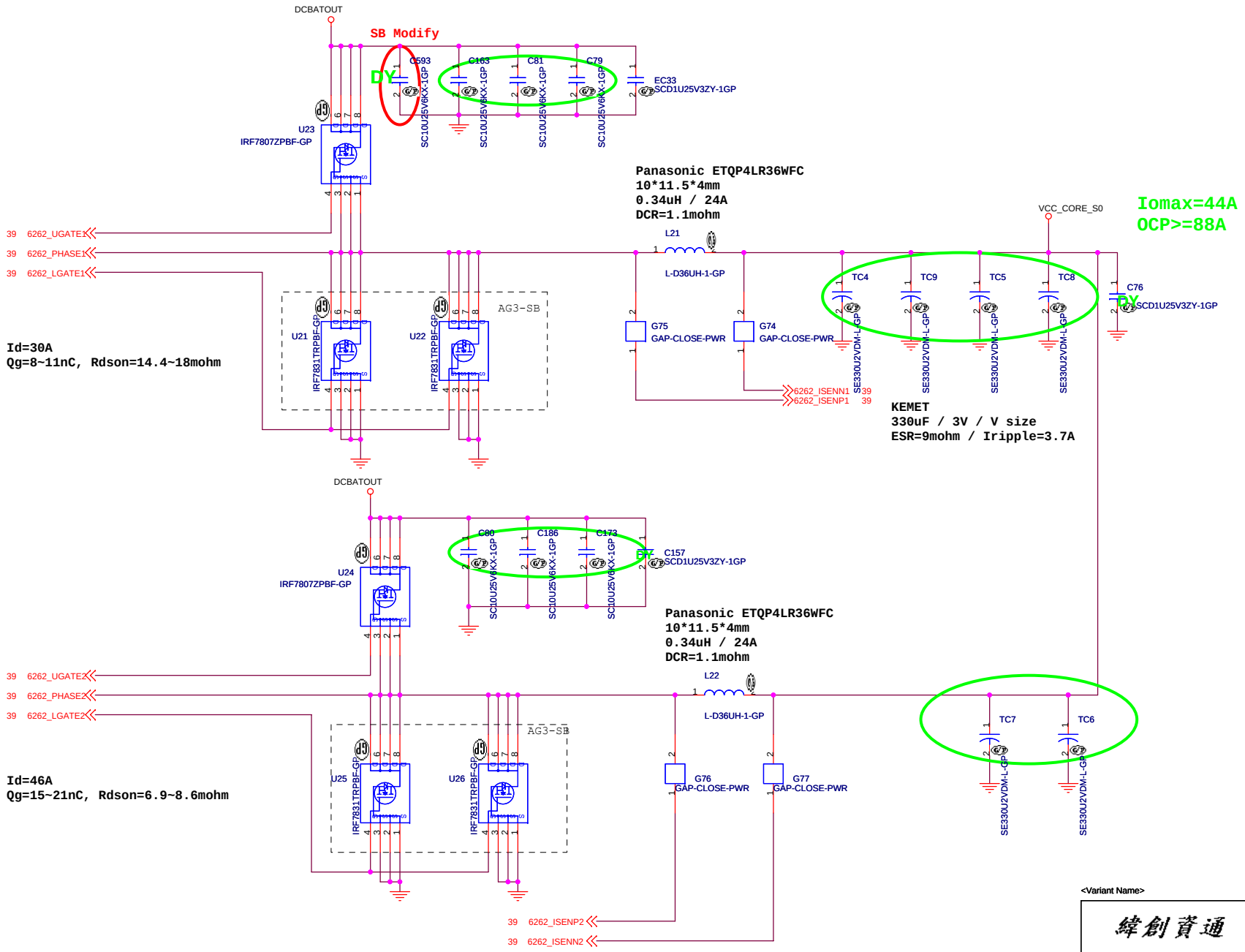

<Variant Name>

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Title: ***CPU Vcore Power_2/2***

Size	Document Number	Rev
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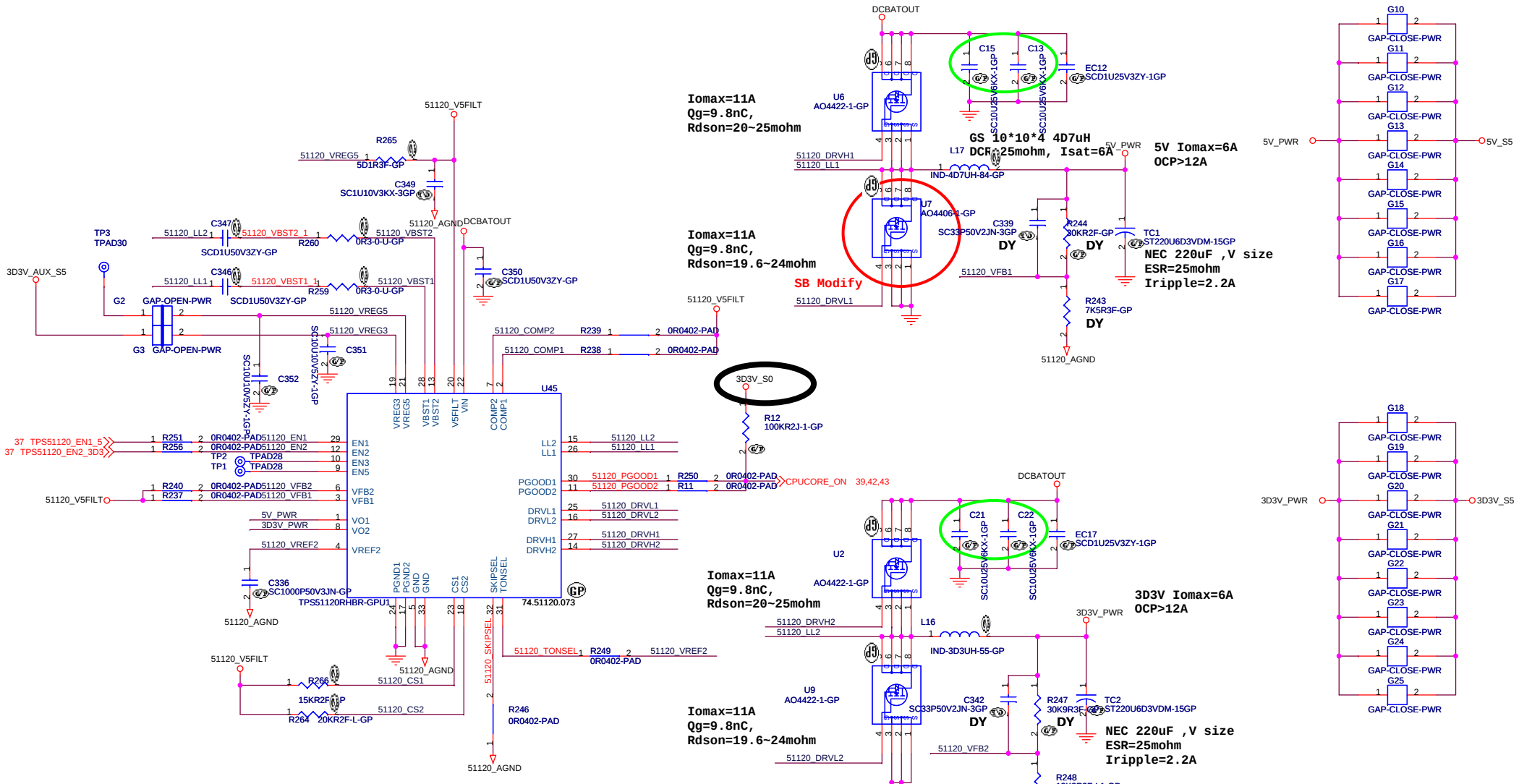

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

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Title: TPS51120_3D3V_5V

Size: A3 | Document Number: Garda-5 | Rev: SB

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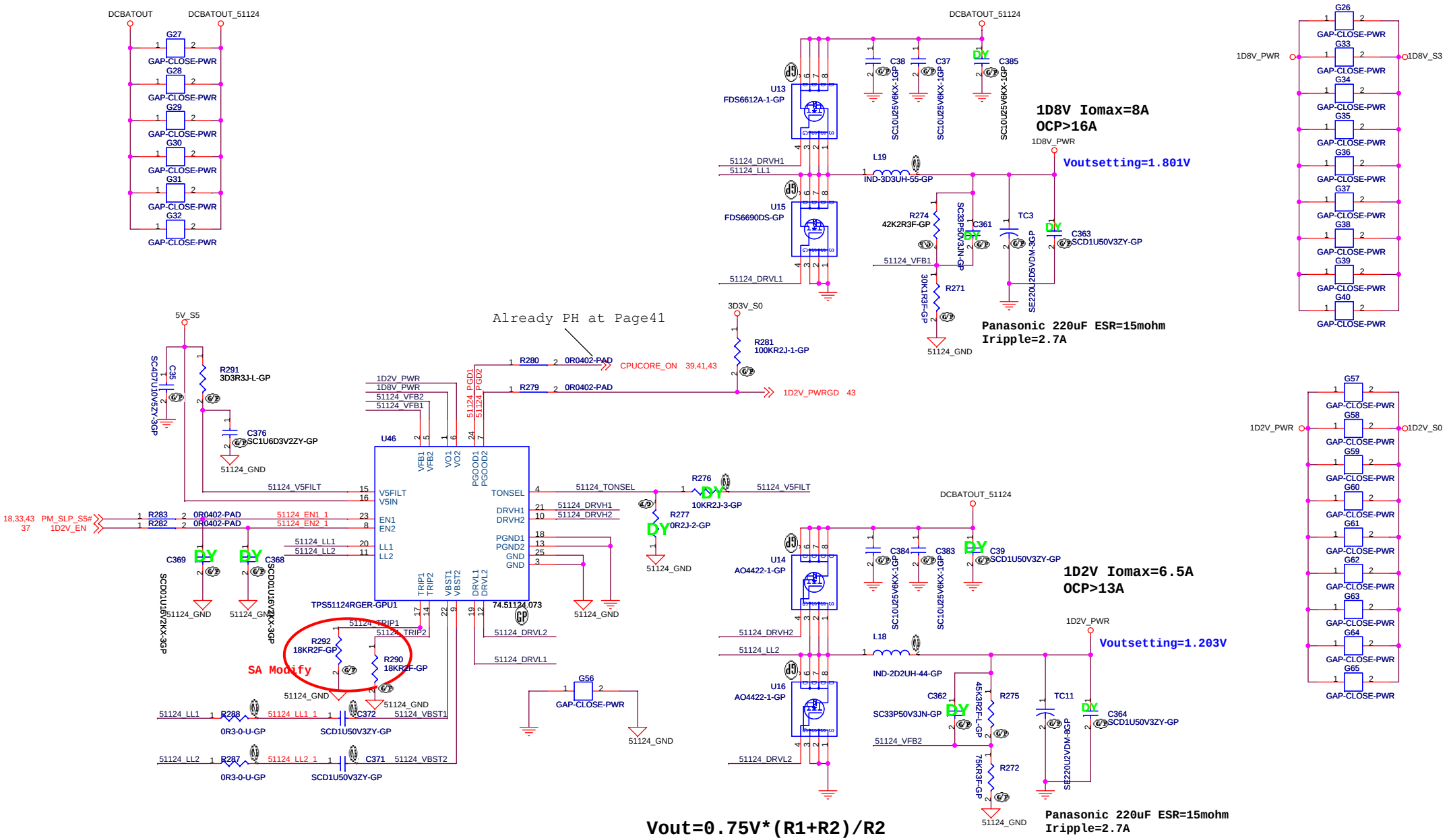

Vout=0.75V*(R1+R2)/R2

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

<Variant Name>

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Title: TPS51124_1D8V_1D2V

Size: A3 | Document Number: Garda-5 | Rev: SA

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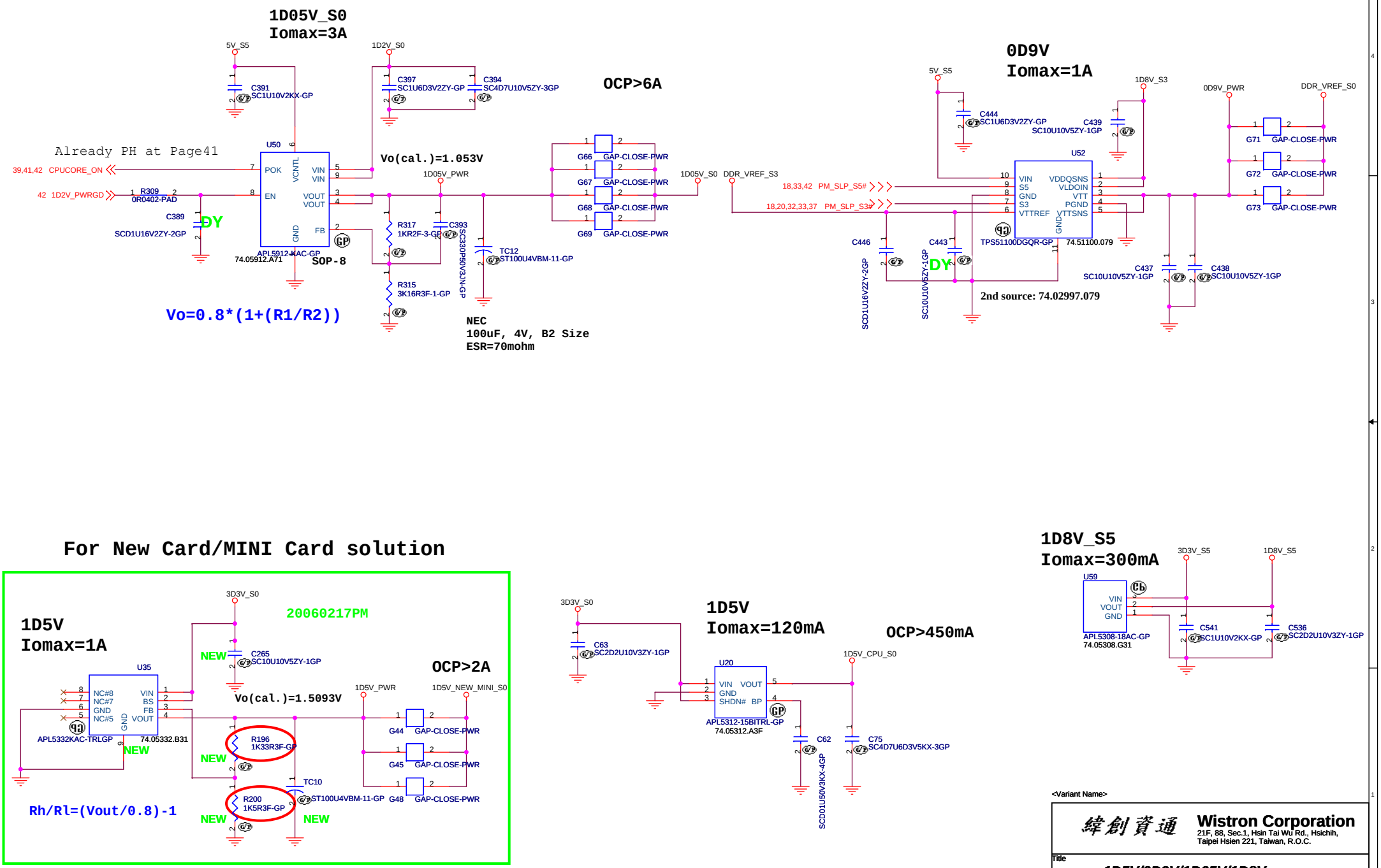

<Variant Name>

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Title: **1D5V/0D9V/1D05V/1D8V**

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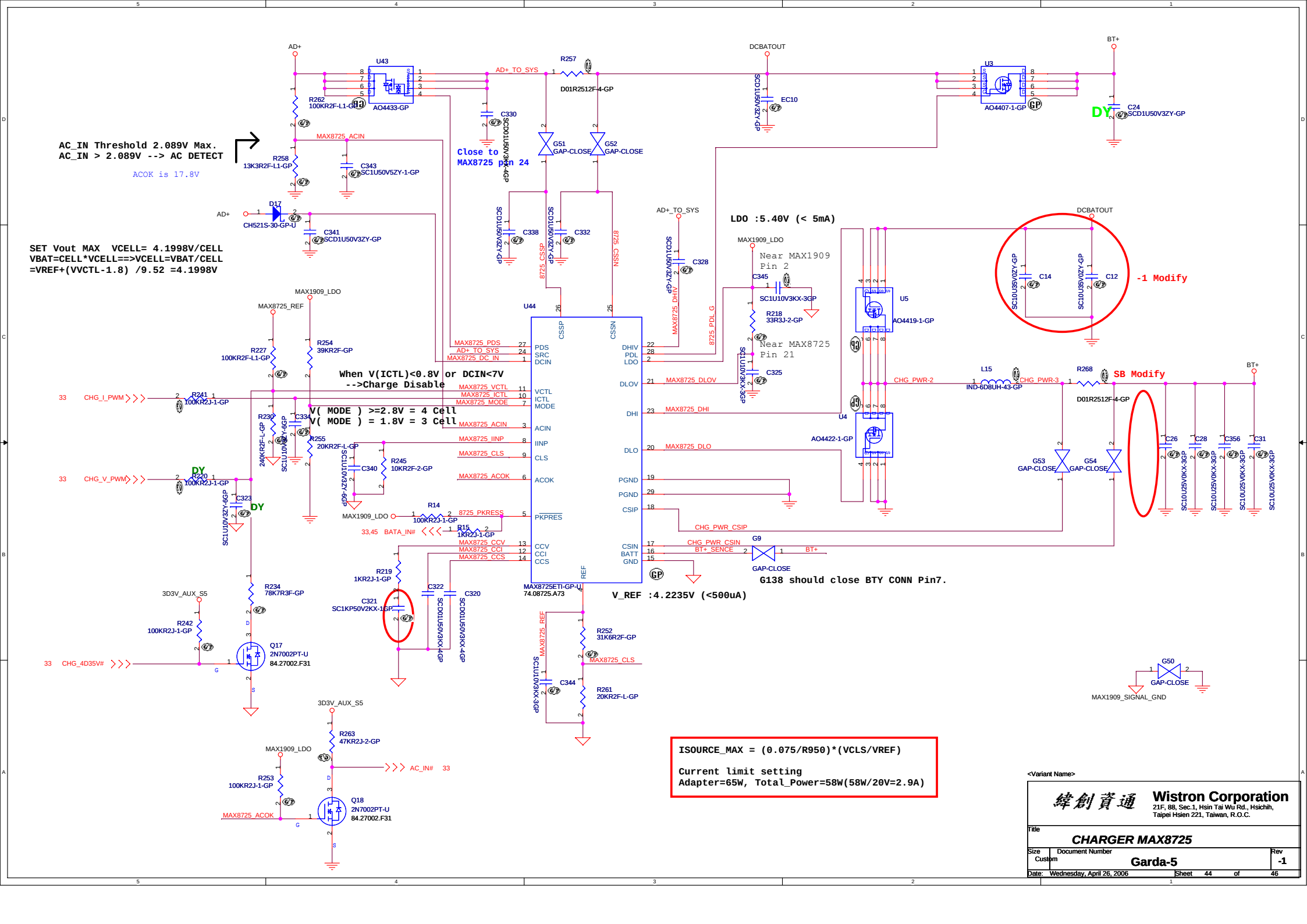
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
Close to MAX8725 pin 24
LDO :5.40V (< 5mA)
Near MAX1909 Pin 2
Near MAX8725 Pin 21
-1 Modify
SB Modify
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
V_REF :4.2235V (<500uA)
G138 should close BTY CONN Pin7.
ISOURCE_MAX = (0.075/R950)*(VCLS/VREF)
Current limit setting
Adapter=65W, Total_Power=58W(58W/20V=2.9A)
Wistron Corporation
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CHARGER MAX8725
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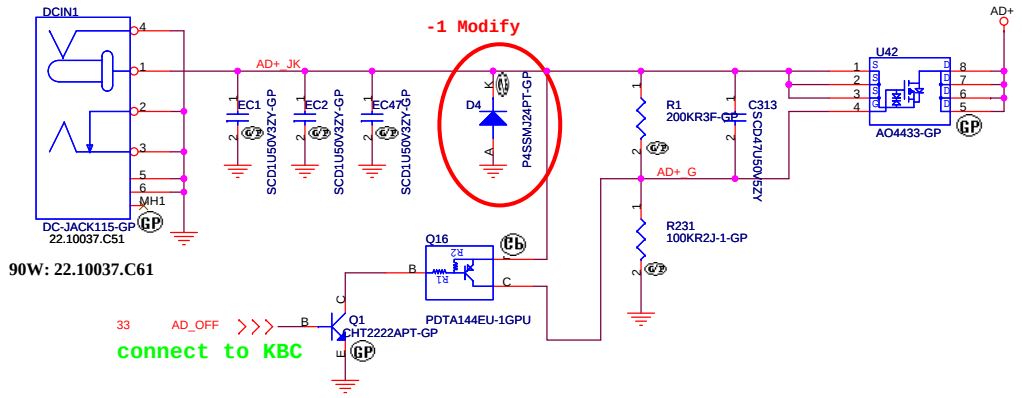
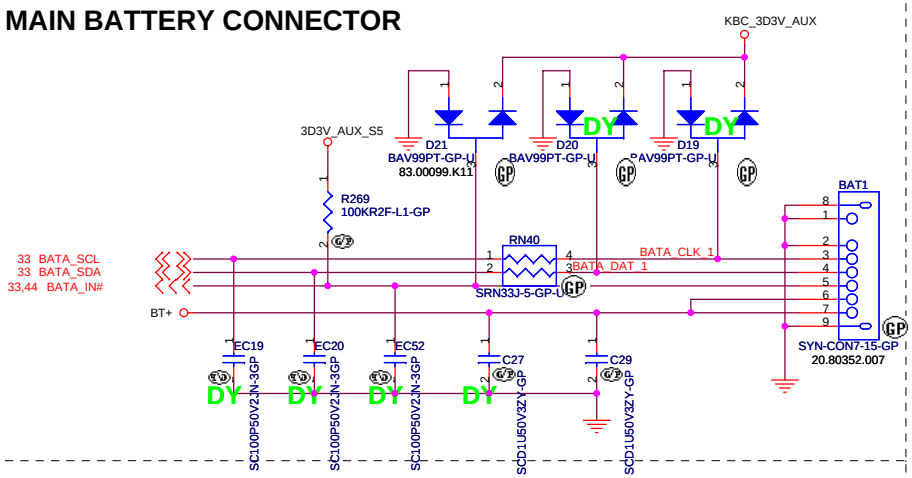
ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



<Variant Name>

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Title	***AD/BATT CONN***
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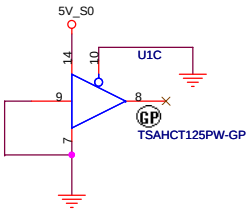
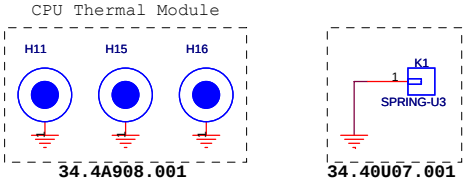
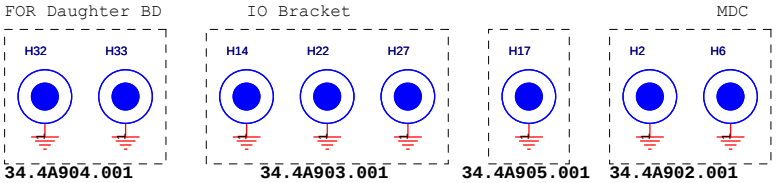
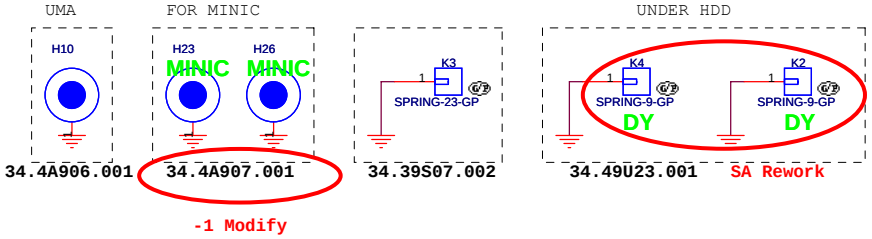


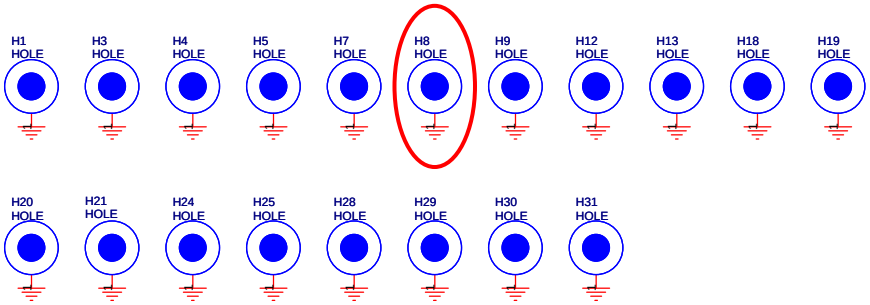
TOP SIDE:



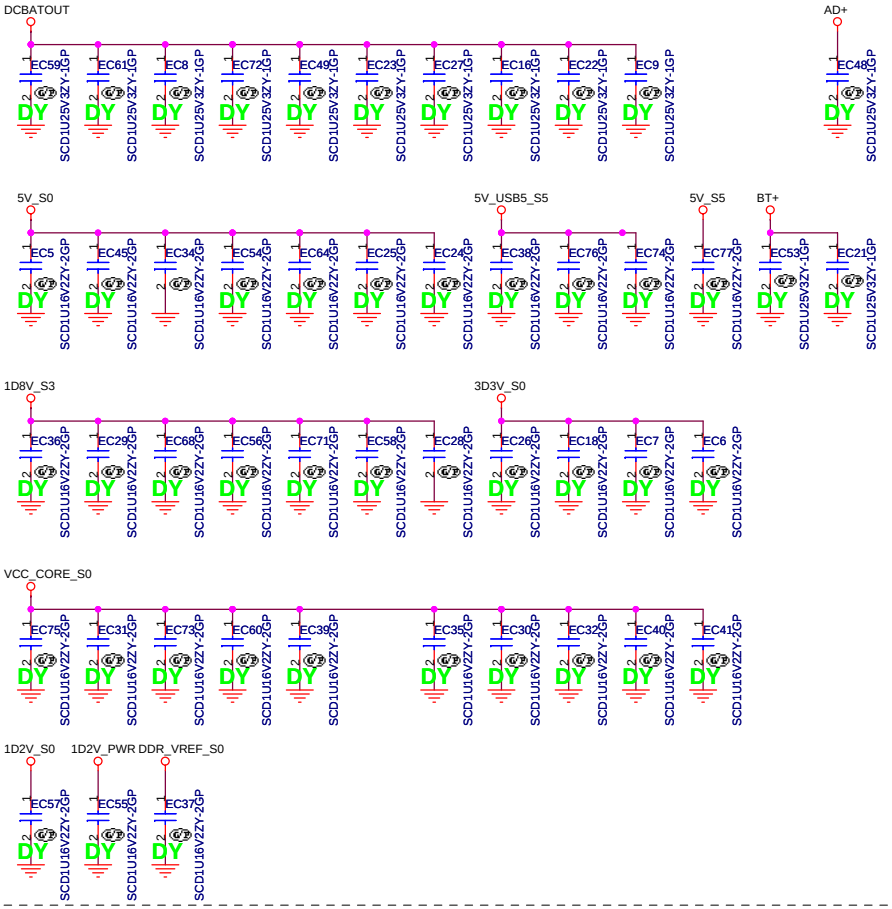
BOTTOM SIDE:







EMI CAP



<Variant Name>

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Title: **SPRING & BOSS**

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