Pamirs UMA Block Diagram

笔记本技术联盟
www.bbjianmeng.com

Project code : 91.4S401.001
PCB P/N :06228
Revision : SB

CLK GEN
ICS9LPRS355AKLFT-GP
3

Intel CPU
Meron 2M/4M SV
FSB:667 or 800 MHz
4,5,6

Host BUS 533/667MHz

DDRII 533/667 Slot 0 13
DDRII 533/667 Slot 1 14
DDRII 667 Channel A
DDR II 667 Channel B

Crestline-GM/GML
AGTL+ CPU I/F DDR I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
7,8,9,10,11,12

RGB CRT → CRT 15
LVDS → LCD 16
SVIDEO → TVOUT 15
PCIE x 16

DMI I/F 100MHz

1394 25
SD/SDIO/MMC MS/MS Pro/xD 25
1394 Ricoh R5C832 CardReader 24,25
PCI

INTEL ICH8-M
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
18,19,20,21

RJ45 CONN 28
10/100 NIC Marvell 88E8039 27
LCI

USB 2.0 → CAMERA 32, BLUE TOOTH 32, USB x 3 23
SATA → HDD 23
PATA → ODD 23
LPC Bus → TPM SLB9635TT 34

RJ11 CONN 29
AMOM
MODEM CX20548
HD AUDIO CODEC CX20549-12Z 29
HD Audio
INTERNAL ARRAY MIC
MIC IN
LINE OUT
SPDIF
2CH SPEAKER
OP AMP APA2031 30

Ricoh R5538 28
PCIE+USB 2.0
PCIE x 1
PCIE x 1 USB 2.0 x 1

New Card 28
Mini-Card 802.11a/b/g 26
Mini-Card WWAN 26

KBC ENE KB3910SF 31
Capacity Button 32
Touch Pad 32
Int. KB 32
CIR
Thermal & Fan G792 22
Flash ROM 1MB 33

DOCK
CRT MIC IN LINE OUT S/PDIF TVOUT 10/100 Ethernet CIR

SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_AUX_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D5V_S0 1D8V_S3

SYSTEM DC/DC
ISL6269CRZ

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Pamirs | Rev: SC
Date: Wednesday, November 08, 2006 | Sheet 1 of 41

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	TP3	AZ_DOUT_ICH	Description
0	0	0	RSVD
0	0	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

8.2K PULL HIGH

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

19,21 +RTCVCC → +RTCVCC
4,5,6,7,9,10,11,19,21,38,41 1D05V_S0 → 1D05V_S0
3,7,10,21,38 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
5,10,17,19,20,21,26,28,37,38,41 1D5V_S0 → 1D5V_S0
7,10,11,13,14,37,38,41 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5
29,30 3D3V_AUD_S0 → 3D3V_AUD_S0
19,31,32,33,36,39,40 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
3,4,7,9,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,41 3D3V_S0 → 3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,41 3D3V_S5 → 3D3V_S5
22,29,31,34,36 5V_AUX_S5 → 5V_AUX_S5
16,23,32,33,34,36,37,38 5V_S3 → 5V_S3
15,16,17,20,21,22,23,26,29,30,31,32,33,34,35,41 5V_S0 → 5V_S0
16,21,34,37,38 5V_S5 → 5V_S5
17,39,40,41 AD+ → AD+
16,17,34,35,36,37,38,39,41 DCBATOUT → DCBATOUT
13,14,38,41 DDR_VREF_S0 → DDR_VREF_S0
7,13,14,38 DDR_VREF_S3 → DDR_VREF_S3
22,31,33,39 KBC_3D3V_AUX → KBC_3D3V_AUX
16 LCDVDD_S0 → LCDVDD_S0
5,6,35 VCC_CORE_S0 → VCC_CORE_S0

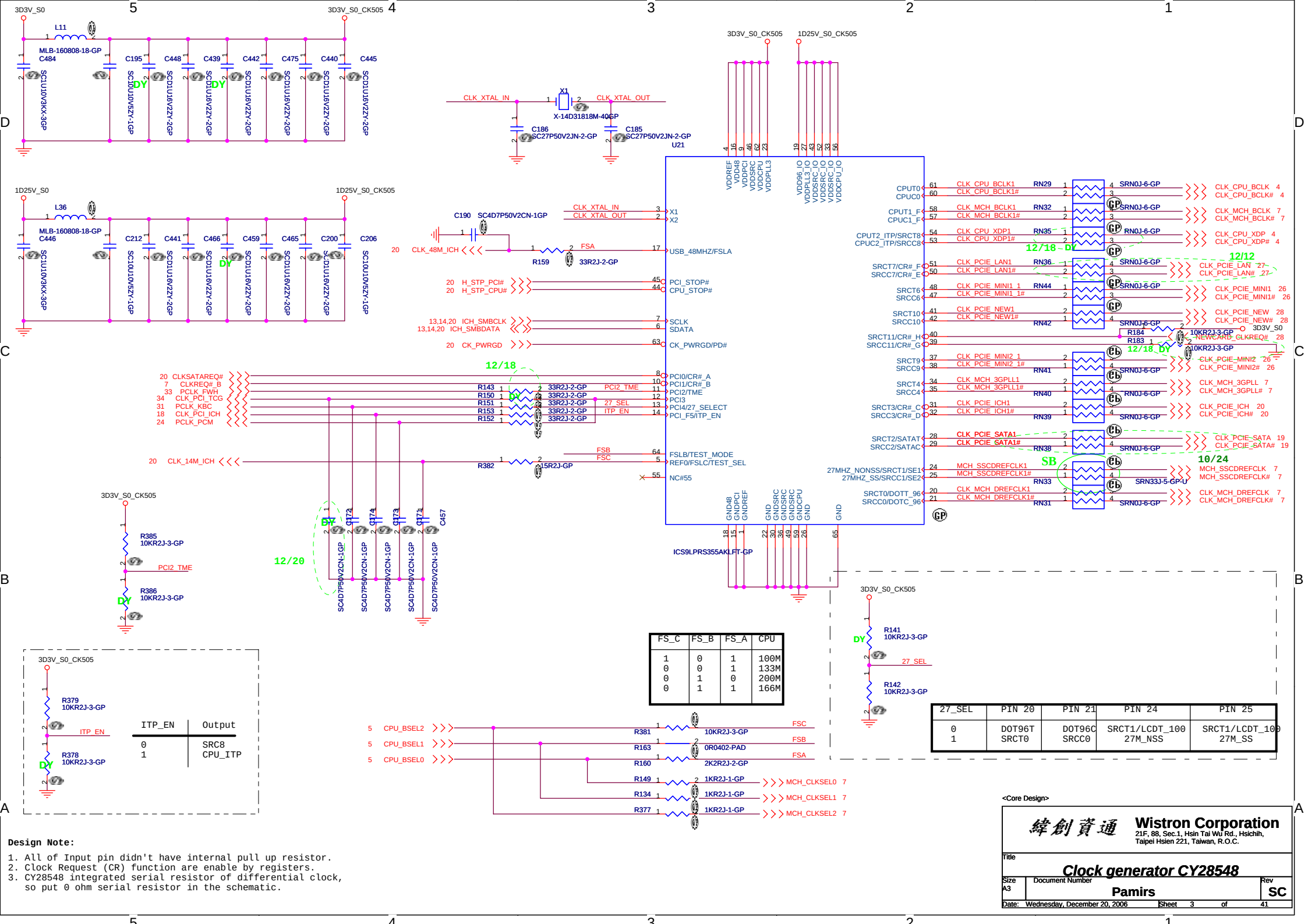
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

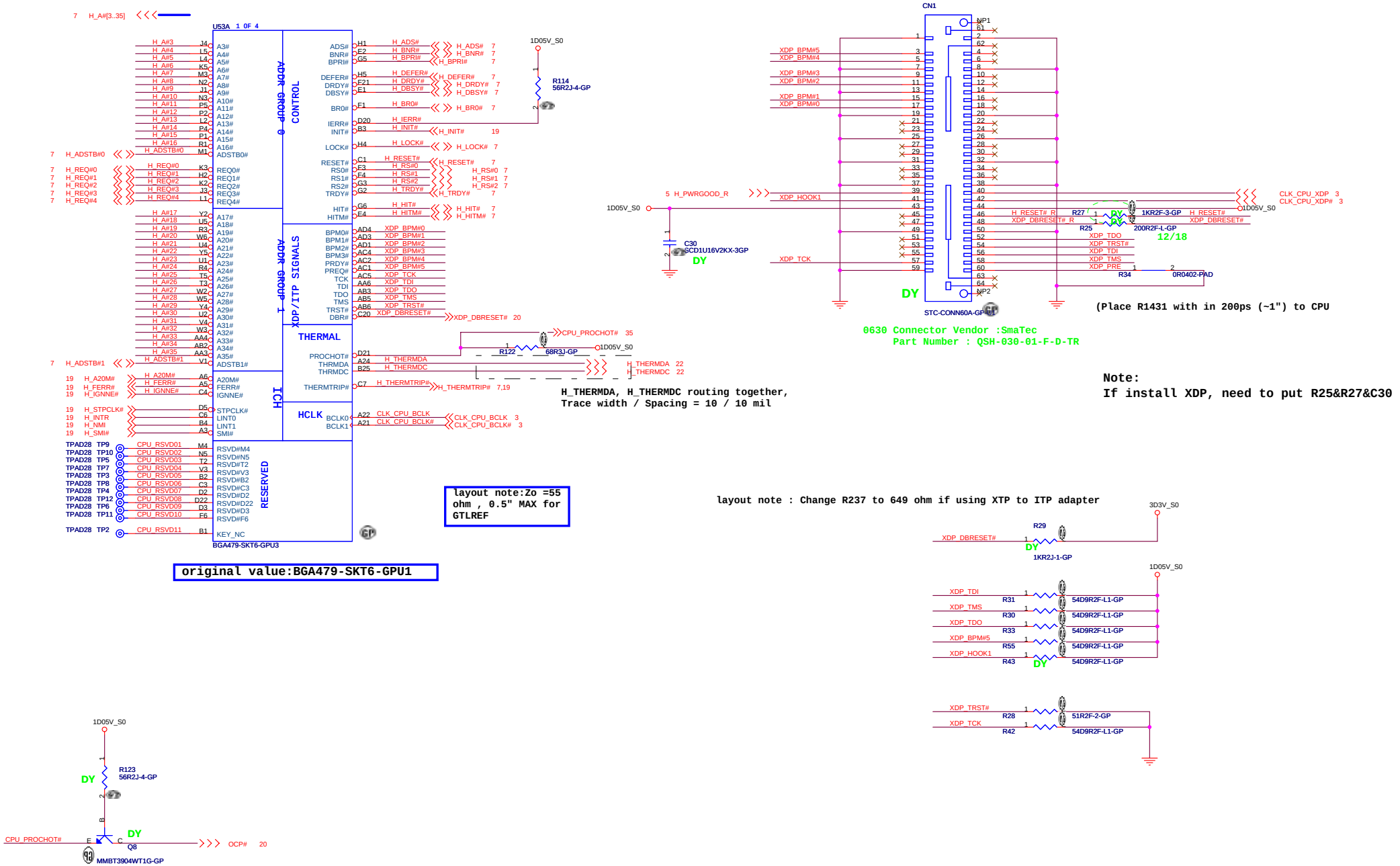
Title: Table of Content

Size	Document Number	Rev
A3	Pamirs	SC

Date: Wednesday, November 08, 2006 Sheet 2 of 41

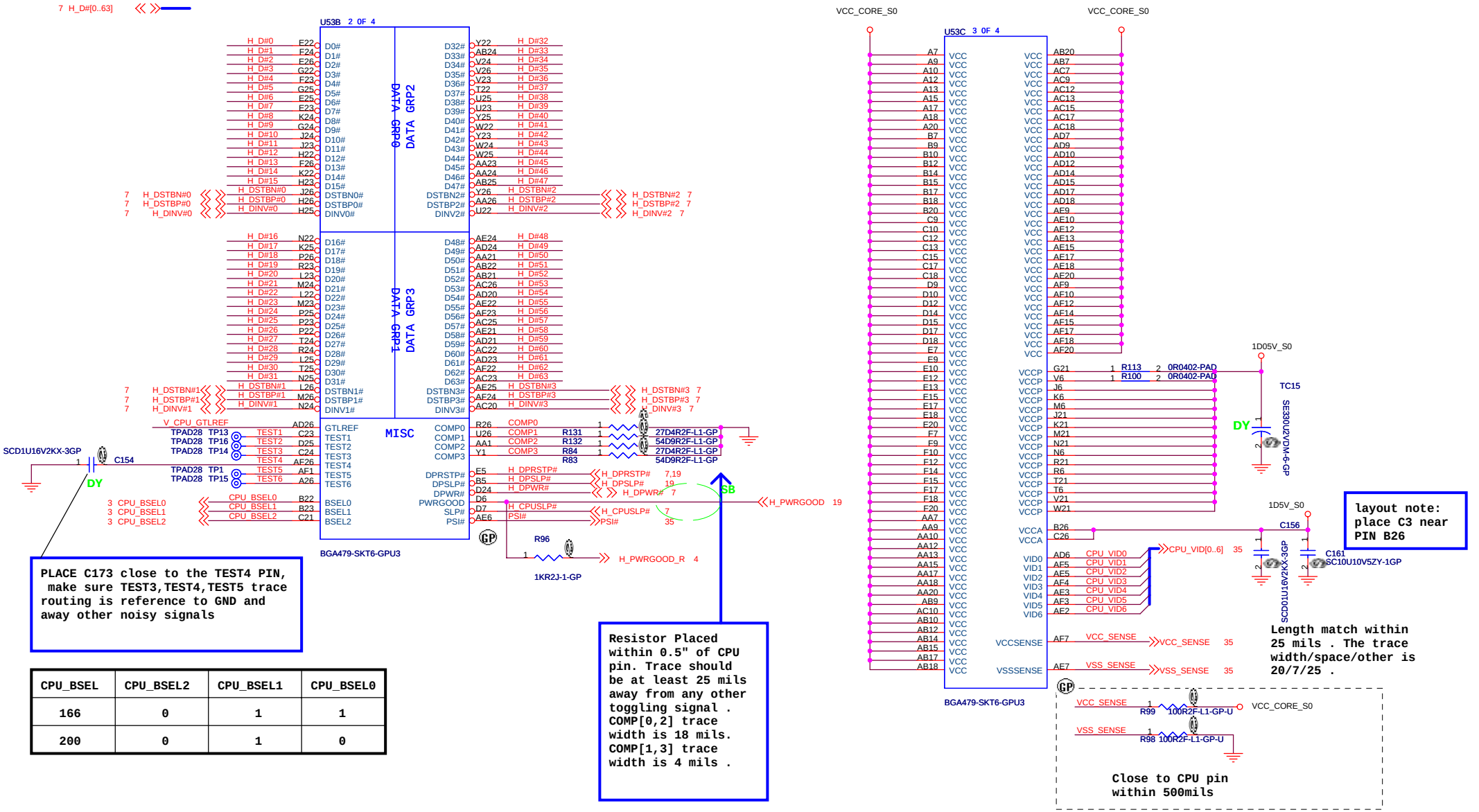

3D3V_S0
L11
MLB-160808-18-GP
C484
C195
C448
C439
C442
C475
C440
C445
SC1U10V3KX-3GP
SC10U10V5ZY-1GP
SC1U16V2ZY-2GP
DY
3D3V_S0_CK505
1D25V_S0
L36
MLB-160808-18-GP
C446
C212
C441
C466
C459
C465
C200
C206
SC10U10V5ZY-1GP
SC1U16V2ZY-2GP
SC1U10V3KX-3GP
1D25V_S0_CK505
SC10U10V5ZX-1GP
CLK_XTAL_IN
CLK_XTAL_OUT
X1
X-14D31818M-40GP
C186
SC27P50V2JN-2GP
C185
SC27P50V2JN-2GP
U21
C190
SC4D7P50V2CN-1GP
R159
33R2J-2-GP
CLK_48M_ICH
FSA
USB_48MHZ/FSLA
H_STP_PCI#
H_STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
12/18
CLKSATAREQ#
CLKREQ#_B
PCLK_FWH
CLK_PCI_TCG
PCLK_KBC
CLK_PCI_ICH
PCLK_PCM
R143
R150
R151
R153
R152
33R2J-2-GP
PCI2_TME
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_14M_ICH
R382
15R2J-GP
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS9LPRS355AKLFT-GP
3D3V_S0_CK505
1D25V_S0_CK505
R385
10KR2J-3-GP
R386
10KR2J-3-GP
C172
C174
C173
C171
C457
SC4D7P50V2CN-1GP
12/20
CPUT0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
SRCT0/DOTT_96
SRCC0/DOTC_96
CLK_CPU_BCLK1
CLK_CPU_BCLK1#
CLK_MCH_BCLK1
CLK_MCH_BCLK1#
CLK_CPU_XDP1
CLK_CPU_XDP1#
CLK_PCIE_LAN1
CLK_PCIE_LAN1#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_PCIE_NEW1
CLK_PCIE_NEW1#
CLK_PCIE_MINI2_1
CLK_PCIE_MINI2_1#
CLK_MCH_3GPLL1
CLK_MCH_3GPLL1#
CLK_PCIE_ICH1
CLK_PCIE_ICH1#
CLK_PCIE_SATA1
CLK_PCIE_SATA1#
MCH_SSCDREFCLK1
MCH_SSCDREFCLK1#
CLK_MCH_DREFCLK1
CLK_MCH_DREFCLK1#
RN29
RN32
RN35
RN36
RN44
RN42
RN41
RN40
RN39
RN38
RN33
RN31
SRN0J-6-GP
SRN33J-5-GP-U
R184
10KR2J-3-GP
R183
NEWCARD_CLKREQ#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_CPU_XDP
CLK_CPU_XDP#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_NEW
CLK_PCIE_NEW#
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_PCIE_ICH
CLK_PCIE_ICH#
CLK_PCIE_SATA
CLK_PCIE_SATA#
MCH_SSCDREFCLK
MCH_SSCDREFCLK#
CLK_MCH_DREFCLK
CLK_MCH_DREFCLK#
12/18
12/12
10/24
SB
R141
10KR2J-3-GP
R142
10KR2J-3-GP
27_SEL
FS_C | FS_B | FS_A | CPU
1 | 0 | 1 | 100M
0 | 0 | 1 | 133M
0 | 1 | 0 | 200M
0 | 1 | 1 | 166M
27_SEL | PIN 20 | PIN 21 | PIN 24 | PIN 25
0 | DOT96T | DOT96C | SRCT1/LCDT_100 | SRCT1/LCDT_100
1 | SRCT0 | SRCC0 | 27M_NSS | 27M_SS
R379
10KR2J-3-GP
R378
10KR2J-3-GP
ITP_EN
ITP_EN | Output
0 | SRC8
1 | CPU_ITP
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
R381
10KR2J-3-GP
R163
0R0402-PAD
R160
2K2R2J-2-GP
R149
R134
R377
1KR2J-1-GP
FSC
FSB
FSA
MCH_CLKSEL0
MCH_CLKSEL1
MCH_CLKSEL2
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock generator CY28548
Size A3
Document Number
Pamirs
Rev SC
Date: Wednesday, December 20, 2006
Sheet 3 of 41

XDP Connector



<core_design>

蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Meron(1/3)-AGTL+/XDP***	
Size: Custom	Document Number: **Pamirs**	Rev: **SC**
Date: Wednesday, December 20, 2006	Sheet 4 of 41	
</core_design>



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

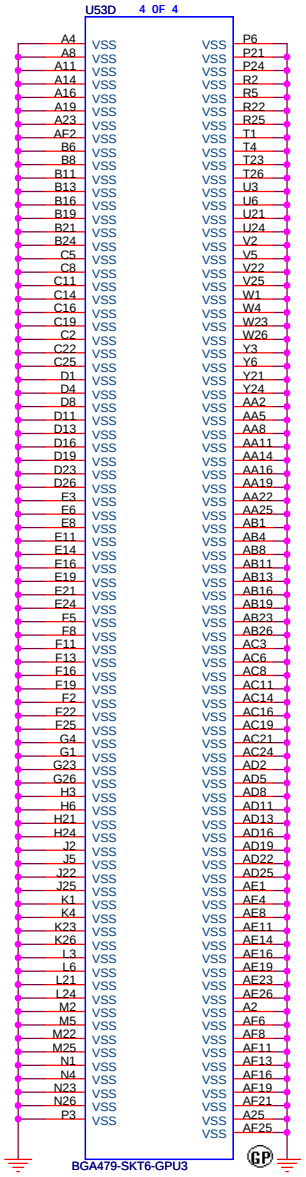
<Core Design>

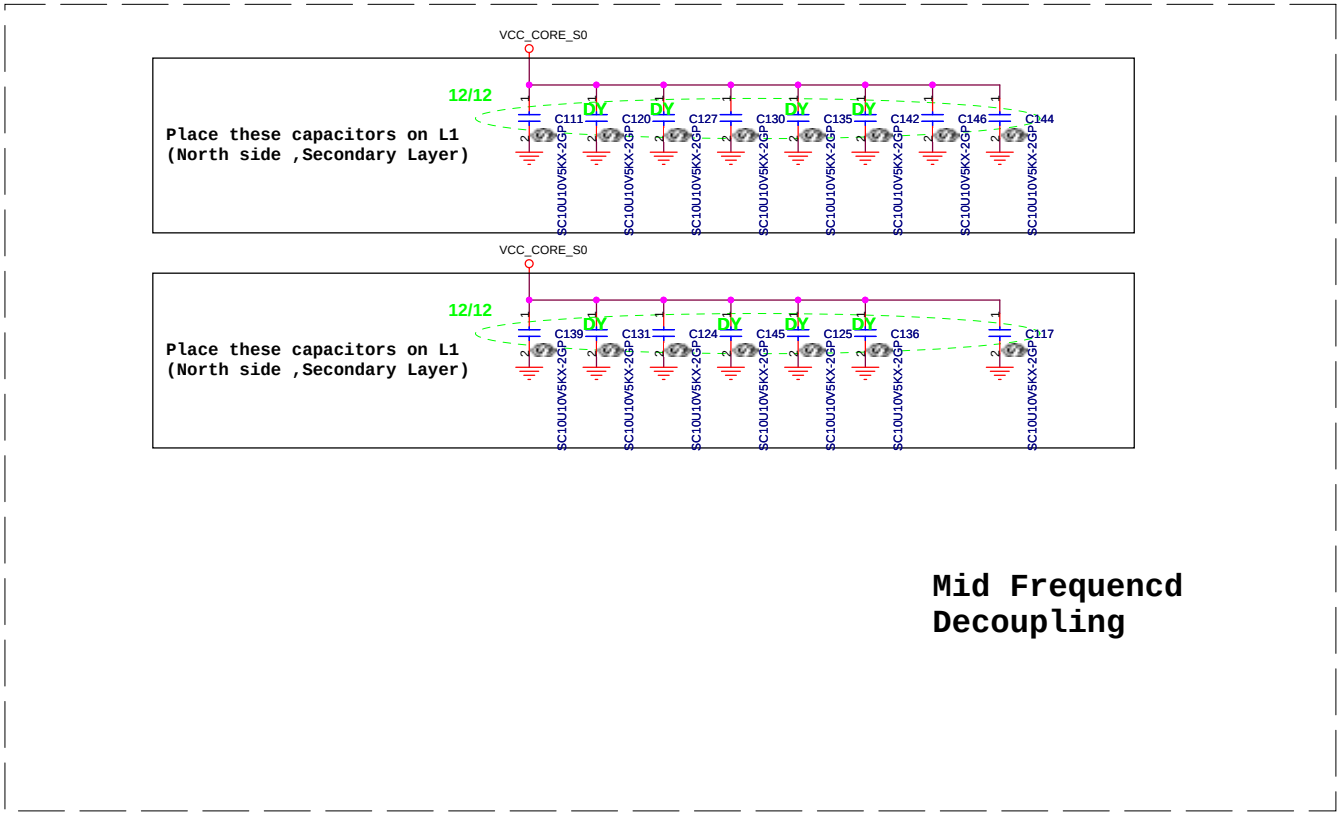
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

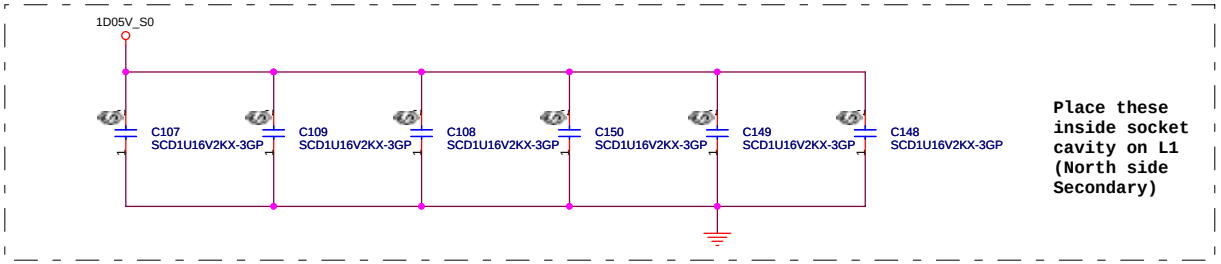
Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Pamirs | Rev: SC

Date: Friday, December 15, 2006 | Sheet 5 of 41







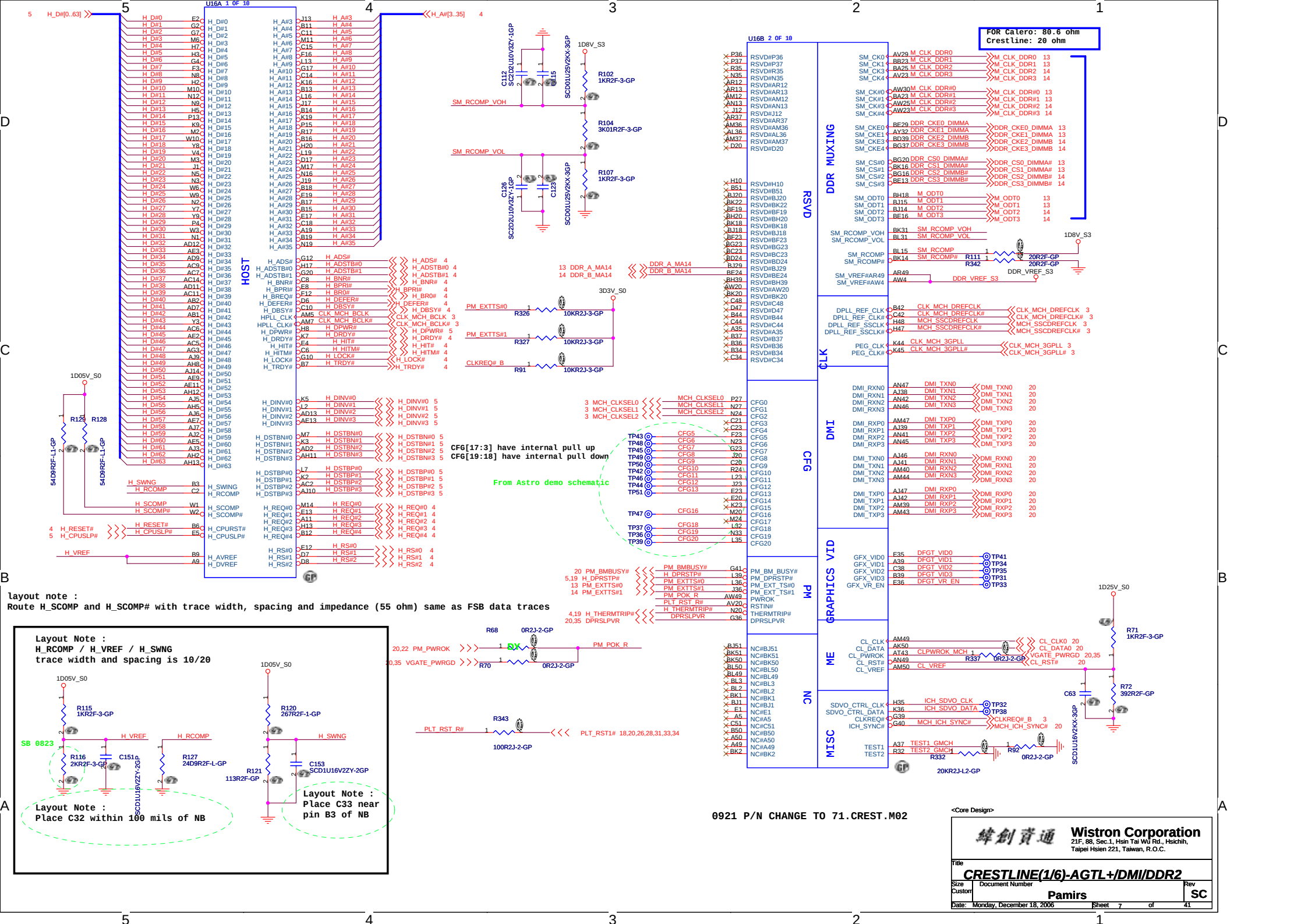
<Core Design>

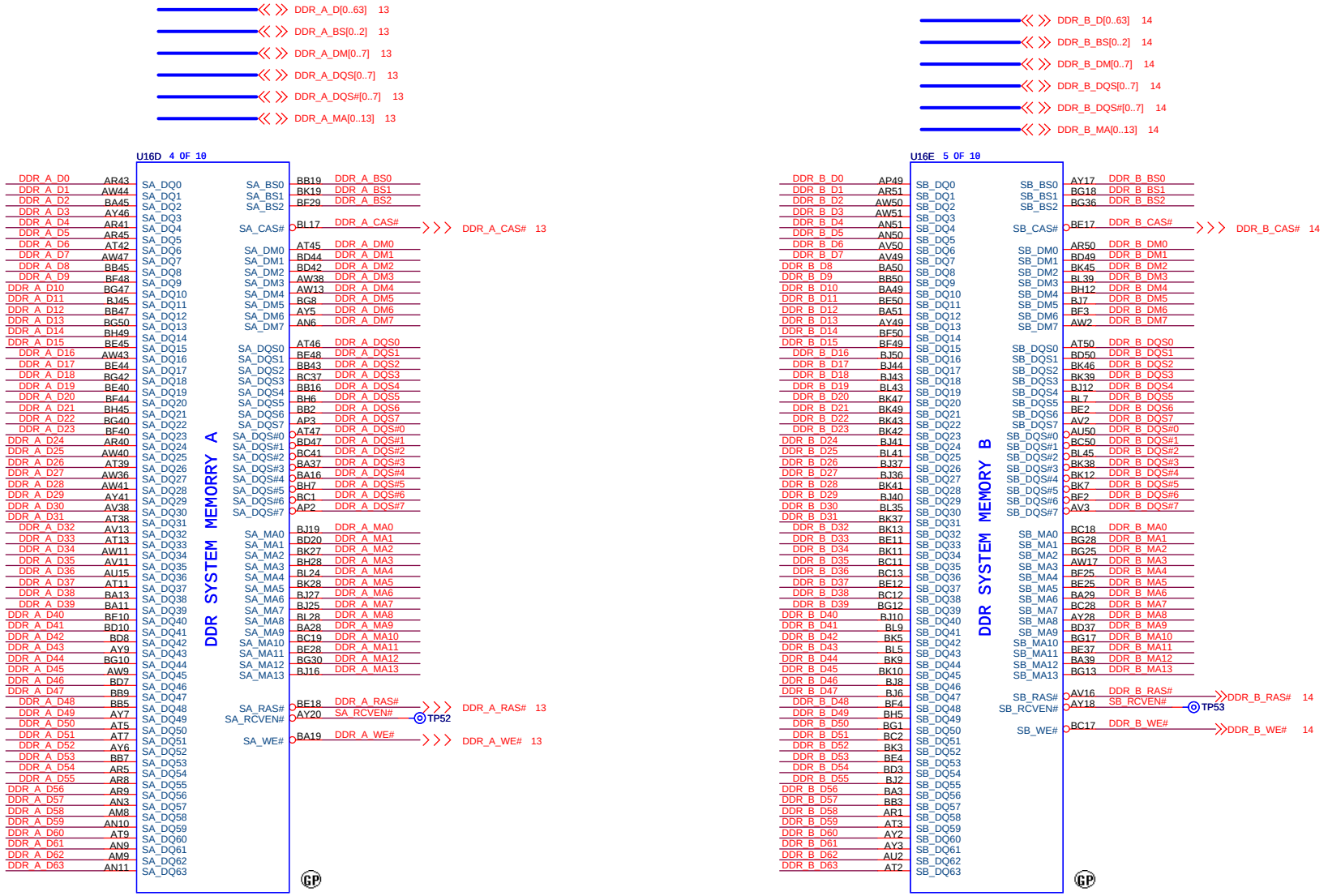
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Meron(3/3)-GND&Bypass

Size	Document Number	Rev
A3	Pamirs	SC

Date: Wednesday, December 20, 2006 Sheet 6 of 41


FOR Calero: 80.6 ohm
Crestline: 20 ohm
U16A 1 OF 10
HOST
U16B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
From Astro demo schematic
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note :
Place C32 within 100 mils of NB
Layout Note :
Place C33 near
pin B3 of NB
SB 0823
0921 P/N CHANGE TO 71.CREST.M02
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
Size Custom
Document Number
Pamirs
Rev
SC
Date: Monday, December 18, 2006
Sheet 7 of 41



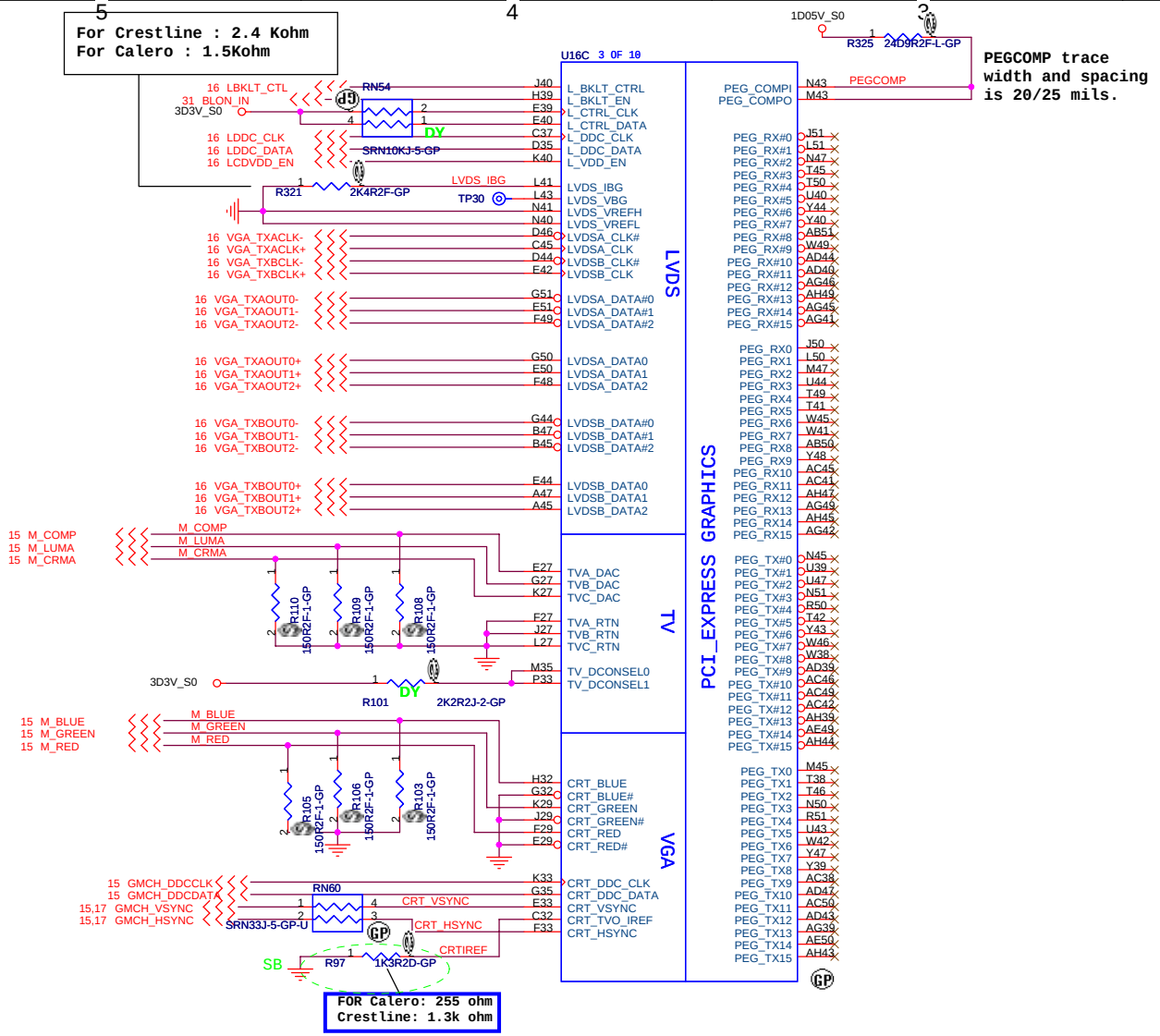
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
A3	Pamirs	SC

Date: Monday, December 18, 2006 Sheet 8 of 41



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

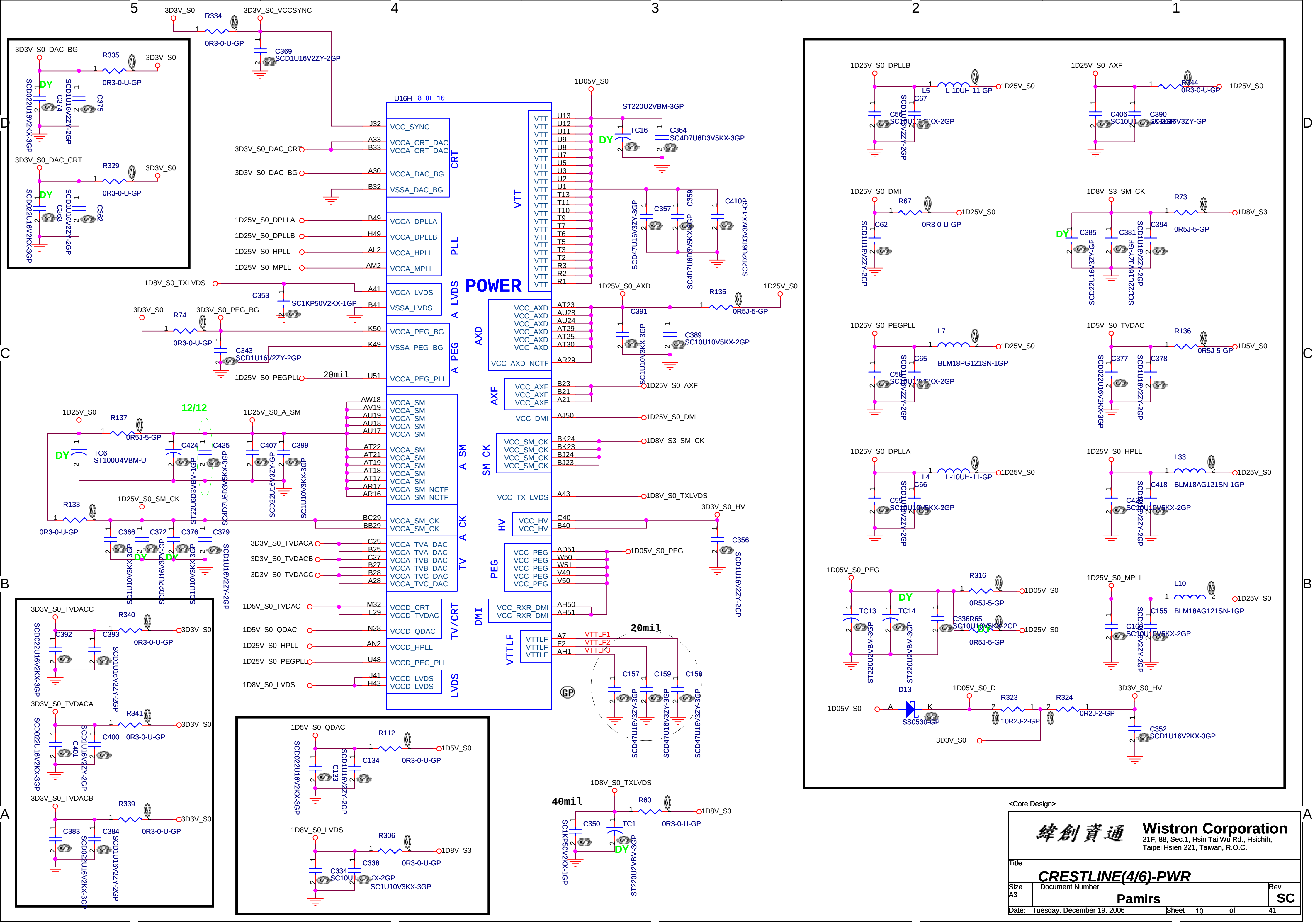
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size: A3 | Document Number: Pamirs | Rev: SC

Date: Monday, December 18, 2006 | Sheet 9 of 41



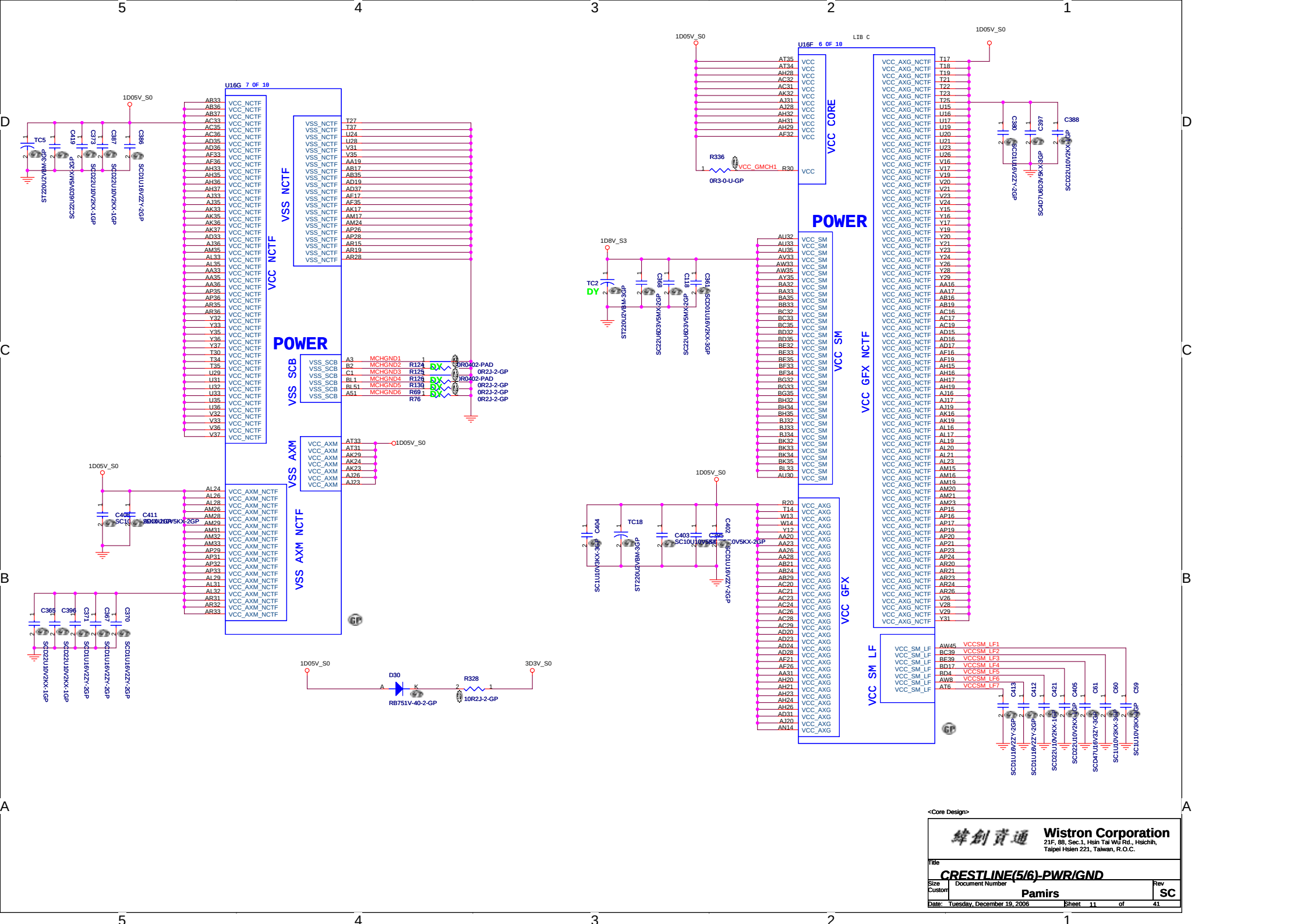
<Core Design>

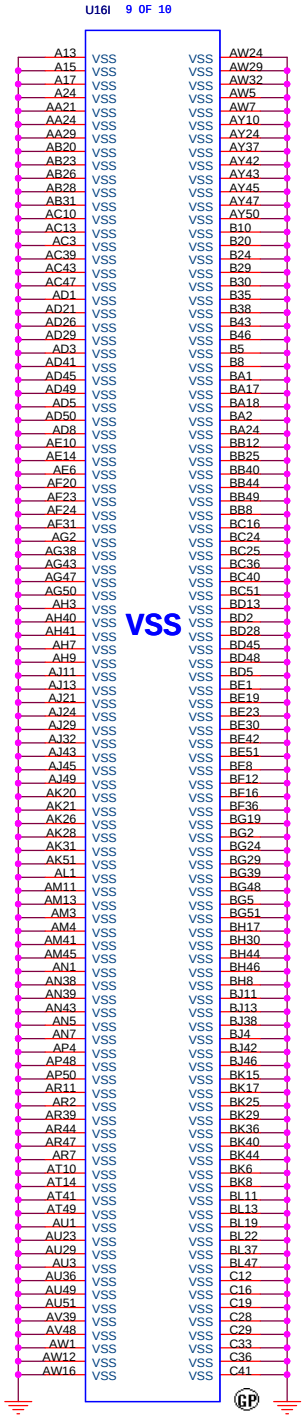
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

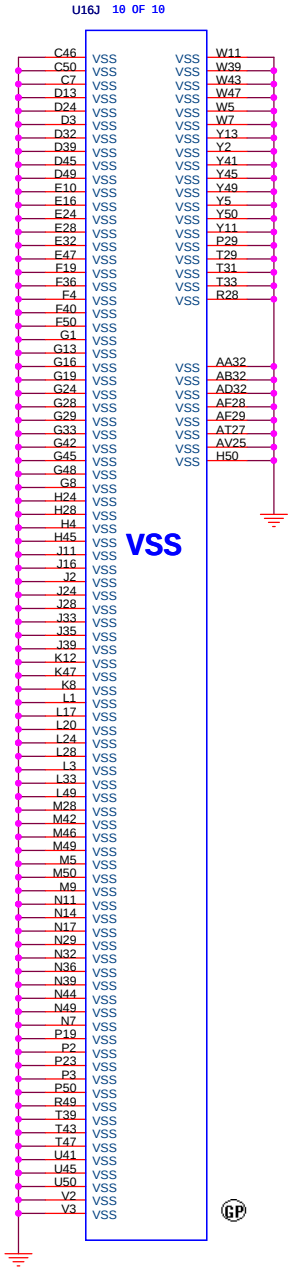
Title: CRESTLINE(4/6)-PWR

Size: A3 | Document Number: Pamirs | Rev: SC

Date: Tuesday, December 19, 2006 | Sheet 10 of 41


U16G 7 OF 10
POWER
VSS NCTF
VCC NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
1D05V_S0
3D3V_S0
D30
RB751V-40-2-GP
R328
10R2J-2-GP
U16F 6 OF 10
LIB C
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
1D8V_S3
R336
0R3-0-U-GP
VCC_GMCH1
0R0402-PAD
0R2J-2-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(5/6)-PWR/GND
Size
Custom
Document Number
Pamirs
Rev
SC
Date: Tuesday, December 19, 2006
Sheet 11 of 41





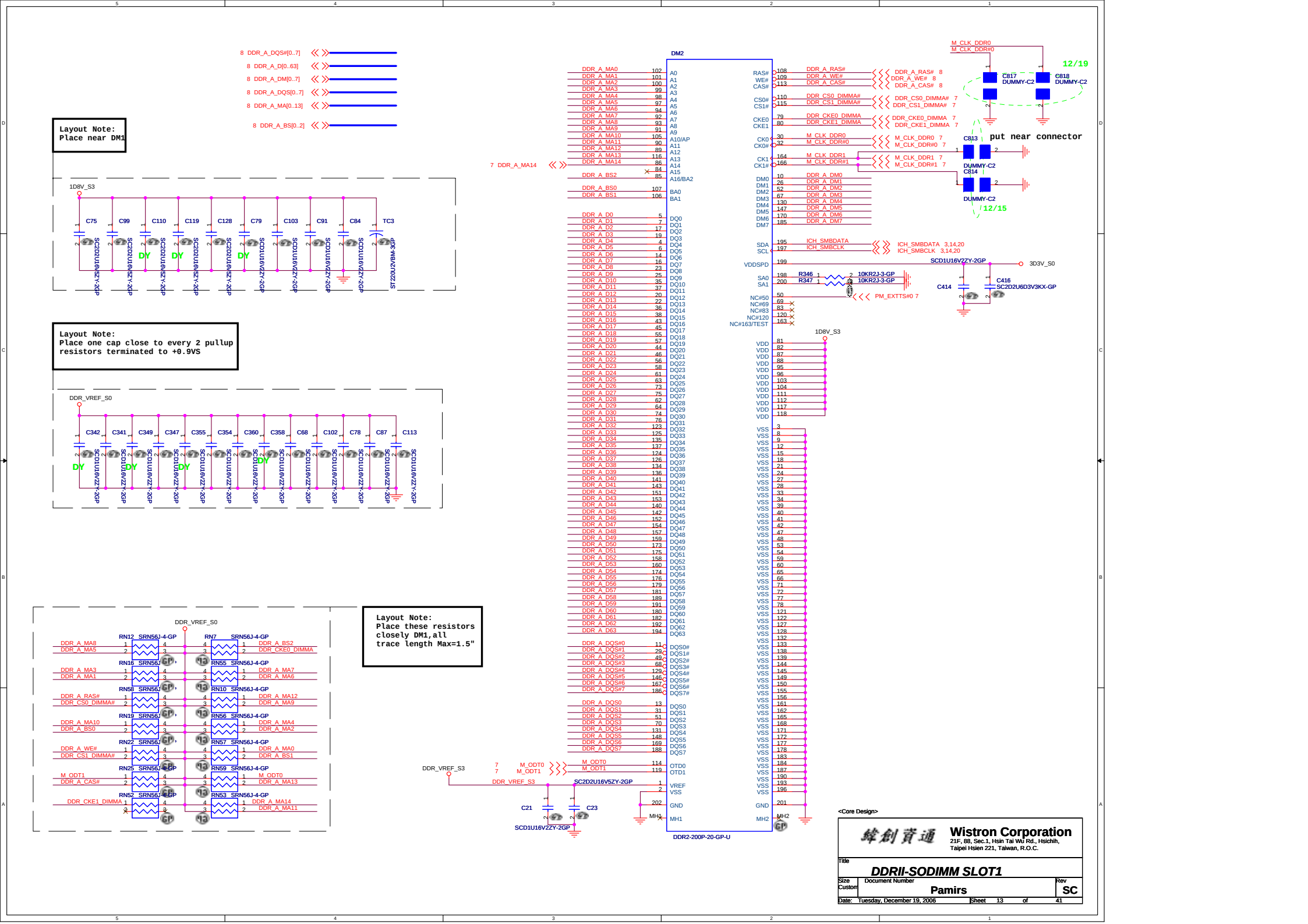
<Core Design>

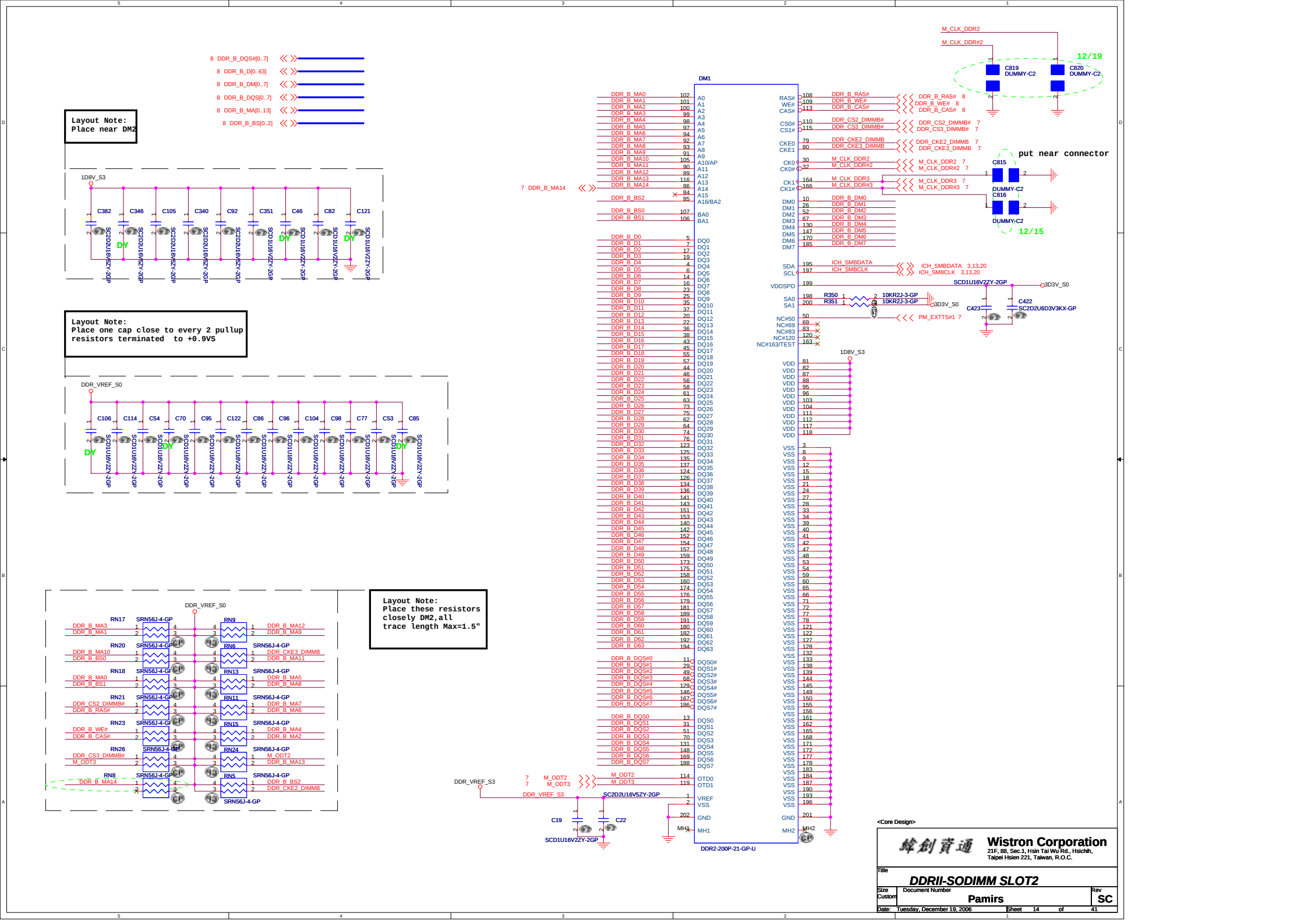
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
A3	Pamirs	SC

Date: Monday, December 18, 2006 Sheet 12 of 41


8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C75 C99 C110 C119 C128 C79 C103 C91 C84 TC3
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C342 C341 C349 C347 C355 C354 C360 C358 C68 C102 C78 C87 C113
DY
DDR_VREF_S0
RN12 SRN56J-4-GP
DDR_A_MA8
DDR_A_MA5
RN7 SRN56J-4-GP
DDR_A_BS2
DDR_CKE0_DIMMA
RN16 SRN56J
DDR_A_MA3
DDR_A_MA1
RN55 SRN56J-4-GP
DDR_A_MA7
DDR_A_MA6
RN58 SRN56J
DDR_A_RAS#
DDR_CS0_DIMMA#
RN10 SRN56J-4-GP
DDR_A_MA12
DDR_A_MA9
RN19 SRN56J
DDR_A_MA10
DDR_A_BS0
RN56 SRN56J-4-GP
DDR_A_MA4
DDR_A_MA2
RN22 SRN56J
DDR_A_WE#
DDR_CS1_DIMMA#
RN57 SRN56J-4-GP
DDR_A_MA0
DDR_A_BS1
RN25 SRN56J-4-GP
M_ODT1
DDR_A_CAS#
RN59 SRN56J-4-GP
M_ODT0
DDR_A_MA13
DDR_CKE1_DIMMA
RN52 SRN56J-4-GP
RN53 SRN56J-4-GP
DDR_A_MA14
DDR_A_MA11
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
DDR_A_MA0 DDR_A_MA1 DDR_A_MA2 DDR_A_MA3 DDR_A_MA4 DDR_A_MA5 DDR_A_MA6 DDR_A_MA7 DDR_A_MA8 DDR_A_MA9 DDR_A_MA10 DDR_A_MA11 DDR_A_MA12 DDR_A_MA13 DDR_A_MA14
DDR_A_BS2 DDR_A_BS0 DDR_A_BS1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D4 DDR_A_D5 DDR_A_D6 DDR_A_D7 DDR_A_D8 DDR_A_D9 DDR_A_D10 DDR_A_D11 DDR_A_D12 DDR_A_D13 DDR_A_D14 DDR_A_D15 DDR_A_D16 DDR_A_D17 DDR_A_D18 DDR_A_D19 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27 DDR_A_D28 DDR_A_D29 DDR_A_D30 DDR_A_D31 DDR_A_D32 DDR_A_D33 DDR_A_D34 DDR_A_D35 DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D44 DDR_A_D45 DDR_A_D46 DDR_A_D47 DDR_A_D48 DDR_A_D49 DDR_A_D50 DDR_A_D51 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59 DDR_A_D60 DDR_A_D61 DDR_A_D62 DDR_A_D63
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
RAS# WE# CAS#
DDR_A_RAS# DDR_A_WE# DDR_A_CAS#
DDR_A_RAS# 8 DDR_A_WE# 8 DDR_A_CAS# 8
CS0# CS1#
DDR_CS0_DIMMA# DDR_CS1_DIMMA#
DDR_CS0_DIMMA# 7 DDR_CS1_DIMMA# 7
CKE0 CKE1
DDR_CKE0_DIMMA DDR_CKE1_DIMMA
DDR_CKE0_DIMMA 7 DDR_CKE1_DIMMA 7
CK0 CK0#
M_CLK_DDR0 M_CLK_DDR#0
M_CLK_DDR0 7 M_CLK_DDR#0 7
CK1 CK1#
M_CLK_DDR1 M_CLK_DDR#1
M_CLK_DDR1 7 M_CLK_DDR#1 7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7
SDA SCL
ICH_SMBDATA ICH_SMBCLK
ICH_SMBDATA 3,14,20 ICH_SMBCLK 3,14,20
VDDSPD
SCD1U16V2ZY-2GP
3D3V_S0
SA0 SA1
R346 10KR2J-3-GP
R347 10KR2J-3-GP
C414
C416 SC2D2U6D3V3KX-GP
PM_EXTTS#0 7
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
1D8V_S3
VDD
VSS
M_CLK_DDR0
M_CLK_DDR#0
12/19
C817 DUMMY-C2
C818 DUMMY-C2
C813
put near connector
DUMMY-C2
C814
DUMMY-C2
12/15
DDR_VREF_S3
7 M_ODT0
7 M_ODT1
M_ODT0 M_ODT1
SC2D2U16V5ZY-2GP
C21 C23
SCD1U16V2ZY-2GP
VREF VSS GND MH1 MH2
DDR2-200P-20-GP-U
<Core Design>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
Pamirs
Rev SC
Date: Tuesday, December 19, 2006
Sheet 13 of 41


8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
C382
C346
C105
C340
C92
C351
C46
C82
C121
SCD2U16V2ZY-2GP
SCD1U16V2ZY-2GP
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C106
C114
C54
C70
C95
C122
C86
C96
C104
C98
C77
C53
C85
SCD1U16V2ZY-2GP
DY
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
DDR_VREF_S0
RN17
RN20
RN18
RN21
RN23
RN26
RN8
RN9
RN6
RN13
RN11
RN15
RN24
RN5
SRN56J-4-GP
DDR_B_MA3
DDR_B_MA1
DDR_B_MA12
DDR_B_MA9
DDR_B_MA10
DDR_B_BS0
DDR_CKE3_DIMMB
DDR_B_MA11
DDR_B_MA0
DDR_B_BS1
DDR_B_MA5
DDR_B_MA8
DDR_CS2_DIMMB#
DDR_B_RAS#
DDR_B_MA7
DDR_B_MA6
DDR_B_WE#
DDR_B_CAS#
DDR_B_MA4
DDR_B_MA2
DDR_CS3_DIMMB#
M_ODT3
M_ODT2
DDR_B_MA13
DDR_B_MA14
DDR_B_BS2
DDR_CKE2_DIMMB
DM1
DDR2-200P-21-GP-U
DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14
DDR_B_BS2
DDR_B_BS0
DDR_B_BS1
DDR_B_D0
DDR_B_D1
DDR_B_D2
DDR_B_D3
DDR_B_D4
DDR_B_D5
DDR_B_D6
DDR_B_D7
DDR_B_D8
DDR_B_D9
DDR_B_D10
DDR_B_D11
DDR_B_D12
DDR_B_D13
DDR_B_D14
DDR_B_D15
DDR_B_D16
DDR_B_D17
DDR_B_D18
DDR_B_D19
DDR_B_D20
DDR_B_D21
DDR_B_D22
DDR_B_D23
DDR_B_D24
DDR_B_D25
DDR_B_D26
DDR_B_D27
DDR_B_D28
DDR_B_D29
DDR_B_D30
DDR_B_D31
DDR_B_D32
DDR_B_D33
DDR_B_D34
DDR_B_D35
DDR_B_D36
DDR_B_D37
DDR_B_D38
DDR_B_D39
DDR_B_D40
DDR_B_D41
DDR_B_D42
DDR_B_D43
DDR_B_D44
DDR_B_D45
DDR_B_D46
DDR_B_D47
DDR_B_D48
DDR_B_D49
DDR_B_D50
DDR_B_D51
DDR_B_D52
DDR_B_D53
DDR_B_D54
DDR_B_D55
DDR_B_D56
DDR_B_D57
DDR_B_D58
DDR_B_D59
DDR_B_D60
DDR_B_D61
DDR_B_D62
DDR_B_D63
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7
DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7
M_ODT2
M_ODT3
DDR_VREF_S3
SC2D2U16V5ZY-2GP
SCD1U16V2ZY-2GP
C19
C22
RAS#
WE#
CAS#
CS0#
CS1#
CKE0
CKE1
CK0
CK0#
CK1
CK1#
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
SDA
SCL
VDDSPD
SA0
SA1
NC#50
NC#69
NC#83
NC#120
NC#163/TEST
VDD
VSS
GND
MH1
MH2
DDR_B_RAS#
DDR_B_WE#
DDR_B_CAS#
DDR_CS2_DIMMB#
DDR_CS3_DIMMB#
DDR_CKE2_DIMMB
DDR_CKE3_DIMMB
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
ICH_SMBDATA
ICH_SMBCLK
3,13,20
SCD1U16V2ZY-2GP
3D3V_S0
R350
R351
10KR2J-3-GP
C423
C422
SC2D2U6D3V3KX-GP
PM_EXTTS#1
1D8V_S3
12/19
C819
C820
DUMMY-C2
put near connector
C815
C816
12/15
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size
Custom
Document Number
Pamirs
Rev
SC
Date: Tuesday, December 19, 2006
Sheet 14 of 41

CRT I/F & CONNECTOR

0721

Layout Note:
Place these resistors close to the CRT-out connector

9 M_RED
9 M_GREEN
9 M_BLUE

L3 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

CRT_R → CRT_R 17
CRT_G → CRT_G 17
CRT_B → CRT_B 17

R7 150R2F-1-GP
R6 150R2F-1-GP
R5 150R2F-1-GP
C16 C13 C11 C14 C12 C10 SC10P50V2JN-4GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0
C7 SCD01U16V2KX-3GP
F1 FUSE-1D1A6V-8GP
5V_S0
D4 RB751V-40-2-GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U1 20.20424.015
CRT_R
CRT_G
CRT_B
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON

C8 SC33P50V2JN-3GP DY
C9 SC33P50V2JN-3GP DY
C6 SC22P50V2JN-4GP
C5 SC22P50V2JN-4GP

D10 BAV99-7-F-GP DY
D12 BAV99-7-F-GP DY
DDC_DATA_CON
DDC_CLK_CON

5V_CRT1_S0
U2 PACDN009MR-GP-U DY
GMCH_HSYNC
GMCH_VSYNC
CRT_R
CRT_G
CRT_B

5V_S0
C320 SCD1U16V2ZY-2GP
PR_INSERT 17

9,17 GMCH_HSYNC
9,17 GMCH_VSYNC
U5A TSAHCT125PW-GP
U5B TSAHCT125PW-GP
HSYNC_5
VSYNC_5
RN4 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP
U1 2N7002DW-1-GP
9 GMCH_DDCDATA
17 DDC_CLK_CON
DDC_DATA_CON
DDC_CLK_CON
DDC_DATA_CON 17
GMCH_DDCCLK 9

5V @ ext. CRT side

TV OUT CONN

connector

0721

9 M_CRMA
9 M_COMP
9 M_LUMA

L23 BLM18BB470SN1-GP
L24 BLM18BB470SN1-GP
L25 BLM18BB470SN1-GP

TV_CRMA 17
TV_COMP 17
TV_LUMA 17

R271 150R2F-1-GP
R1 150R2F-1-GP
R2 150R2F-1-GP
C293 C292 C295 C294 C297 C296 SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-18-GP 22.10021.H31
TV_LUMA
TV_CRMA
TV_COMP
LUMA
CRMA
COMP
NC#2
NC#5
GND

D1 BAV99-7-F-GP DY
D3 BAV99-7-F-GP DY
D2 BAV99-7-F-GP DY
3D3V_S0
C1 SCD1U16V2ZY-2GP DY
C3 SCD1U16V2ZY-2GP DY
C2 SCD1U16V2ZY-2GP DY

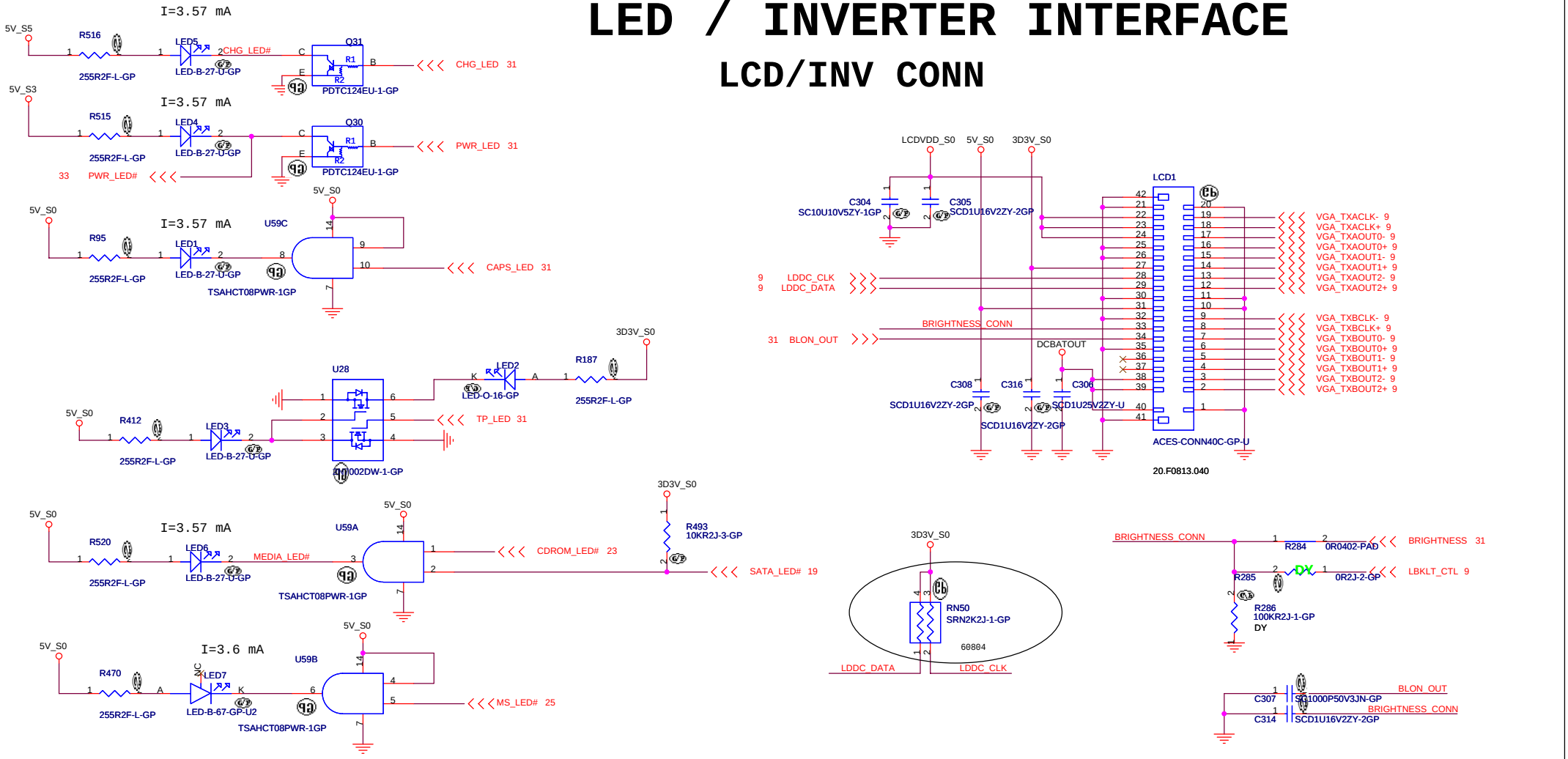
<Core Design>

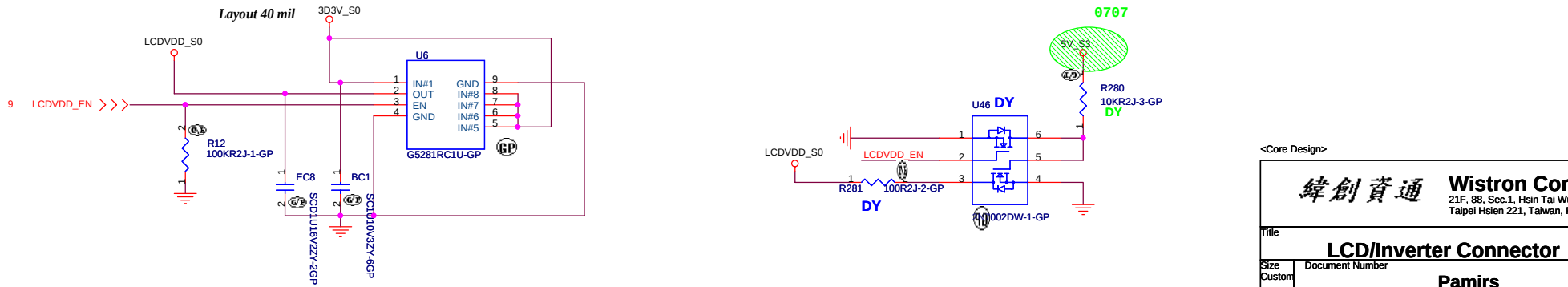
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Pamirs
Rev: SC
Date: Friday, December 15, 2006
Sheet 15 of 41

LED / INVERTER INTERFACE

LCD/INV CONN





<Core Design>

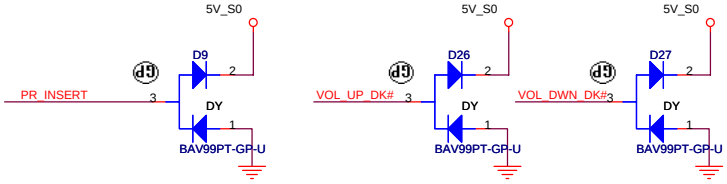
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

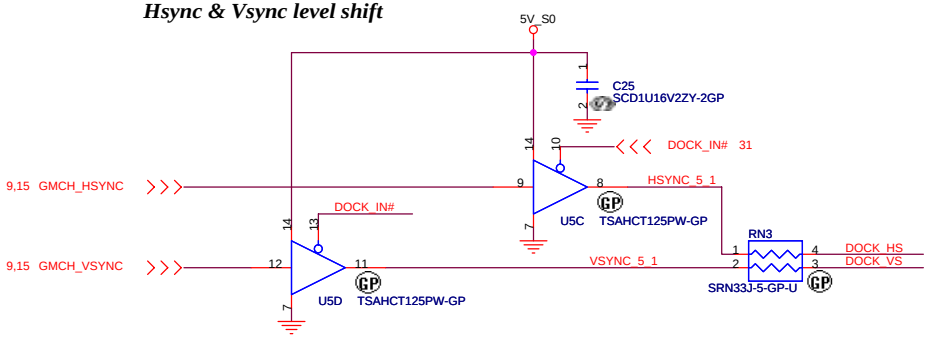
Size	Document Number	Rev
Custom	Pamirs	SC

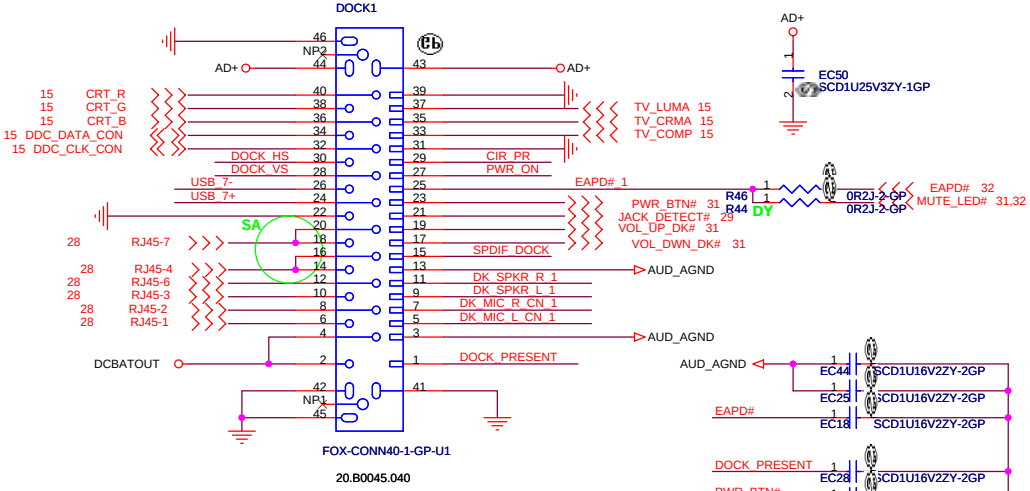
Date: Tuesday, December 19, 2006 Sheet 16 of 41

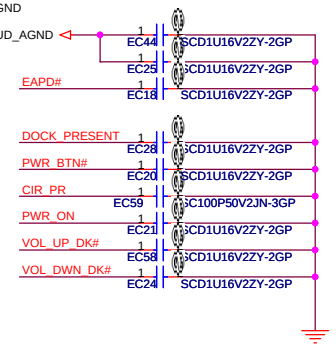
Docking Connector

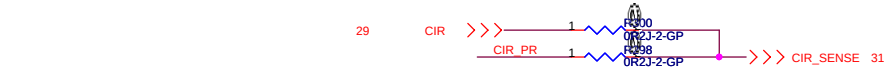


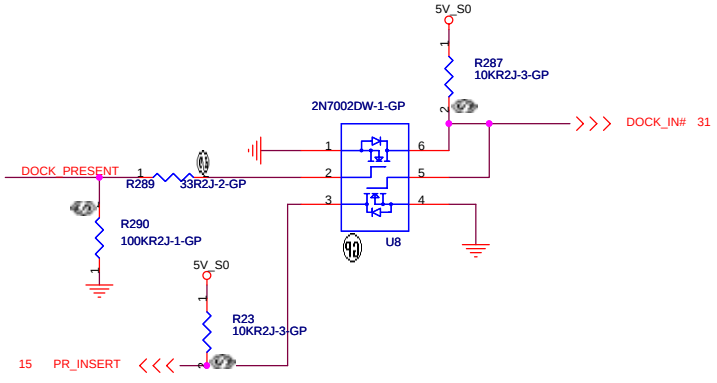
Hsync & Vsync level shift

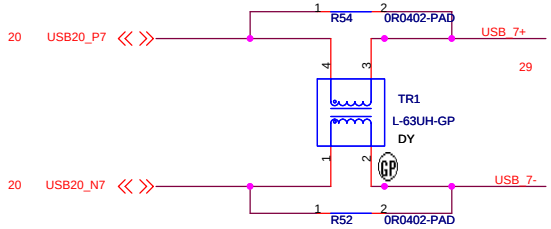


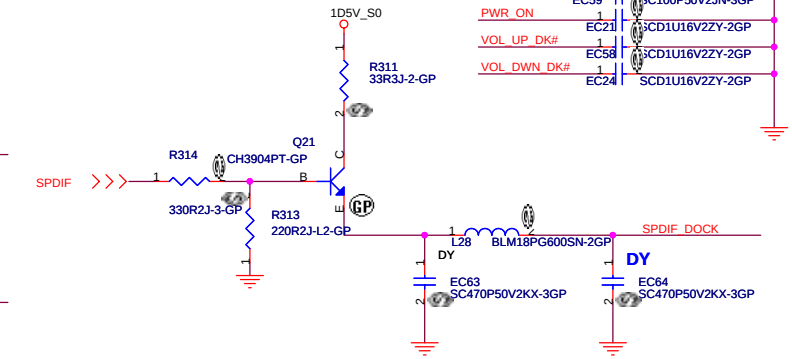


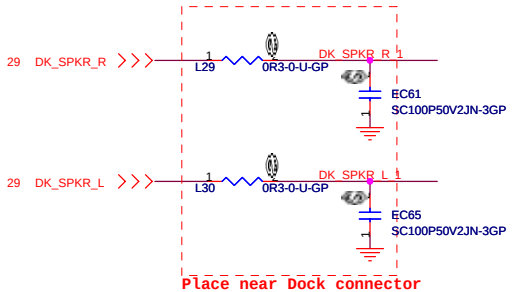


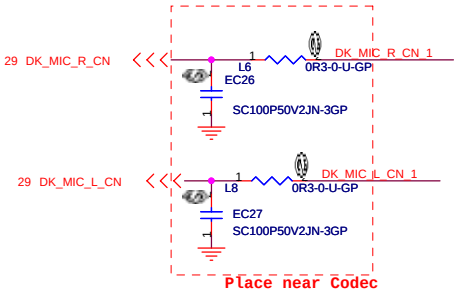


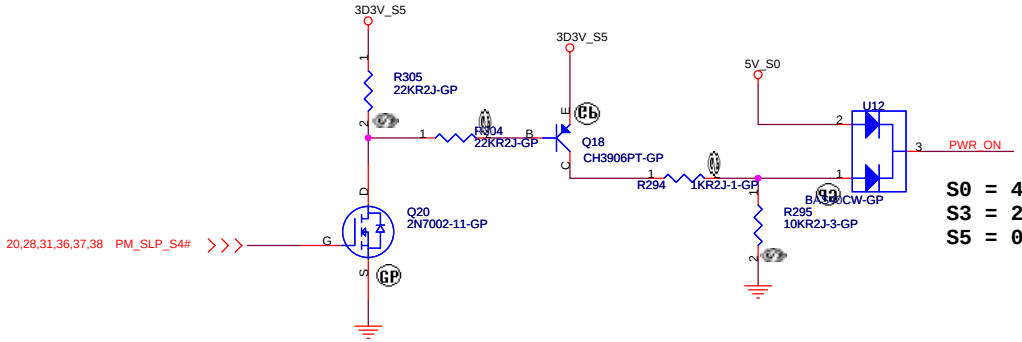












S0 = 4V
S3 = 2.5V
S5 = 0V

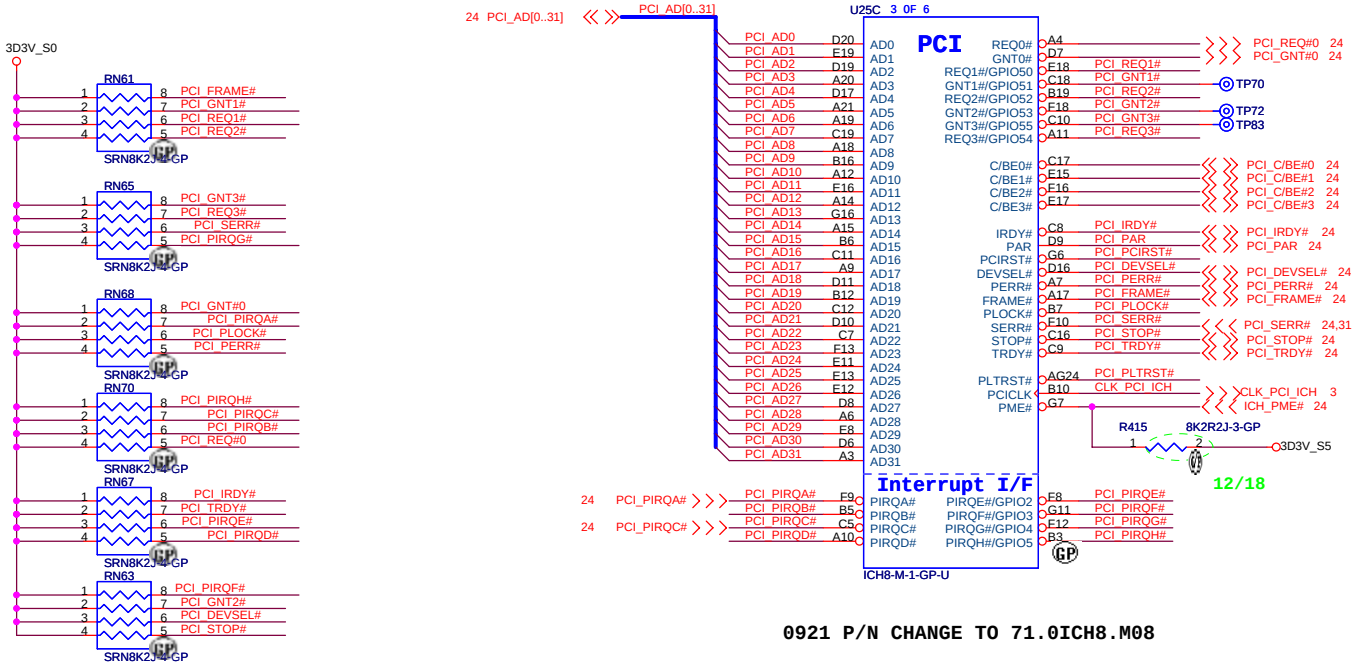
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

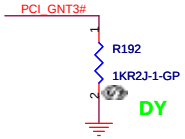
Title: **Board to board conn/ Docking**

Size	Document Number	Rev
A3	Pamirs	SC

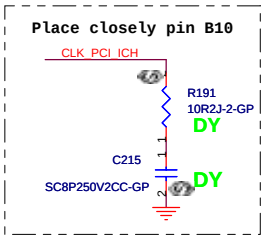
Date: Friday, December 15, 2006 Sheet 17 of 41



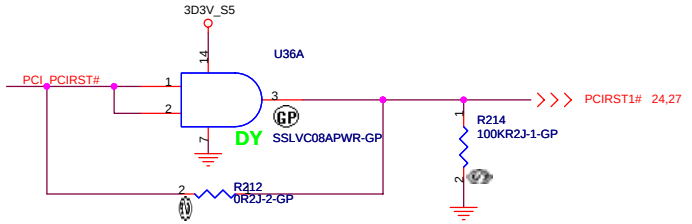
0921 P/N CHANGE TO 71.0ICH8.M08

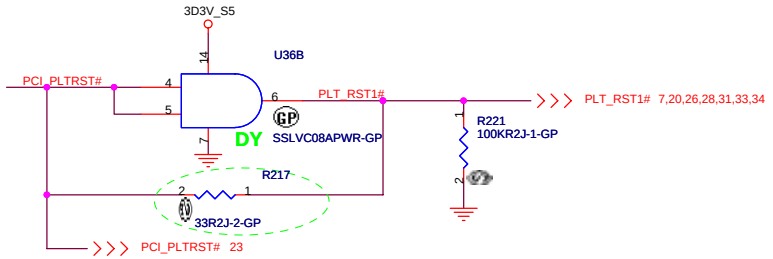


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





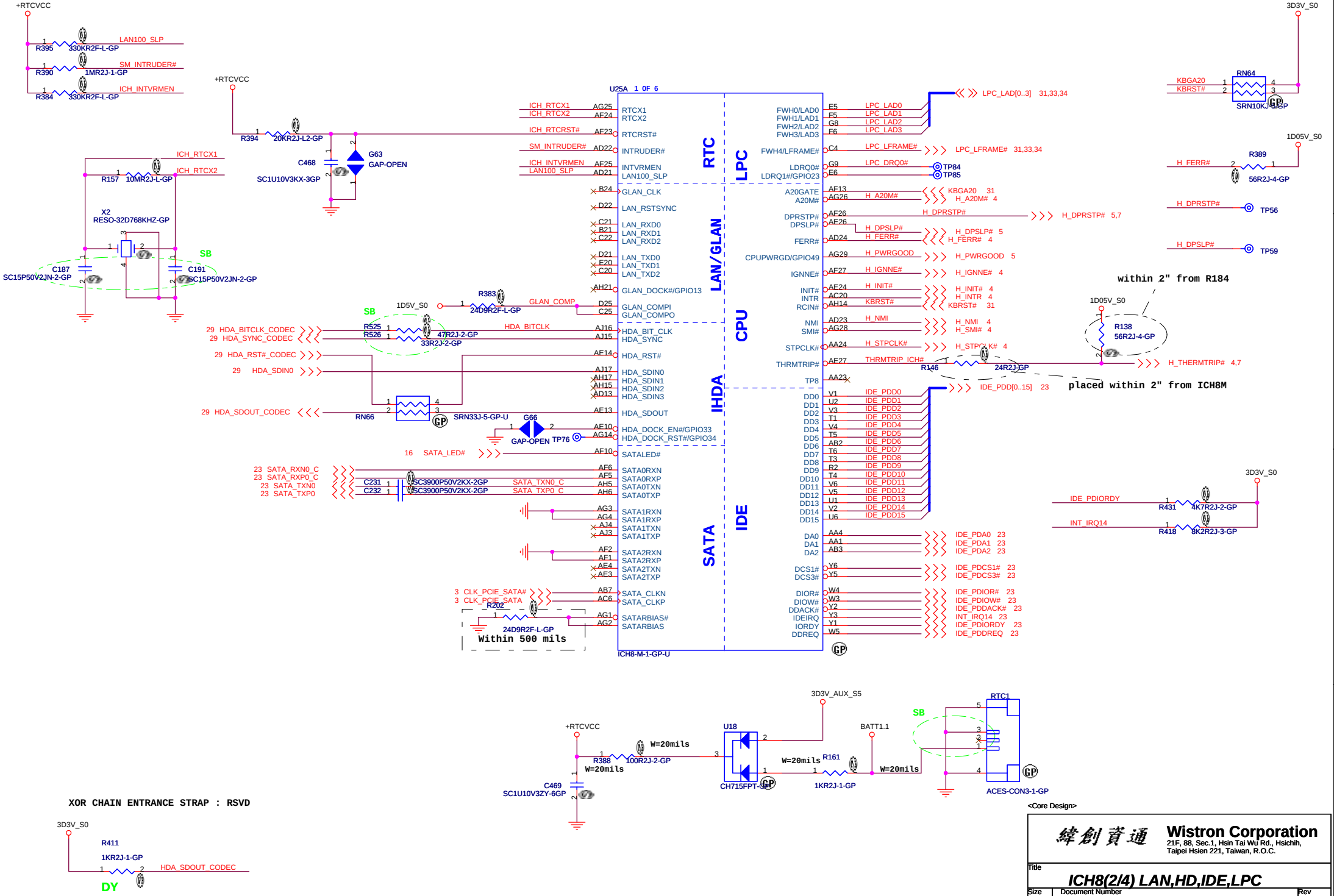
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Pamirs | Rev: SC

Date: Monday, December 18, 2006 | Sheet 18 of 41



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size	Document Number	Rev
A3	Pamirs	SC

Date: Friday, December 15, 2006 Sheet 19 of 41

Place closely pin G5

Place closely pin AG9

11/08

32K suspend clock output

Low--> default

High--> No boot

New Card

LAN

Mini Card 1

Mini Card 2

USB1

New Card

USB2

USB3

CAMERA

BT

MINICARD 1

DOCK

Finger Printer

Within 500 mils

Within 500 mils

<Core Design>

Wistron Corporation

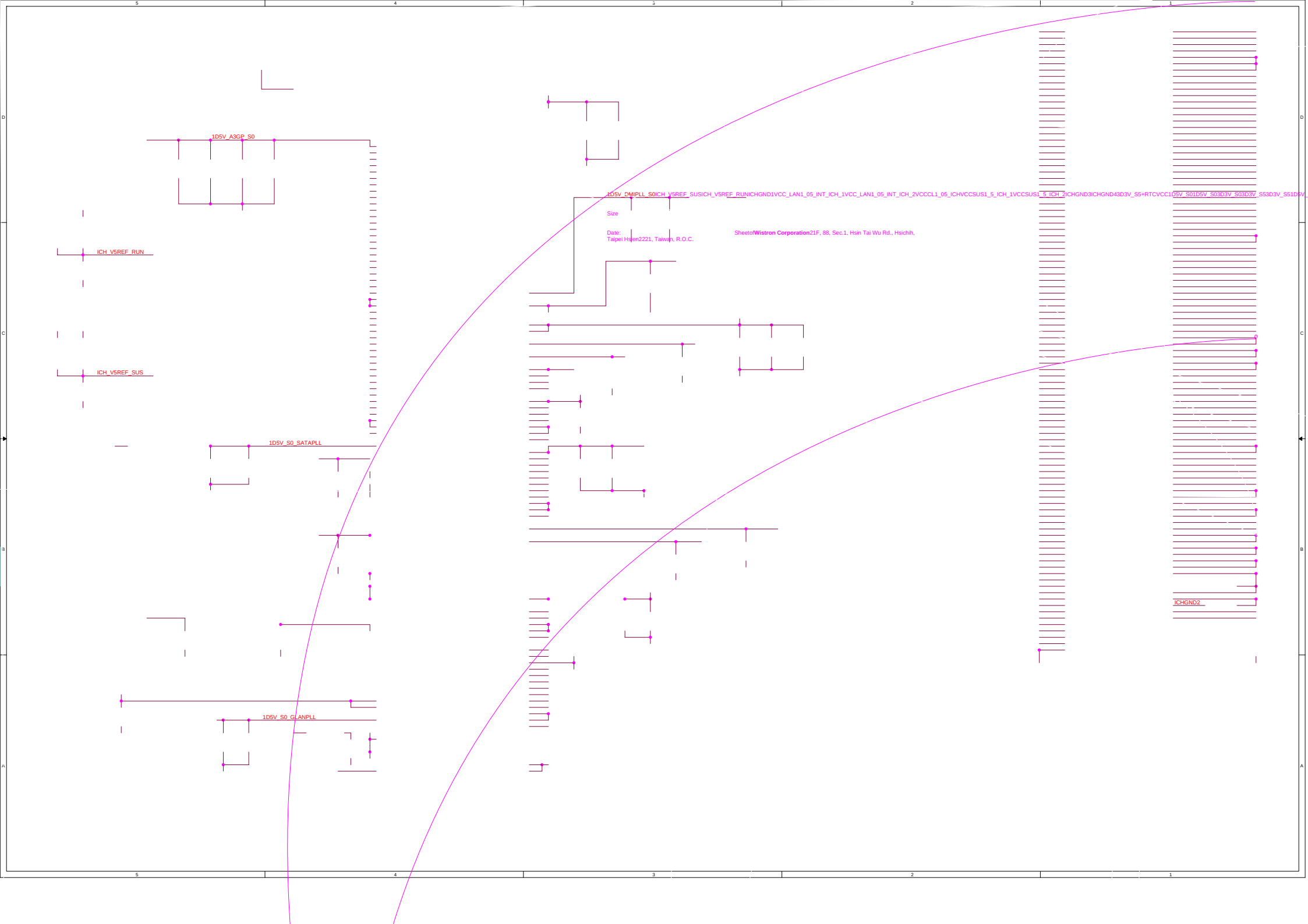
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

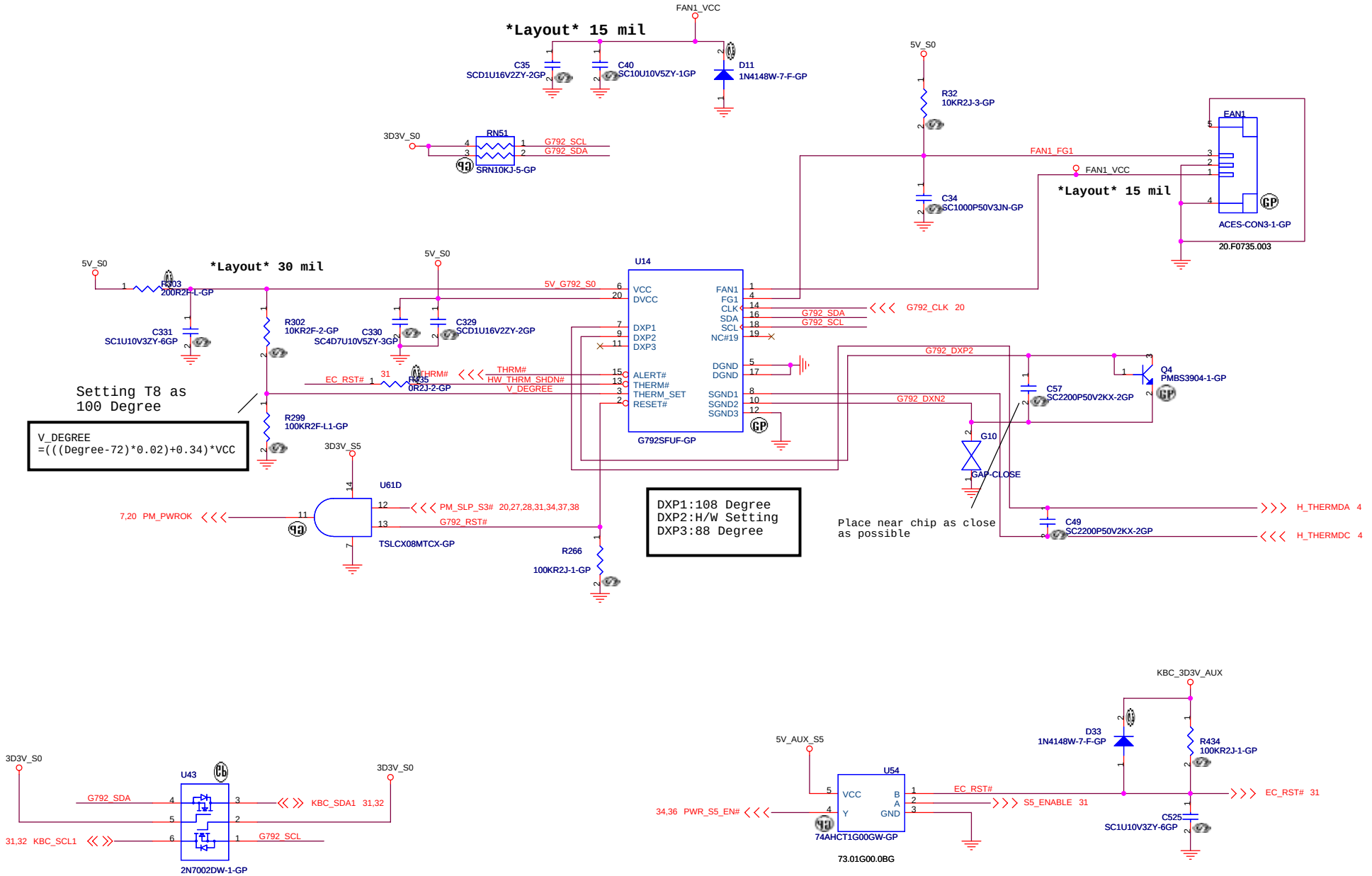
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(3/4) PM,USB,GPIO

Size: Custom | Document Number: Pamirs | Rev: SC

Date: Friday, December 15, 2006 | Sheet 20 of 41


1D5V_A3GP_S0
ICH_V5REF_RUN
ICH_V5REF_SUS
1D5V_S0_SATAPLL
1D5V_S0_GLANPLL
1D5V_DMIPLL_S0ICH_V5REF_SUSICH_V5REF_RUNICHGND1VCC_LAN1_05_INT_ICH_1VCC_LAN1_05_INT_ICH_2VCCCL1_05_ICHVCCSUS1_5_ICH_1VCCSUS1_5_ICH_2ICHGND3ICHGND43D3V_S5+RTCVCC1D5V_S01D5V_S03D3V_S03D3V_S53D3V_S51D5V_
Size
Date:
Taipei Hsien2221, Taiwan, R.O.C.
SheetofWistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
ICHGND2



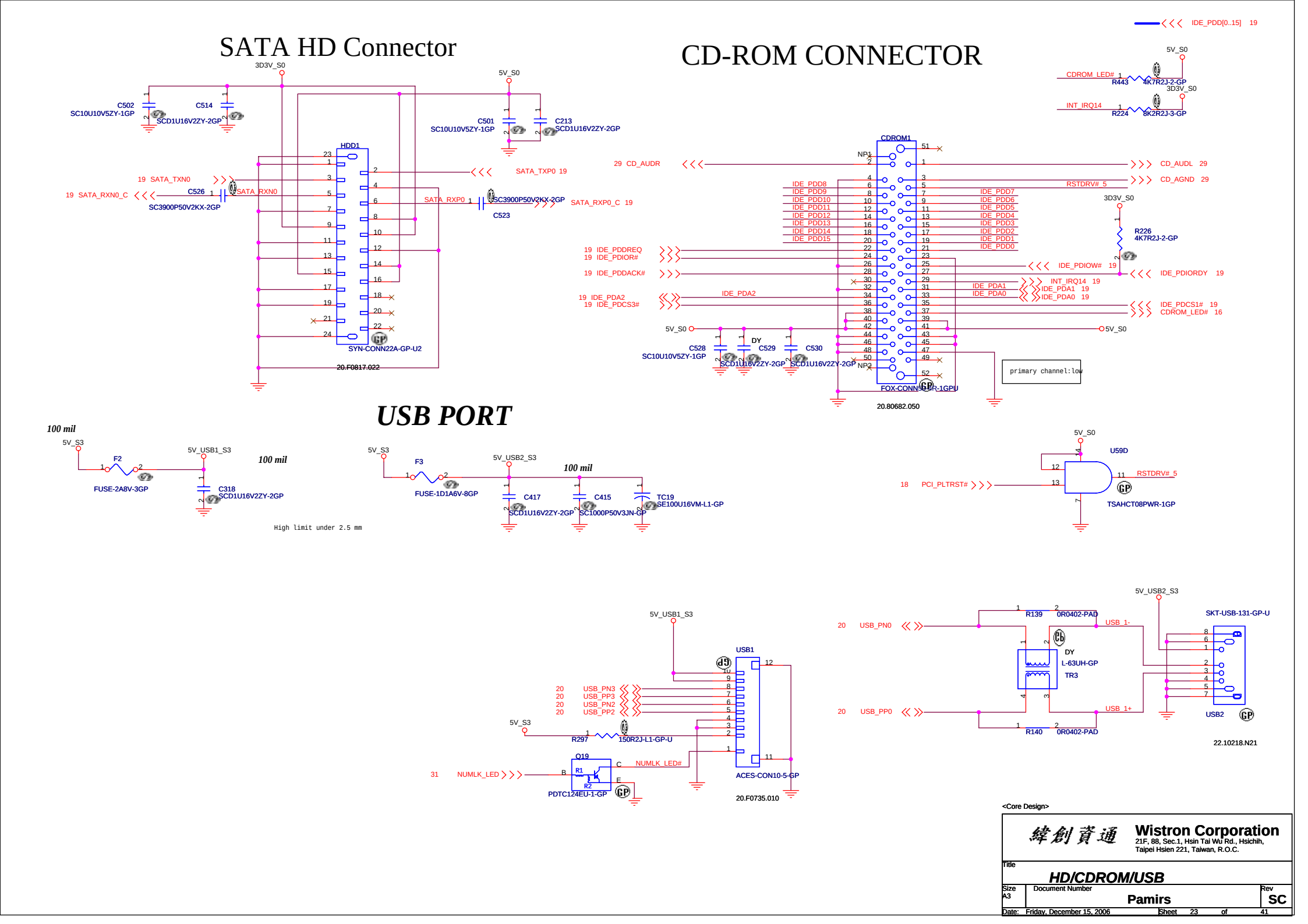
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

Size	Document Number	Rev
Custom	**Pamirs**	**SC**

Date: Friday, December 15, 2006 Sheet 22 of 41



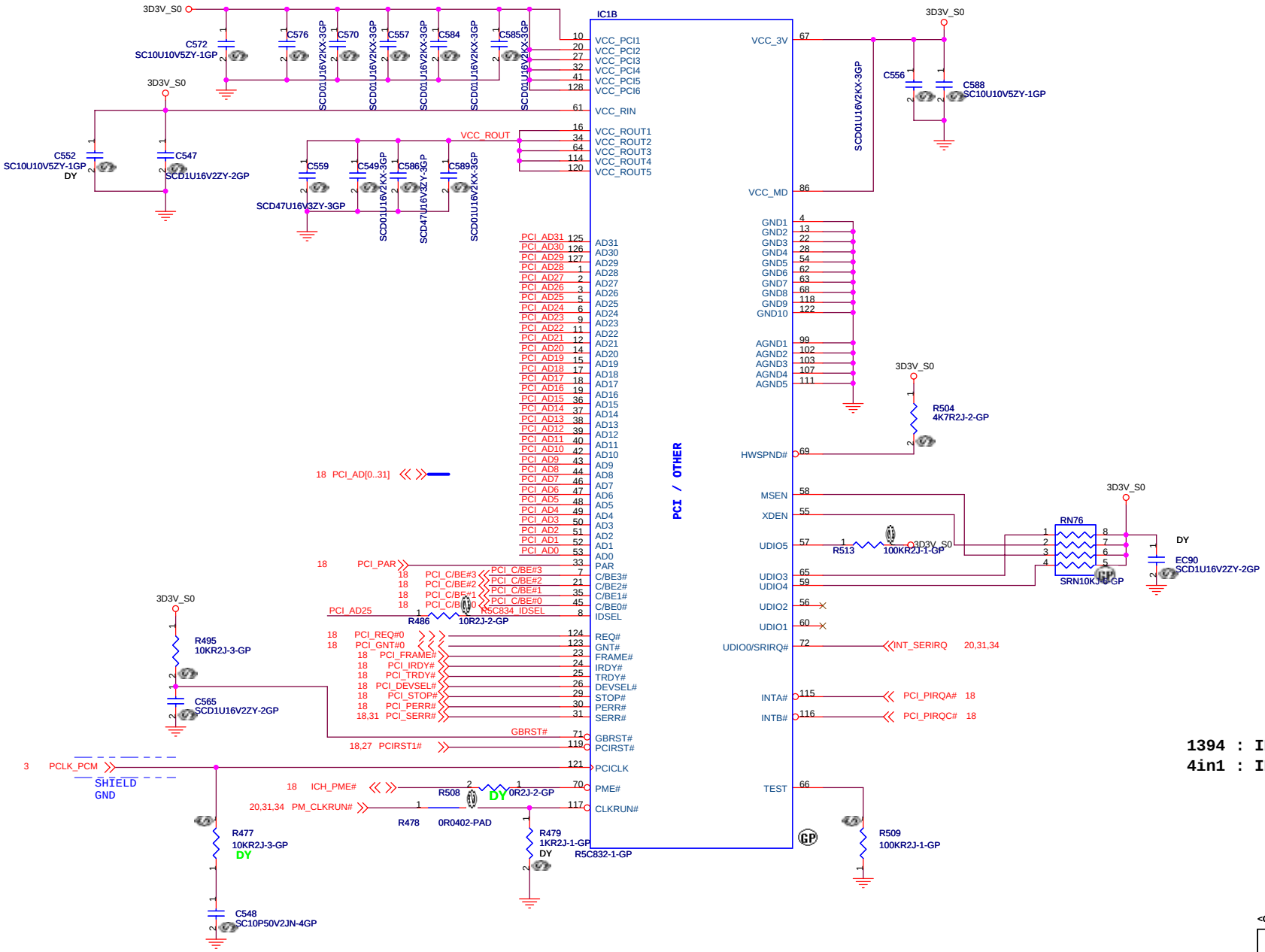
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HD/CDROM/USB***

Size	Document Number	Rev
A3	Pamirs	SC

Date: Friday, December 15, 2006 Sheet 23 of 41



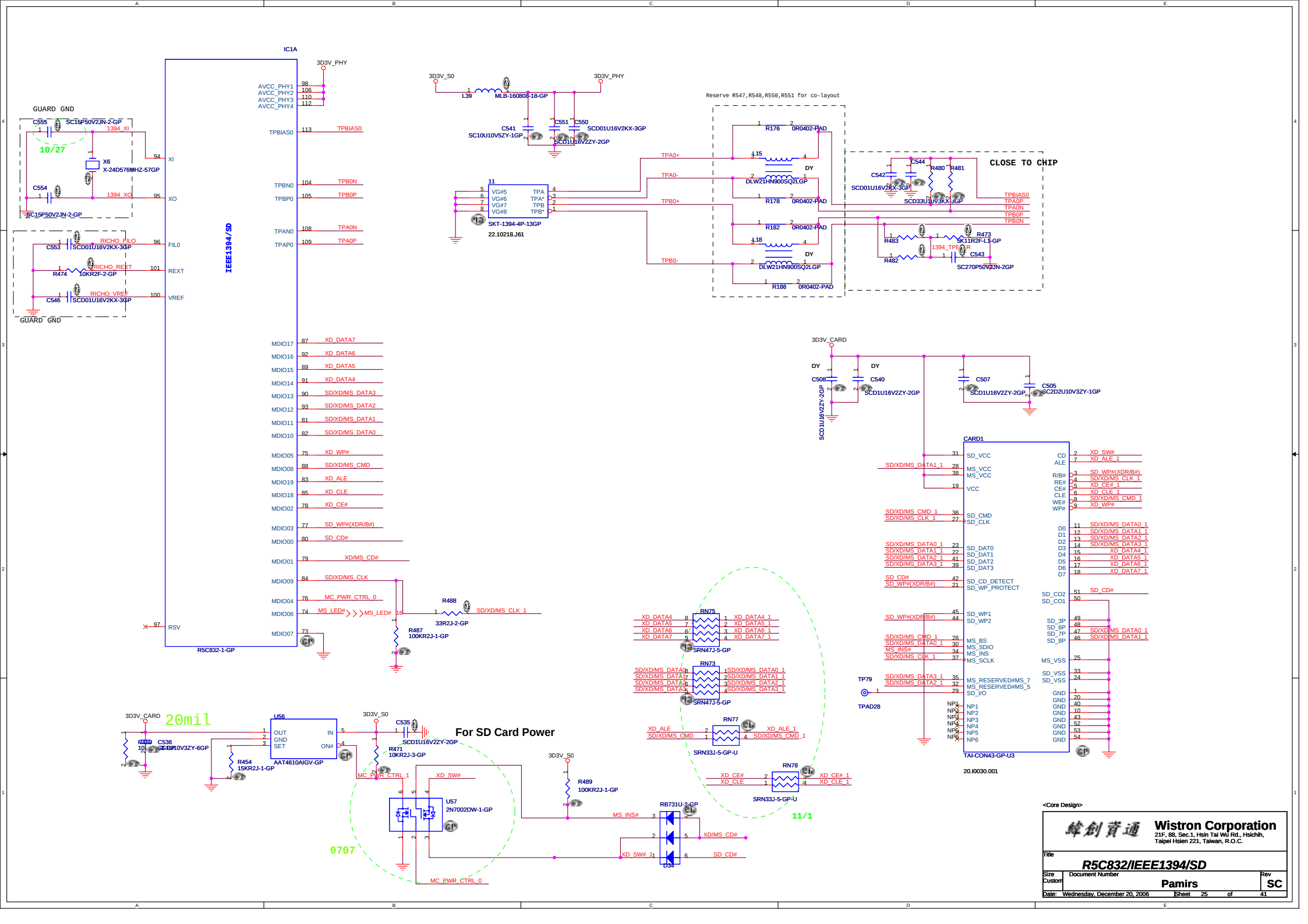
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

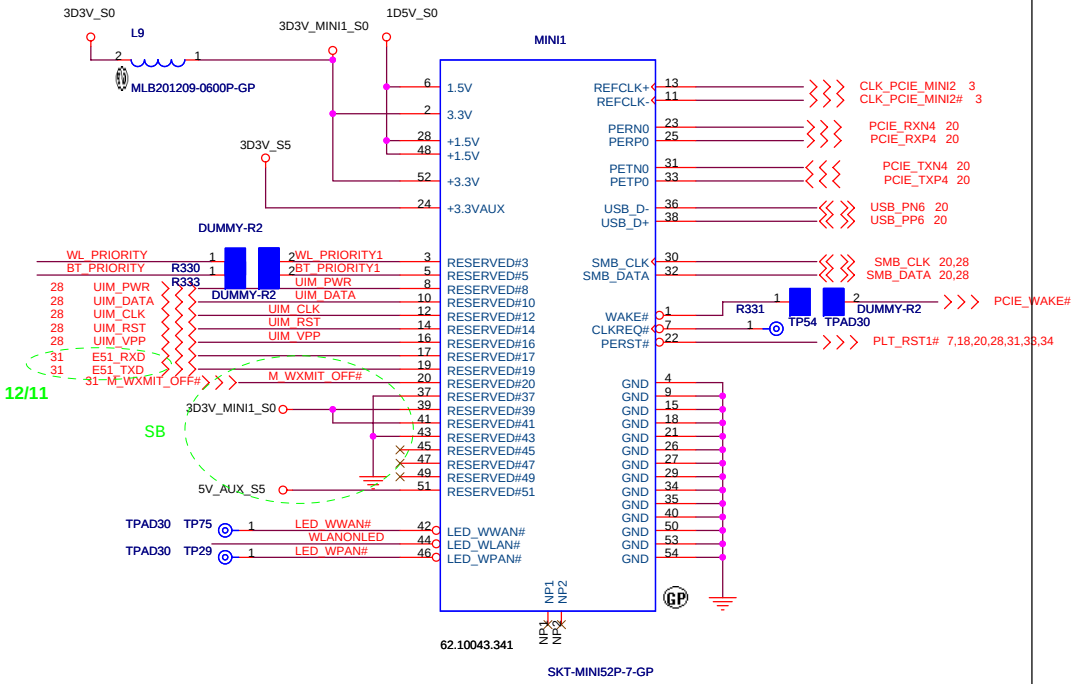
Size: A3 | Document Number: Pamirs | Rev: SC

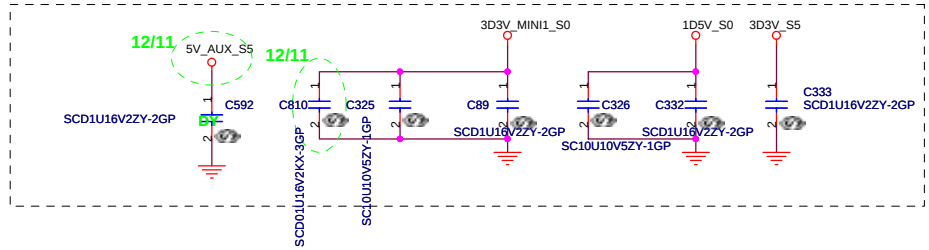
Date: Monday, December 18, 2006 | Sheet 24 of 41


IC1A
IEEE1394/SD
R5C832-1-GP
3D3V_PHY
3D3V_S0
3D3V_CARD
GUARD GND
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
XI
XO
FIL0
REXT
VREF
RSV
1394_XI
1394_XO
RICHO_FILO
RICHO_REXT
RICHO_VREF
X6
X-24D576MHZ-57GP
SC15P50V2JN-2-GP
SCD01U16V2KX-3GP
10KR2F-2-GP
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
XD_DATA7
XD_DATA6
XD_DATA5
XD_DATA4
SD/XD/MS_DATA3
SD/XD/MS_DATA2
SD/XD/MS_DATA1
SD/XD/MS_DATA0
XD_WP#
SD/XD/MS_CMD
XD_ALE
XD_CLE
XD_CE#
SD_WP#(XDR/B#)
SD_CD#
XD/MS_CD#
SD/XD/MS_CLK
MC_PWR_CTRL_0
MS_LED#
R488
33R2J-2-GP
R487
100KR2J-1-GP
L39
MLB-160808-18-GP
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SCD01U16V2KX-3GP
SC1D1U16V2ZY-2GP
Reserve R547,R548,R550,R551 for co-layout
TPA0+
TPA0-
TPB0+
TPB0-
R176
R178
R182
R186
0R0402-PAD
DLW21HN900SQ2LGP
DY
SKT-1394-4P-13GP
22.10218.J61
CLOSE TO CHIP
C542
C544
R480
R481
SCD33U10V3KX-3GP
R483
R482
R473
SK11R2F-L1-GP
1394_TPBIAS
C543
SC270P50V2JN-2GP
CARD1
TAI-CON43-GP-U3
20.I0030.001
SD_VCC
MS_VCC
VCC
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CD_DETECT
SD_WP_PROTECT
SD_WP1
SD_WP2
MS_BS
MS_SDIO
MS_INS
MS_SCLK
MS_RESERVED#MS_7
MS_RESERVED#MS_5
SD_I/O
NP1
NP2
NP3
NP4
NP5
NP6
GND
MS_VSS
SD_VSS
SD_CO1
SD_CO2
SD_1P
SD_4P
SD_7P
SD_8P
TP79
TPAD28
C505
SC2D2U10V3ZY-1GP
C507
C508
C540
RN75
SRN47J-5-GP
RN73
RN77
SRN33J-5-GP-U
RN78
20mil
U56
AAT4610AIGV-GP
R454
15KR2J-1-GP
R471
10KR2J-3-GP
C535
C536
For SD Card Power
U57
2N7002DW-1-GP
R489
100KR2J-1-GP
RB731U-2-GP
D34
0707
11/1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size
Custom
Document Number
Pamirs
Rev
SC
Date: Wednesday, December 20, 2006
Sheet 25 of 41

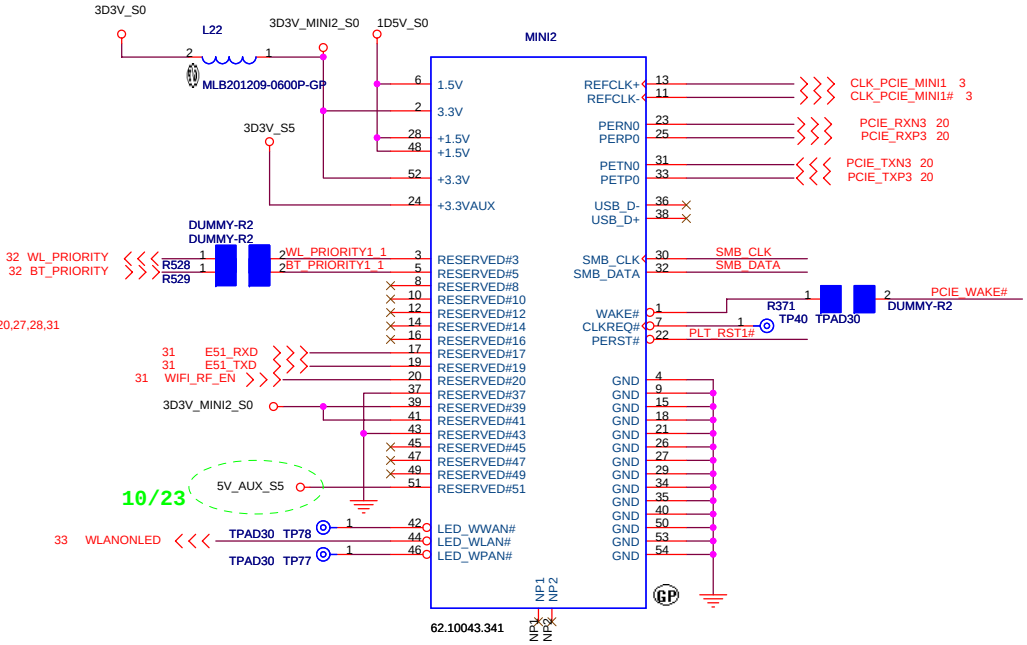
Mini Card Connector

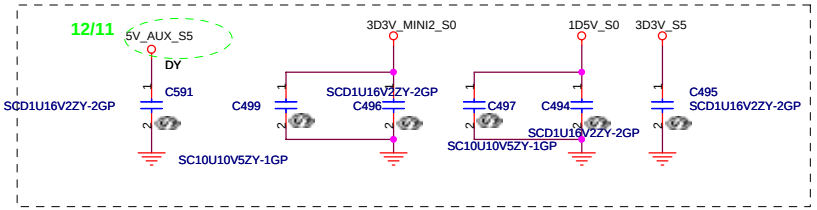
Mini Card Connector 1(WWAN)





Mini Card Connector 2(802.11a/b/g)





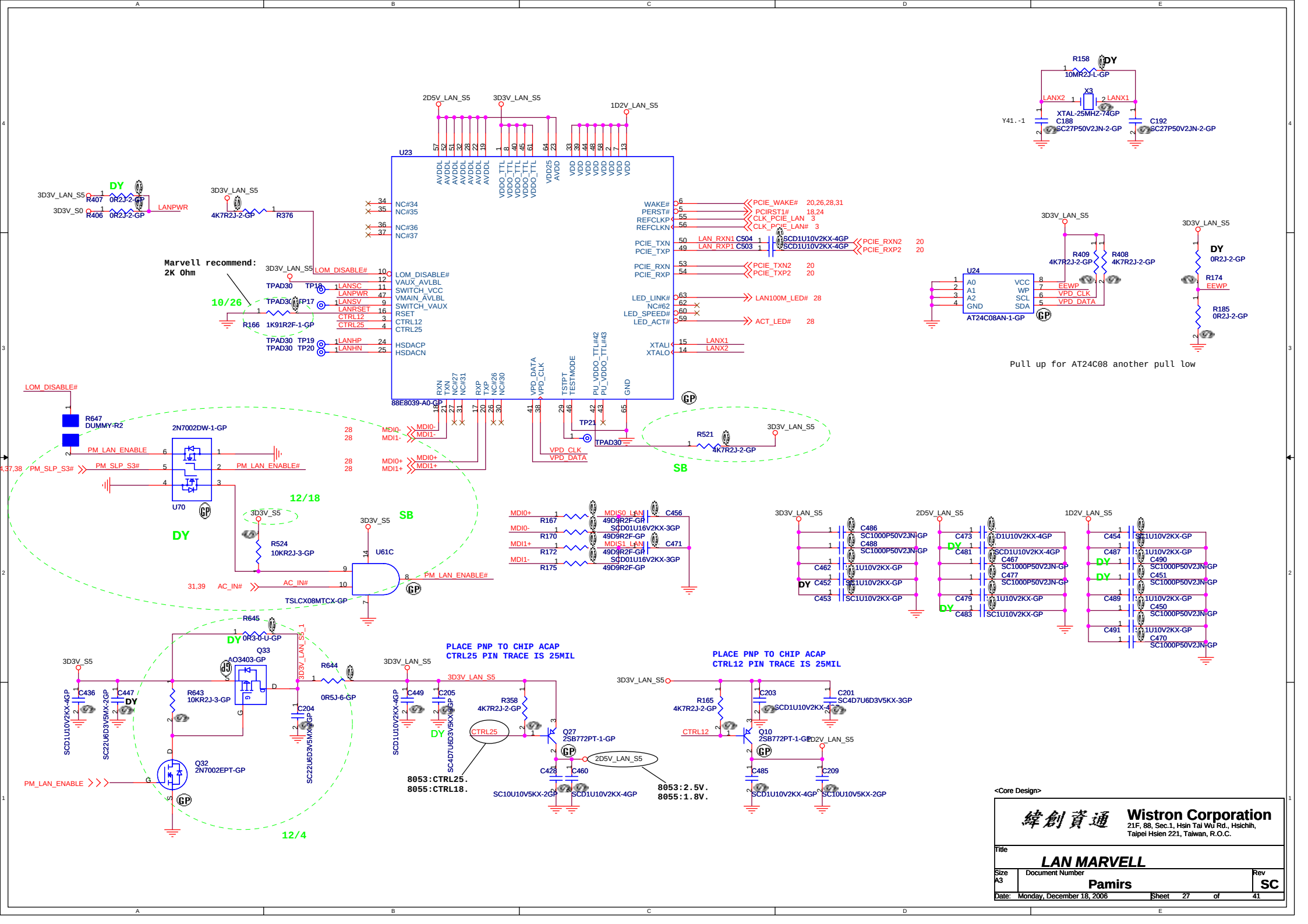
<Core Design>

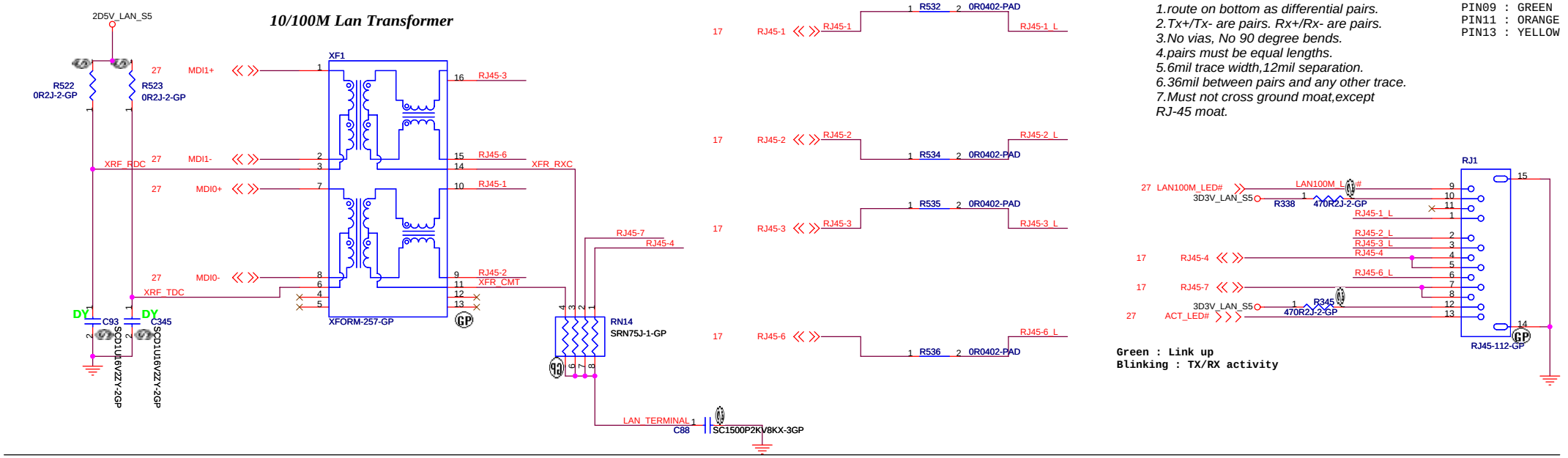
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

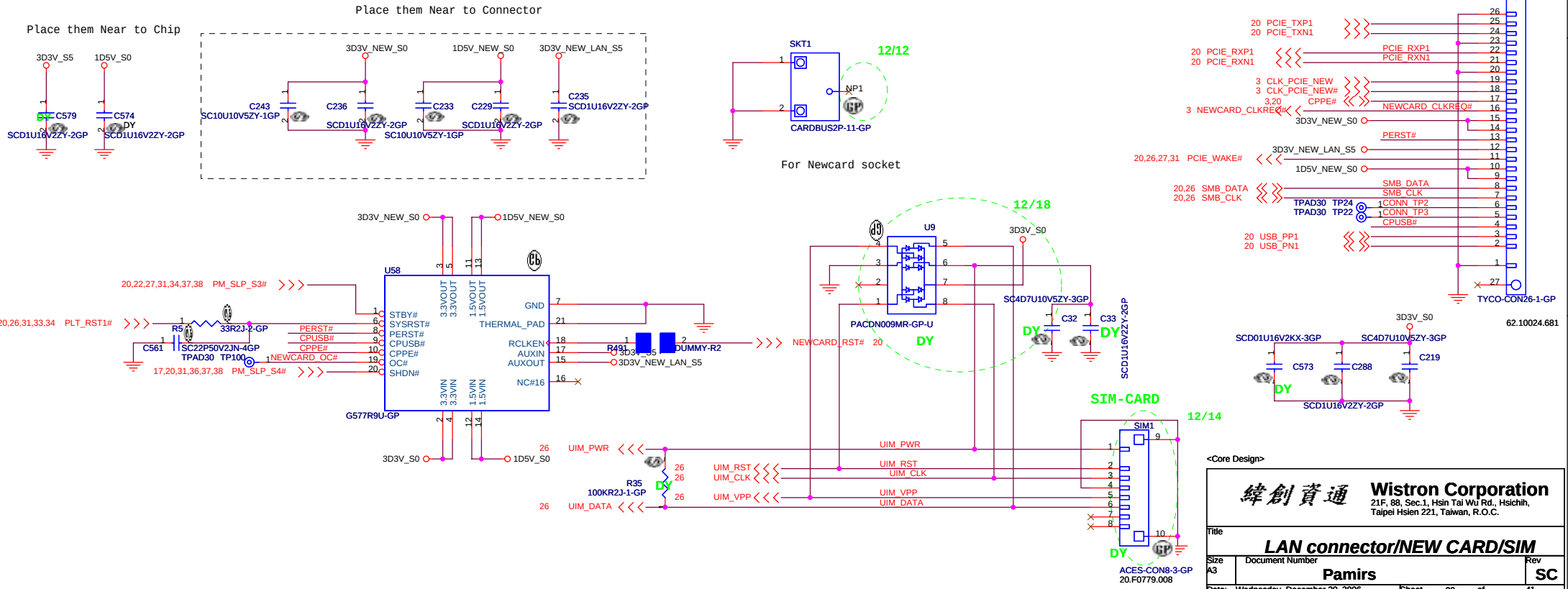
Size	Document Number	Rev
A3	Pamirs	SC

Date: Tuesday, December 19, 2006 Sheet 26 of 41


U23
88E8039-A0-GP
Marvell recommend:
2K Ohm
10/26
12/18
12/4
SB
DY
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
Pull up for AT24C08 another pull low
U70
U61C
U24
AT24C08AN-1GP
Q33
AO3403-GP
Q32
2N7002EPT-GP
Q27
2SB772PT-1-GP
Q10
2SB772PT-1-GP
2N7002DW-1-GP
TSLCX08MTCX-GP
XTAL-25MHZ-74GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN MARVELL
Size A3
Document Number
Pamirs
Rev
SC
Date: Monday, December 18, 2006
Sheet 27 of 41

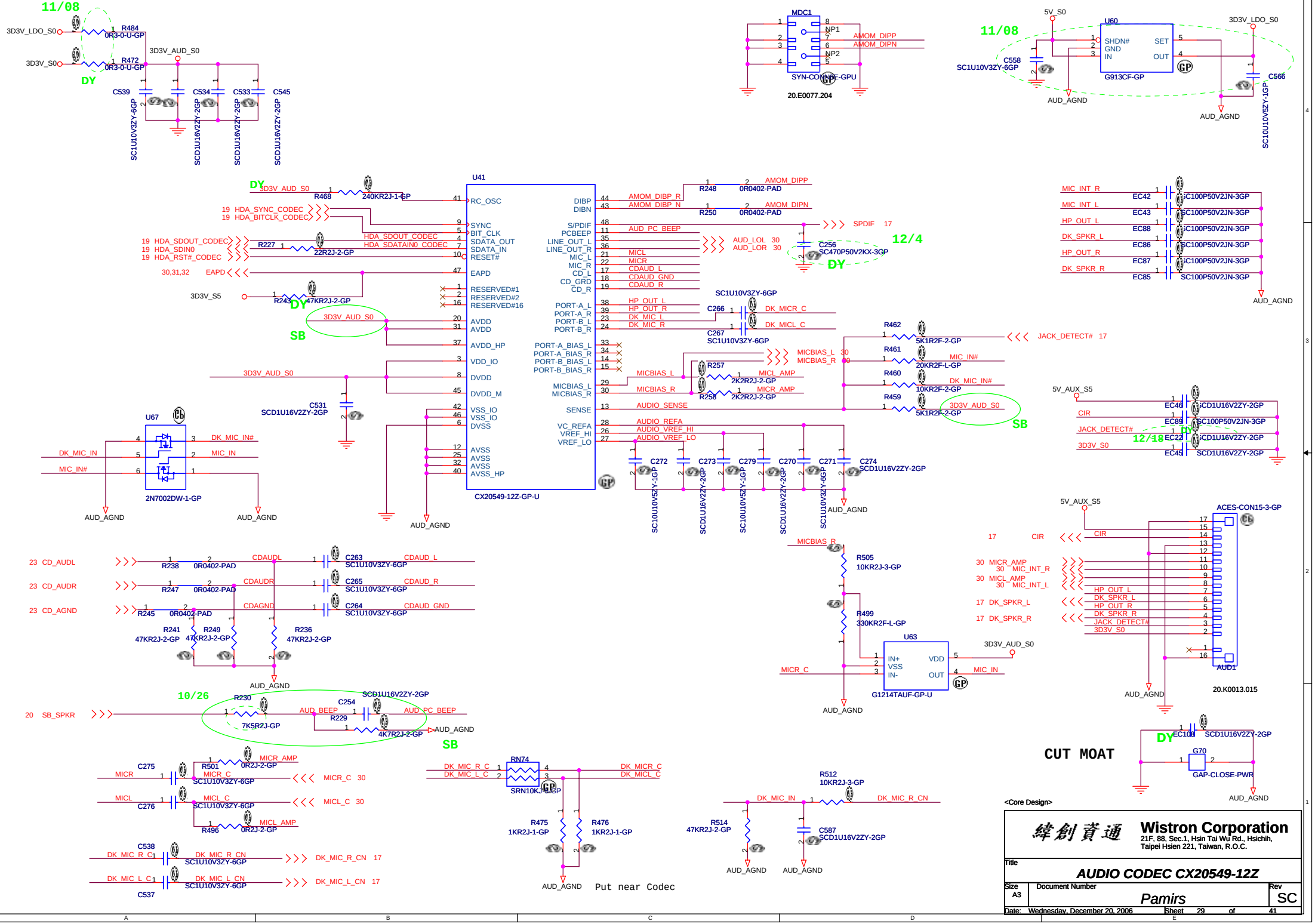


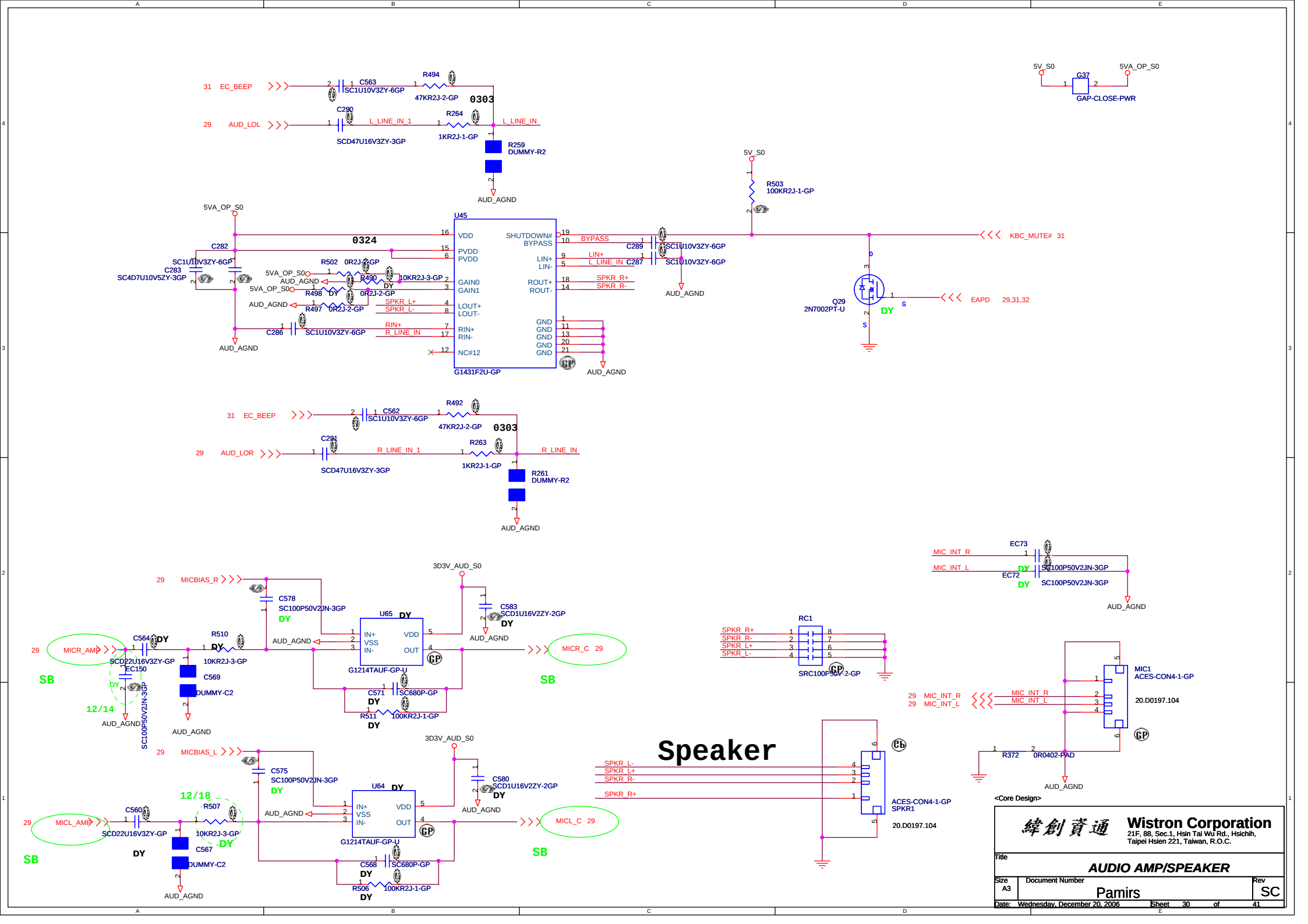
NEWCARD Connector



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN connector/NEW CARD/SIM
Size A3	Document Number: Pamirs
Rev	SC
Date: Wednesday, December 20, 2006	Sheet 28 of 41


11/08
3D3V_LDO_S0
R484
0R3-0-U-GP
3D3V_S0
R472
0R3-0-U-GP
3D3V_AUD_S0
DY
C539
C534
C533
C545
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONN-GPU
20.E0077.204
5V_S0
11/08
U60
SHDN#
GND
IN
SET
OUT
G913CF-GP
3D3V_LDO_S0
C558
SC1U10V3ZY-6GP
C566
SC10U10V5ZY-1GP
AUD_AGND
U41
CX20549-12Z-GP-U
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
3D3V_AUD_S0
R468
240KR2J-1-GP
HDA_SYNC_CODEC
HDA_BITCLK_CODEC
HDA_SDOUT_CODEC
HDA_SDATAIN0_CODEC
R227
22R2J-2-GP
HDA_SDOUT_CODEC
HDA_SDIN0
HDA_RST#_CODEC
EAPD
3D3V_S5
R243
47KR2J-2-GP
DY
SB
C531
SCD1U16V2ZY-2GP
AUD_AGND
R248
0R0402-PAD
R250
0R0402-PAD
AMOM_DIPP
AMOM_DIPN
AUD_PC_BEEP
SPDIF
AUD_LOL
AUD_LOR
C256
SC470P50V2KX-3GP
12/4
DY
HP_OUT_L
HP_OUT_R
DK_MIC_L
DK_MIC_R
C266
C267
SC1U10V3ZY-6GP
DK_MICR_C
DK_MICL_C
MICBIAS_L
MICBIAS_R
R257
R258
2K2R2J-2-GP
MICL_AMP
MICR_AMP
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C272
C273
C279
C270
C271
C274
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SC10U10V3ZY-6GP
R462
5K1R2F-2GP
R461
20KR2F-L-GP
R460
10KR2F-2GP
R459
5K1R2F-2GP
JACK_DETECT#
MIC_IN#
DK_MIC_IN#
3D3V_AUD_S0
SB
MIC_INT_R
MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
EC42
EC43
EC88
EC86
EC87
EC85
SC100P50V2JN-3GP
AUD_AGND
5V_AUX_S5
CIR
JACK_DETECT#
3D3V_S0
12/18
DY
EC46
EC89
EC22
EC45
SCD1U16V2ZY-2GP
SC100P50V2JN-3GP
U67
2N7002DW-1-GP
DK_MIC_IN
MIC_IN#
DK_MIC_IN#
MIC_IN
AUD_AGND
23 CD_AUDL
23 CD_AUDR
23 CD_AGND
R238
R247
R245
0R0402-PAD
CDAUDL
CDAUDR
CDAGND
C263
C265
C264
SC1U10V3ZY-6GP
CDAUD_L
CDAUD_R
CDAUD_GND
R241
R249
R236
47KR2J-2-GP
AUD_AGND
10/26
R230
7K5R2J-GP
C254
SCD1U16V2ZY-2GP
R229
4K7R2J-2-GP
AUD_BEEP
AUD_PC_BEEP
20 SB_SPKR
SB
MICBIAS_R
R505
10KR2J-3-GP
R499
330KR2F-L-GP
U63
G1214TAUF-GP-U
IN+
IN-
VSS
VDD
OUT
MICR_C
MIC_IN
3D3V_AUD_S0
AUD_AGND
17 CIR
30 MICR_AMP
30 MICL_AMP
30 MIC_INT_R
30 MIC_INT_L
17 DK_SPKR_L
17 DK_SPKR_R
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
JACK_DETECT#
3D3V_S0
ACES-CON15-3-GP
AUD1
20.K0013.015
C275
C276
C538
C537
R501
R496
0R2J-2-GP
MICR_AMP
MICL_AMP
MICR_C
MICL_C
SC1U10V3ZY-6GP
MICR_C 30
MICL_C 30
DK_MIC_R_CN
DK_MIC_L_CN
DK_MIC_R_CN 17
DK_MIC_L_CN 17
RN74
SRN10KJ-GP
DK_MIC_R_C
DK_MIC_L_C
DK_MICR_C
DK_MICL_C
R475
R476
1KR2J-1-GP
Put near Codec
R512
10KR2J-3-GP
R514
47KR2J-2-GP
C587
SCD1U16V2ZY-2GP
DK_MIC_IN
DK_MIC_R_CN
CUT MOAT
DY
EC108
SCD1U16V2ZY-2GP
G70
GAP-CLOSE-PWR
AUD_AGND
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
Pamirs
Rev SC
Date: Wednesday, December 20, 2006
Sheet 29 of 41

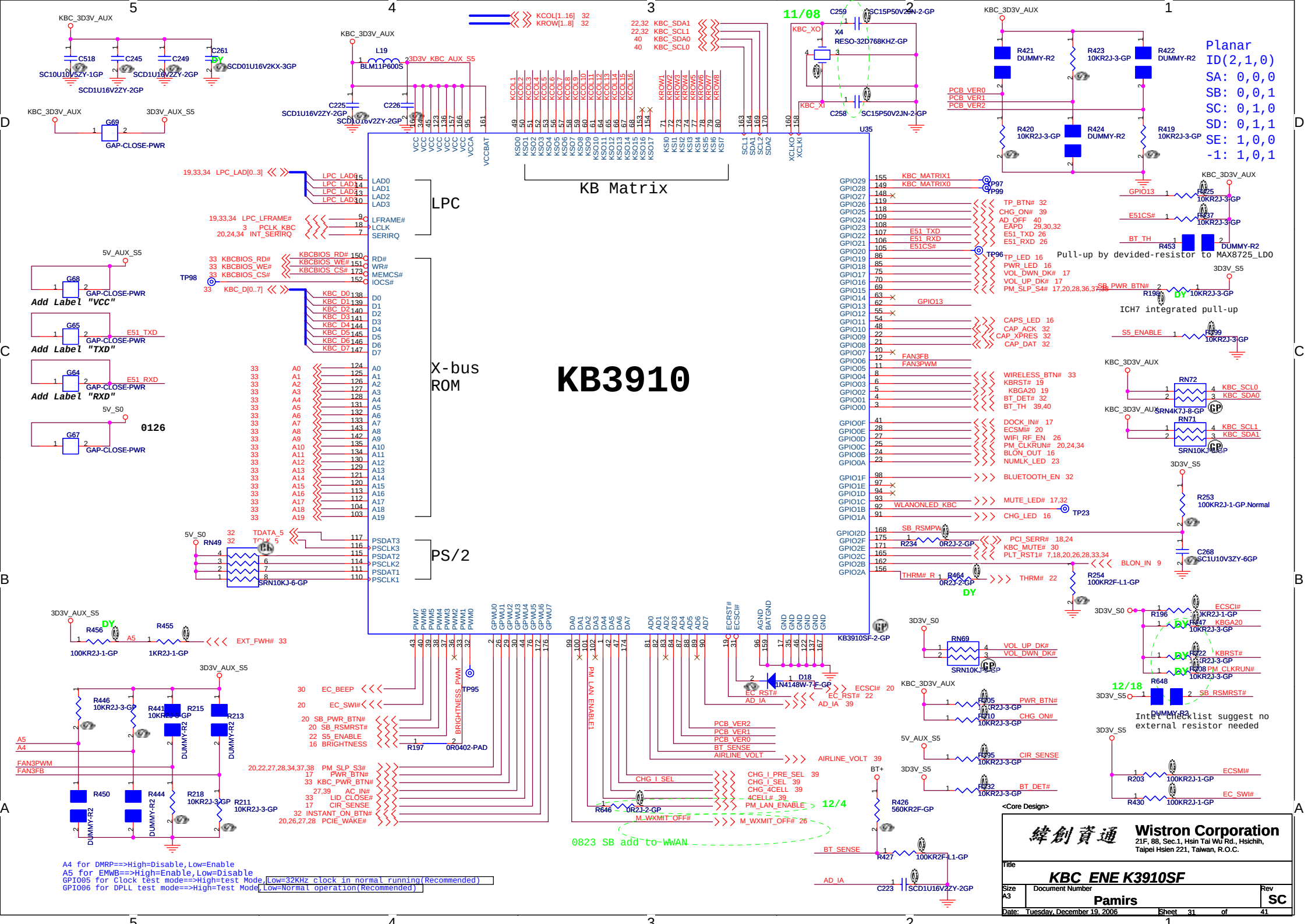


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP/SPEAKER**

Size	Document Number	Rev
A3	Pamirs	SC

Date: Wednesday, December 20, 2006 Sheet 30 of 41


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Inter checklist suggest no external resistor needed
0823 SB add to WWAN
11/08
12/4
12/18
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs
Tuesday, December 19, 2006
31 of 41

CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

KB1
ACES-CON24-2-GP
20.K0220.024

CAM1
20.D0197.105
ACES-CON5-1GP
R9 0R5J-6-GP DY
R11 0R5J-6-GP DY
C335 SCD1U16V2ZY-2GP
C337 SC4D7U10V5ZY-3GP
USB_4-
USB_4+
12/4

11/09
(3.93V)
U71
G913CF-GP
R641 68KR2F-GP
R642 31K6R2F-GP
C809 SC1U10V3ZY-6GP
C808 SC10U10V5ZY-1GP

BT1
ACES-CON8-4-GP
20.F0772.008
BT_LED
WL_PRIORITY
BT_PRIORITY
BT_DET#

R89 0R0402-PAD
R90 0R0402-PAD
TR2 L-63UH-GP DY
USB_PN4
USB_PP4

EC93 DY
EC94 DY
EC95 SCD1U16V2ZY-2GP DY
EC96 DY SCD1U16V2ZY-2GP

Close to CN8
0717Change from S5
MAX 150mA
C582 SC1U10V3ZY-6GP
U66
G913CF-GP
C581 SC4D7U10V5ZY-3GP
C577 SCD1U16V2ZY-2GP
BLUETOOTH_EN

R268 0R0402-PAD
TR4 L-63UH-GP DY
USB_PN5
USB_PP5

D31 BAV99W-1-GP DY
TDATA_5

TouchPad Connector

D32 BAV99W-1-GP DY
TCLK_5
C430 SCD1U16V2ZY-2GP
C433 SC1U10V3ZY-6GP
R354 10KR2J-3-GP
R355 10KR2J-3-GP
TPAD1
FOX-CON4-12-GP
C431 SC33P50V2JN-3GP
C432 SC33P50V2JN-3GP

D17 BAV99W-1-GP DY
TP_BTN_1#

R14 10KR2J-3-GP
Q2 2N7002-11-GP
EAPD#
EAPD

D8 BAV99W-1-GP DY
CAP_ACK
D6 BAV99W-1-GP DY
CAP_DAT

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
20.K0228.012
EC7 SCD1U16V2ZY-2GP
R276 0R2J-2-GP DY
R275 0R2J-2-GP DY
R274 0R2J-2-GP
R279 47R0R2J-2-GP DY
R49 0R2J-2-GP
R48 0R2J-2-GP DY
EC149 DY
MUTE_LED_1#
MUTE_LED#
CAP_XPRES
KBC_SCL1
KBC_SDA1
INSTANT_ON_BTN#
EC49 SCD1U16V2ZY-2GP
EC10 SC100P50V2JN-3GP
EC13 SCD1U16V2ZY-2GP
EC11 SCD1U16V2ZY-2GP
EC6 SCD1U16V2ZY-2GP

D7 BAV99W-1-GP DY
INSTANT_ON_BTN#

TOUCH-PAD SWITCH

SW1 SW-TACT-68-GP-U
62.40009.451
R416 10KR2J-3-GP
100R2J-2-GP R413
C515 SC1000P50V3JN-GP DY
TP_BTN# 31

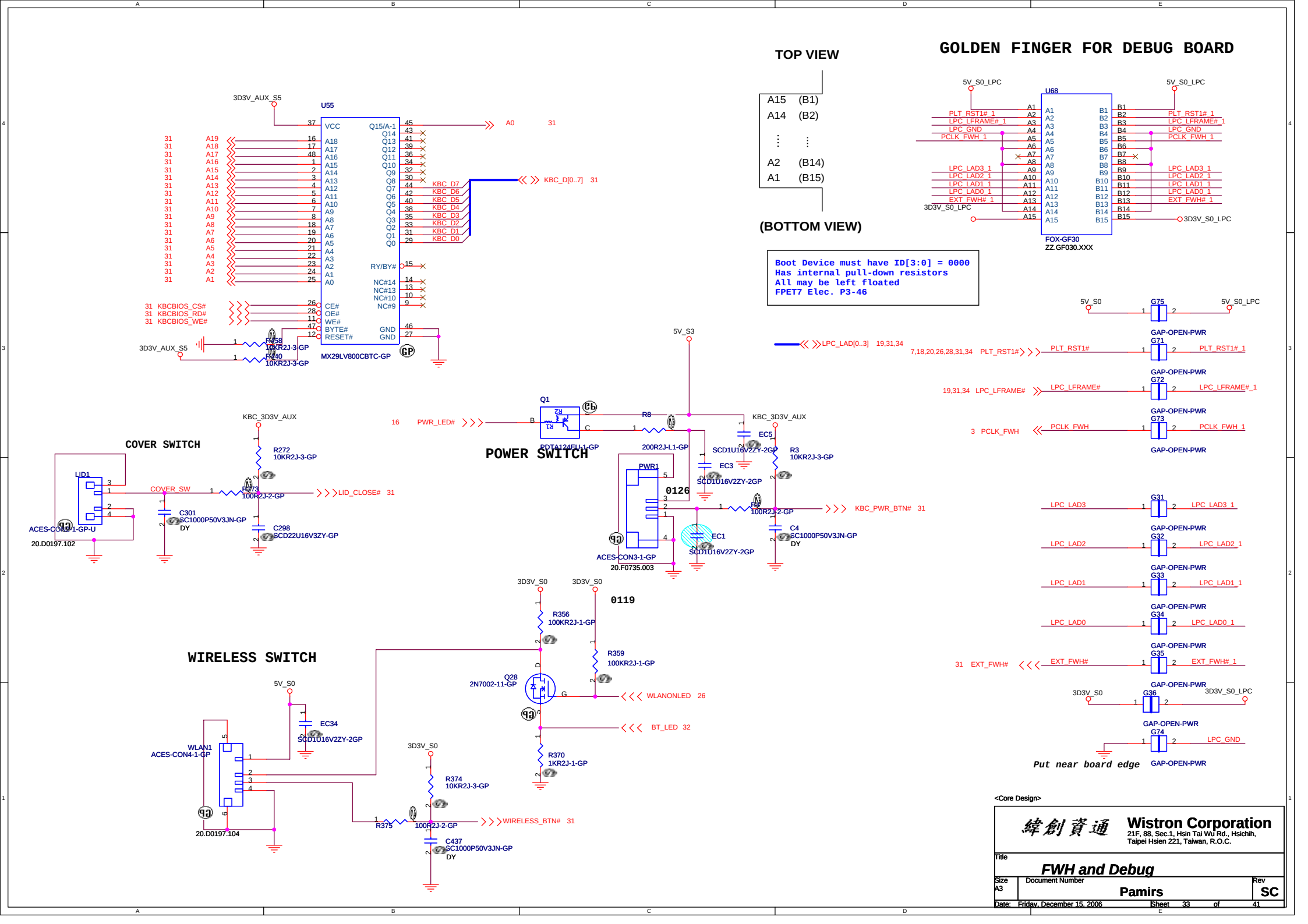
D5 BAV99W-1-GP DY
EAPD#

RC6 SRC100P50V-2-GP
RC2 SRC100P50V-2-GP
RC5 SRC100P50V-2-GP
RC7 SRC100P50V-2-GP
RC3 SRC100P50V-2-GP
RC4 SRC100P50V-2-GP
for EMI

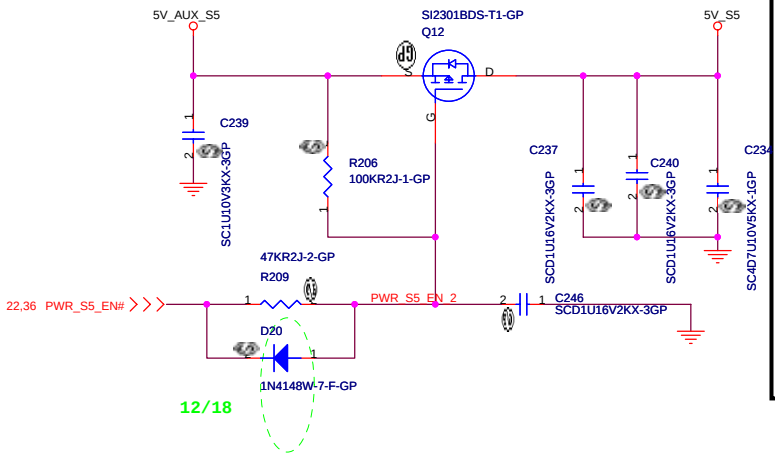
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

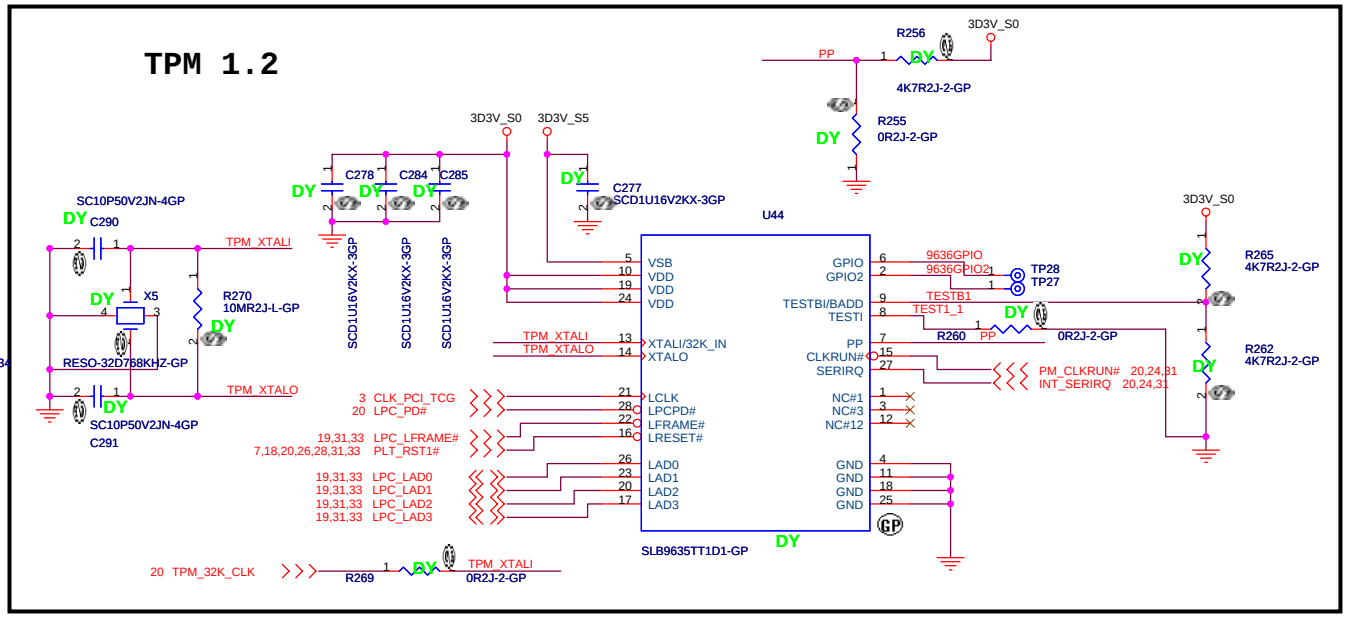
Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs
Rev: SC
Date: Tuesday, December 19, 2006
Sheet 32 of 41


TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
U68
FOX-GF30
ZZ.GF030.XXX
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
U55
MX29LV800CBTC-GP
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
0126
0119
Put near board edge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
FWH and Debug
Pamirs
Friday, December 15, 2006

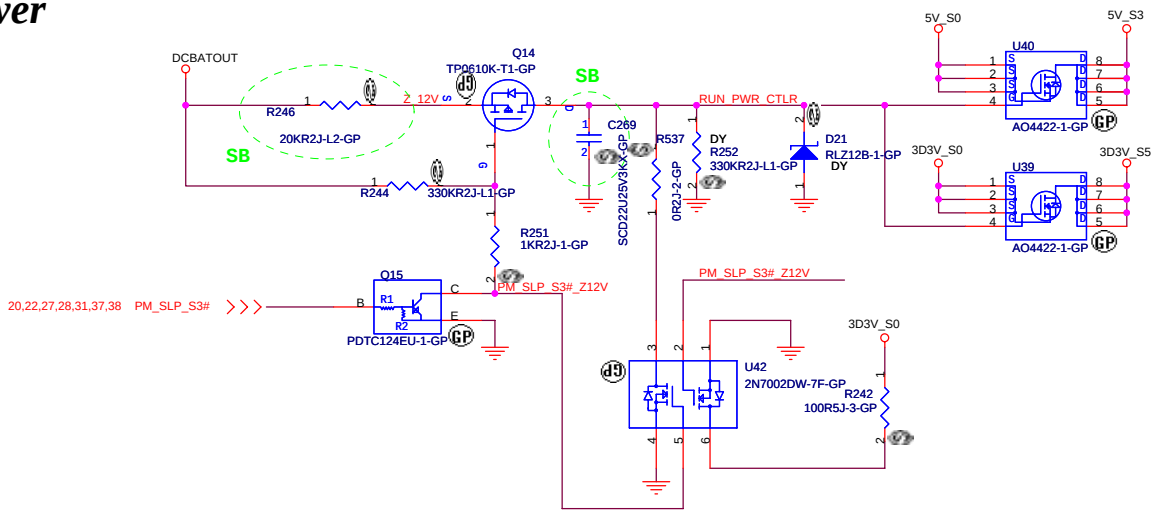
5V_AUX_S5 TO 5V_S5



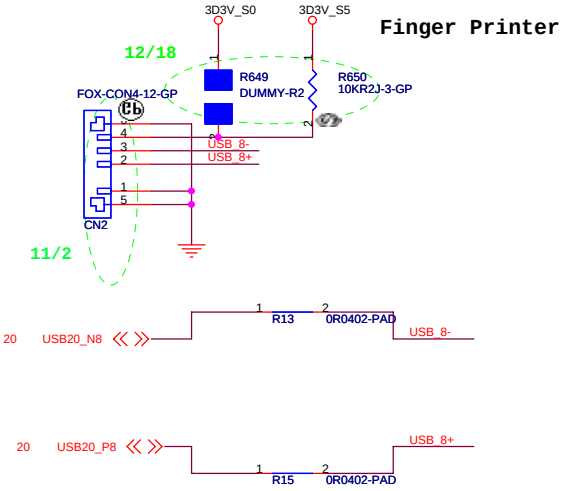
TPM 1.2



Run Power

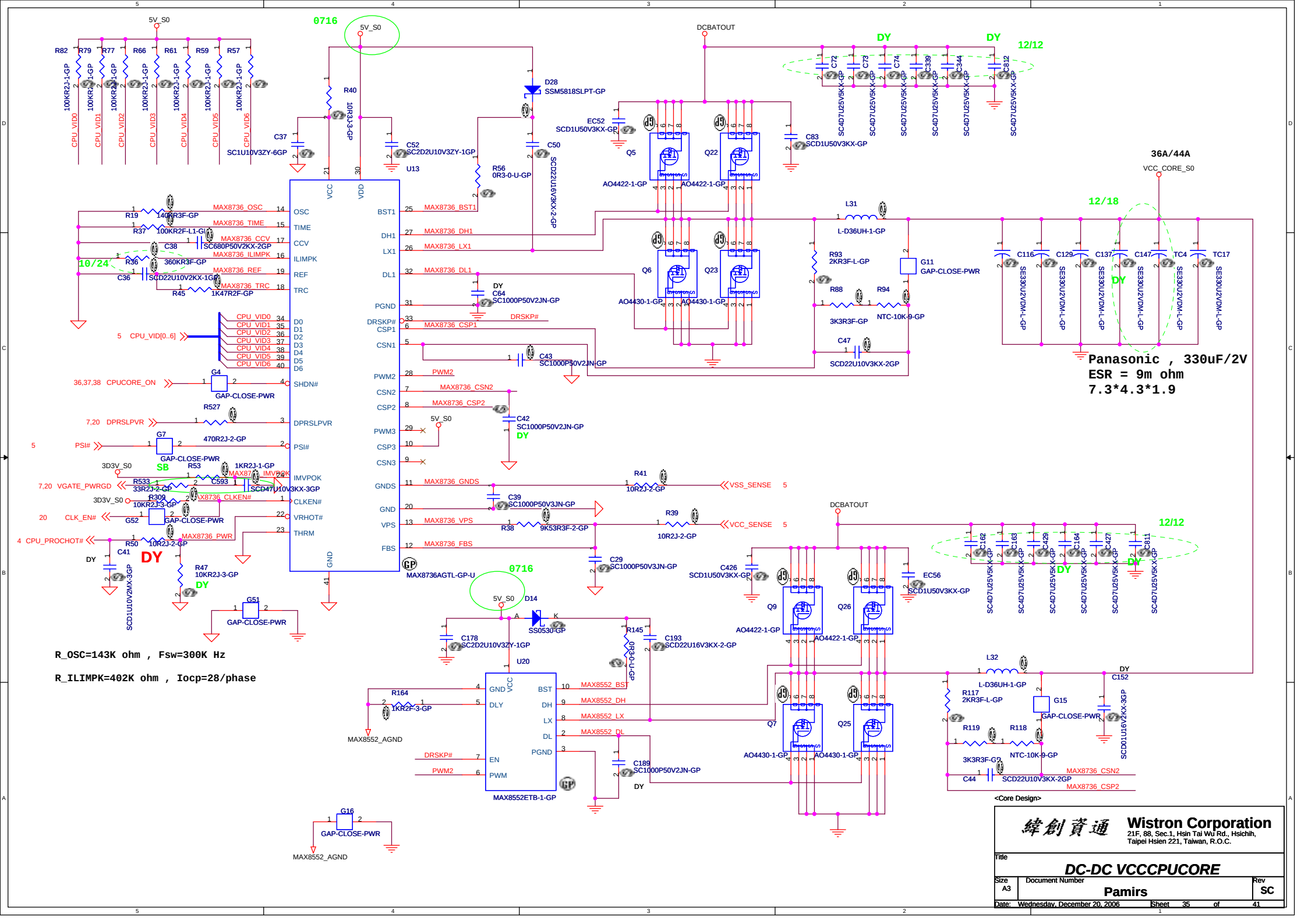


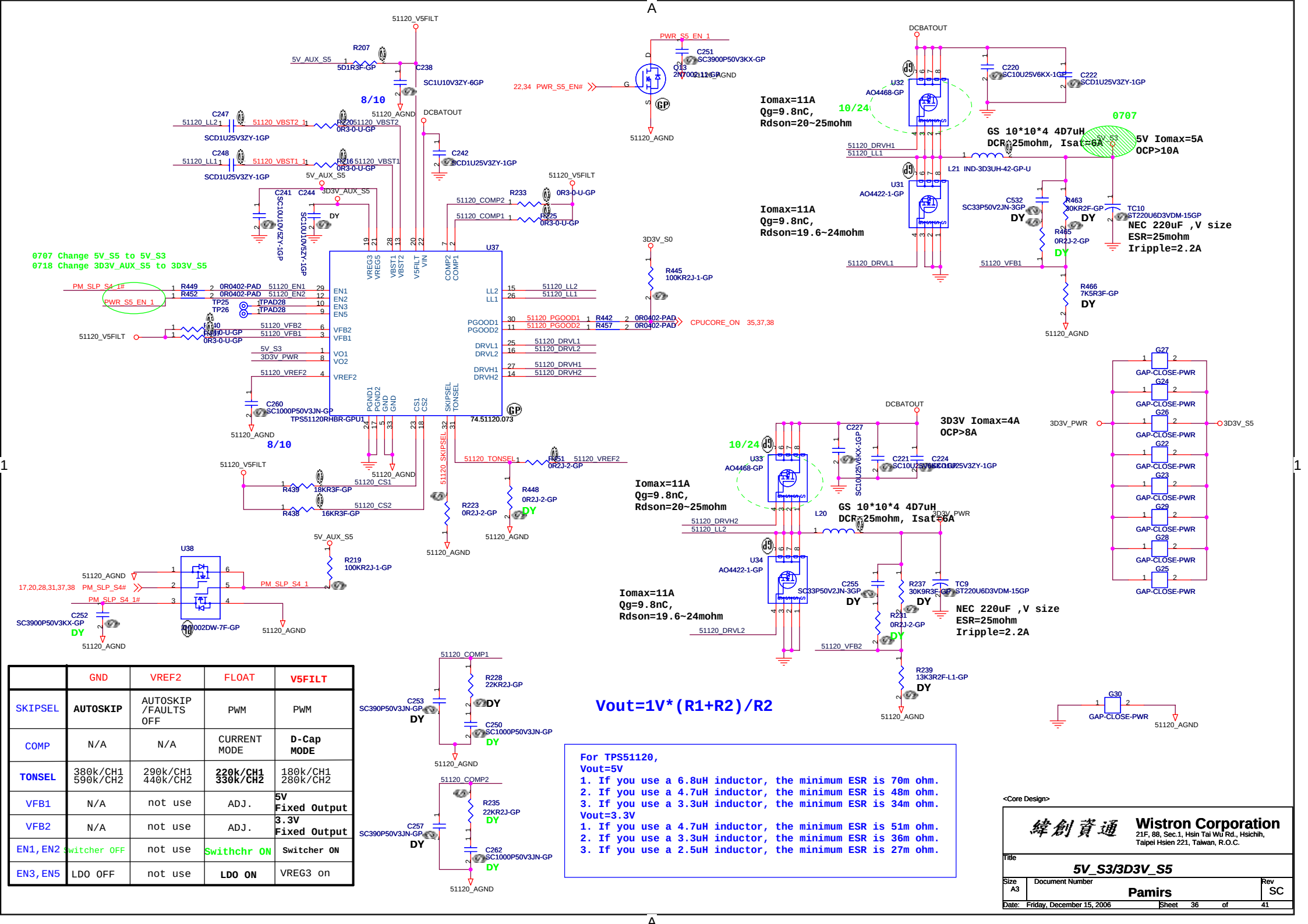
Finger Printer



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWRPLANE&RESETLOGIC***
Size A3	Document Number: **Pamirs** Rev: **SC**
Date: Monday, December 18, 2006	Sheet 34 of 41


0716
5V_S0
DCBATOUT
DY
12/12
36A/44A
VCC_CORE_S0
12/18
10/24
SB
MAX8736AGTL-GP-U
MAX8552ETB-1-GP
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCCPUCORE
Size A3
Document Number
Pamirs
Rev SC
Date: Wednesday, December 20, 2006
Sheet 35 of 41



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S3/3D3V_S5

Size: A3 | Document Number: Pamirs | Rev: SC

Date: Friday, December 15, 2006 | Sheet 36 of 41

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

0721

5V_S5 — R168 DUMMY-R2 — 5V_MAX8743_VCC
5V_S3 — R171 0R3-0-U-GP

1D8V / 7.0A
OCP>=14A

1D8V_S3 — 1D8V_PWR
G57 G56 G60 G59 G58 G61 G55 G62 — GAP-CLOSE-PWR

DCBATOUT
C217 EC77 SC10U25V6KX-1GP
SCD1U25V3ZY-1GP
U26 AO4468-GP — 10/24

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

L16
TC8 SE220U2D5VDM-3GP — DY
C197 SCD1U25V3ZY-1GP
Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

U27 FDS6690DS-GP

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

R180 8K2R3F-GP
R181 10KR3F-L-GP
Voutsetting=1.820V

5V_MAX8743_VCC
C199 SCD1U10V2MX-3GP
C198 SC1U10V3ZY-8GP
C211 SCD1U10V2MX-3GP
C207 SC1U25V5ZY-4GP
8/18

R173 10R3J-3-GP
D15 BAW56-7-F-GP

MAX8743_BST2
MAX8743_VCC
R369 100KR2F-L1-GP
C208 SC1U10V3ZY-6GP
R362 100KR2F-L1-GP
R377 0R3-0-U-GP
R363 90K9R3F-GP
C210 SCD1U25V3ZY-1GP
R357 90K9R3F-GP
R387 0R3-0-U-GP
C196 SCD1U25V3ZY-1GP

U22 MAX8743EEI-1-GP
74.08743.A79

UVP	VCC	VDD	V+
ILIM1			ILIM2
BST1			BST2
DH1			DH2
LX1			LX2
DL1			DL2
CS1			CS2
OUT1			OUT2
FB1			FB2
ON1			ON2
TON			PGOOD
REF			OVP
SKIP#		GND	

MAX8743_ILIM1 MAX8743_BST1R MAX8743_DH1 MAX8743_LX1 MAX8743_DL1
MAX8743_BST2R MAX8743_DH2 MAX8743_LX2 MAX8743_DL2
MAX8743_ON1 MAX8743_TON MAX8743_VREF MAX8743_FB1
MAX8743_ON2 MAX8743_PGOOD MAX8743_FB2

C434 SCD47U10V3KX-3GP
DY C435 SCD1U25V3ZY-1GP

DCBATOUT
U30 AO4468-GP — 10/24
U29 FDS6690DS-GP

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5

EC82 SCD1U25V3ZY-1GP
C216 SC10U25V6KX-1GP
C214 SC10U25V6KX-1GP

1D5V_S0/5A
OCP>=10A

1D5V_PWR — 1D5V_S0
G19 G17 G18 G21 G20 — GAP-CLOSE-PWR

L17
TC7 SE220U2VDM-8GP
DY C194 SCD1U25V3ZY-1GP
Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

R156 5K11R2F-L1-GP
R162 10KR3F-L-GP
Voutsetting=1.511V

Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

R365 0R0402-PAD — CPUCORE_ON 35,36,38

5V_MAX8743_VCC
R367 0R2J-2-GP — DY 8/18
MAX8743_VREF
R366 DUMMY-R2
R368 DUMMY-R2

0205
PM_SLP_S3# — R373 220KR2J-L2-GP
PM_SLP_S4# — DY R364 220KR2J-L2-GP
MAX8743_SKIP#
C202 SC1000P50V3JN-GP
R169 0R2J-2-GP — DY

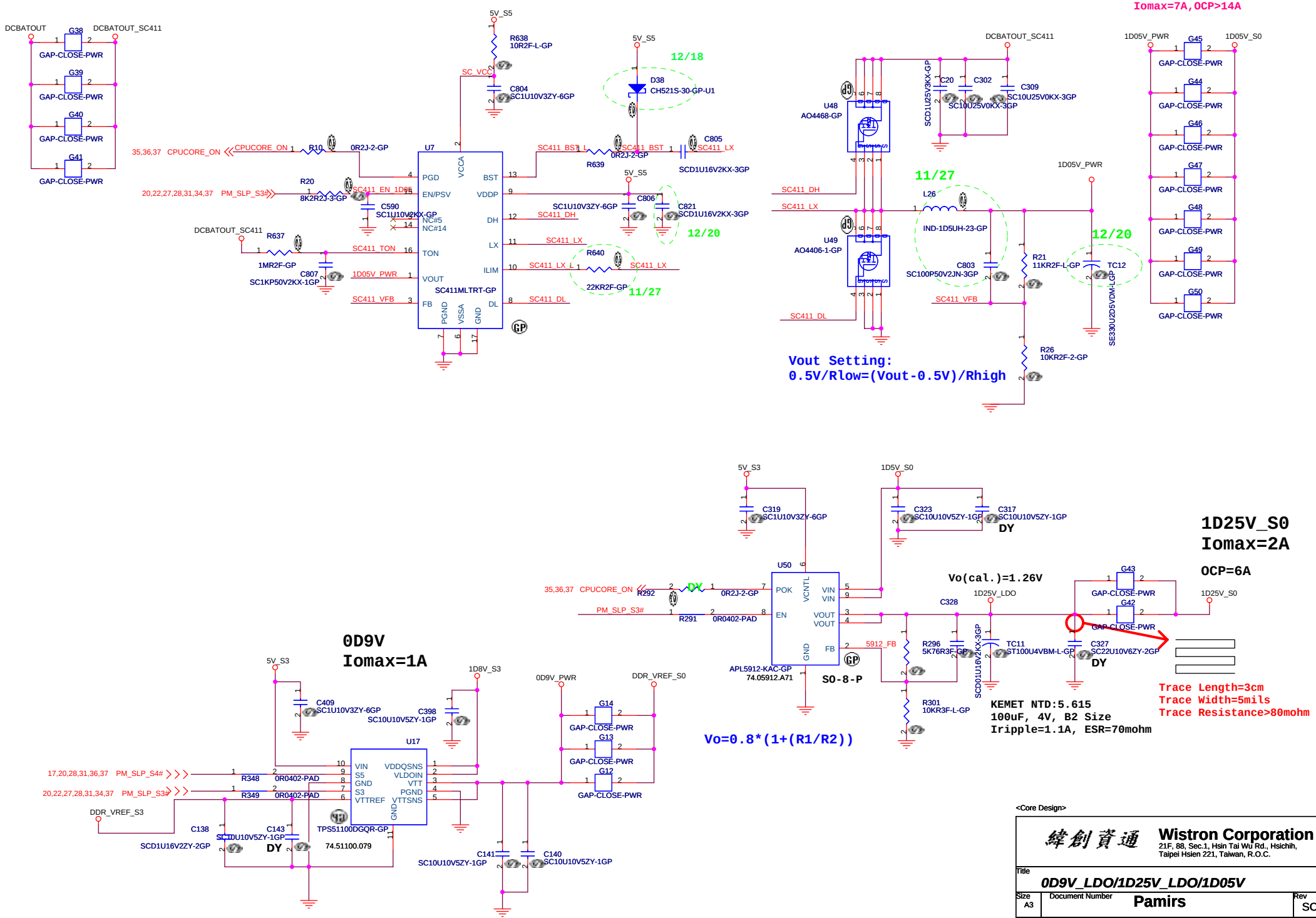
17,20,28,31,36,38 PM_SLP_S4# — R360 5K1R2-GP — MAX8743_ON1
20,22,27,28,31,34,38 PM_SLP_S3# — R361 5K1R2-GP — MAX8743_ON2
0830 SB

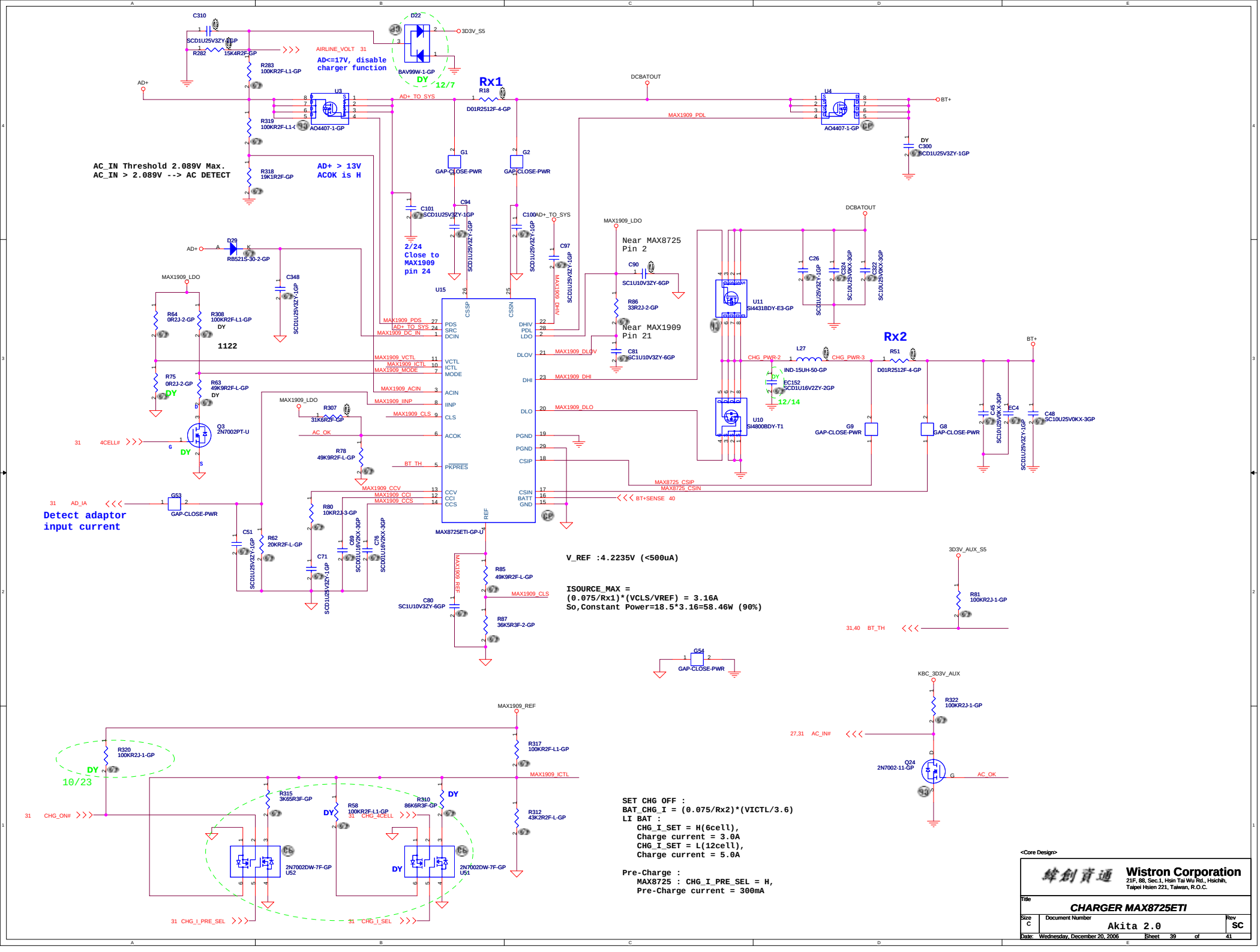
Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

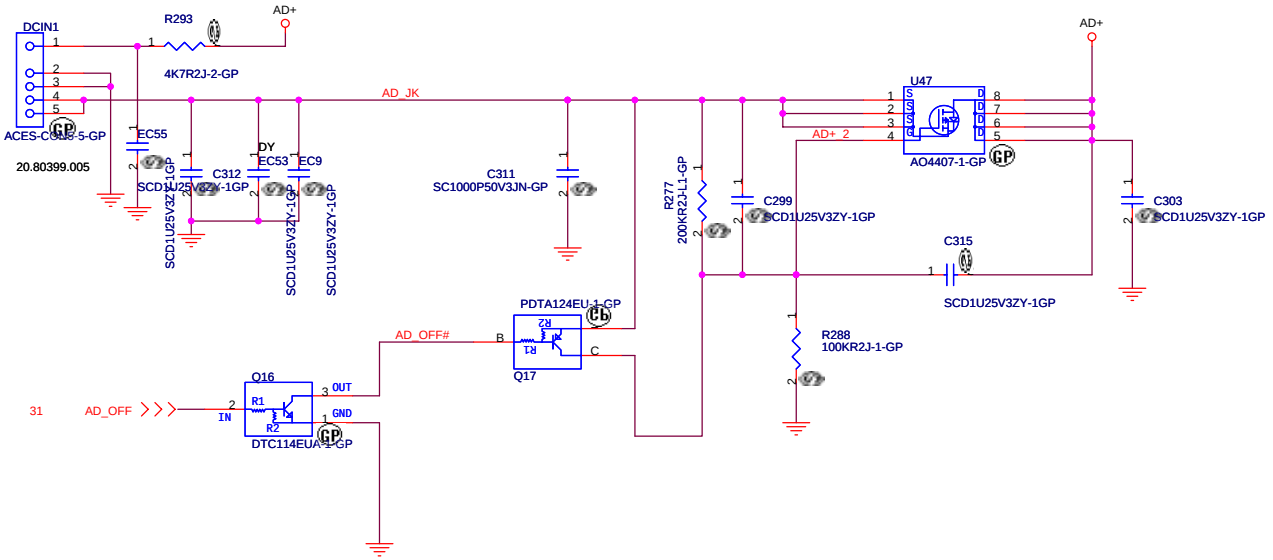
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V_S3/1D5V_S0*
Size: A3 | Document Number: Pamirs | Rev: SC
Date: Friday, December 15, 2006 | Sheet 37 of 41

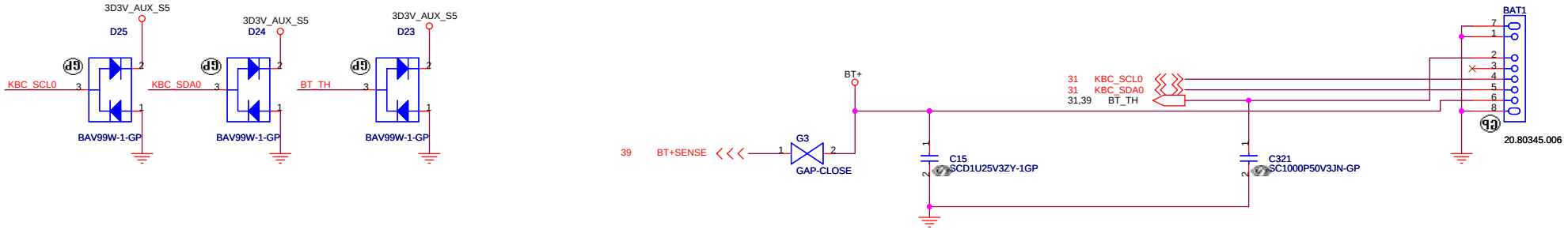

Iomax=7A,OCP>14A
DCBATOUT
DCBATOUT_SC411
GAP-CLOSE-PWR
5V_S5
R638 10R2F-L-GP
SC_VCC
C804 SC1U10V3ZY-6GP
D38 CH521S-30-GP-U1
12/18
35,36,37 CPUCORE_ON
R10 0R2J-2-GP
U7
SC411_BST_L
R639 0R2J-2-GP
SC411_BST
C805 SCD1U16V2KX-3GP
SC411_LX
20,22,27,28,31,34,37 PM_SLP_S3#
R20 8K2R2J-3-GP
SC411_EN_1D05
C590 SC1U10V2KX-GP
C806 SC1U10V3ZY-6GP
C821 SCD1U16V2KX-3GP
12/20
SC411_DH
SC411_LX
SC411_TON
SC411_VFB
SC411_DL
1D05V_PWR
R637 1MR2F-GP
C807 SC1KP50V2KX-1GP
R640 22KR2F-GP
11/27
SC411MLTRT-GP
PGD
EN/PSV
NC#5
NC#14
TON
VOUT
FB
VCCA
BST
VDDP
DH
LX
ILIM
DL
PGND
VSSA
GND
U48 AO4468-GP
U49 AO4406-1-GP
C20 SCD11U25V3KX-GP
C302
C309 SC10U25V0KX-3GP
SC10U25V0KX-3GP
L26 IND-1D5UH-23-GP
C803 SC100P50V2JN-3GP
R21 11KR2F-L-GP
TC12 SE330U2D5VDM-L-GP
R26 10KR2F-2-GP
Vout Setting:
0.5V/Rlow=(Vout-0.5V)/Rhigh
1D05V_S0
G38
G39
G40
G41
G44
G45
G46
G47
G48
G49
G50
1D25V_S0
Iomax=2A
OCP=6A
5V_S3
C319 SC1U10V3ZY-6GP
C323 SC10U10V5ZY-1GP
C317 SC10U10V5ZY-1GP
DY
U50
35,36,37 CPUCORE_ON
R292
PM_SLP_S3#
R291 0R0402-PAD
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5912-KAC-GP
74.05912.A71
SO-8-P
5912_FB
Vo(cal.)=1.26V
1D25V_LDO
C328
R296 5K76R3F-GP
R301 10KR3F-L-GP
SCD01U16V2KX-3GP
TC11 ST100U4VBM-L-GP
C327 SC22U10V6ZY-2GP
G43
G42
Vo=0.8*(1+(R1/R2))
KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm
0D9V
Iomax=1A
1D8V_S3
0D9V_PWR
DDR_VREF_S0
C409 SC1U10V3ZY-6GP
C398 SC10U10V5ZY-1GP
U17
17,20,28,31,36,37 PM_SLP_S4#
20,22,27,28,31,34,37 PM_SLP_S3#
R348 0R0402-PAD
R349 0R0402-PAD
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
TPS51100DGQR-GP
74.51100.079
DDR_VREF_S3
C138 SCD1U16V2ZY-2GP
C143 SC10U10V5ZY-1GP
DY
C141 SC10U10V5ZY-1GP
C140 SC10U10V5ZY-1GP
G14
G13
G12
GAP-CLOSE-PWR
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
0D9V_LDO/1D25V_LDO/1D05V
Size A3
Document Number
Pamirs
Rev SC
Date: Wednesday, December 20, 2006
Sheet 38 of 41


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable charger function
Rx1
Rx2
Near MAX8725 Pin 2
Near MAX1909 Pin 21
2/24 Close to MAX1909 pin 24
1122
Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
AO4407-1-GP
SI4431BDY-E3-GP
SI4800BDY-T1
2N7002DW-7F-GP
2N7002PT-U
Q24 2N7002-11-GP
D01R2512F-4-GP
IND-15UH-50-GP
RB521S-30-2-GP
BAV99W-1-GP
GAP-CLOSE-PWR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Akita 2.0
Wednesday, December 20, 2006
Sheet 39 of 41

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



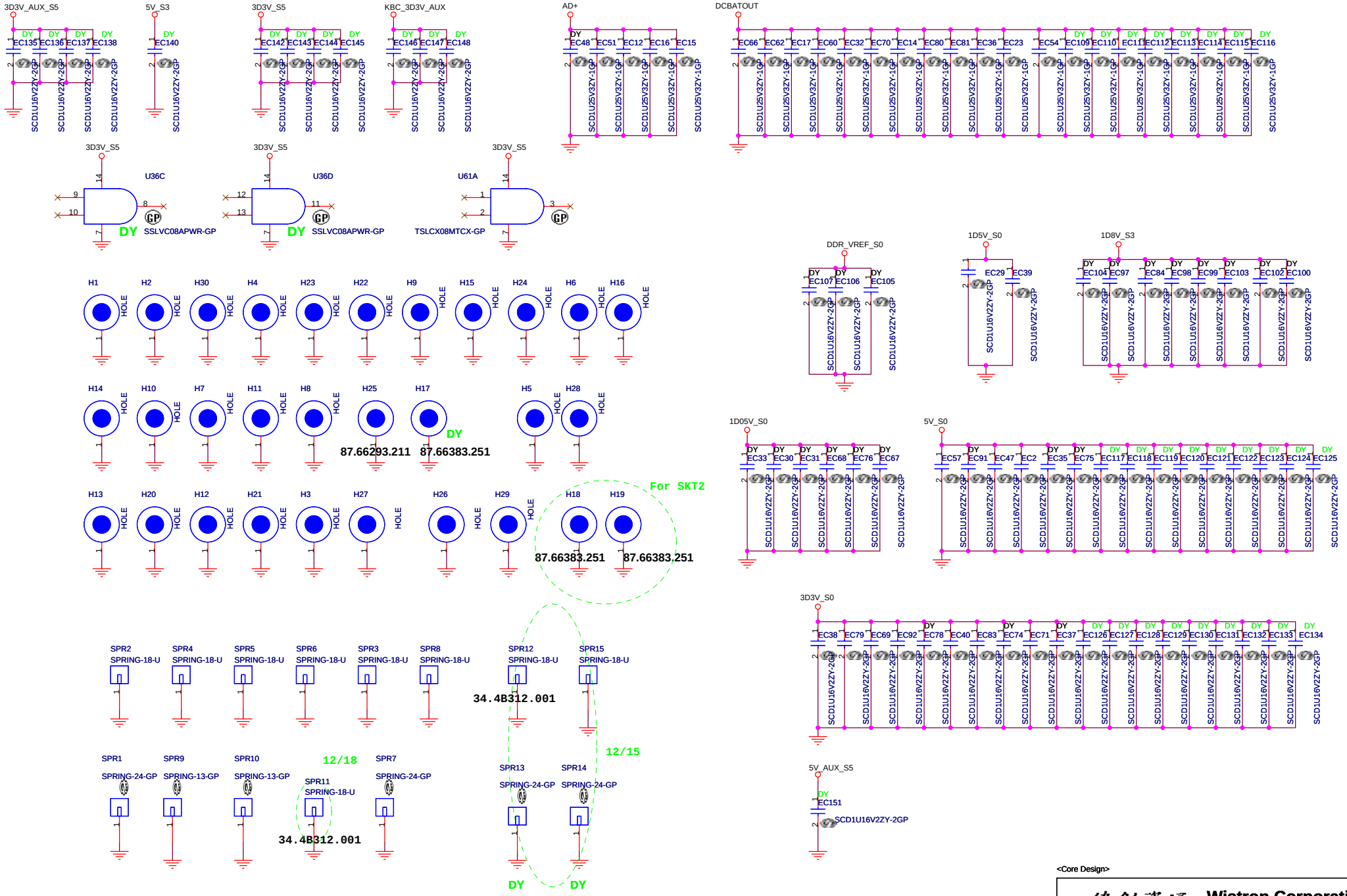
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	Akita 2.0	SC

Date: Friday, December 15, 2006 Sheet 40 of 41



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size	Document Number	Rev
A3	Pamirs	SC

Date: Wednesday, December 20, 2006 Sheet 41 of 41