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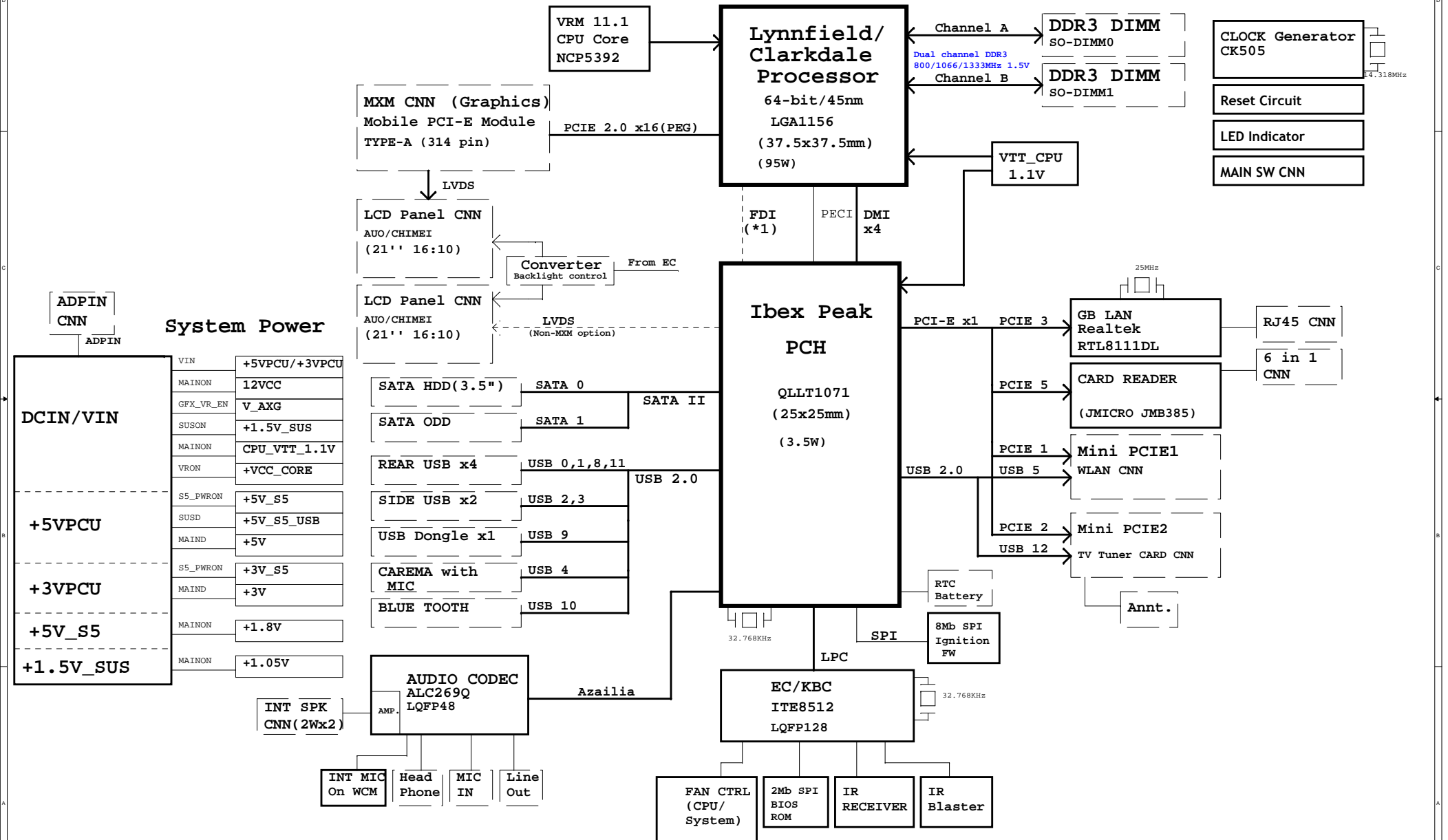


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PROJECT : ZN2

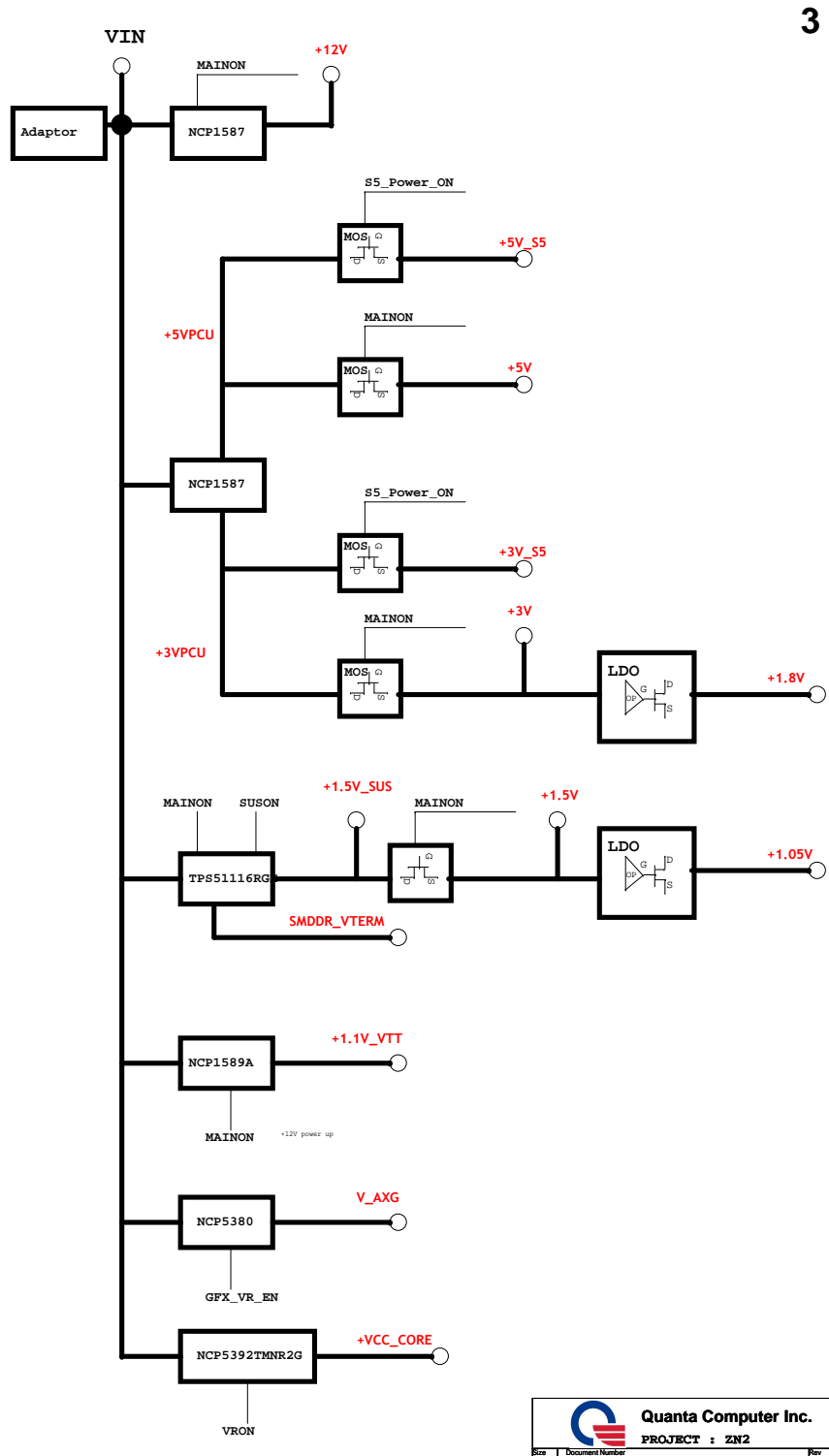
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Block Diagram :

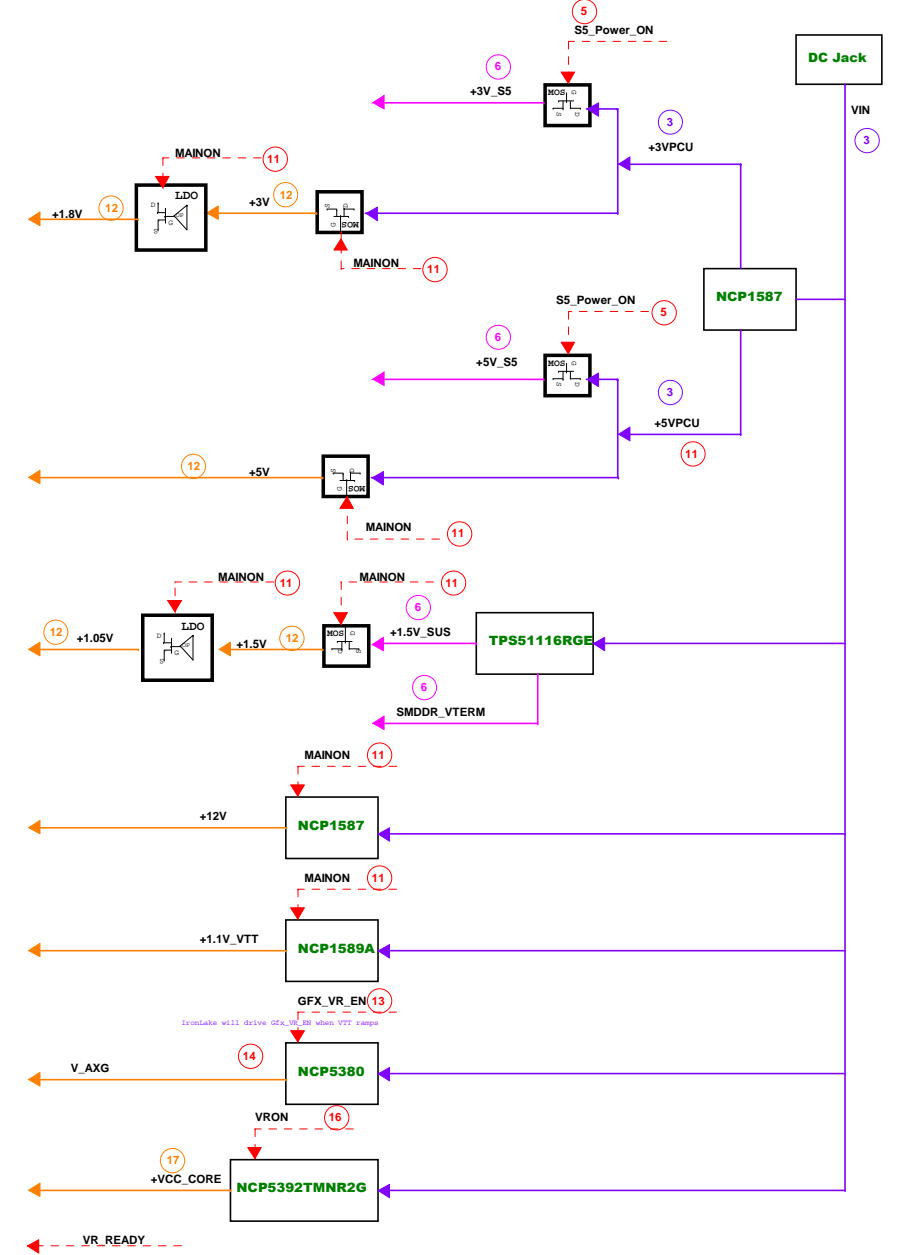
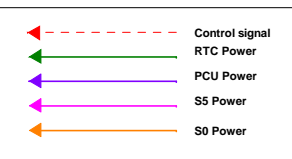
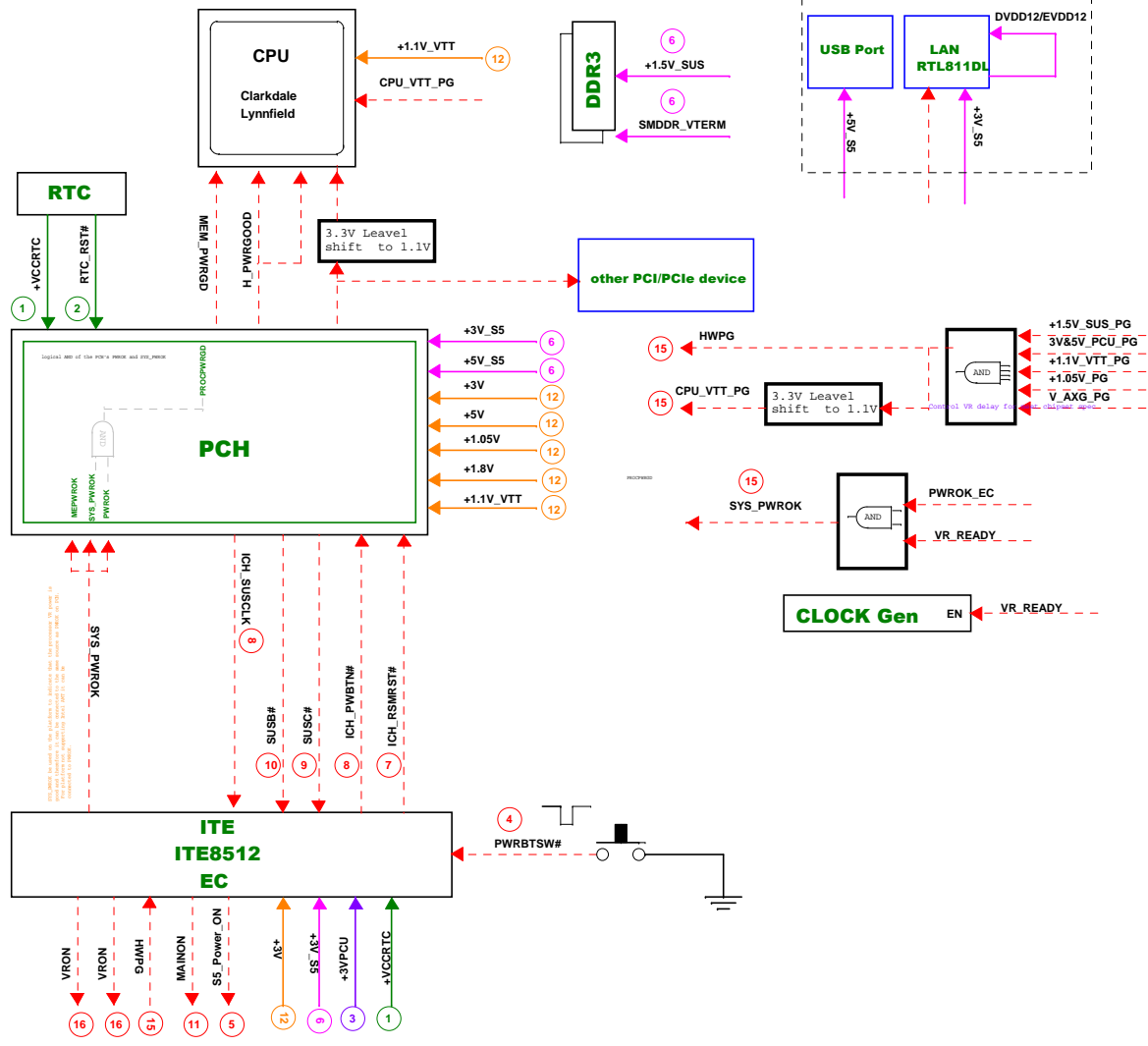


(*1)FDI - Used only for the Clarkdale processor.

Power Rail	Destination	Voltage	SO Current
+VCC_CORE	Lynnfield : Default for initial power up	0.65V-1.4V 1.1V	90A(TDC)
V_AXG	for 92W TDP SKU for 79W TDP SKU	0.5-1.3V	10A (TDC) 16A (TDC)
+1.1V_VTT	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V-1.1V-1.155V 1.1V 1.05V-1.1V-1.16V	30A(TDC) 0.065A 0.001A
+1.8V	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F	1.71V-1.8V-1.89V 1.71V-1.8V-1.89V 1.71V-1.8V-1.89V	1.1A 0.196A 0.156A
+1.5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V-1.5V-1.575V	6A
SMDDR_VTERM	DDRIII Terminator:	0.75V	2A
+1.05V	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power	0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V	1.629A 3.251A 0.065A 0.075A 0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)		
+3V	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CH7308 : LVDD ALC662S : DVDD Mini PCIE : +3.3V(WLAN) CAREMA	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.357A 0.069A
+5V	Ibex Peak : Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) ALC662S : AVDD Touch Screen LCD Panel USB: x 12 ports	4.75V-5V-5.25V 5V	0.001A 6A
MXM_12V HDD_12V			
+3V_S5	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN 82578DM : VDD CLK Gen.CK505 : VDD EC(IT8512) : VSTBY SPI FLASH ROM	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.086A 0.168A 0.006A
+5V_S5	Ibex Peak : Suspend well Ref. Voltage	4.75V-5V-5.25V	0.001A
	INVERTER : Vin FAN_CPU		
+3VPCU			
+5VPCU			
15VPCU			
VIN			



Power Sequence



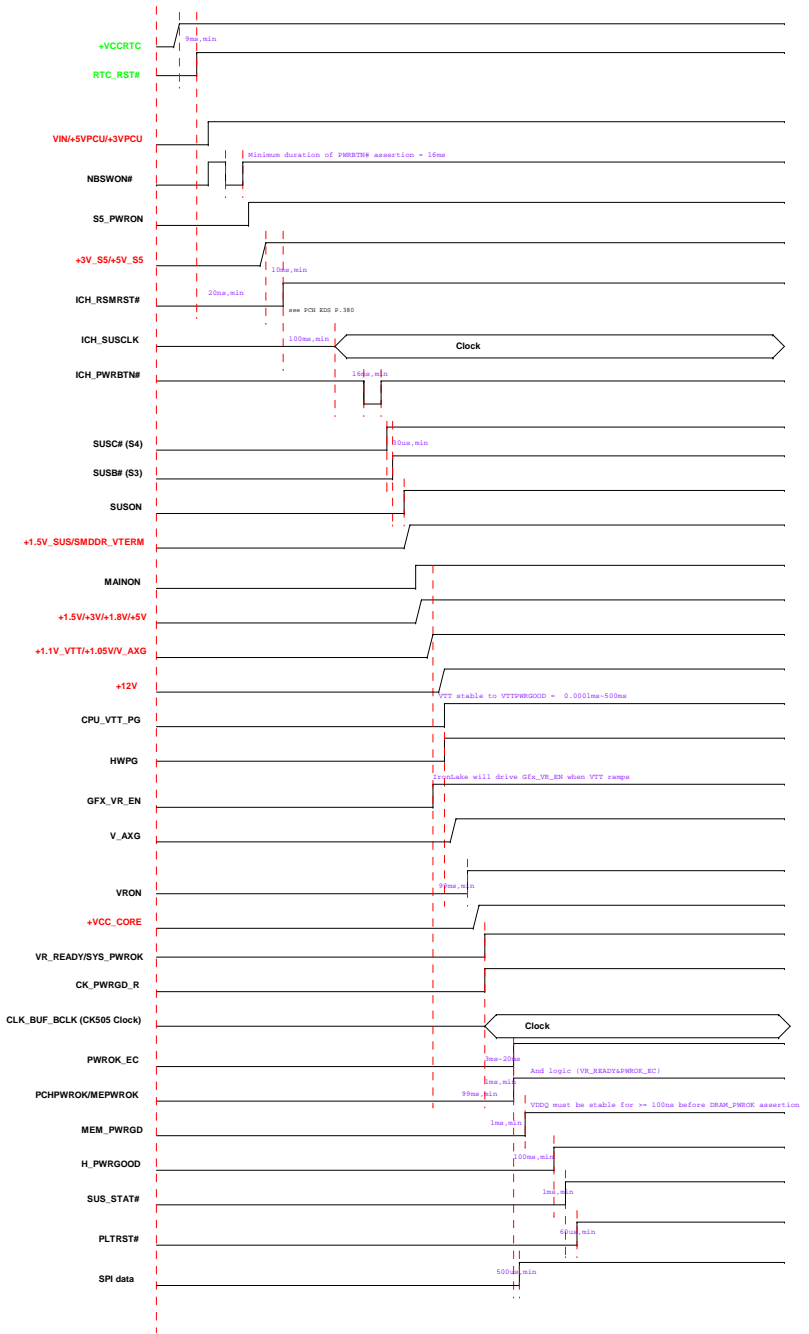
POWER SEQUENCE

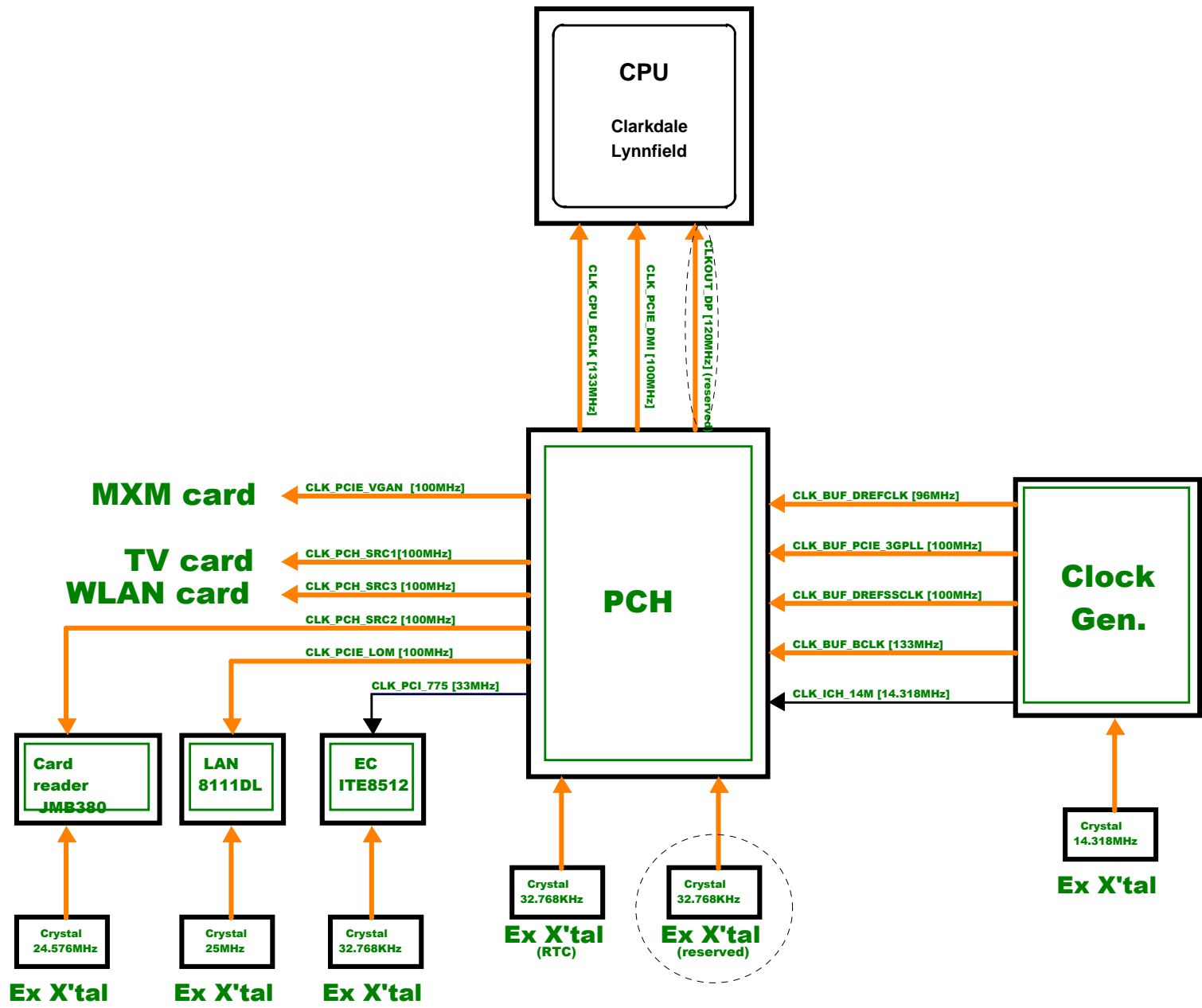
Voltage Rails

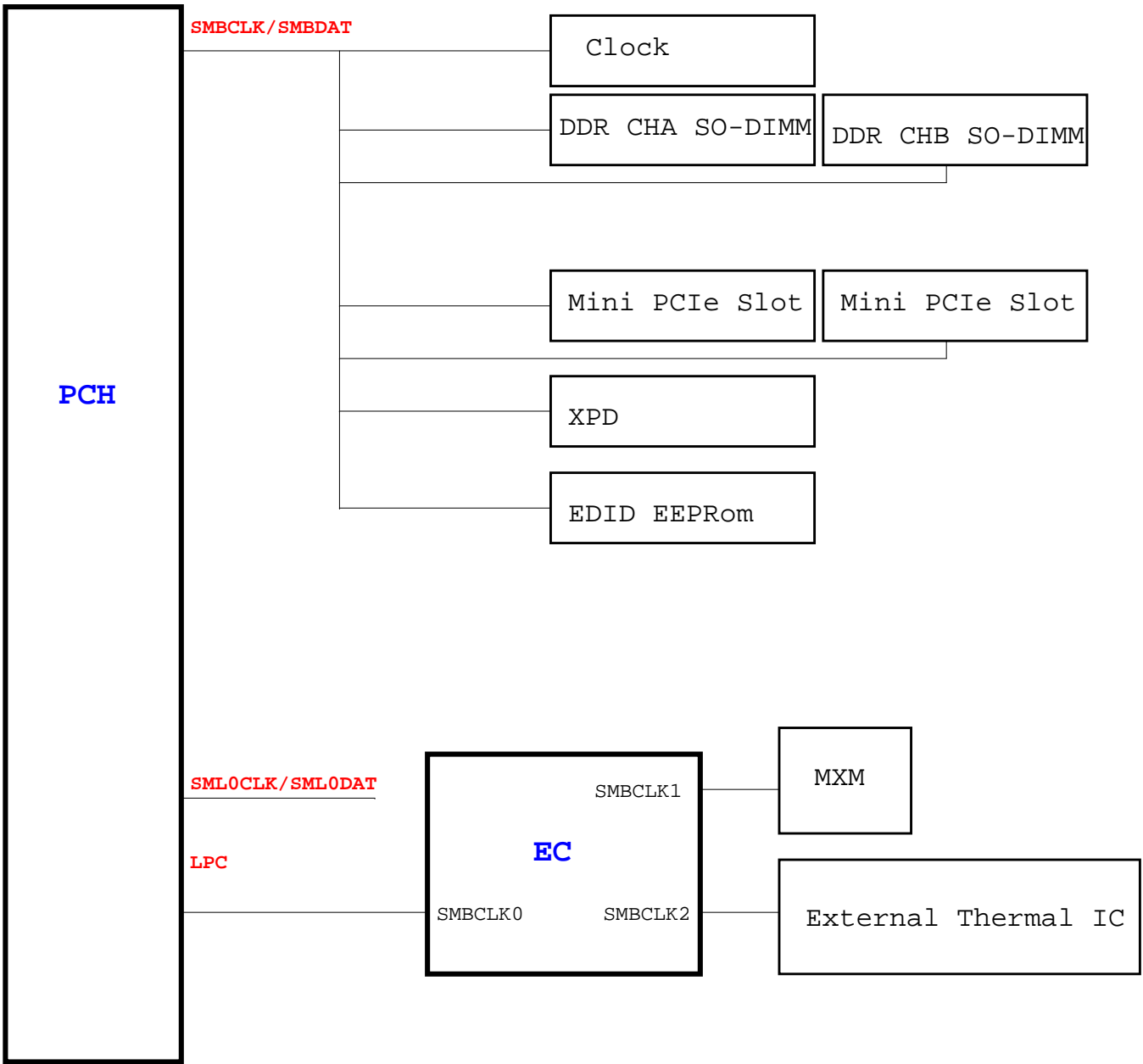
Power	Voltage	S0	S3	S4	S5	PCU	G3	Ch Signal
+VCCRTC	3V	ON	ON	ON	ON	ON	ON	
VN	19.5V	ON	ON	ON	ON	ON	OFF	Adapter In
+5VPCU	5V	ON	ON	ON	ON	ON	OFF	Adapter In
+3VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adapter In
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_PWRON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_PWRON
+1.5V_S0S	1.5V	ON	ON	OFF	OFF	OFF	OFF	SUSON
SMODR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	OFF	SUSON
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.2V	1.2V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.1V_VTT	1.1V/1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
V_AXG	??V	ON	OFF	OFF	OFF	OFF	OFF	GFV_VR_EN
+VCC_CORE	??V	ON	OFF	OFF	OFF	OFF	OFF	VRON

EC
PCH BUS,
Sys Management, PCH Resume Well, Intel HD Audio, USB, WLAN,
DDR3 Memory
DDR3 Memory
SATA, PCI REF
PCI Express, SATA, HV CMOS, CRT, Band Gap voltages, Intel HD Audio
Mini PCIe, Intel HD Audio
PCH core, PCH PLL voltages, PCH CLK Buffer, SATA, USB, PCH fuse, Display Link, Display Port, PCIe
LVDSIO, SFR, FLASH
CPU VTT, FDUPEG, DMI, VCCTADDR, PCH DMLPCH V, CPU_ID
Mini PCIe, Intel HD Audio
CPU Core

Power	Voltage	S0	S3	S4	S5	PCU	G3
VN_MXM							
+5V_MXM							
+3V_MXM							
USBVCC2							
3VPCU_EC							
LCDEVCC							
OCV_PMR							
VIN_LCD							
VDDA_CODEC							



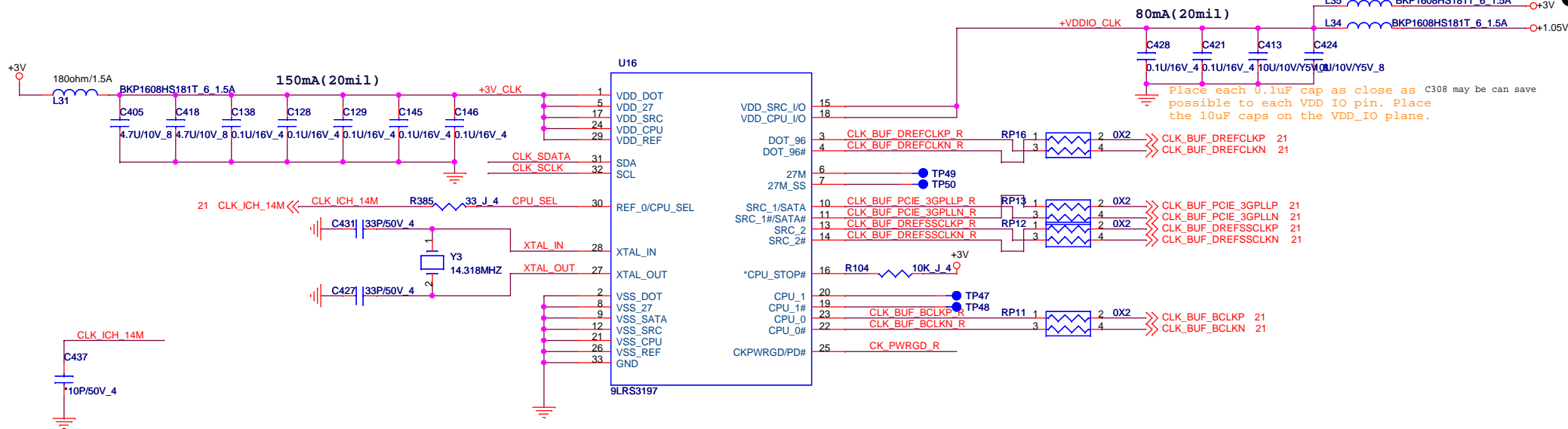




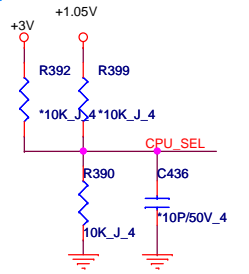
NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITIAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
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Clock Generator

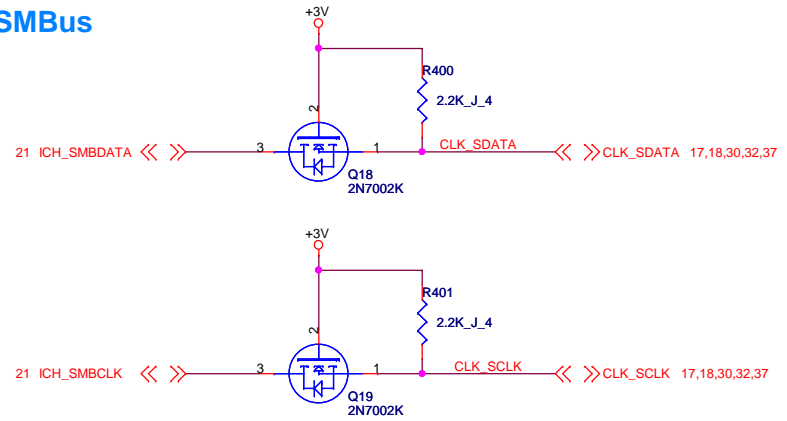


CPU_CLK select

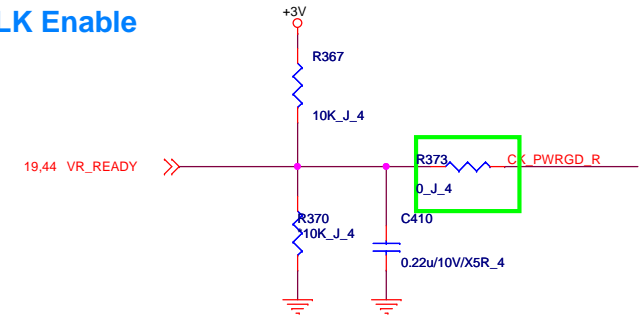



CPU_SEL	0	1
	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable

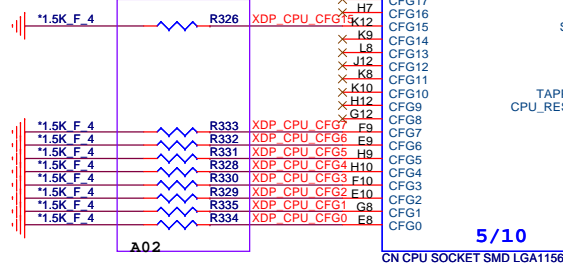
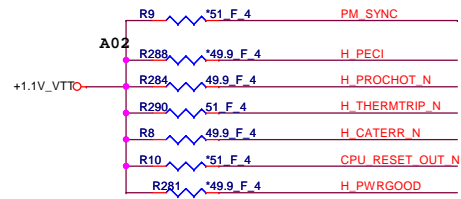
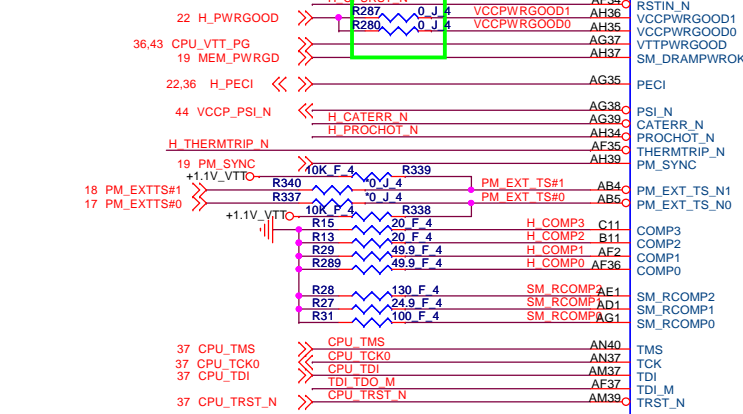




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	Clock Generator	A
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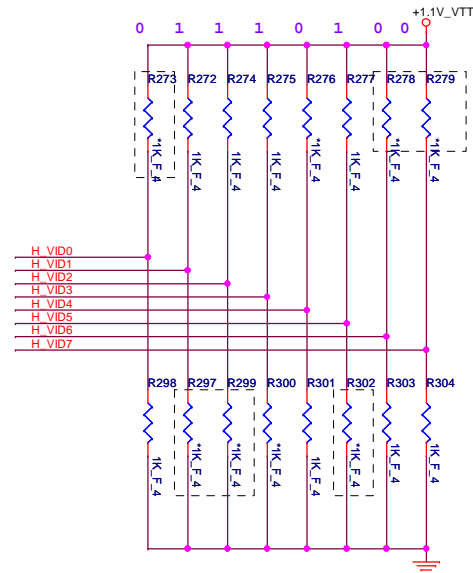
120MHz DP REFCLK 21 DPCLK_PCH
 21 DPCLK_PCH# 21 DPCLK_PCH#
 133MHz CPU BCLK 22 CLK_CPU_BCLKP
 22 CLK_CPU_BCLKN 22 CLK_CPU_BCLKN



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CN CPU SOCKET SMD LGA1156

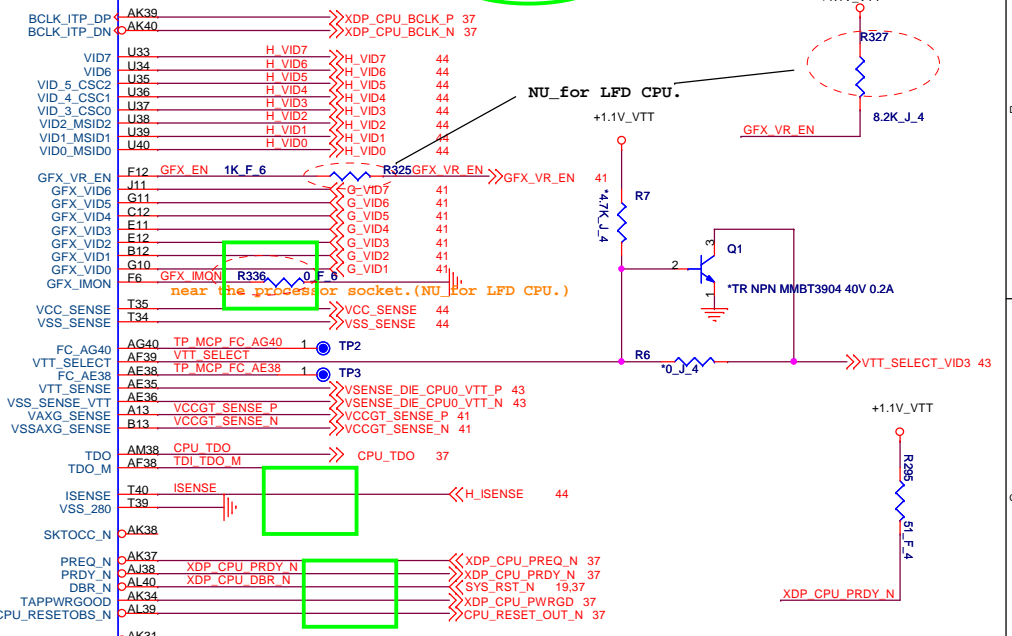
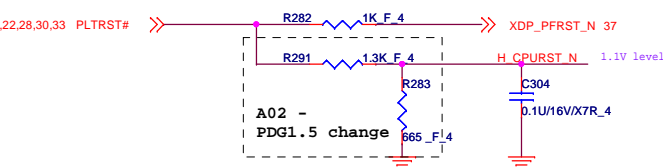
VID[7:0] : 00101110 => 1.325V@VCC_Max
 2009B FMB processors supported



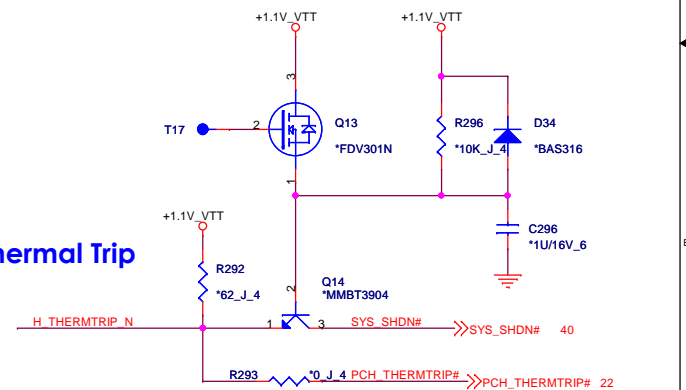
CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

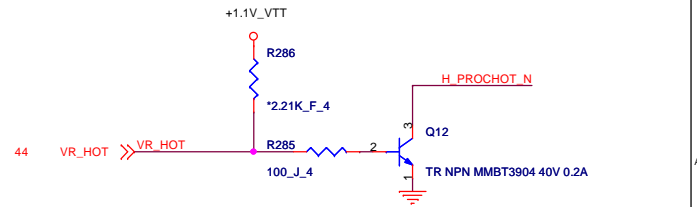
Need to be placed close to processor to minimize ESD risk



Thermal Trip

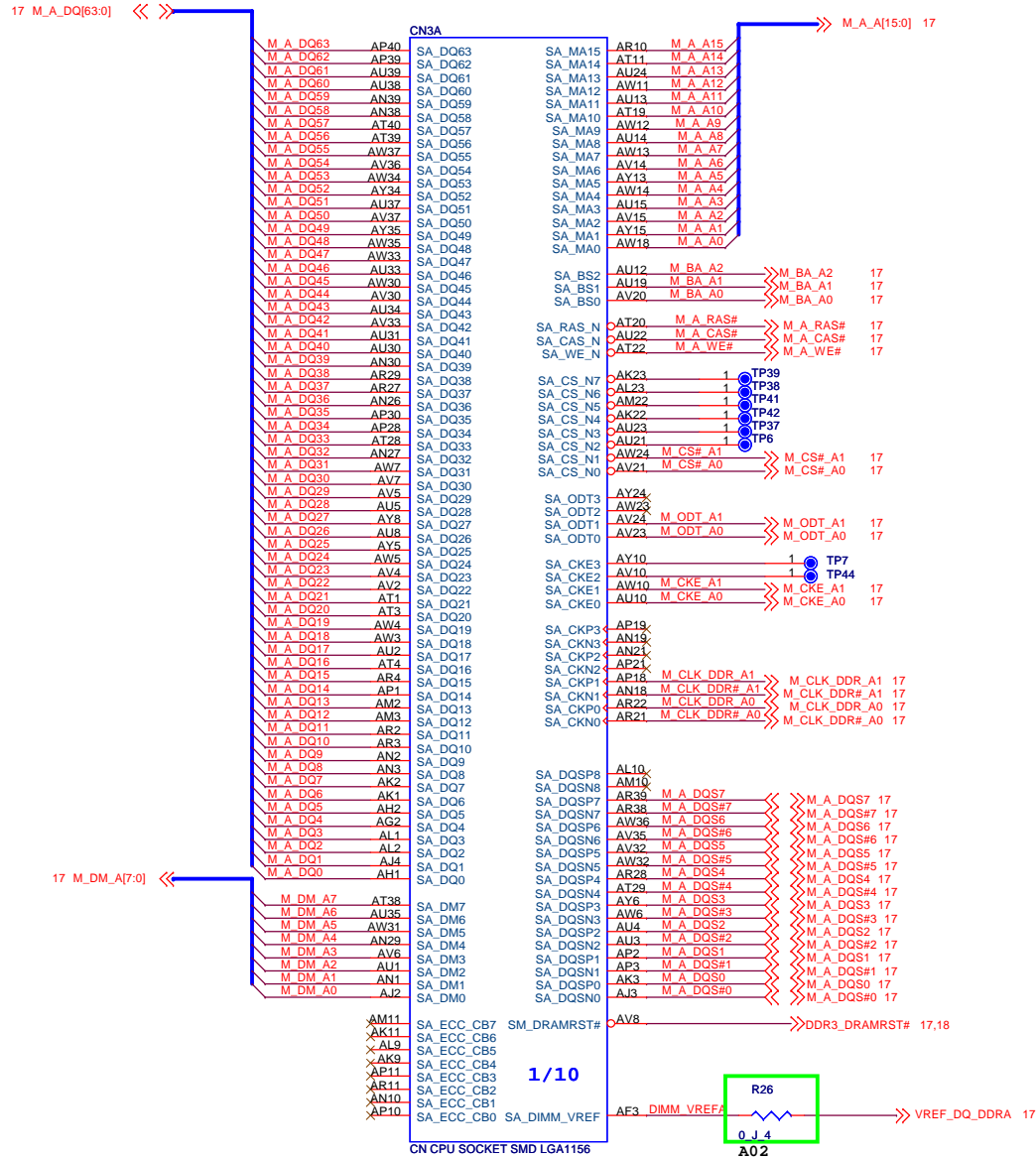


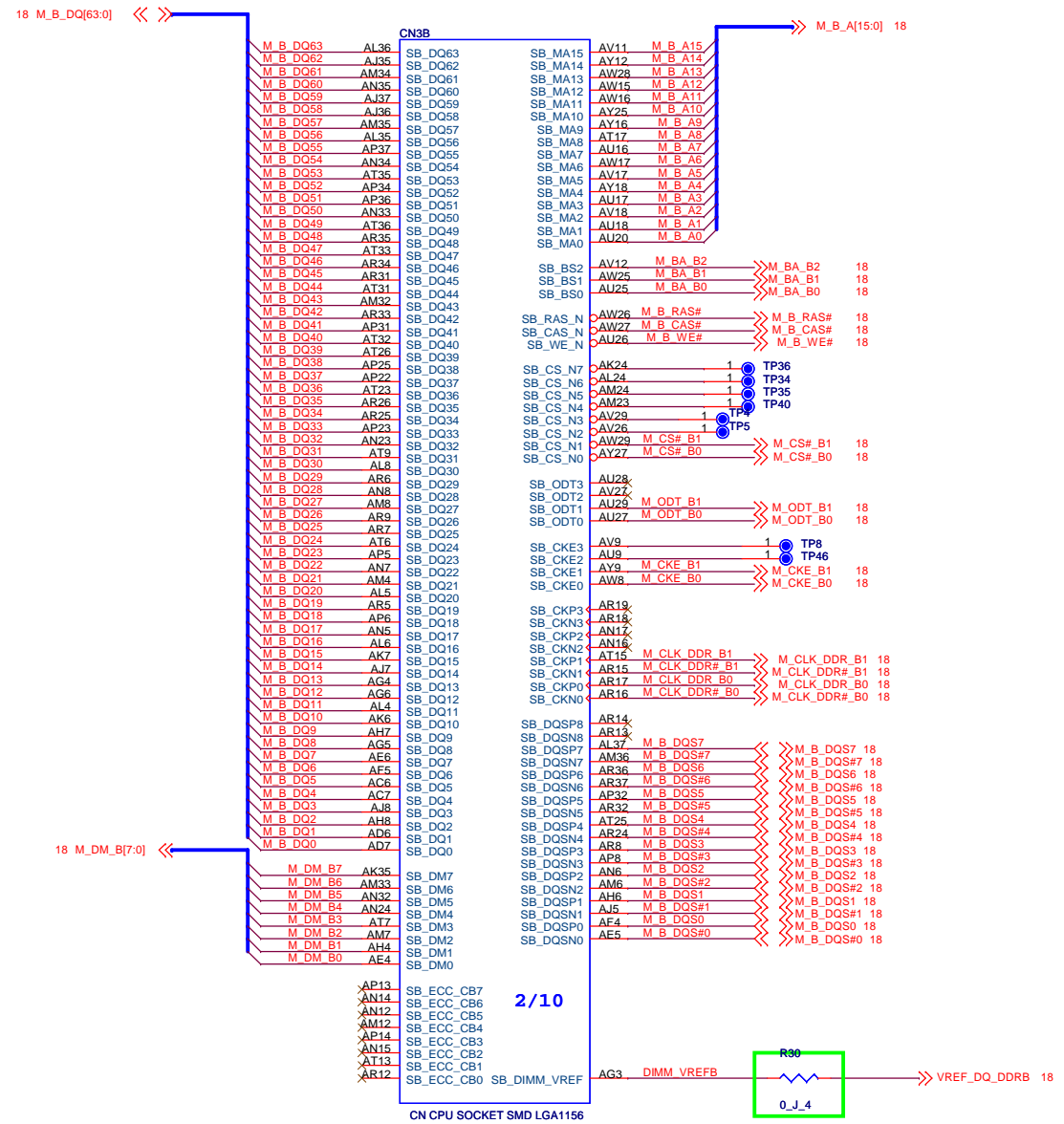
CAD NOTE:
 PLACE TDO TERMINATION NEAR XDP CONNECTOR
 PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

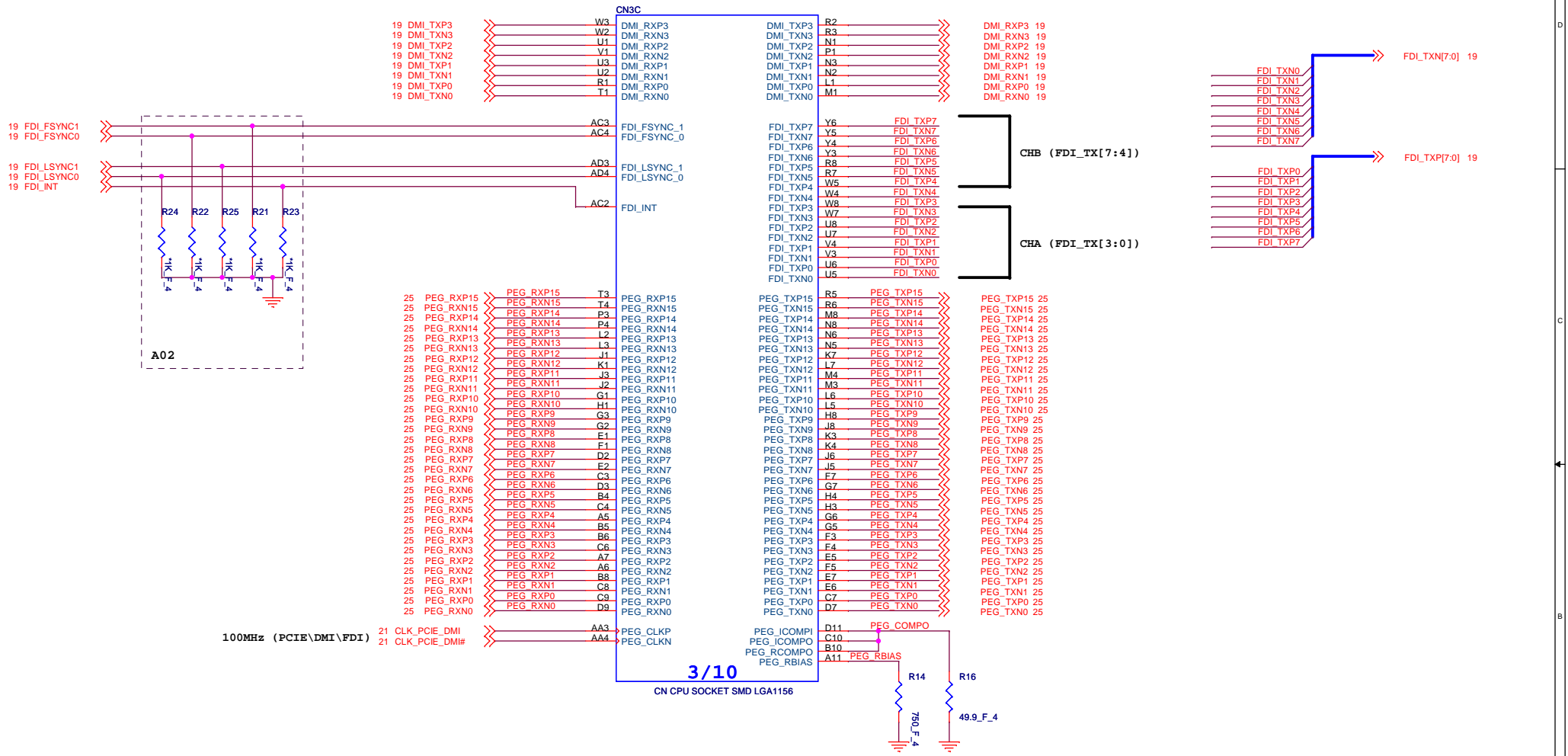


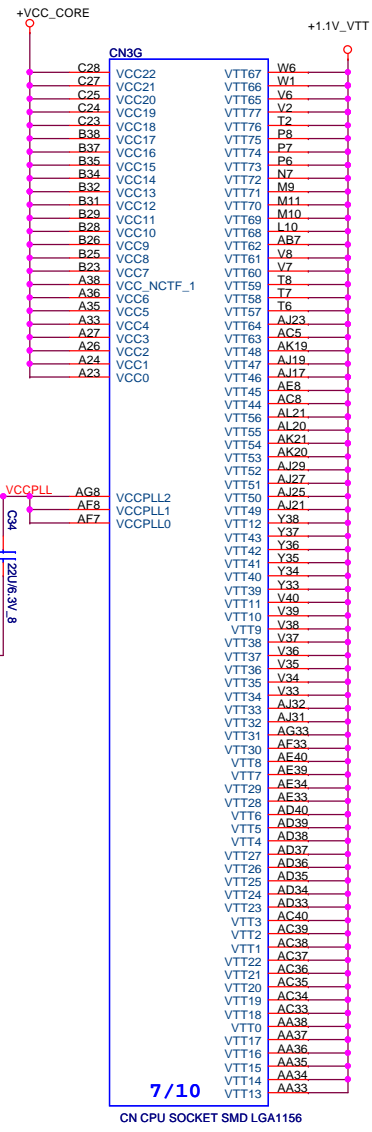
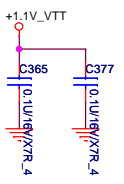
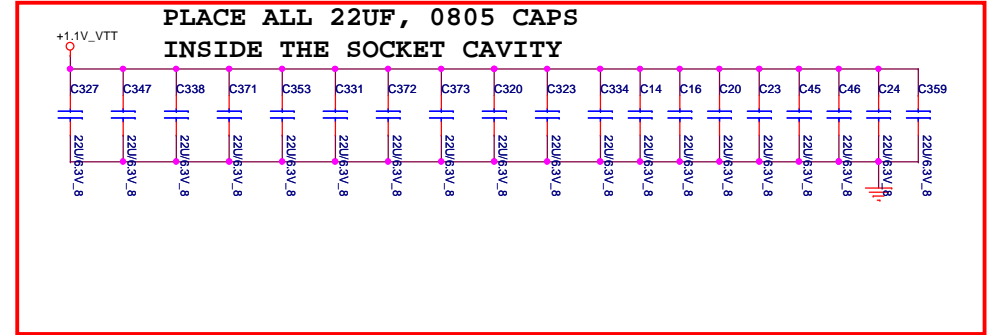
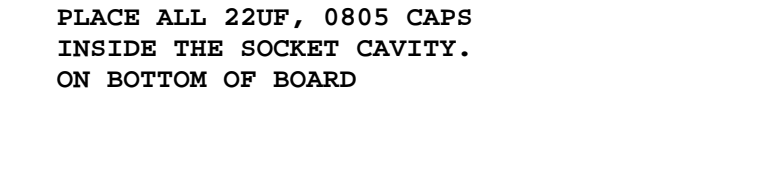
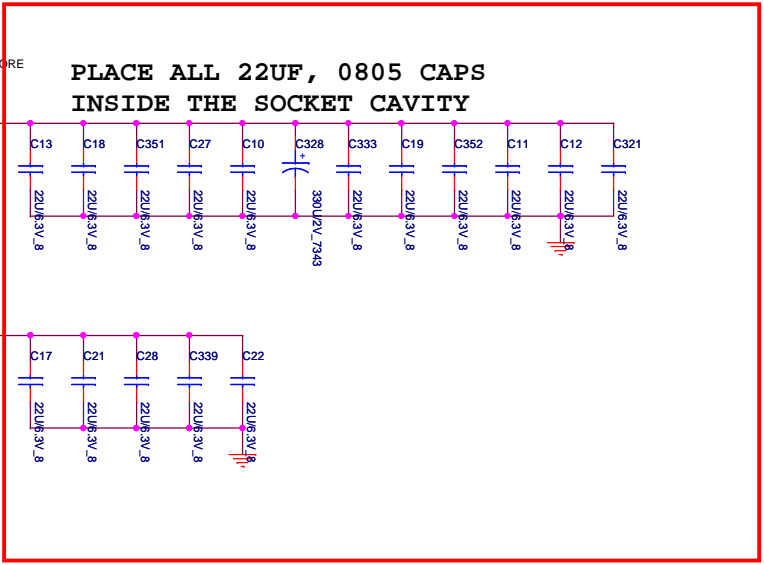
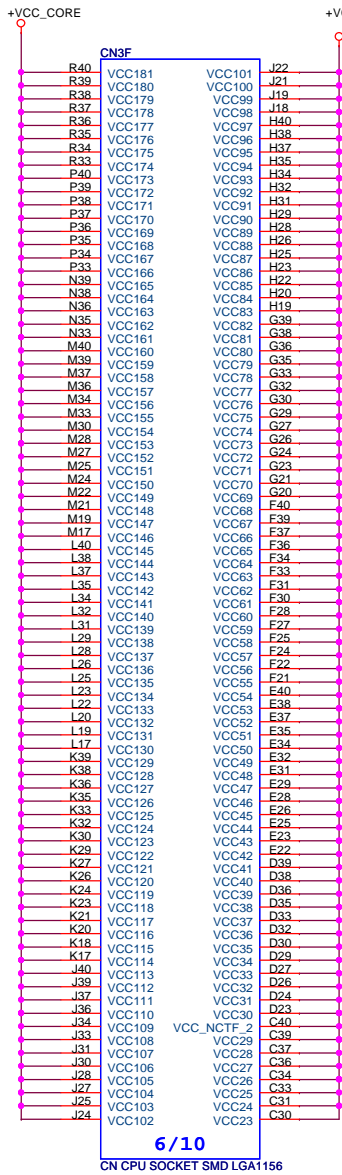
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	MCP (CLK/CTRL/MISC)	A
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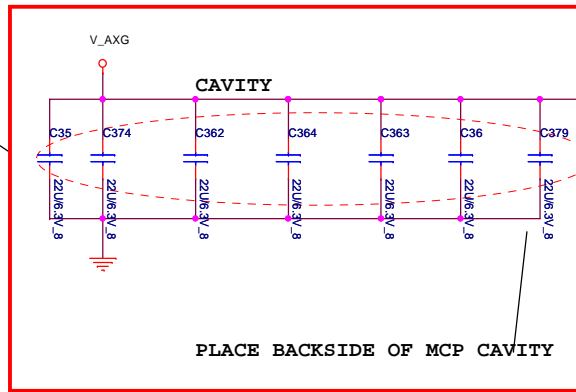




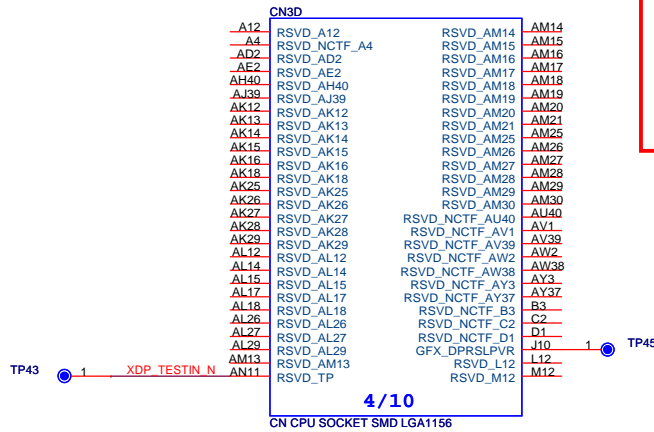
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	MCP (VCCP)	A
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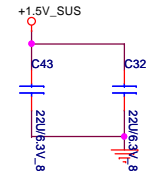
VAXG tie to GND for LFD CPU.



PLACE BACKSIDE OF MCP CAVITY



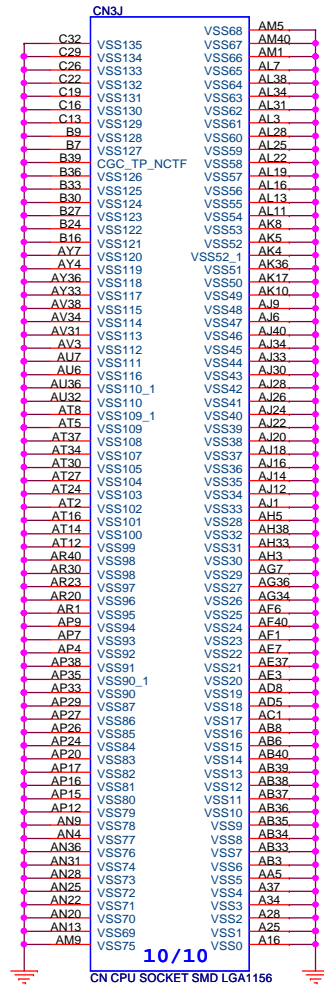
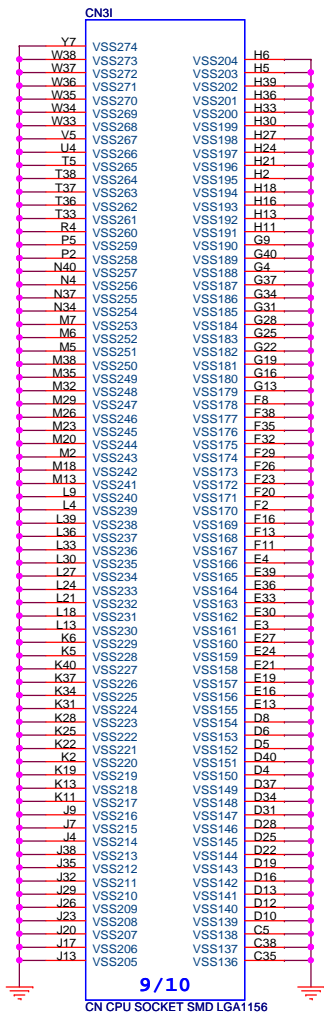
+1.5V_SUS

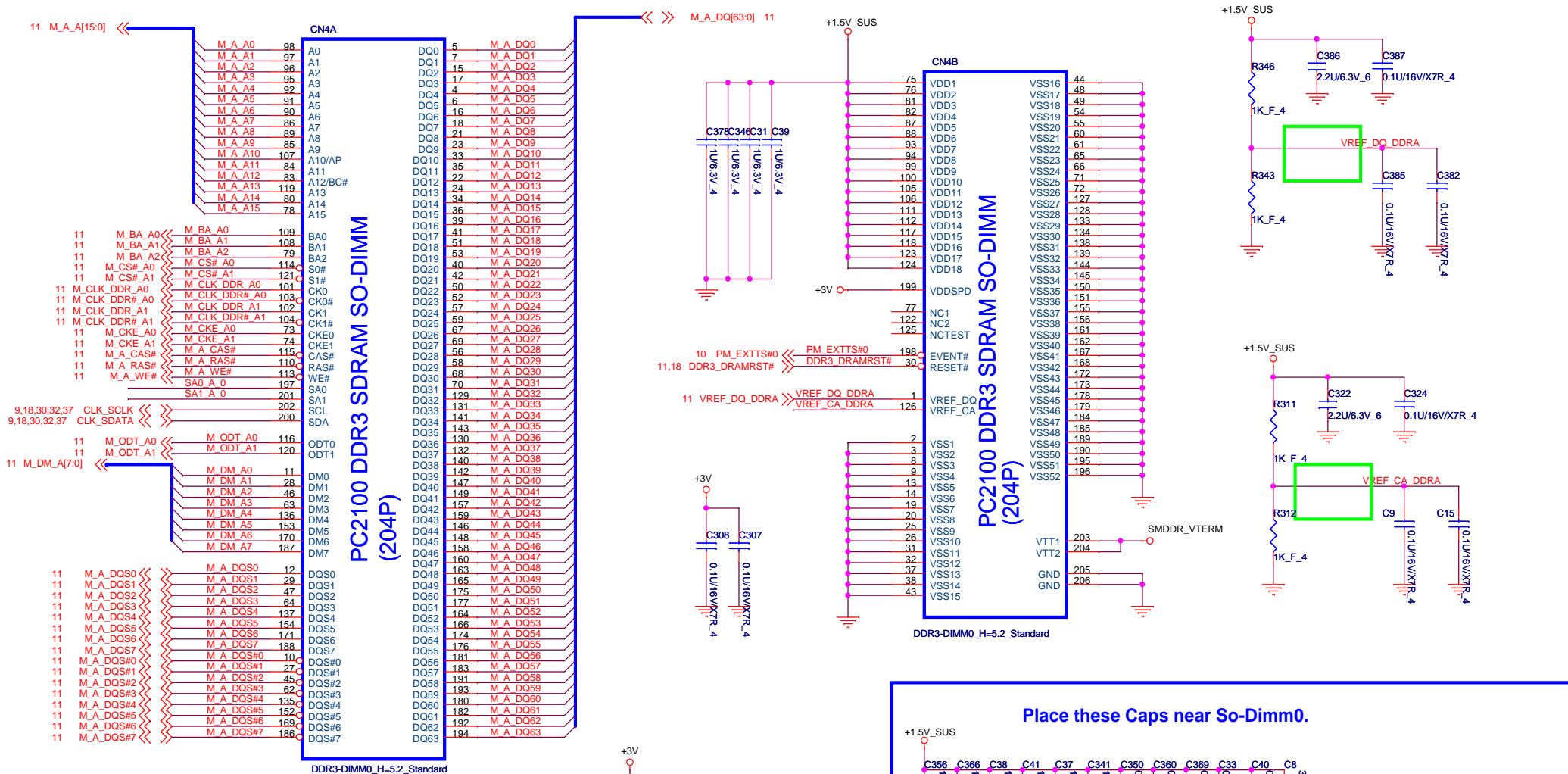


SOCKET CAVITY

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CN CPU SOCKET SMD LGA1156

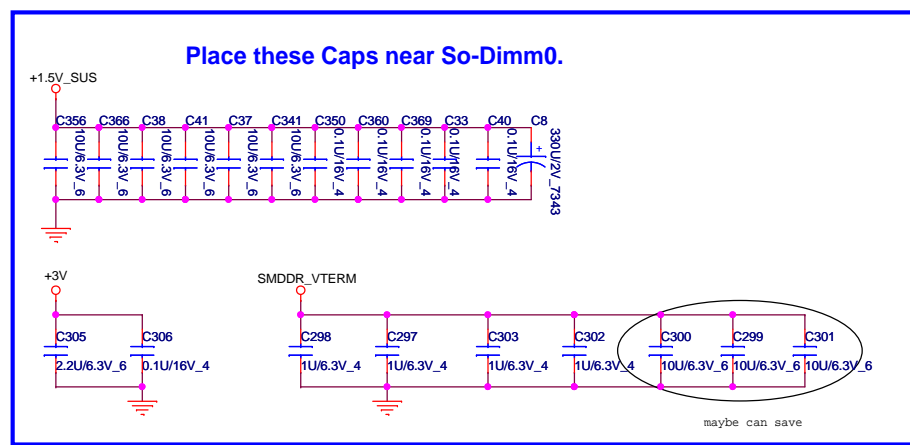
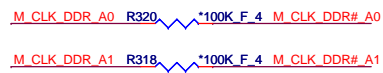




PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H-5.2_Standard

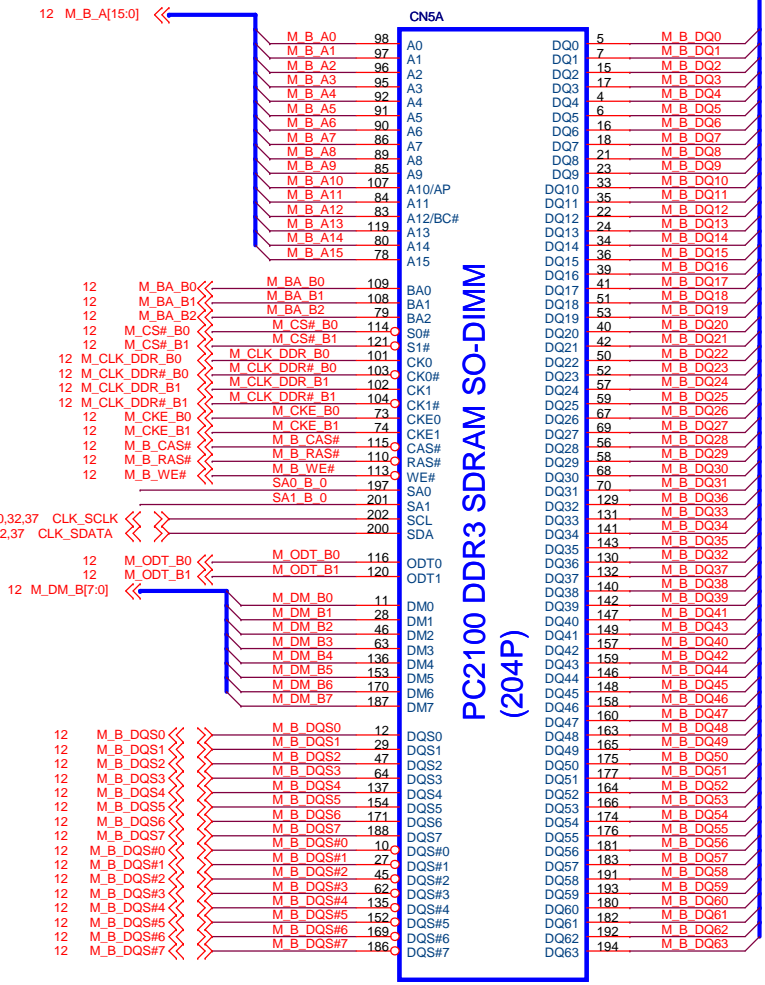
11 M_A_A[15:0]	M A A0	98	A0	DQ0	5	M A DQ0
	M A A1	97	A1	DQ1	7	M A DQ1
	M A A2	96	A2	DQ2	15	M A DQ2
	M A A3	95	A3	DQ3	17	M A DQ3
	M A A4	92	A4	DQ4	4	M A DQ4
	M A A5	91	A5	DQ5	6	M A DQ5
	M A A6	90	A6	DQ6	18	M A DQ6
	M A A7	89	A7	DQ7	21	M A DQ7
	M A A8	86	A8	DQ8	23	M A DQ8
	M A A9	85	A9	DQ9	33	M A DQ9
	M A A10	107	A10/AP	DQ10	35	M A DQ10
	M A A11	84	A11	DQ11	100	M A DQ11
	M A A12	83	A12/BC#	DQ12	22	M A DQ12
	M A A13	119	A13	DQ13	24	M A DQ13
	M A A14	80	A14	DQ14	34	M A DQ14
	M A A15	78	A15	DQ15	36	M A DQ15
				DQ16	39	M A DQ16
				DQ17	41	M A DQ17
				DQ18	51	M A DQ18
				DQ19	53	M A DQ19
				DQ20	40	M A DQ20
				DQ21	42	M A DQ21
				DQ22	50	M A DQ22
				DQ23	52	M A DQ23
				DQ24	57	M A DQ24
				DQ25	59	M A DQ25
				DQ26	67	M A DQ26
				DQ27	69	M A DQ27
				DQ28	58	M A DQ28
				DQ29	68	M A DQ29
				DQ30	70	M A DQ30
				DQ31	72	M A DQ31
				DQ32	129	M A DQ32
				DQ33	131	M A DQ33
				DQ34	141	M A DQ34
				DQ35	143	M A DQ35
				DQ36	130	M A DQ36
				DQ37	132	M A DQ37
				DQ38	140	M A DQ38
				DQ39	142	M A DQ39
				DQ40	147	M A DQ40
				DQ41	149	M A DQ41
				DQ42	157	M A DQ42
				DQ43	159	M A DQ43
				DQ44	146	M A DQ44
				DQ45	148	M A DQ45
				DQ46	158	M A DQ46
				DQ47	160	M A DQ47
				DQ48	163	M A DQ48
				DQ49	165	M A DQ49
				DQ50	175	M A DQ50
				DQ51	177	M A DQ51
				DQ52	164	M A DQ52
				DQ53	166	M A DQ53
				DQ54	174	M A DQ54
				DQ55	176	M A DQ55
				DQ56	181	M A DQ56
				DQ57	183	M A DQ57
				DQ58	191	M A DQ58
				DQ59	193	M A DQ59
				DQ60	180	M A DQ60
				DQ61	182	M A DQ61
				DQ62	192	M A DQ62
				DQ63	194	M A DQ63



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	DDR3 CHA DIMM 0	A
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CHANNEL B DIMM 2

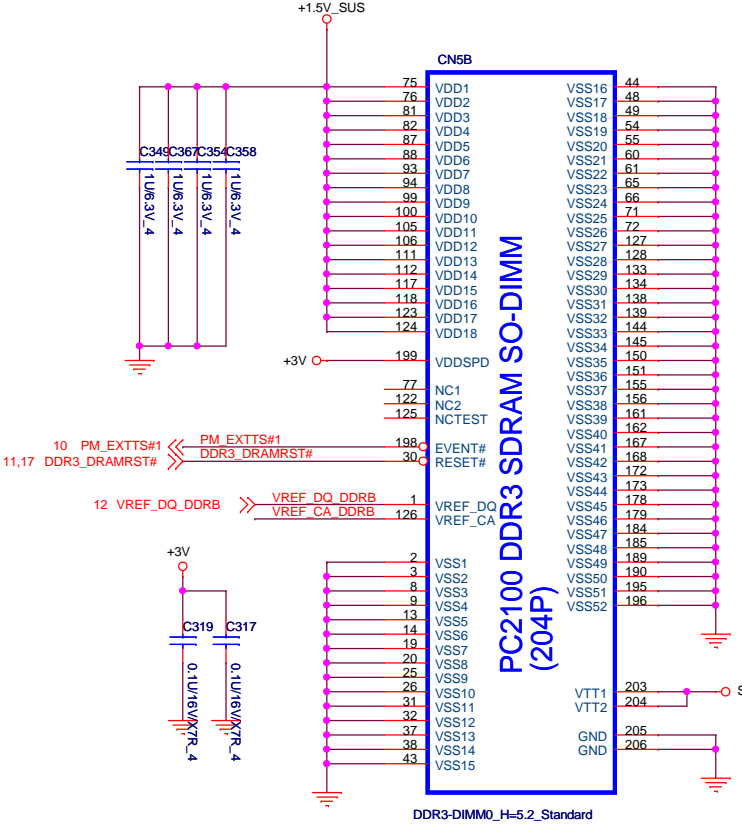
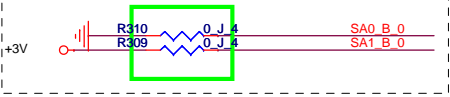


DDR3-DIMM0_H=5.2_Standard

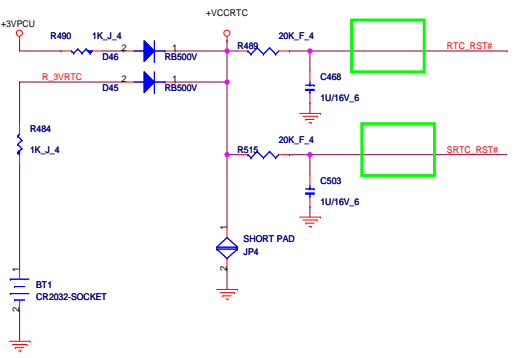
M_B_DQ32----JDIM4.130----JDIM3.130
M_B_DQ36----JDIM4.129----JDIM3.129

M_B_DQ41----JDIM4.147----JDIM3.147
M_B_DQ43----JDIM4.149----JDIM3.149
M_B_DQ42----JDIM4.159----JDIM3.159
M_B_DQ40----JDIM4.157----JDIM3.157

SPD SA0	0
SPD SA1	1



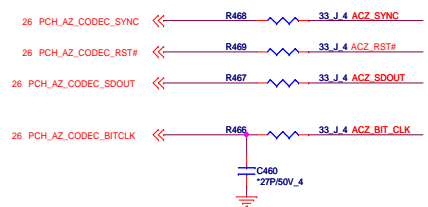
RTC Circuitry



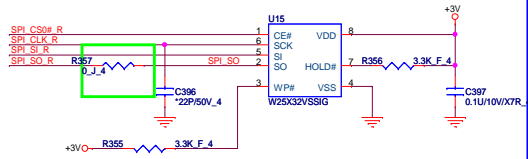
Intruder Detect: This signal can be set to disable system if box detected open.

HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V

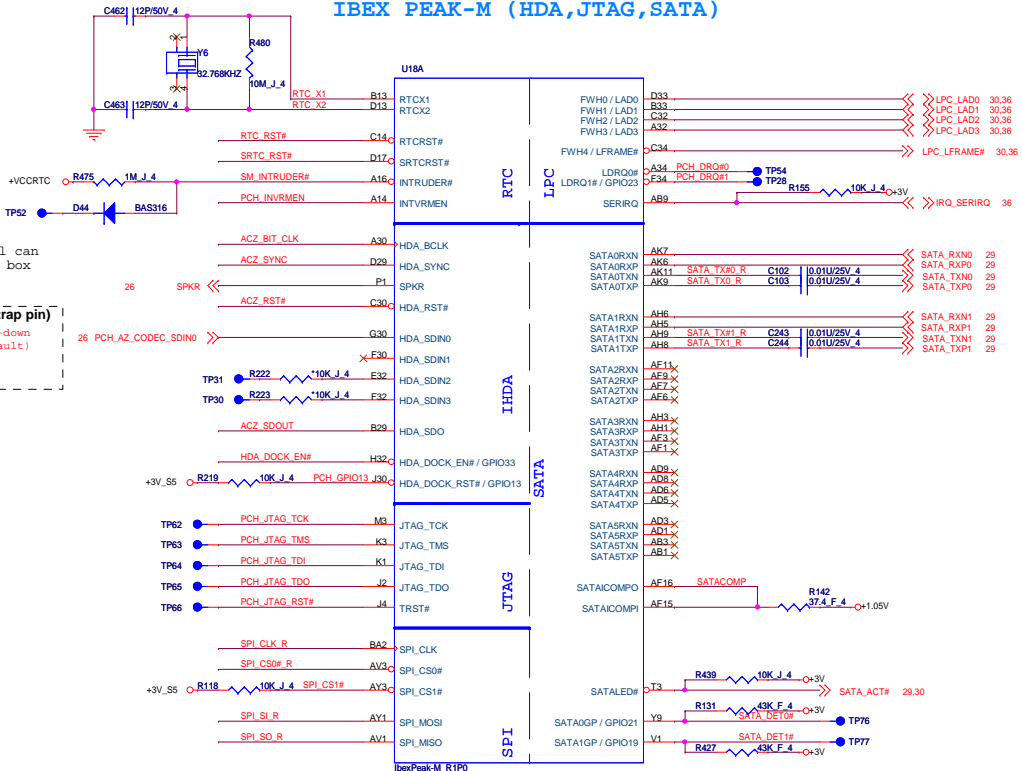
HDA Bus



PCH SPI

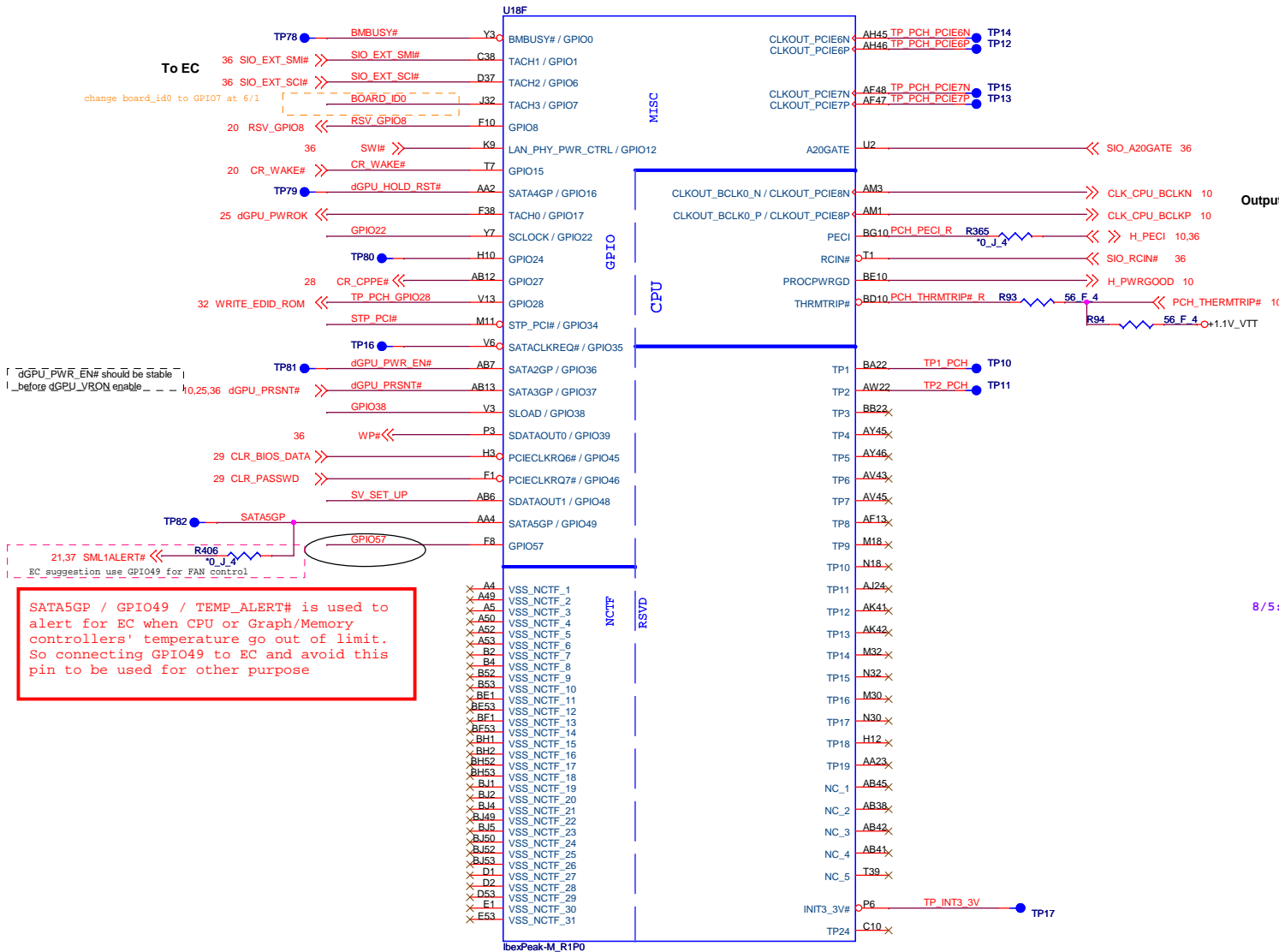


IBEX PEAK-M (HDA, JTAG, SATA)

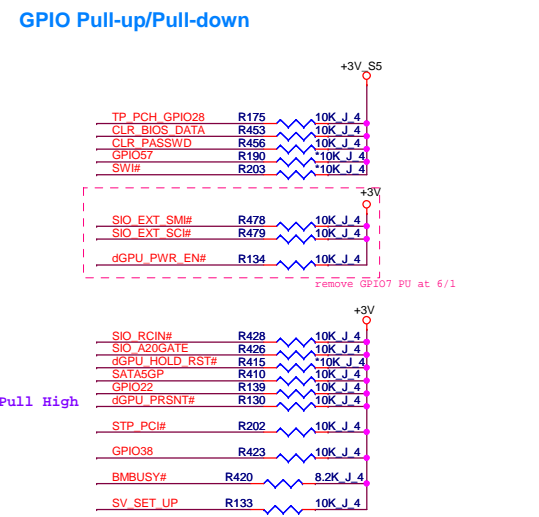
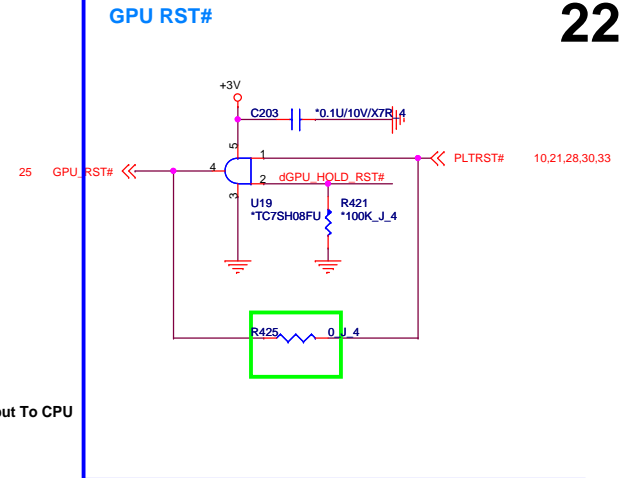


PCH Strap Table

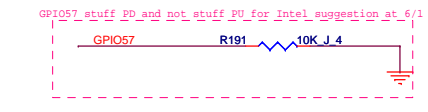
Pin Name	Strap description	Sampled	Configuration	ZN2 note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V - R458 - *10K J.4 - SPKR												
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R461 - *10K J.4 - PCL_GNT3# 21												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC - R477 - 330K J.4 - PCH_INVRMEN												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		R195 - *1K J.4 - PCL_GNT0# 21 R196 - *1K J.4 - PCL_GNT1# 21												
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V - R378 - *1K J.4 - NV_ALE - NV_ALE 21												
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V - R110 - *1K J.4 - NV_CLE - NV_CLE 21												
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	R220 - *1K J.4 - HDA_DOCK_EN# +3V - R221 - *10K J.4 - HDA_DOCK_EN#												
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V - R378 - *1K J.4 - SPI_SI_R												
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	-3V_S5 - R187 - *10K J.4 - RSV_GPIO8 22												
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 - R148 - *1K J.4 - CR_WAKE# 22												



SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

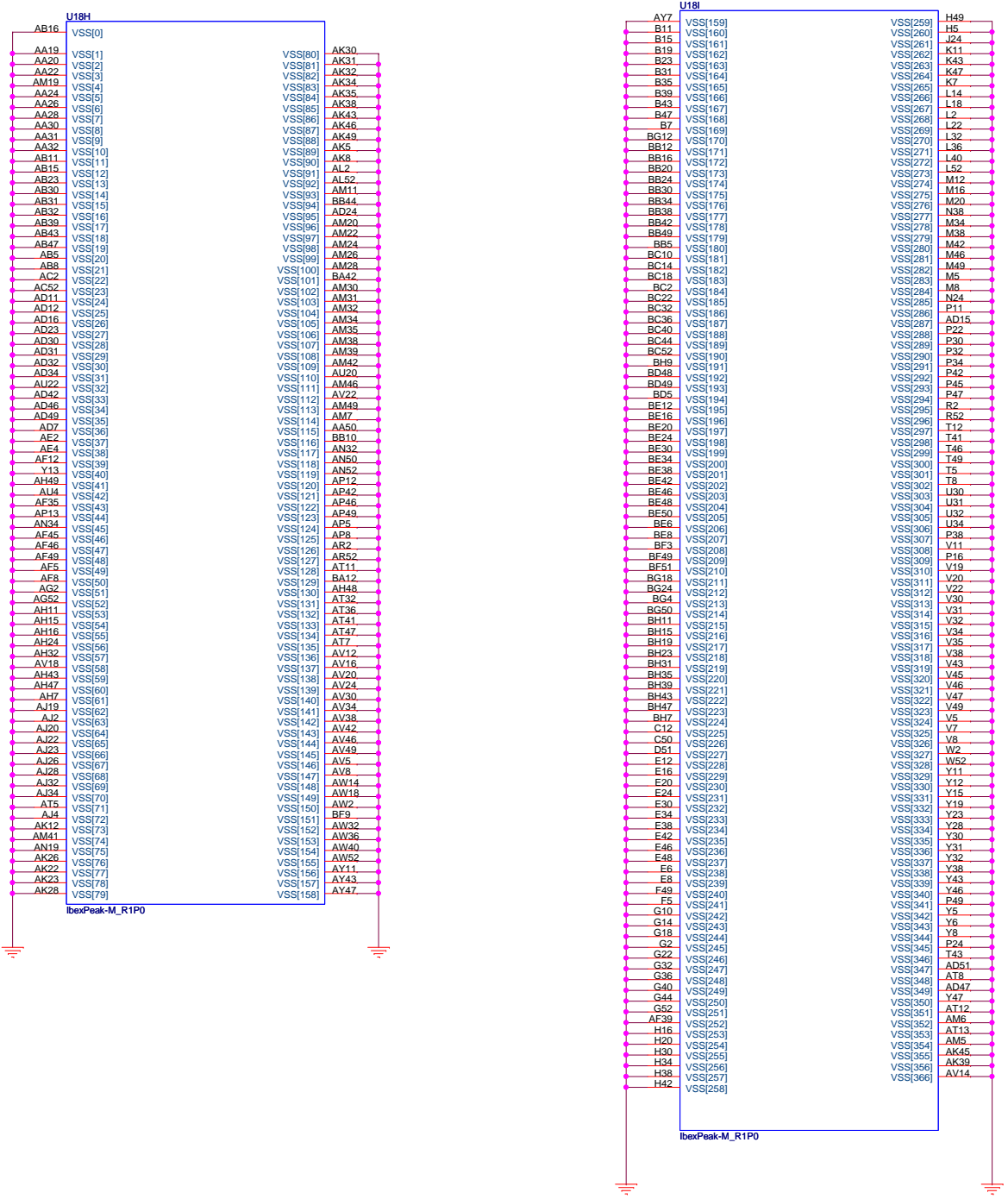


SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

IBEX PEAK-M (GND)

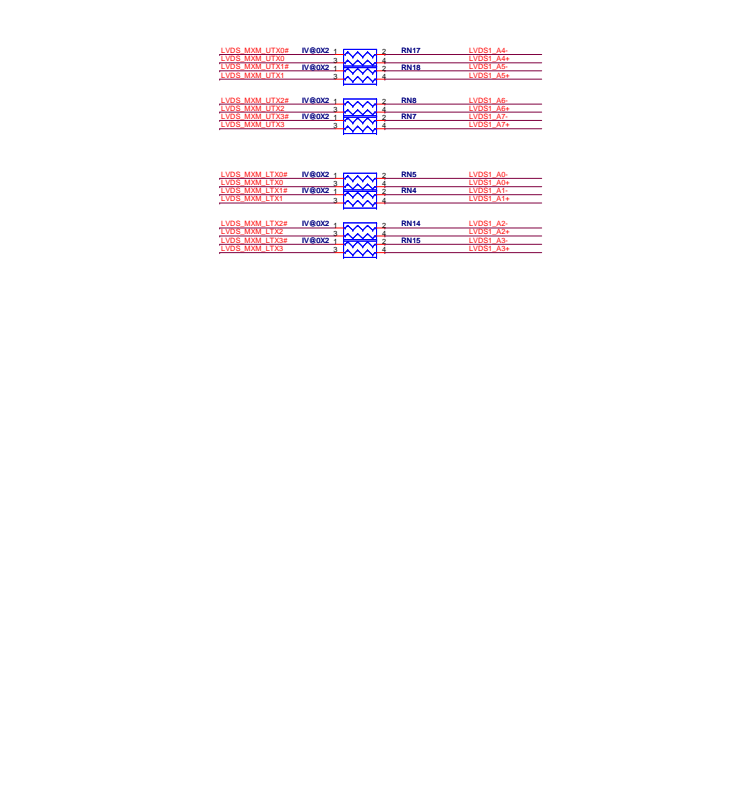
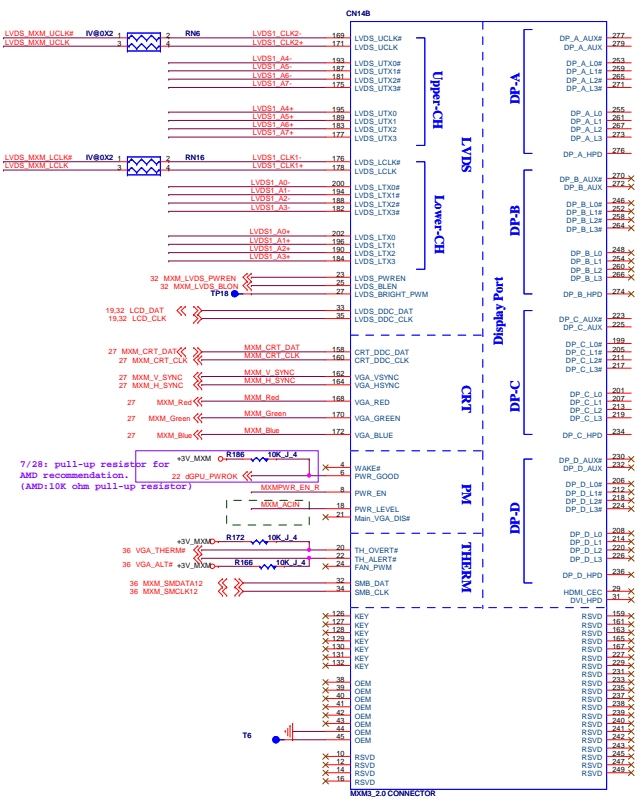
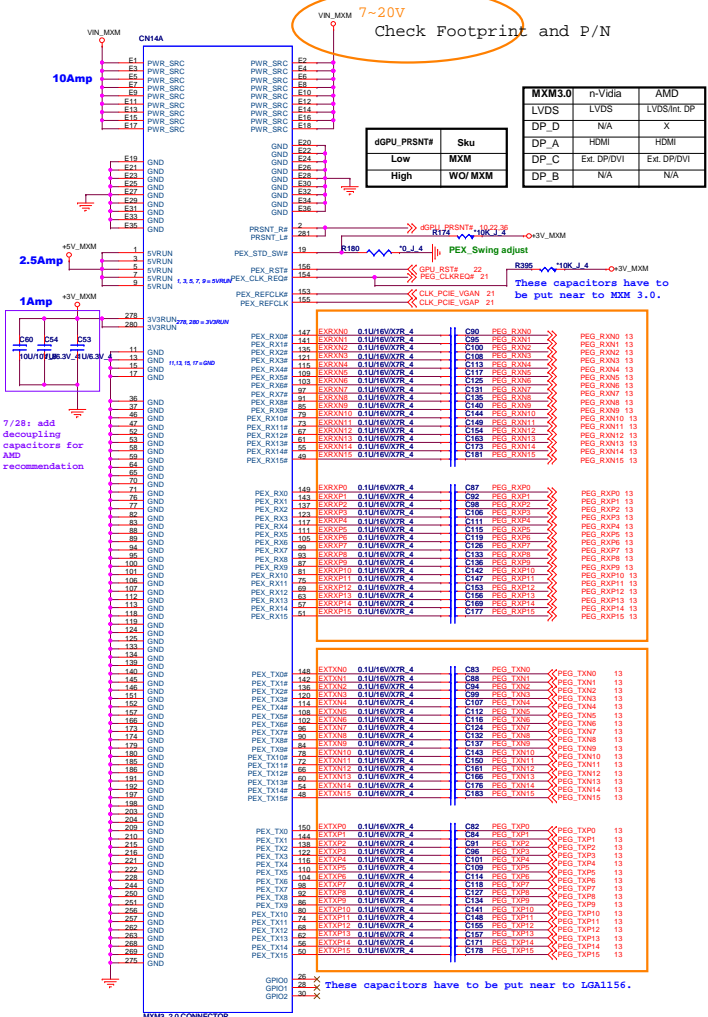


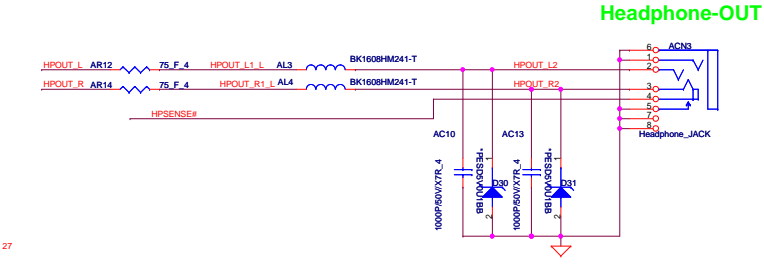
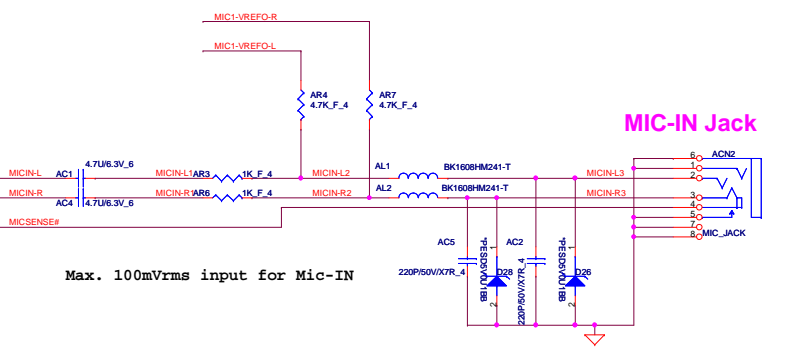
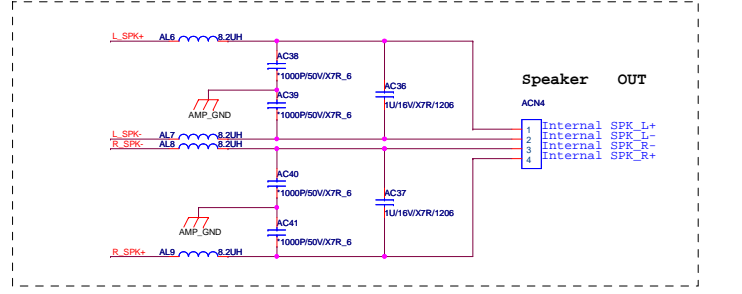
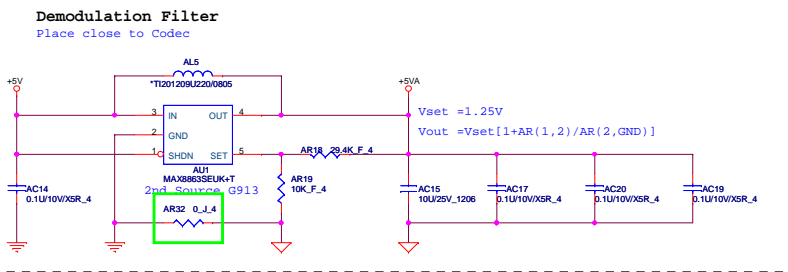
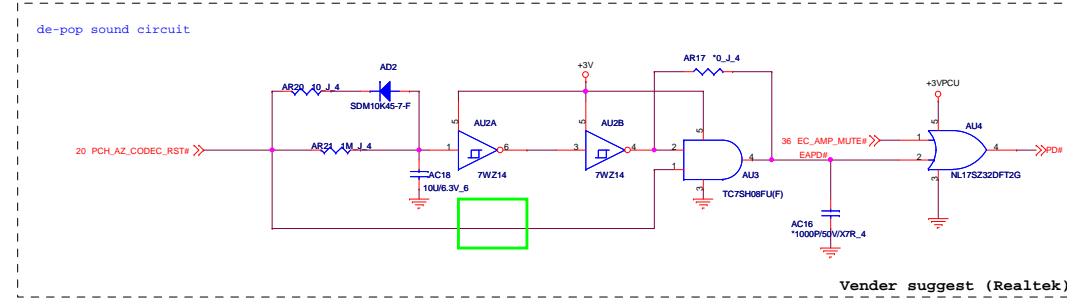
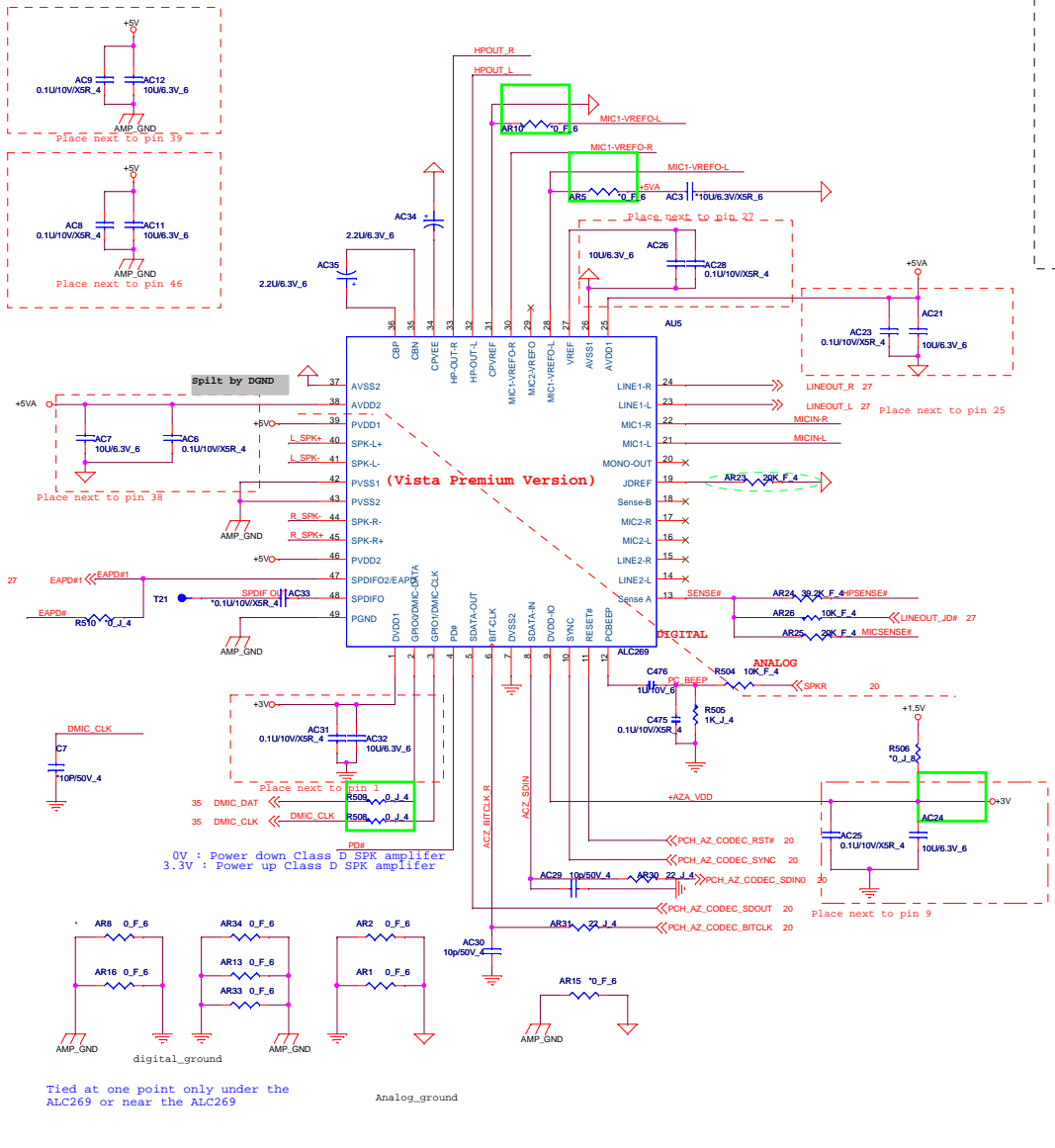
Quanta Computer Inc.
PROJECT : ZN2

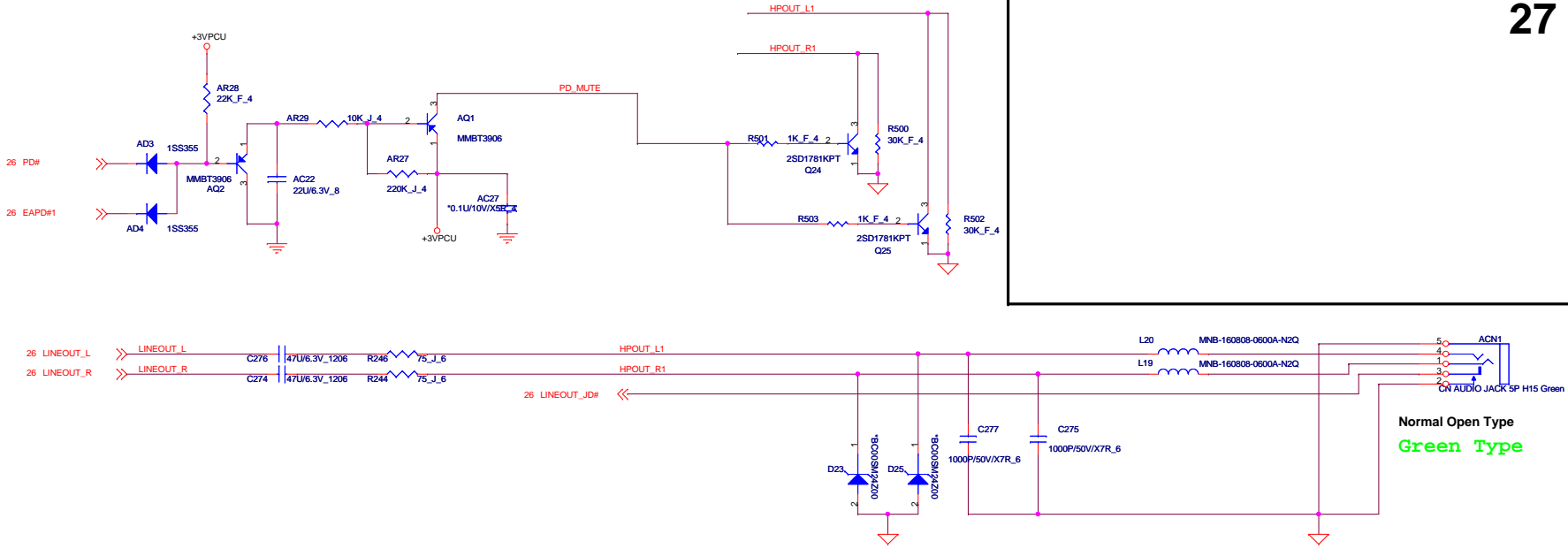
Size	Document Number	Rev
	PCH (GND)	A
Date:	Tuesday, March 16, 2010	Sheet 24 of 49

025 Change CN22 pin define and footprint at C test.

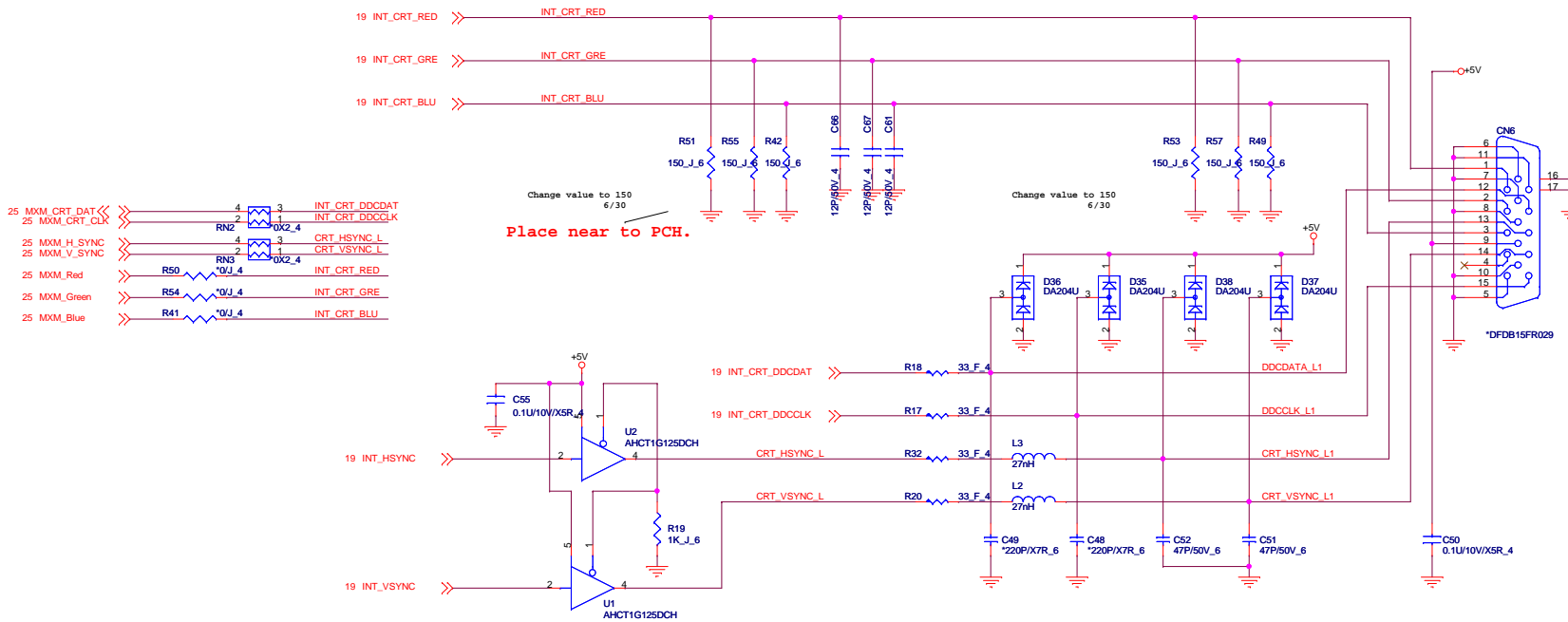
At 1121 update MXM footprint to mm-mm70-314-310B1-1-2709





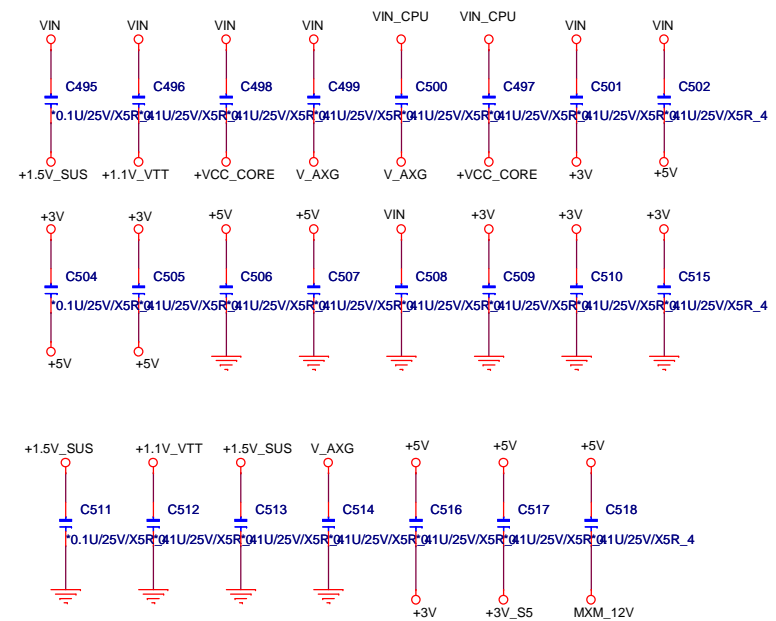
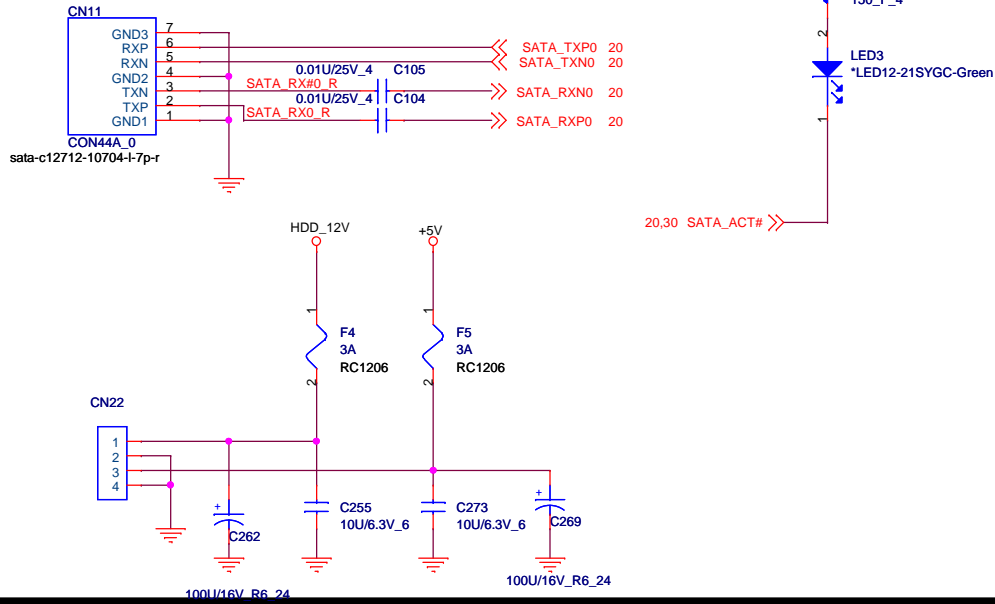


Reserve to CRT



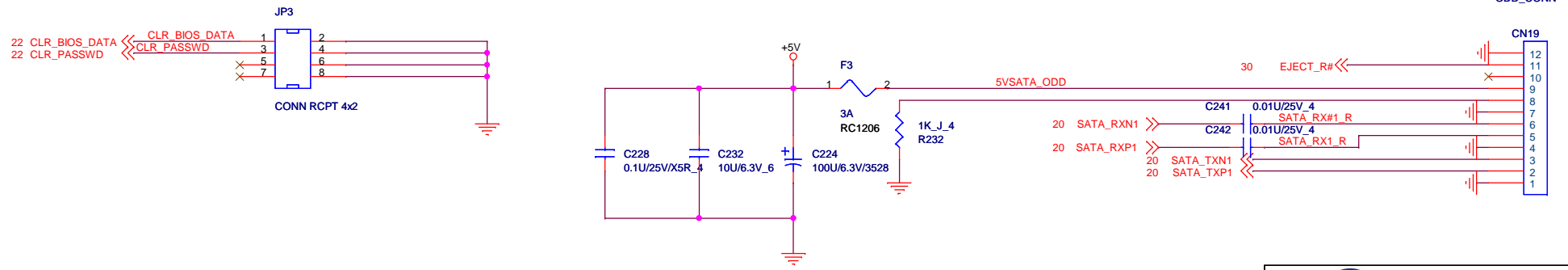
SATA HDD(3.5")

SATA HDD CONNECT



FOR EMI DEMAND

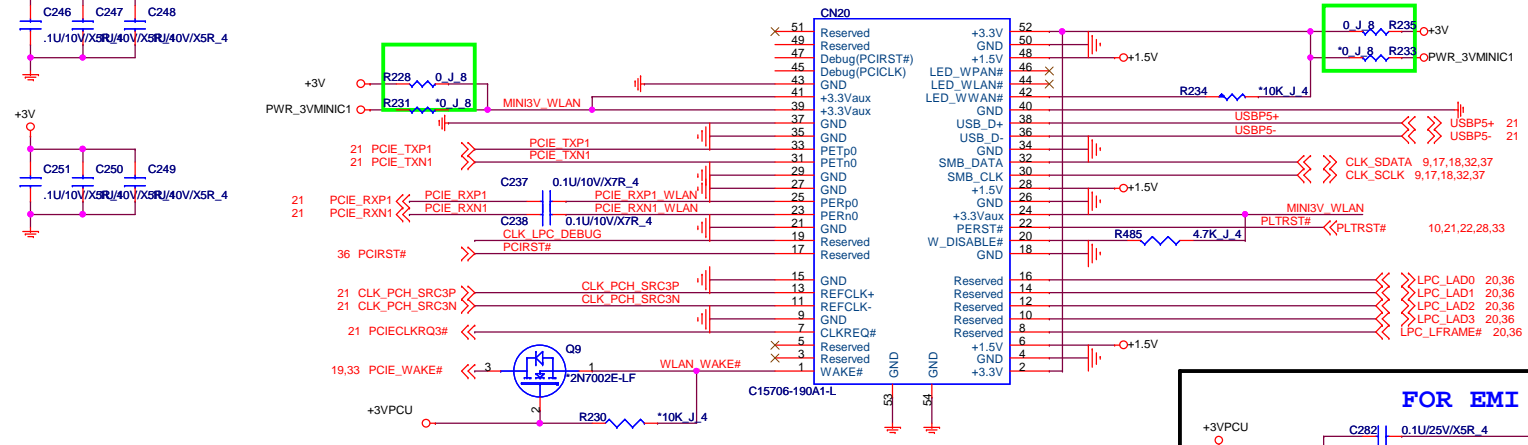
SATA ODD CONNECTOR



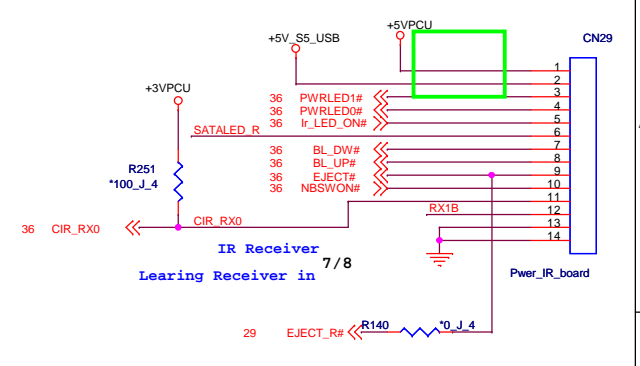
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	SATA HDD/ODD	1A
Date:	Tuesday, March 16, 2010	Sheet 29 of 49

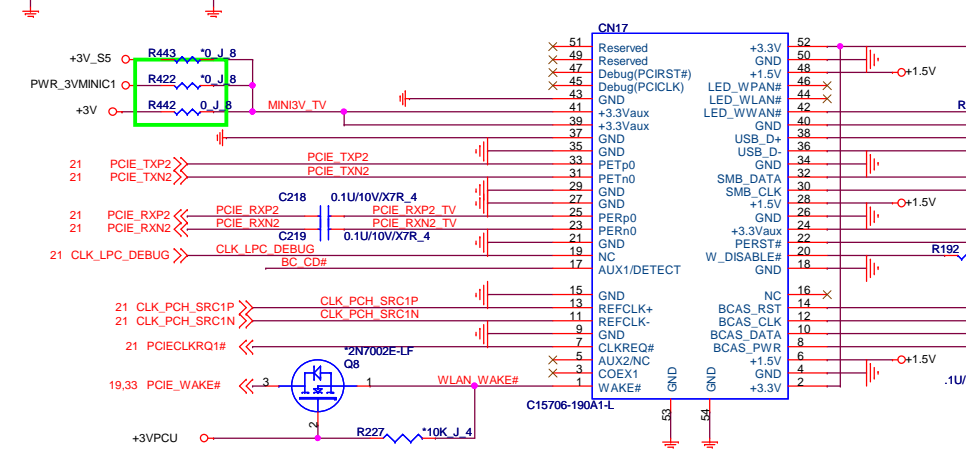
For wireless Lan card/Bluetooth



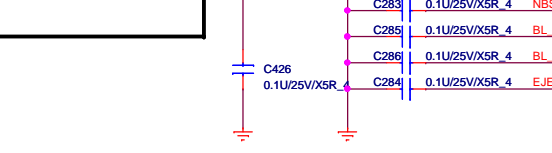
TO POWER BUTTON & LED LIGHT & IR



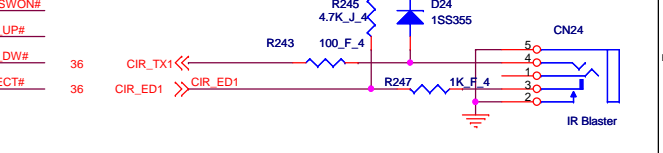
For TV MODULE CARD



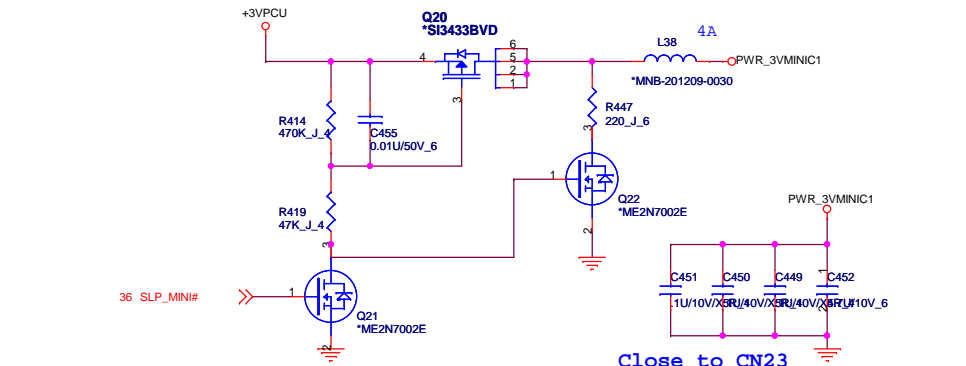
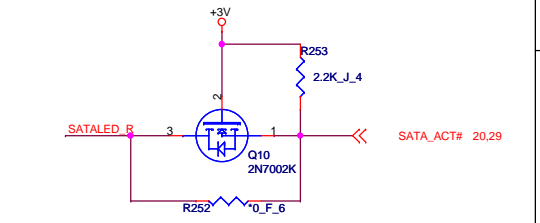
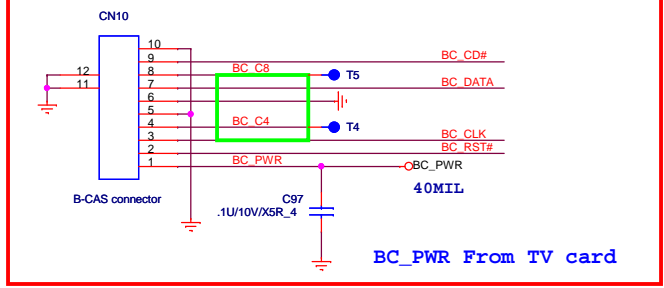
FOR EMI

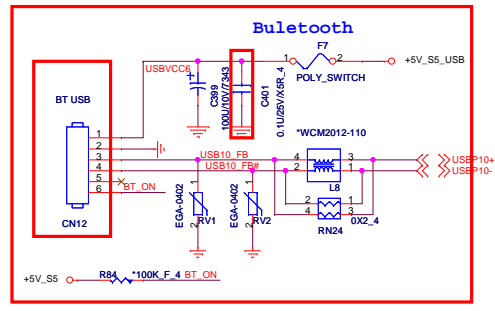
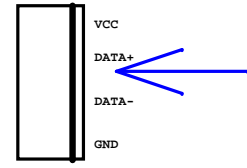
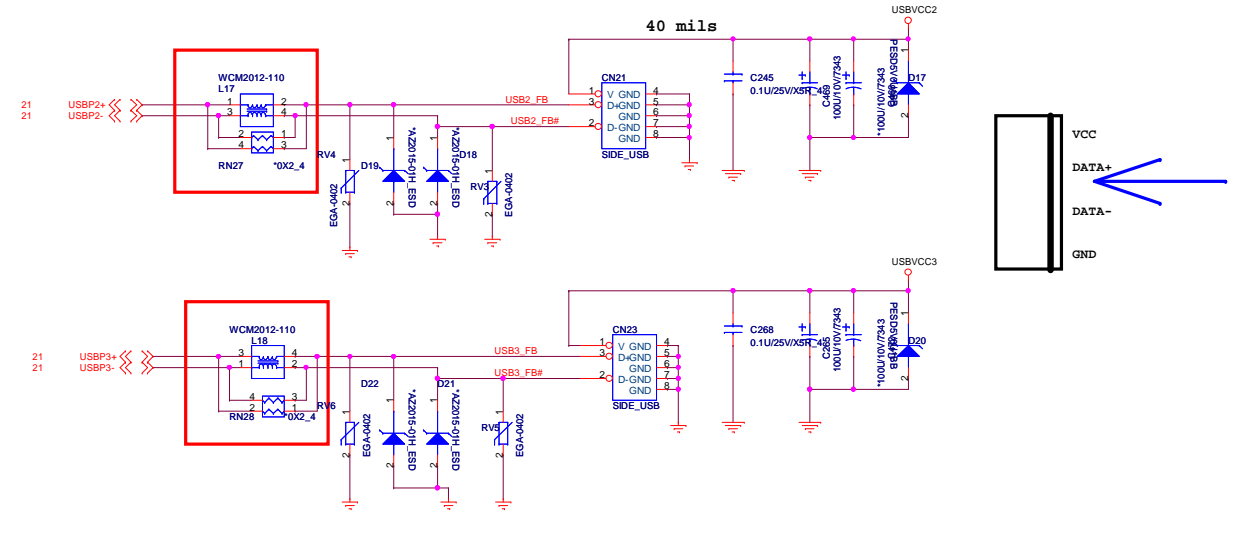
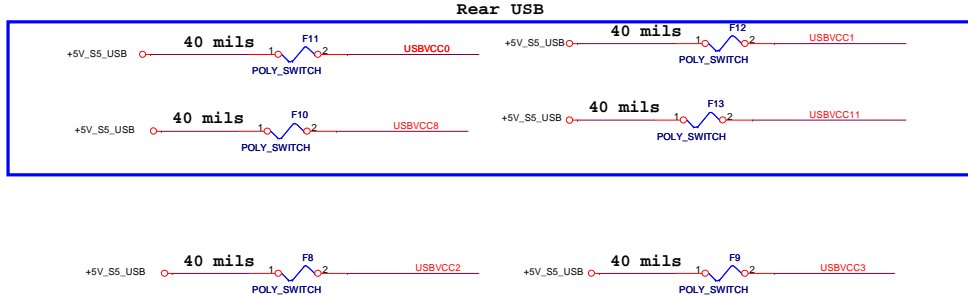
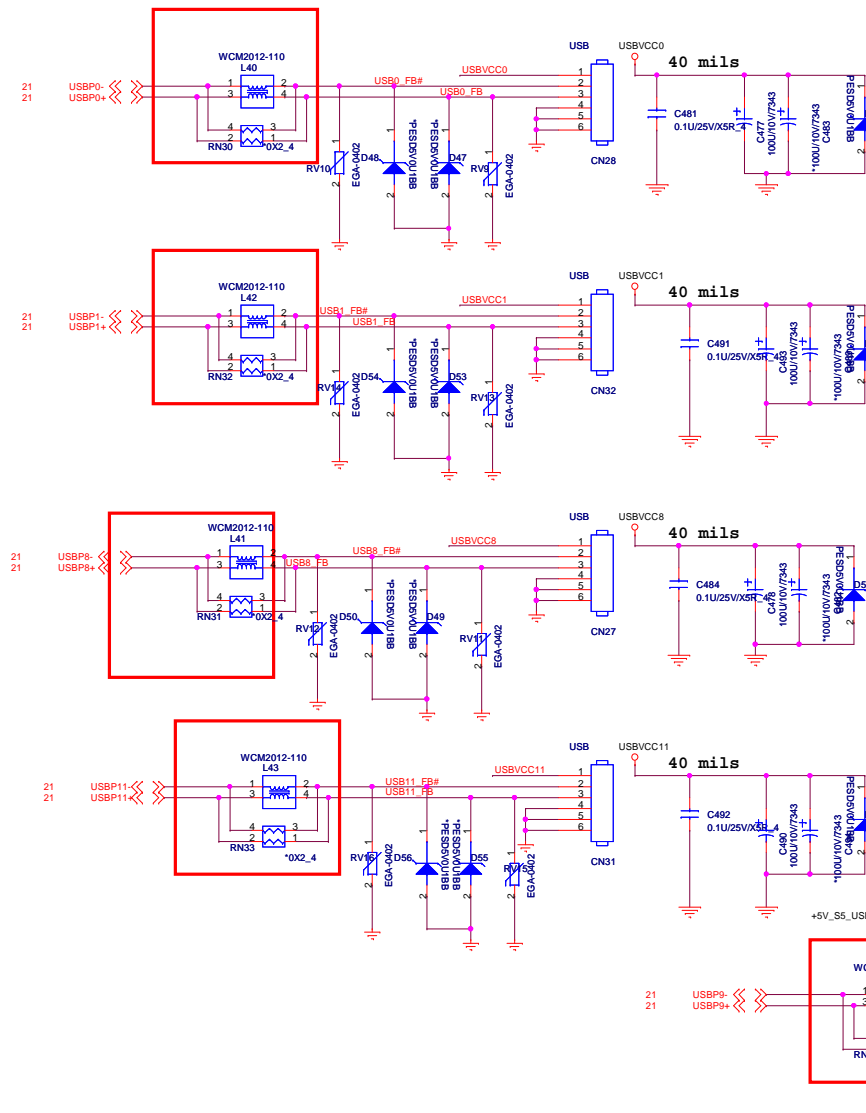


IR Blaster



B-CAS CONN

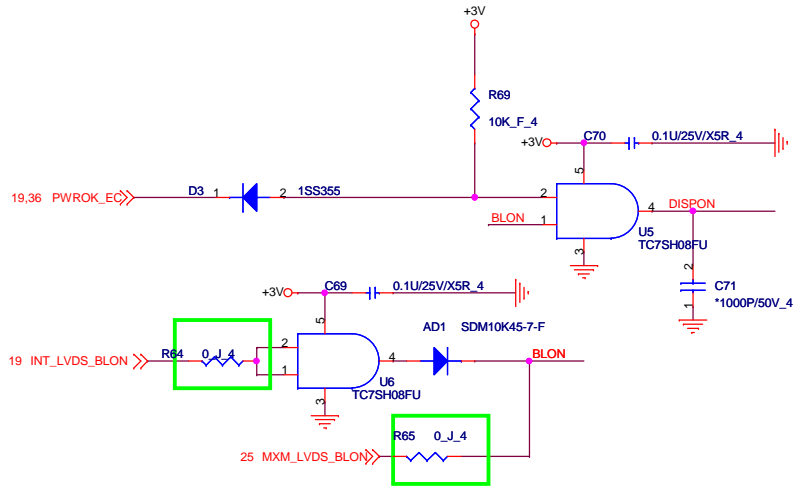




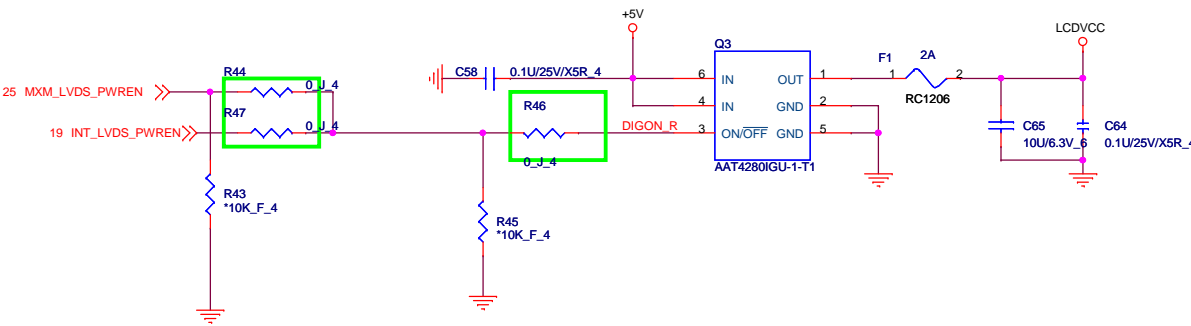
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	ON BOARD USB	A
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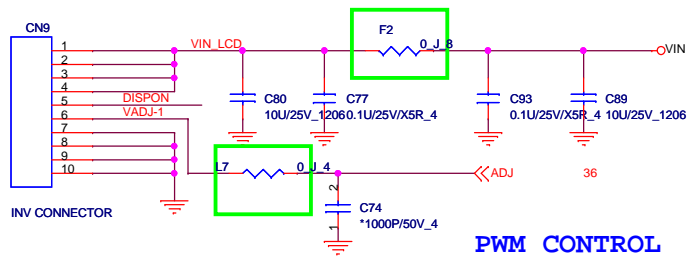
BACKLIGHT CONTROL



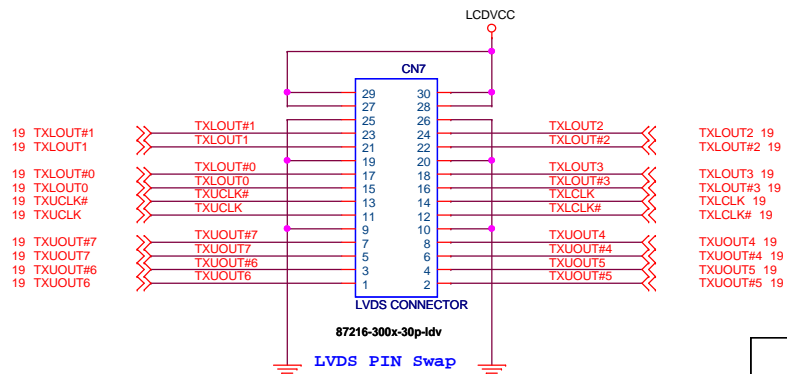
PANEL VCC CONTROL



TO INVERTER CONNECT



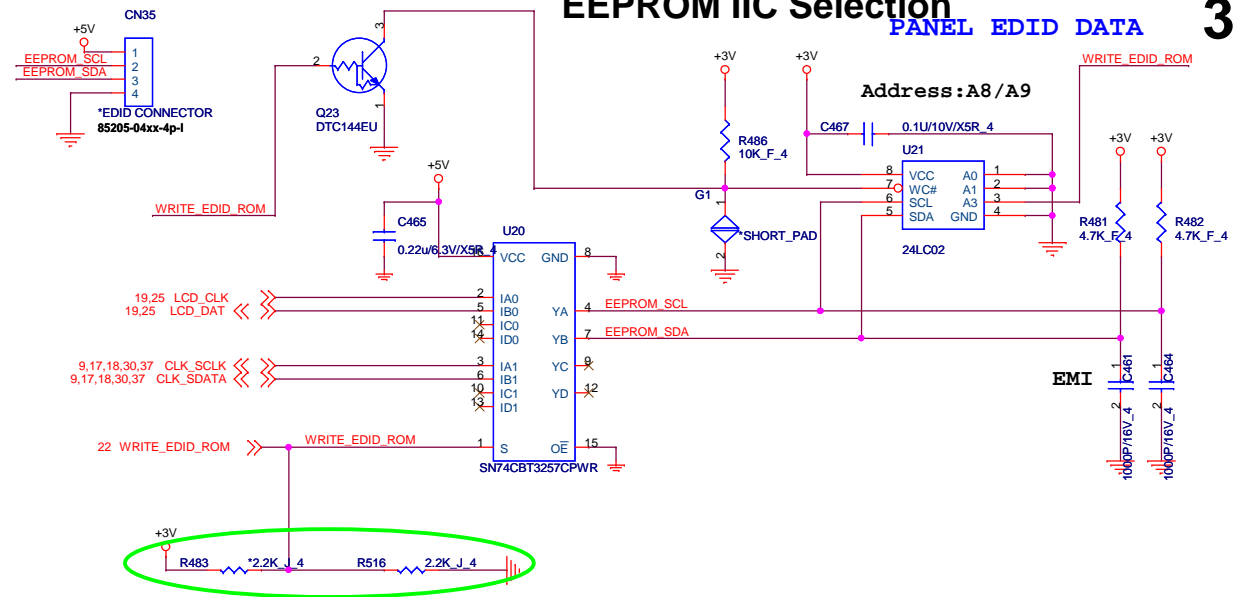
LCD PANEL CONNECTOR



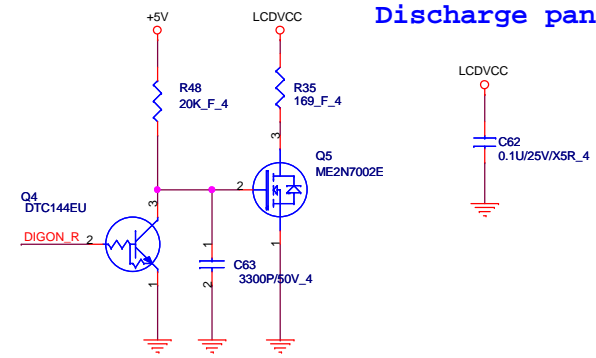
EEPROM IIC Selection

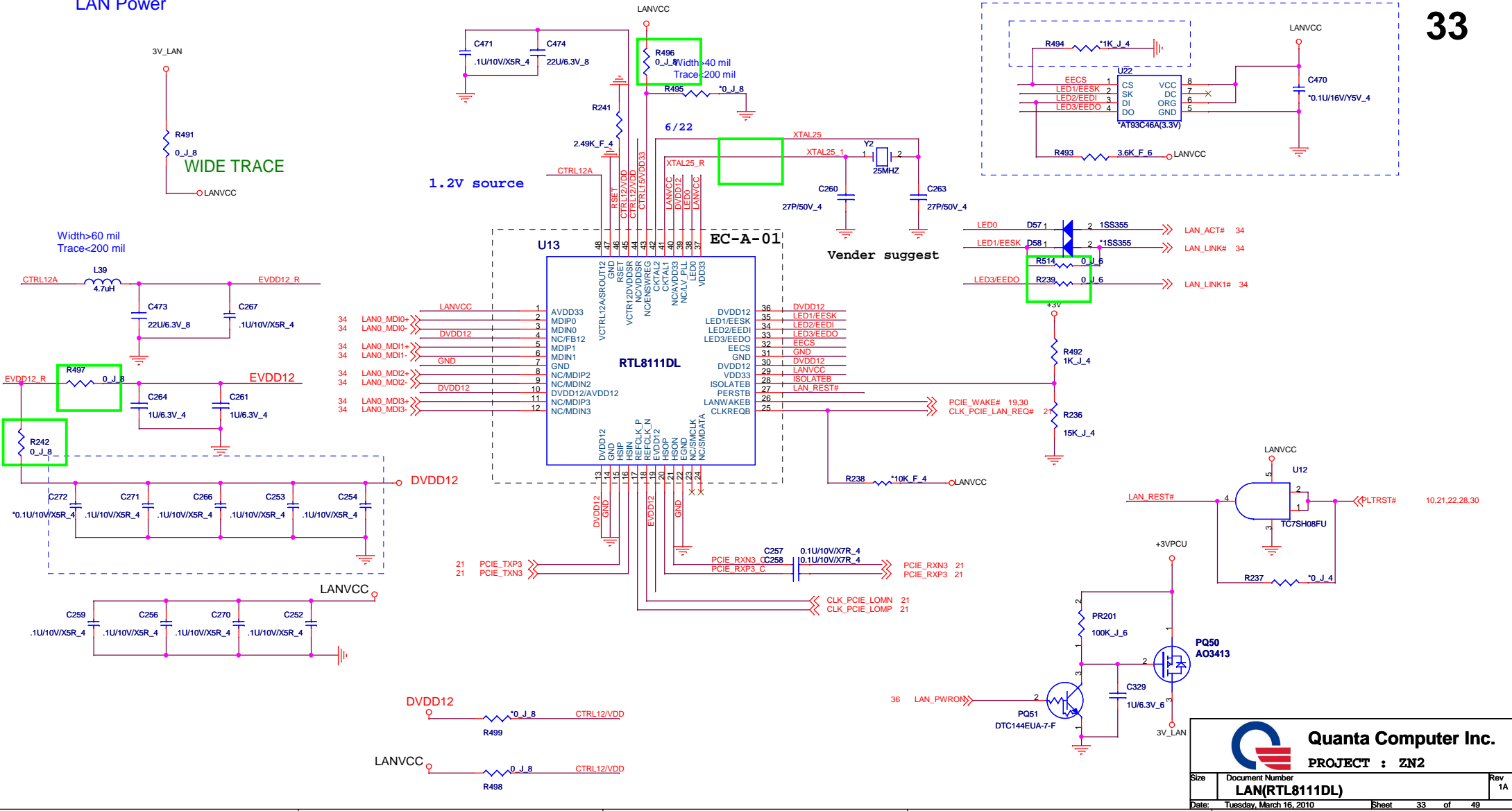
PANEL EDID DATA

32



Discharge panel power

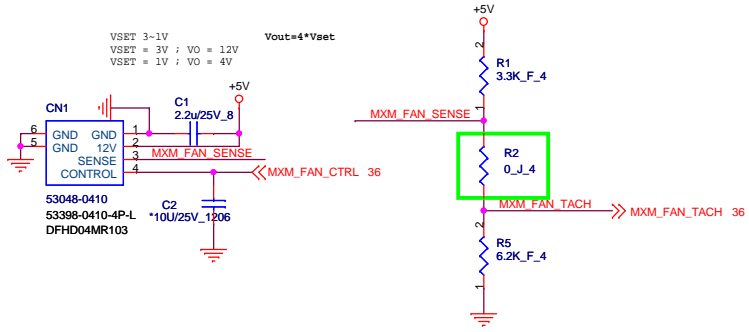




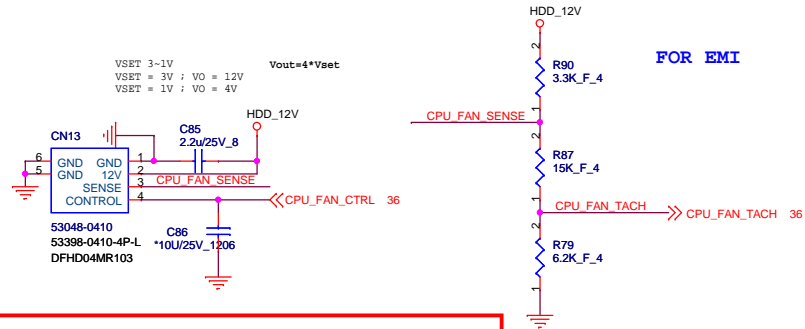
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	LAN(RTL8111DL)	1A
Date:	Tuesday, March 16, 2010	Sheet 33 of 49

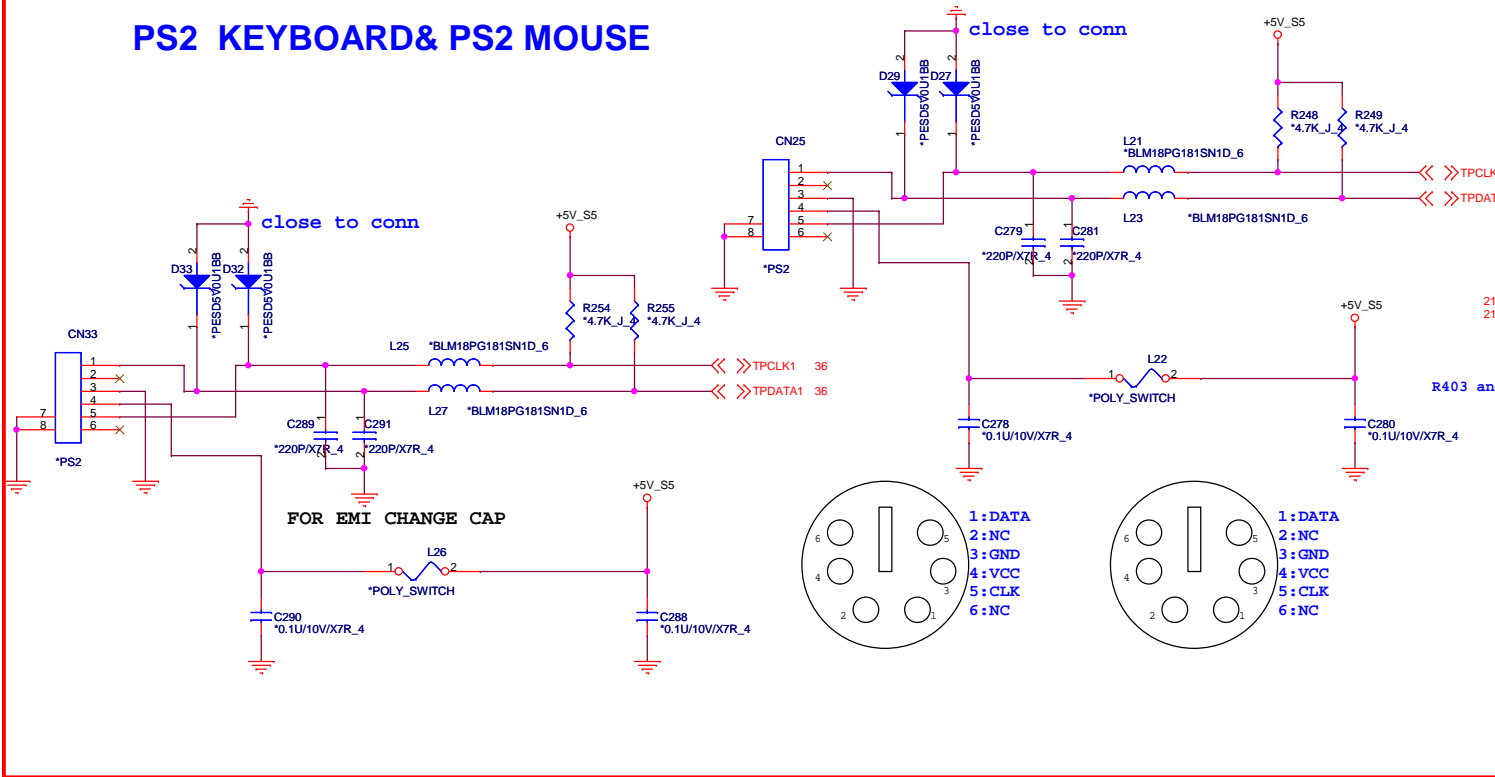
2nd FAN CONN



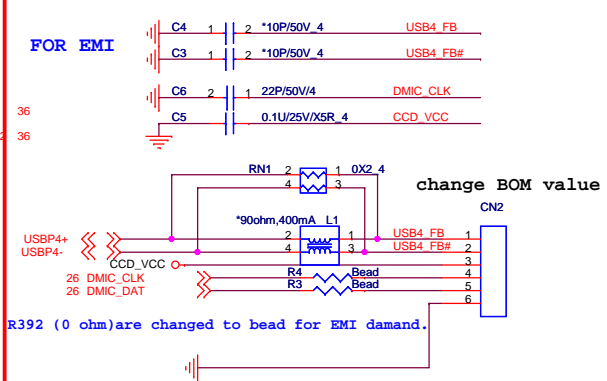
SYSTEM FAN CONN



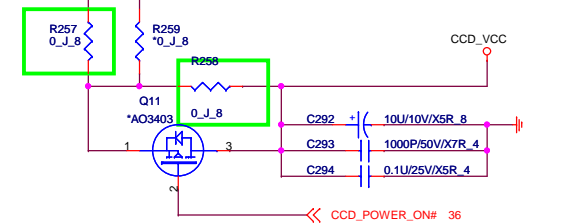
PS2 KEYBOARD & PS2 MOUSE



TO WEB CAM MODULE



CAMERA POWER CONTROL



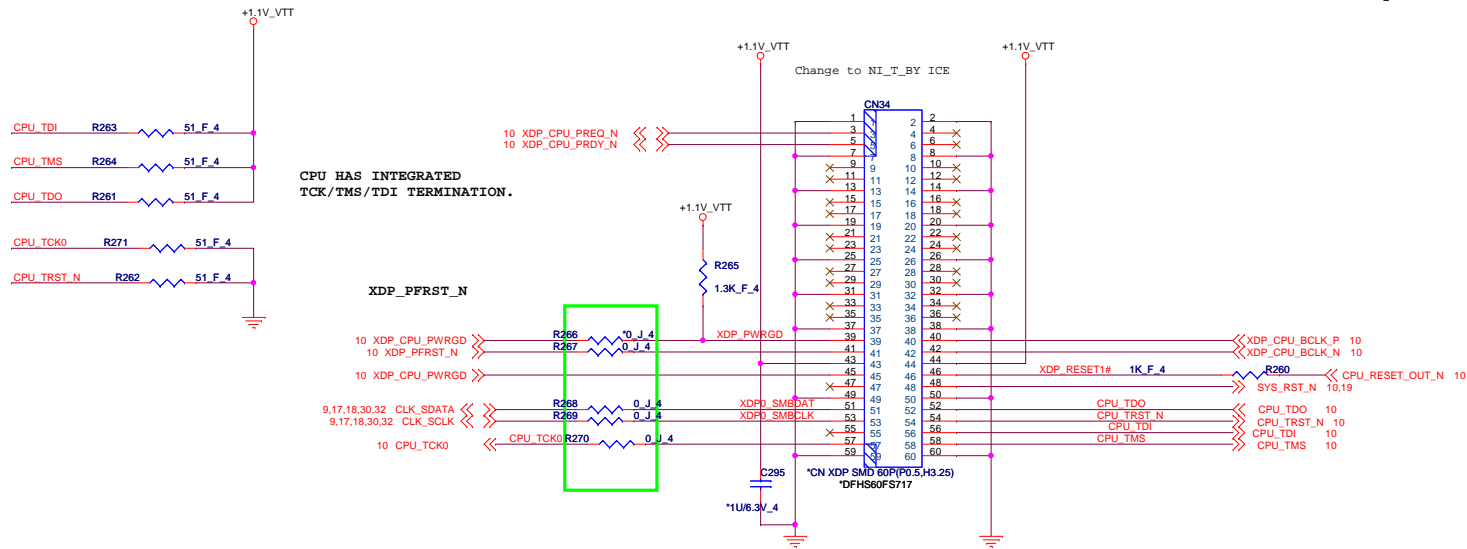
Quanta Computer Inc.
PROJECT : ZN2

Size	Document Number	Rev
	FAN/Webcam/PS2	A
Date:	Tuesday, March 16, 2010	Sheet 35 of 49

CPU XDP Connector

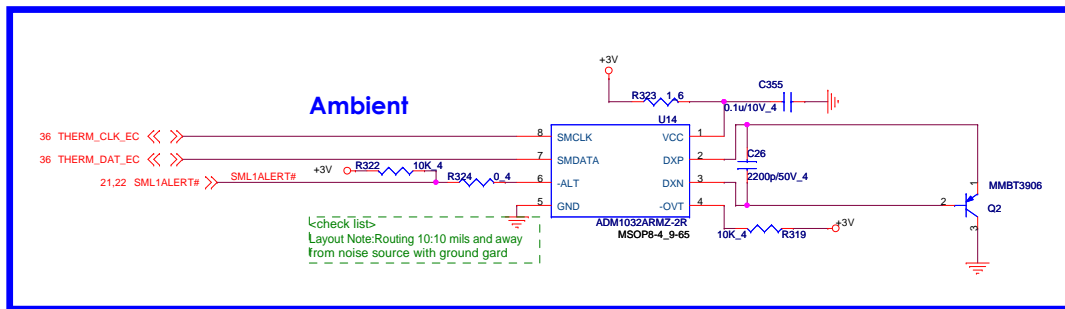
XDP0 - CPU

bsh-060-01-1-d-60p-1dv
bsh-060-01-1-d-60p-1dv

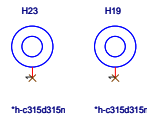


CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

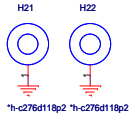
PCH XDP Connector



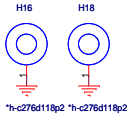
Coaxil conn



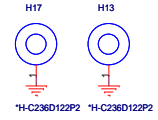
WLAN



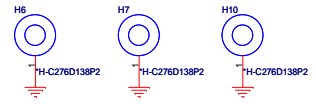
TV



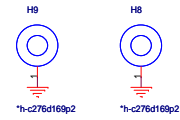
MXM



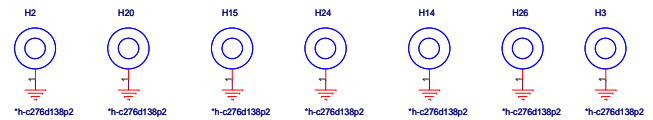
CPU frame



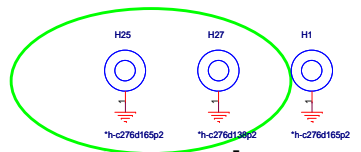
CPU fan



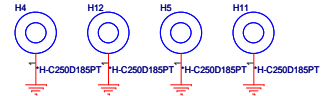
Board screw holes



GND SHAPE for EMI in DDR3

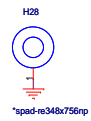


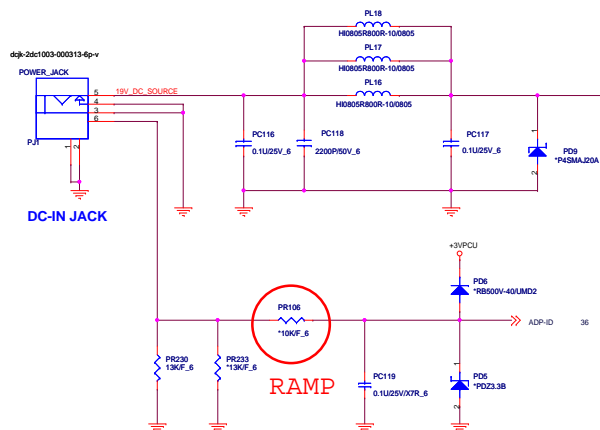
CPU socket



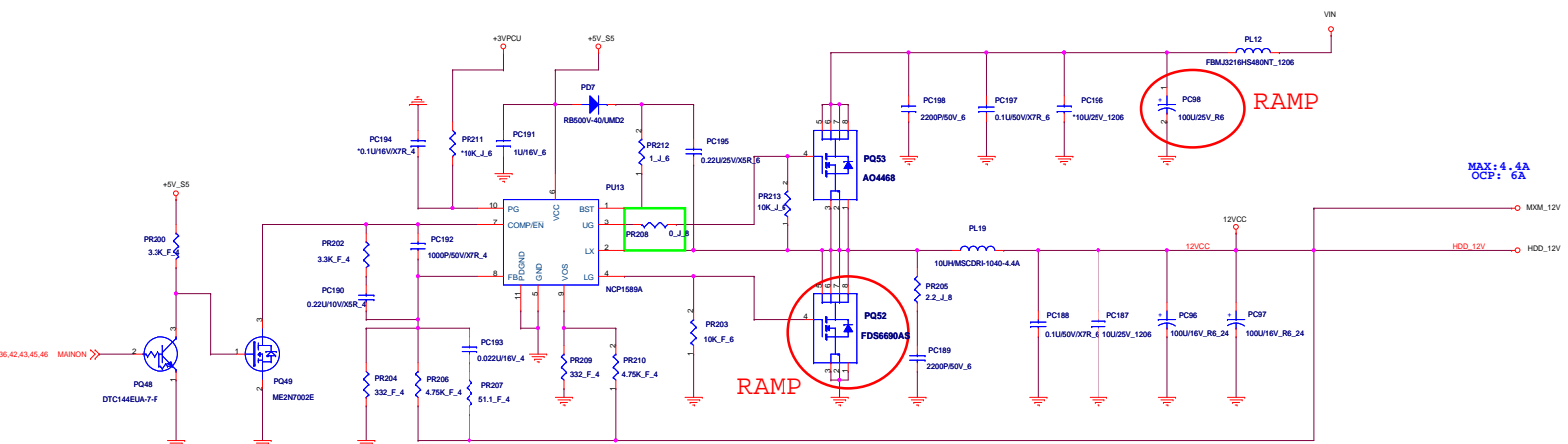
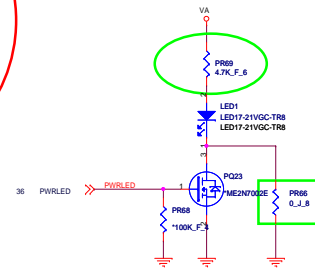
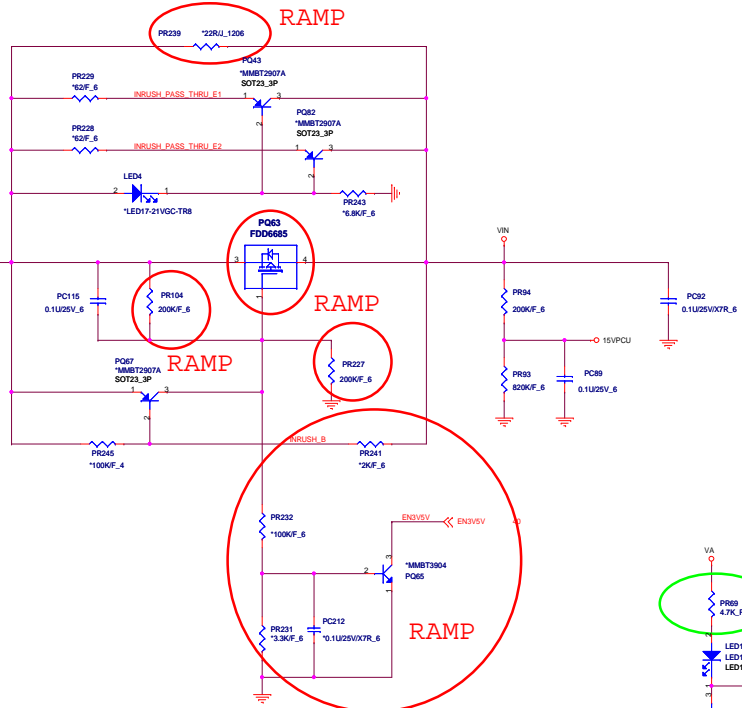
Need discuss with ME/EMI

Delete



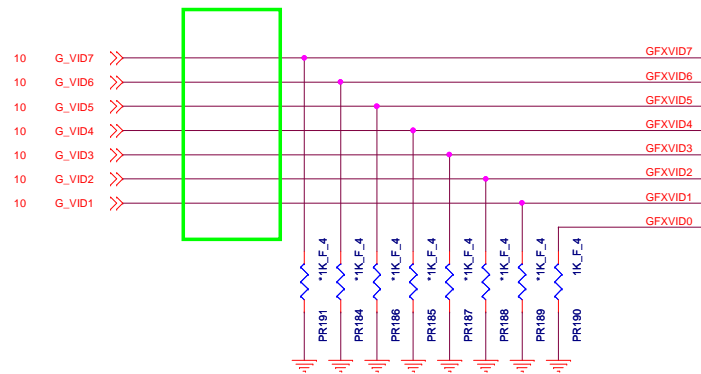
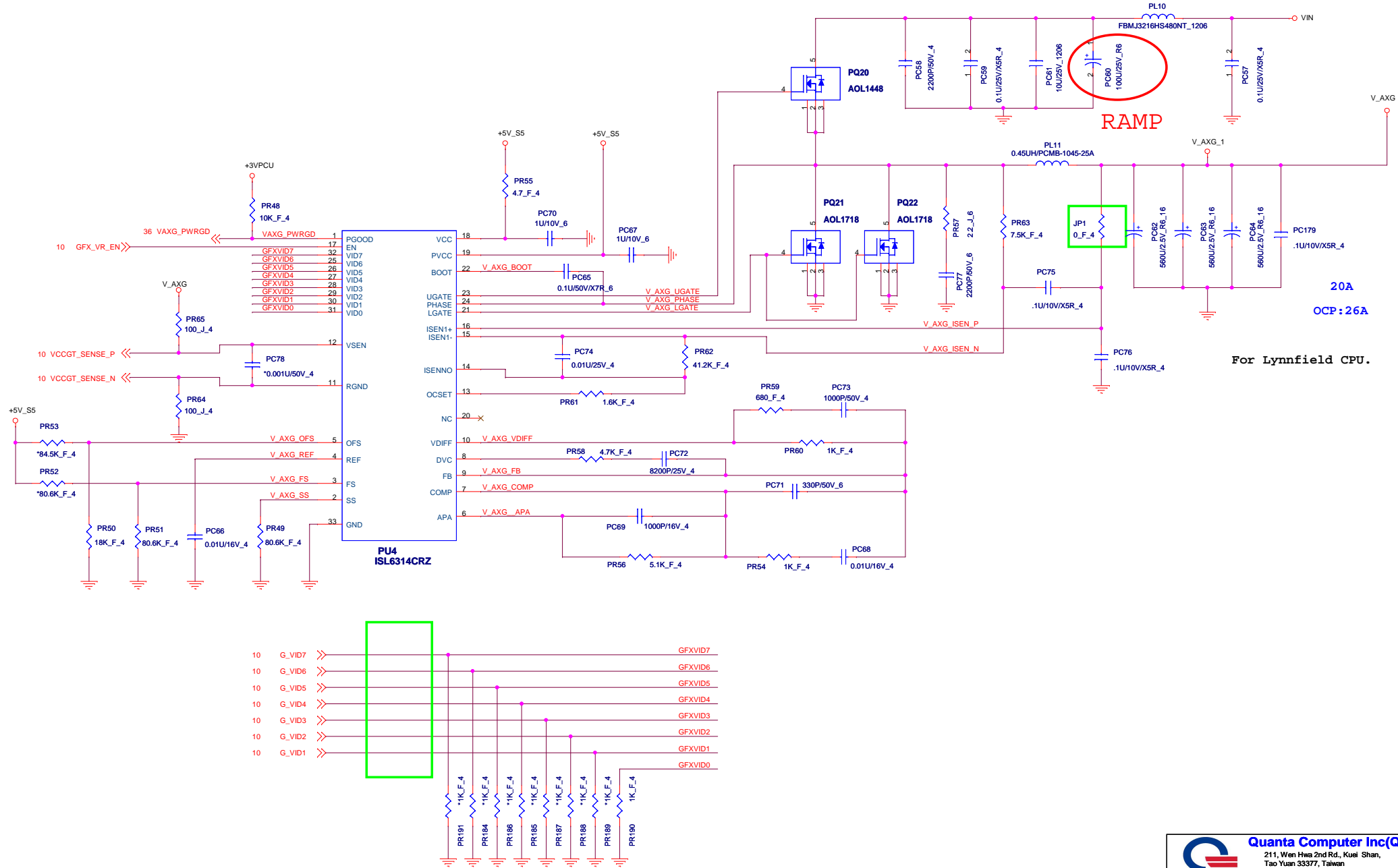


Adapter Support (Adapter ID)
 Rid with no MXM stuffing: 64.9K Recommend use 150W adapter.
 Rid with MXM stuff: 49.9K Recommend use 180W adapter.



$$I_{octh} = (I_{ocset} * R_{ocset}) / R_{ds(on)}$$

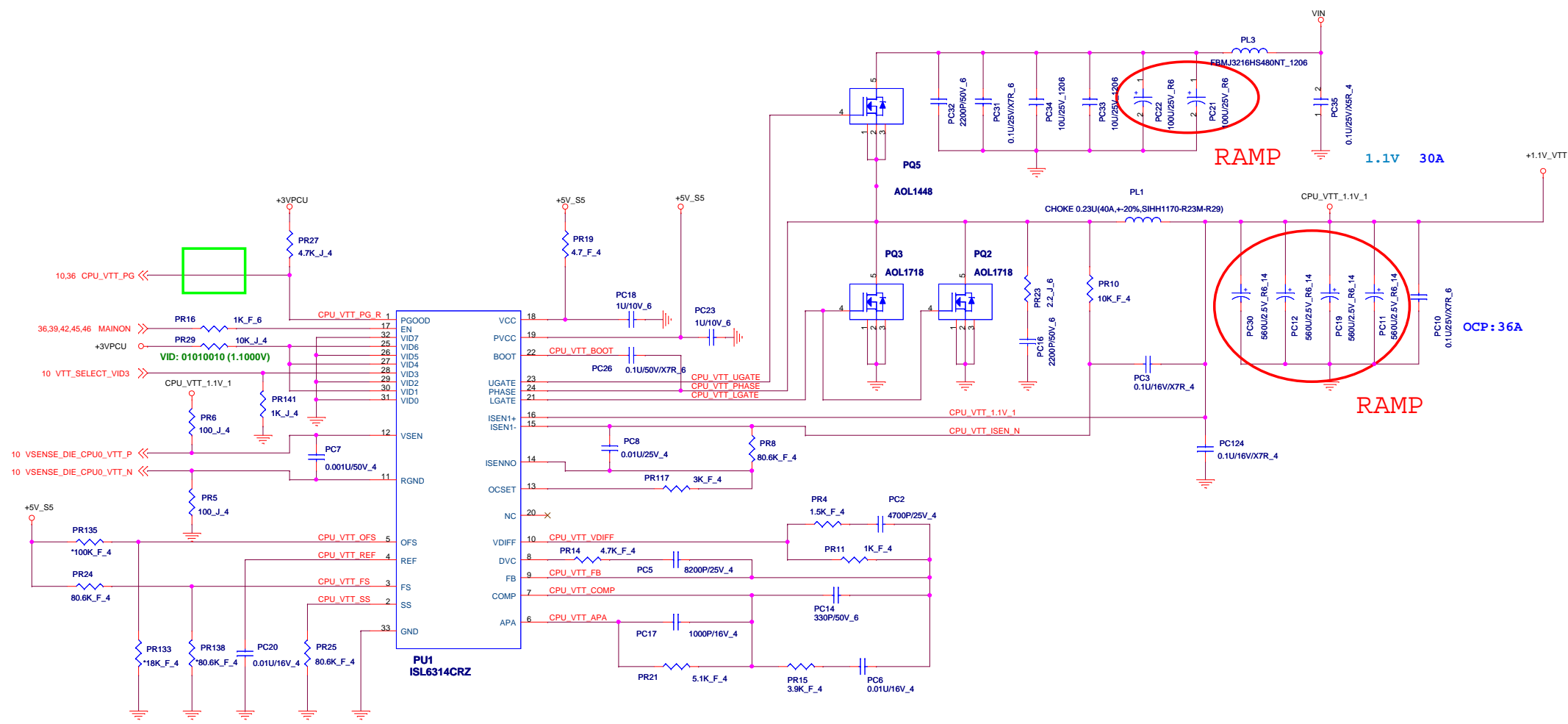
$FDS6690AS R_{ds(on)} = 15 \text{ m ohm}$
 $I_{ocset} = 10 \text{ uA}$
 $R_{ocset}(R266) = 10 \text{ k ohm}$
 $I_{octh} = (10 \text{ uA} * 10 \text{ k}) / 15 \text{ m ohm} = 6.667A$



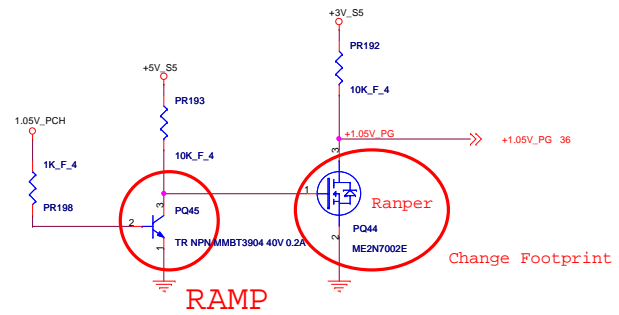
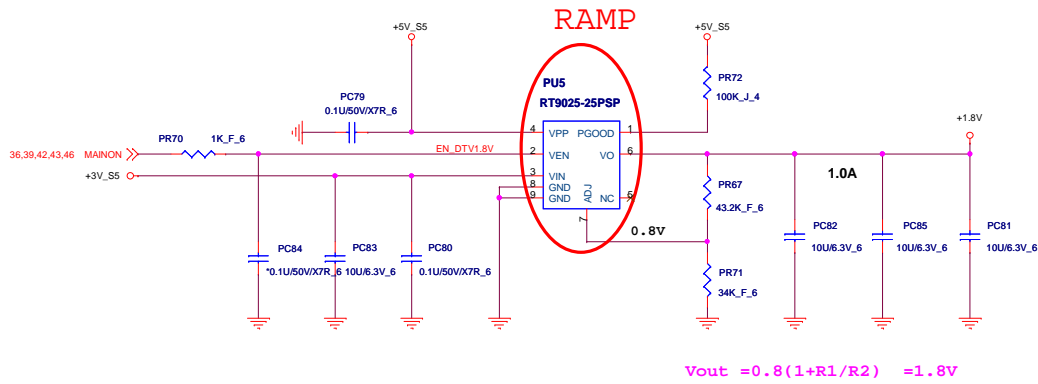
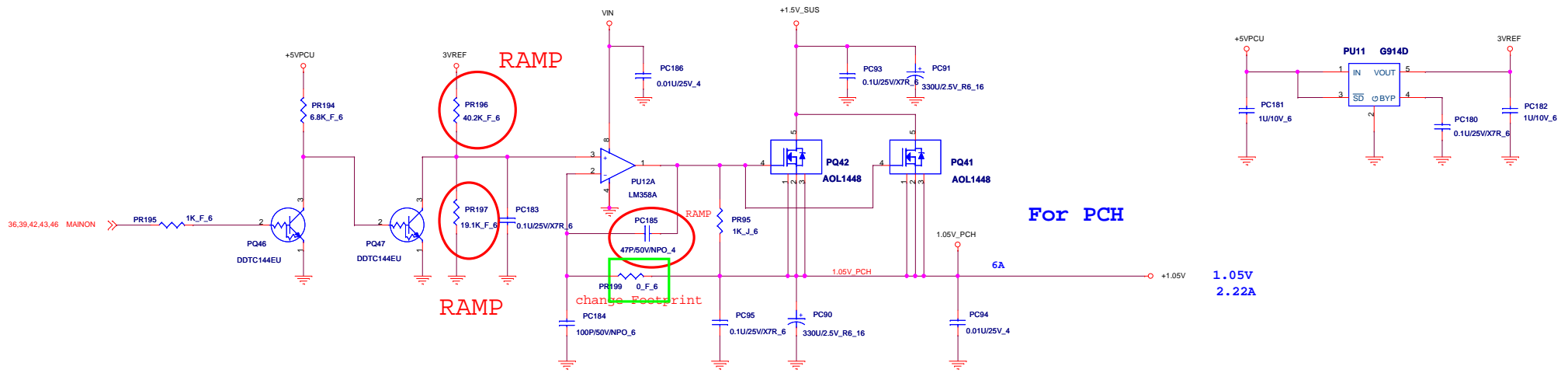
Quanta Computer Inc(QCI).
 211, Wen Hwa 2nd Rd., Kuei Shan,
 Tao Yuan 33377, Taiwan
 Tel.: +886-3-327-2345

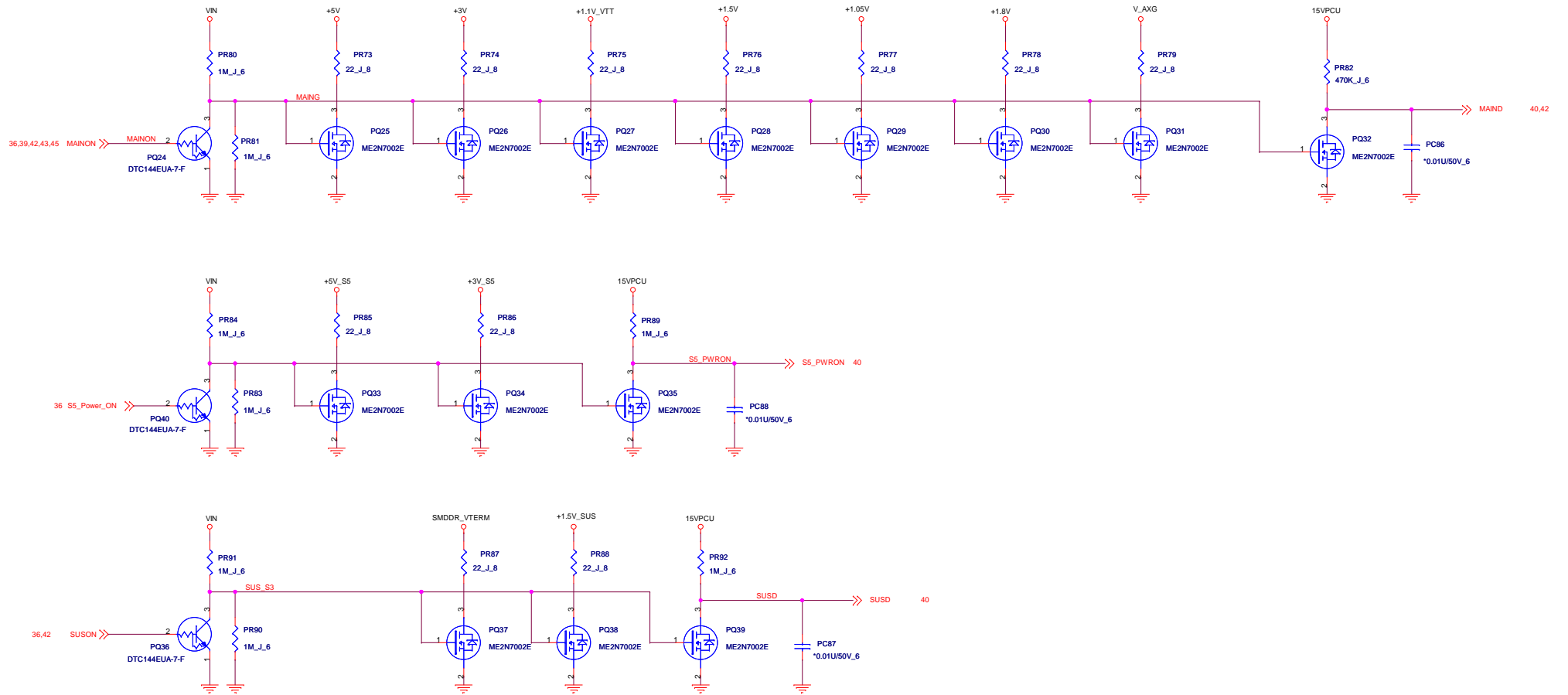
Title ZN2		
Size Custom	Document Number V_AXG(GFX)	Rev A01
Date: Tuesday, March 16, 2010	Sheet 41	of 49

CPU_VTT(1.1V)




Quanta Computer Inc.
PROJECT : ZN2
CPU_VTT_1.1V
 Date: Tuesday, March 16, 2010 Sheet 43 of 49






DATE	ZN2 Schematic file	ZN2 Board file	Revision
DATE	Schematic Change Description		
10.Oct.2009	1. Add +3V pull up trace to CPU_SEL (page 09)		
10.Oct.2009	2. Add the VTT_Select circuit as EL5 does. (page 10)		
10.Oct.2009	3. Change the off page symbol of FDI Sync and Int as output from PCH to Processor. (Page 19)		
10.Oct.2009	4. Populate the series resistance with ICH_PWRBTN# to EC. (Page 19)		
10.Oct.2009	5. Add the CLKRUN# net from EC to ICH. (Page 36)		
10.Oct.2009	6. Change the off page symbol of PMSYNC as the output type from PCH. (Page 19)		
10.Oct.2009	7. Add the test point for L_BKLTCTL (Page 19)		
10.Oct.2009	8. Correct the connection of the following net names: PWROK_EC, MXM_LVDS_BLON, MXM_LVDS_PWREN, (Page 32)		
10.Oct.2009	9. Correct the connection of LCD_CLK and LCD_DAT. (Page 19)		
10.Oct.2009	10. Remove the nets of CRT function and HDMI audio on MXM (Page 25)		
11.Oct.2009	11. Remove the redudant enable for unused port and add the switch IC for DP dual mode. (Page 19)		
11.Oct.2009	12. Add the capacitors for SATA transmitter. (Page 20)		
11.Oct.2009	13. Add GPIO WRITE_EDID_ROM for L10 EDID update (Page 22)		
11.Oct.2009	14. Remove the HDMI audio from PCH to MXM (Page 20)		
11.Oct.2009	15. Reserve the GPIO CR_CPPE# of PCH. (Page 22)		
11.Oct.2009	16. Add the function for CLR_BIOS_DATA and CLR_PASSWD. (Page 22)		
11.Oct.2009	17. Correct the symbol of CLR_BIOS_DATA and CLR_PASSWD. (Page 29)		
11.Oct.2009	18. Correct the STAT capacitors of ODD to receiver. (Page 29)		
11.Oct.2009	19. Use 5V_PCU and +5V_S5 to CN21. (Page 30)		
11.Oct.2009	20. Reserve the GPIO control of CCD_POWER_ON#. (Page 36)		
11.Oct.2009	21. Delete CRT debug from MXM. (Page 25)		
12.Oct.2009	22. Correct the power net for 3VPCU and 5VPCU. (Page 30, 26, 27, 36)		
12.Oct.2009	23. Correct the connection of M_A_DQ46 and M_A_DQ47. (Page 17)		
12.Oct.2009	24. Correct the net name to VR_HOT. (Page 10)		
12.Oct.2009	25. Change the net name of USB4_FB and USB4_FB#. (Page 35)		
12.Oct.2009	26. Change the net name of DDR3 VTT to DDR_VTERM. (Page 17, 18) ==> no change~!!!		
12.Oct.2009	27. Reserve the resistnaces for CK0 and CK1 pairs of CHA and CHB. (Page 17, 18)		
12.Oct.2009	28. Change the MXM_12V on MXM page. (Page 25)		
27.Nov.2009	29. Change net VR_ready Pull High(Page 9)		
27.Nov.2009	30. Delete MXM to VGA port circuit(Page 25/27)		
27.Nov.2009	31. Change ACN4 to right angle typy(Page26)		
27.Nov.2009	32. Delete CN16 XDP connect (Page37)		
27.Nov.2009	33. Swap USB2, USB3, USB10, differential signal(Page31)		
27.Nov.2009	34. Delete all JP connection		
27.Nov.2009	35. CN14 LCD_Clk & LCD_Data swap(Page25)		
27.Nov.2009	36. CLK_LPC_DEBUG net change to CN17 pin19(Page30)		
27.Nov.2009	37. PEG_CLKREQ#_R pull low,Change R457 resistor to R454(Page21)		

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DATE	ZN2 Schematic file	ZN2 Board file	Revision

DATE	Schematic Change Description
27.Nov.2009	38. Change ACin Soft start Function and add Adaptor ID to identify Function and disable ID to identify and delete Short Pad JP5, JP6 (Page 39)
27.Nov.2009	39. Delete Short Pad PJP7, PJP8, PJP9, PJP10, PJP11, PJP12 (Page 40)
27.Nov.2009	40. Delete short Pad PJP4, PJP5 and Place up PR190 for V_AXG initial setting Voltage Place up PR48 for V_AXG PG Pull high (Page 41)
27.Nov.2009	41. Change PR116 Value to 6.81K ohm and PL4 Value to 0.88uH and add Location PC210, PC211, PQ64 and delete Short Pad PJP1 (Page 42)
27.Nov.2009	42. Delete Short Pad PJP2, PJP3 (Page 43)
27.Nov.2009	43. Change CPU core Value PR132, PR122, PR140, PR145, PR150, PR154 (Page 44)
27.Nov.2009	44. Delete Short Pad PJP6 (Page 45)
27.Nov.2009	45. Place up PQ27, PQ28, PQ29, PQ30, PQ31, PQ38, PR88 (Page 46)
29.Nov.2009	46. MOVE EC circuit (PAGE 36)'s LED indicate circuit to (Page 39) ACin circuit
2.Dec.2009	47. Connect GFX_VR_EN to dGPU_PRSENT# (Page 10)
2.Dec.2009	48. Add RC circuit for SRTC_RST# (Page 20)
2.Dec.2009	49. Change CLK_PCIE_DMI# differential pair RP15 to L44/L45 (Page 21)
2.Dec.2009	50. Change C328 to 330uF and Delete C329,C335,C336,C343,C344(Page 14)
2.Dec.2009	51. Remove R174 10Kohm(Page 25)
2.Dec.2009	52. Remove R389 , place R374 to 0 ohm, 1394 component, Change U17 to JMB385 (Page 28)
2.Dec.2009	53. Change CN11 to right angle type(Page 29)
2.Dec.2009	54. Place the SATA_ACT circuit component(Page 30)
2.Dec.2009	55. Remove the hall sensor component and add LED5(Page 36)
2.Dec.2009	56. Add SW1 (Page 36)
7.Dec.2009	57. Reverse HDD connect pin (Page 29)
26.Jan.2010	58. Change Write_EDID_ROM to GPIO28 (Page 22)
26.Jan.2010	59. Reserve MXM to CRT function (Page 25/27)
26.Jan.2010	60. Reserve R395 for PEG_CLKREQ pull high (Page 25)
26.Jan.2010	61. Change C274/C276 to 47u (Page 27)
26.Jan.2010	62. Change CN29 Pin2 power to +5V_S5_USB (Page 30)
26.Jan.2010	63. Change F7/F8/F9 power to +5V_S5_USB (Page 31)
26.Jan.2010	64. Change C447,C483,C493,C489,C478,C482,C490,C494,,C287,C399,C265,C472,C469,C466 to 100u/7343 type (Page 31)
26.Jan.2010	65. Add D61 (Page 31)
26.Jan.2010	66. Reserve R232 for Write_EDID_ROM pull low function (Page 32)
26.Jan.2010	67. Add C329 for Lan loss solution (Page 33)
26.Jan.2010	68. CN29 Pin15/16 floating (Page 34)
26.Jan.2010	69. Change R257 power to +5V_S5_USB (Page 35)
26.Jan.2010	70. Reserve R63 (Page 36)
26.Jan.2010	71. Add ADP-ID to EC ADC1 (Page 36/39)
26.Jan.2010	72. Change Screw H23,H19,H2,H4,H5,H11,H28 (Page 38)
26.Jan.2010	73. Change ACin Adaptor ID to identify Function circuit and add delay time for EN3V5V enable circuit(Page 39)

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4. Nat name Description :

Voltage Rails

VIN	Primary DC system power supply
+5VPCU	5.0V always on power rail by LATCH or ACIN
+3VPCU	3.3V always on power rail by LATCH or ACIN
+5V_S5	5.0V always on power rail by DCON
+3V_S5	3.3V always on power rail by DCON

+5V_S5_USB	5.0V power rail by SUSD
+3V	3.3V switched power rail by MAIND
+5V	5.0V switched power rail by MAIND

+VCC_CORE	Core Voltage for CPU
CPU_VTT_1.1V	1.1V power rail for AGTL+ termination/Core for GMCH by MAINON
1.05V_PCH	1.05V power rail for PCH Core Power by MAINON
+1.8V	1.8V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for VRM/NVRAM by MAINON
+1.5V	1.5V power rail for MiniPCI by MAIND
+1.5V_SUS	1.5V power rail for DDRIII by SUSON
SMDDR_VTERM	0.75V DDRIII Termination Voltage by MAINON

Part Naming Conventions

C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

Net Name Suffix

#	= Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Normal Signal / Ground 1 Plane
Layer 5		Power Plane
Layer 6		Solder Side, Microstrip signal Layer

Layers : 6 Depth 1.6mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		