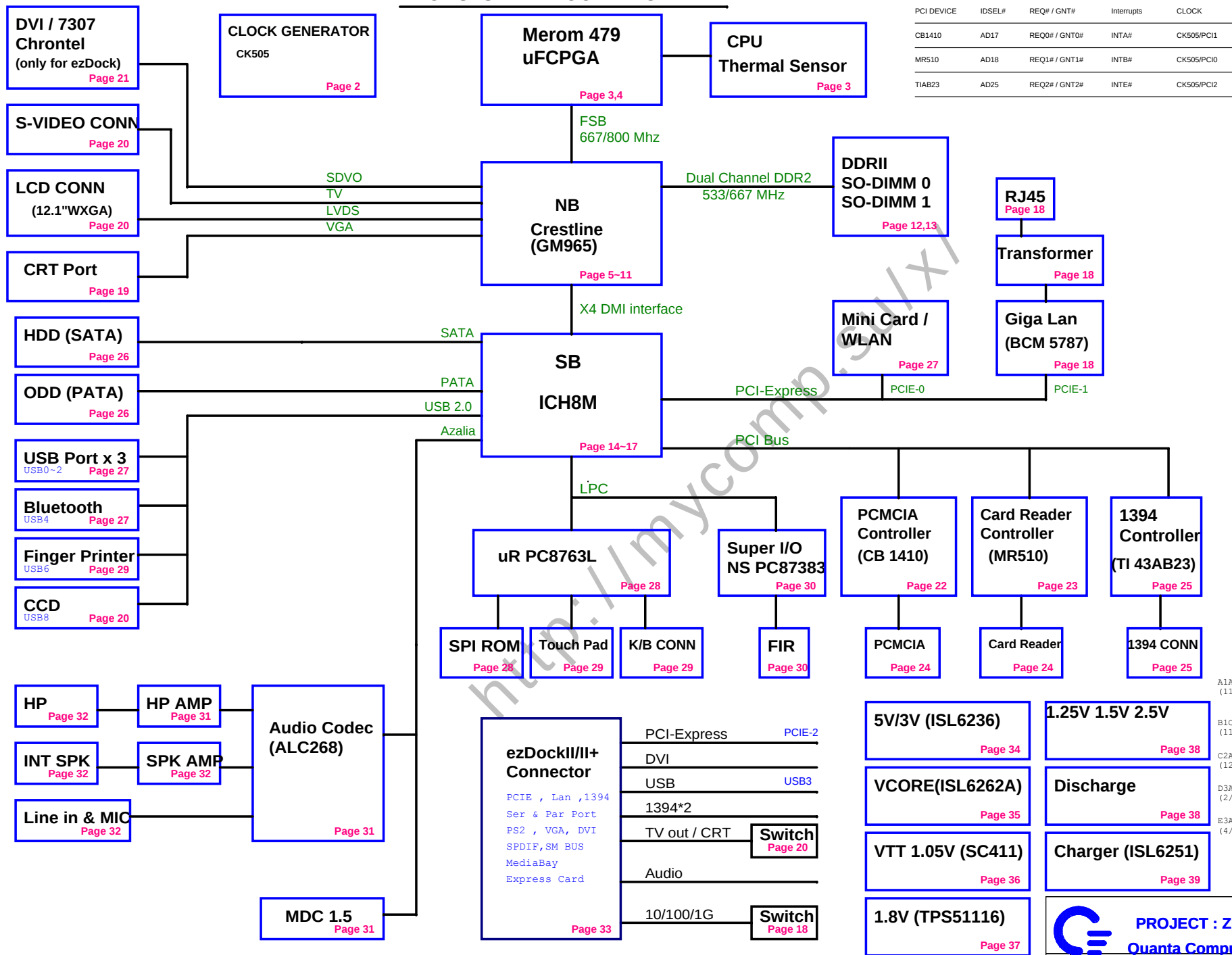


ZU1 SYSTEM BLOCK DIAGRAM



A1A
(11/2): (1) Re-name.
(2) Gerber out

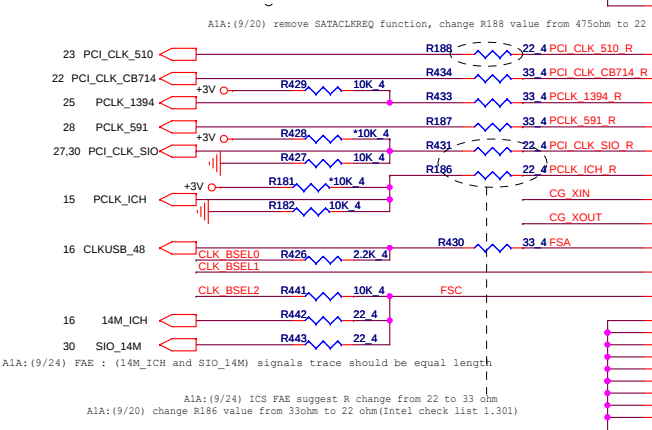
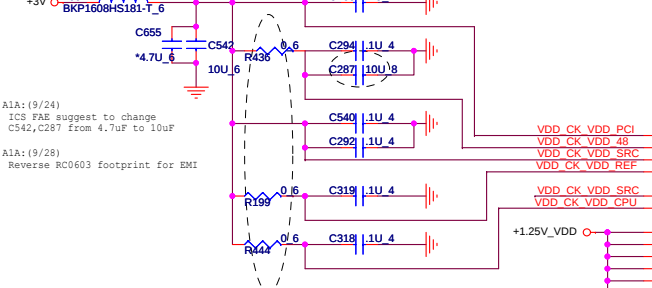
B1C
(11/29): Gerber out

C2A
(12/28): Gerber out

D3A
(2/12): Gerber out

E3A
(4/2): Gerber out

Clock Generator



A1A: (9/24) ICS FAE suggest to change C542, C287 from 4.7uF to 10uF

A1A: (9/28) Reverse RC0603 footprint for EMI

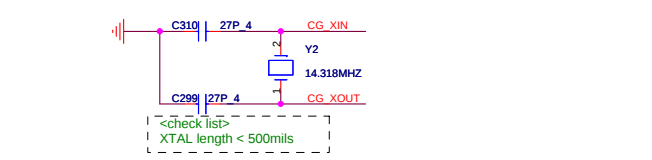
A1A: (9/20) remove SATACLKREQ function, change R188 value from 475ohm to 22 ohm

A1A: (9/24) FAE : (14M_ICH and SIO_14M) signals trace should be equal length

A1A: (9/24) ICS FAE suggest R change from 22 to 33 ohm

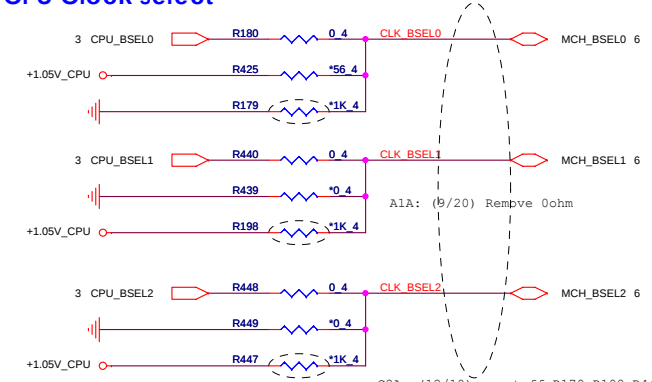
A1A: (9/20) change R186 value from 33ohm to 22 ohm (Intel check list 1.301)

C2A: (12/26) Base on vendor-FCE suggestion, change C310/C299 from CH03306JB07 (33p) to CH02706JB06 (27p)



<check list>
XTAL length < 500mils

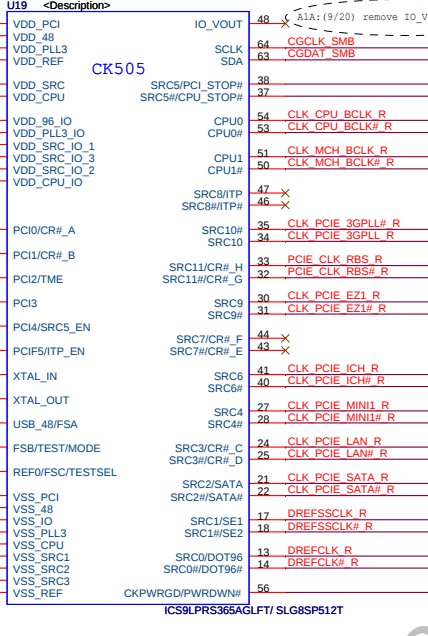
CPU Clock select



C2A: (12/10) no stuff R179, R198, R447 for auto CPU frequency selection (follow ZD1, Z01)

E3A: (3/16) Change C542 from 0805(CH6102K9A01) to 0603(CH6101K9905) base on ME request (HDD Mylar issue)

ICS9LPRS365BGLFT
SLG8SP512T: AL8SP512K05

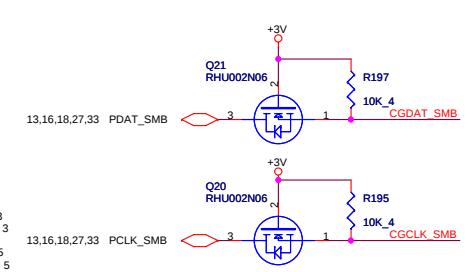


<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.
(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock. If PD be detect at powe-on, the CK505 will setting Pin 37/38 to PCL_STOP/CUP_SOTP (Default is setting to PCL_STOP/CUP_SOTP)
(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock. If PD be detect at powe-on, the CK505 will setting Pin 46/47 to SRC8 (Default is setting to SRC8)
(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M, Pin 37, 38 will fixed be use CPU_Stop and PCL_Stop.
(5)SLG505Y64 CK505 Standard parts follow standard setting

BSEL Frequency Select Table

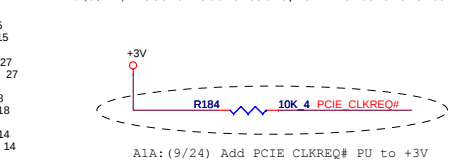
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Clock Gen I2C



Pin	Active	Control signal
32	Low	SRC9/9#
33	Low	SRC10/10#

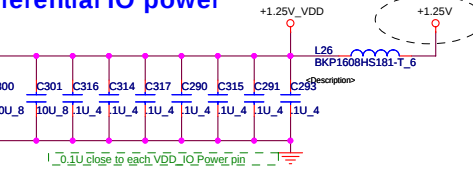
A1A: (9/24) Base on above table, SWAP SRC3 and SRC9



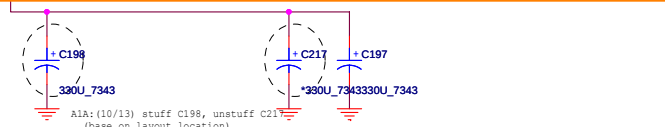
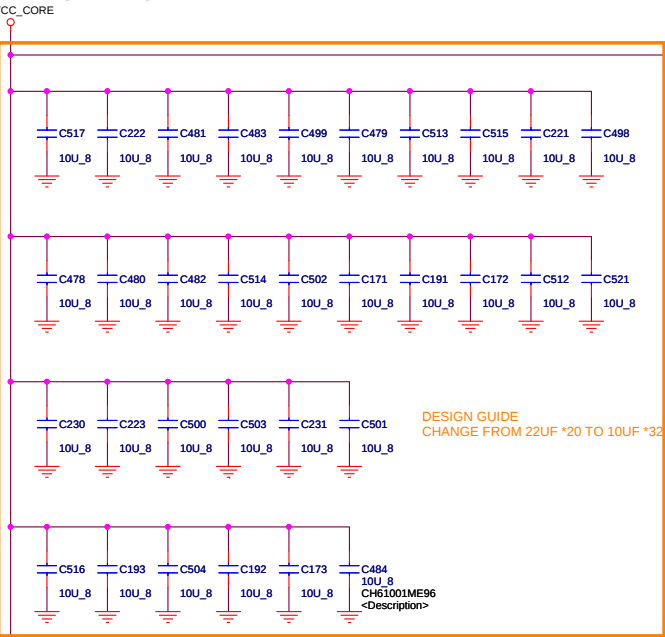
A1A: (9/24) Add PCIE_CLKREQ# PU to +3V

C2A: (12/12) change from +1.05V to +1.25V. Because VDD_IO will drop out when high loading

Clock Gen Differential IO power



CPU(Power)

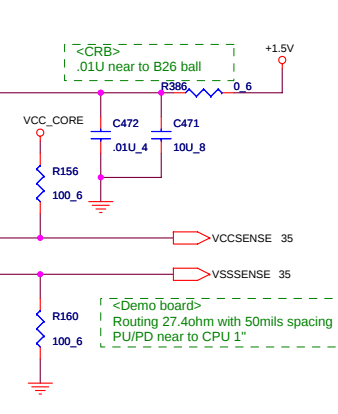
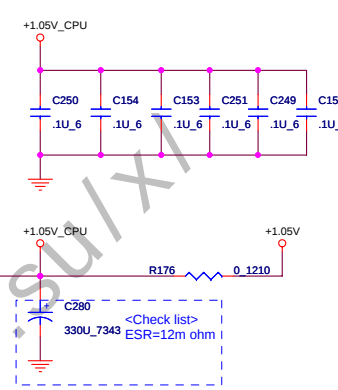


<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U30C		
A7	VCC[001]	VCC[068]
A9	VCC[002]	VCC[069]
A10	VCC[003]	VCC[070]
A12	VCC[004]	VCC[071]
A13	VCC[005]	VCC[072]
A15	VCC[006]	VCC[073]
A17	VCC[007]	VCC[074]
A18	VCC[008]	VCC[075]
A20	VCC[009]	VCC[076]
B7	VCC[010]	VCC[077]
B9	VCC[011]	VCC[078]
B10	VCC[012]	VCC[079]
B12	VCC[013]	VCC[080]
B14	VCC[014]	VCC[081]
B15	VCC[015]	VCC[082]
B17	VCC[016]	VCC[083]
B18	VCC[017]	VCC[084]
B20	VCC[018]	VCC[085]
C9	VCC[019]	VCC[086]
C10	VCC[020]	VCC[087]
C12	VCC[021]	VCC[088]
C13	VCC[022]	VCC[089]
C15	VCC[023]	VCC[090]
C17	VCC[024]	VCC[091]
C18	VCC[025]	VCC[092]
D9	VCC[026]	VCC[093]
D10	VCC[027]	VCC[094]
D12	VCC[028]	VCC[095]
D14	VCC[029]	VCC[096]
D15	VCC[030]	VCC[097]
D17	VCC[031]	VCC[098]
D18	VCC[032]	VCC[099]
E7	VCC[033]	VCC[100]
E9	VCC[034]	VCC[101]
E10	VCC[035]	VCC[102]
E12	VCC[036]	VCC[103]
E13	VCC[037]	VCC[104]
E15	VCC[038]	VCC[105]
E17	VCC[039]	VCC[106]
E18	VCC[040]	VCC[107]
E20	VCC[041]	VCC[108]
F7	VCC[042]	VCC[109]
F9	VCC[043]	VCC[110]
F10	VCC[044]	VCC[111]
F12	VCC[045]	VCC[112]
F14	VCC[046]	VCC[113]
F15	VCC[047]	VCC[114]
F17	VCC[048]	VCC[115]
F18	VCC[049]	VCC[116]
F20	VCC[050]	VCC[117]
AA7	VCC[051]	VCC[118]
AA9	VCC[052]	VCC[119]
AA10	VCC[053]	VCC[120]
AA12	VCC[054]	VCC[121]
AA13	VCC[055]	VCC[122]
AA15	VCC[056]	VCC[123]
AA17	VCC[057]	VCC[124]
AA18	VCC[058]	VCC[125]
AA20	VCC[059]	VCC[126]
AB9	VCC[060]	VCC[127]
AC10	VCC[061]	VCC[128]
AB10	VCC[062]	VCC[129]
AB12	VCC[063]	VCC[130]
AB14	VCC[064]	VCC[131]
AB15	VCC[065]	VCC[132]
AB17	VCC[066]	VCC[133]
AB18	VCC[067]	VCC[134]

U30D		
AB20	VCC[068]	VCC[135]
AB21	VCC[069]	VCC[136]
AC7	VCC[070]	VCC[137]
AC9	VCC[071]	VCC[138]
AC12	VCC[072]	VCC[139]
AC15	VCC[073]	VCC[140]
AC17	VCC[074]	VCC[141]
AC18	VCC[075]	VCC[142]
AD7	VCC[076]	VCC[143]
AD9	VCC[077]	VCC[144]
AD10	VCC[078]	VCC[145]
AD12	VCC[079]	VCC[146]
AD14	VCC[080]	VCC[147]
AD15	VCC[081]	VCC[148]
AD17	VCC[082]	VCC[149]
AD18	VCC[083]	VCC[150]
AE9	VCC[084]	VCC[151]
AE10	VCC[085]	VCC[152]
AE12	VCC[086]	VCC[153]
AE13	VCC[087]	VCC[154]
AE15	VCC[088]	VCC[155]
AE17	VCC[089]	VCC[156]
AE18	VCC[090]	VCC[157]
AE20	VCC[091]	VCC[158]
AE9	VCC[092]	VCC[159]
AE10	VCC[093]	VCC[160]
AE12	VCC[094]	VCC[161]
AE17	VCC[095]	VCC[162]
AE15	VCC[096]	VCC[163]
AE18	VCC[097]	VCC[164]
AE17	VCC[098]	VCC[165]
AE18	VCC[099]	VCC[166]
AE20	VCC[100]	VCC[167]

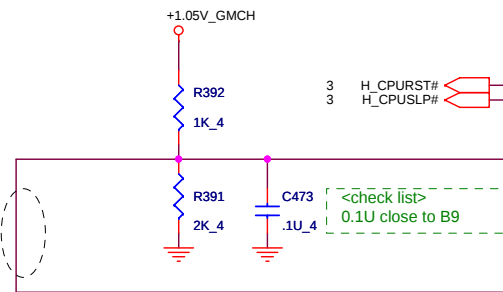
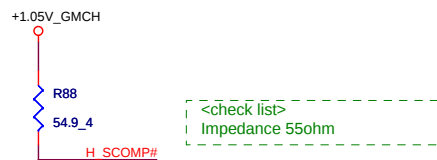
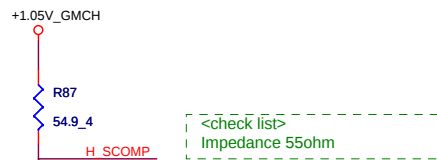
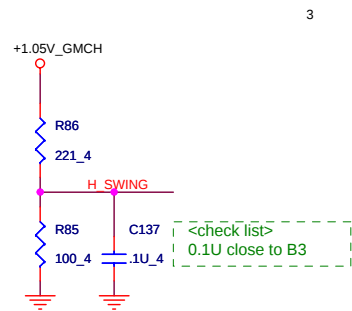
<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA



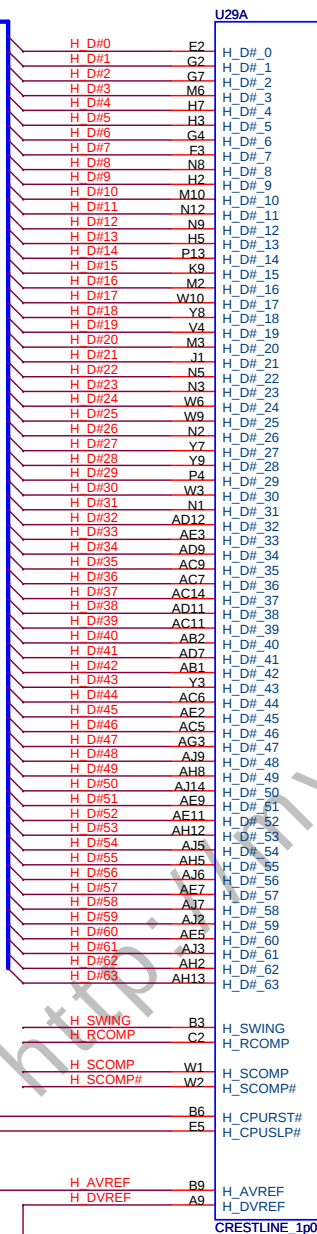
U30D		
AA4	VSS[001]	VSS[082]
AA8	VSS[002]	VSS[083]
AA11	VSS[003]	VSS[084]
AA14	VSS[004]	VSS[085]
AA16	VSS[005]	VSS[086]
AA19	VSS[006]	VSS[087]
AA23	VSS[007]	VSS[088]
AA27	VSS[008]	VSS[089]
AA30	VSS[009]	VSS[090]
AA33	VSS[010]	VSS[091]
AA36	VSS[011]	VSS[092]
AA39	VSS[012]	VSS[093]
AA42	VSS[013]	VSS[094]
AA45	VSS[014]	VSS[095]
AA48	VSS[015]	VSS[096]
AA51	VSS[016]	VSS[097]
AA54	VSS[017]	VSS[098]
AA57	VSS[018]	VSS[099]
AA60	VSS[019]	VSS[100]
AA63	VSS[020]	VSS[101]
AA66	VSS[021]	VSS[102]
AA69	VSS[022]	VSS[103]
AA72	VSS[023]	VSS[104]
AA75	VSS[024]	VSS[105]
AA78	VSS[025]	VSS[106]
AA81	VSS[026]	VSS[107]
AA84	VSS[027]	VSS[108]
AA87	VSS[028]	VSS[109]
AA90	VSS[029]	VSS[110]
AA93	VSS[030]	VSS[111]
AA96	VSS[031]	VSS[112]
AA99	VSS[032]	VSS[113]
AA102	VSS[033]	VSS[114]
AA105	VSS[034]	VSS[115]
AA108	VSS[035]	VSS[116]
AA111	VSS[036]	VSS[117]
AA114	VSS[037]	VSS[118]
AA117	VSS[038]	VSS[119]
AA120	VSS[039]	VSS[120]
AA123	VSS[040]	VSS[121]
AA126	VSS[041]	VSS[122]
AA129	VSS[042]	VSS[123]
AA132	VSS[043]	VSS[124]
AA135	VSS[044]	VSS[125]
AA138	VSS[045]	VSS[126]
AA141	VSS[046]	VSS[127]
AA144	VSS[047]	VSS[128]
AA147	VSS[048]	VSS[129]
AA150	VSS[049]	VSS[130]
AA153	VSS[050]	VSS[131]
AA156	VSS[051]	VSS[132]
AA159	VSS[052]	VSS[133]
AA162	VSS[053]	VSS[134]
AA165	VSS[054]	VSS[135]
AA168	VSS[055]	VSS[136]
AA171	VSS[056]	VSS[137]
AA174	VSS[057]	VSS[138]
AA177	VSS[058]	VSS[139]
AA180	VSS[059]	VSS[140]
AA183	VSS[060]	VSS[141]
AA186	VSS[061]	VSS[142]
AA189	VSS[062]	VSS[143]
AA192	VSS[063]	VSS[144]
AA195	VSS[064]	VSS[145]
AA198	VSS[065]	VSS[146]
AA201	VSS[066]	VSS[147]
AA204	VSS[067]	VSS[148]
AA207	VSS[068]	VSS[149]
AA210	VSS[069]	VSS[150]
AA213	VSS[070]	VSS[151]
AA216	VSS[071]	VSS[152]
AA219	VSS[072]	VSS[153]
AA222	VSS[073]	VSS[154]
AA225	VSS[074]	VSS[155]
AA228	VSS[075]	VSS[156]
AA231	VSS[076]	VSS[157]
AA234	VSS[077]	VSS[158]
AA237	VSS[078]	VSS[159]
AA240	VSS[079]	VSS[160]
AA243	VSS[080]	VSS[161]
AA246	VSS[081]	VSS[162]
AA249	VSS[082]	VSS[163]

NB(HOST)

D3A: (2/1) Change 965GM from ES sample to QS sample
Change U29 P/N from AJ0QN120T37 to AJ0QP200T09

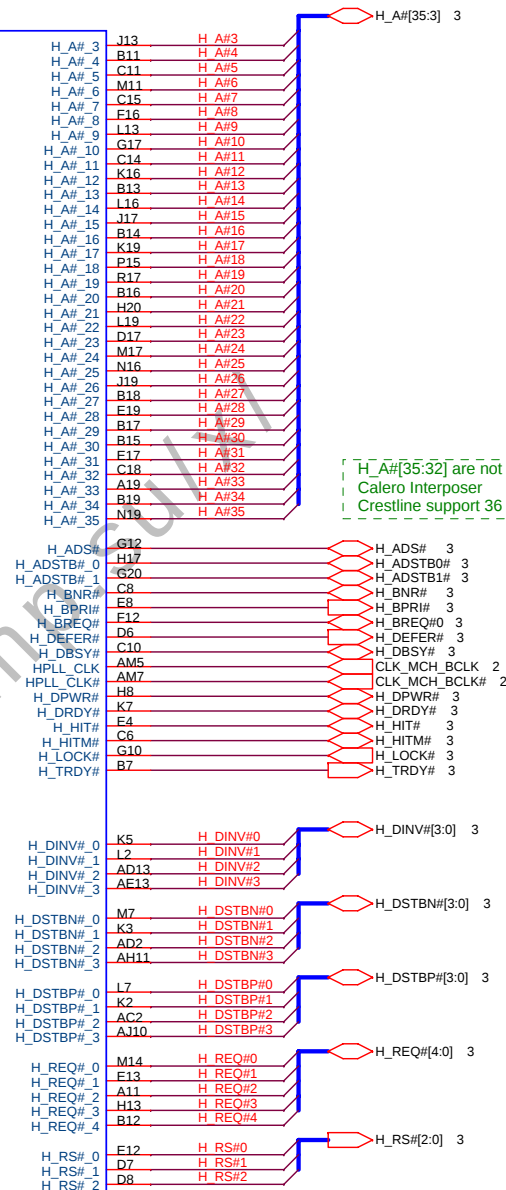


A1A: (9/20) remove R74 (0 ohm)



CRESTLINE_1p0

HOST



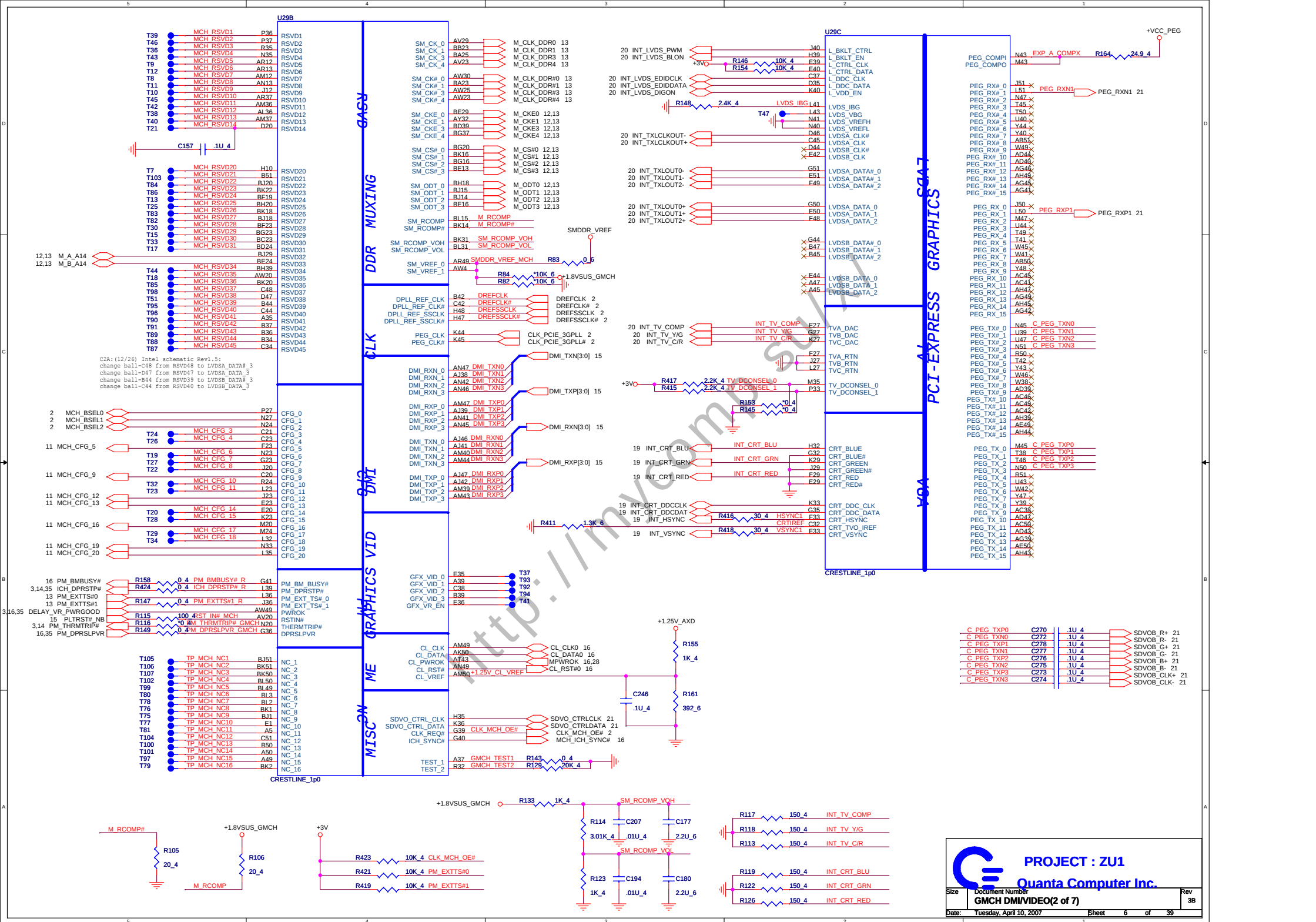
H_A#35:32 are not supported in
Calero Interposer
Crestline support 36 bit address



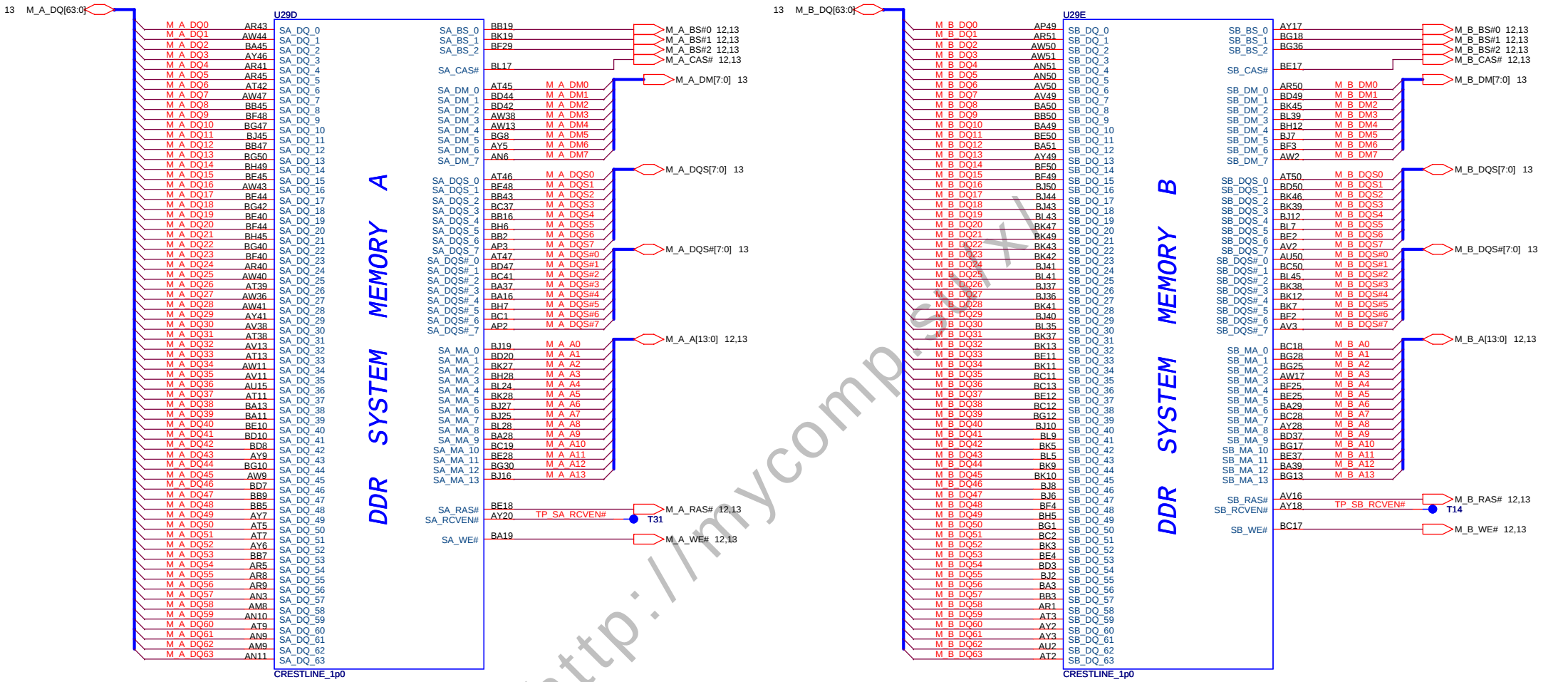
PROJECT : ZU1

Quanta Computer Inc.

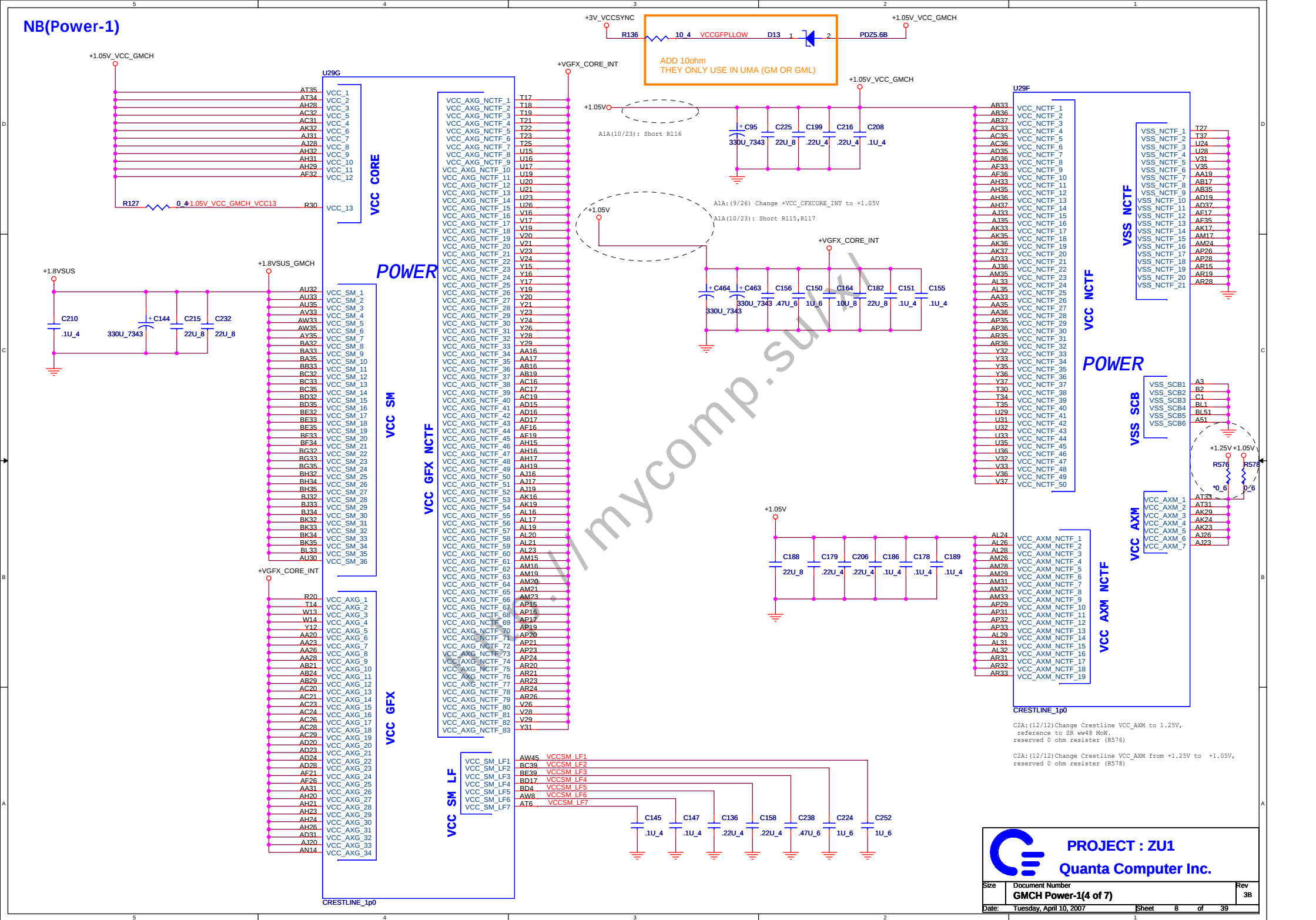
Size	Document Number	Rev
	GMCH HOST(1 of 7)	3B
Date:	Tuesday, April 10, 2007	Sheet 5 of 39



NB(Memory controller)



NB(Power-1)



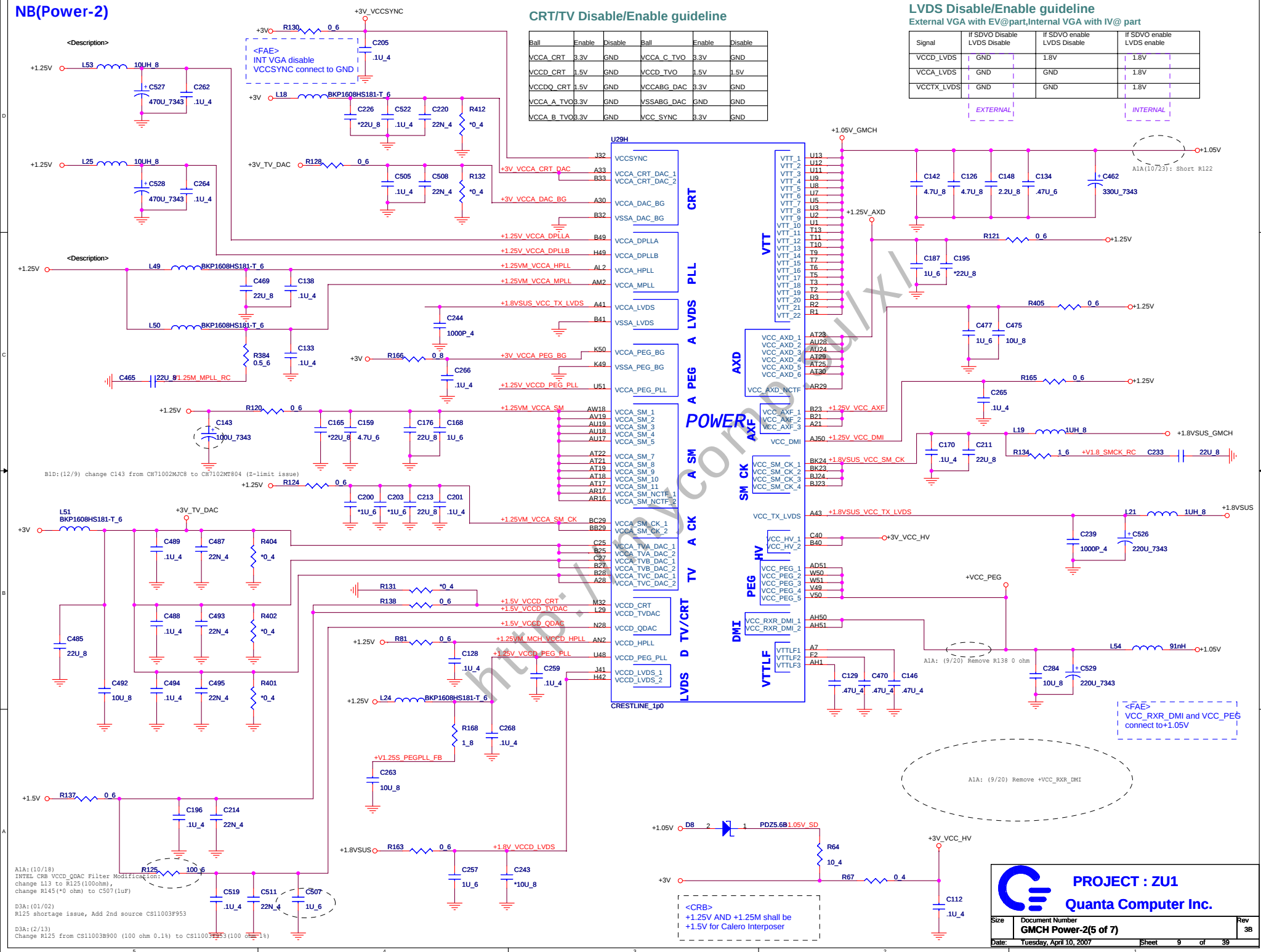
NB(Power-2)

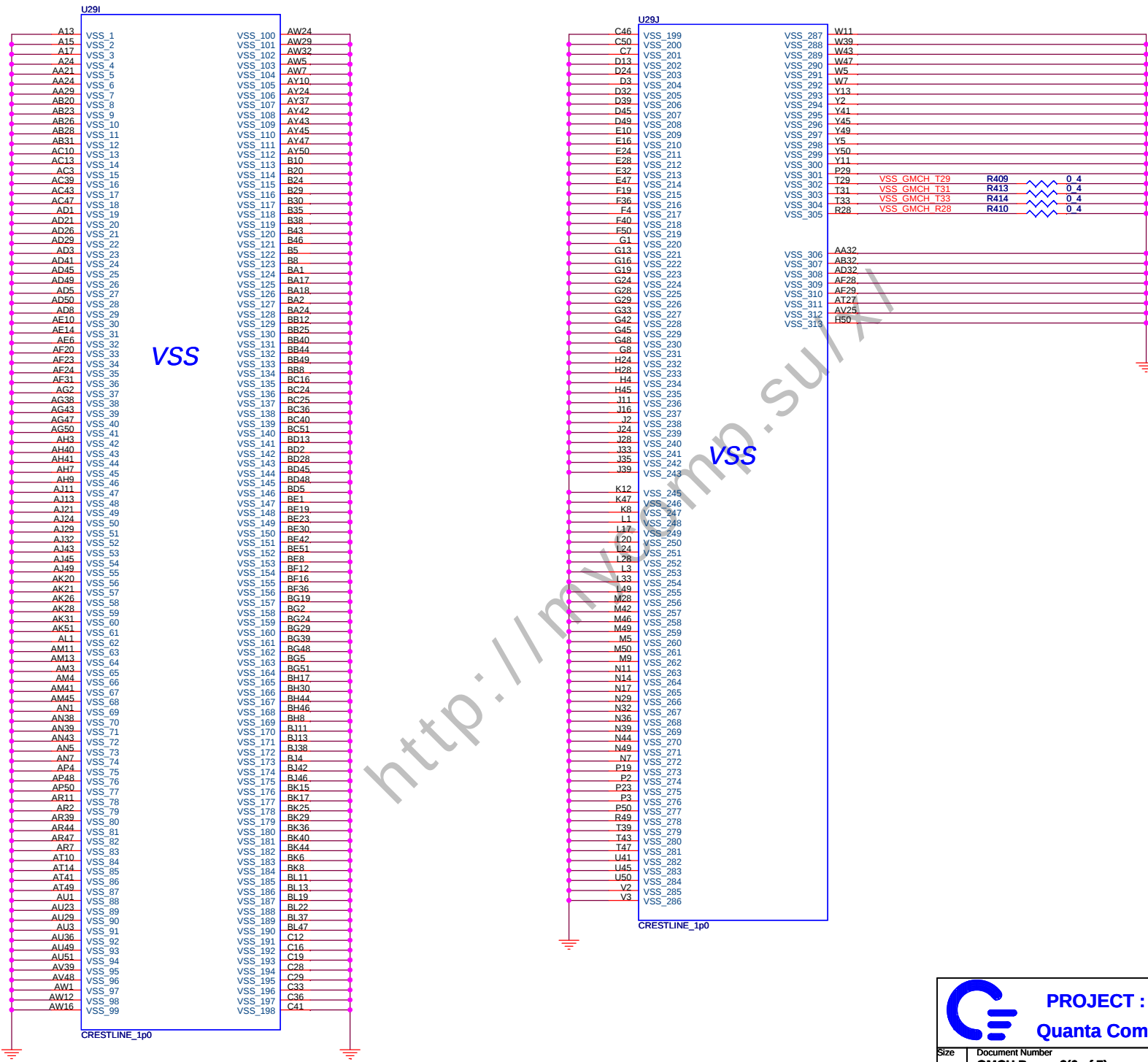


LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V





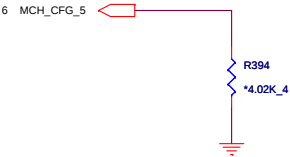
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

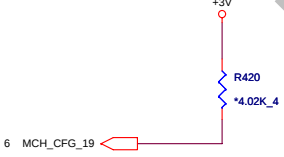
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
-----------	---------------------------------------



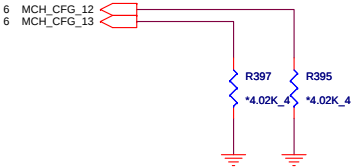
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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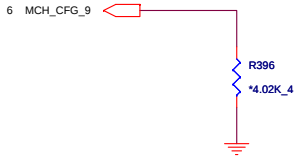
XOR /Allz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

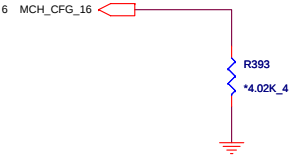


SDVO Present

Strap define at External DVI control page

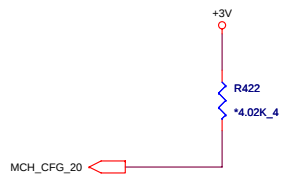
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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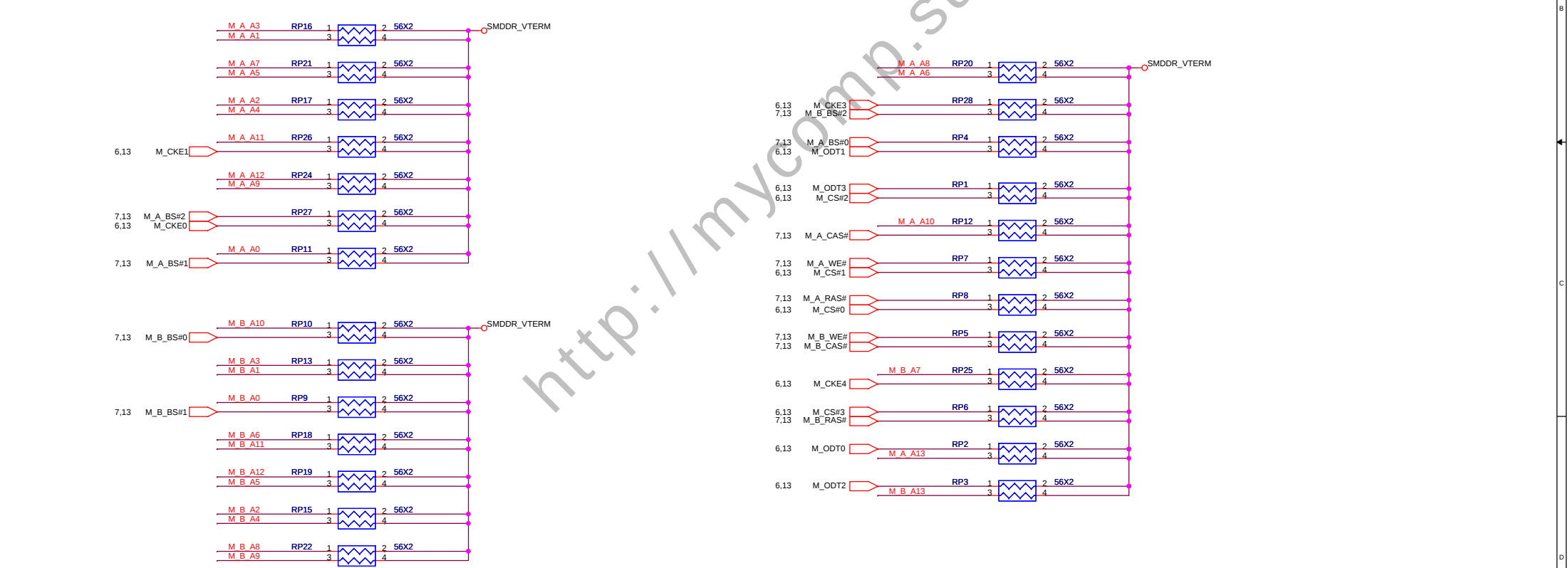
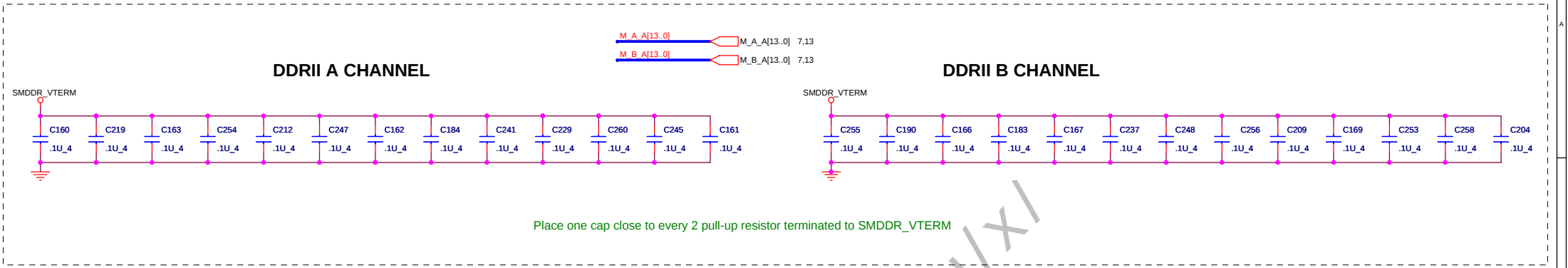
SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port
------------	--



PROJECT : ZU1
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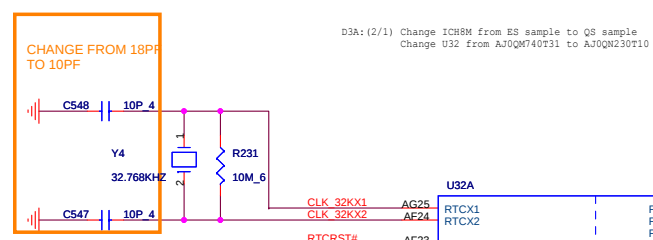
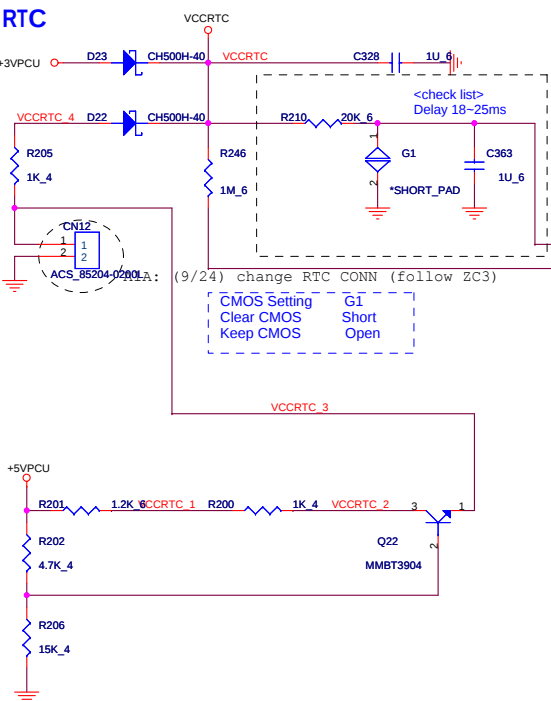
DDR2 Dual channel A/B PU



INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

The diagram shows a pull-up resistor network for MA14, with resistors R144 and R135 connected to SMDDR_VTERM.

RTC



E3A: (3/30) Intel checklist Rev 4.6
The GLAN_COMP0/GLAN_COMP1 connection to 1.5-V rail through the resistor remains even if non-Intel LAN is used.
Stuff R232 (CS02492F29)

A1A: 9/1 Remove GLAN

A1A: (9/20) Remove SATA1/SATA2

SATA Disable

- 1.Connect to GND: SATA[2:0]RXp/n, SATARBIAS, SATARBIAS#, SATA_CLKP, SATACLKN
- 2.NC: SATA[2:0]TXp/n, SATALED#
- 3.VccSATAPLL should be connected directly to Vcc1_5, Filter cap are not required
- 4.BIOS disable

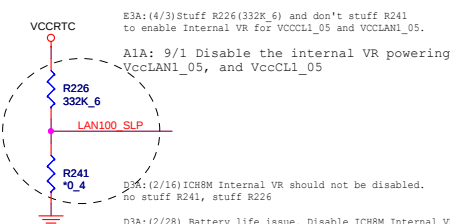
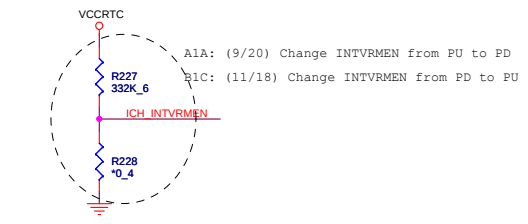
SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

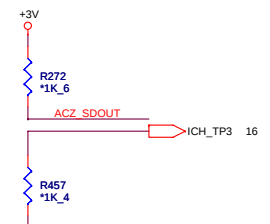
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---



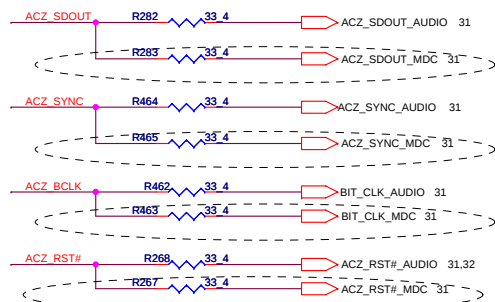
XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1



HDA

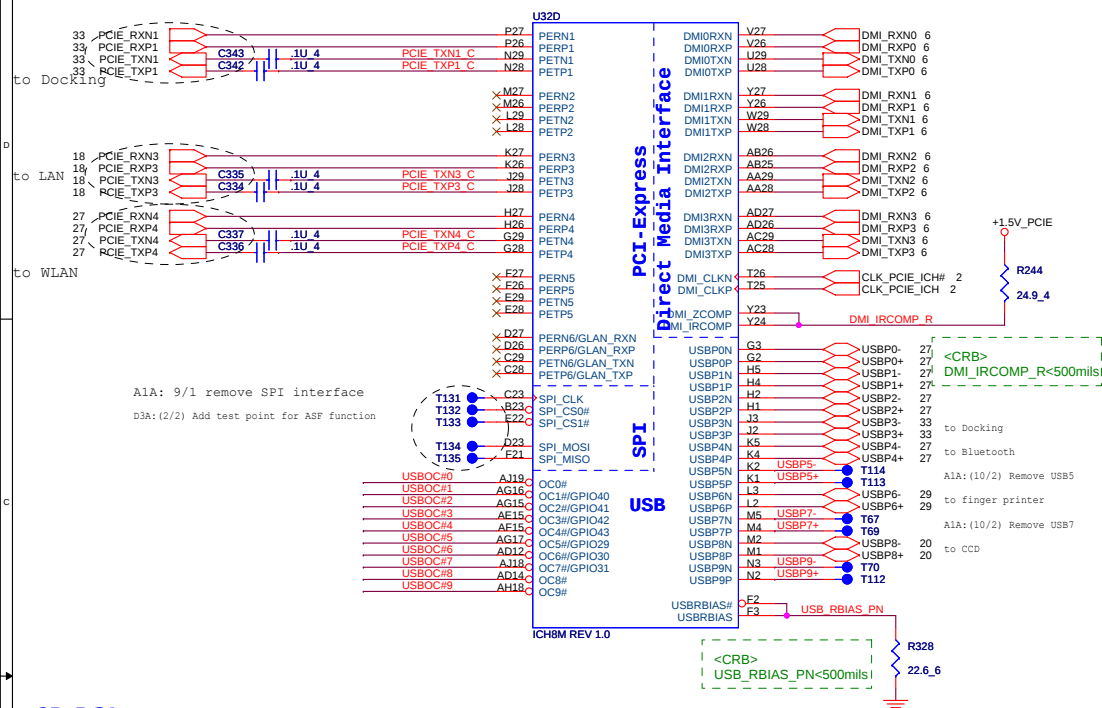
A1A: 9/6 base on Intel design guide, add it.



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	3B
Date:	Tuesday, April 10, 2007	Sheet 14 of 39

SB-PCIE/USB/DMI

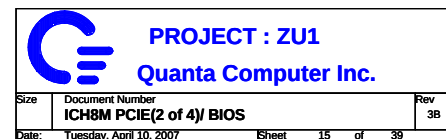
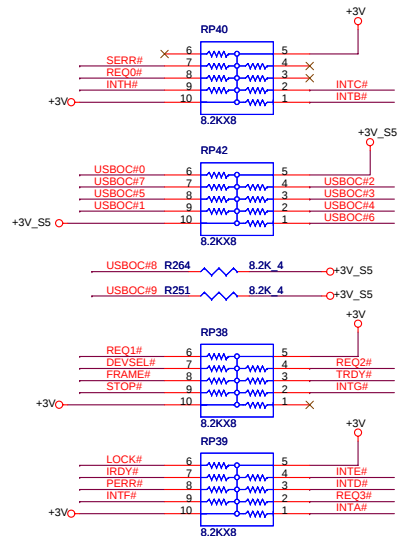
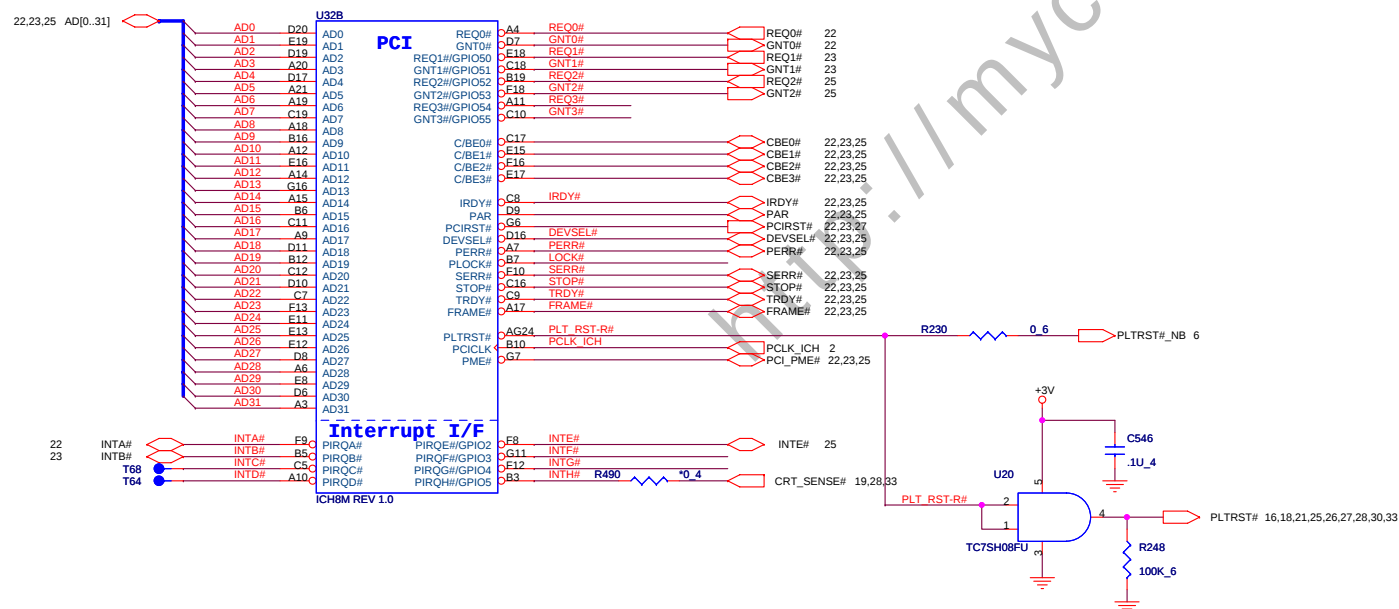


A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

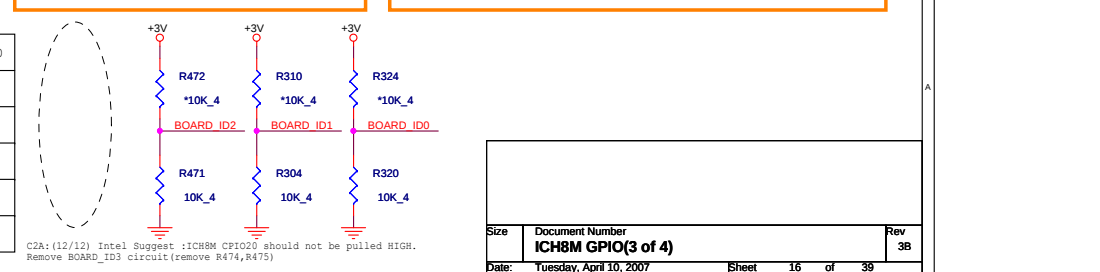
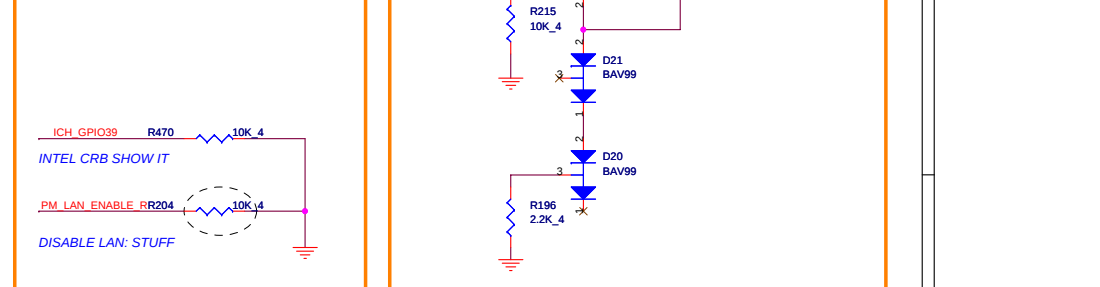
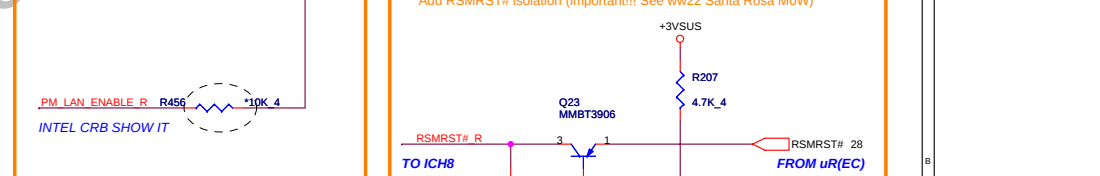
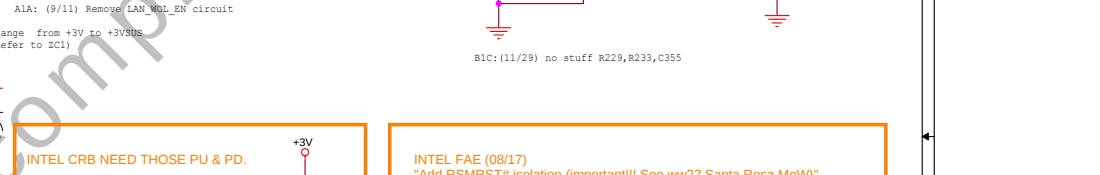
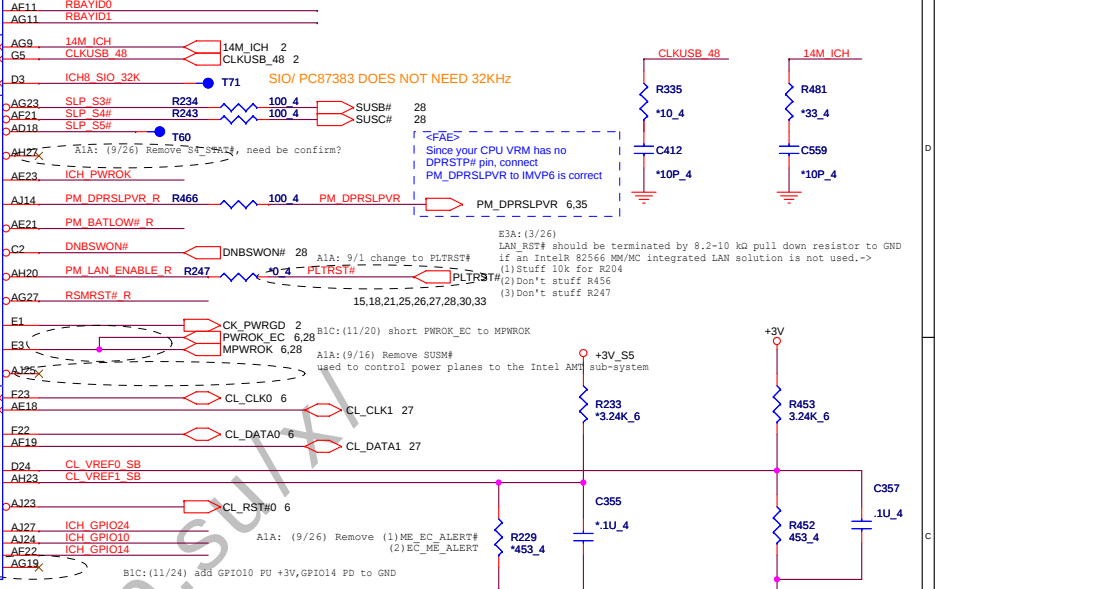
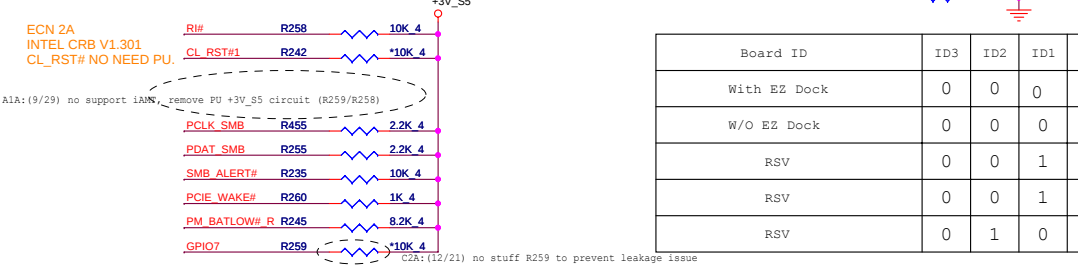
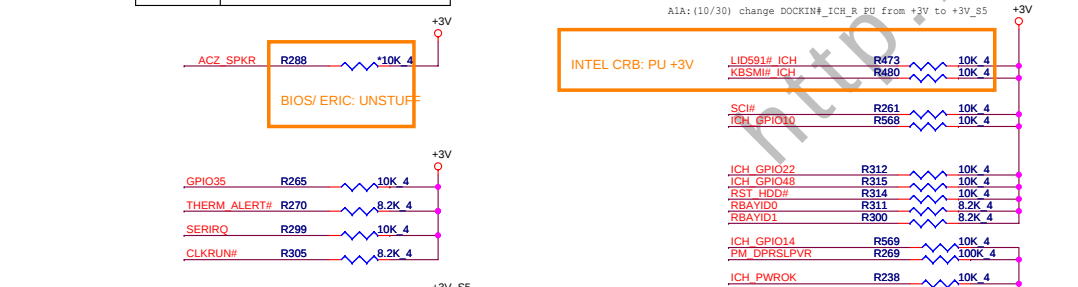
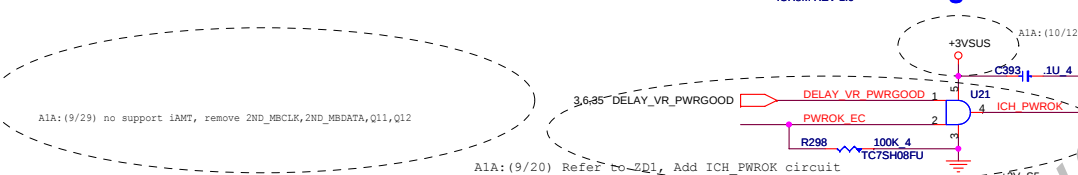
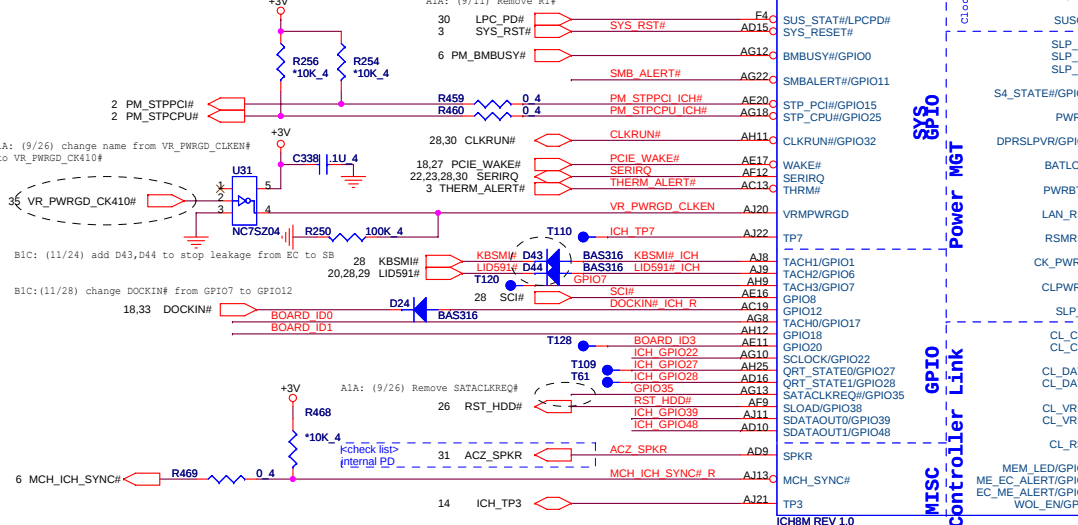


SB-PCI



SB-GPIO

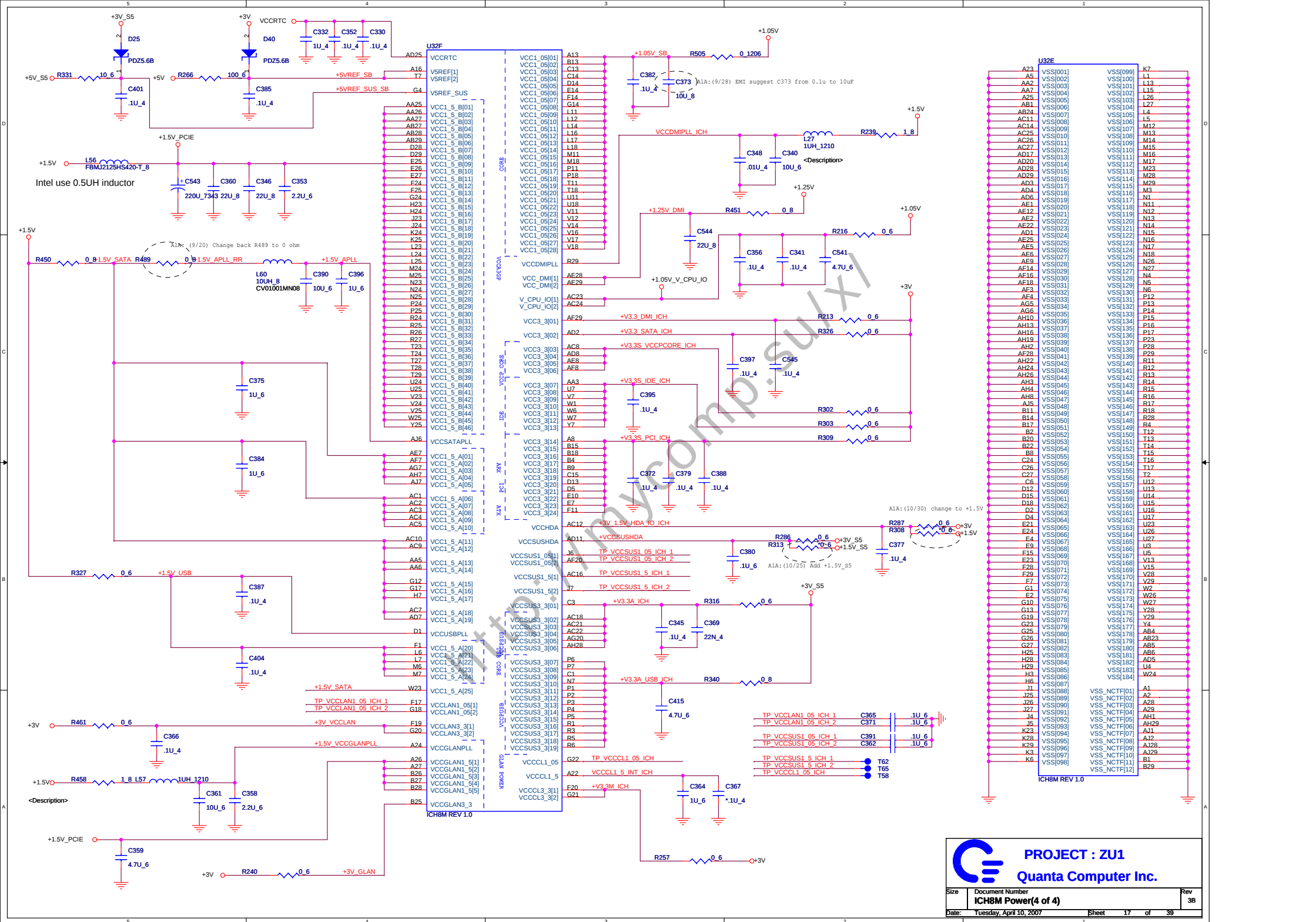
D3A: (1/31) ASP issue: when iAMT is not implemented, ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474, R475 for debug use)
A1A: (9/29) no support iAMT, remove SMB_CLK_ME, SMB_DATA_ME



No Reboot strap

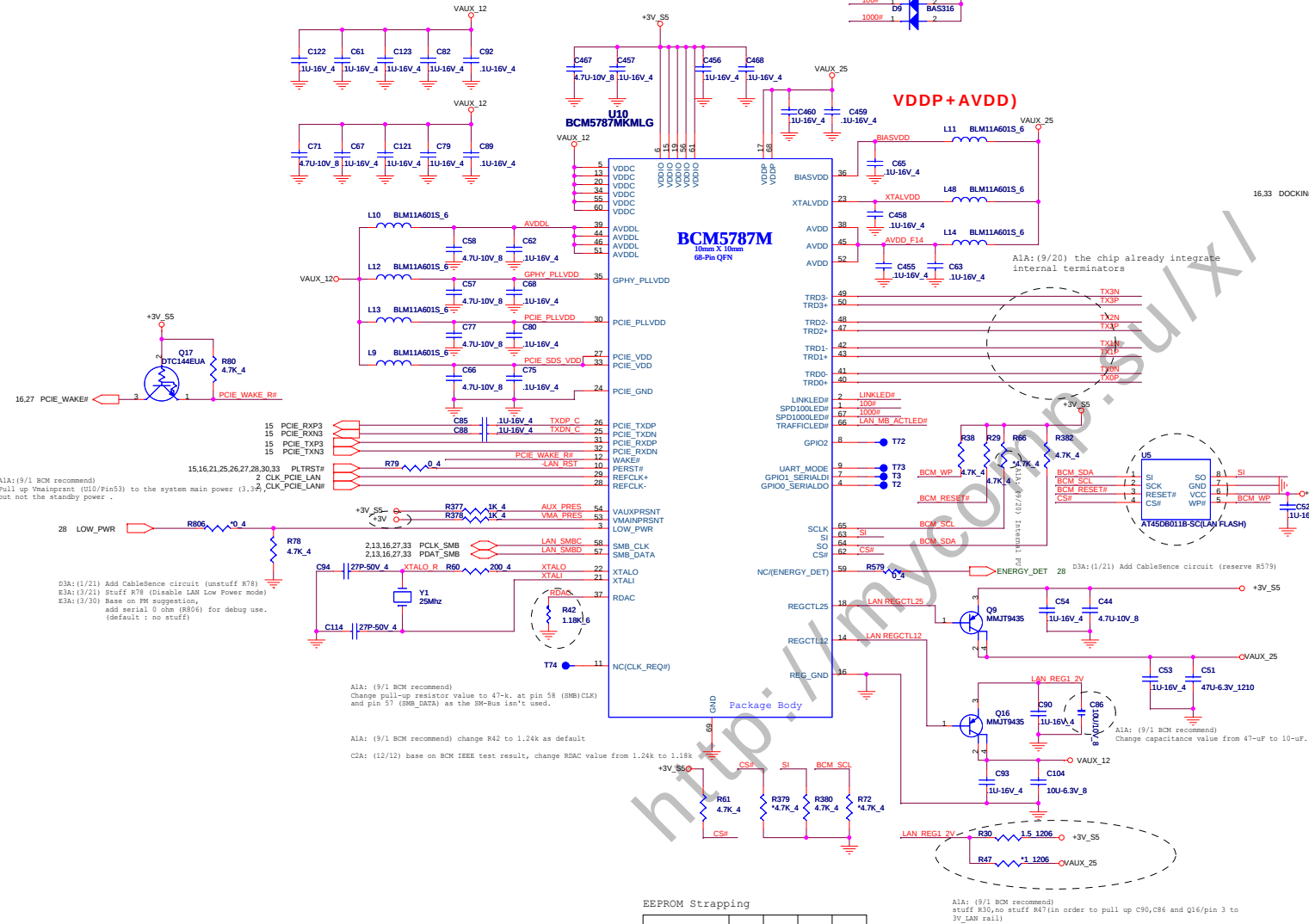
HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

Board ID	ID3	ID2	ID1	ID0
With EZ Dock	0	0	0	0
W/O EZ Dock	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

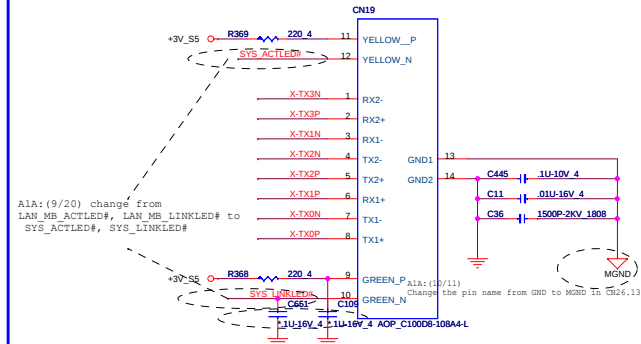
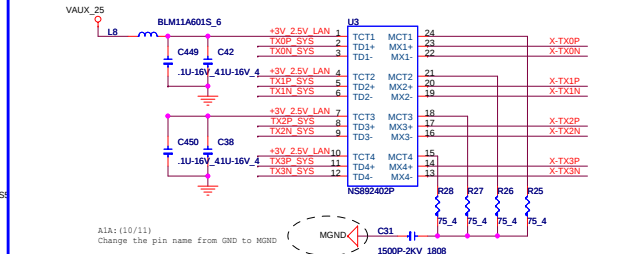
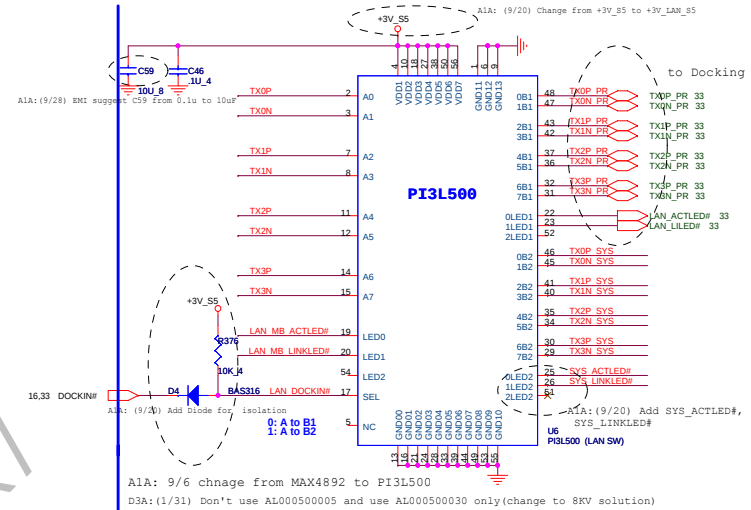


Giga LAN BCM5787M

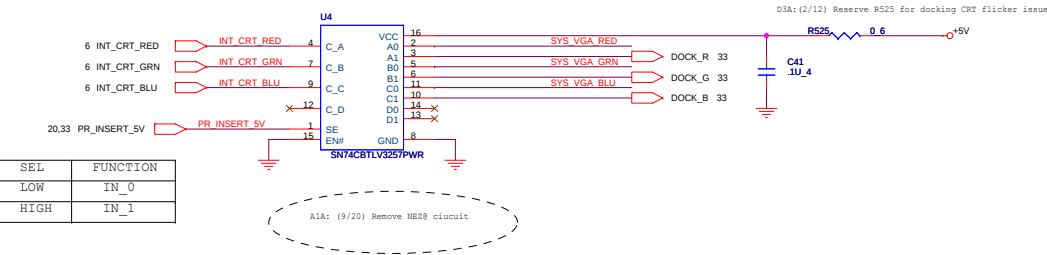
A1A: (9/27) Change +3V_LAN_S5 to +3V_S5



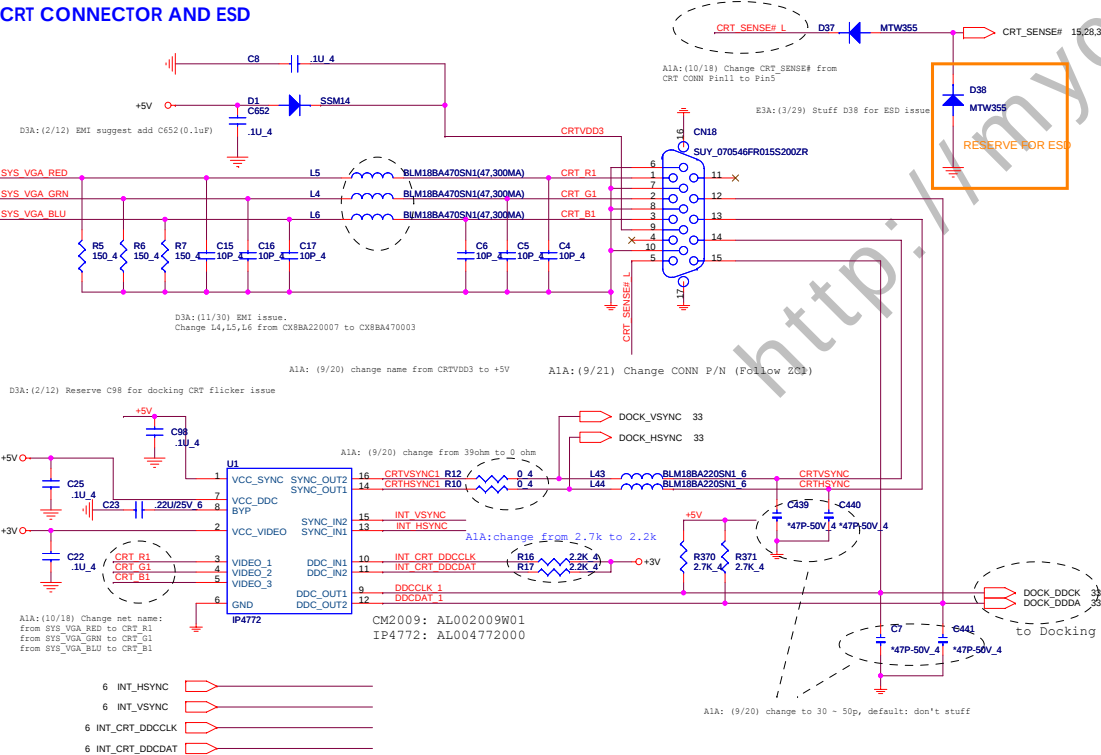
EEPROM Strapping				
	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

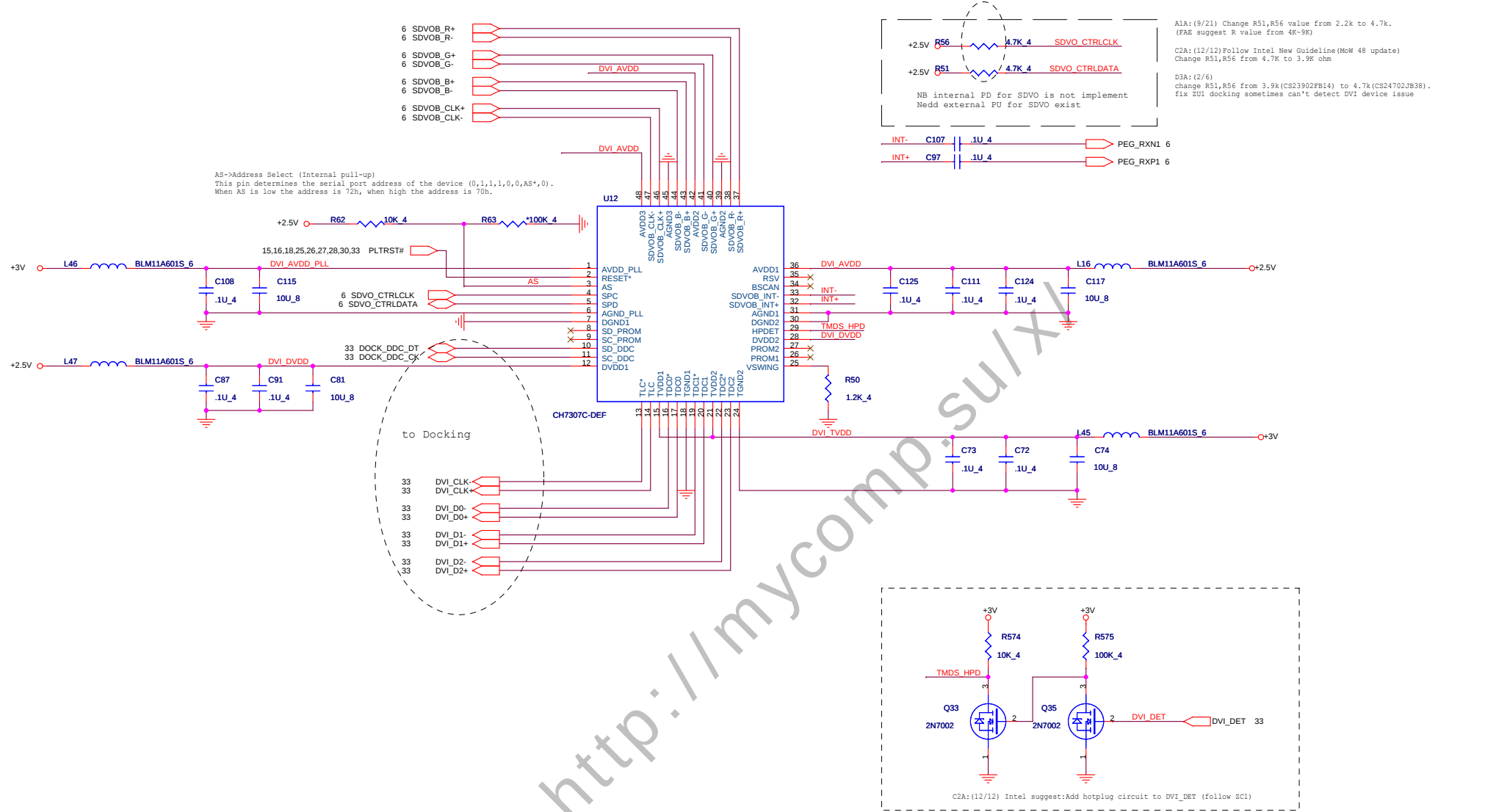


CRT Select



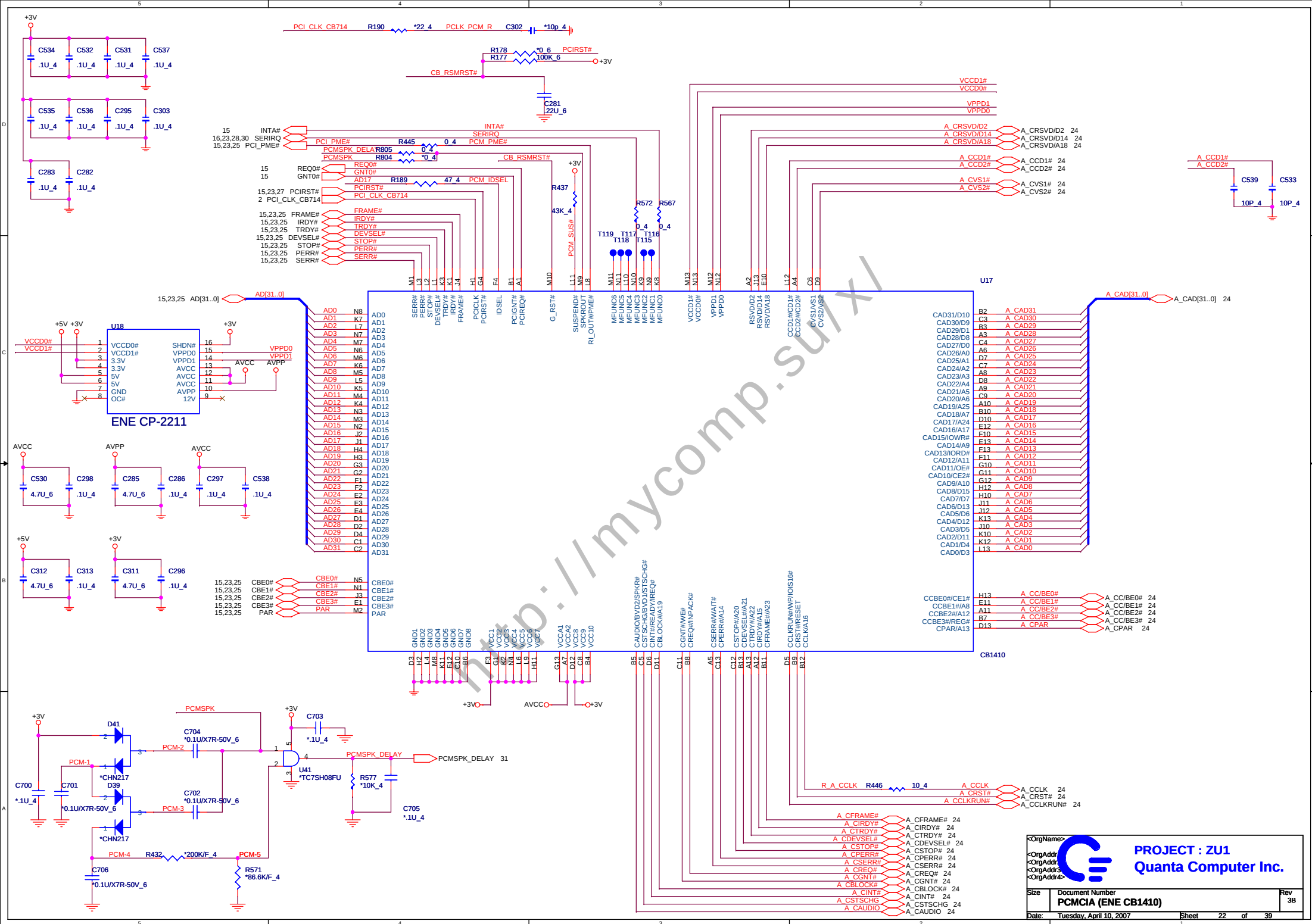
CRT CONNECTOR AND ESD

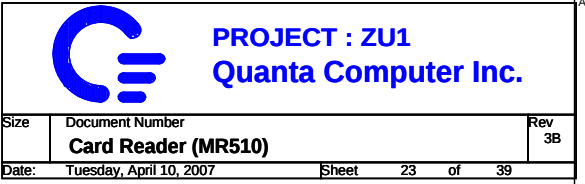




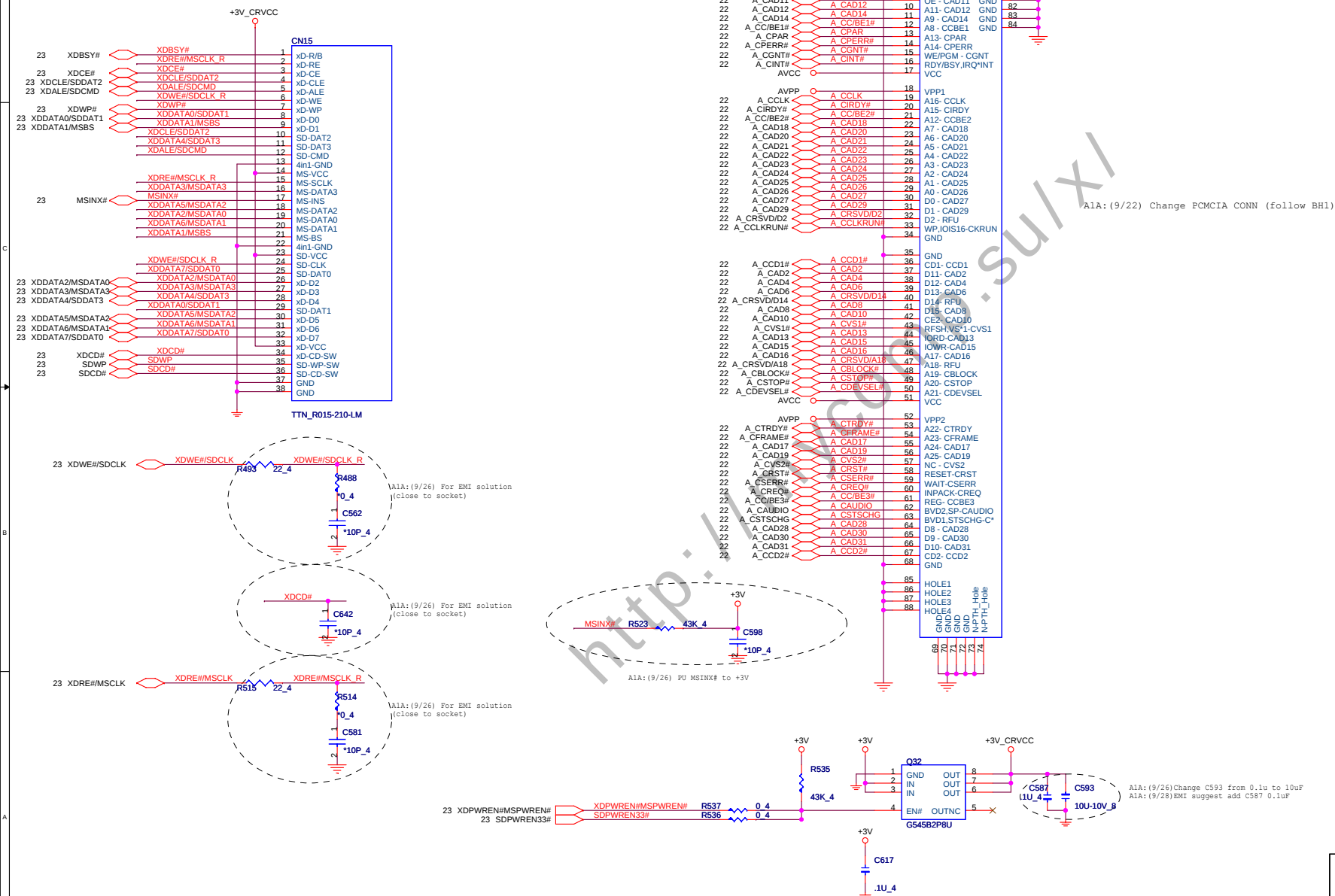
D3A: (1/30) remove U13, R68, R75, R73, C98
1/16 confirm with CHRONTEL FAE,
he said we can remove CH9901 (U13),
if ZU1 need support HDCP,
just need change controller from CH7307 to CH7313.
CH7313 already integrated HDCP function, no need external EEPROM.

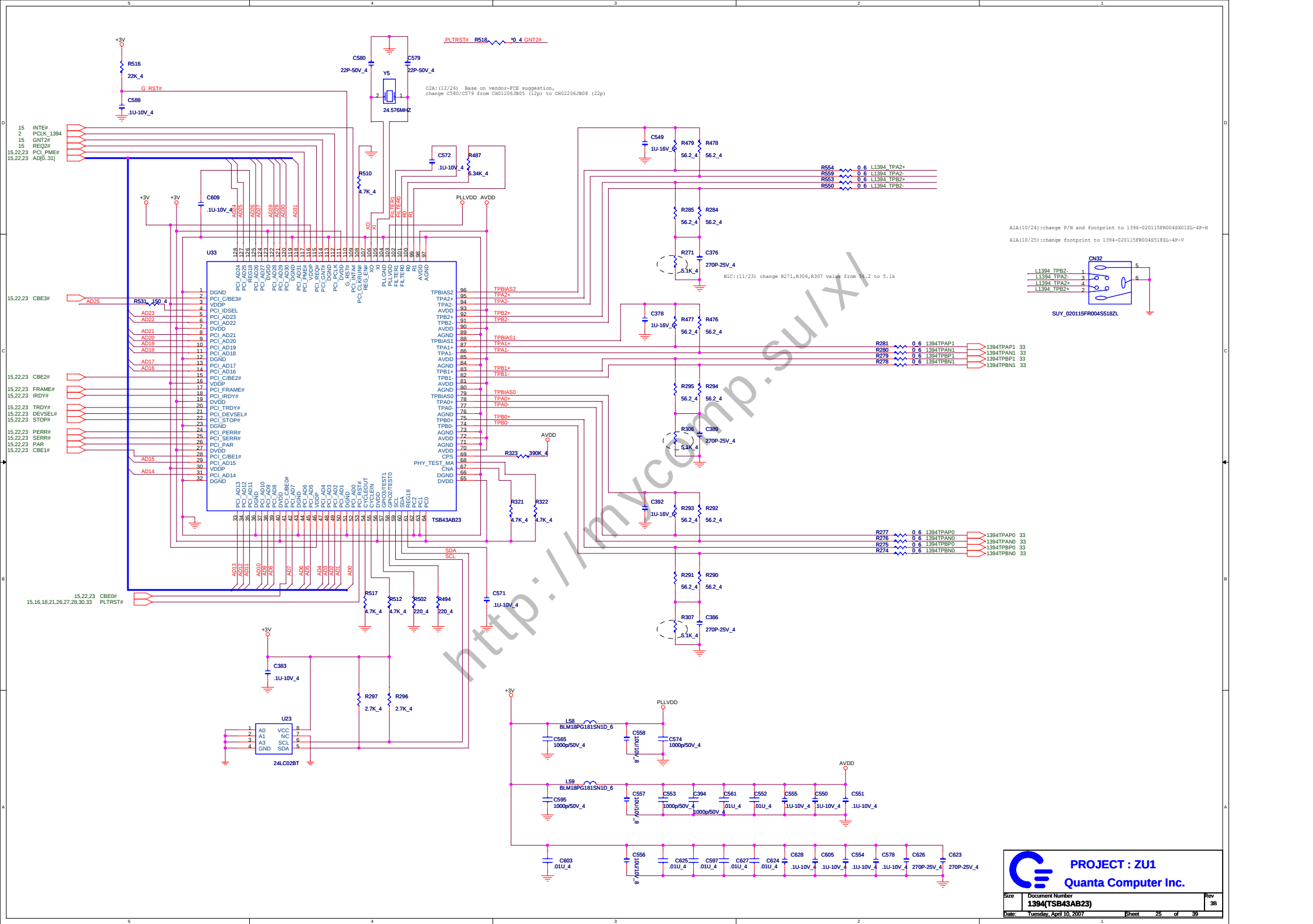
C2A: (12/22) confirm with FAE ->
Due to Intel VBIOS already integrate the EEPROM function.
ZU1 will remove the U11, R57, R52, C109 to save layout space.



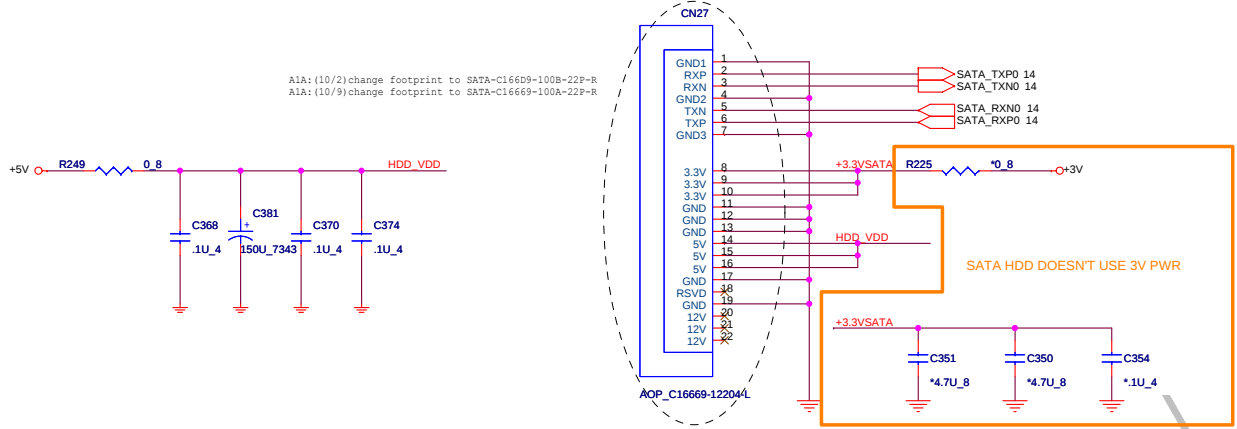


Main Source:TTN DFHD36MR000
2nd Source:NorthStar DFHS36FR003

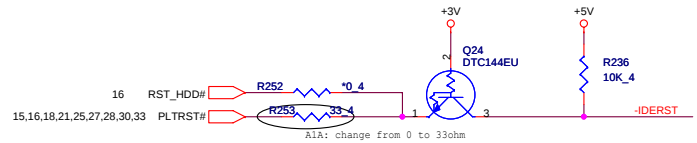




SATA HDD

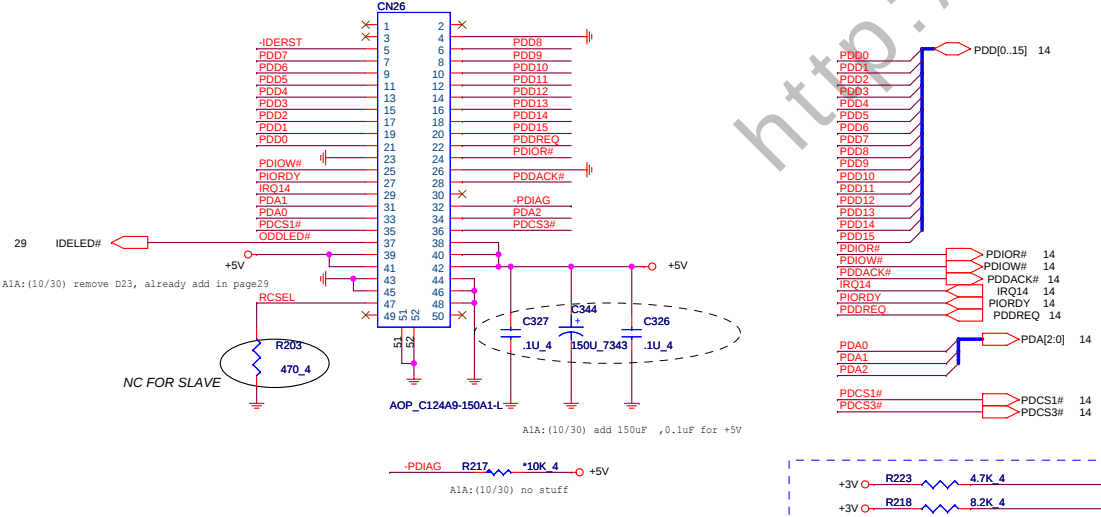


PATA ODD

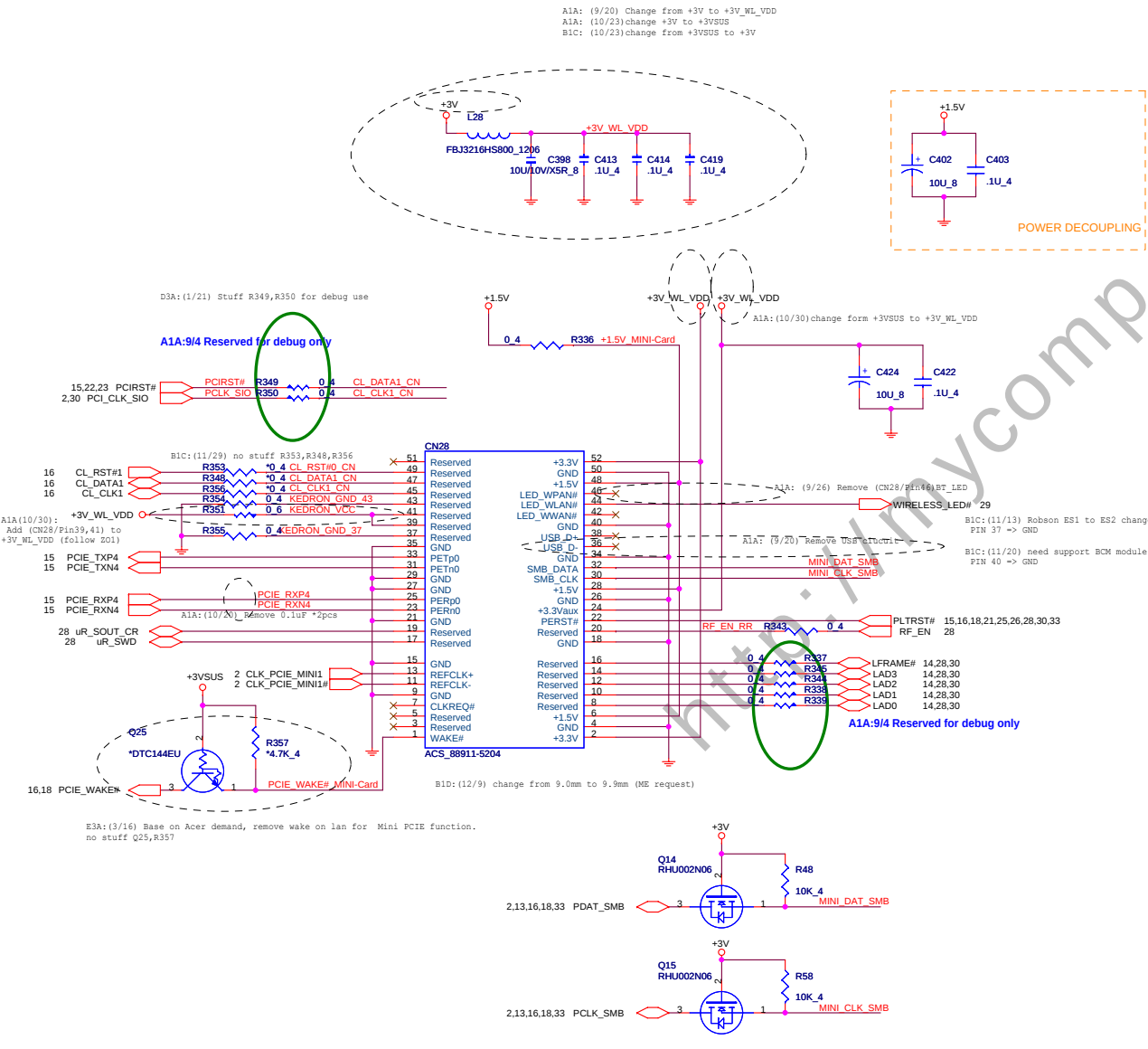


A1A: (9/29) change footprint: CDR-C124A9-100C-50P

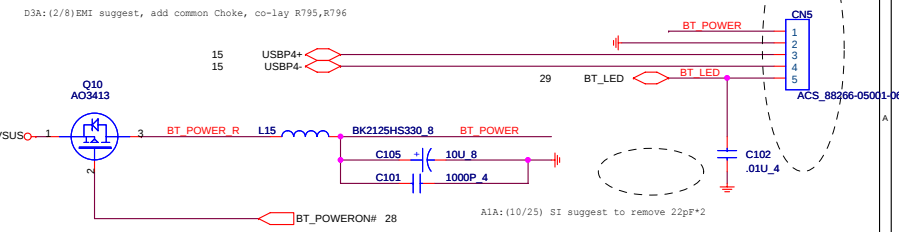
ODD Connector



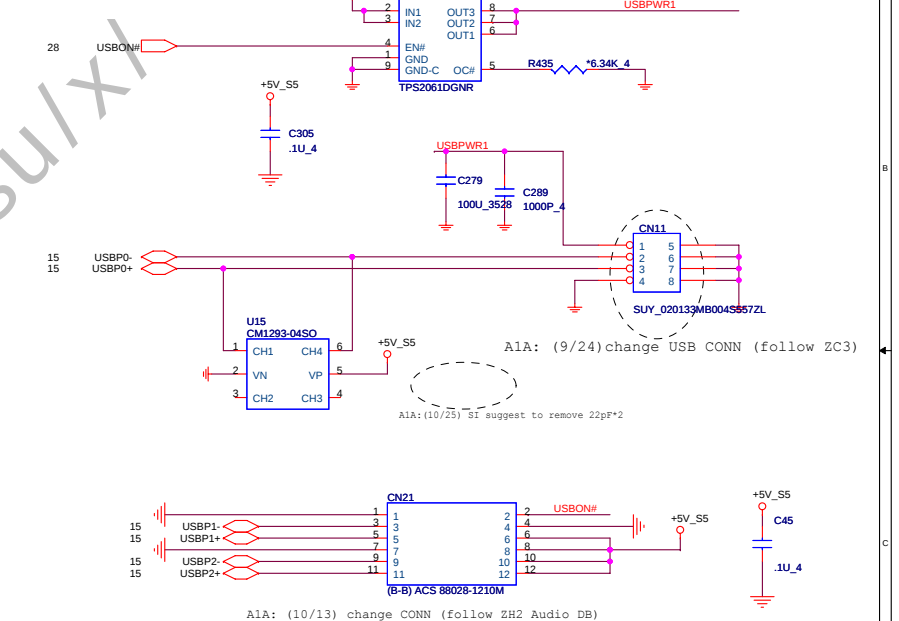
MINI-Card



BLUETOOTH MODULE CONNECTOR



USB CONN



A1A: (9/16) Change from WPC8769 to WPC8763

A1A: (9/25) place the above capacitors as close to the pins as possible

PCCLK_591
R142
22_4
C240
10P_4

08/10 FAE: SMI DOESN'T NEED DIODE

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

+5V
RP23
4.7KX4
33 PR_KB_CLK
33 PR_KB_DATA
33 PR_MS_CLK
33 PR_MS_DATA

A1A: (9/25)
FAE: PUT Y6 WITH EC IN THE SAME SIDE

A1A: (9/27) change C130, C131 from 6.8p to 5.6p

C2A: (12/26) Base on vendor-FCE suggestion,
change C130/C131 from CH-56067B01 (5.6p) to CH01006J501 (10p)

A1A: (9/26) Add HWPQ_CU103

C2A: (12/25) Steven: D16 not necessary if 3V/5V fail, EC can't work.
This monitor circuit is necessary.

E3A: (3/16) PE request move D15-D18 location for FFC cable issue. Remove D16 footprint and net (HWPQ_3/5VPCU) to save layout space.

+3VPCU
A1A: (9/25) change VBAT from +3VPCU to +A3VPCU
+A3VPCU
VDD must power up after VCC/AVCC
1/13 Confirm by vendor mail:
VBAT for keep PLL power let power up can quick
If no VBAT will switch to VCC power.
If PLL no power will cause boot time delay.

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SM BUS PU

+3VPCU
MBCLK R98 4.7K_4
MBDATA R99 4.7K_4
2ND_MBCLK R102 4.7K_4
2ND_MBDATA R100 4.7K_4
+3V
EC_GPIO42 R139 4.7K_4
CRT_SENSE# R398 4.7K_4

I/O ADDRESS SETTING

I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 CCD_POWERON# R408 10K_4
BADDR1 SOUT_CR_DEBUG R407 10K_4
SHBM RF_EN R399 10K_4

1/13 Confirm by vendor mail:
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ACER ID

A1A: (9/29) change from MBCLK/MDATA to 2ND_MBCLK/2ND_MBDATA
U7
SCL A0 1
SDA A1 2
2ND_MBCLK 6
2ND_MBDATA 5
WP VCC 8
GND 4
C69 10U_4

SPI FLASH

+3VPCU
R45 10K_4
SPI_SDI uR 2
SPI_SDO uR 5
SPI_SCK uR 6
SPI_CS# uR 1
U26 W25X80VSSIG
VDD 8
HOLD 7
WP 3
VSS 4

1/13 Confirm by vendor mail:
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX

MX0 29
MX1 29
MX2 29
MX3 29
MX4 29
MX5 29
MY16 29

DEBUG PORTS

EC Debug Port

+3VPCU
SOUT_CR_DEBUG 1
SWD_DEBUG 2
3
4
*ACS_88231-04001

LPC debug card

A1A(10/5): Change LPC debug CONN to DFPC10FR103
E3A: (3/22) confirm with BIOS-CM, no need LPC debug CONN,
Remove CM6, R432 footprint to save space for layout.

INTERNAL KEYBOARD STRIP SET

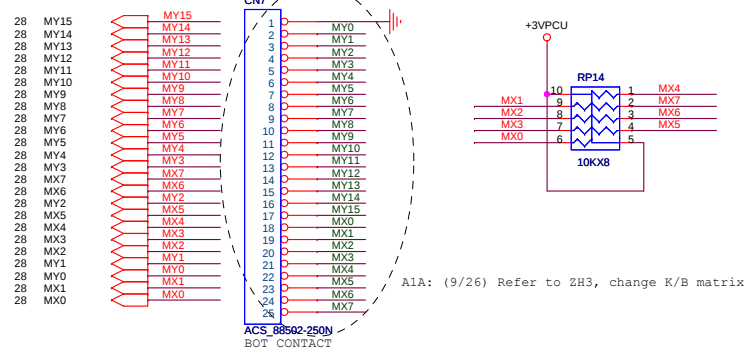
MY0 R110 10K_4
+3VPCU



PROJECT : ZU1
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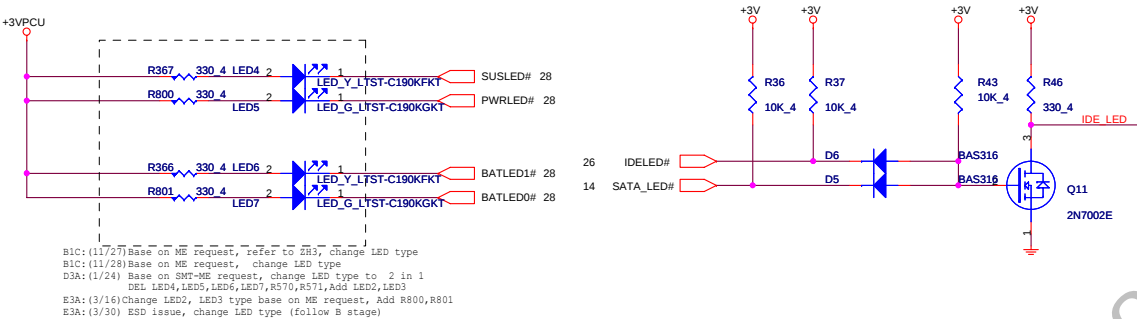
Size	Document Number	Rev
	EC (PC8763LDG)/ FLASH	3B
Date:	Tuesday, April 10, 2007	Sheet 28 of 39

INT K/B

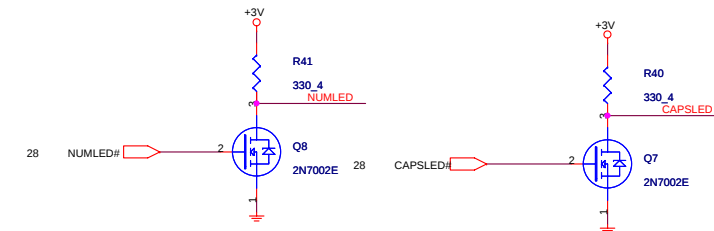


A1A: (9/26) Refer to ZH3, change K/B matrix

LED

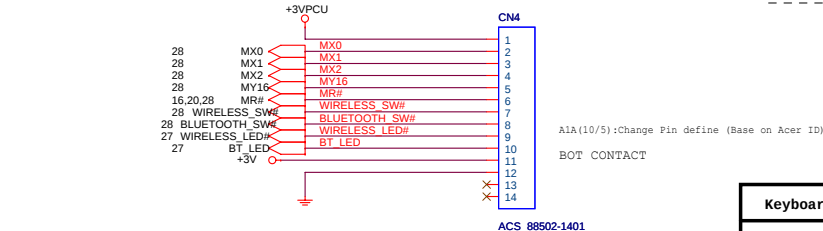


B1C: (11/27) Base on ME request, refer to ZH3, change LED type
B1C: (11/28) Base on ME request, change LED type
D3A: (1/24) Base on SMT-ME request, change LED type to 2 in 1
D3A: (1/24) LED4, LED5, LED6, LED7, R570, R571, Add LED2, LED3
E3A: (3/16) Change LED2, LED3 type base on ME request, Add R800, R801
E3A: (3/30) ESD issue, change LED type (follow B stage)



A1A: (10/30) no stuff (ZUI no support EMAIL LED)
E3A: (3/30) Remove Q27, R1 footprint to save space for layout
ZUI no support E-Mail LED

Function Board

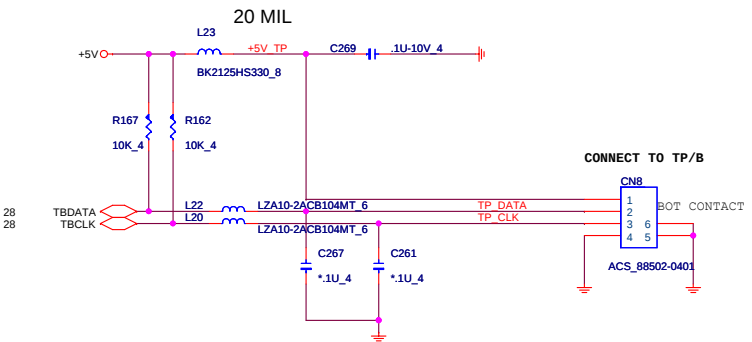


A1A: (9/27) Add Function Board CONN (14pin)

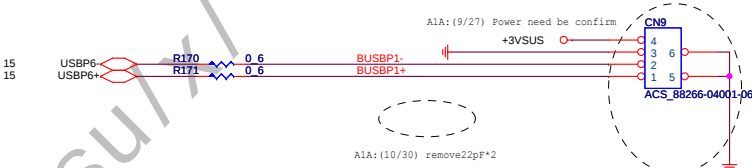
A1A: (10/30) add +3V for Daughter Board use

Keyboard Matrix	Button
MX0/MY16	acer EAP Button
MX1/MY16	acer EMAIL Button
MX2/MY16	acer WWW Button
MX3/MY16	acer EPM Button
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

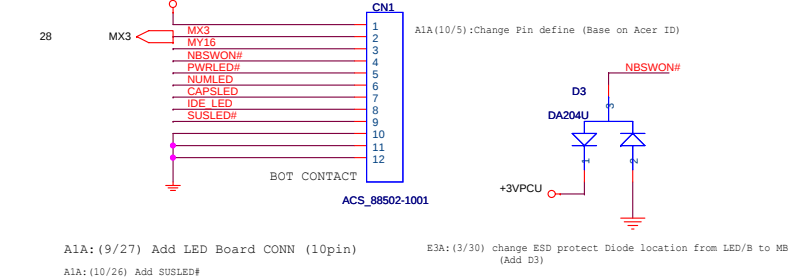
TOUCH PAD



Finger Printer



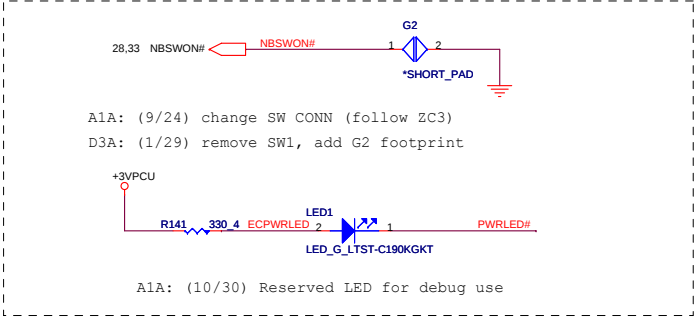
LED Board



A1A: (9/27) Add LED Board CONN (10pin)

A1A: (10/26) Add SUSLED#

E3A: (3/30) change ESD protect Diode location from LED/B to MB (Add D3)

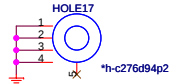


A1A: (9/24) change SW CONN (follow ZC3)

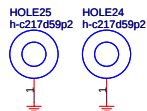
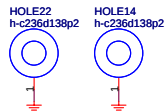
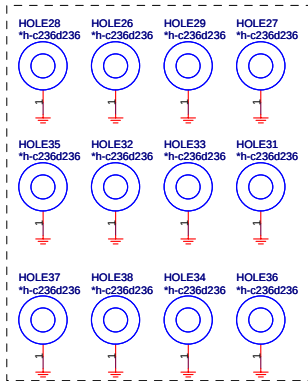
D3A: (1/29) remove SW1, add G2 footprint

A1A: (10/30) Reserved LED for debug use





HOLE



HOLE16
 h-c217d122p2

HOLE19
 h-c217d122p2

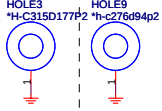
HOLE30
 h-c217d122p2

HOLE18
 h-c217d122p2

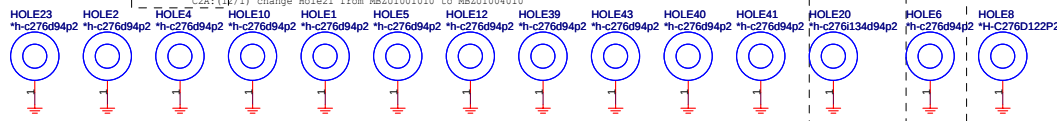
HOLE15
 h-c217d122p2

HOLE21
 h-c217d122p2

HOLE11
 h-c217d122p2



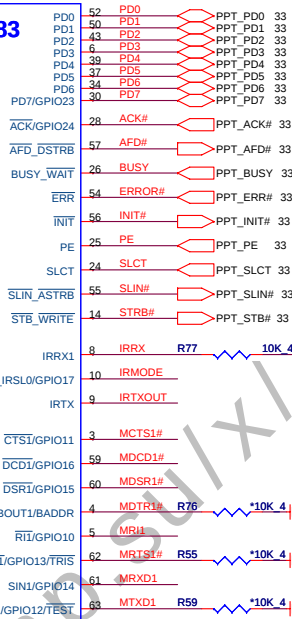
C2A: (1p/1) change Hole21 from MBZU1001010 to MBZU1004010



U9

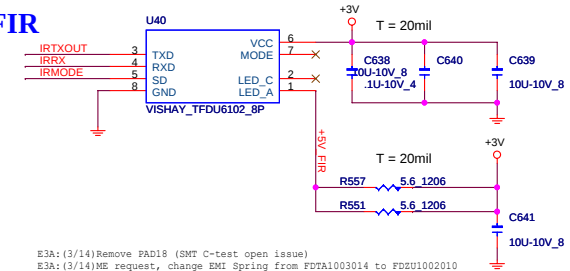
2	LAD0
5	LAD1
1	LAD2

NS PC87383

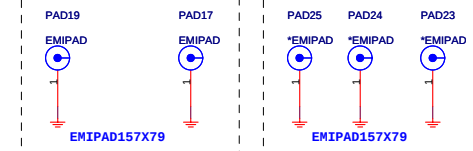


OPEN : normal Device operation
LOW : XOR pin tree

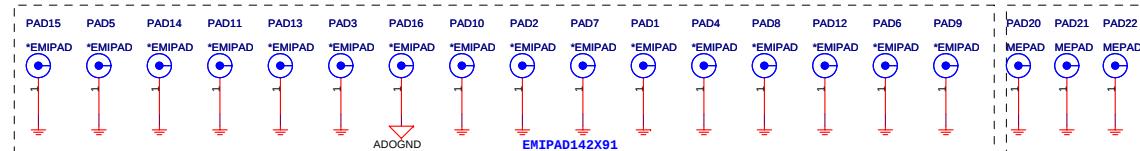
FIR



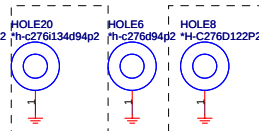
PAD19	PAD17	PAD25	PAD24	PAD23
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ESDPad



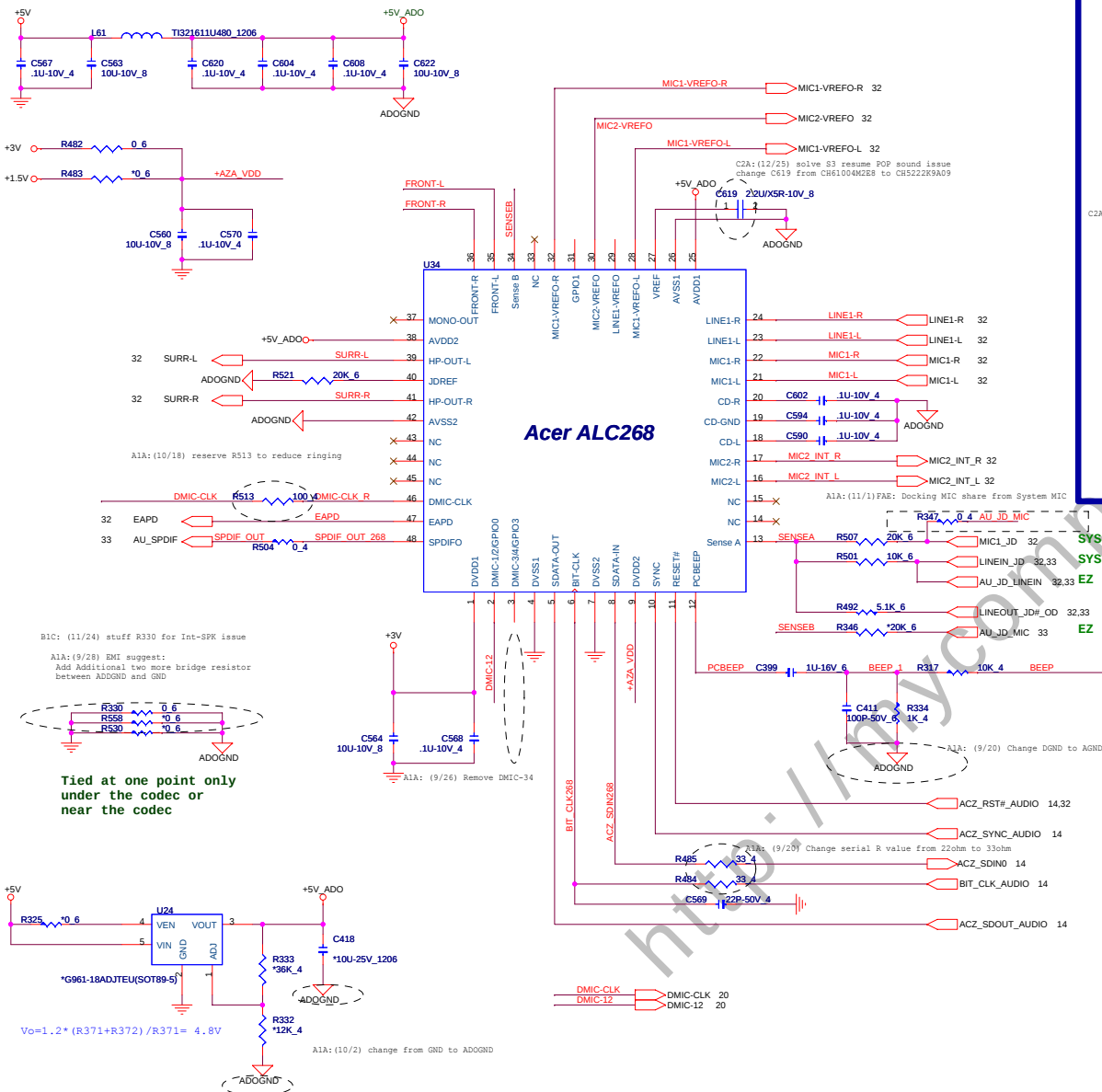
ADOGND EMIPAD142X91



PROJECT : ZU1
Quanta Computer Inc.

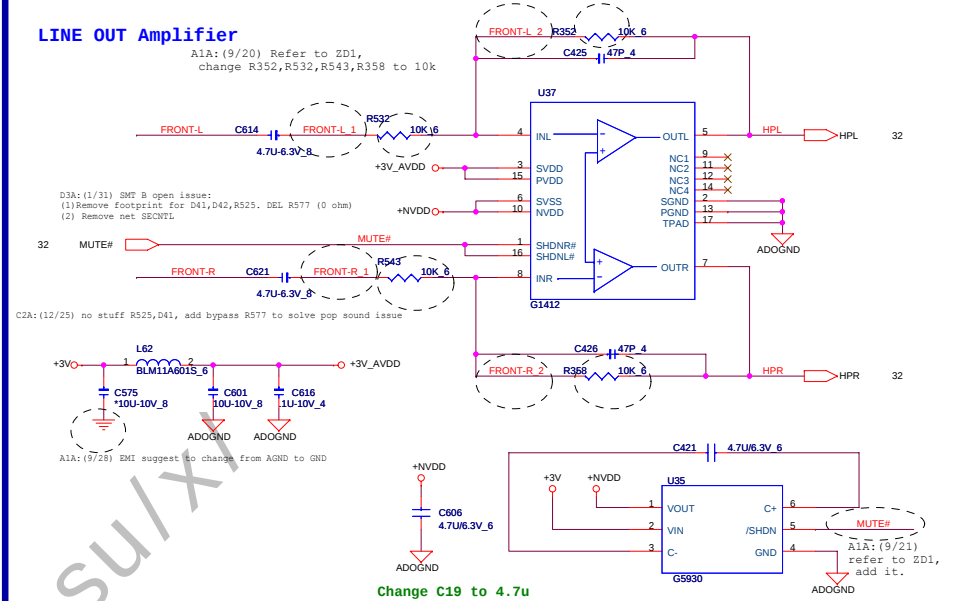
Size	Document Number SUPER-10/FIR/HOLE	Rev 3B
Date:	Tuesday, April 10, 2007	Sheet 30 of 39

CODEC (ALC268)

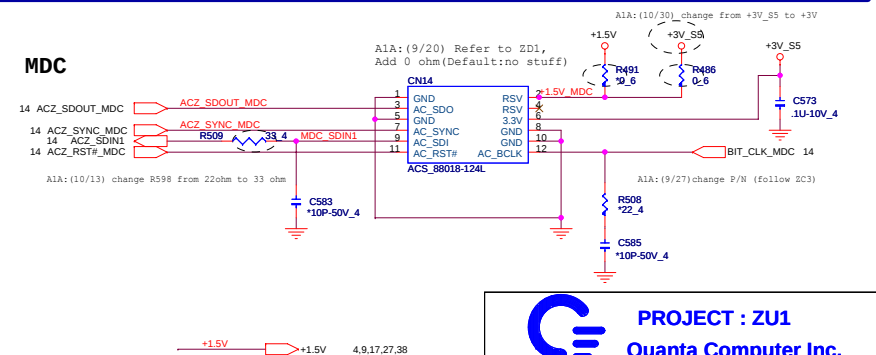


LINE OUT Amplifier

A1A: (9/20) Refer to ZD1,
change R352,R532,R543,R358 to 10k



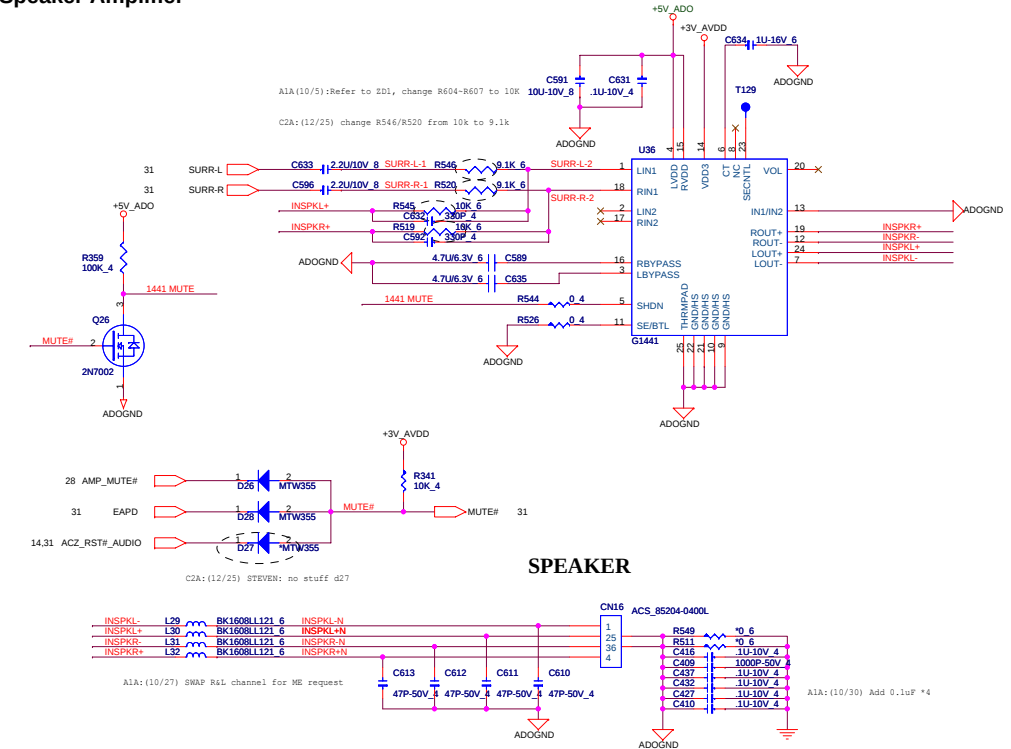
MDC



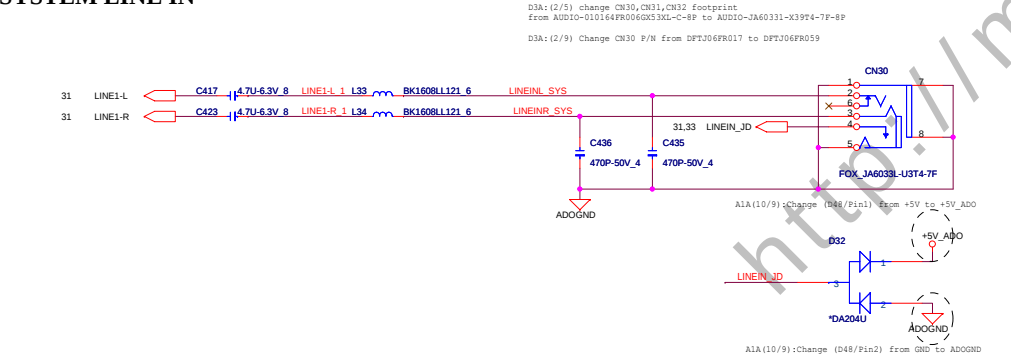
PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number AUDIO(ALC268)/AMP/MDC	Rev 3B
Date:	Tuesday, April 10, 2007	Sheet 31 of 39

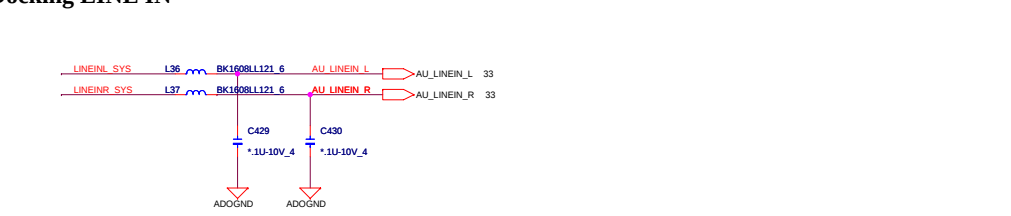
Speaker Amplifier



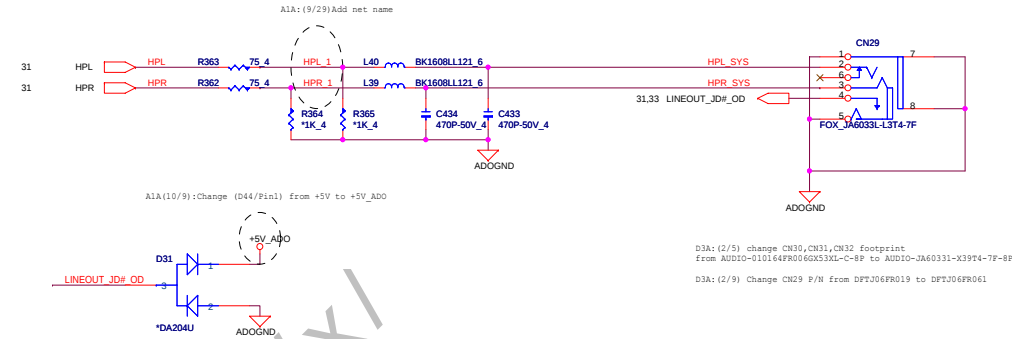
SYSTEM LINE IN



Docking LINE IN



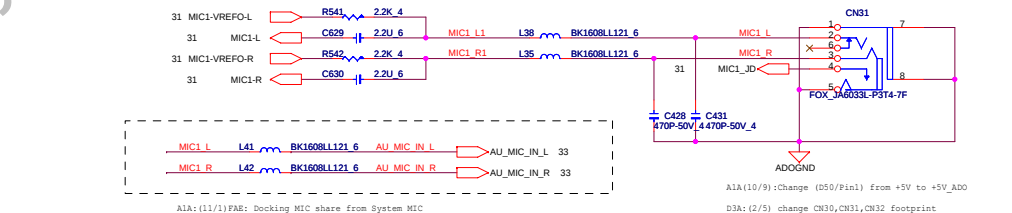
SYSTEM LINE OUT



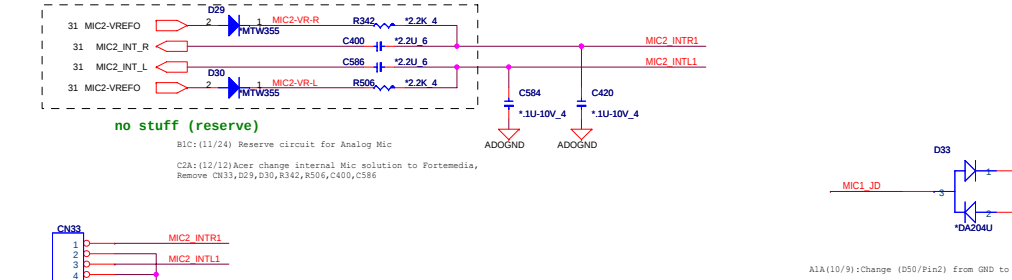
Docking LINE OUT/SPDIF

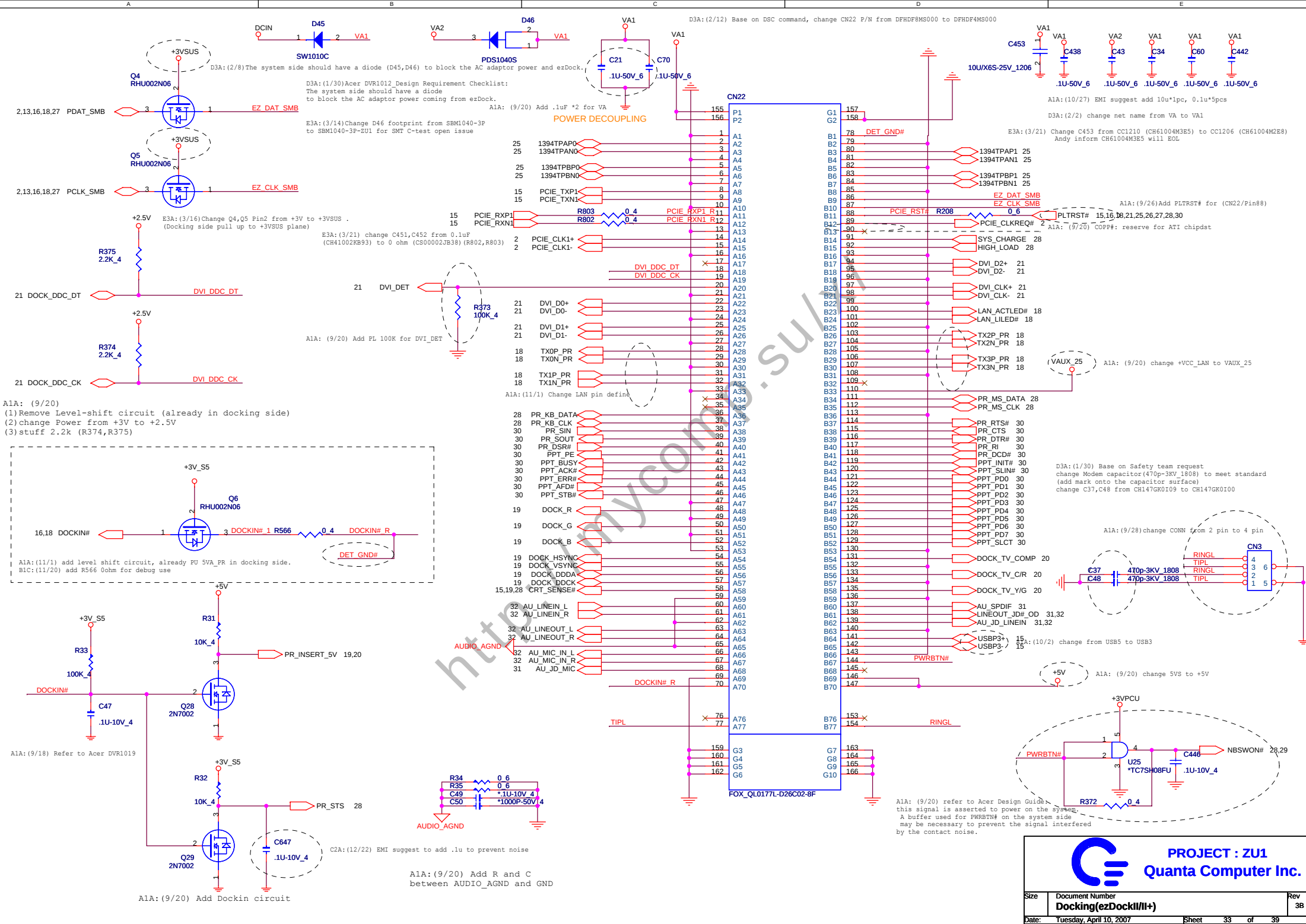


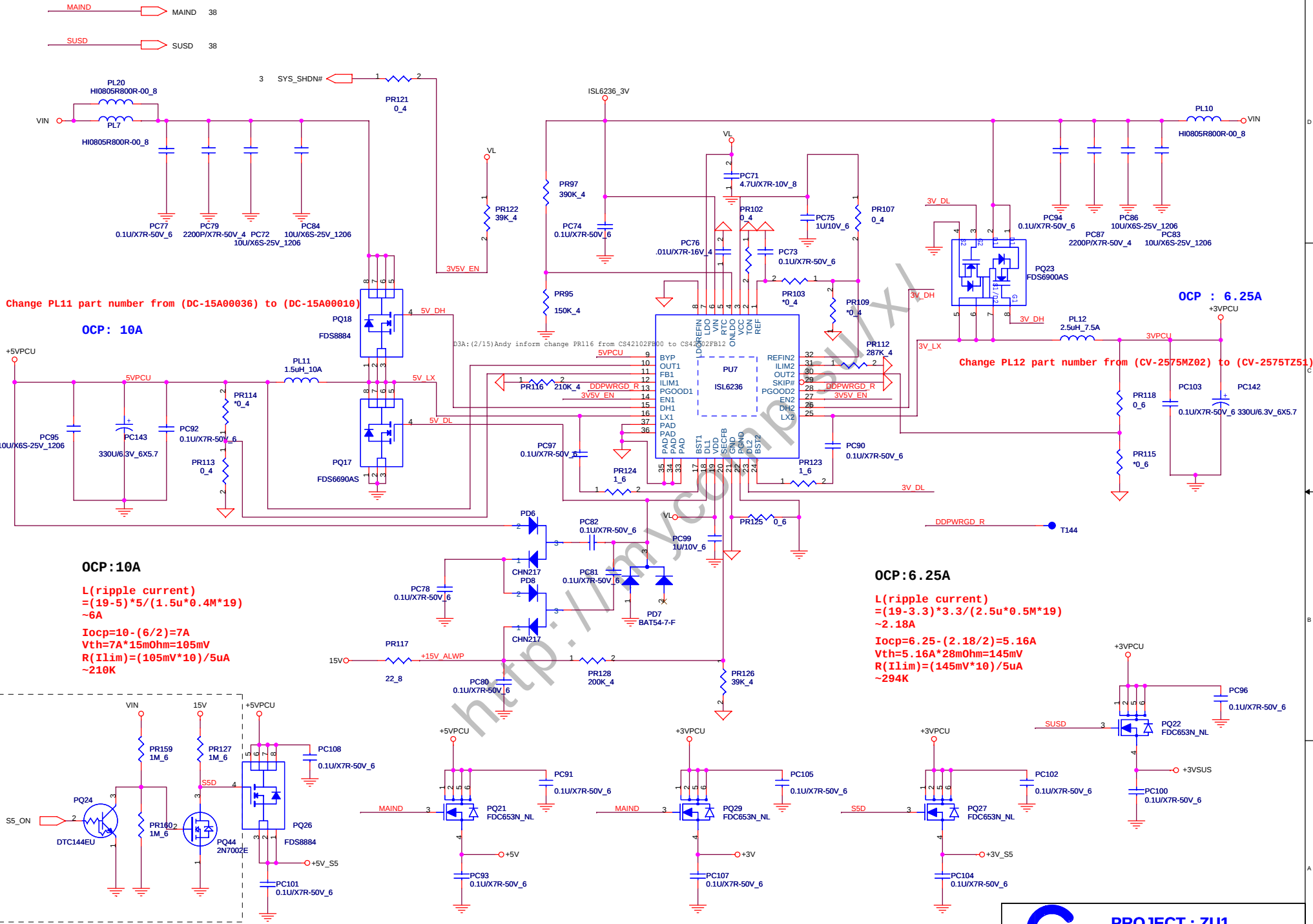
SYSTEM MIC



Analog MIC







Change PL11 part number from (DC-15A00036) to (DC-15A00010)

OCP: 10A

OCP: 10A

$L(\text{ripple current}) = (19-5) * 5 / (1.5u * 0.4M * 19) \sim 6A$
 $I_{ocp} = 10 - (6/2) = 7A$
 $V_{th} = 7A * 15m\Omega = 105mV$
 $R(I_{lim}) = (105mV * 10) / 5uA \sim 210K$

OCP: 6.25A

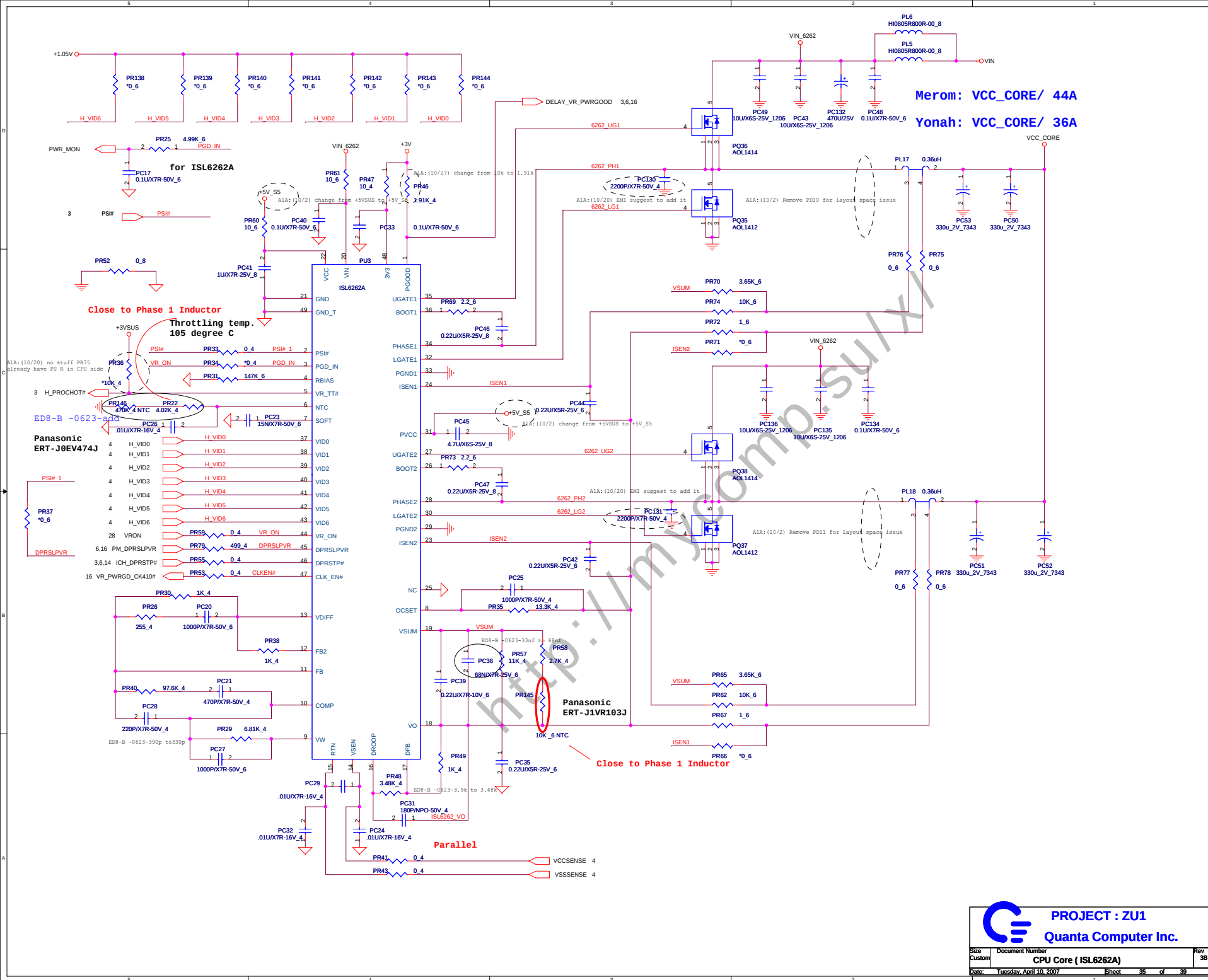
$L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5u * 0.5M * 19) \sim 2.18A$
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$
 $V_{th} = 5.16A * 28m\Omega = 145mV$
 $R(I_{lim}) = (145mV * 10) / 5uA \sim 294K$

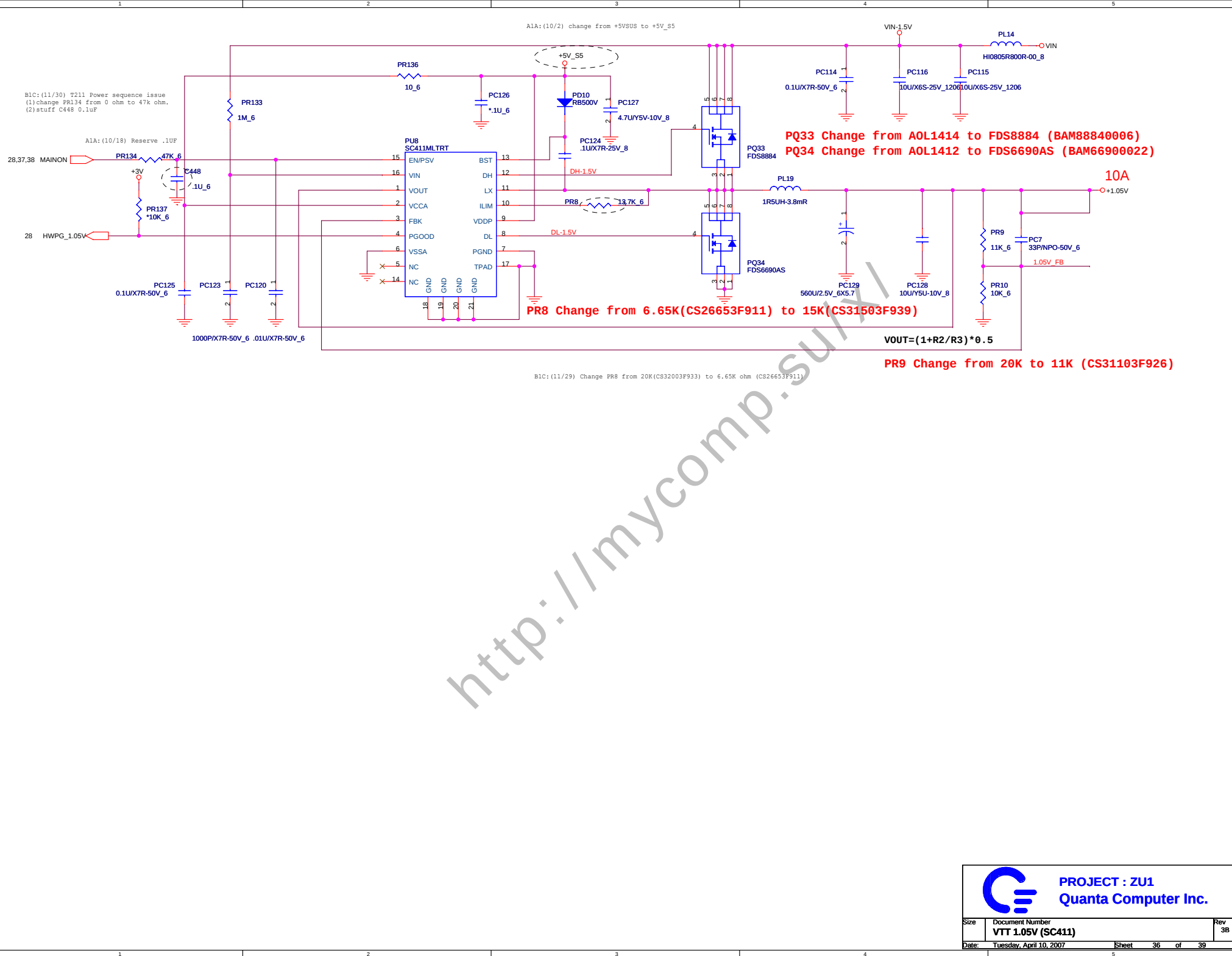
C2A: (12/10) change S5_ON control circuit

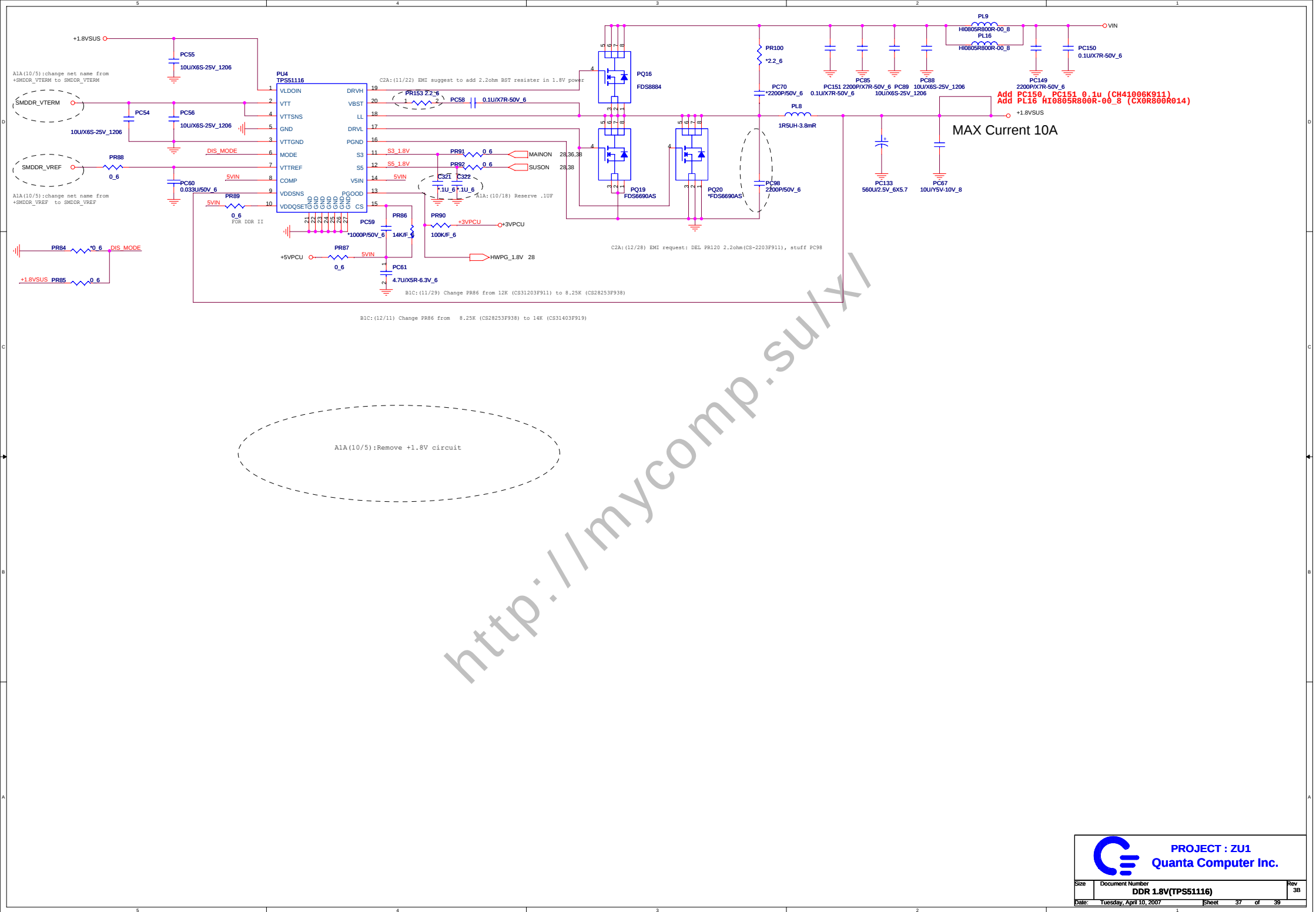
B1C: (11/29) change PQ26 from FDS6690AS (BAM6690022) to FDS8884 (BAM8884006)

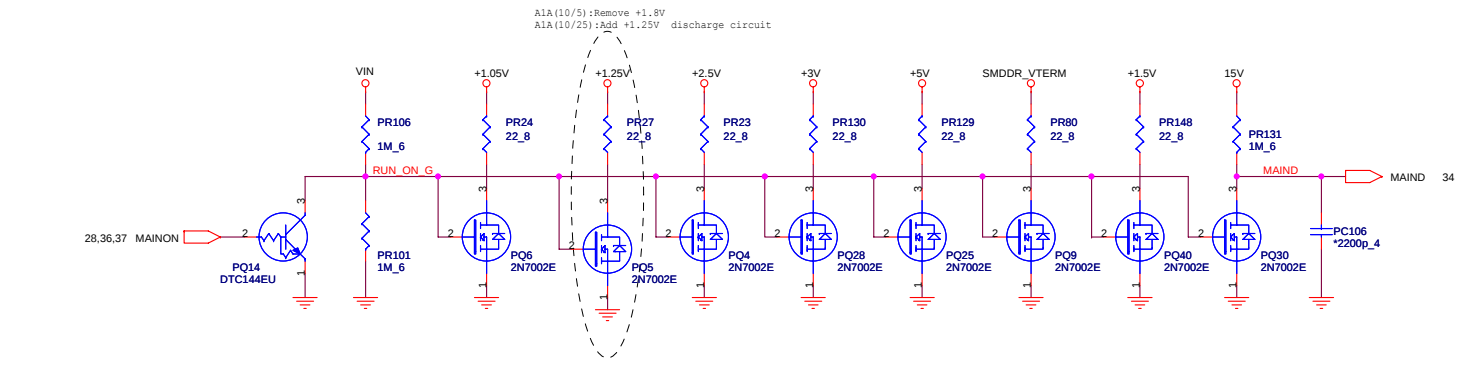
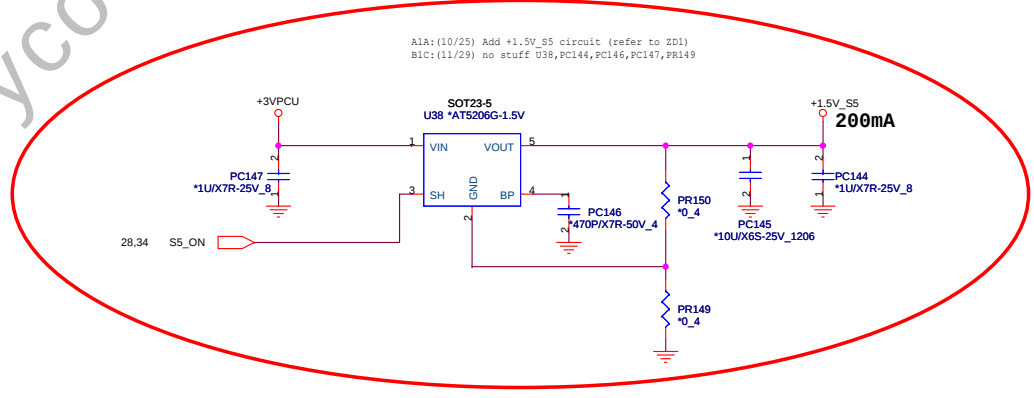
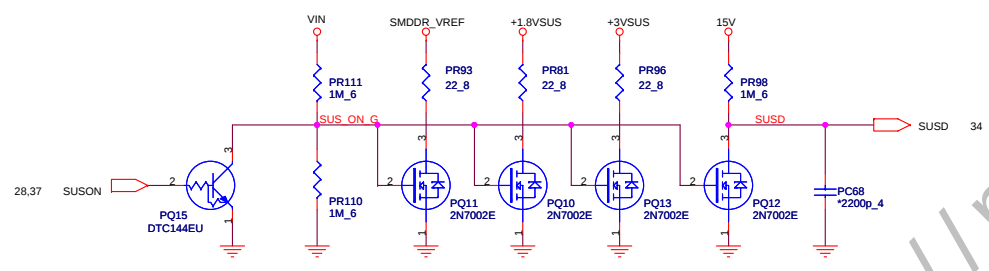
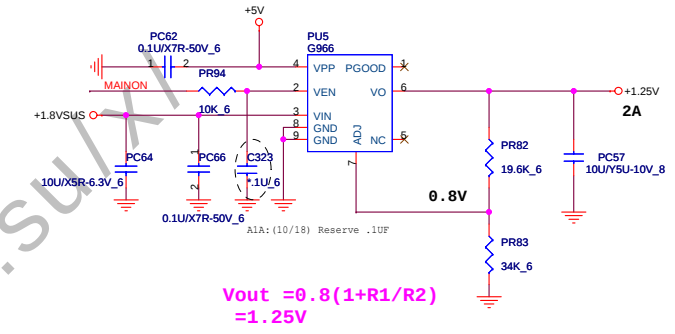
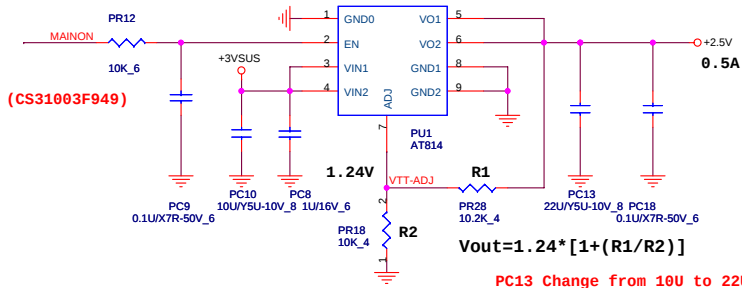
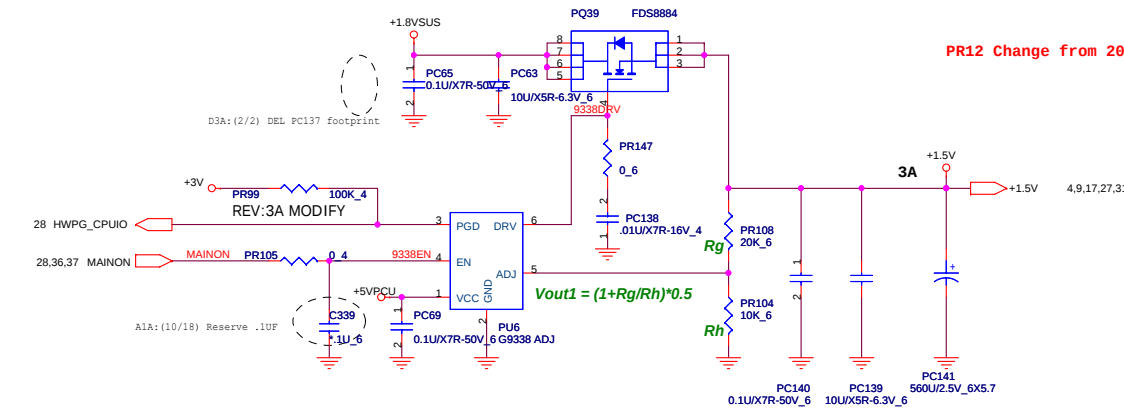
**PROJECT : ZU1**
Quanta Computer Inc.
SYSTEM 5V/3V (ISL6236)

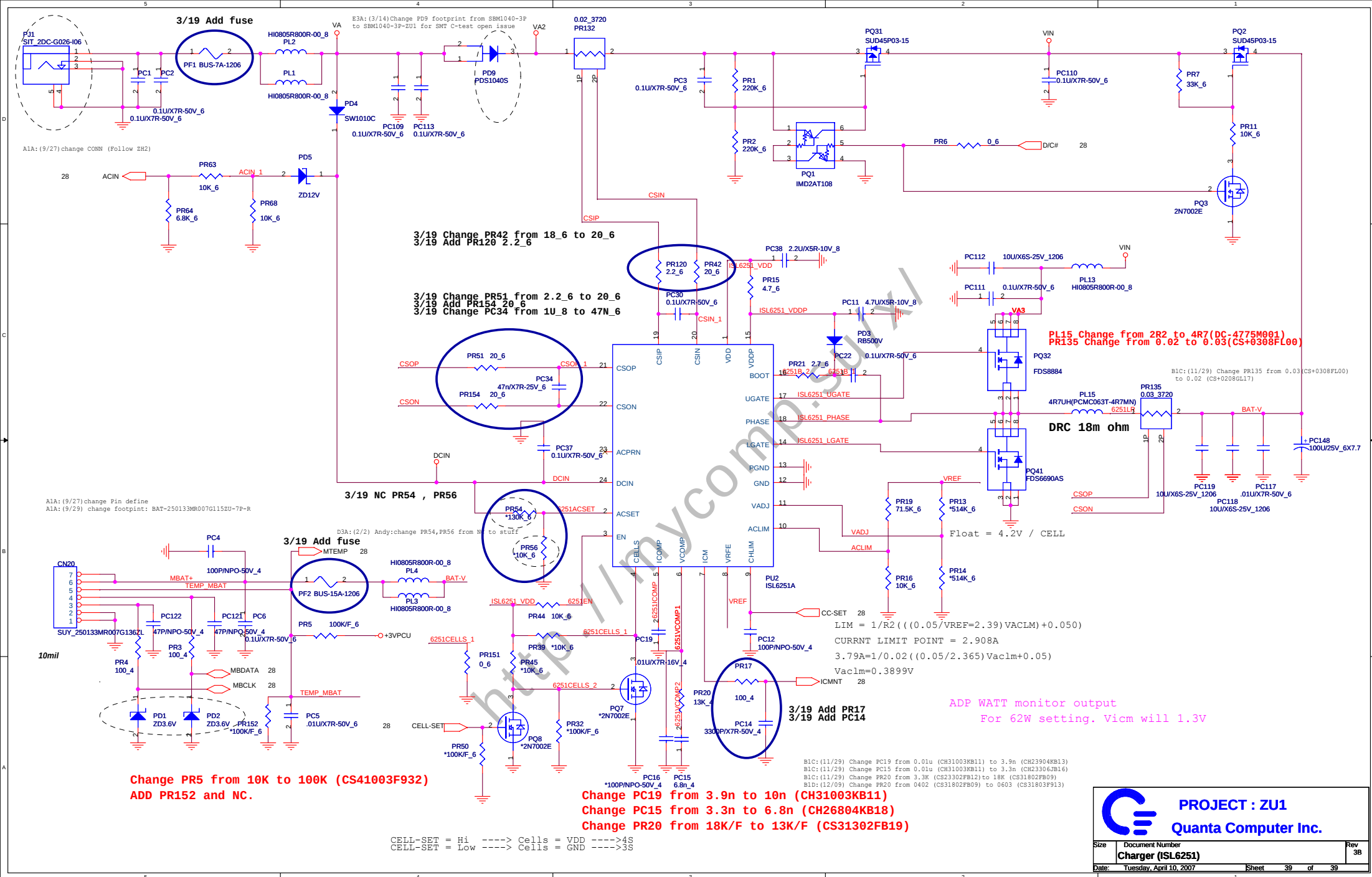
Size	Document Number	Rev
		3B
Date:	Tuesday, April 10, 2007	Sheet 34 of 39

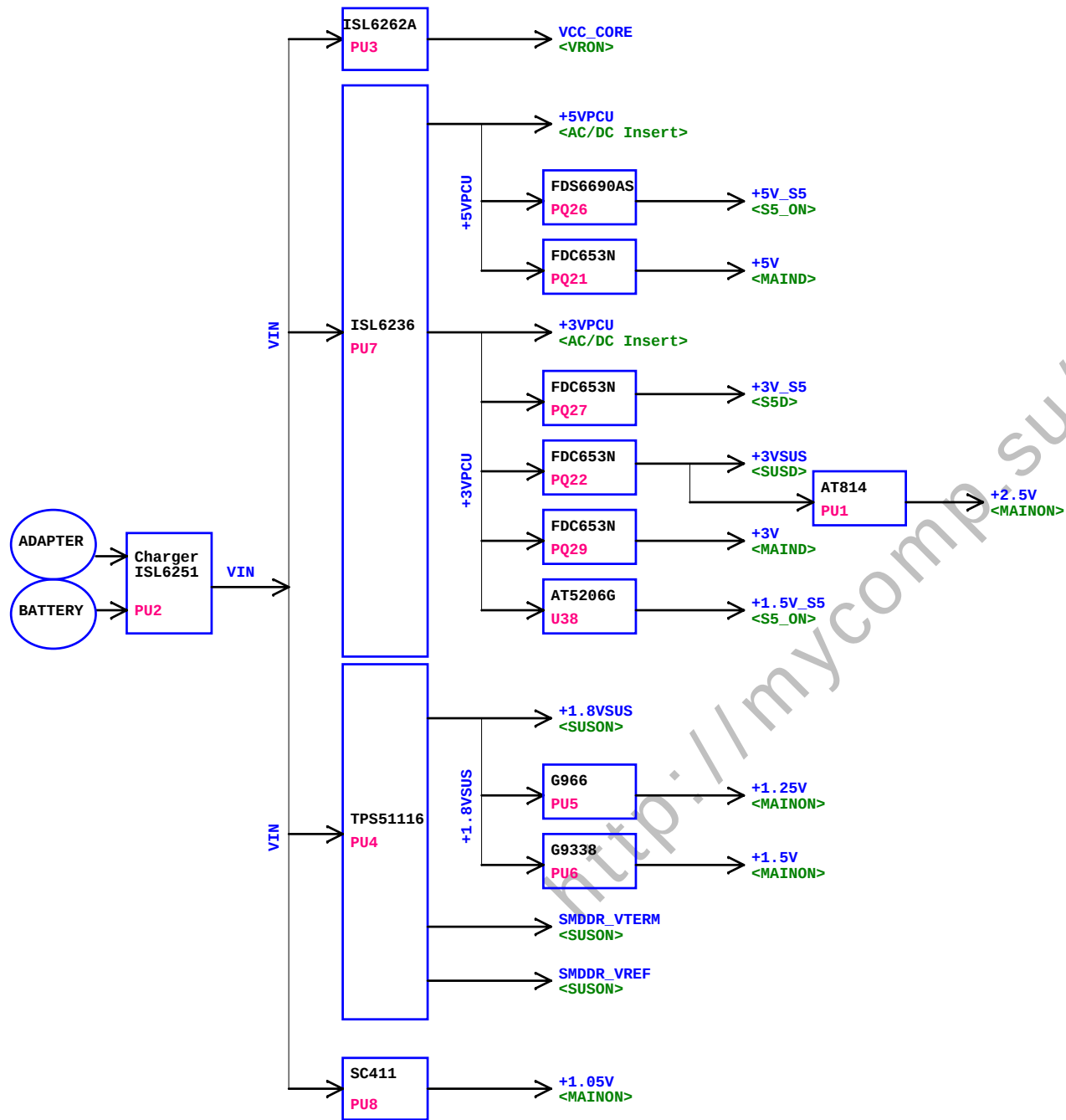












ZU1 Power Table

ZU1 Power Sequence

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page		
1	CPU Clock select issue	Stuff R179,R198,R447 for CPU Clock select issue	A1A	2		
2	PCI Clock issue	change R186 value from 33ohm to 22 ohm (refer to Intel check list 1.301)	A1A	2		
3	CK505 issue	ICS FAE suggest to change C542,C287 from 4.7u to 10u	A1A	2		
4	EMI issue	EMI suggest to reserve R436,R199,R444 for EMI test	A1A	2		
5	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2		
6	CK505 issue	SWAP SRC3 and SRC9	A1A	2		
7	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2		
8	CK505 issue	Remove U19/Pin48 (no use)	A1A	2		
9	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2		
10	CK505 issue	remove SATACLKREQ function, change R188 value from 475ohm to 22 ohm	A1A	2		
11	CK505 issue	FAE : (14M_ICH and SIO_14M) signals trace should be equal length	A1A	3		
12	CPU issue	Remove XDP/ITP signals (no use)	A1A	3		
13	CPU issue	Retain the termination resistors (R157,R150~R152) on these signals even when ITP700 not implemented.	A1A	3		
14	Thermal Trip issue	change Q19/Pin3 net name from THERM_SYS_PWR to SYS_SHDN#	A1A	3		
15	CPU FAN issue	change CPU FAN CONN (follow ZC3)	A1A	3		
16	CPU FAN issue	Add CPUFAN#_ON to (U28/PIN1)	A1A	3		
17	CPU FAN issue	Add Diode D39 and PU +5V for (U28/Pin1)	A1A	3		
18	CPU Thermal monitor issue	Add (U27/Pin6) PU to 3V	A1A	3		
19	CPU Thermal monitor issue	remove R389, already PU in ICH8	A1A	3		
20	CPU Thermal monitor issue	change SMBUS from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA (Q30,Q31)	A1A	3		
21	CPU Power issue	stuff C198, unstuff C217 (base on layout location)	A1A	4		
22	GMCH Power issue	Short R115~R117,change +VCC_CFXCORE_INT to +1.05V	A1A	8		
23	GMCH Power issue	Short R122,R138, remove VCC_RXR_DMI circuit (connect to +VCC_PEG directly)	A1A	9		
24	GMCH Power issue	INTEL CRB VCCD_QDAC Filter Modification:change L13 to R125(100ohm), change R145(*0 ohm) to C507(1uF)	A1A	9		
25	DDR Power issue	stuff R192, no stuff R191,R193 for SMDDR_VREF_DIMM	A1A	13		
26	RTC BAT issue	Change RTC_BATTERY CONN CN12(follow to ZC3)	A1A	14		
27	ICH8-M Strap issue	Stuff R241, no stuff R266 (Disable Internal VR powering VccLAN1_05, VccCL1_05)	A1A	14		
28	ICH8-M HDA issue	add R283,R465,R463,R267 for MDC module (base on Intel Design Giude)	A1A	14		
29	ICH8-M issue	PU RCIN# to +3V	A1A	14		
30	ICH8-M issue	Remove ICH8-M GLAN/SATA1/SATA2 circuit (no use)	A1A	14		
31	ICH8-M issue	change net name (U31/Pin2) from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#	A1A	16		
32	ICH8-M issue	Remove SATACLKREQ#(U32/Pin:AG13),RI# (U32/Pin:AF17) ;{no use}	A1A	16		
33	ICH8-M issue	no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME	A1A	16		
34	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16		
PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1	CHANGE LIST SHEET 1
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page		
35	Power sequence issue	change (U21/Pin5) from +3V to +3VSUS (refer to ZC1)	A1A	16		
36	ICH8-M issue	Remove WOL_EN (U32/Pin:AG19) -no use	A1A	16		
37	ICH8-M issue	Remove SUSM# (used to control power planes to the Intel AMT sub-system)	A1A	16		
38	ICH8-M issue	Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT (no use)	A1A	16		
39	ICH8-M issue	connect LAN_RST#(U32/Pin:AH20) to PLTRST# (If no use internal LAN MAC connect LAN_RST# to PLTRST#)	A1A	16		
40	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16		
41	EMI issue	EMI suggest C373 from 0.1u to 10uF	A1A	17		
42	ICH8-M Power issue	Reserve R308,R313 for +1.5V MDC module	A1A	17		
43	LAN Power issue	change LAN power from +3V_LAN_S5 to +3V_S5	A1A	18		
44	LAN Power issue	BCM FAE: Pull up Vmainprst (U10/Pin53) to the system main power (3.3v), but not the standby power	A1A	18		
45	LAN Power issue	BCM FAE: Change capacitance value from 47-uF to 10-uF.	A1A	18		
46	LAN Power issue	BCM FAE:stuff R30,no stuff R47(in order to pull up C90,C86 and Q16/pin 3 to 3V_LAN rail)	A1A	18		
47	LAN Switch issue	EMI suggest C59 from 0.1u to 10uF	A1A	18		
48	LAN Switch issue	Add Diode D4 for isolation (Dockin#)	A1A	18		
49	LAN Switch issue	change LAN Switch from MAX4892 to PI3L500	A1A	18		
50	LAN Transformer issue	change TRANSFORMER GND(U3/Pin15,18,21,24) to MGND	A1A	18		
51	LAN CONN issue	Change CONN P/N (follow ZC1)	A1A	18		
52	LAN CONN issue	change CONN GND(CN19/Pin13,14) to MGND	A1A	18		
53	CRT issue	change C439, C440,C7,C441 to 30-50pF(default :no stuff)	A1A	19		
54	CRT issue	Change CRT_SENSE# from CRT CONN Pin11 to Pin5 (follow Acer define)	A1A	19		
55	CRT issue	Change CRT CONN P/N(follow ZC1)	A1A	19		
56	CRT issue	change R16,R17 from 2.7k to 2.2k ; R10,R12 from 39 to 0 ohm	A1A	19		
57	CRT issue	change U1 from CM2009 to IP4772	A1A	19		
58	LVDS issue	change CCD function from USB7 to USB8	A1A	20		
59	LVDS issue	Change C12 from CH6102M9900 to CH61004M3E5 (refer to ZC3)	A1A	20		
60	TV issue	Change CN17 CONN P/N (follow ZC1)	A1A	20		
61	SDVO issue	Change R51,R56 value from 2.2k to 4.7k (FAE suggest R value from 4K-9K)	A1A	21		
62	PCMCIA issue	refer to BL3. Add G_RST# circuit.	A1A	22		
63	PCMCIA issue	FAE suggest R189's value under 47 ohm.	A1A	22		
64	Card reader issue	no stuff R496,R522	A1A	23		
65	Card reader issue	FAE suggest R503's value under 47 ohm.	A1A	23		
66	Card reader issue	Remove U39/Pin99, no use (XMDAT4B is for 8 bit MMC,remove it.)	A1A	23		
67	Card reader issue	Change C593 from 0.1u to 10uF,EMI suggest add C587 0.1uF	A1A	24		
68	PCMCIA issue	change PCMCIA CONN (follow BH1)	A1A	24		
PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1	CHANGE LIST SHEET 2
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:			Schematic Rev.	Page
69	PATA ODD issue	change R253 from 0 to 33ohm			A1A	26
70	PATA ODD issue	Add C326,C327,C344 for +5V			A1A	26
71	PATA ODD issue	Remove D23, already add in page29			A1A	26
72	Mini Card issue	Reserve R349,R350,R337,R345,R344,R338,R339 for debug card use			A1A	27
73	Mini Card issue	Add (CN28/Pin39,41) to +3V_WL_VDD (follow Z01)			A1A	27
74	Mini Card issue	Remove (CN28/Pin36,38) USB circuit			A1A	27
75	Mini Card issue	Remove (CN28/Pin46) BT LED			A1A	27
76	Mini Card issue	Remove 0.1uF (CN28/Pin23,25), already in WL module			A1A	27
77	Bluetooth issue	SI suggest to remove 22pF*2 (CN5/Pin3,4)			A1A	27
78	USB CONN issue	SI suggest to remove 22pF*2 (CN11/Pin2,3)			A1A	27
79	EC issue	Change EC from WPC8769 to WPC8763			A1A	28
80	EC issue	change U7/Pin5,6 from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA			A1A	28
81	EC issue	Remove ME_EC_ALERT#			A1A	28
82	EC issue	FAE:Change U14/Pin80 from +3VPCU to +A3VPCU			A1A	28
83	EC issue	change C130,C131 from 6.8p to 5.6p			A1A	28
84	EC issue	Add D18 for HWPG_CPUIO			A1A	28
85	Finger Printer issue	SI suggest to remove 22pF*2 (CN9/Pin2,3)			A1A	29
86	SuperIO issue	Remove PPT PU 4.7K circuit (already in docking)			A1A	30
87	Audio issue	Change Serial resister R484,R485 value from 22 ohm to 33 ohm			A1A	31
88	Audio issue	reserve R513 to reduce ringing			A1A	31
89	Audio issue	Refer to ZD1, change R546,R520,R545,R519 to 10k			A1A	32
90	Docking issue	(CN22/Pin18,Pin19):(1)Remove Level-shift circuit (2)change Power from +3V to +2.5V (3)stuff 2.2k			A1A	33
91	Docking Power issue	Add .1u*7 , 10U*1 for VA			A1A	33
92	Docking issue	Reserve U25 for docking PWRBTN#			A1A	33
93	Docking issue	Change Docking Pin141/142 from USB5 to USB3			A1A	33
94	Docking issue	PL DVI_DET 100k to GMD (CN22/Pin20)			A1A	33
95	Docking issue	Change LAN pin define			A1A	33
96	Audio issue	Change CN29,CN30,CN31 P/N (Base on Acer request)			A1B	32
97	ICH8-M Strap issue	Change INTVRMEN from PD to PU			B1C	14
98	Leakage issue	add D43,D44 to stop leakage from EC to SB			B1C	16
99	ICH8-M issue	change DOCKIN# from GPIO7 to GPIO12			B1C	16
100	Power sequence issue	short PWROK_EC to MPWROK			B1C	16
101	ICH8-M issue	PU GPIO10 to +3V, PD GPIO14 to GND			B1C	16
102	ICH8-M issue	remove R229,R233,C355			B1C	16
 PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1 / A2	CHANGE LIST SHEET 3
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:			Schematic Rev.	Page
103	PCMCIA issue	Reserve R572 for debug use			B1C	22
104	1394 issue	Change R271,R306,R307 from 56.2 to 5.1k ohm (fix 1394 can't detect issue)			B1C	25
105	Mini Card issue	no stuff R353,R348,R356			B1C	27
106	Mini Card issue	need support BCM WL Module, Connect CN28/Pin40 to GND			B1C	27
107	EC issue	SWAP GPIO1 and GPIO3			B1C	28
108	EC issue	Change CN10/Pin1 from +3V to +3VPCU			B1C	28
109	LED issue	Base on Me request, change PWR/SUS/BAT LED type			B1C	29
110	Audio issue	Stuff R330 to fix Internal SPK issue (floating GND issue)			B1C	27
111	Docking issue	Add R566 for Debug use			B1C	33
112	Mini Card issue	ME request :change CN28 P/N from DFHD52MS049 to DFHS52FR082 (9.0mm to 9.9mm)			B1D	27
113	GMCH Power issue	Change C143 from CH71002MJC8 to CH7102MT804 (Z-limit issue,H2.9mm to H1.5mm)			B1D	9
114	CPU Clock issue	Set CPU Frequency to auto selection (no stuff R179,R198,R447)			C2A	2
115	S5_ON issue	Change S5_ON control circuit (follow Z01/ZD1)			C2A	34
116	CK505 issue	change CK505 VDD_IO from +1.05V to +1.25V. Because VDD_IO will drop out when high loading			C2A	2
117	G995 issue	Add level shift circuit (follow Z01), remove D39,no stuff R383.			C2A	3
118	BIOS EMI issue	FAE suggest add 22 Ohm dumping resistors R596,R597 to avoid potential EMI problem			C2A	28
119	LAN issue	Base on BCM IEEE test result, change RDAC value (R42) from 1.24k to 1.18k			C2A	18
120	Audio issue	Acer change internal Mic solution to Fortemedia, Remove CN33,D29,D30,R342,R506,C400,C586			C2A	32
121	DVI Detect issue	Intel suggest:Add hotplug circuit to DVI_DET (follow ZC1)			C2A	21
122	ICH8M issue	Intel Suggest :ICH8M CPI020 should not be pulled HIGH.Remove BOARD_ID3 circuit(remove R474,R475)			C2A	16
123	SDVO issue	Intel Suggest :Follow Intel New Guideline(MoW 48 update) Change R51,R56 from 4.7K to 3.9K ohm			C2A	21
124	GMCH Power issue	Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW.reserved 0 ohm resister (R576)			C2A	8
125	SuperIO issue	Intel Suggest :All LPC devices support LPCPD# protocol, stuff D7			C2A	30
126	ICH8M issue	no stuff R259 to prevent leakage issue			C2A	16
127	EMI issue	EMI suggest add C647 to prevent noise for PR_STS			C2A	33
128	EMI issue	EMI suggest to add .1u *2 to prevent noise (+3V)			C2A	30
129	EMI issue	EMI suggest to add 2.2ohm BST resister (PR153) in 1.8V power			C2A	37
130	EMI issue	EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)			C2A	30
131	ME issue	ME request add three pad for fix wire (PAD20,21,22)			C2A	30
132	DVI issue	remove the U11,R57,R52,C109 to save layout space.			C2A	21
133	Power monitor issue	D16 not necessary if 3V/5V fail, EC can't work.			C2A	28
134	S3 resume POP sound issue	change C619 from CH61004M2E8 to CH5222K9A09 to solve S3 resume POP sound issue			C2A	31
135	POP sound issue	no stuff R525,D41, add bypass R577 to solve pop sound issue			C2A	31
136	AUDIO issue	no stuff D27			C2A	32
 PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : King Wang	DRAWING BY:Barry Lee	Stage: A2 / B	CHANGE LIST SHEET 4
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page		
137	Audio issue	change R546/R520 from 10k to 9.1k	C2A	32		
138	GMCH POWER issue	Change Crestline VCC_AXM from +1.25V to +1.05V, reserved 0 ohm resister (R578)	C2A	8		
139	XTAL issue	Base on vendor-FCE suggestion, change C580/C579 from CH01206JB05 (12p) to CH02206JB08 (22p)	C2A	25		
140	XTAL issue	Base on vendor-FCE suggestion, change C310/C299 from CH03306JBD7 (33p) to CH02706JB06 (27p)	C2A	2		
141	XTAL issue	Base on vendor-FCE suggestion, change C130/C131 from CH-5606TB01 (5.6p) to CH01006JBD1 (10p)	C2A	28		
142	EMI issue	EMI request: DEL PR120 2.2ohm(CS-2203F911), stuff PC98	C2A	37		
143	EMI issue	EMI request: reserve .1U for (CN19/pin9,10)	C2A	18		
144	EMI issue	EMI request: reserve L-C footprint for debug use (R52,C650)	C2A	20		
145	debug issue	Stuff R349 , R350 for debug use	D3A	27		
146	Modem wake from S3 fail issue	Change CN14/pin 2 from +3v to +3v_s5.	D3A	31		
147	CableSence circuit issue	Add CableSence circuit (unstuff R78)	D3A	18		
148	CableSence circuit issue	Add CableSence circuit (reserve R579)	D3A	18		
149	LED type issue	Base on SMT-ME request, change LED type to 2 in 1,DEL LED4,LED5,LED6,LED7,R570,R571,Add LED2,LED3	D3A	29		
150	SW button issue	Base on ASSEMBLY -Line request, remove SW1, add G2 footprint	D3A	29		
151	change Modem capacitor to meet safety standard	change C37,C48 from CH147GK0I09 to CH147GK0I00	D3A	33		
152	Power issue	The system side should have a diode (D45,D46) to block the AC adaptor power and ezDock.	D3A	33		
153	EMI issue	Change L4,L5,L6 from CX8BA220007 to CX8BA470003	D3A	19		
154	DVI issue	remove U13,R68,R75,R73,C98 for layout space issue	D3A	21		
155	ASF issue	Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)	D3A	16		
156	SMT B open issue	(1)Remove footprint for D41,D42,R525. DEL R577 (0 ohm) (2) Remove net SECNTL	D3A	31		
157	CableSence circuit issue	change LAN Low power pin from GPIO47 to GPIO52	D3A	28		
158	LAN switch issue	Change U6 from AL000500005 to AL000500030 (change to 8KV solution)	D3A	18		
159	Change 965GM from ES sample to QS sample	Change U29 P/N from AJ0QN120T37 to AJ0QP200T09	D3A	5~11		
160	Change ICH8M from ES sample to QS sample	Change U32 from AJ0QM740T31 to AJ0QN230T10	D3A	14~17		
161	Audio Jack issue	change CN30,CN31,CN32 footprint from AUDIO-010164FR006GX53XL-C-8P to AUDIO-JA60331-X39T4-7F-8P	D3A	32		
162	docking sometimes can't detect DVI device issue	change R51,R56 from 3.9k(CS23902FB14) to 4.7k(CS24702JB38).	D3A	21		
163	EMI issue	EMI suggest, add common Choke, co-lay R795,R796	D3A	27		
164	Audio Jack issue	Change CN30 P/N from DFTJ06FR017 to DFTJ06FR059	D3A	32		
165	Audio Jack issue	Change CN29 P/N from DFTJ06FR019 to DFTJ06FR061	D3A	32		
166	Audio Jack issue	Change CN31 P/N from DFTJ06FR018 to DFTJ06FR060	D3A	32		
167	backlight control issue	Follow Z01 design,Remove R24 footprint, DEL D3(BC000316Z07).Add R73,Q36,Q37	D3A	20		
168	docking CRT flicker issue	Reserve C98,R525 for docking CRT flicker issue	D3A	19		
169	EMI issue	EMI suggest add C652(0.1uF)	D3A	19		
170	system sometimes will no backlight issue .	For short term solution:change R22 from 10k(CS31002JB28) to 1K (CS21002FB24)	D3A			
PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: B/C	CHANGE LIST SHEET 5
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Kin Wang	DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
171	Quanta DSC Team issue	Base on DSC command, change CN22 P/N from DFHDF8MS000 to DFHDF4MS000	D3A	33
172	rise time of LCDVCC is >0.5ms and <=10ms.	change U2 from AL004280000(AAT4280IGU-3-T1) to AL004280018(AAT4280IGU-1-T1).	D3A	23
173	Card reader issue	no stuff 43K(CS34302JB19):R562,R527,R533,R538,R539,R565,R561,R540,R498,R497,R500,R552,R555	D3A	23
174	Card reader issue	no stuff 10k(CS31002JB28) : R560	D3A	23
175	Card reader issue	Change R547 from 43k (CS34302JB19) to 8.2k (CS28202JB14)	D3A	23
176	Card reader issue	Change R528 from 10K(CS31002JB28) to 43K(CS34302JB19)	D3A	23
177	Shortage issue	Change R125 from CS11003B900 (100 ohm 0.1%) to CS11003F953(100 ohm 1%)	D3A	9
178	EMI issue	EMI request add two of clip(FDTA1003014) in PAD17 and PAD19 for EMI issue	D3A	30
179	DPST issue	Acer inform no support DPST in C build, remove R15	D3A	20
180	Shortage issue	Andy inform change PR116 from CS42102FB00 to CS42002FB12	D3A	34
181	ICH8M Power issue	ICH8M Internal VR should not be disabled.no stuff R241, stuff R226	D3A	14
182	implement it for CPU protect in C build.	Change R111 from *2.2k to 0ohm,Change R107 from 56.2(CS05622FB22) to 1k(CS21002FB24)	D3A	3
183	Battery life issue.	Battery life issue. Disable ICH8M Internal VR (LAN). stuff R241, no stuff R226 for C-build	D3A	14
184	Change EMI Spring Material	ME request, change EMI Spring from FDTA1003014 to FDZU1002010	E3A	30
185	C-Test SMT open issue	C-test SMT open issue, remove PAD18	E3A	30
186	ZR1 issue	Change CN2 Pin define to cover production line issue(Inverter short with signal to burn system)	E3A	20
187	C-Test SMT open issue	Change PD9,D46 footprint from SBM1040-3P to SBM1040-3P-ZU1 for SMT C-test open issue	E3A	33 & 39
188	Change NB P/N for RAMP	Change U29 P/N form AJ0QP200T09 to AJSLA5T0T05	E3A	5~11
189	Change SB P/N for RAMP	Change U32 P/N from AJ0QN230T10 to AJSLA5Q0T05	E3A	14~17
190	Material Lead issue	Change R214 from CS02403F908 to CS02403F916 (Lead free)	E3A	14
191	G995 failure rate issue	Add C653 base on G995 failure rate issue	E3A	3
192	Run-in auto shot down issue	ICMNT connect to EC pin100 , reserve R570 0ohm for debug use, Add C654 to avoid noise	E3A	28 & 39
193	remove wake on lan for Mini PCIE function.	Base on Acer demand, remove wake on lan for Mini PCIE function.no stuff Q25,R357	E3A	27
194	move D15~D18 location for FFC cable issue	Remove footprint (D16), Remove net (HWP6_3/5VPCU),no stuff PR119	E3A	28 & 34
195	LED issue	Change LED2, LED3 type base on ME request, Add R800,R801	E3A	29
196	HDD Mylar issue	Change C542 from 0805(CH6102K9A01) to 0603(CH6101M9905) base on ME request(HDD Mylar issue)	E3A	2
197	Docking issue	Change Q4,Q5 Pin2 from +3V to +3VSUS .(Docking side pull up to +3VSUS plane)	E3A	33
198	Docking issue	change C451,C452 from 0.1uF (CH41002KB93) to 0 ohm (CS00002JB38)(R802,R803)	E3A	33
199	Disable LAN Low Power mode	Stuff R78(CS24702JB38)	E3A	18
200	EOL issue	Change C453 from CC1210 (CH61004M3E5) to CC1206 (CH61004M2E8)	E3A	33
201	LPC CONN issue	confirm with BIOS-CM, no need LPC dedug CONN,Remove CN6,R432 footprint to save space for layout.	E3A	28
202	LAN_RST# issue	(1)Stuff 10k for R204(2)Don't stuff R456(3)Don't stuff R247	E3A	16
203	PO" sounds when insert PCMCIA card	Add 0 ohm (R804) for PCMSPK	E3A	22
204	ESD issue	Stuff D38 for CRT port	E3A	19
 PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1 APPROVE BY : Kin Wang DRAWING BY:Barry Lee Stage: C / Ramp	CHANGE LIST SHEET 6	
MB ASSY'S P/N : 31ZU1MB0000		PROJECT LEADER:Jack Wu DOCUMENT NO:	DATE :2006/12/09	

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page		
205	PCMCIA POP SOUND issue	Refer to BU1, add circuit for POP sound issue	E3A	24		
206	GLAN issue	Stuff R232 (CS02492FB29), The GLAN_COMP0/GLAN_COMPI connection to 1.5-V rail through the resistor remains	E3A	14		
207	ESD issue	change LED type (follow B stage) DEL LED2,LED3, Add LED4~7	E3A	29		
208	ESD issue	change ESD protect Diode from location LED/B to MB	E3A	29		
209	Disable LAN Low power mode	Base on PM suggestion, add serial 0 ohm (R806) for debug use.(no stuff)	E3A	18		
210			E3A			
211			E3A			
212			E3A			
213			E3A			
214			E3A			
215			E3A			
216			E3A			
217			E3A			
218			E3A			
219			E3A			
220			E3A			
221			E3A			
222			E3A			
223			E3A			
224			E3A			
225			E3A			
226			E3A			
227			E3A			
228			E3A			
229			E3A			
230			E3A			
231			E3A			
232			E3A			
233			E3A			
234			E3A			
235			E3A			
236			E3A			
237			E3A			
238			E3A			
 PROJECT : ZU1 Quanta Computer Inc.		PROJECT : ZU1	APPROVE BY : Kin Wang	DRAWING BY:Barry Lee	Stage: Ramp	CHANGE LIST SHEET 7
		MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2007/03/29	