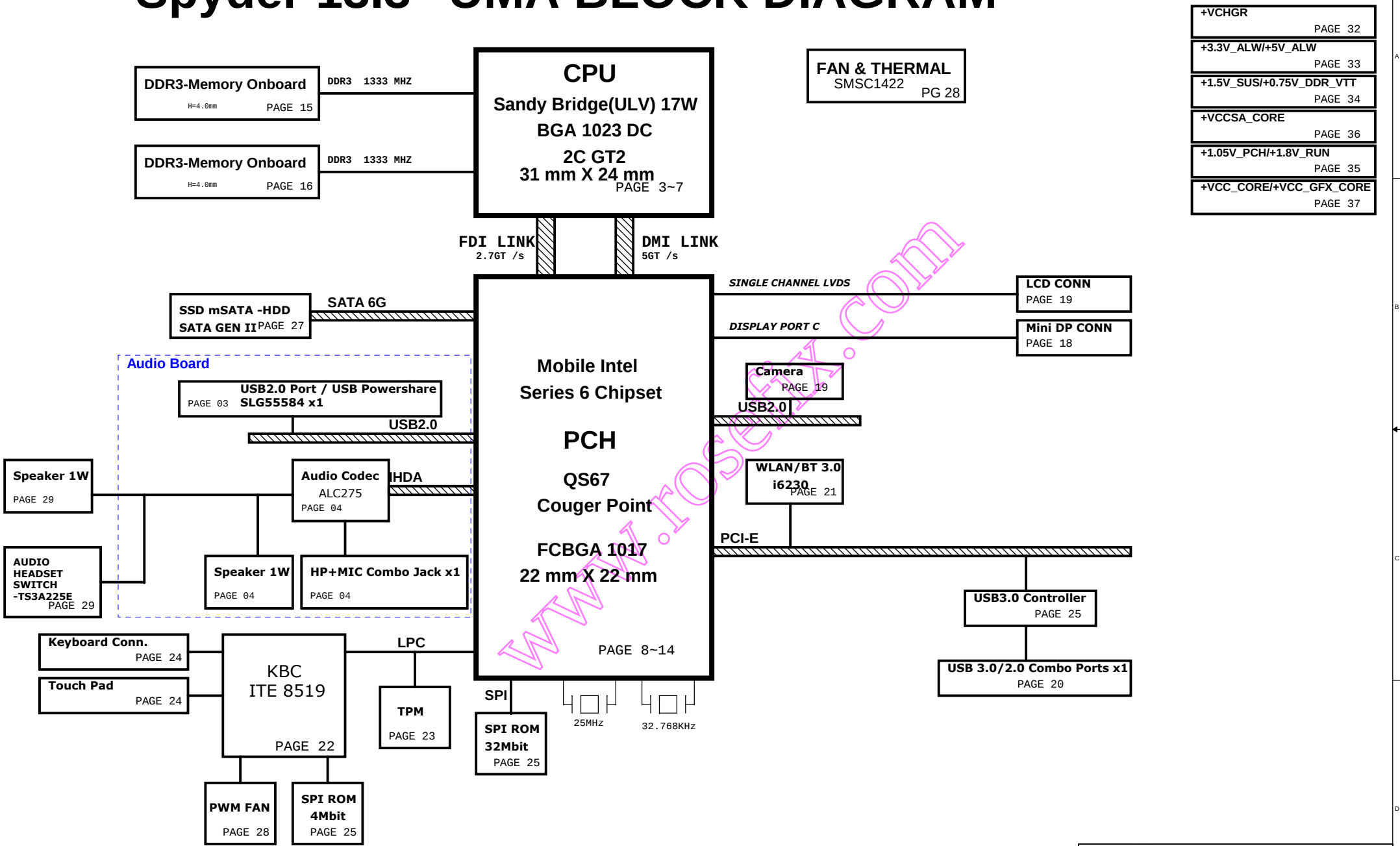


Spyder 13.3" UMA BLOCK DIAGRAM



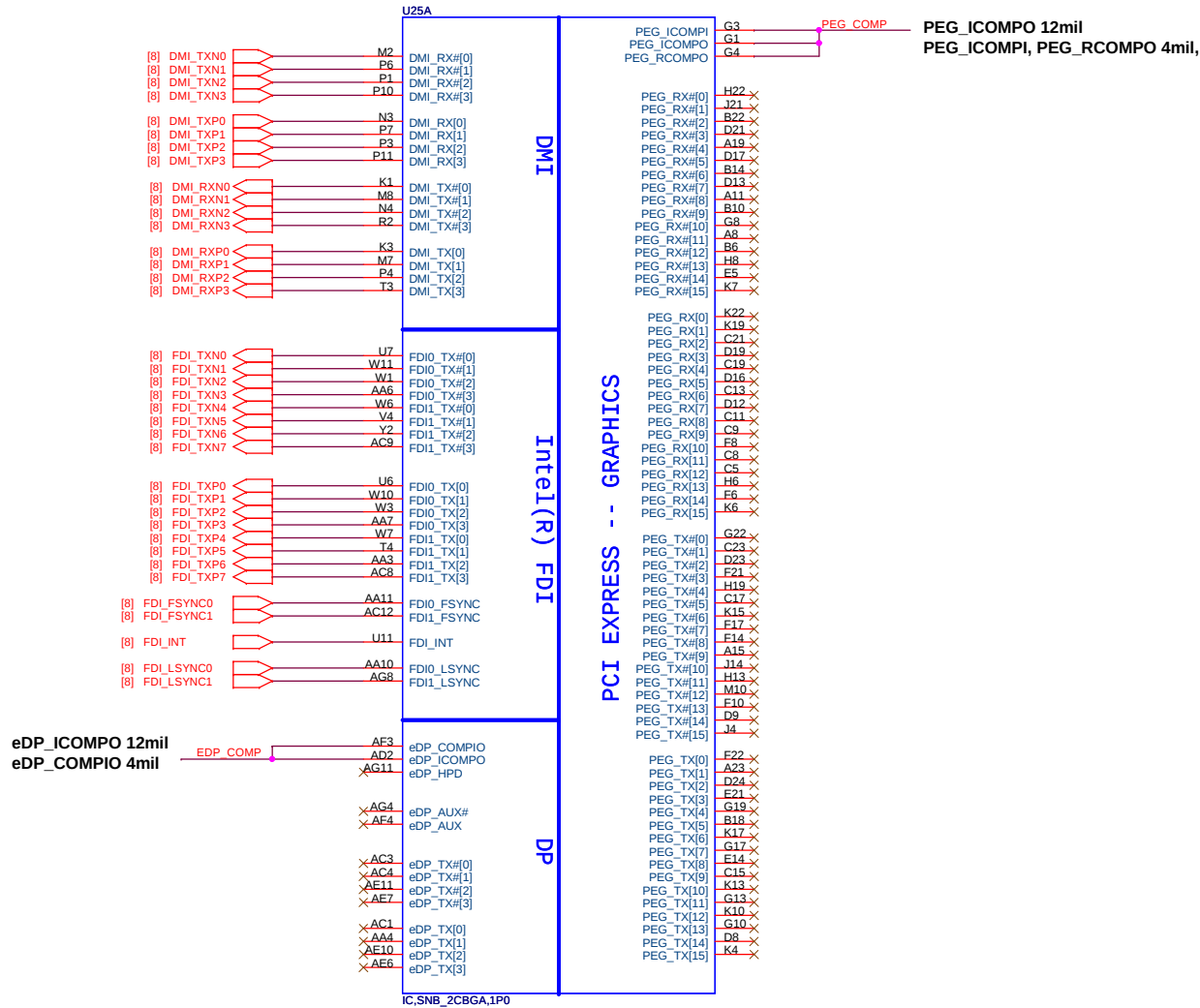
power State	SLP_S3#	SLP_S4#	SLP_S5#	ALW_ON	+3.3V_ALW	+5V_ALW	SUS_ON	+3.3V_SUS	+5V_SUS	RUN_ON	+3.3V_RUN	+5V_RUN	A0AC flag	USB2.0 Power share USB_BAK_EN#
S0	H	H	H	H	H	H	H	H	H	H	H	H	L	L
S3	L	H	H	H	H	H	H	H	H	L	L	L	L	L
S4/S5 AC	L	L	L	H	H	H	L	L	L	L	L	L	L	L
S4/S5 DC Only	L	L	L	L	L	L	L	L	L	L	L	L	L	L
AC/DC No Exist	L	L	L	L	L	L	L	L	L	L	L	L	L	L
A0AC(S4)	L	L	L	H	H	H	H	H	H	L	L	L	H	H



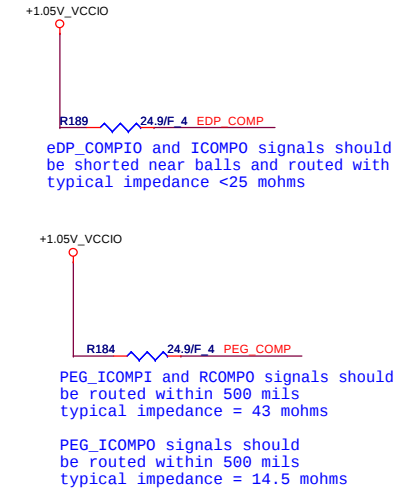
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PROJECT : D13

Sandy Bridge Processor (DMI, PEG, FDI)

CPU is i7 in schematic

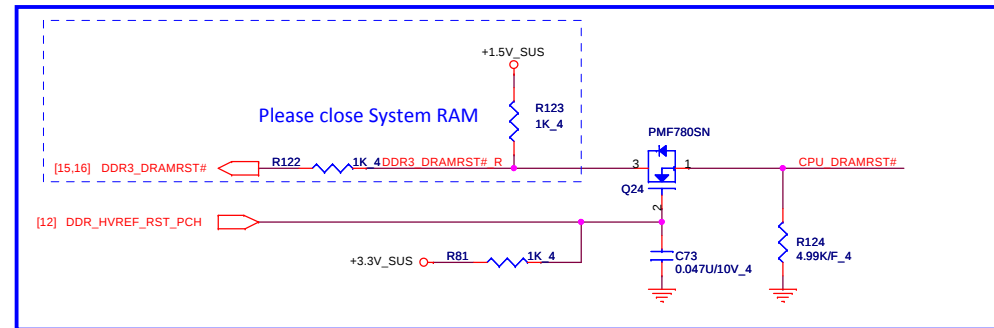
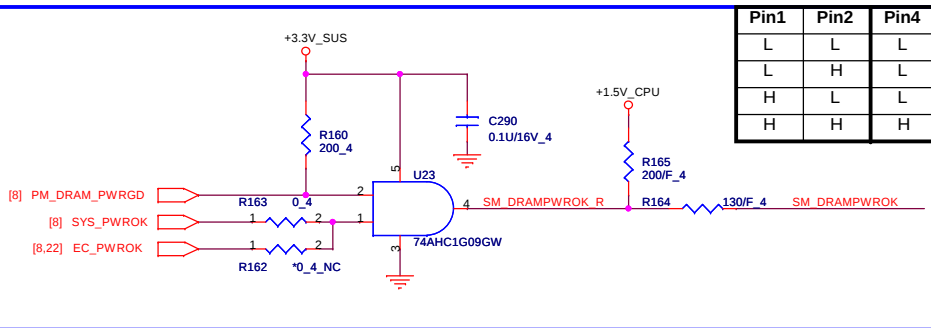
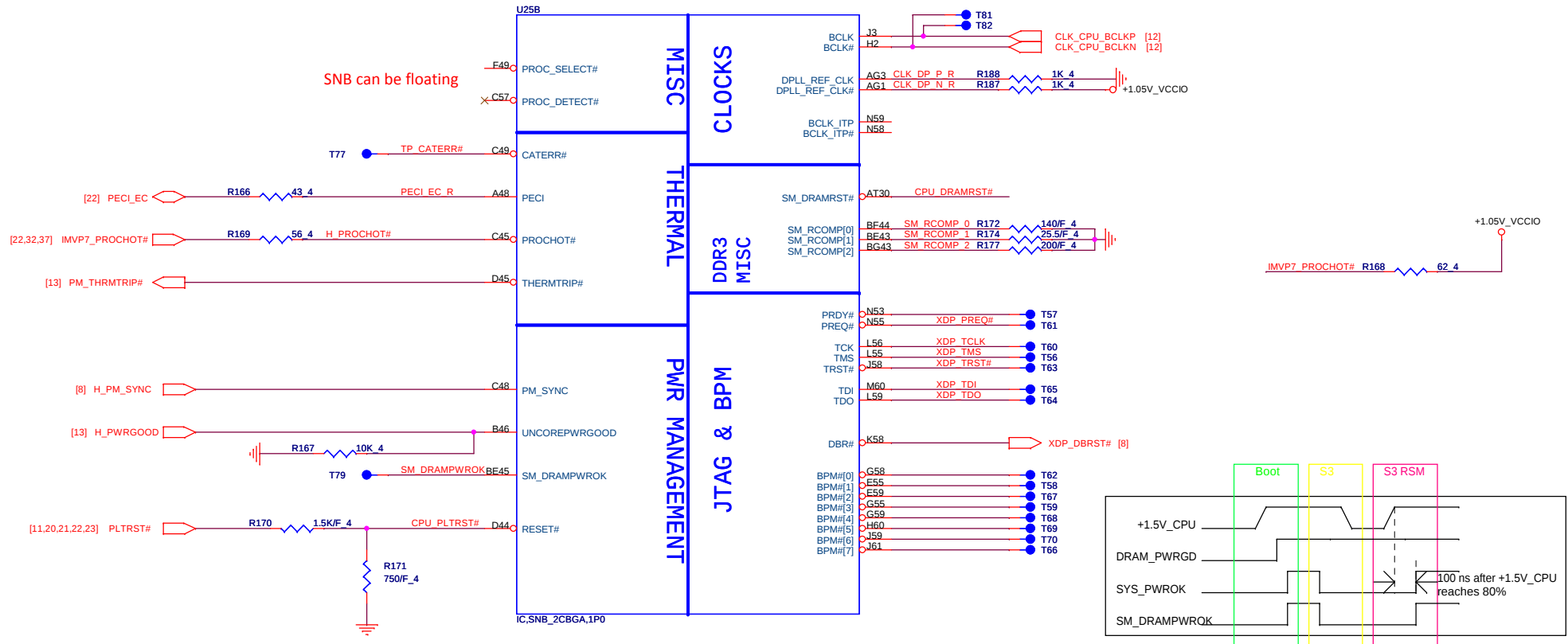


DP & PEG Compensation



Sandy Bridge Processor (CLK,MISC,JTAG)

CPU is i7 in schematic

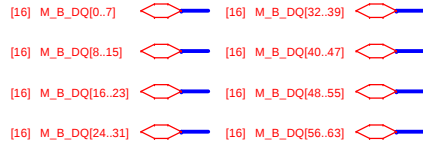
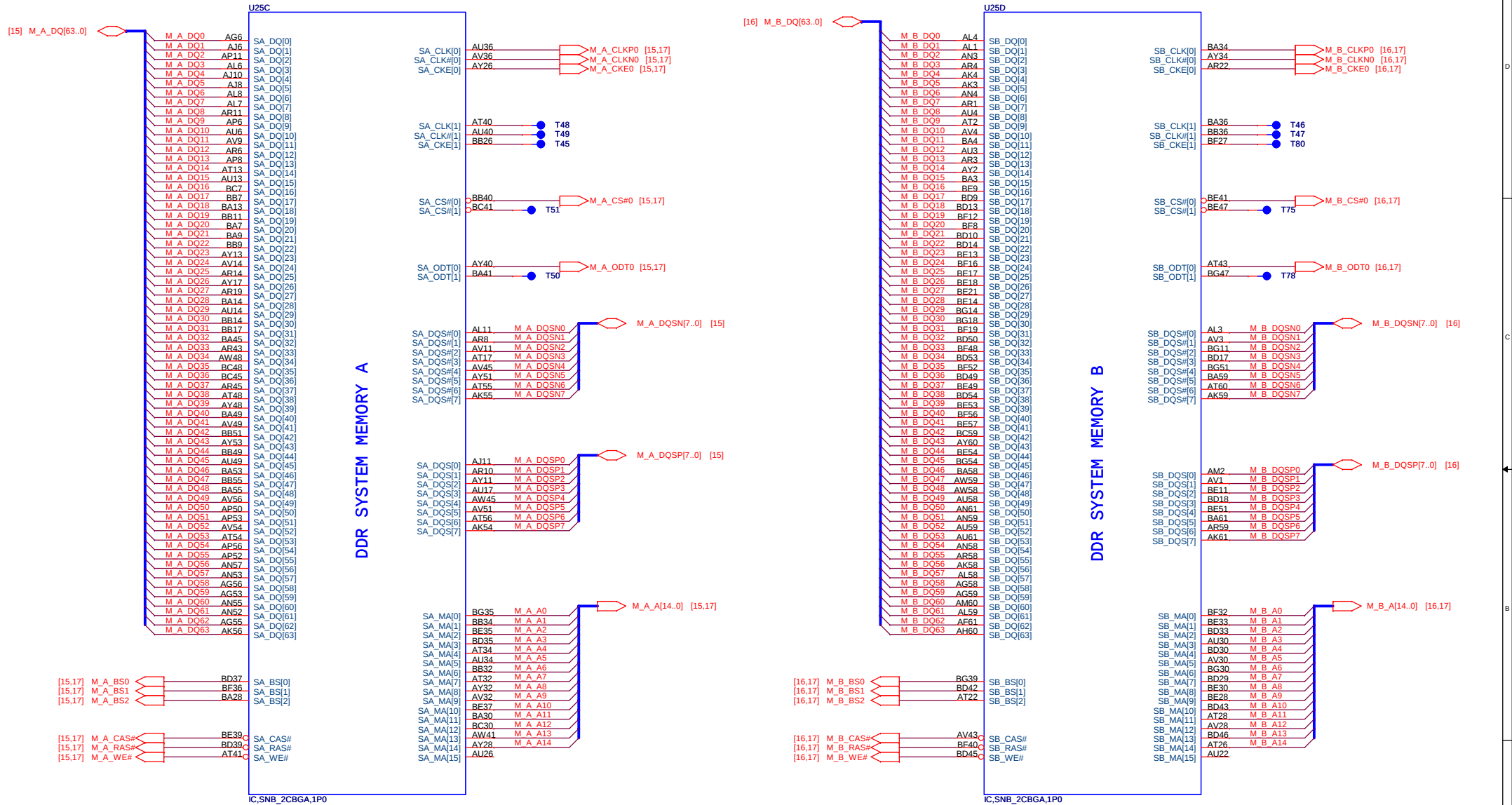


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Sandy Bridge Processor (DDR3)

CPU is i7 in schematic

CPU is i7 in schematic



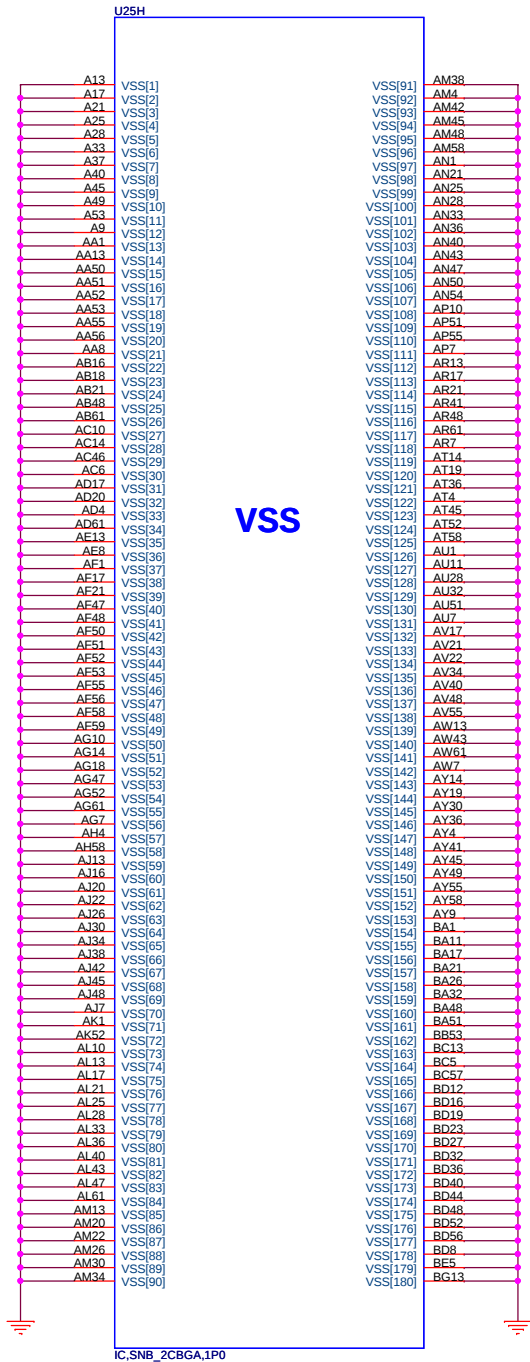
--	--

2

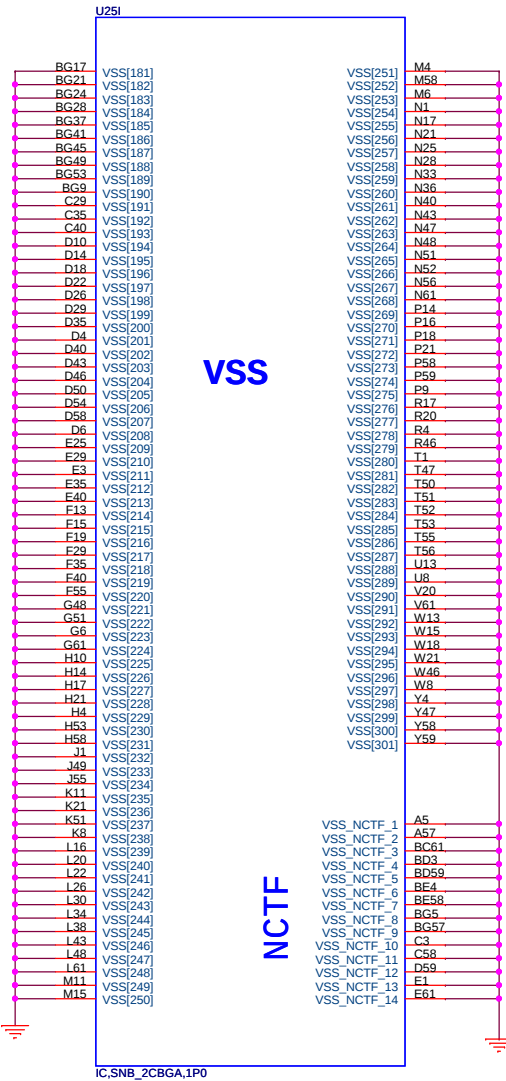


Sandy Bridge Processor (GND)

CPU is i7 in schematic



CPU is i7 in schematic

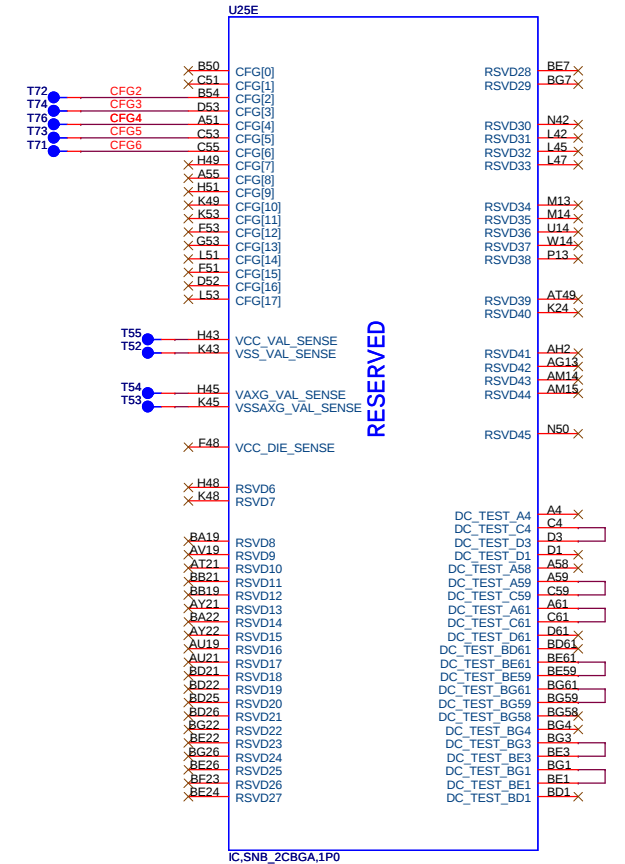


Processor Strapping

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

Sandy Bridge Processor (RESERVED, CFG)

CPU is i7 in schematic



PGB straping pin unused for UMA only

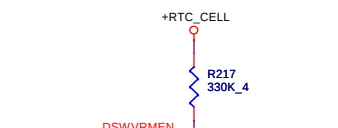
CFG[6:5] (PCIe Port Bifurcation Straps)

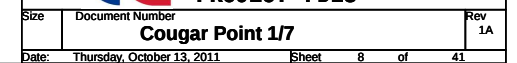
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



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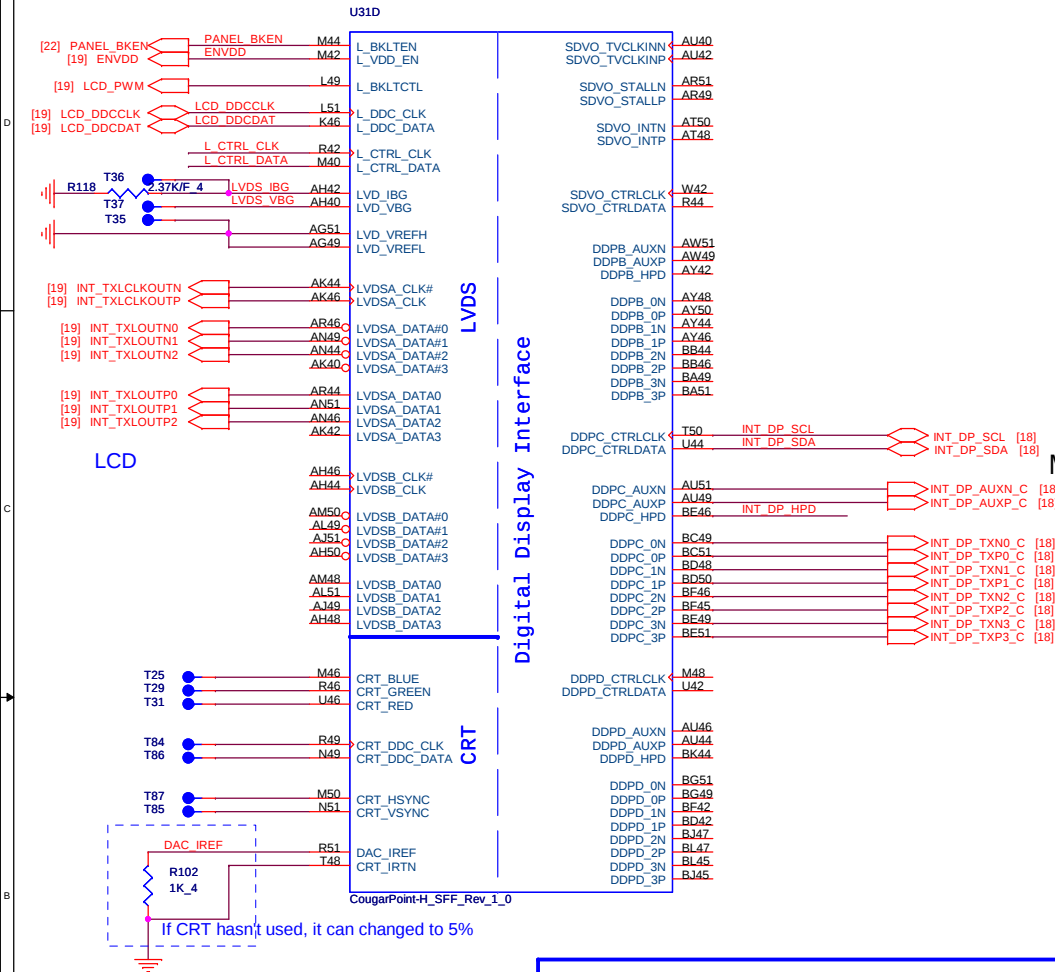
U31C



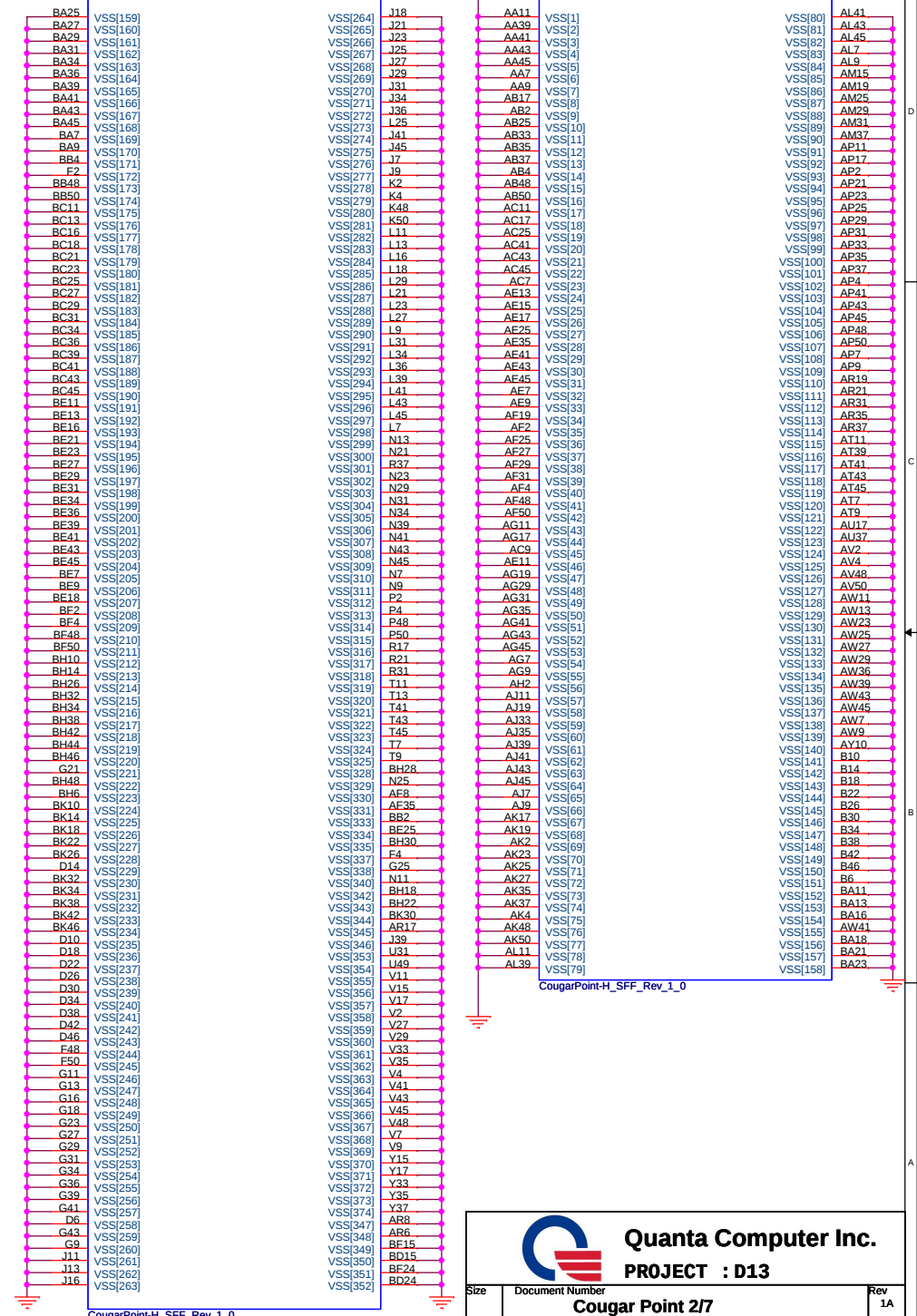


Cougar Point (LVDS,DDI)

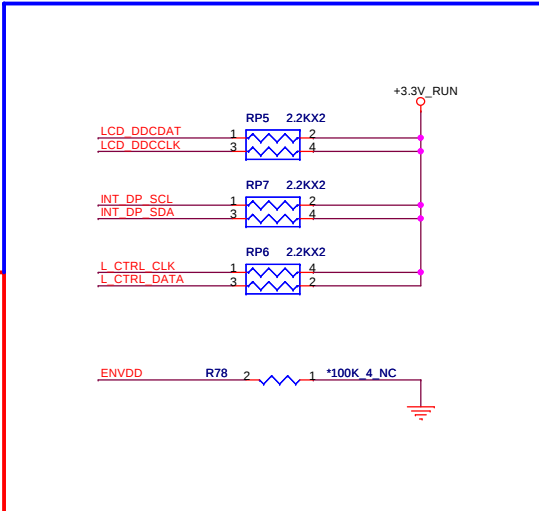
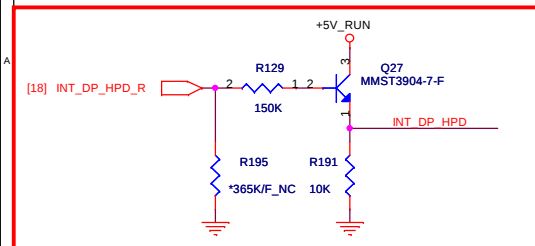
Cougar Point (GND)



Mini DP



Follow R05 QT stage design



The schematic diagram illustrates the internal connections of the CougarPoint-H_SFF Rev_1.0 module. It features several functional blocks and their associated pins:

- RTC (Real-Time Clock):** Includes components like Y3 (32.768KHZ), R219 (10M_4), C319, and R90. Pins include RTC_X1, RTC_X2, RTC_RST#, SRTC_RST#, SM_INTRUDER#, PCH_INTVRMEN, INTRUDER#, and INTVRMEN.
- IHDA (Intel High Definition Audio):** Connects to HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33, and HDA_DOCK_RST# / GPIO13.
- JTAG (Joint Test Action Group):** Connects to JTAG_TCK, JTAG_TMS, JTAG_TDI, and JTAG_TDO.
- SPI (Serial Peripheral Interface):** Connects to SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, and SPI_MISO.
- SATA (Serial ATA):** Connects to SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA2RXN, SATA2RXP, SATA2TXN, SATA2TXP, SATA3RXN, SATA3RXP, SATA3TXN, SATA3TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, and SATA5TXP.
- mSATA (Mini Serial ATA):** Connects to SATA_RXN0 [23], SATA_RXP0 [23], SATA_TXN0 [23], and SATA_TXP0 [23].
- Open-drain Output:** Connects to W10, M2, and R1.

The diagram also shows power supply connections (+3V, +3V_SS) and ground connections. Various passive components like resistors (R223, R216, R227, R222, R210, R208) and capacitors (C784, C317, C374/F 4, 49.9/F 4, 750/F 4) are shown with their values and tolerances.

MP remove(Intel)

+3.3V_SUS

PCH_JTAG_TMS R98 200 4

PCH_JTAG_TDI R95 200 4

PCH_JTAG_TMS R104 1 2 100 4

PCH_JTAG_TDI R97 1 2 100 4

PCH_JTAG_TCK R107 51 4

+3.3V_SUS

PCH_JTAG_TDO R99 200 4

R105 1 2 100 4

+3.3V_4

+RTC_CELL

R100 20K/F 4

R224 20K/F 4

RTC_RST#

SRTC_RST#

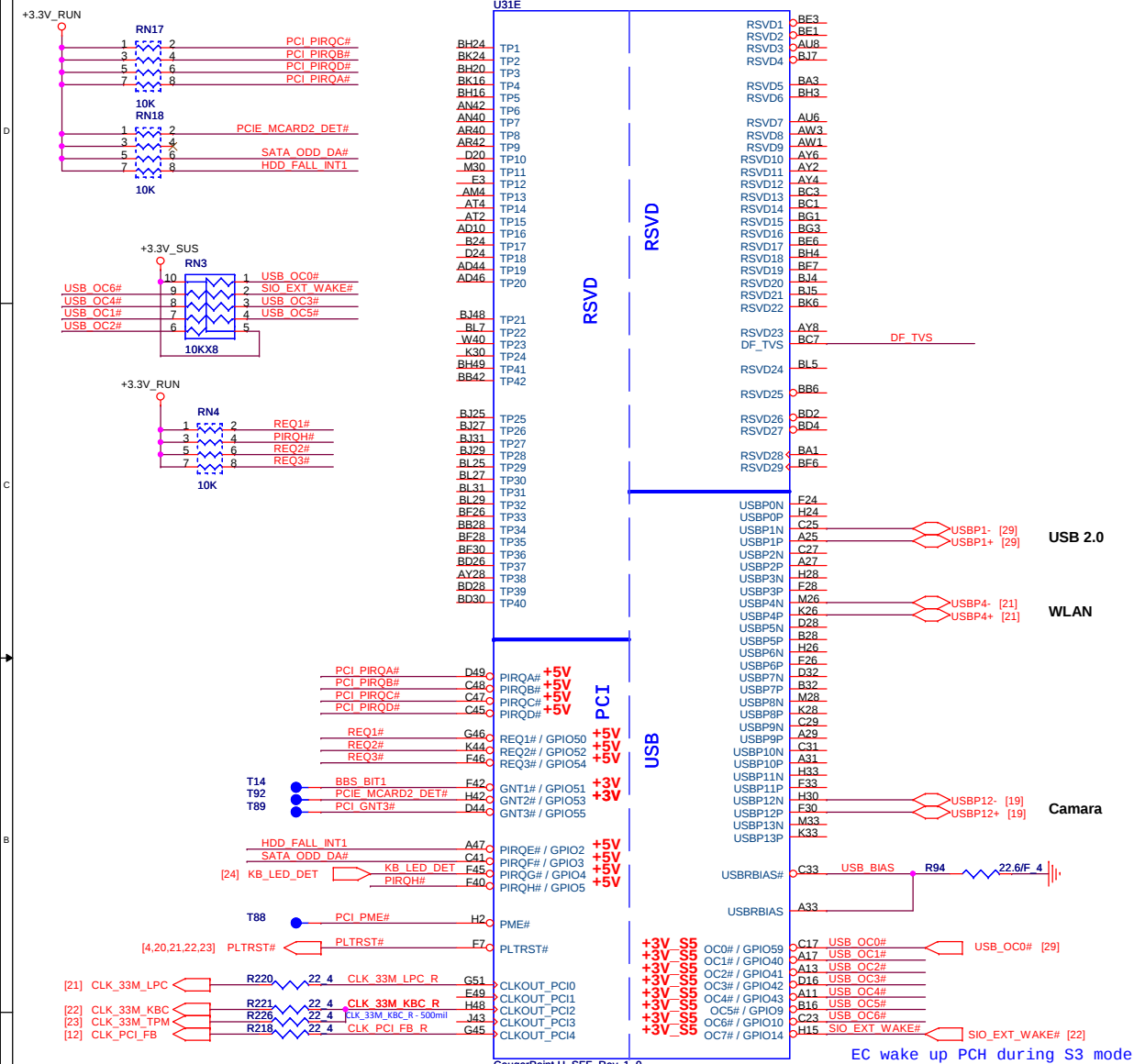
C77 1U/6.3V_4

C320 1U/6.3V_4

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	

PCI/USBOC# Pull-up(CLG)

Cougar Point-M (PCI, USB, NVRAM)

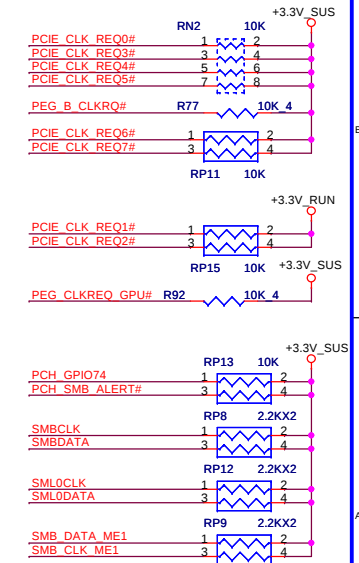


Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 10K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 10K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# (Internal PU)												
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
R19a 2 2.2K 4 +1.8V_RUN DF_TVS												
CheckList_1.5 p72; HR_v1.5 p476												



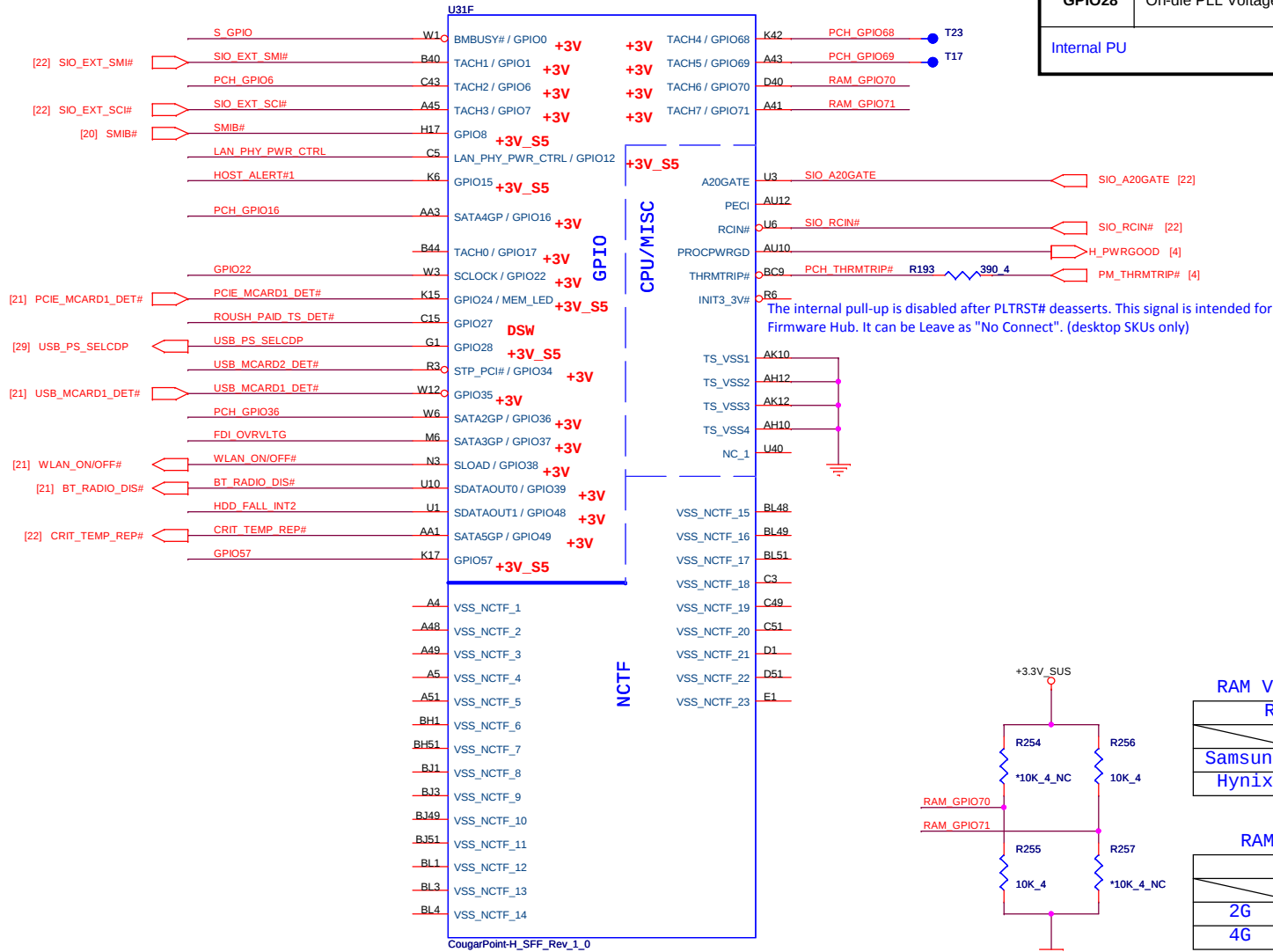
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For BIOS:
drop the PCH_SMB_ALERT from touchpad due to
SMBUS will control it by host notify mechanism



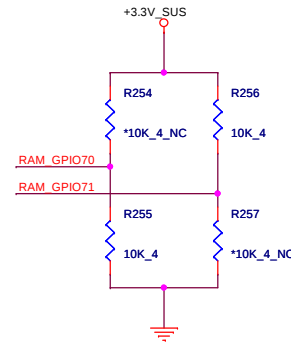
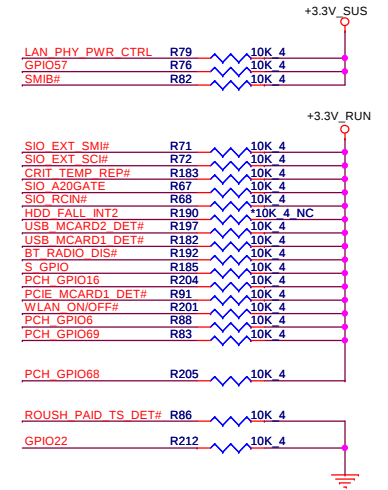
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Cougar Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
Internal PU		USB_PS_SELCDP	R215 *10K 4 NC

GPIO Pull-up/Pull-down(CLG)



RAM Vender select

RAM_GPIO70

	R254(1)	R255(0)
Samsung		V
Hynix	V	

RAM size select

RAM_GPIO71

	R256(1)	R257(0)
2G		V
4G	V	

FDI TERMINATION VOLTAGE OVERRIDE

Low - Tx, Rx terminated to same voltage

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

Reserve (PDC)

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

del 0527

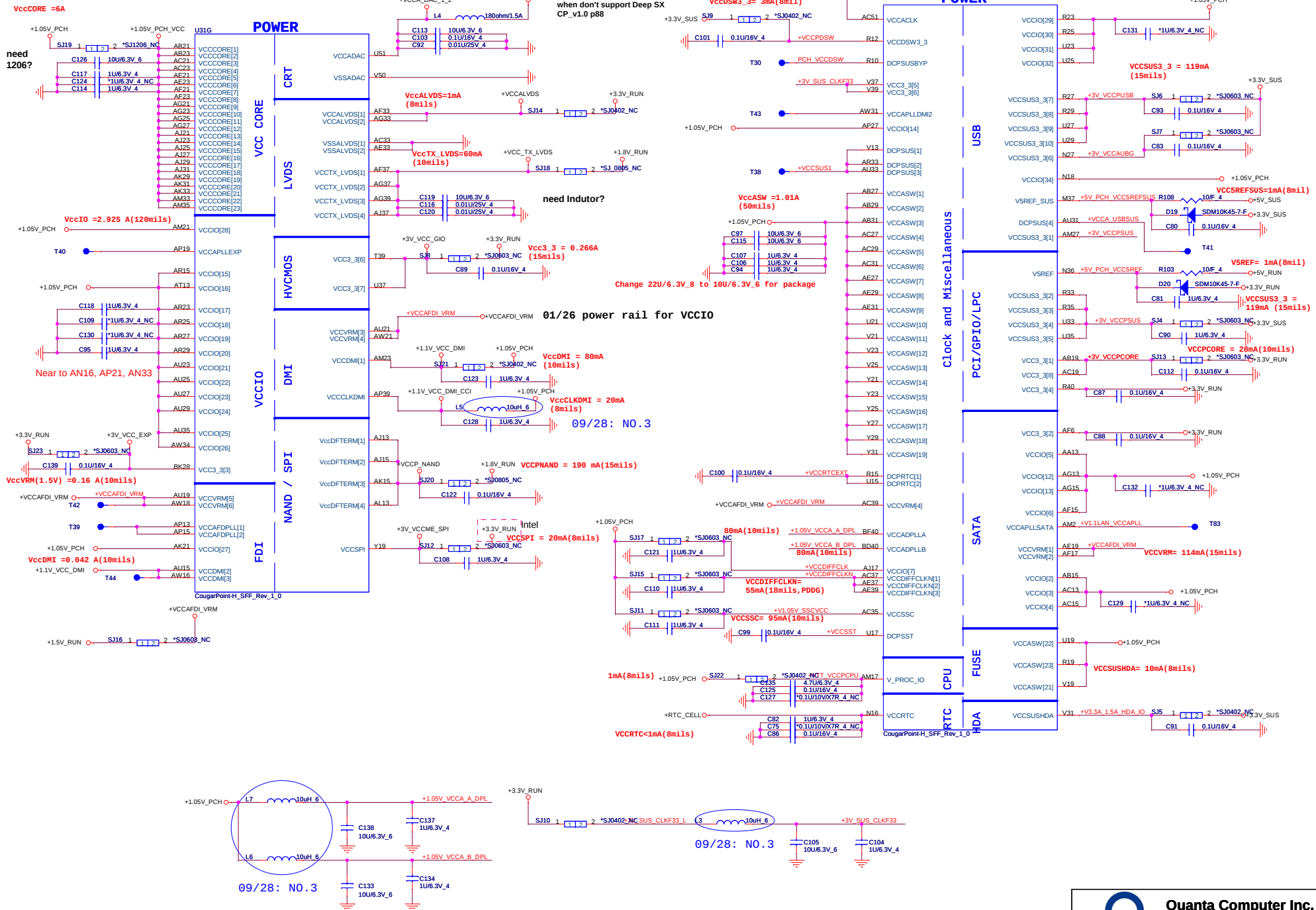


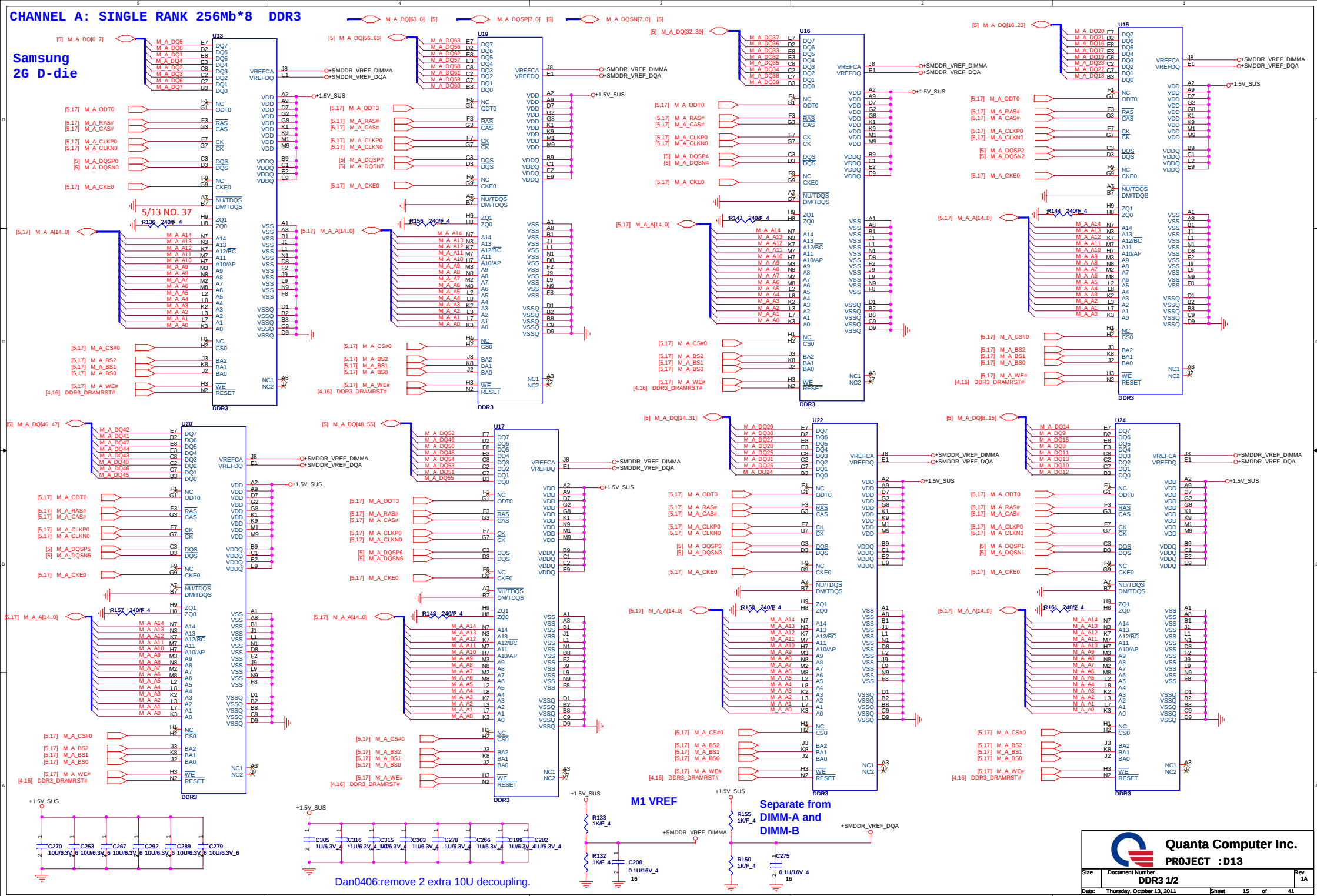
Quanta Computer Inc.

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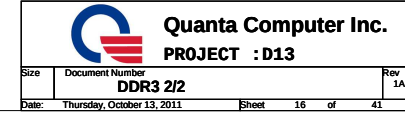
Cougar Point (POWER)

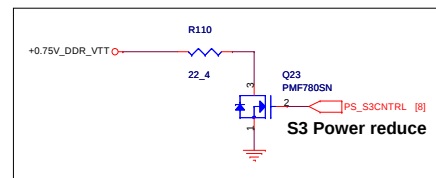
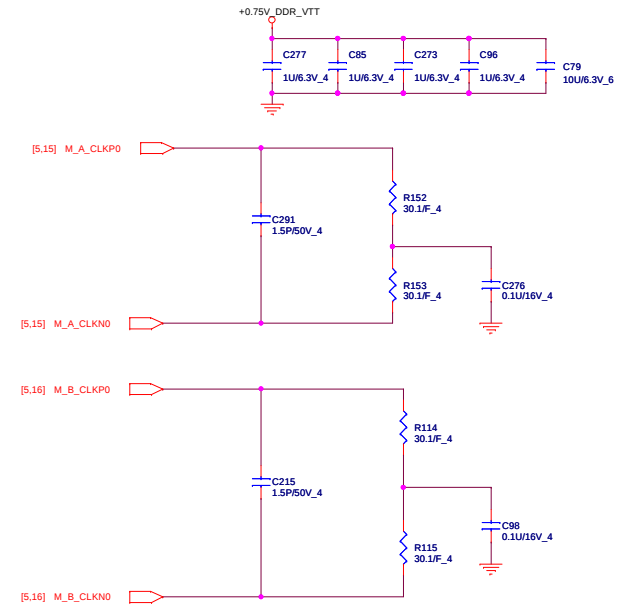
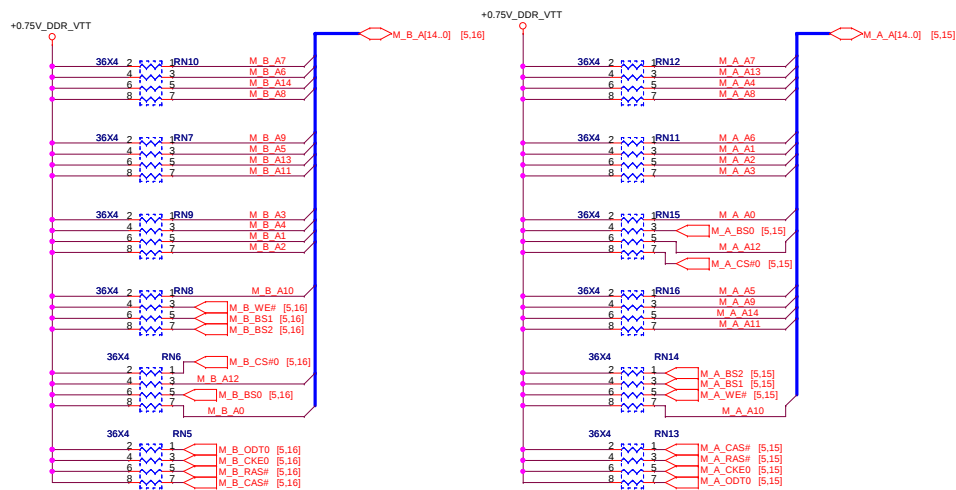
COUGAR POINT (POWER)



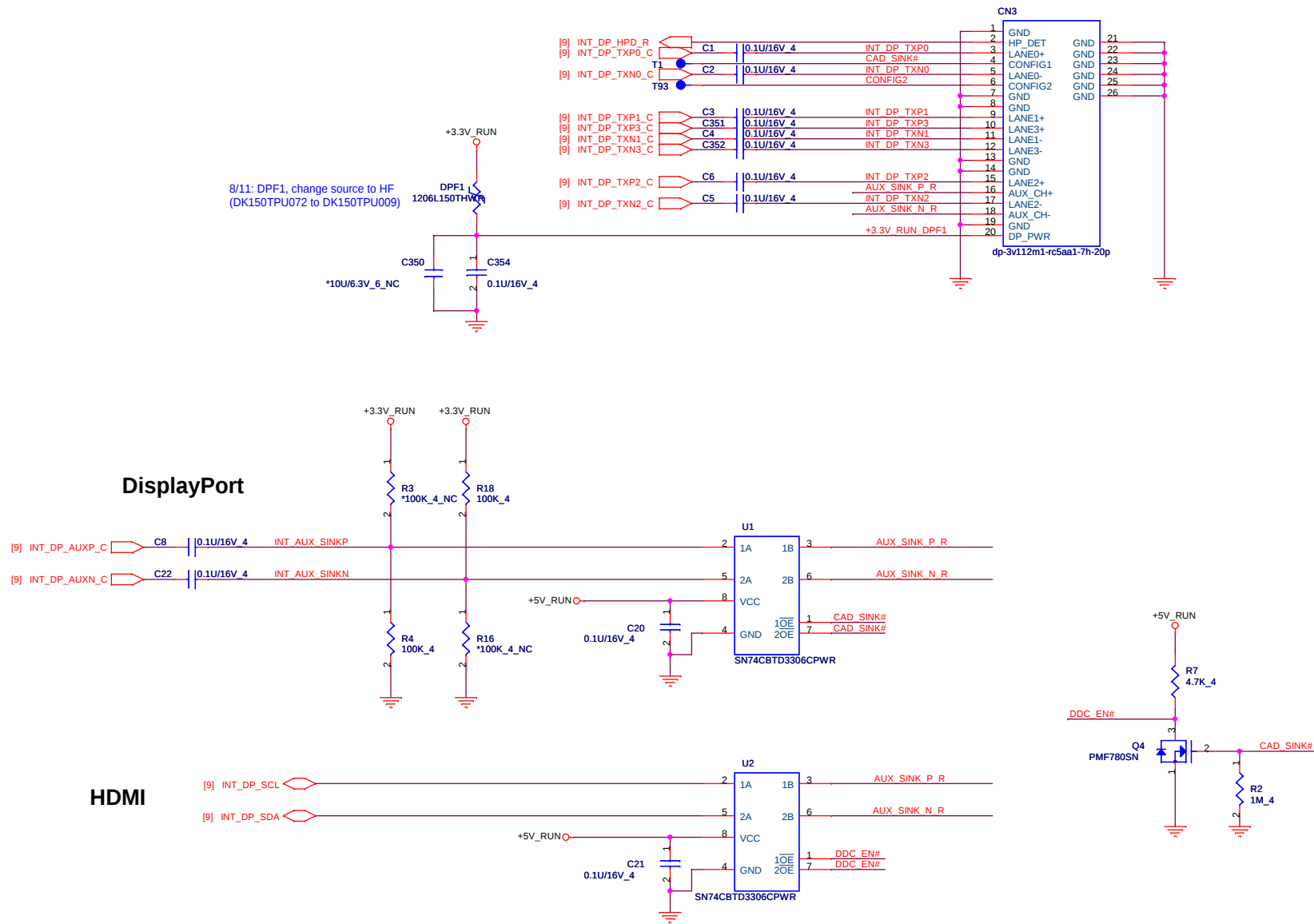


Samsung
2G D-die

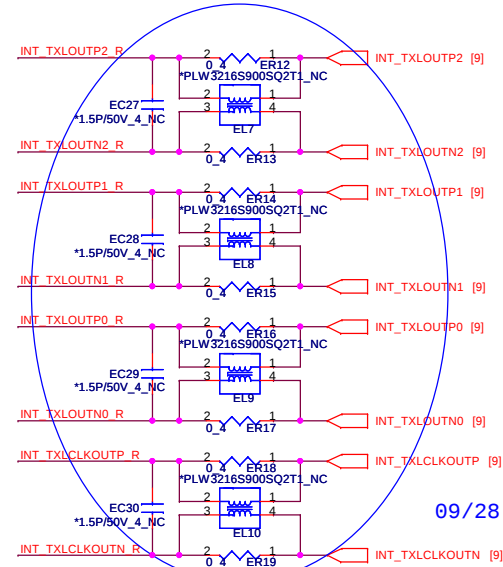
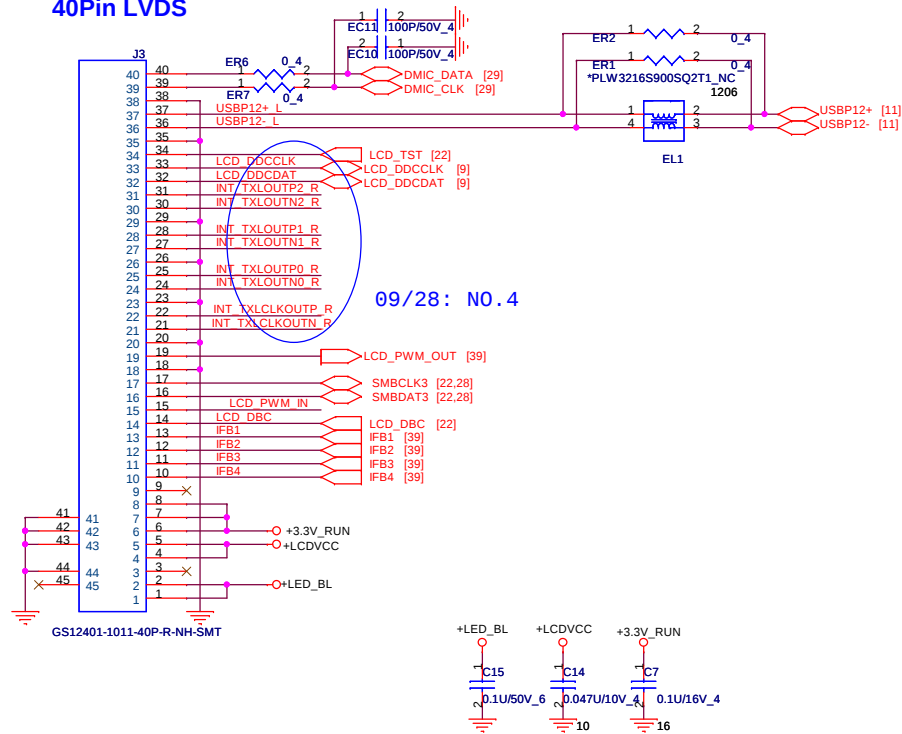




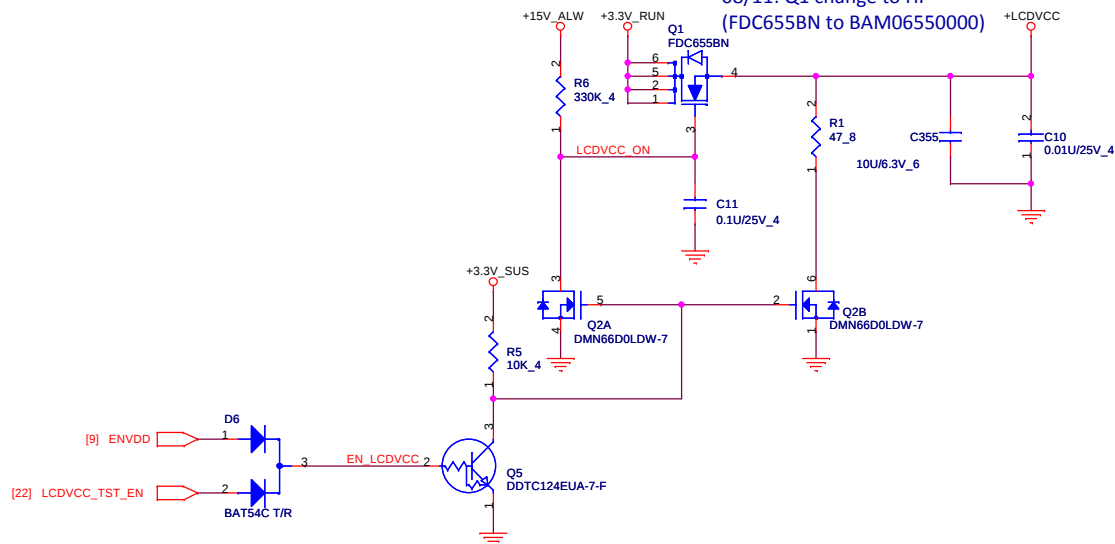
MINI DISPLAY PORT CONNECTOR



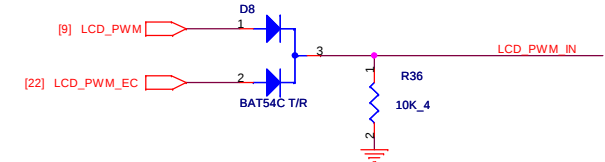
40Pin LVDS



08/11: Q1 change to HF
(FDC655BN to BAM06550000)



Brightness Control



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AVCC33X				PVCCA33X			
Min	Typ	Max		Min	Typ	Max	
3.15V	3.30V	3.45V		3.15V	3.30V	3.45V	
Current = 36mA				Current = 72mA			

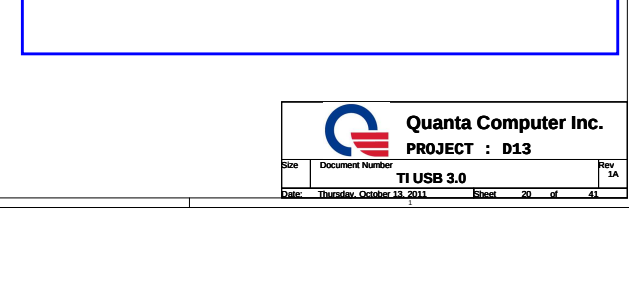
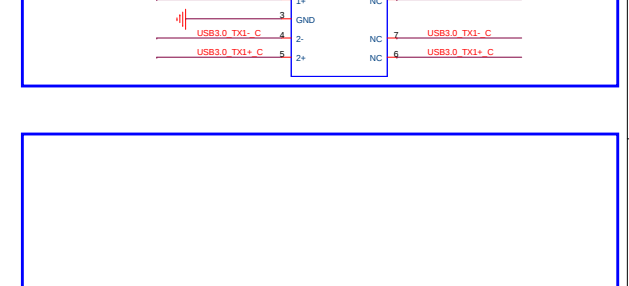
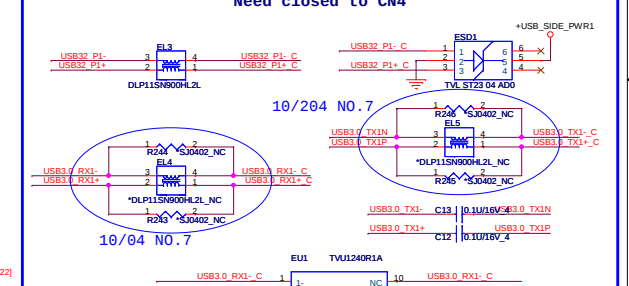
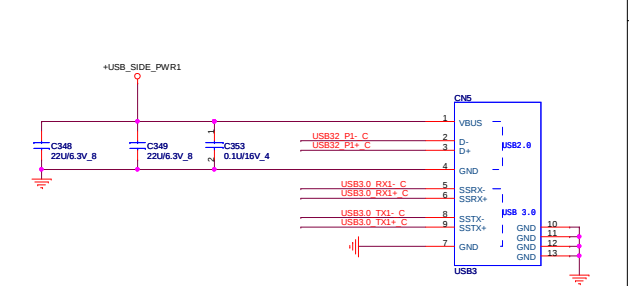
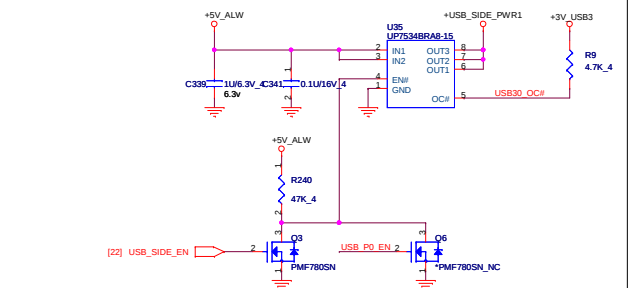
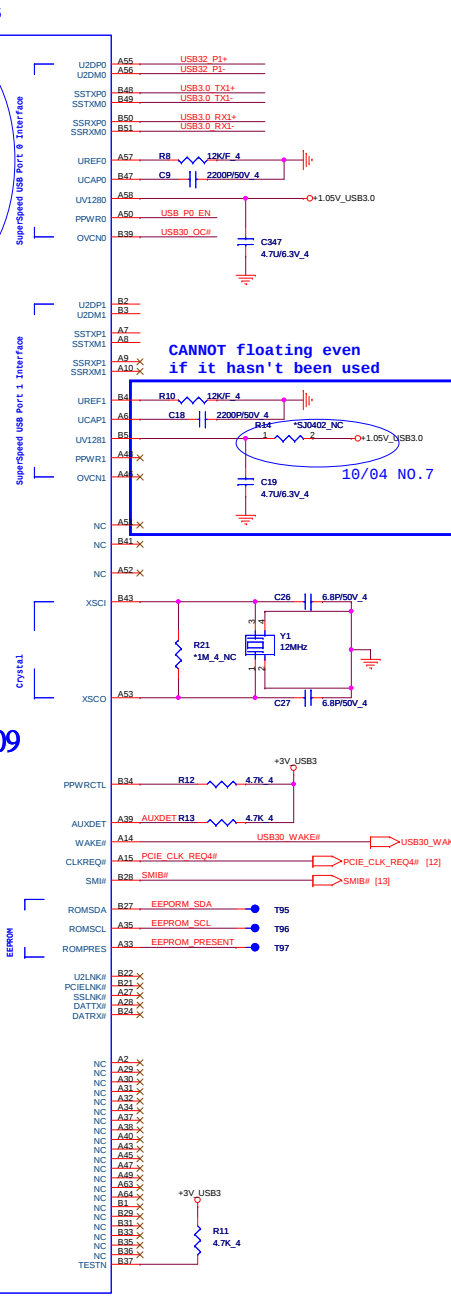
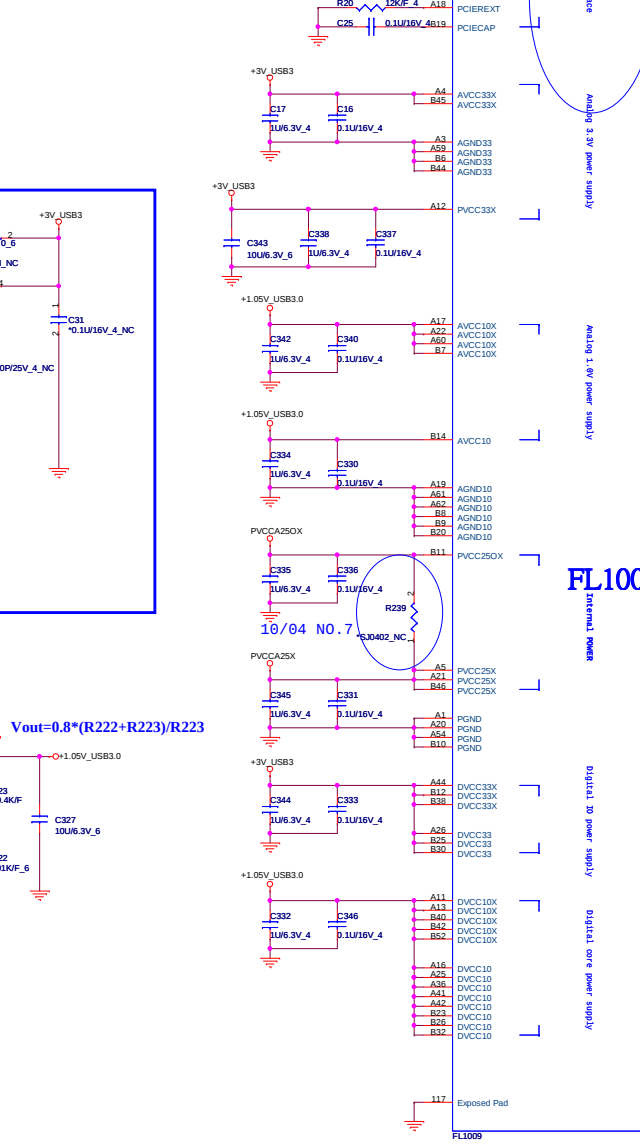
AVCC18X				AVCC10			
Min	Typ	Max		Min	Typ	Max	
1.08V	1.05V	1.10V		1.08V	1.05V	1.10V	
Current = 164mA				Current = 9mA			

DVCC33X				DVCC33			
Min	Typ	Max		Min	Typ	Max	
2.97V	3.30V	3.63V		2.97V	3.30V	3.63V	
Current = 9mA				Current = 5mA			

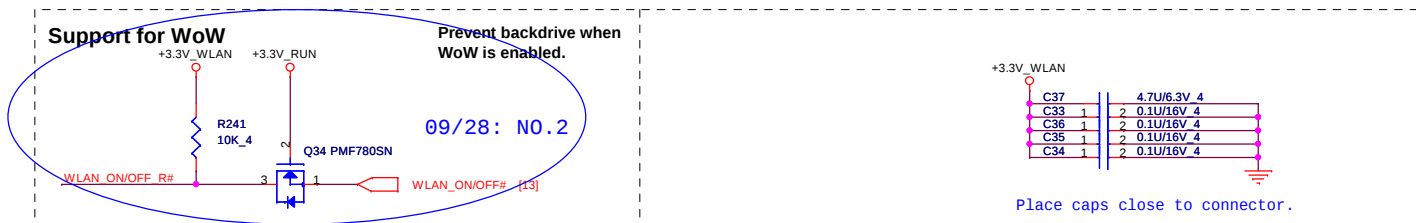
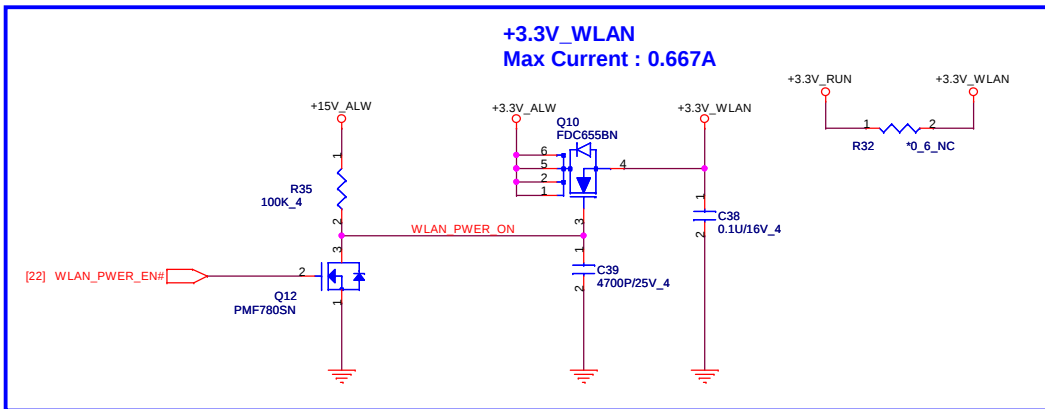
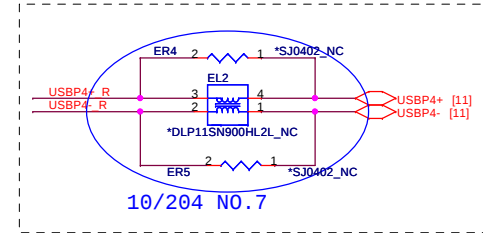
DVCC18X				DVCC10			
Min	Typ	Max		Min	Typ	Max	
1.08V	1.05V	1.10V		1.08V	1.05V	1.10V	
Current = 25mA				Current = 99mA			

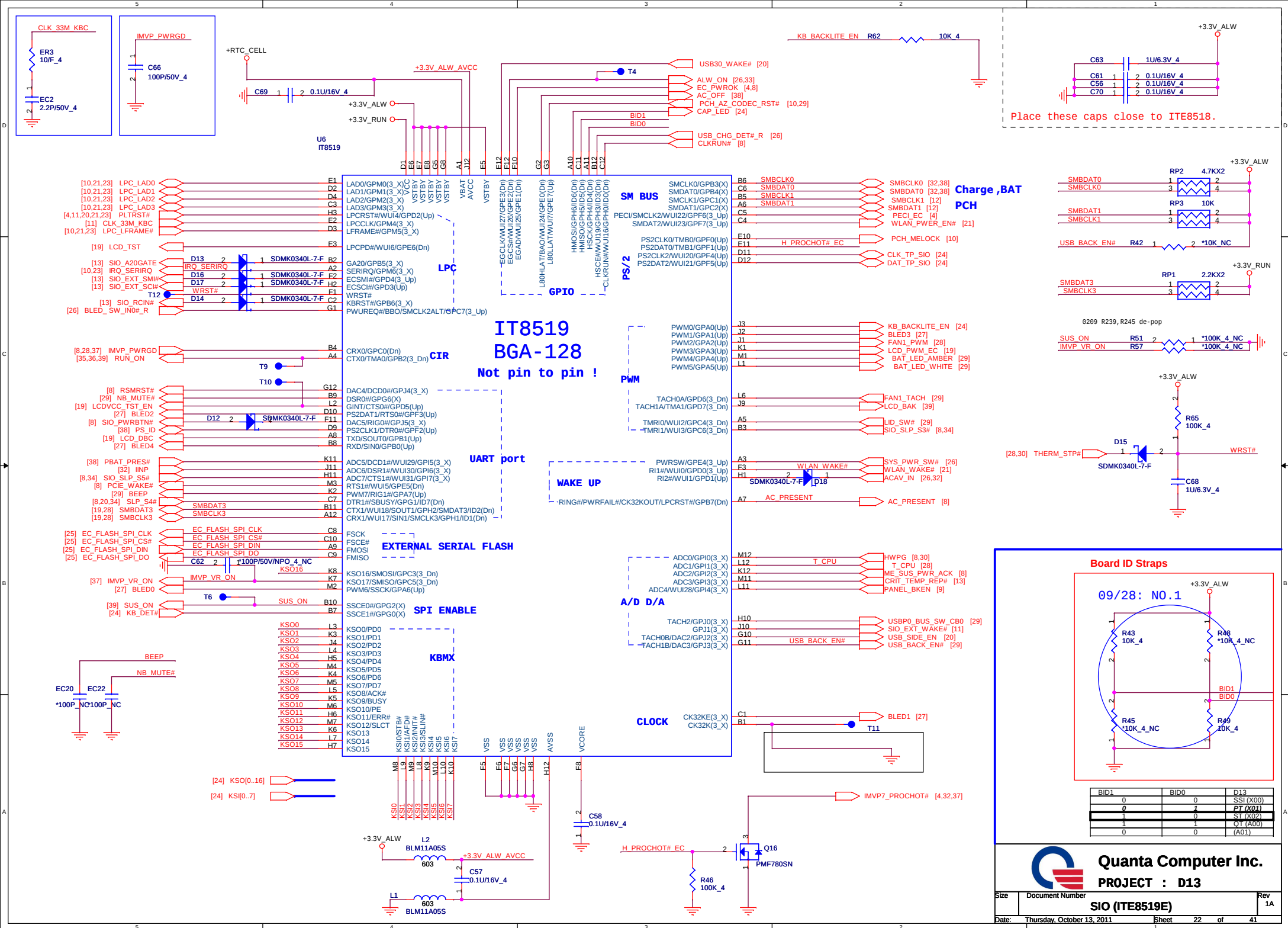
09/28: NO.5

TX base on FL1009
RX base on FL1009



MiniCard WLAN connector



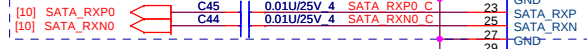


mSATA Connector

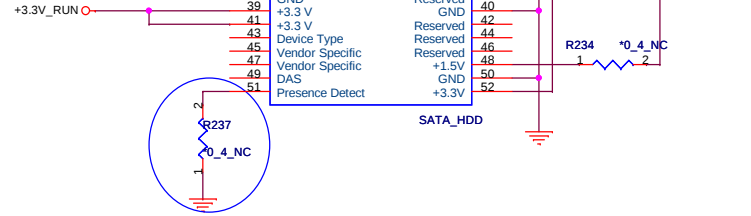
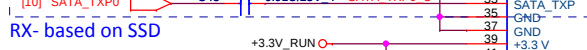
+5V_RUN is for testing mSATA by factory.
+1.5V are NC pin for this connector.

Max = 6000 mils
Min = 1000 mils
DG: Place TX cap close to connector

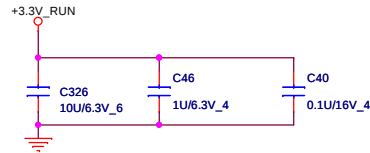
TX- based on SSD



RX- based on SSD

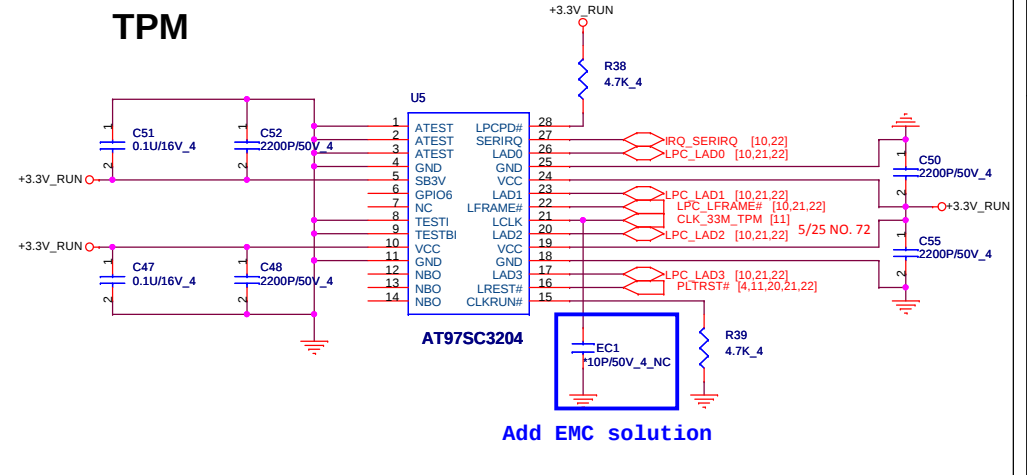


10/204 NO.7



Place caps close to connector.

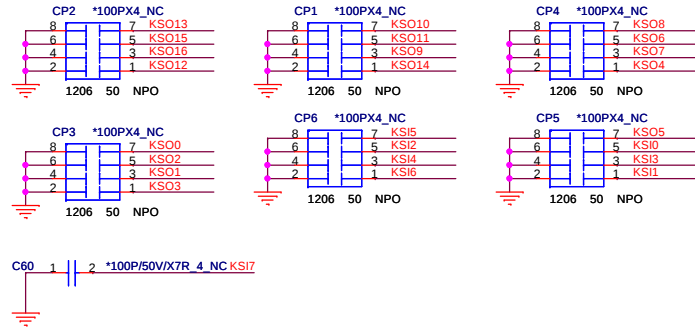
TPM



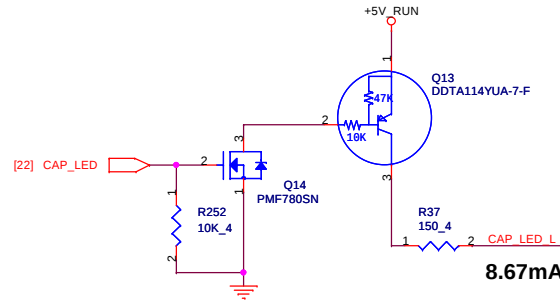
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KEYBOARD CONNECTOR

03/30 Change CP1,CP2,CP3,CP4,CP5,CP6,C382 from Pop to Depop

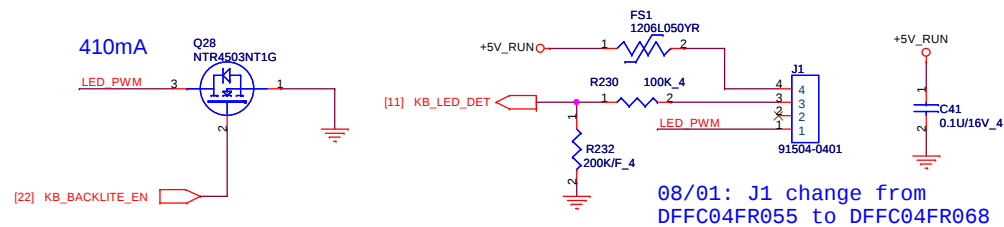


$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$

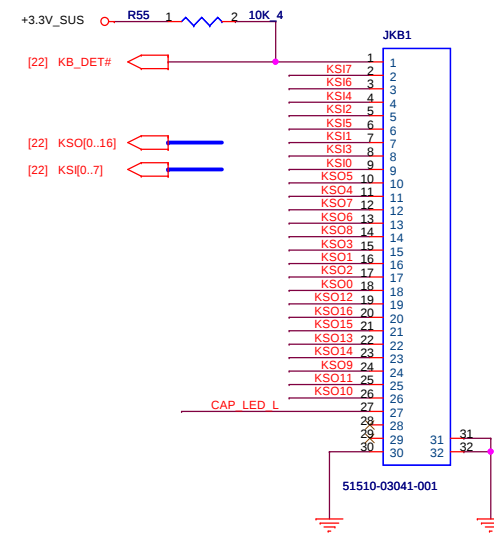


Key board illumination

+KB_LED power trace width >10 mil

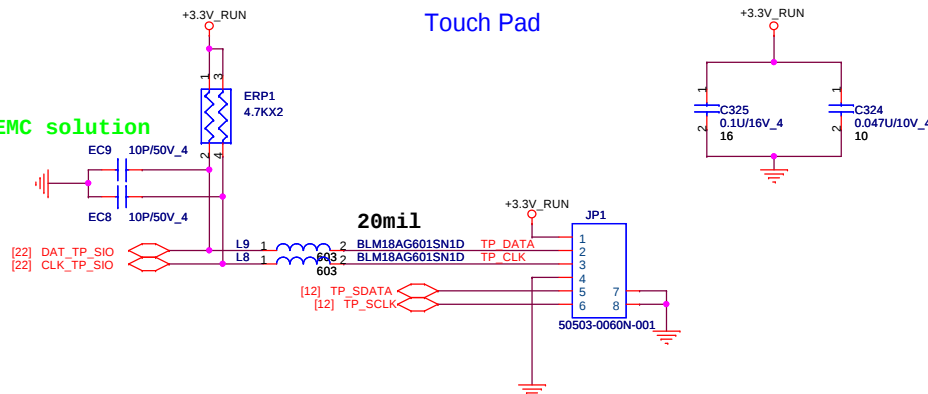


KEYBOARD CONNECTOR



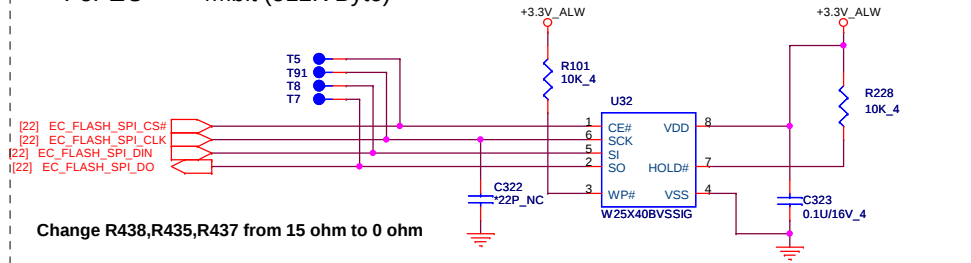
Touch Pad

Add EMC solution

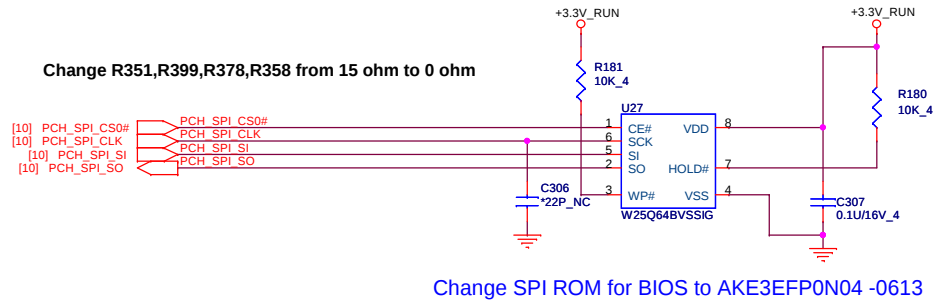


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For EC 4Mbit (512K Byte)

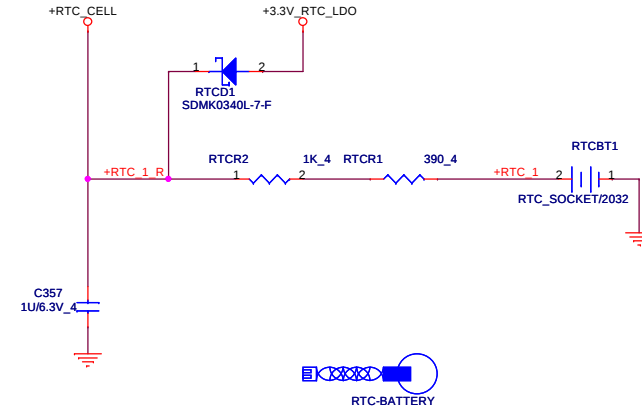


For PCH 64Mbit (8M Byte)



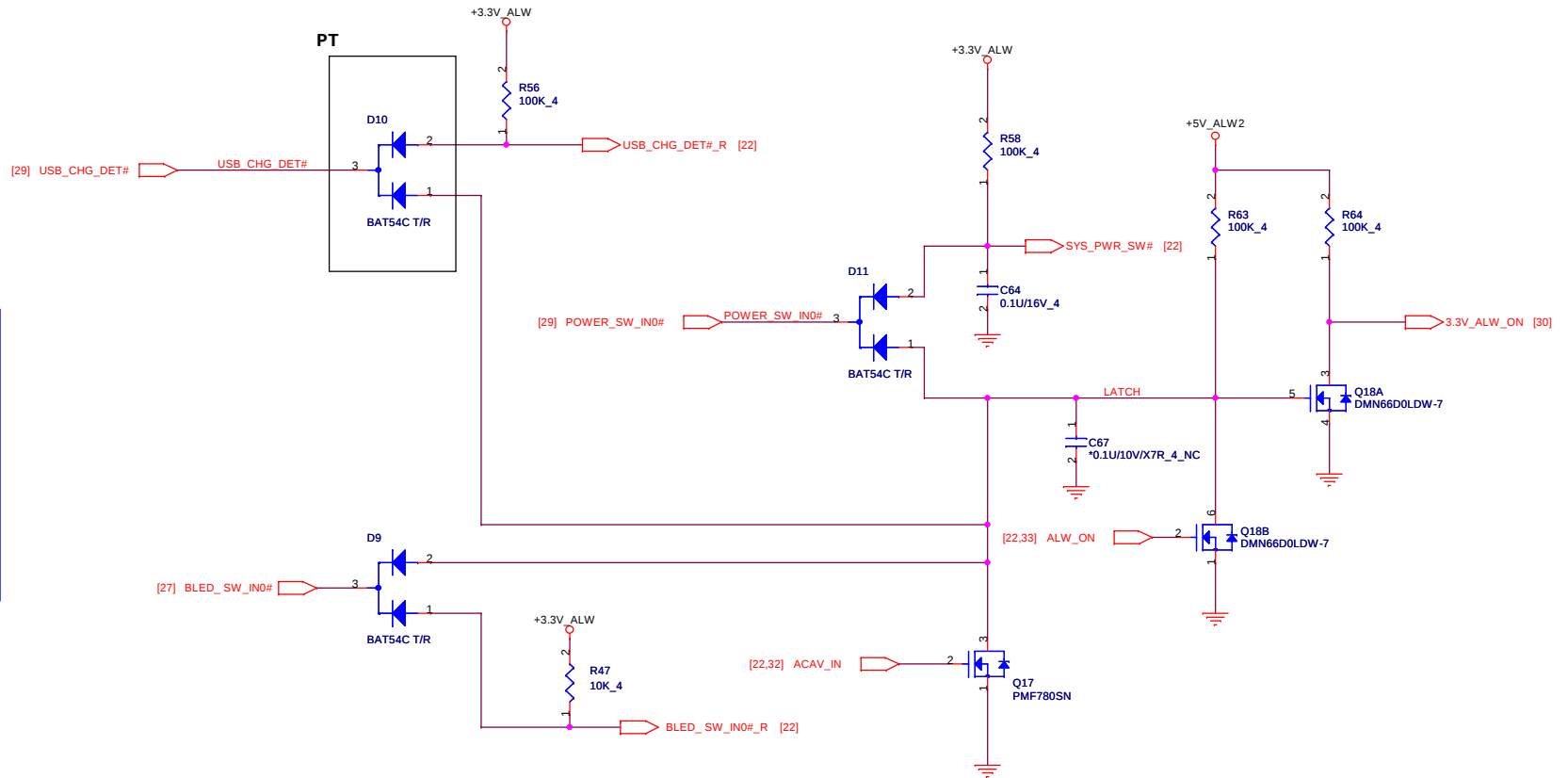
RTC BATTERY

The max charge current is flow on charged at the end voltage of battery
2V. And the charge current is 1mA.
 $R \geq (+RTC_CELL - 2)/1mA$



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3VALW ON POWER LOGIC

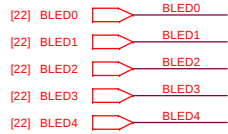


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PWR SW/LED

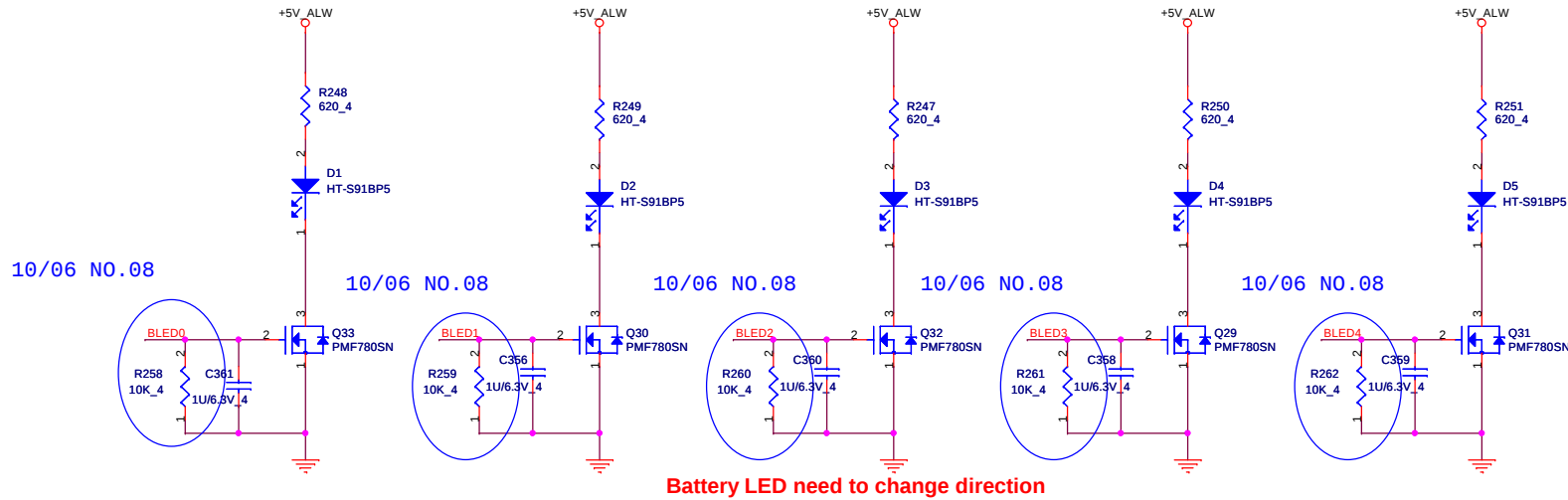
Battery Status LED



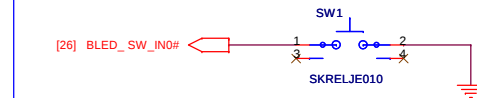
Truth table of Battery LED

Battery Power State	BLED4	BLED3	BLED2	BLED1	BLED0	LED State
<20%	0	0	0	0	0	N/A
20%	0	0	0	0	1	D29
40%	0	0	0	1	1	D29 D30
60%	0	0	1	1	1	D29 D30 D31
80%	0	1	1	1	1	D29 D30 D31 D32
100%	1	1	1	1	1	D29 D30 D31 D32 D33

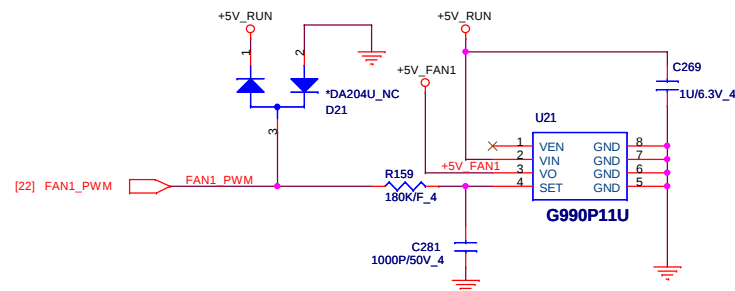
10/14, change current limit resistor from 365 ohm to 620



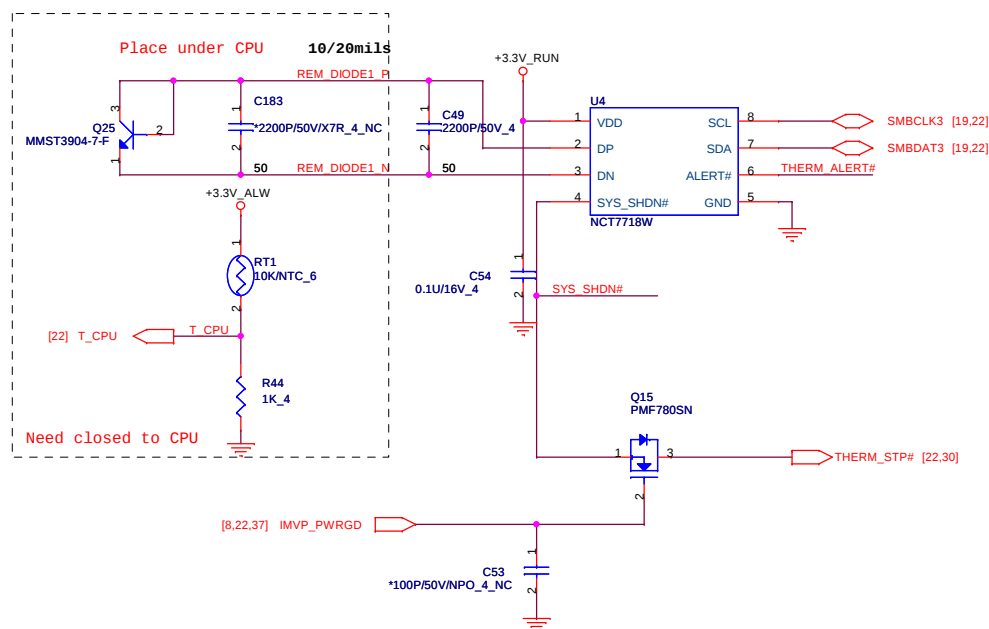
Battery LED button



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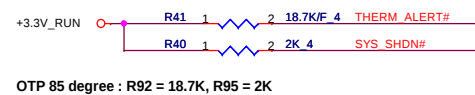


THERMAL IC



SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77 'C	87 'C	97 'C	107 'C	117 'C
7.5K	79 'C	89 'C	99 'C	109 'C	119 'C
10.5K	81 'C	91 'C	101 'C	111 'C	121 'C
14K	83 'C	93 'C	103 'C	113 'C	123 'C
18.7K	85 'C	95 'C	105 'C	115 'C	125 'C

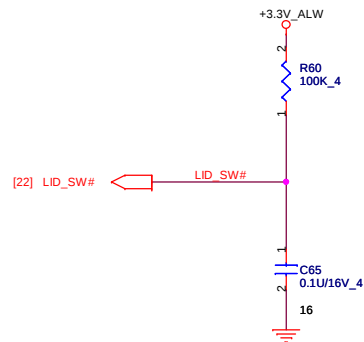
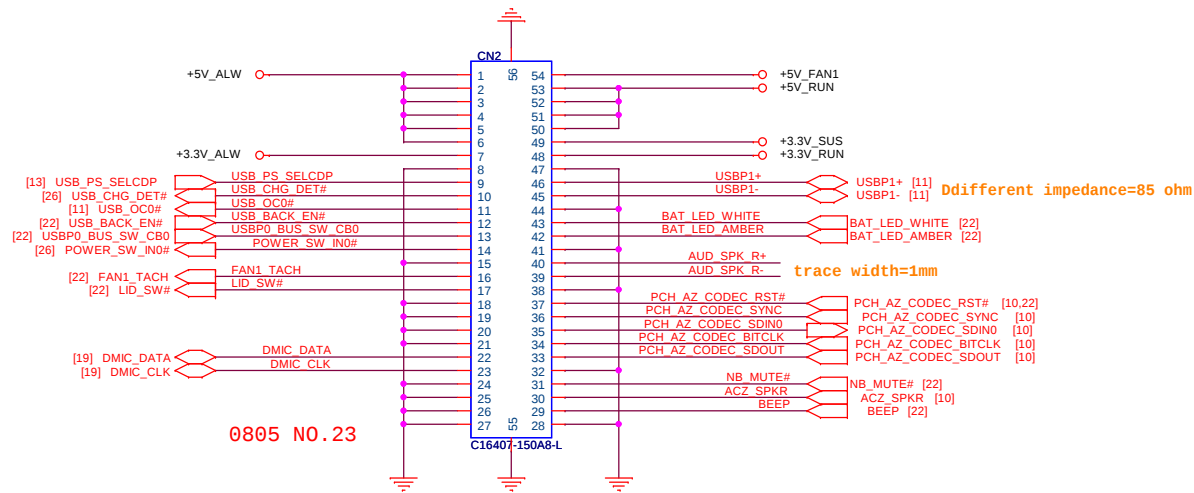
OTP 85 degree C



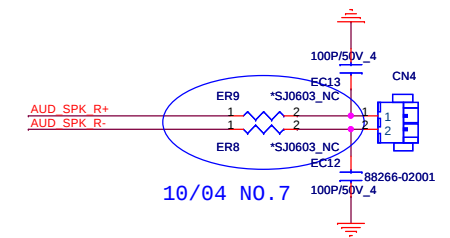
OTP 85 degree : R92 = 18.7K, R95 = 2K



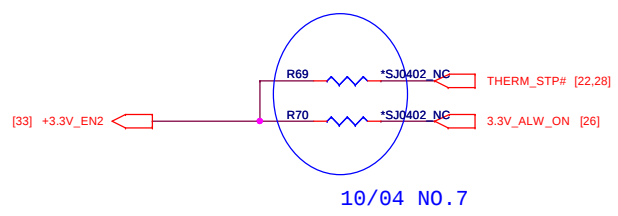
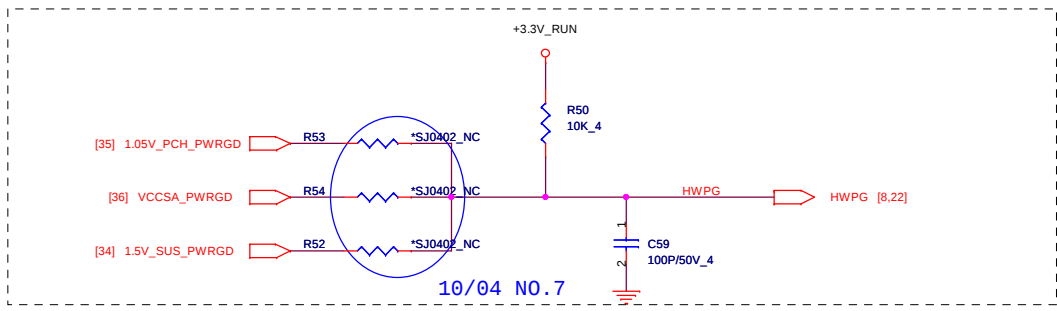
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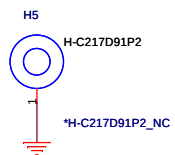
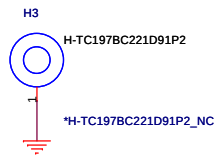
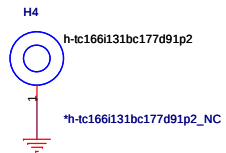


08/01: change CN4 PN from DFHD02MR401 change to DFHD02MR045

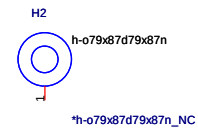
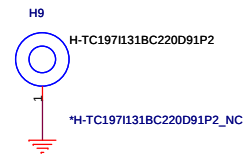
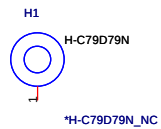
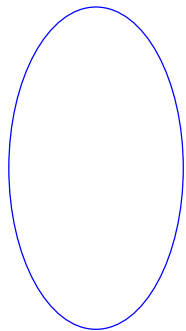


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09/30: NO.6



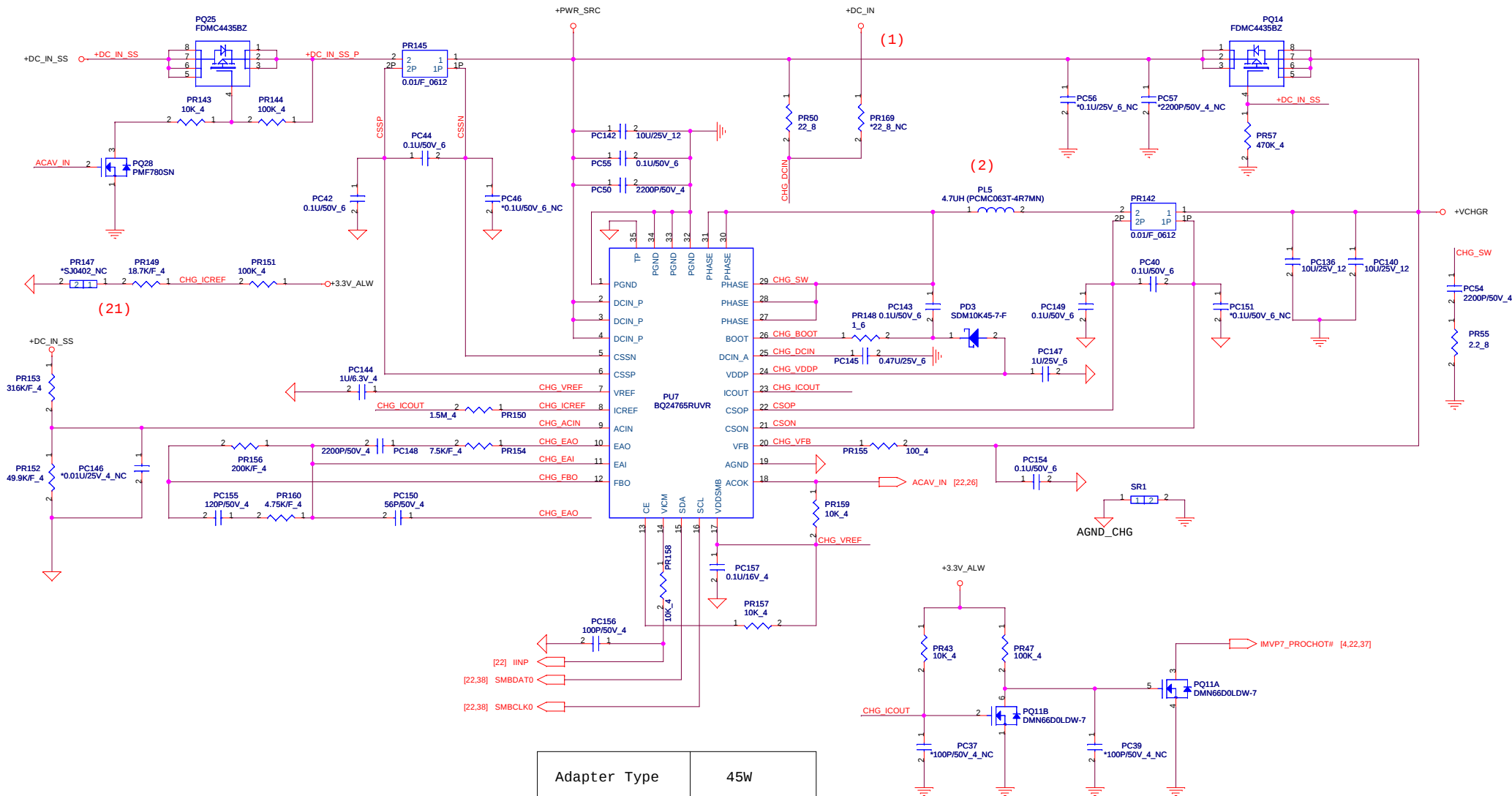
Need to add in BOM			
H7 h-tc217bc197d102p2 h-tc217bc197d102p2 H11 h-tc217bc197d102p2 h-tc217bc197d102p2	H8 h-tc217bc197d102p2 h-tc217bc197d102p2 H12 h-tc217bc197d102p2 h-tc217bc197d102p2	H6 h-tc217bc197d102p2 h-tc217bc197d102p2	H10 H-C220D142P2 H-C220D142P2 TOP-Size

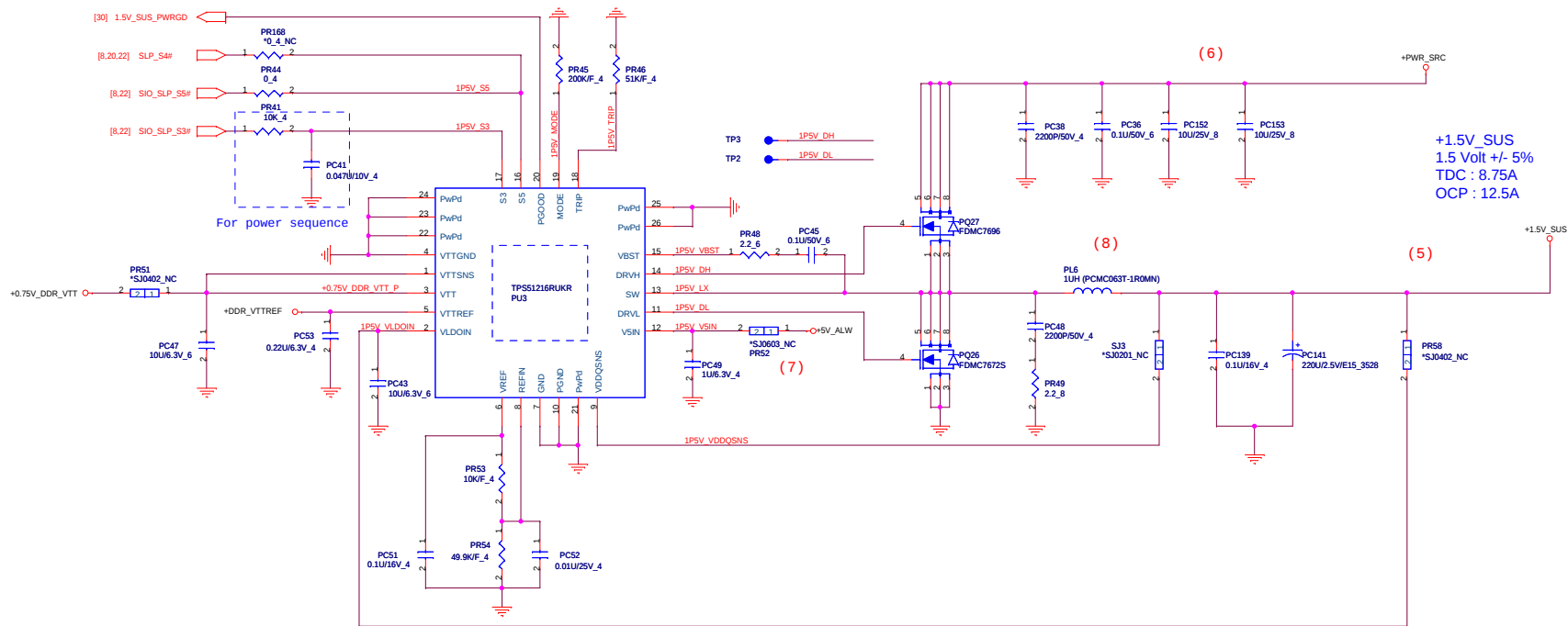
**BOT-Size
Need to modify PN**

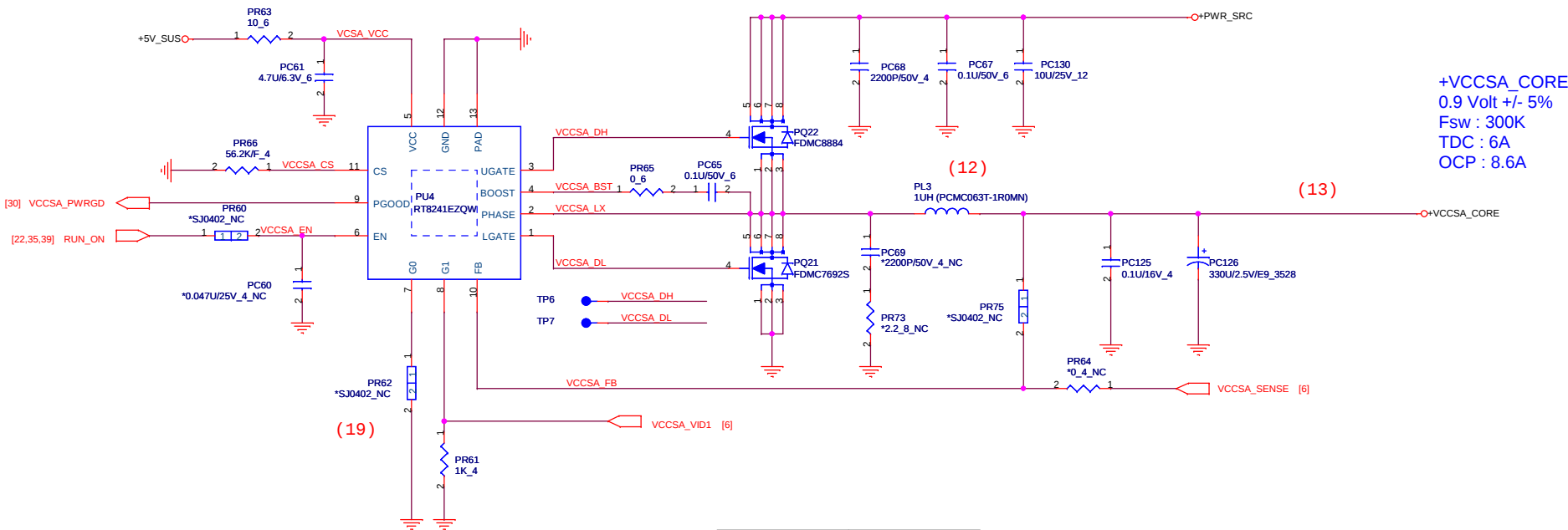


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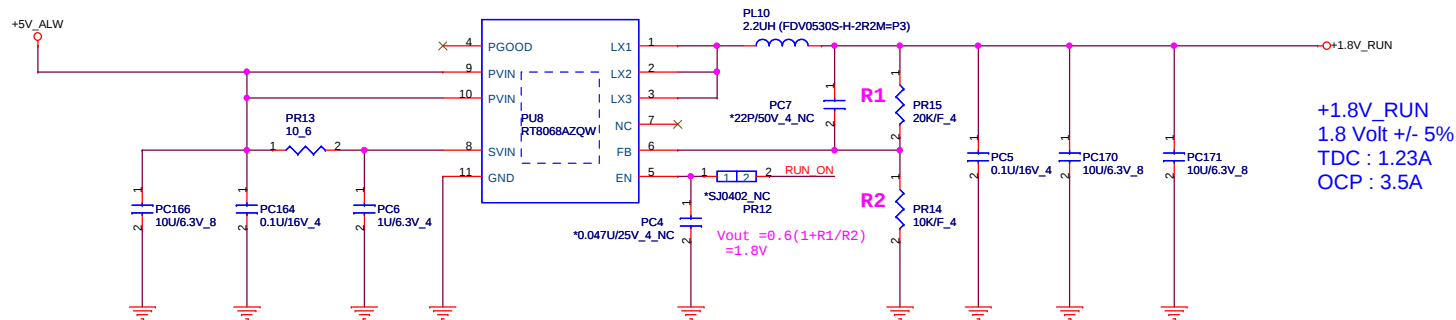
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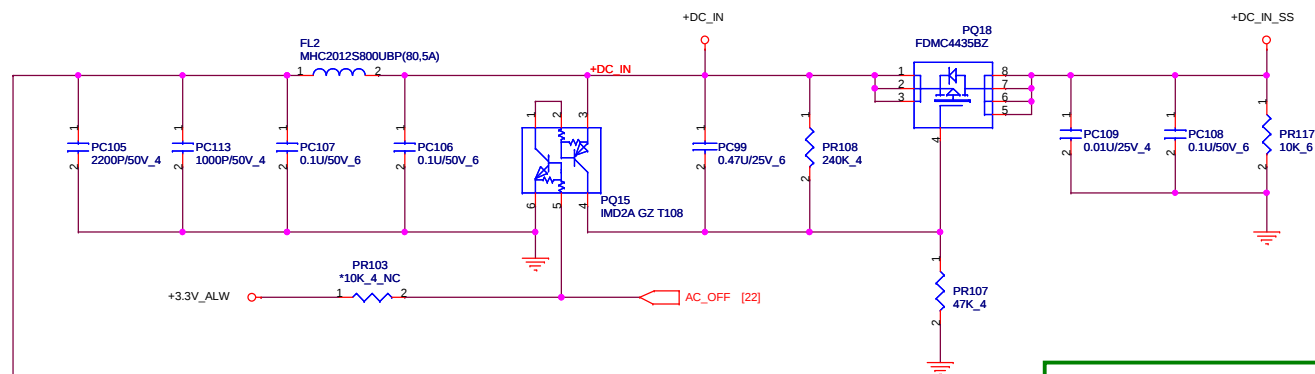
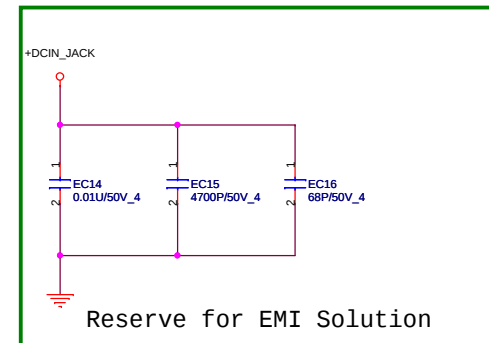
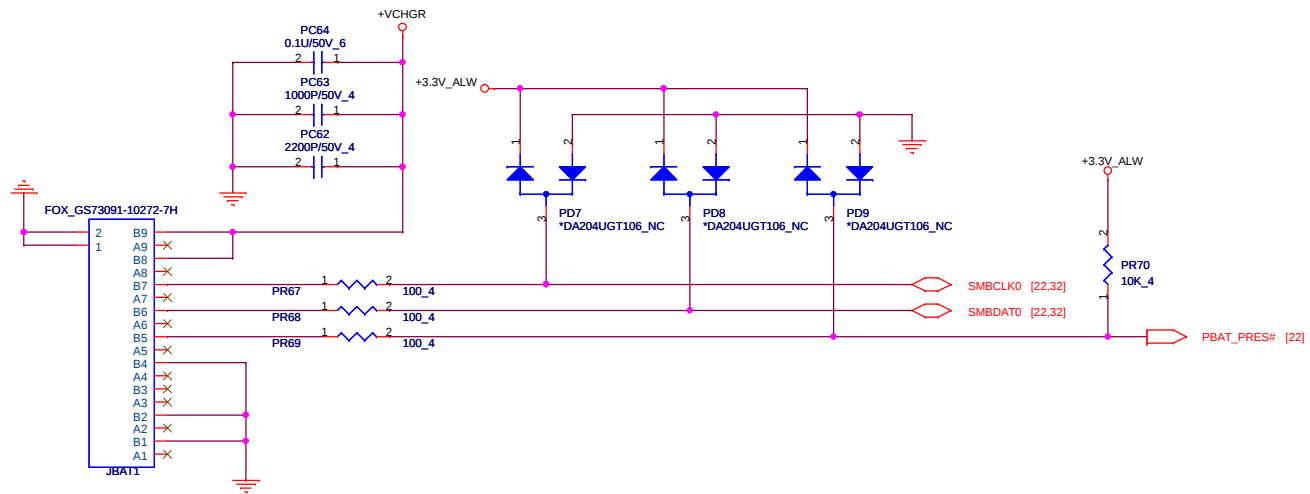




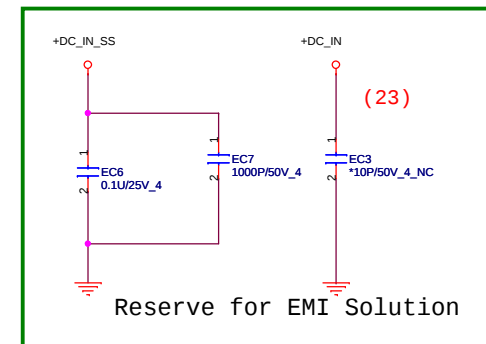
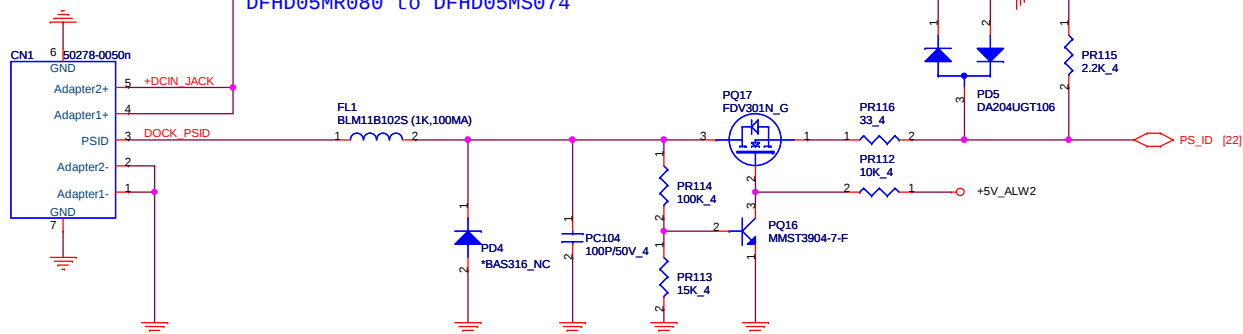


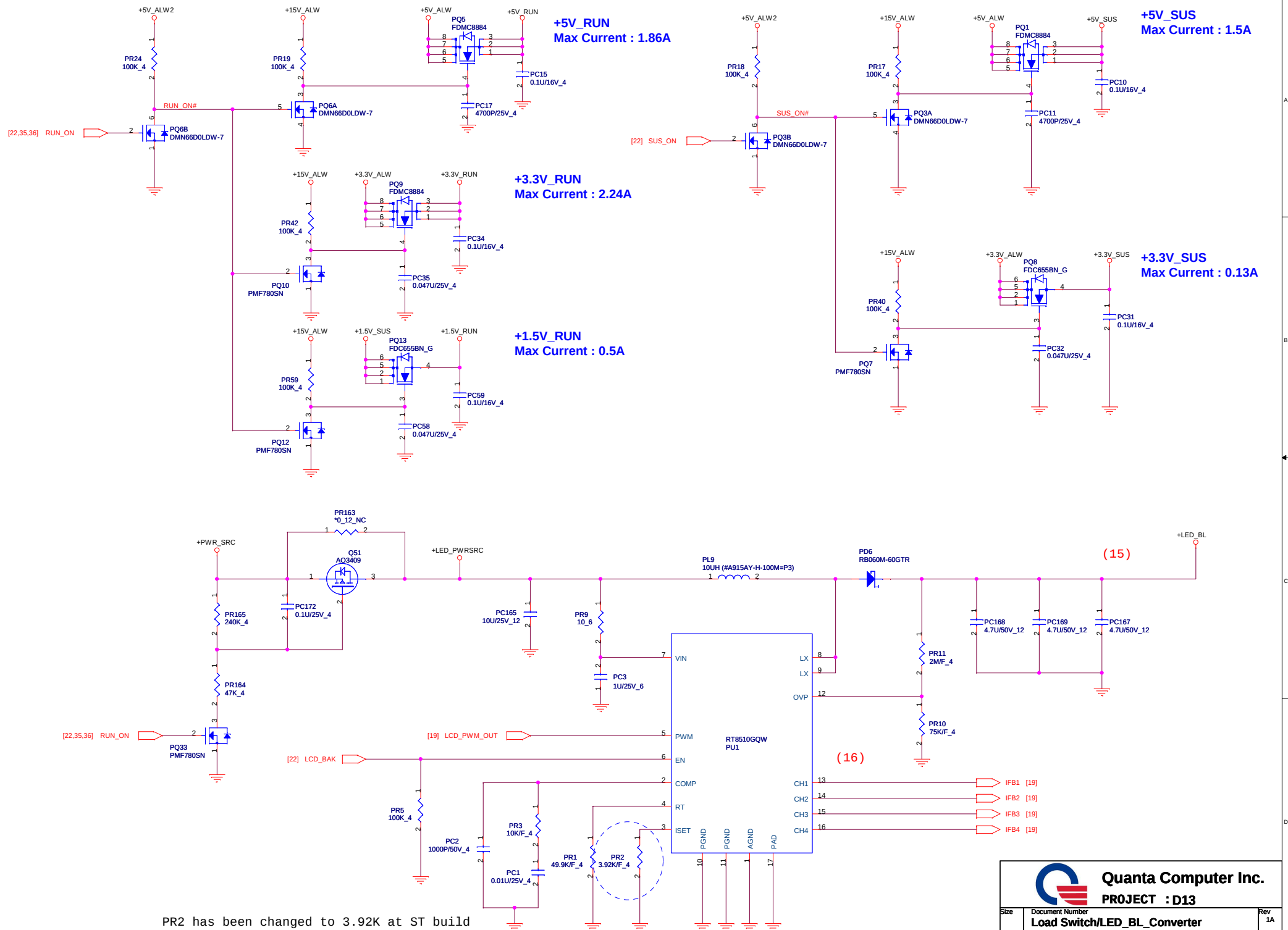
VCCSA_VID1	VCCSA_CORE
Low	0.9V
High	0.85V

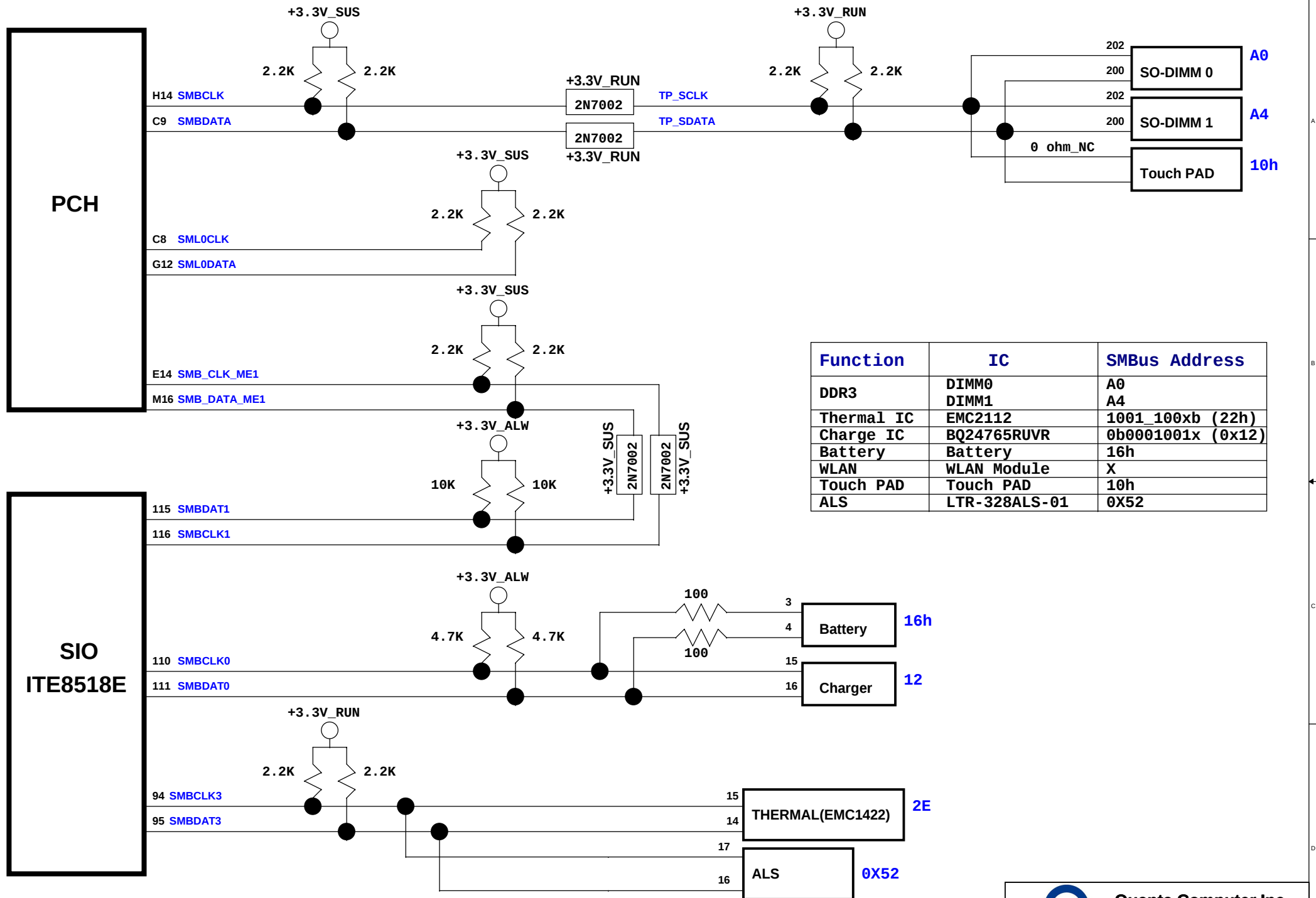




9/30: CN1 change from D
DFHD05MR080 to DFHD05MS074







Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
Thermal IC	EMC2112	1001_100xb (22h)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
WLAN	WLAN Module	X
Touch PAD	Touch PAD	10h
ALS	LTR-328ALS-01	0X52

