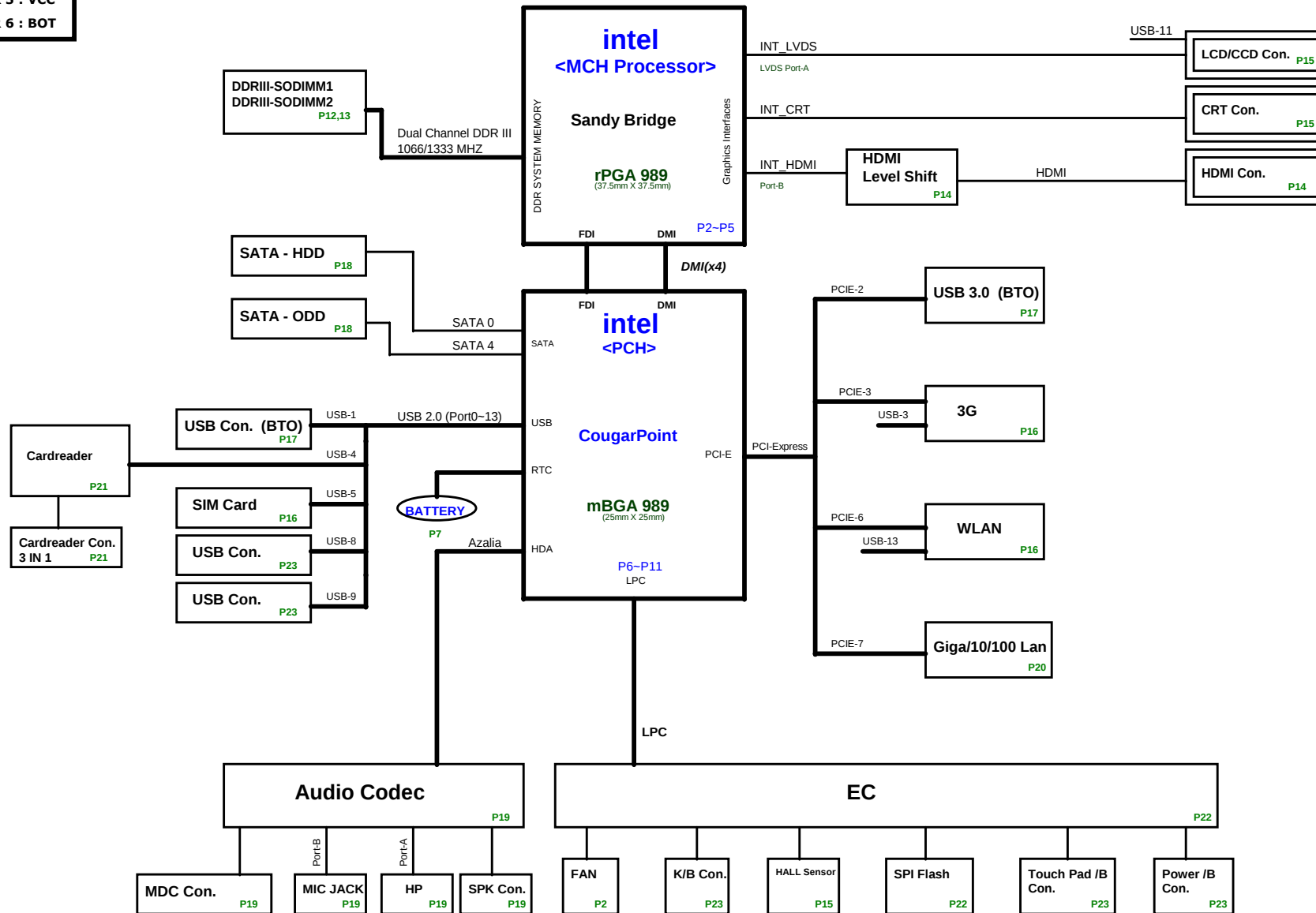


BLB Block Diagram

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



POWER SYSTEM

ISL88731CHRTZ-T P. 25
ISL95835HRTZ-T P. 30
RT8207LGQW P. 27
RT8240BGQW P. 28
G9661-25ADJF12U P. 31
PM6686TR P. 26
ISL95870AHRUZ-T P. 29

+VCC_CORE

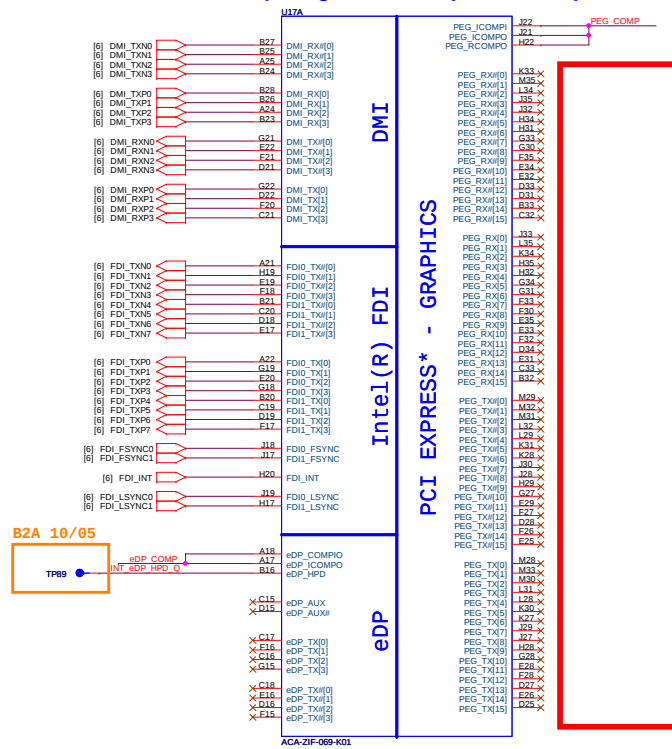
+1.5V
+1.5VSUS

+VTT
+1.05V

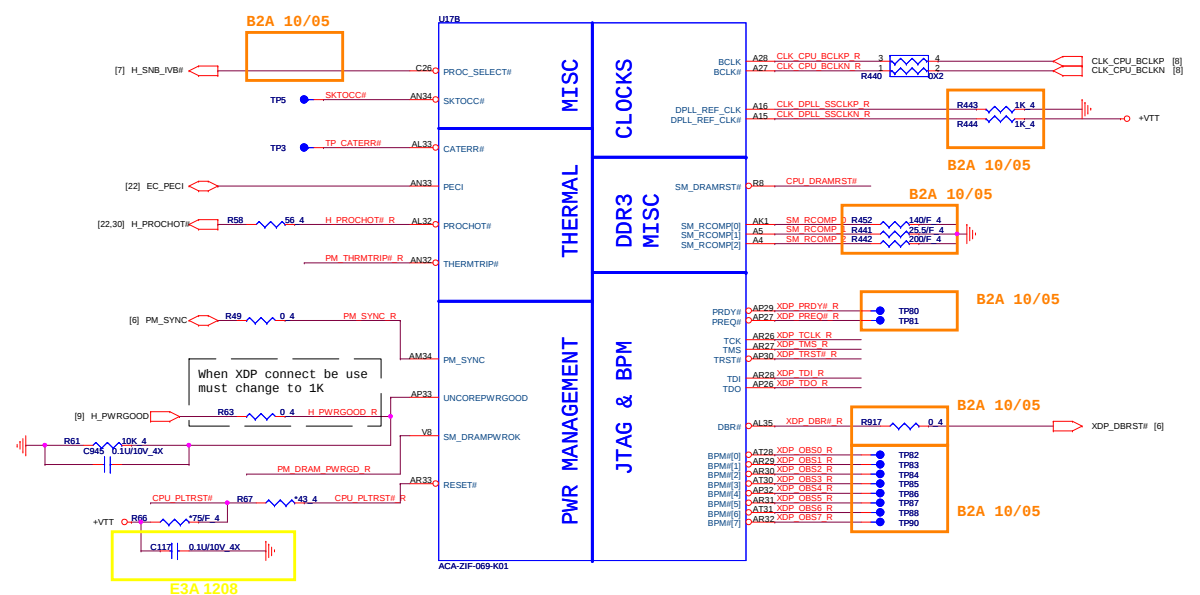
+1.8V

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF
+VGPU_CORE
+VAXG
+VCCSA

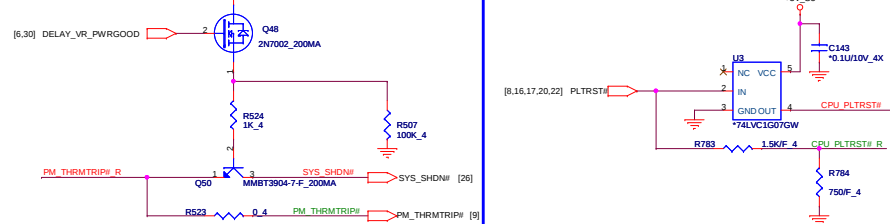
Sandy Bridge Processor (DMI,PEG,FDI) <CPU>



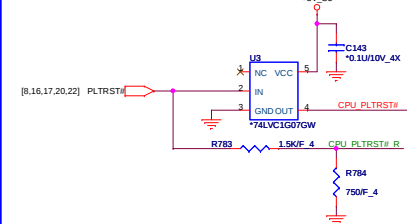
Sandy Bridge Processor (CLK,MISC,JTAG) <CPU>



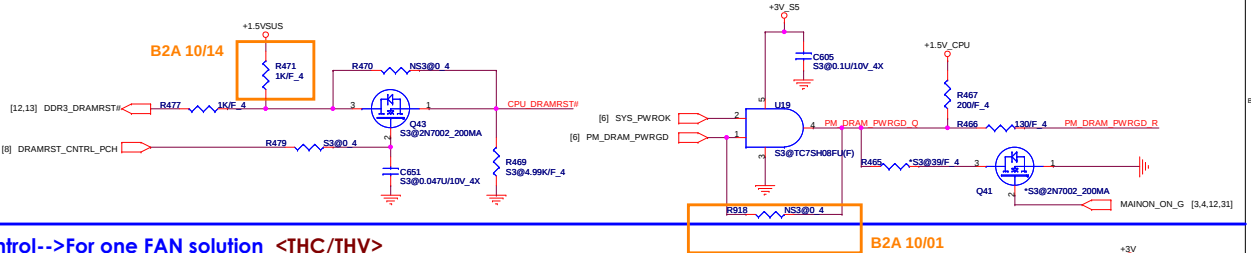
Thermal Trip <CPU>



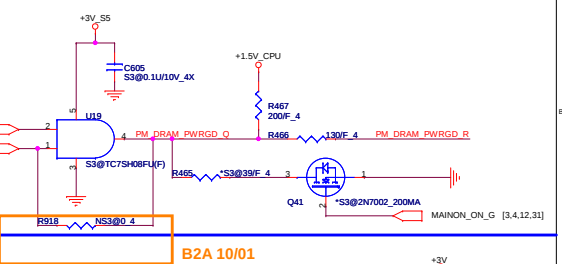
Level Shift <CPU>



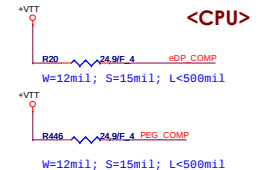
S3 Power Reduction (SM_DRAMRST#) <S3P>



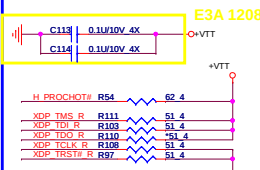
S3 Power Reduction (SM_DRAMPWROK) <S3P>



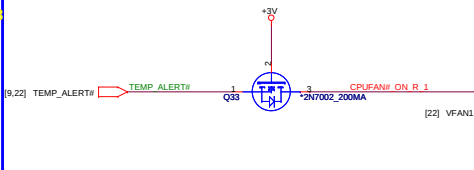
DP & PEG Compensation



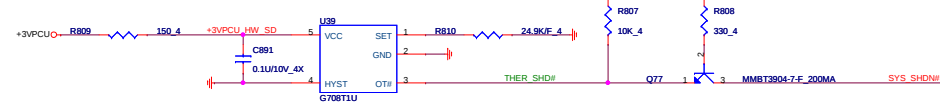
Processor pull-up <CPU>



FAN Control-->For one FAN solution <THC/THV>



CPU Thermal sensor / MB Local TEMP <THC>



Rset(Kohm)=0.0012T*-0.9308T+96.147, Shut down on 86dgree
Hysteresis is 30C

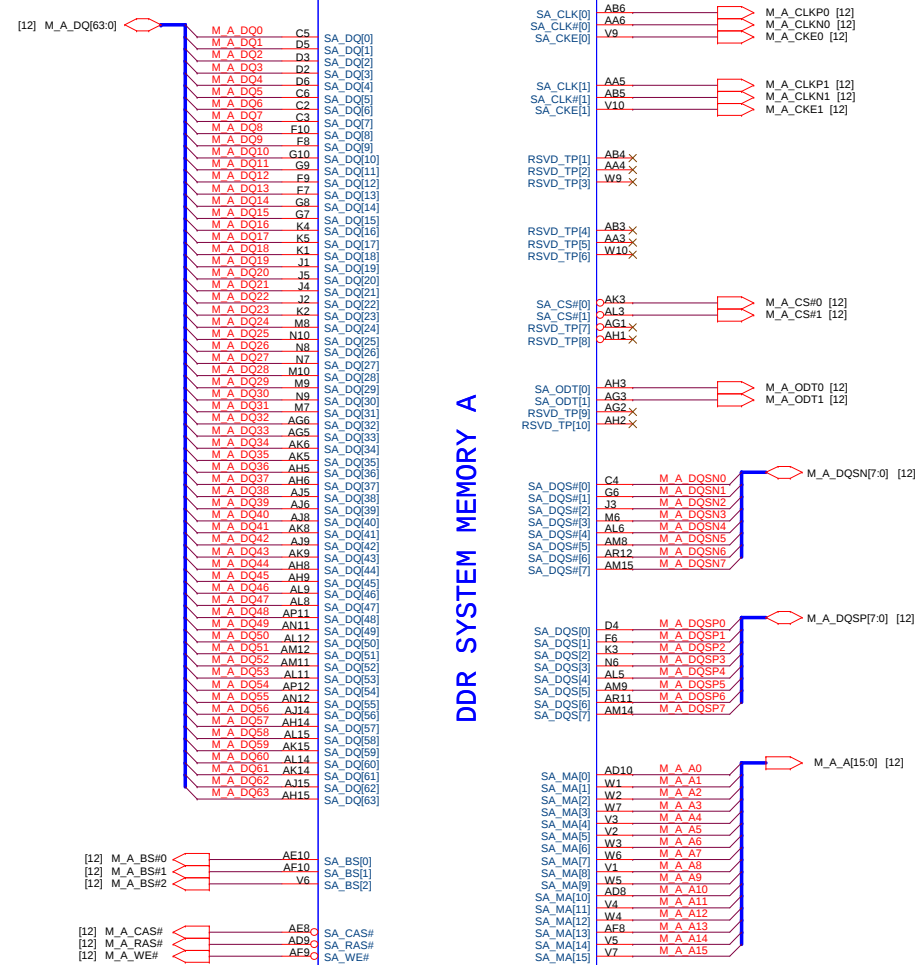
Sandy Bridge Processor (DDR3) <CPU>

03

U17C

DDR SYSTEM MEMORY A

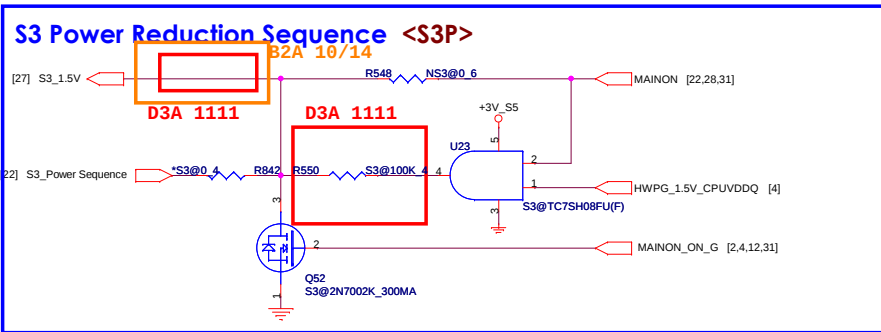
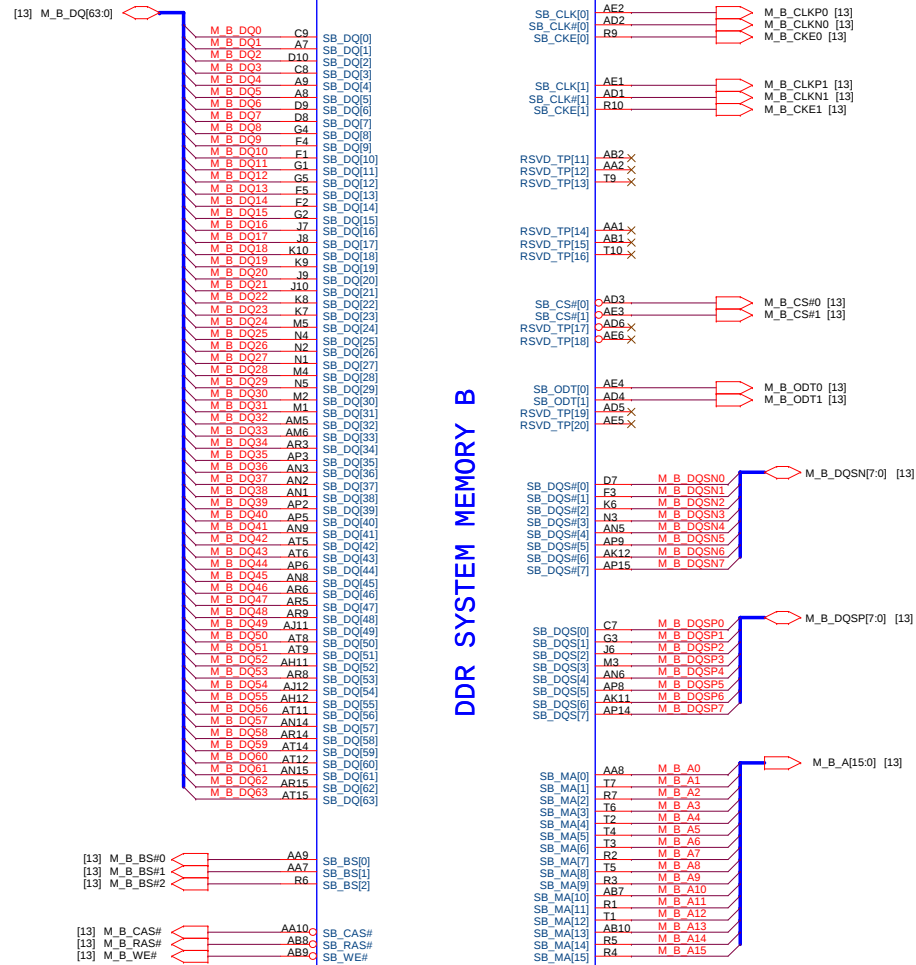
ACA-ZIF-069-K01



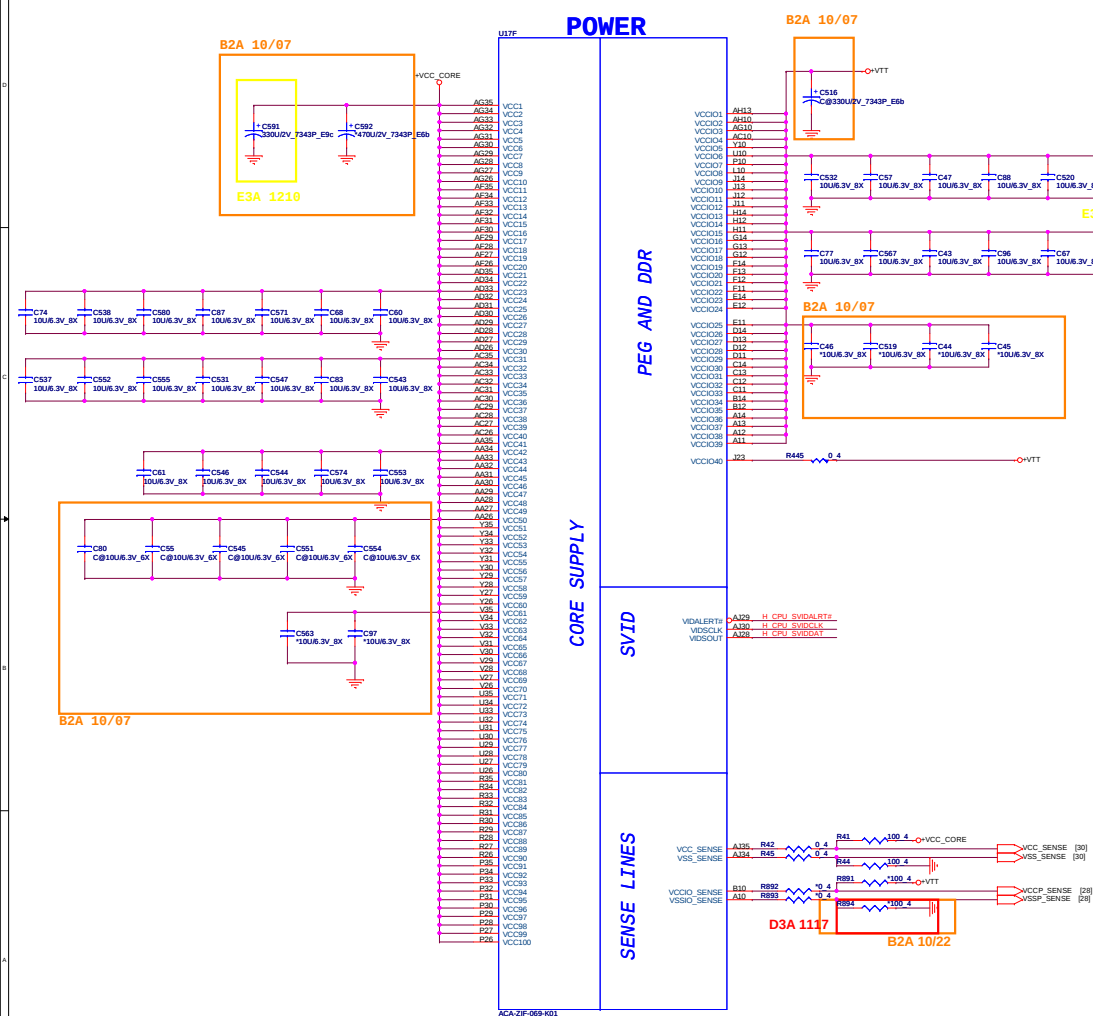
U17D

DDR SYSTEM MEMORY B

ACA-ZIF-069-K01

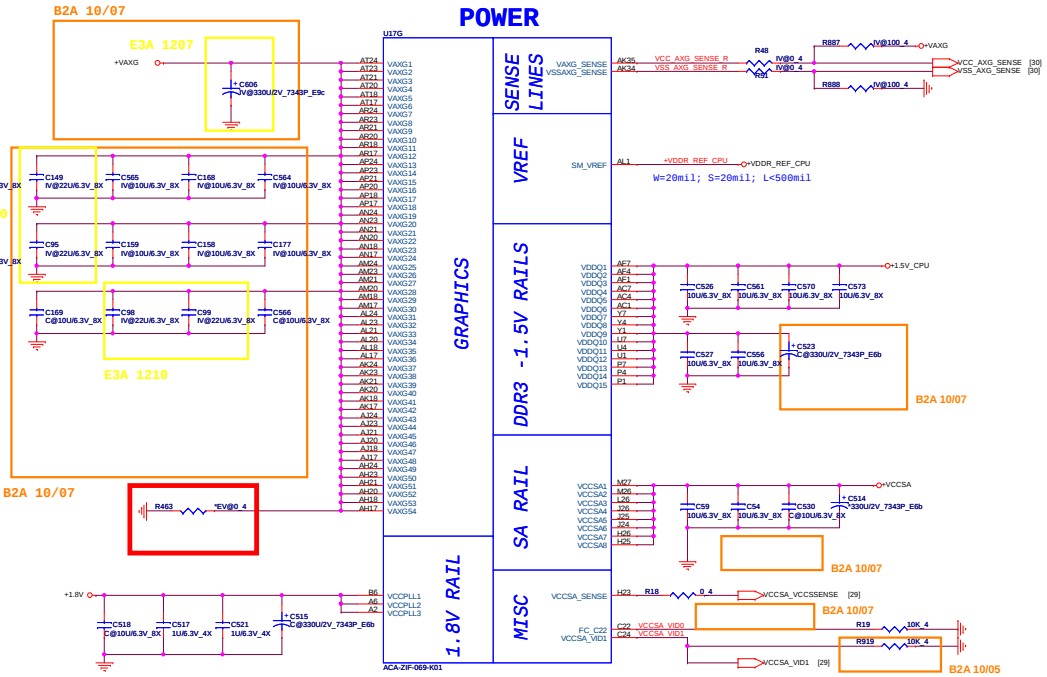


POWER



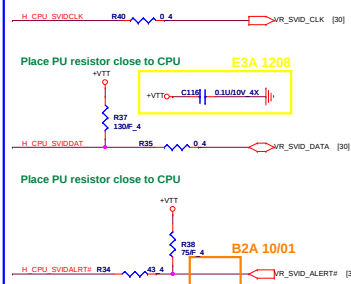
Sandy Bridge Processor (GRAPHIC POWER) <CPU>

POWER

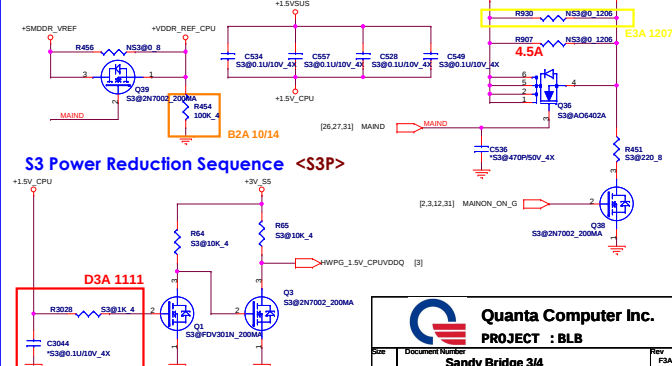


SVID <CPU>

Layout note: need routing together and ALERT need between CLK and DATA



S3 Power Reduction (CPU POWER) <S3P>





	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

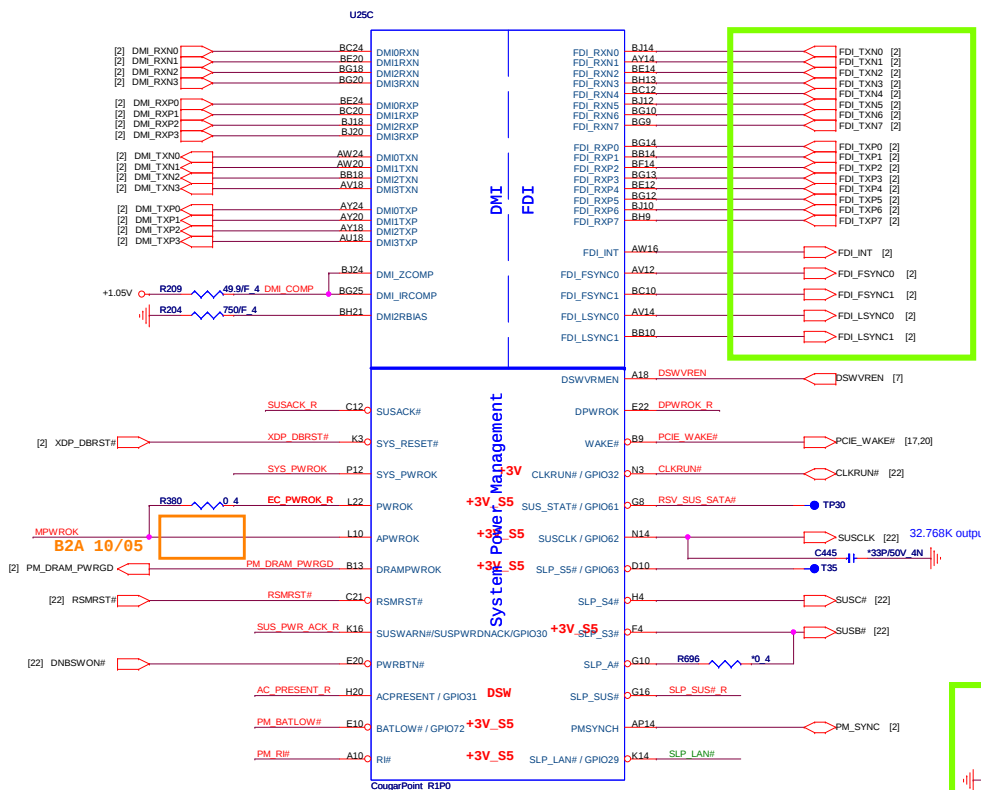


```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

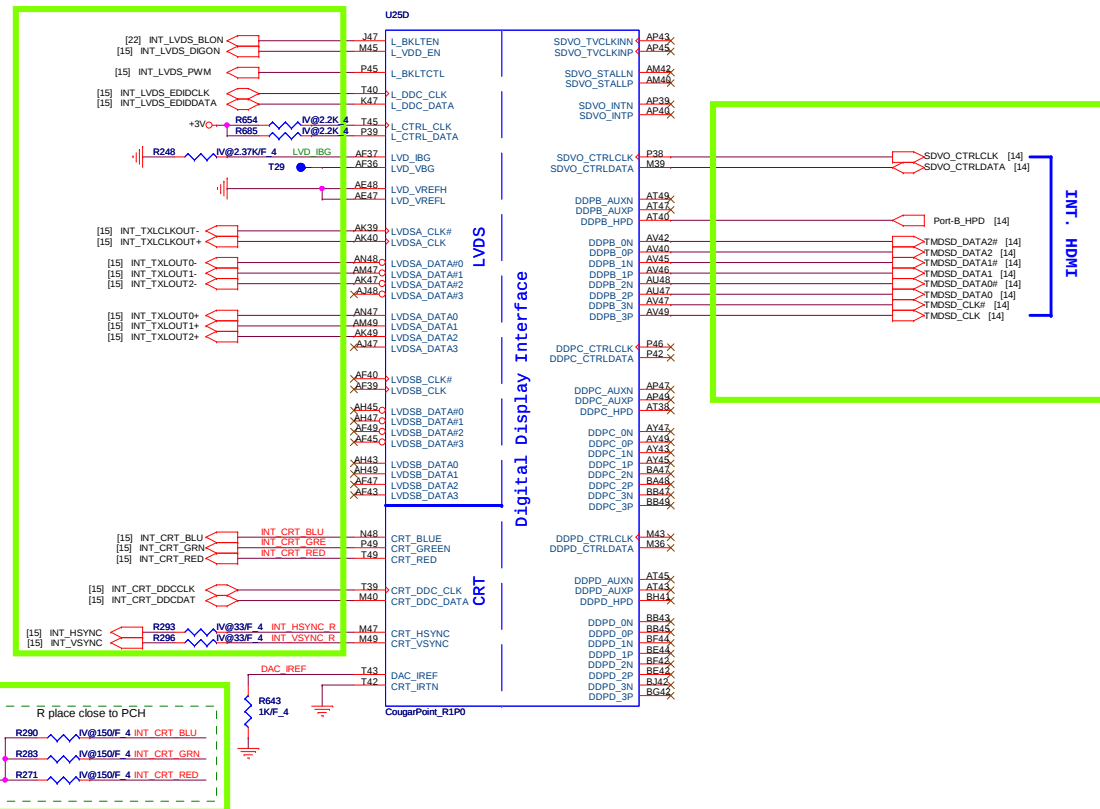


Date:	Friday, December 24, 2010	Sheet	5	of	36
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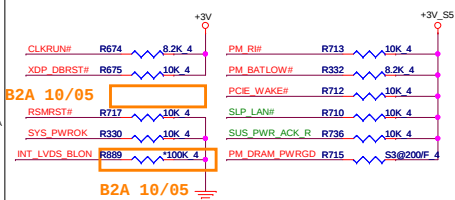
Cougar Point (DMI,FDI,PM) <CLG>



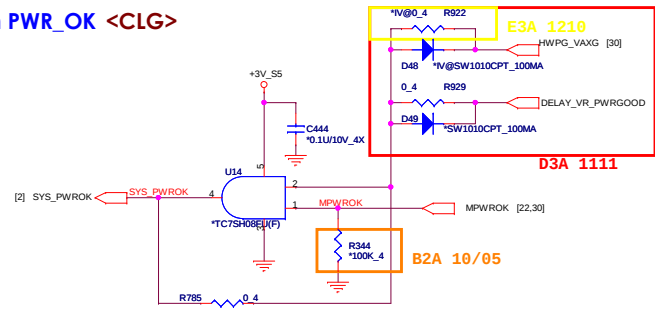
Cougar Point (LVDS,DDI) <CLG/UGA>



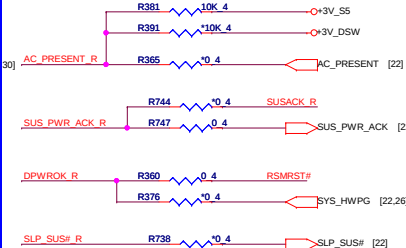
PCH Pull-high/low <CLG>



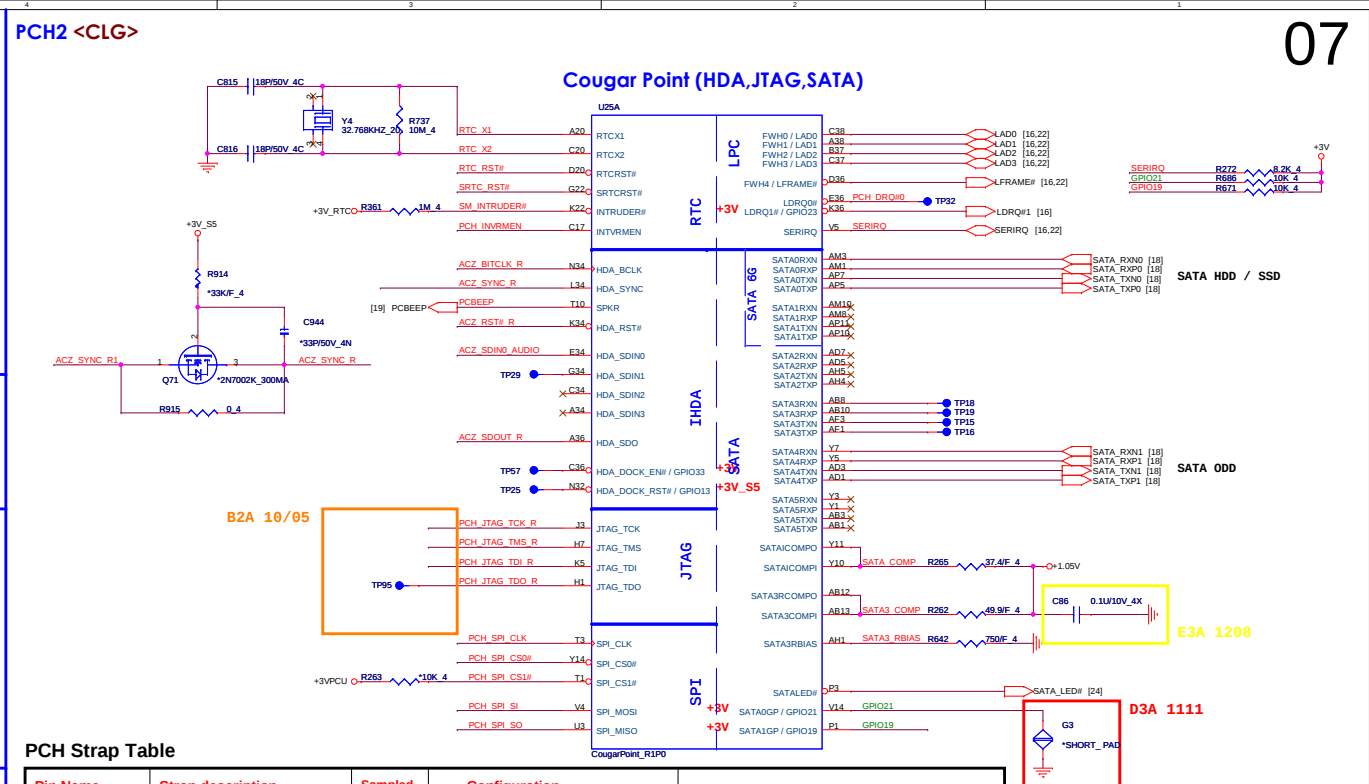
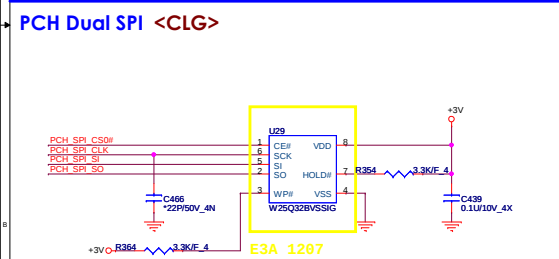
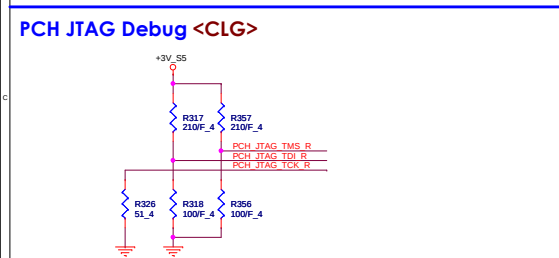
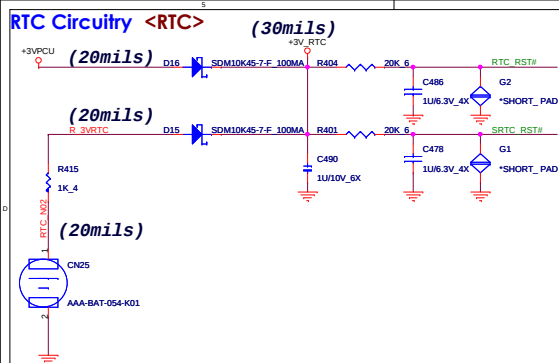
System PWR_OK <CLG>



Deep Sx <CLG>



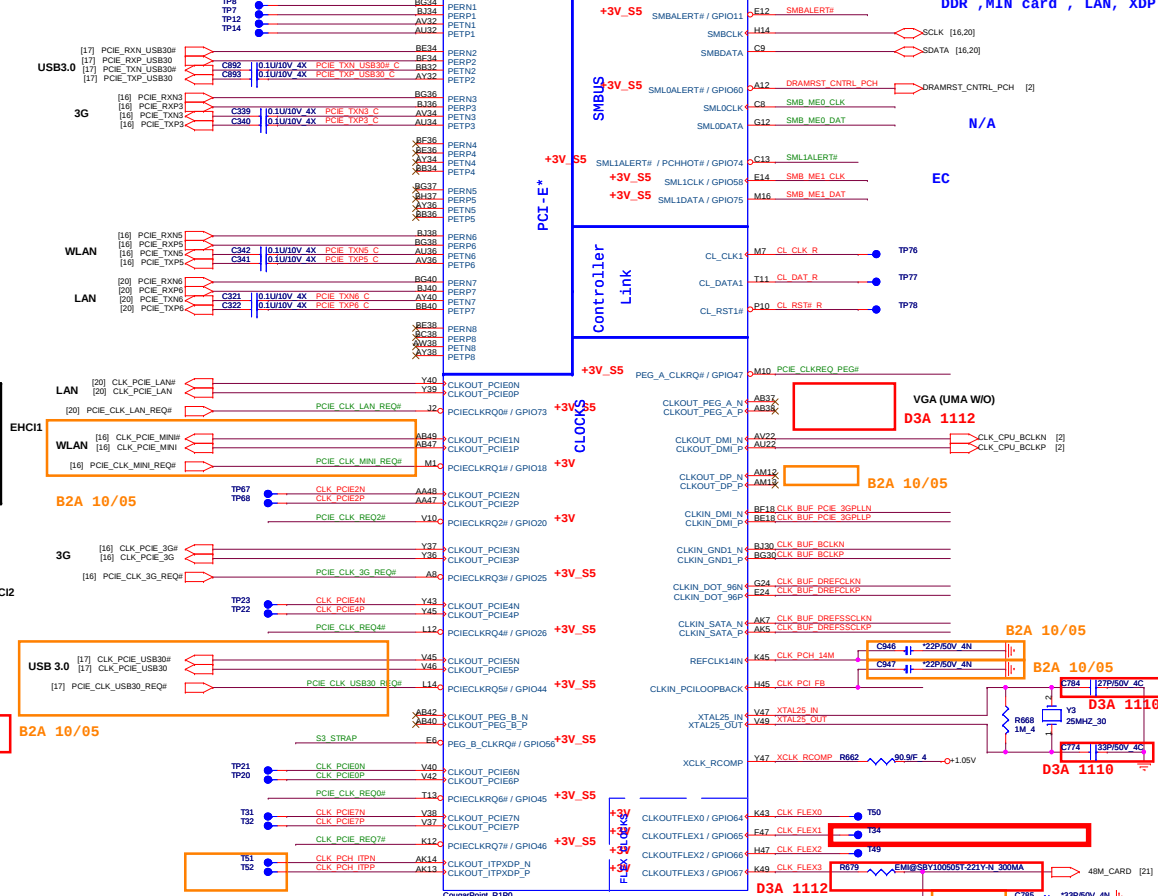
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	R391,R365 stuff	R381 stuff
SUS_PWR_ACK	R744 stuff	R747 stuff
DPWROK	R376 stuff	R360 stuff
SLP_SUS	R738 stuff	R738 No stuff



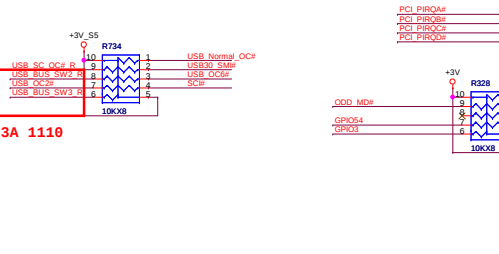
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT3#/ GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1#/ GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile 1 = Override	Should not pull low for desktop and mobile									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Default (weak pull-up 20K) 1 = Override										
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Default. Support by 1.8V 1 = Support by 1.5V										
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality										
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable										
SATA2GPI/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled hight when strap is sampled									
SATA3GPI/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled hight when strap is sampled									

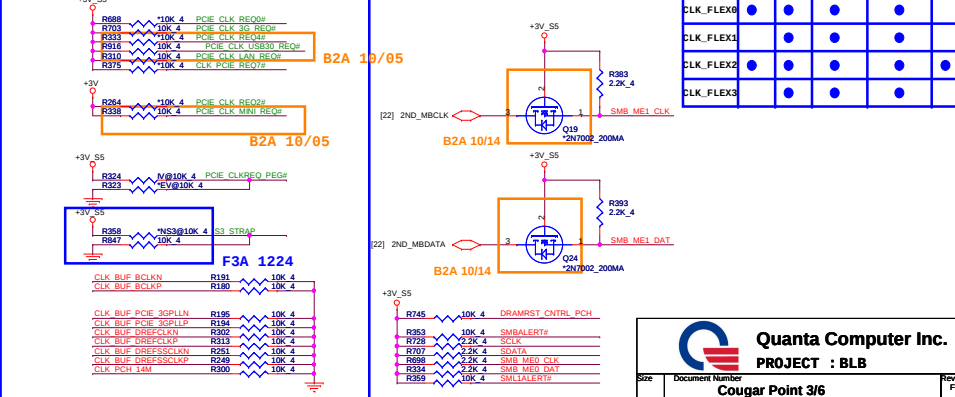
Cougar Point-M (PCI-E,SMBUS,CLK) <CLG>



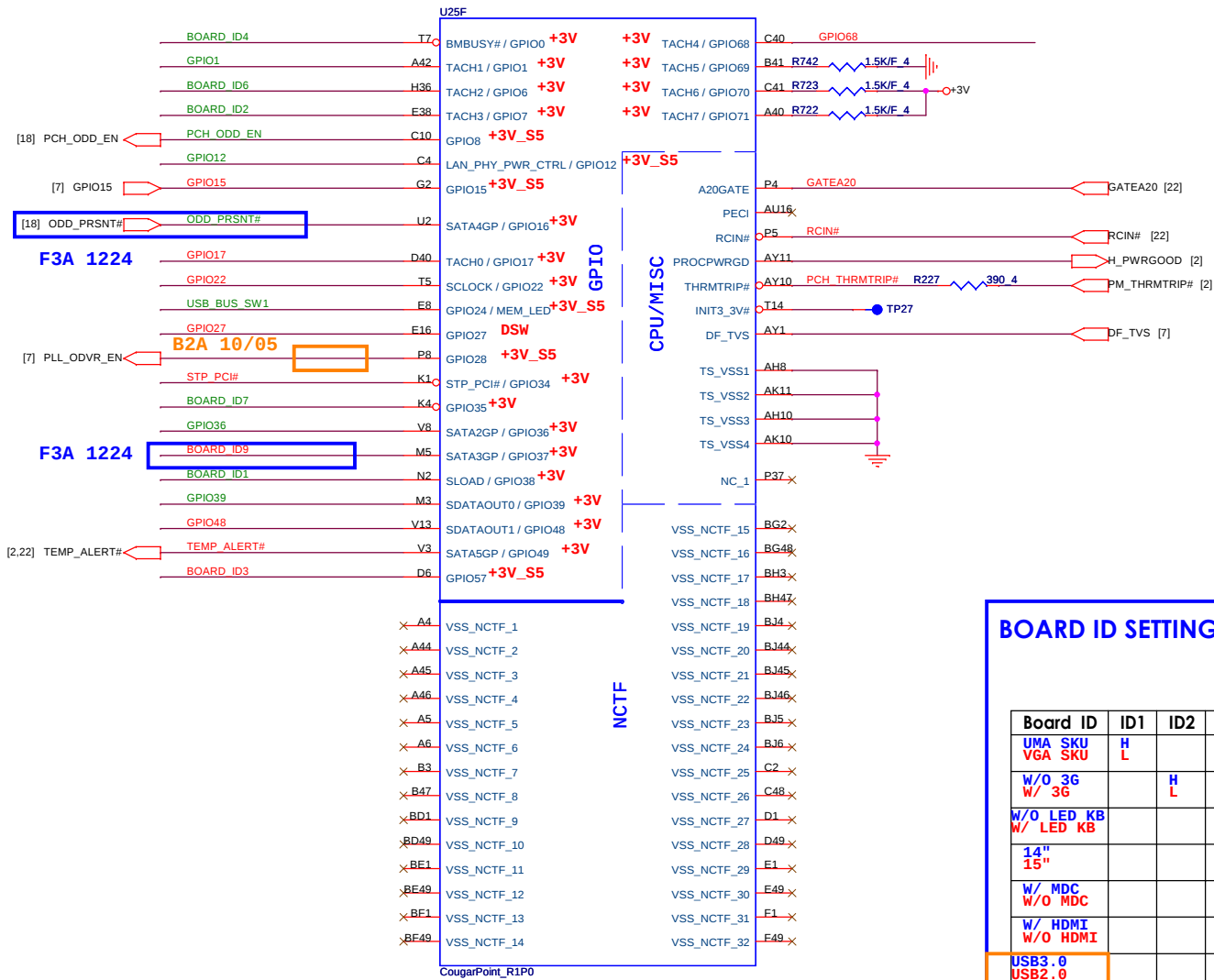
PCI/USBOC# Pull-up <CLG>



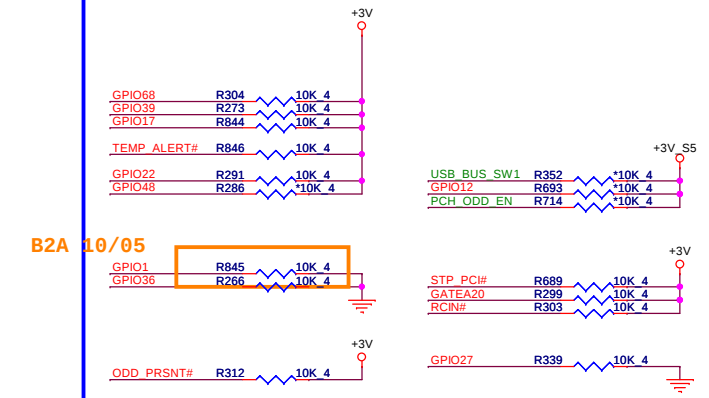
SMBus/Pull-up <CLG>



Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>



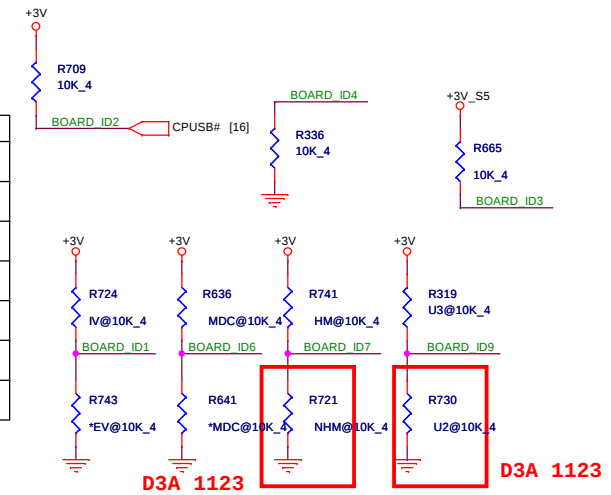
GPIO Pull-up/Pull-down <CLG>

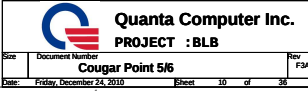


BOARD ID SETTING <CLG>

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9
UMA SKU	H						
VGA SKU	L						
W/O 3G		H					
W/O 3G		L					
W/O LED KB			H				
W/ LED KB			L				
14"				H			
15"				L			
W/ MDC					H		
W/O MDC					L		
W/ HDMI						H	
W/O HDMI						L	
USB3.0							H
USB2.0							L

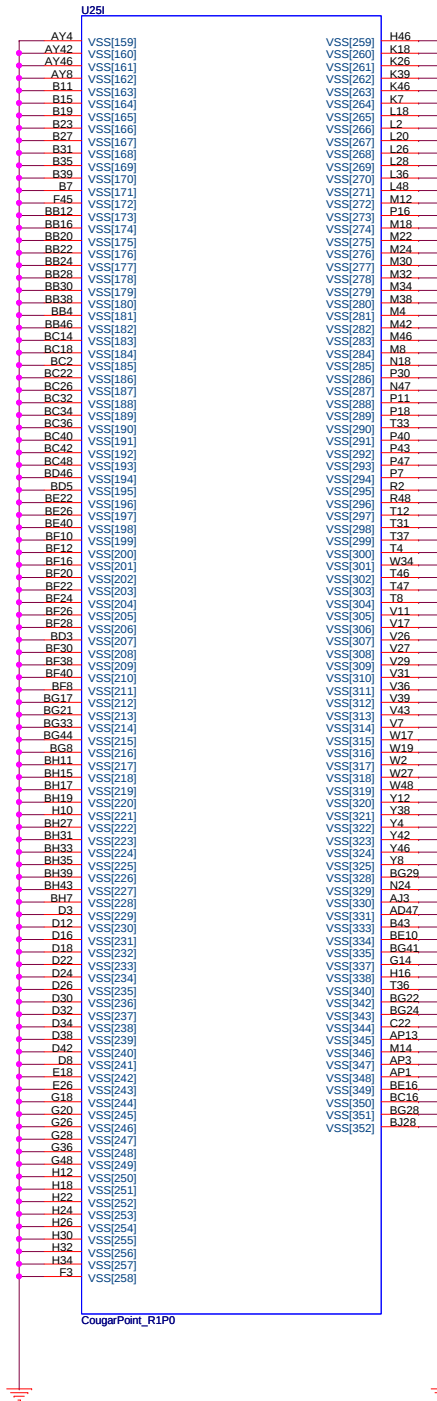
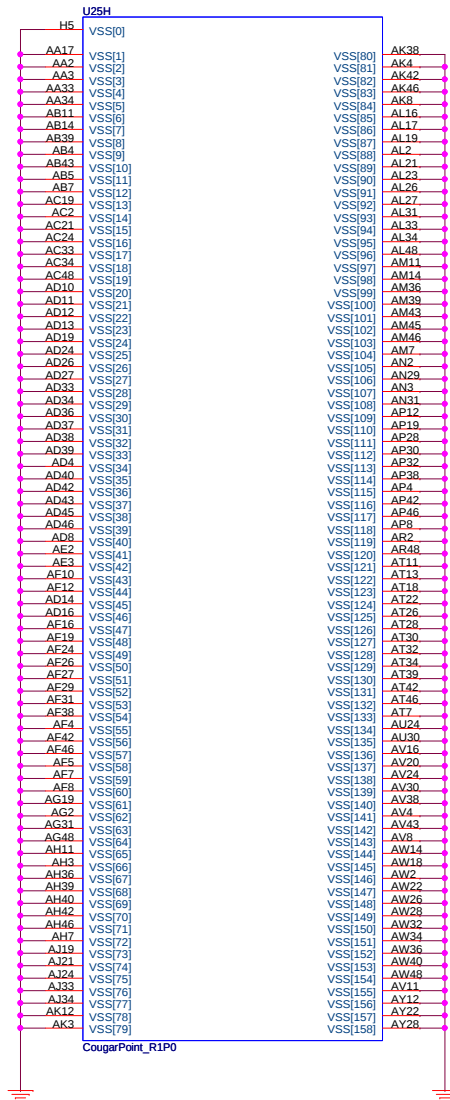
B2A 10/05





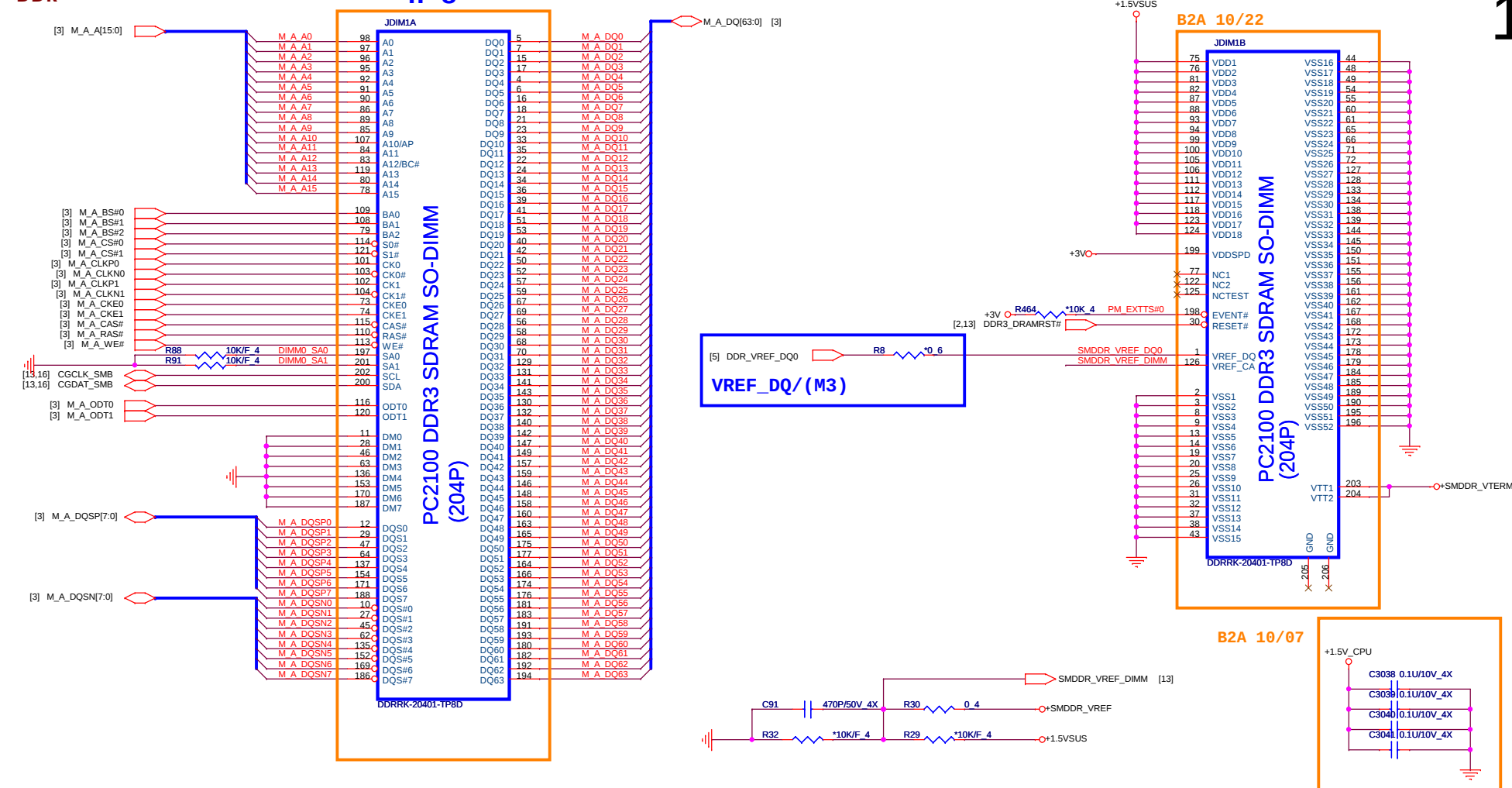
Cougar Point (GND)

Cougar Point (GND)

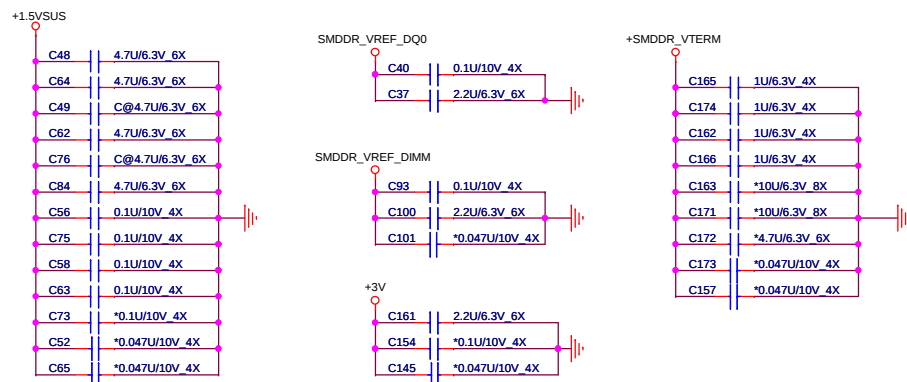


Quanta Computer Inc.
PROJECT : BLB

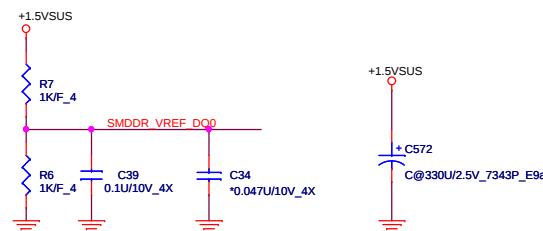
Size	Document Number	Rev
	Cougar Point 6/6	F3A
Date:	Friday, December 24, 2010	Sheet 11 of 36



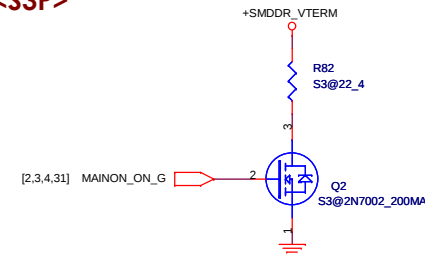
Place these Caps near So-Dimm0. <DDR>



VREF DQ/(M1) <DDR>



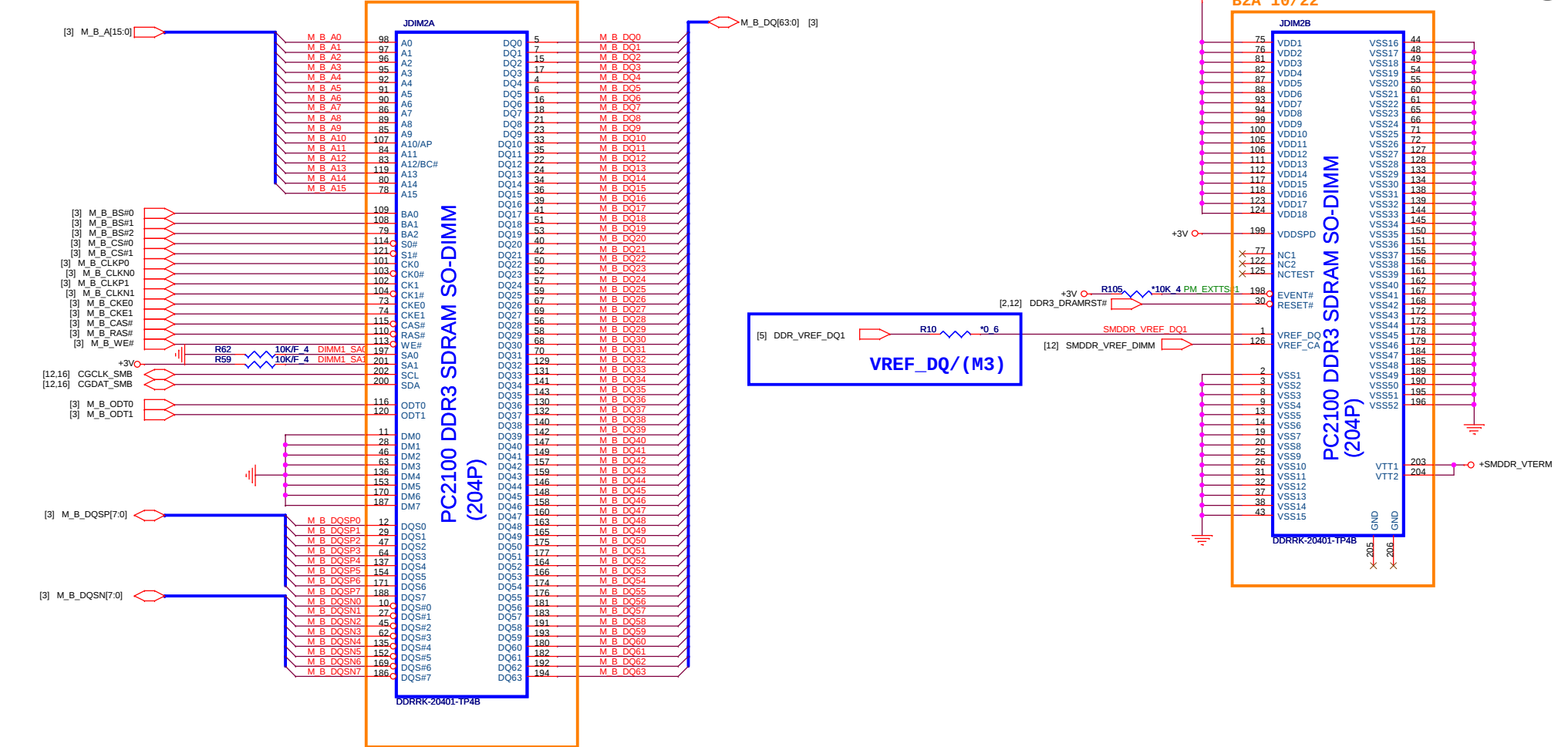
For S3 Power Reduction VTT discharge
<S3P>



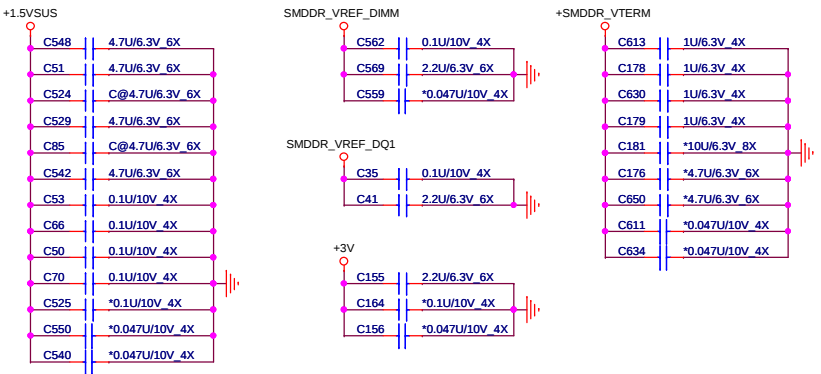
Quanta Computer Inc.
PROJECT : BLB

DDR3 DIMM-0

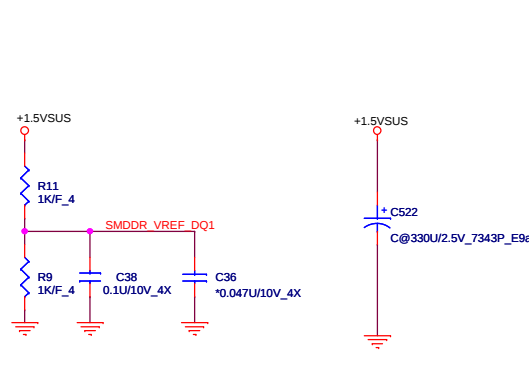
Size	Document Number	Rev
	DDR3 DIMM-0	F3A
Date:	Friday, December 24, 2010	Sheet 12 of 36



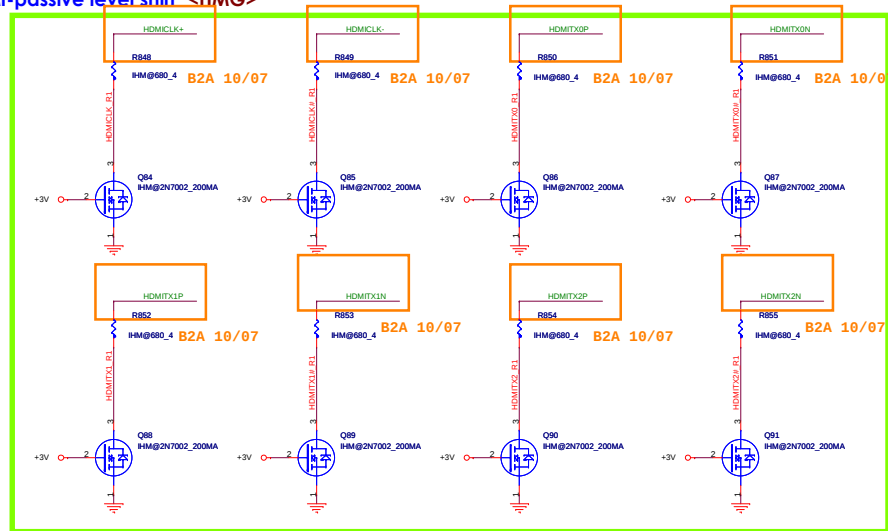
Place these Caps near So-Dimm1. <DDR>



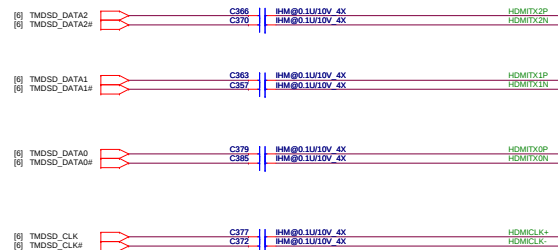
VREF_DQ/(M1) <DDR>



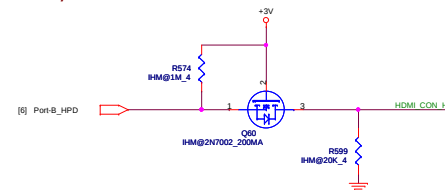
HDMI-passive level shift <HMG>



UMA HDMI <HMG>

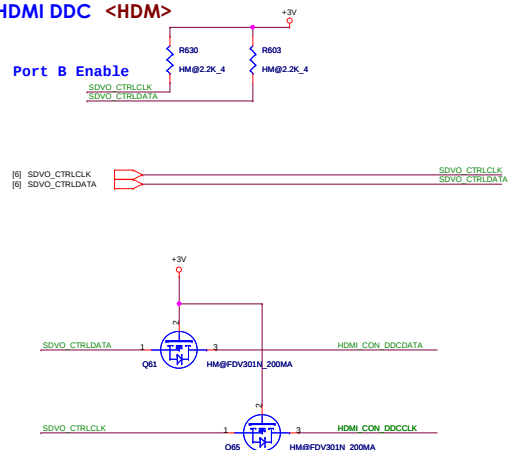


HDMI HPD <HMP/HMG>

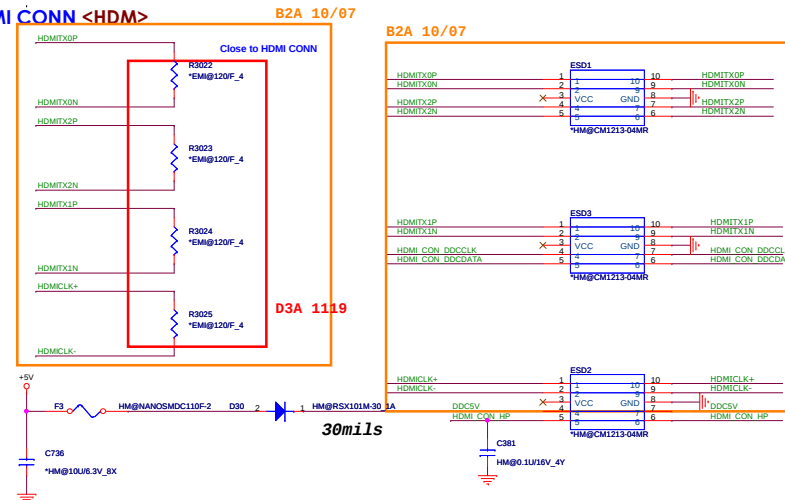


HDMI DDC <HDM>

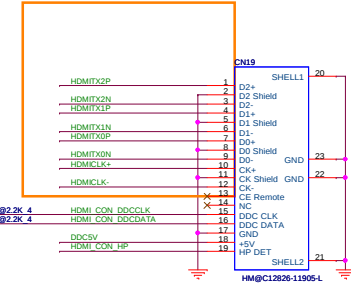
Port B Enable



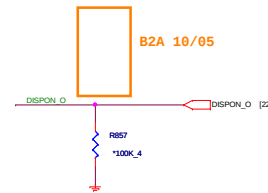
HDMI CONN <HDM>



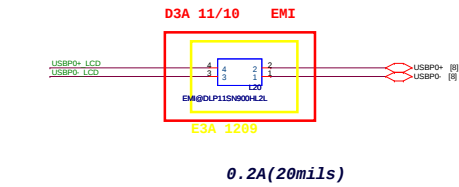
B2A 10/07



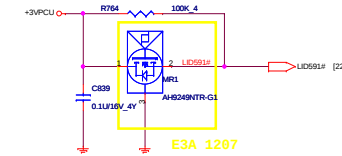
Panel backlight control <LDS>



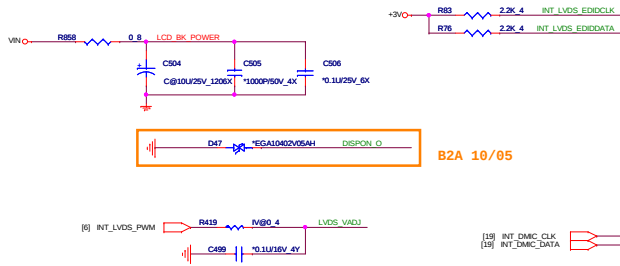
CCD <CCD>



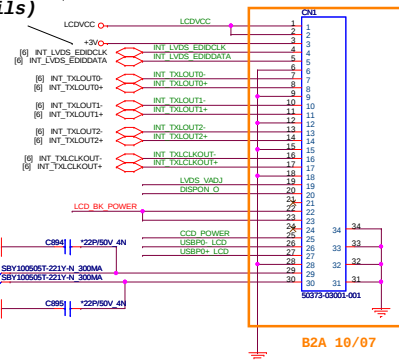
HALL SENSOR <HSR>



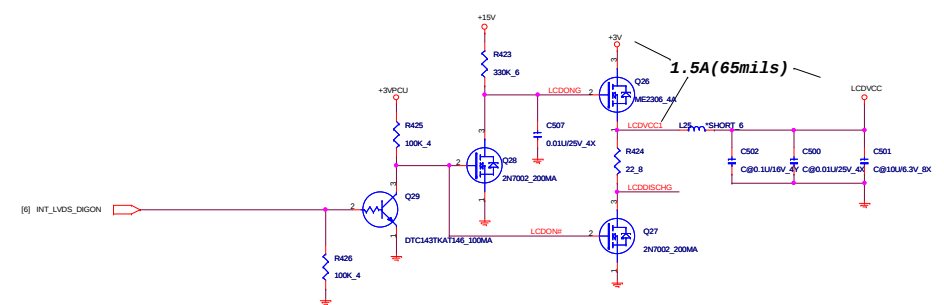
LCD Panel Module <LDS>



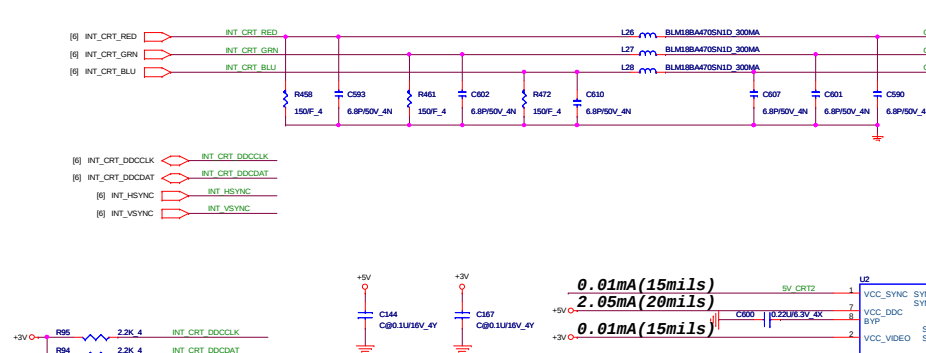
0.3A (20mils)



LCD POWER SWITCH <LDS>



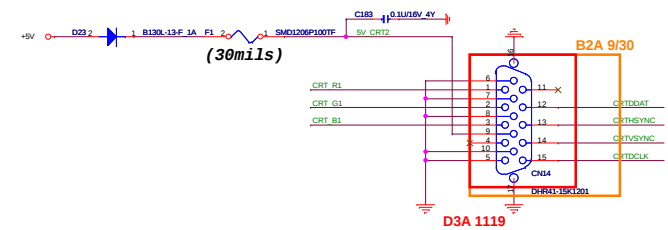
CRT <CRT>



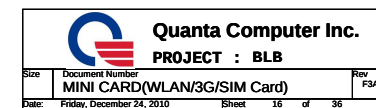
0.01mA (15mils)

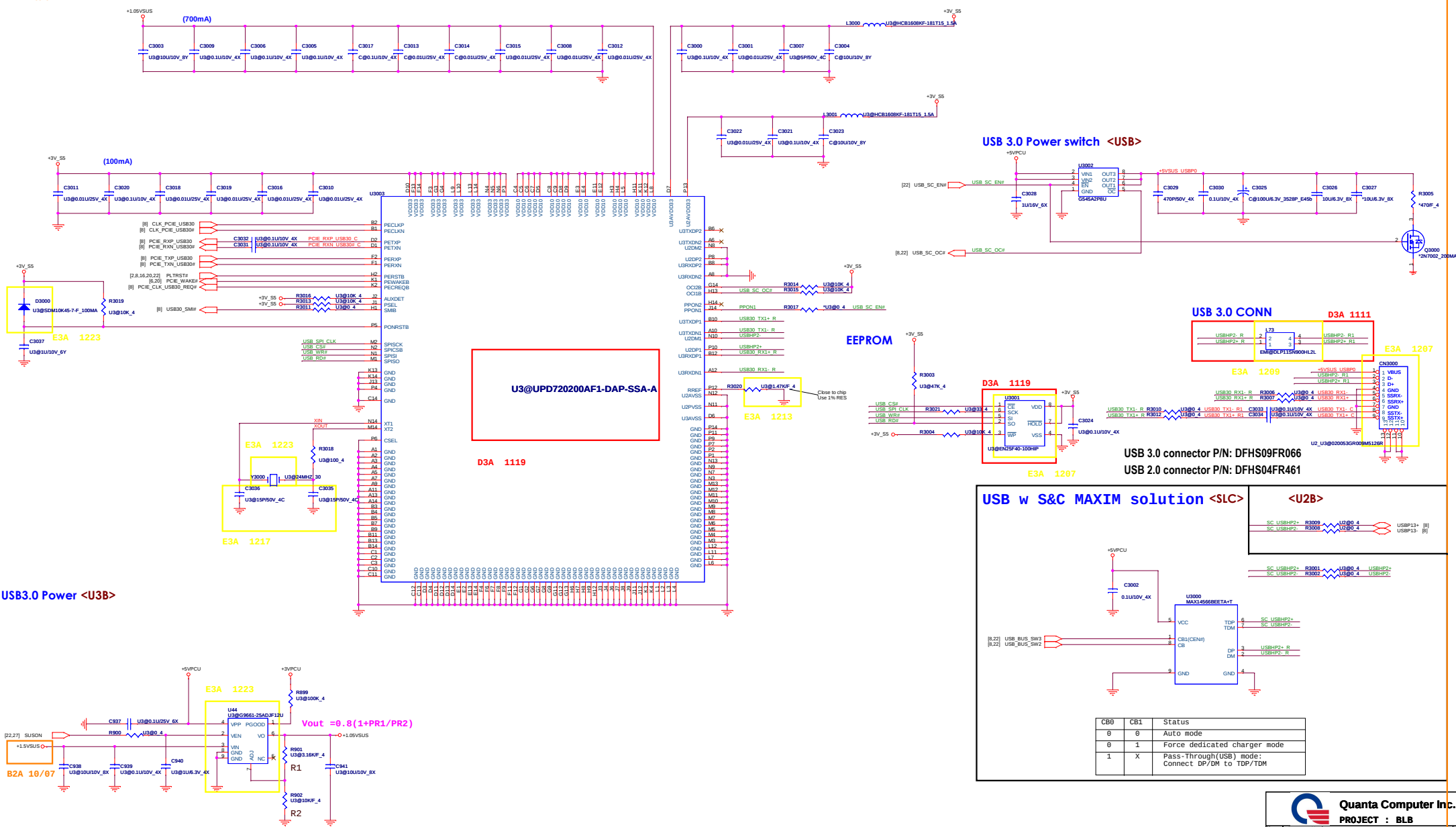
2.05mA (20mils)

0.01mA (15mils)

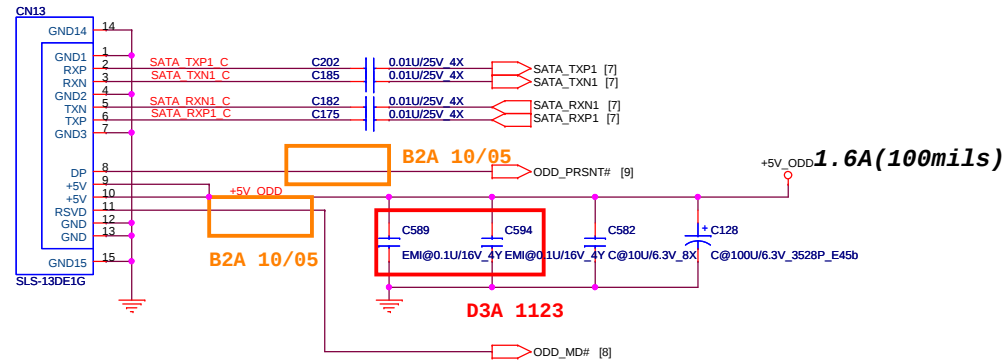


(30mils)

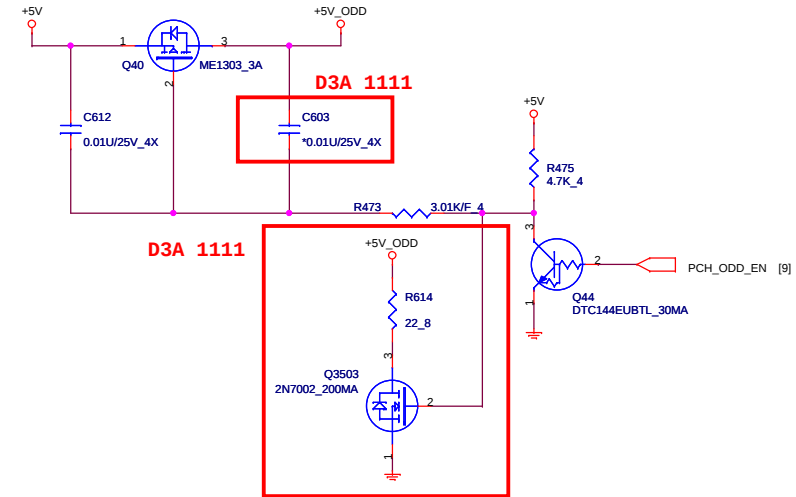




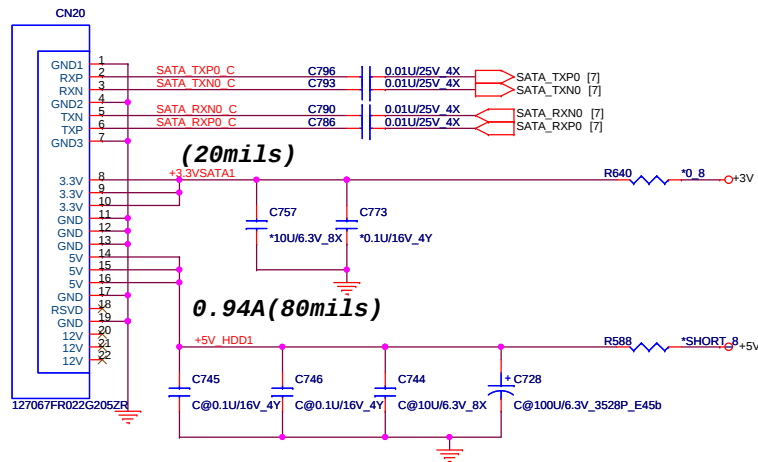
SATA ODD <ODD>



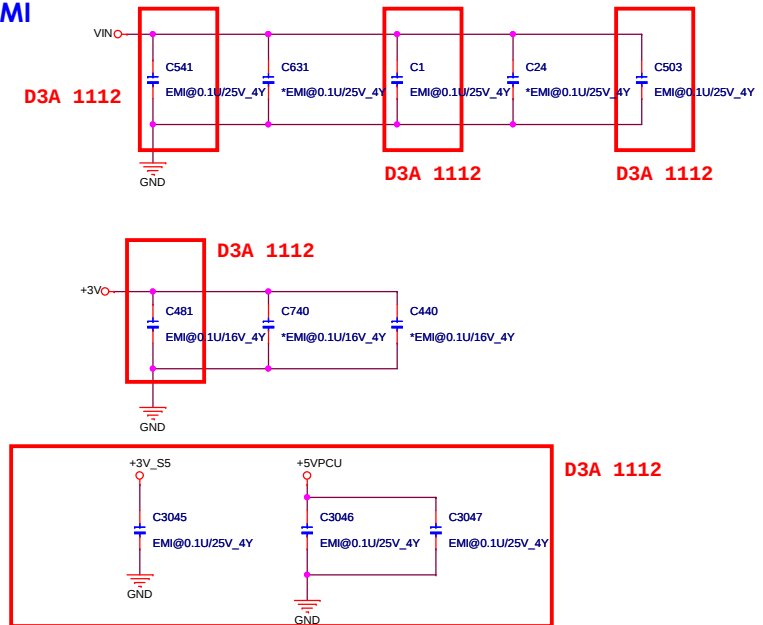
ODD Zero power . (Only for Intel) <OZP>

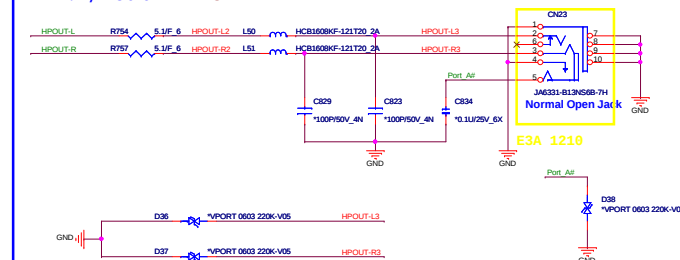


SATA HDD <HDD>

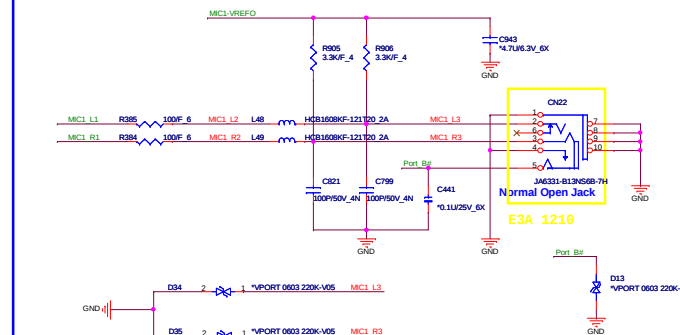


EMI



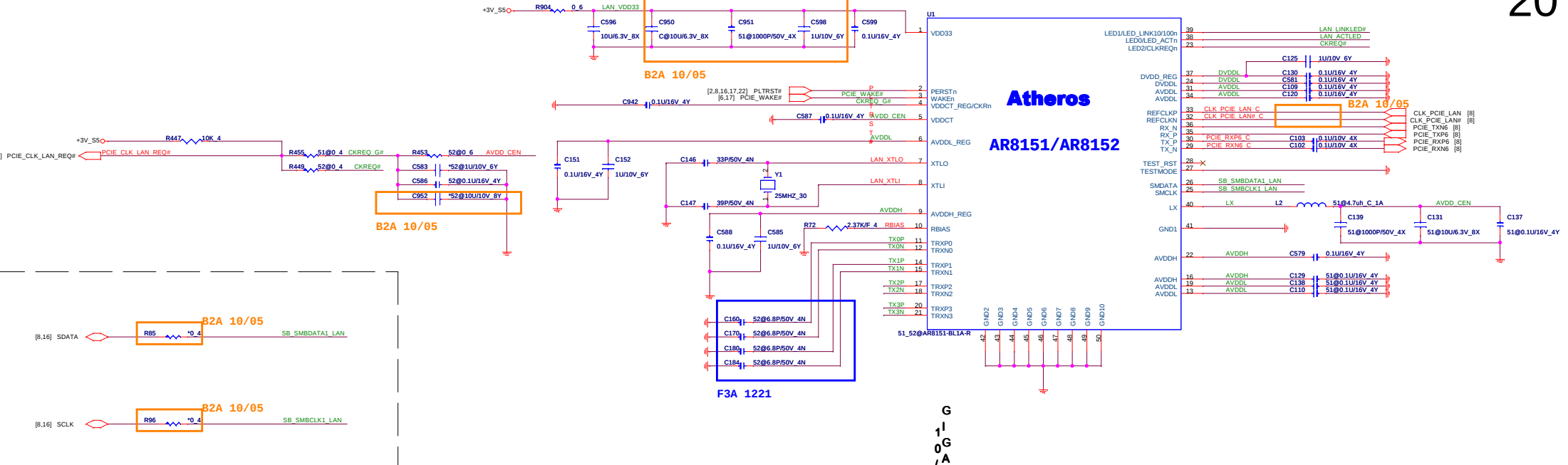


100

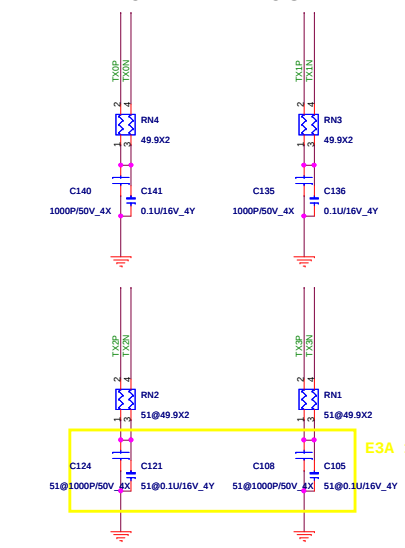


The schematic diagram illustrates the electrical connections for the E3A 1213 board. It features two diode components: MDC and MDC2. The MDC component, labeled MDC@130P150V_4N, is connected to the DB_P and DB_N pins. The MDC2 component, labeled MDC@68015-12N0, is also connected to the DB_P and DB_N pins. Both components have their cathodes connected to GND. The diagram shows the internal wiring and component placement on the PCB.

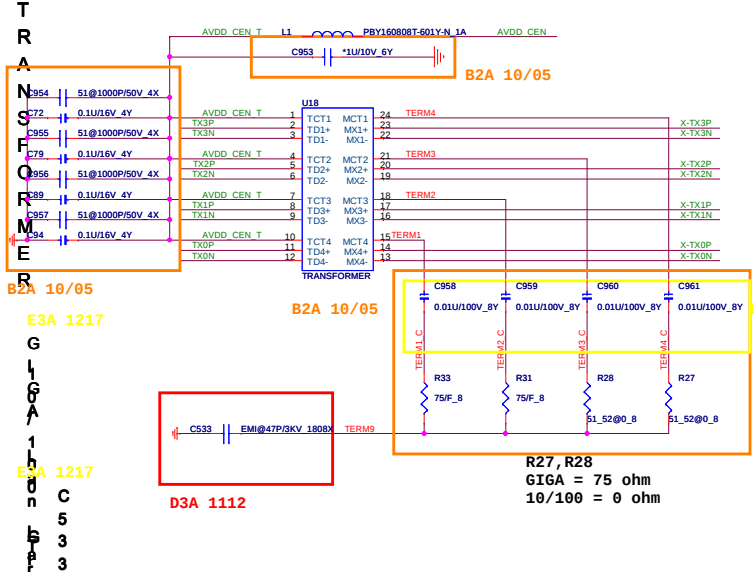
Atheros Lan <LAN/LN1/LNG>



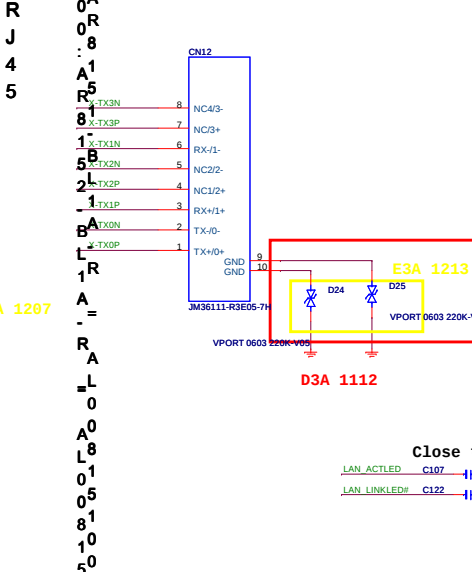
LAN-terminator <LAN/LN1/LNG>
PLACE NEAR LAN IC SIDE



LAN-Transformer <LAN/LN1/LNG>

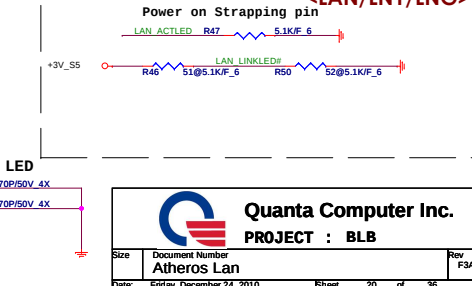


LAN(RJ45)-CONN Interface <LAN>



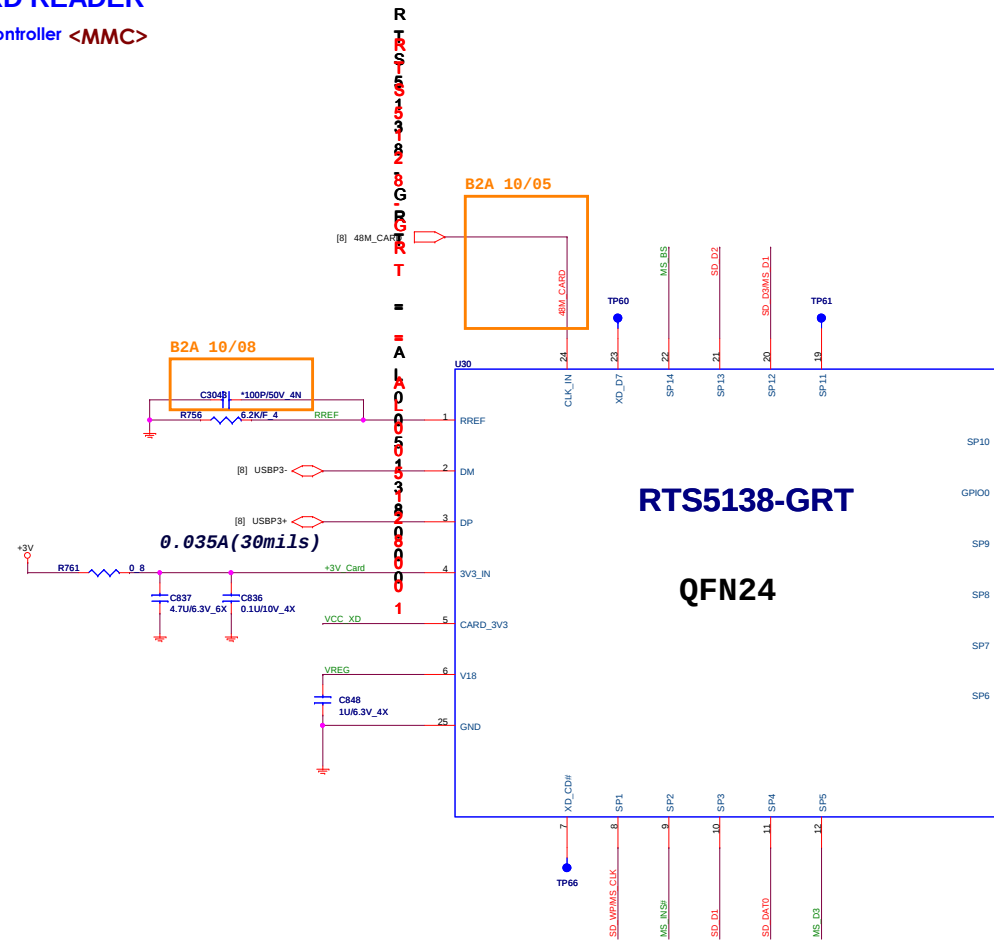
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull high (default = 1)
	0	LD0 linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN-Strap function <LAN/LN1/LNG>



3 IN 1 CARD READER

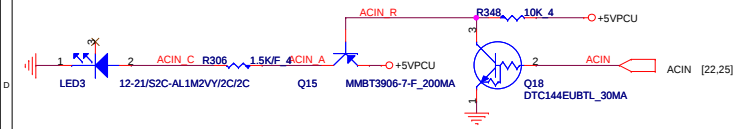
Card reader controller <MMC>



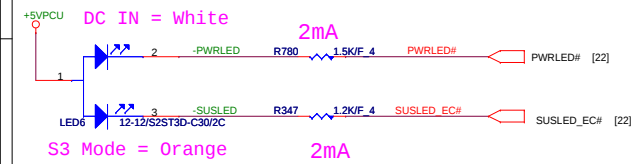
 Quanta Computer Inc. PROJECT : BLB		
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LED <LED>

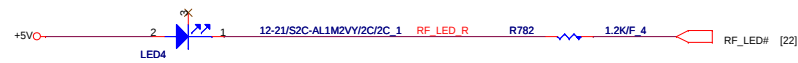
AC-IN



POWER



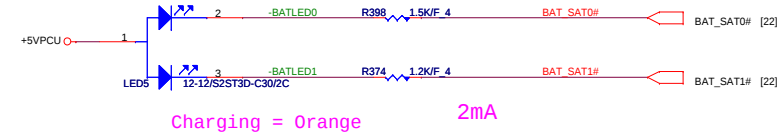
RF LED



BATTERY

Full Charge = White

2mA

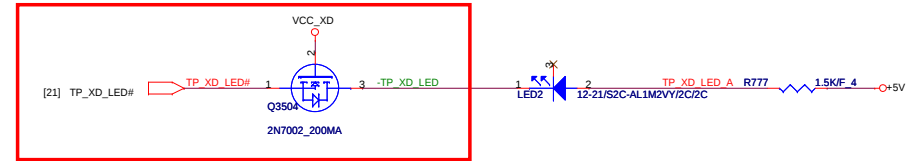


Charging = Orange

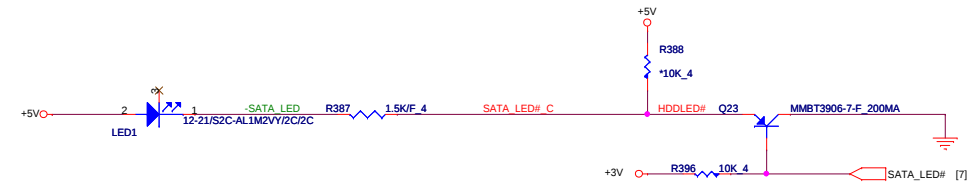
2mA

CARDREADER

D3A 1110

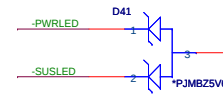


HDD/ODD



ESD Protect

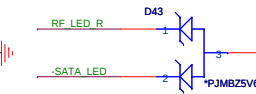
FOR POWER LED



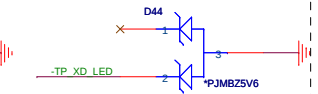
FOR BATTERY LED



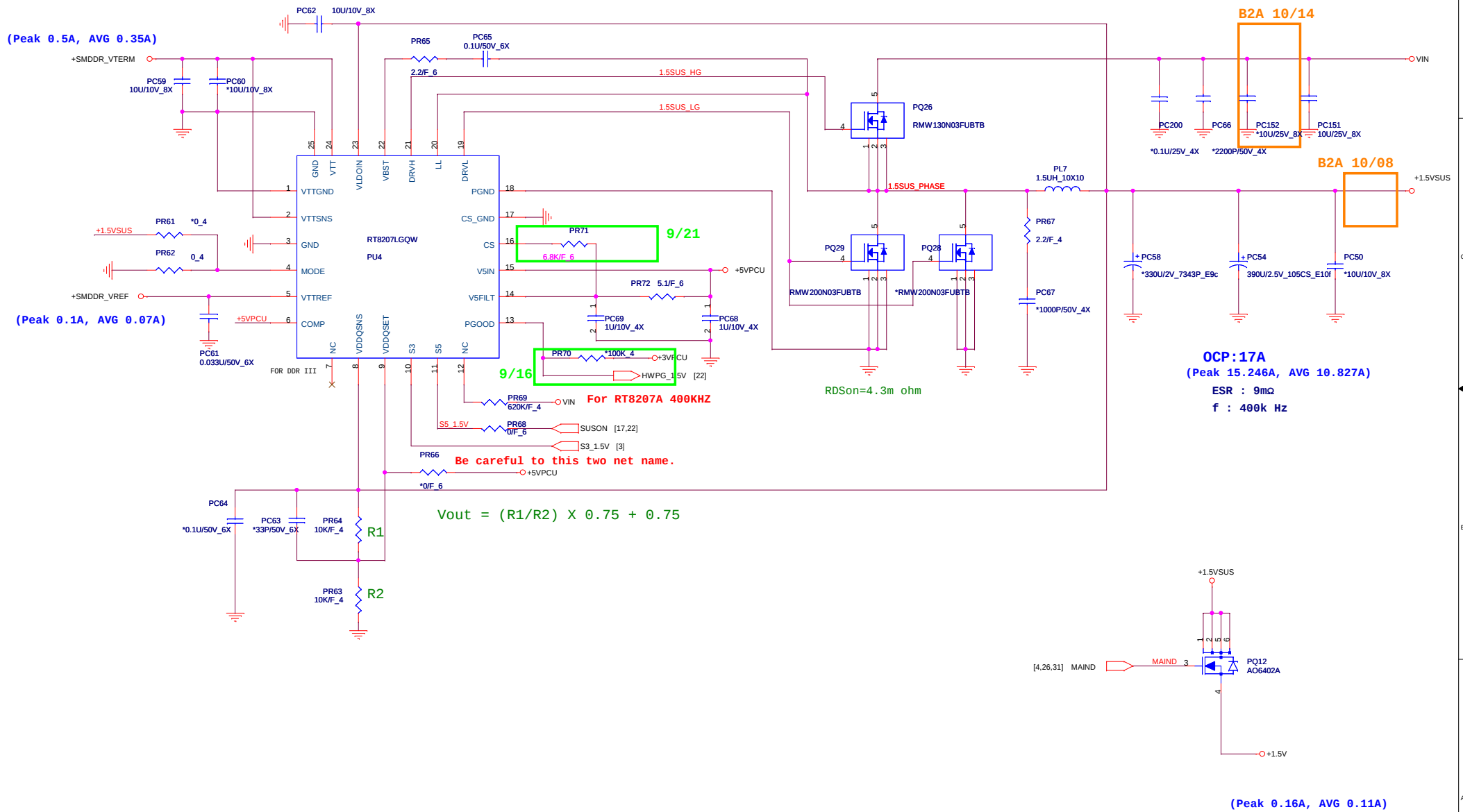
FOR HDD/RF LED

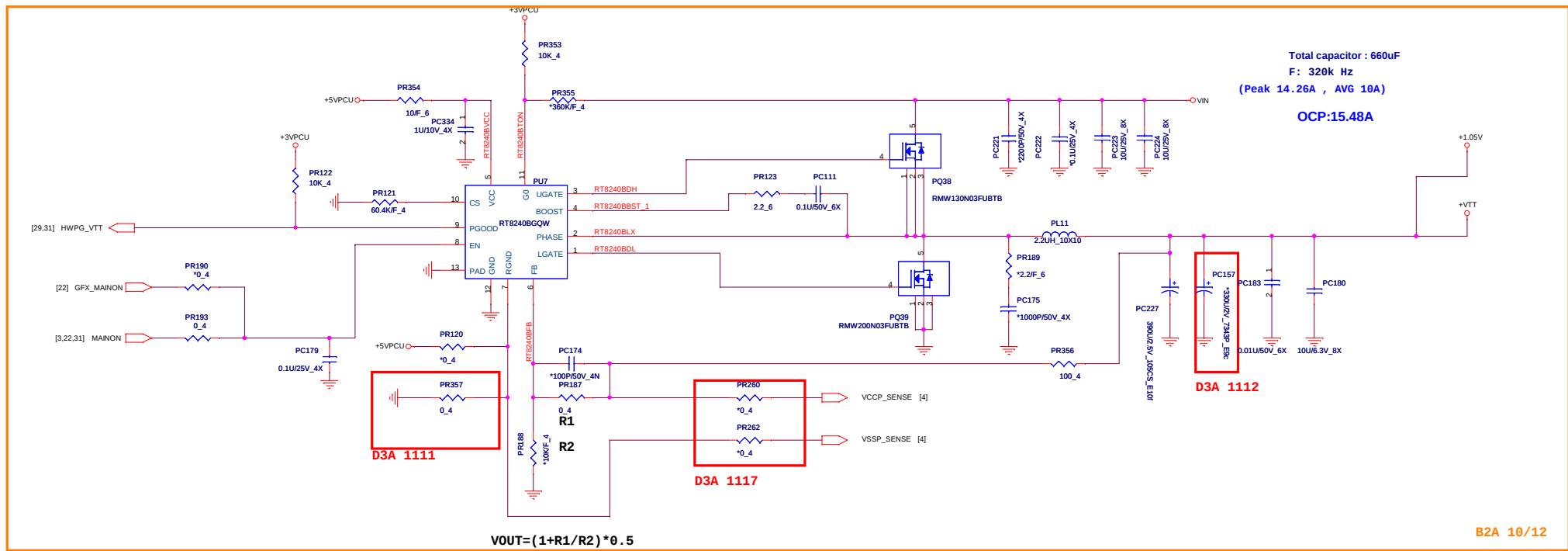


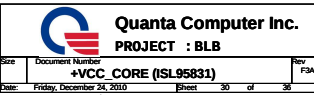
FOR CARDREADER LED

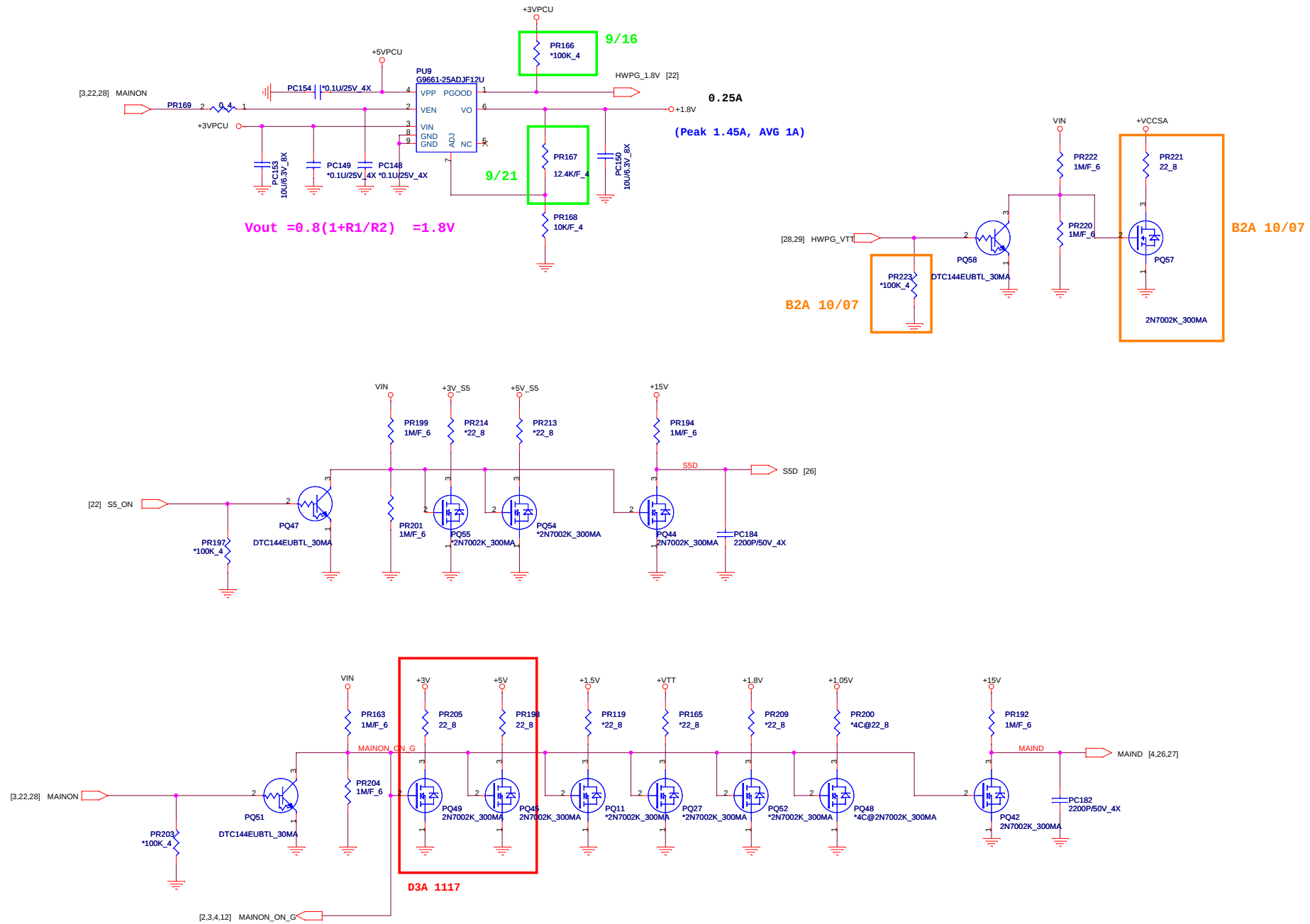


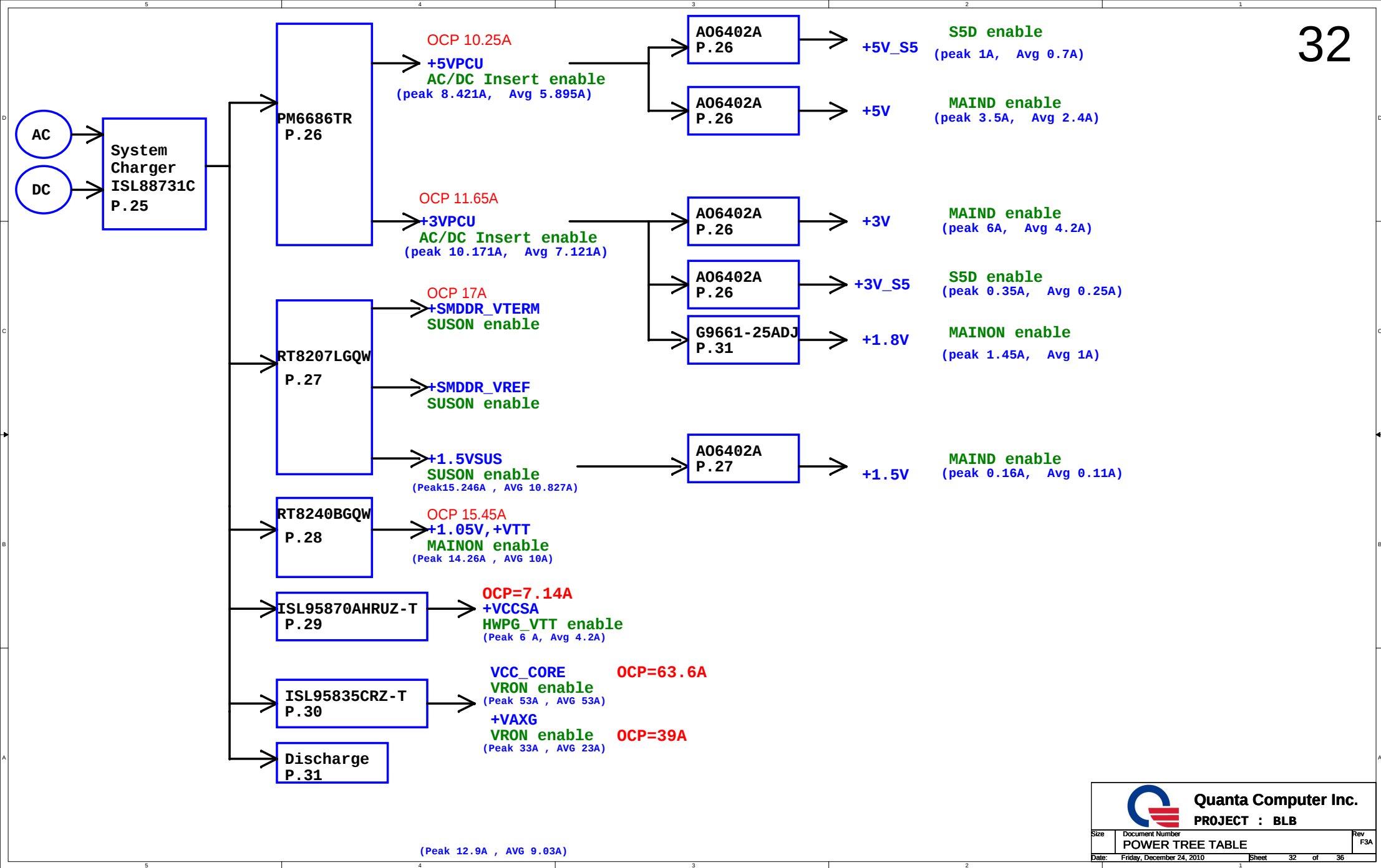












Model		REV	CHANGE LIST	BLB		
				MODEL	FROM	To
BLB MB	B2A	PAGE 2 : Remove R14 and add TP89	1	2A	3A	
		PAGE 2 : Remove R15	2	2A	3A	
		PAGE 2 : Remove R439	3	2A	3A	
		PAGE 2 : R441 change to 25.5 ohm 1% 0402	4	2A	3A	
		PAGE 2 : Remove XDP; R106,R107,R102,R109,R98,R87,R78,R84	5	2A	3A	
		PAGE 2 : Add R917 and Remove TP80,TP81,TP82,TP83,TP84,TP85,TP86,TP87,TP88,TP90	6	2A	3A	
		PAGE 2 : Remove S3@ of R471	7	2A	3A	
		PAGE 2 : Add R918 for non-S3 power reduction	8	2A	3A	
		PAGE 3 : R550 change to 0 ohm 0402 for S3 power reduction sequence.	9	2A	3A	
		PAGE 4 : Remove C71,C90 for cost down and C591,C592 add " * "no stuff.	10	2A	3A	
		PAGE 4 : C563, C97 change to 10U/6.3V 0805 no stuff.	11	2A	3A	
		PAGE 4 : Remove C649 for cost down	12	2A	3A	
		PAGE 4 : C46, C519, C44, C45 change to 10U/6.3V 0805 no stuff.	13	2A	3A	
		PAGE 4 : R894 stuff 100 ohm 0402 for power issue <Cann't power on>.	14	2A	3A	
		PAGE 4 : Remove C633, C150,C160,C148,C170 for cost down	15	2A	3A	
		PAGE 4 : C565, C168, C564, C159, C158, C177, C98, C99 change to 10U/6.3V 0805 no stuff.	16	2A	3A	
		PAGE 4 : R463 add " * "no stuff.	17	2A	3A	
		PAGE 4 : Remove R39	18	2A	3A	
		PAGE 4 : Remove C576, C535 for cost down	19	2A	3A	
		PAGE 4 : Remove R890 for VCCSA SENSE.	20	2A	3A	
		PAGE 4 : Remove R890 and NET name "VCCSA_VID0" and R919 for VCCSA VID.	21	2A	3A	
		PAGE 4 : Remove S3@ of R454	22	2A	3A	
		PAGE 5 : Add TP91	23	2A	3A	
		PAGE 5 : Remove R60, R56 and add TP92,TP93	24	2A	3A	
		PAGE 5 : R74 add " * " no stuff.	25	2A	3A	
		PAGE 6 : Remove R340, R682.	26	2A	3A	
		PAGE 6 : R889, R344 add " * " no stuff.	27	2A	3A	
		PAGE 7 : Remve R342, R325 and add TP95	28	2A	3A	
		PAGE 8 : Remve R748, R749	29	2A	3A	
		PAGE 8 : Change TP36 footprint to TP3050	30	2A	3A	
		PAGE 8 : WLAN PCIE clock <CLK_PCIE_MINI# , CLK_PCIE_MINI, PCIE_CLK_MINI_REQ#> change to PCIE clock port1.	31	2A	3A	
		PAGE 8 : USB 3.0 PCIE clock <CLK_PCIE_USB30# , CLK_PCIE_USB30, PCIE_CLK_USB30_REQ#> change to PCIE clock port5.	32	2A	3A	
		PAGE 8 : Remove R247 and add T51,T52	33	2A	3A	
		PAGE 8 : Remove C946,C947,R680	34	2A	3A	
		PAGE 8 : R916 change PU to +3V_S5 for USB3.0 PCIE CLK	35	2A	3A	
		PAGE 8 : R338 change PU to +3V for WLAN PCIE CLK				
		PAGE 8 : Q19 and Q18 add " * " no stuff.				
		PAGE 9 : Remove R305				
		PAGE 9 : R845 change PD to GND for PCH GPIO1				
		PAGE 9 : Change BOARD ID for USB3.0 and USB 2.0				
		PAGE 10 : Reserve C948, C949 no stuff.				
		PAGE 10 : Remove R673				
		PAGE 10 :Change power source to +1.05V of V_PROC_IO, VCCDMI[2], VCCDMI[1]				
		PAGE 10 : Add R3026 and L36, C714, C 700 add " * " no stuff for cost down.				
		PAGE 12 : JDIM1 Change Main source P/N: DGMK4000087; 2nd source P/N: DGMK4000178				
		PAGE 12 : Add C3038, C3039, C3040, C3041 for SI				
		PAGE 13 : JDIM2 Change Main source P/N: DGMK4000005; 2nd source P/N: DGMK0000120				
		PAGE 14 : Remove RN6,RN5,RN8,RN9 and add R3022, R3023, R3024,R3025 for EMI				
		PAGE 15 : Remove R856				
		PAGE 15 : Reserve D47 for ESD				
		PAGE 15 : CN1 LVDS connector change footprint and PN:DFHS30FR015				
		PAGE 15 : CN14 CRT connector change PN:DFDS15FR158				
		PAGE 16 : Remove R205				
		PAGE 16 : CN18 WLAN connector change PN:DFHD52MR016				
		PAGE 16 : CN21 3G connector change PN:DFHD52MR032				
		PAGE 16 : CN21 3G connector pin48, pin28,pin6 change power source +1.5V				
		PAGE 16 : Add R921 and Reserve R920,Q94 for leakage				
		PAGE 17 : USB3.0 change NEC solution				
		PAGE 17 : Change power source +1.5VSUS for VIN of USB3.0 LDO				
		PAGE 18 : Remove R77, R53 for cost down				
		PAGE 19 : C492 close to R409; C843 close to R417; R2,R3,R4,R5,C25,C26,C27,C28 close to U15				
		PAGE 19 : Remove L52 and Add R3027 for conexant suggest.				
		PAGE 19 : Remove C29,C30,C31,C32 for conexant suggest.				
		PAGE 20 : Add C950,C951,C952,C954,C955,C956,C957,C953 for Atheros suggest.				
DOC NO. 204		PROJECT MODEL :	BLB	APPROVED BY:	DATE:	2010/12/21
		PART NUMBER:	31BLBMB0IG0	DRAWING BY:	REVISION:	F3A
		 Quanta Computer Inc. PROJECT : BLB Change list				Size Document Number Rev F3A
		Date: Friday, December 24, 2010				Sheet 33 of 36

Model		REV	CHANGE LIST	MODEL BLB		
				PAGE	FROM	To
BLB MB	B2A	PAGE 20 :	R85, R96 add " * "no stuff.	1	2A	3A
		PAGE 20 :	Remove R450, R448 for cost down.	2	2A	3A
		PAGE 20 :	Add C958,C959,C960,C961 for Atheros suggest.	3	2A	3A
		PAGE 21 :	Remove R755 for cost down.	4	2A	3A
		PAGE 21 :	Add C3043 for Realtek suggest.	5	2A	3A
		PAGE 22 :	Remove R615,R614 and add TP97,TP94,TP98,TP99,TP96,TP100,TP101,TP102,TP103,TP104	6	2A	3A
		PAGE 22 :	Add C3042 for EMI	7	2A	3A
		PAGE 22 :	Add R923,R926,R924,R927,R925,R928 for SKU strap of EC code	8	2A	3A
		PAGE 22 :	EC GPIO56 change to SKU_STRAP_1	9	2A	3A
		PAGE 22 :	EC GPIO15 change to SKU_STRAP_3	10	2A	3A
		PAGE 22 :	EC GPIO66 change to SKU_STRAP_2	11	2A	3A
		PAGE 22 :	3ND_MBCLK and 3ND_MBDATA change PU 4.7K to 3V	12	2A	3A
		PAGE 22 :	Add D48, R922 for HWPG VAXG	13	2A	3A
		PAGE 23 :	C9,C5,C6,C7,C8,C3,C4,C2,C20,C21,C10,C11,C16,C17,C18,C19,C12,C13,C14,C15 remove " * " stuff for EMI.	14	2A	3A
		PAGE 23 :	Hole11 change footprint: intel-cpu-bkt2	15	2A	3A
		PAGE 23 :	Hole20 change PN to MBZK6002010	16	2A	3A
		PAGE 23 :	Hole21 change PN to MBIM3001010	17	2A	3A
		PAGE 23 :	Hole30 change footprint: HG-TC268BC335D118P2	18	2A	3A
		PAGE 25 :	PCN2 change PN: DFHD04MS988	19	2A	3A
		PAGE 25 :	Add PU10 for ESD	20	2A	3A
		PAGE 26 :	Remove PJP6, PJP5 short pad	21	2A	3A
		PAGE 26 :	PR100 add " * "no stuff and PR93 change to 0 ohm	22	2A	3A
		PAGE 26 :	Add PD14 and PR352 no stuff and Add PR35	23	2A	3A
		PAGE 26 :	Add PR350	24	2A	3A
		PAGE 26 :	PR278 change to 287Kohm	25	2A	3A
		PAGE 26 :	PR74, PR75 add " * "no stuff	26	2A	3A
		PAGE 27 :	Remove PJP1	27	2A	3A
		PAGE 27 :	PC152 add " * "no stuff	28	2A	3A
		PAGE 28 :	+VTT/+1.05V change to RT8240BGQW solution.	29	2A	3A
		PAGE 29 :	Remove PJP4	30	2A	3A
		PAGE 29 :	PC143 add " * "no stuff	31	2A	3A
		PAGE 29 :	Remove net :VCCSA_VSSSENSE	32	2A	3A
		PAGE 29 :	Remove PR34,PR28 and add TP105	33	2A	3A
		PAGE 29 :	PR40 add " * "no stuff	34	2A	3A
		PAGE 30 :	PR301,PR9,PR7add " * "no stuff	35	2A	3A
	PAGE 30 :	PR302,PR300,PC232remove " * " stuff				
	PAGE 30 :	PR139 change to 3.09K 1% 0402				
	PAGE 30 :	PR131 change to 267K 1% 0402				
	PAGE 30 :	PC116 change to 680P 50V 0402				
	PAGE 30 :	PC323 remove " * " stuff				
	PAGE 30 :	Add PC332,PC333,PC331,PC330				
	PAGE 30 :	PC145,PC146 add " * "no stuff				
	PAGE 31 :	PR223 add " * "no stuff				
	PAGE 31 :	PR221,PQ57 remove " * " stuff				
	D3A	PAGE 3:	R550 change to 100k and connect to U23 pin4.			
		PAGE 4:	Add R3028 and C3044 for S3 power reduction sequence.			
		PAGE 4:	R894 add " * "no stuff			
		PAGE 4:	Add R922, D48, R929, D49 power sequence.			
		PAGE 7:	Add G3.			
		PAGE 8:	Add R908, R909 for USB Sleep and Charge.			
		PAGE 8:	C784 change to 27pF.			
		PAGE 8:	C774 change to 33pF.			
		PAGE 8:	Net name change to USB_BUS_SW2_R abd USB_BUS_SW3_R.			
		PAGE 8:	R679 change to SBY100505T-221Y-N_300MA for EMI			
		PAGE 8:	Remove discrete VGA PCIE CLK " CLK_PCIE_VGA ; CLK_PCIE_VGA#"			
		PAGE 9:	R730 remove " * " for USB2.0 SKU Board_ID9 PD.			
		PAGE 9:	R721 remove " * " for no HDMI SKU			
		PAGE 10:	Remove R598.			
		PAGE 10:	Add C393 for LCD flicker.			
		PAGE 14:	R3022, R3023, R3024, R3025 add " * "no stuff .			
		PAGE 15:	Add L20 for EMI.			
		PAGE 15:	CN14 P/N change to DFDS15FR252.			
		PAGE 17 :	USB3.0 EEPROM U3001 Change Main source P/N: AKE37ZN0Q01; 2nd source P/N: AKE37FN0N01			
		PAGE 17 :	USB3.0 Chip U3003 Change to MP P/N: AJ202000T03			
DOC NO. 204		PROJECT MODEL :	BLB	APPROVED BY:	DATE:	2010/12/21
		PART NUMBER:	31BLBMB0IG0	DRAWING BY:	REVISION:	F3A
						 Quanta Computer Inc. PROJECT : BLB Size Document Number Change list Date: Friday, December 24, 2010 Rev F3A Sheet 34 of 36

Model		REV	CHANGE LIST				MODEL BLB			
							PAGE	FROM	To	
BLB MB	D3A	PAGE 17 : Add L73 for EMI.						1	2A	3A
		PAGE 18 : C603 add " * " no stuff for ODD zero power.						2	2A	3A
		PAGE 18 : Add R614, Q3503 for ODD zero power.						3	2A	3A
		PAGE 18 : C541, C1, C503, C481remove " * " stuff for EMI.						4	2A	3A
		PAGE 18 : Add C3045, C3046, C3047, C589, C594 for EMI.						5	2A	3A
		PAGE 19 : C840, C471, C798 remove " * " stuff for EMI.						6	2A	3A
		PAGE 20 : C533 change to 47p for EMI.						7	2A	3A
		PAGE 20 : Add C30458 for EMI.						8	2A	3A
		PAGE 22: Add R3029, R3030 for USB Sleep and Charge.						9	2A	3A
		PAGE 22: R923, R924, R925 change to PU to +3VPCU.						10	2A	3A
		PAGE 22: R895 add " * " no stuff						11	2A	3A
		PAGE 22: R536,R535 change to 4.7K						12	2A	3A
		PAGE 23 : Add L3002,L3003, C3049, R3031, R3032 , C106 for EMI.						13	2A	3A
		PAGE 23 : C104 remove " * " stuff						14	2A	3A
		PAGE 23 : HOLE20, HOLE21, HOLE26 change footprint.						15	2A	3A
		PAGE 23 : Remove Hole5, Hole9						16	2A	3A
		PAGE 24 : Remove Q22 and add Q3504 for card reader LED.						17	2A	3A
		PAGE 25 : PC51, PC52, PC133, PR5, PC2 stuff for EMI.						18	2A	3A
		PAGE 26 : PD14 remove " * " stuff.						19	2A	3A
		PAGE 26 : PR351 add " * " no stuff.						20	2A	3A
		PAGE 26 : PR79 change to 150K ohm 1%						21	2A	3A
		PAGE 26 : PR352 change to 147K ohm 1%						22	2A	3A
		PAGE 26 : PU5 Change Main source P/N: AL006686000; 2nd source P/N: AL006188000						23	2A	3A
		PAGE 28 : Add PR357, PC157.						24	2A	3A
		PAGE 28 : PR260, PR262 add " * " no stuff.						25	2A	3A
		PAGE 29 : PC143 change to 330U/2V_7343P_E9c.						26	2A	3A
		PAGE 30 : PR338 change to 750 ohm 1%						27	2A	3A
		PAGE 30 : PR332 change to 2.8K ohm 1%						28	2A	3A
		PAGE 30 : PR322 change to 330p 50V						29	2A	3A
		PAGE 30 : PR334 change to 2K ohm 1%						30	2A	3A
		PAGE 30 : PR31 change to 1.47K ohm 1%						31	2A	3A
		PAGE 30 : PR139 change to 3.16K ohm 1%						32	2A	3A
		PAGE 30 : PR132 remove " * " stuff.						33	2A	3A
		PAGE 30 : PC300 remove " * " stuff.						34	2A	3A
		PAGE 30 : PR156, PR127, PR128, PC4 remove " * " stuff.						35	2A	3A
		PAGE 30 : PQ23, PQ20, PQ24, PQ25, PQ60, PQ61 Change Main source P/N: BAM02000000 ; 2nd source P/N: BAM14120000								
		PAGE 30 : PC145, PC56, PC146, PC57, PC314, PC316 change to 330U/2V_7343P_E9c.								
		PAGE 30 : PR341, PC329 stuff for EMI.								
		PAGE 31 : Add PR205, PQ49, PR198, PQ45.								
E3A	PAGE 2 : Add C113,C114,C117 for ESD									
	PAGE 4 : Add R930									
	PAGE 4 : C606 remove " * " stuff.									
	PAGE 4 : Change the C591 to 330uF .									
	PAGE 4 : Add C116 for ESD									
	PAGE 6 : R922 remove " * " stuff.									
	PAGE 6, 7, 8, 9, 10, 11 : PCH U25 change to AJSLH9D0T06									
	PAGE 7: U29 change to AKE391P0N00									
	PAGE 7 : Add C86 for ESD									
	PAGE 10: Add C69, C71,C78,C81,C82,C90,C92,C112,C118,C119,C123,C132,C133,C134 for ESD									
	PAGE 15: MR1 remove 2ND soucre AL002618001, add 2ND soucre AL003661003									
	PAGE 15: L20 change footprint.									
	PAGE 16 : C720 remove " * " stuff.									
	PAGE 16 : Add R883									
	PAGE 16 : R644 remove " * " stuff									
	PAGE 16 : R605,R648,R649,R568,R569,R570,R571,R572 add " * " no stuff									
	PAGE 17 : CN3000 change footprint to usb-020053gr009m5176r-9p-smt									
	PAGE 17: U3001 change to AKE37ZN0Q01									
	PAGE 17: L73 change footprint.									
	PAGE 17 : R3020 change to 1.47k.									
	PAGE 17 : C3036, C3035 change to 15pf									
	PAGE 19 : CN2 change P/N to DFHD04MR752									
	PAGE 19 : CN22,CN23 change footprint.									
	PAGE 19 : C832 and C833 change to 150p for EMI									
	PAGE 20 : C958,C959,C960,C961 change to 0.01U/100V 0805									
DOC NO. 204		PROJECT MODEL :		BLB	APPROVED BY:	DATE:	2010/12/21	 Quanta Computer Inc. PROJECT : BLB		
		PART NUMBER:		31BLBMB0IG0	DRAWING BY:	REVISION:	F3A			
								Size	Document Number	
								Date:	Friday, December 24, 2010	
								Sheet	35 of 36	
								Rev	F3A	
								Change list		

Model		REV	CHANGE LIST				MODEL BLB		
							PAGE	FROM	To
BLB MB	E3A	PAGE 20 : Remove C3048 and add D24,D25 for ESD					1	2A	3A
		PAGE 21 : R276,R275,R280,R279,R289,R277,R274,R288 change to 33ohm for EMI.					2	2A	3A
		PAGE 22: U10 change to AKE37FN0N01					3	2A	3A
		PAGE 22: U5 remove 2ND soucre AKE3K8B0Y17					4	2A	3A
		PAGE 22 : Add R122 for ESD					5	2A	3A
		PAGE 23: CN3 remove 2ND soucre DFFC34R002					6	2A	3A
		PAGE 23: HOLE2, HOLE3 ,Hole27 change footprint and P/N.					7	2A	3A
		PAGE 23: L3002, L3003 change footprint.					8	2A	3A
		PAGE 23 : C446 remove " * " stuff for EMI.					9	2A	3A
		PAGE 30 : Add C115 for ESD					10	2A	3A
		PAGE 30 : Change the PC132 to 0.15uF from 0.1uF.					11	2A	3A
		PAGE 30 : Change the PR338 to 7870hm from 750Ohm					12	2A	3A
		PAGE 30 : Change the PR334 to 20kOhm from NC.					13	2A	3A
		PAGE 04 : Change the C95,C149 to 22uF from 10uF.					14	2A	3A
		PAGE 04 : Change the C98,C99 to 22uF from NC.					15	2A	3A
		PAGE 29 : PR40 *10K/F 4 Change the 10K/F 4					16	2A	3A
		PAGE 30 : PR11 change to 20.5k					17	2A	3A
		PAGE 25 : Add PU10 for ESD					18	2A	3A
		PAGE 20 : C124,C121,C108,C105 add "51@" for Giga LAN					19	2A	3A
		PAGE 17 : D3000 ,Y3000,U44 remove 2ND source.					20	2A	3A
		PAGE 25 : PD9 remove 2ND source.					21	2A	3A
	F3A	PAGE 9 : NET: ODD_PRSNT# change to PCH pin U2 <SATA4GP/GPIO16>					22	2A	3A
		PAGE 9 : NET: BOARD_ID9 change to PCH pin M5 <SATA3GP/GPIO37>					23	2A	3A
		PAGE 8 : R358 add "" no stuff.					24	2A	3A
		PAGE 8 : R847 remove "S3@" and stuff.					25	2A	3A
		PAGE 23 : Add C3050, C3051 for EMI					26	2A	3A
		PAGE 20 : Add C160,C170,C180,C184 for EMI					27	2A	3A
							28	2A	3A
							29	2A	3A
							30	2A	3A
							31	2A	3A
							32	2A	3A
							33	2A	3A
							34	2A	3A
							35	2A	3A
DOC NO. 204		PROJECT MODEL : PART NUMBER:		BLB 31BLBMB0IG0	APPROVED BY: DRAWING BY:	DATE: REVISION:	2010/12/21 F3A	 Quanta Computer Inc. PROJECT : BLB Size Document Number Change list Date: Friday, December 24, 2010 Rev F3A Sheet 36 of 36	