

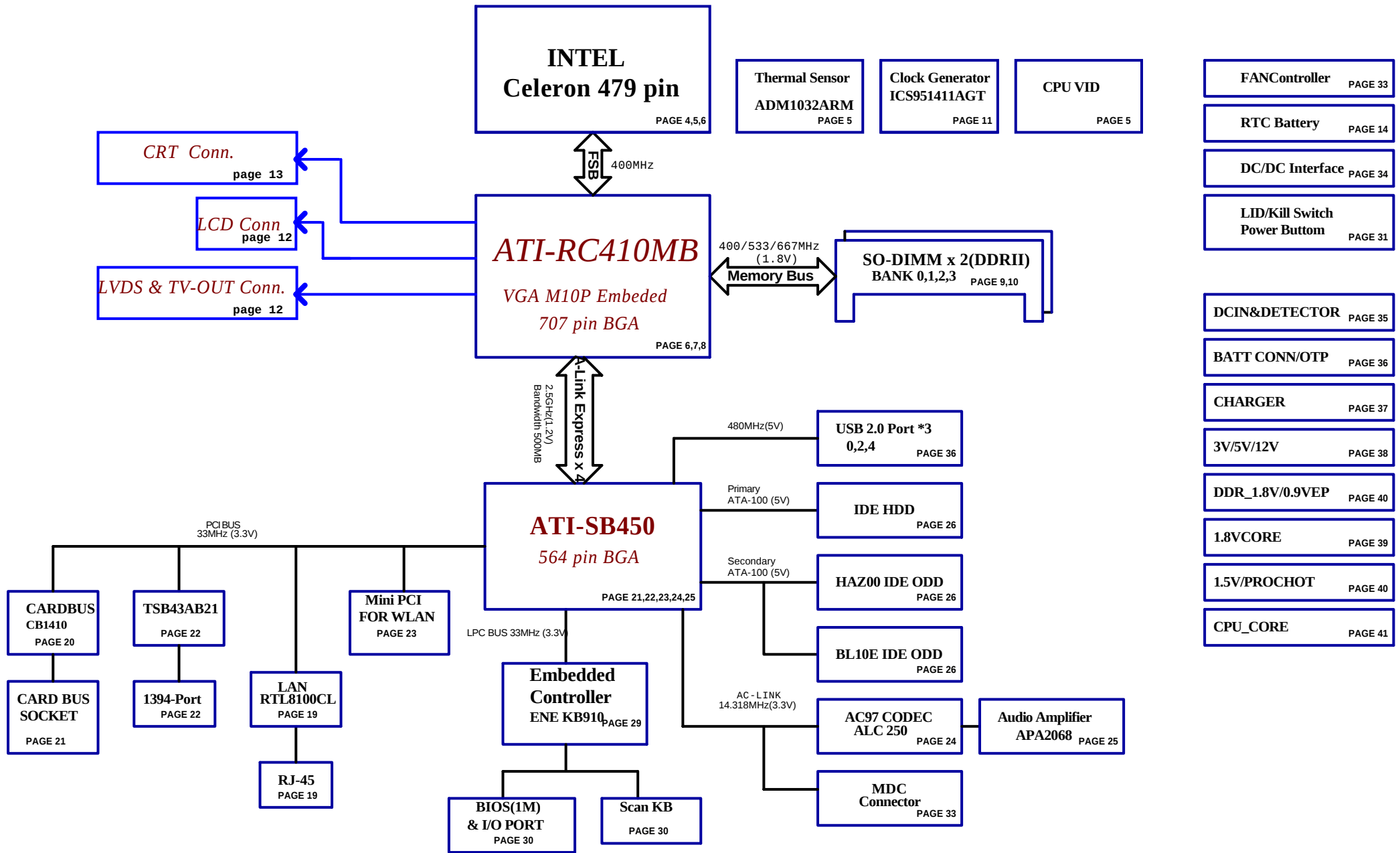
HAZ00/HTW01

LA-2861 REV 1.0 Schematic

UFC-PGA Dothan/ RC410MD(RC410MB)/ SB450
2005-07-11 Rev.1.0

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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	Black Diagram
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HAZ00 & HTW01 LA-2861 FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
TI 1410	AD20	2	PIRQA/PIRQB
LAN	AD22	1	PIRQG
Mini-PCI(WLAN)	AD18	3	PIRQF/PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS951413BGLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

STATE	SIGNAL					
	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

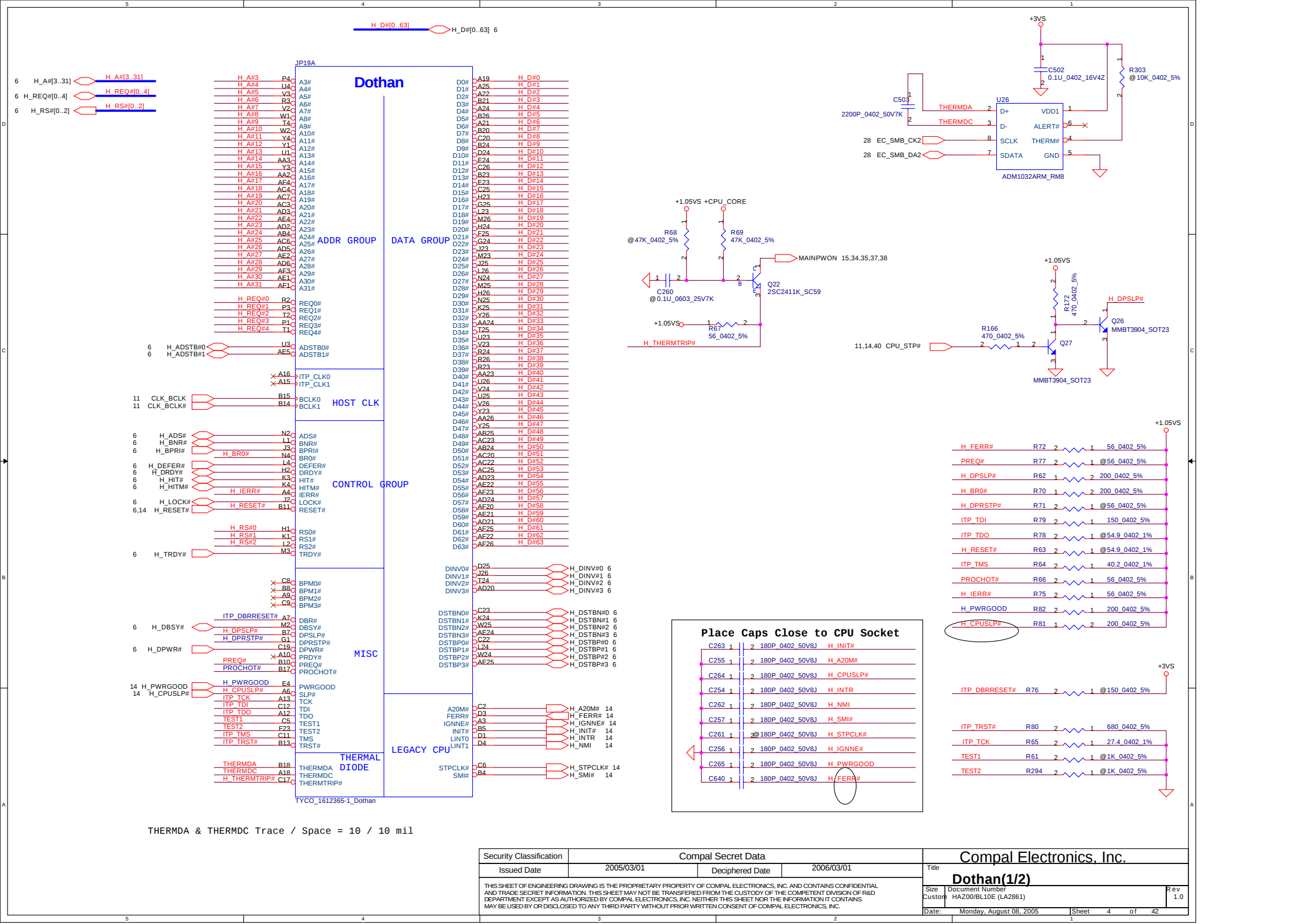
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

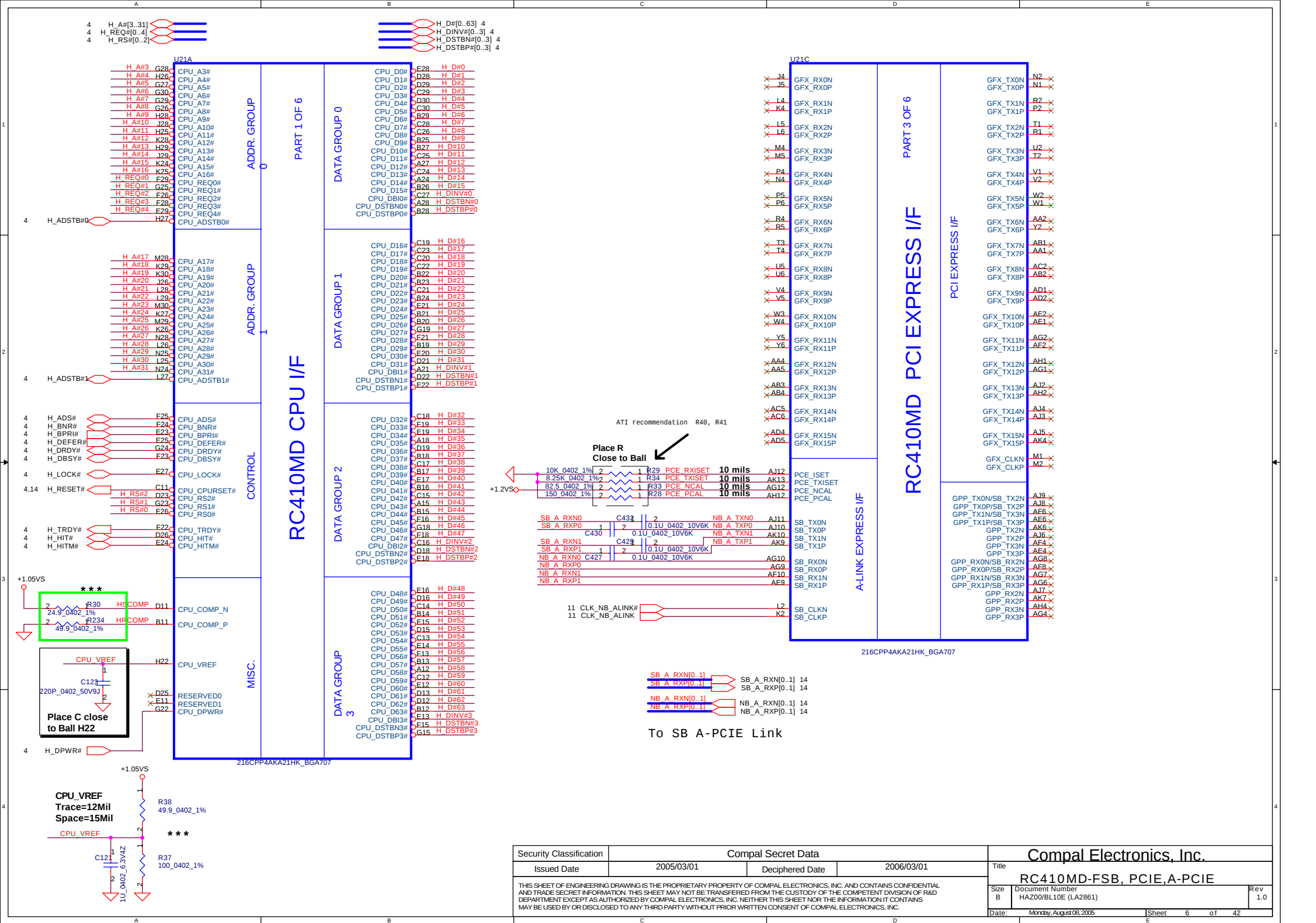
Board ID	PCB Revision
0	0.1, 0.2
1	0.3
2	1.0
3	
4	
5	
6	
7	

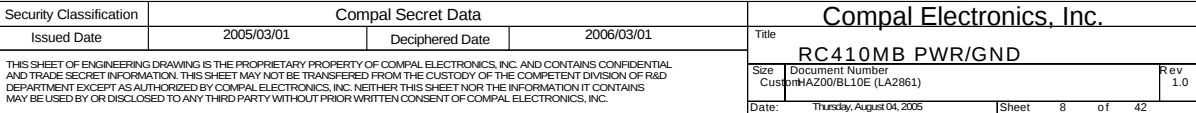
SKU ID	SKU Status
0	
1	
2	
3	
4	
5	1 Buttons
6	
7	7 Buttons

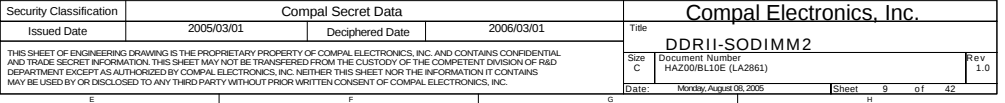
	HDD Password
0	NO
1	Yes

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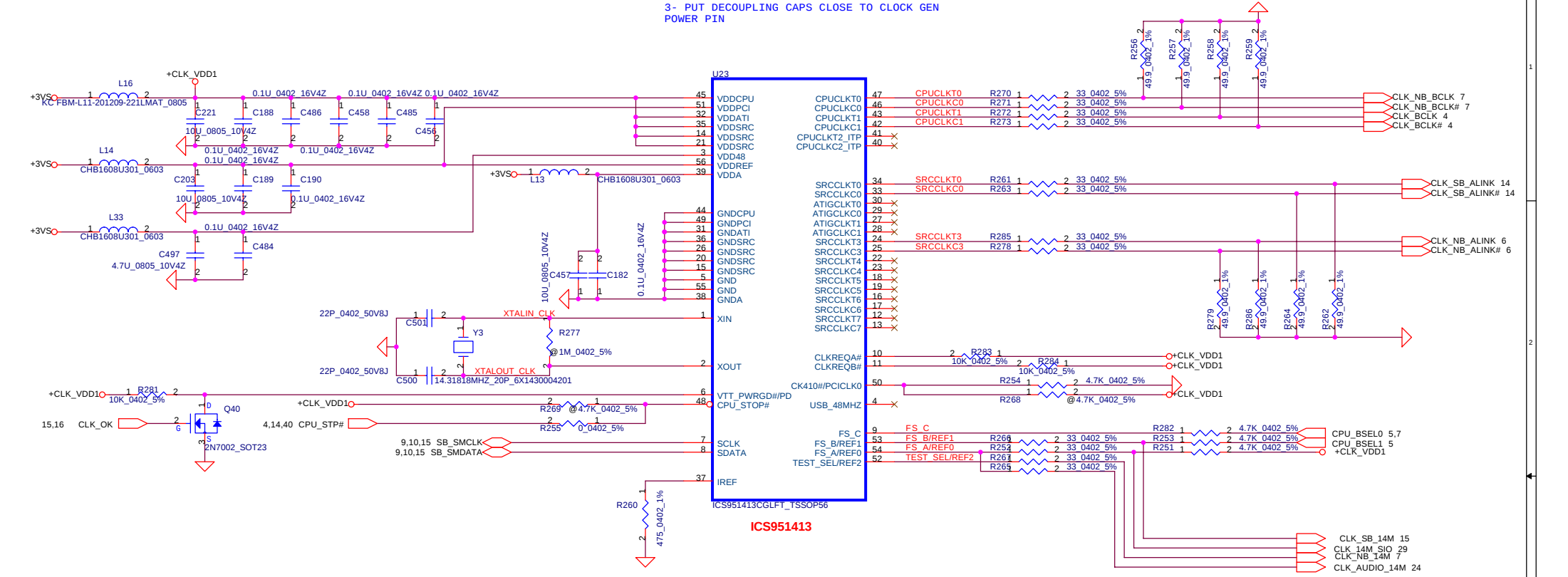






Clock Generator

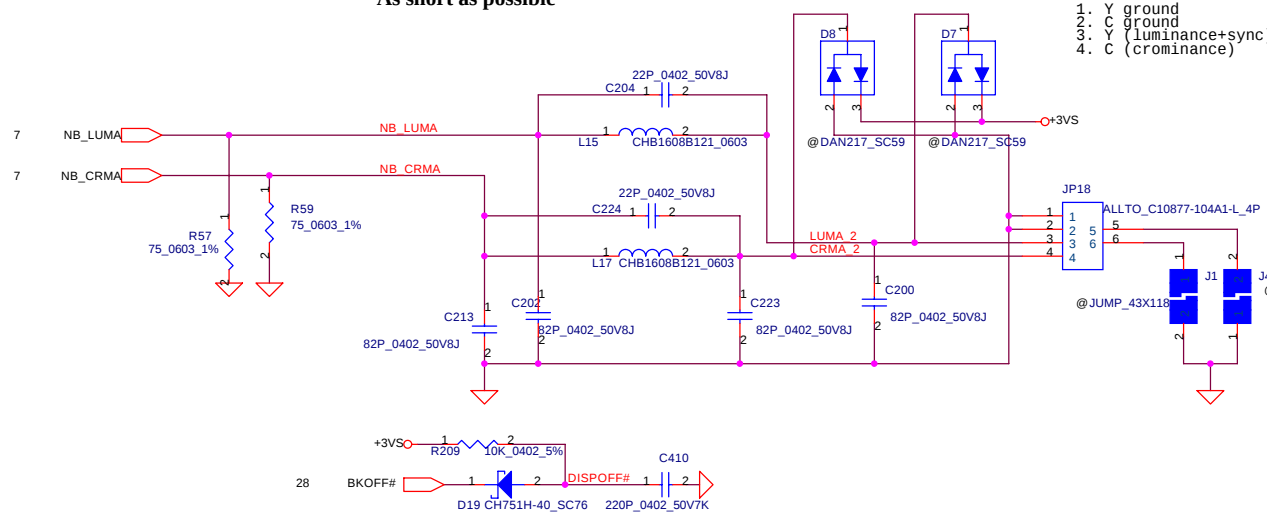
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



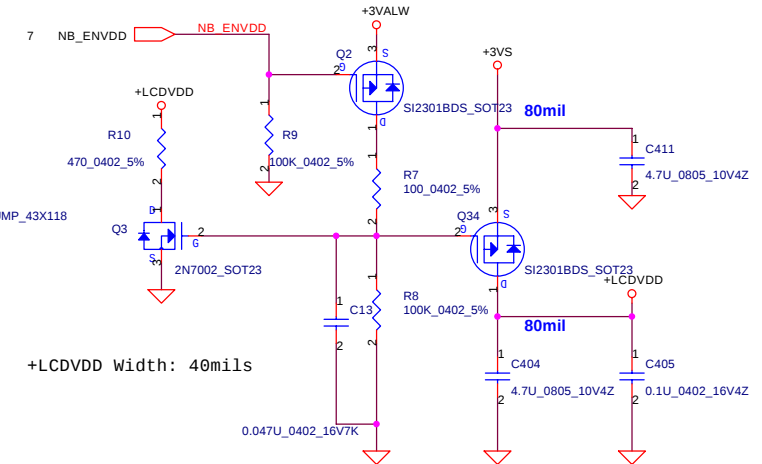
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
1	1	1	---	---	---	---	---

TV-OUT CONNECTOR

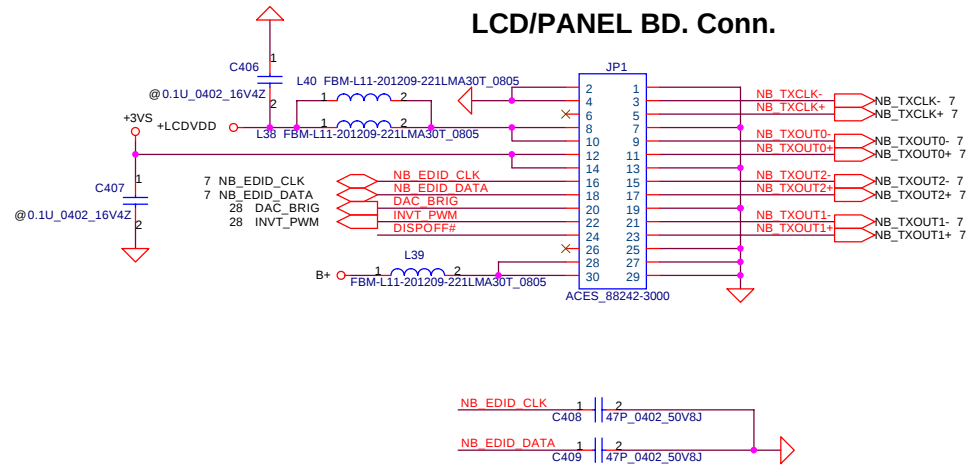
Reduce LUMA_1 and CRMA_1 length
As short as possible



PANEL +LCDVDD CTRL CKT

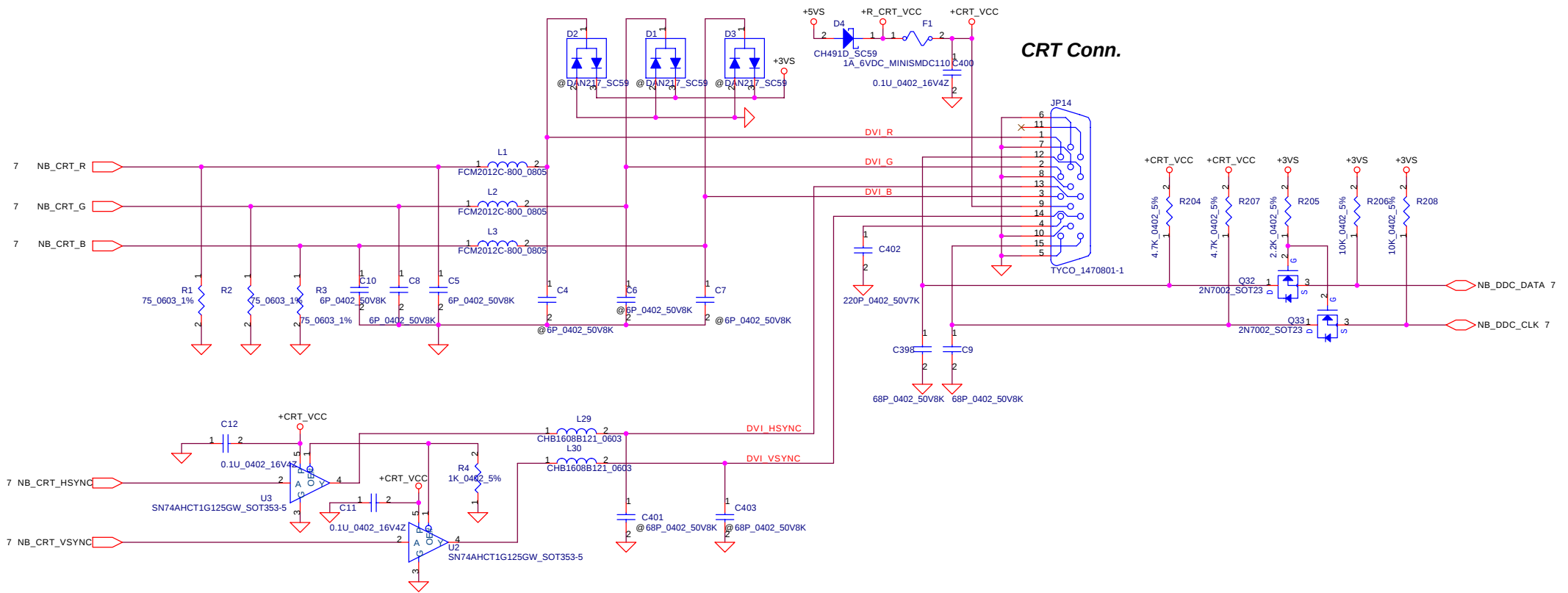


LCD/PANEL BD. Conn.

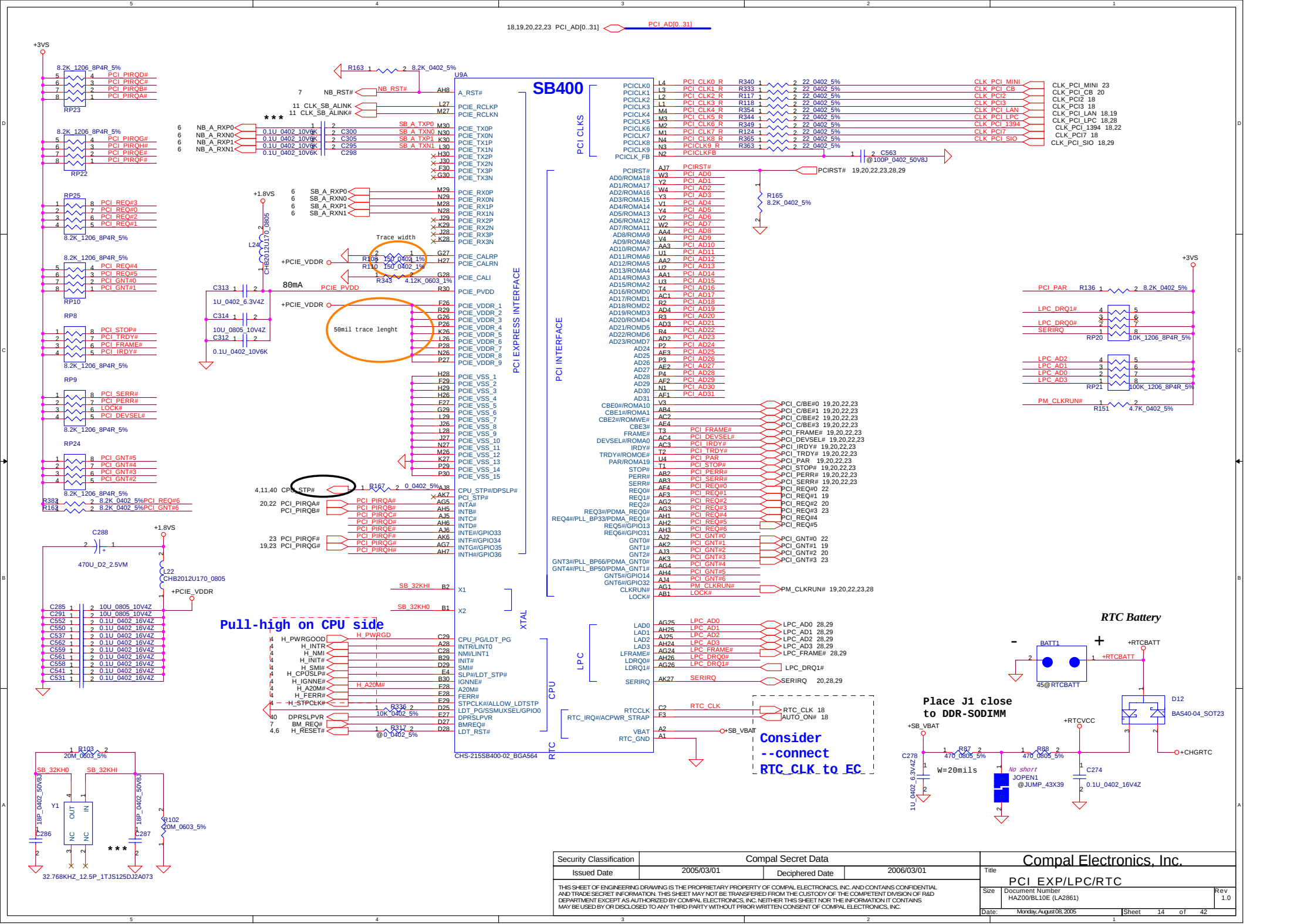


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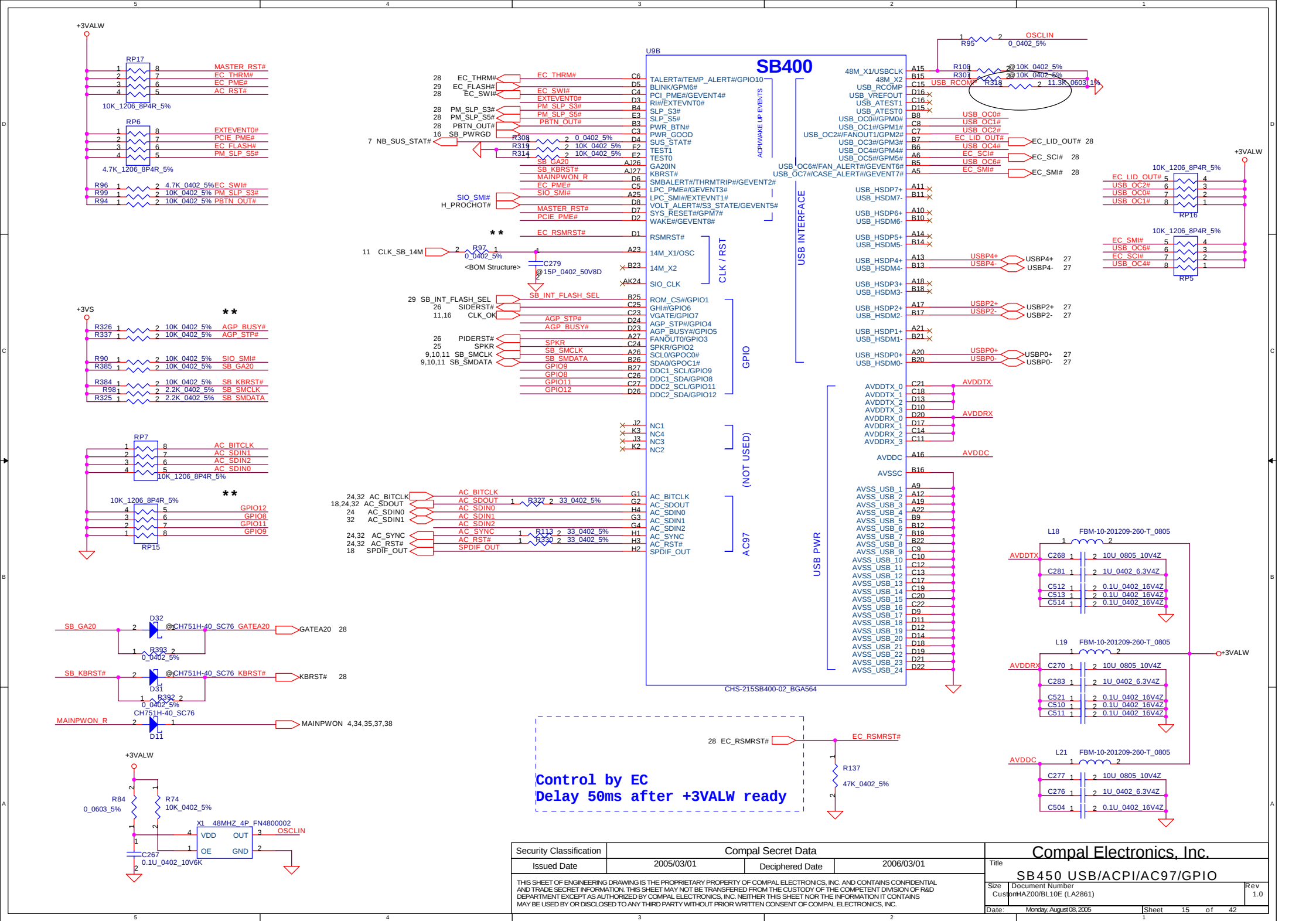
CRT CONNECTOR



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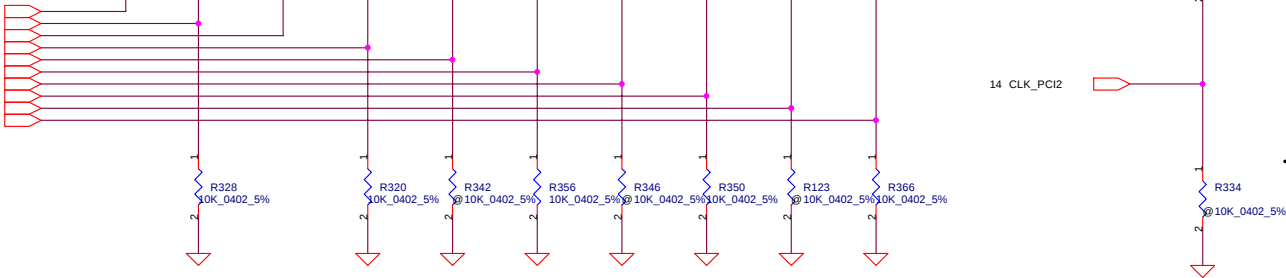
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Size		Document Number		Rev	
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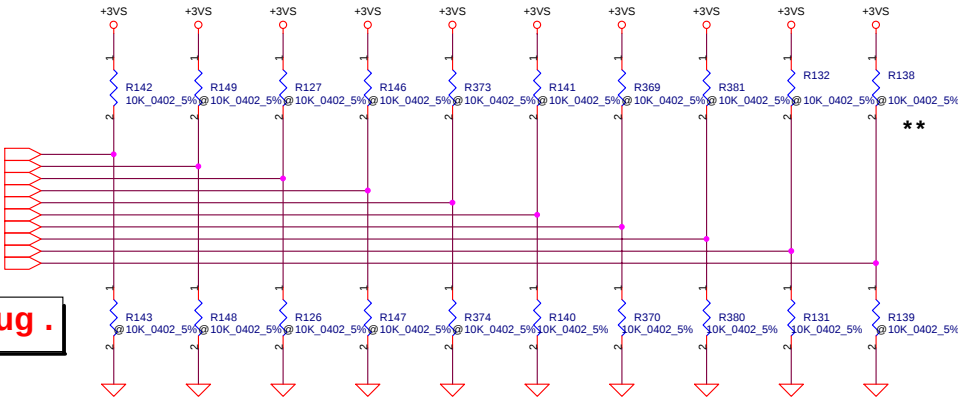
REQUIRED STRAPS

14 AUTO_ON#
15,24,32 AC_SDOUT
14 RTC_CLK
15 SPDIF_OUT
14 CLK_PCI3
14,19 CLK_PCI_LAN
14,28 CLK_PCI_LPC
14,22 CLK_PCI_1394
14 CLK_PCI7
14,29 CLK_PCI_SIO



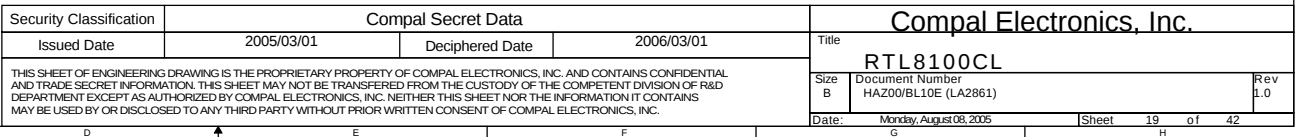
	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	CLK_PCI_MINI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL DEFAULT	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Clock input buffer DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712) DEFAULT	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH DEFAULT	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Crytsal Pad

16,26 IDE_PDDACK#
14,19,20,22,23 PCI_AD31
14,19,20,22,23 PCI_AD30
14,19,20,22,23 PCI_AD29
14,19,20,22,23 PCI_AD28
14,19,20,22,23 PCI_AD27
14,19,20,22,23 PCI_AD26
14,19,20,22,23 PCI_AD25
14,19,20,22,23 PCI_AD24
14,19,20,22,23 PCI_AD23

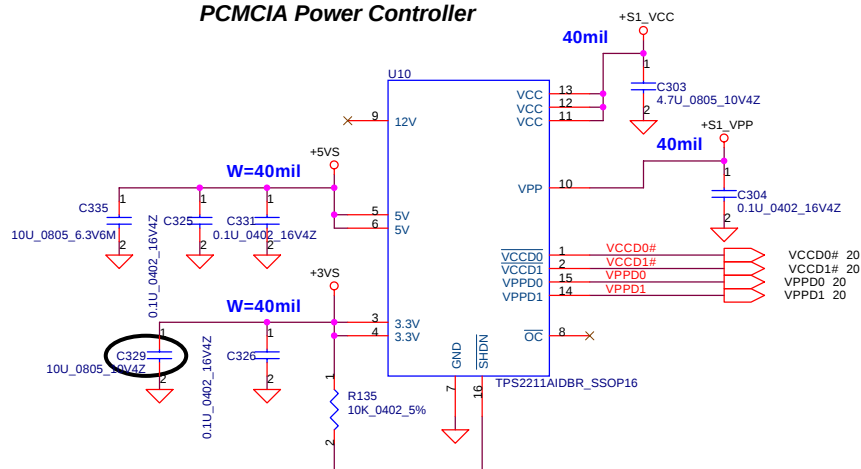


DEBUG STRAPS

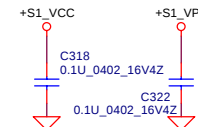
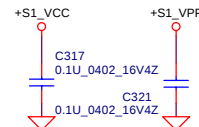
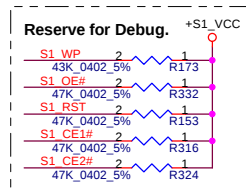
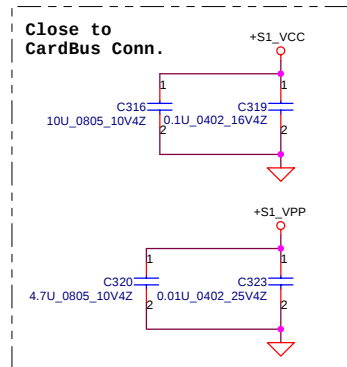
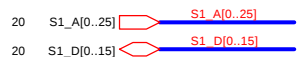
	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL DEFAULT	BYPASS ACPI BCLK DEFAULT	BYPASS IDE PLL DEFAULT	USE EEPROM PCIE STRAPS DEFAULT	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



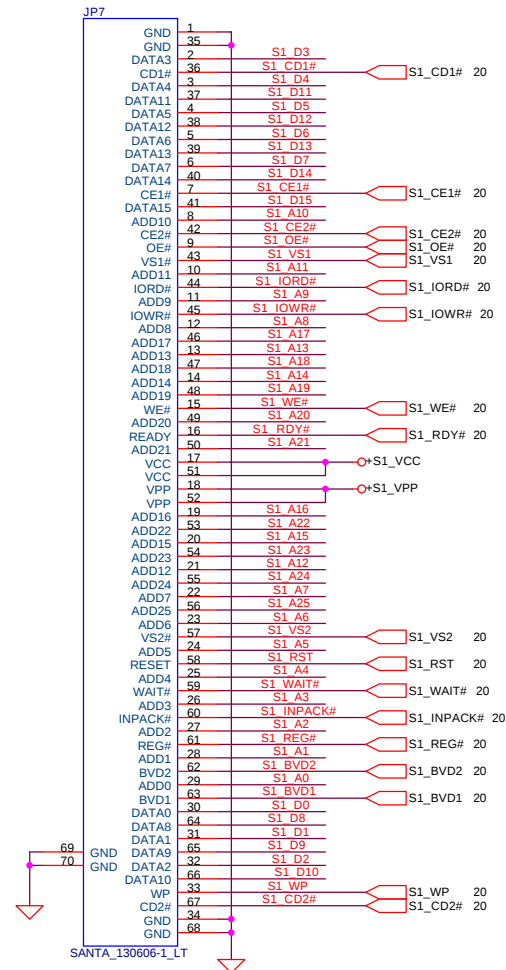
PCMCIA Power Controller



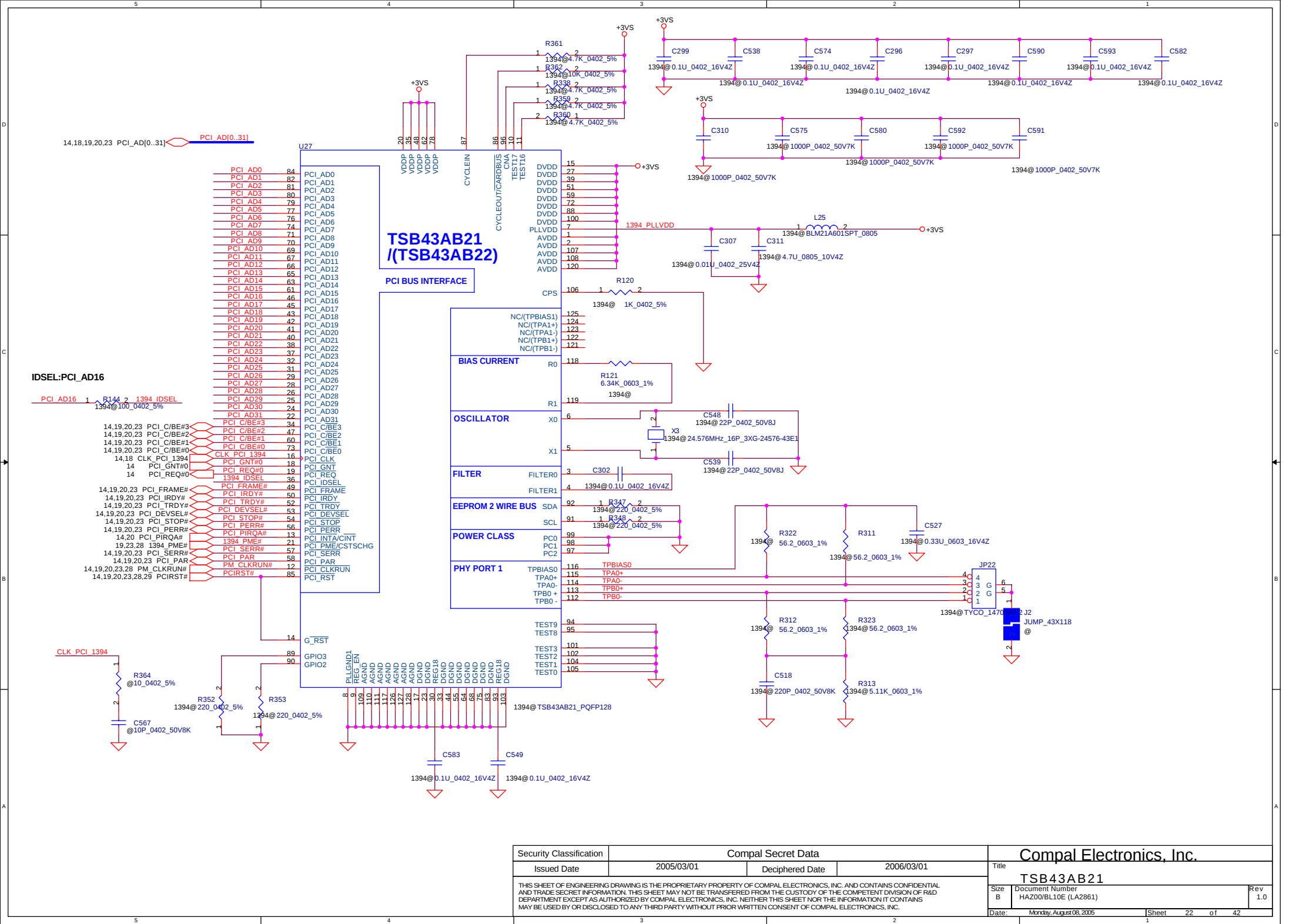
CardBus Socket



CardBus Socket



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PCI_AD[0..31] PCI_AD[0..31] 14,18,19,20,22

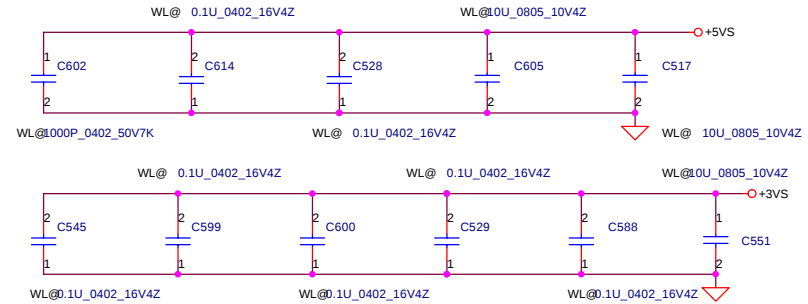


Diagram illustrating the connection between the R456 component and the JP29 connector (labeled JP29).

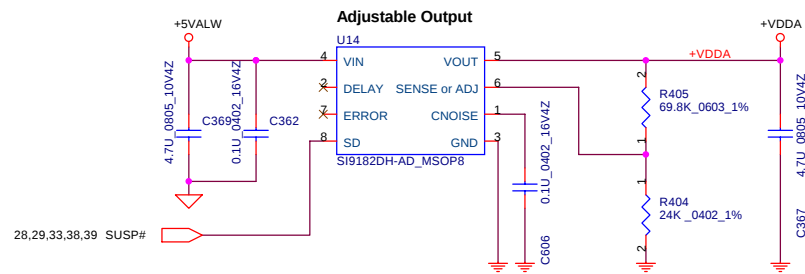
The R456 component has pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20. The JP29 connector has pins 1 through 20.

The connections are as follows:

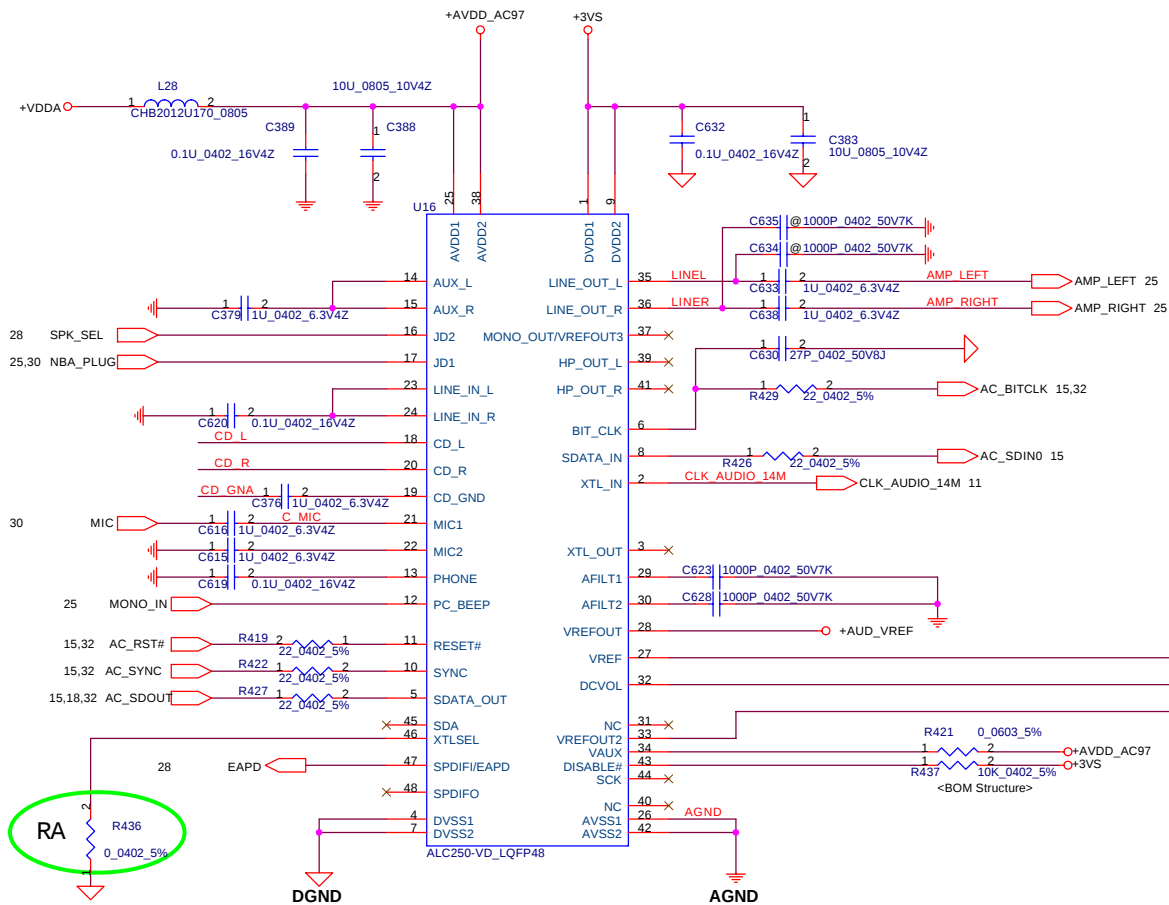
- R456 Pin 1 to JP29 Pin 1 (CLK_PCI_MINI)
- R456 Pin 2 to JP29 Pin 2 (@0_0402_5%)
- R456 Pin 3 to JP29 Pin 3 (+5VS)
- R456 Pin 4 to JP29 Pin 4 (PCIRST#)
- R456 Pin 5 to JP29 Pin 5 (PCI FRAME#)
- R456 Pin 6 to JP29 Pin 6 (PCI TRDY#)
- R456 Pin 7 to JP29 Pin 7 (PCI AD9)
- R456 Pin 8 to JP29 Pin 8 (PCI C/BE#3)
- R456 Pin 9 to JP29 Pin 9 (PCI AD8)
- R456 Pin 10 to JP29 Pin 10 (PCI C/BE#2)
- R456 Pin 11 to JP29 Pin 11 (PCI C/BE#1)
- R456 Pin 12 to JP29 Pin 12 (PCI AD7)
- R456 Pin 13 to JP29 Pin 13 (PCI AD5)
- R456 Pin 14 to JP29 Pin 14 (PCI AD3)
- R456 Pin 15 to JP29 Pin 15 (PCI AD1)
- R456 Pin 16 to JP29 Pin 16 (PCI AD0)
- R456 Pin 17 to JP29 Pin 17 (PCI AD2)
- R456 Pin 18 to JP29 Pin 18 (PCI AD4)
- R456 Pin 19 to JP29 Pin 19 (PCI AD6)
- R456 Pin 20 to JP29 Pin 20 (PCI C/BE#0)

The JP29 connector is labeled JP29 and ACES_85201-2005.

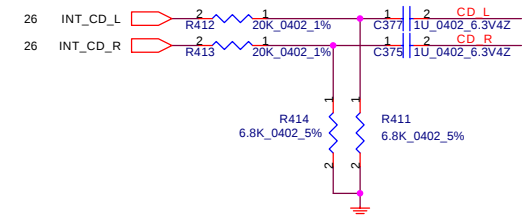
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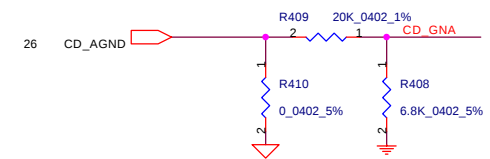
AC97 Codec



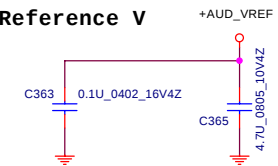
Audio Signal Bias Circuit



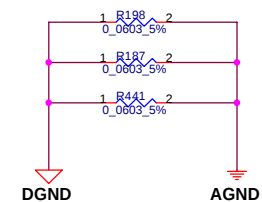
CD_AGND To CD_GNA Bypass



Analog Reference V

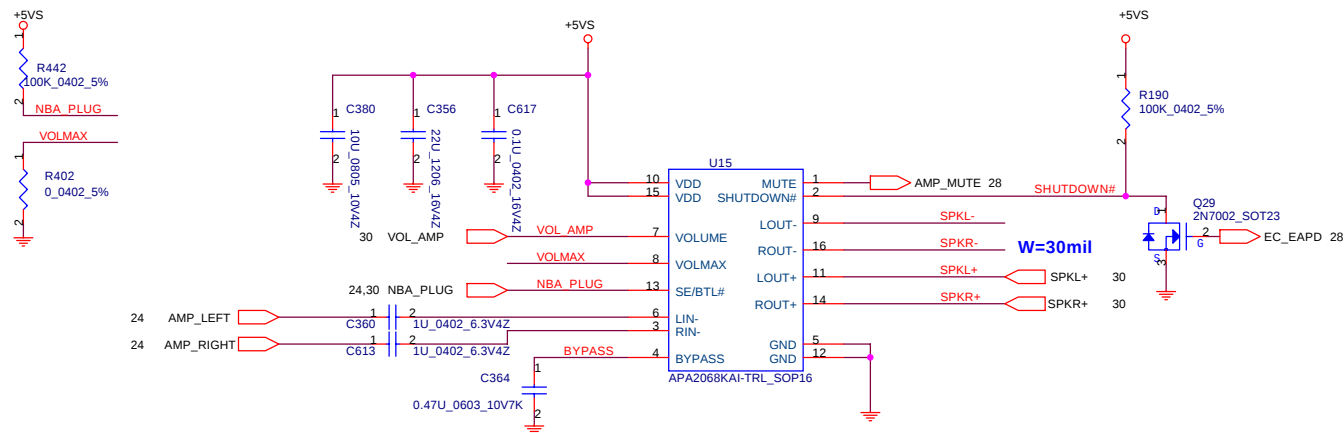


DGND To AGND Bypass

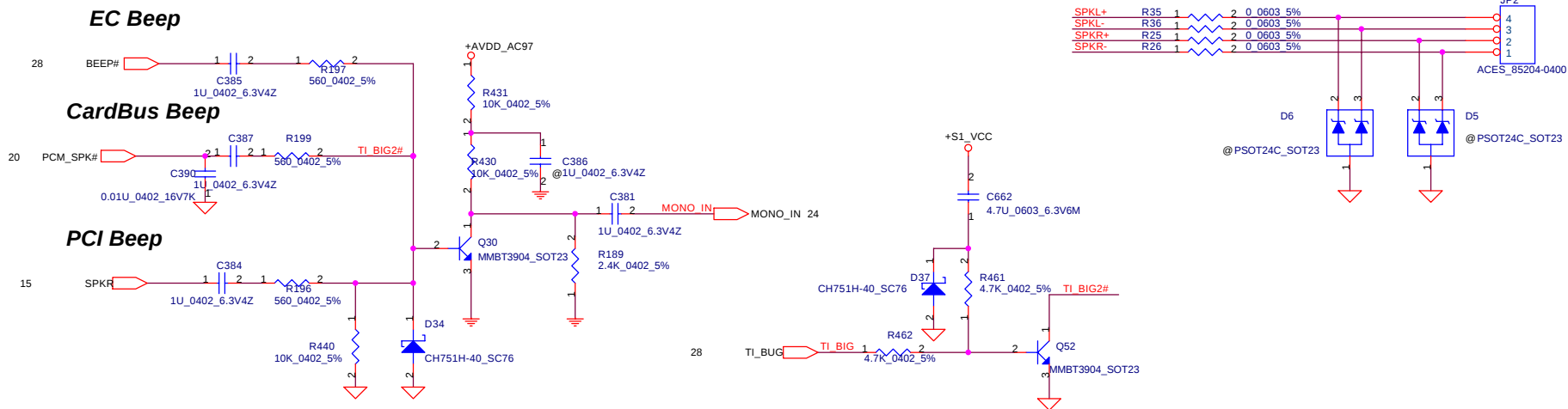


WITH 14.318MHz : RA POP
WITH 24.576MHz : RA DEPOP

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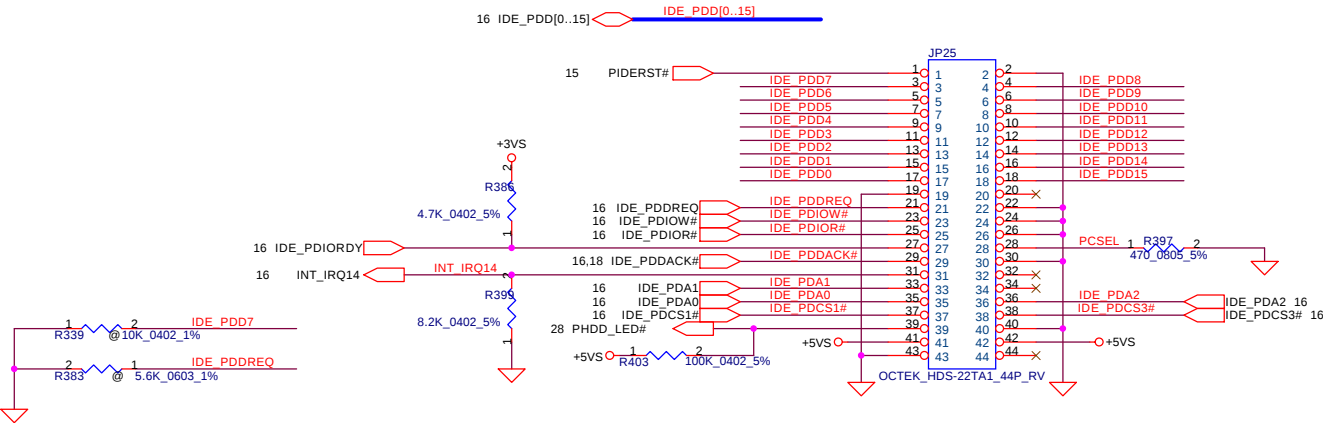


Speaker Conn.

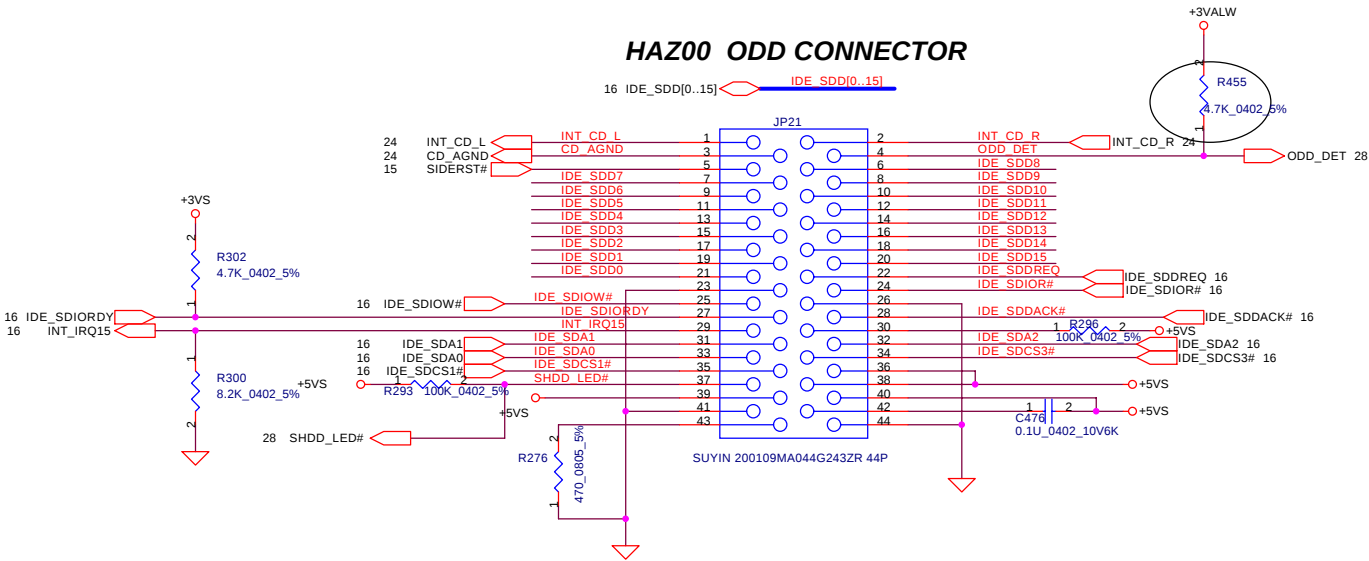


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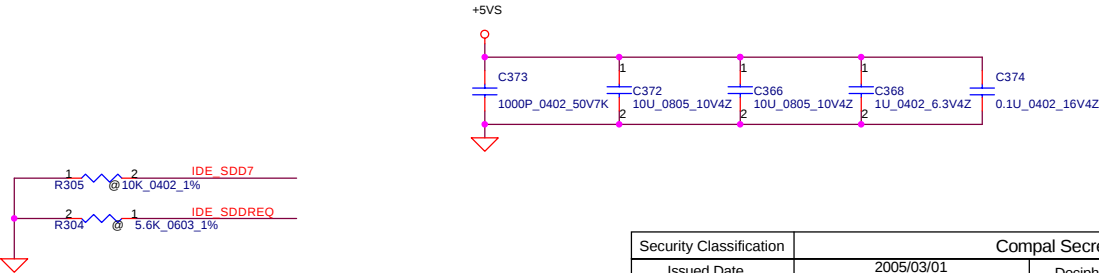
HDD CONNECTOR



HAZ00 ODD CONNECTOR

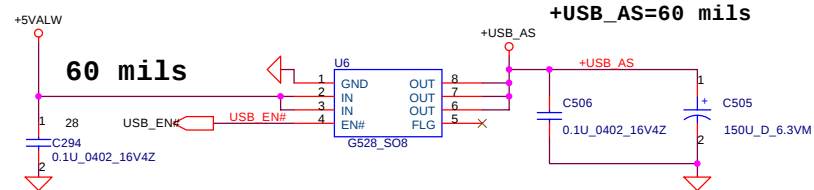


Place caps. near HDD
CONN.

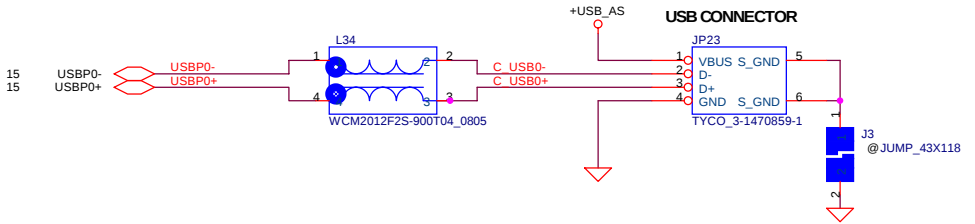


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Size B	Document Number HAZ00/BL10E (LA2861)			Rev 1.0
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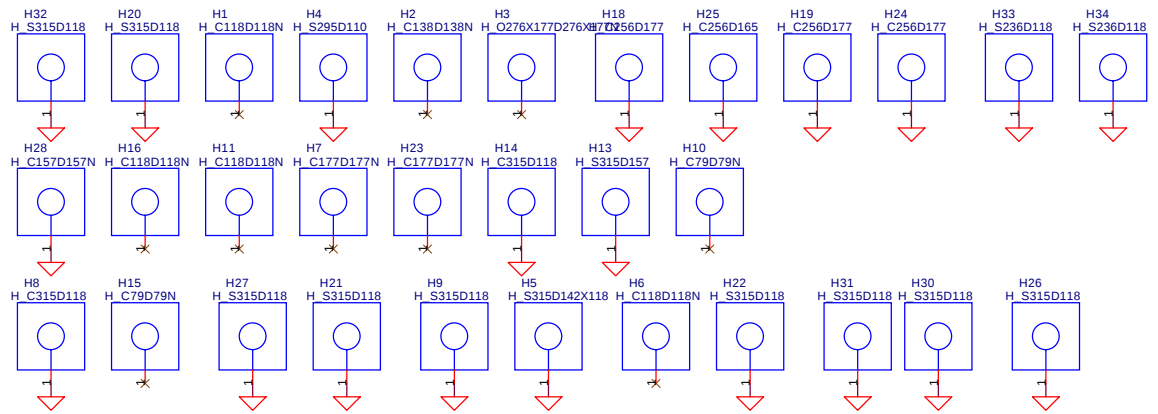
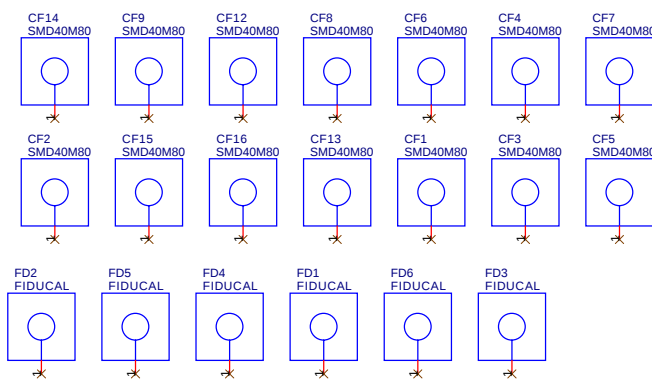
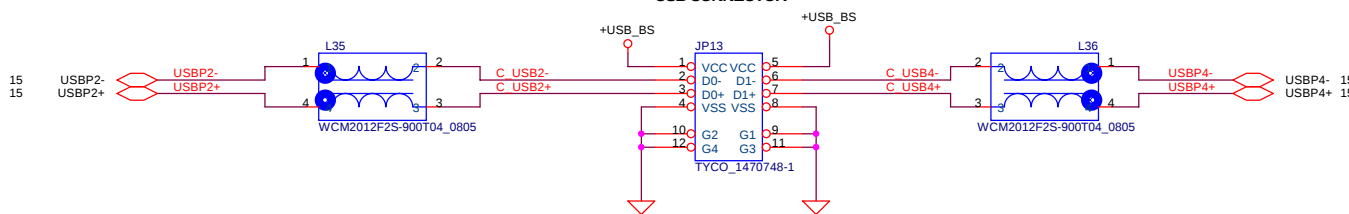
1.4A



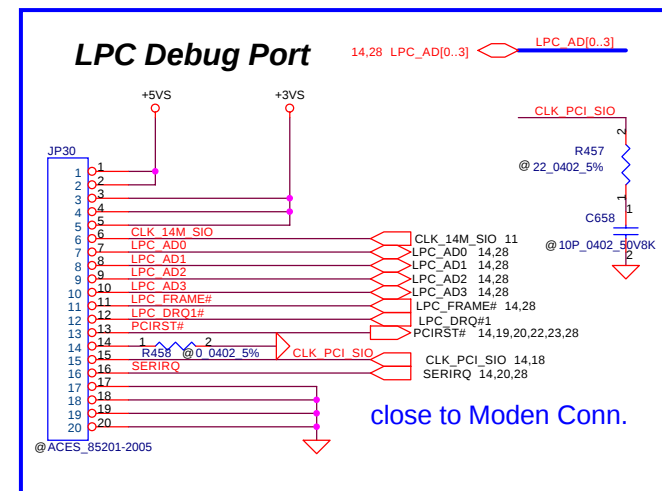
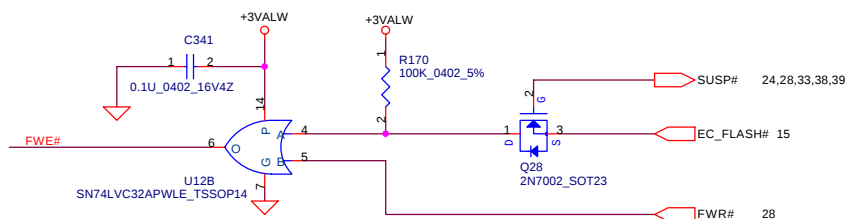
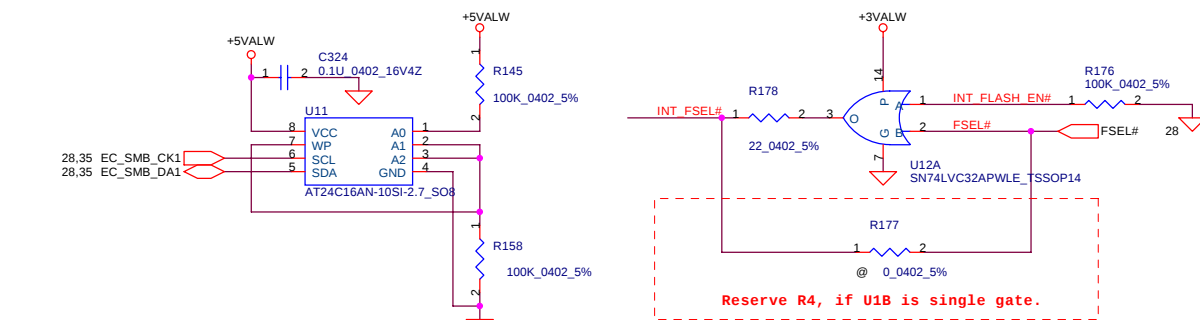
Keep 20 mils minimum spacing between USB signals and others signals



USB CONNECTOR



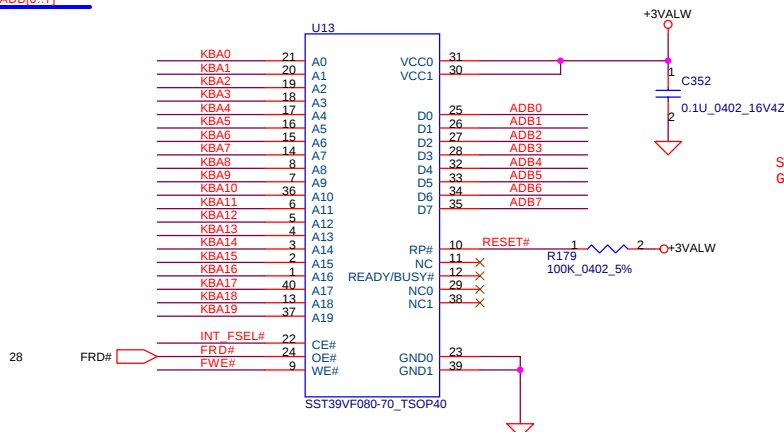
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Size	B	Document Number	HAZ00/BL10E (LA2861)	Rev 1.0
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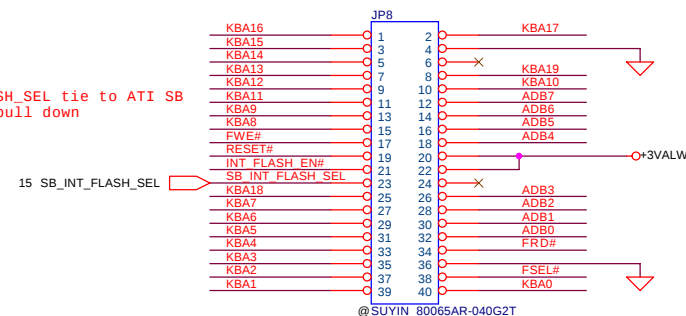
1MB Flash ROM

28 KBA[0..19] KBA[0..19]

28 ADB[0..7] ADB[0..7]

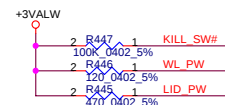
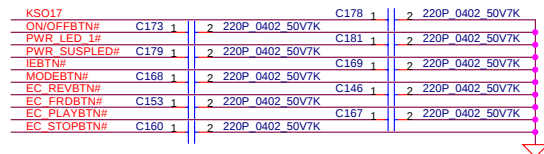
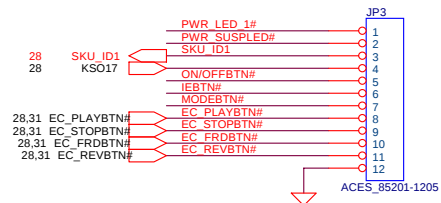
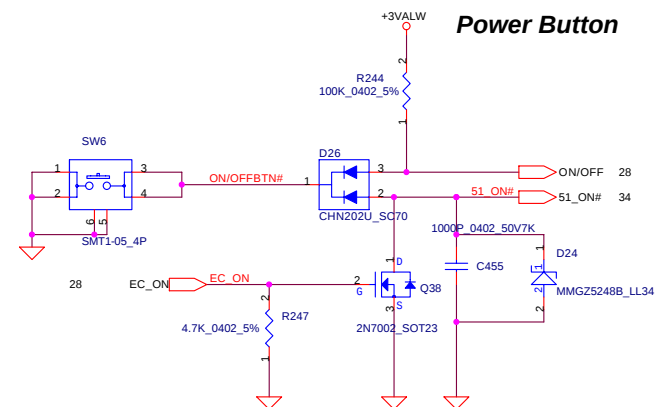
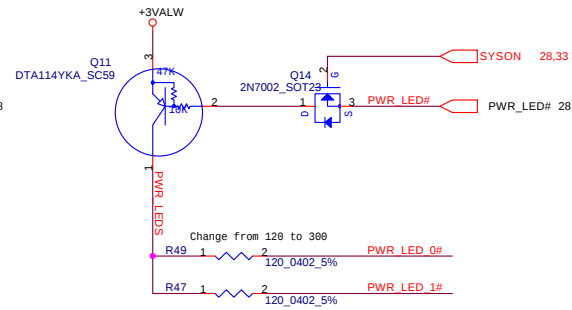
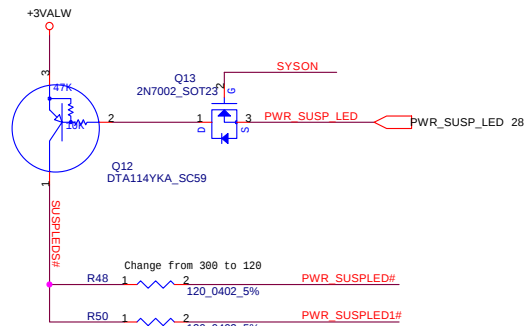
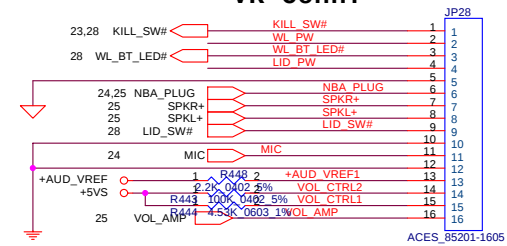


1MB ROM Socket

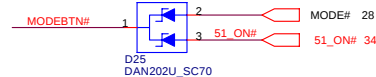
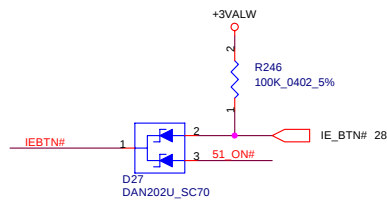


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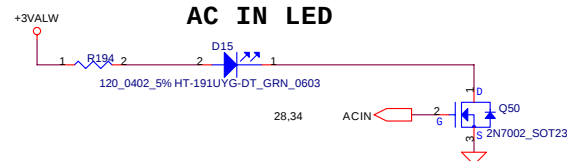
Switch Board Conn.

**VR Conn.**

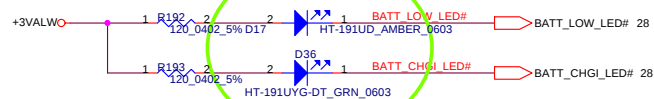
Power Button



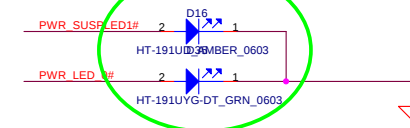
AC IN LED



BATTERY CHG



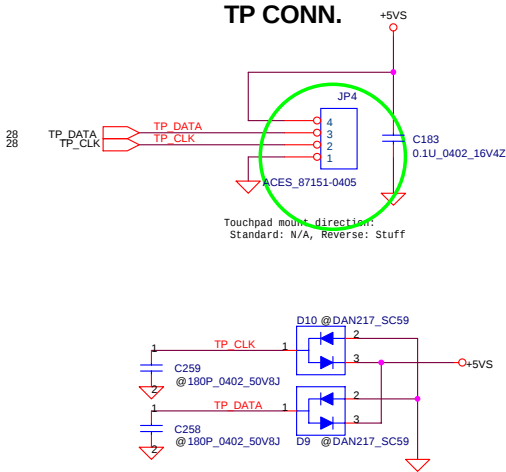
POWER/ON LED



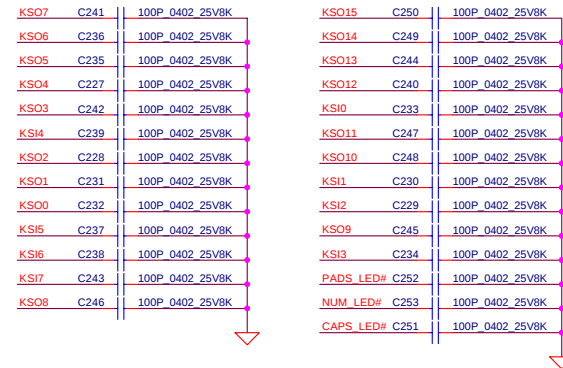
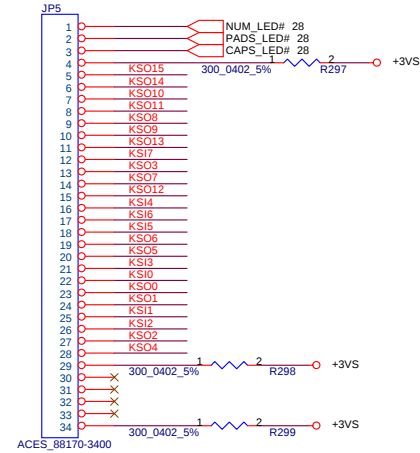
HDD LED



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				Cust	brnHAZ00BL10E (LA2861)	
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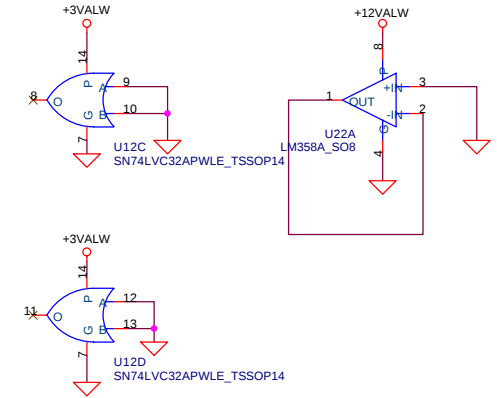
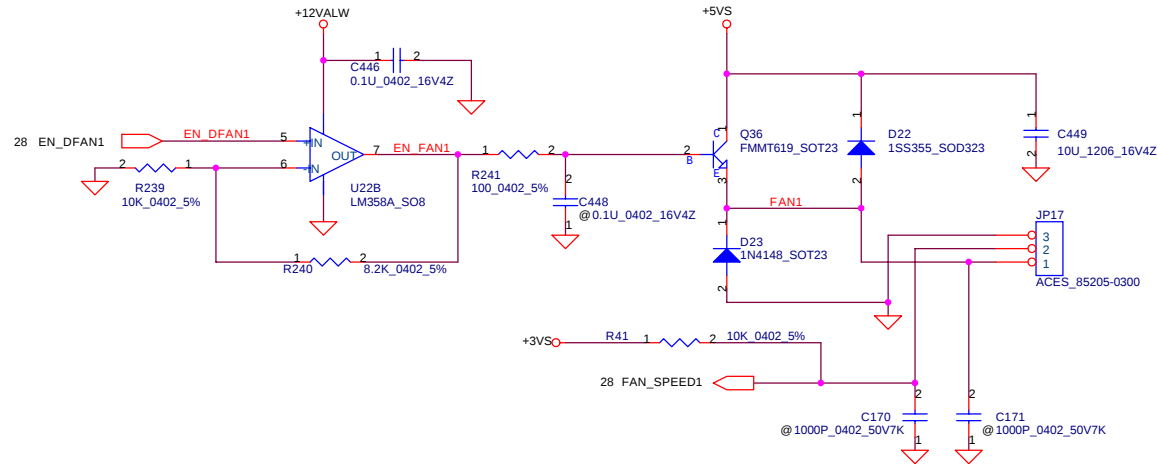


INT_KBD CONN.

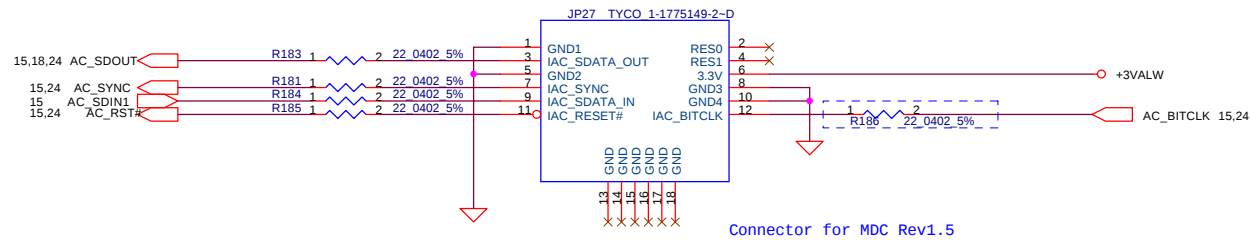


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Custom		HAZ00/BL10E (LA2861)		1.0	
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FAN Conn



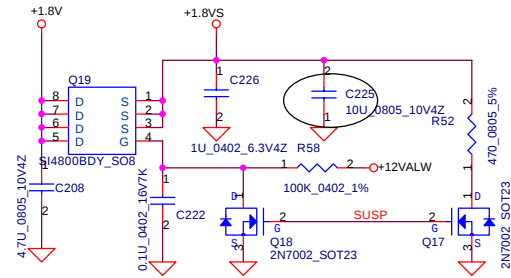
MDC CONN.



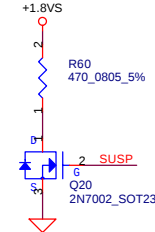
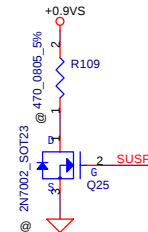
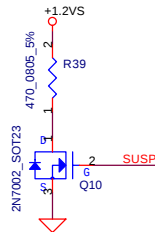
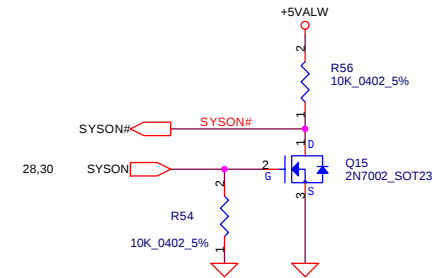
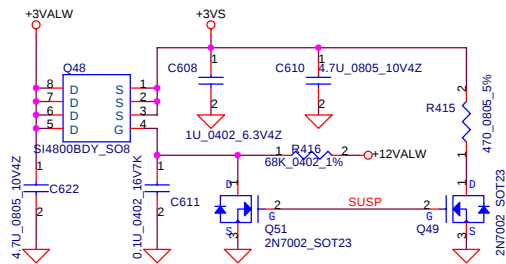
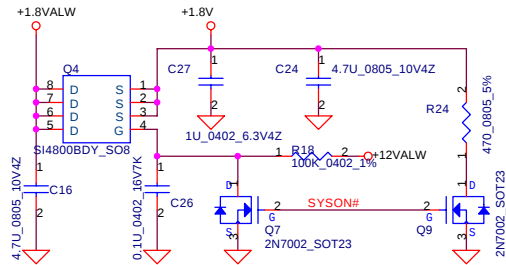
Connector for MDC Rev1.5

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8VALW T0 +1.8V

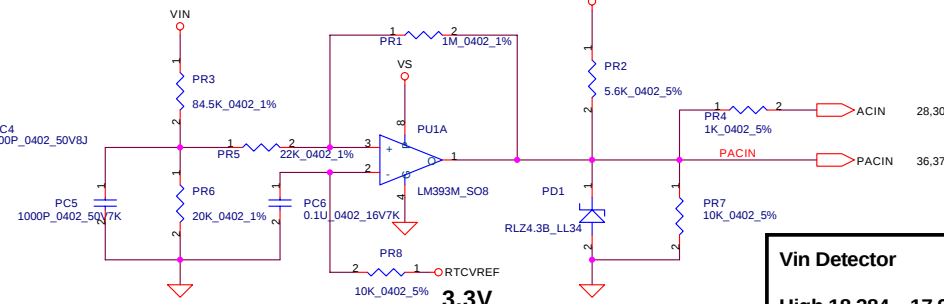
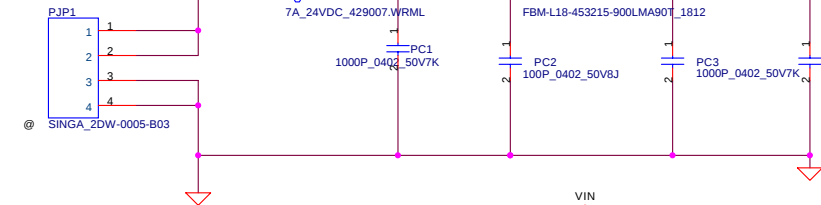


+1.8VALW TO +1.8V

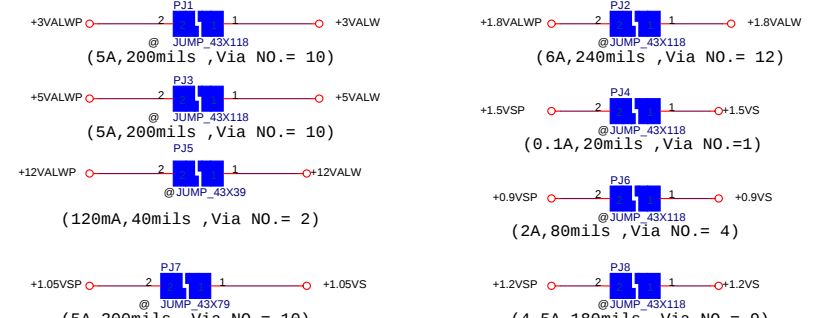
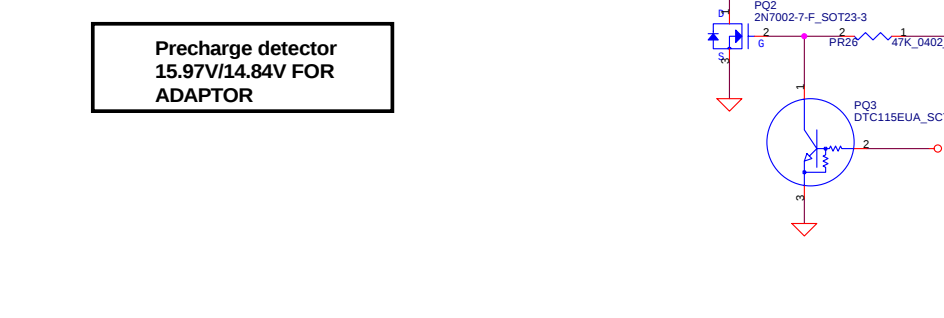
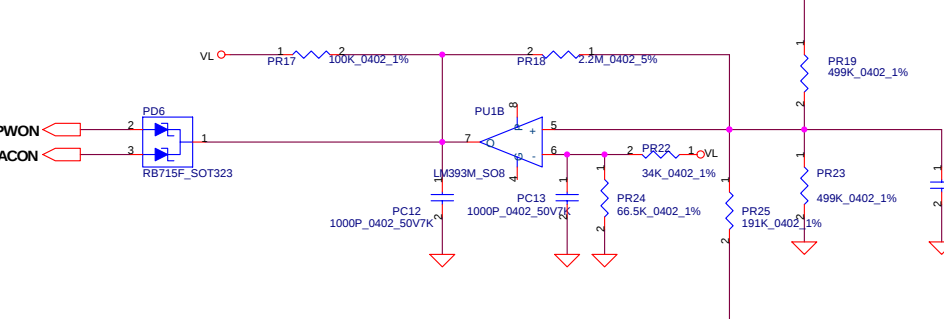
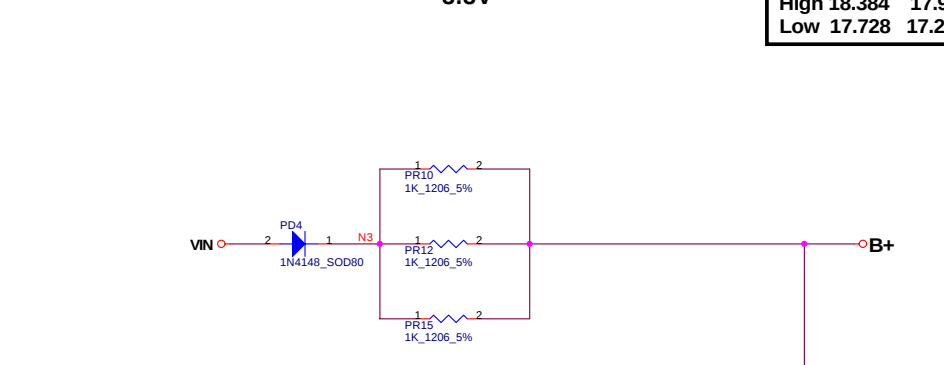
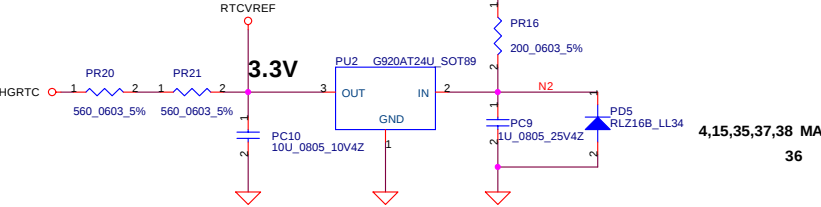
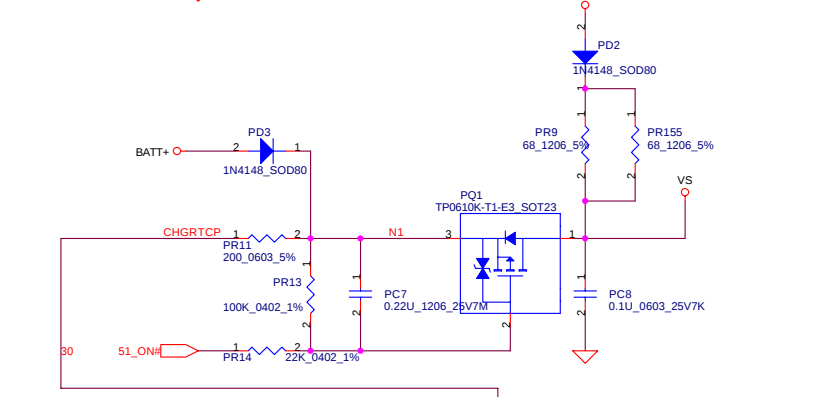


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				DC-DC INTERFACE			
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DC301000F00



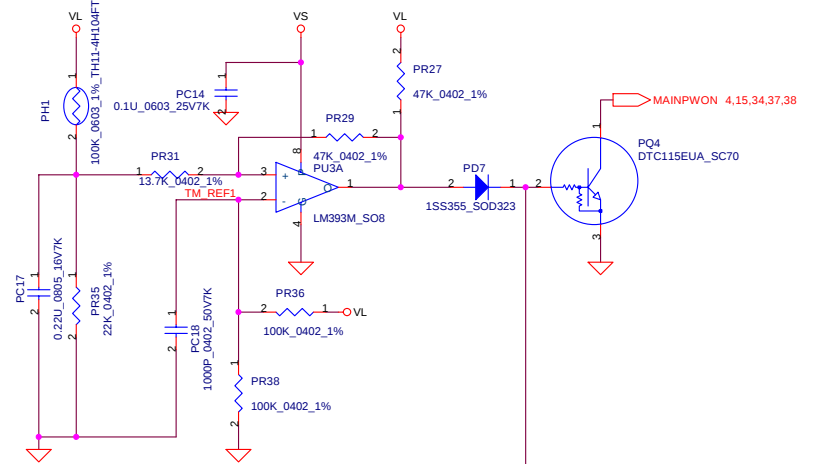
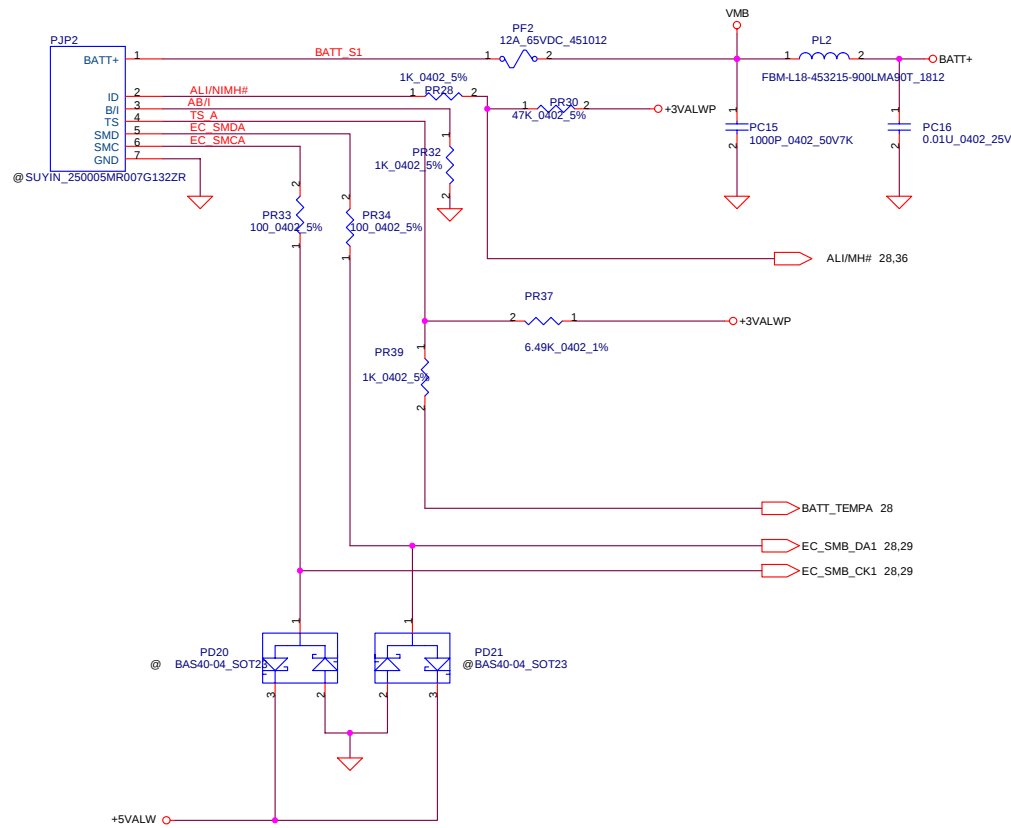
Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



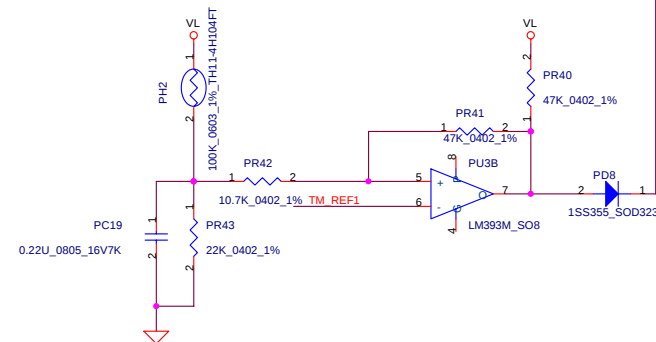
**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

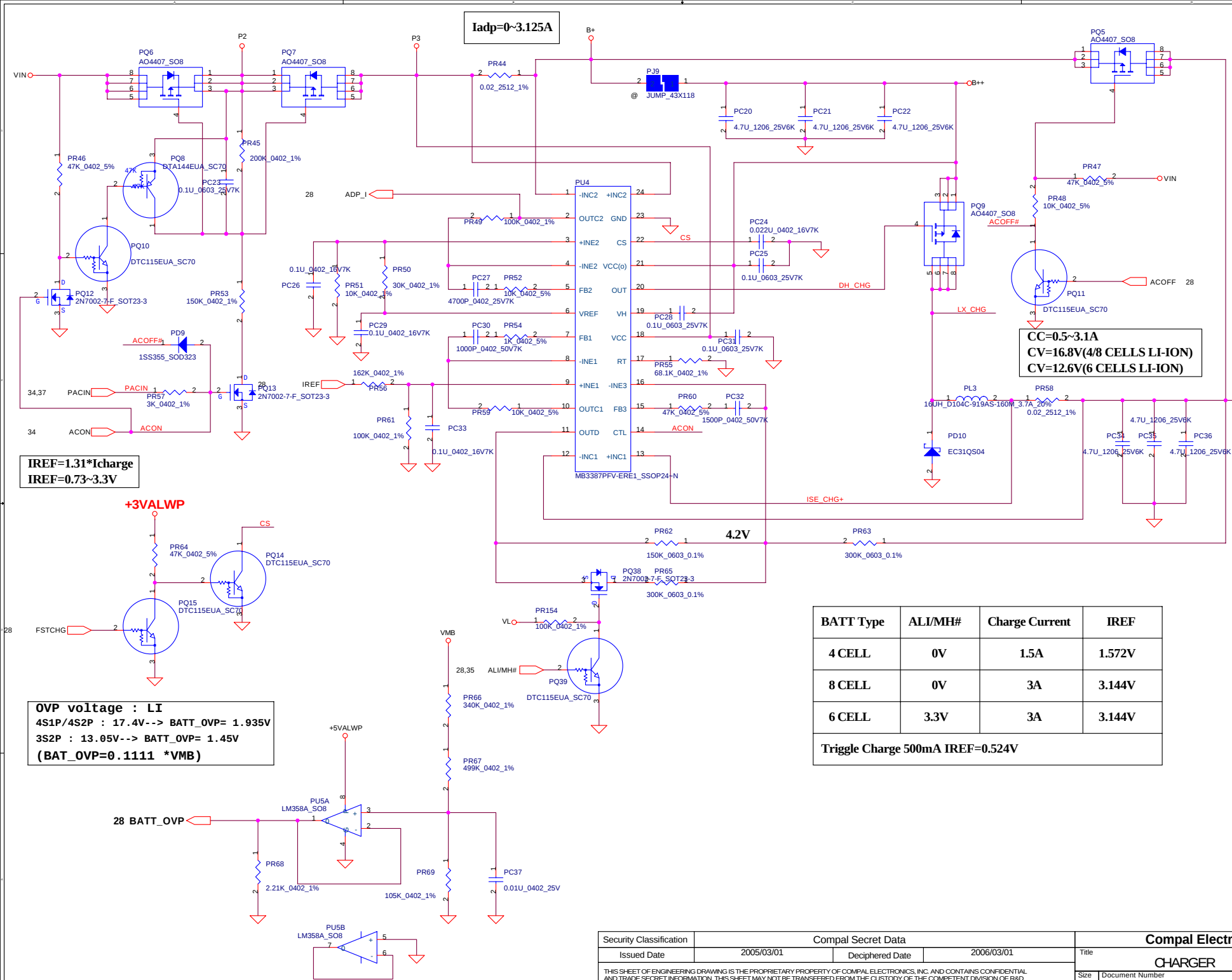
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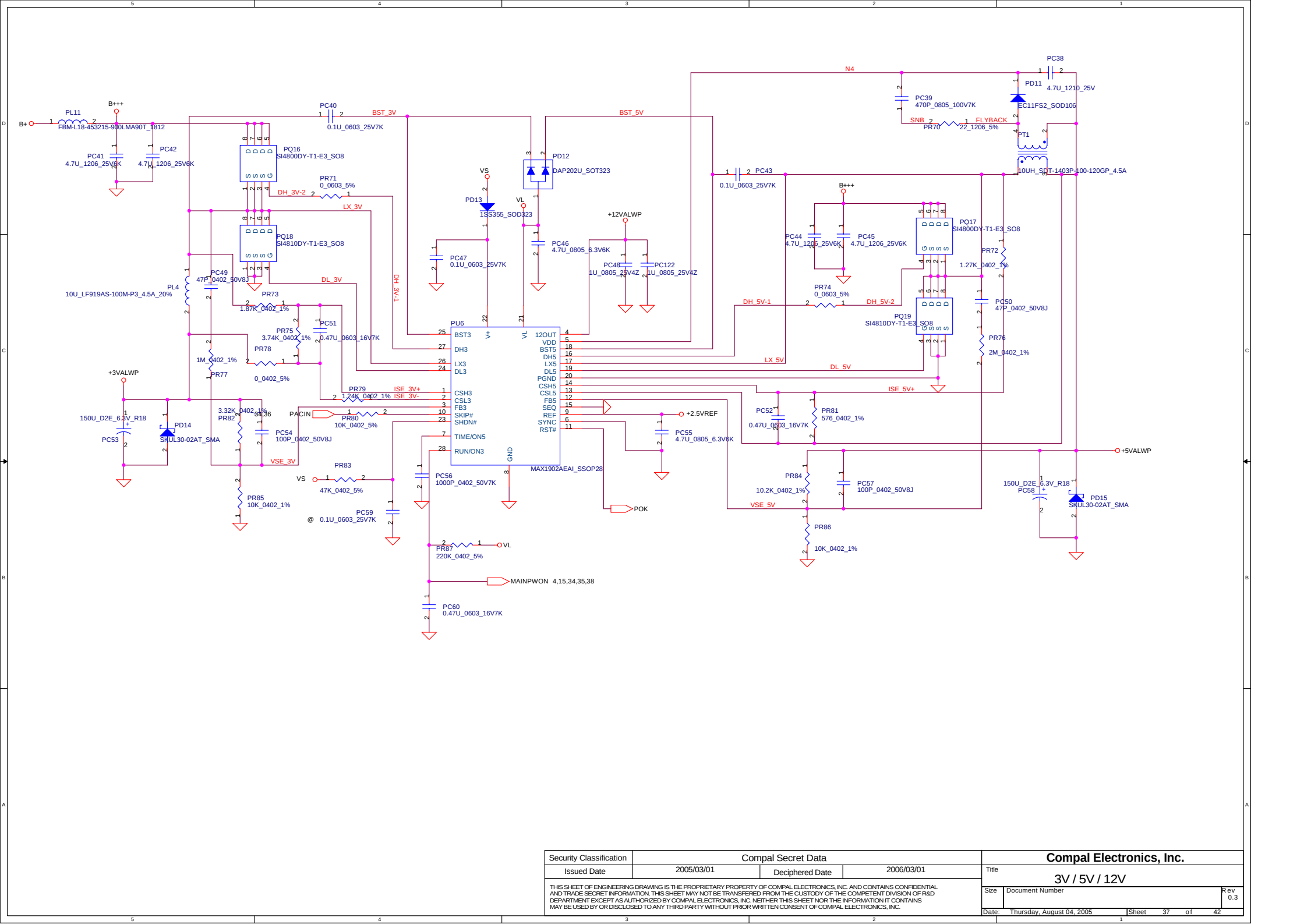
PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

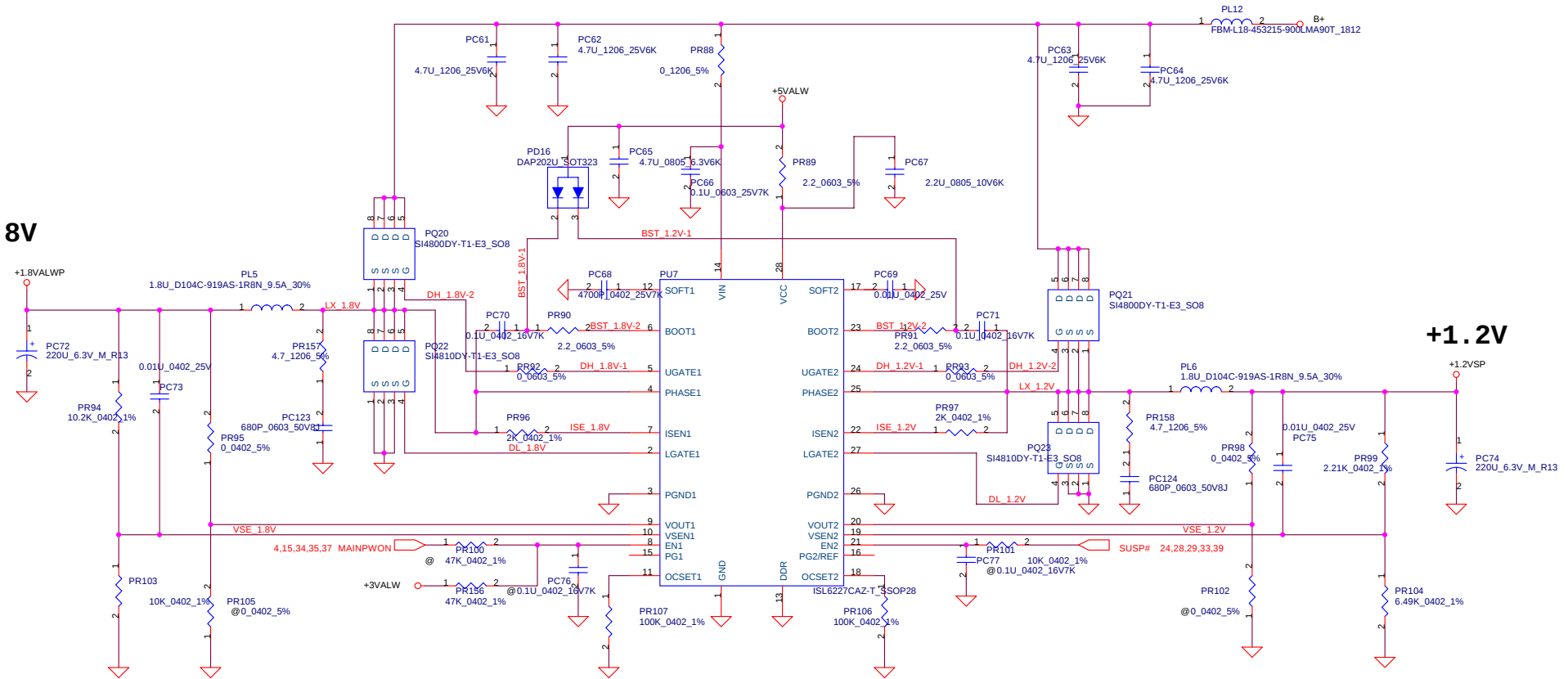




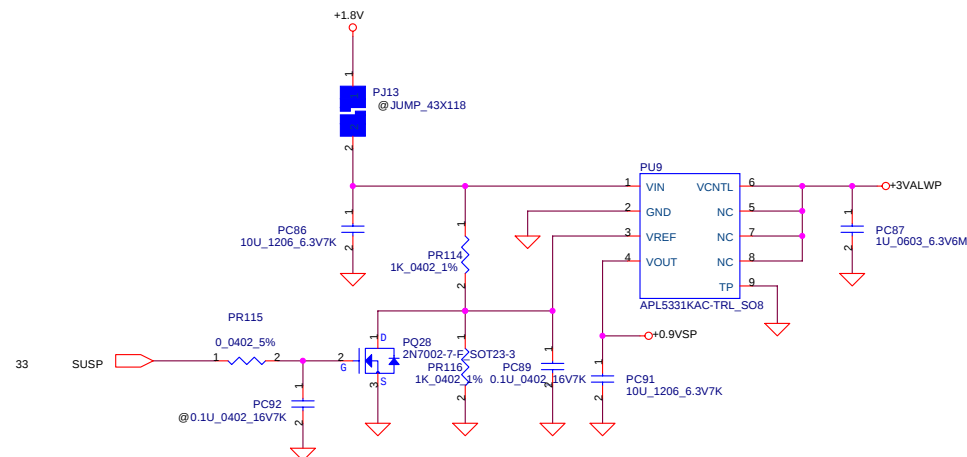
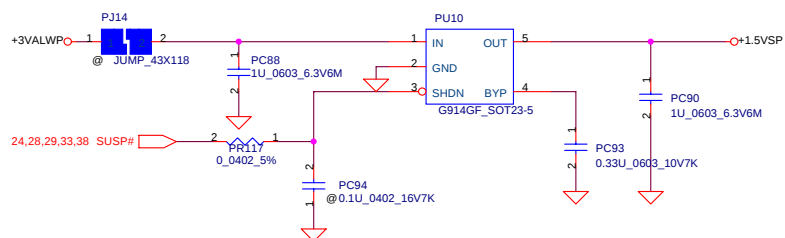
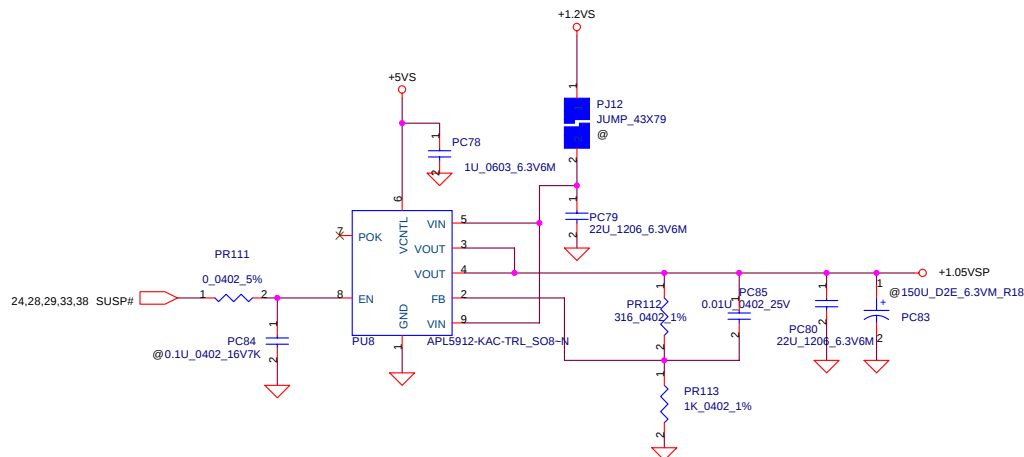


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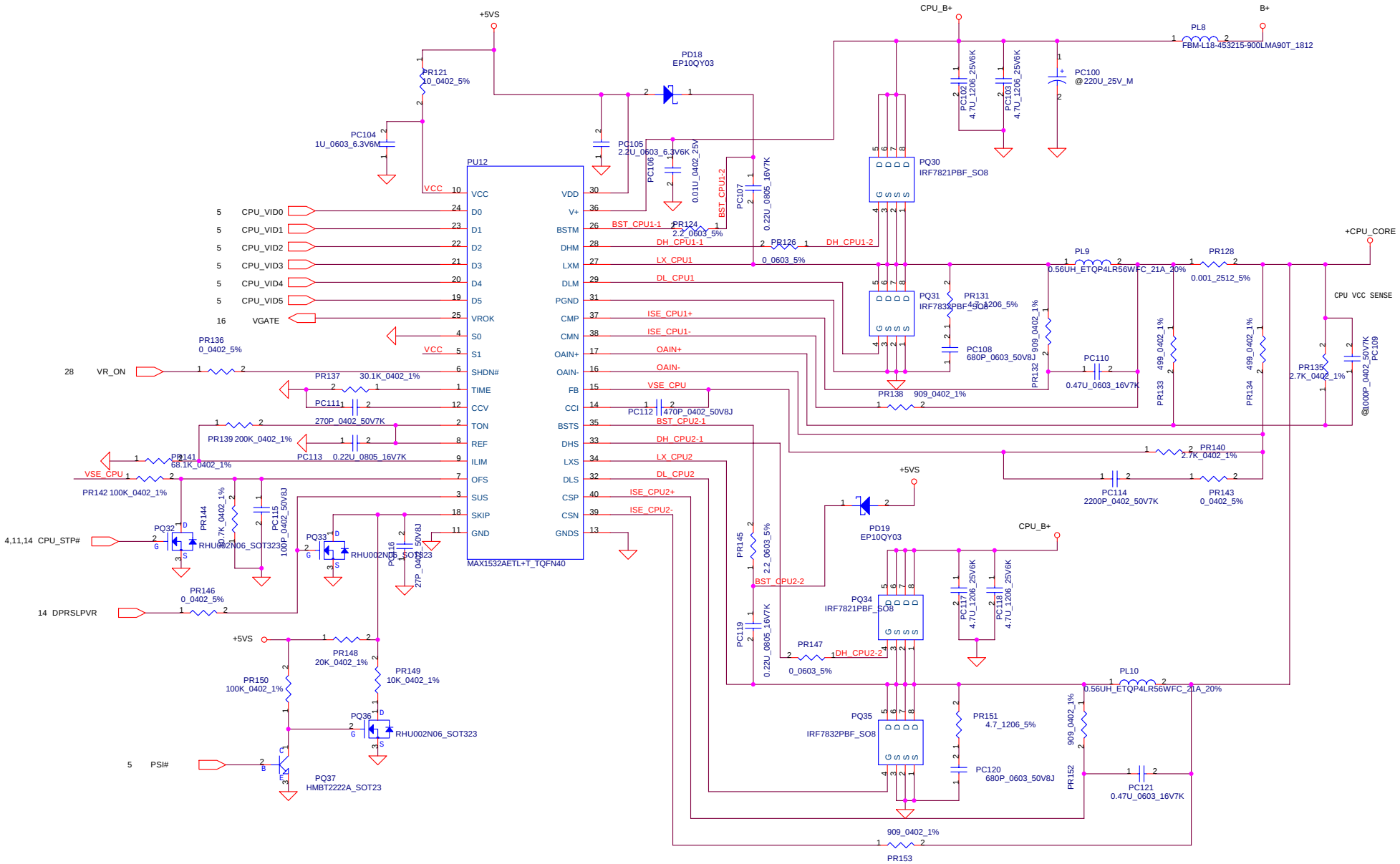
+1.8V



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				Size	Document Number		Rev
							0.3
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0.1==>0.2		Written by Timo	
Date	Page	Action	Purpose
6/12	9	Add C642, C643 and C644	For Increase the DDR bypass capaciotrs
6/12	10	Add C645, C646 and C647	For Increase the DDR bypass capaciotrs
	12	Modify JP18 circuit	Making TV out function become correct
	15	Add @ on R317	Metting ATI reference circuit
	24	Del @ on R436	Solving MDC issue and sound slow issue
	26	Del R306 (move to sub board)	To differentiate between HAZ00 and HTW01 BIOS
	28	Add @ on Super I/O circuit	For DVT build
	29	Modify pin74 net-name of KB910	Solving reserve button no function
	31	Modify D16, D17	
		Add D35, D36	Change from double colors to signal color LED
6/22	27	Add H34, H33	For Me update new drawing

0.2==>0.3		Written by Timo	
7/8	8	Add C648, C649 and C650	Seperate the AVDD and DVDD for TVout and CRT
	17	Add C651~C657	
		Change C585, C587, C566, C533, C560, C573, C536 from 10 to 4.7U	For height limited of SB
	34	Change C225 from 4.7 to 10U	For height limited of SB
7/11	25	Del R456	
		Add Q52	For insert card bus device beep sound issue.
	27	Del R449~R454	For EMI request
7/13		Del Super I/O circuit	
	29	Add JP30, R457, C658	For LPC debug port
	23	ADD JP29, R456	For Port80 Debug card connector
	28	ADD R459, R460	For HDD password detect pin
	12	ADD J1, J4	
	22	ADD J2	
	27	ADD J3	For EMI request

0.3==>1.0		Written by Timo	
7/28	25	Add C662, R461, D37, R462, Q52	For Insert card bus device PoPo noise sound
	29	Change R101 from 8.2k to 18kohm	For Board ID change
	14	Change C587, C585, C651, C652, C566, C553, C560, C573, C653, C654, C655, C656, C536, C657	
	17	from 4.7U to 1U	For avoide the interfere area of HDD
		Change C288 from 150U fo 470UF	Making the capacitors of 1.8VS source blance of SB
		Add C660, C661	Making the capacitors of 1.8VALW and 3VS sources blance of SB
7/30	4	Add @ in C261	For throttle issue
	5	Add @ in C180	For cost down
	12	Add L38, L39, L40	For EMI issue

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