

NDU00/NDU10

Streamline-S 11.6"

Streamline-M 13.3"

LA-6031P REV 1.0 Schematic

Intel Arrandale SFF/IBEX PEAK

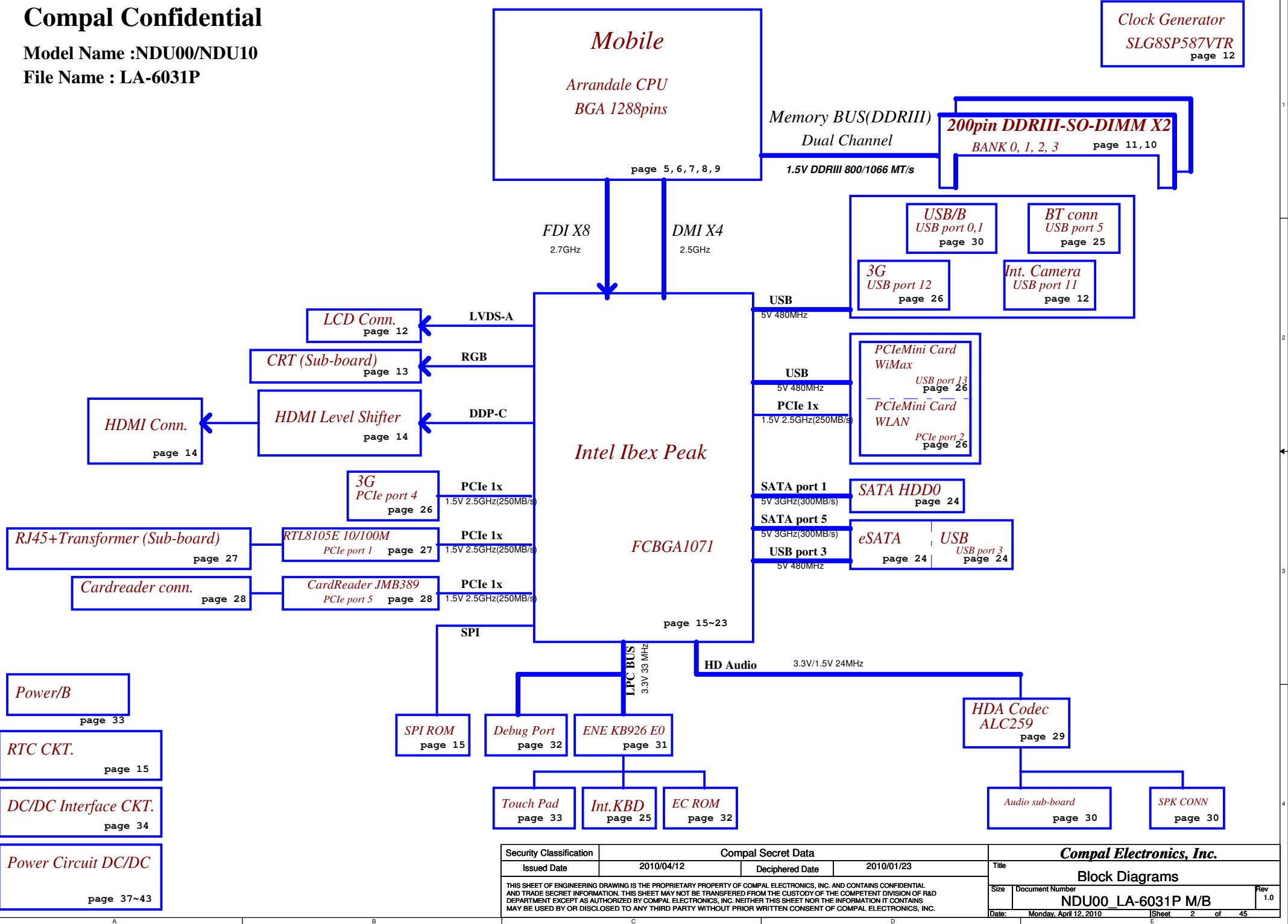
2010-04-12 Rev 1.0

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		2010/01/23		Title	
				Cover Page	
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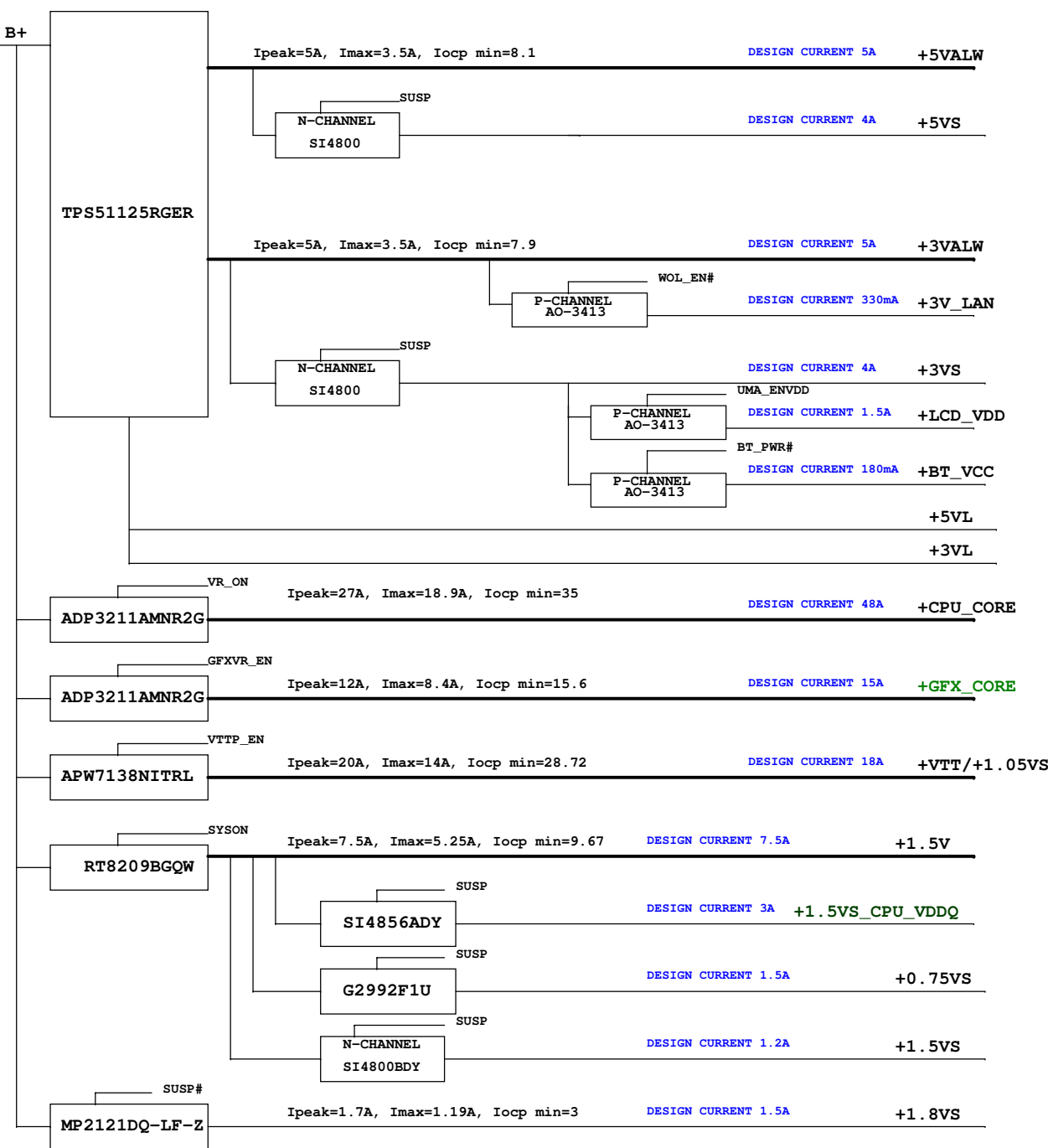
Model Name :NDU00/NDU10

File Name : LA-6031P



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NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	main	2nd
						R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

EC SM Bus2 address

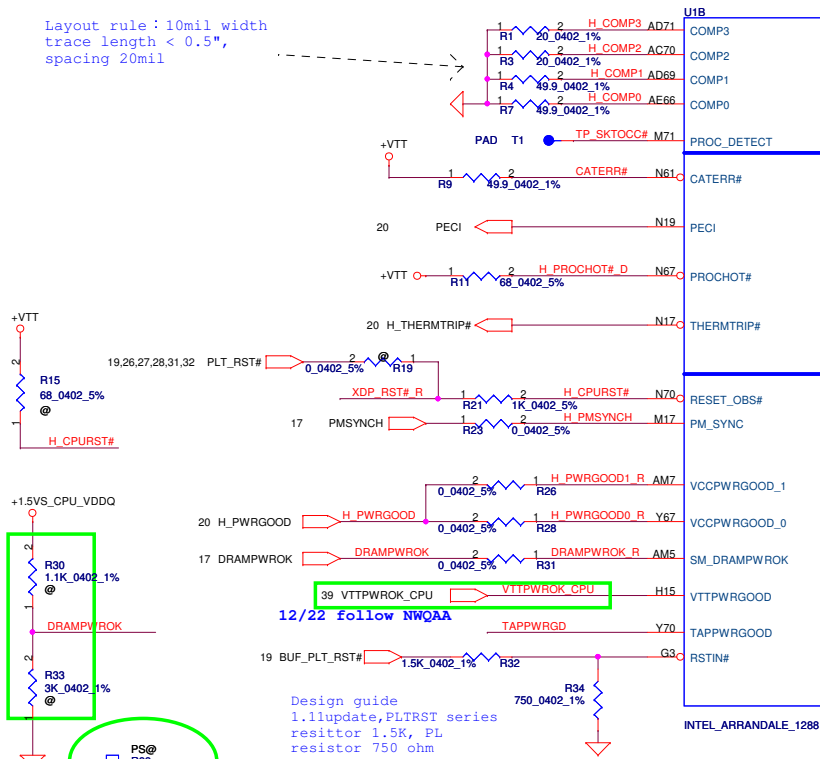
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011x b	+3VS	Gensor	
			+3VS	PCH	0100 110x b

PCH SM Bus address

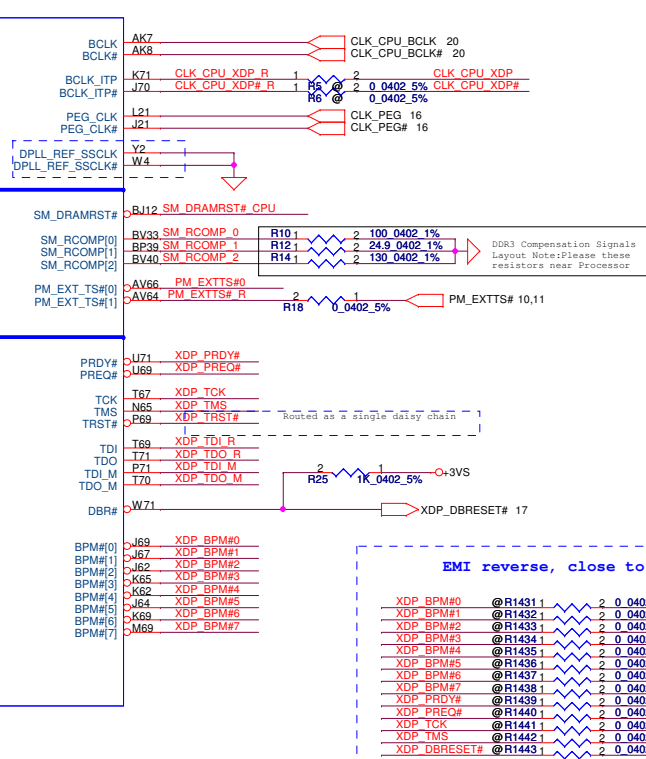
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

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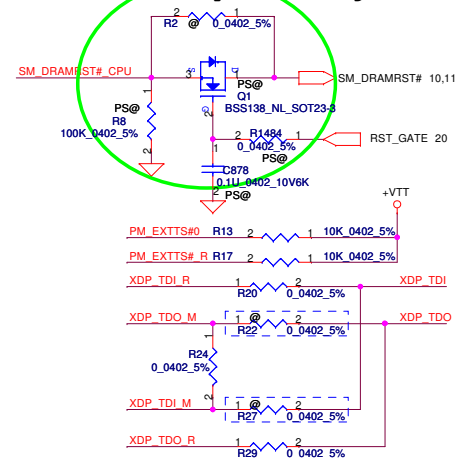
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trace length < 0.5",
spacing 20mil



Clocks
Thermal
Power Management
JTAG & MBP



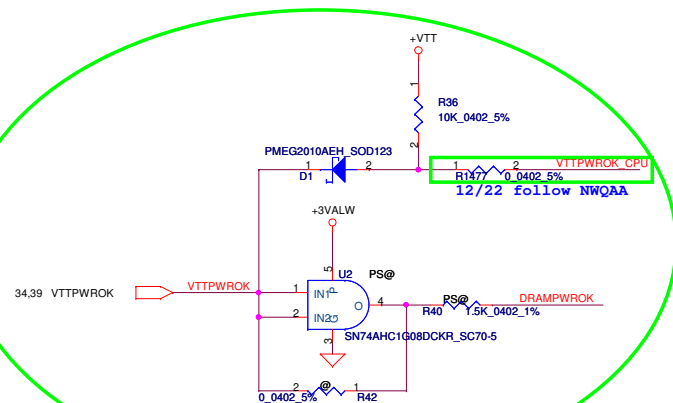
For S3 CPU power saving



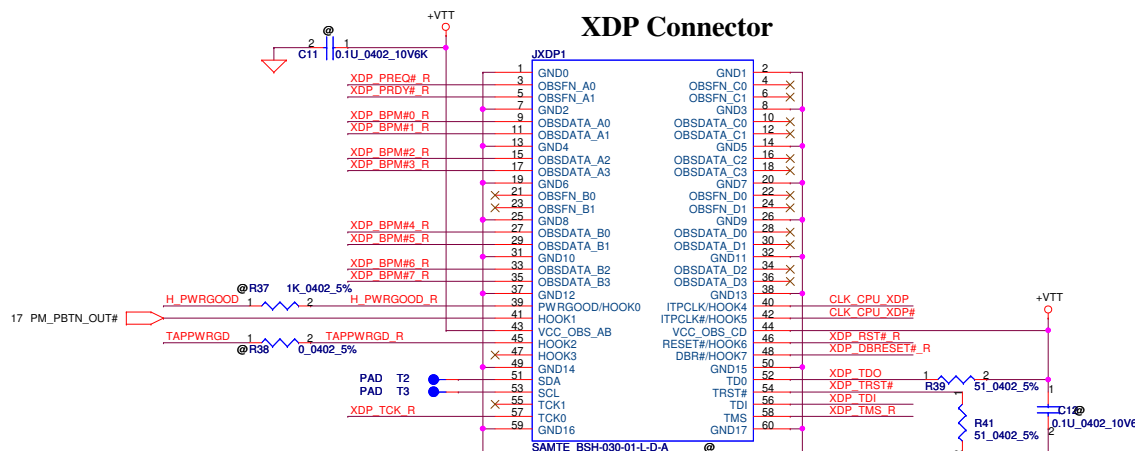
JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

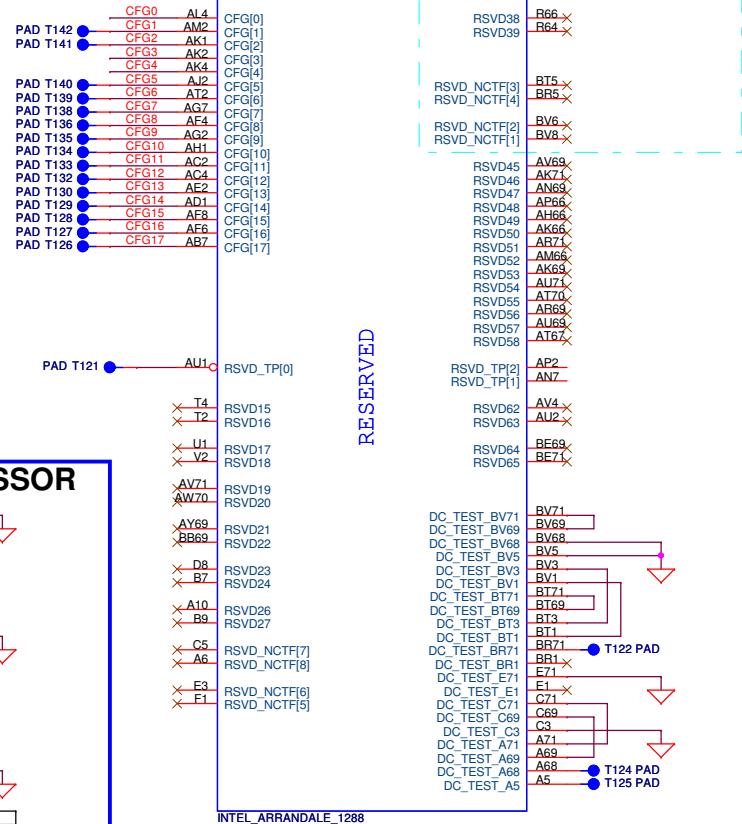
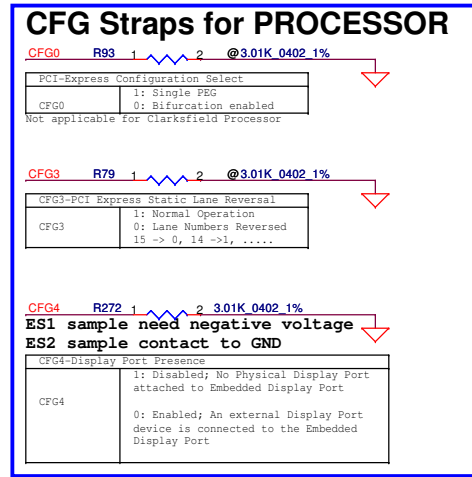
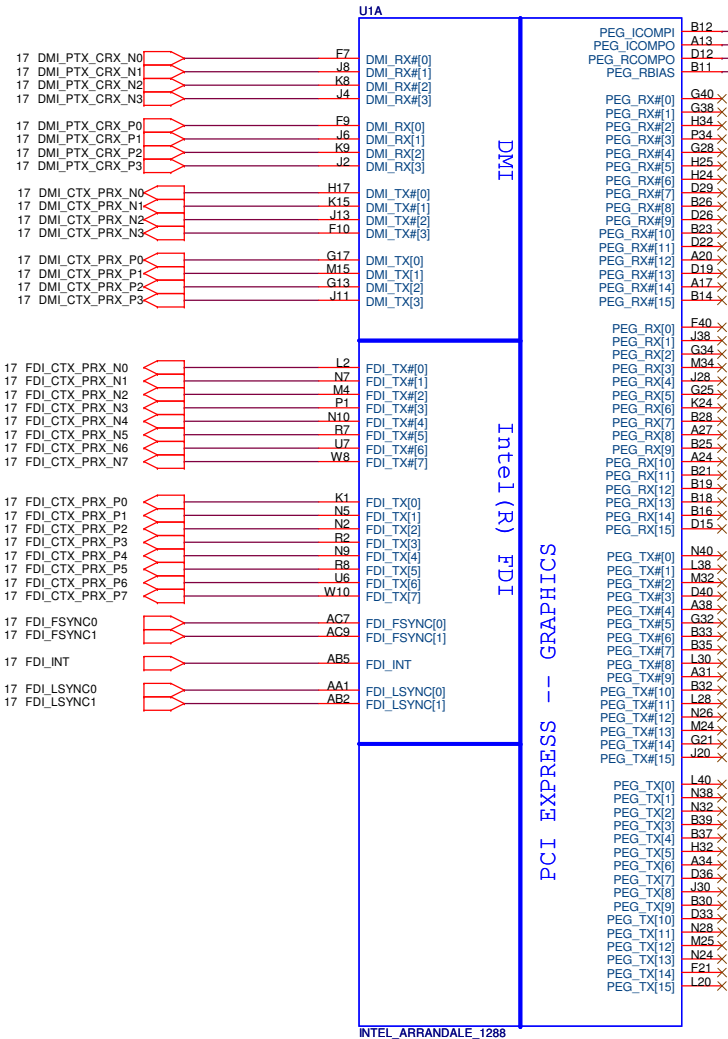
For S3 CPU power saving



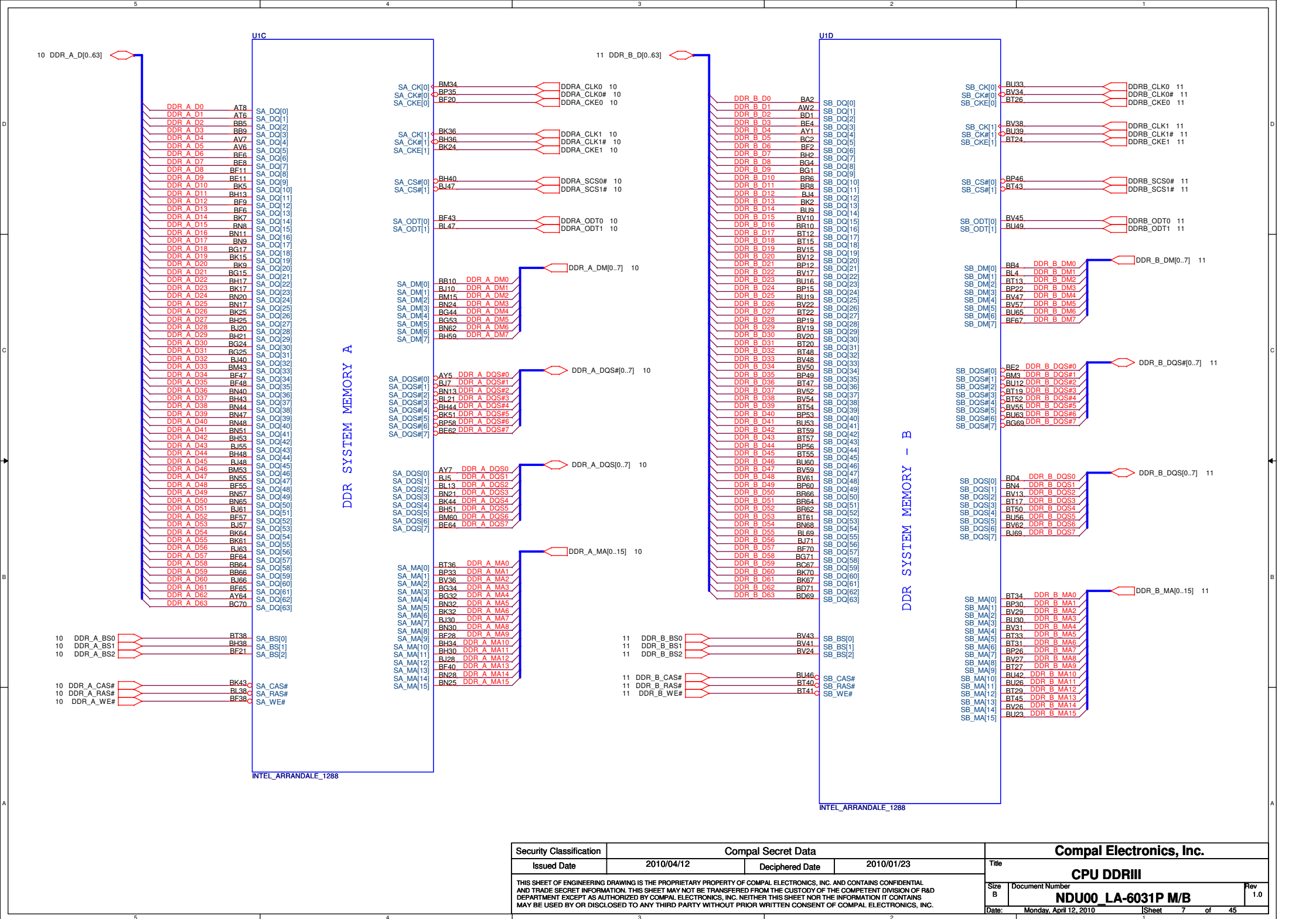
XDP Connector

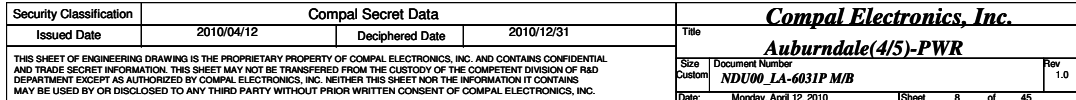


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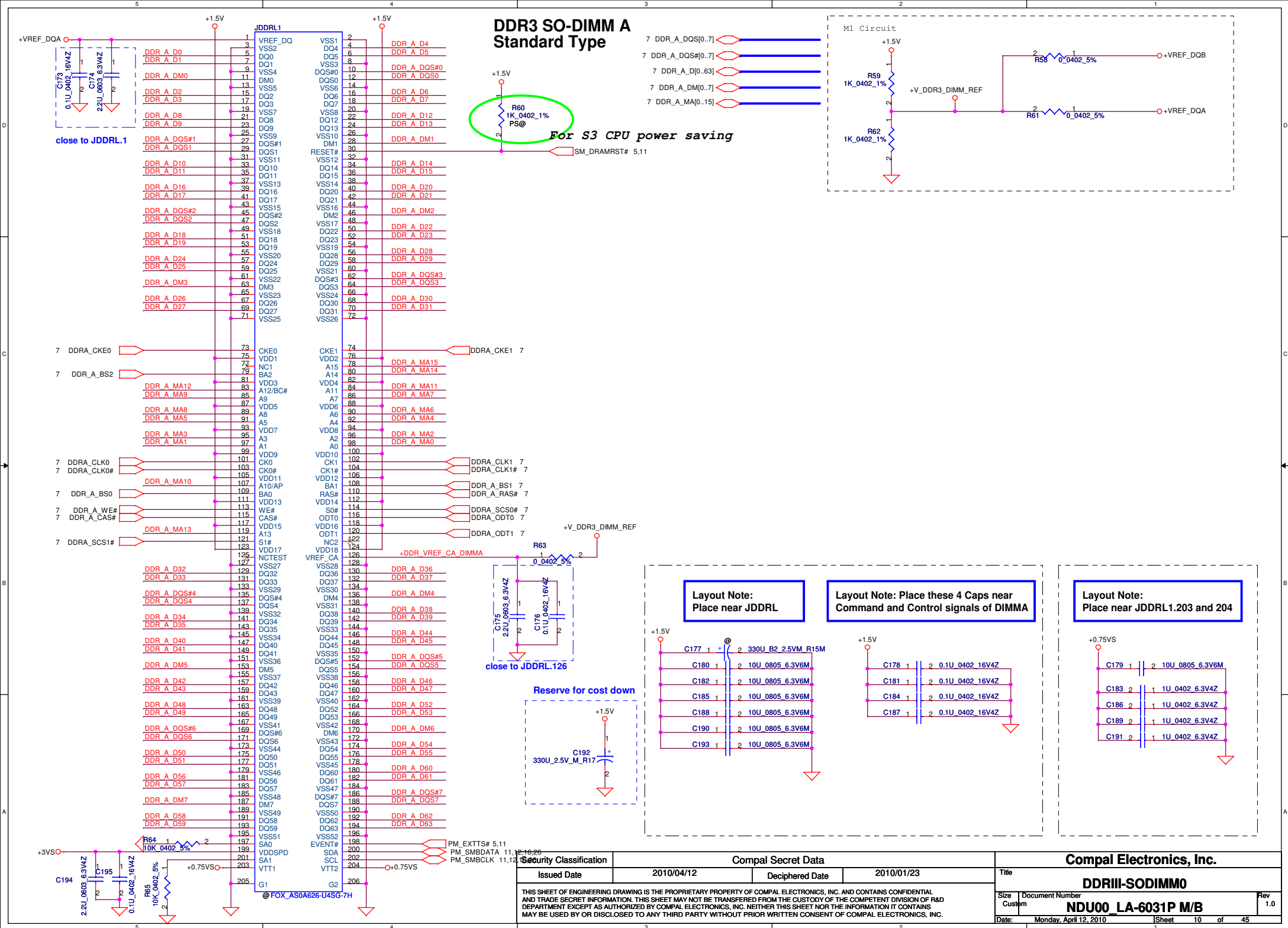


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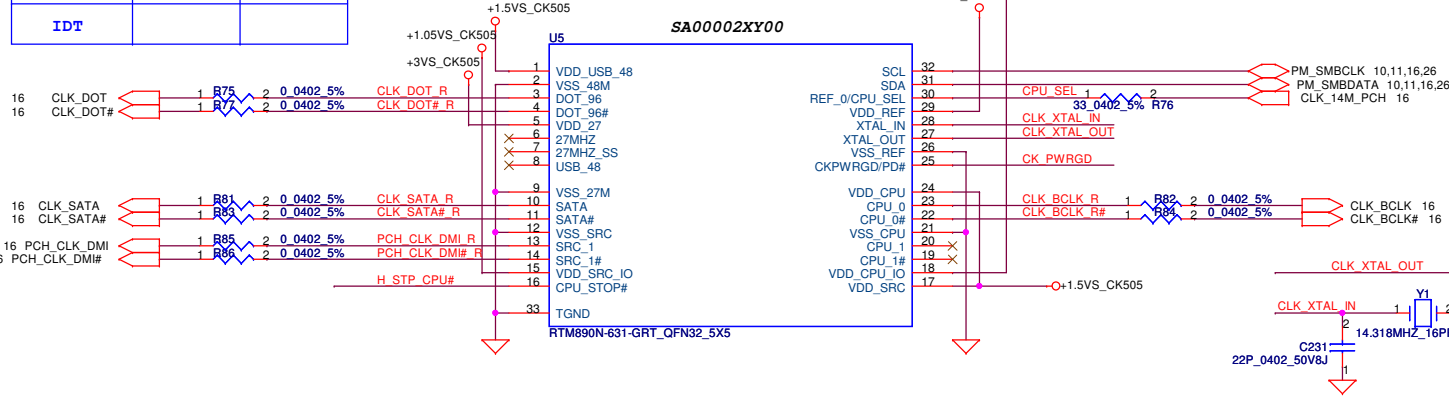
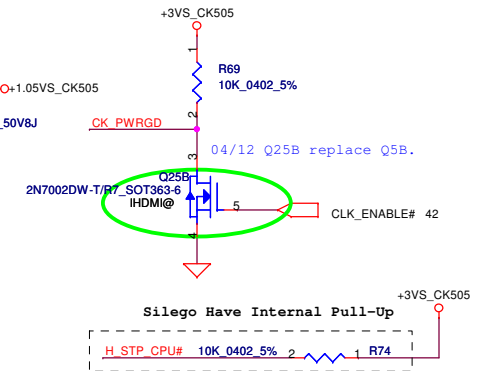
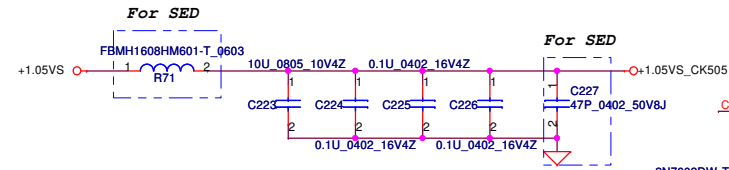
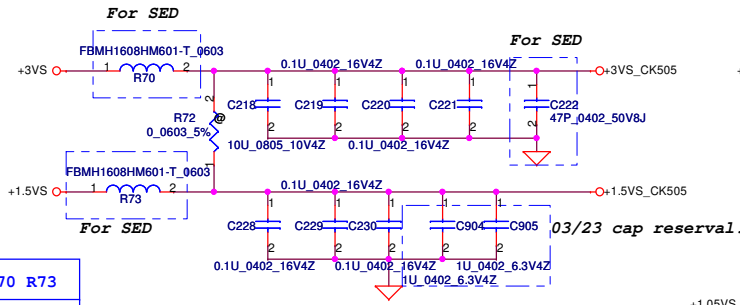


U11		AY24		U1J		
BU62	VSS1	VSS90		AH33	VSS202	VSS404
BU68	VSS2	VSS91	AY23	AH31	VSS203	VSS405
BU69	VSS3	VSS92	AY21	AH32	VSS204	VSS406
BU70	VSS4	VSS93		AH33	VSS205	VSS407
BU71	VSS5	VSS94		AH34	VSS206	VSS408
BU72	VSS6	VSS95		AH35	VSS207	VSS409
BU73	VSS7	VSS96		AH36	VSS208	VSS410
BU74	VSS8	VSS97		AH37	VSS209	VSS411
BU75	VSS9	VSS98		AH38	VSS210	VSS412
BU76	VSS10	VSS99		AH39	VSS211	VSS413
BU77	VSS11	VSS100	AW57	AH40	VSS212	VSS414
BU78	VSS12	VSS101	AW58	AH41	VSS213	VSS415
BU79	VSS13	VSS102	AW59	AH42	VSS214	VSS416
BU80	VSS14	VSS103	AW60	AH43	VSS215	VSS417
BU81	VSS15	VSS104	AW61	AH44	VSS216	VSS418
BU82	VSS16	VSS105	AW62	AH45	VSS217	VSS419
BU83	VSS17	VSS106	AW63	AH46	VSS218	VSS420
BU84	VSS18	VSS107	AW64	AH47	VSS219	VSS421
BU85	VSS19	VSS108	AW65	AH48	VSS220	VSS422
BU86	VSS20	VSS109	AW66	AH49	VSS221	VSS423
BU87	VSS21	VSS110	AW67	AH50	VSS222	VSS424
BU88	VSS22	VSS111	AW68	AH51	VSS223	VSS425
BU89	VSS23	VSS112	AW69	AH52	VSS224	VSS426
BU90	VSS24	VSS113	AW70	AH53	VSS225	VSS427
BU91	VSS25	VSS114	AW71	AH54	VSS226	VSS428
BU92	VSS26	VSS115	AW72	AH55	VSS227	VSS429
BU93	VSS27	VSS116	AW73	AH56	VSS228	VSS430
BU94	VSS28	VSS117	AW74	AH57	VSS229	VSS431
BU95	VSS29	VSS118	AW75	AH58	VSS230	VSS432
BU96	VSS30	VSS119	AW76	AH59	VSS231	VSS433
BU97	VSS31	VSS120	AW77	AH60	VSS232	VSS434
BU98	VSS32	VSS121	AW78	AH61	VSS233	VSS435
BU99	VSS33	VSS122	AW79	AH62	VSS234	VSS436
BU100	VSS34	VSS123	AW80	AH63	VSS235	VSS437
BU101	VSS35	VSS124	AW81	AH64	VSS236	VSS438
BU102	VSS36	VSS125	AW82	AH65	VSS237	VSS439
BU103	VSS37	VSS126	AW83	AH66	VSS238	VSS440
BU104	VSS38	VSS127	AW84	AH67	VSS239	VSS441
BU105	VSS39	VSS128	AW85	AH68	VSS240	VSS442
BU106	VSS40	VSS129	AW86	AH69	VSS241	VSS443
BU107	VSS41	VSS130	AW87	AH70	VSS242	VSS444
BU108	VSS42	VSS131	AW88	AH71	VSS243	VSS445
BU109	VSS43	VSS132	AW89	AH72	VSS244	VSS446
BU110	VSS44	VSS133	AW90	AH73	VSS245	VSS447
BU111	VSS45	VSS134	AW91	AH74	VSS246	VSS448
BU112	VSS46	VSS135	AW92	AH75	VSS247	VSS449
BU113	VSS47	VSS136	AW93	AH76	VSS248	VSS450
BU114	VSS48	VSS137	AW94	AH77	VSS249	VSS451
BU115	VSS49	VSS138	AW95	AH78	VSS250	VSS452
BU116	VSS50	VSS139	AW96	AH79	VSS251	VSS453
BU117	VSS51	VSS140	AW97	AH80	VSS252	VSS454
BU118	VSS52	VSS141	AW98	AH81	VSS253	VSS455
BU119	VSS53	VSS142	AW99	AH82	VSS254	VSS456
BU120	VSS54	VSS143	AW100	AH83	VSS255	VSS457
BU121	VSS55	VSS144	AW101	AH84	VSS256	VSS458
BU122	VSS56	VSS145	AW102	AH85	VSS257	VSS459
BU123	VSS57	VSS146	AW103	AH86	VSS258	VSS460
BU124	VSS58	VSS147	AW104	AH87	VSS259	VSS461
BU125	VSS59	VSS148	AW105	AH88	VSS260	VSS462
BU126	VSS60	VSS149	AW106	AH89	VSS261	VSS463
BU127	VSS61	VSS150	AW107	AH90	VSS262	VSS464
BU128	VSS62	VSS151	AW108	AH91	VSS263	VSS465
BU129	VSS63	VSS152	AW109	AH92	VSS264	VSS466
BU130	VSS64	VSS153	AW110	AH93	VSS265	VSS467
BU131	VSS65	VSS154	AW111	AH94	VSS266	VSS468
BU132	VSS66	VSS155	AW112	AH95	VSS267	VSS469
BU133	VSS67	VSS156	AW113	AH96	VSS268	VSS470
BU134	VSS68	VSS157	AW114	AH97	VSS269	VSS471
BU135	VSS69	VSS158	AW115	AH98	VSS270	VSS472
BU136	VSS70	VSS159	AW116	AH99	VSS271	VSS473
BU137	VSS71	VSS160	AW117	AH100	VSS272	VSS474
BU138	VSS72	VSS161	AW118	AH101	VSS273	VSS475
BU139	VSS73	VSS162	AW119	AH102	VSS274	VSS476
BU140	VSS74	VSS163	AW120	AH103	VSS275	VSS477
BU141	VSS75	VSS164	AW121	AH104	VSS276	VSS478
BU142	VSS76	VSS165	AW122	AH105	VSS277	VSS479
BU143	VSS77	VSS166	AW123	AH106	VSS278	VSS480
BU144	VSS78	VSS167	AW124	AH107	VSS279	VSS481
BU145	VSS79	VSS168	AW125	AH108	VSS280	VSS482
BU146	VSS80	VSS169	AW126	AH109	VSS281	VSS483
BU147	VSS81	VSS170	AW127	AH110	VSS282	VSS484
BU148	VSS82	VSS171	AW128	AH111	VSS283	VSS485
BU149	VSS83	VSS172	AW129	AH112	VSS284	VSS486
BU150	VSS84	VSS173	AW130	AH113	VSS285	VSS487
BU151	VSS85	VSS174	AW131	AH114	VSS286	VSS488
BU152	VSS86	VSS175	AW132	AH115	VSS287	VSS489
BU153	VSS87	VSS176	AW133	AH116	VSS288	VSS490
BU154	VSS88	VSS177	AW134	AH117	VSS289	VSS491
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BU156	VSS90	VSS179	AW136	AH119	VSS291	VSS493
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BU158	VSS92	VSS181	AW138	AH121	VSS293	VSS495
BU159	VSS93	VSS182	AW139	AH122	VSS294	VSS496
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BU162	VSS96	VSS185	AW142	AH125	VSS297	VSS499
BU163	VSS97	VSS186	AW143	AH126	VSS298	VSS500
BU164	VSS98	VSS187	AW144	AH127	VSS299	VSS501
BU165	VSS99	VSS188	AW145	AH128	VSS300	VSS502
BU166	VSS100	VSS189	AW146	AH129	VSS301	VSS503
BU167	VSS101	VSS190	AW147	AH130	VSS302	VSS504
BU168	VSS102	VSS191	AW148	AH131	VSS303	VSS505
BU169	VSS103	VSS192	AW149	AH132	VSS304	VSS506
BU170	VSS104	VSS193	AW150	AH133	VSS305	VSS507
BU171	VSS105	VSS194	AW151	AH134	VSS306	VSS508
BU172	VSS106	VSS195	AW152	AH135	VSS307	VSS509
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BU180	VSS114	VSS203	AW160	AH143	VSS315	VSS517
BU181	VSS115	VSS204	AW161	AH144	VSS316	VSS518
BU182	VSS116	VSS205	AW162	AH145	VSS317	VSS519
BU183	VSS117	VSS206	AW163	AH146	VSS318	VSS520
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BU185	VSS119	VSS208	AW165	AH148	VSS320	VSS522
BU186	VSS120	VSS209	AW166	AH149	VSS321	VSS523
BU187	VSS121	VSS210	AW167	AH150	VSS322	VSS524
BU188	VSS122	VSS211	AW168	AH151	VSS323	VSS525
BU189	VSS123	VSS212	AW169	AH152	VSS324	VSS526
BU190	VSS124	VSS213	AW170	AH153	VSS325	VSS527
BU191	VSS125	VSS214	AW171	AH154	VSS326	VSS528
BU192	VSS126	VSS215	AW172	AH155	VSS327	VSS529
BU193	VSS127	VSS216	AW173	AH156	VSS328	VSS530
BU194	VSS128	VSS217	AW174	AH157	VSS329	VSS531
BU195	VSS129	VSS218	AW175	AH158	VSS330	VSS532
BU196	VSS130	VSS219	AW176	AH159	VSS331	VSS533
BU197	VSS131	VSS220	AW177	AH160	VSS332	VSS534
BU198	VSS132	VSS221	AW178	AH161	VSS333	VSS535
BU199	VSS133	VSS222	AW179	AH162	VSS334	VSS536
BU200	VSS134	VSS223	AW180	AH163	VSS335	VSS537
BU201	VSS135	VSS224	AW181	AH164	VSS336	VSS538
BU202	VSS136	VSS225	AW182	AH165	VSS337	VSS539
BU203	VSS137	VSS226	AW183	AH166	VSS338	VSS540
BU204	VSS138	VSS227	AW184	AH167	VSS339	VSS541
BU205	VSS139	VSS228	AW185	AH168	VSS340	VSS542
BU206	VSS140	VSS229	AW186	AH169	VSS341	VSS543
BU207	VSS141	VSS230	AW187	AH170	VSS342	VSS544
BU208	VSS142	VSS231	AW188	AH171	VSS343	VSS545
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BU211	VSS145	VSS234	AW191	AH174	VSS346	VSS548
BU212	VSS146	VSS235	AW192	AH175	VSS347	VSS549
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BU225	VSS159	VSS248	AW205	AH188	VSS360	VSS562
BU226	VSS160	VSS249	AW206	AH189	VSS361	VSS563
BU227	VSS161	VSS250	AW207	AH190	VSS362	VSS564
BU228	VSS162	VSS251	AW208	AH191	VSS363	VSS565
BU229	VSS163	VSS252	AW209	AH192	VSS364	VSS566
BU230	VSS164	VSS253	AW210	AH193	VSS365	VSS567
BU231	VSS165	VSS254	AW211	AH194	VSS366	VSS568
BU232	VSS166	VSS255	AW212	AH195	VSS367	VSS569
BU233	VSS167	VSS256	AW213	AH196	VSS368	VSS570
BU234	VSS168	VSS257	AW214	AH197	VSS369	VSS571
BU235	VSS169	VSS258	AW215	AH198	VSS370	VSS572
BU236	VSS170	VSS259	AW216	AH199	VSS371	VSS573
BU237	VSS171	VSS260	AW217	AH200	VSS372	VSS574
BU238	VSS172	VSS261	AW218	AH201	VSS373	VSS575
BU239	VSS173	VSS262	AW219	AH202	VSS374	VSS576
BU240	VSS174	VSS263	AW220	AH203	VSS375	VSS577
BU241	VSS175	VSS264	AW221	AH204	VSS376	VSS578
BU242	VSS176	VSS265	AW222	AH205	VSS377	VSS579
BU243	VSS177	VSS266	AW223	AH206	VSS378	VSS580
BU244	VSS178	VSS267	AW224	AH207	VSS379	VSS581
BU245	VSS179	VSS268	AW225	AH208	VSS380	VSS582
BU246	VSS180	VSS269	AW226	AH209	VSS381	VSS583
BU247	VSS181	VSS270	AW227	AH210	VSS382	VSS584
BU248	VSS182	VSS271	AW228	AH211	VSS383	VSS585
BU249	VSS183	VSS272	AW229	AH212	VSS384	VSS586
BU250	VSS184	VSS273	AW230	AH213	VSS385	VSS587
BU251	VSS185	VSS274	AW231	AH214	VSS386	VSS588
BU252	VSS186	VSS275	AW232</			



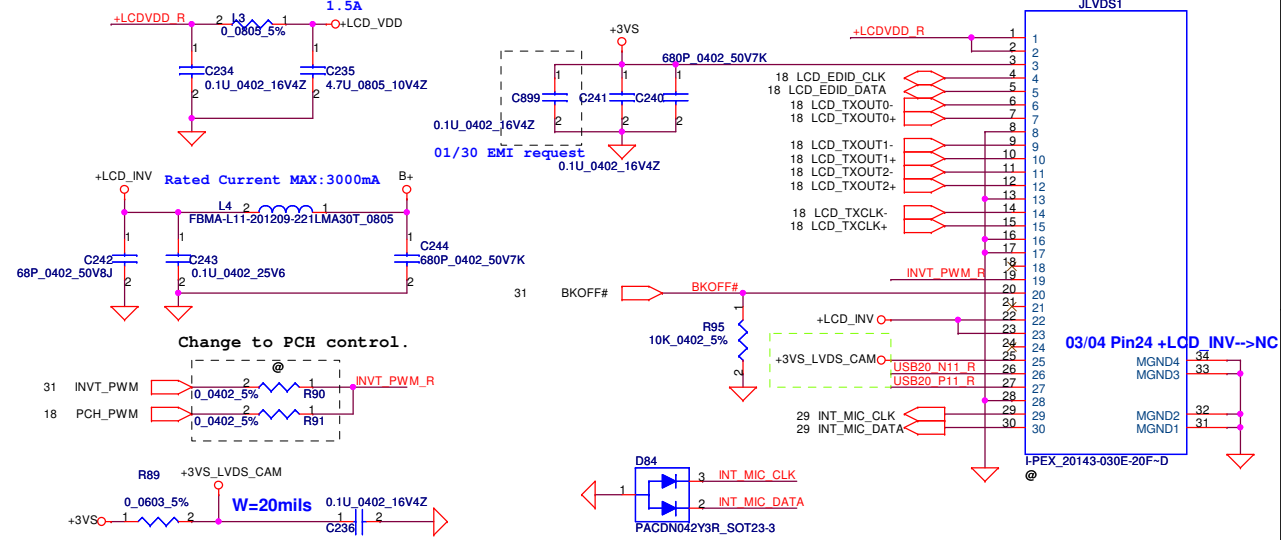
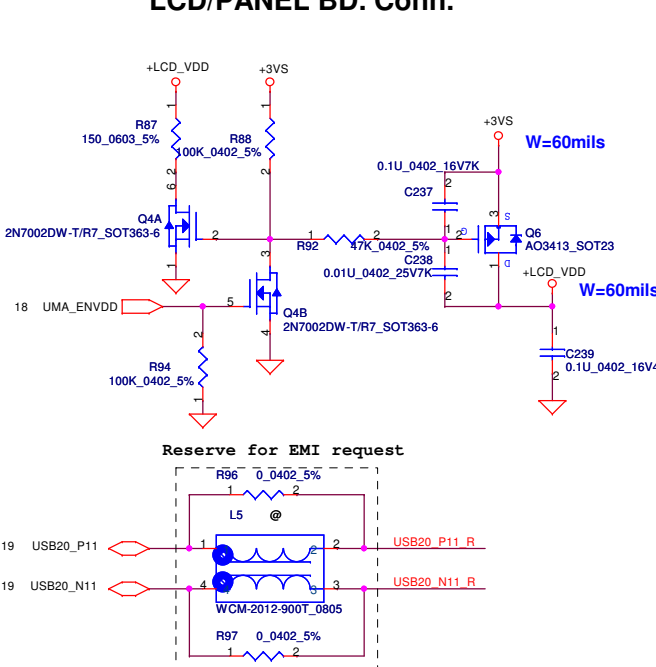
Clock Generator

Clock gen	R72	R70 R73
RTM	no-mount	mount
IDT		



CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LCD/PANEL BD. Conn.



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Size	Document Number	Rev		1.0	
Custom	NDU00_LA-6031P M/B	Date		Monday, April 12, 2010	
Sheet		12		of 45	

CRT CONNECTOR

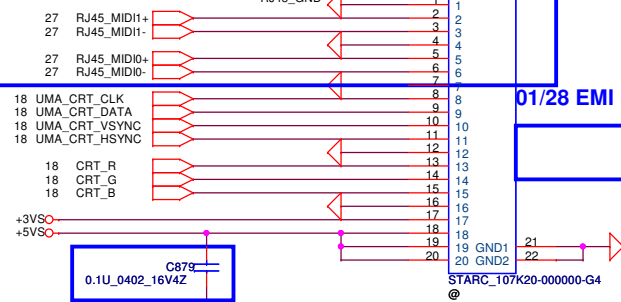
12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND

12/21 pin 2,3 to RJ45_GND

12/22 Fine tune JP4 pin define

02/08 update connector footprint.

12/21 transformer on board.

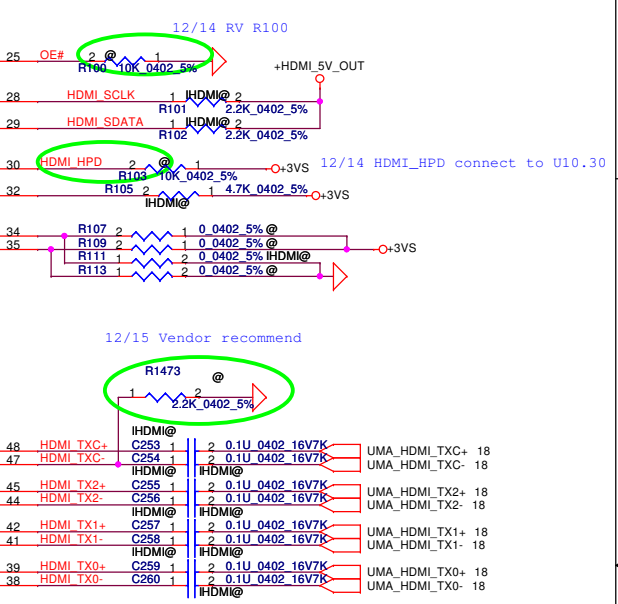
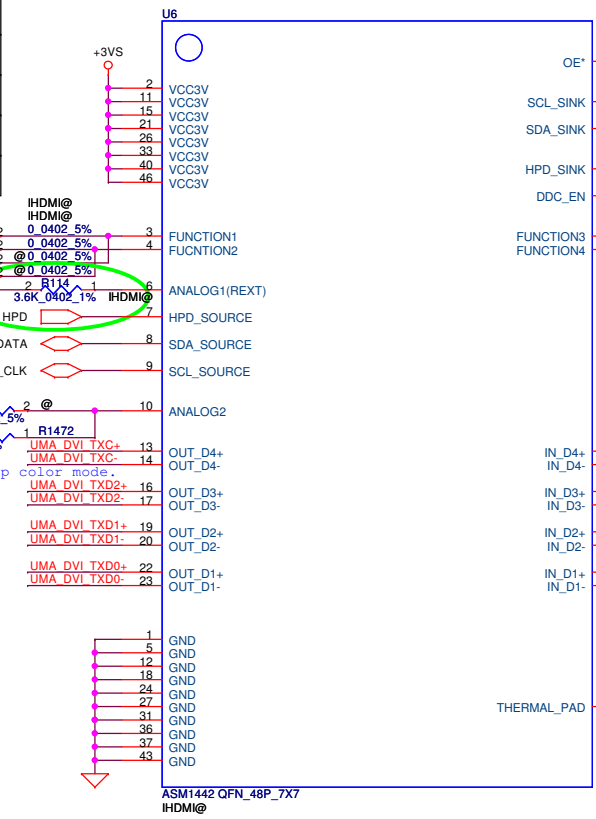
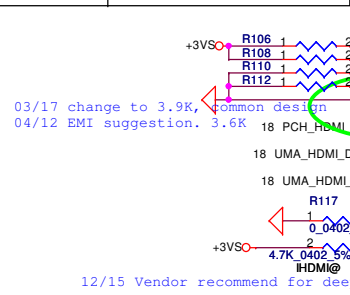
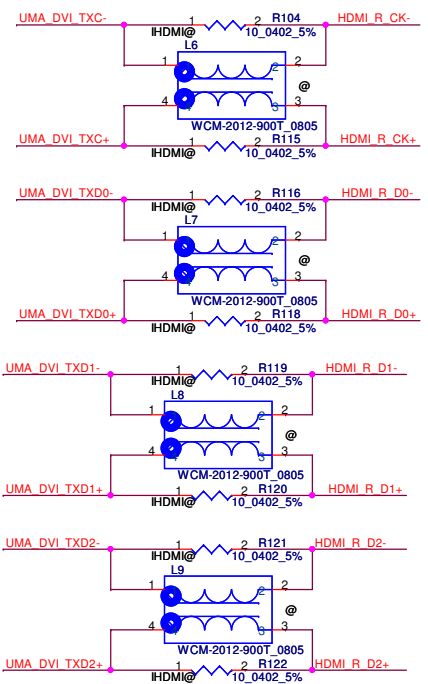
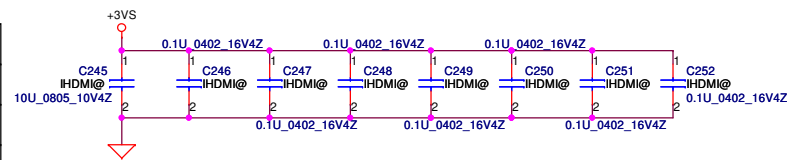


01/28 EMI request. Change pin definition.

12/17 EMI request.

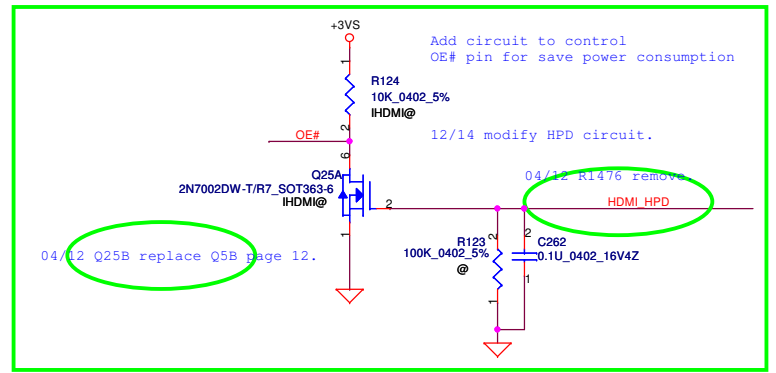
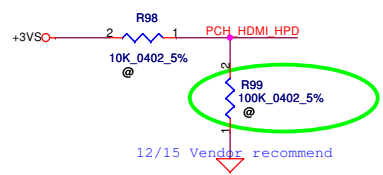
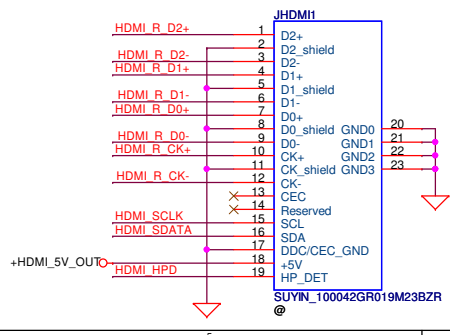
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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ANALOG2	Function2	Function1	Swing	Pre-Amp	Slew-rate	Note
Low	Low	Low	450	0	0	
Low	Low	High	420	0	-3dB	Shortest trace
Low	High	Low	450	0	-3dB	Shortest trace
Low	High	High	460	0	-4dB	Streamline PVT2 setting
High	Low	Low	340	0	0	Longest Trace
High	High	Low	400	2dB	0	Longest Trace
High	High	High	420	0	0	

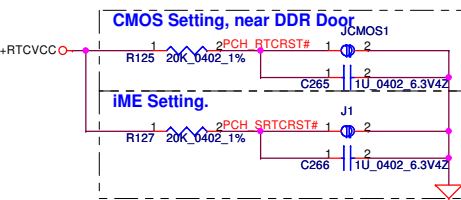


HDMI Connector

<01/27 update HDMI Connector >



Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/12	Deciphered Date	2010/01/23	HDMI Connector	
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Integrated SUS 1.05V VRM Enable

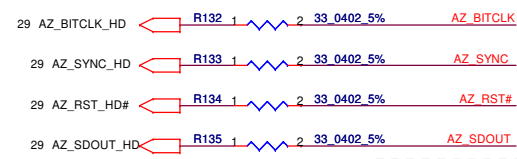
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC
 This signal has a weak internal pull down.
 H=>On Die PLL is supplied by 1.5V
 L=>On Die PLL is supplied by 1.8V

HDA_SDO
 This signal has a weak internal pull down.
 This signal can't PU

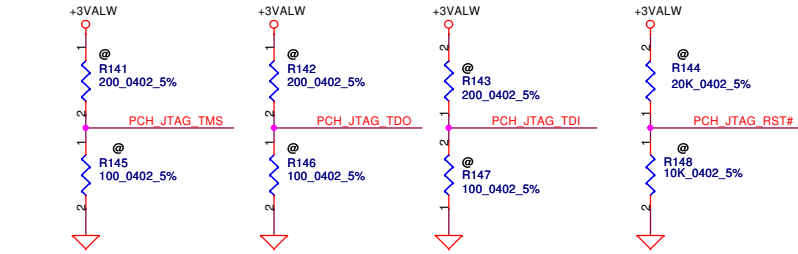
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



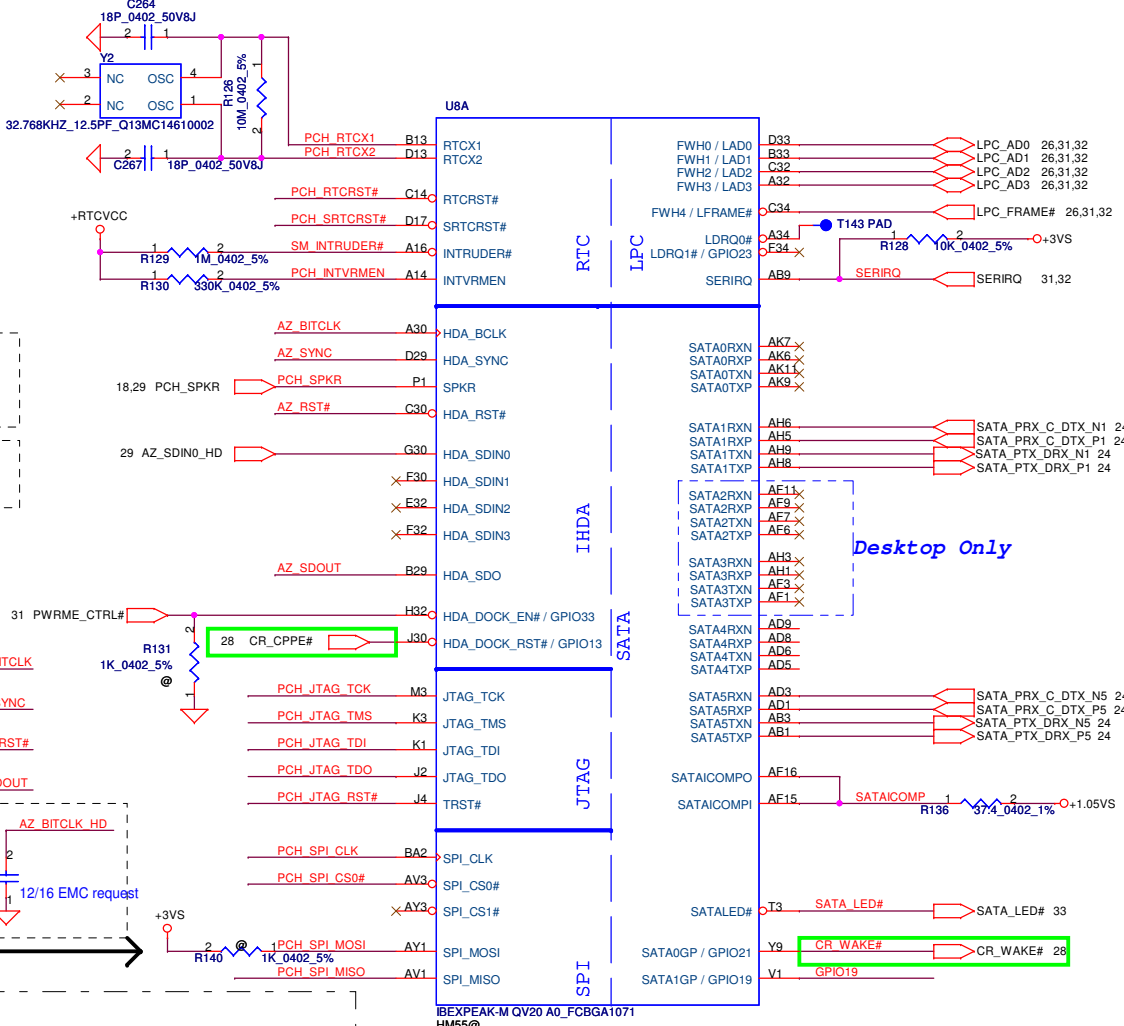
ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



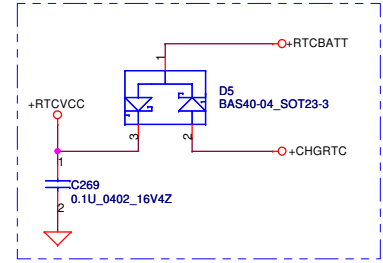
06/01 change R125 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_RST#	R517	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install

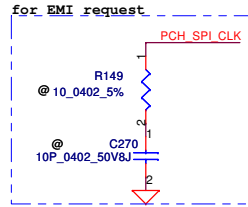
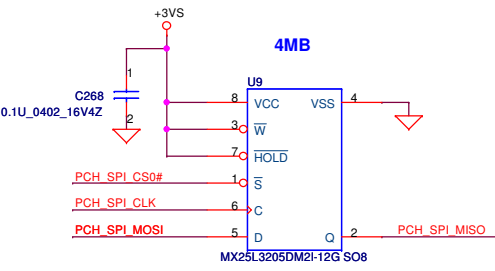


1ST HDD

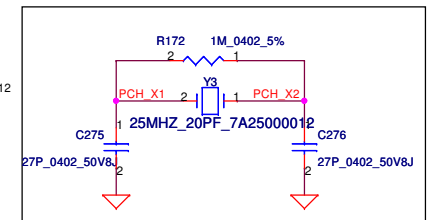
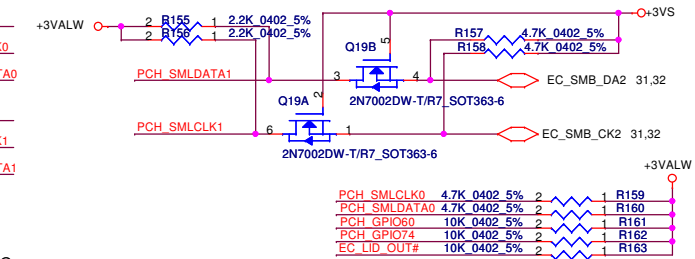
eSATA



2/8 change back to original.(Lion Wang)
 del D86 and R1494.
 2/1 Add R1494 D86 (EMI)

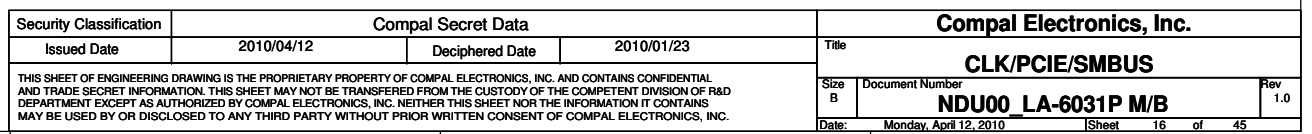


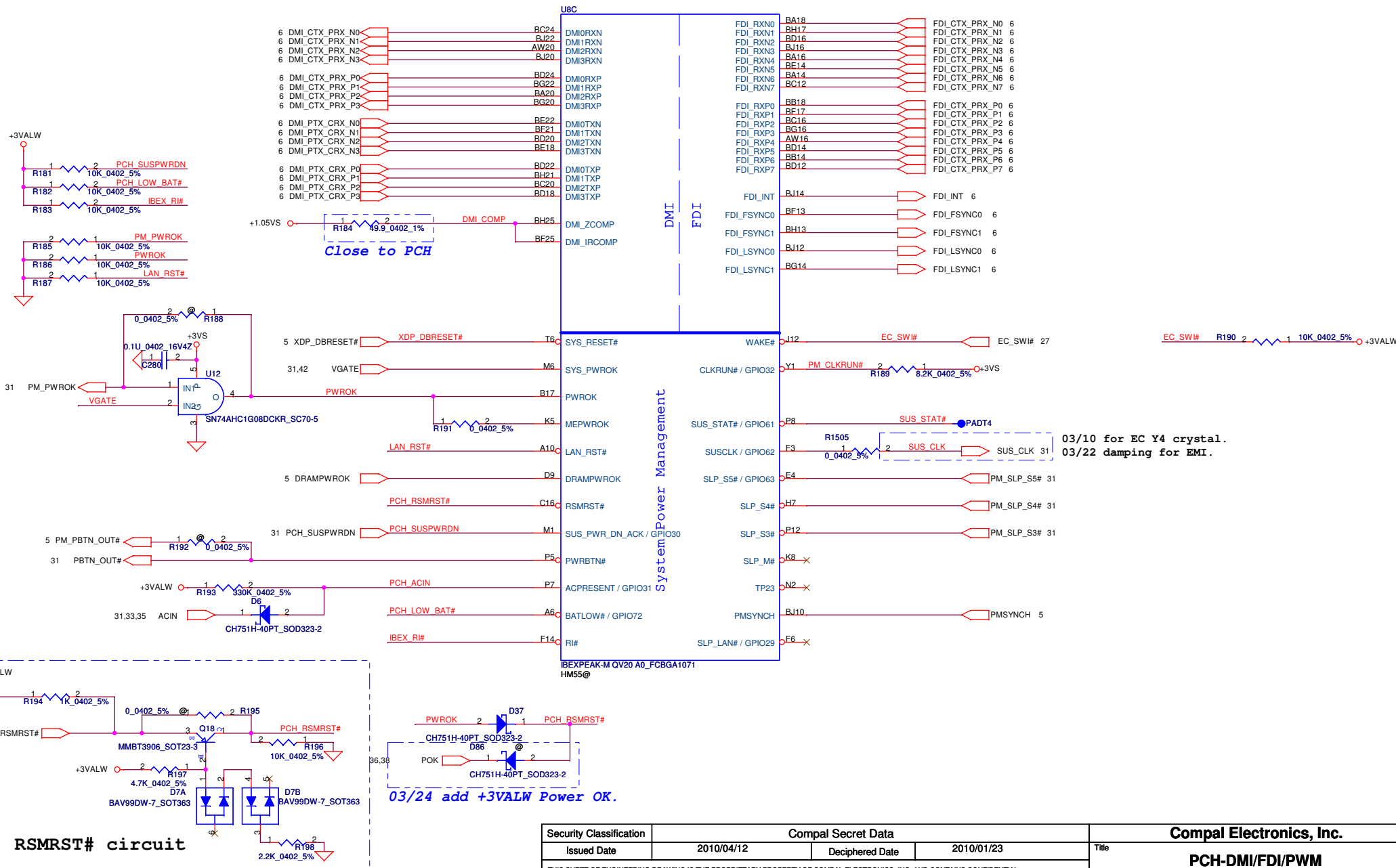
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Issued Date		2010/04/12		Deciphered Date		2010/01/23		Title	
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		Size	Document Number						Rev
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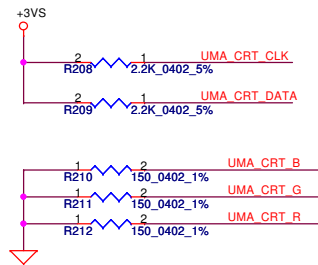
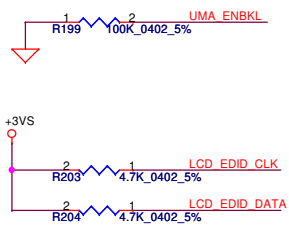
 C277 @
0_0402_5%

Note: Stuff 0 ohm if
25MHz crystal un-stuff

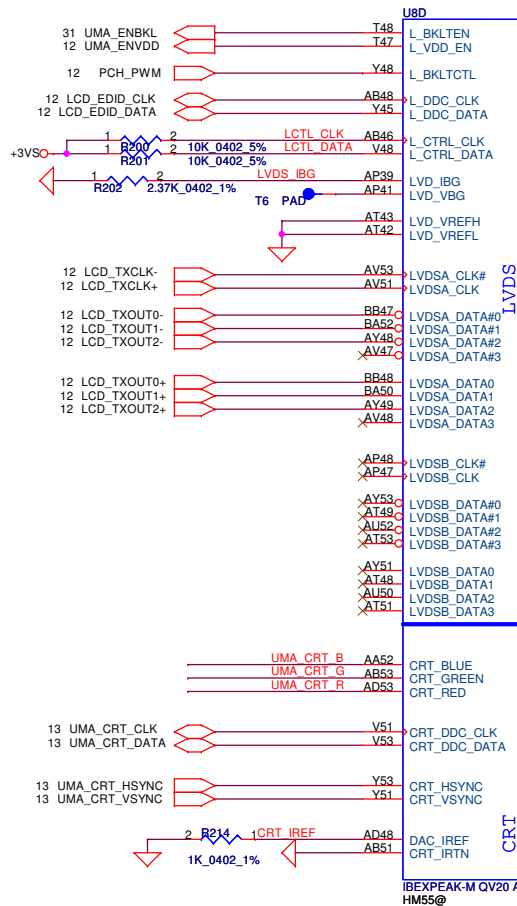
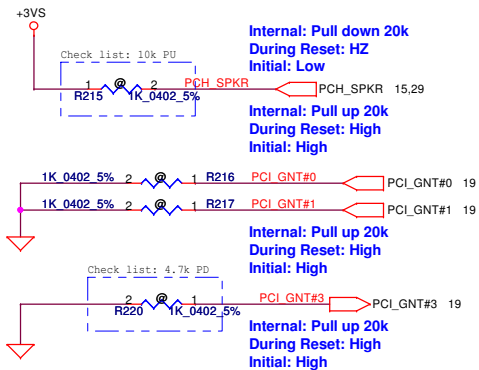




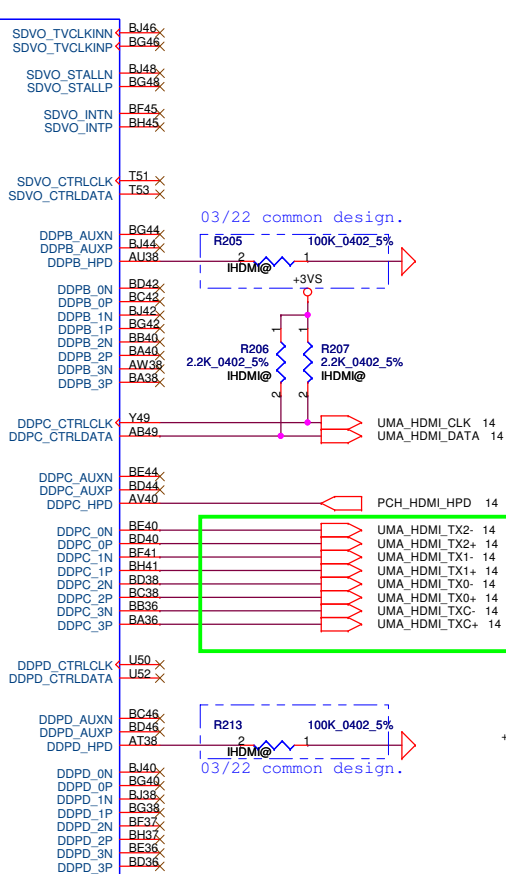
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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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PCH Strap Pin



Digital Display Interface

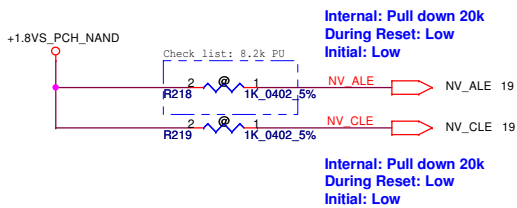


03/22 common design.

03/22 common design.

HDMI

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)



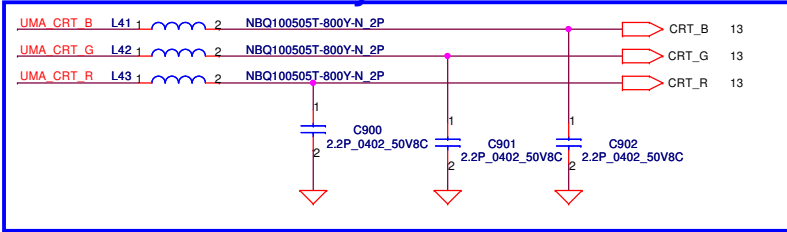
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

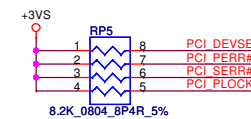
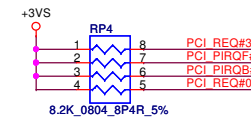
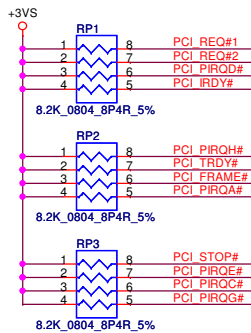
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

modify....



2/2 Add L41 L42 L43 C900 C901 C902 for EMI request



GNT2#: Not pull low, internal pull up 20K

32 CLK_PCI_DDR
31 CLK_PCI_EC
16 CLK_PCI_LOOP

18 PCI_GNT#0
18 PCI_GNT#1
18 PCI_GNT#3

T37 PAD

5,26,27,28,31,32 PLT_RST#

PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3

PCI_PIRQA#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#

PCI_IRDY#
PCI_DEVSEL#
PCI_FRAME#
PCI_PLOCK#

PCI_SERR#
PCI_PERR#
PCI_TRDY#

PCI_PERR#
PCI_PERR#
PCI_PERR#

PCI_PERR#
PCI_PERR#
PCI_PERR#

PCI_PERR#
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U8E
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AD26
AD27
AD28
AD29
AD30
AD31

C/BE0#
C/BE1#
C/BE2#
C/BE3#

PIRQA#
PIRQB#
PIROC#
PIRQD#

REQ0# / GPIO50
REQ1# / GPIO52
REQ2# / GPIO54
REQ3# / GPIO55

GNT0# / GPIO51
GNT1# / GPIO53
GNT2# / GPIO55
GNT3# / GPIO55

PIRQA# / GPIO2
PIRQB# / GPIO3
PIROC# / GPIO4
PIRQD# / GPIO5

PCIRST#
SERR#
PERR#

IRDY#
PAIR#
DEVSEL#
FRAME#

PLOCK#
STOP#
TRDY#

PME#
PLTRST#

CLKOUT_PCIO
CLKOUT_PC11
CLKOUT_PC12
CLKOUT_PC13
CLKOUT_PC14

CLK_SIO
CLK_EC
CLK_PCH

CLKOUT_PCIO
CLKOUT_PC11
CLKOUT_PC12
CLKOUT_PC13
CLKOUT_PC14

CLKOUT_PCIO
CLKOUT_PC11
CLKOUT_PC12
CLKOUT_PC13
CLKOUT_PC14

CLKOUT_PCIO
CLKOUT_PC11
CLKOUT_PC12
CLKOUT_PC13
CLKOUT_PC14

CLKOUT_PCIO
CLKOUT_PC11
CLKOUT_PC12
CLKOUT_PC13
CLKOUT_PC14

NVRAM

PCI

USB

NV_CE#0
NV_CE#1
NV_CE#2
NV_CE#3
NV_DQS0
NV_DQS1
NV_DQ0 / NV_IO0
NV_DQ1 / NV_IO1
NV_DQ2 / NV_IO2
NV_DQ3 / NV_IO3
NV_DQ4 / NV_IO4
NV_DQ5 / NV_IO5
NV_DQ6 / NV_IO6
NV_DQ7 / NV_IO7
NV_DQ8 / NV_IO8
NV_DQ9 / NV_IO9
NV_DQ10 / NV_IO10
NV_DQ11 / NV_IO11
NV_DQ12 / NV_IO12
NV_DQ13 / NV_IO13
NV_DQ14 / NV_IO14
NV_DQ15 / NV_IO15

NV_ALE
NV_CLE

NV_RCOMP
NV_RB#

NV_WR#0_RE#
NV_WR#1_RE#

NV_WE#_CK0
NV_WE#_CK1

USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
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USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P

USB20_N0 30
USB20_P0 30
USB20_N1 30
USB20_P1 30
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USB20_P3 24
USB20_N5 25
USB20_P5 25

USB20_N10 26
USB20_P10 26
USB20_N11 12
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USB20_P13 26

AY9
BD1
AP15
BD8
AV9
BG8
AP7
AP6
AT9
BB1
AV6
BB3
BA4
BE4
BB6
BD6
BB7
BC8
BJ8
BJ6
BG6

BD3
AY6

AV7
AV8
AY5

AV11
BF5

USB20_N0 30
USB20_P0 30
USB20_N1 30
USB20_P1 30
USB20_N3 24
USB20_P3 24
USB20_N5 25
USB20_P5 25

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NV_CLE 18

USB-RIGHT1
USB-RIGHT2

eSATA-USB

BT

8 pins SIM card
Int. Camera
3G
WiMax(WLAN)

Within 500 mils

03/23 common design.

SLP_CHG_M3_PCH 24
SLP_CHG_M4_PCH 24

SLP_CHG_M3_PCH 24
SLP_CHG_M4_PCH 24

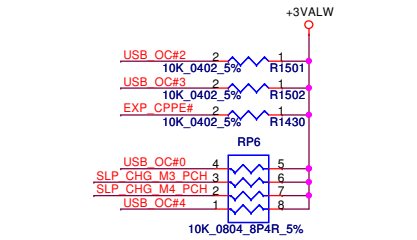
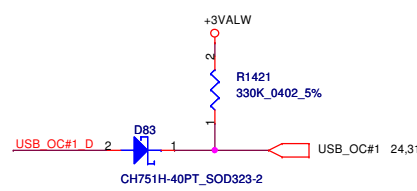
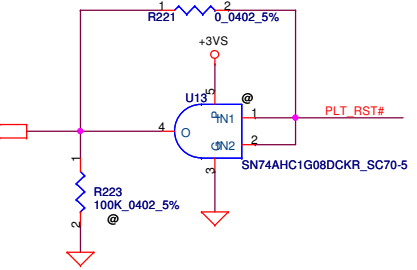
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SLP_CHG_M4_PCH 24

SLP_CHG_M3_PCH 24
SLP_CHG_M4_PCH 24

SLP_CHG_M3_PCH 24
SLP_CHG_M4_PCH 24

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SLP_CHG_M4_PCH 24

SLP_CHG_M3_PCH 24
SLP_CHG_M4_PCH 24



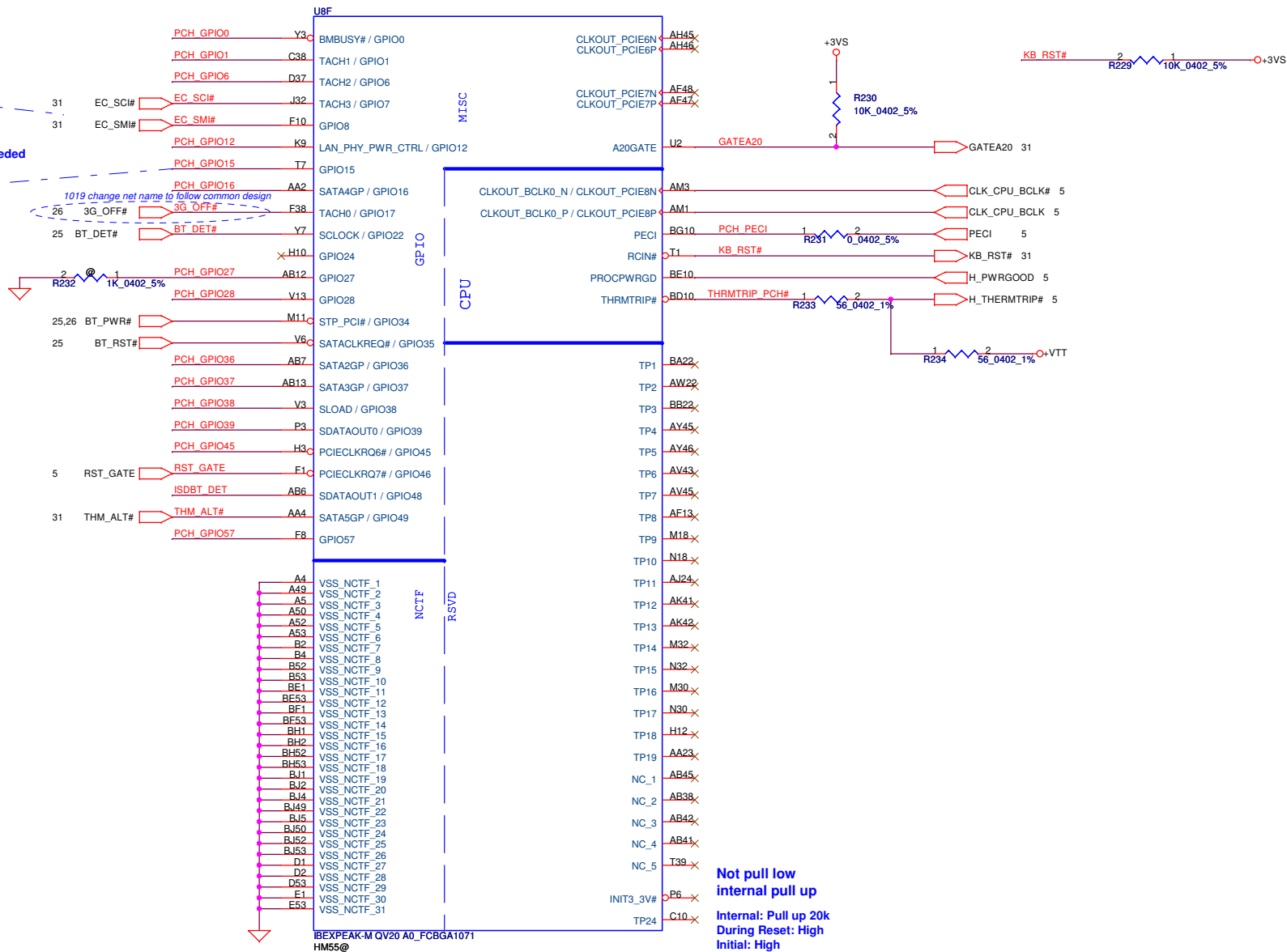
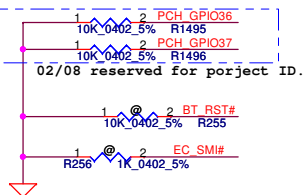
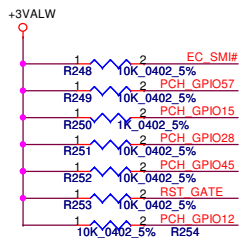
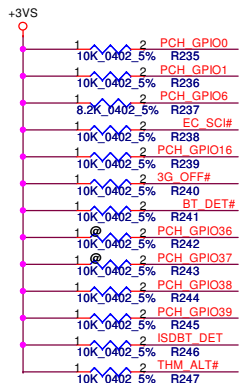
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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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				Date: Monday, April 12, 2010	Sheet 19 of 45

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

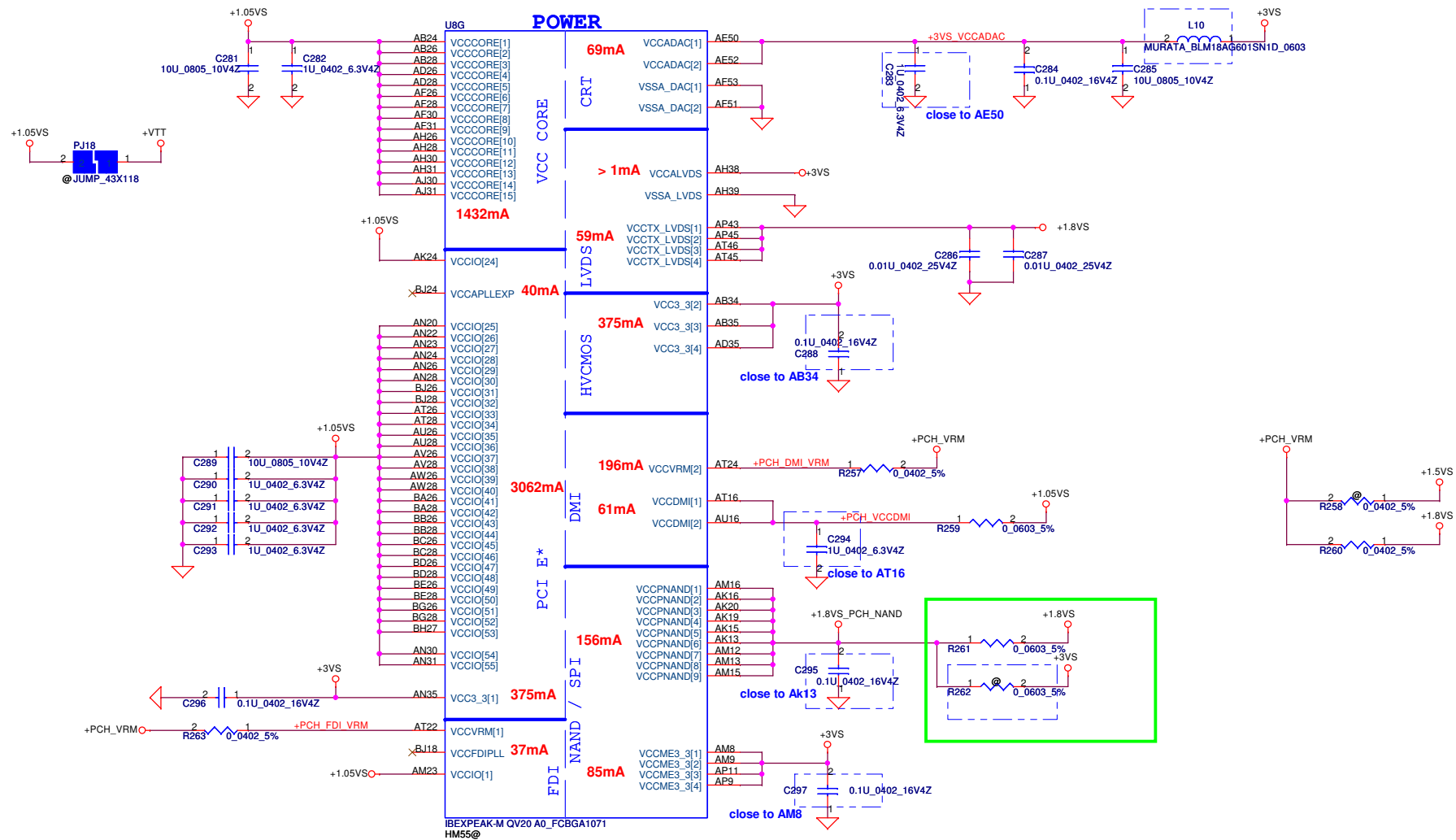
On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled

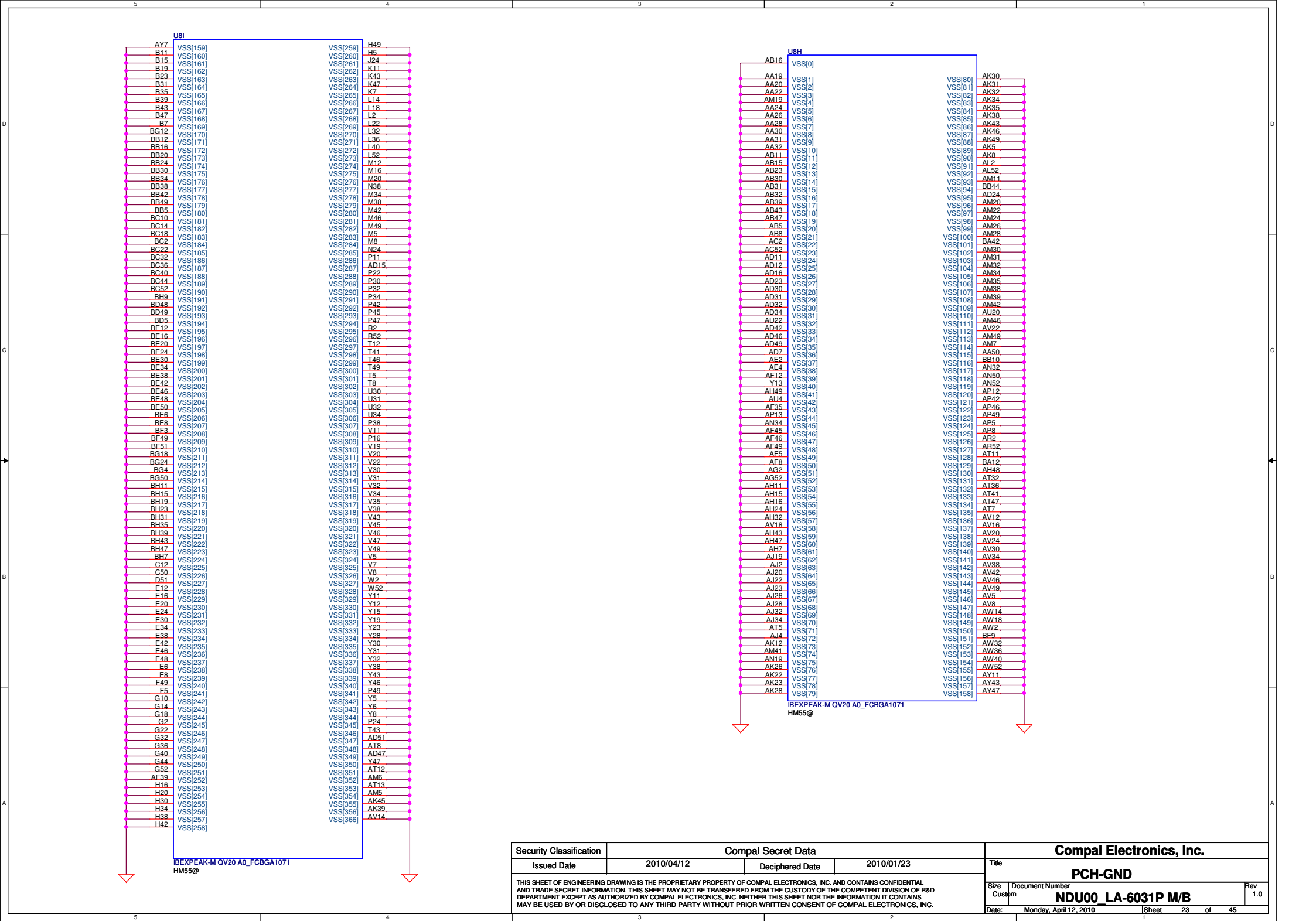


Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

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Size B	Document Number	NDU00_LA-6031P M/B		Rev	1.0
Date:	Monday, April 12, 2010	Sheet	20	of	45

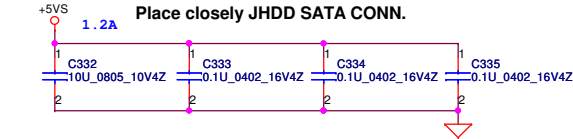


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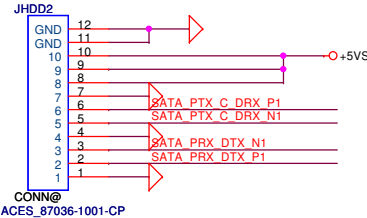
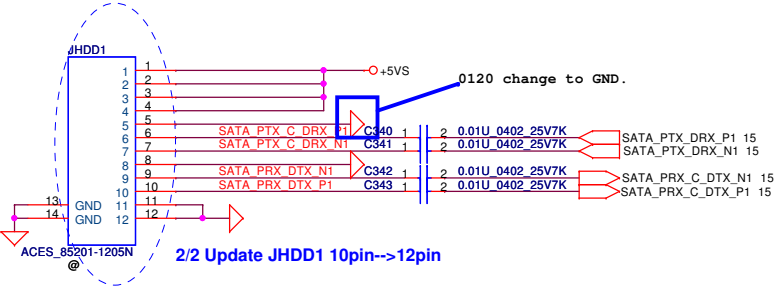
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						Size	Document Number				Rev
						Custom	NDU00 LA-6031P M/B				1.0
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SATA HDD Conn.



1/28 Add JHDD2

JHDD2 Layout symbol reverse JHDD1, reverse the pin define

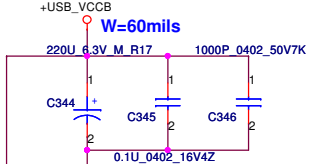
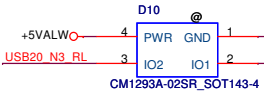
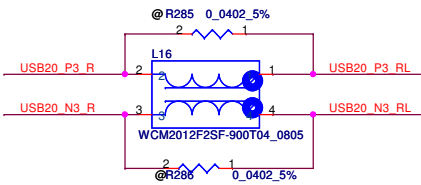
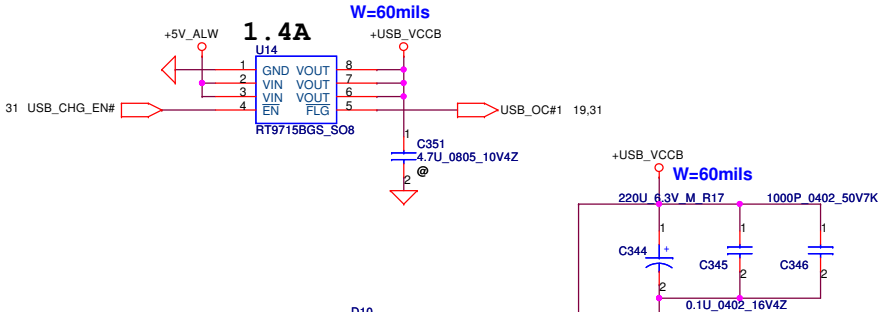
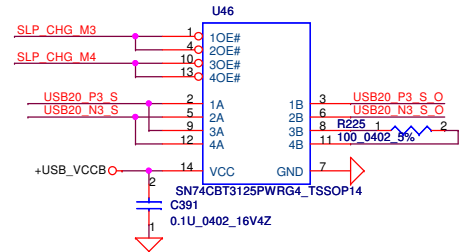
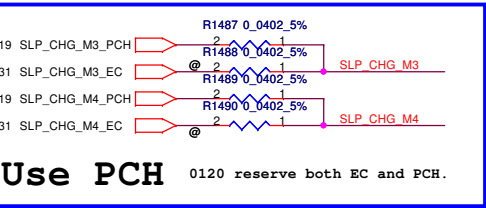
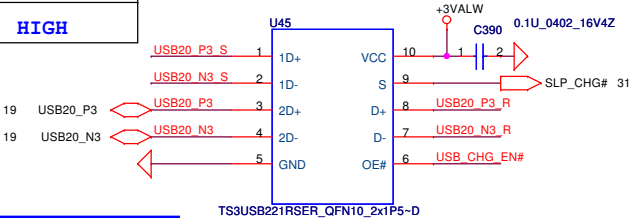


Add wire connector for H/W SATA verify

eSATA/USB Combo

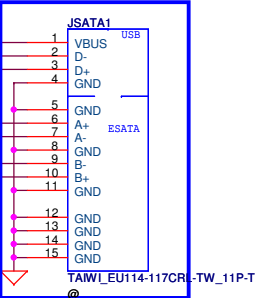
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



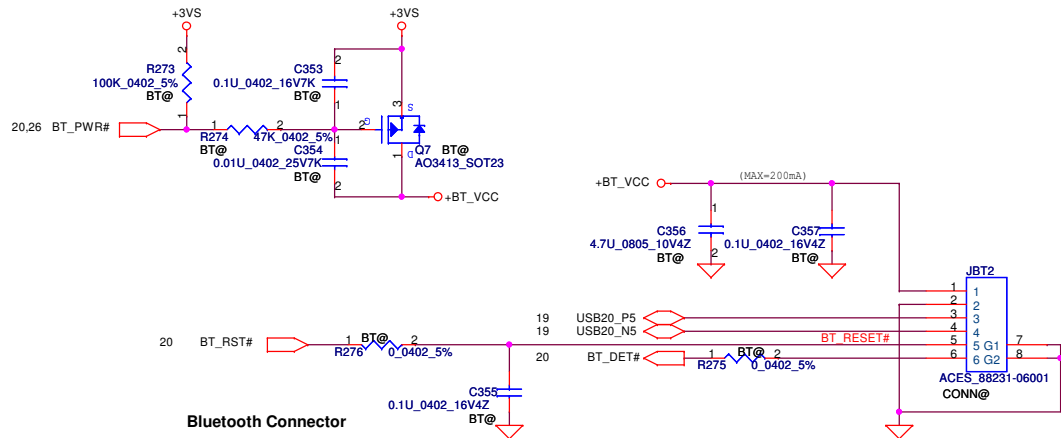
eSATA/USB Conn

1/26 update JSATA1 footprint



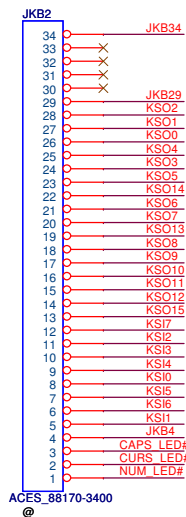
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						Size		Document Number		Rev	
						NDU00_LA-6031P M/B		1.0			
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BlueTooth Interface

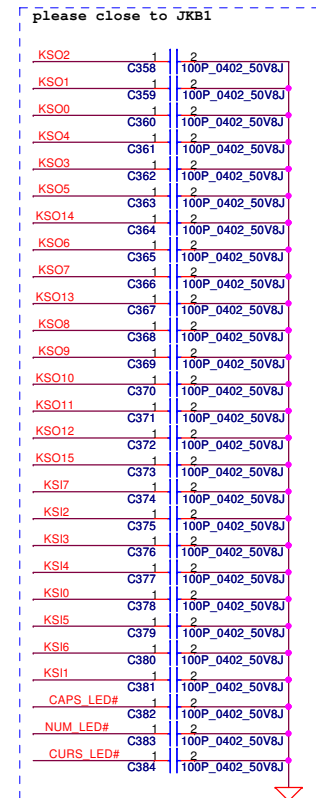
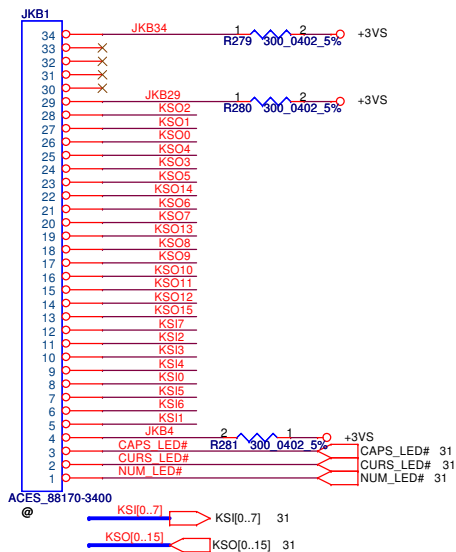


Bluetooth Connector

KEYBOARD CONN. for 11.6"

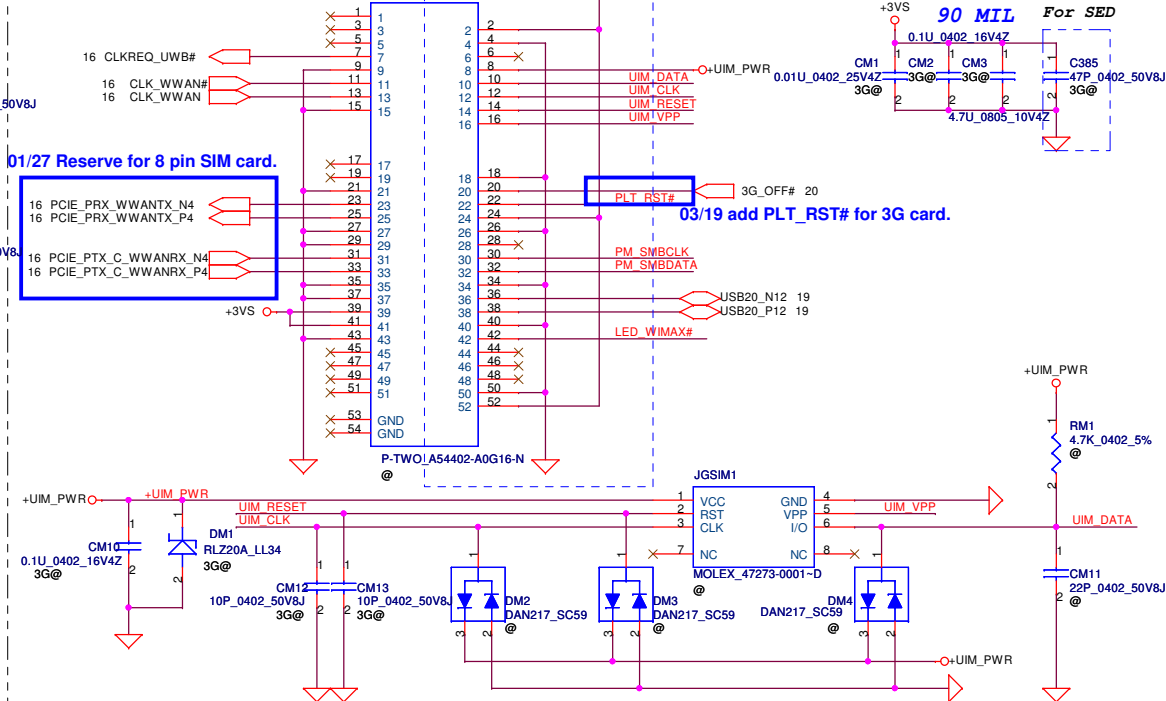


KEYBOARD CONN. for 13.3"



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PCIe Mini Card-3G



	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

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				Size	Document Number	Rev
				NDU00_LA-6031P M/B Date: <u>Monday, April 12, 2010</u> Sheet <u>26</u> of <u>45</u>		

12/14 Fine tune pin define UL1 Pin37 Pin40 -->Dummy

Main: SHI000AA00 2nd : SHI000AB00
Can change to 2.2uH&4.7uF
+LAN_REGOUT
Layout Note: LL1 must be within 200mil to Pin36
CL8, CL9 must be within 4.7U_0805_6.3V6M
200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin 27,39,12,47,48

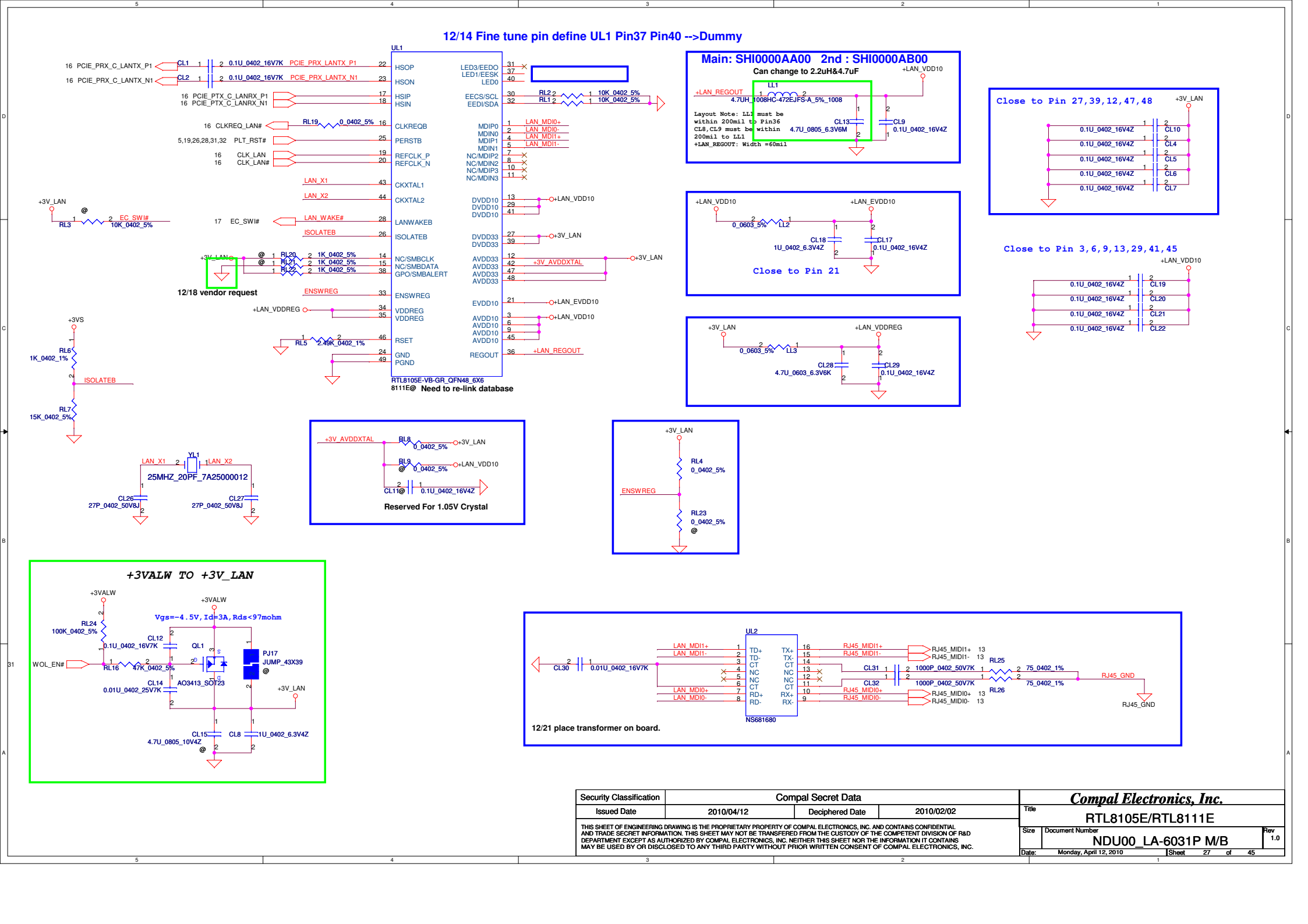
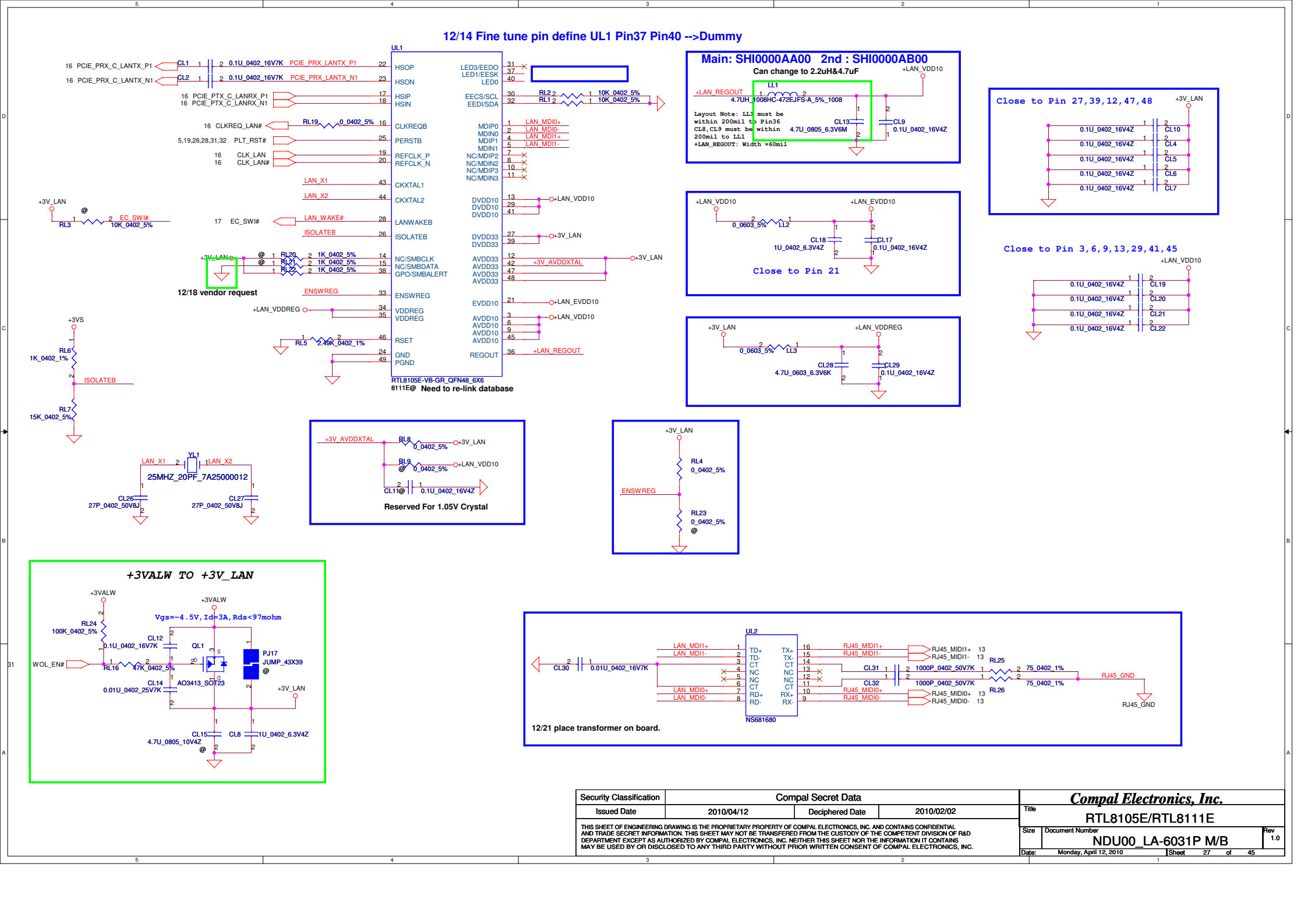
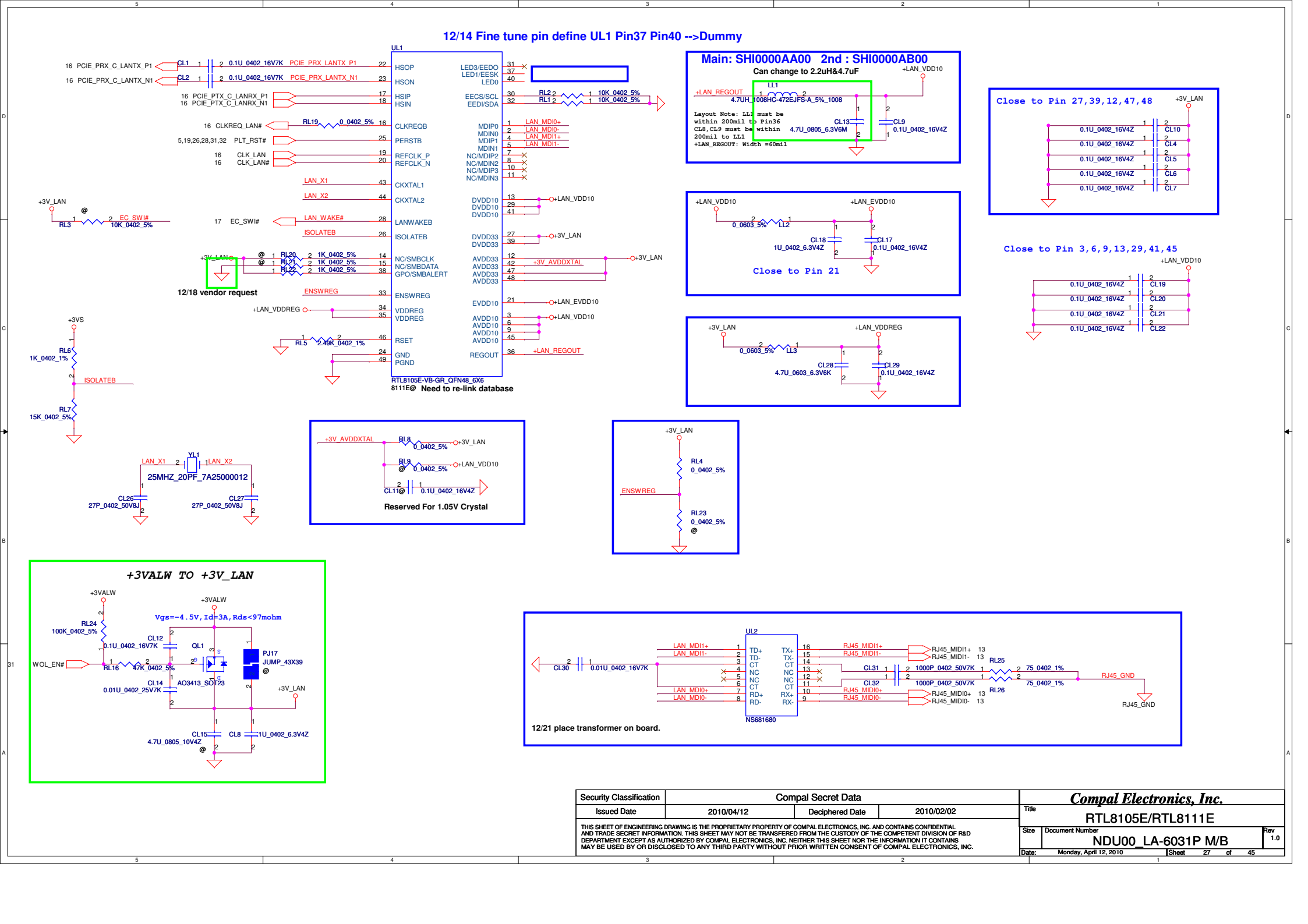
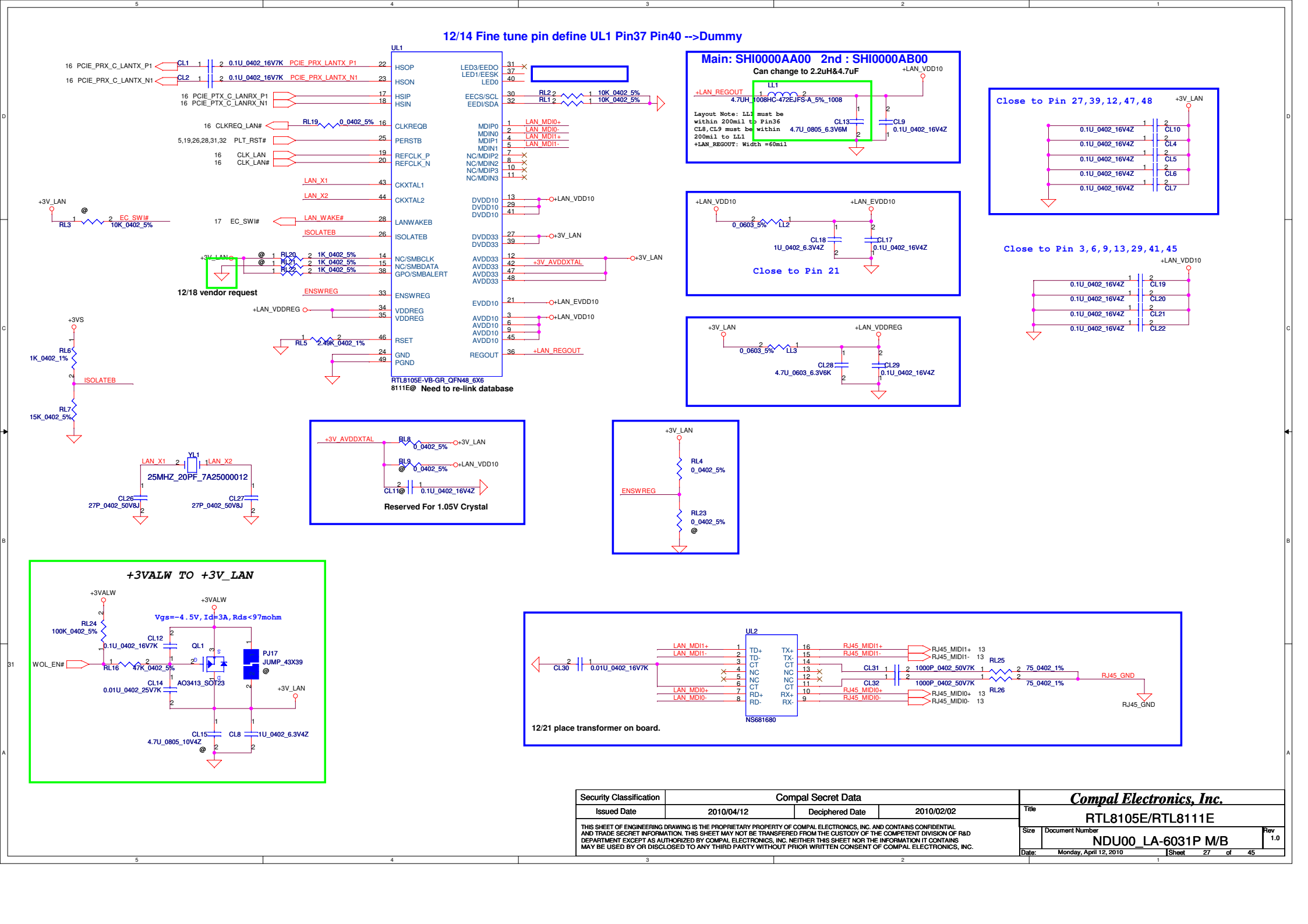
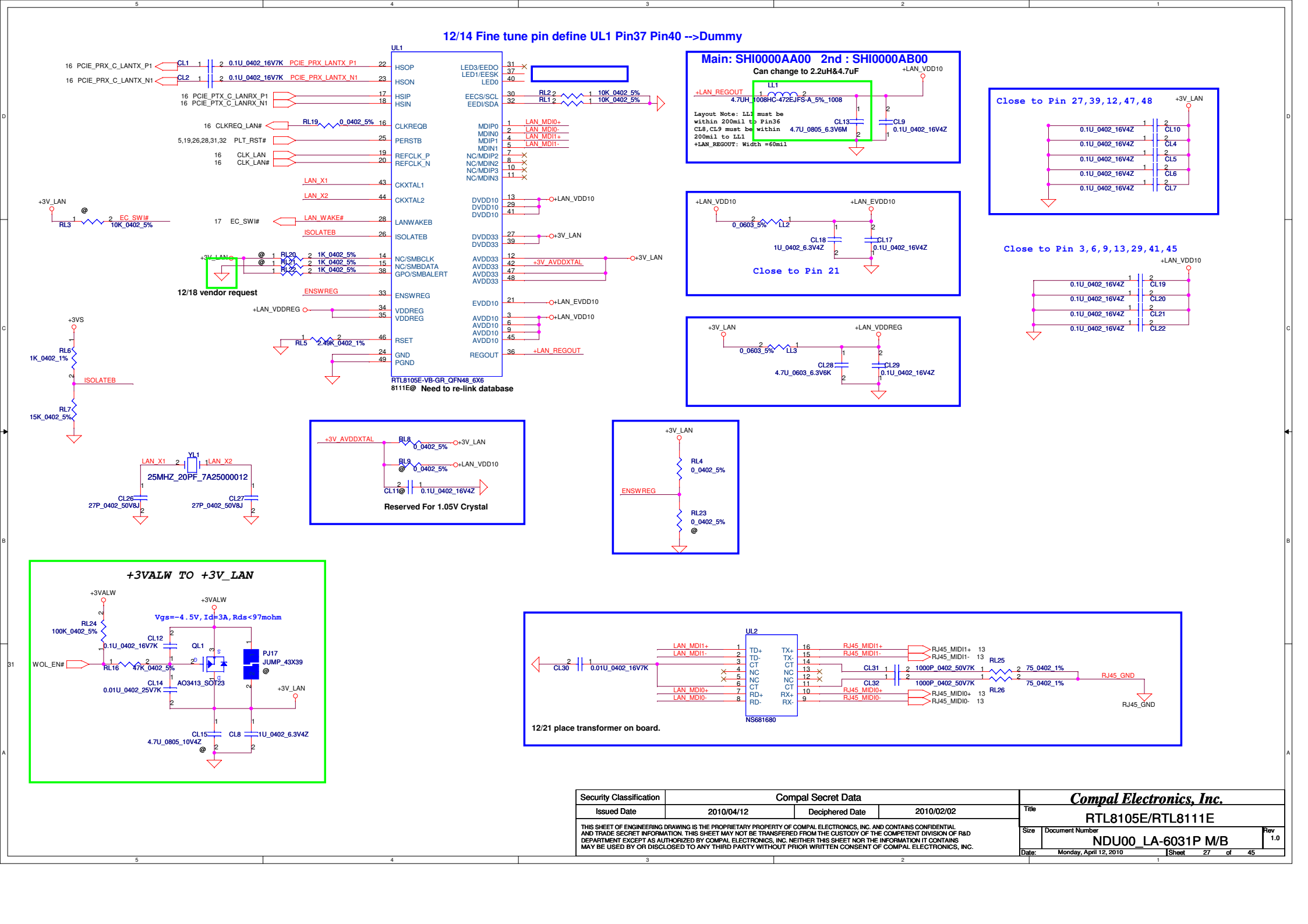
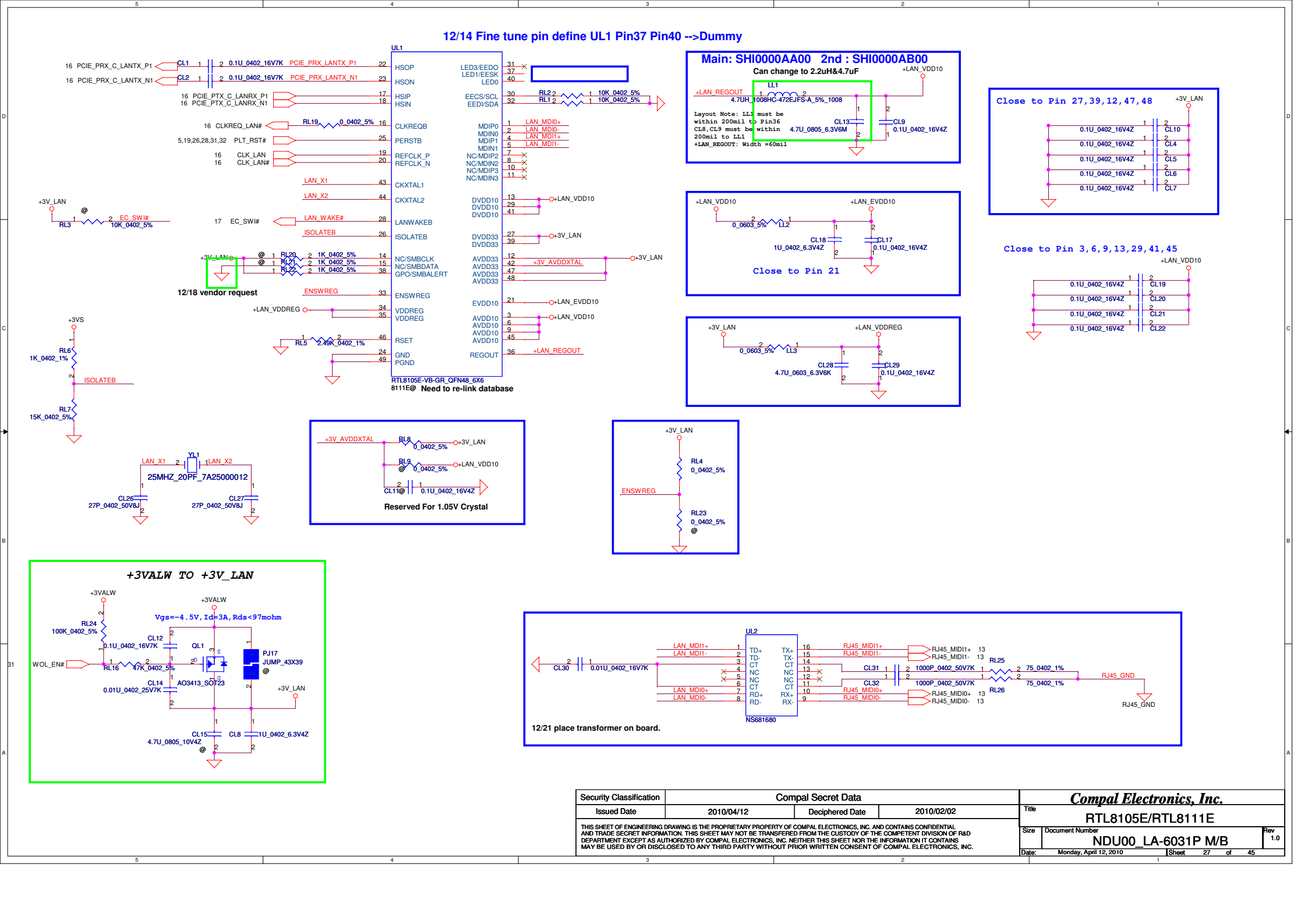
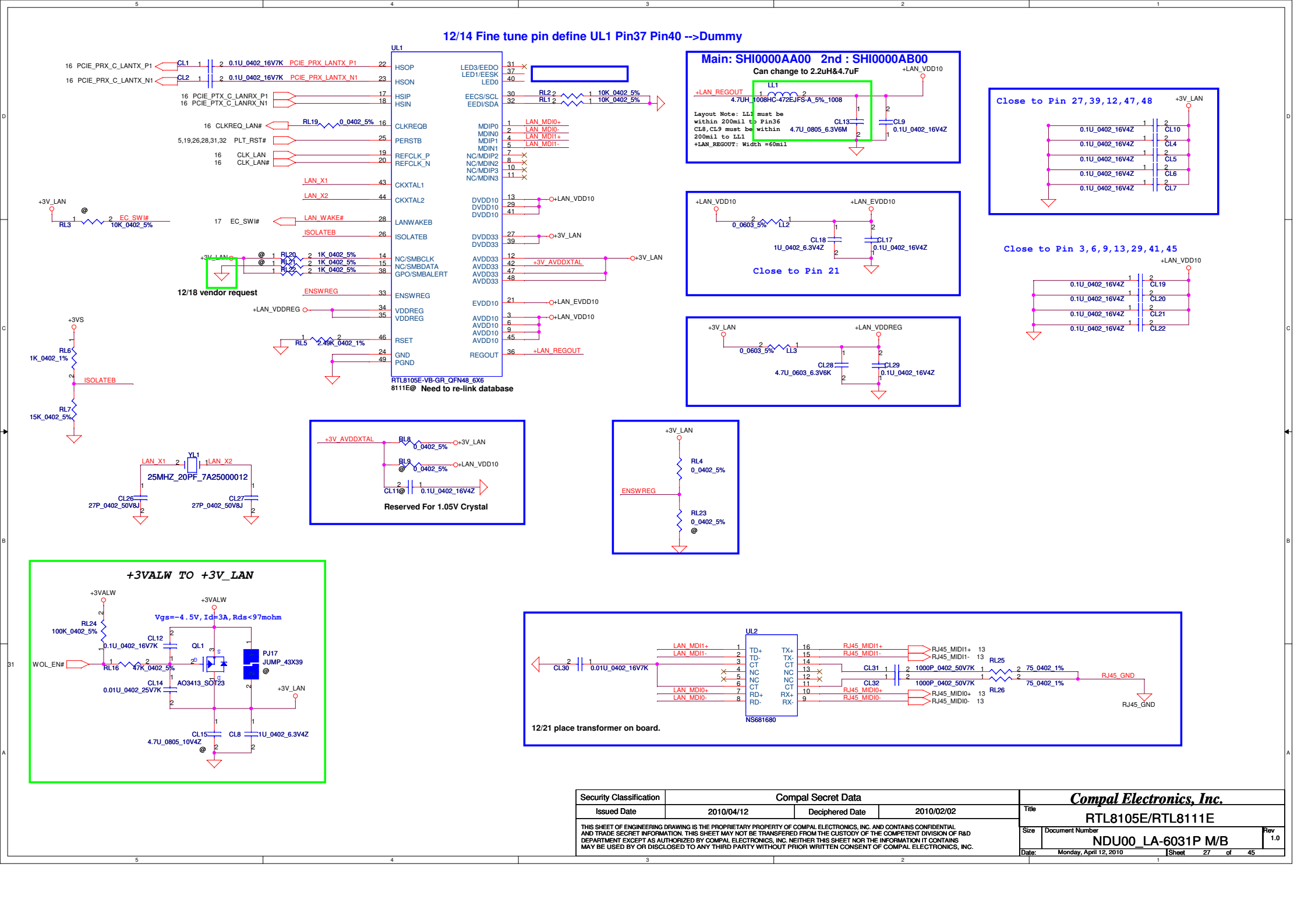
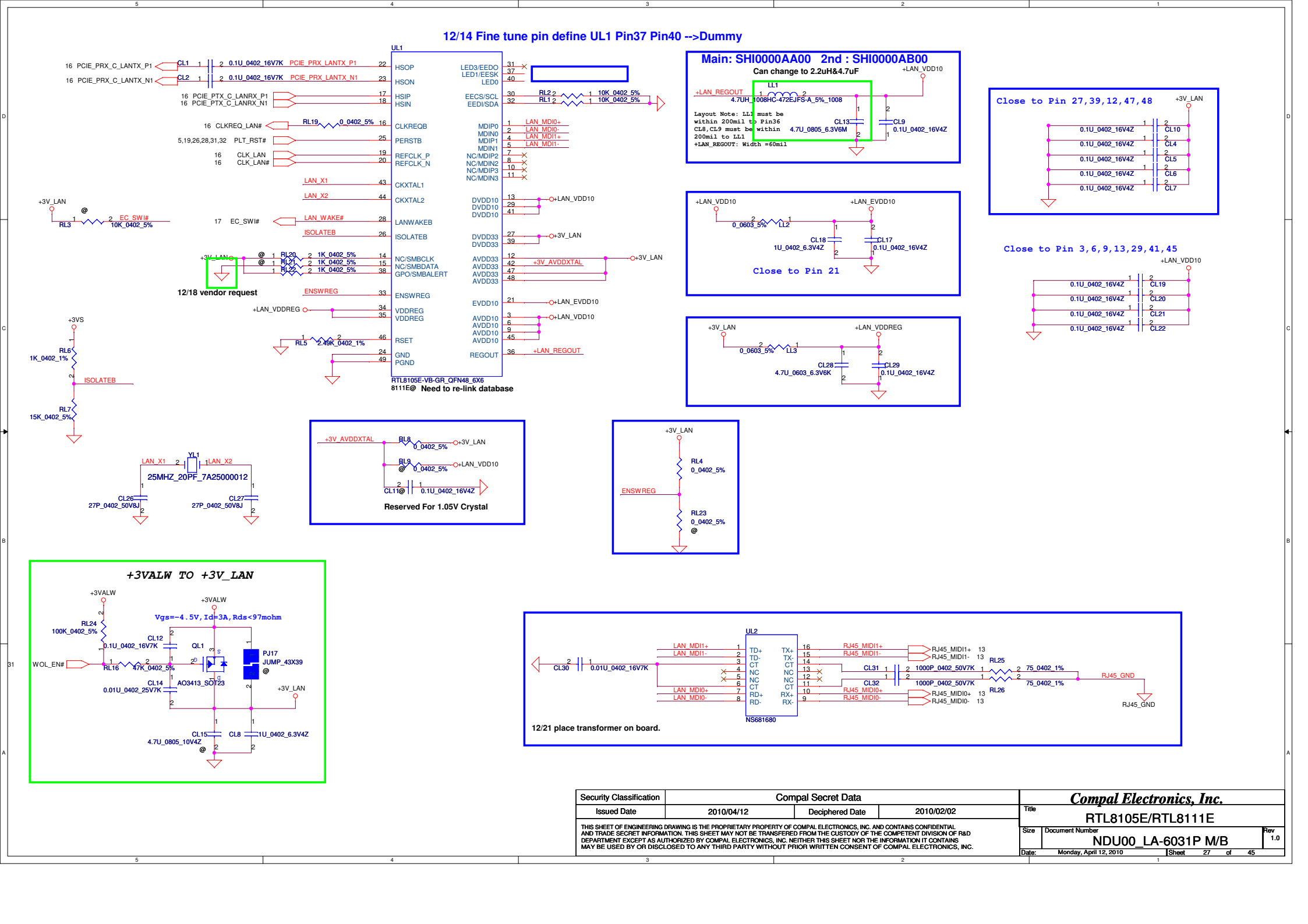
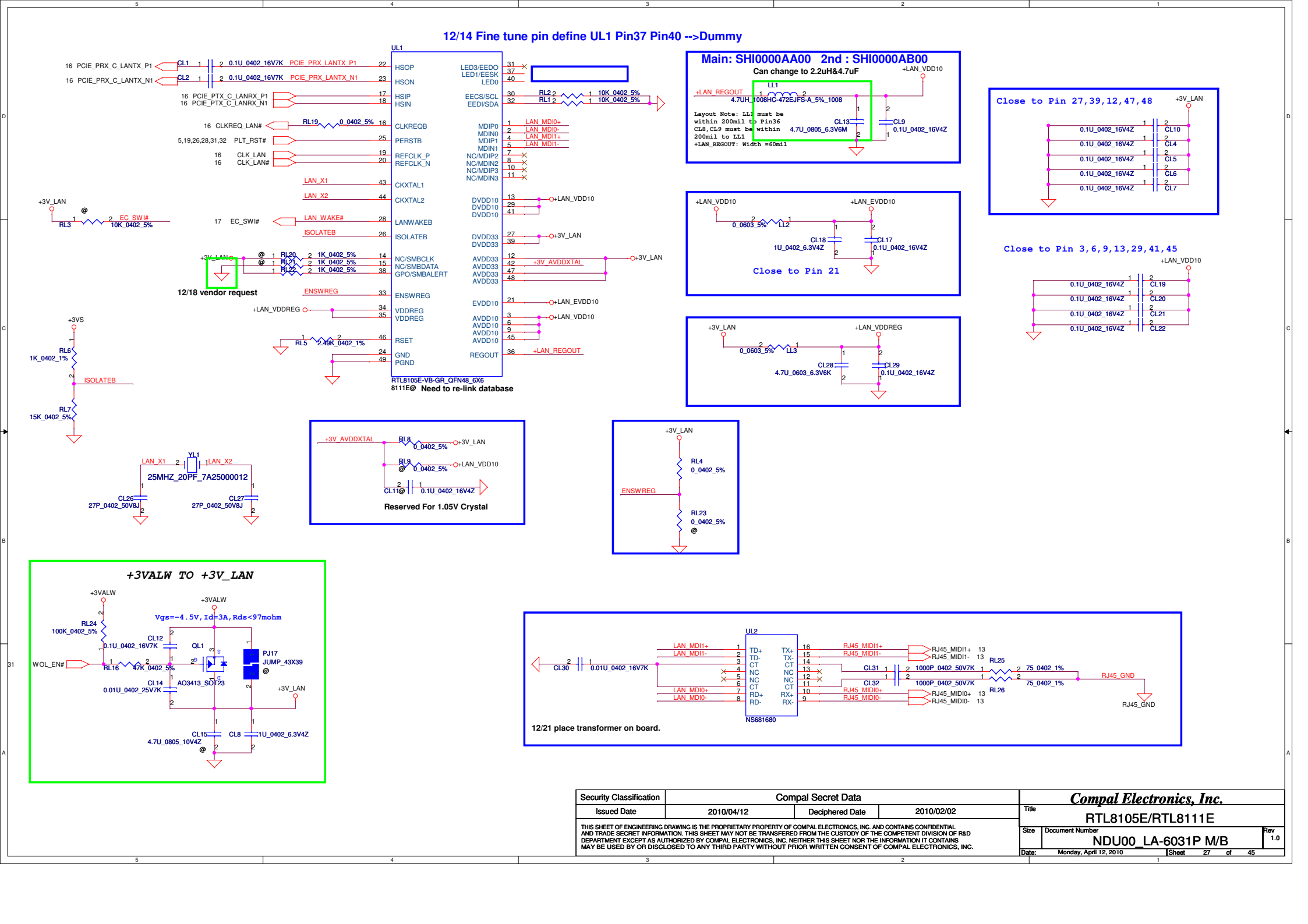
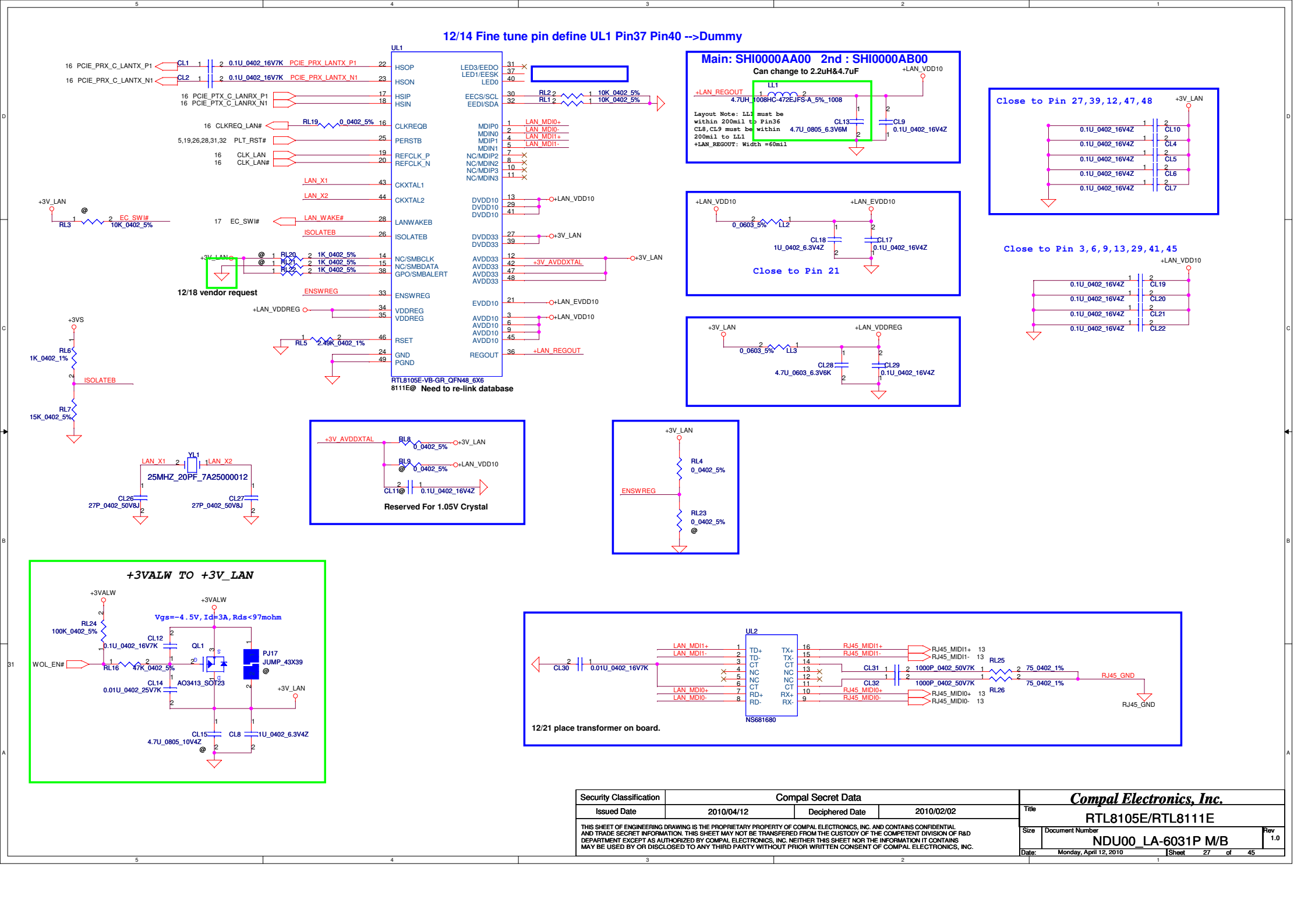
Close to Pin 21

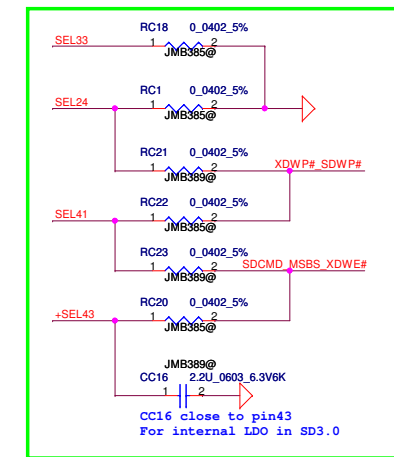
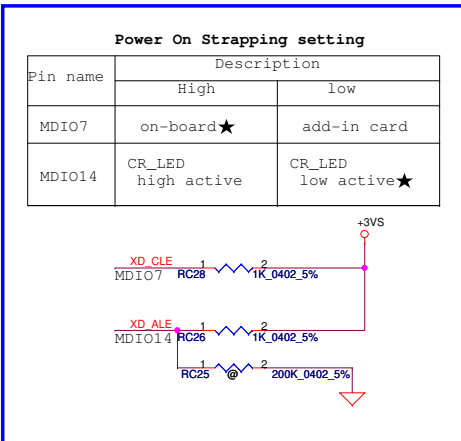
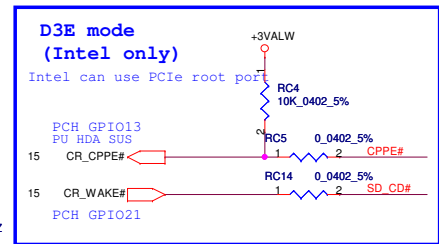
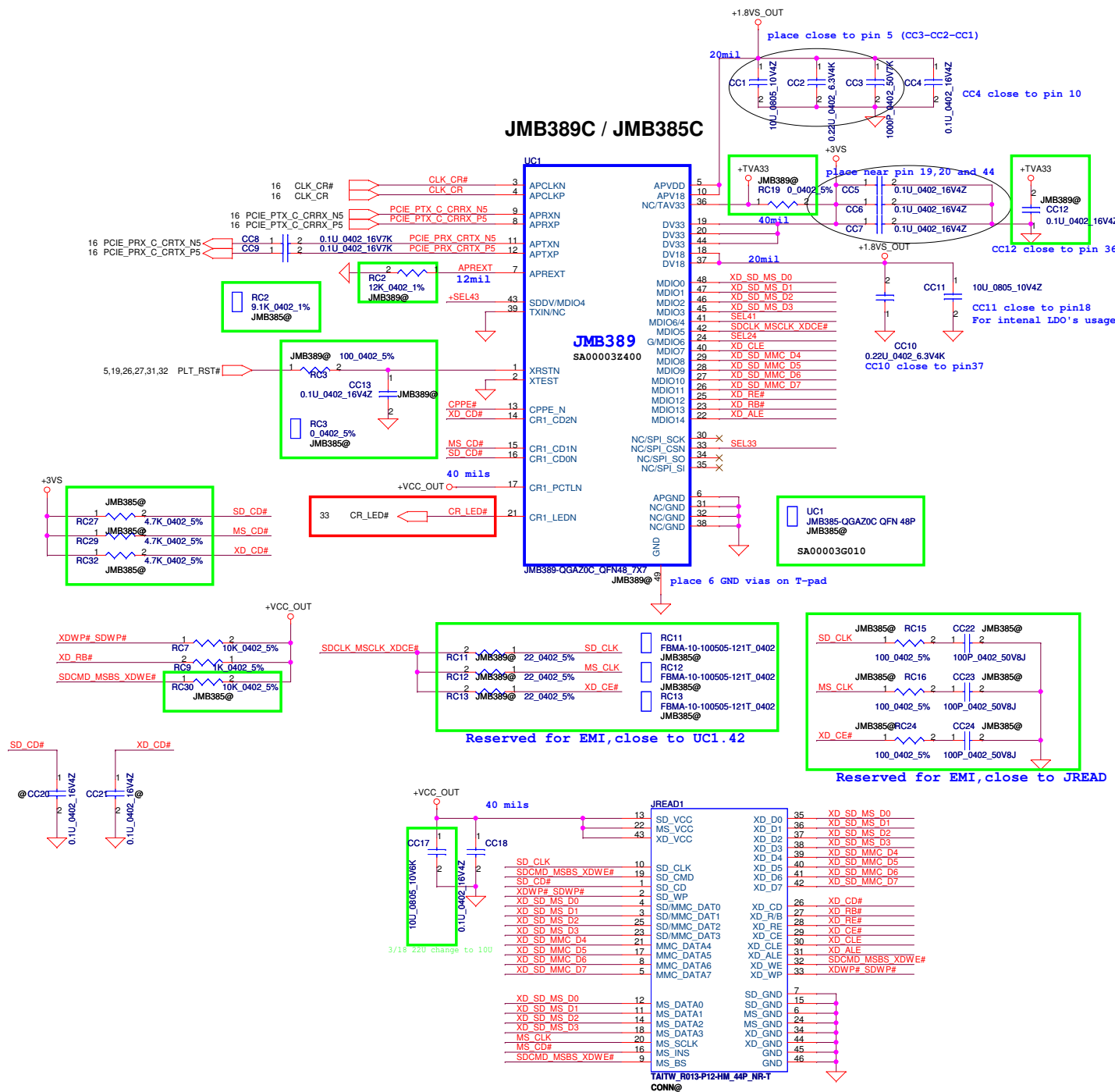
Close to Pin 3,6,9,13,29,41,45

+3VALW TO +3V_LAN
Vgs=-4.5V, Id=3A, Rds<97mohm
P17 JUMP_43X39
AO3413_SOT23
4.7U_0805_10V4Z

12/21 place transformer on board.

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Compal Secret Data
Issued Date: 2010/04/12
Deciphered Date: 2010/02/02
Title: RTL8105E/RTL8111E
Size: Document Number NDU00 LA-6031P M/B Rev 1.0
Date: Monday, April 12, 2010 Sheet 27 of 45





01/26 Update new card reader symbol to EVT

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				Date:	Monday, April 12, 2010
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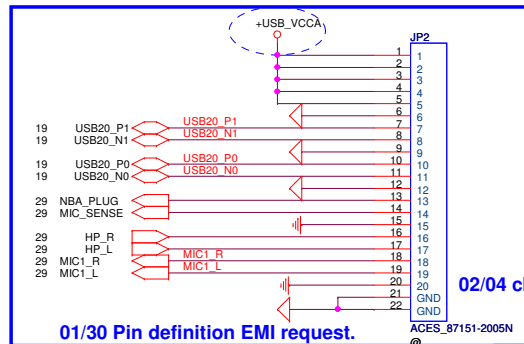
Compal Electronics, Inc.

Card Reader-JMB389C/385C

NBQAA LA6071P M/R

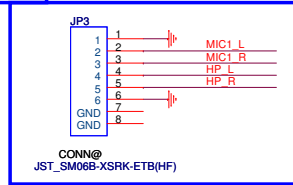
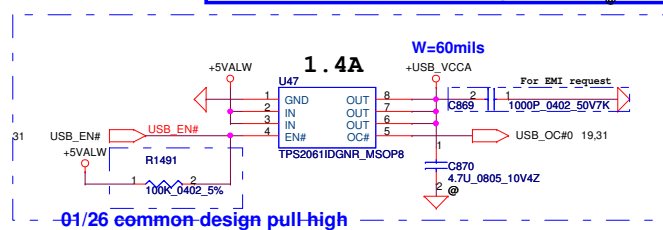
USB+Audio FFC conn Pin=20pin, pitch=0.5

01/30 New JP2 Layout symbol reverse old conn, reserse the pin define



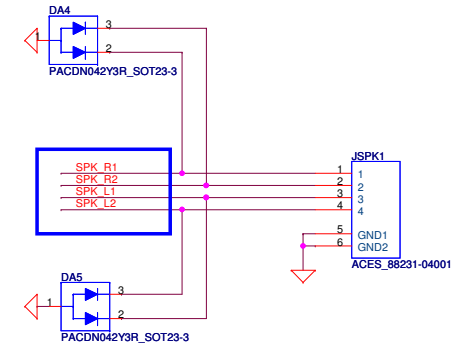
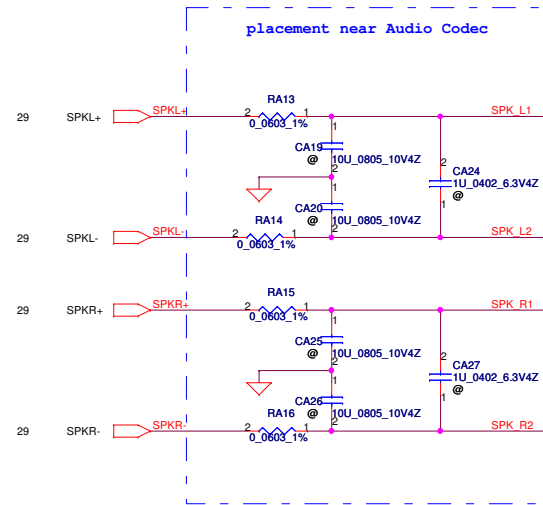
02/04 change back to 20 pins.

01/30 Pin definition EMI request.



12/19 Reserved JP6 for audio test

Speaker Connector



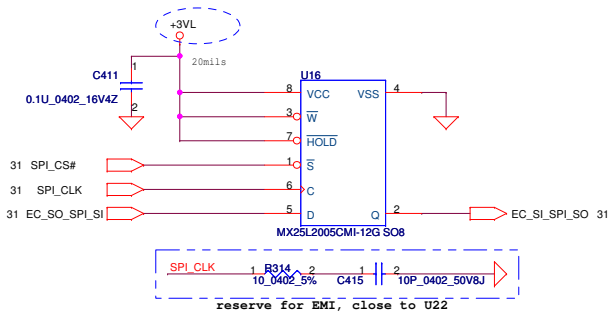
12/16 Fine tune SPK_L1, SPK_L2, SPK_R1 and SPK_R2 for SPK

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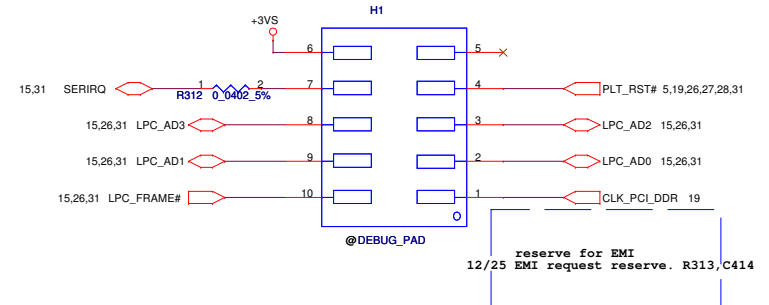
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

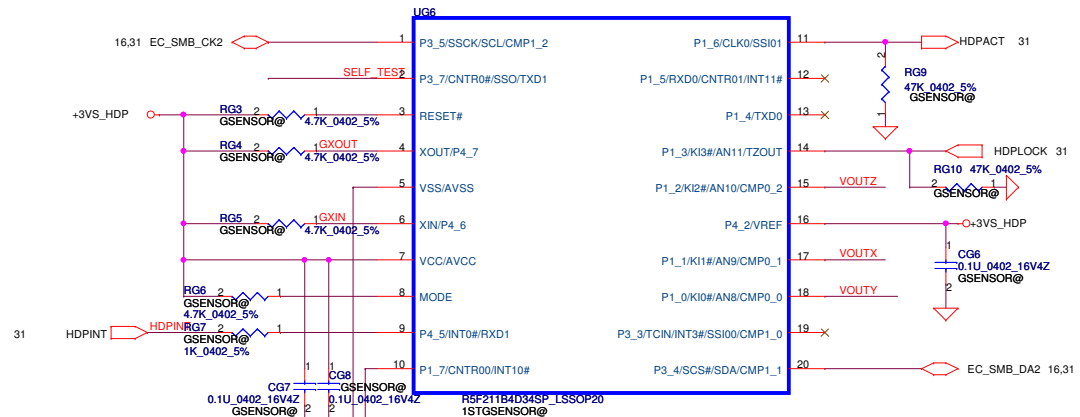
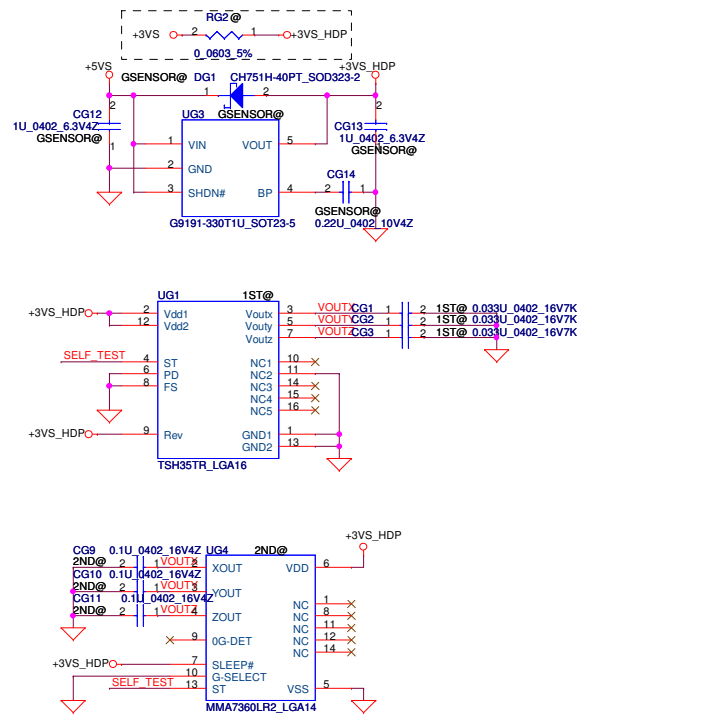


LPC Debug Port

Please place the PAD under DDR DIMM.

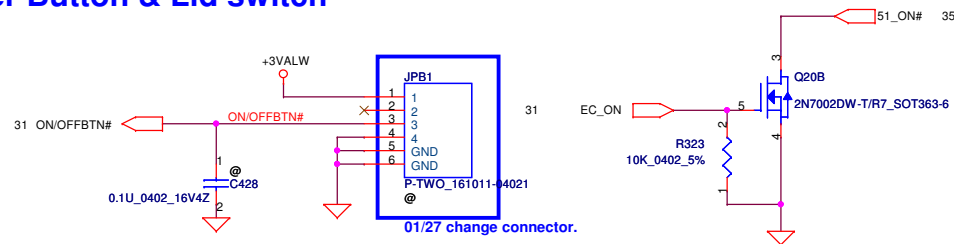


G-Sensor

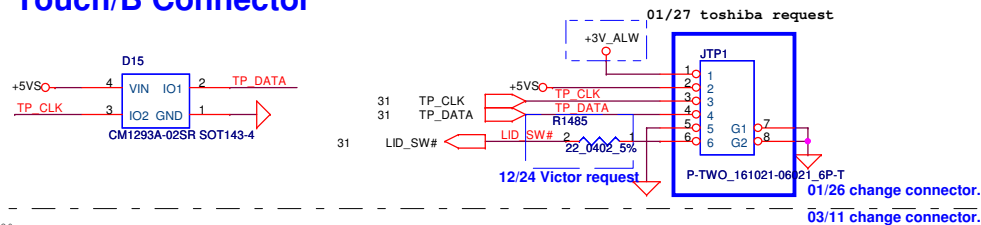


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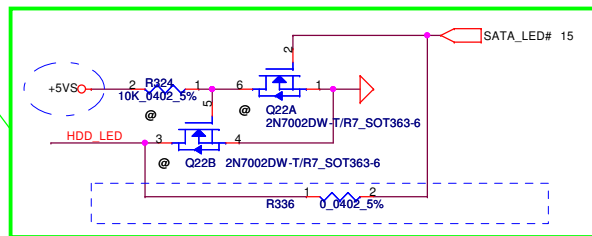
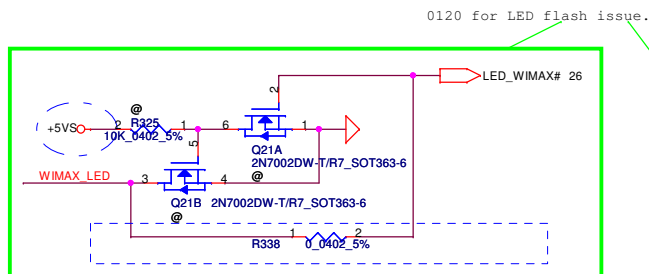
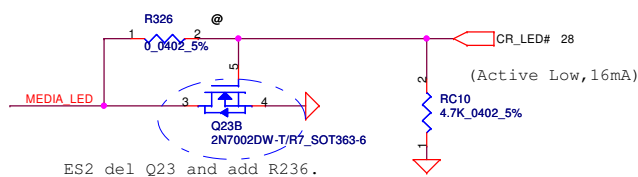
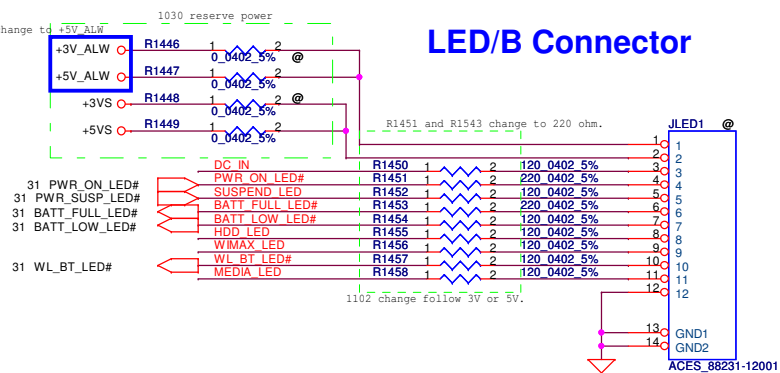
Power Button & Lid switch



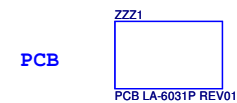
Touch/B Connector



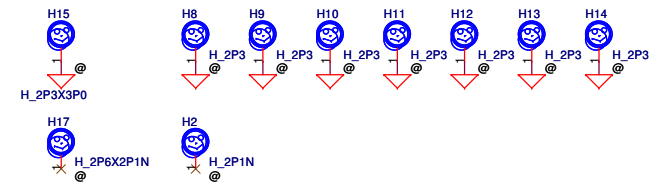
LED/B Connector



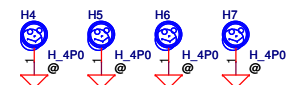
ISPD



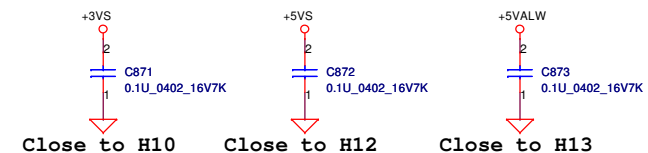
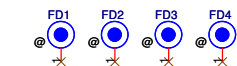
Screw Hole



CPU

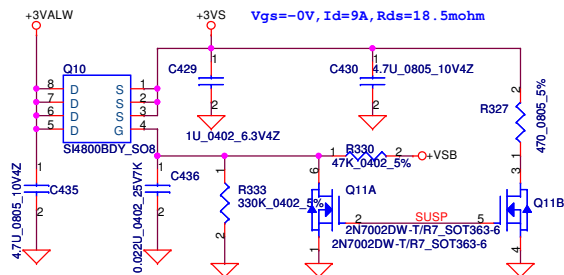


PCB Fedical Mark PAD

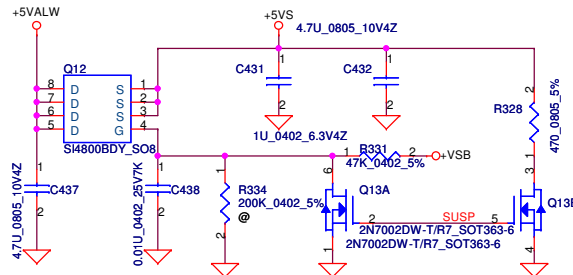


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				Size	Document Number
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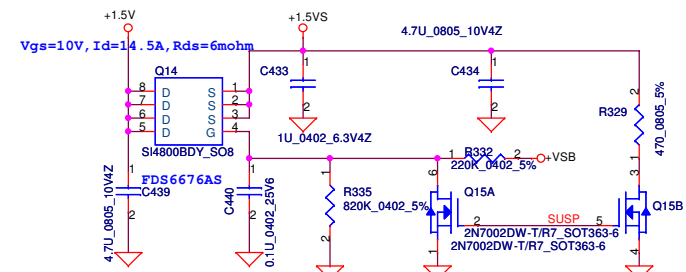
+3VALW TO +3VS



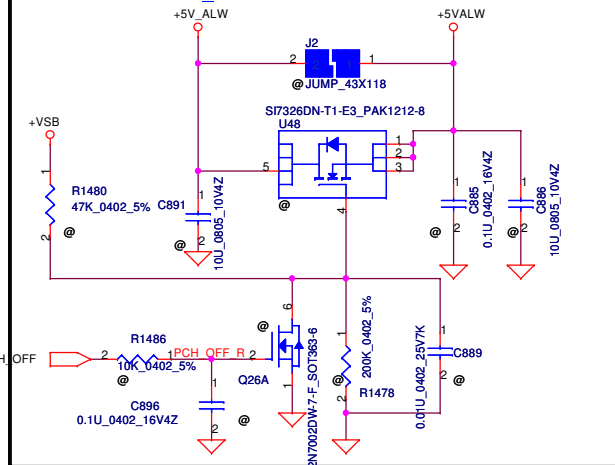
+5VALW TO +5VS



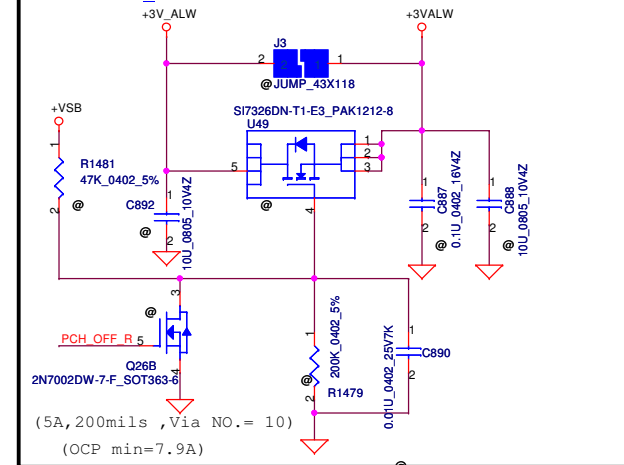
+1.5V to +1.5VS



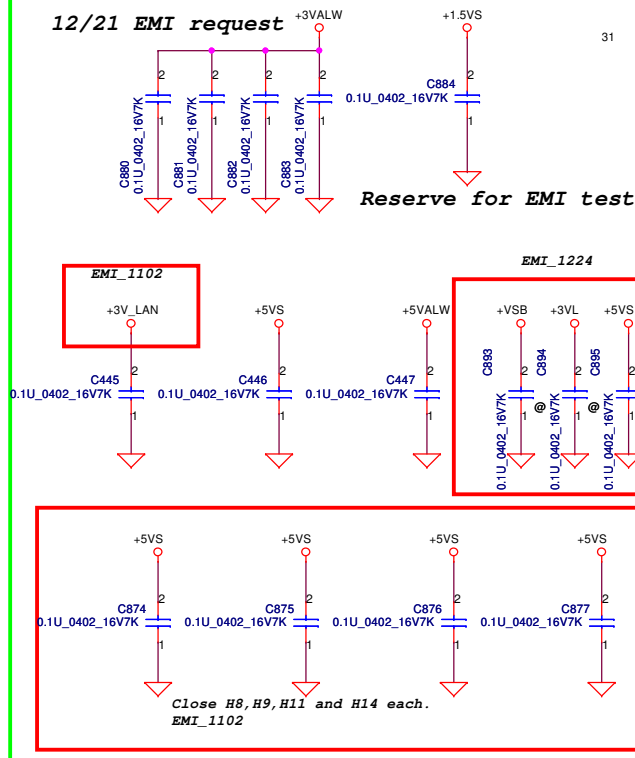
+5V_ALW to +5VALW Transfer



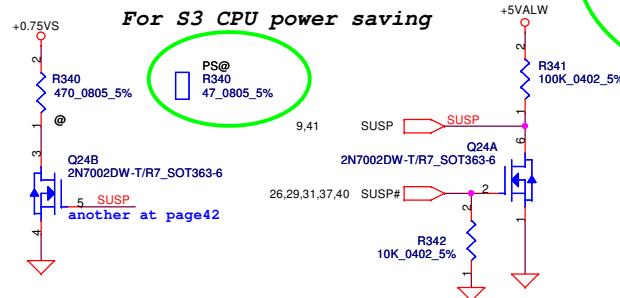
+3V_ALW to +3VALW Transfer



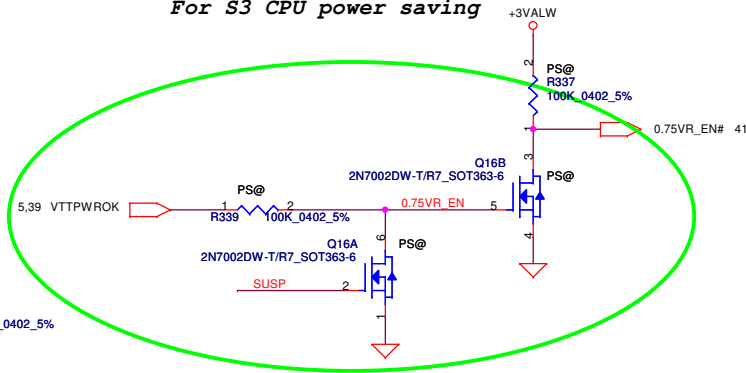
12/21 EMI request



For S3 CPU power saving

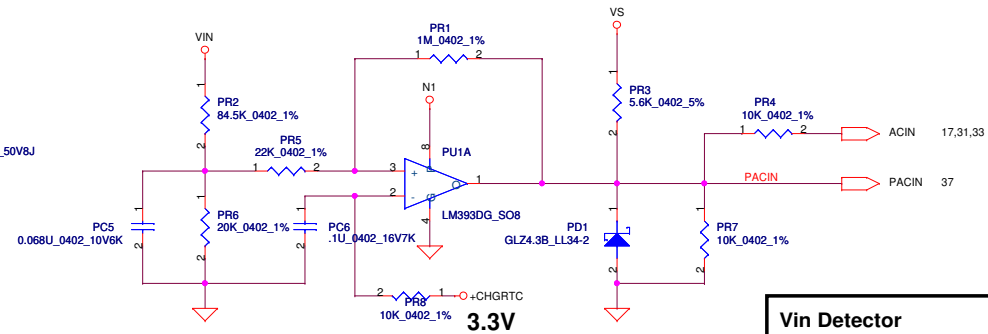
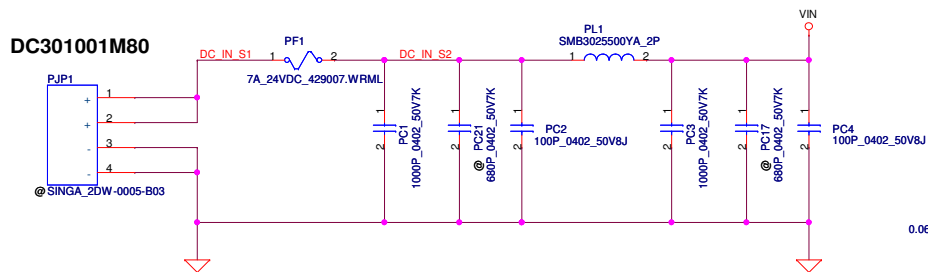


For S3 CPU power saving



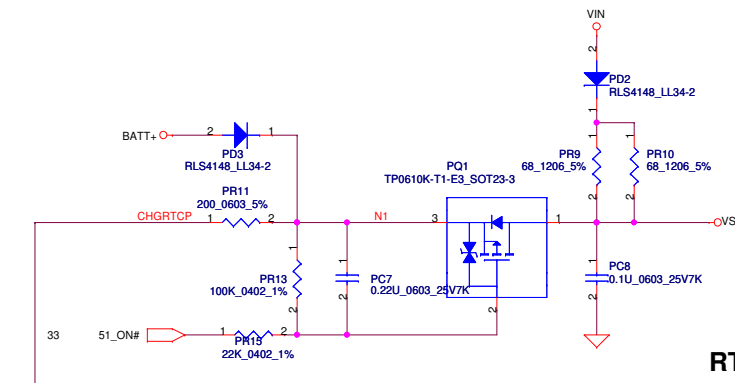
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DC301001M80

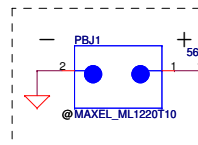


Vin Detector

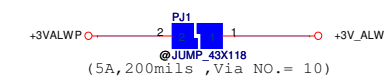
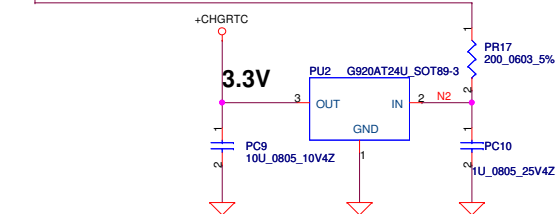
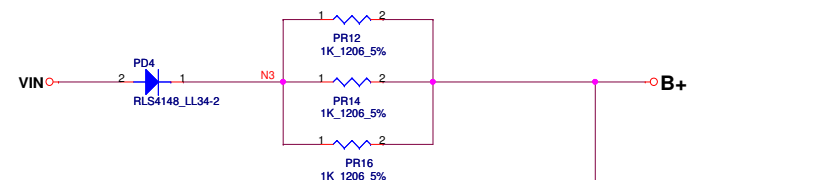
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



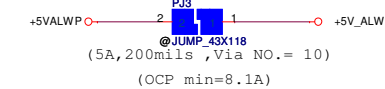
RTC Battery



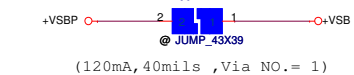
SP093MX0000



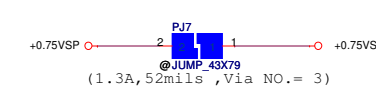
(5A, 200mils, Via NO.= 10)
(OCP min=7.9A)



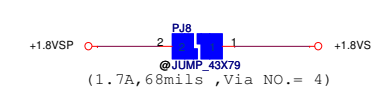
(5A, 200mils, Via NO.= 10)
(OCP min=8.1A)



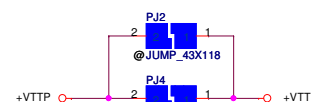
(120mA, 40mils, Via NO.= 1)



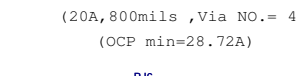
(1.3A, 52mils, Via NO.= 3)



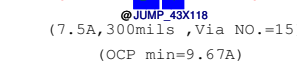
(1.7A, 68mils, Via NO.= 4)
(OCP min=3A)



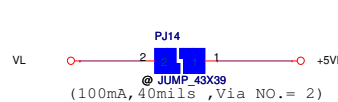
(20A, 800mils, Via NO.= 40)
(OCP min=28.72A)



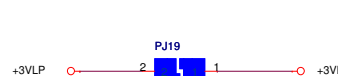
(7.5A, 300mils, Via NO.=15)
(OCP min=9.67A)



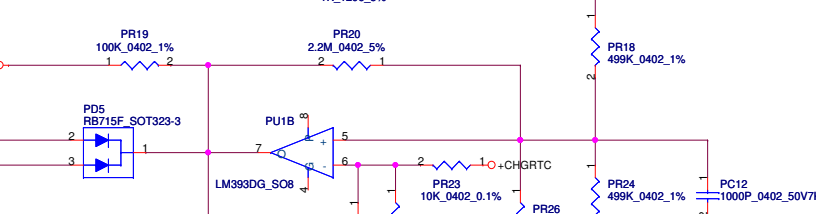
(12A, 480mils, Via NO.=24)
(OCP min=15.6A)



(100mA, 40mils, Via NO.= 2)



(100mA, 40mils, Via NO.= 2)

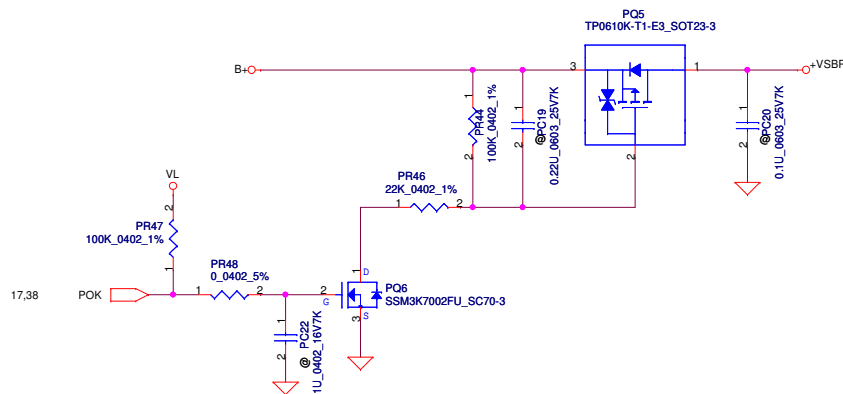
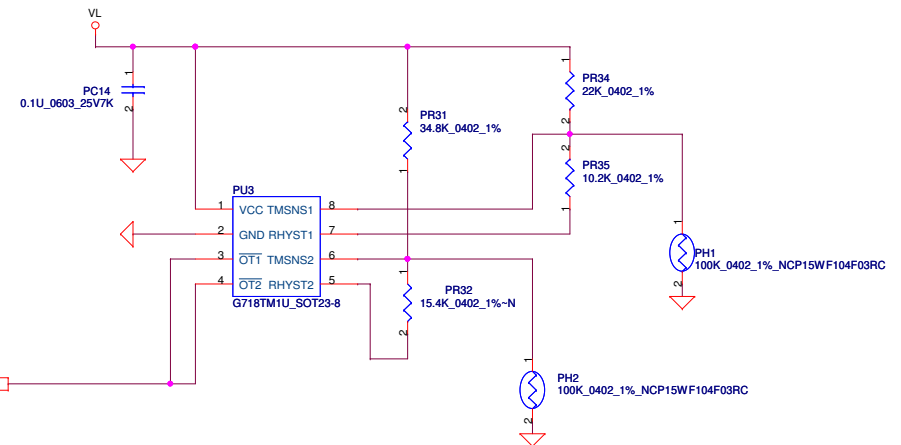
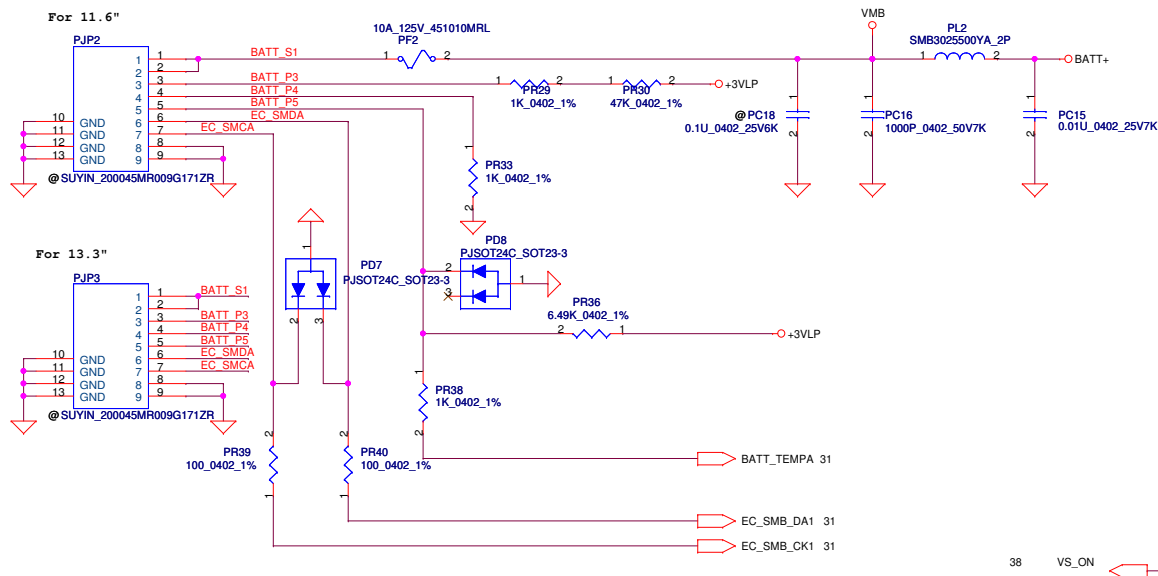


Precharge detector 15.97V/14.84V FOR ADAPTOR

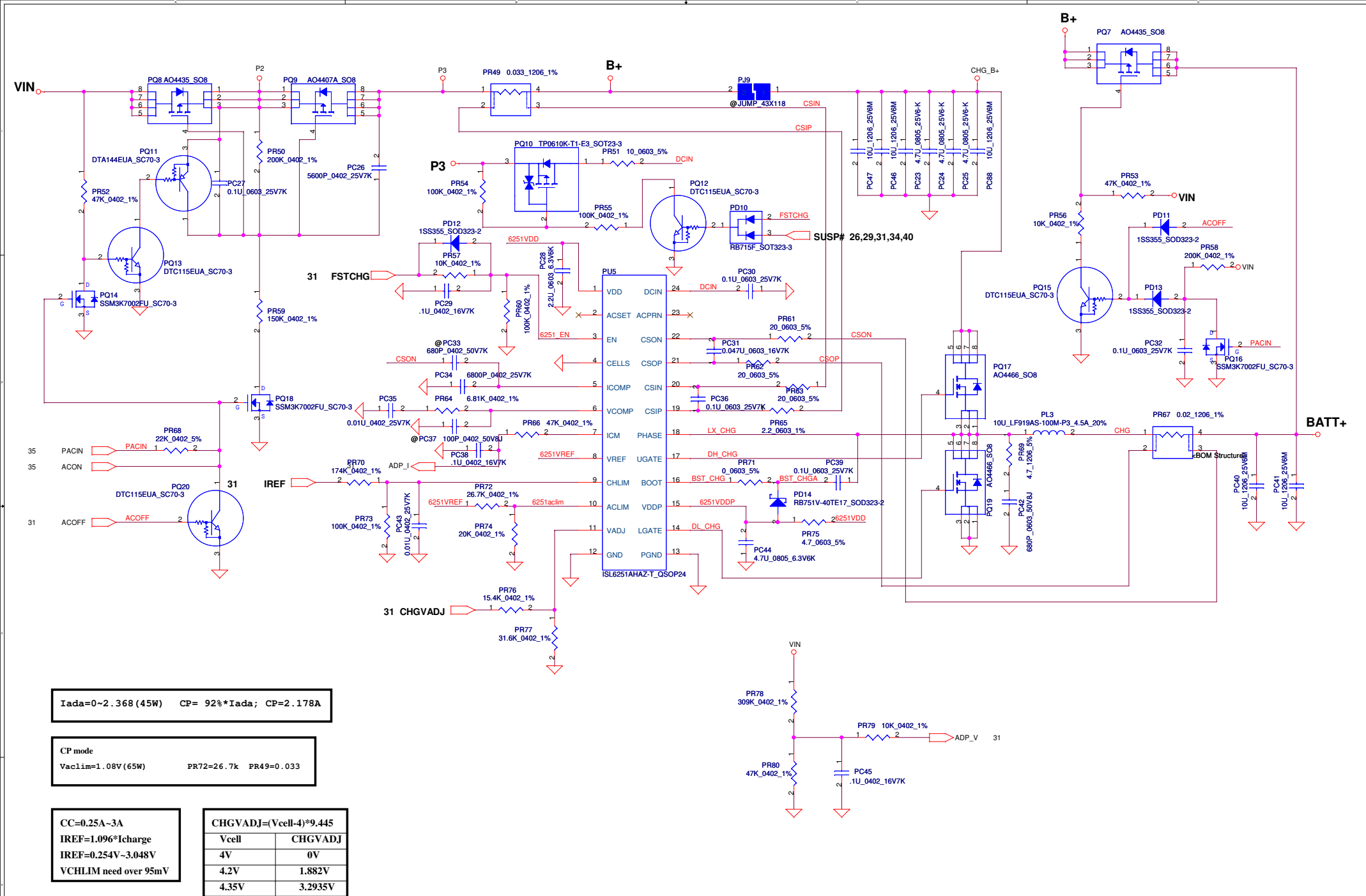
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PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

PH2 near main battery CONN:
 BAT.thermal protection at 78 degree C
 Recovery at 42 degree C



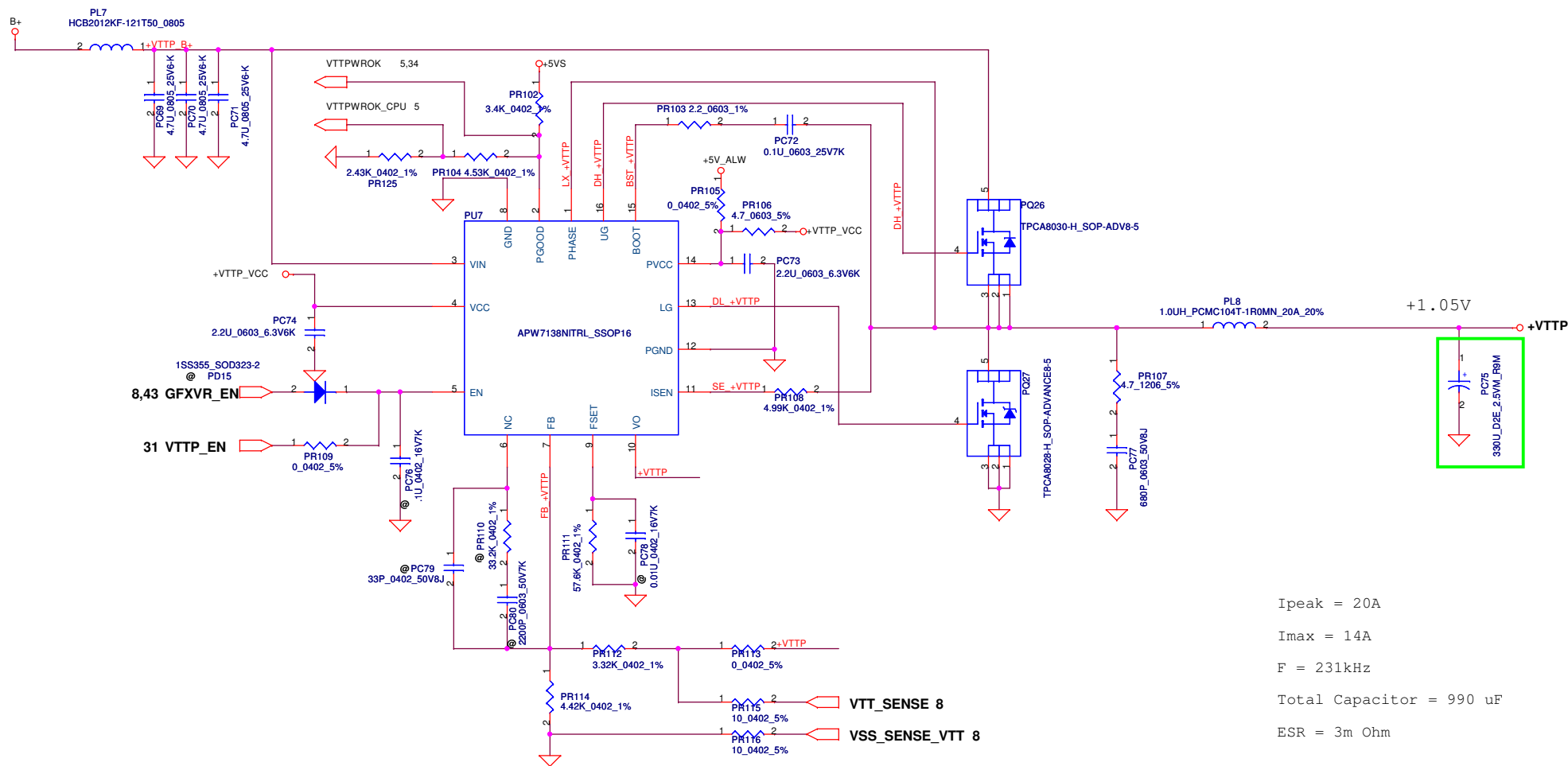
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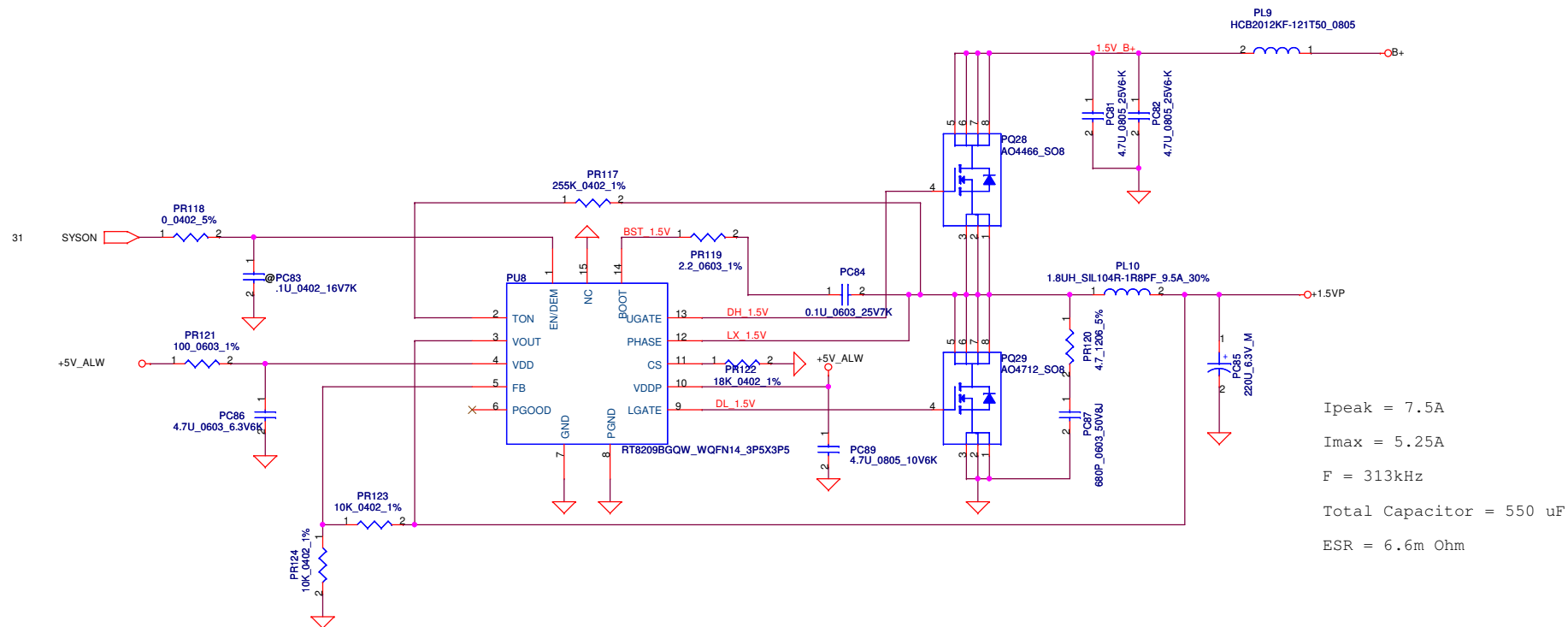
Ipeak = 5A
Imax = 3.5A
F = 305kHz
Total Capacitor = 150 uF
ESR = 18m Ohm

Ipeak = 5A
Imax = 3.5A
F = 245kHz
Total Capacitor = 150 uF
ESR = 18m Ohm

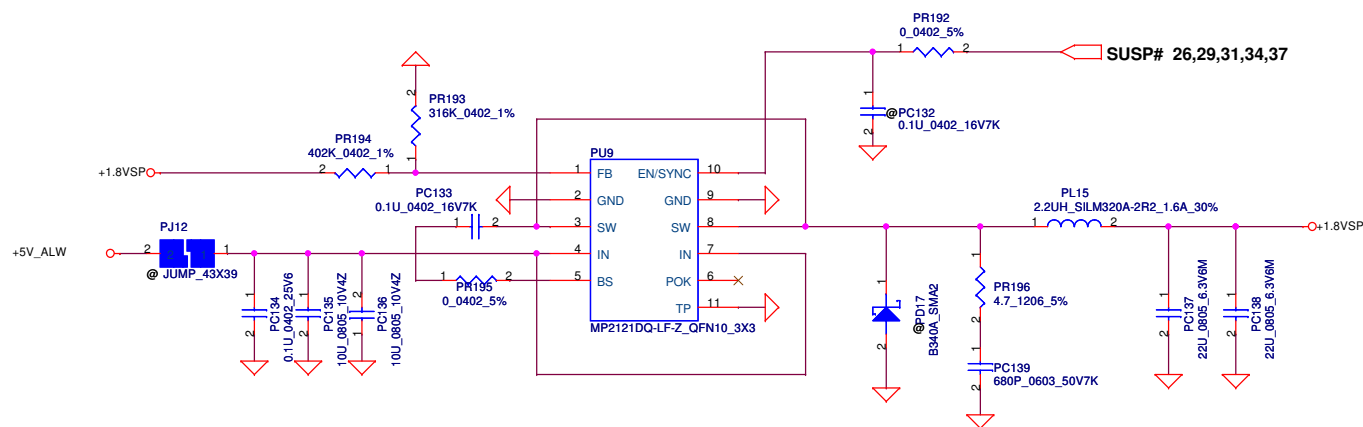
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								Size	Document Number						Rev 1.
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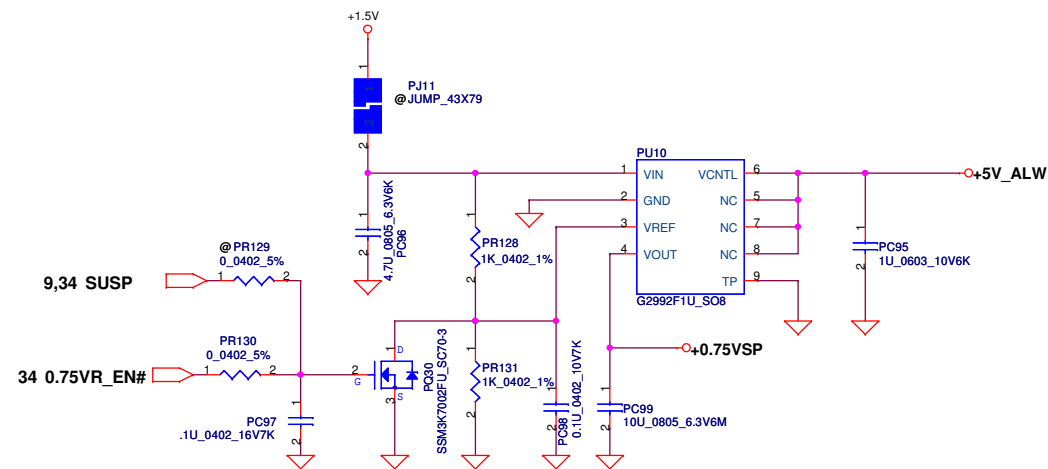


Ipeak = 7.5A
 Imax = 5.25A
 F = 313kHz
 Total Capacitor = 550 uF
 ESR = 6.6m Ohm



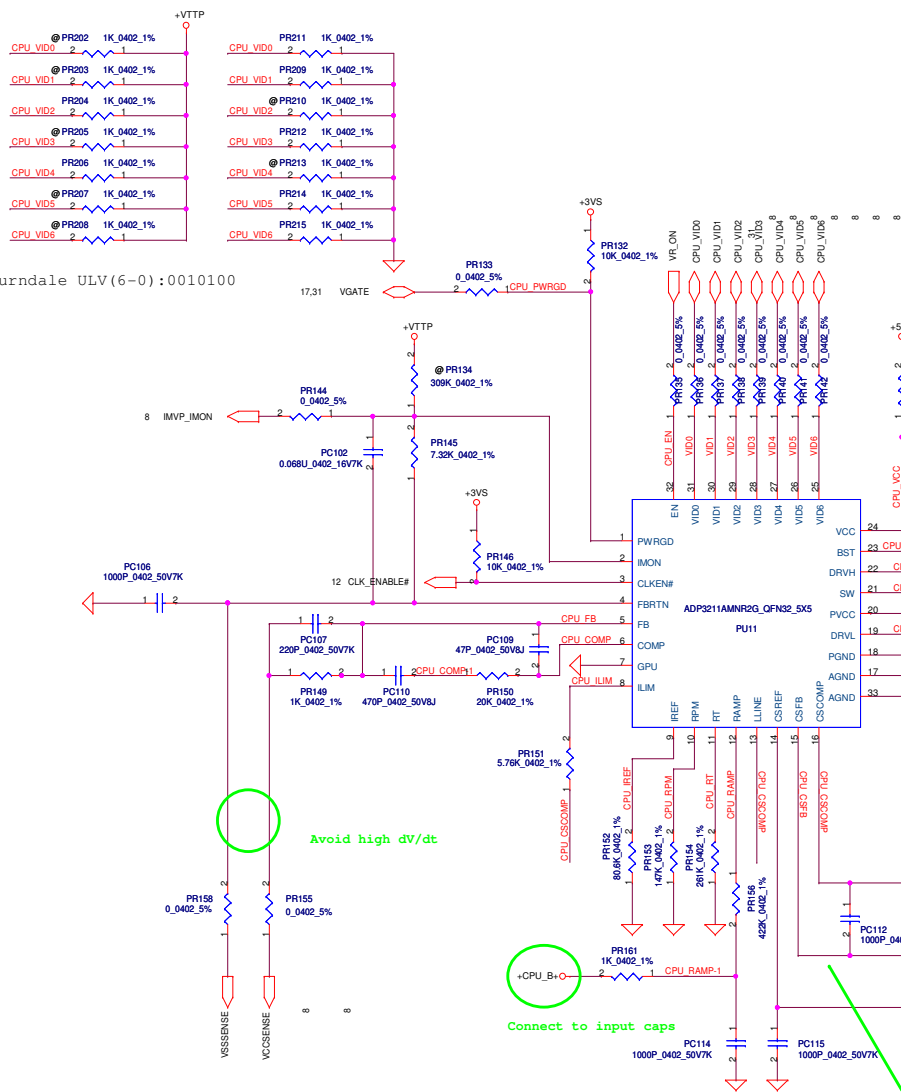
Ipeak = 1.7A
 Imax = 5.25A
 F = 1.5MHz
 Total Capacitor = 44 uF
 ESR = 2.5m Ohm

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								0.75VSP			
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Anburndale ULV(6-0):0010100



Ipeak = 27A
 Imax = 18.9A
 F = 350kHz
 Total Capacitor = 1320 uF
 ESR = 2.25m Ohm

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104KM8 to SE076104K80	change to A5l material
2009/11/9 (EVT)	P39	+VTTP	Resever PD15	Design change
2009/11/9 (EVT)	P41	+0.75VSP	Change PQ30 to SB000009610	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PU11 change to ADP3211	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PH3 &PH4	change to A5l material
2009/11/9 (EVT)	P37	CHARGE	Change PR49 change to 33m	Design change
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
2009/12/1 (DVT)	P39	+CPU-CORE	Add PR202~PR215 pull-up & pull-down	Design change
2009/12/17 (DVT)	P36	Battery	Change PR31,PR32,PR34,PR35	Design change
2009/12/17 (DVT)	P37	CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
2009/12/22 (DVT)	P42	CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P43	GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P39	+VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
2010/01/25 (PVT)	P36	Battery	Add PD7,PD8	EMI require
2010/01/27 (PVT)	P37	CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
2010/02/04 (PVT)	P41	+0.75VSP	Resever PR129 Add PR130 and PC97	Design change
2009/02/04 (PVT)	P38	+5VALWP/+3VALWP	Change PQ38	Design change
2010/02/04 (PVT)	P42	CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
2010/02/08 (PVT-2)	P36	Battery	Change PR21&PR22 and +CHGRIC	Design change

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Issued Date	2010/04/12	Deciphered Date	2010/10/02	Title		
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C878, R8, R40 and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPDI circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN soft	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damage when insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add two ALW power transfer circuits (3V_ALW to 3VALW & 5V_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRS LPVR pull up 1k ohm to VIT	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SW# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24,31	Add R1487,R1488,R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change cardreader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5, and add L1C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH(U8)		layout change	03/04	PVT2
38	Change O2 to JMicon card reader.	28		03/22	PVT2
39	USB OC# change	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2