

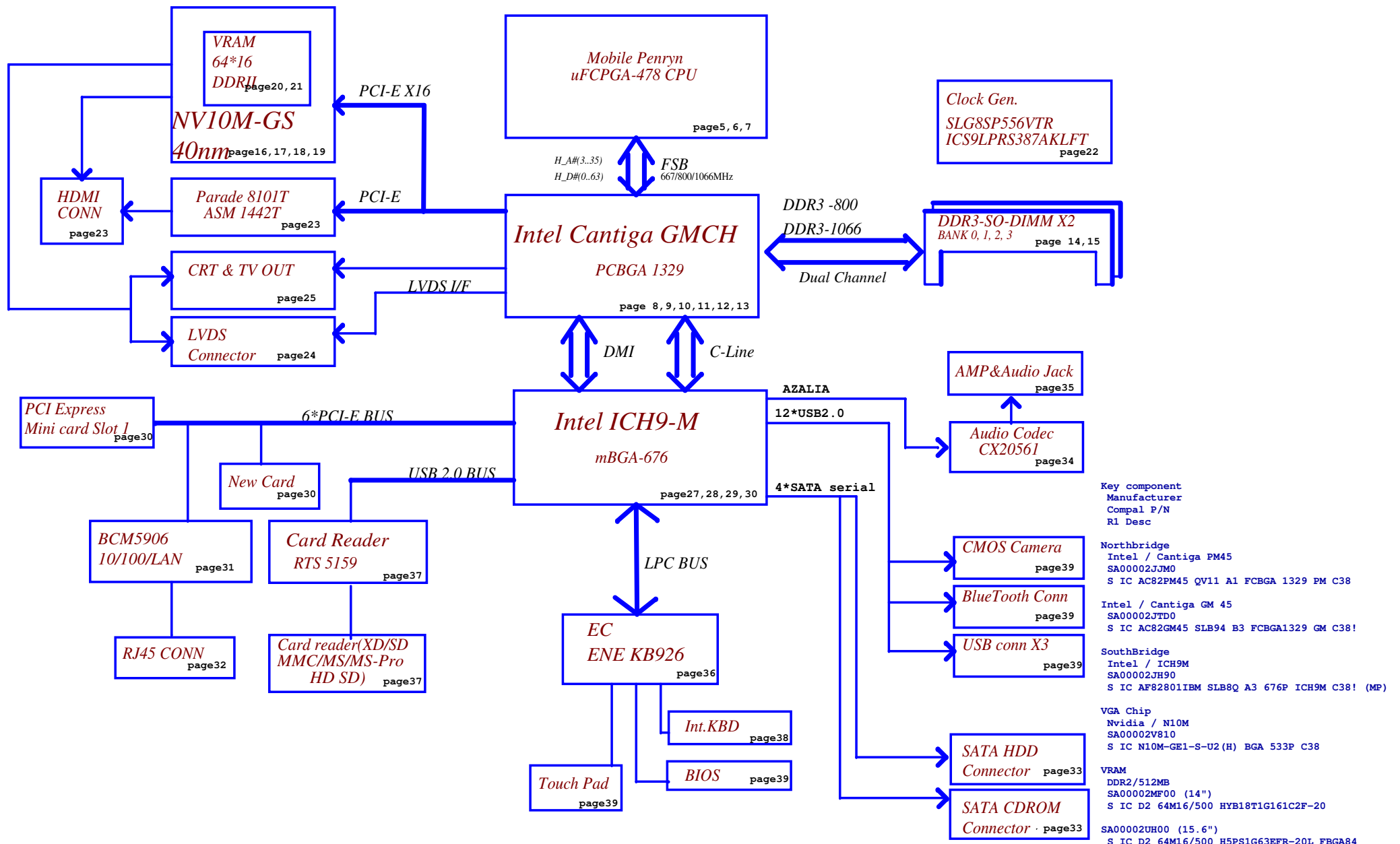
KIWA5/A6

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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				Custmr		

DDR3 Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCCP +CPU_CORE +VGA_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICKL_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	N10M	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	N10M	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT (55nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	N10M	X	X	X	V	X	X	X	X	X	X	X	X	X
IFPC_AUX IFPC_AUX_N (40nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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VGA and DDR2 Voltage Rails (N10M)

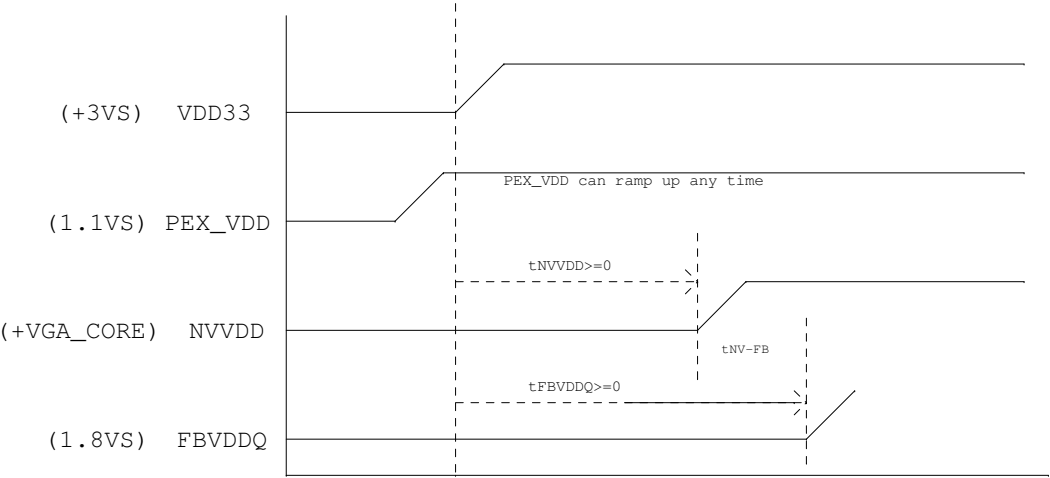
State \ power plane	+3VS +VGA_CORE +1.1VS +1.8VS
S0	○
S1	○
S3	✗
S5 S4/AC	✗
S5 S4/ Battery only	✗
S5 S4/AC & Battery don't exist	✗

EDP at Tj = 97C*

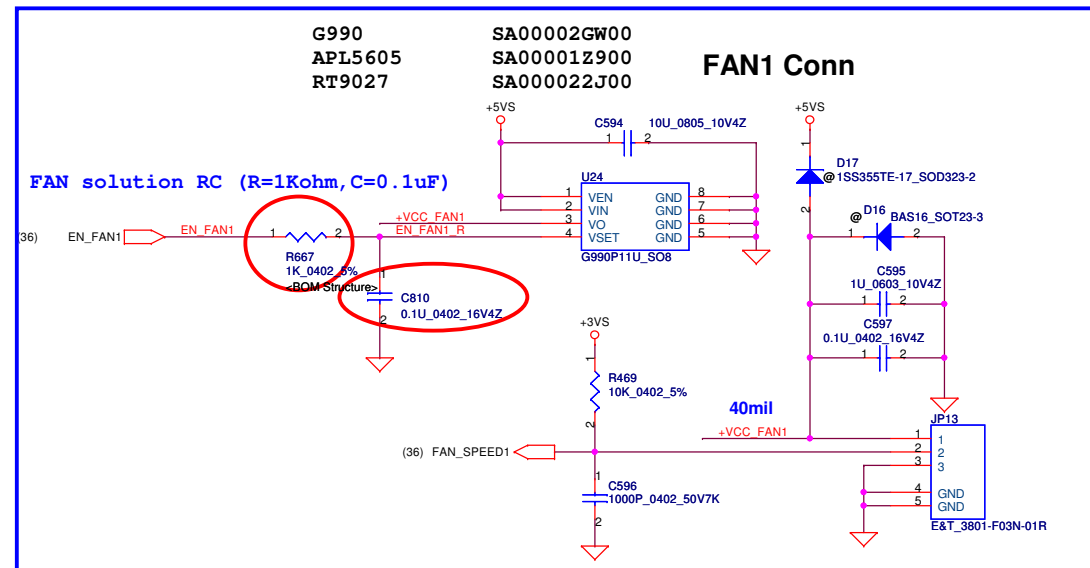
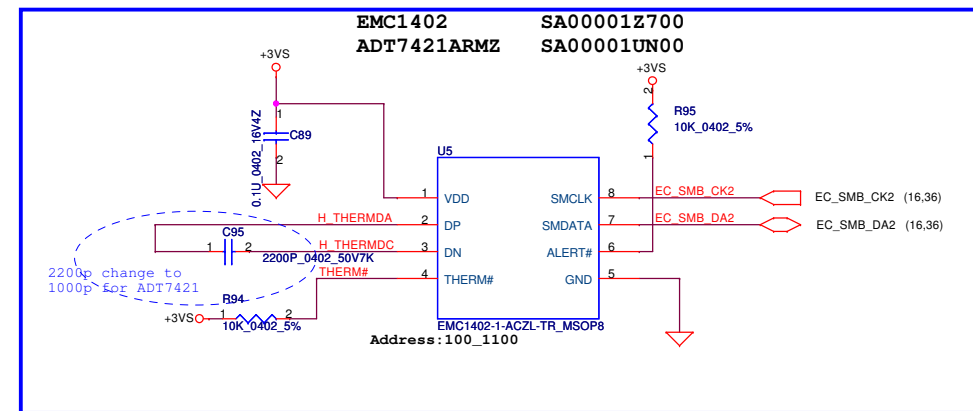
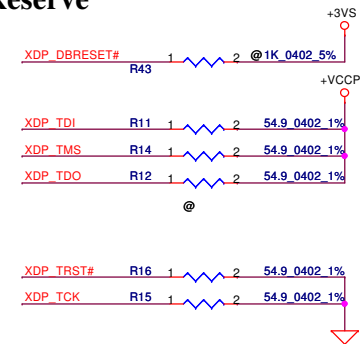
Power Supply Rail (V)		NB10M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SEQUENCE

The ramp time for any rail must be more than 40us



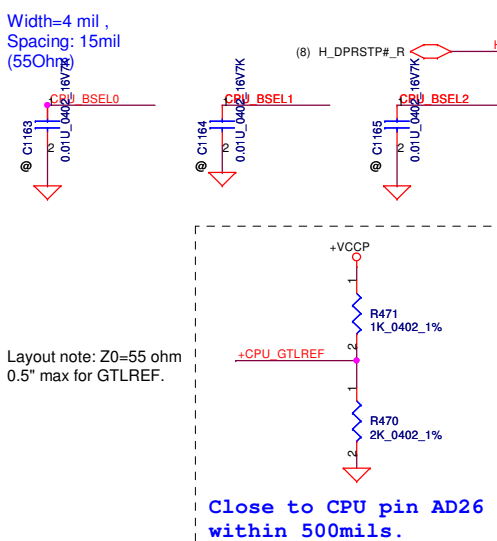
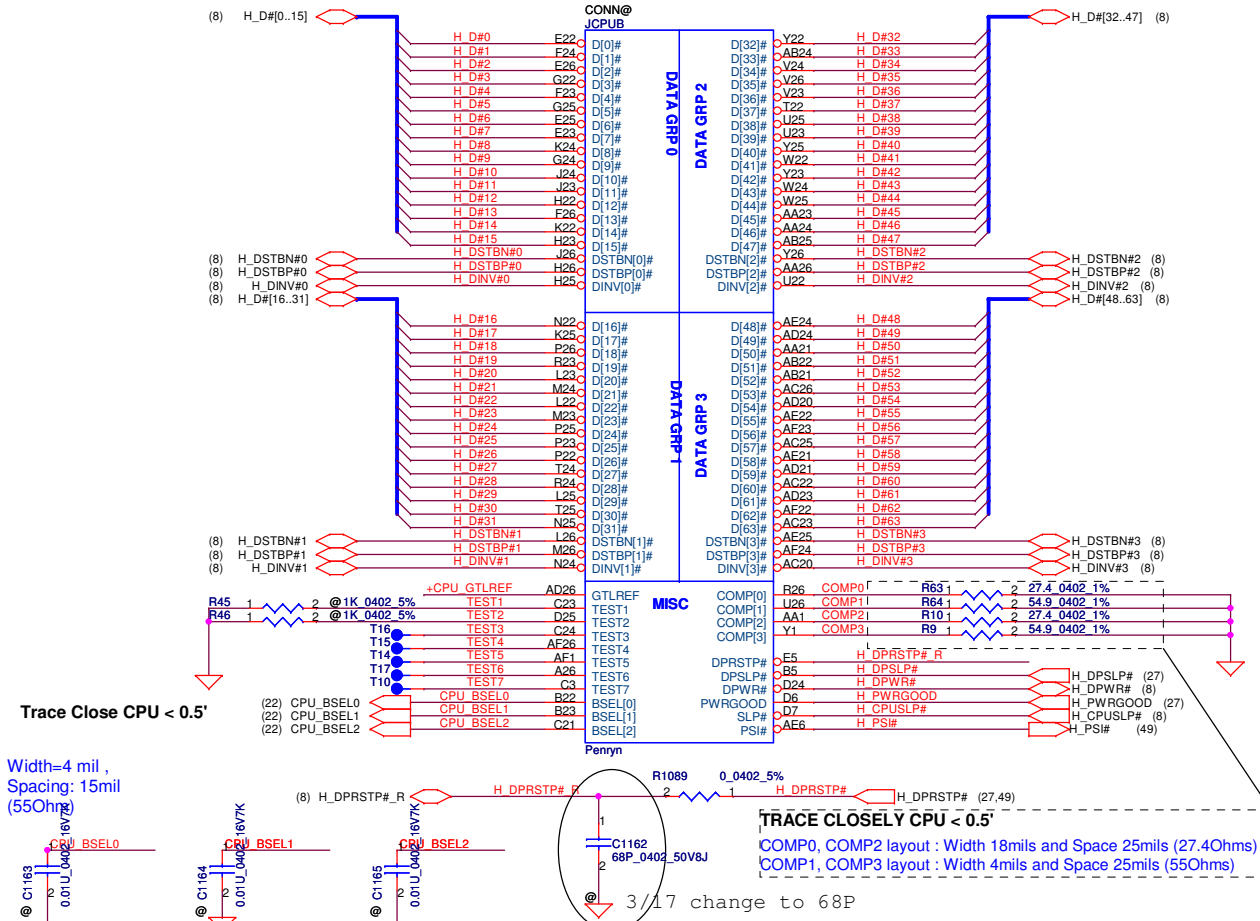
XDP Reserve



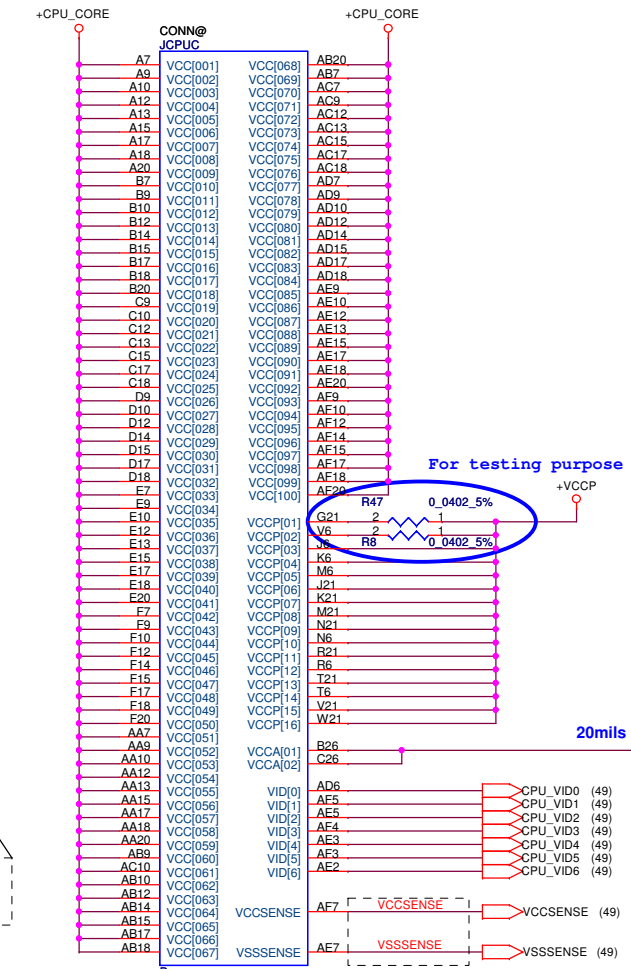
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

RSVD pins on the CPU
should be left as NO
CONNECT

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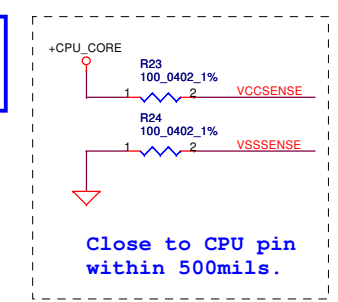


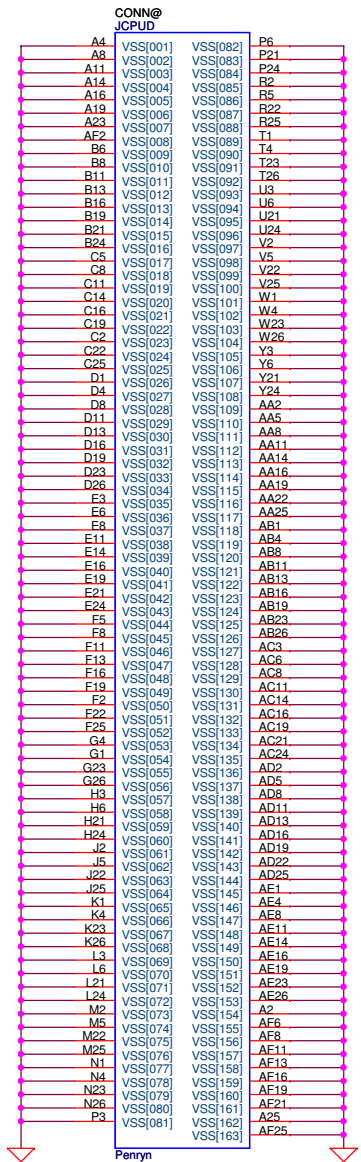
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



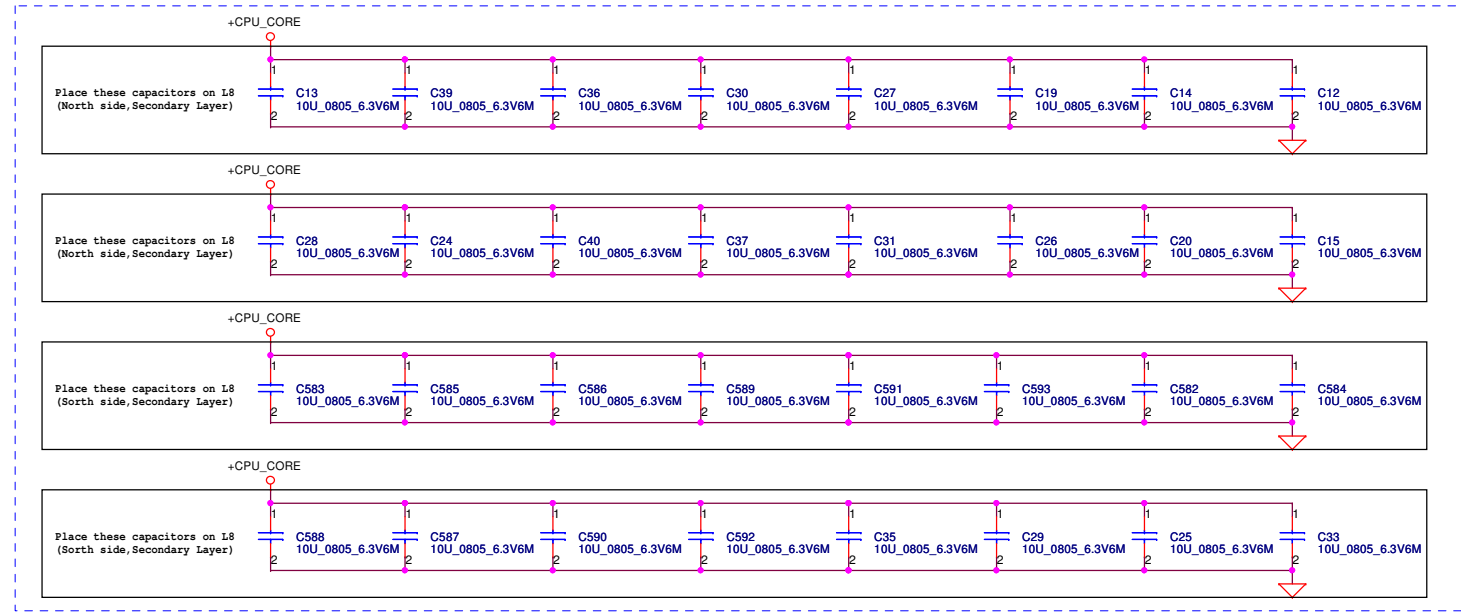
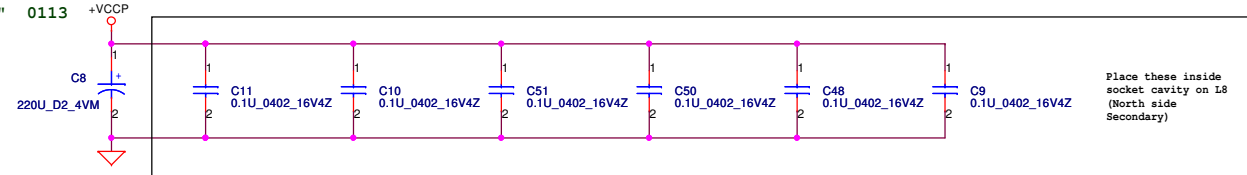
Length match within 25 mils.
The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

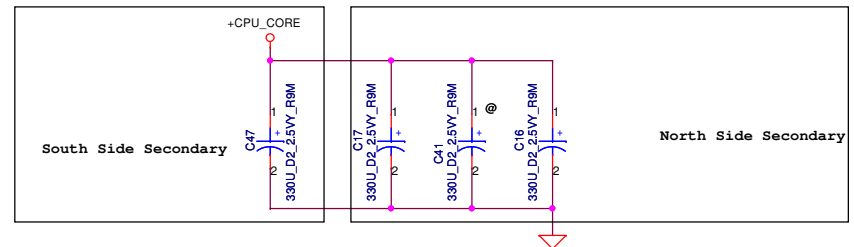




Delete "REMOVE?" 0113

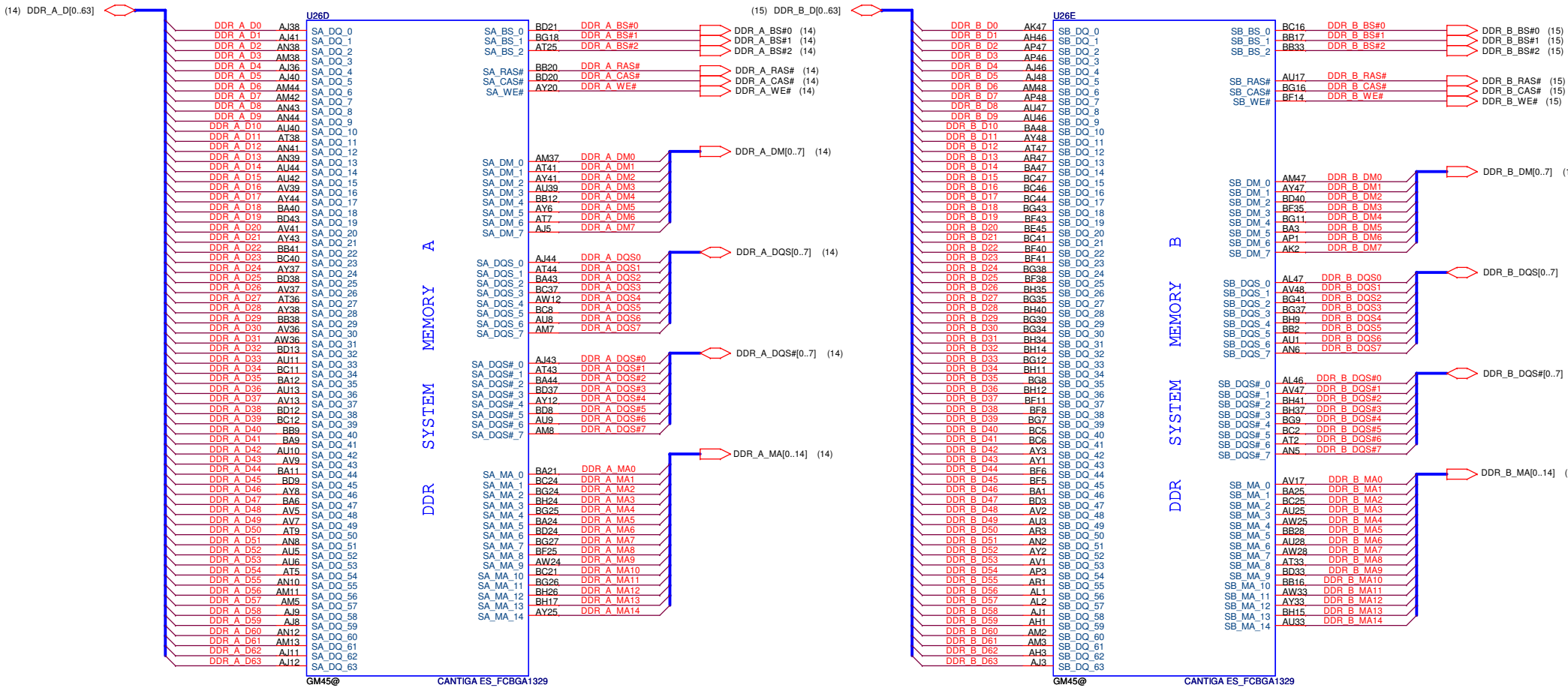


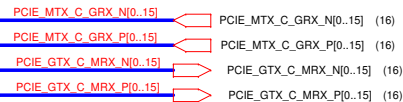
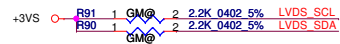
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

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Place the resistor within 500mils (1.27mm) of the (GMCH)

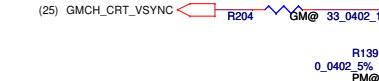
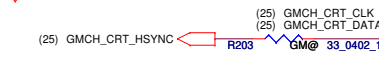
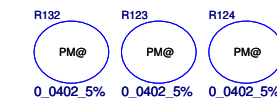
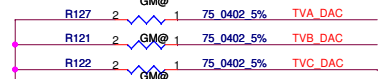
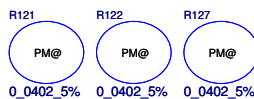
PEGCOMP trace width and spacing is 20/25 mils.

Please check Power source if want support IAMT

For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

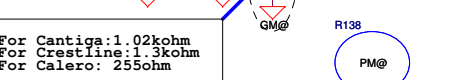
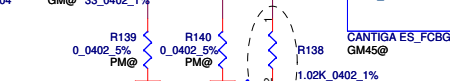
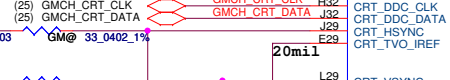
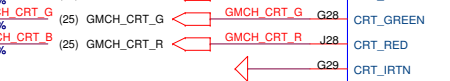
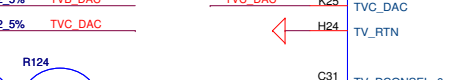
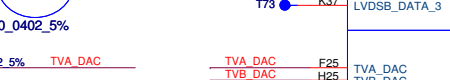
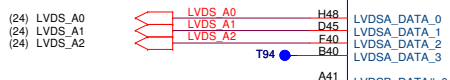
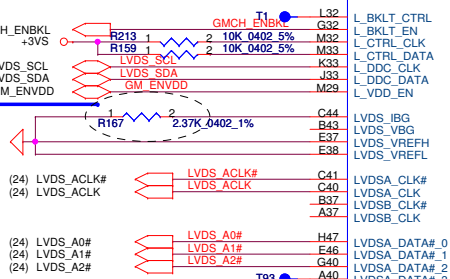
Layout Note: Place 150 Ohm termination resistors close to GMCH



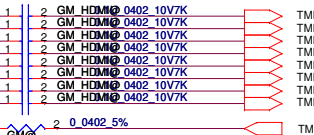
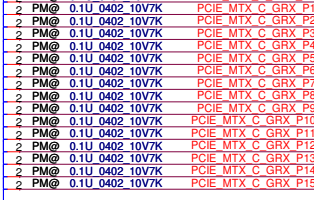
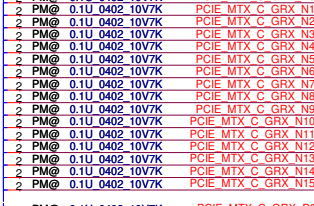
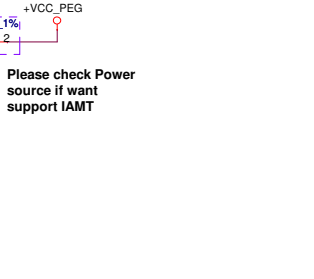
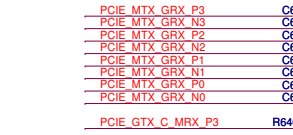
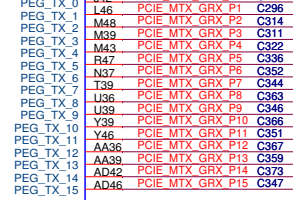
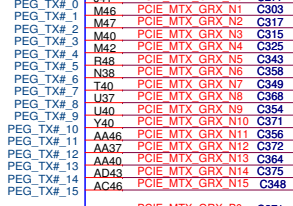
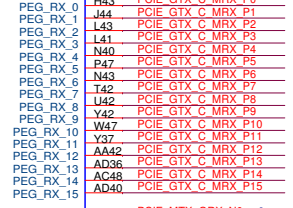
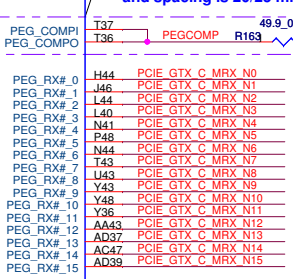
For Cantiga: 1.02kohm
For Crestline: 1.3kohm
For Calero: 255ohm



U26C

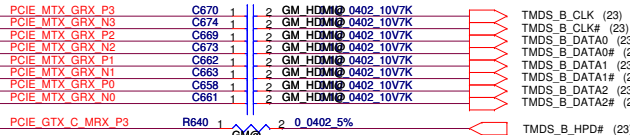


LVDS
PCI-EXPRESS
VGA



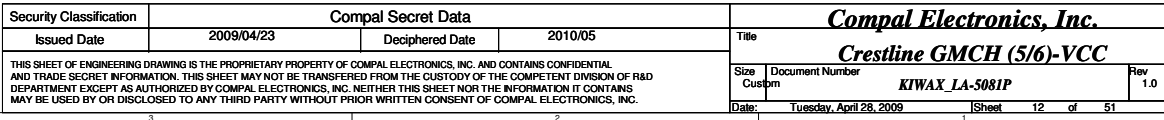
Strap Pin Table

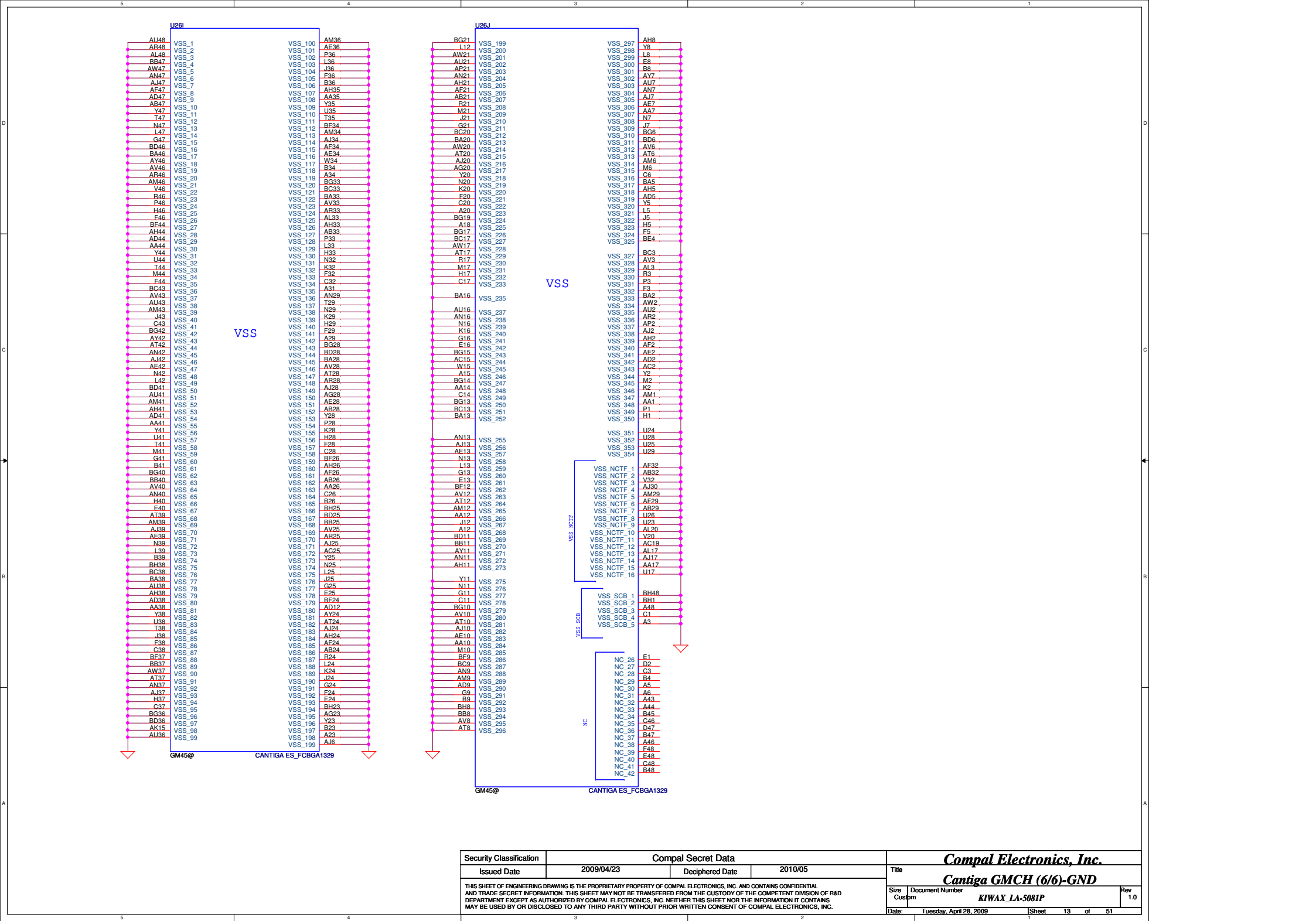
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *



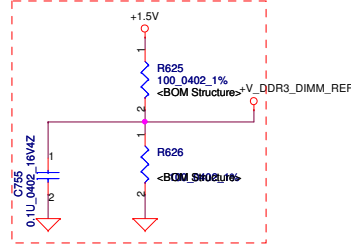
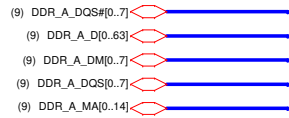
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Compal Electronics, Inc.	
Cantiga GMCH (3/6)-VGA/LVDS/TV	
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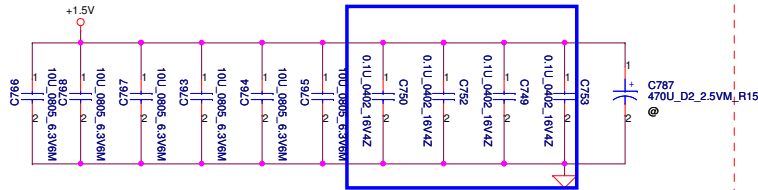


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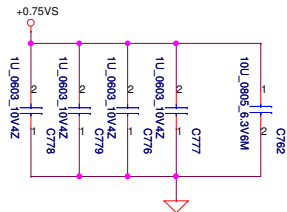


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

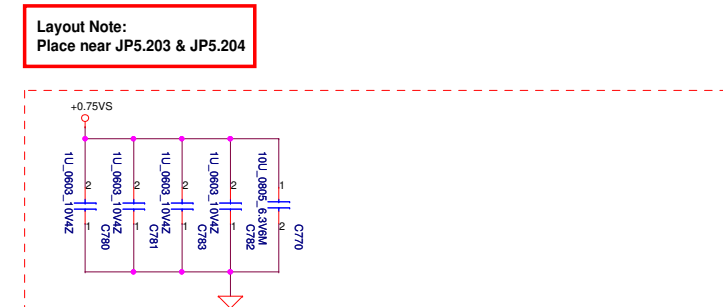
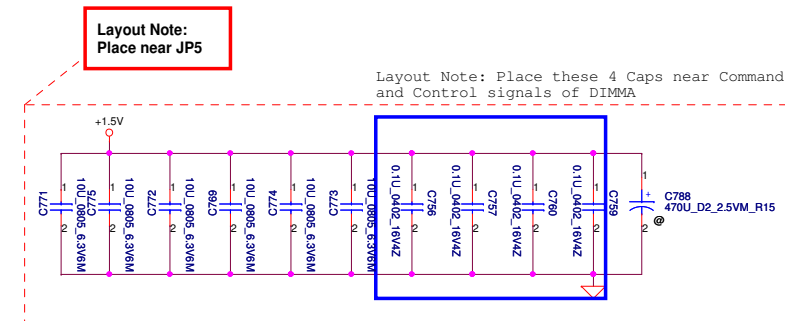
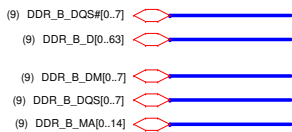


Layout Note:
Place near JP4.203 & JP4.204

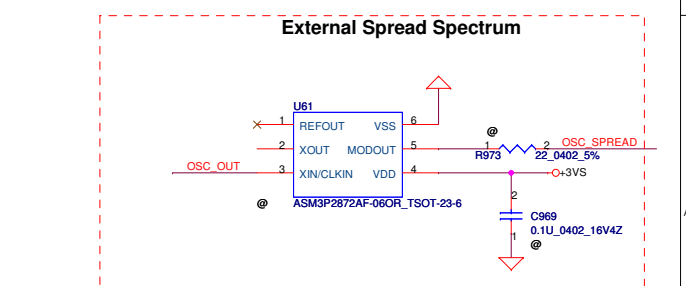
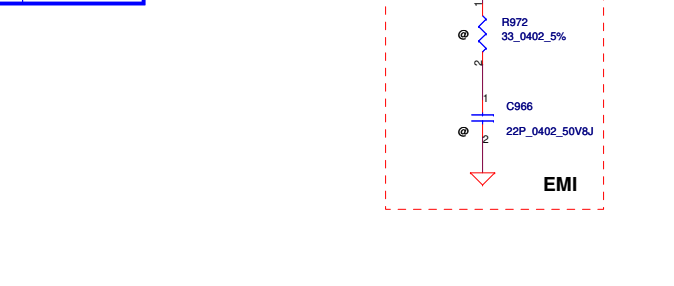
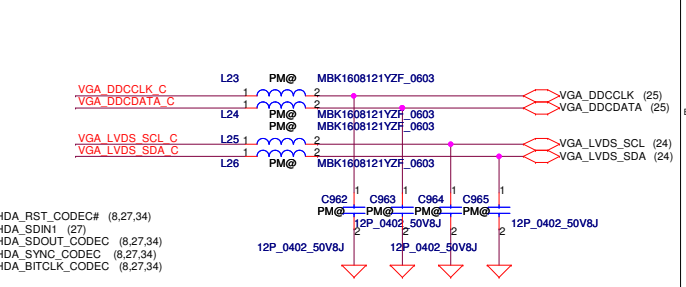
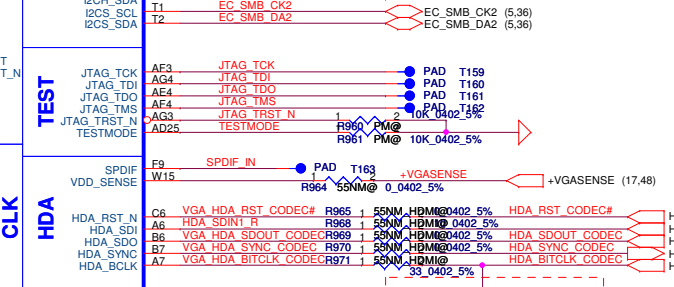
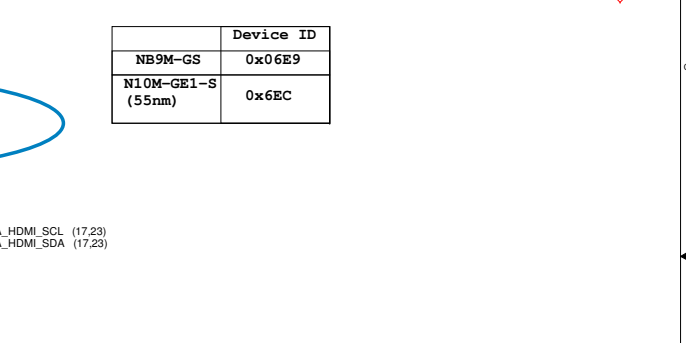
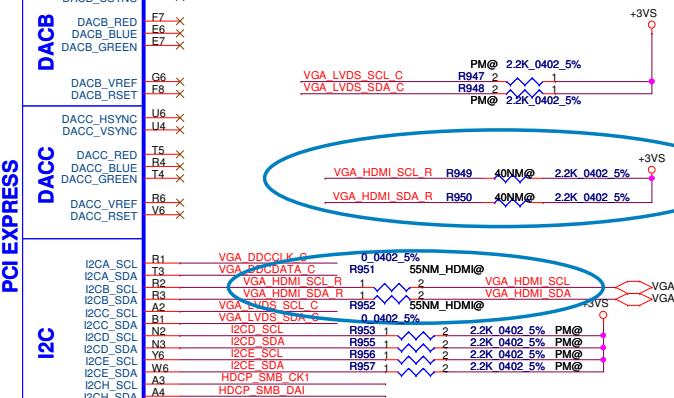
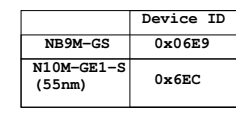
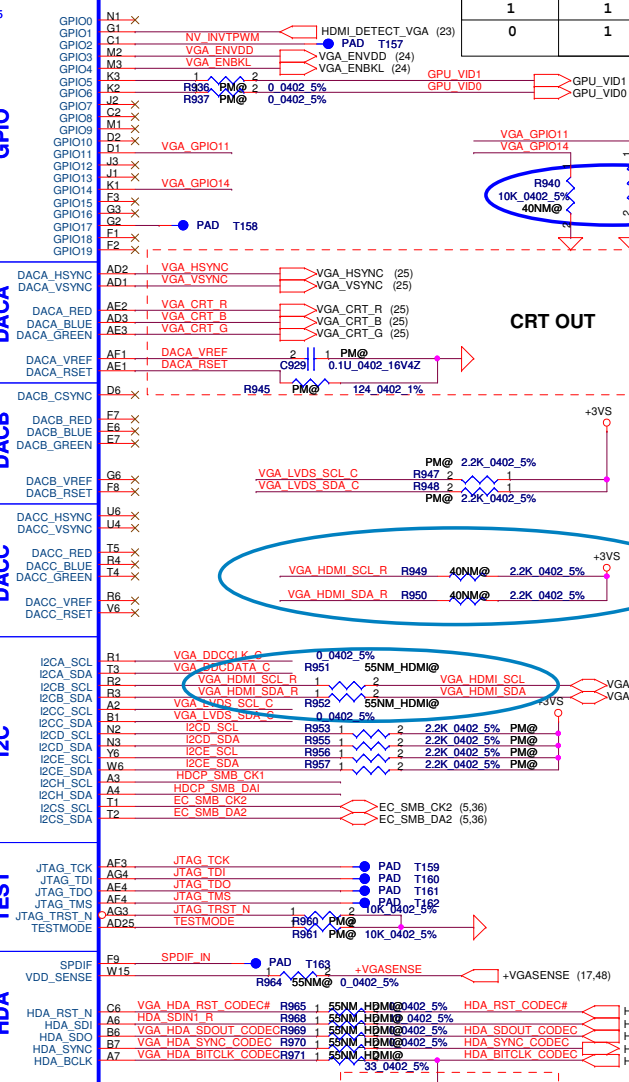


DDR3 SO-DIMM A REVERSE

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Size		Document Number		Rev	
Custor		KIWAX JA-5081P		1.0	
Date		Tuesday, April 28, 2009		Sheet 14 of 51	

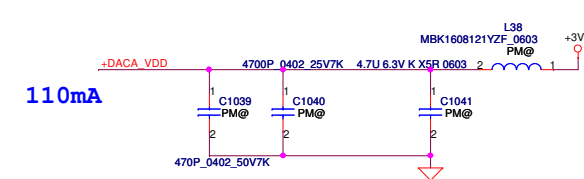
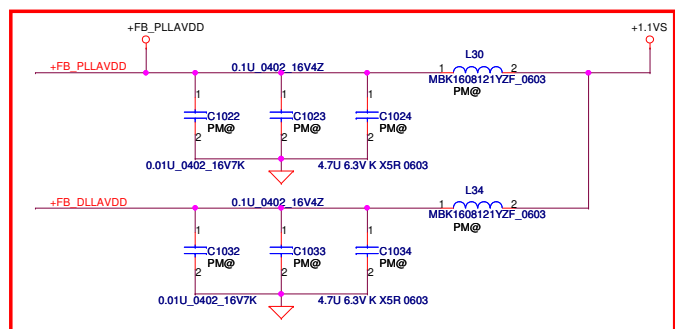
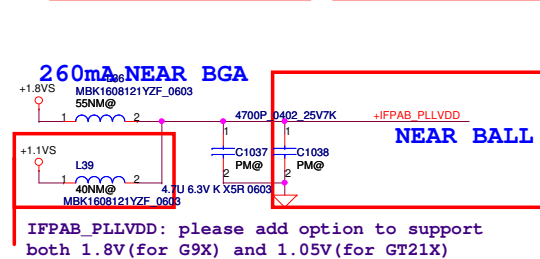
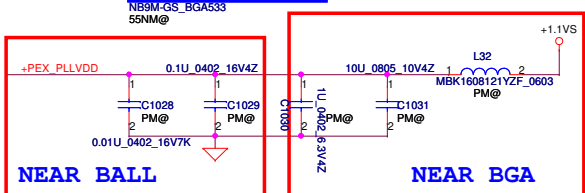
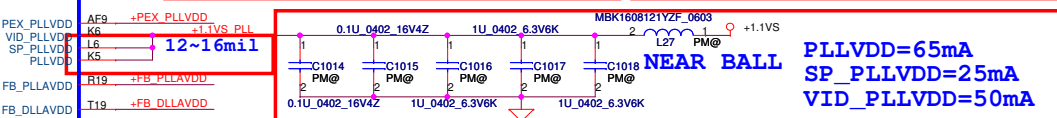
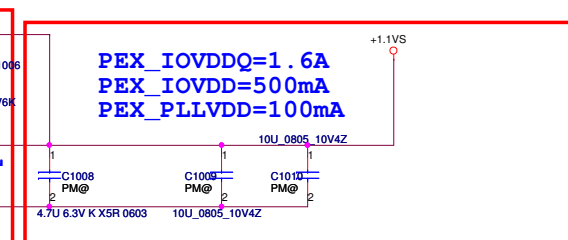
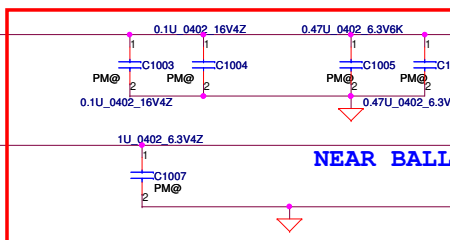
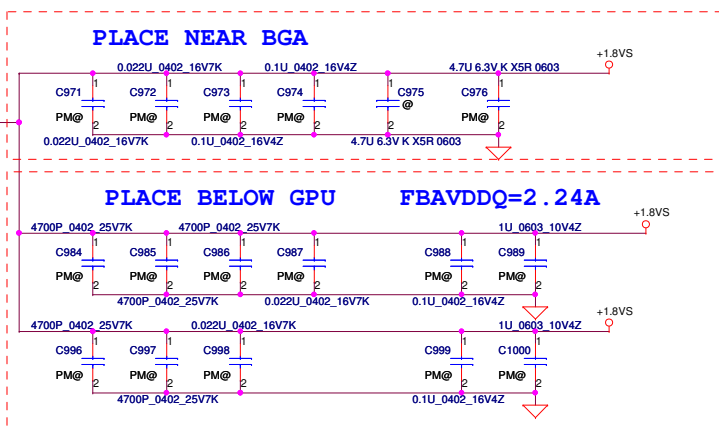
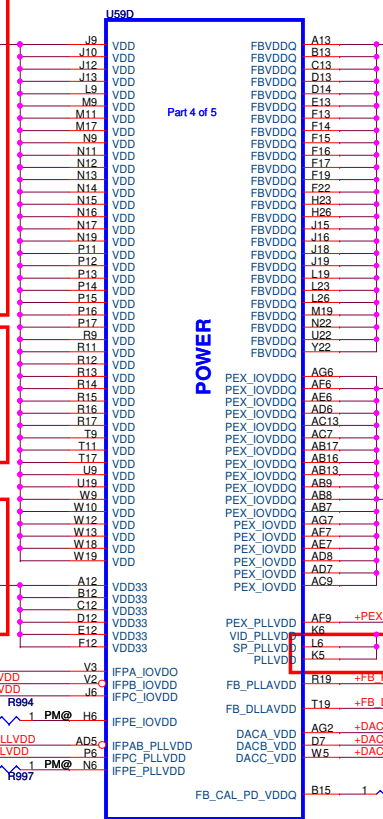
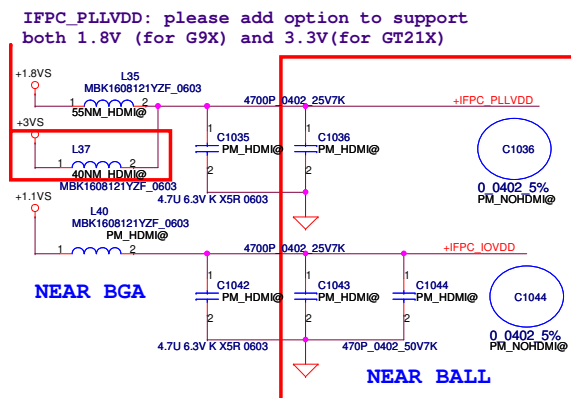
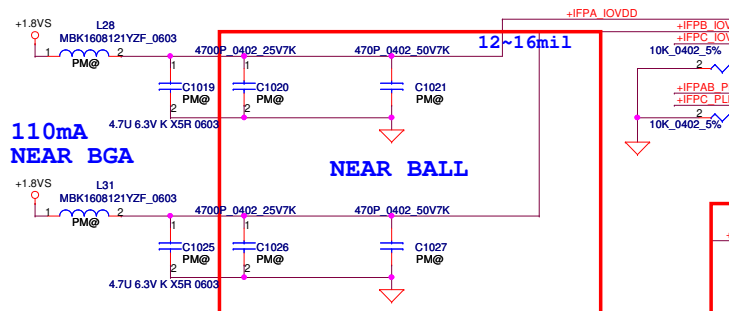
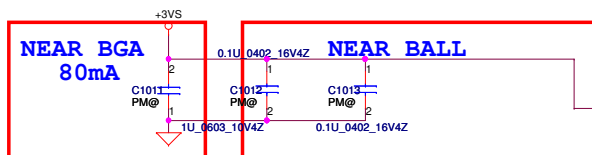
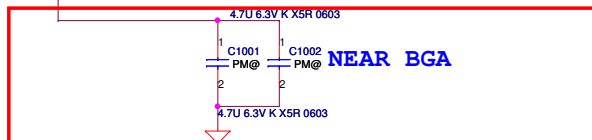
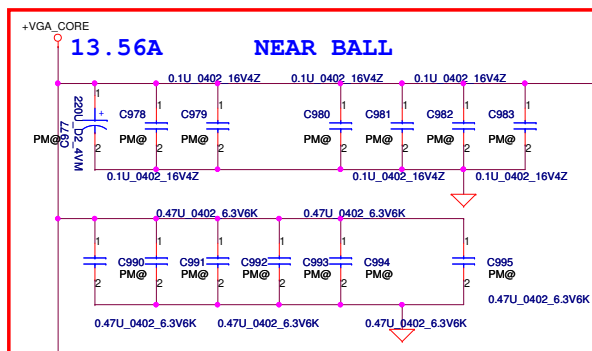


Security Classification	Compal Secret Data			Compal Electronics, Inc. DDRIII-SODIMM SLOT2		
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					KIWX_LA-5081P	1.0
				Date:	Tuesday, April 28, 2009	Sheet 15 of 51



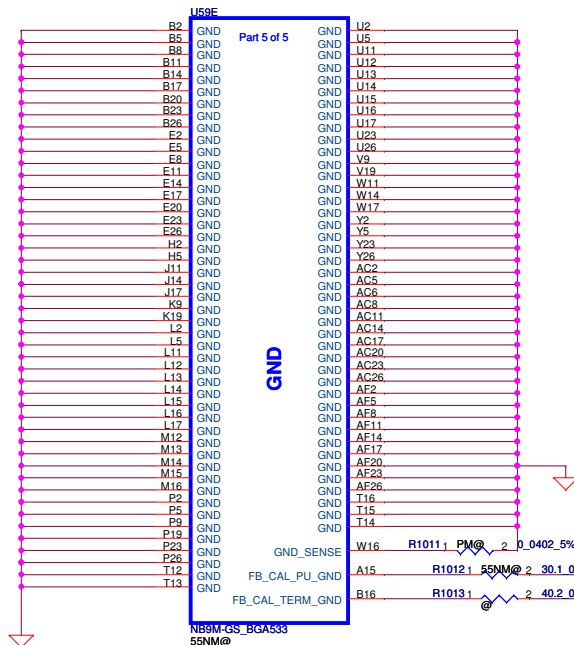
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Issued Date	2009/04/23	Deciphered Date	2010/05	Title	
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				Date: Tuesday, April 28, 2009	Rev 1.0 Sheet 16 of 51

FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS



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				NB10M Power		
				Size Custom	Document Number KIWA5/6 LA-5081P	Rev 1.0
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A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



R148 pop 25K ohm
when use N10M-GE1-S (55nm)

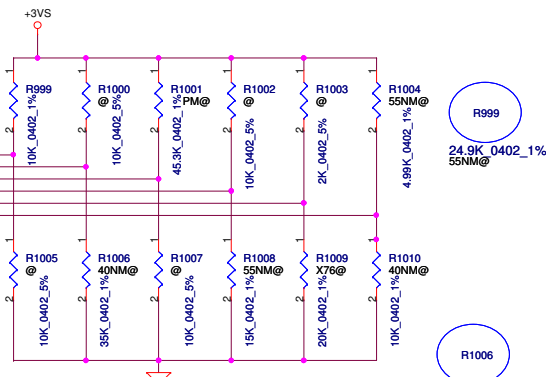
(17) STRAP2
(17) STRAP1
(17) STRAP0
(17) ROM_SCLK
(17) ROM_SI
(17) ROM_SO

R1002
15K 0402_1%
40NM@

R1005
24.9K 0402_1%
40NM@

R1012
44.2 0402_1%
40NM@

R1013
40.2 0402_1%
40NM@



GB1 Family GPU Strap Options

X76

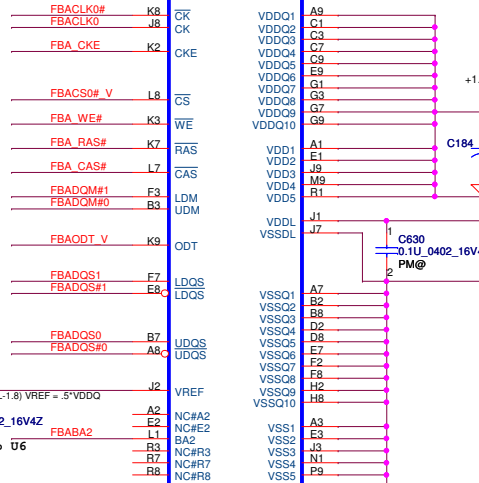
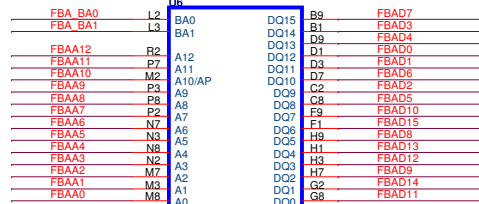
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung 64Mx16	PU 5K	PD 15K	PD 20K	PU 25K	PD 10K	PU 45K
	Hynix 64Mx16	PU 5K	PD 15K	PD 5K	PU 25K	PD 10K	PU 45K
	Qimonda 64Mx16	PU 5K	PD 15K	PD 15K	PU 25K	PD 10K	PU 45K
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung 64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 35K	PU 45K
	Hynix 64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 35K	PU 45K
	Qimonda 64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 35K	PU 45K

4/23 update strap1 10K to 35K
according to N10M latest PUN

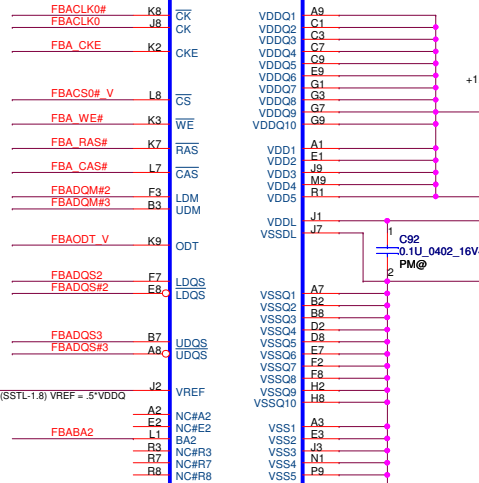
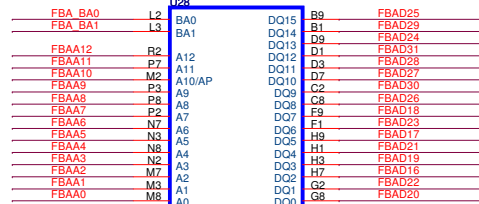
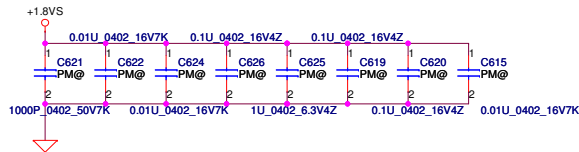
Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

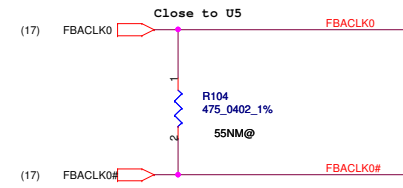
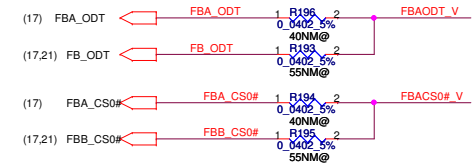
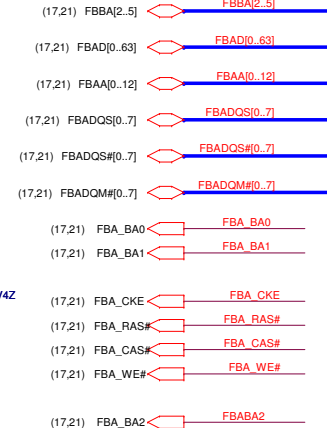
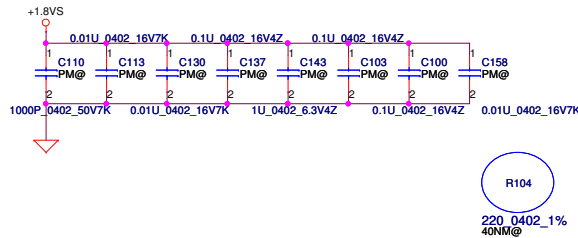
U59
NB10M-GS-S
40NM@



DDR2 BGA MEMORY

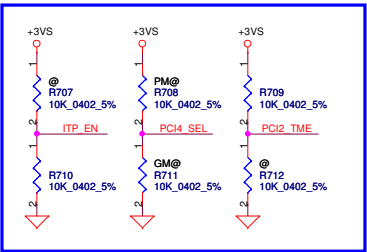
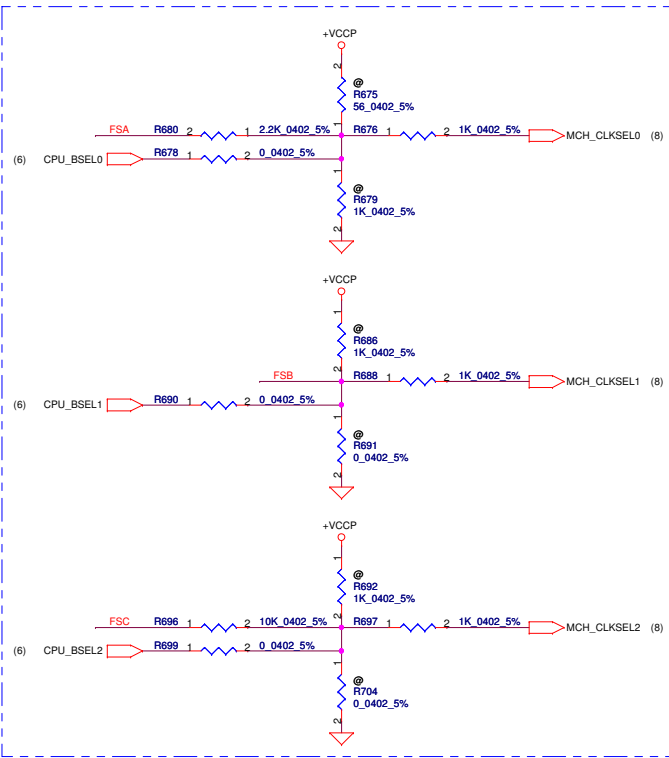


DDR2 BGA MEMORY

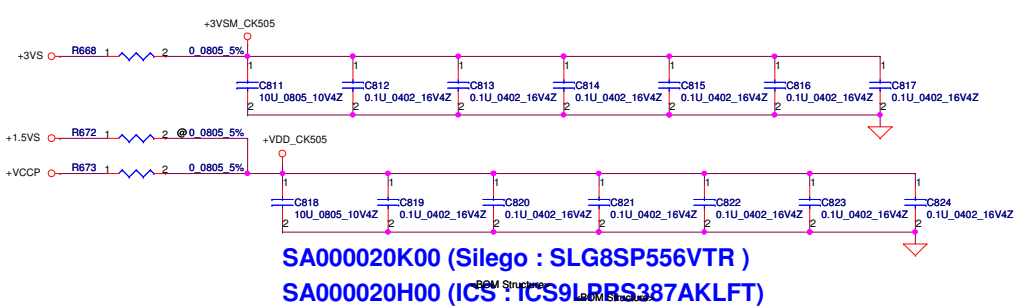


Security Classification	Compal Secret Data			Title	
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				Date: Tuesday, April 28, 2009	Rev 1.0
				Sheet 20 of 51	

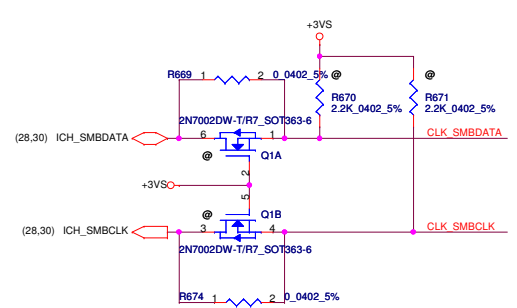
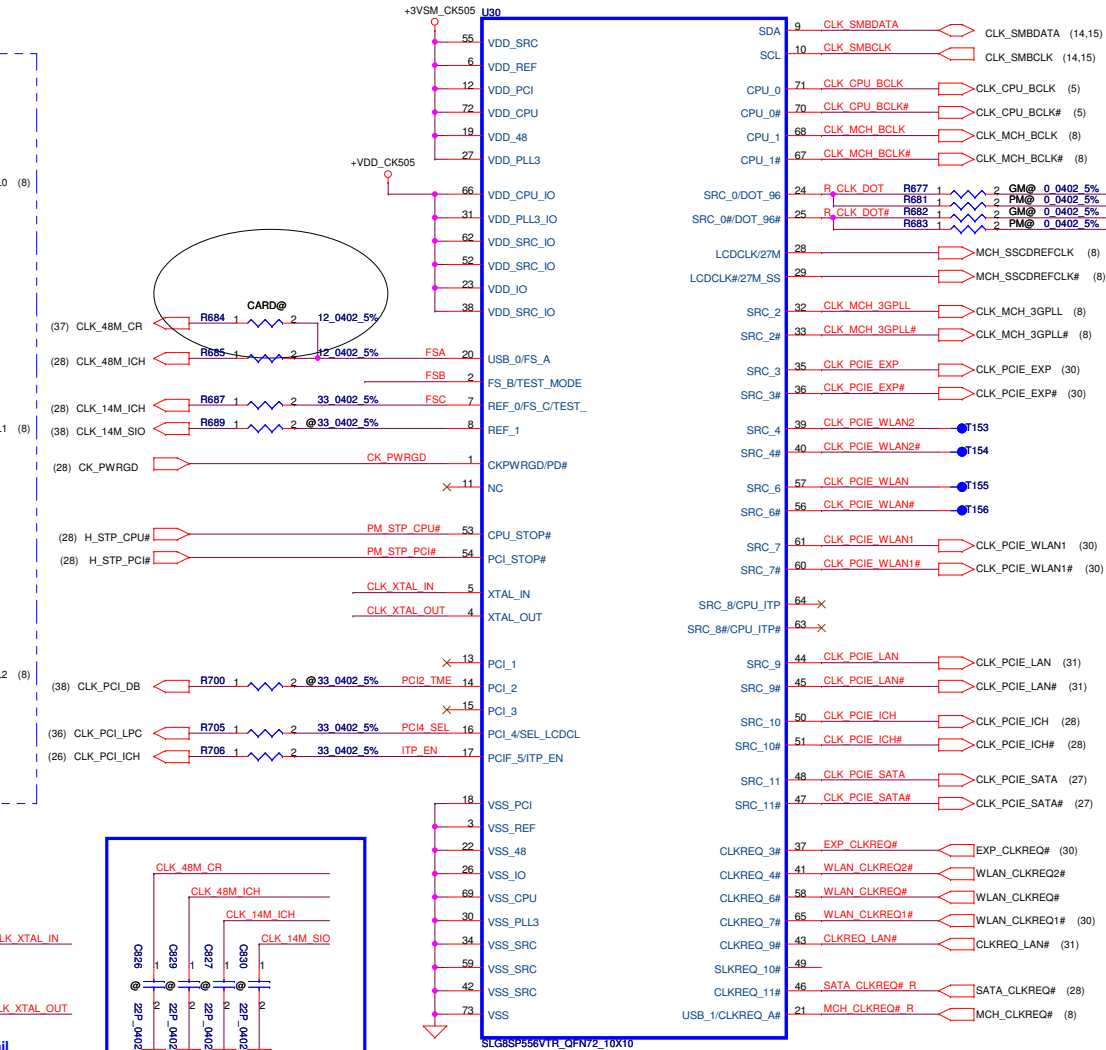
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

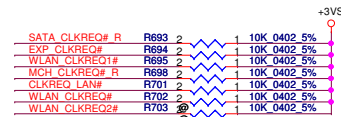


SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN
SRC6	PCIE_WLAN1
SRC8	PCIE_WLAN
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



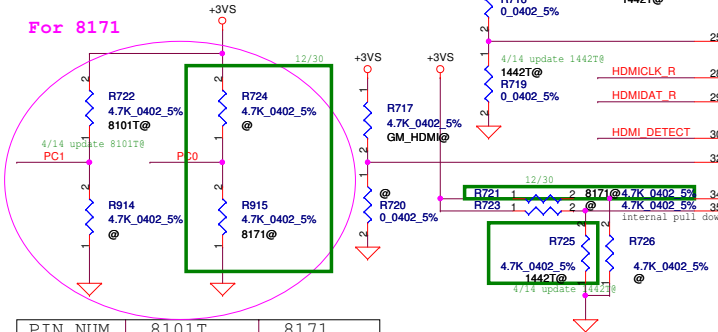
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	PCIE_SATA
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

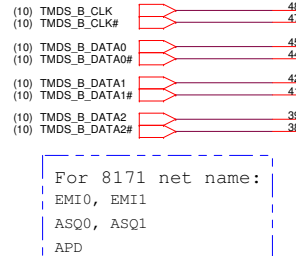
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Issued Date		2009/04/23		Deciphered Date		2010/05		Title		Clock Generator CK505	
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						Custom		KIWA5/6 LA-5081P		1.	
						Date: Tuesday, April 28, 2009		Sheet 22 of 51			

10/30 update PS8171 co-lay circuit
4/14 update 1442T co-lay circuit

For 8171

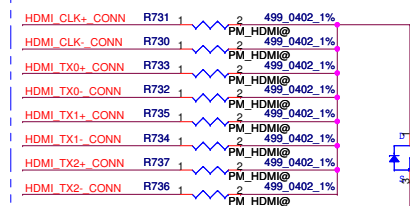


PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	APD
PIN12	GND	ASQ1
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

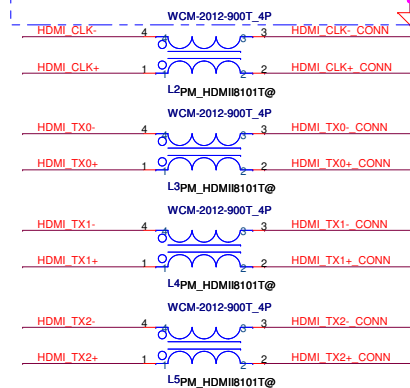


For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD

TMDS pull down (500ohm) resistors for ATI M92-S2 XT

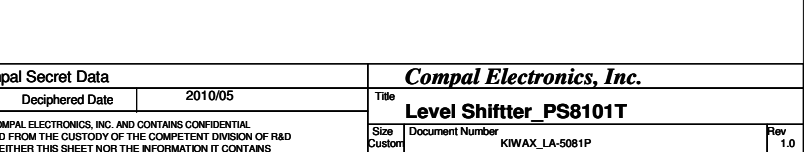
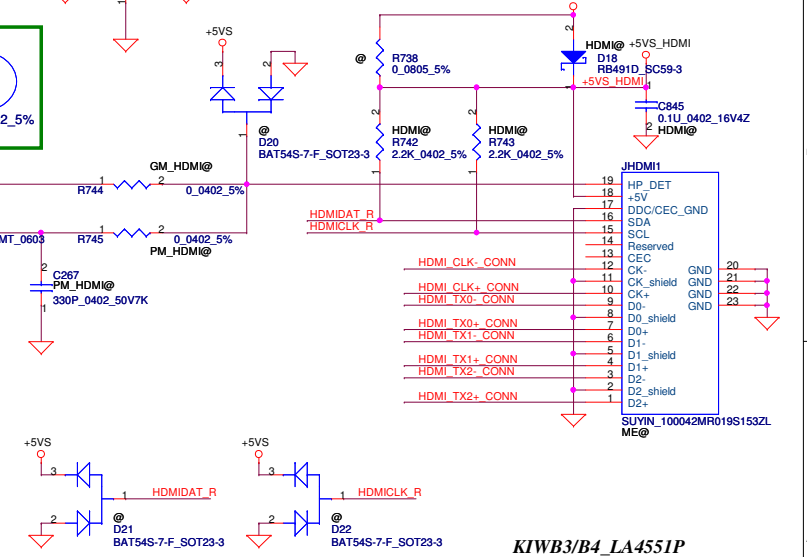
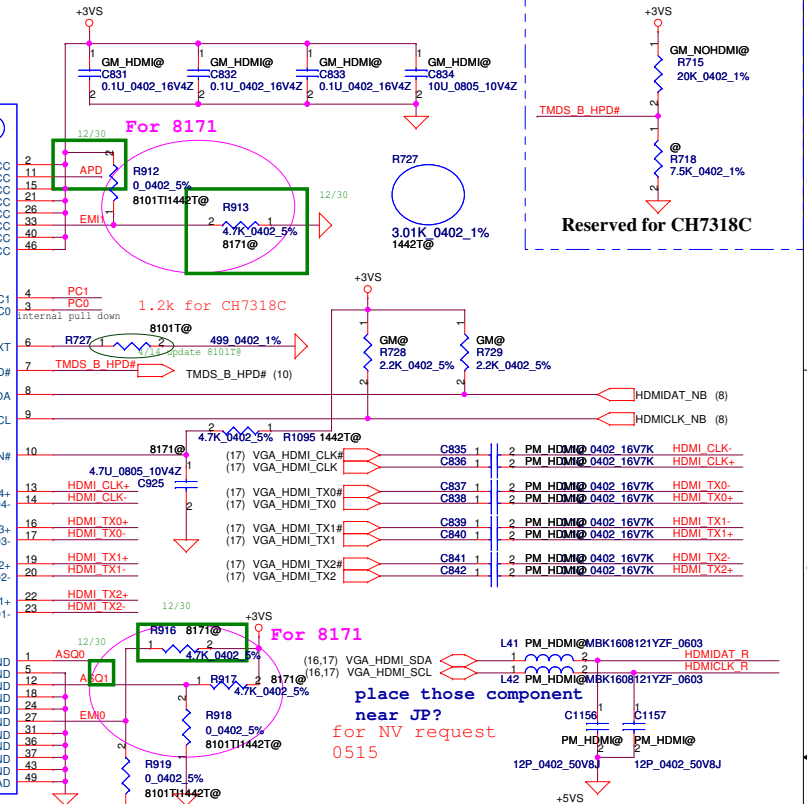
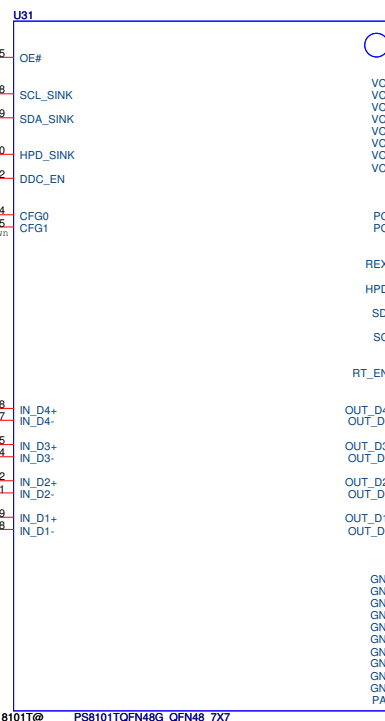


NEAR CONNECTOR



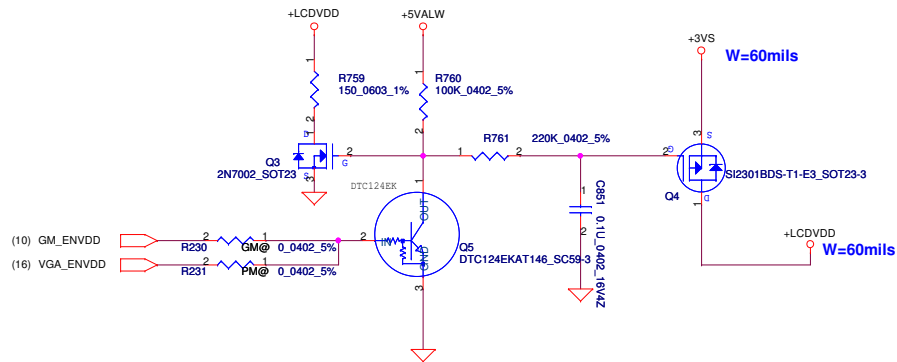
HDMI CLK+	R751	1442T@	2	0.0402_5%	HDMI CLK+ CONN
HDMI CLK-	R752	1442T@	2	0.0402_5%	HDMI CLK- CONN
HDMI TX0+	R753	1442T@	2	0.0402_5%	HDMI TX0+ CONN
HDMI TX0-	R754	1442T@	2	0.0402_5%	HDMI TX0- CONN
HDMI TX1+	R755	1442T@	2	0.0402_5%	HDMI TX1+ CONN
HDMI TX1-	R756	1442T@	2	0.0402_5%	HDMI TX1- CONN
HDMI TX2+	R757	1442T@	2	0.0402_5%	HDMI TX2+ CONN
HDMI TX2-	R758	1442T@	2	0.0402_5%	HDMI TX2- CONN

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

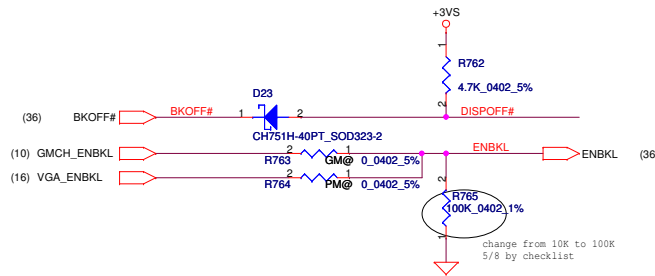


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				Date Tuesday, April 28, 2009	Sheet 23 of 51

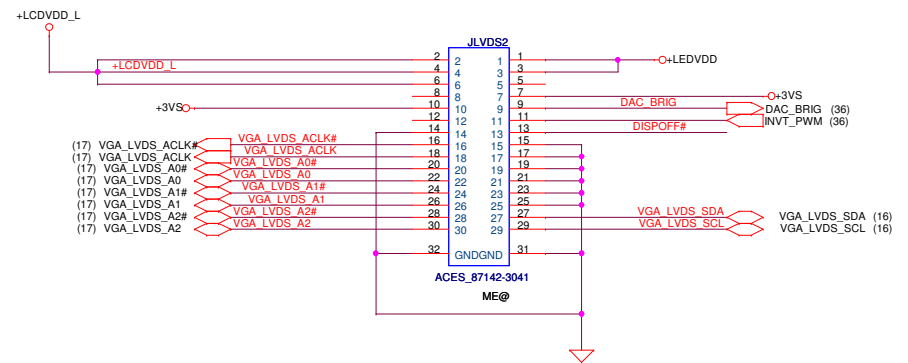
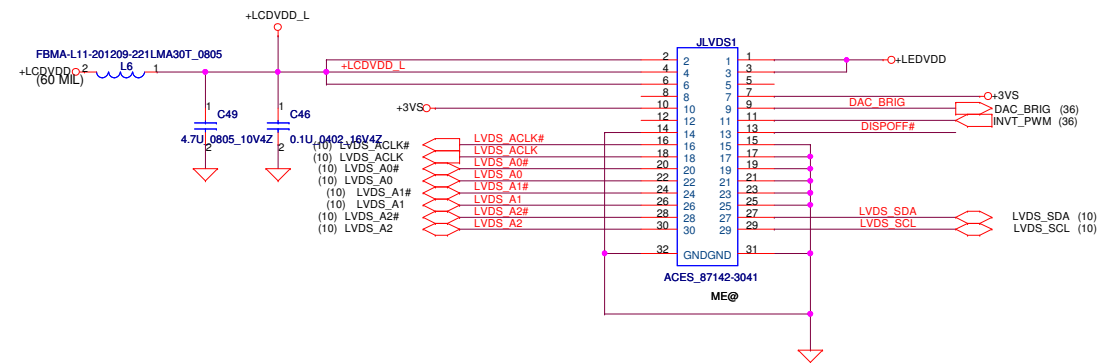
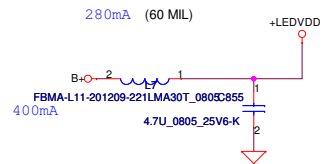
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.
FOR UMA



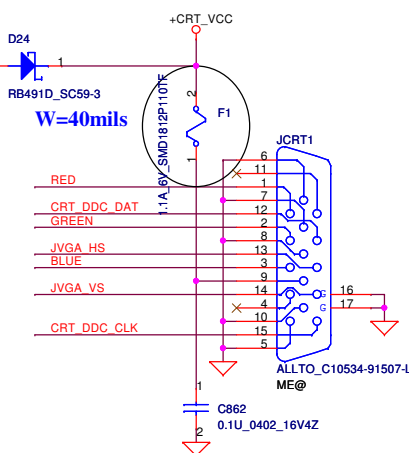
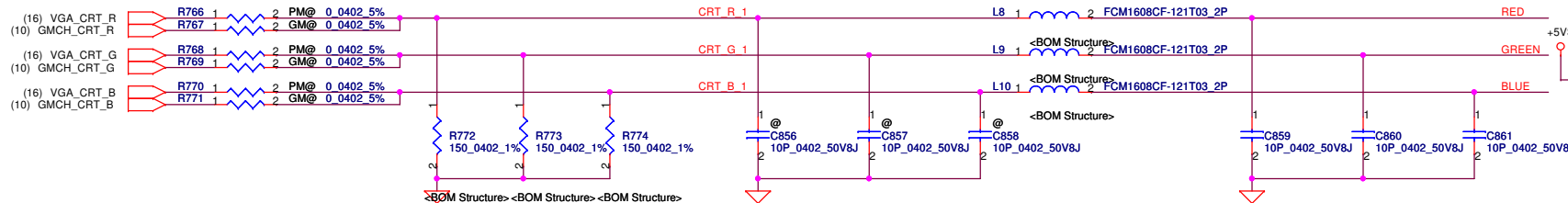
LCD/PANEL BD. Conn.
FOR DIS



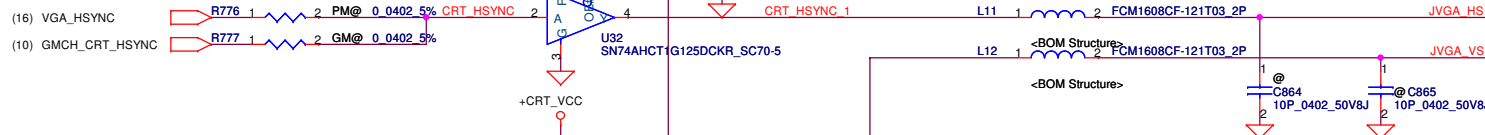
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	Compal Electronics, Inc.	
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				Size B	Rev 1.0
Date: Tuesday, April 28, 2009		Sheet 24 of 51		KIWA5/6 LA-5081P	

CRT Connector

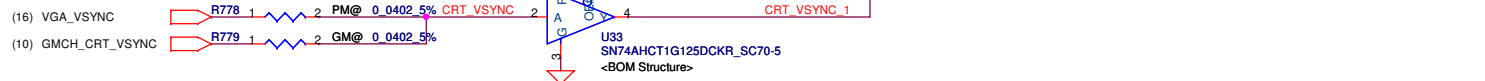
CLOSE TO CONN



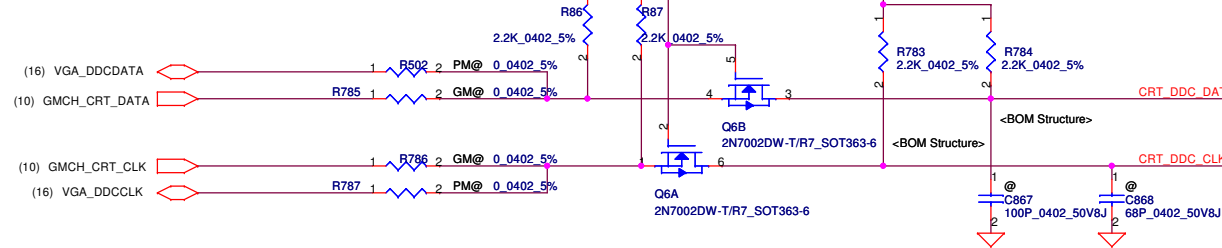
CLOSE TO CONN



CLOSE TO CONN



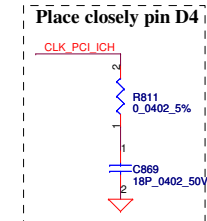
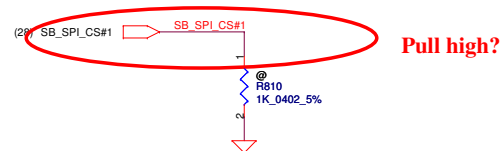
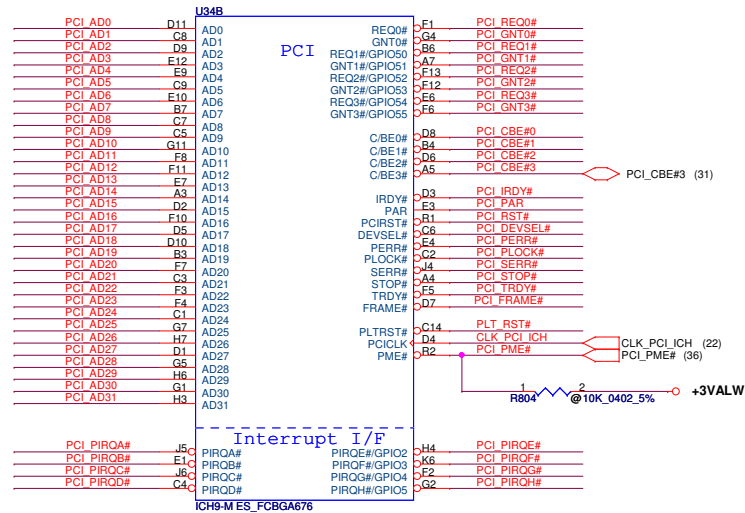
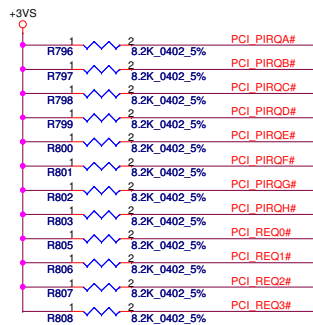
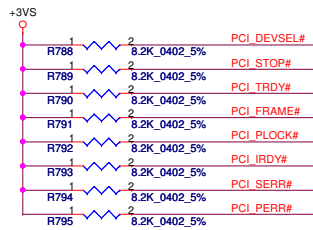
CLOSE TO CONN



PIN ASSIGMENT

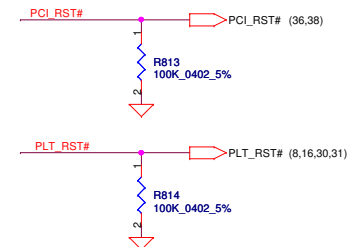
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

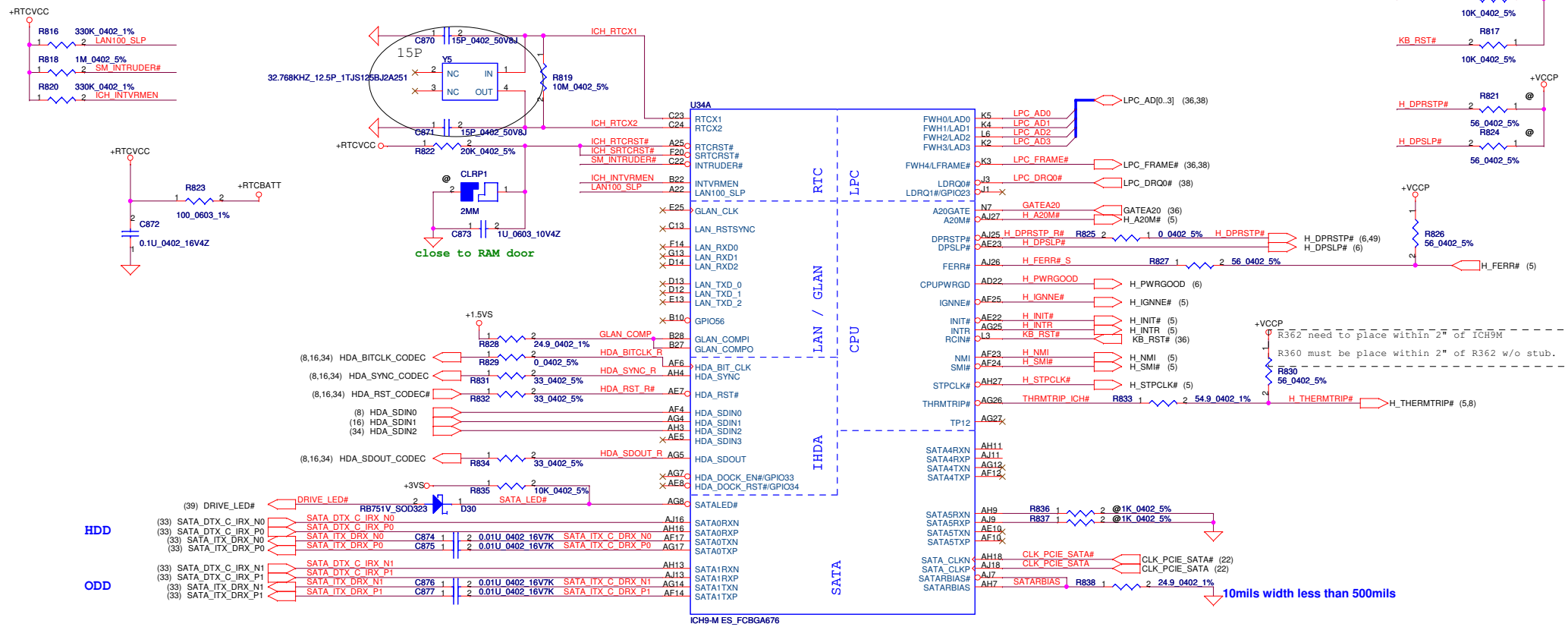
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Custom	Document Number	KIWA5/6 LA-5081P	Rev	1.0
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A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

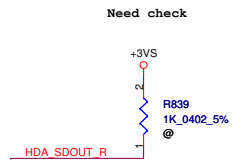
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

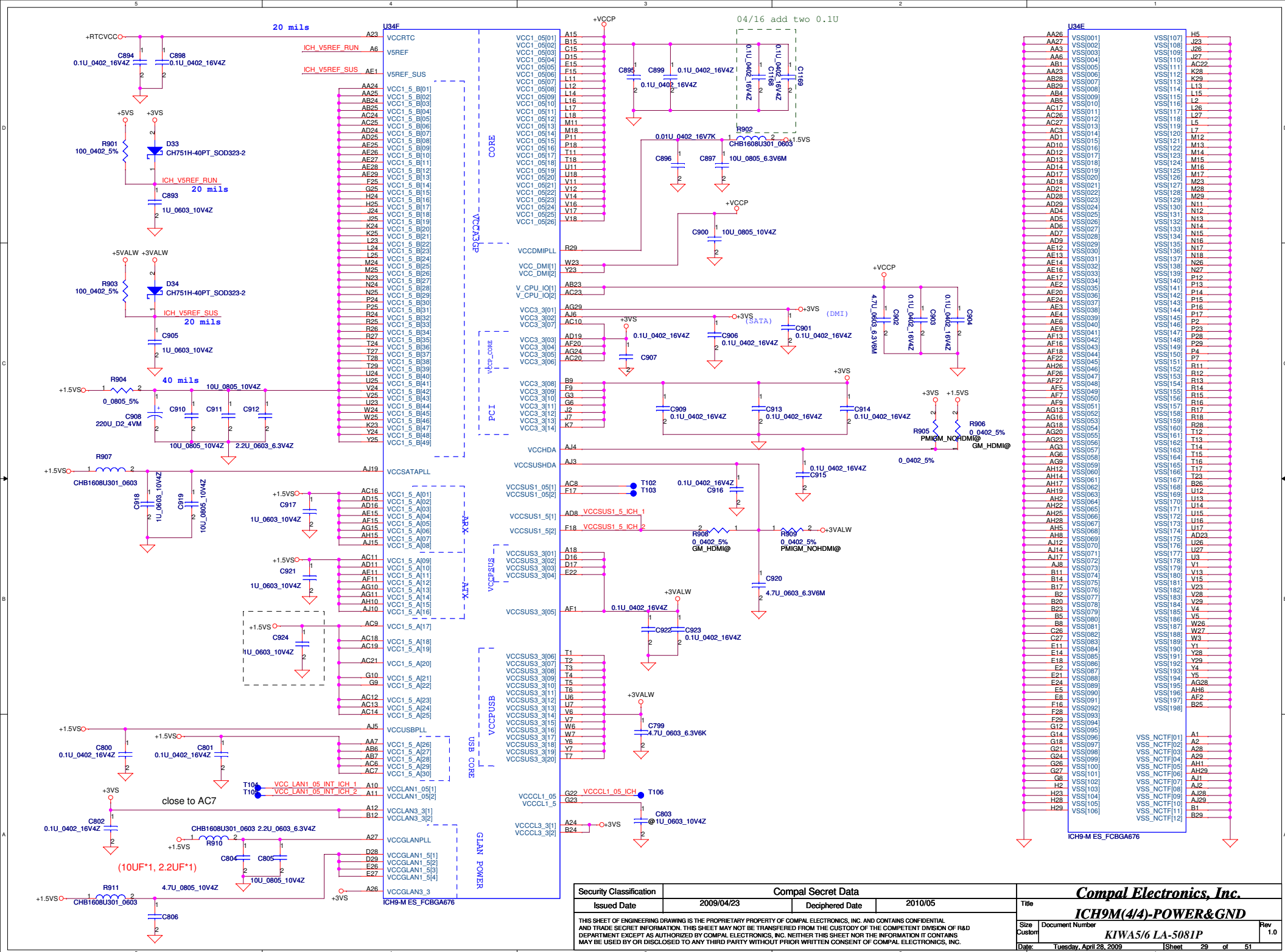




SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1





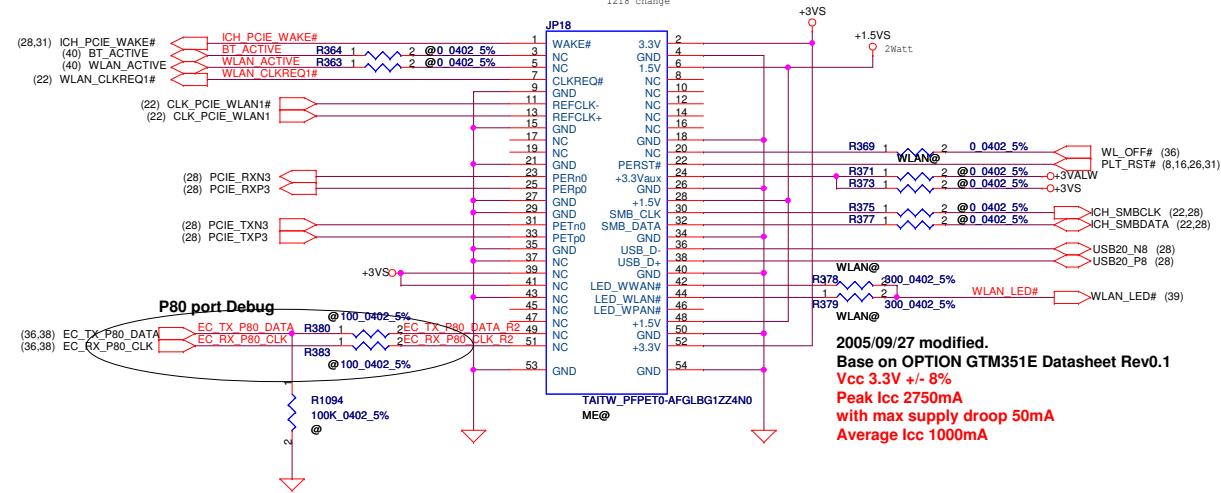
Security Classification			Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05		Size	Document Number
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				Date	Tuesday, April 28, 2009	Sheet 29 of 51

Compal Electronics, Inc.

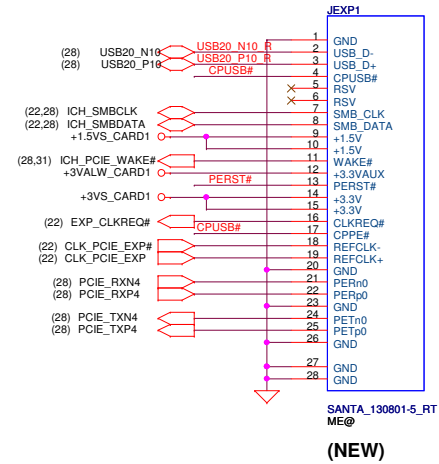
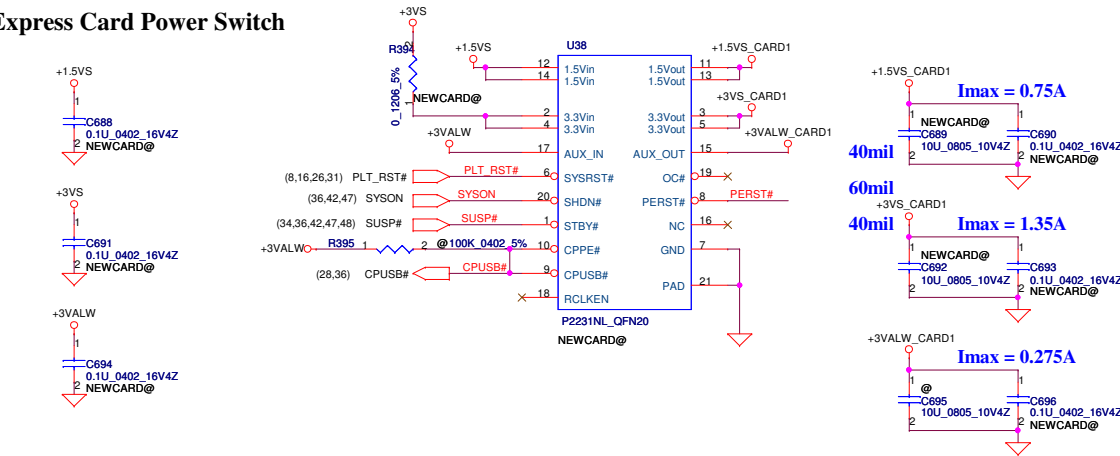
ICH9M(4/4)-POWER&GND

Rev 1.0

Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

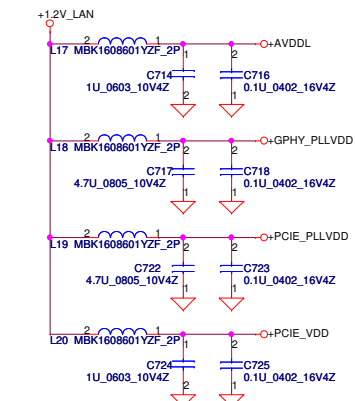
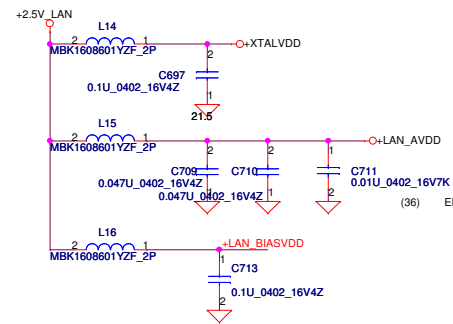


Express Card Power Switch

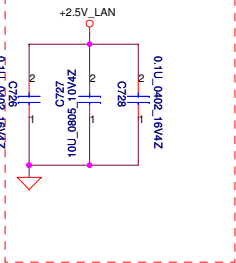


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Issued Date		2009/04/23		Deciphered Date		2010/05		Title					
								Mini-Card/3G/TV /BT					
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								Date	Tuesday, April 28, 2009	Sheet	30	of	51

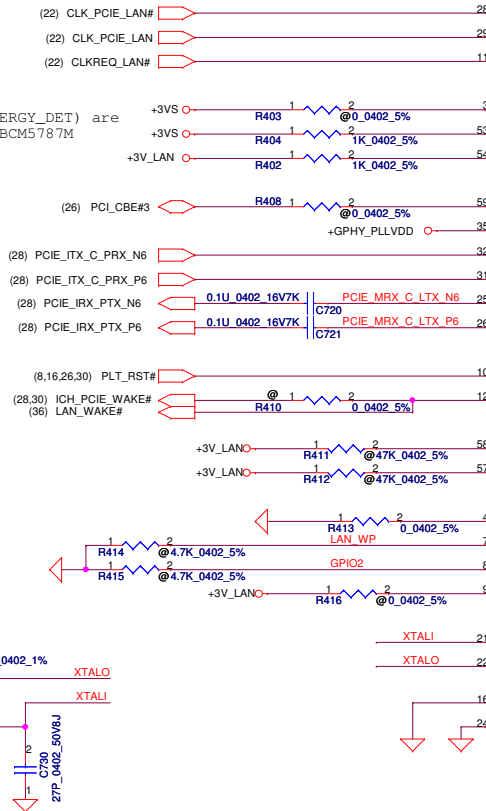
Layout Notice : Filter place as close chip as possible.



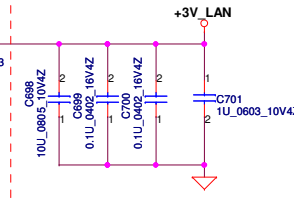
Layout Notice : Place as close chip as possible.



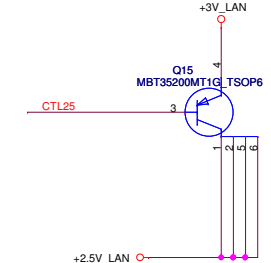
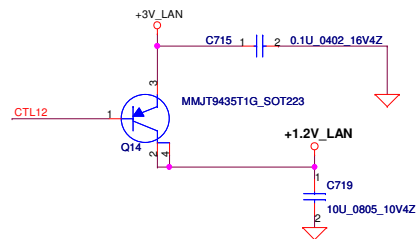
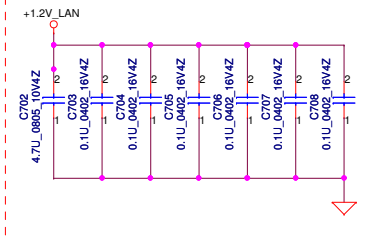
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Layout Notice : Place as close chip as possible.

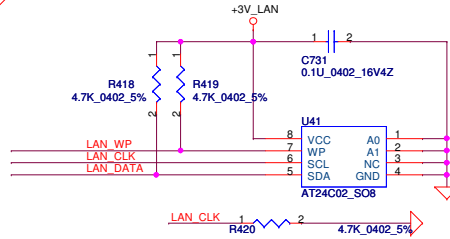


Layout Notice : 1.2V filter. Place as close chip as possible.

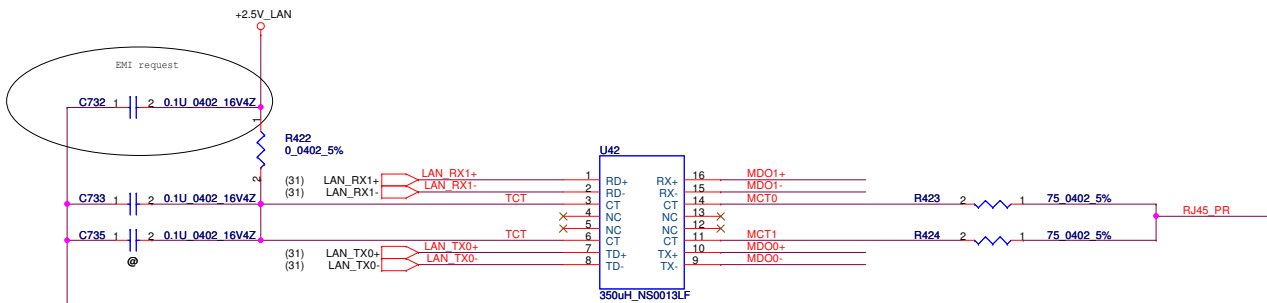


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

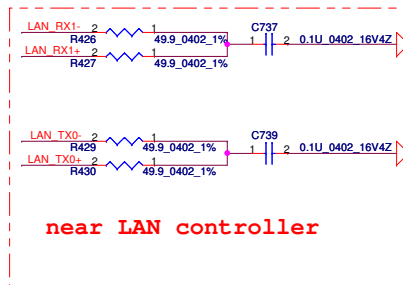
Layout Notice : Filter place as close chip as possible.



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2010/05				2010/05				2010/05			
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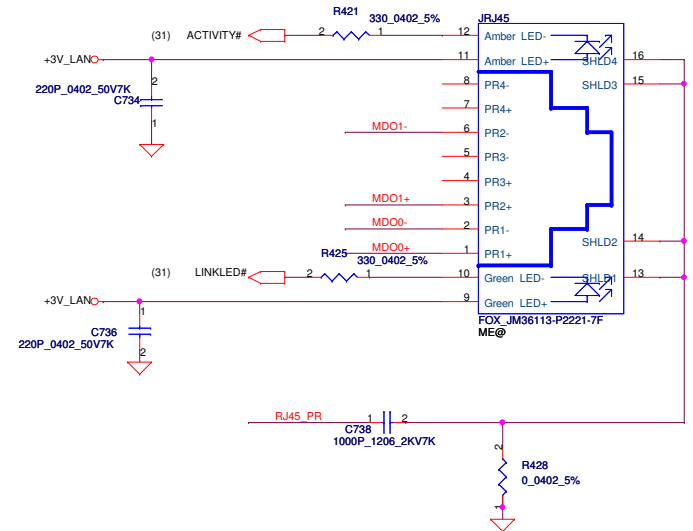


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

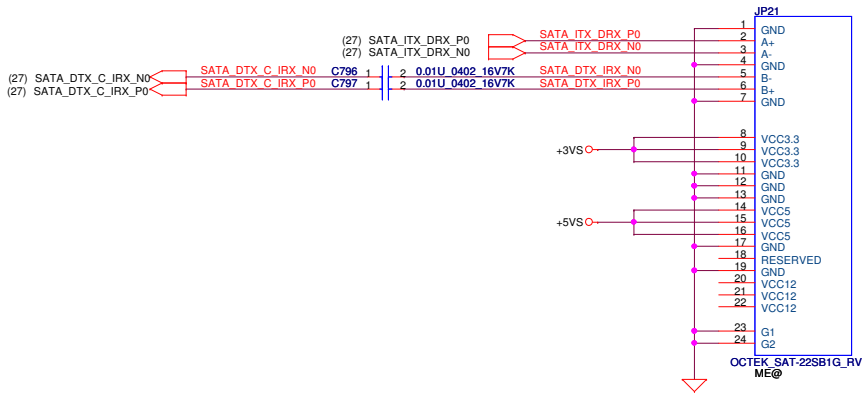


near LAN controller

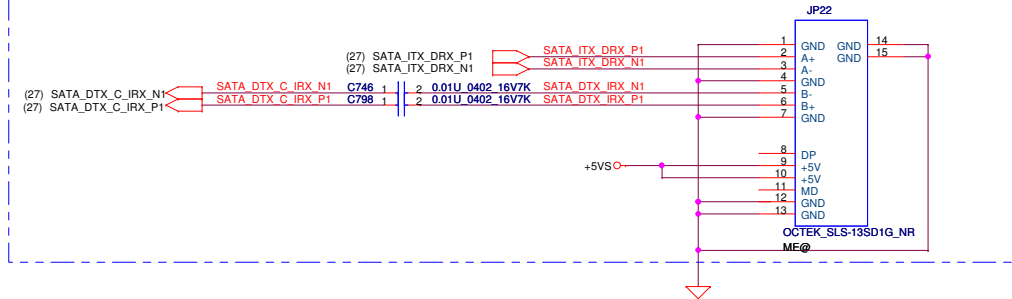
RJ45 CONN



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Deciphered Date				2010/05				LAN CONTROLLER			
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				Document Number				Rev			
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SATA ODD Conn.



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				Size B	Document Number	Rev
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AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF

CODEC POWER

(3.33V)
250mW

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

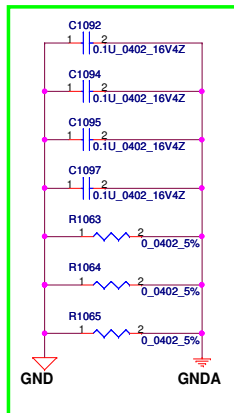
W=40Mil

CX20548
AMOM DAA

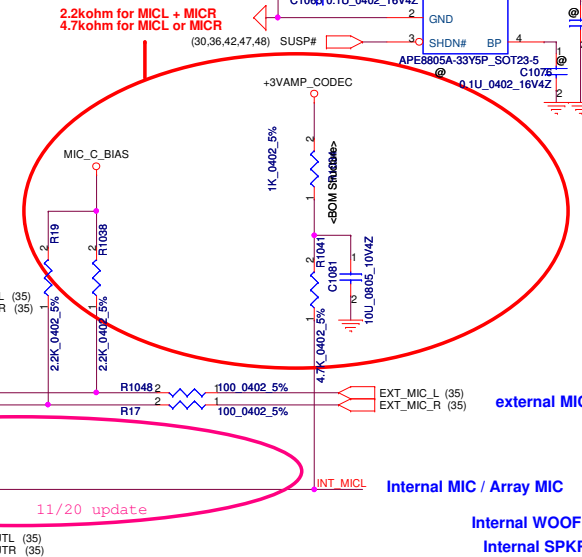
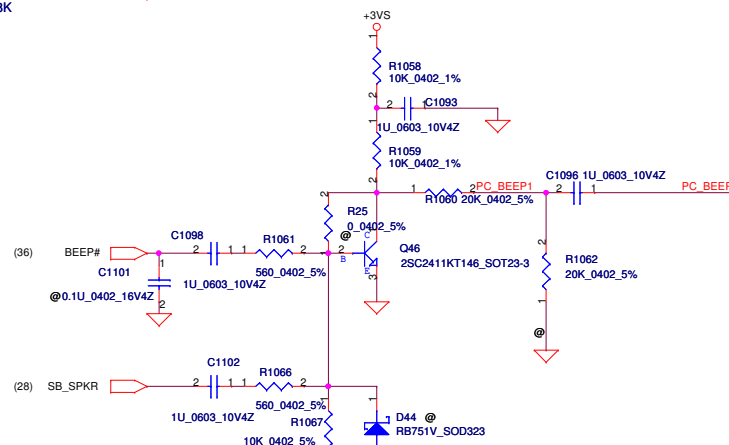
11/20 update
PC_BEEP dB control

0216_Change value.

DIGITAL **ANALOG**



Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

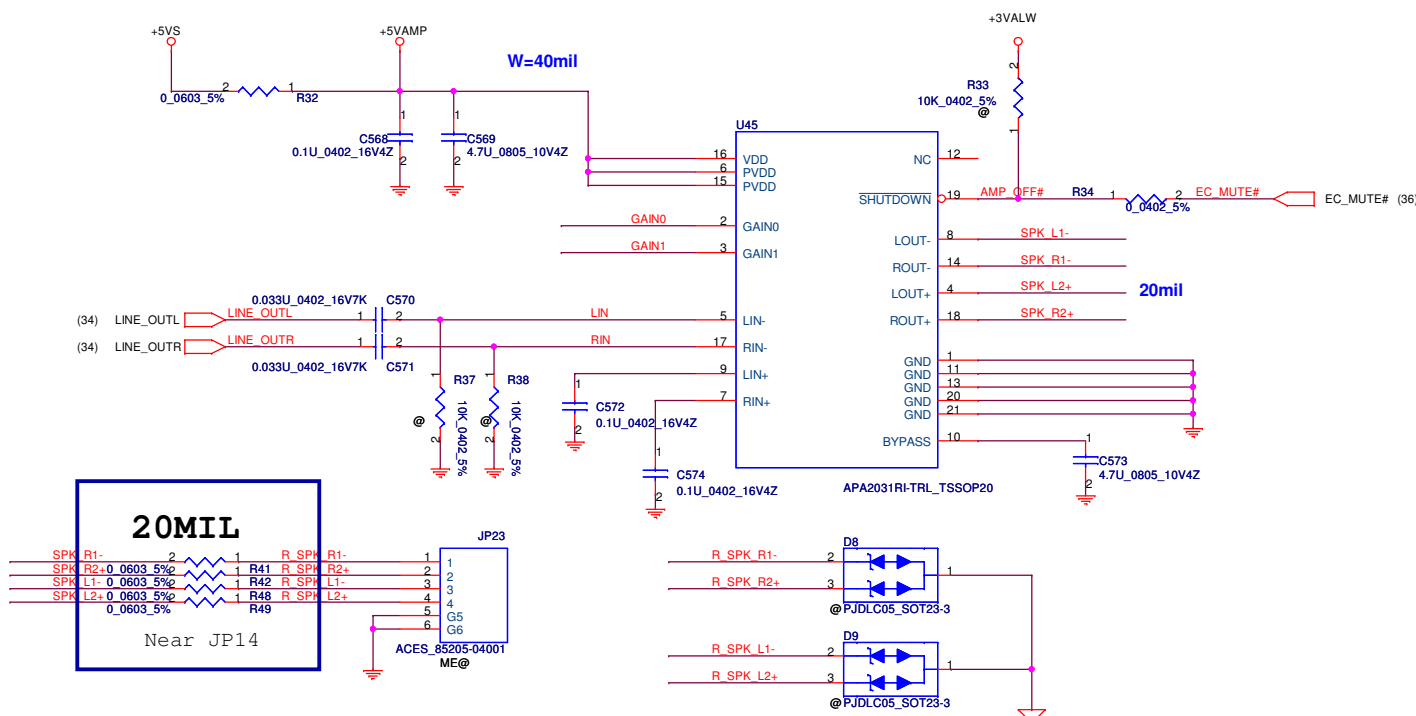


Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

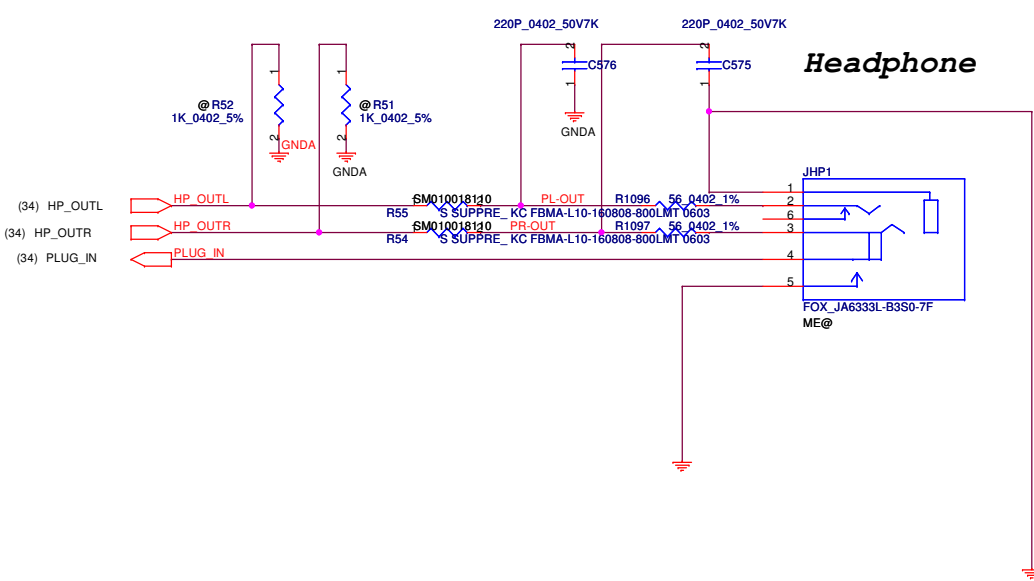
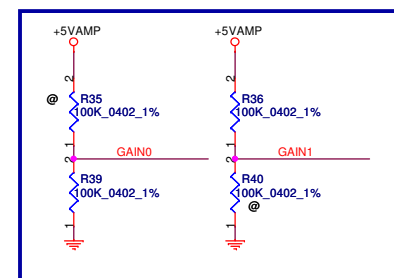
port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

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Size	Document Number	KIWA/56 LA-5081P		Rev 1.0	
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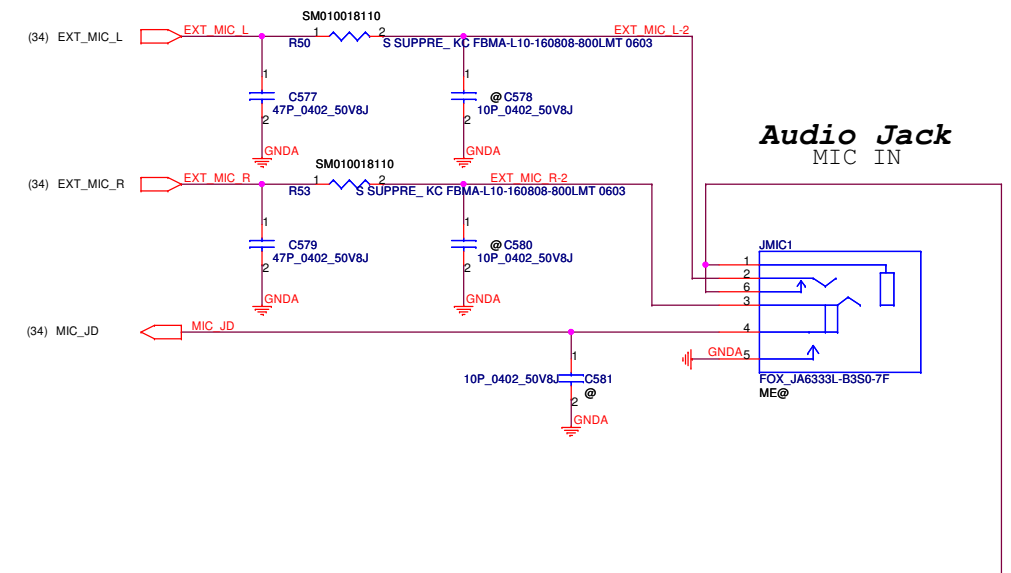
Speaker Connector



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

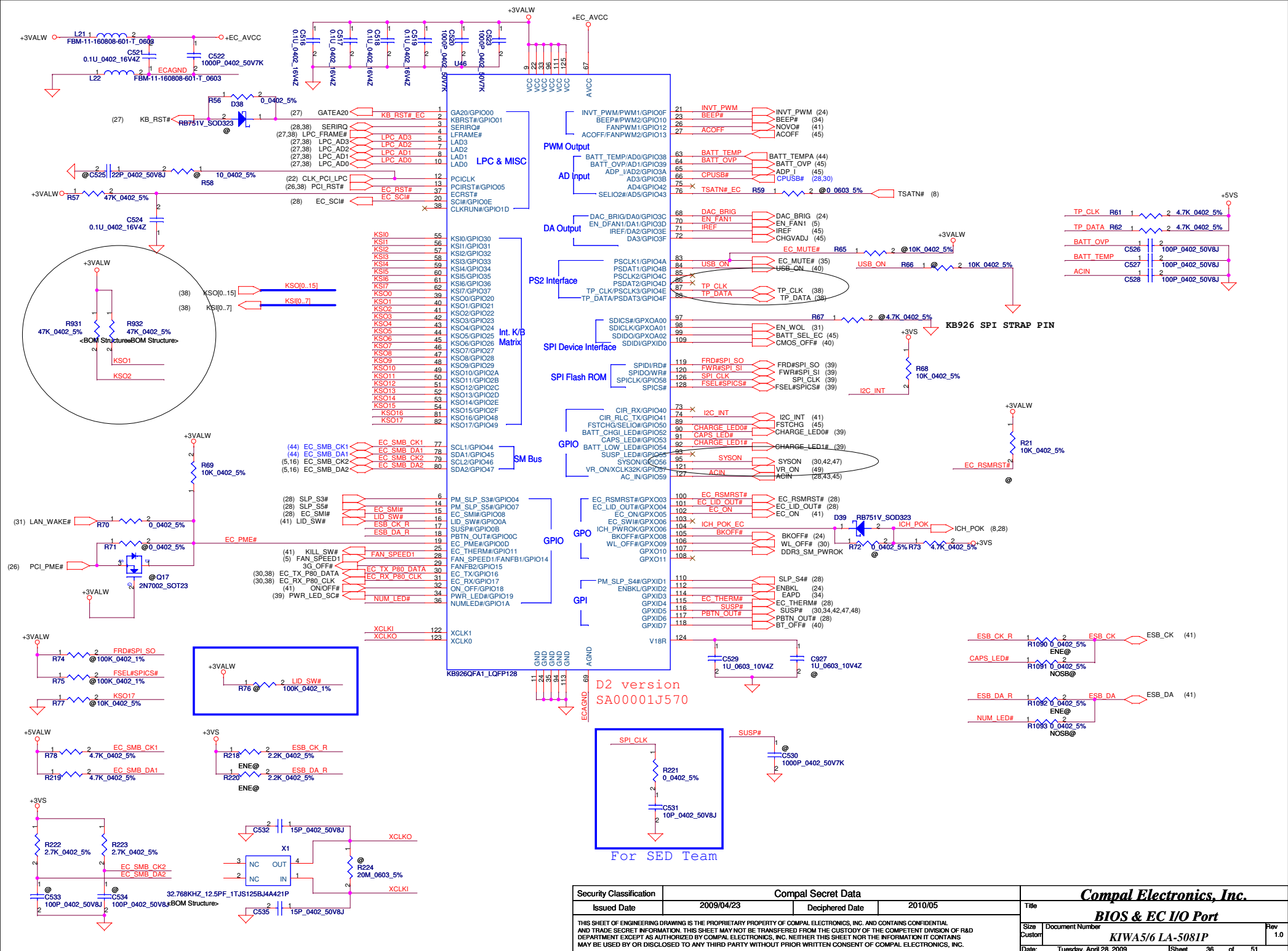


Audio Jack



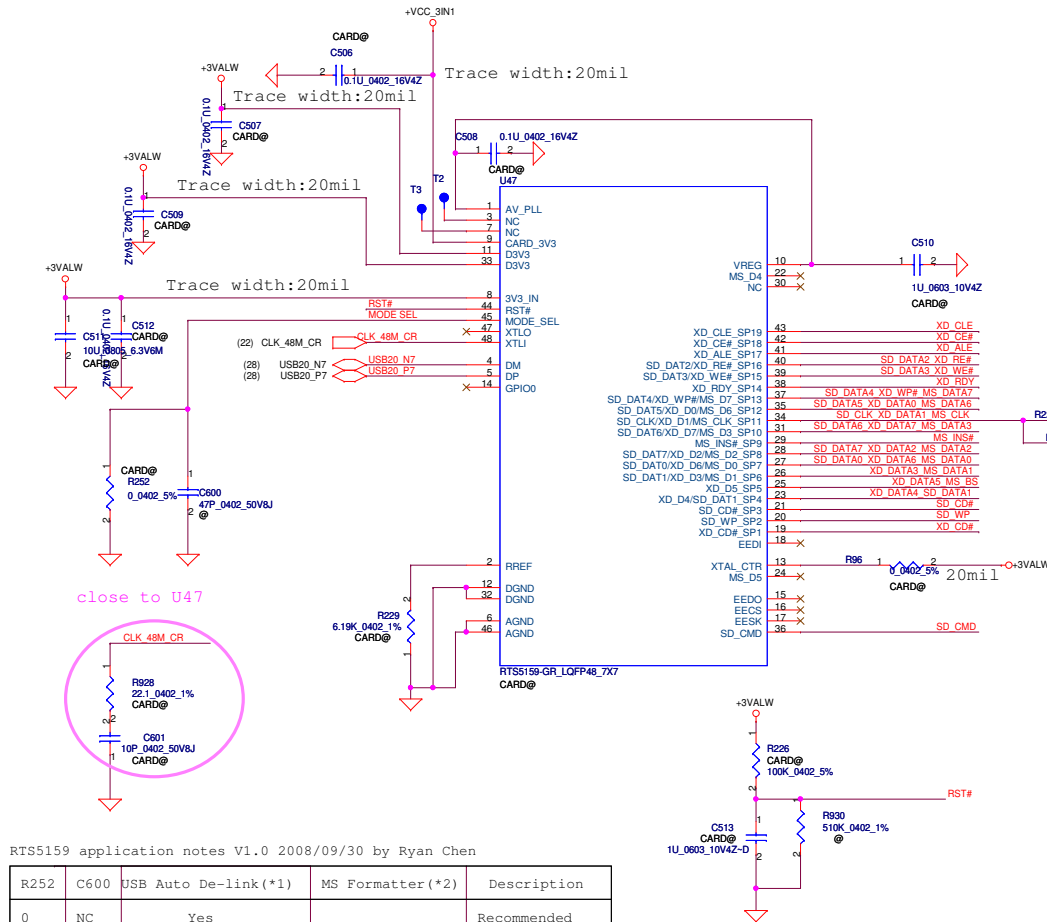
Audio Jack MIC IN

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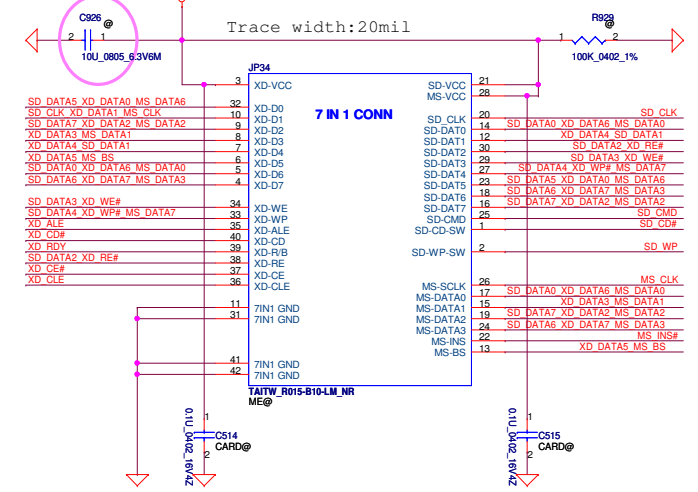
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Issued Date	2009/04/23	Deciphered Date	2010/05	Title BIOS & EC I/O Port		
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				Date: Tuesday, April 29, 2009	Sheet 36 of 51	

Card reader(XD/SD/MMC/MS/MS-Pro HD SD)

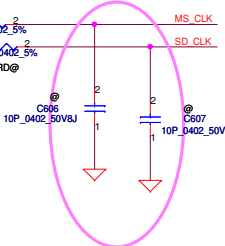


11/04 new added

7 in 1 Card Reader



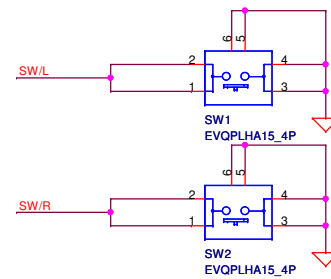
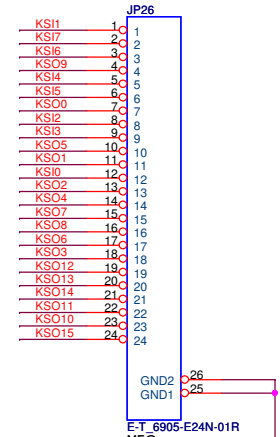
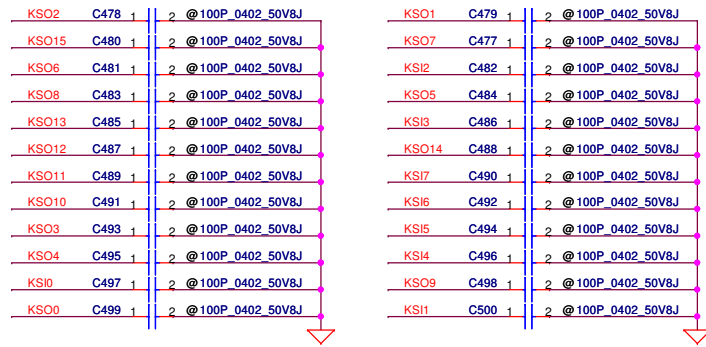
close to connector (JP34)



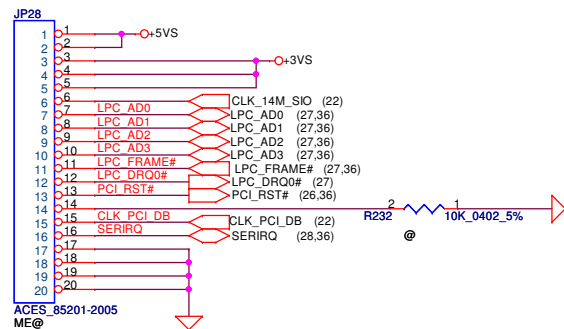
Source:SP010001E00
2nd source:SP010001F00
30 pin

INT_KBD Conn.

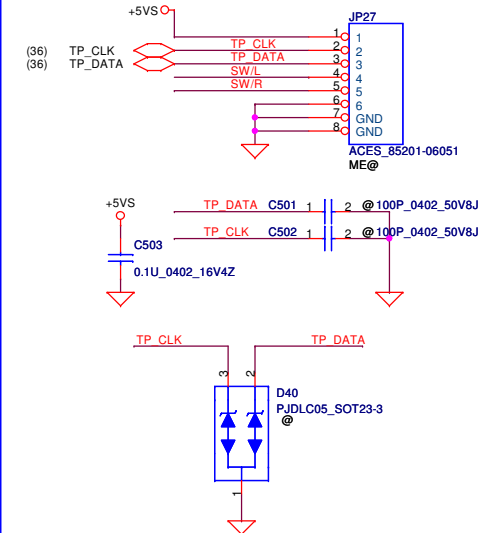
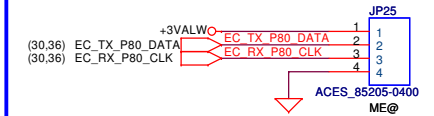
KS[0..7] (36)
KSO[0..15] (36)



FOR LPC SIO DEBUG PORT

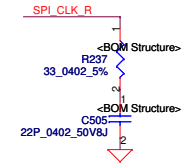
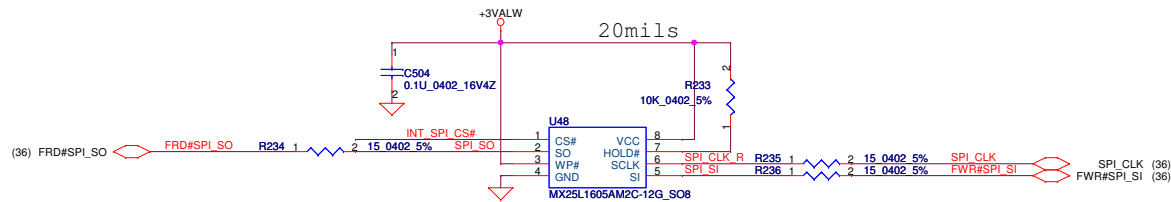


EC DEBUG PORT

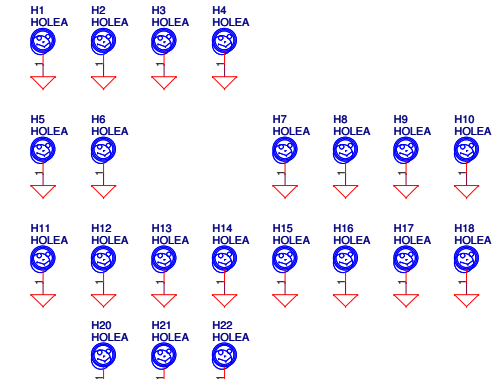
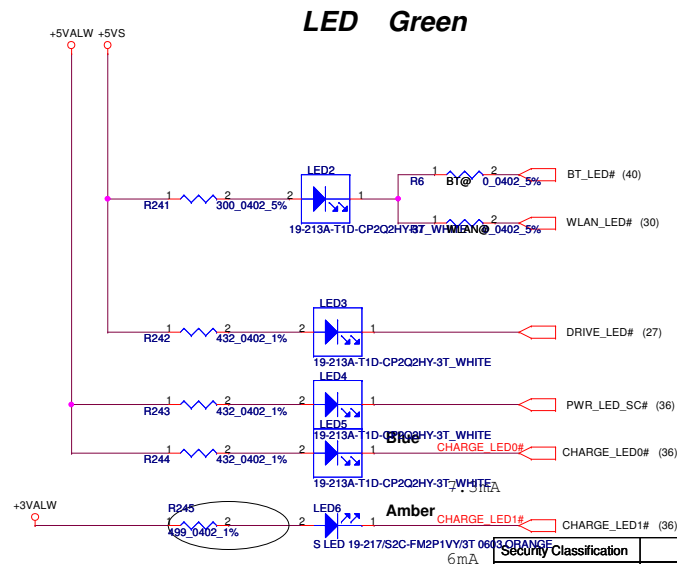
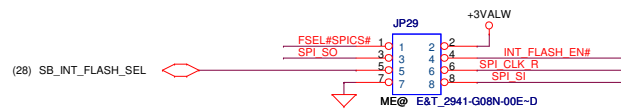
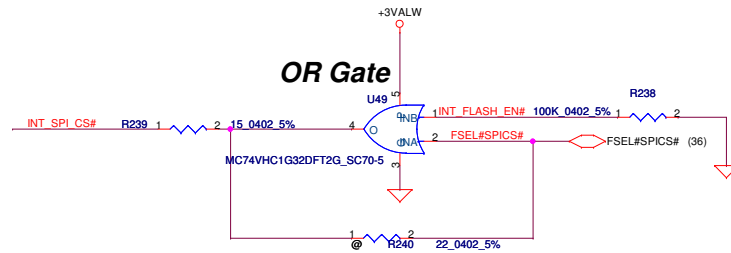


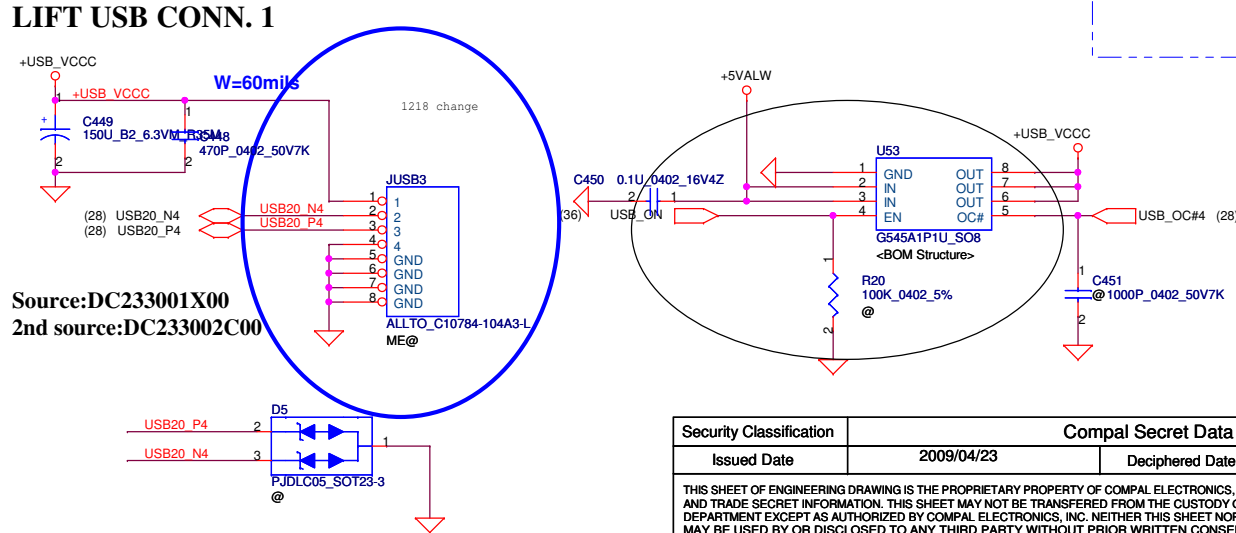
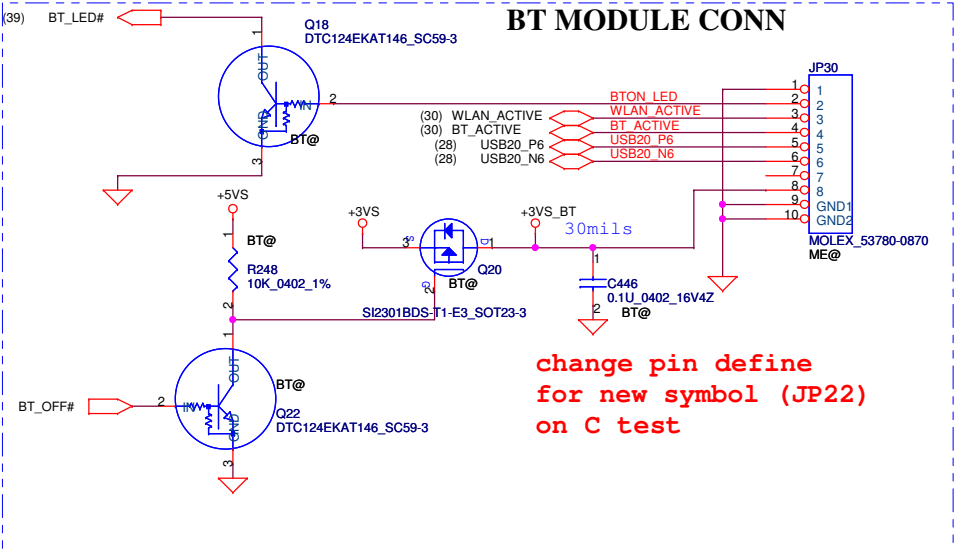
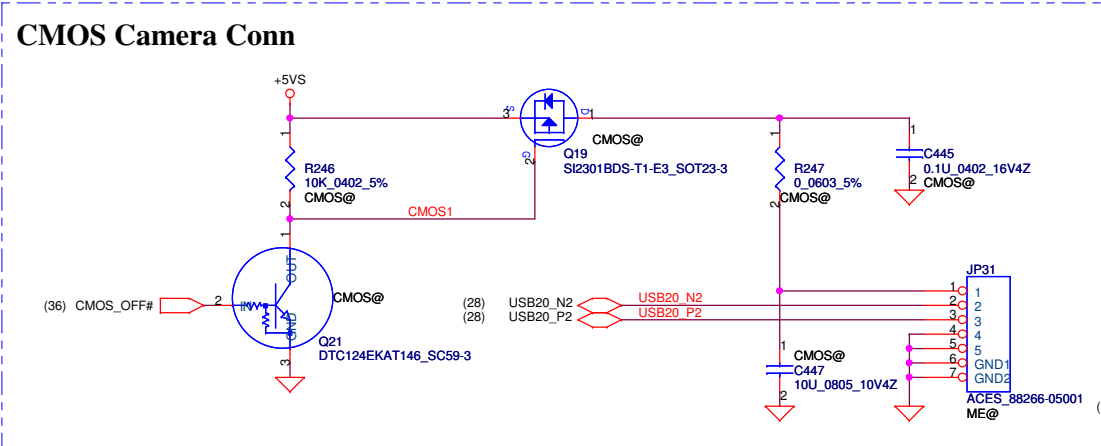
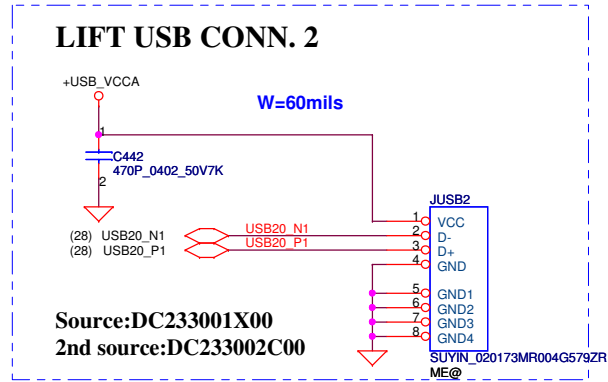
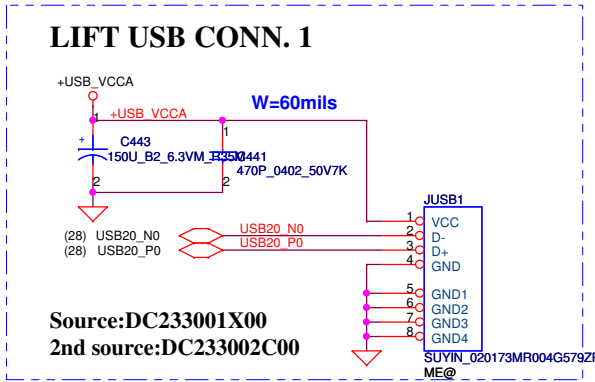
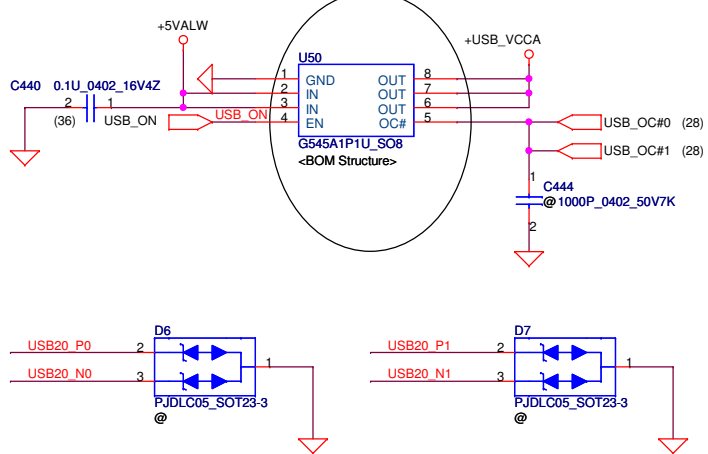
Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/23	Deciphered Date	2010/05	Compal Electronics, Inc.	
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FOR EC 16M SPI ROM



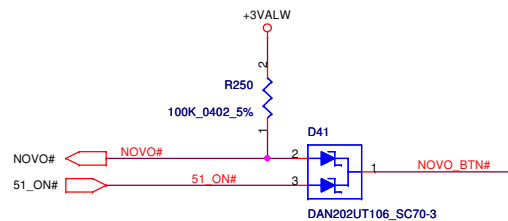
INPUT		OUTPUT Y
A	B	
L	L	L
H	L	H
L	H	H
H	H	H



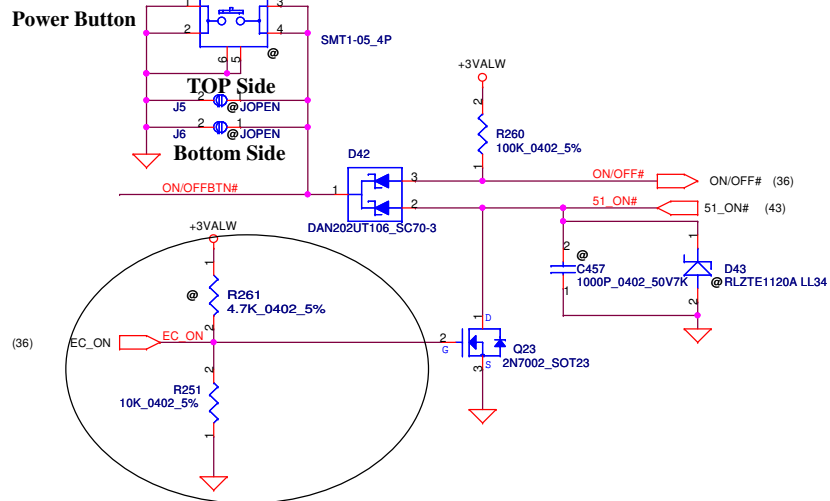


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				Custom	KIWA5/6 LA-5081P
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				Tuesday, April 28, 2009	1.0
				Sheet	40 of 51

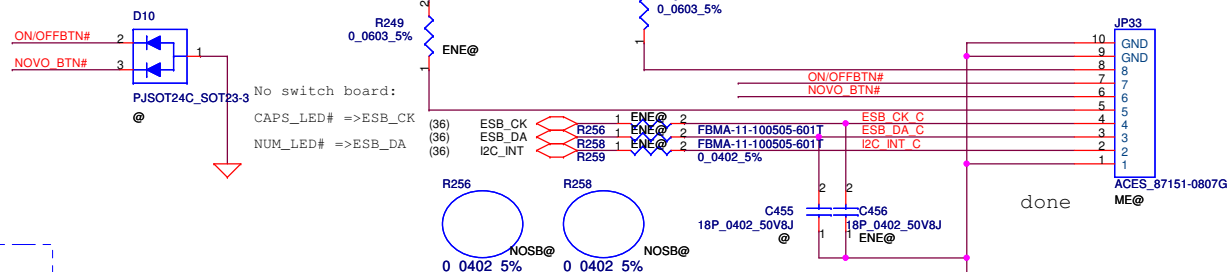
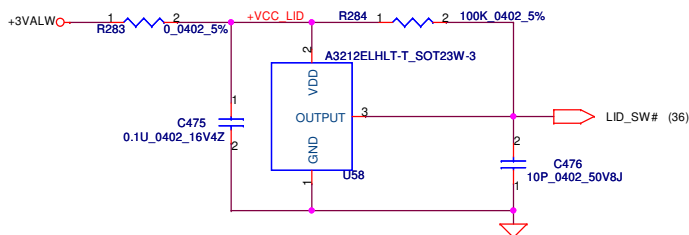
(36)
(43)



ON/OFF switch

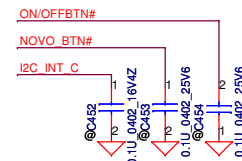
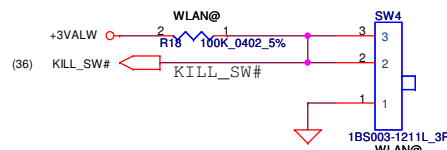


Lid Switch



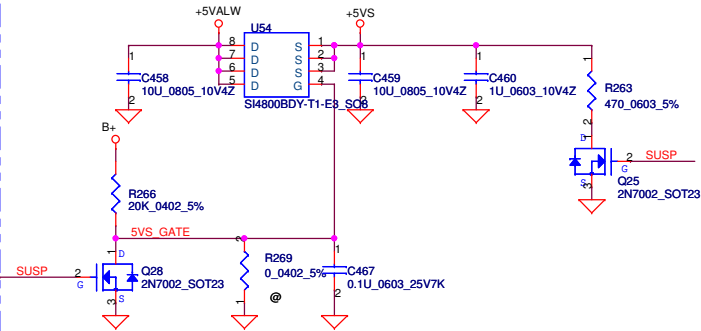
02/26 remove SMBus for CY

Kill Switch

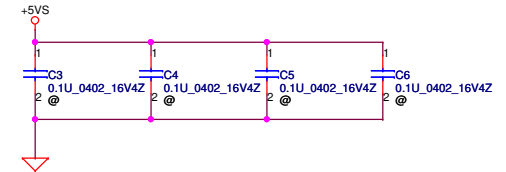
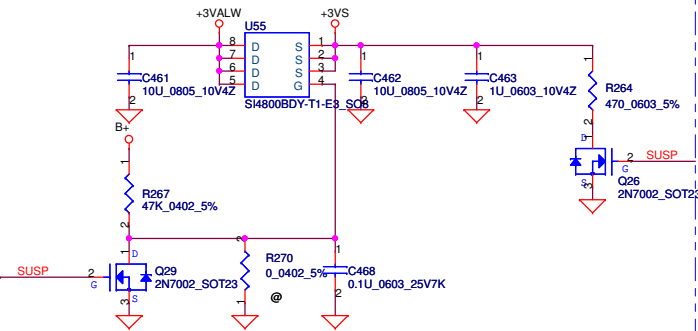


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				Size Custom	Document Number
				KIWA5/6 LA-5081P	
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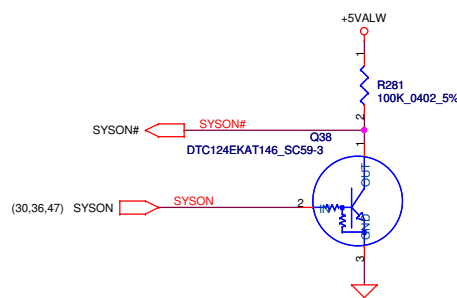
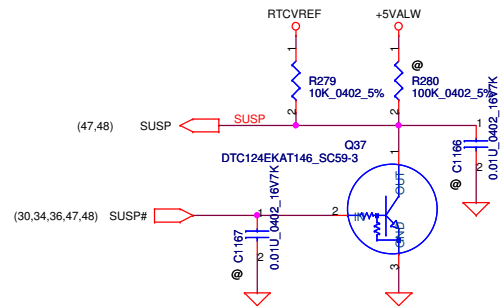
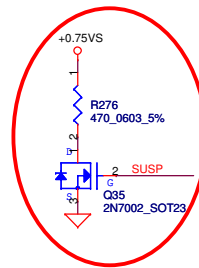
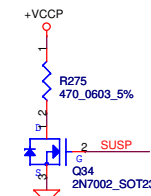
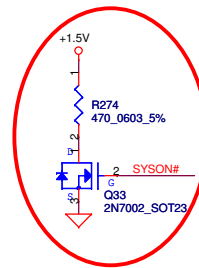
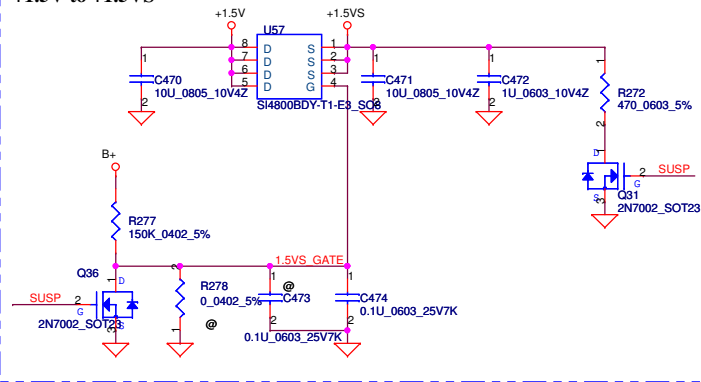
+5VALW TO +5VS



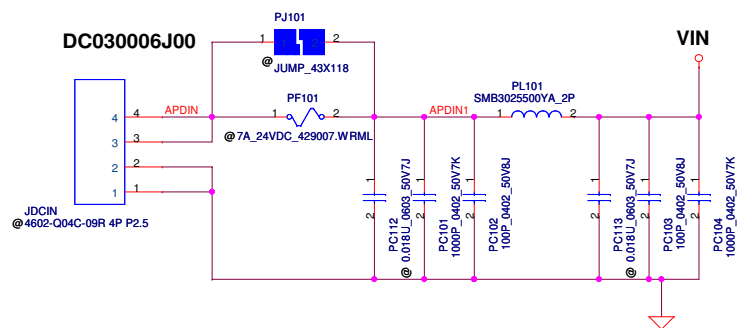
+3VALW TO +3VS



+1.5V to +1.5VS

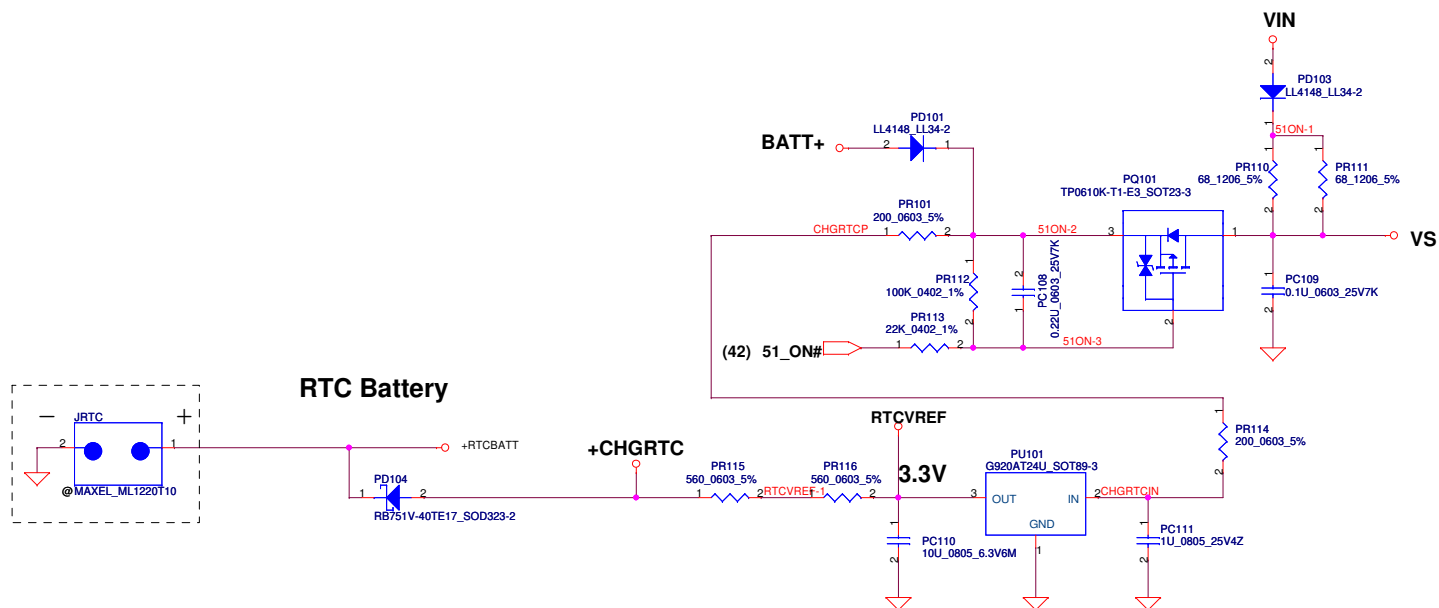
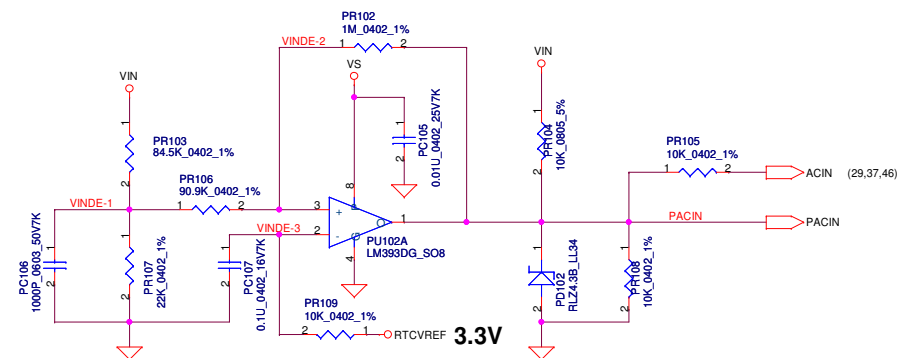


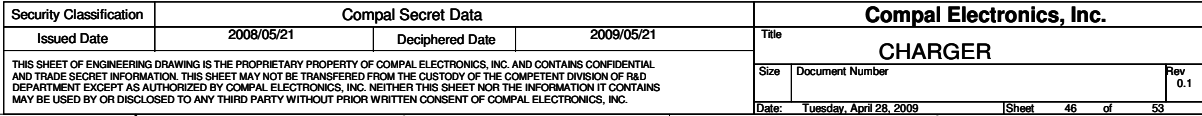
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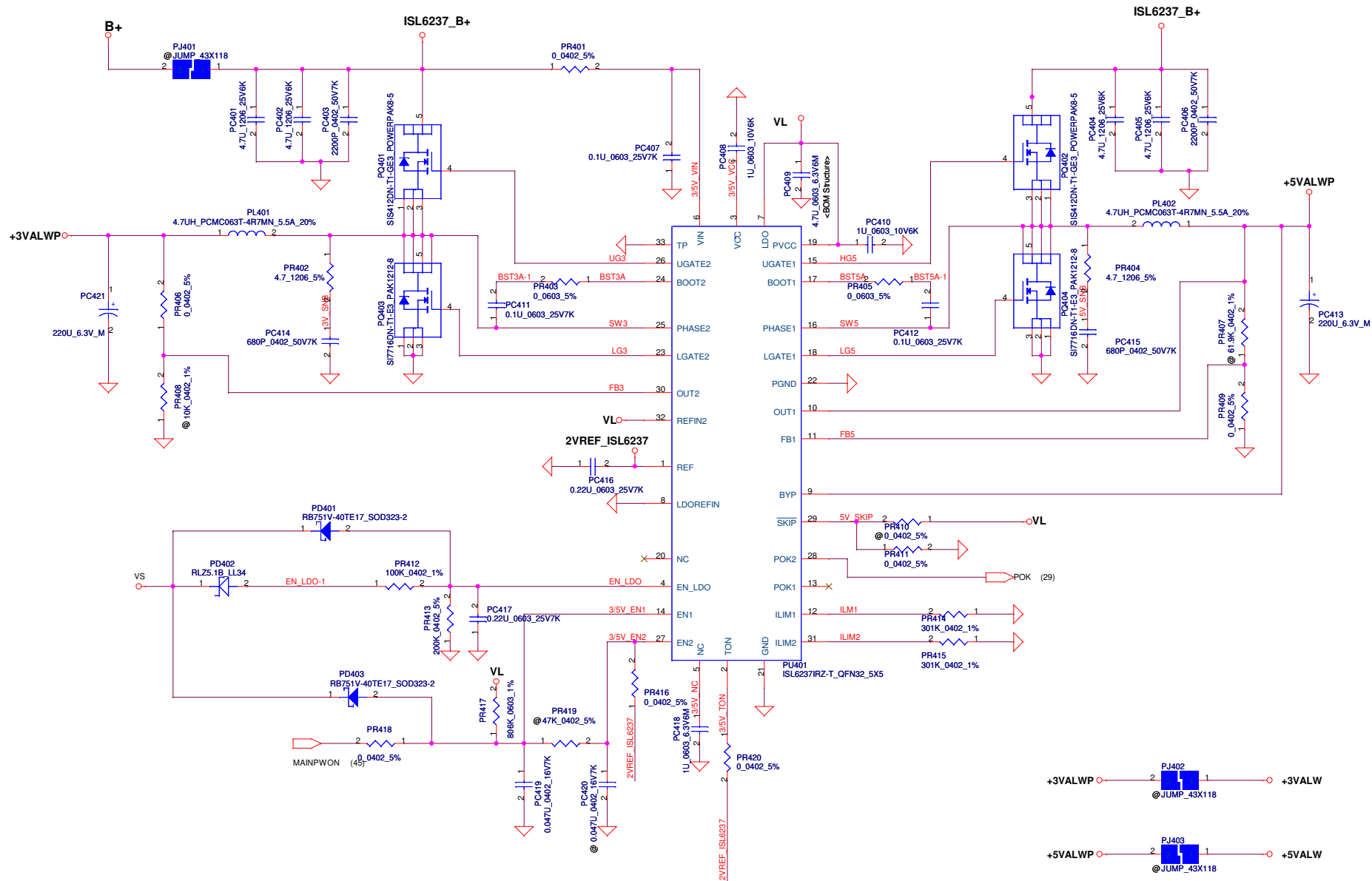


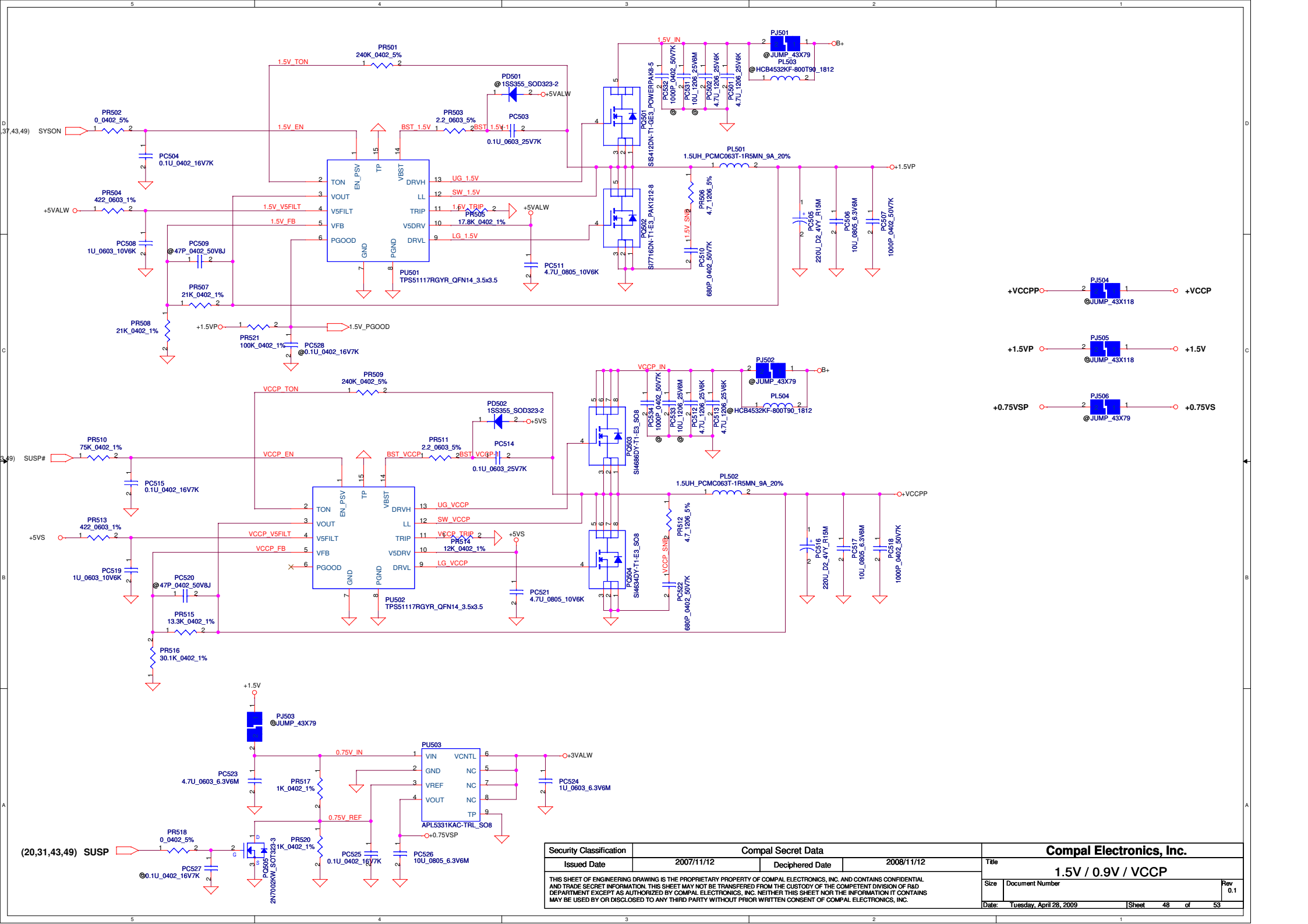
Vin Detector

High	17.944	17.706	17.470
Low	16.242	16.027	15.808









For N10M-GE1
GPIO15 GPIO20

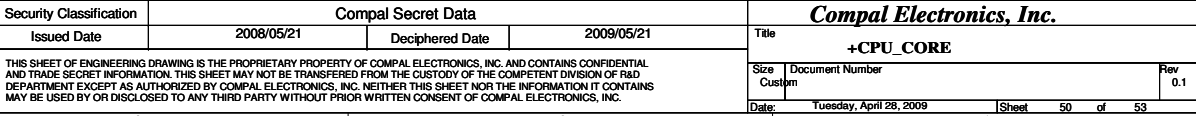
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.9V
1	1	1.0V

Security Classification	Compal Secret Data	
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2007/11/12		2008/11/12
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Compal Electronics, Inc.		
VGA_CORE/1.8V/1.1VS		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)	2009.01.14	
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			5	4	3	2	1
NO	DATE	PAGE	MODIFICATION LIST				PURPOSE
1	12/10	39	Remove D11, and add R6, R7				
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34				
2	1/15	39	modify H18 hold size, and change the H5、H6 and H18 hold type.				
		42	add 4 CAPs C3, C4, C5 and C6 for EMI.				
		35	change C572 and C574 footprint from 0603 to 0402.				
		34	add R25 for BEEP# test				
3	3/16	06	add R1089, C1162 and H_DPRSTP#_R				
			add C1163, C1164,and C1165 for EMC request.				
		08	change H_DPRSTP# to H_DPRSTP#_R				
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU				
			R999 change to 24.9K				
		23	add R1095 pull high				
		35	swap HP_OUTL and HP_OUTR				
		36	add R1090, R1091, R1092, R1093				
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R				
		41	add R256, R258 Bom configuration				
			Remove CY SMBus				
		42	add C1166, C1167 for EMC request.				
4	4/20	27	R829 changed to 0ohm.				
		08	R80 changed to 33ohm				
		34	R1044 changed to 33ohm				
			R1056 changed to 33ohm				
			C1089 changed to 10P				