

Compal Confidential

QAZ00 (Shuriken 13.3) M/B Schematics Document

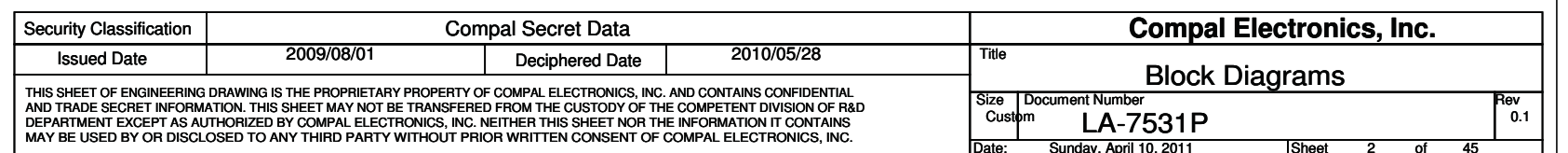
Intel Sandy Bridge ULV Processor with DDRIII + Cougar Point PCH SFF

LA-7531P

Date : 2011/04/10
Version 0.1 modify

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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2011/04/10



Voltage Rails

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

Device	Address
DDR DIMM0	1010 0000b
Mini Card1	
Mini Card2	
Mini Card3	

SMBUS Control Table

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
	UHCI1	2	
		3	Camera
	UHCI2	4	Mini Card(WLAN)
		5	WWAN (3G)
	UHCI3	6	
		7	mSATA
EHCI2	UHCI4	8	
		9	USB/B (Right Side)
	UHCI5	10	
		11	
	UHCI6	12	
		13	

USB 3.0	Port	2 External USB Port
	1	
	2	USB/B (Right Side)
	3	
	4	

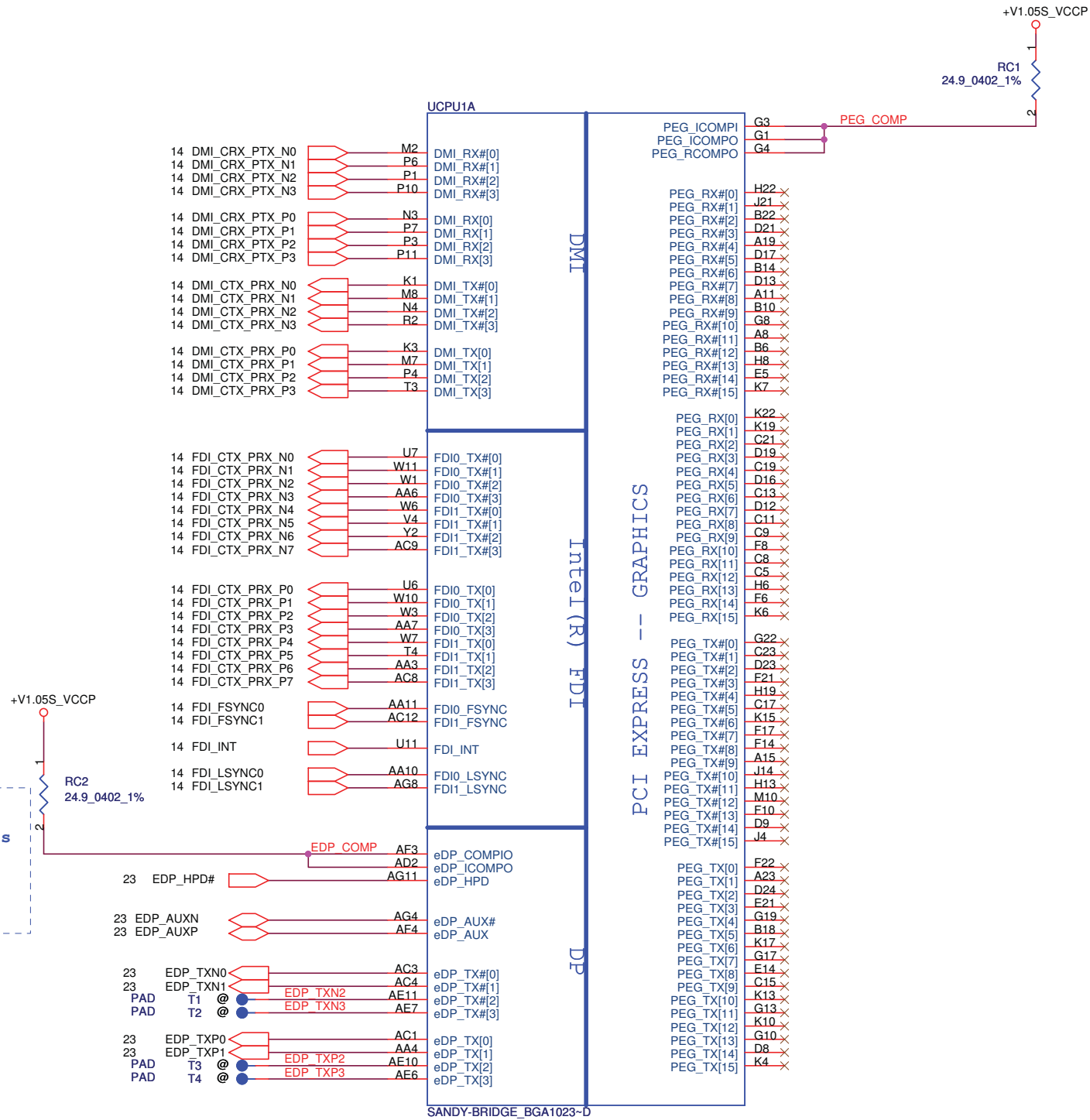
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None	Symbol Note :  : means Digital Ground  : means Analog Ground	
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Option	@		HDMI@		EMI@
UMA	X	X	V	X	X

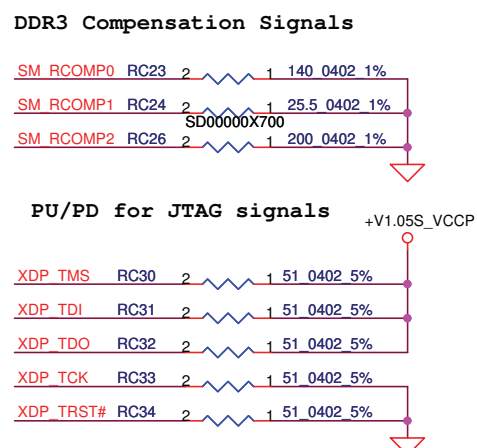
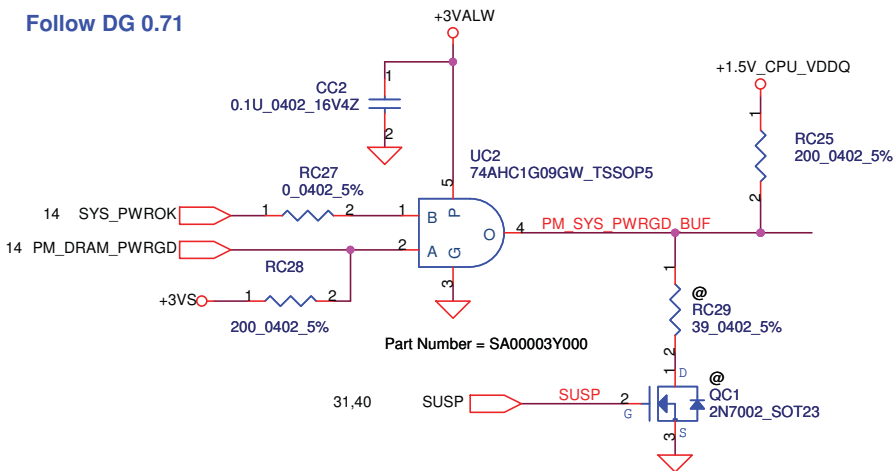
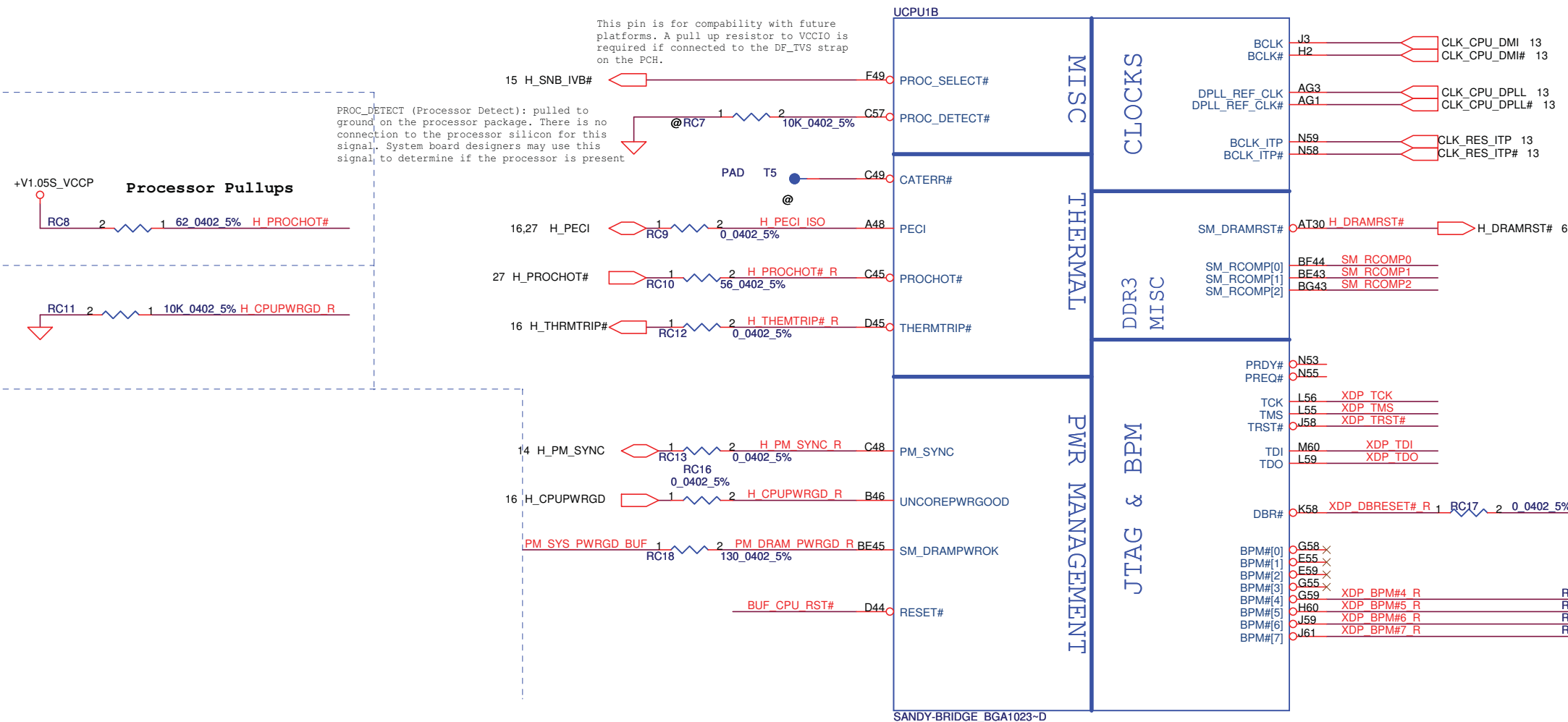
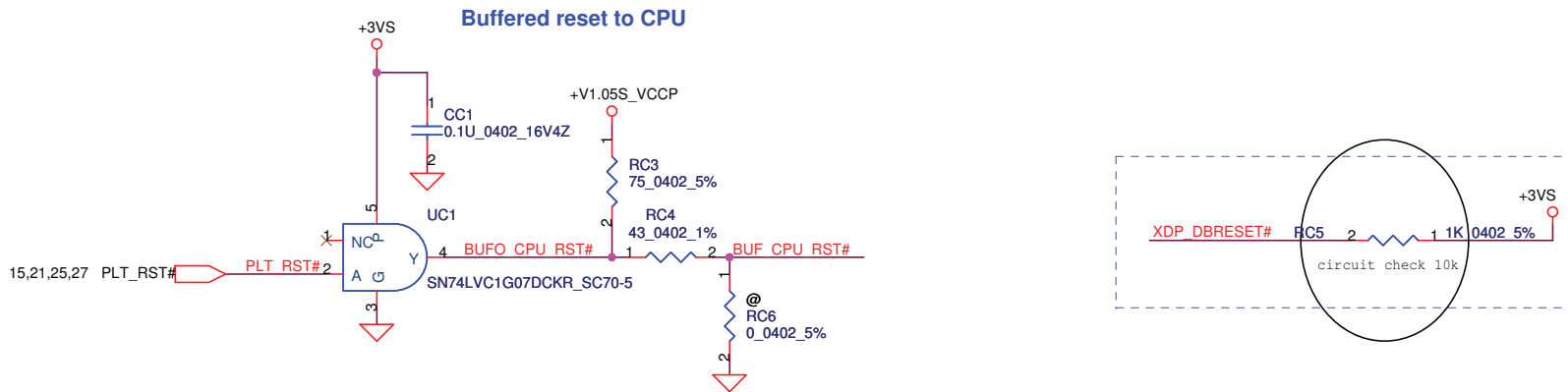
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eDP_COMPPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

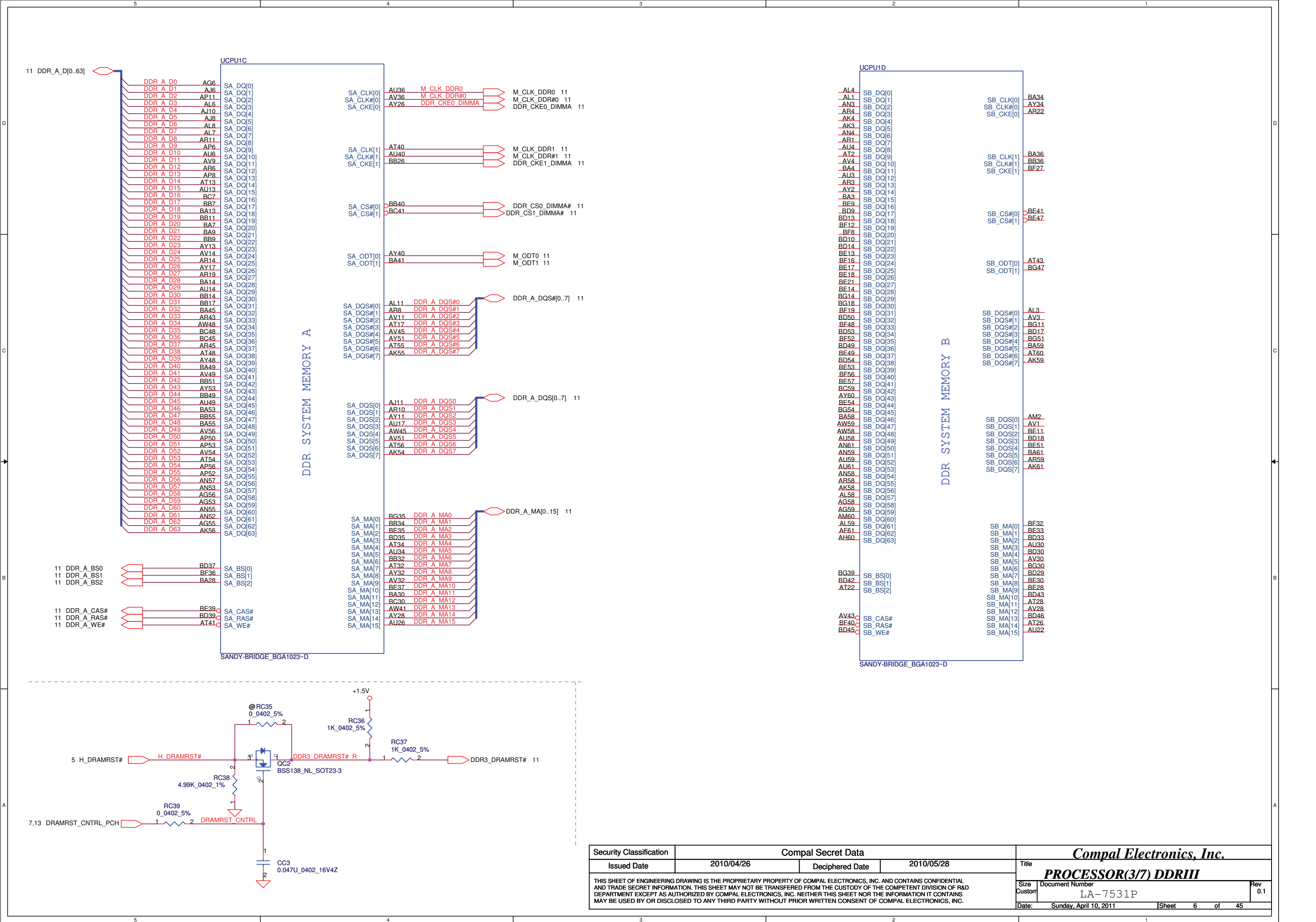
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

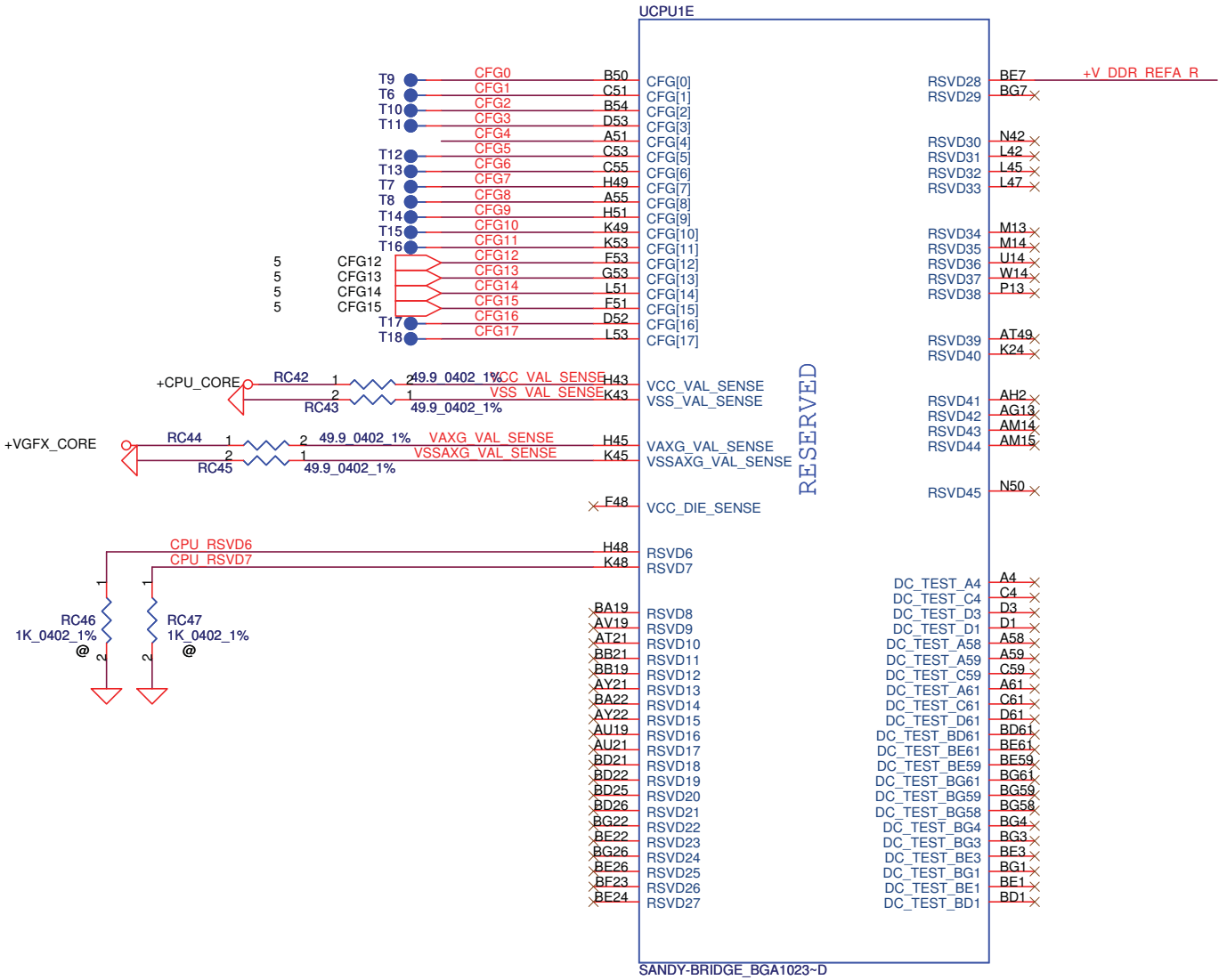
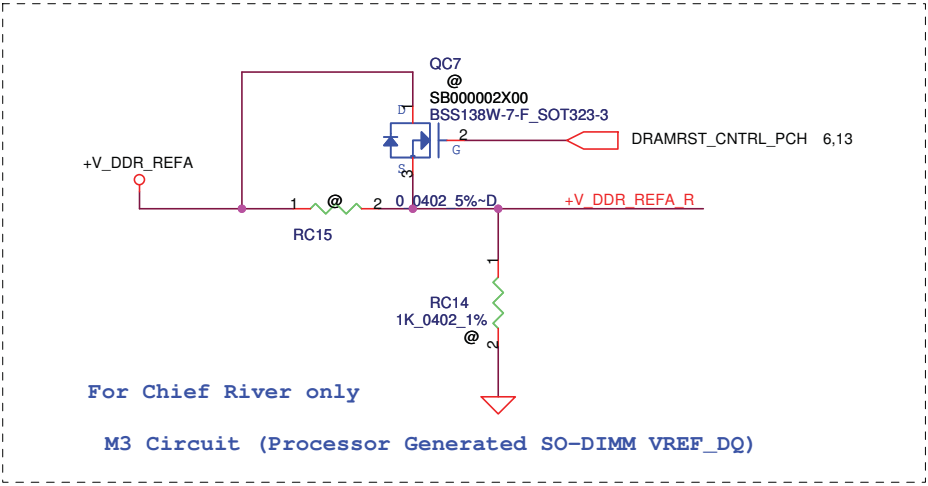


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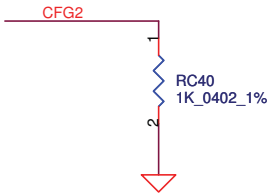


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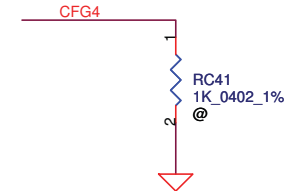




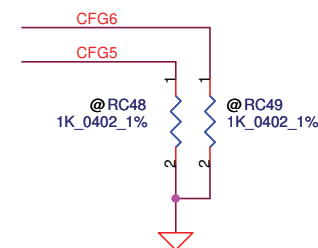
CFG Straps for Processor



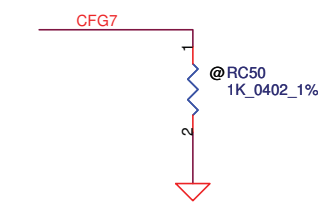
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



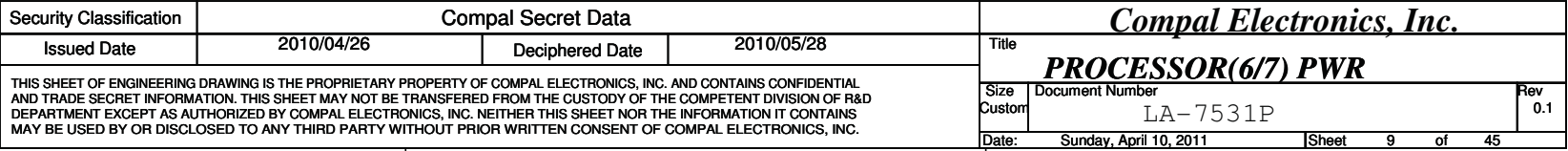
Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

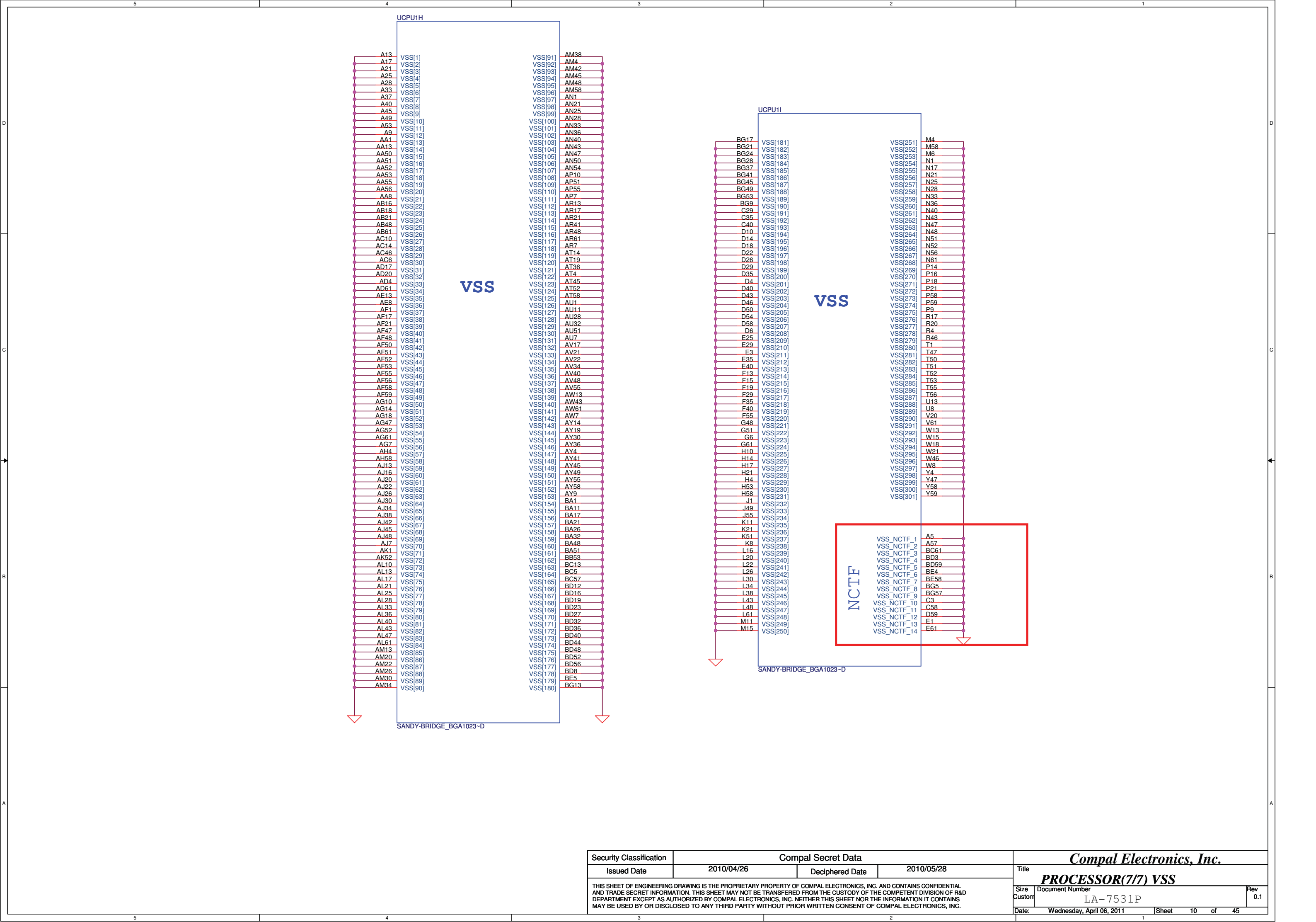


PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



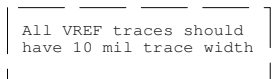
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



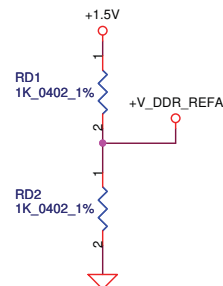


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Issued Date	2010/04/26	Deciphered Date	2010/05/28	Title PROCESSOR(7/7) VSS	
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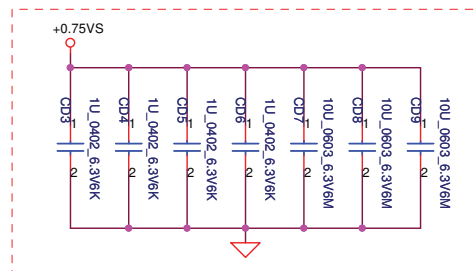
TOP SLOT



Delete DDR_A_DM[0..7]

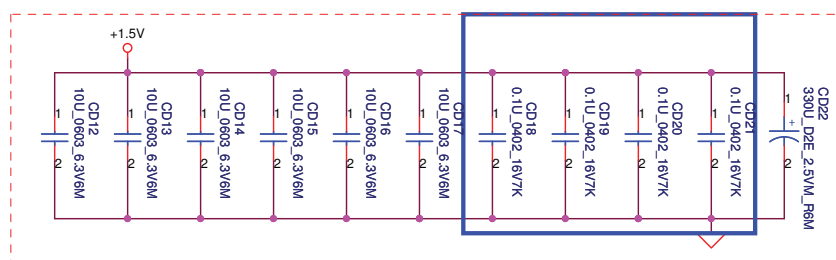


Layout Note:
Place near JDIMM1.203 & JDIMM1.204

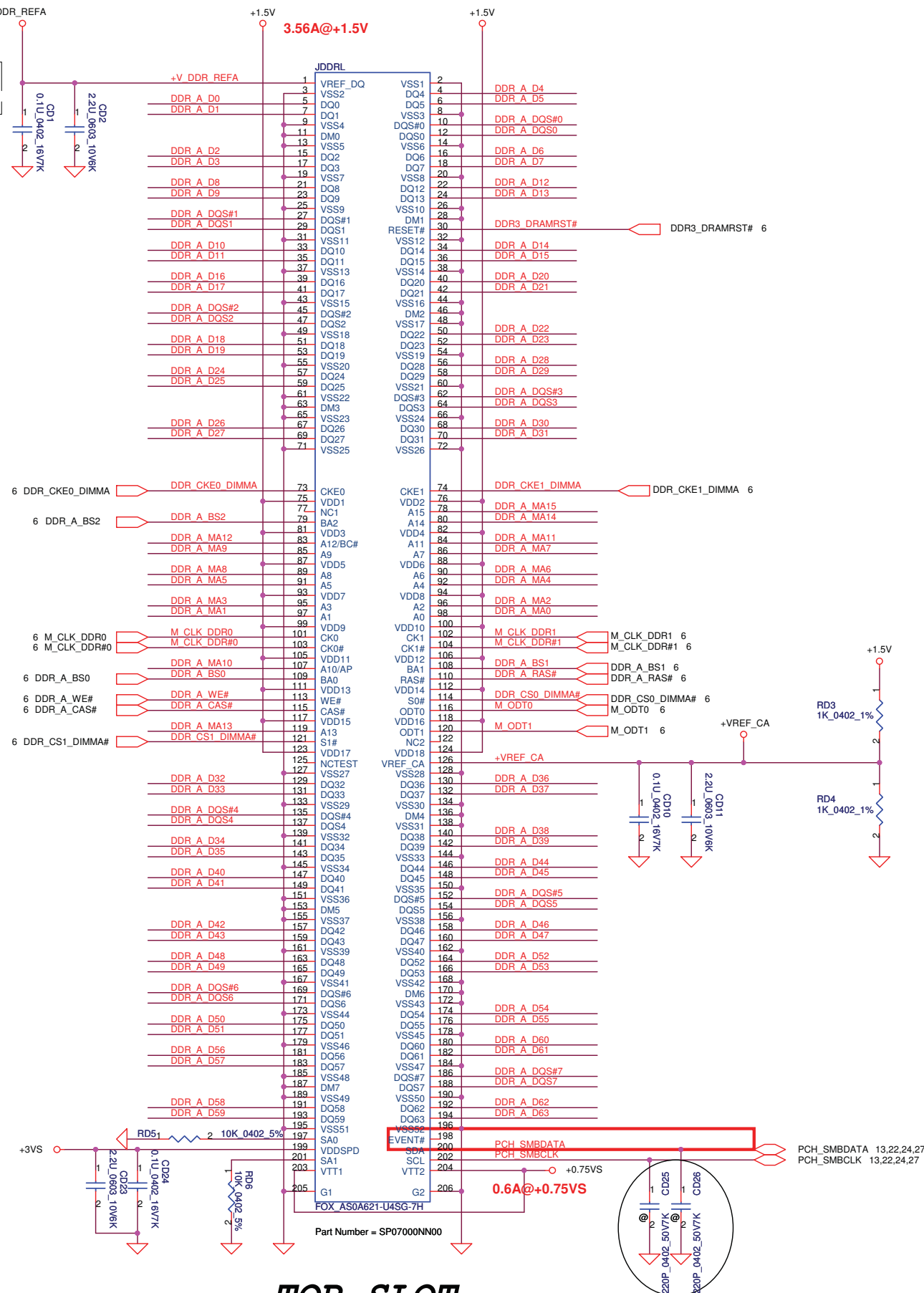


Layout Note:
Place near JDIMM1

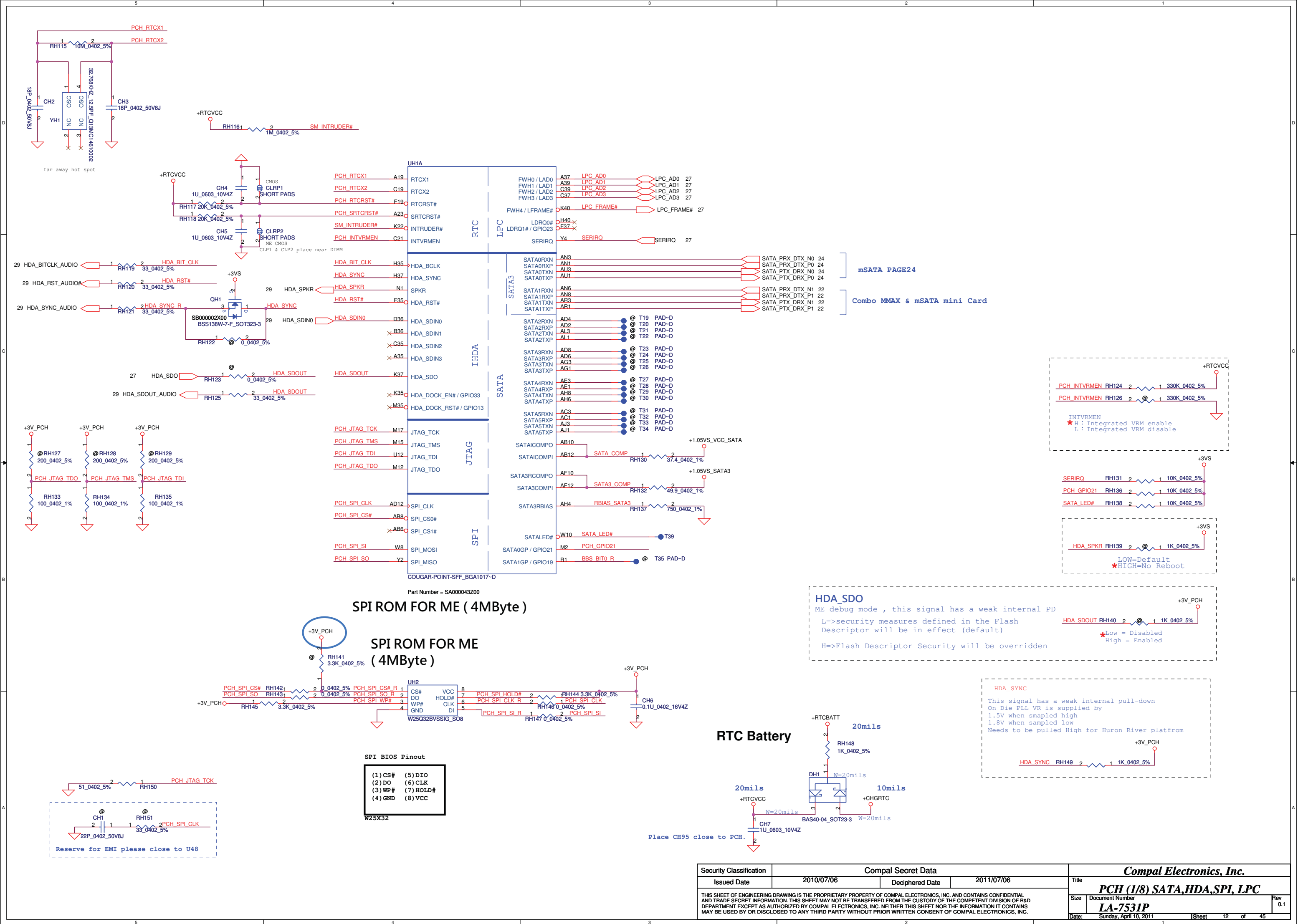
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

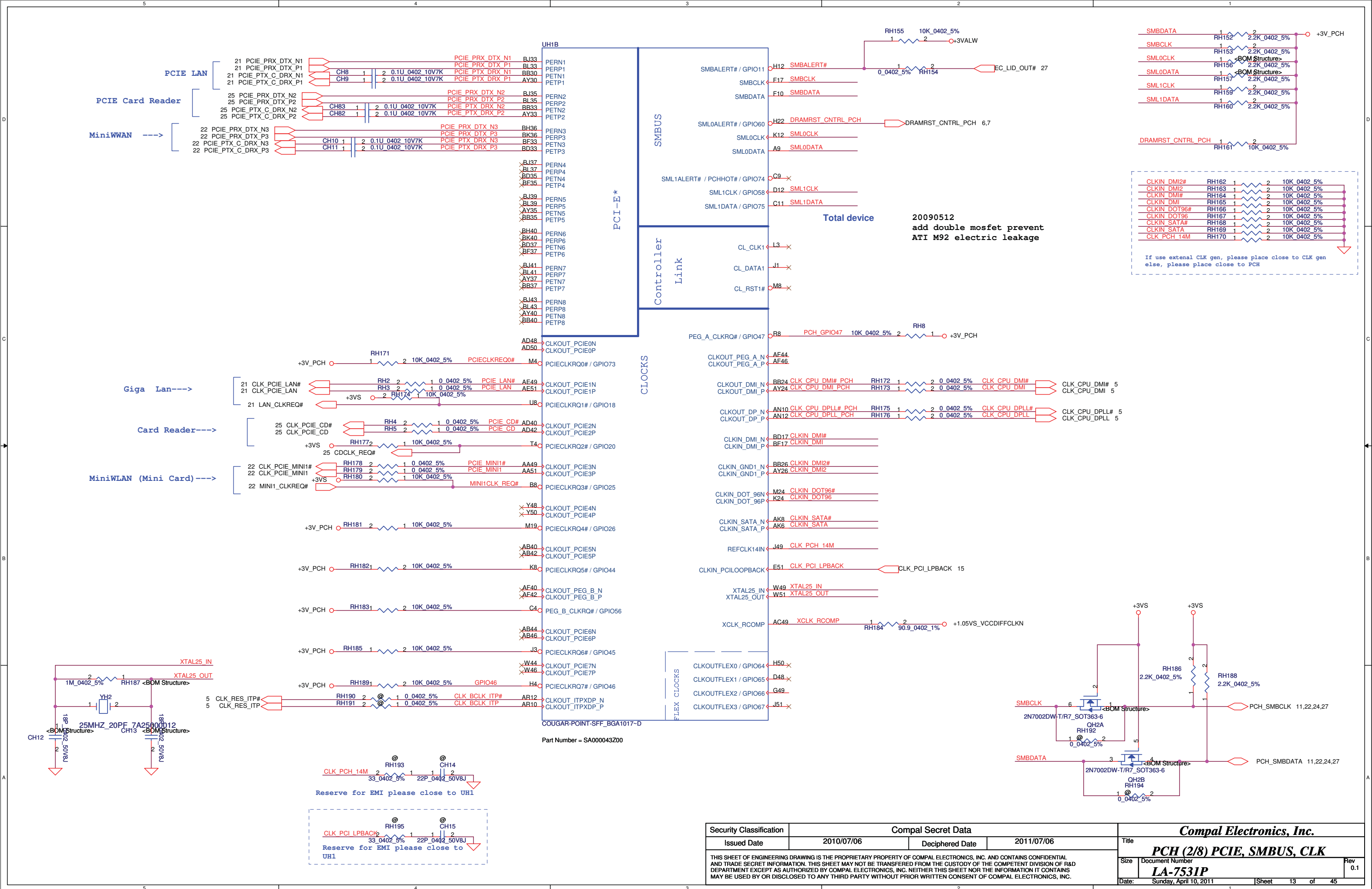


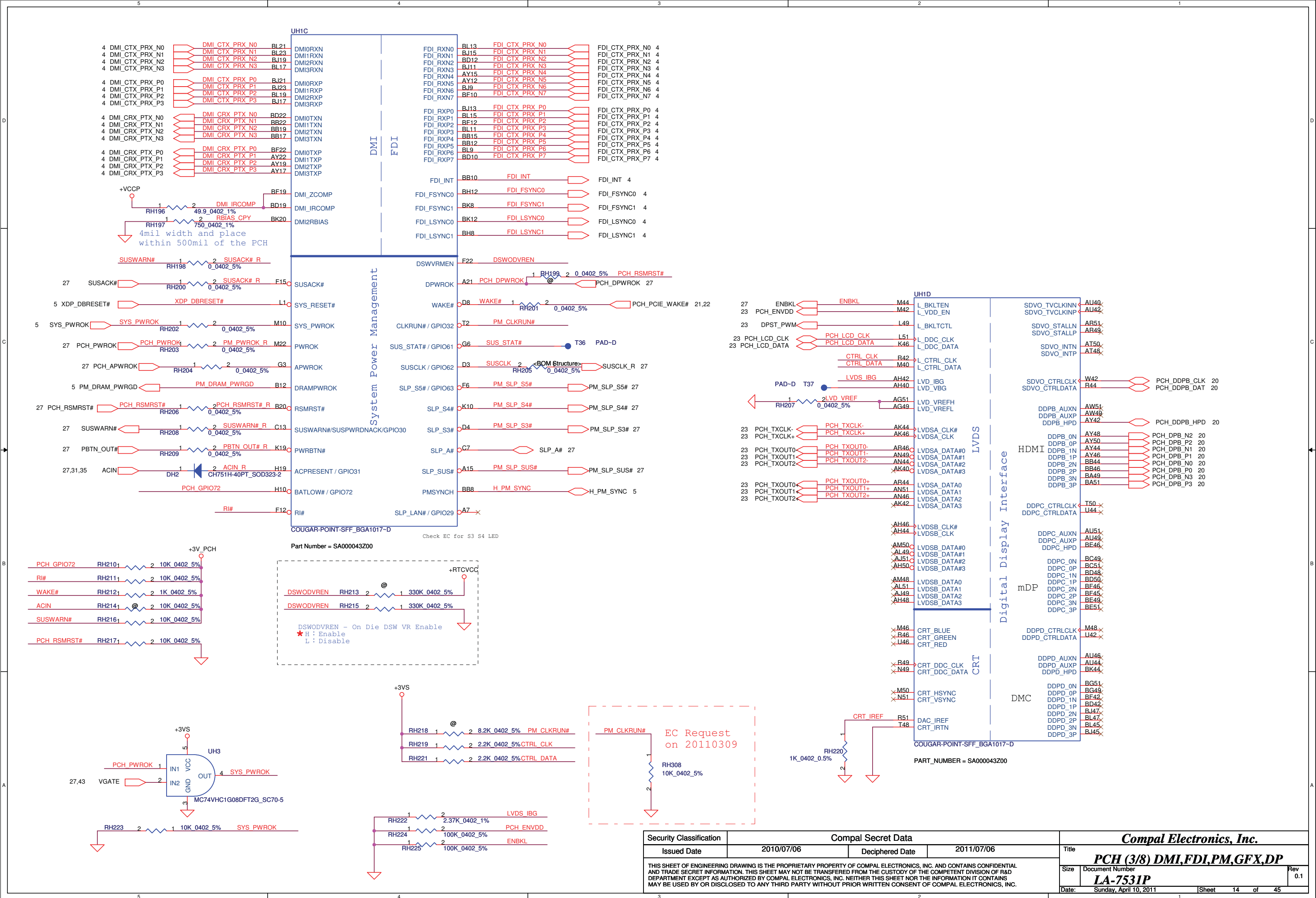
DDR3 SO-DIMM A

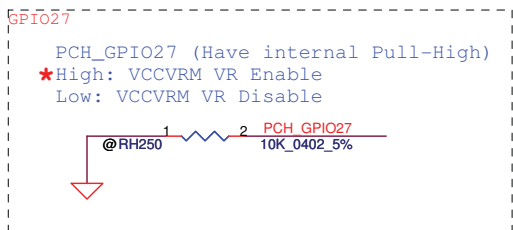
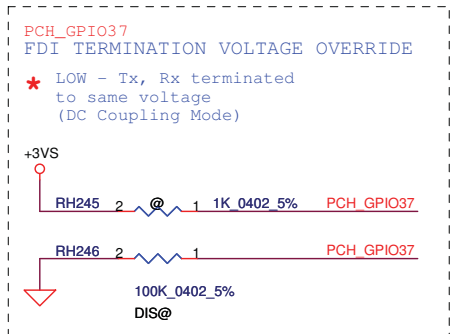
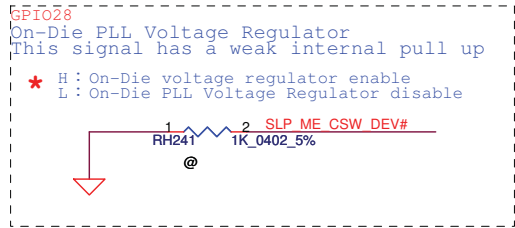


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				DDRIII DIMM	
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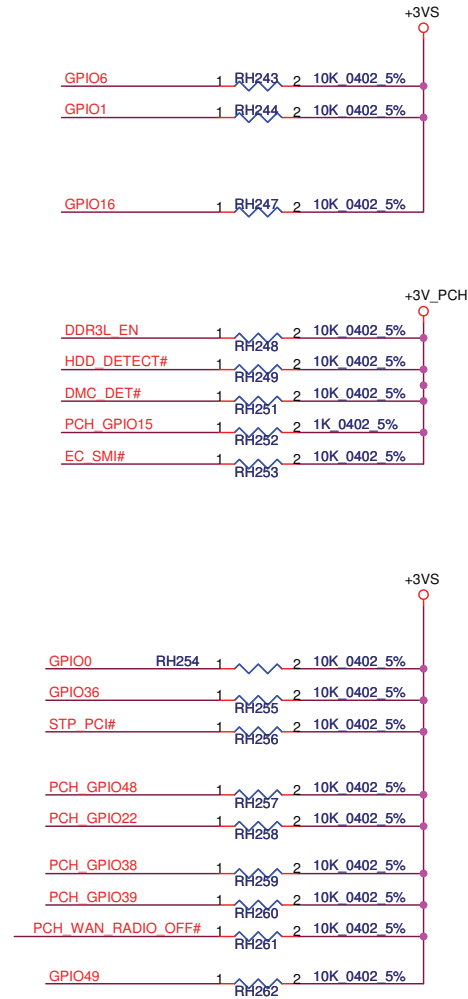




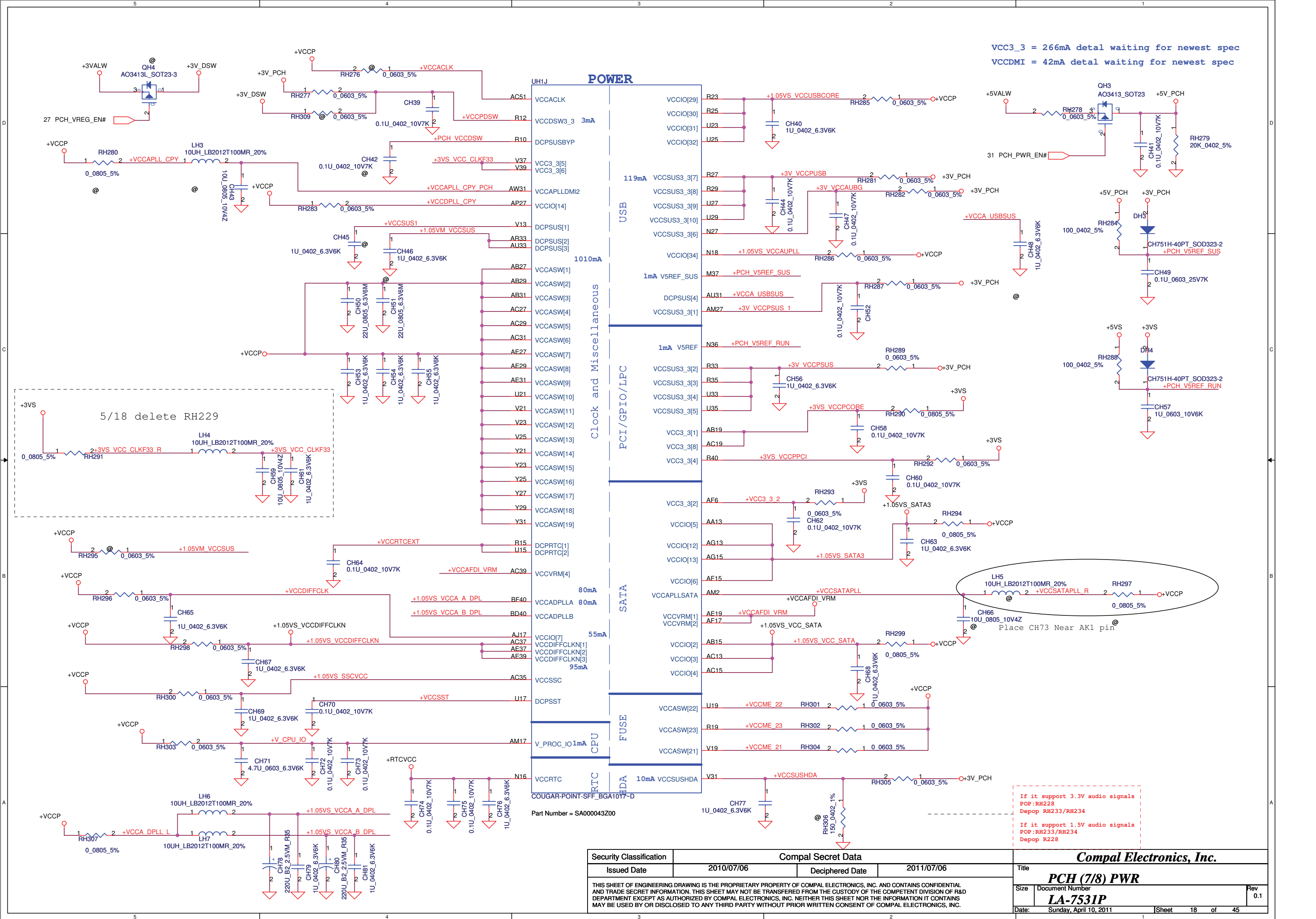


PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5



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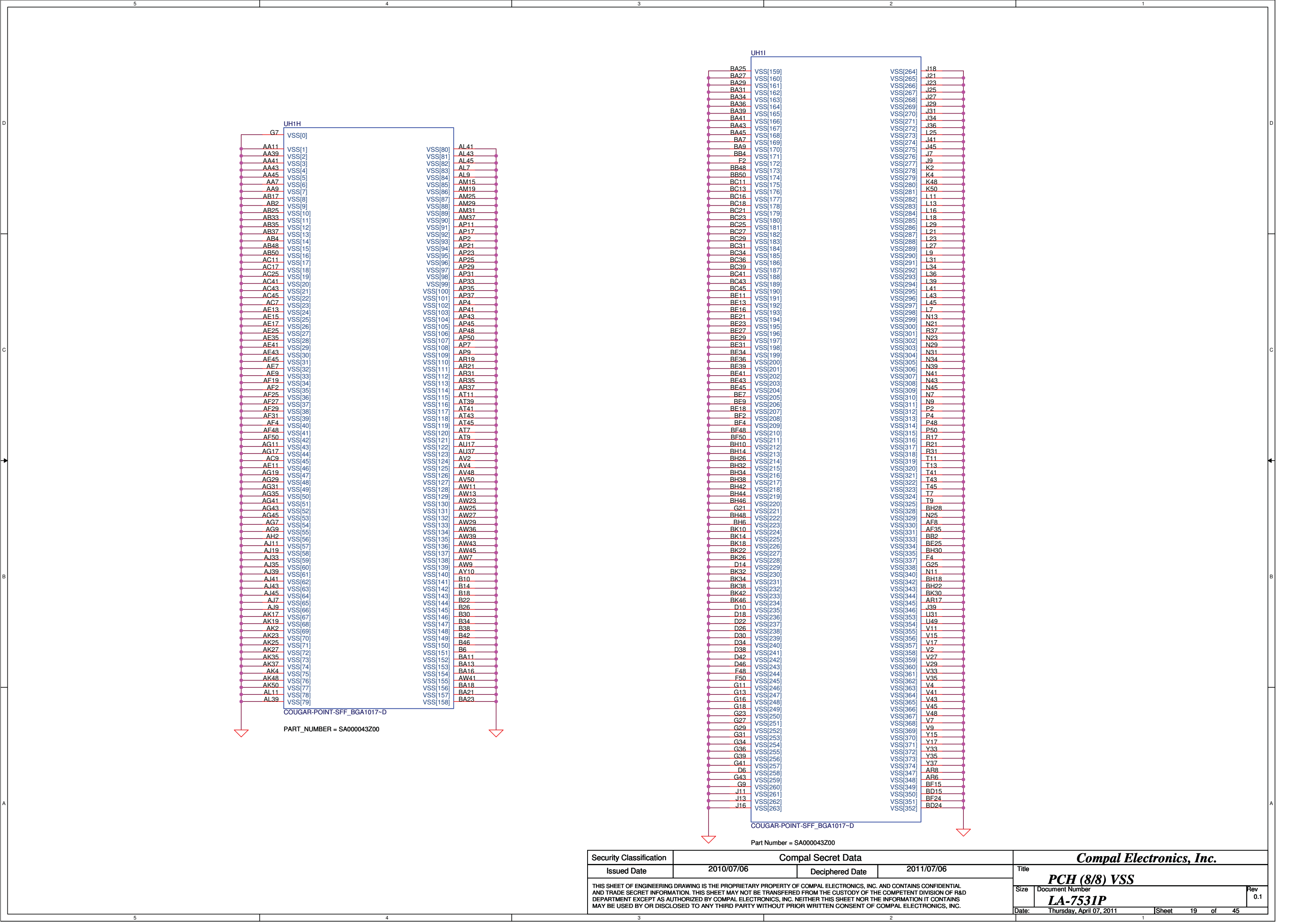


VCC3_3 = 266mA detail waiting for newest spec
VCCDMI = 42mA detail waiting for newest spec

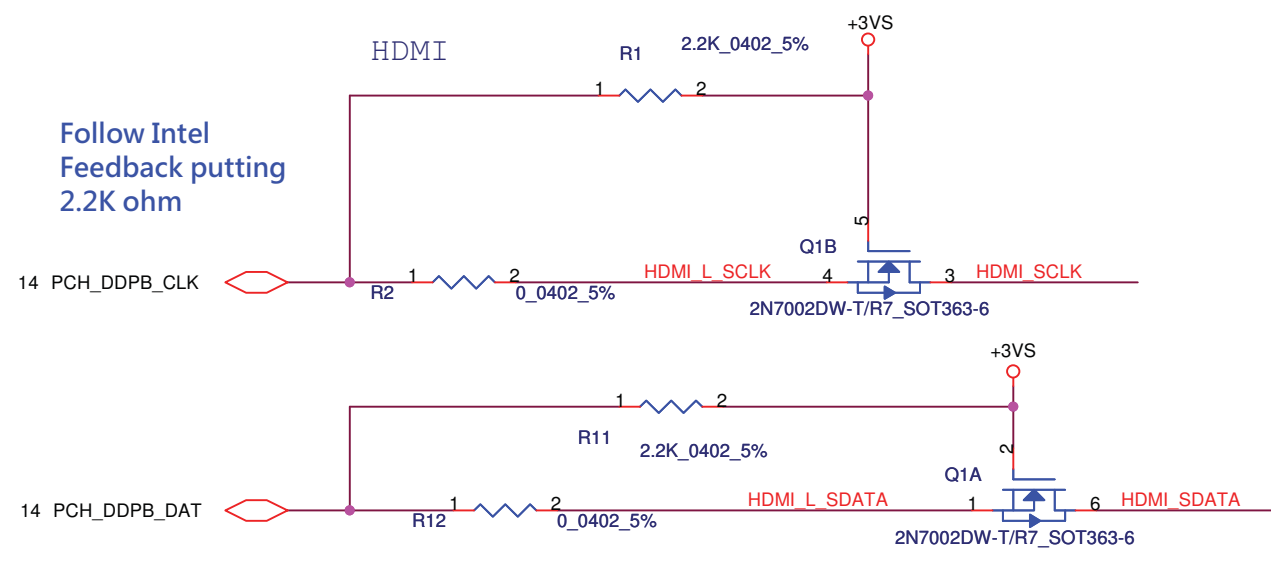
If it support 3.3V audio signals
POP: RH228
Depop RH233/RH234

If it support 1.5V audio signals
POP: RH233/RH234
Depop R228

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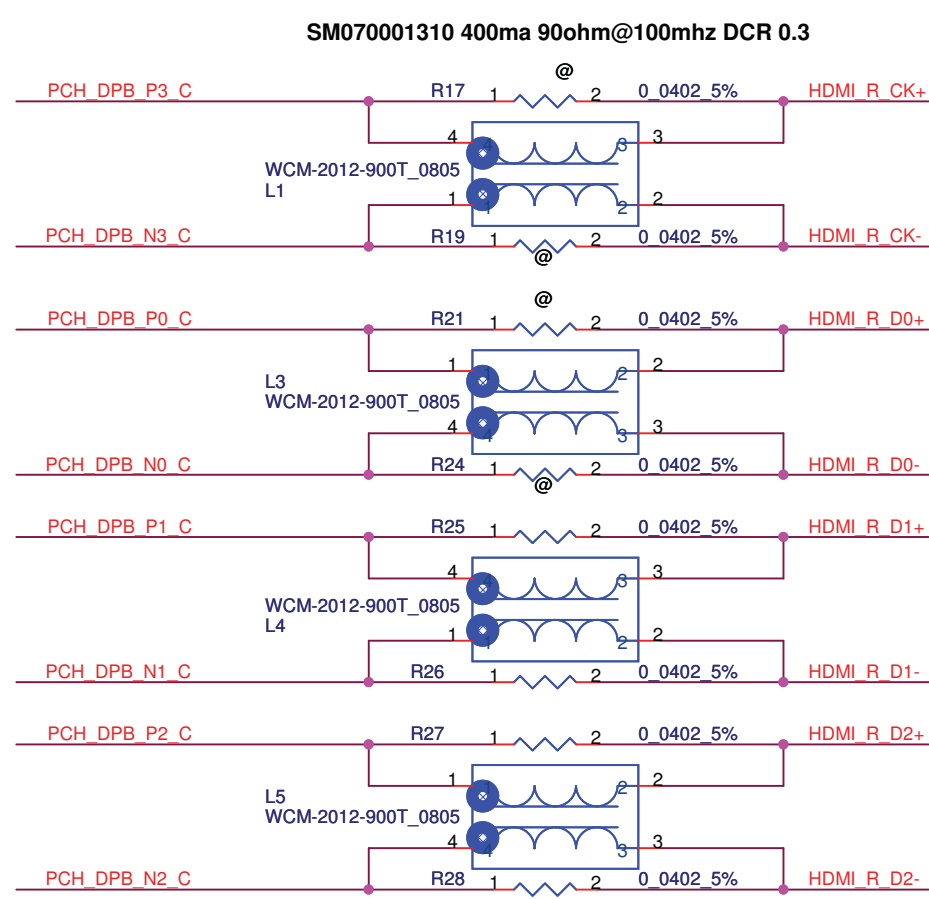
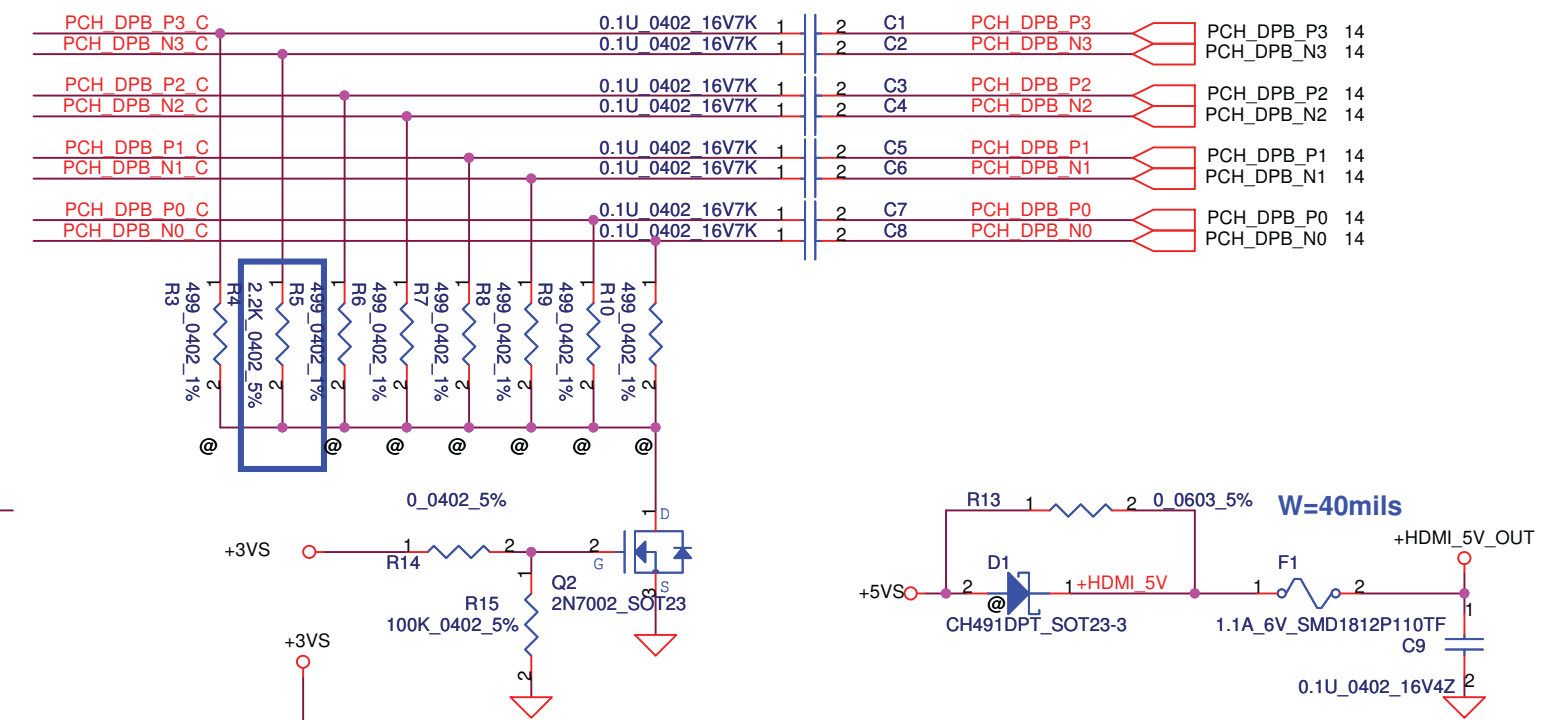


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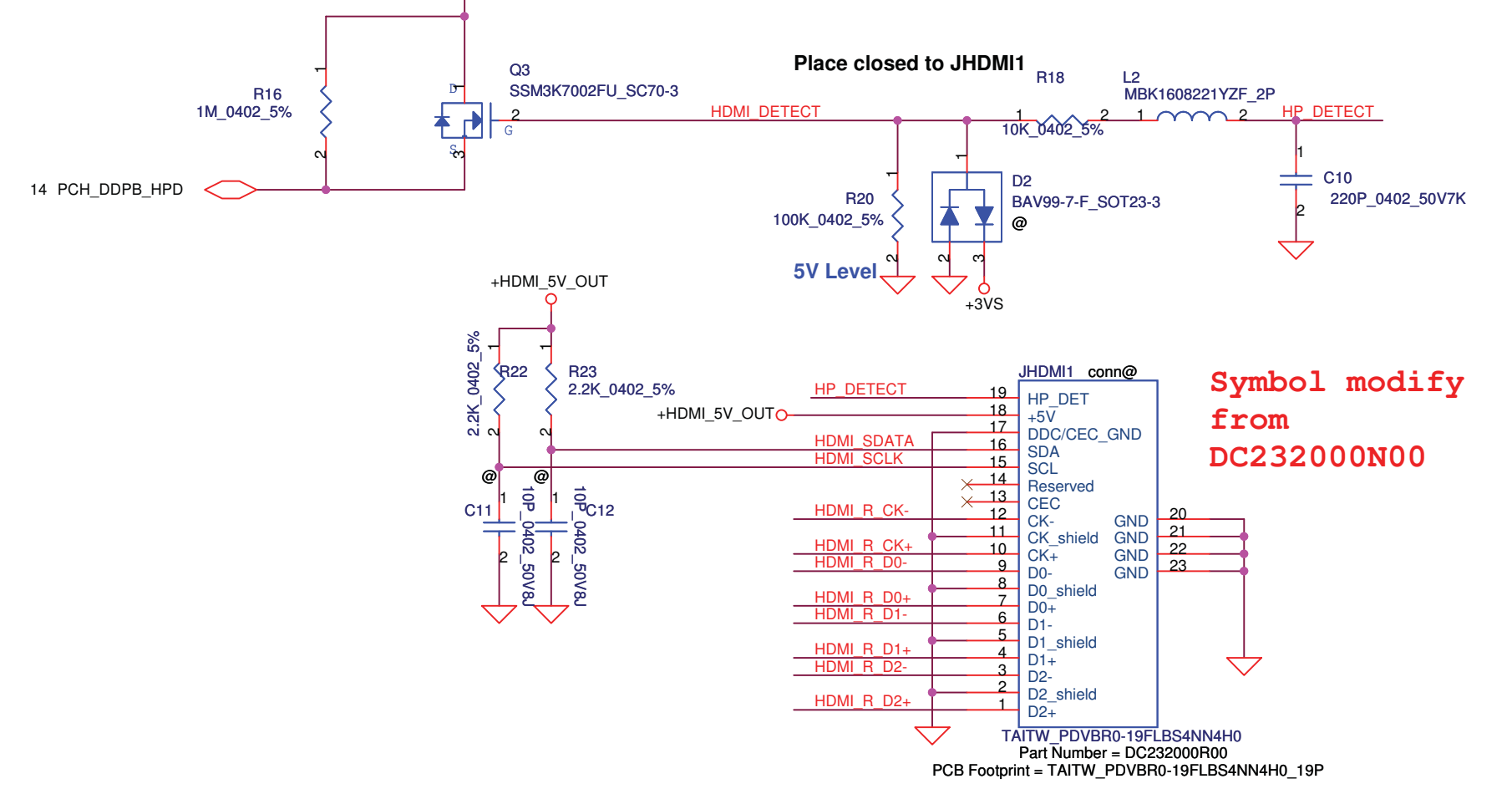


Follow Intel
Feedback putting
2.2K ohm

5V PULL UP IN CONNECTER SIDE



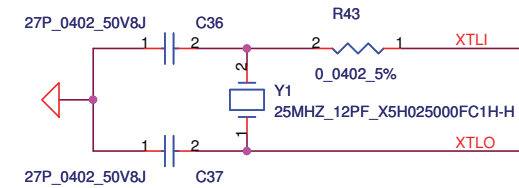
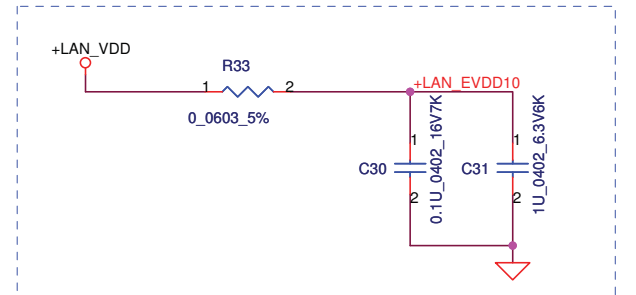
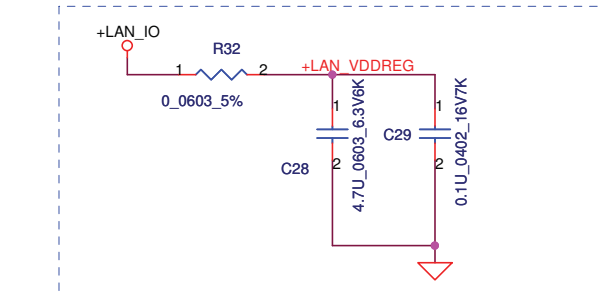
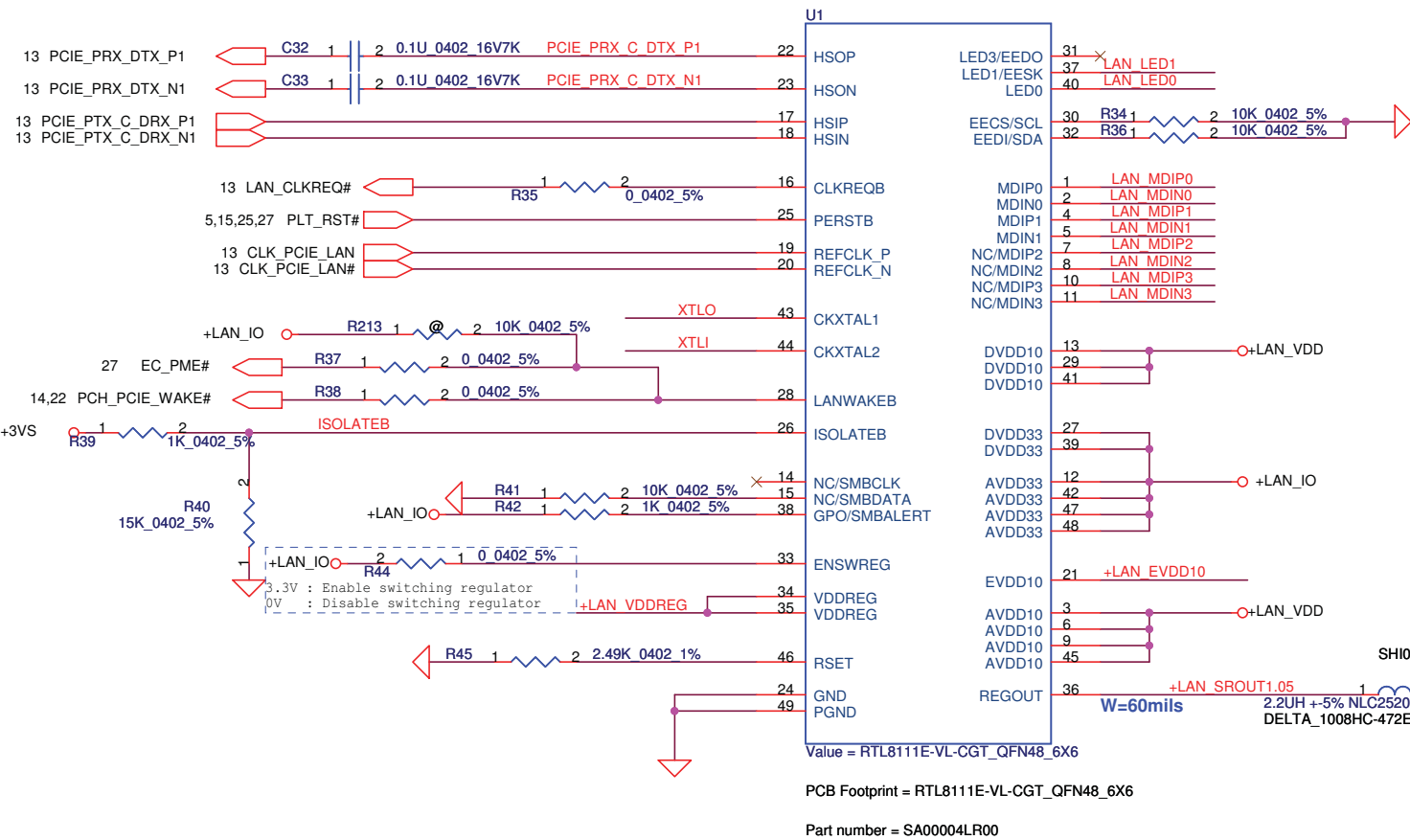
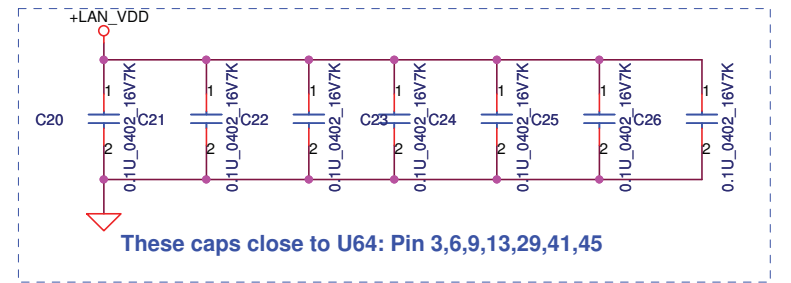
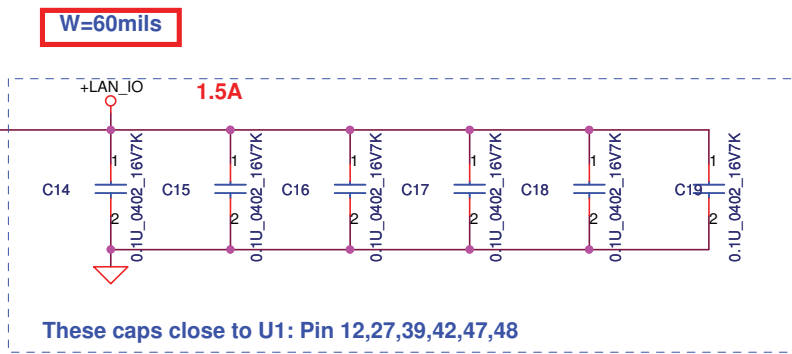
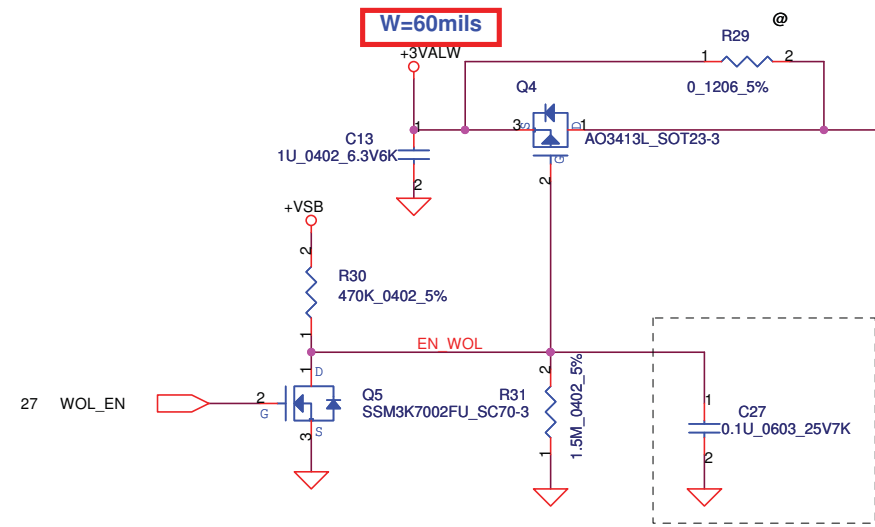
SM070001310 400ma 90ohm@100mhz DCR 0.3



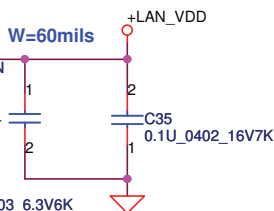
Place closed to JHDMI1

Symbol modify
from
DC232000N00

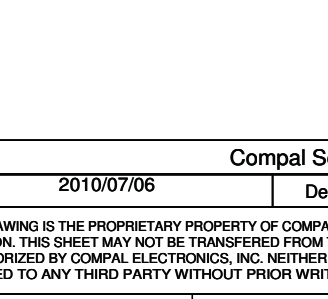
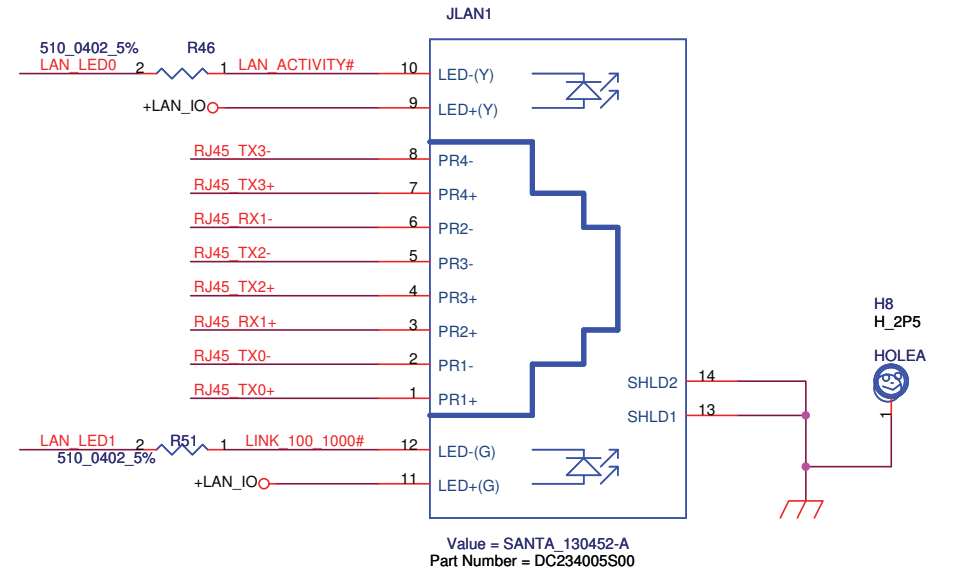
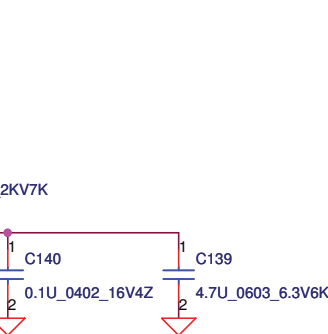
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	HDMI Conn	
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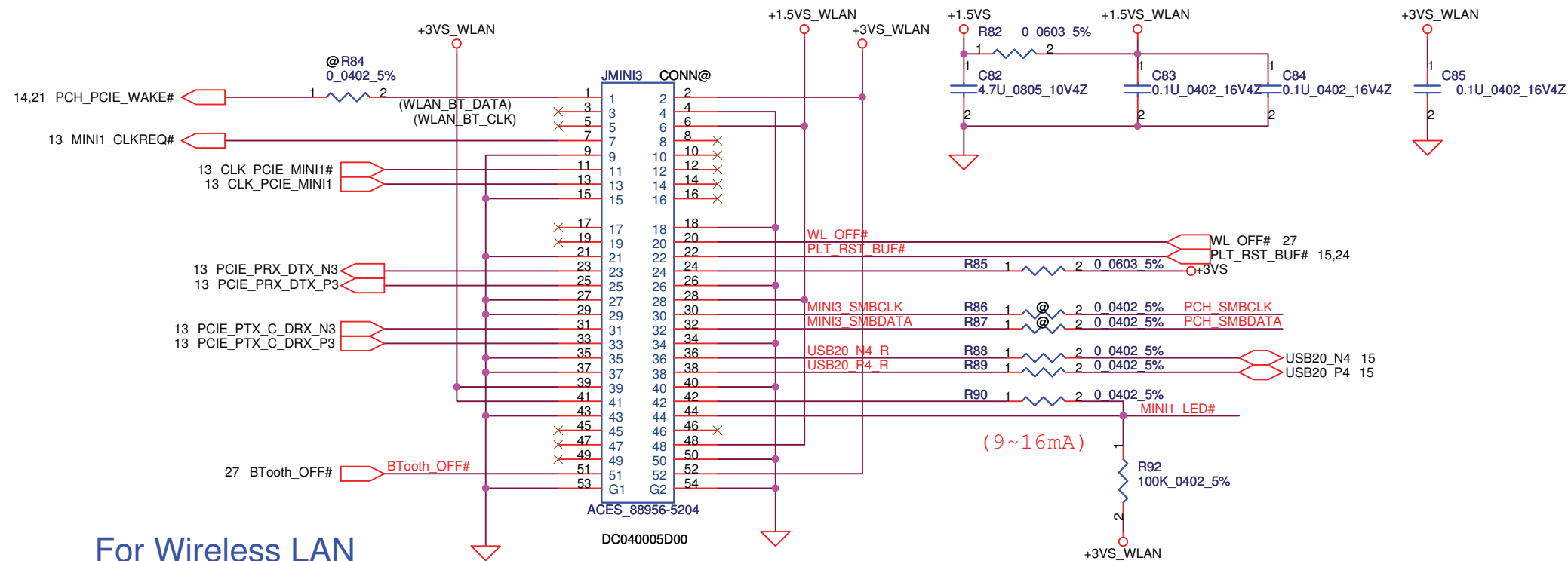
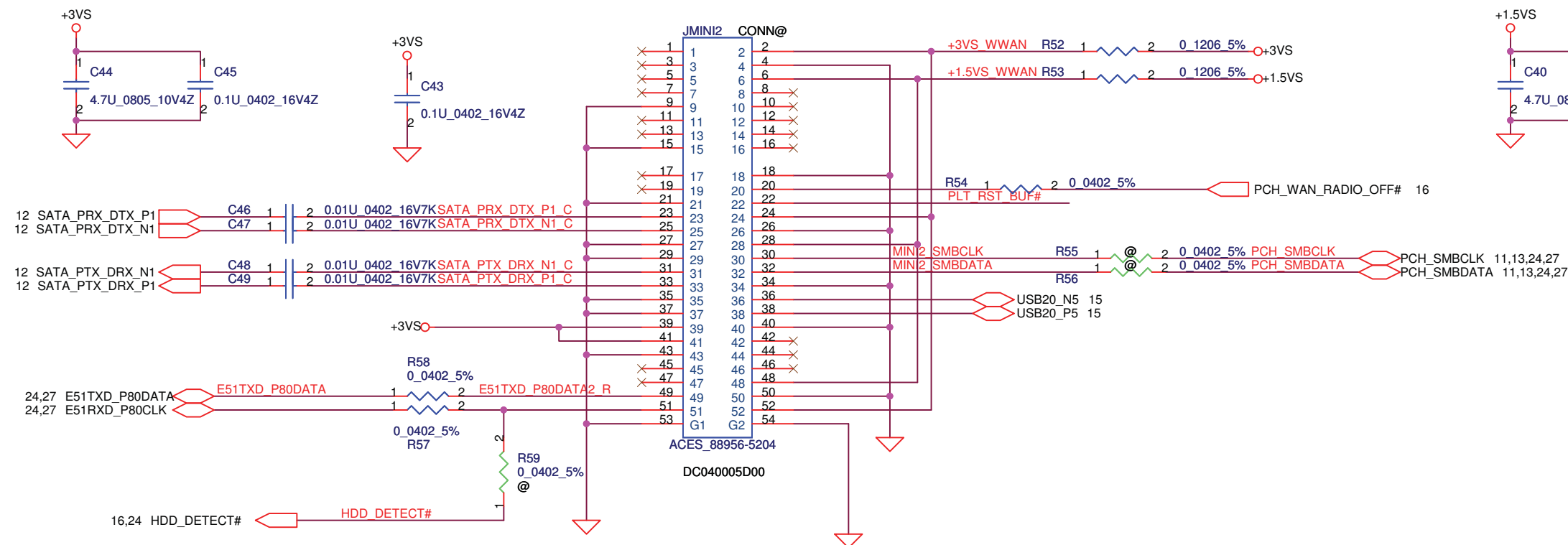
H_2P5 (6.0)



These components close to U44: Pin 36
(Should be place within 200 mils)

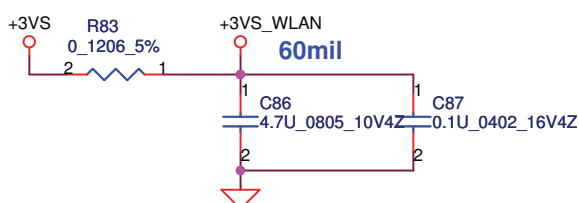


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				Sheet 21 of 45



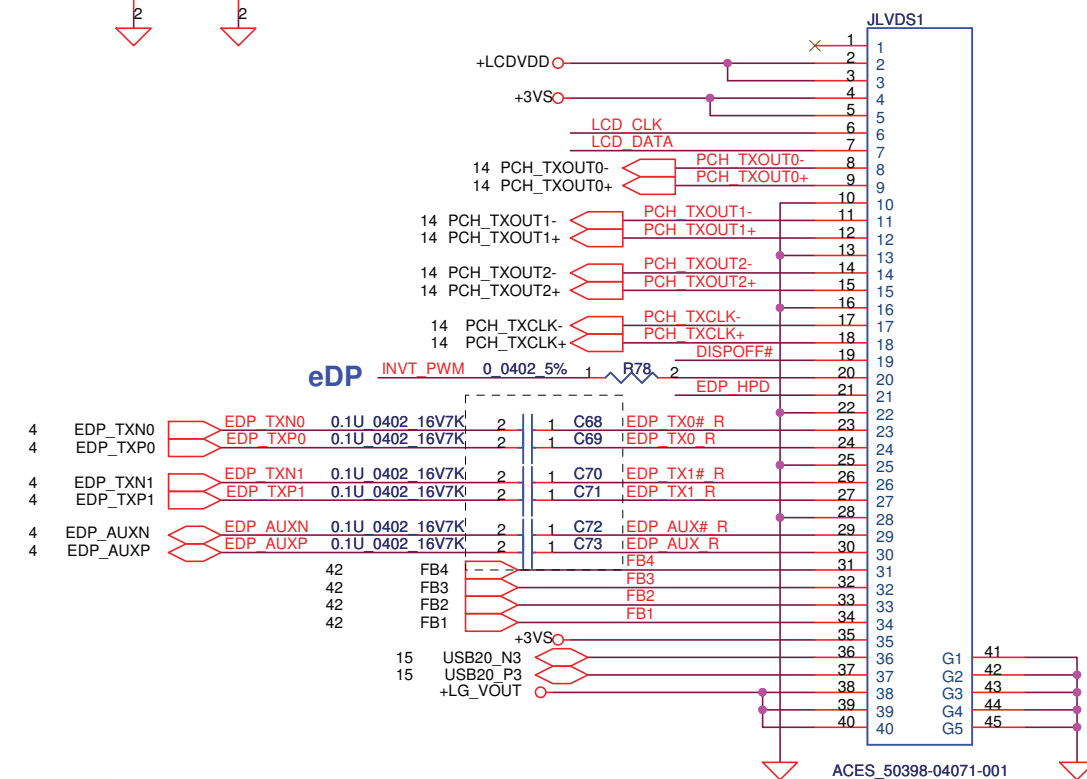
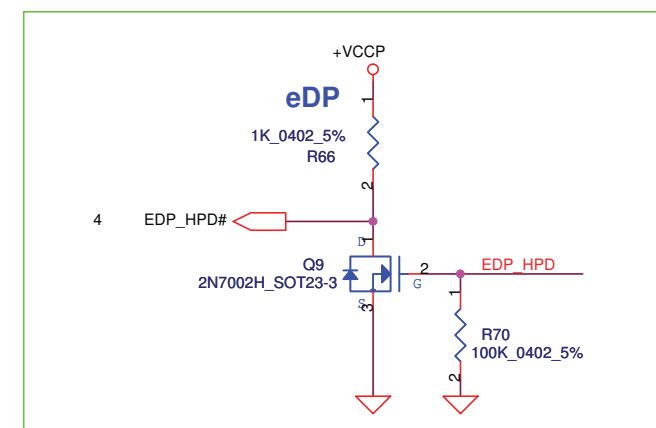
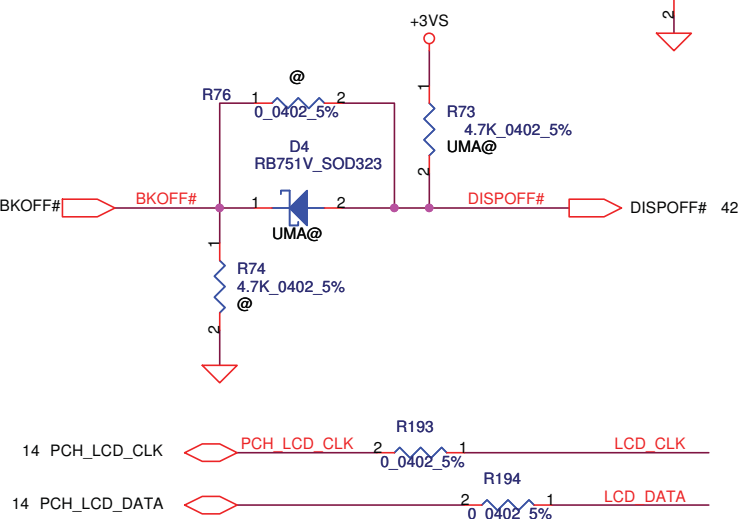
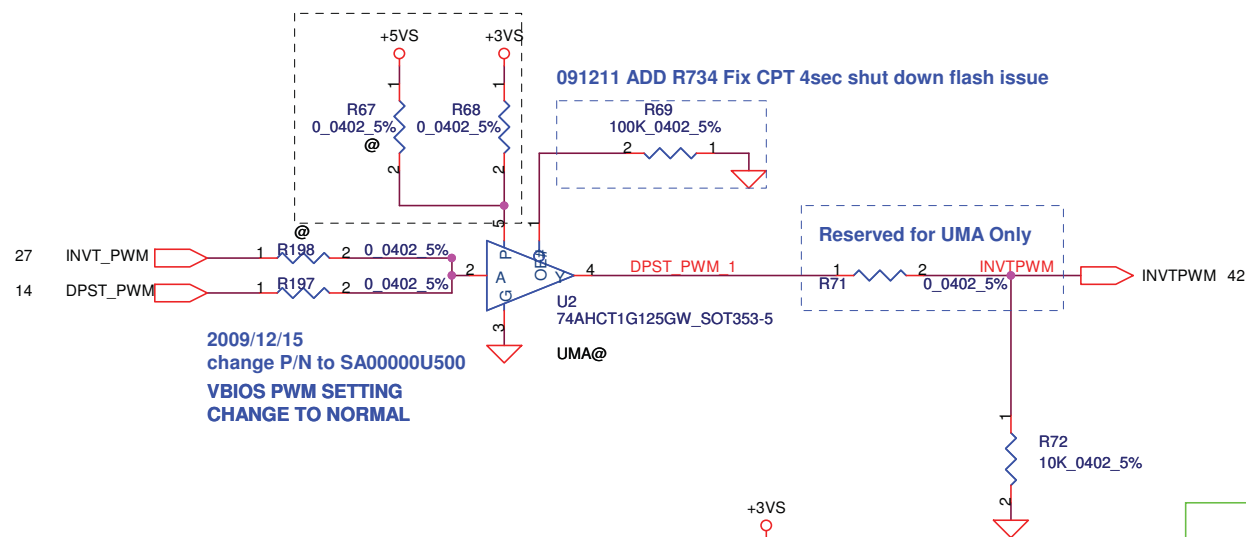
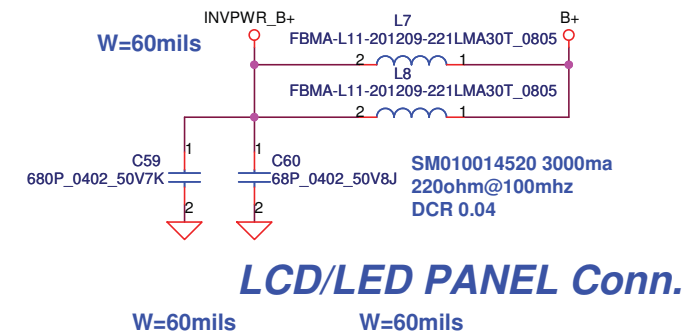
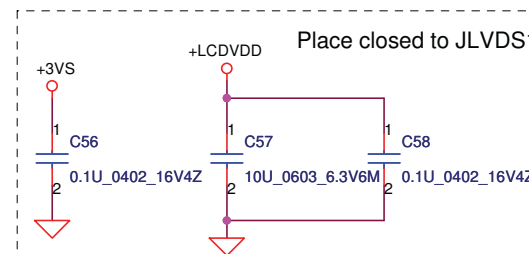
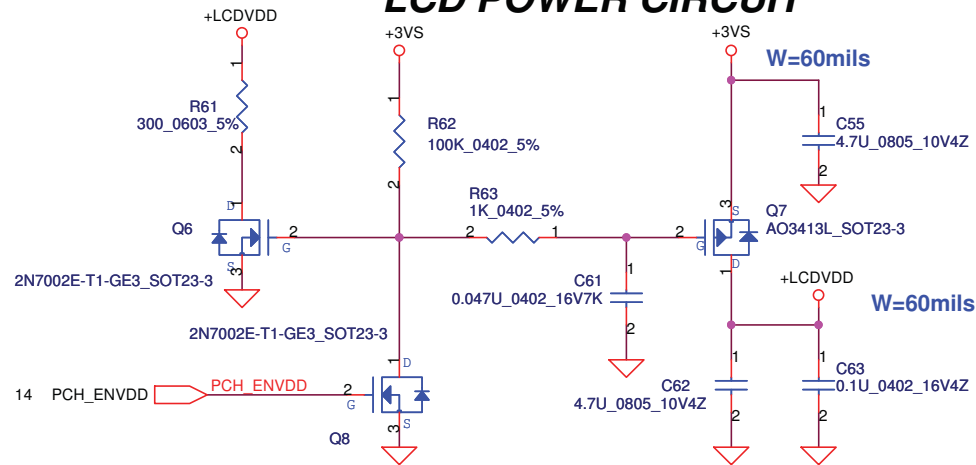
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For Wireless LAN



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				Size	Document Number	Rev
					LA-7531P	0.1
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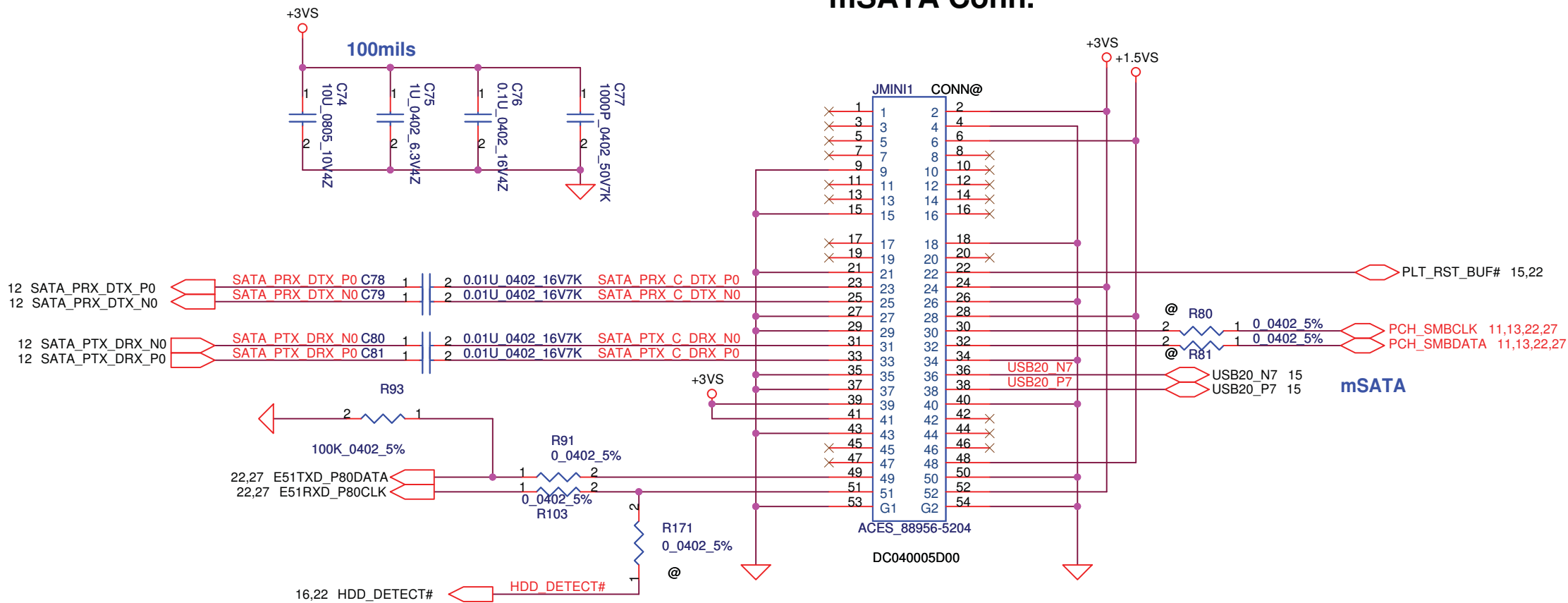
LCD POWER CIRCUIT



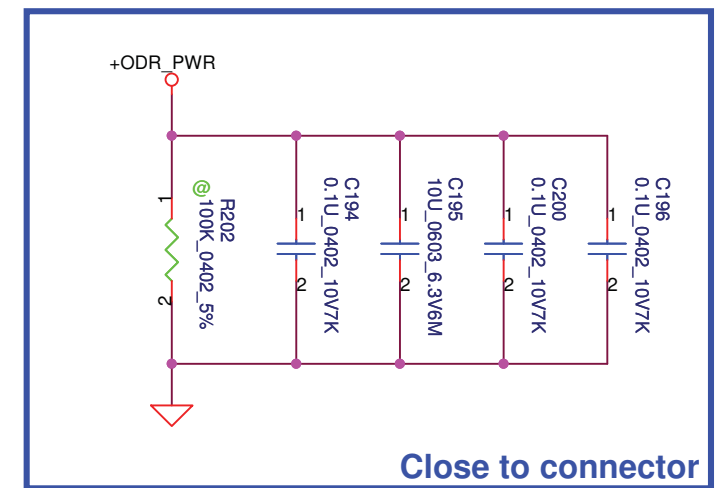
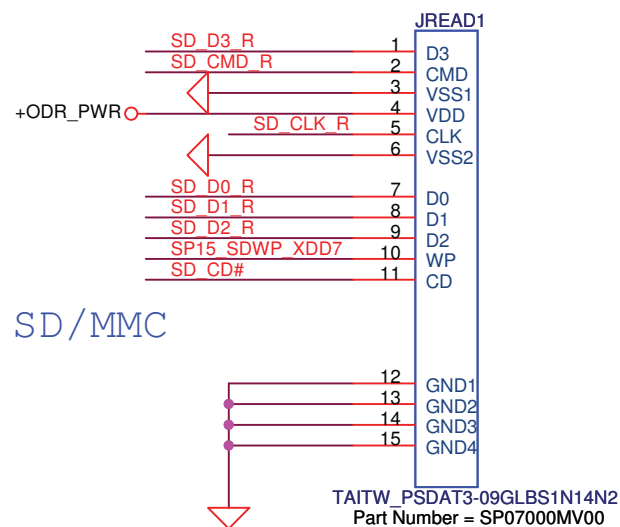
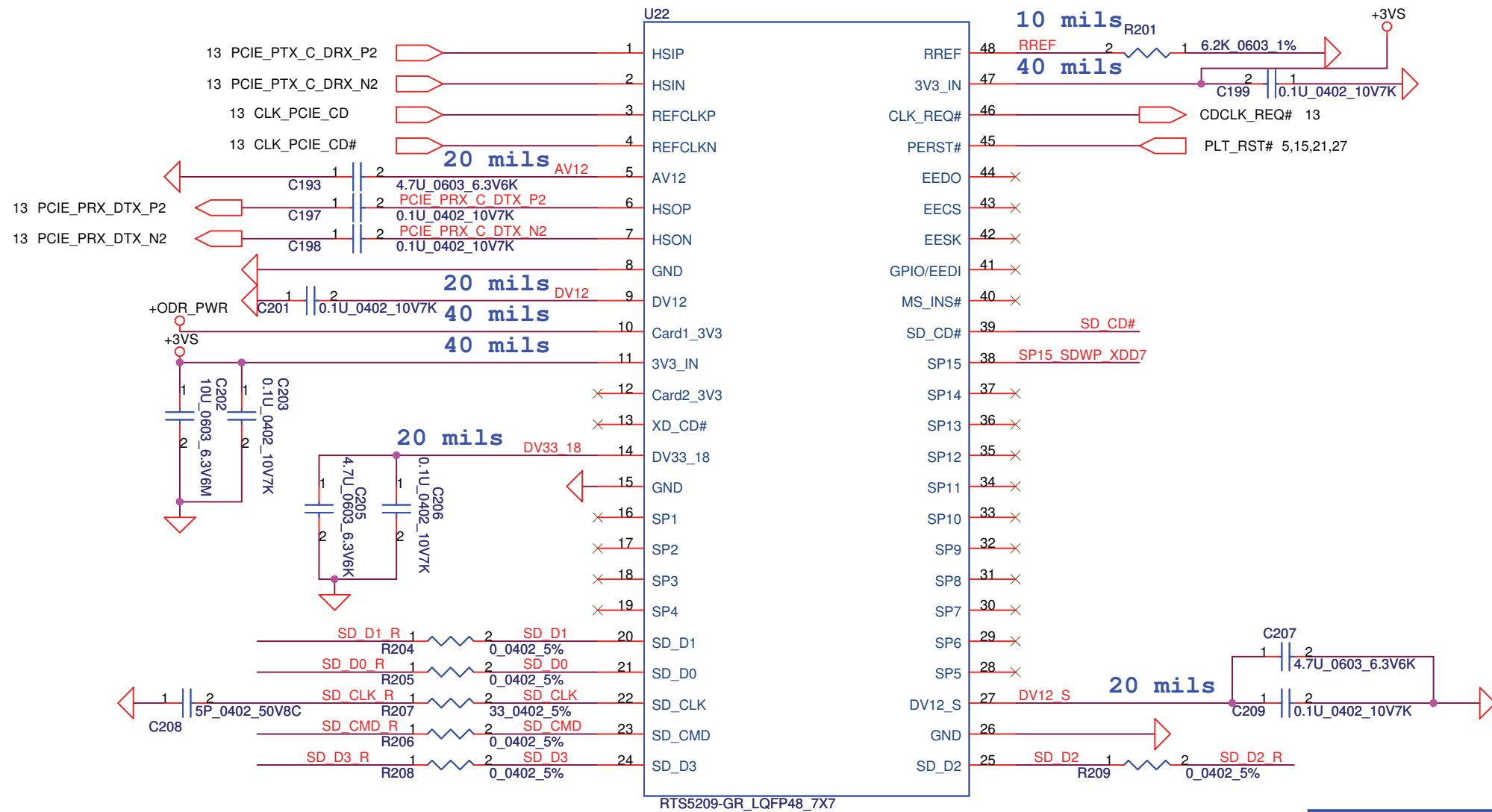
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Part Number = SP010013I00

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				LA-7531P	Rev 0.1
Date:	Sunday, April 10, 2011	Sheet	23	of	45

mSATA Conn.

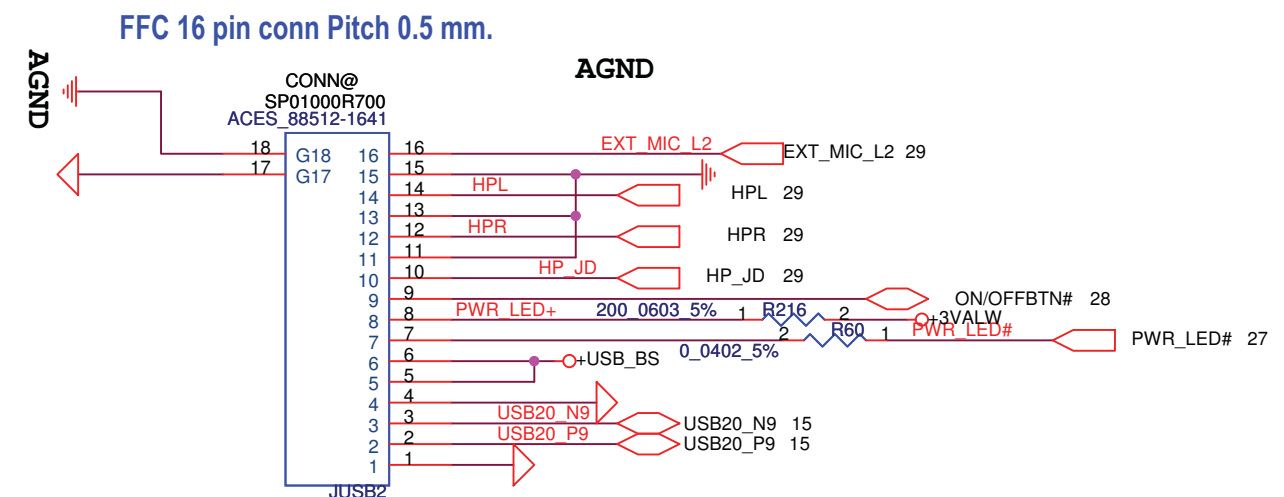
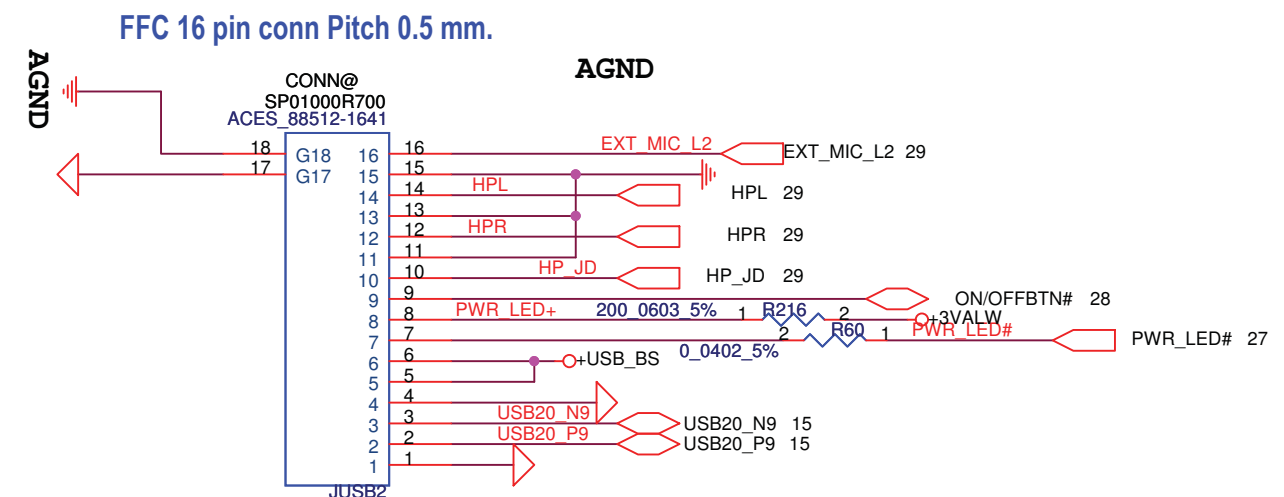
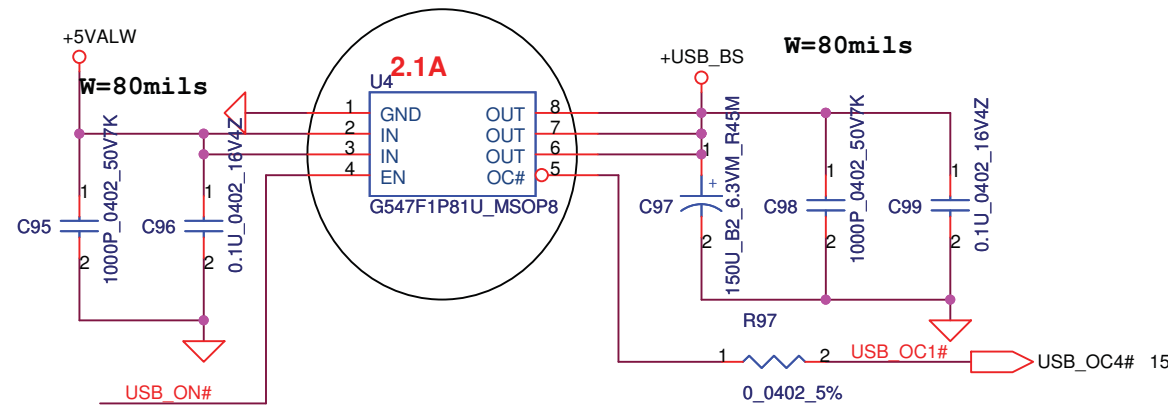
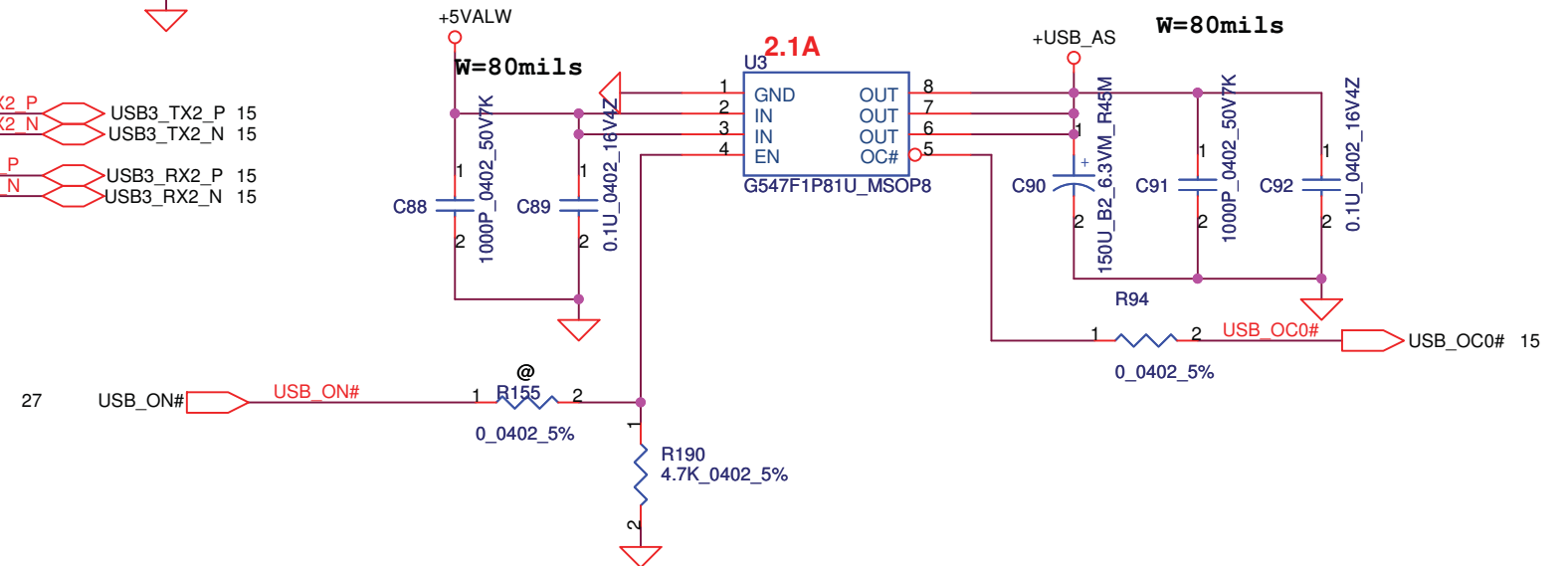
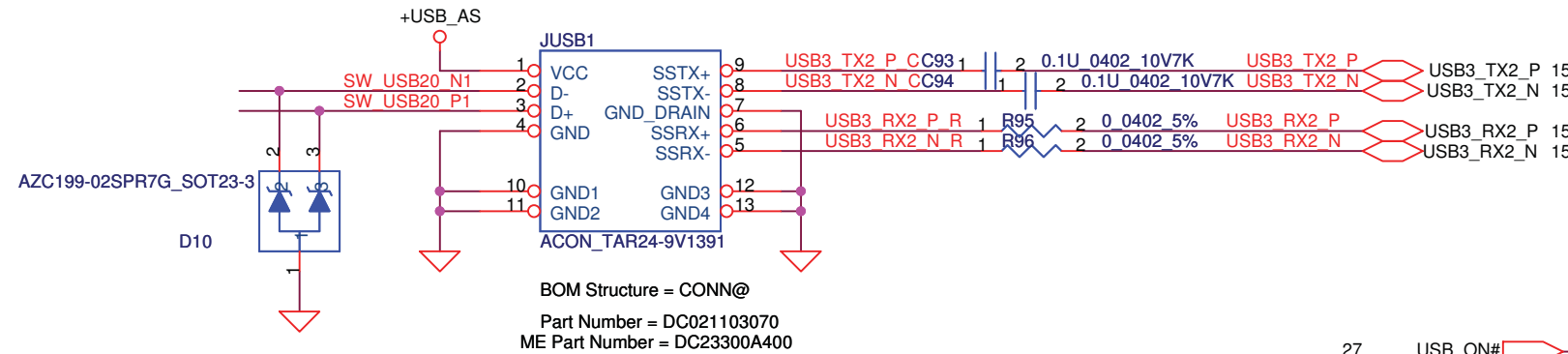
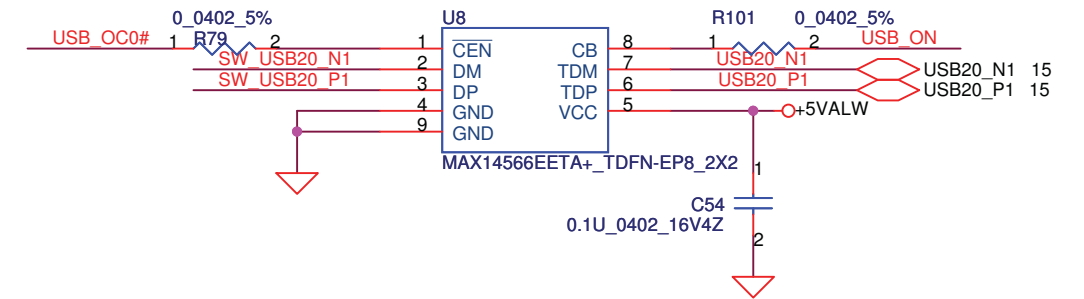
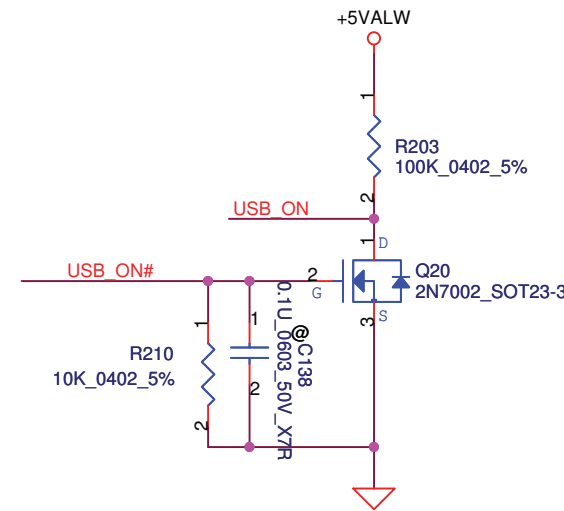
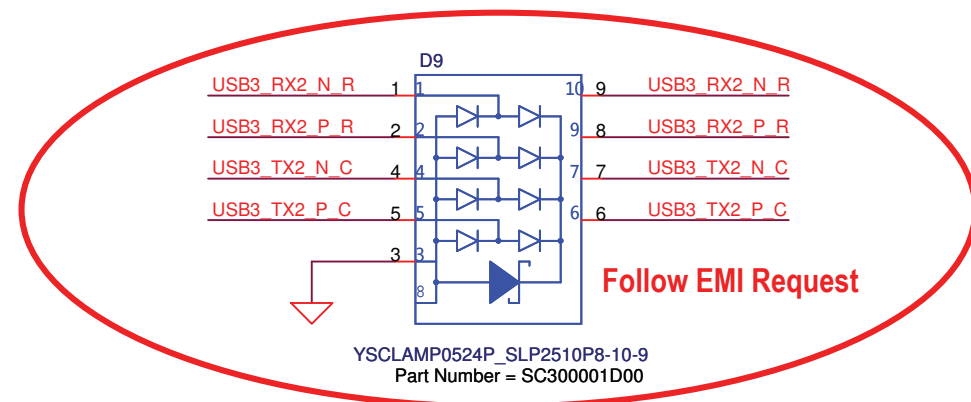


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2010/05/28		Title		mSATA Connector	
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LA-7531P		Rev		0.1	
Date:		Sunday, April 10, 2011		Sheet 24 of 45	



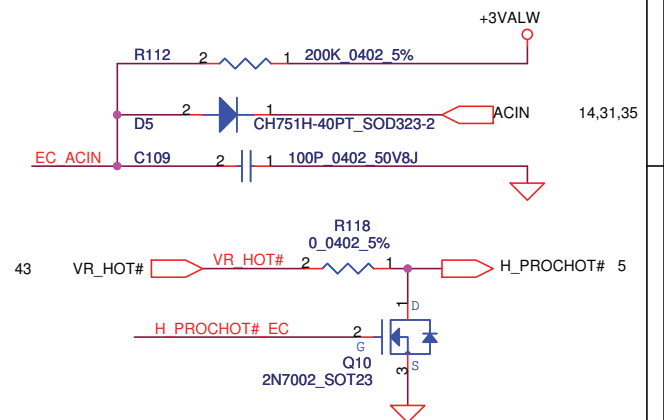
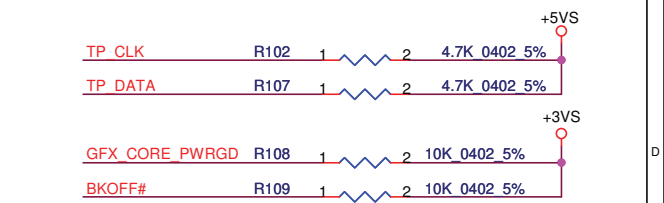
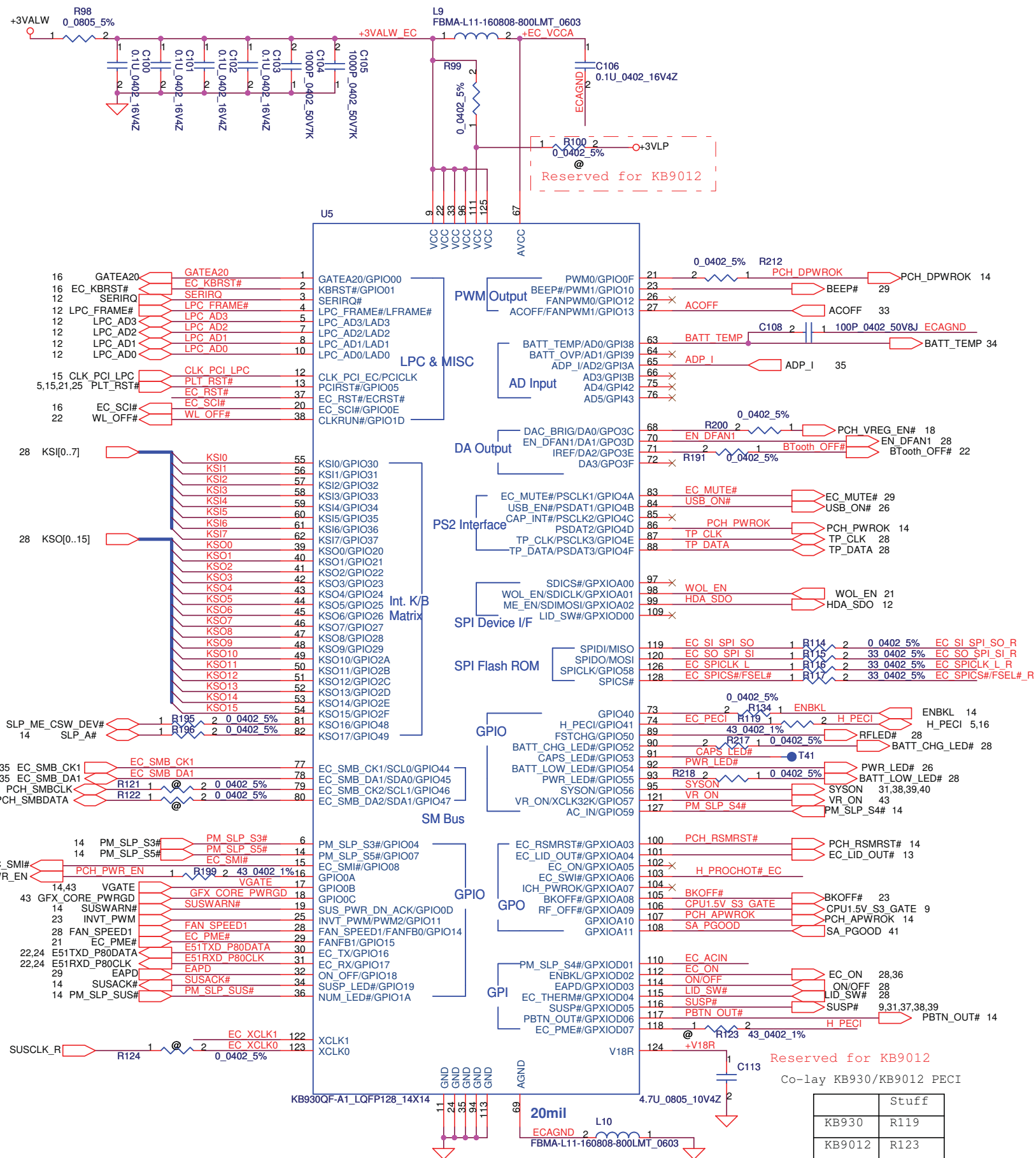
2 in1 SD/MMC

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				Size B	Document Number
				LA-7531P	
				Date:	Rev
				Sunday, April 10, 2011	0.1
				Sheet	25 of 45

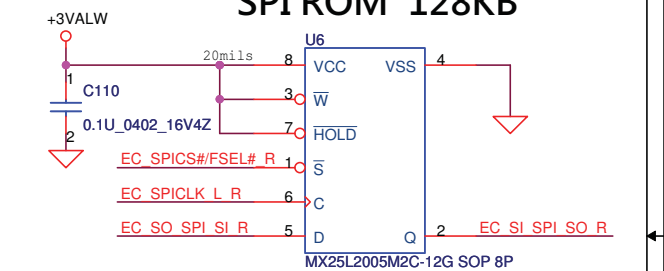


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				Size B	Rev 0.1
				Date: Sunday, April 10, 2011	Sheet 26 of 45

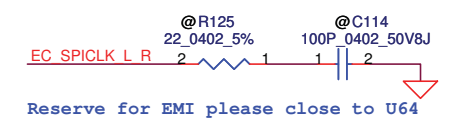
2011/04/09



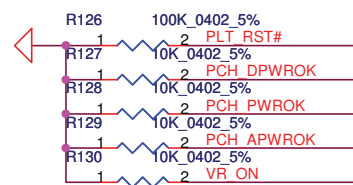
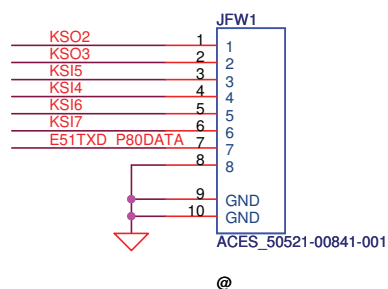
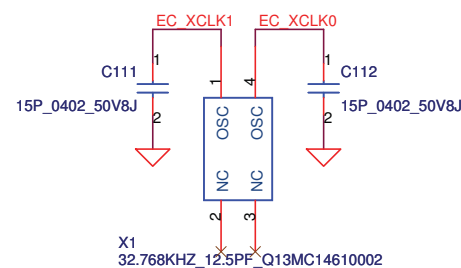
SPI ROM 128KB



SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)



To prevent debug card unwork issue.

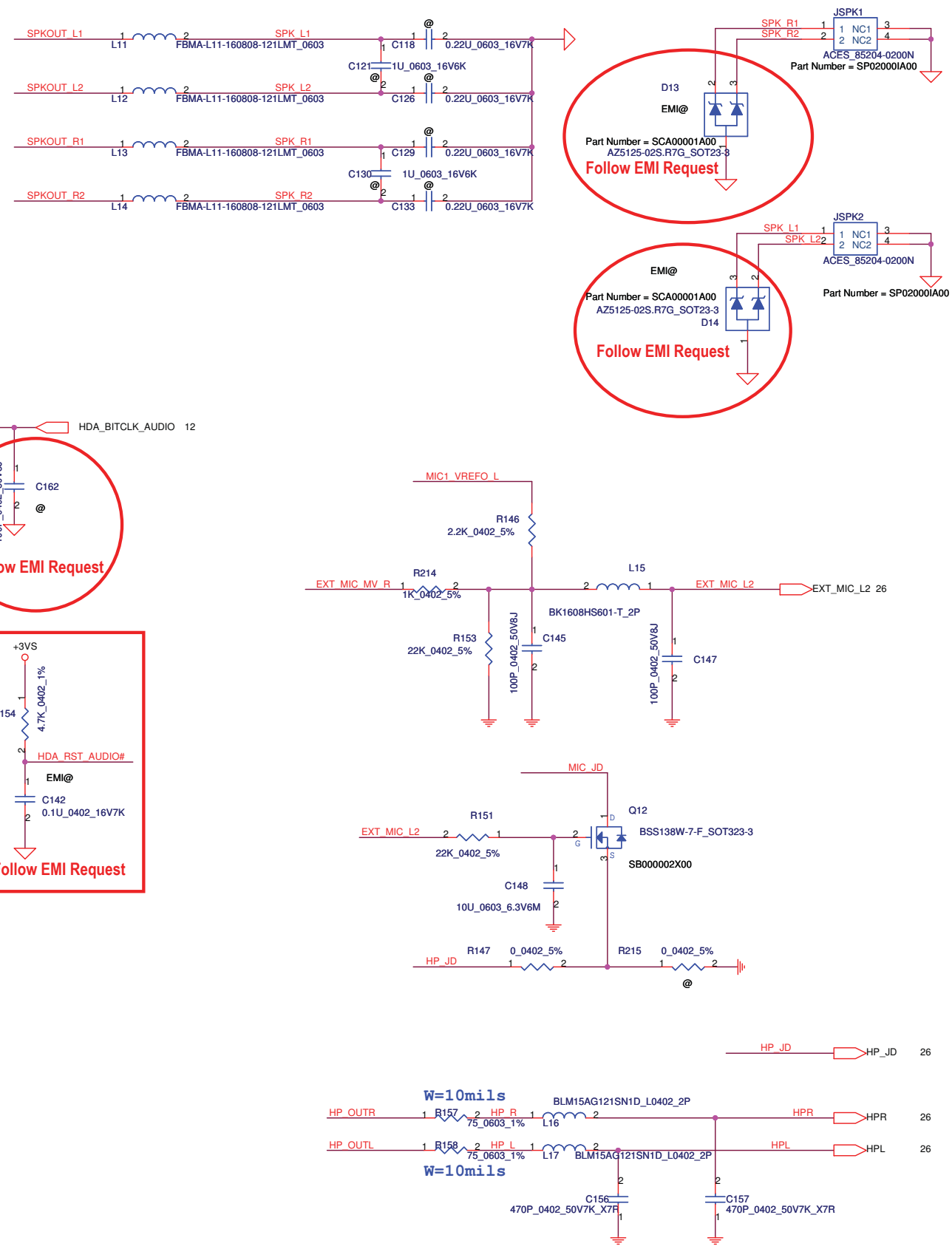
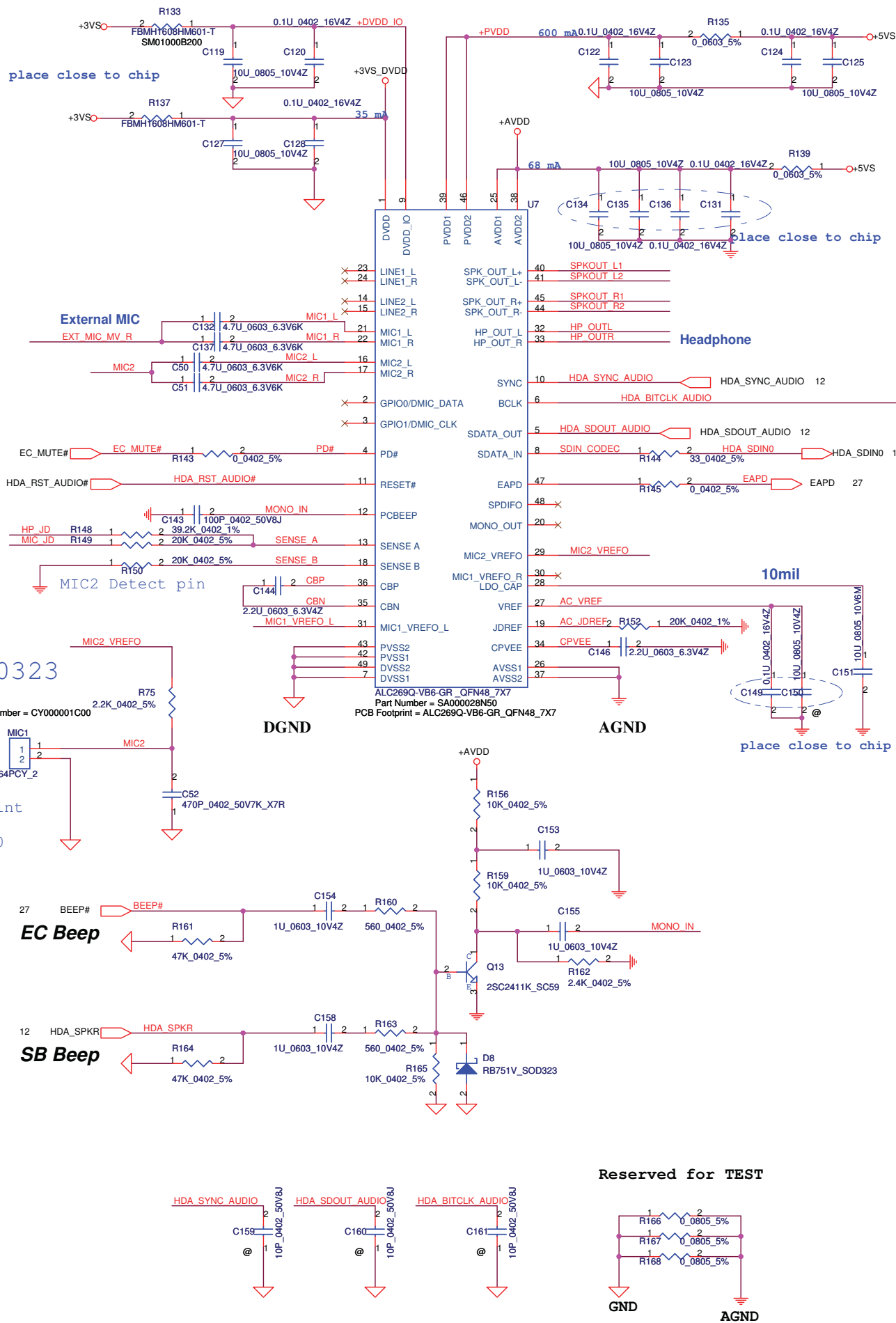


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Issued Date	2010/04/26	Deciphered Date	2010/05/28	Title		
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				Custom	LA-7531P	0.1
				Date:	Sunday, April 10, 2011	JSheat 27 of 45

20110323

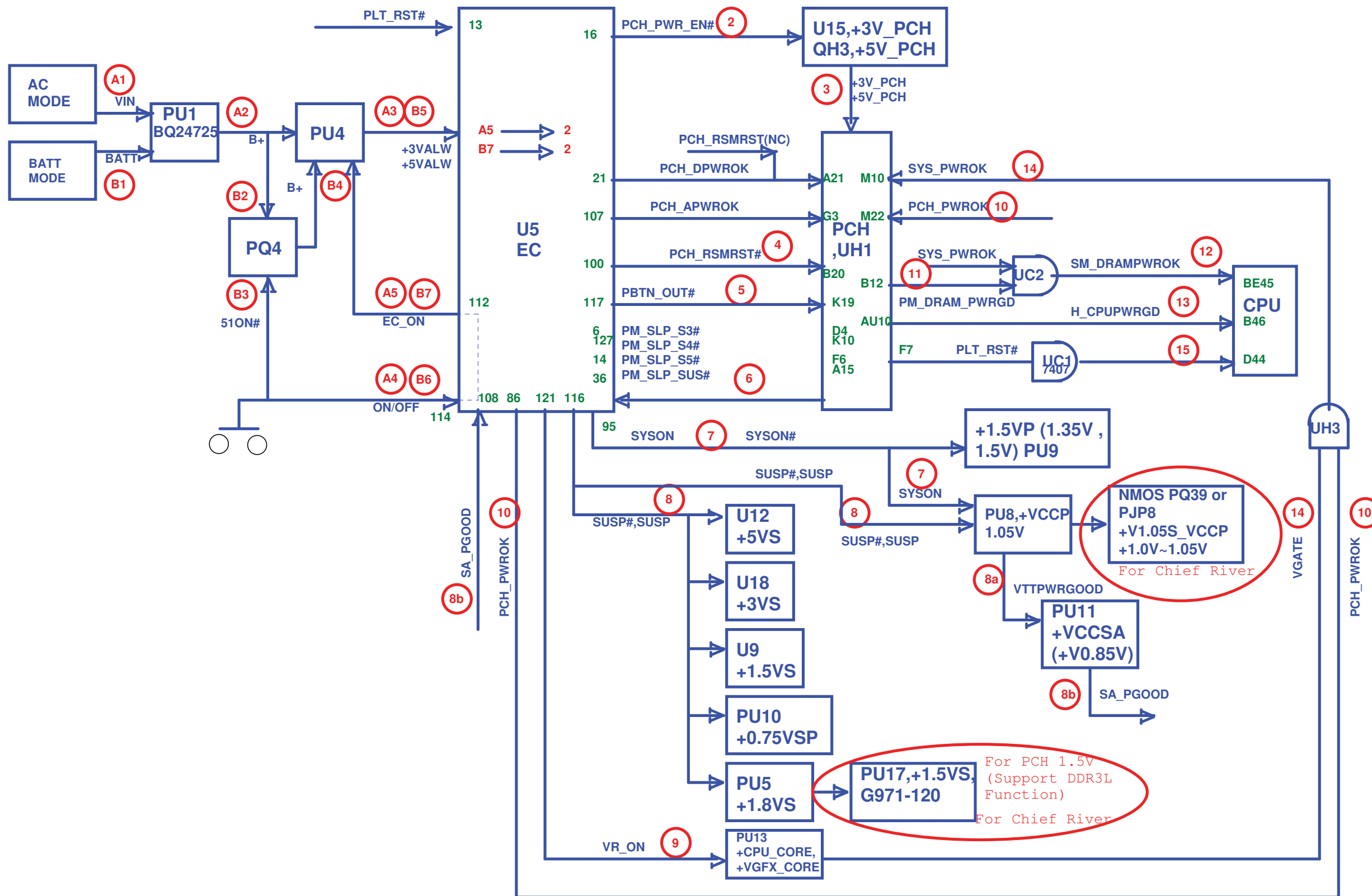
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PCB Footprint
used from
CYWM64P0100



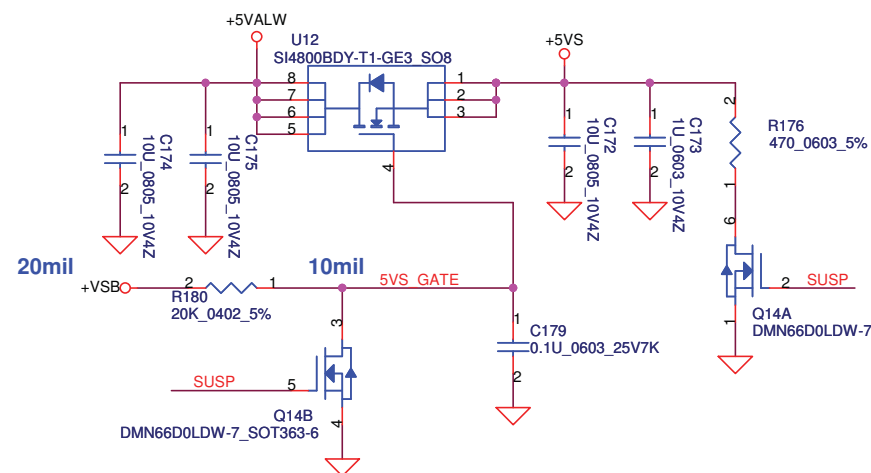
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Size	C	Document Number	LA-7531P	Rev	0.1
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LA-7531P Power Sequence 2011/04/10



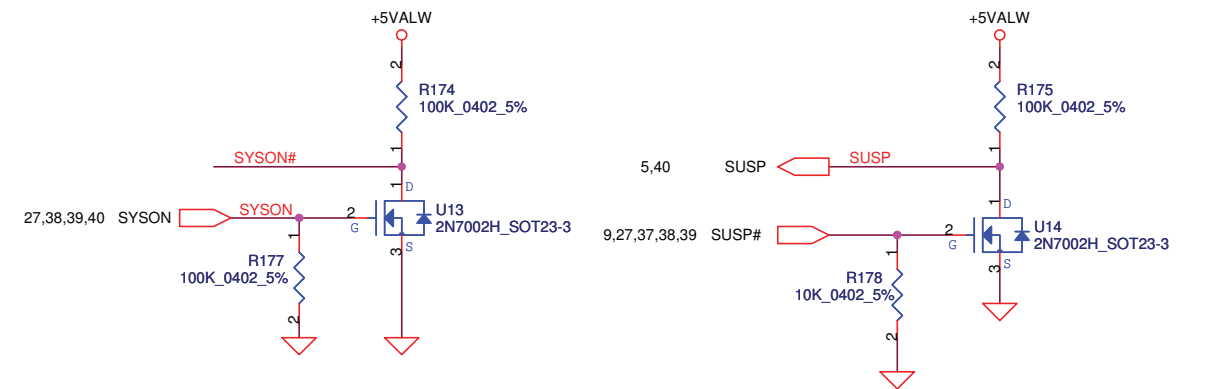
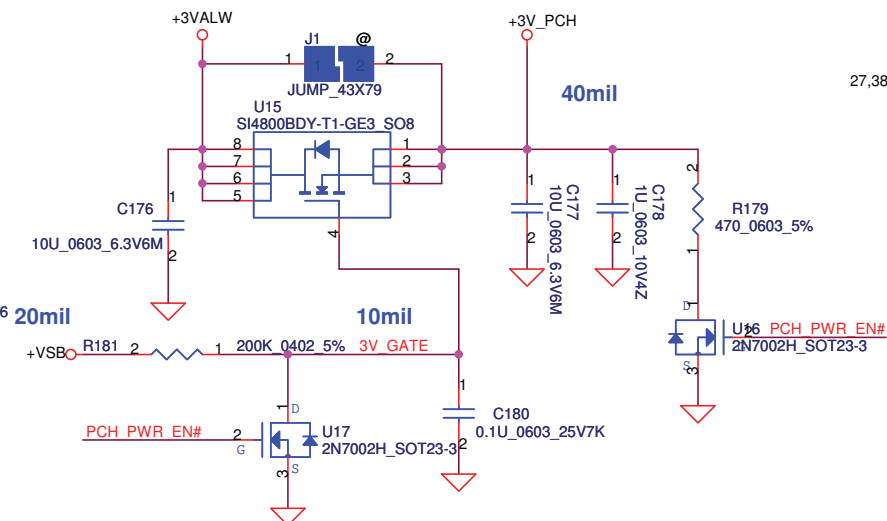
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Issued Date	2010/04/26	Deciphered Date	2010/05/28	Title		
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				Size Custom	Document Number LA-7531P	Rev 0.1
				Date: Sunday, April 10, 2011	Sheet 30 of 45	

+5VALW TO +5VS

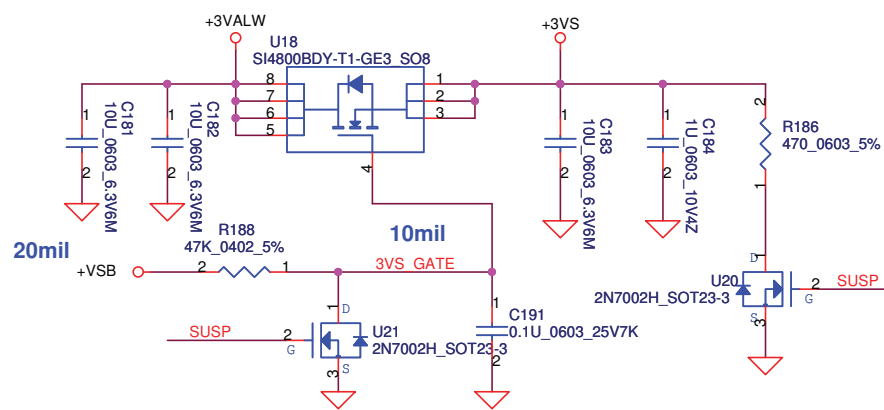


+3VALW TO +3VALW(PCH AUX Power)

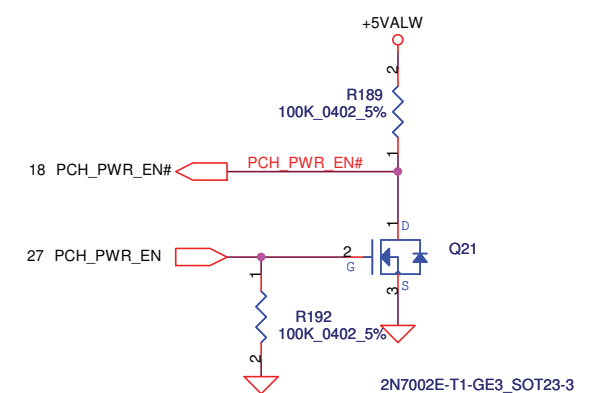
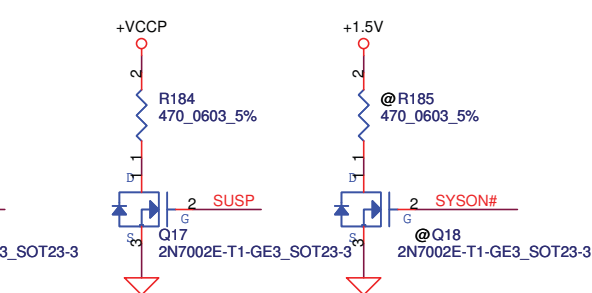
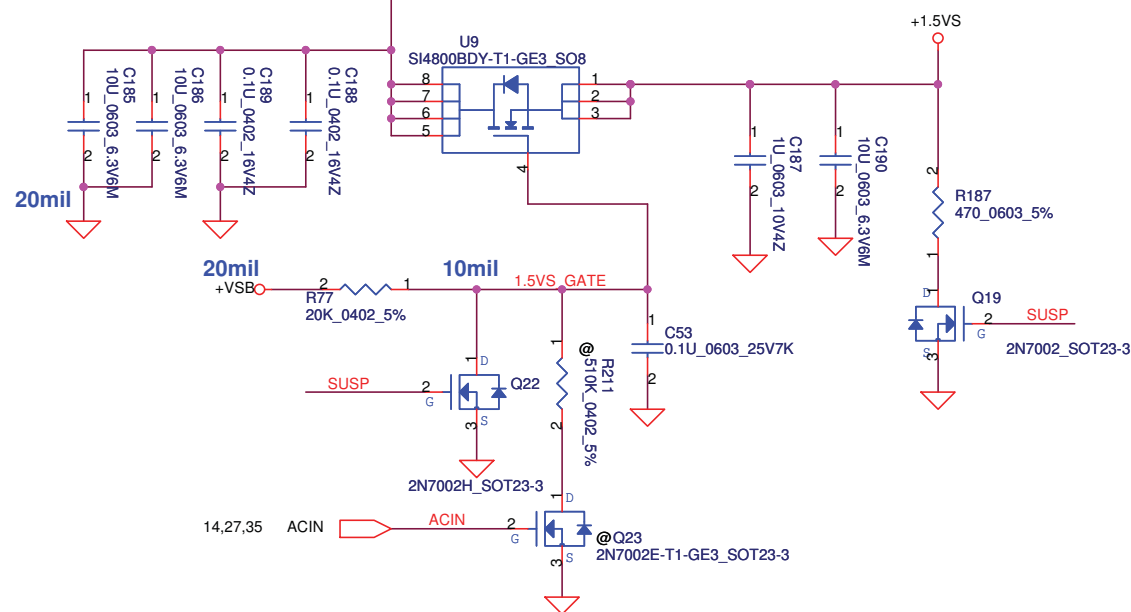
Short J1 for PCH VCCSUS3.3



+3VALW TO +3VS

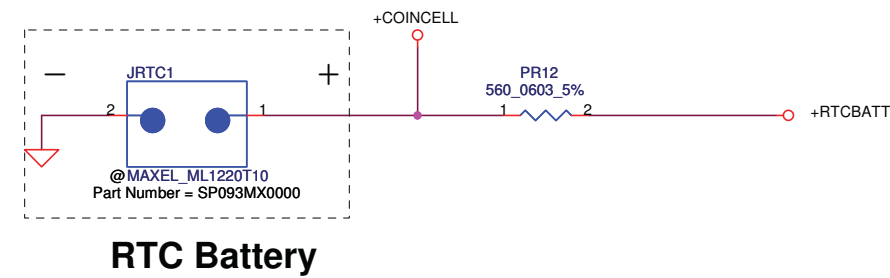
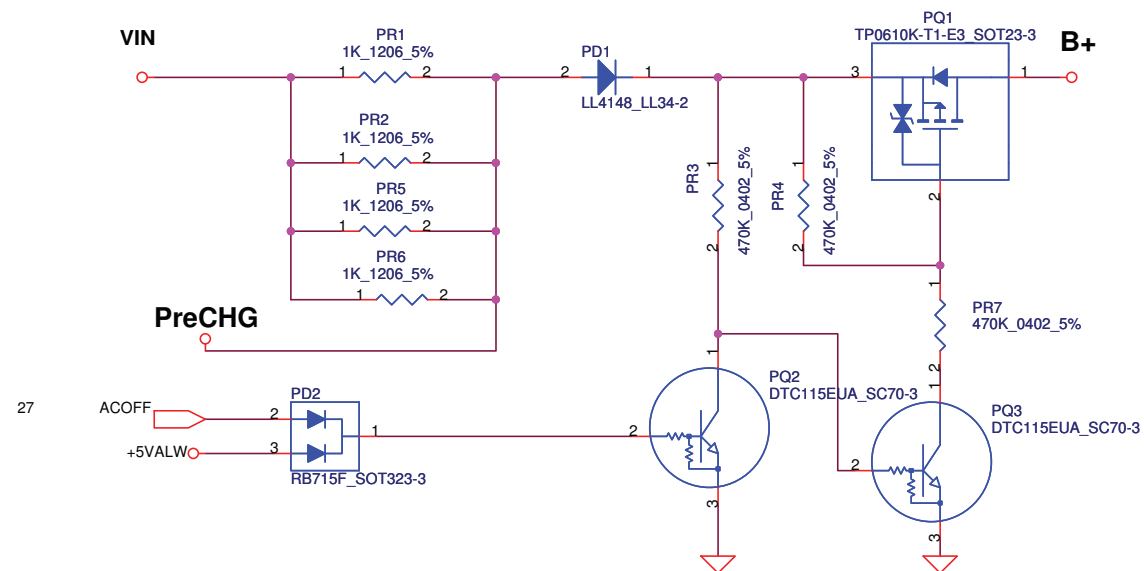
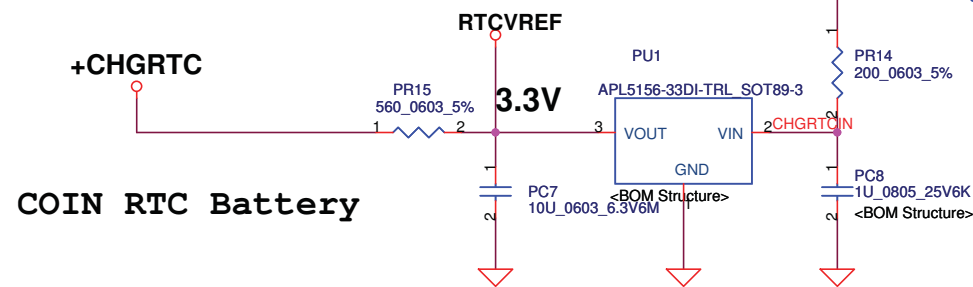
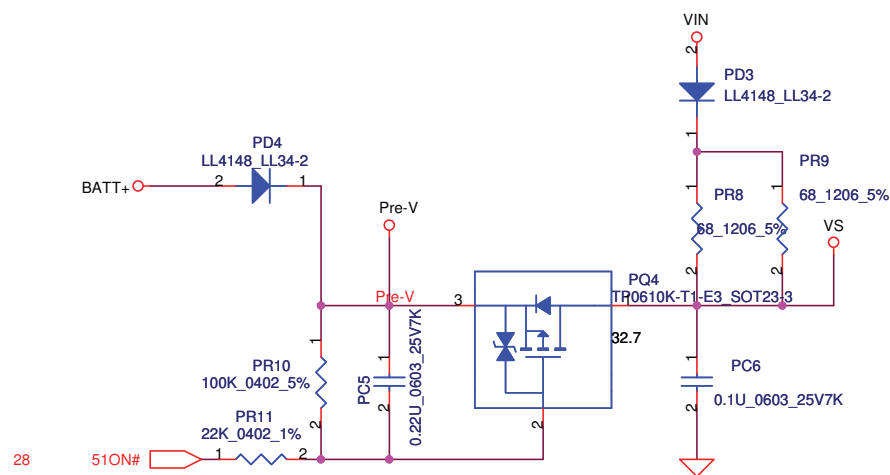
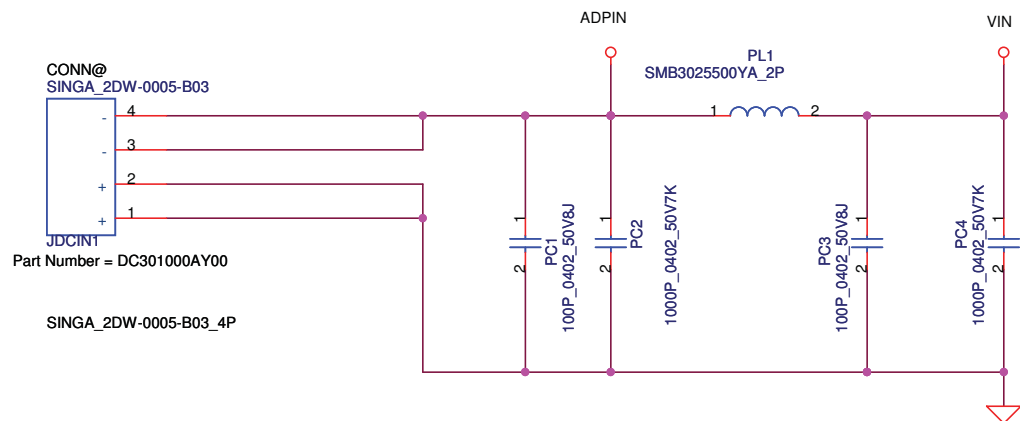


+1.5V TO +1.5VS

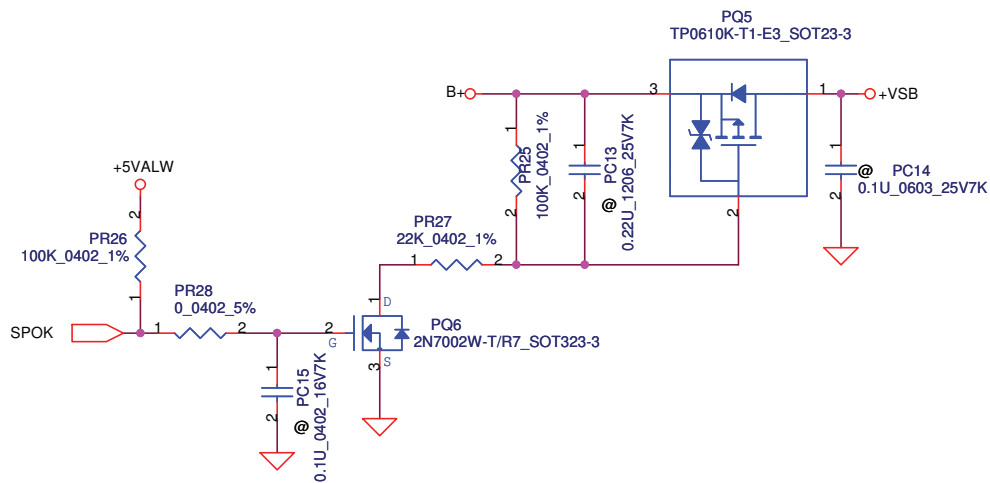
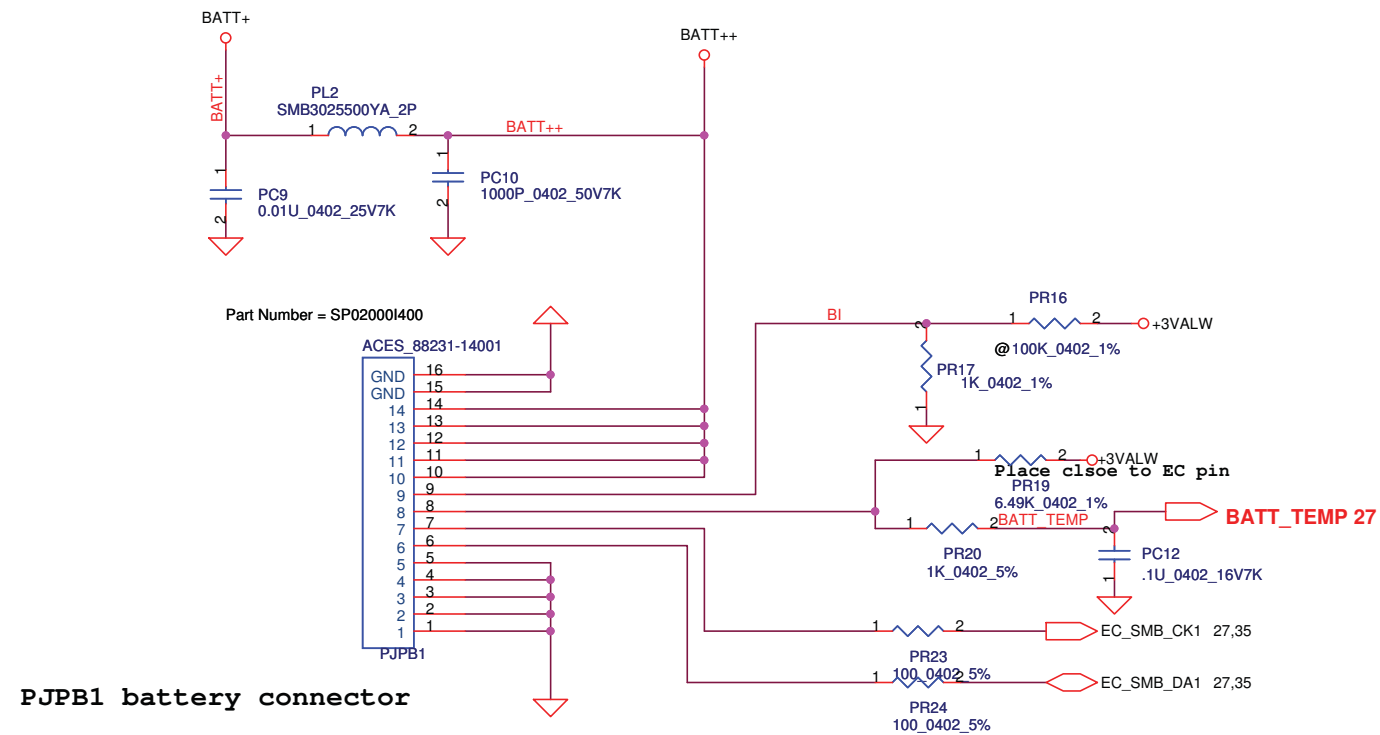


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				Size Custom	Document Number LA-7531P
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	xx	xxx	2011/02/XX	XXXX XXXX	XXXX		Rev01

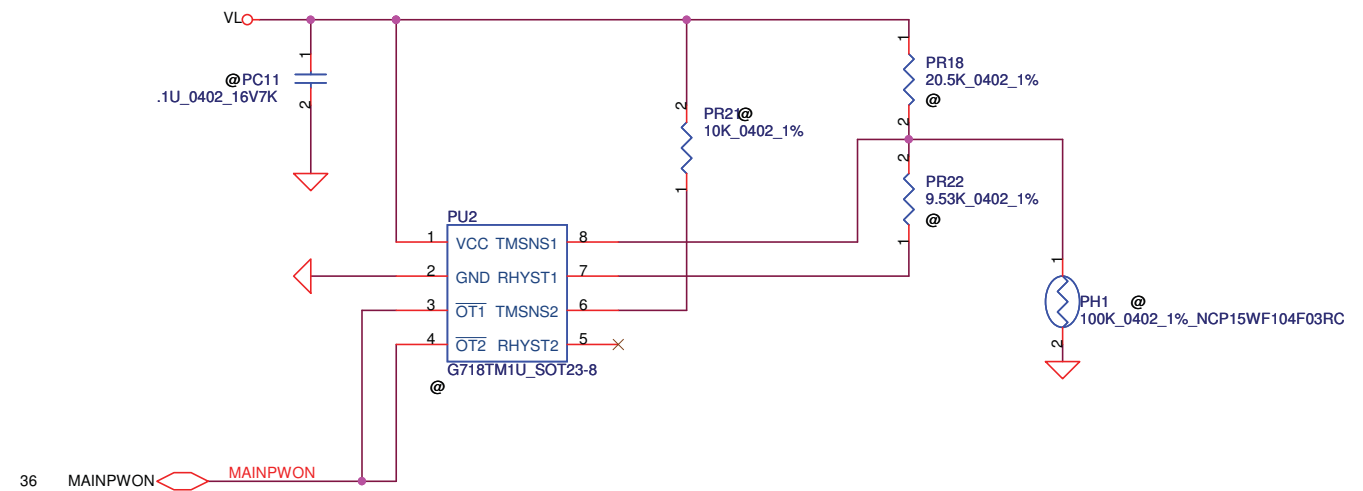


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				Date:	Sunday, April 10, 2011
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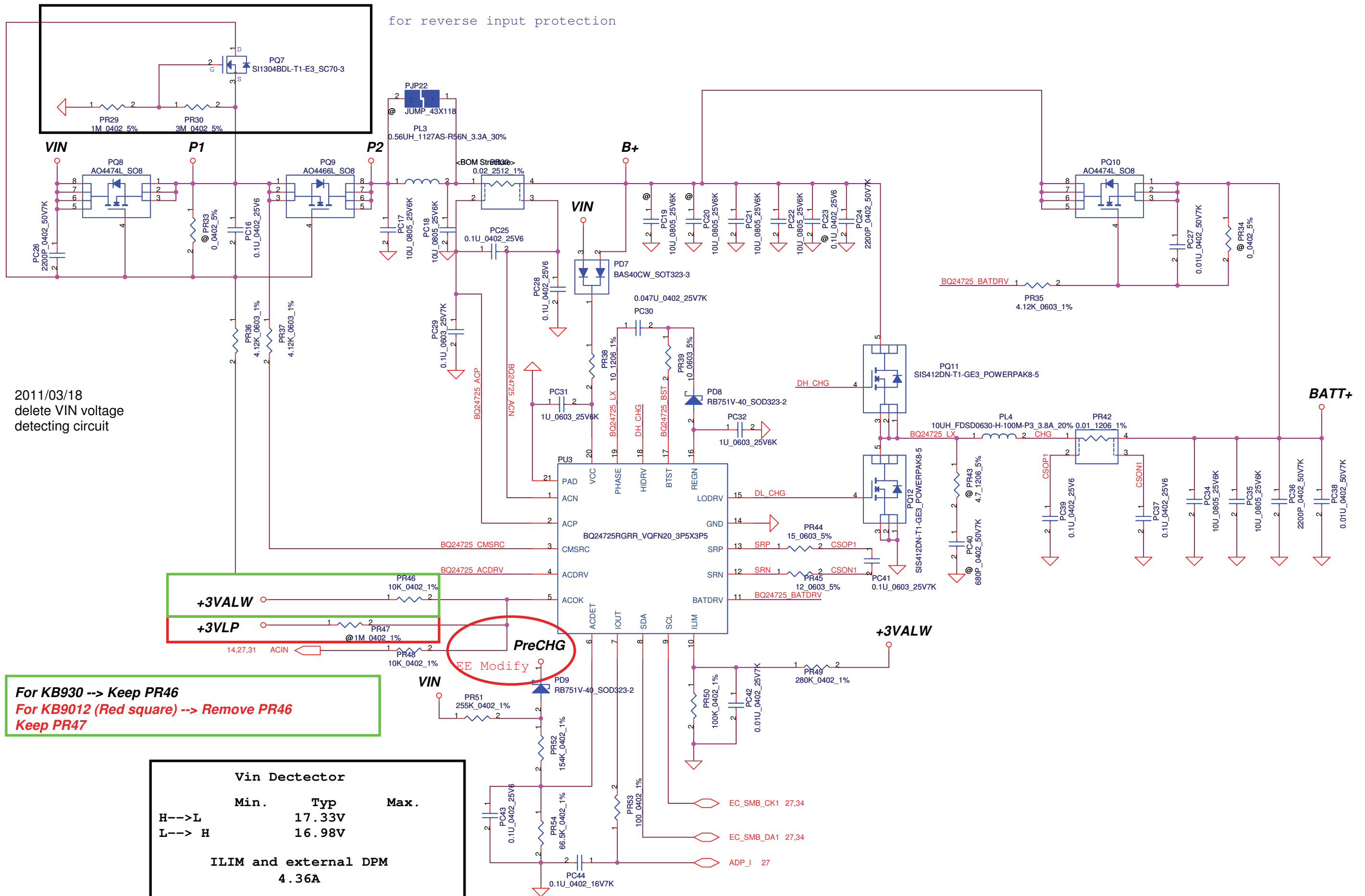


Battery Connect/OTP

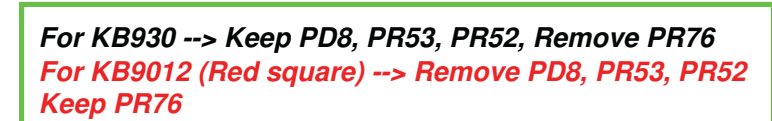
PH3 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



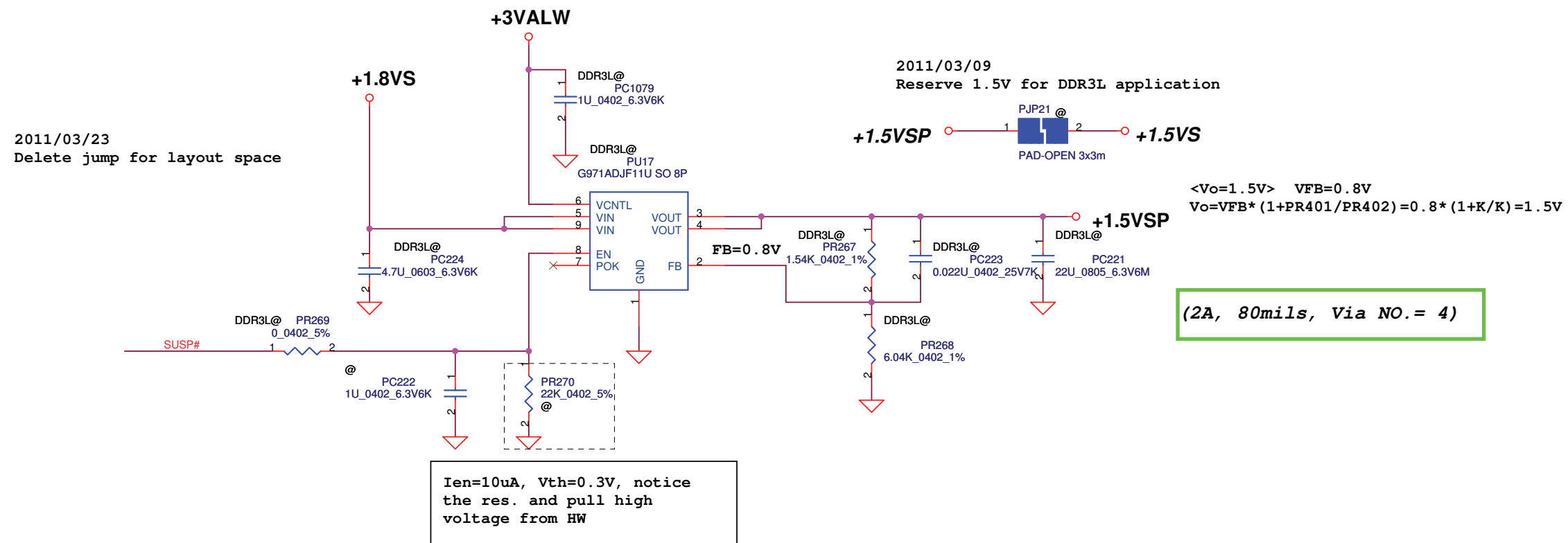
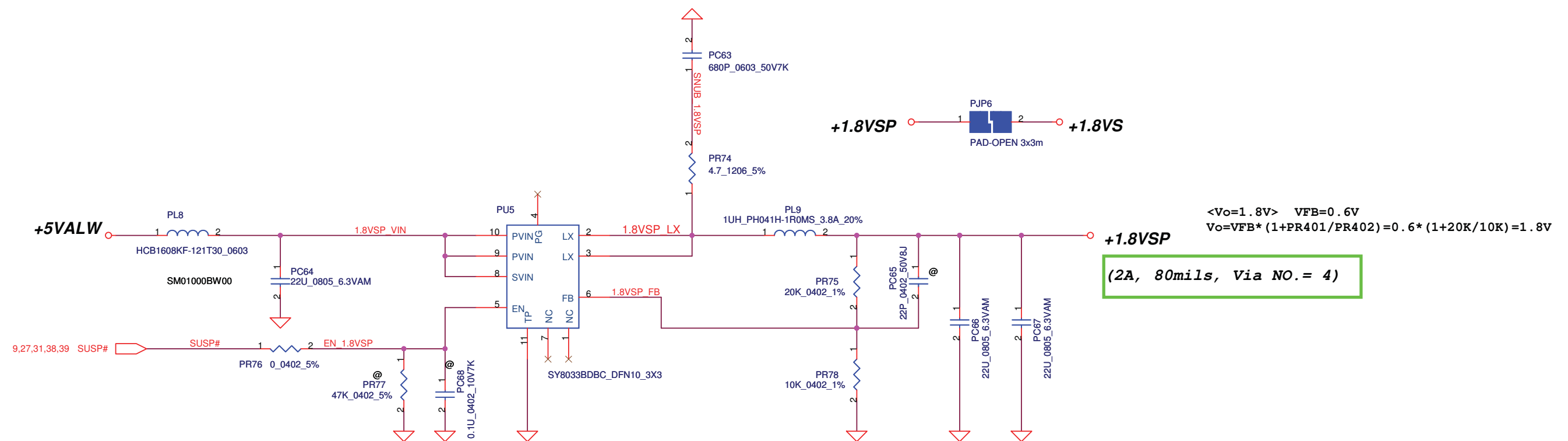
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title PWR-BATTERY CONN	
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				Rev	0.1



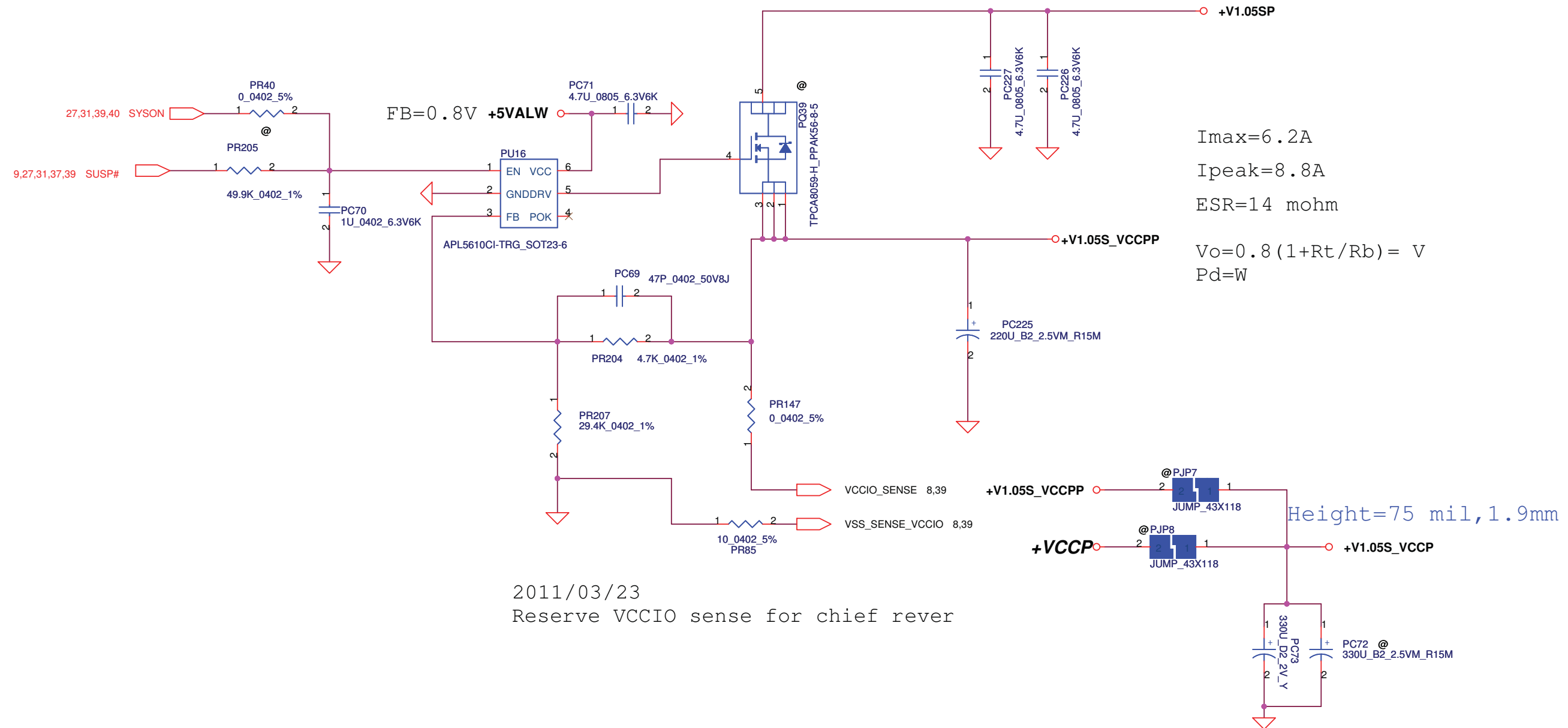
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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Size		Document Number		Rev	
		LA-7531P		0.1	
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Issued Date	2007/08/02	Deciphered Date	2008/08/02			
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				Size	Document Number	Rev
				Custom	LA-7531P	0.1
				Date:	Sunday, April 10, 2011	Sheet 36 of 45



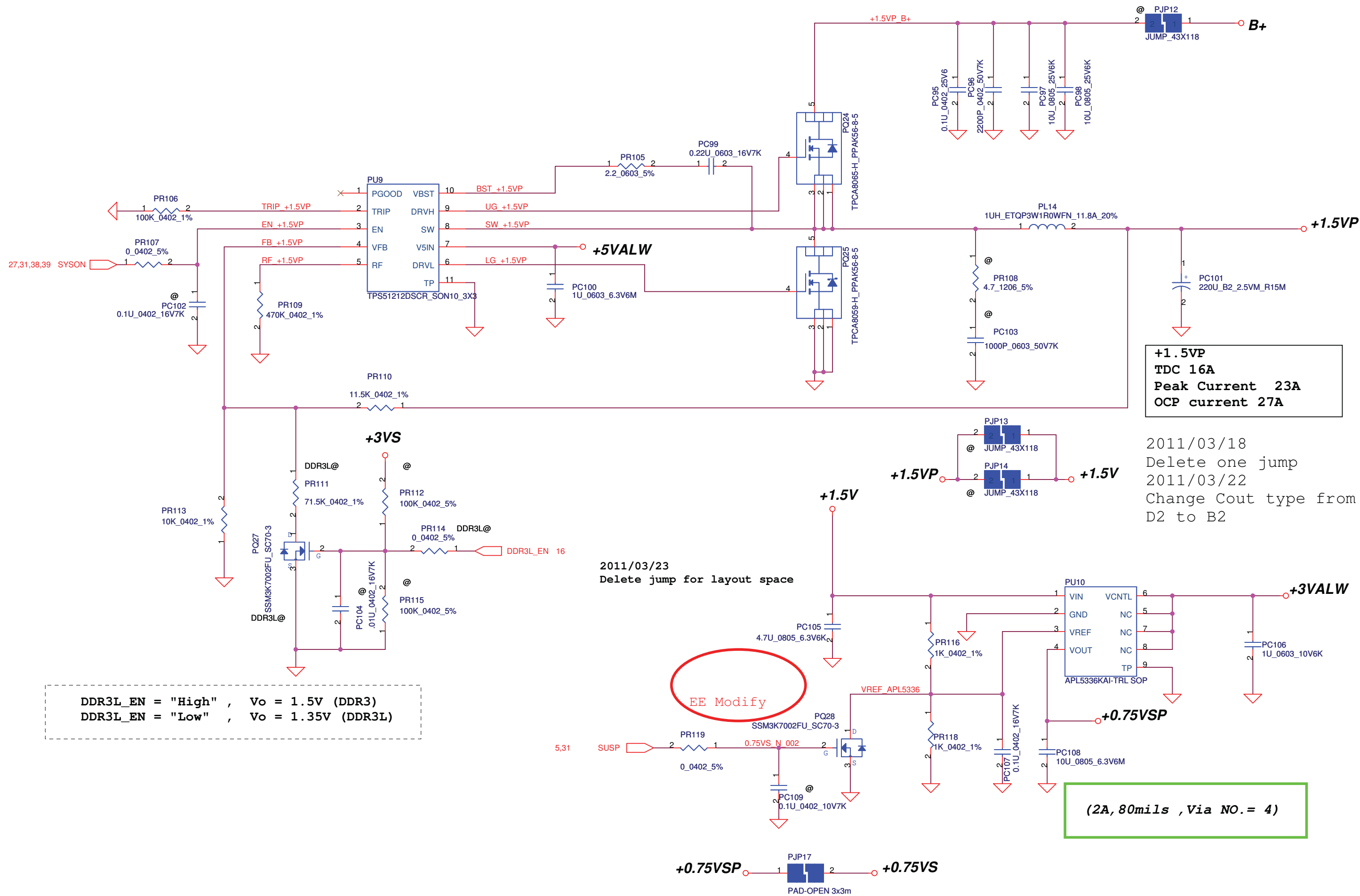
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2011/03/15
Change Cout to D2 type
Change PQ26 to TPCA8059(Rds-on)
2011/03/18
Change Cout from D2 type to B2
typt
2011/03/22
delete input jump
```



2011/03/23
Reserve VCCIO sense for chief rever

2011/03/18
Change PR72 form D2 type to B2 type.
need to take care the ESR differentia

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				Custom	LA-753IP	0.1
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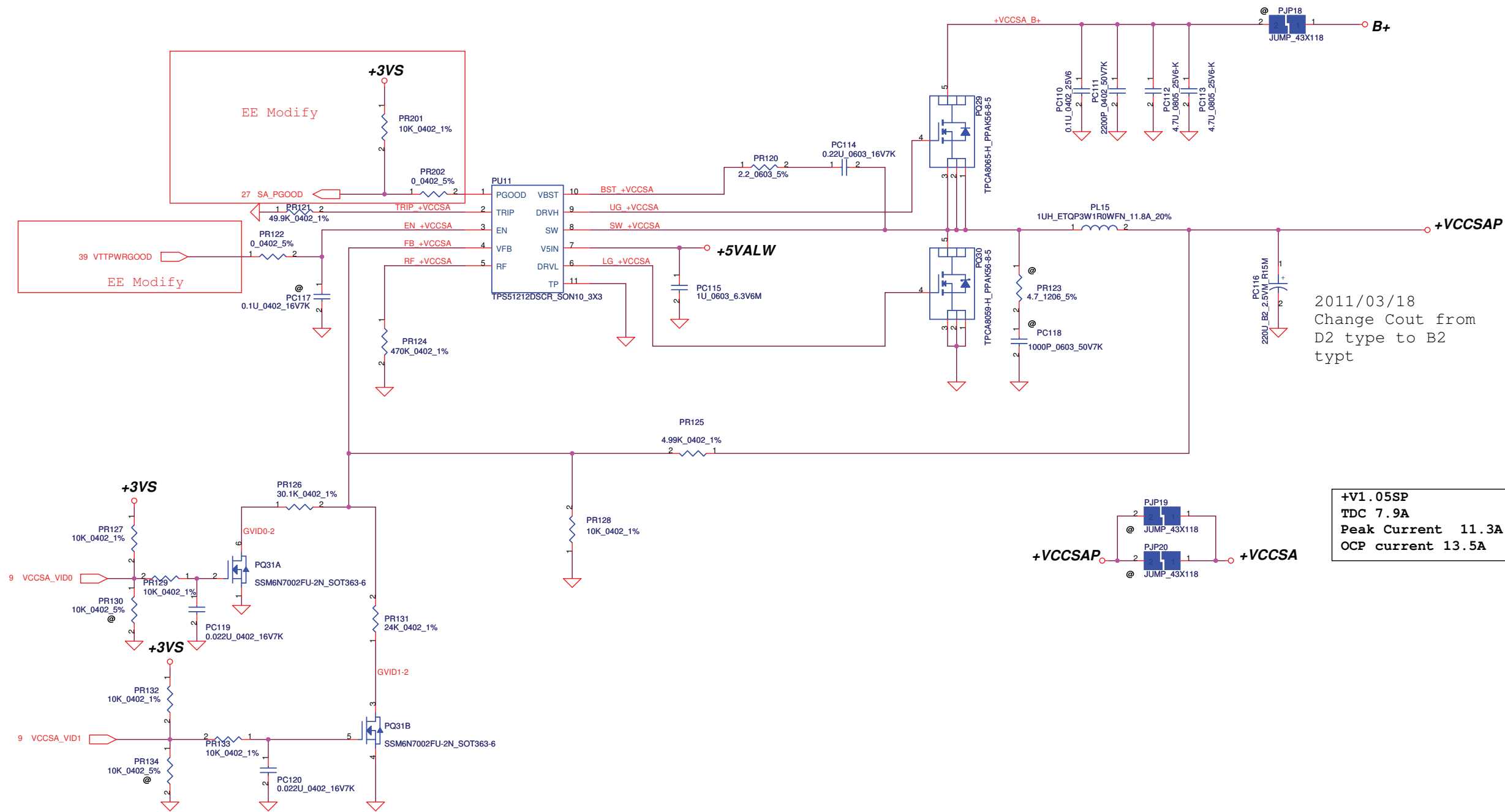


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+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

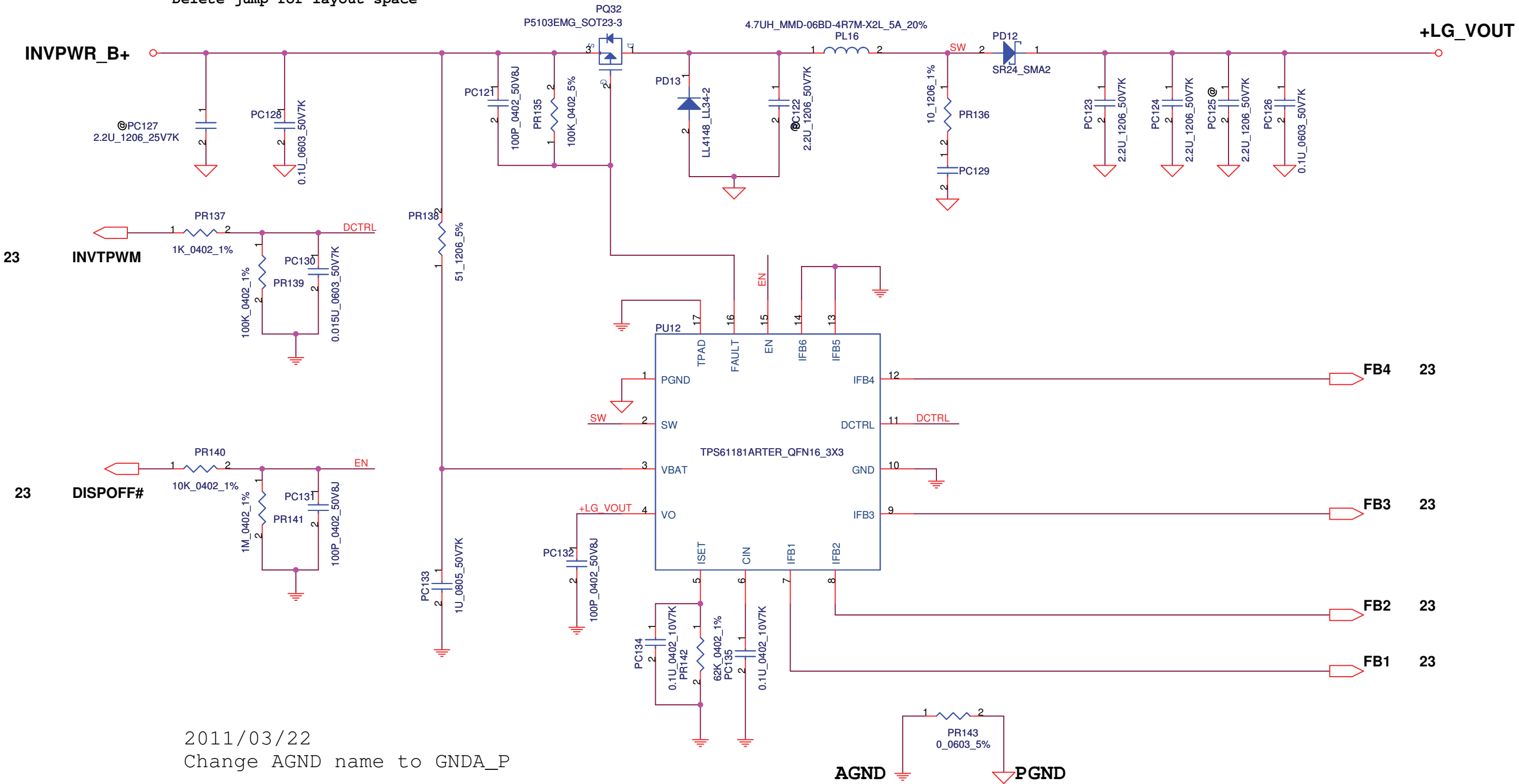
output voltage adjustable network



2011/03/18
Change Cout from
D2 type to B2
typt

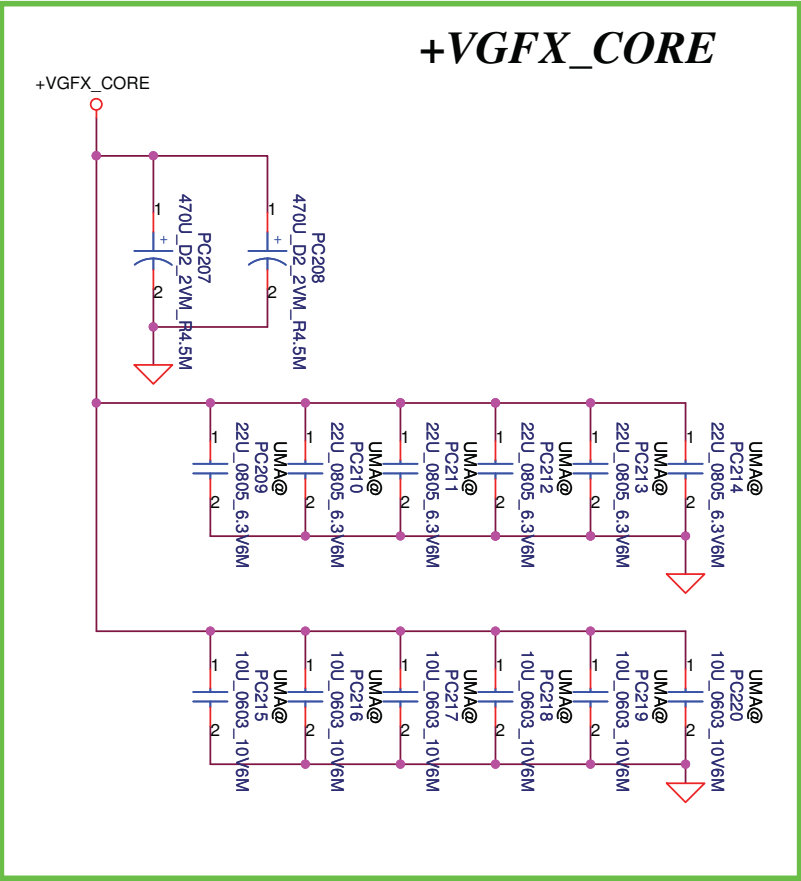
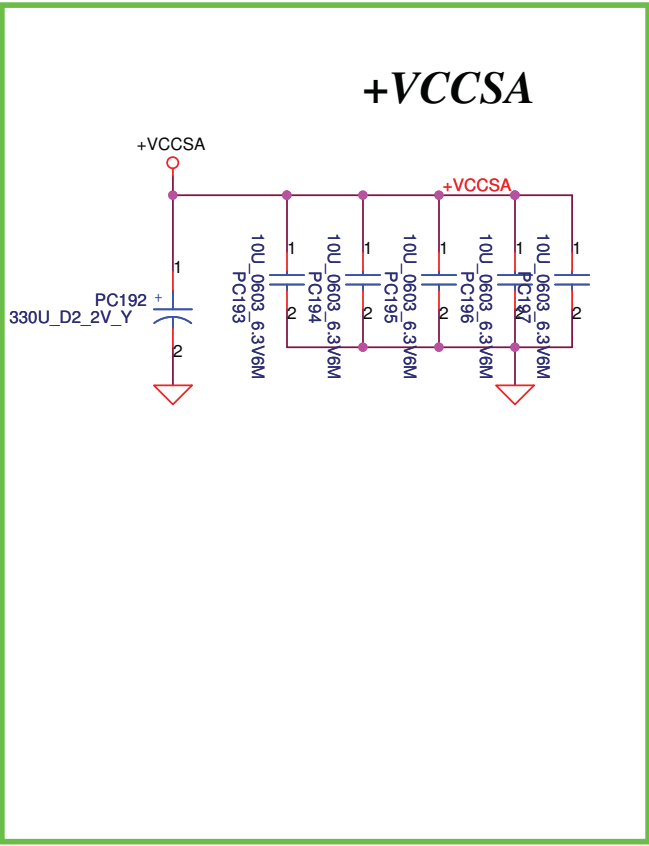
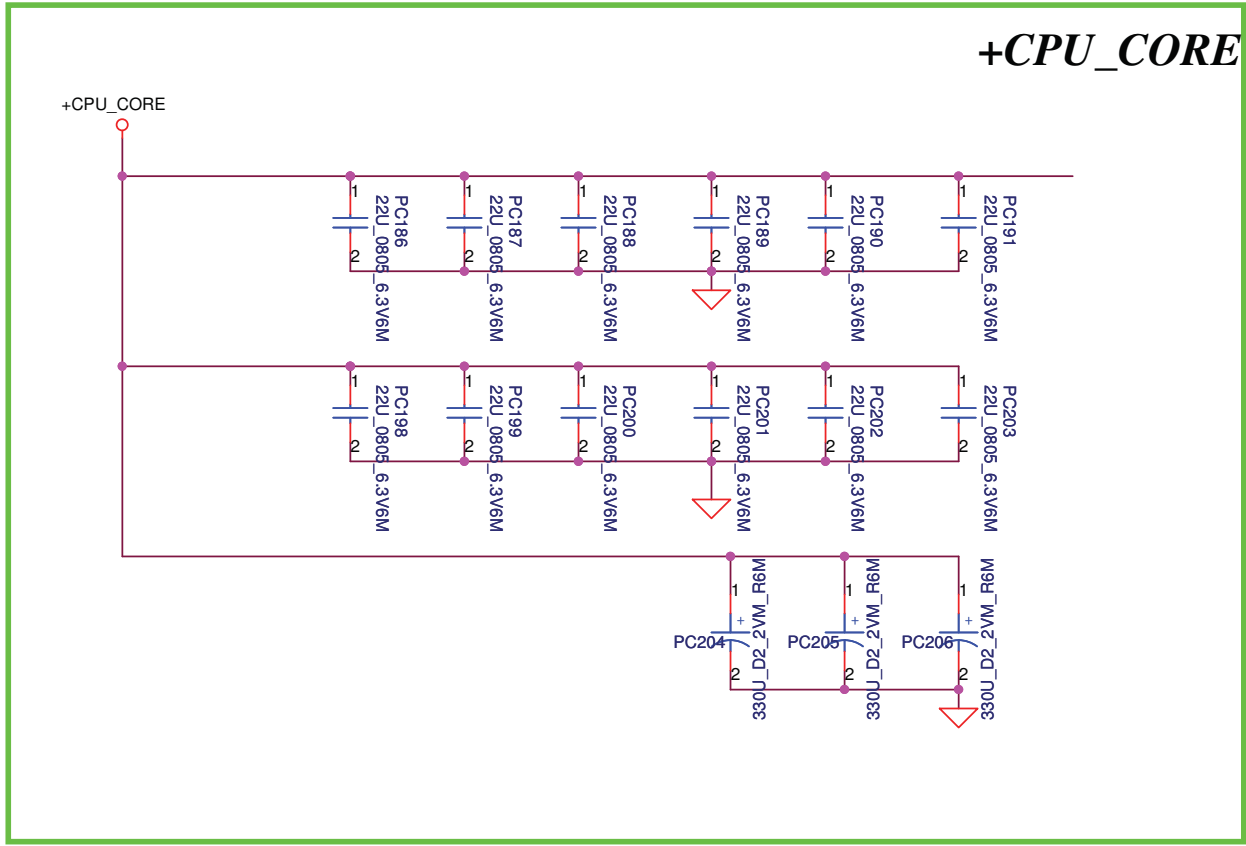
+V1.05SP
TDC 7.9A
Peak Current 11.3A
OCP current 13.5A

2011/03/23
Delete jump for layout space



2011/03/22
Change AGND name to GNDA_P

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				Size B	Rev 0.1
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					LA-7531P
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