Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel Crestline_PM+ICH8-M core logic

2007-05-15

REV:1.0

機密 等級

硬體二部	
產出人員	
產出日期	
解密日期	

Security Classification	Compal Secret Data		
Issued Date	2006/04/13	Deciphered Date	2006/06/30

Compal Electronics, Inc.

Title

Cover Sheet

Size	Document Number	Rev
Custom	*LA-3331P*	1.0

Date: Tuesday, May 15, 2007

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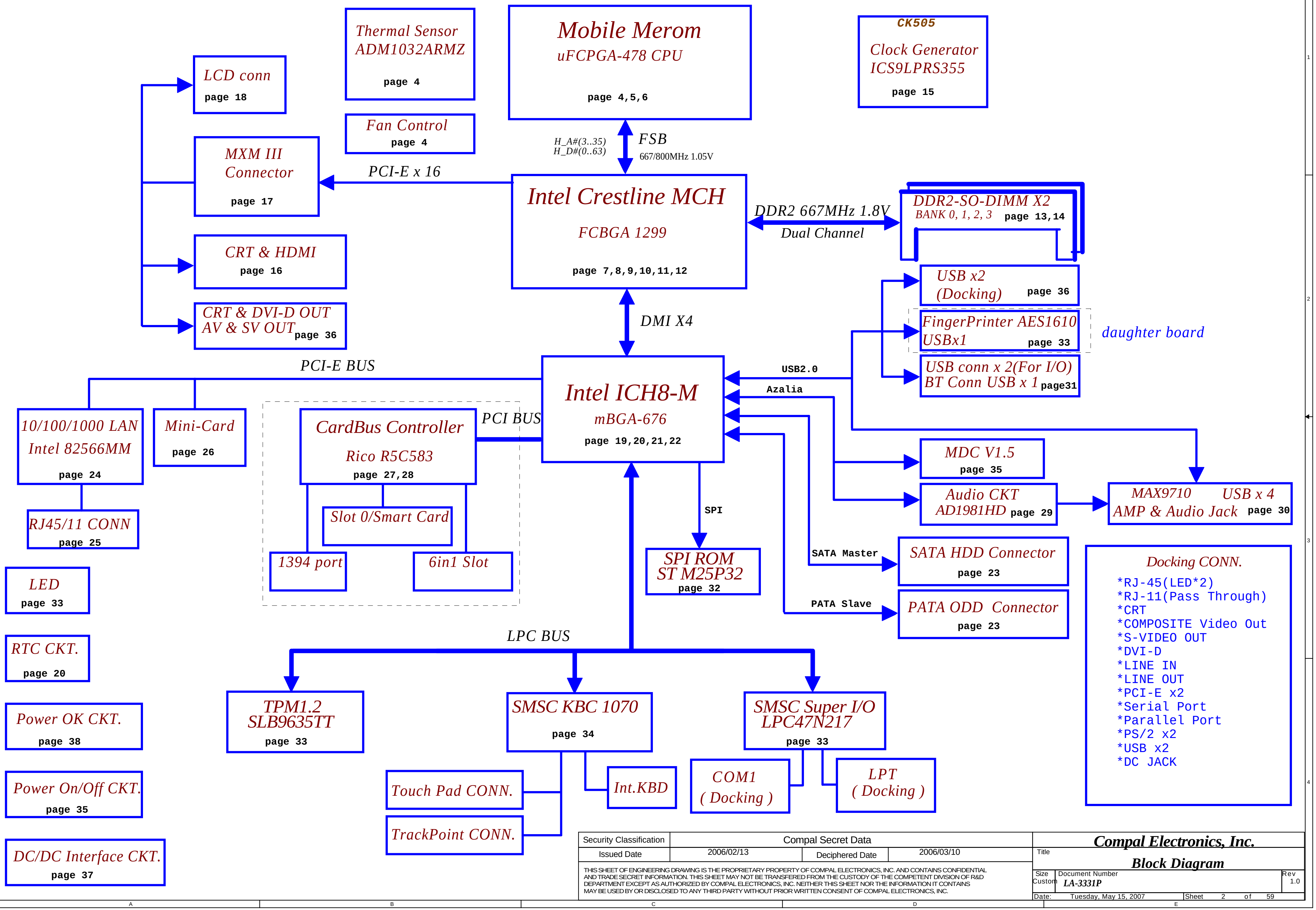
Compal confidential

File Name : LA-3331P

ABITA



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Title **Block Diagram**

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Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+3VM +1.25VM +1.05VM	+5V +1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON   X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	M/B
1	Finger Printer
2	M/B
3	On Audio Board
4	On Audio Board
5	On Audio Board
6	Blut Tooth
7	Docking
8	On Audio Board
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass strorage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

Security Classification	Compal Secret Data			**Compal Electronics, Inc.**
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title **Notes List**
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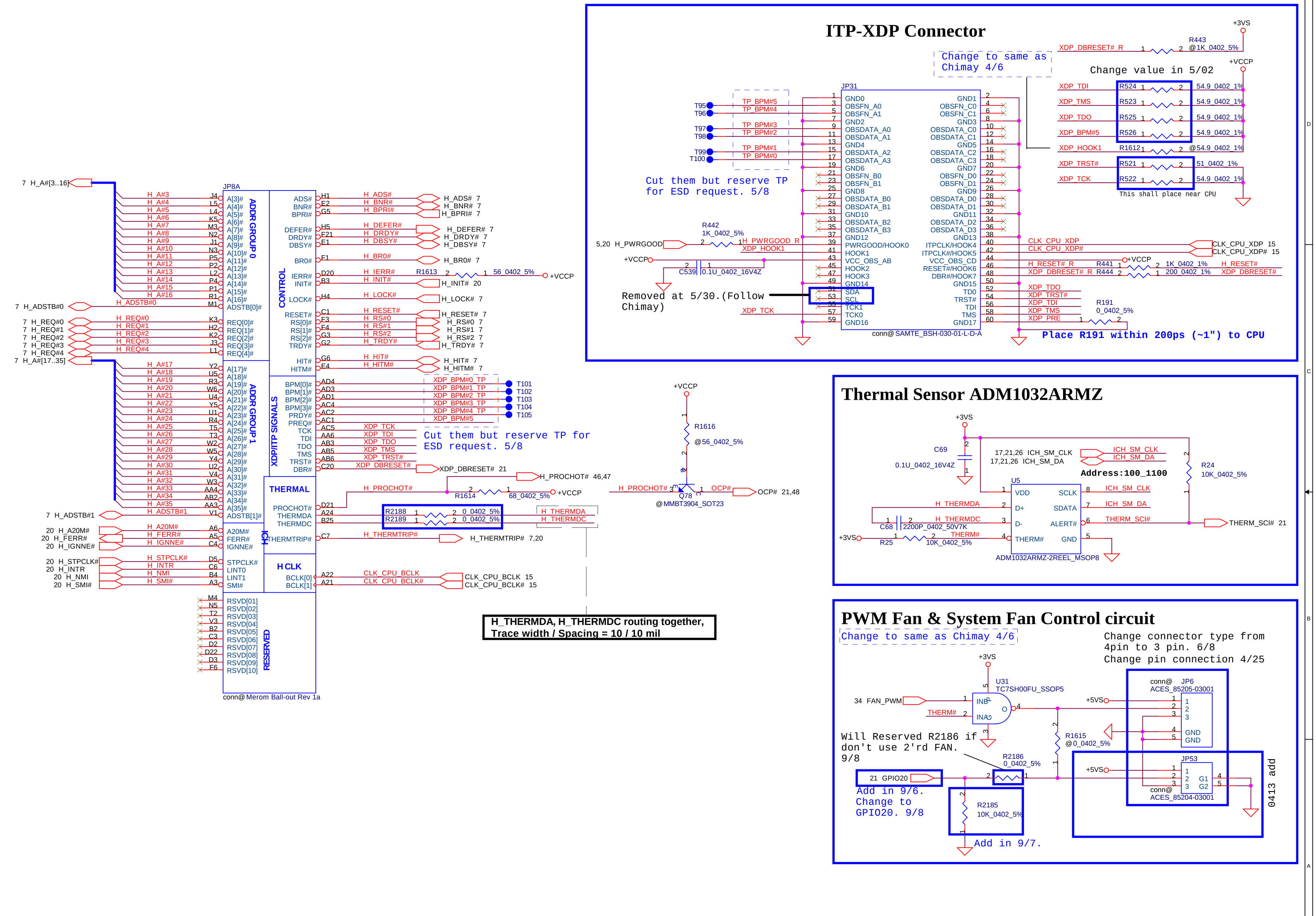

Change to same as Chimay 4/6

Change value in 5/02

Cut them but reserve TP for ESD request. 5/8

Removed at 5/30.(Follow Chimay)

This shall place near CPU

Place R191 within 200ps (~1") to CPU

Cut them but reserve TP for ESD request. 5/8

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Change to same as Chimay 4/6

Change connector type from 4pin to 3 pin. 6/8
Change pin connection 4/25

Will Reserved R2186 if don't use 2'rd FAN. 9/8

Add in 9/6. Change to GPIO20. 9/8

Add in 9/7.

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Title
Merom(1/3)-AGTL+/XDP

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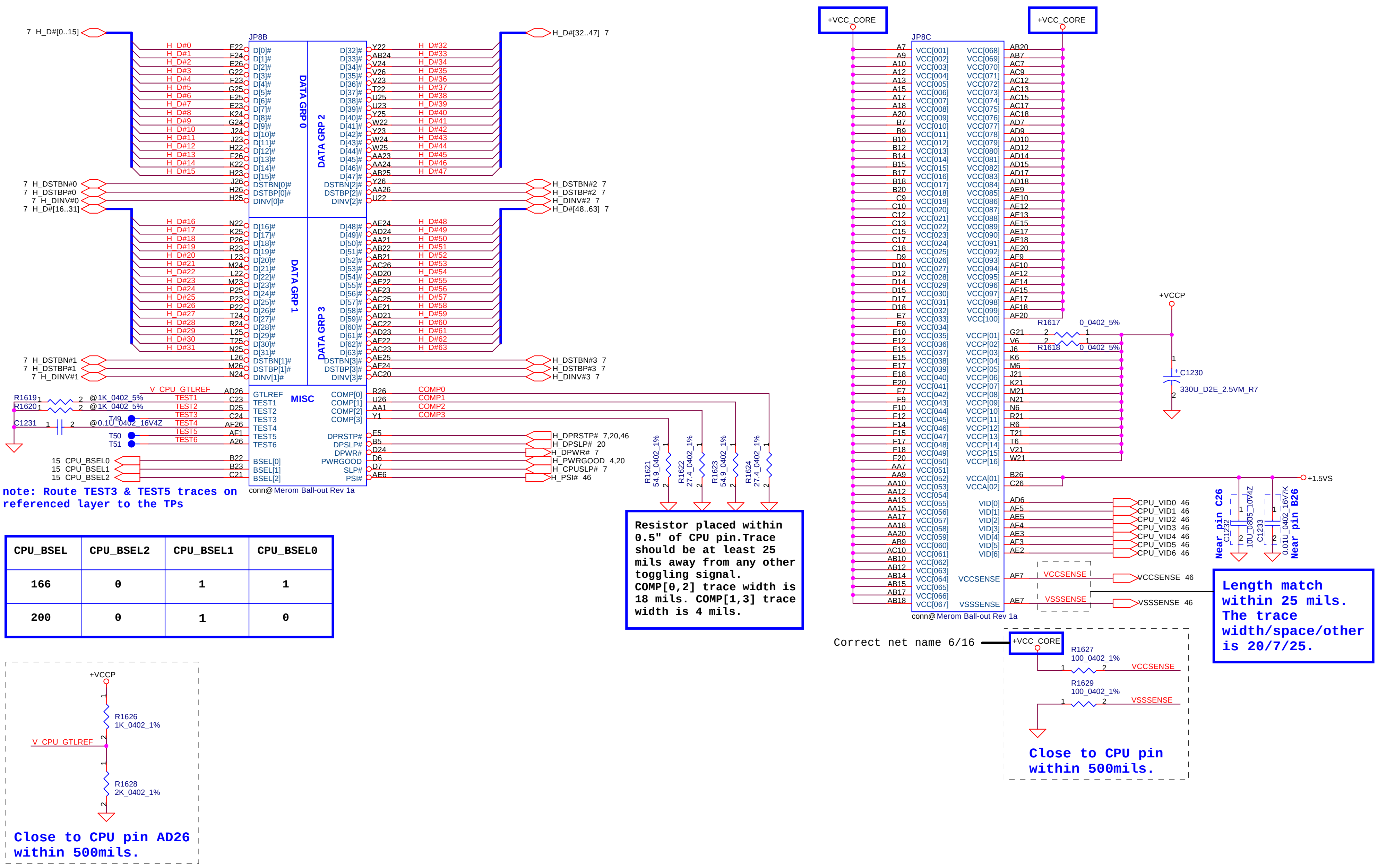
Rev 1.0

Correct net name 4/27



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

Correct net name 6/16

Close to CPU pin within 500mils.

Close to CPU pin AD26 within 500mils.

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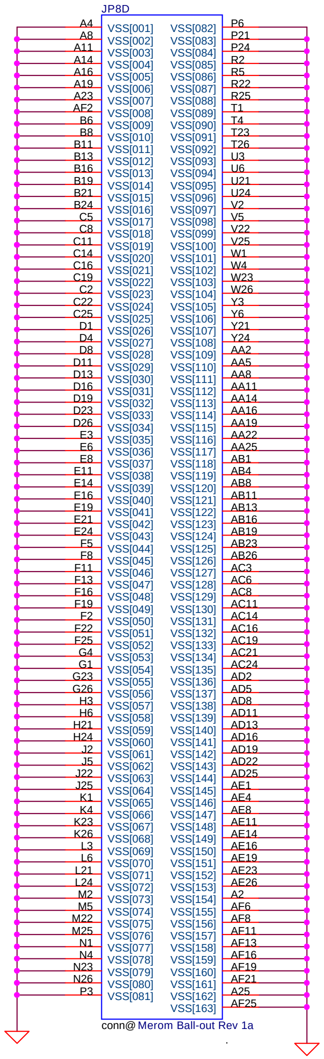
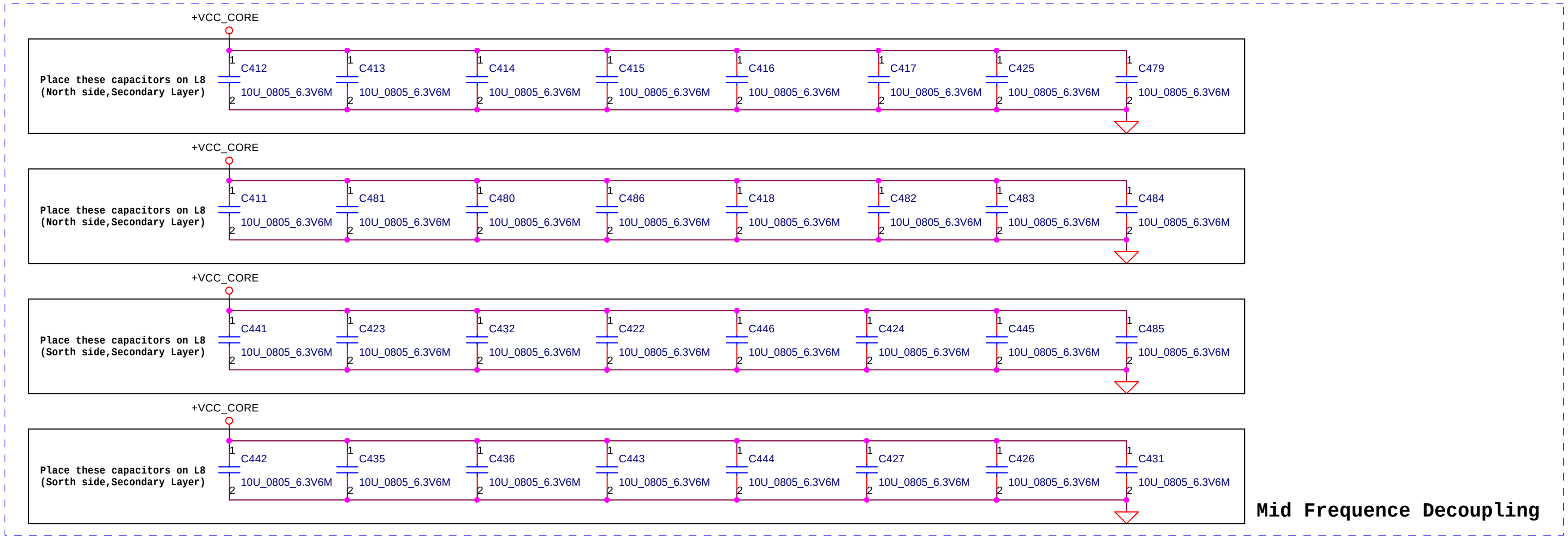
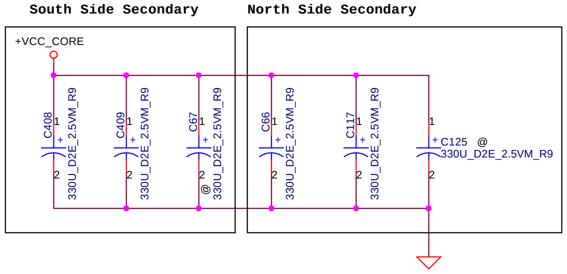


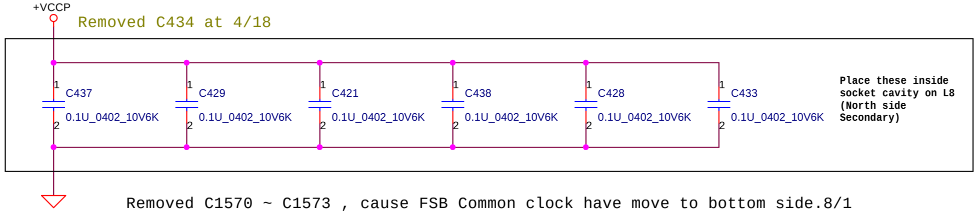


Mid Frequence Decoupling

No istall C67 , C125 at 2007/03/23.



ESR <= 1.5m ohm
Capacitor > 1980uF



Removed C434 at 4/18

Removed C1570 ~ C1573 , cause FSB Common clock have move to bottom side.8/1

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title
Merom(3/3)-GND&Bypass

Size Custom
Document Number *LA-3331P*
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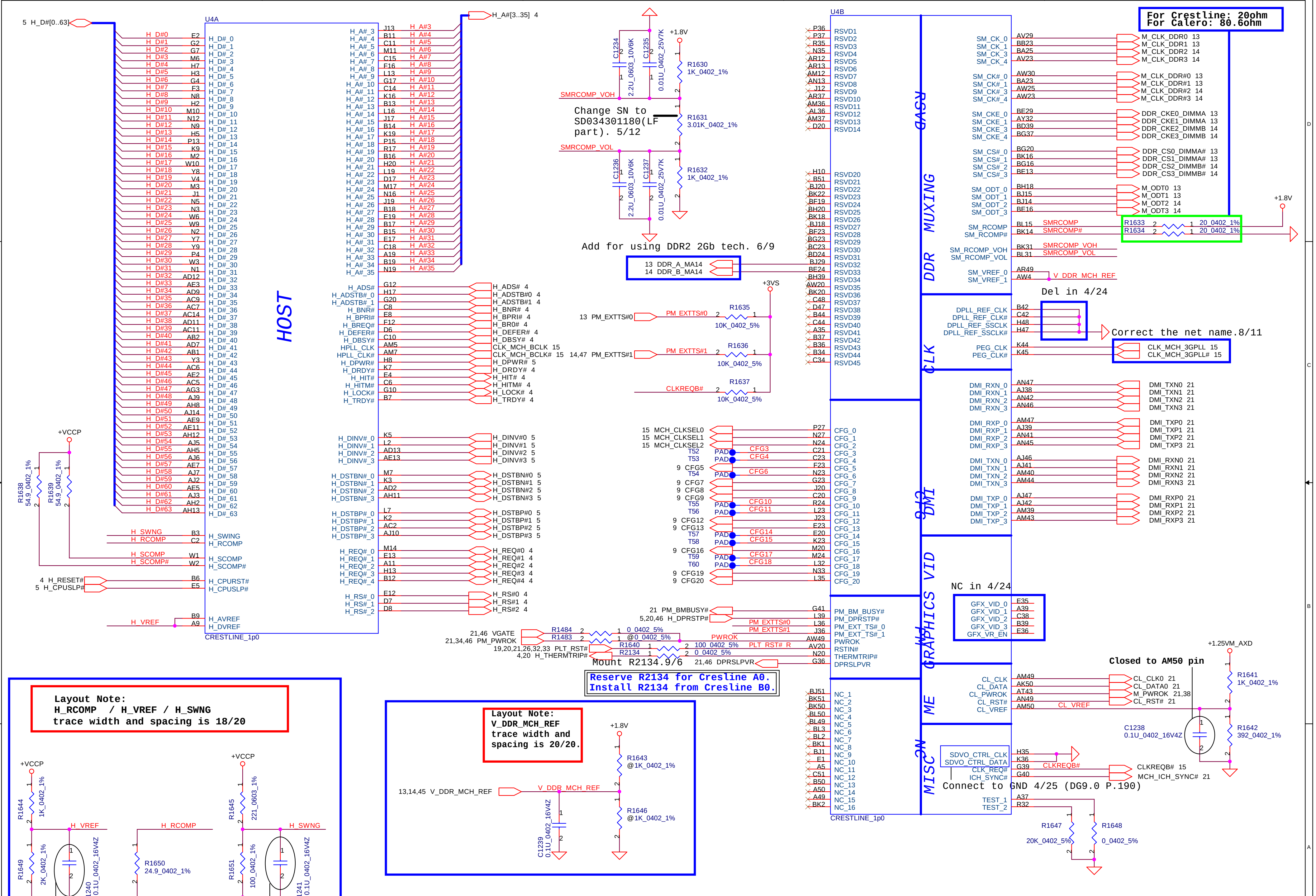

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 18/20

Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title: **CRESTLINE(1/6)-AGTL+/DMI/DDR2**
				Size: Custom; Document Number: LA-3331P; Rev 1.0
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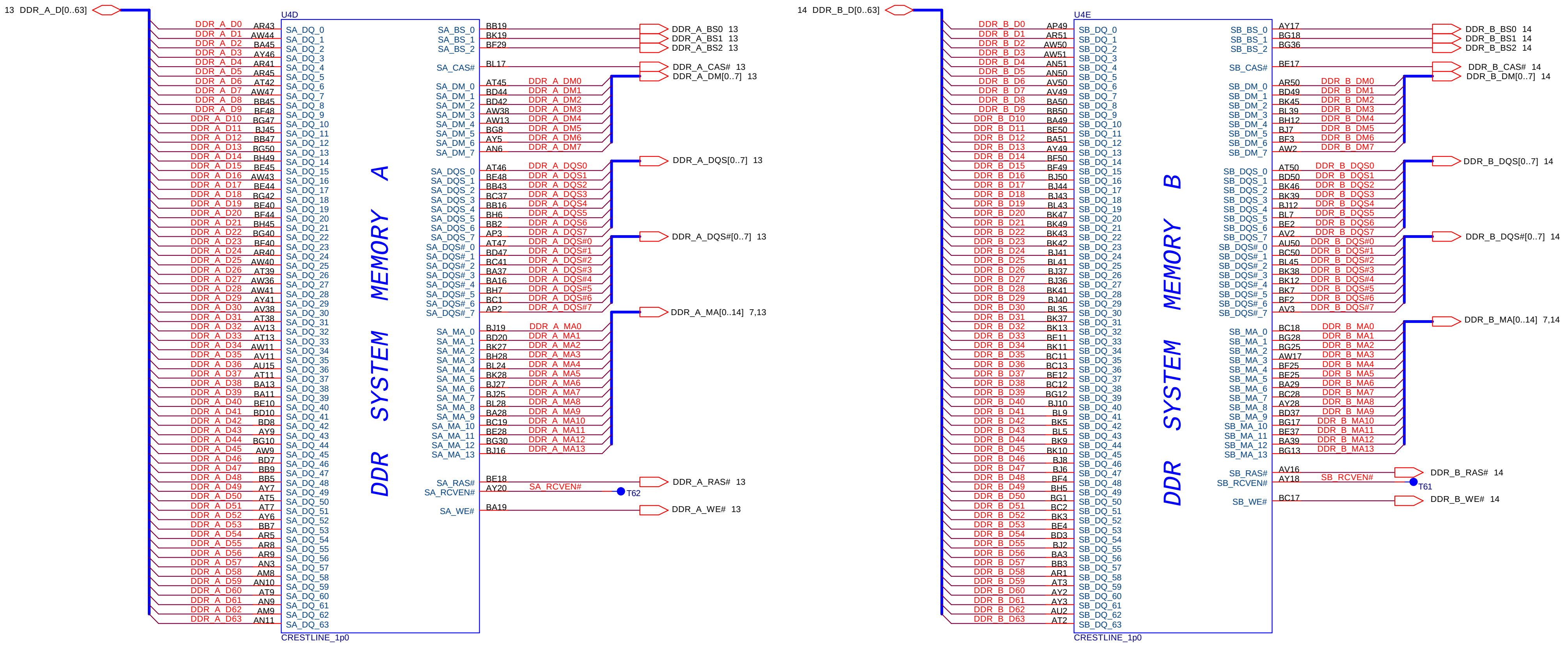

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Compal Electronics, Inc.

Title
CRESTLINE((2/6)-DDR2 A/B CH

Size	Document Number	Rev
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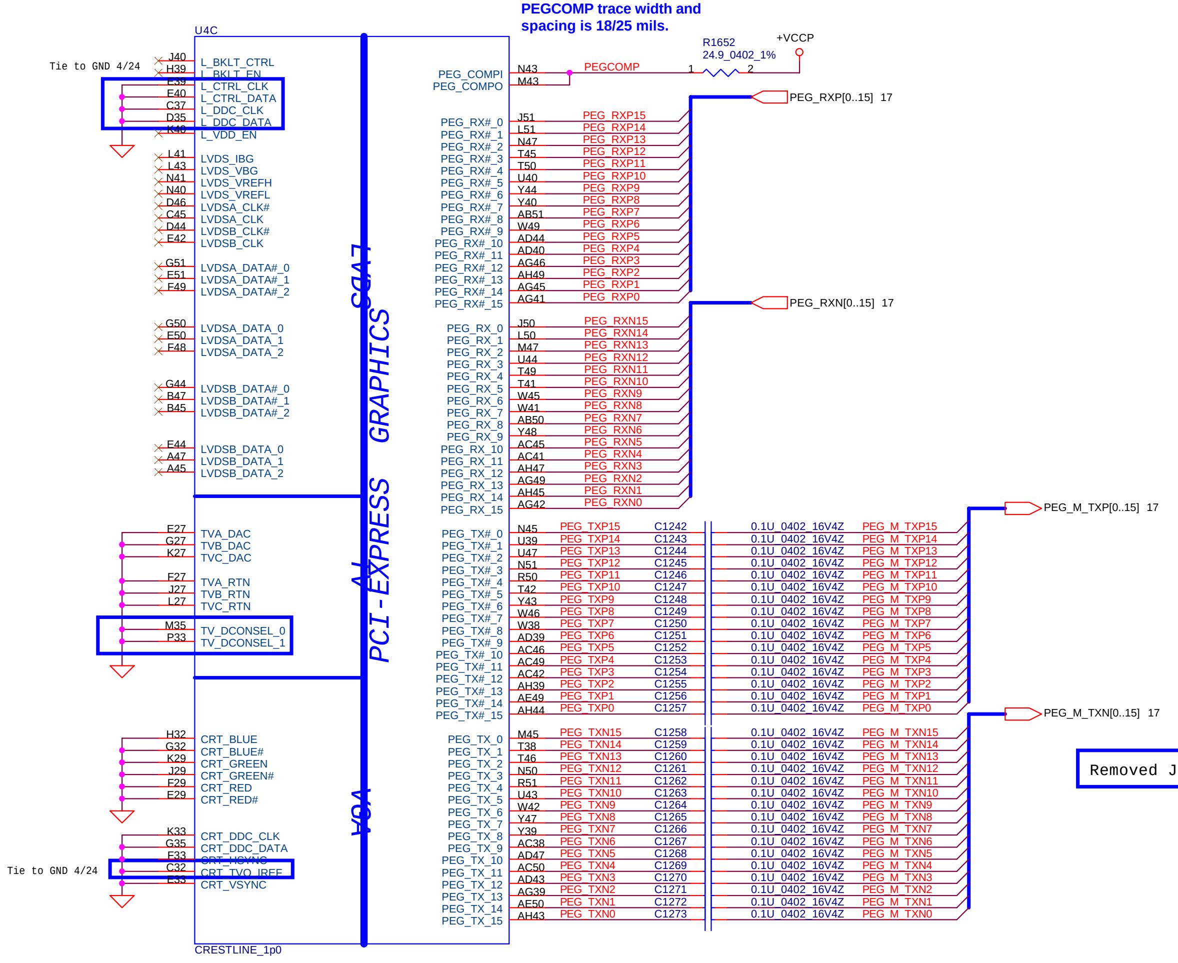
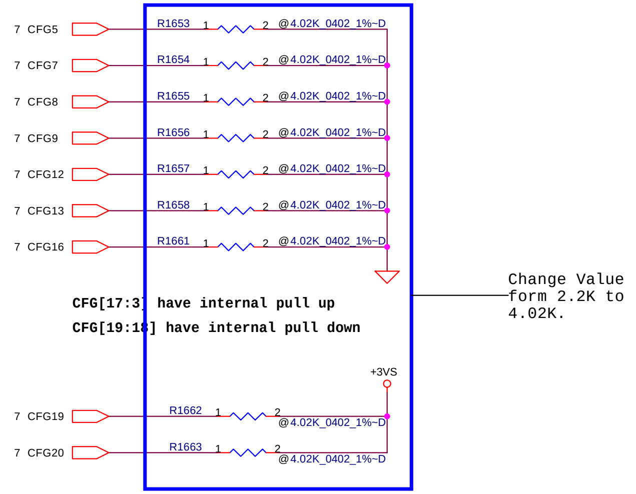


Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

Removed J14 4/27



CFG[17:3] have internal pull up

CFG[19:18] have internal pull down

Change Value form 2.2K to 4.02K.

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title: CRESTLINE((3/6)-VGA/LVDS/TV

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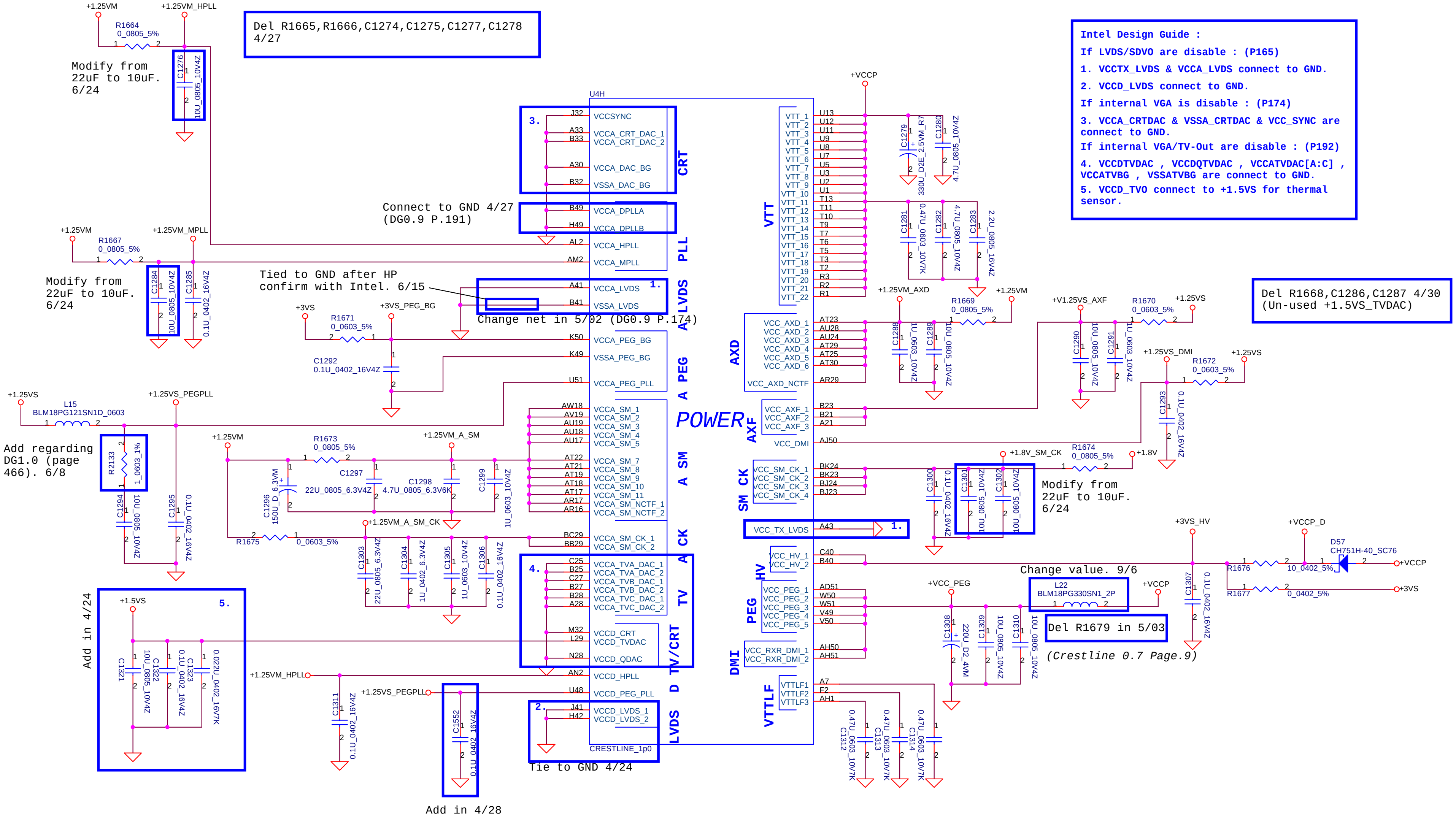

Del R1665,R1666,C1274,C1275,C1277,C1278
4/27

Modify from
22uF to 10uF.
6/24

Connect to GND 4/27
(DG0.9 P.191)

Modify from
22uF to 10uF.
6/24

Tied to GND after HP
confirm with Intel. 6/15

Change net in 5/02 (DG0.9 P.174)

Add regarding
DG1.0 (page
466). 6/8

Add in 4/24

Add in 4/28

Tie to GND 4/24

Intel Design Guide :

If LVDS/SDVO are disable : (P165)

1. VCCTX_LVDS & VCCA_LVDS connect to GND.

2. VCCD_LVDS connect to GND.

If internal VGA is disable : (P174)

3. VCCA_CRTDAC & VSSA_CRTDAC & VCC_SYNC are connect to GND.

If internal VGA/TV-Out are disable : (P192)

4. VCCDTVDAC , VCCDQTVDAC , VCCATVDAC[A:C] , VCCATVBG , VSSATVBG are connect to GND.

5. VCCD_TVO connect to +1.5VS for thermal sensor.

Del R1668,C1286,C1287 4/30
(Un-used +1.5VS_TVDAC)

Modify from
22uF to 10uF.
6/24

Change value. 9/6

Del R1679 in 5/03

(Crestline 0.7 Page.9)

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
CRESTLINE(4/6)-PWR

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Document Number *LA-3331P*
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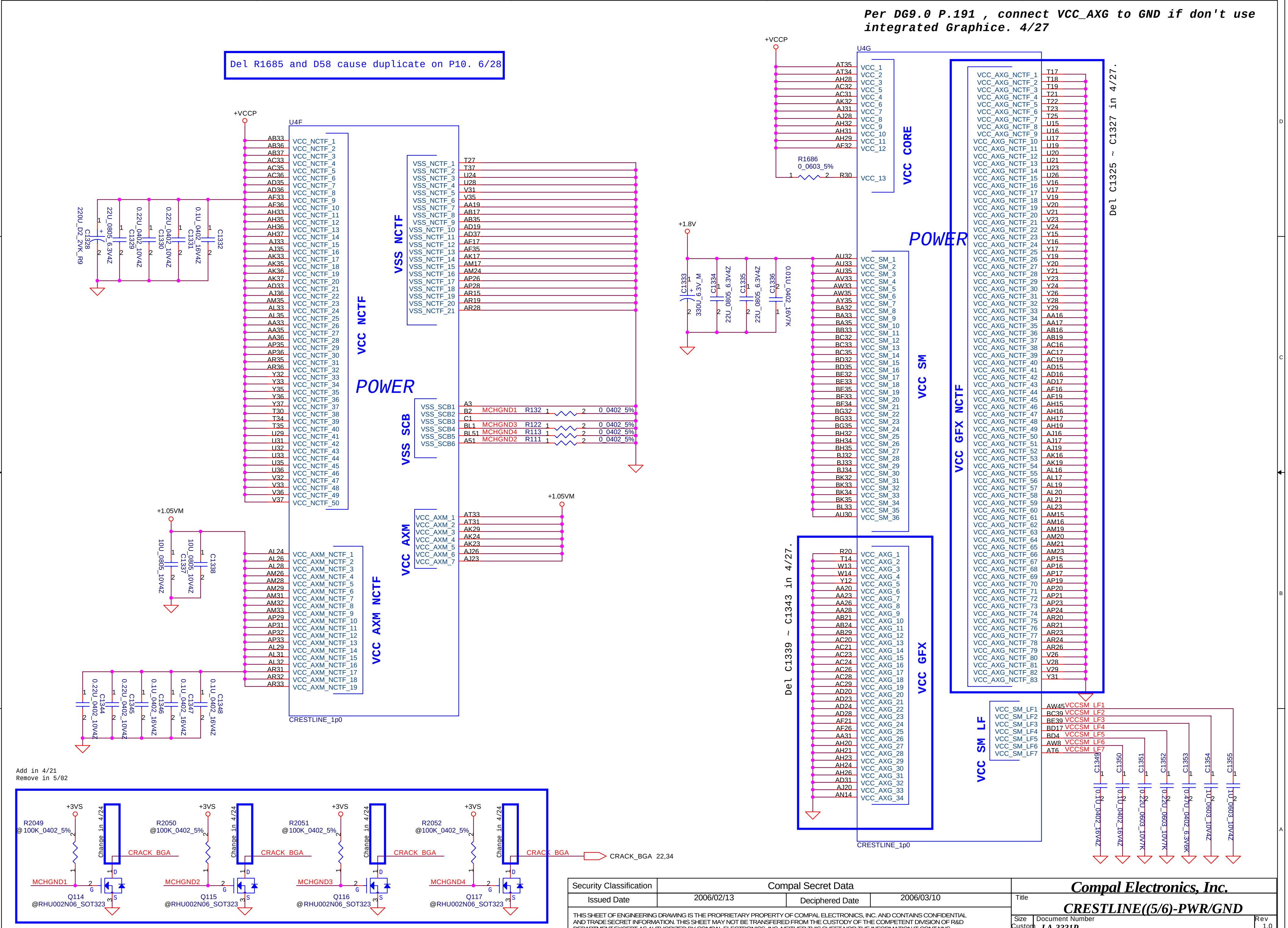

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Title
CRESTLINE((5/6)-PWR/GND

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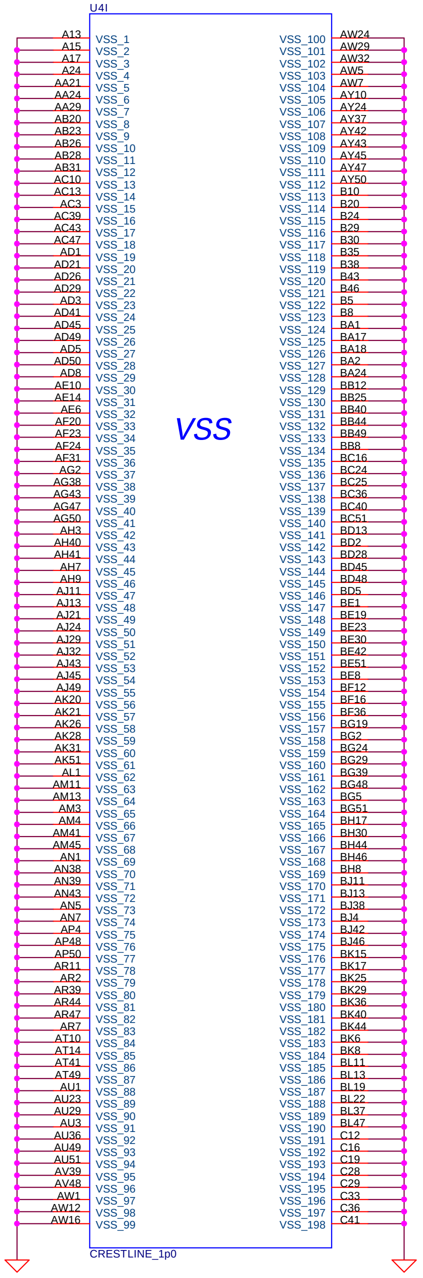

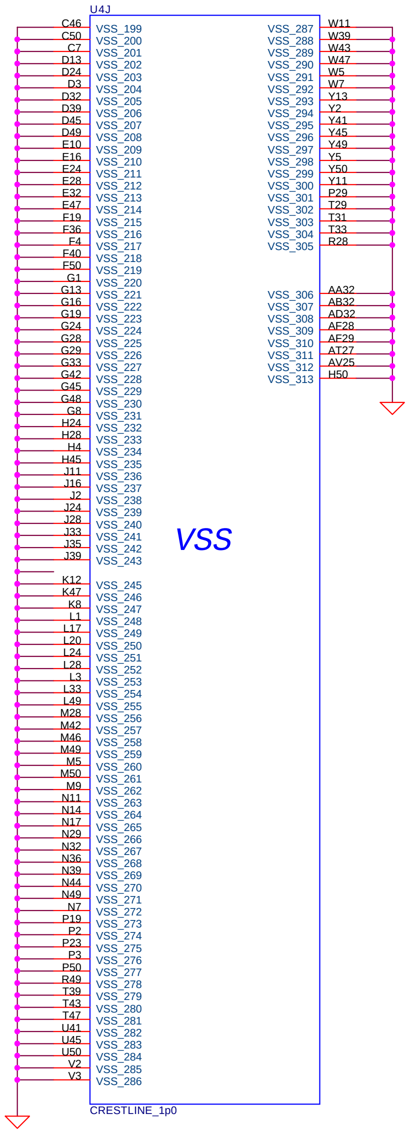

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Title
CRESTLINE((6/6)-PWR/GND

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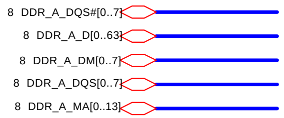
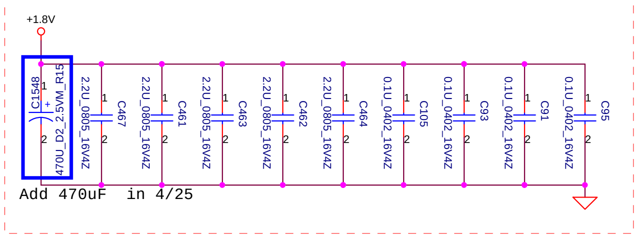
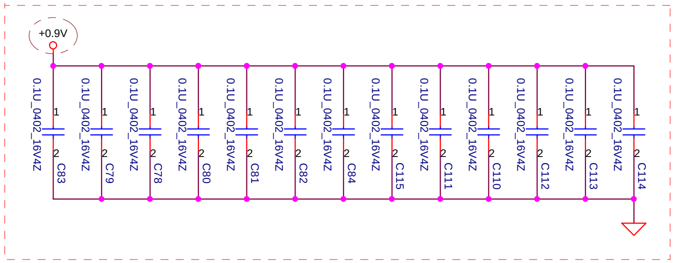


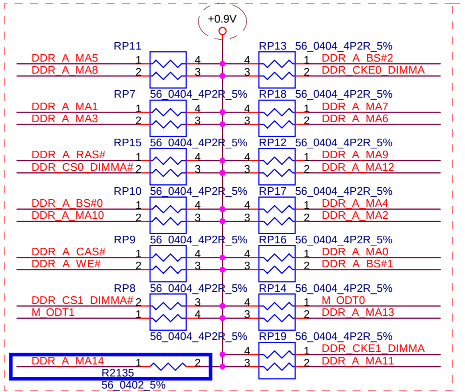
Layout Note:
Place near JP9



Add 470uF in 4/25

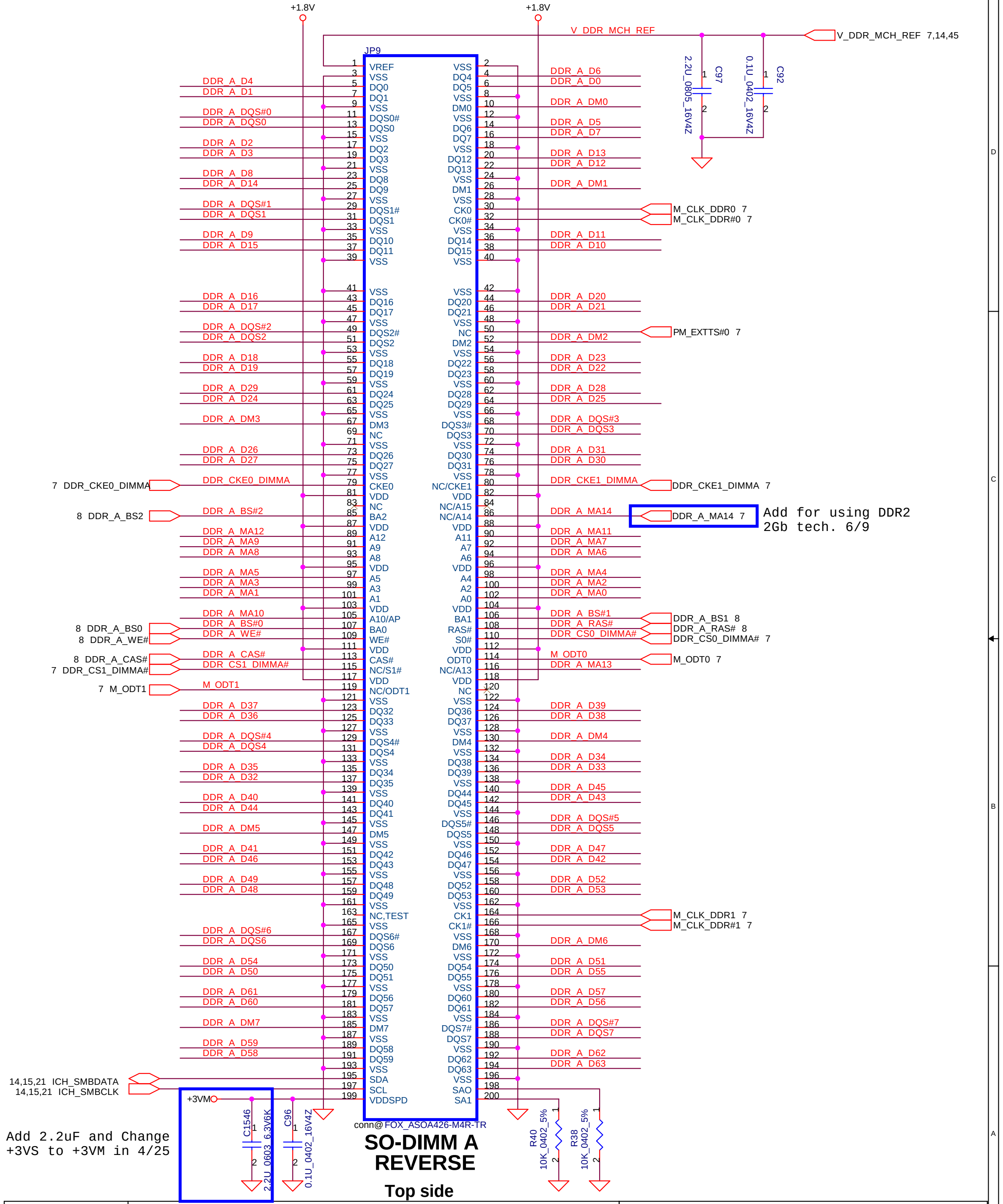
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V





Add for using DDR2 2Gb tech. 6/9

Layout Note:
Place these resistor closely JP9,all trace length Max=1.5"



Add for using DDR2 2Gb tech. 6/9

Add 2.2uF and Change +3VS to +3VM in 4/25

SO-DIMM A REVERSE

Top side

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title *DDRII-SODIMM SLOT1*
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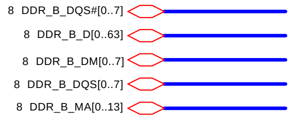
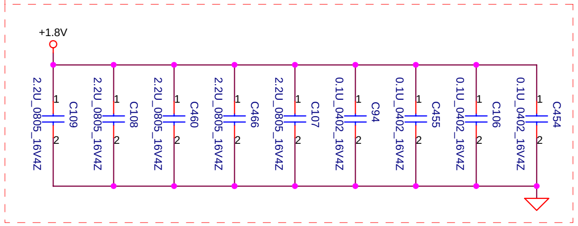
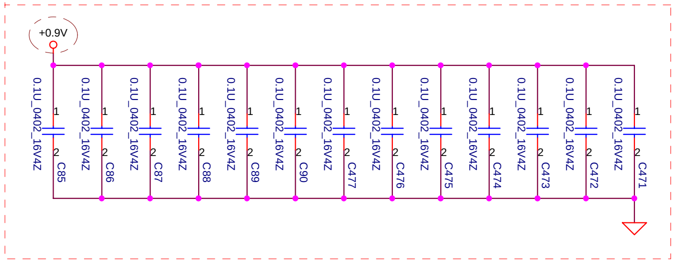


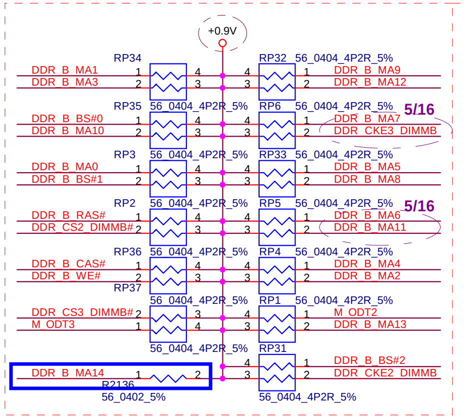
Layout Note:
Place near JP34



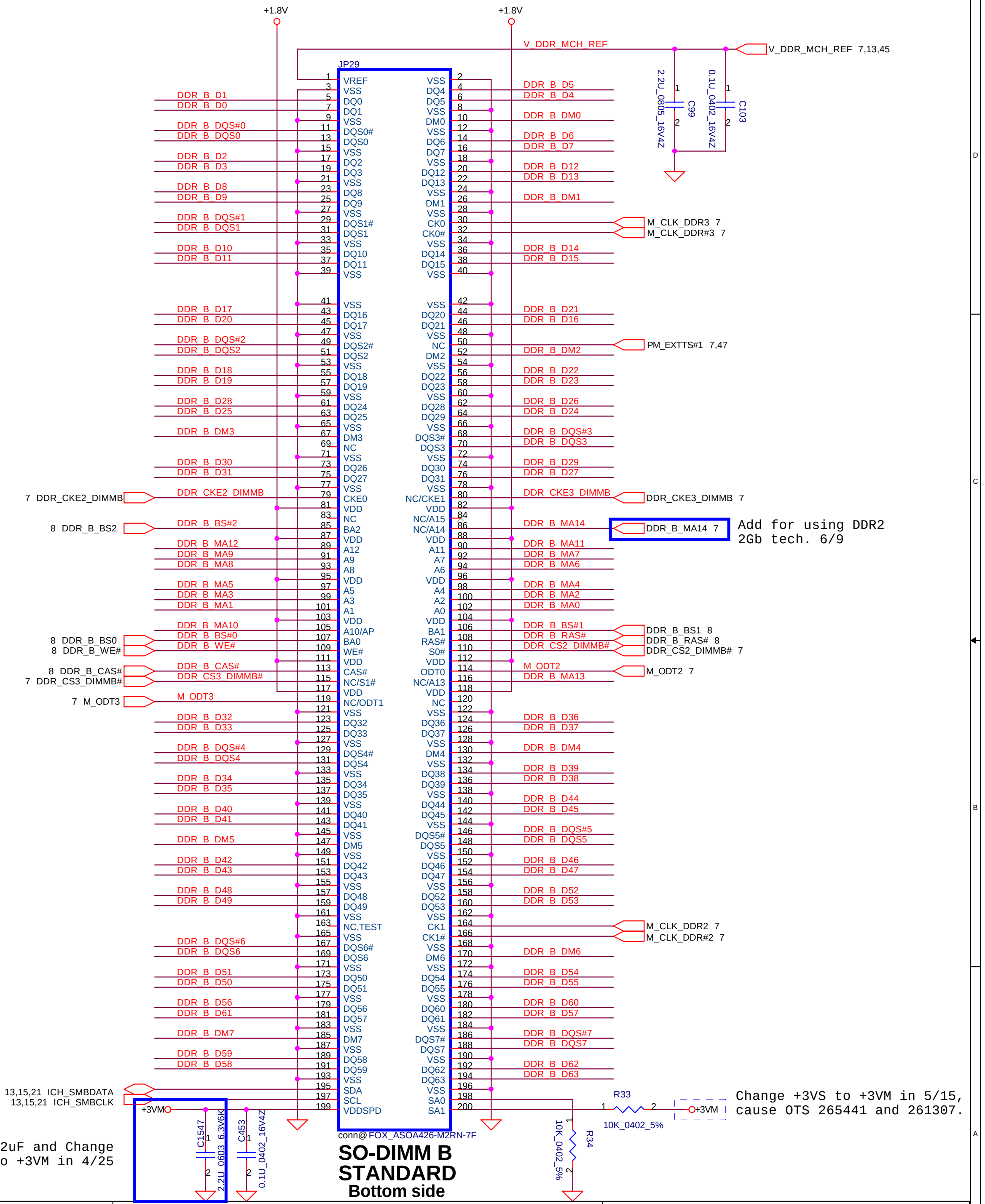
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"



Add for using DDR2 2Gb tech. 6/9



Add for using DDR2 2Gb tech. 6/9

Add 2.2uF and Change +3VS to +3VM in 4/25

Change +3VS to +3VM in 5/15, cause OTS 265441 and 261307.

SO-DIMM B STANDARD
Bottom side

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Compal Electronics, Inc.

Title
DDRII-SODIMM SLOT2

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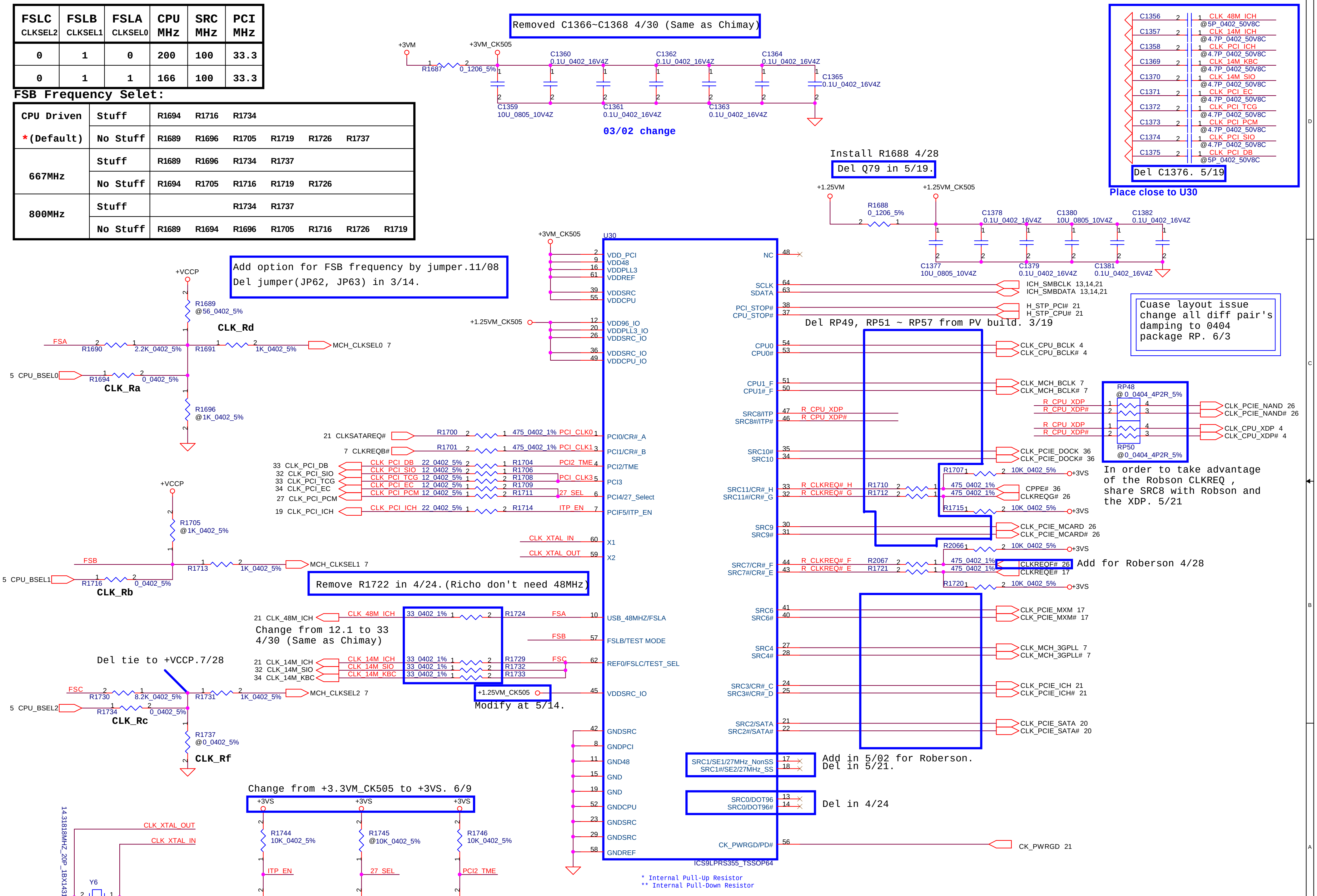
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1694 R1716 R1734
*(Default)	No Stuff	R1689 R1696 R1705 R1719 R1726 R1737
667MHz	Stuff	R1689 R1696 R1734 R1737
	No Stuff	R1694 R1705 R1716 R1719 R1726
800MHz	Stuff	R1734 R1737
	No Stuff	R1689 R1694 R1696 R1705 R1716 R1726 R1719



Removed C1366~C1368 4/30 (Same as Chimay)

03/02 change

Install R1688 4/28

Del Q79 in 5/19.

Del C1376. 5/19

Place close to U30

Add option for FSB frequency by jumper.11/08
Del jumper(JP62, JP63) in 3/14.

Cuase layout issue
change all diff pair's
damping to 0404
package RP. 6/3

Del RP49, RP51 ~ RP57 from PV build. 3/19

In order to take advantage
of the Robson CLKREQ ,
share SRC8 with Robson and
the XDP. 5/21

Add for Roberson 4/28

Remove R1722 in 4/24.(Richo don't need 48MHz)

Change from 12.1 to 33
4/30 (Same as Chimay)

Del tie to +VCCP.7/28

Modify at 5/14.

Add in 5/02 for Roberson.
Del in 5/21.

Del in 4/24

Change from +3.3VM_CK505 to +3VS. 6/9

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
CLOCK GENERATOR

Size Document Number *LA-3331P* Rev 1.0

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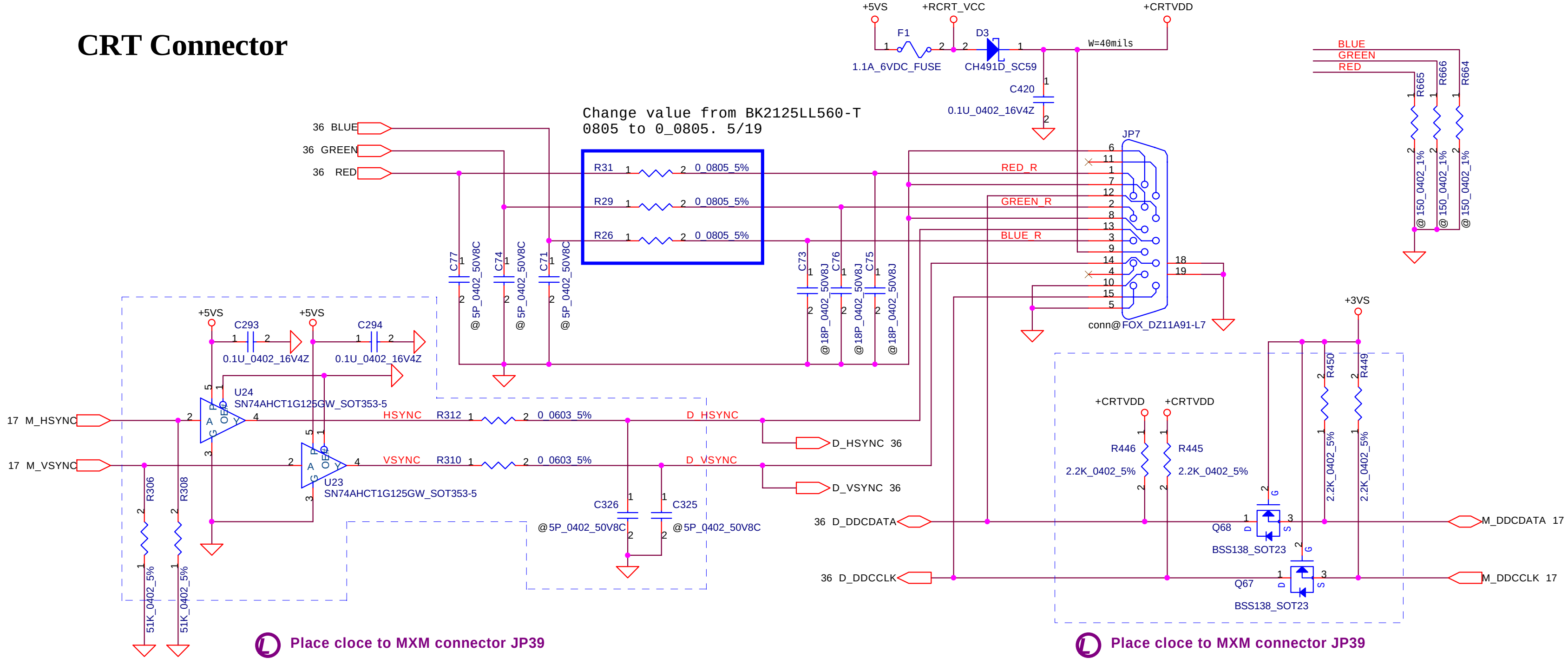
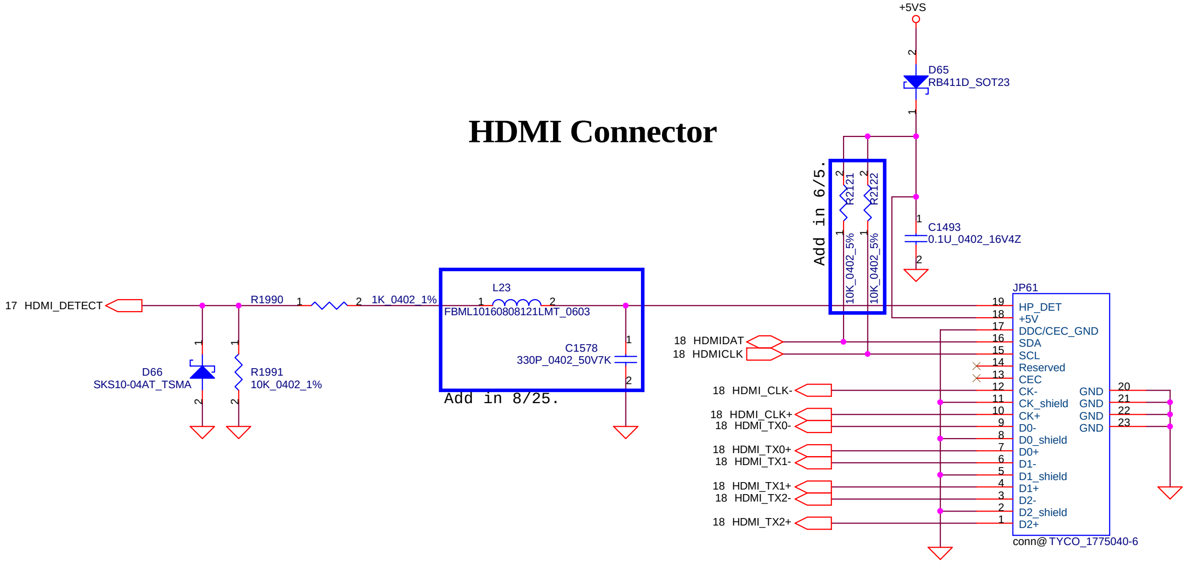
CRT Connector



Place cloce to MXM connector JP39

Place cloce to MXM connector JP39

HDMI Connector



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title: CRT & HDMI

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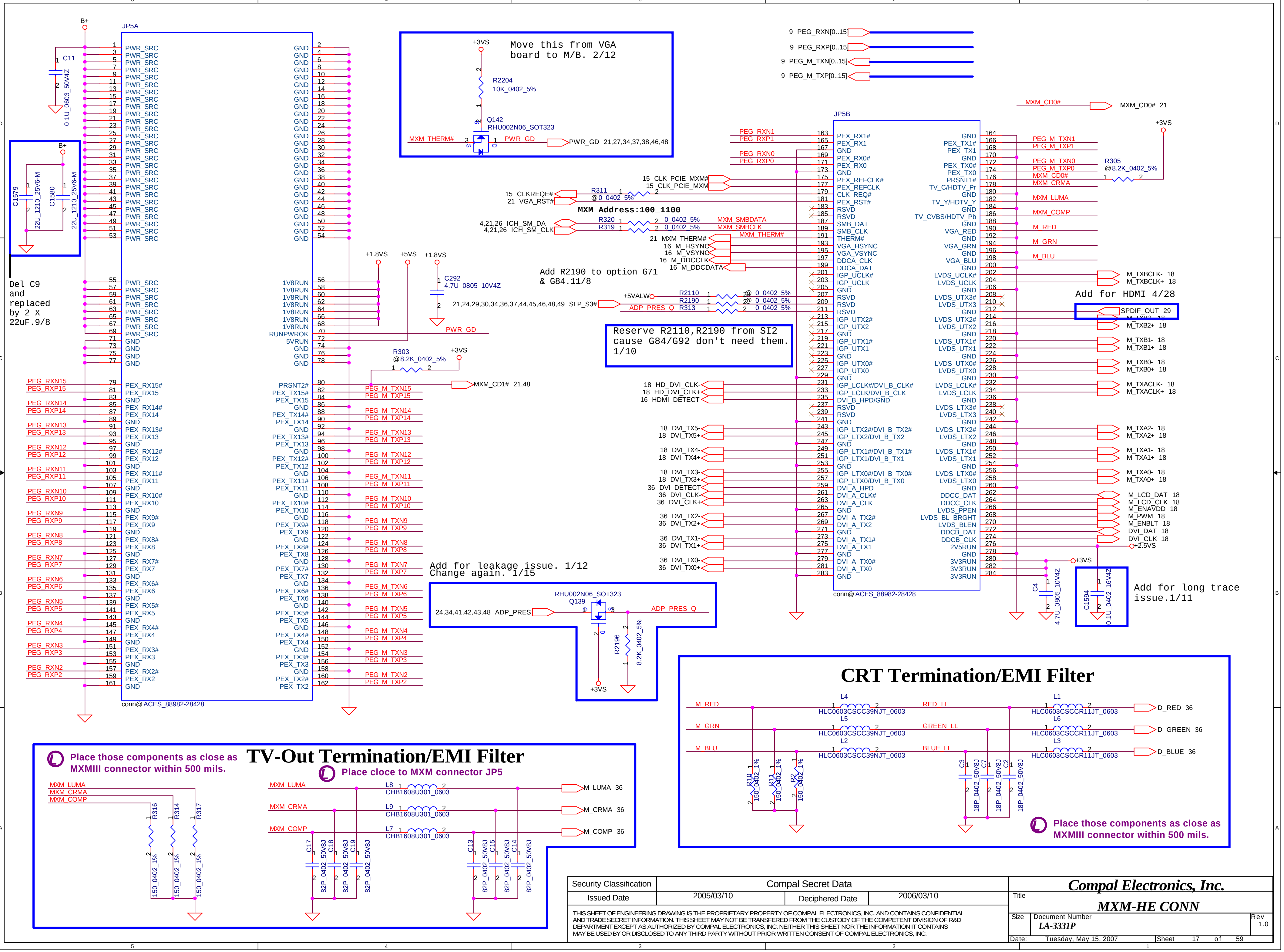

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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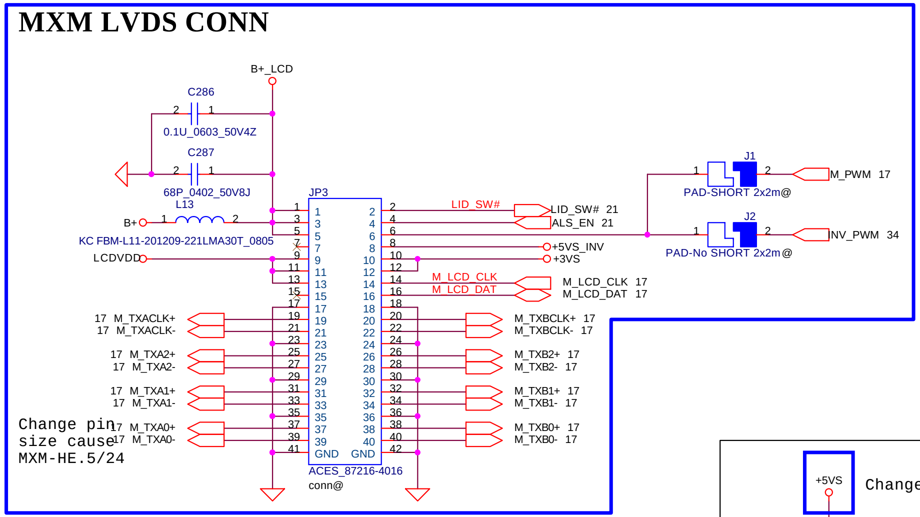
Compal Electronics, Inc.

Title: **MXM-HE CONN**

Size | Document Number: LA-3331P | Rev 1.0

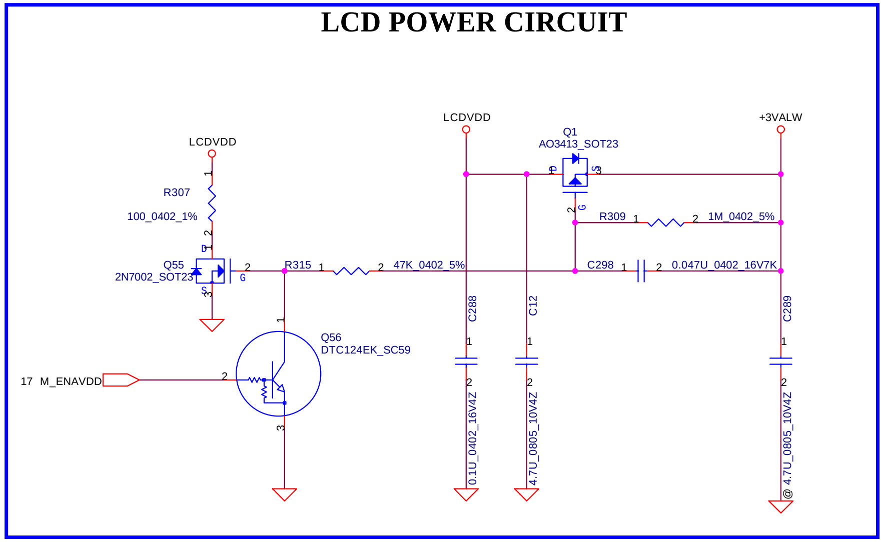
Date: Tuesday, May 15, 2007 | Sheet 17 of 59

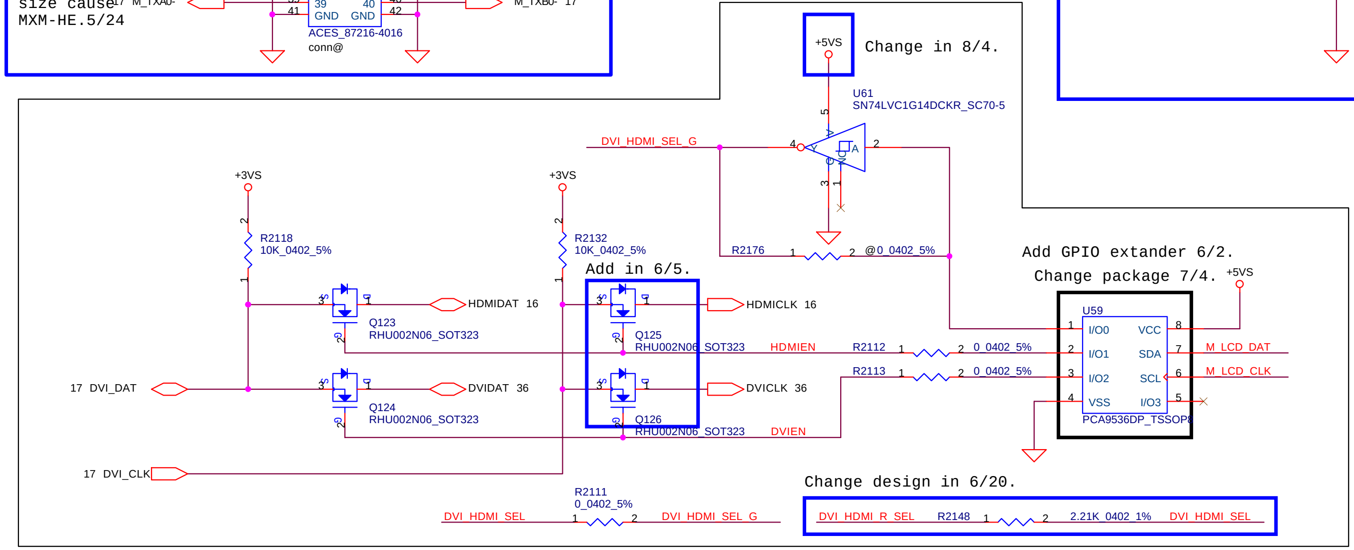
MXM LVDS CONN



Change pin size cause MXM-HE.5/24

LCD POWER CIRCUIT





Change in 8/4.

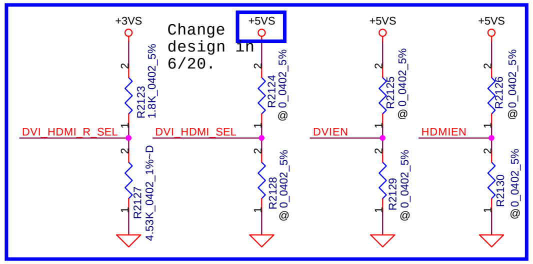
Add in 6/5.

Add GPIO extander 6/2.

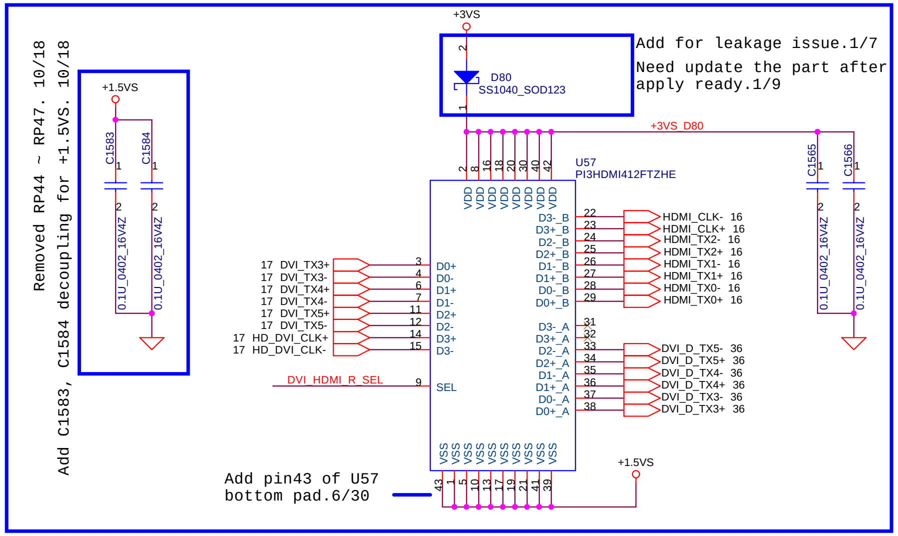
Change package 7/4.

Change design in 6/20.

Function option , Add in 6/5. (Reserved at 6/6)



Change design in 6/20.

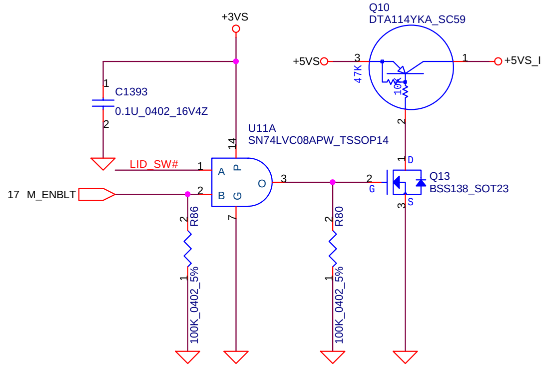


Removed RP44 ~ RP47. 10/18

Add C1583, C1584 decoupling for +1.5VS. 10/18

Add for leakage issue.1/7
Need update the part after apply ready.1/9

Add pin43 of U57 bottom pad.6/30



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title: LCD CONN & Q-Switch & GPIO Ext.

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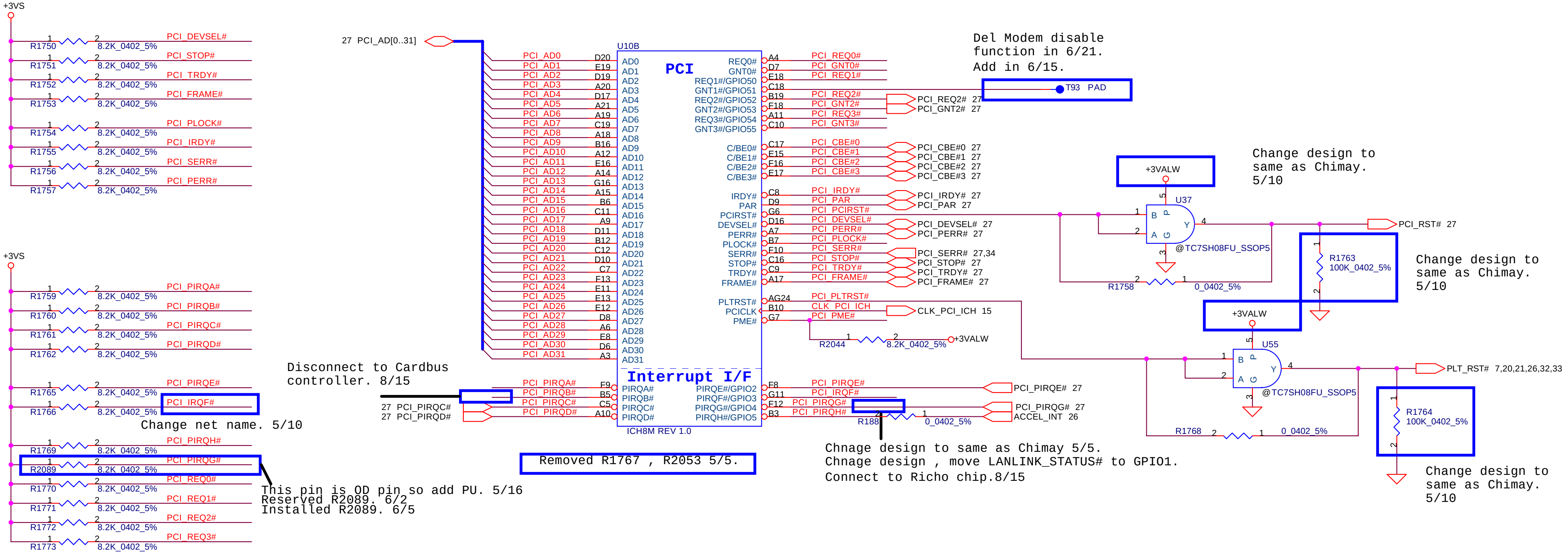


Del Modem disable function in 6/21.
Add in 6/15.

Change design to same as Chimay.
5/10

Change design to same as Chimay.
5/10

Disconnect to Cardbus controller. 8/15

Change net name. 5/10

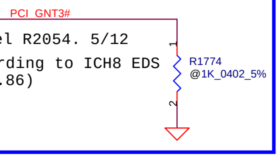
Removed R1767 , R2053 5/5.

This pin is OD pin so add PU. 5/16
Reserved R2089. 6/2
Installed R2089. 6/5

Chnage design to same as Chimay 5/5.
Chnage design , move LANLINK_STATUS# to GPIO1.
Connect to Richo chip.8/15

Change design to same as Chimay.
5/10

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



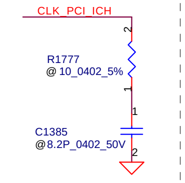
Del R2054. 5/12

(According to ICH8 EDS 1.5 P.86)

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

Place closely pin B10



Security Classification	Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date 2006/03/10

Compal Electronics, Inc.

Title
ICH8(1/4)-PCI/INT

Size Document Number *LA-3331P* Rev 1.0

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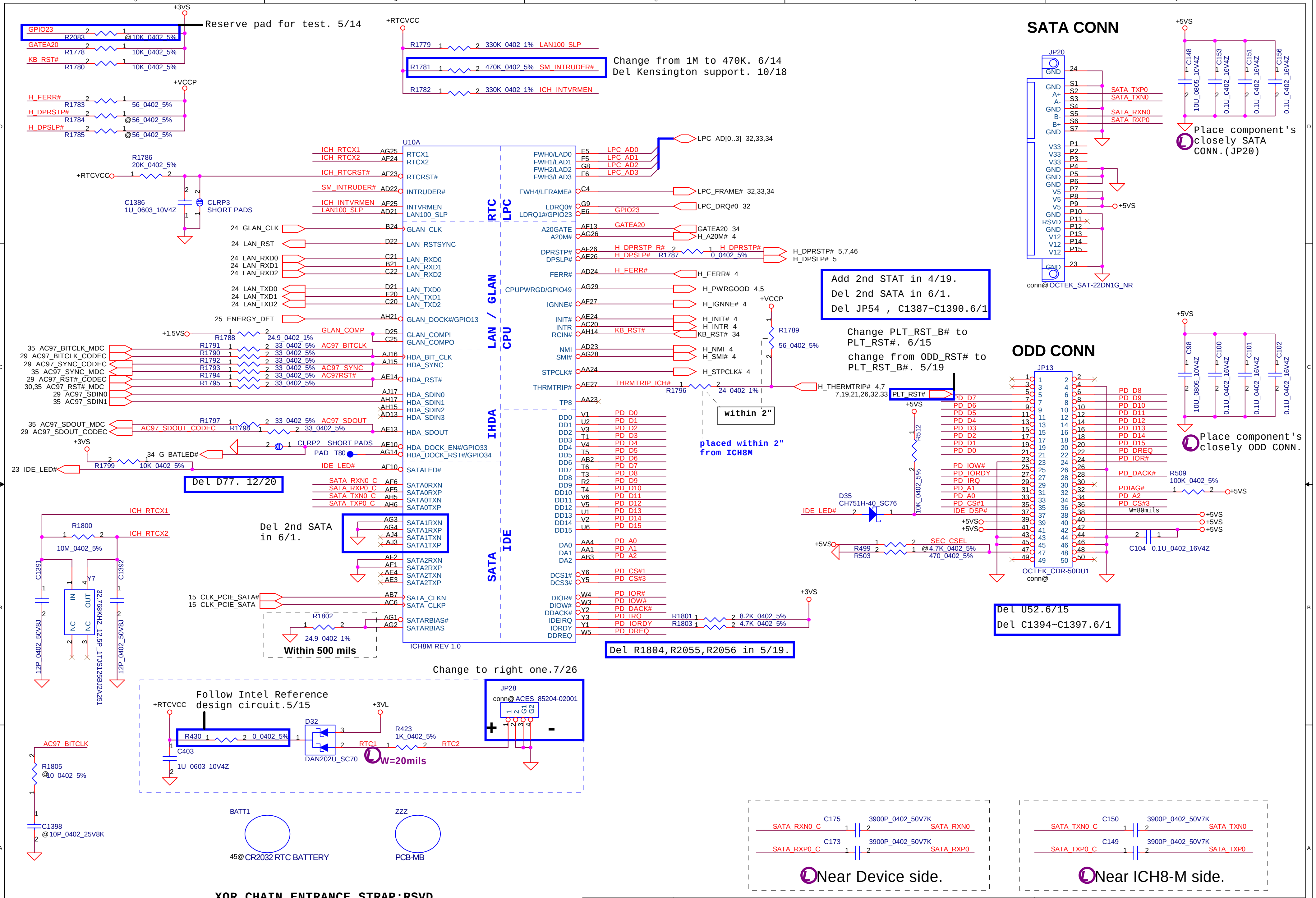

Reserve pad for test. 5/14

Change from 1M to 470K. 6/14
Del Kensington support. 10/18

Place component's closely SATA CONN.(JP20)

Add 2nd STAT in 4/19.
Del 2nd SATA in 6/1.
Del JP54 , C1387~C1390.6/1

Change PLT_RST_B# to PLT_RST#. 6/15

change from ODD_RST# to PLT_RST_B#. 5/19

within 2"

placed within 2" from ICH8M

Place component's closely ODD CONN.

Del D77. 12/20

Del 2nd SATA in 6/1.

Within 500 mils

Del U52.6/15
Del C1394~C1397.6/1

Del R1804,R2055,R2056 in 5/19.

Change to right one.7/26

Follow Intel Reference design circuit.5/15

Near Device side.

Near ICH8-M side.

XOR CHAIN ENTRANCE STRAP:RSVD

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
ICH8(2/4)_LAN,HD,IDE,LPC

Size Custom
Document Number LA-3331P
Rev 1.0

Date: Tuesday, May 15, 2007
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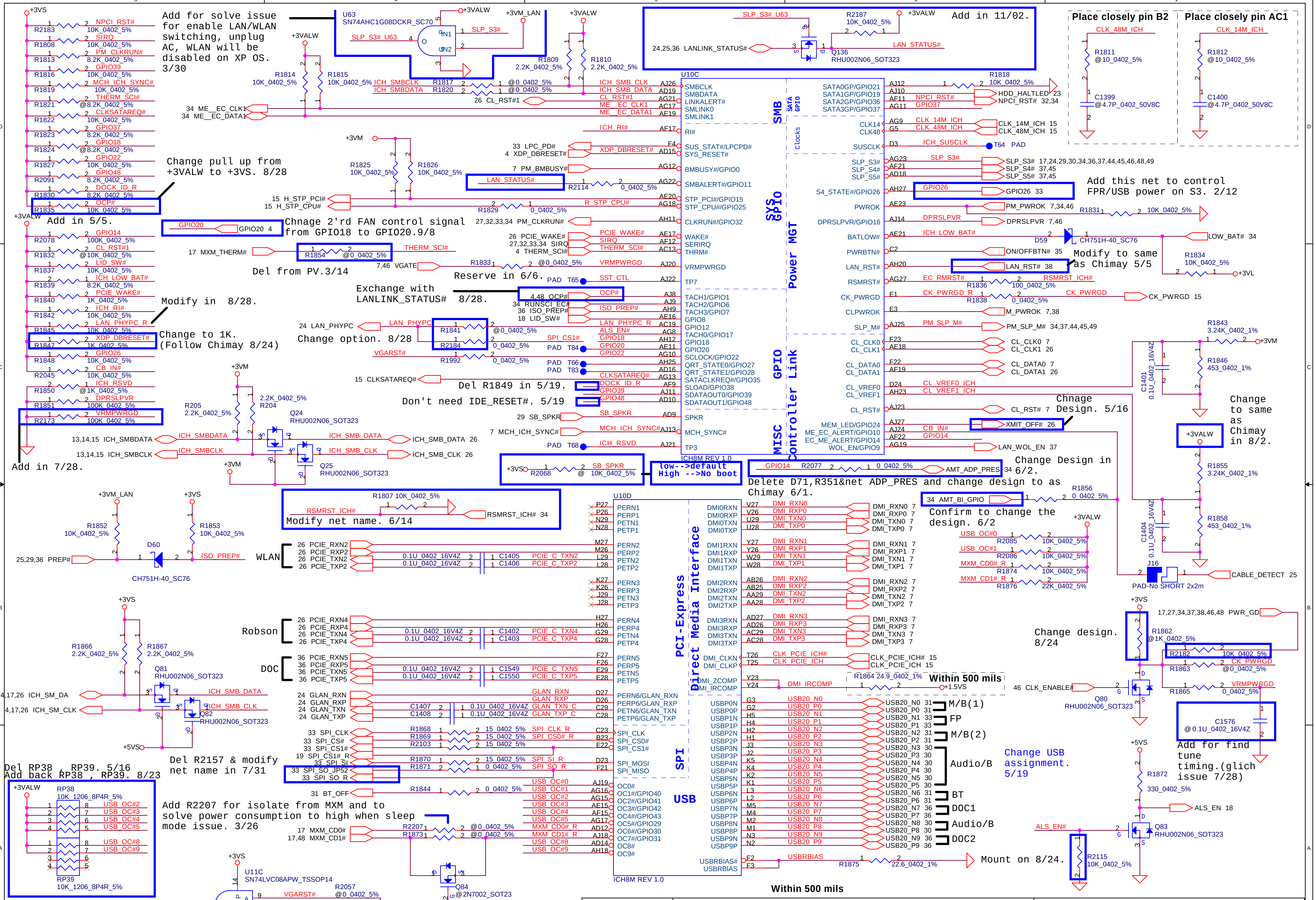

Add for solve issue for enable LAN/WLAN switching, unplug AC, WLAN will be disabled on XP OS. 3/30

Add in 11/02.

Place closely pin B2

Place closely pin AC1

Change pull up from +3VALW to +3VS. 8/28

Add in 5/5.

Chnage 2'rd FAN control signal from GPIO18 to GPIO20.9/8

Del from PV.3/14

Reserve in 6/6.

Exchange with LANLINK_STATUS# 8/28.

Modify in 8/28.

Change to 1K. (Follow Chimay 8/24)

Change option. 8/28

Del R1849 in 5/19.

Don't need IDE_RESET#. 5/19

Add in 7/28.

Add this net to control FPR/USB power on S3. 2/12

Modify to same as Chimay 5/5

Chnage Design. 5/16

Change to same as Chimay in 8/2.

low-->default High -->No boot

Change Design in 6/2.

Delete D71,R351&net ADP_PRES and change design to as Chimay 6/1.

Confirm to change the design. 6/2

Modify net name. 6/14

Change design. 8/24

Within 500 mils

Change USB assignment. 5/19

Add for find tune timing.(glich issue 7/28)

Del RP38 , RP39. 5/16 Add back RP38 , RP39. 8/23

Del R2157 & modify net name in 7/31

Add R2207 for isolate from MXM and to solve power consumption to high when sleep mode issue. 3/26

Mount on 8/24.

Within 500 mils

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title

ICH8(3/4)_PM,USB,GPIO

Size	Document Number	Rev
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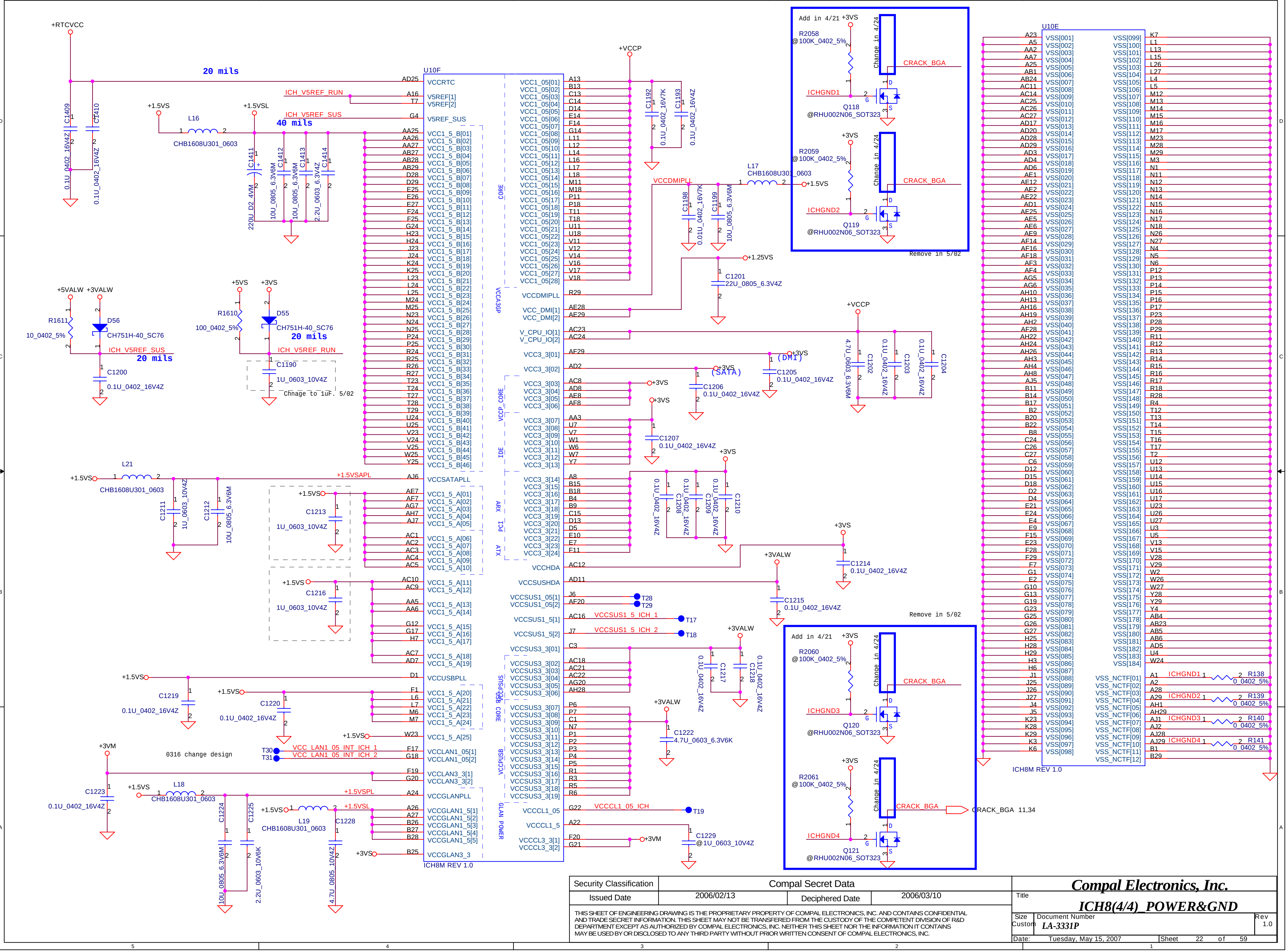

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
ICH8(4/4)_POWER&GND

Size Custom
Document Number LA-3331P
Rev 1.0

Date: Tuesday, May 15, 2007
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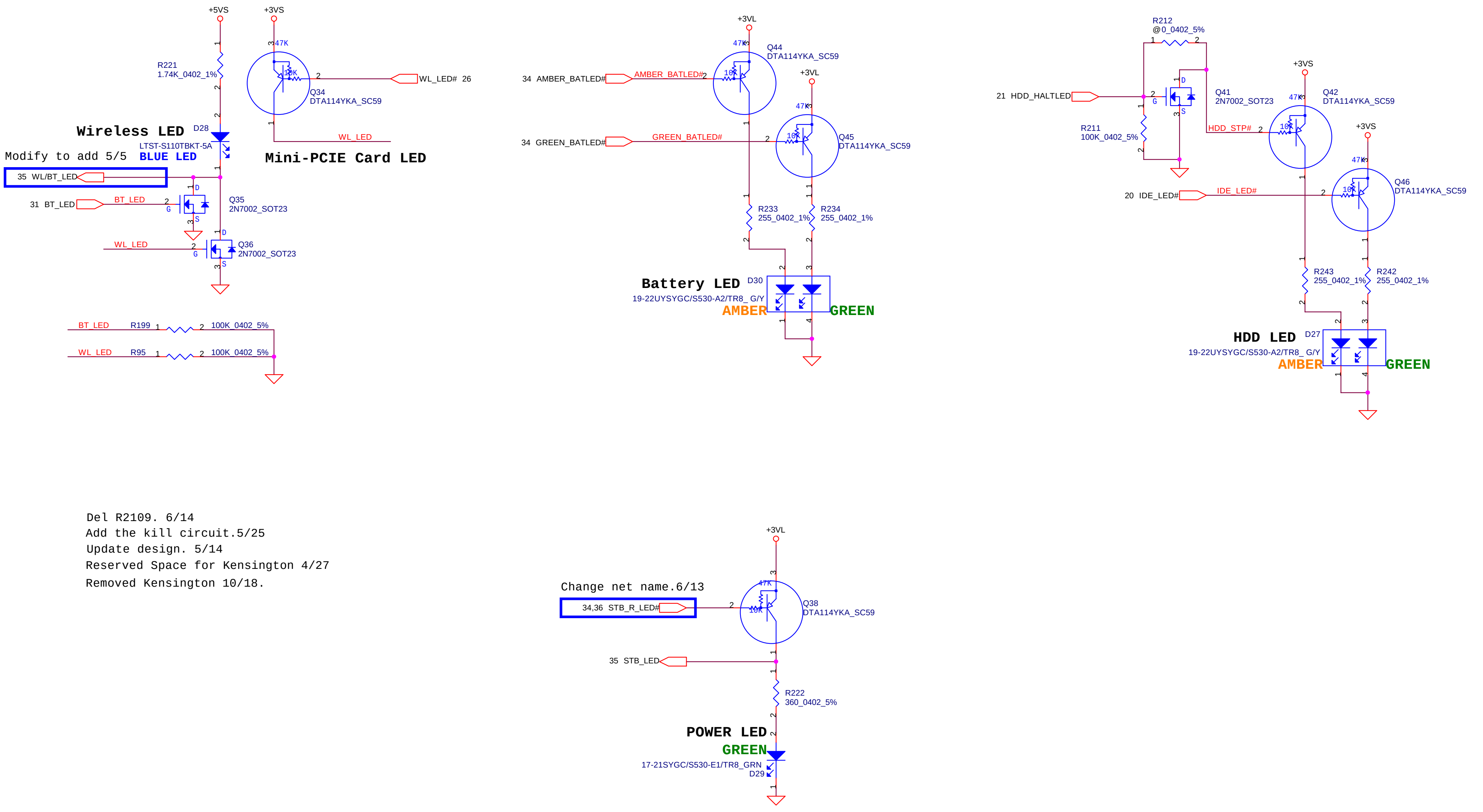


Del R2109. 6/14
Add the kill circuit.5/25
Update design. 5/14
Reserved Space for Kensington 4/27
Removed Kensington 10/18.

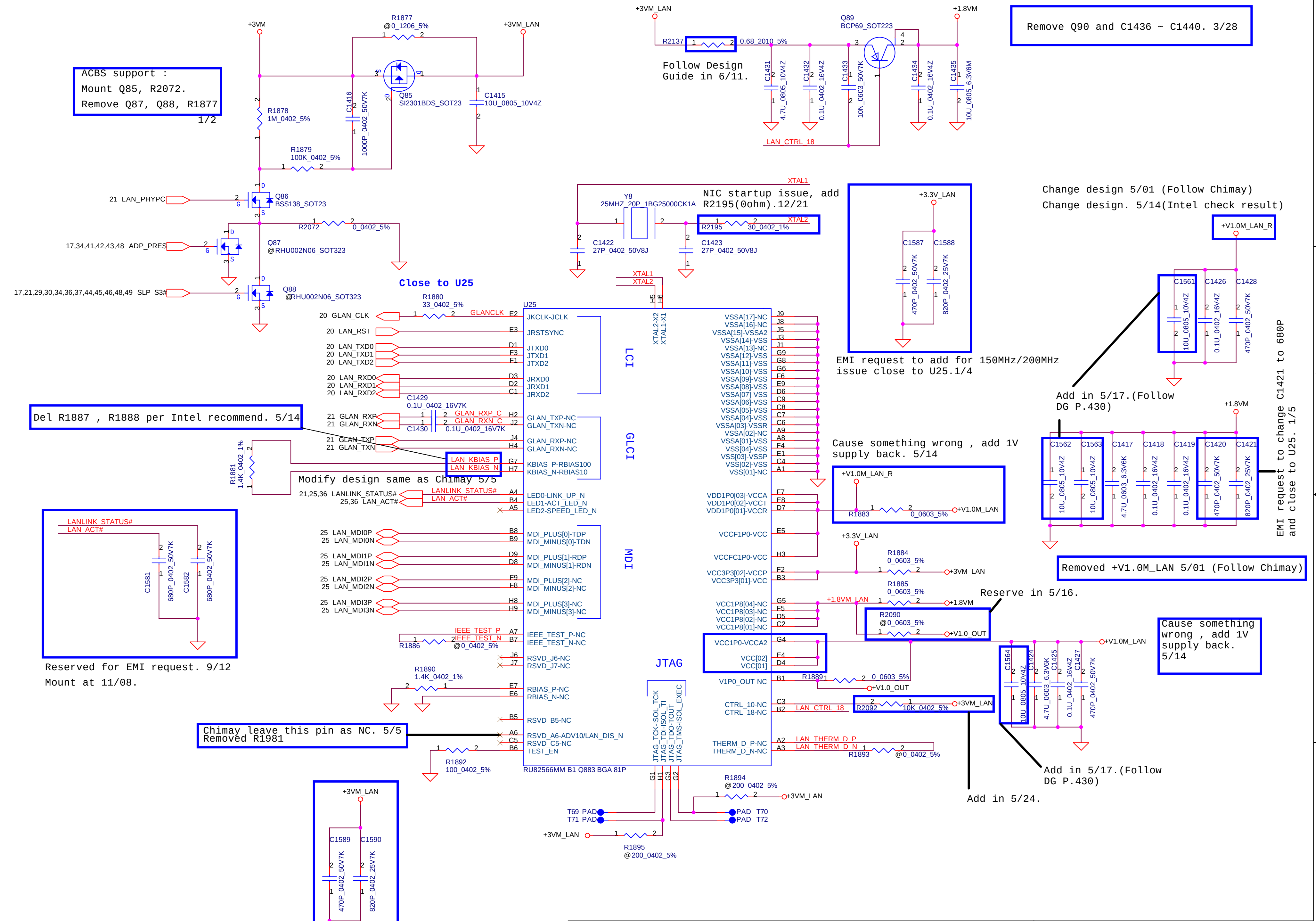
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
LEDS & Kensington

Size Custom
Document Number **LA-3331P**
Rev 1.0

Date: Tuesday, May 15, 2007 Sheet 23 of 59



Remove Q90 and C1436 ~ C1440. 3/28

ACBS support :
Mount Q85, R2072.
Remove Q87, Q88, R1877
1/2

Follow Design
Guide in 6/11.

NIC startup issue, add
R2195(0ohm).12/21

Close to U25

Change design 5/01 (Follow Chimay)
Change design. 5/14(Intel check result)

EMI request to add for 150MHz/200MHz
issue close to U25.1/4

Add in 5/17.(Follow
DG P.430)

EMI request to change C1421 to 680P
and close to U25. 1/5

Del R1887 , R1888 per Intel recommend. 5/14

Modify design same as Chimay 5/5

Cause something wrong , add 1V
supply back. 5/14

Removed +V1.0M_LAN 5/01 (Follow Chimay)

Reserve in 5/16.

Reserved for EMI request. 9/12
Mount at 11/08.

Cause something
wrong , add 1V
supply back.
5/14

Chimay leave this pin as NC. 5/5
Removed R1981

Add in 5/17.(Follow
DG P.430)

Add in 5/24.

EMI request to add for 150MHz/200MHz
issue close to R1894.1/4

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Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title Intel 82566 Nineveh

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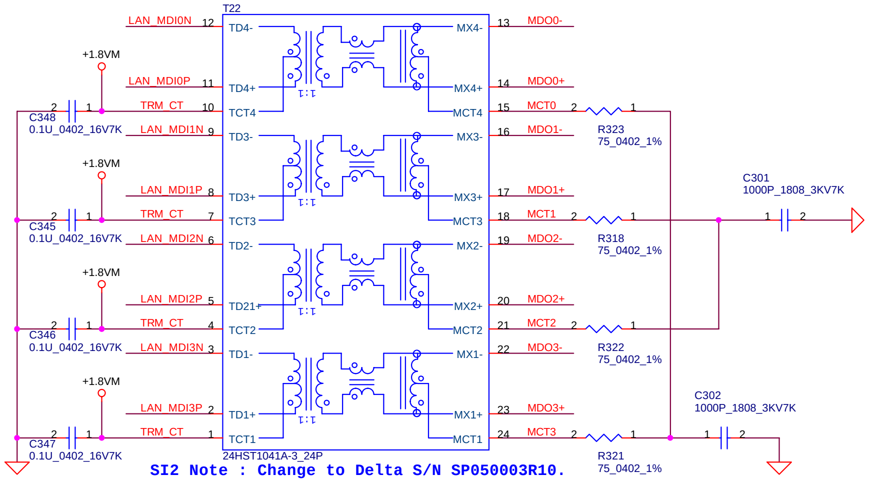
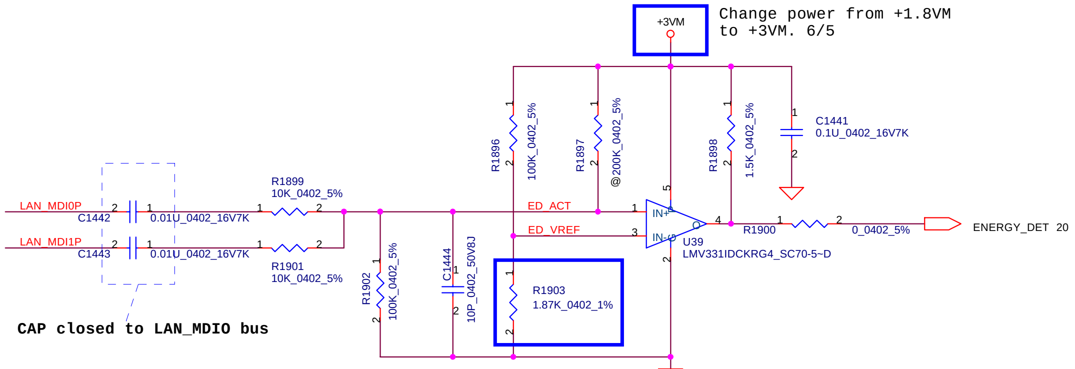
LAN ENERGY DET



SI2 Note : Change to Delta S/N SP050003R10.

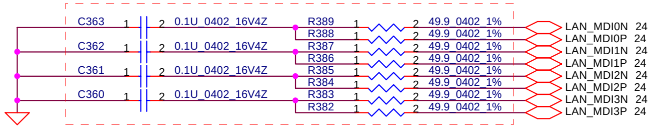


Change power from +1.8VM to +3VM. 6/5

CAP closed to LAN_MDIO bus

Intel design change WW44.11/6
Design chnage from HP per Intel's request from 1.4K to 1.87K.12/18

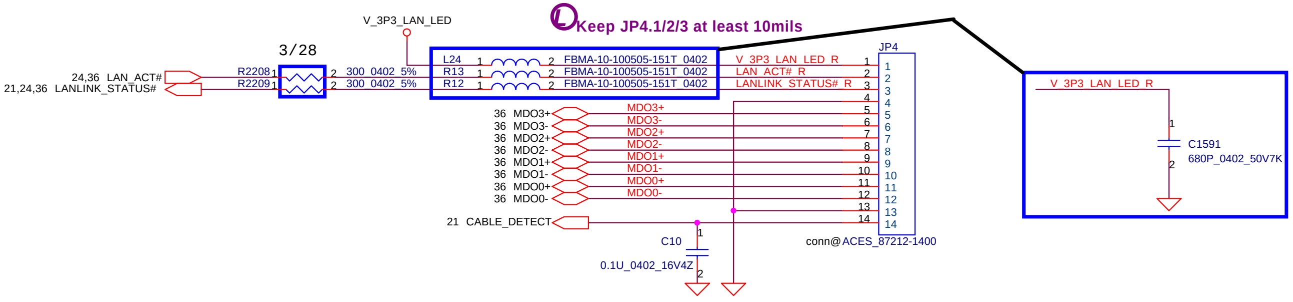
Layout Notice : Place termination as close as Intel 82566 as possible

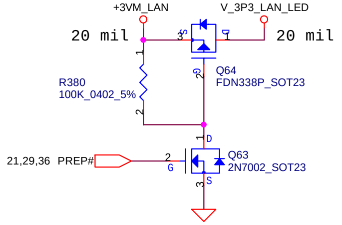


To RJ-45 CONN.

EMI request :
1. Add L24 and C1591.
2. Change R12~R13 to FBMA-10-100505-151T_0402.
3. Add R2208, R2209 to have current limit for E-star. 3/28

Keep JP4.1/2/3 at least 10mils





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Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title
Magnetic & RJ45/RJ11

Size Document Number *LA-3331P* Rev 1.0

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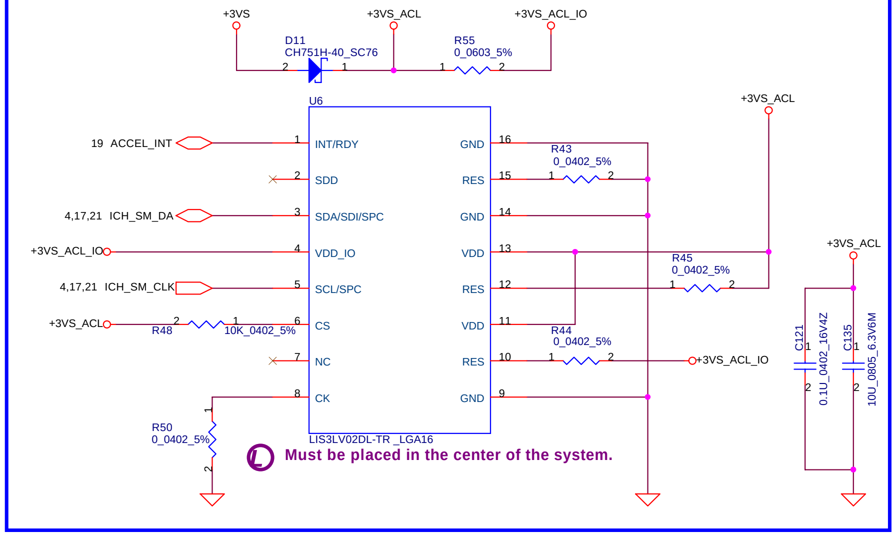
Modify in 9/6.

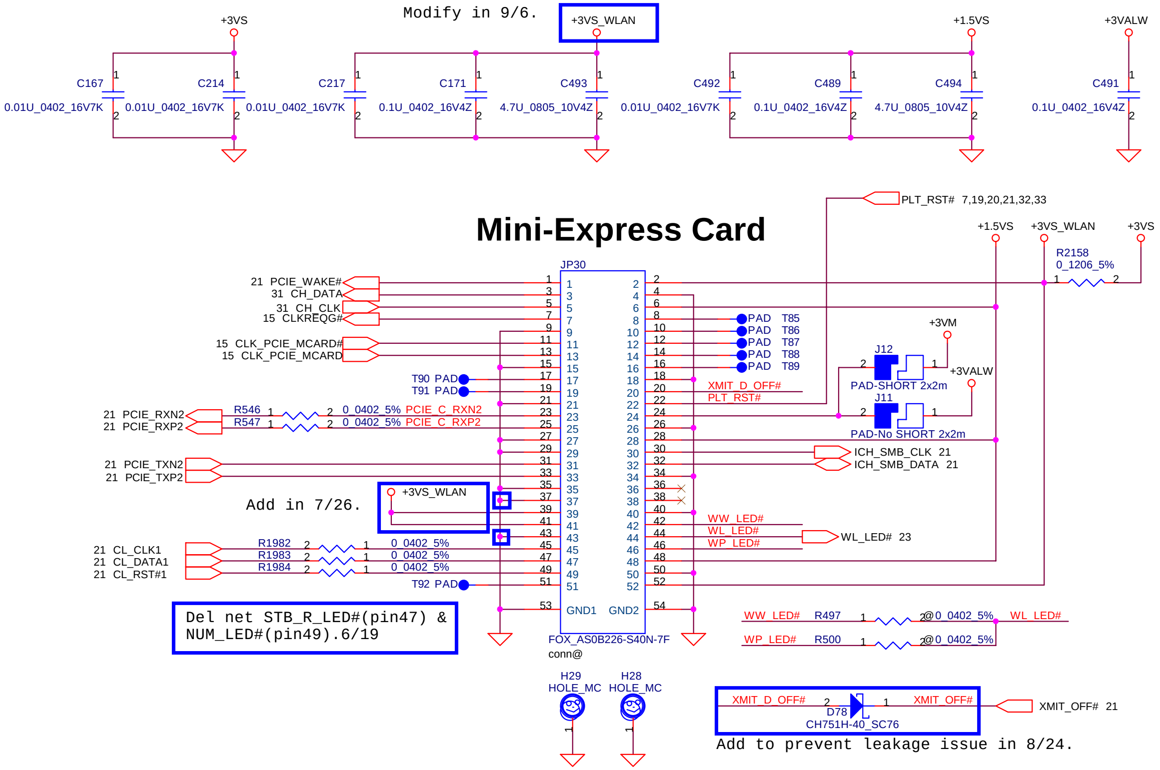
Change U6 to same as Chimay. 7/27

ACCELEROMETER



Must be placed in the center of the system.

Mini-Express Card



Add in 7/26.

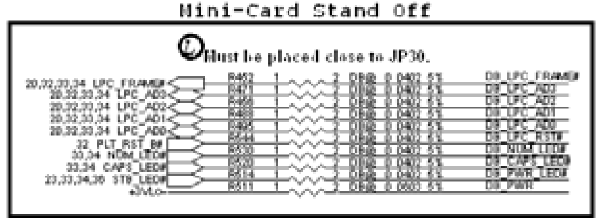
Del net STB_R_LED#(pin47) &
NUM_LED#(pin49).6/19

Add to prevent leakage issue in 8/24.

Chnage Design , Del R92 , R104 , R112 , Q17. 5/16

Del +3VL from JP30 pin 45. 6/15
Del net of JP30 pin 8, 10, 12, 14, 16, 17, 19, 51. 6/15

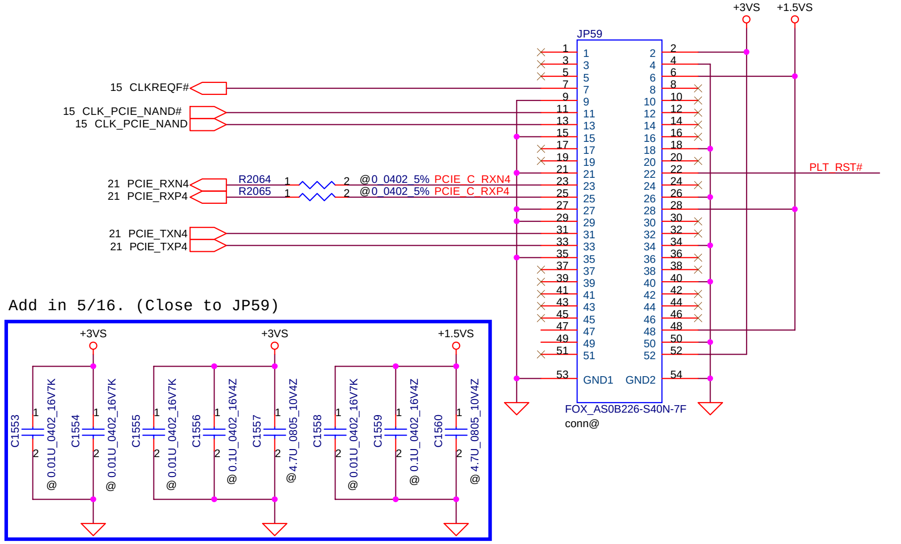
Del resistors & bypass all net as shown in below picture. 5/24



Add in 4/27.

NAND mini Card(Robson support)

Rerserve from PV build. 3/23



Add in 5/16. (Close to JP59)

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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title
Mini-Card/Mini-NAND/Accelerometer

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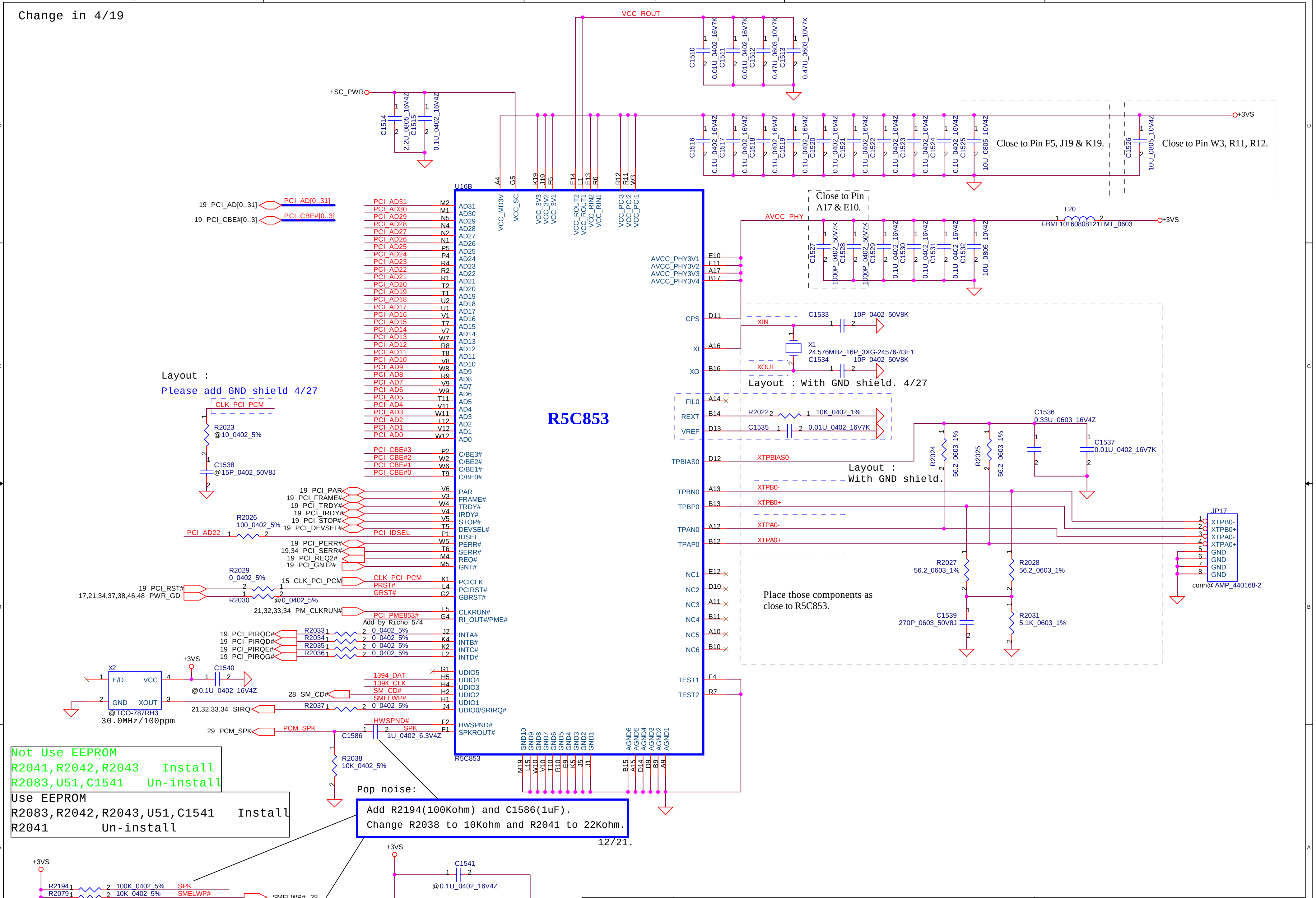
Change in 4/19



Not Use EEPROM
R2041,R2042,R2043 Install
R2083,U51,C1541 Un-install

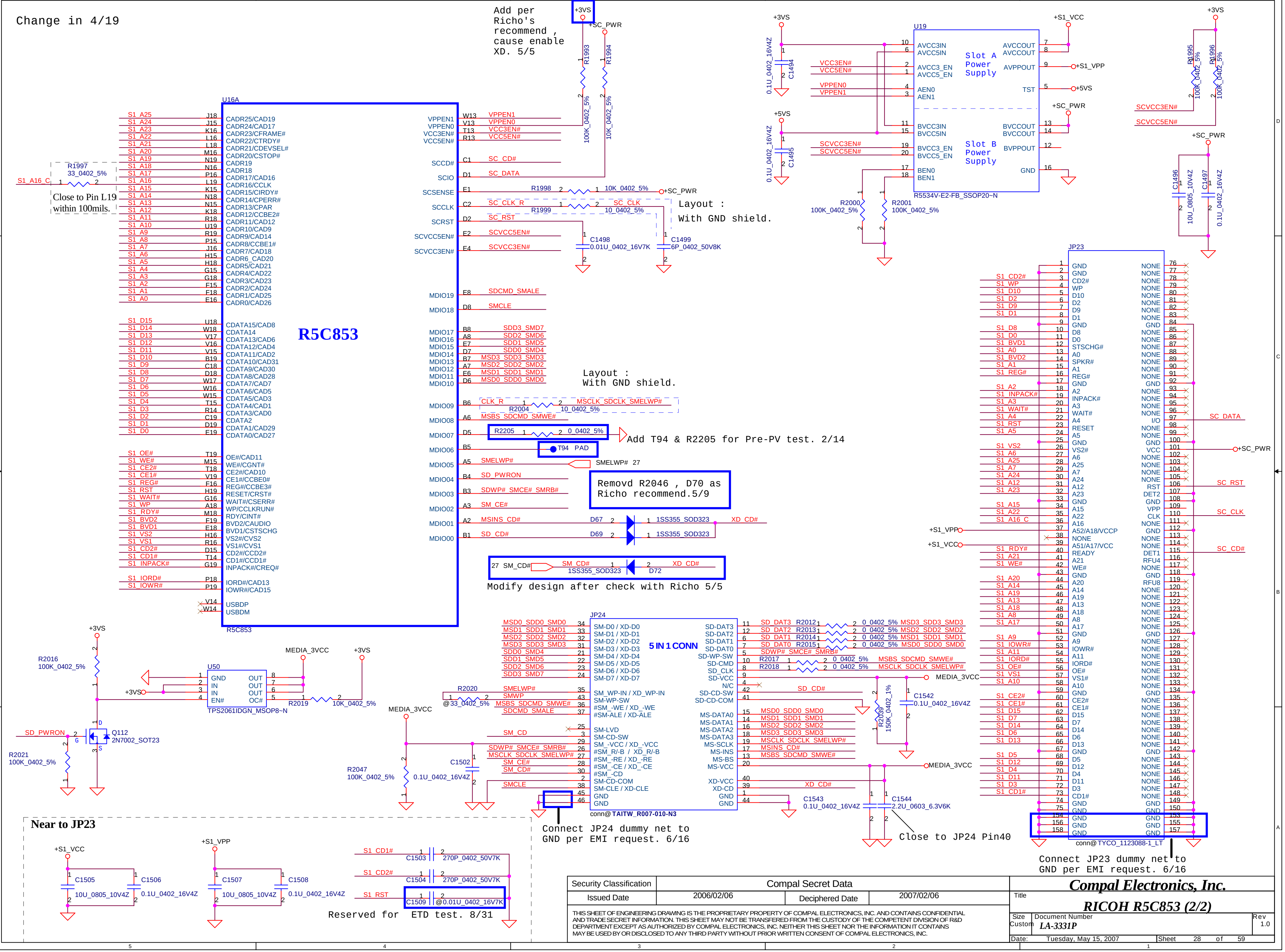
Use EEPROM
R2083,R2042,R2043,U51,C1541 Install
R2041 Un-install

Add R2194(100Kohm) and C1586(1uF).
Change R2038 to 10Kohm and R2041 to 22Kohm.

Security Classification	Compal Secret Data			**Compal Electronics, Inc.**
Issued Date	2006/02/06	Deciphered Date	2007/02/06	Title **RICOH R5C853 (1/2)**

Size Custom
Document Number LA-3331P
Rev 1.0
Date: Tuesday, May 15, 2007

Change in 4/19



Add per Richo's recommend , cause enable XD. 5/5

Layout : With GND shield.

Close to Pin L19 within 100mils.

Layout : With GND shield.

Add T94 & R2205 for Pre-PV test. 2/14

Removd R2046 , D70 as Richo recommend.5/9

Modify design after check with Richo 5/5

Connect JP24 dummy net to GND per EMI request. 6/16

Close to JP24 Pin40

Connect JP23 dummy net to GND per EMI request. 6/16

Near to JP23

Reserved for ETD test. 8/31

Security Classification	Compal Secret Data		
Issued Date	2006/02/06	Deciphered Date	2007/02/06

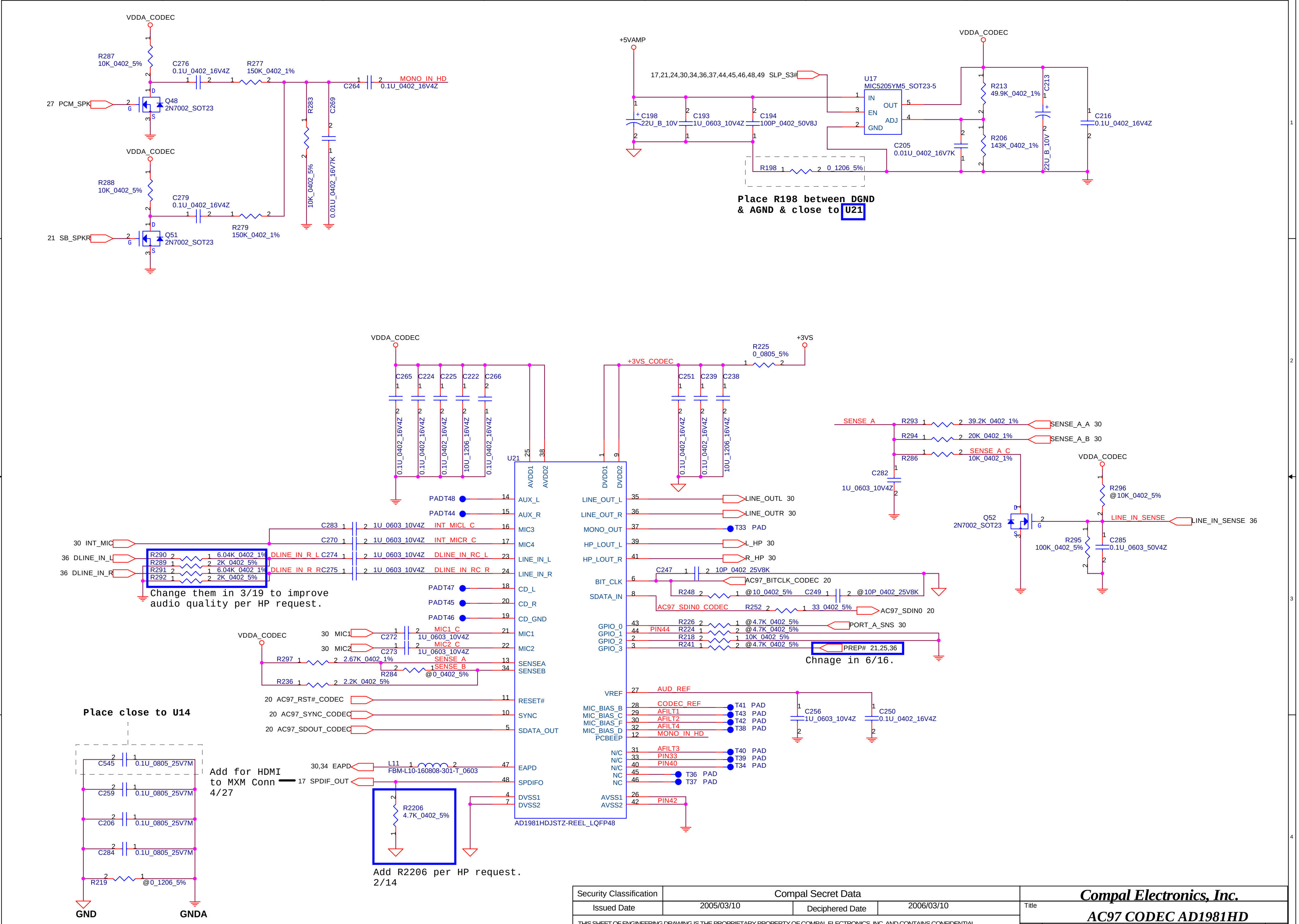
Compal Electronics, Inc.

Title

RICOH R5C853 (2/2)

Size Custom Document Number LA-3331P Rev 1.0

Date: Tuesday, May 15, 2007 Sheet 28 of 59



Place R198 between DGND & AGND & close to U21

Change them in 3/19 to improve audio quality per HP request.

Chnage in 6/16.

Place close to U14

Add for HDMI to MXM Conn 4/27

Add R2206 per HP request. 2/14

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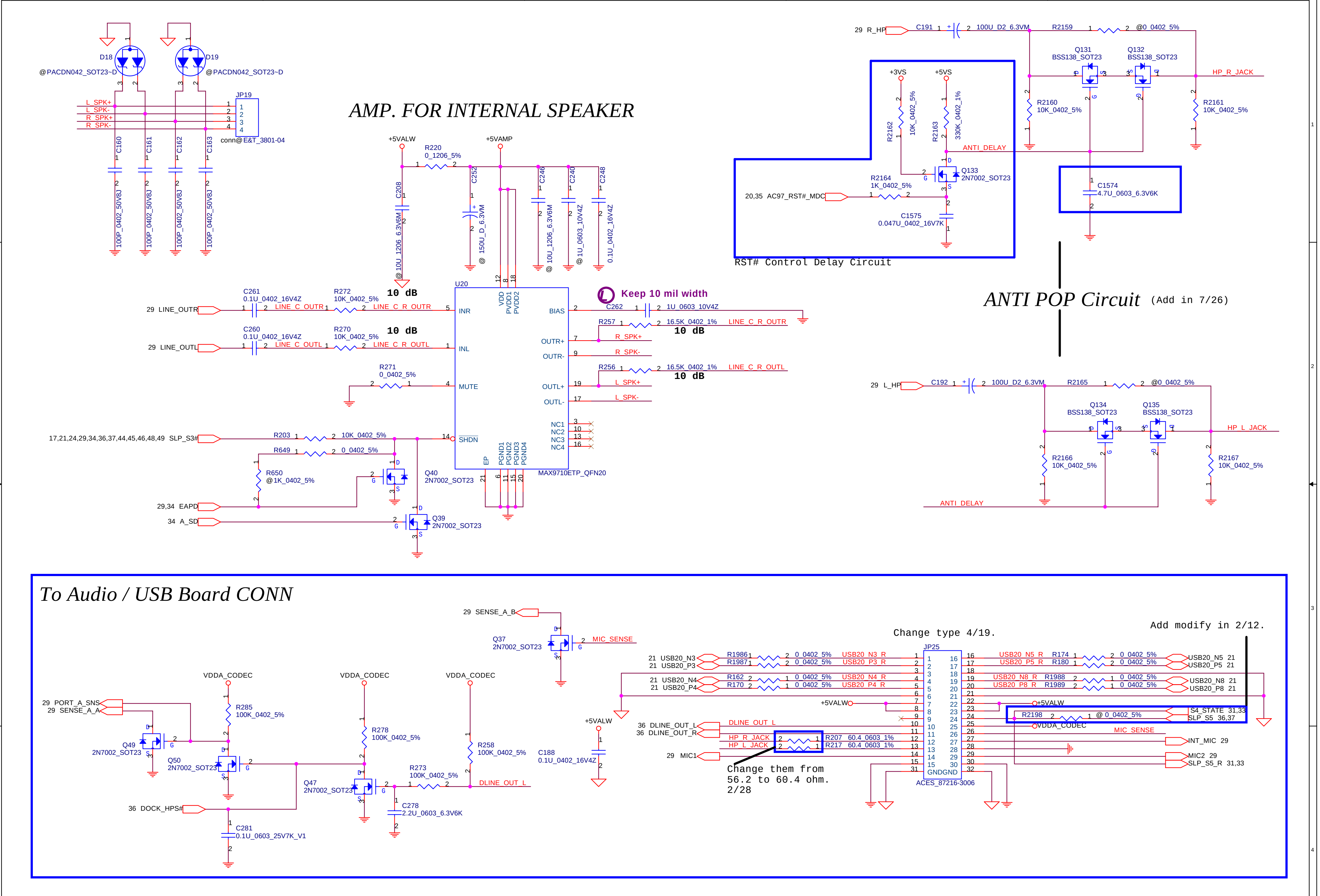
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title *AC97 CODEC AD1981HD*
				Size / Document Number: *LA-3331P* / Rev 1.0
				Date: Tuesday, May 15, 2007 / Sheet 29 of 59



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title AMP & Audio Jack

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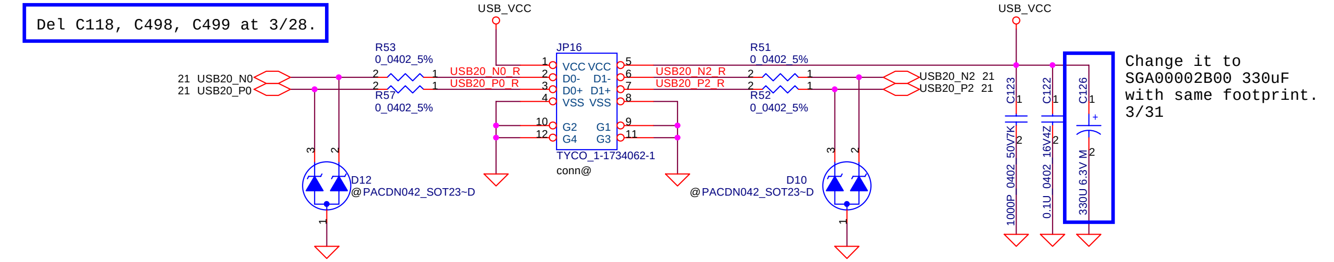
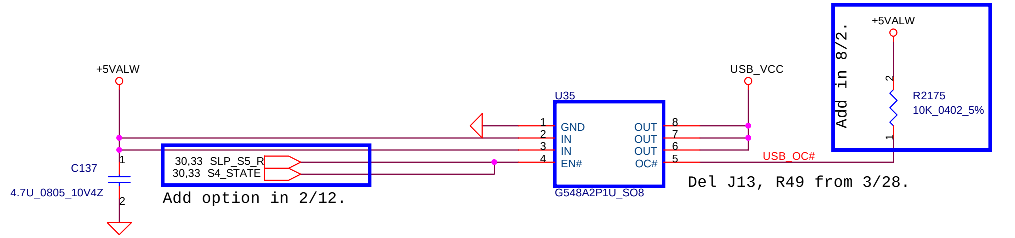
USB CONNECTOR 1



Del C118, C498, C499 at 3/28.

Change it to
SGA00002B00 330uF
with same footprint.
3/31

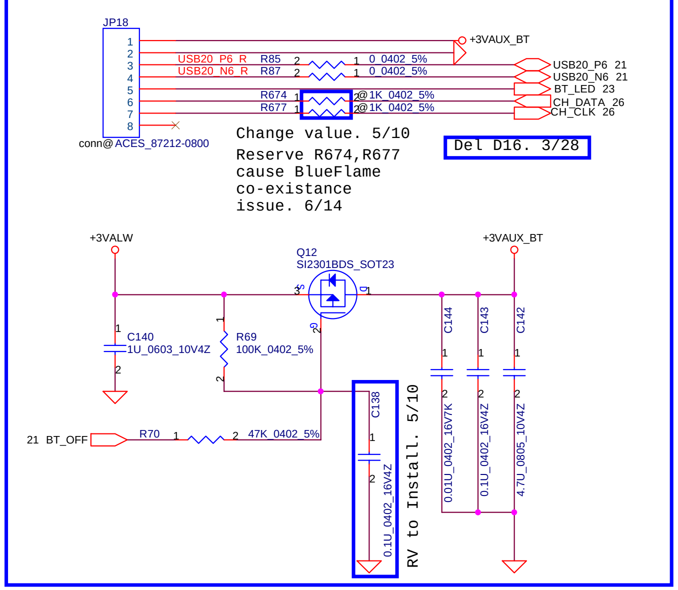
(2A,100mils ,Via NO.=4)



Add option in 2/12.

Del J13, R49 from 3/28.

BT Connector



Change value. 5/10

Reserve R674,R677
cause BlueFlame
co-existance
issue. 6/14

Del D16. 3/28

RV to Install. 5/10

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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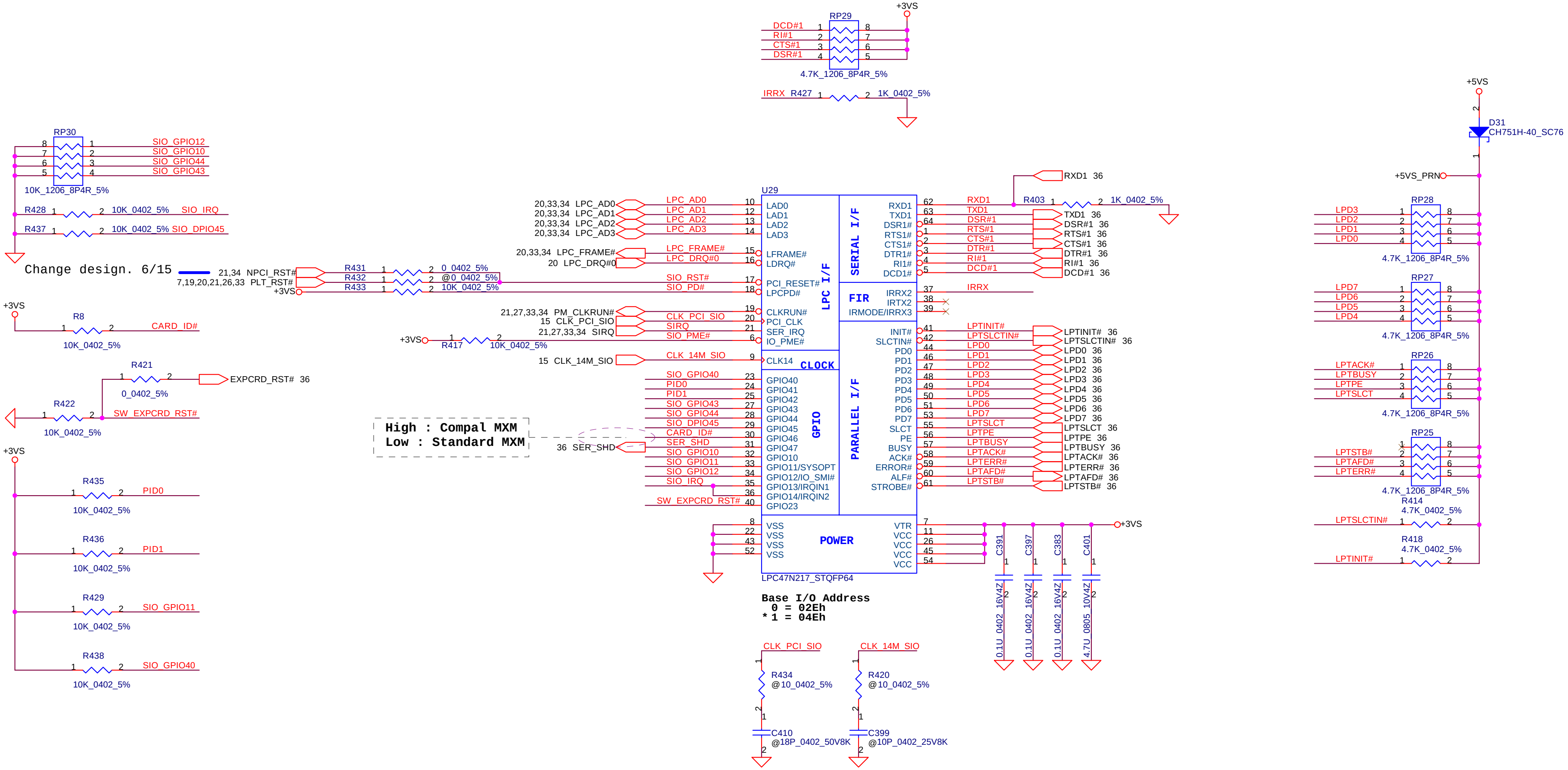
Compal Electronics, Inc.

Title
USB I/O & BT Connector

Size | Document Number ***LA-3331P*** | Rev 1.0

Date: Tuesday, May 15, 2007 | Sheet 31 of 59



Change design. 6/15

High : Compal MXM
Low : Standard MXM

Base I/O Address
0 = 02Eh
***1 = 04Eh**

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

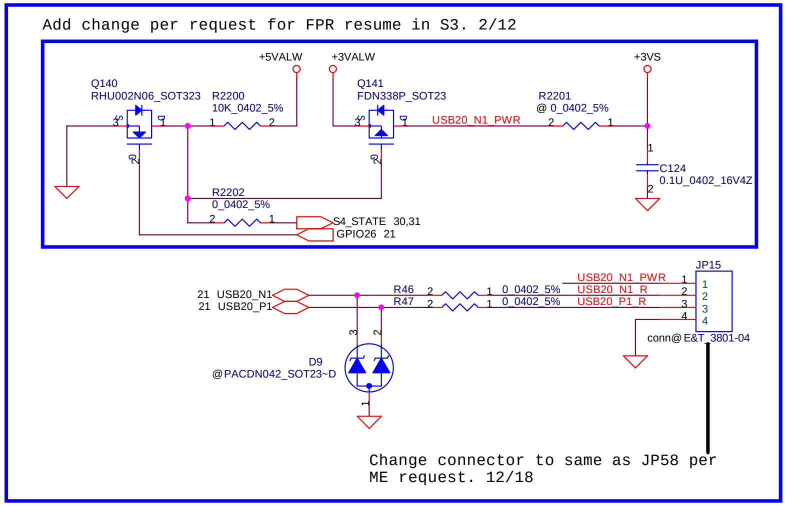
Title
SUPER I/O LPC47N217

Size	Document Number	Rev
	LA-3331P	1.0

Date: Tuesday, May 15, 2007 Sheet 32 of 59

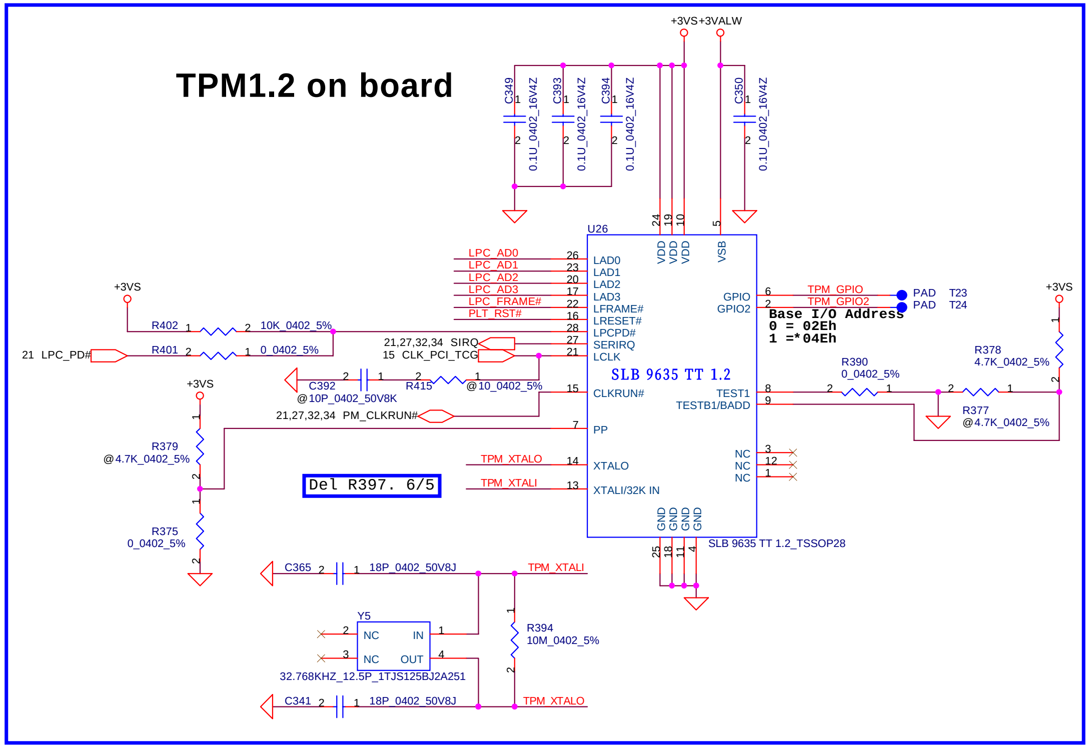
Finger printer

Add change per request for FPR resume in S3. 2/12



Change connector to same as JP58 per ME request. 12/18

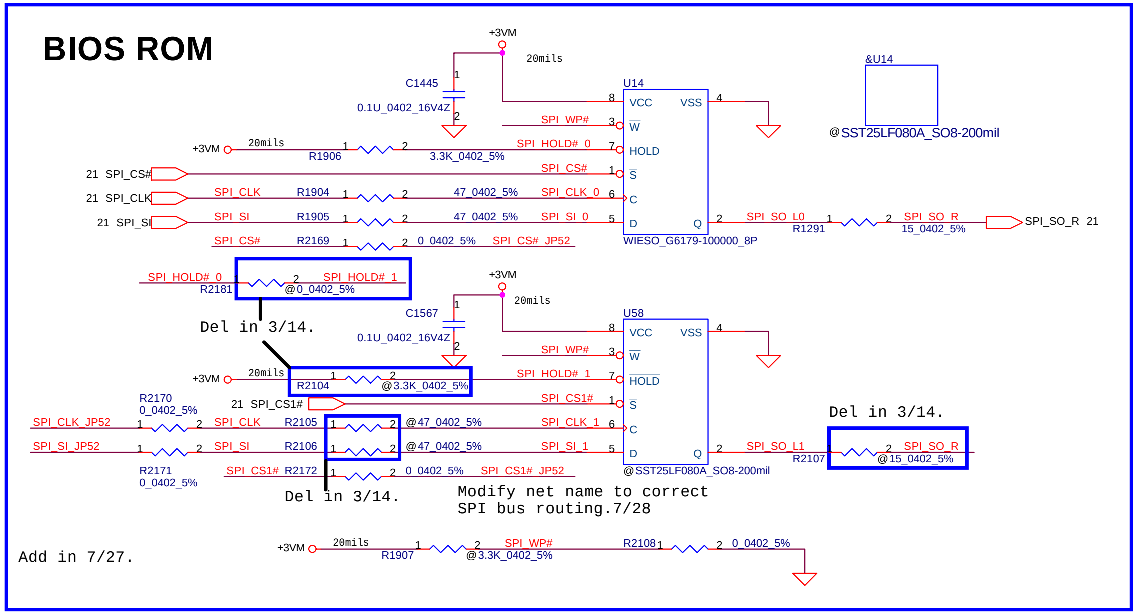
TPM1.2 on board



Del R397. 6/5

Change SPI ROM to 8Mbit(SA00001JX00) from SI2.

BIOS ROM



Del in 3/14.

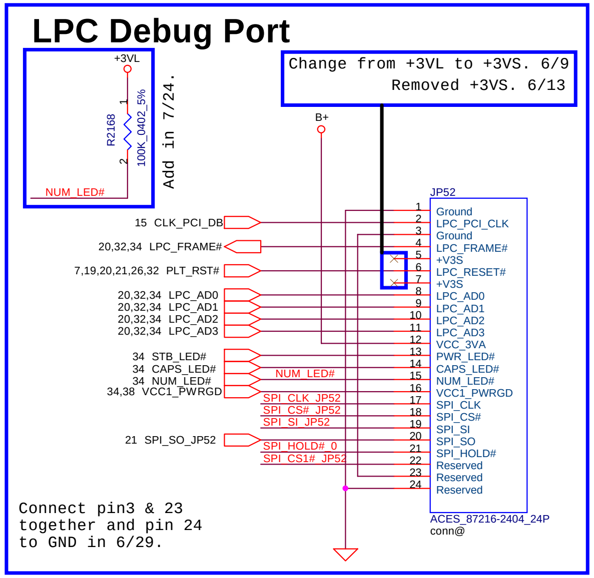
Del in 3/14.

Del in 3/14.

Modify net name to correct SPI bus routing.7/28

Add in 7/27.

LPC Debug Port



Add in 7/24.

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13

Connect pin3 & 23 together and pin 24 to GND in 6/29.

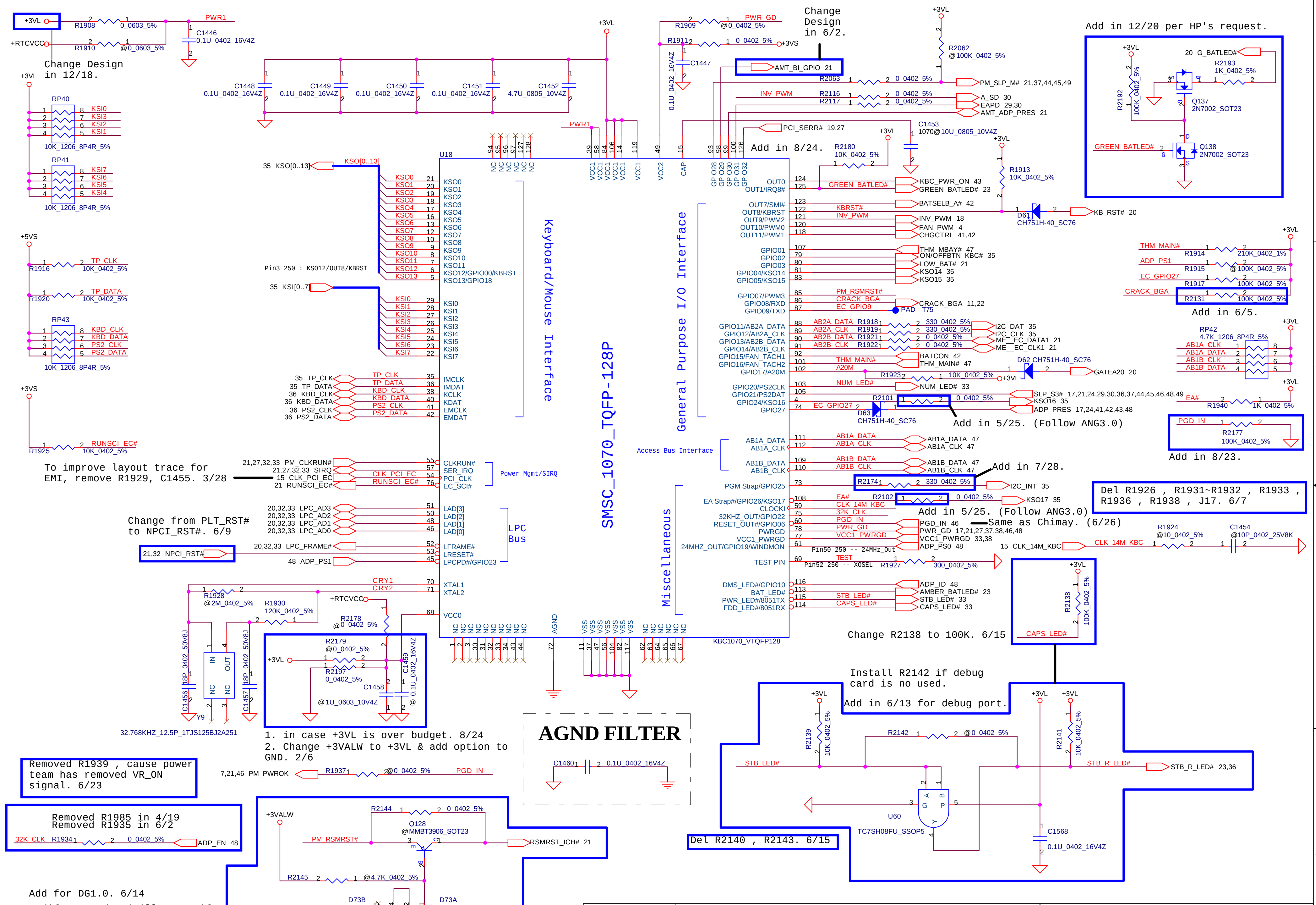
Security Classification	Compal Secret Data			
Issued Date	2005/03/10	Deciphered Date	2006/03/10	

Compal Electronics, Inc.

Title
TCG/BIOS ROM/PS2/SW LPC DEBUG

Size Document Number
LA-3331P
Rev 1.0

Date: Tuesday, May 15, 2007 Sheet 33 of 59



Change Design in 12/18.

Change Design in 6/2.

Add in 12/20 per HP's request.

Add in 8/24.

Add in 6/5.

Add in 5/25. (Follow ANG3.0)

Add in 8/23.

Add in 7/28.

Del R1926 , R1931~R1932 , R1933 , R1936 , R1938 , J17. 6/7

Add in 5/25. (Follow ANG3.0)

Same as Chimay. (6/26)

To improve layout trace for EMI, remove R1929, C1455. 3/28

Change from PLT_RST# to NPCI_RST#. 6/9

Change R2138 to 100K. 6/15

Install R2142 if debug card is no used.

Add in 6/13 for debug port.

1. in case +3VL is over budget. 8/24
2. Change +3VALW to +3VL & add option to GND. 2/6

Removed R1939 , cause power team has removed VR_ON signal. 6/23

Removed R1985 in 4/19
Removed R1935 in 6/2

Del R2140 , R2143. 6/15

Add for DG1.0. 6/14

Modify at 10/27.(will mount if timing issue)
Modify to meet DG1.1.10/30

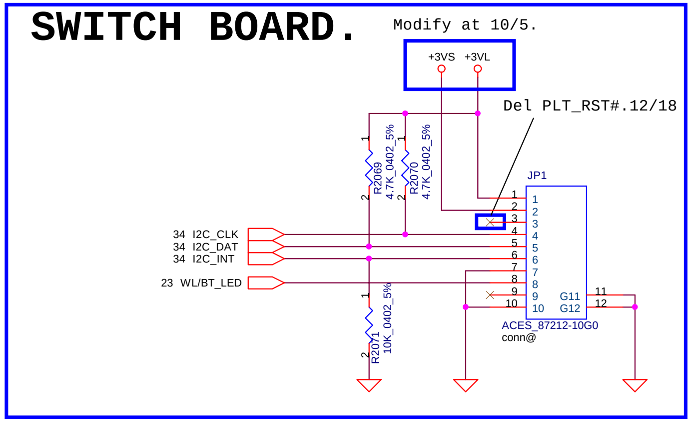
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

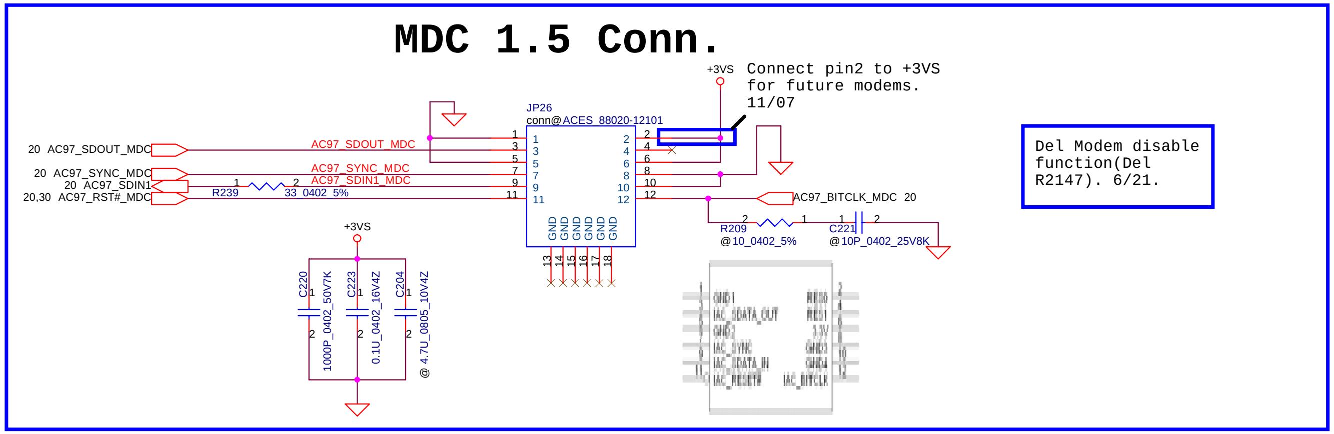
Title
LPC47N1021

Size | Document Number ***LA-3331P*** | Rev 1.0

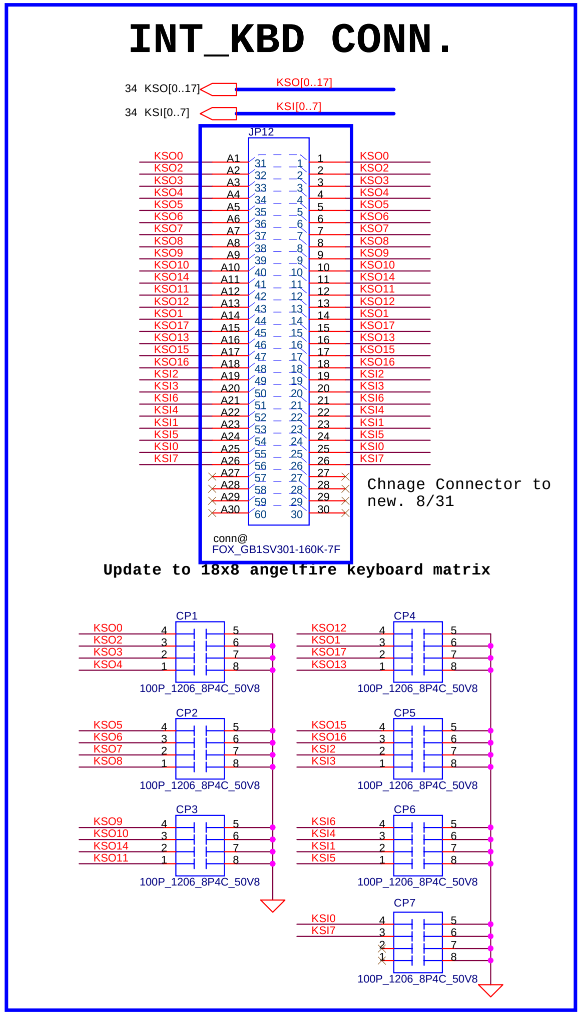
SWITCH BOARD.



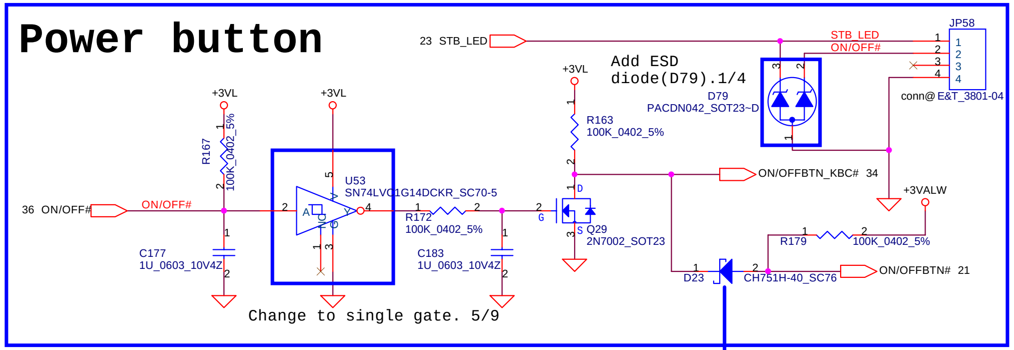
MDC 1.5 Conn.



INT_KBD CONN.

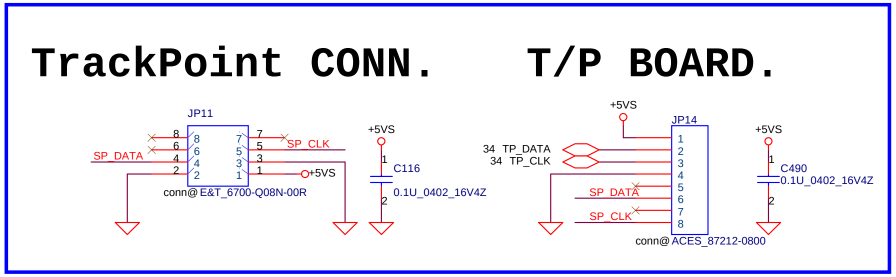


Power button



Change SC1B751V005 to SC1H751H010 to unified spec. 3/26

TrackPoint CONN. T/P BOARD.



Security Classification | Compal Secret Data

Issued Date 2005/03/10 | Deciphered Date 2006/03/10

Compal Electronics, Inc.

Title ***MDC/KBD/ON_OFF/LID***

Size | Document Number *LA-3331P* | Rev 1.0

Date: Tuesday, May 15, 2007 | Sheet 35 of 59

DOCK CONN. 184PIN

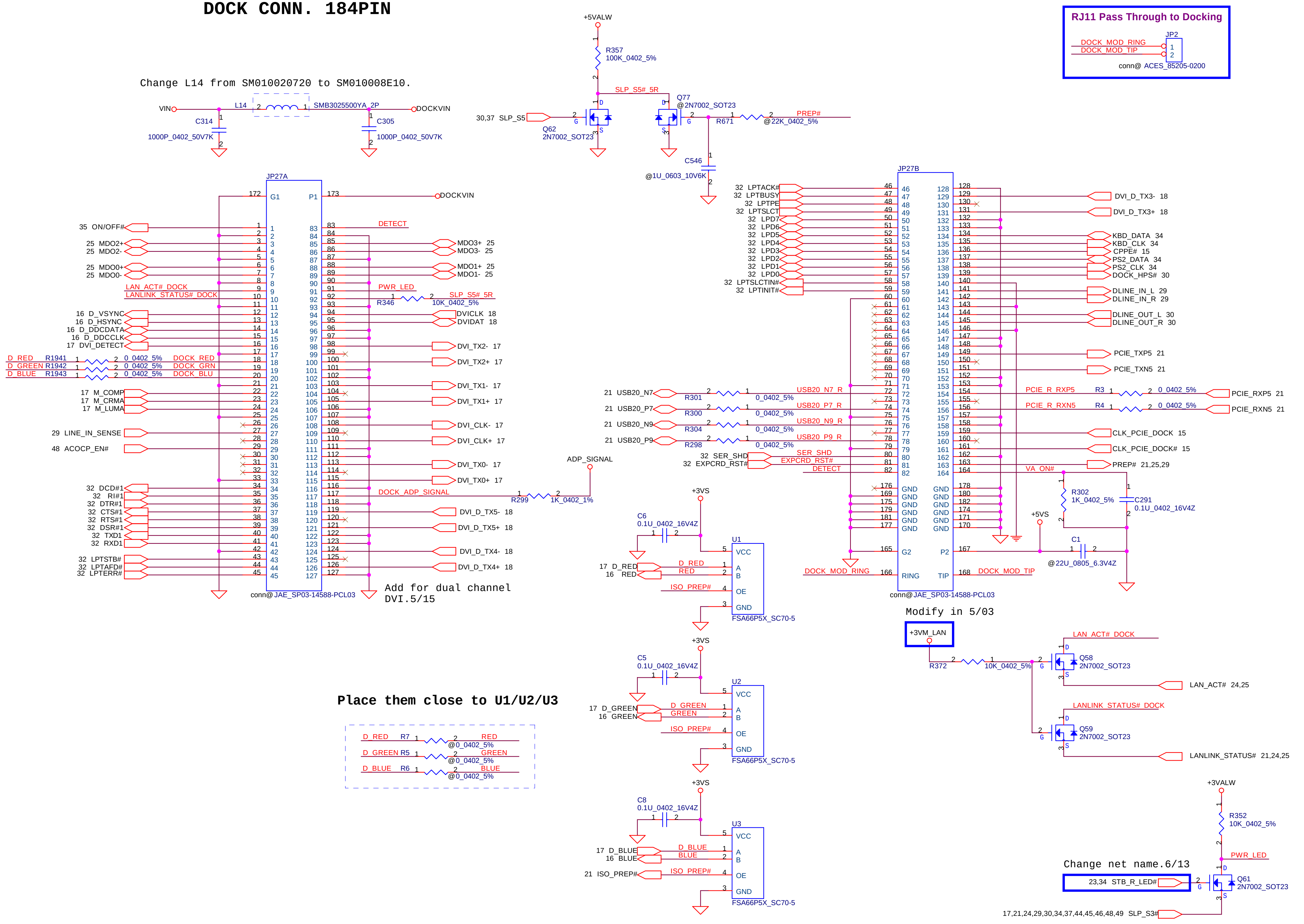
Change L14 from SM010020720 to SM010008E10.

Add for dual channel DVI.5/15

Place them close to U1/U2/U3

Modify in 5/03

Change net name.6/13



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

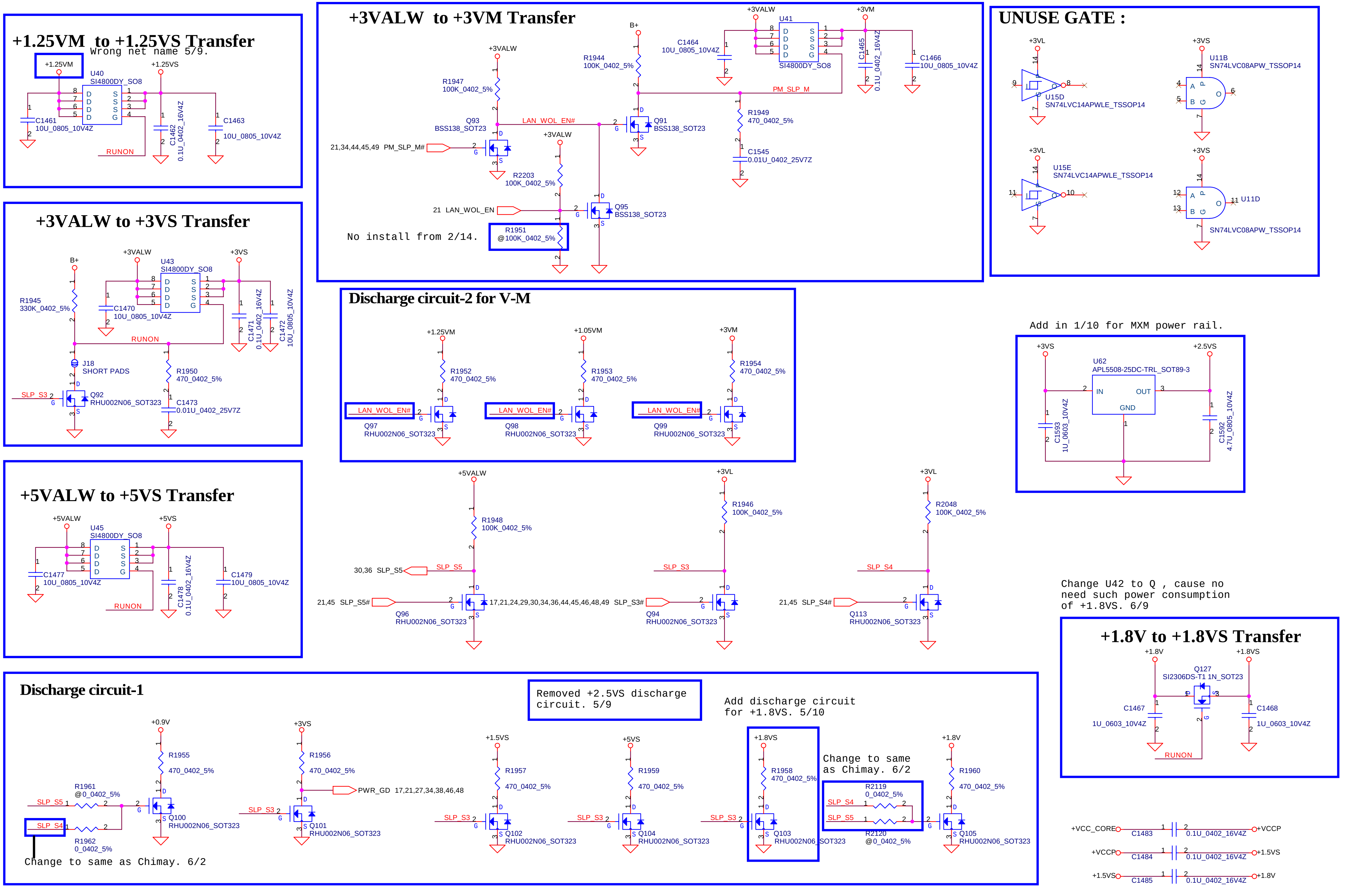
Compal Electronics, Inc.

Title

Docking CONN.

Size Document Number LA-3331P Rev 1.0

Date: Tuesday, May 15, 2007 Sheet 36 of 59



+1.25VM to +1.25VS Transfer

Wrong net name 5/9.

+3VALW to +3VM Transfer

No install from 2/14.

UNUSE GATE :

+3VALW to +3VS Transfer

Discharge circuit-2 for V-M

Add in 1/10 for MXM power rail.

+5VALW to +5VS Transfer

Change U42 to Q , cause no need such power consumption of +1.8VS. 6/9

+1.8V to +1.8VS Transfer

Discharge circuit-1

Removed +2.5VS discharge circuit. 5/9

Add discharge circuit for +1.8VS. 5/10

Change to same as Chimay. 6/2

Change to same as Chimay. 6/2

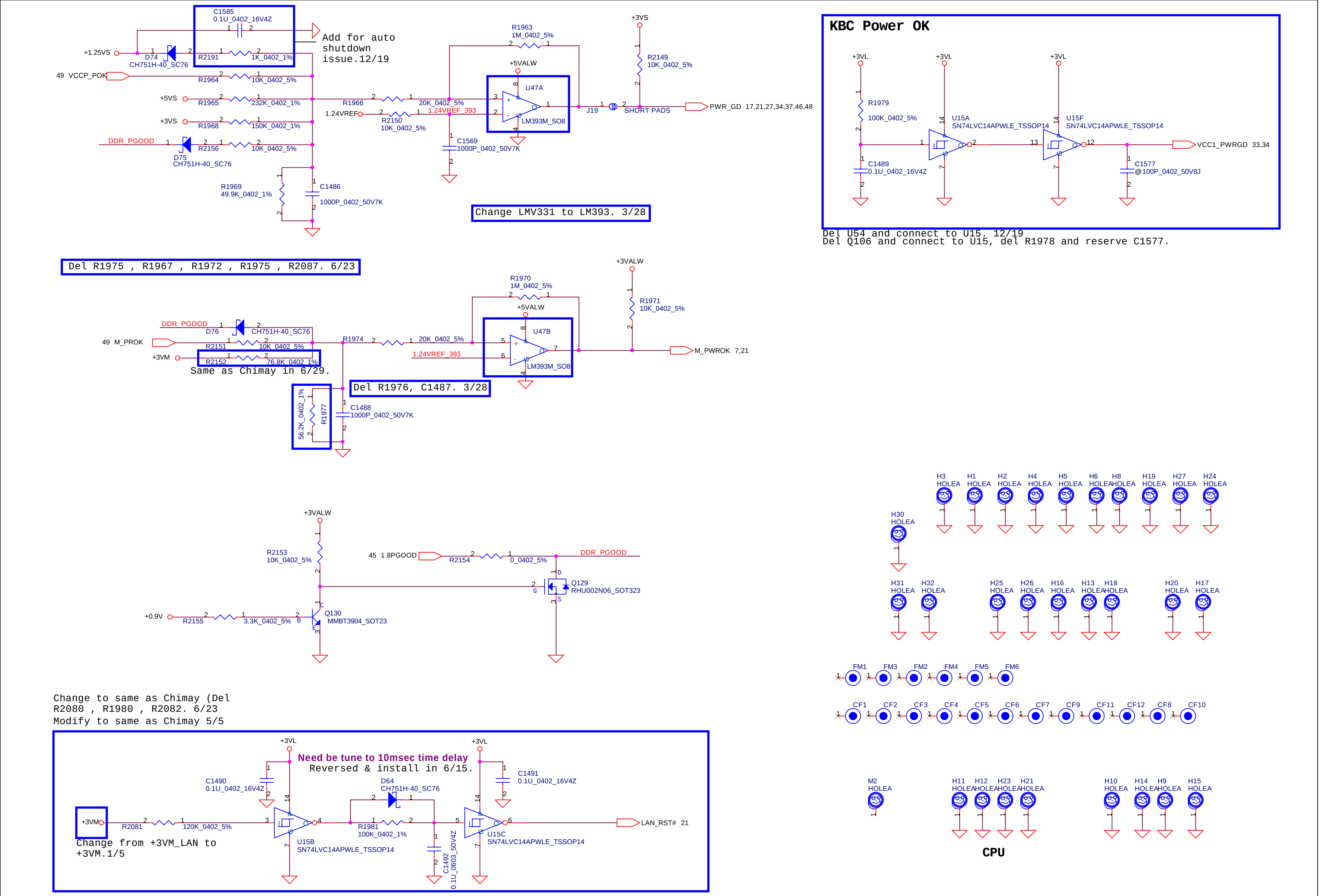
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title
DC/DC Circuits

Size
Document Number
LA-3331P
Rev
1.0

Date: Tuesday, May 15, 2007
Sheet 37 of 59



Add for auto shutdown issue.12/19

Change LMV331 to LM393. 3/28

KBC Power OK

Del U54 and connect to U15. 12/19
Del Q106 and connect to U15, del R1978 and reserve C1577.

Del R1975 , R1967 , R1972 , R1975 , R2087. 6/23

Same as Chimay in 6/29.

Del R1976, C1487. 3/28

Change to same as Chimay (Del
R2080 , R1980 , R2082. 6/23
Modify to same as Chimay 5/5

Need be tune to 10msec time delay
Reversed & install in 6/15.

Change from +3VM_LAN to
+3VM.1/5

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

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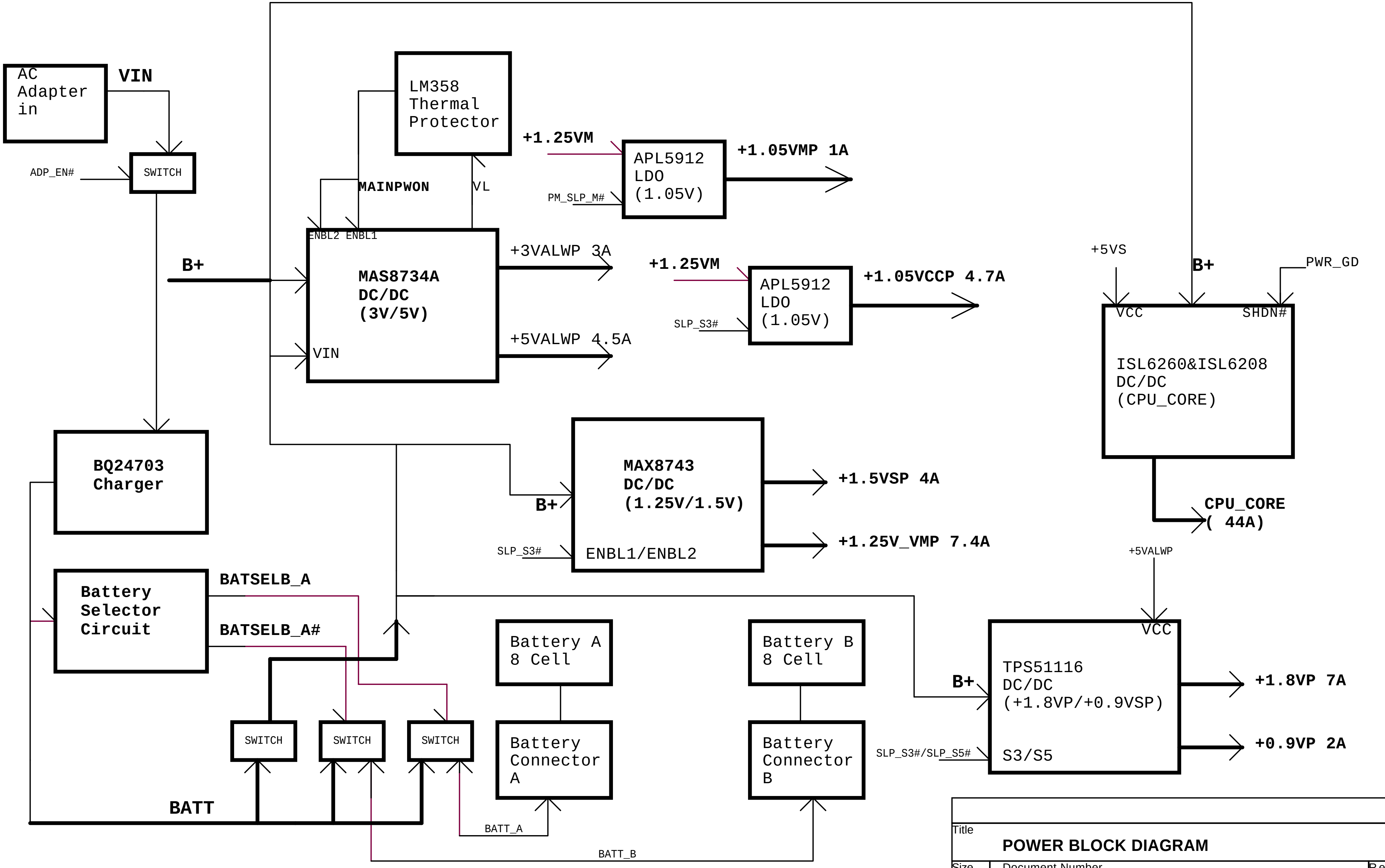
Compal Electronics, Inc.

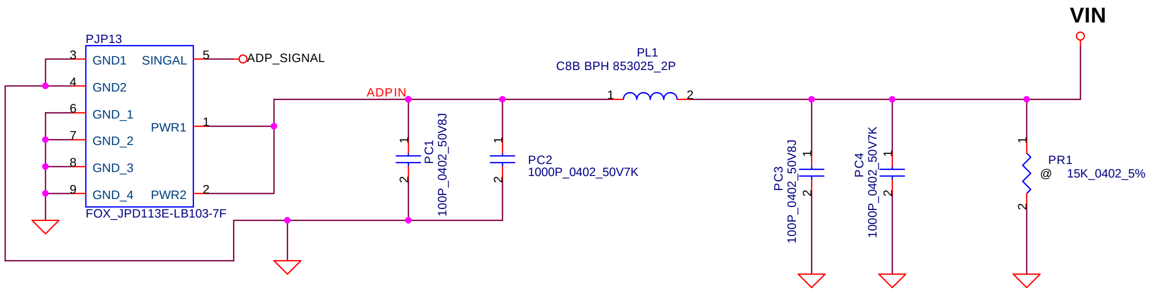
Title
POK CKT

Size
Document Number
LA-3331P
Rev
1.0

Date: Tuesday, May 15, 2007 Sheet 38 of 59



Title	POWER BLOCK DIAGRAM	
Size	Document Number	Rev
Date: Tuesday, May 15, 2007	Sheet 39 of 59	



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

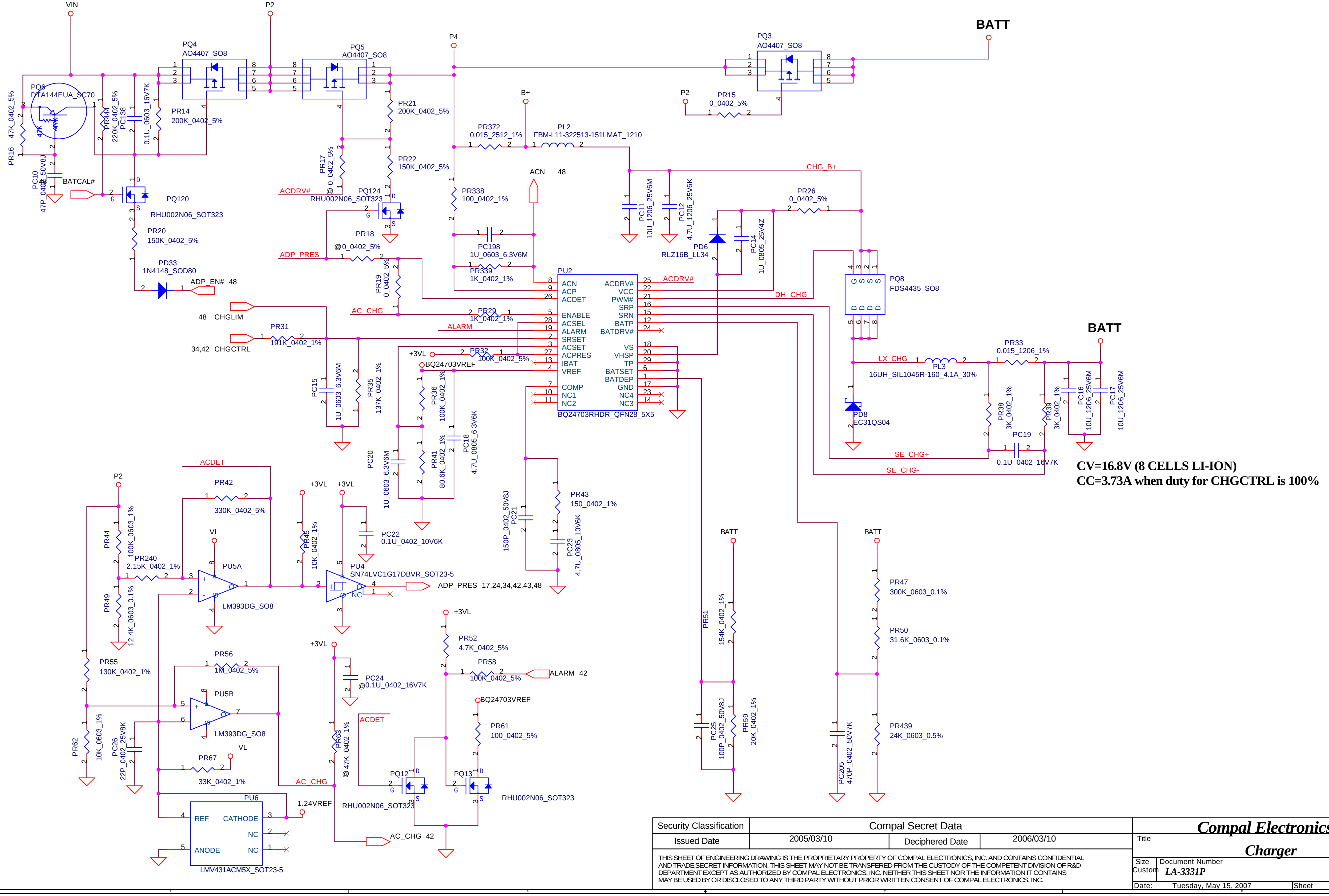
Compal Electronics, Inc.

Title

DCIN

Size
Custom
Document Number
LA-3331P
Rev

Date: Tuesday, May 15, 2007
Sheet 40 of 59



CV=16.8V (8 CELLS LI-ION)
CC=3.73A when duty for CHGCTRL is 100%

Security Classification	Compal Secret Data			**Compal Electronics, Inc.**
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title **Charger**

Size Custom
Document Number *LA-3331P*
Rev
Date: Tuesday, May 15, 2007
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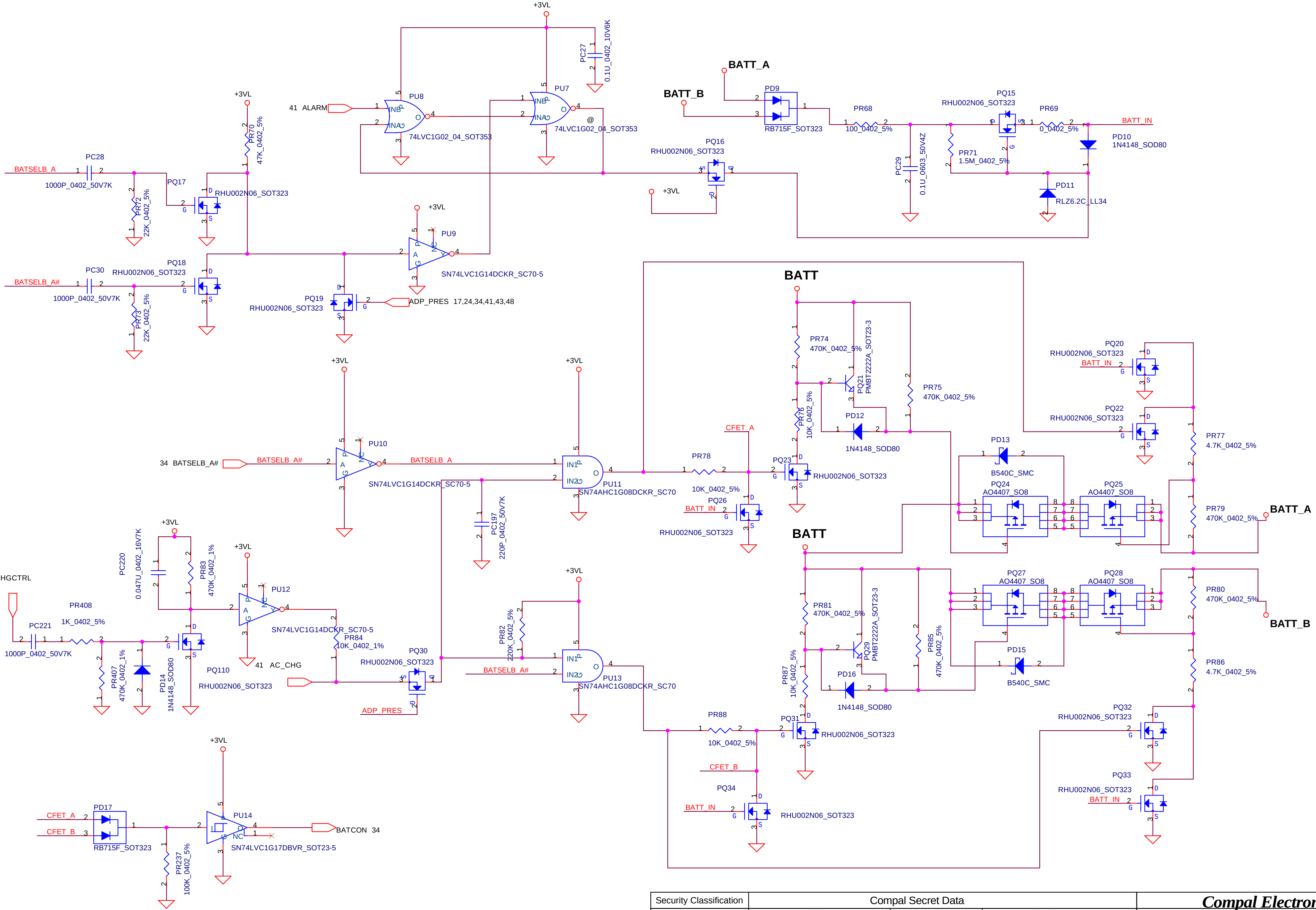

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title

Battery selector

Size Custom
Document Number *LA-3331P*
Rev

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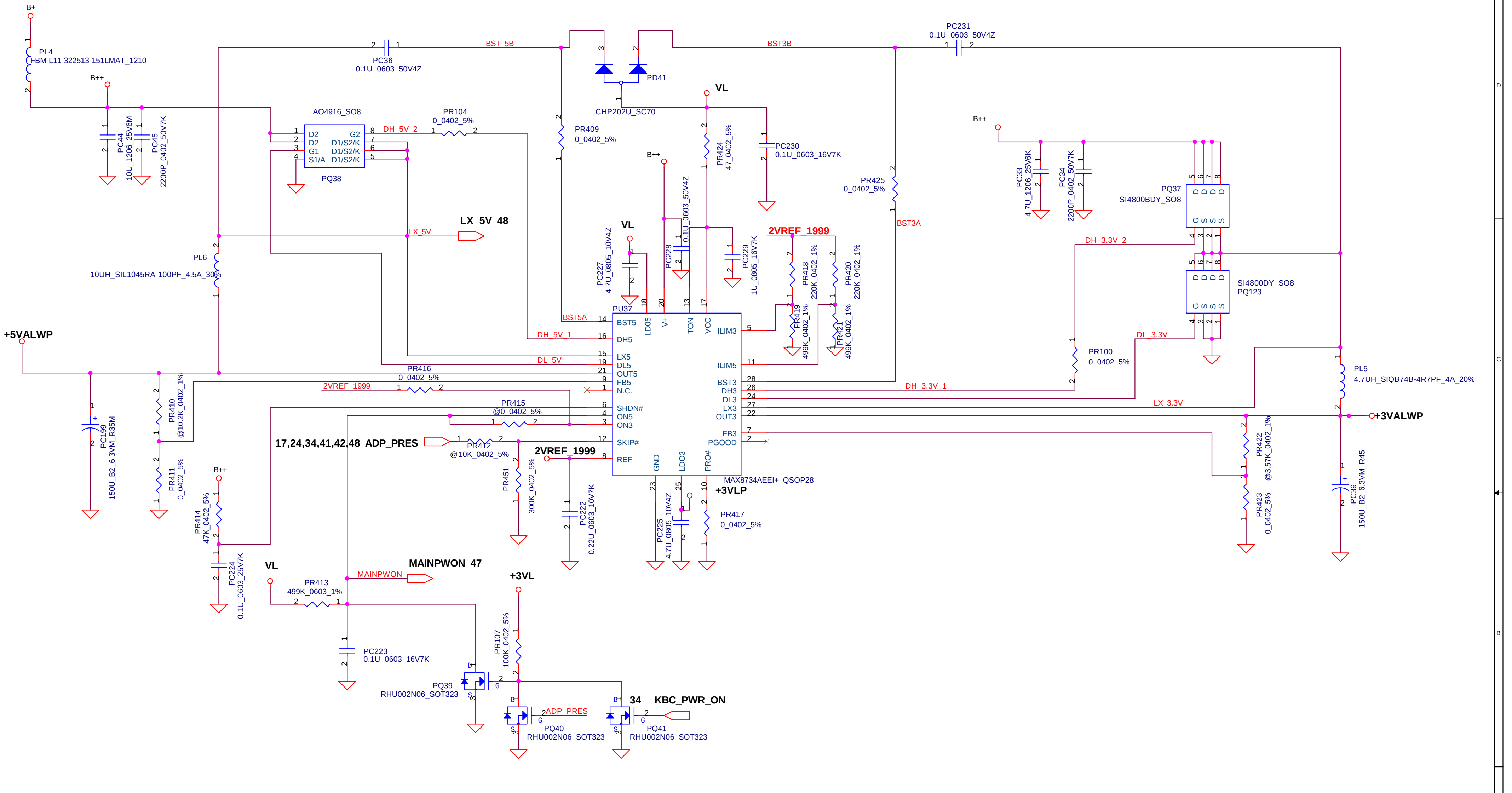
Sheet 42 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
3.3VALW/5VALW

Size Custom
Document Number LA-3331P
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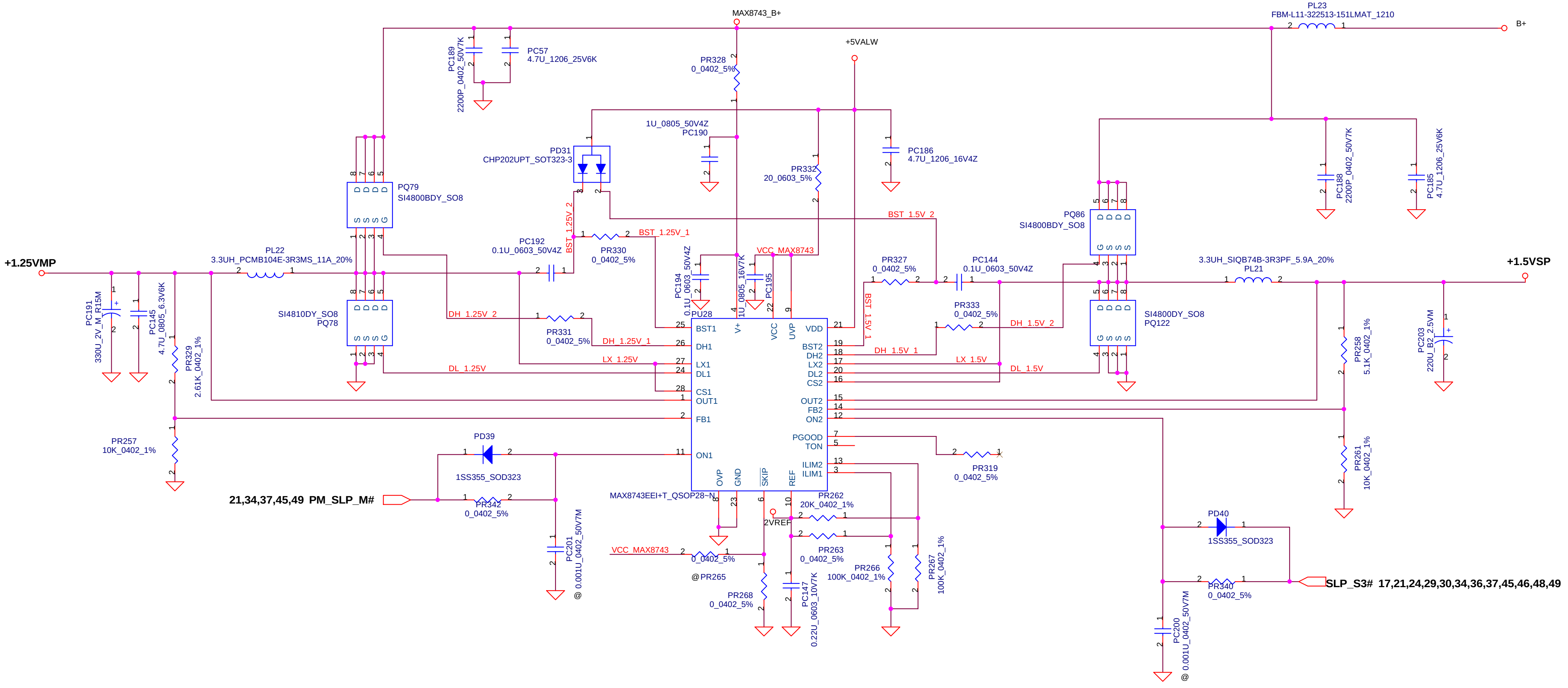
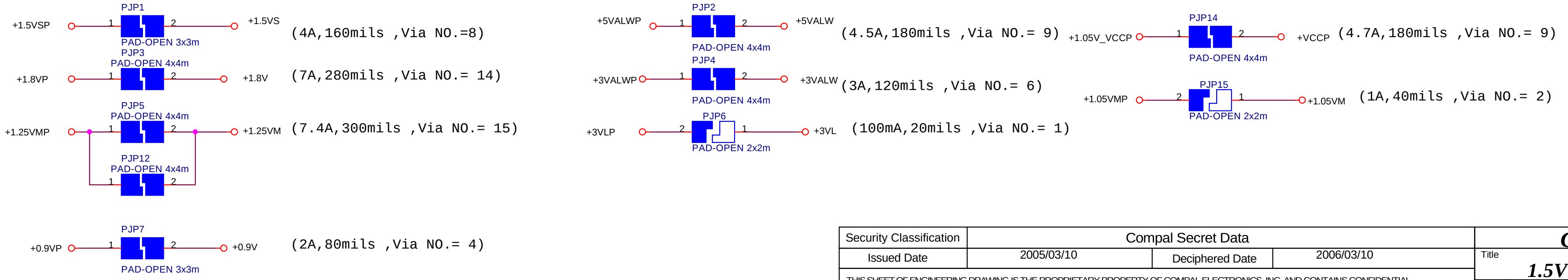


1.5VSP/ +1.25VMP



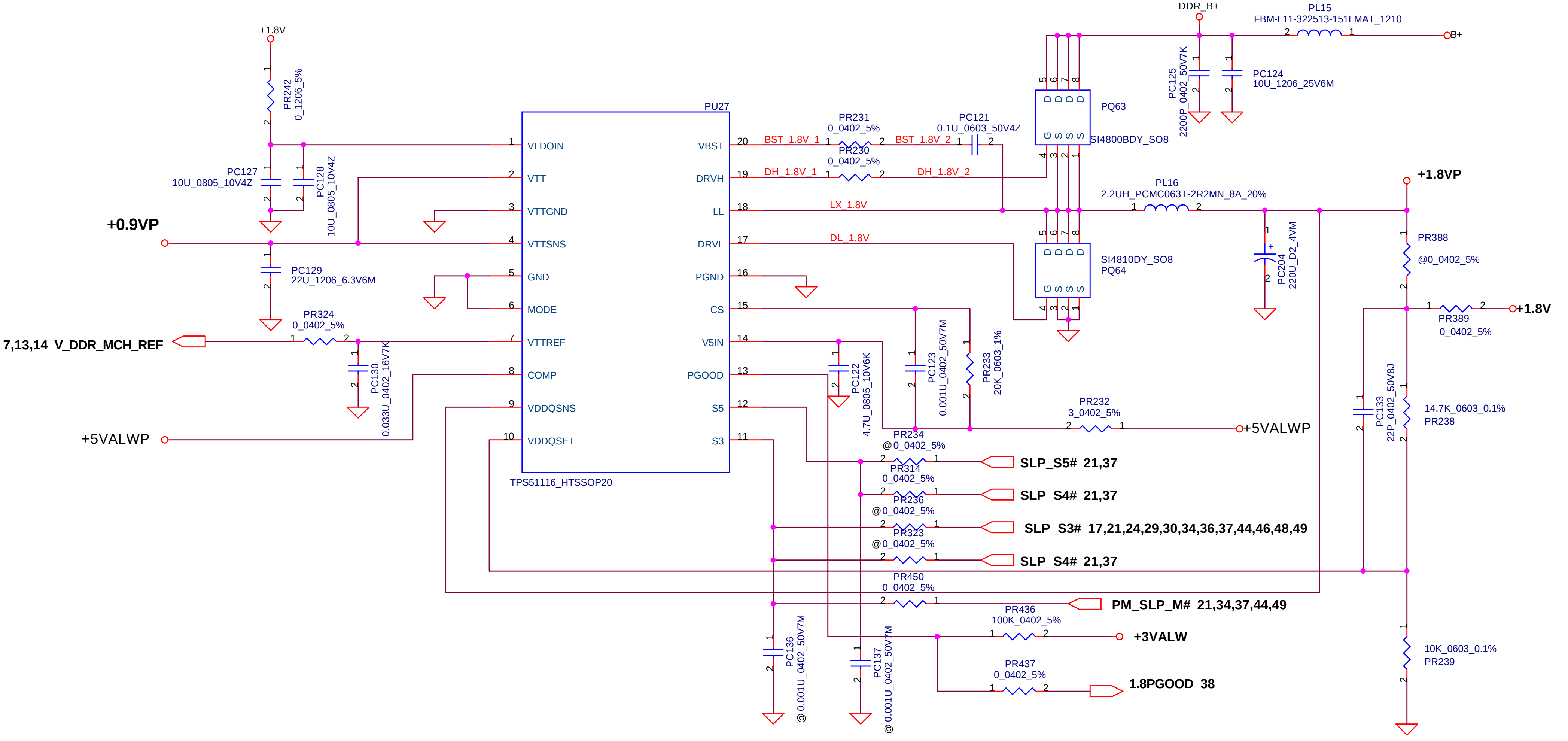
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
1.5VS/1.25VMP

Size Custom
Document Number LA-3331P
Rev

Date: Tuesday, May 15, 2007



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title 1.8V/0.9VS

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Size	Document Number	Rev
B	LA-3331P	

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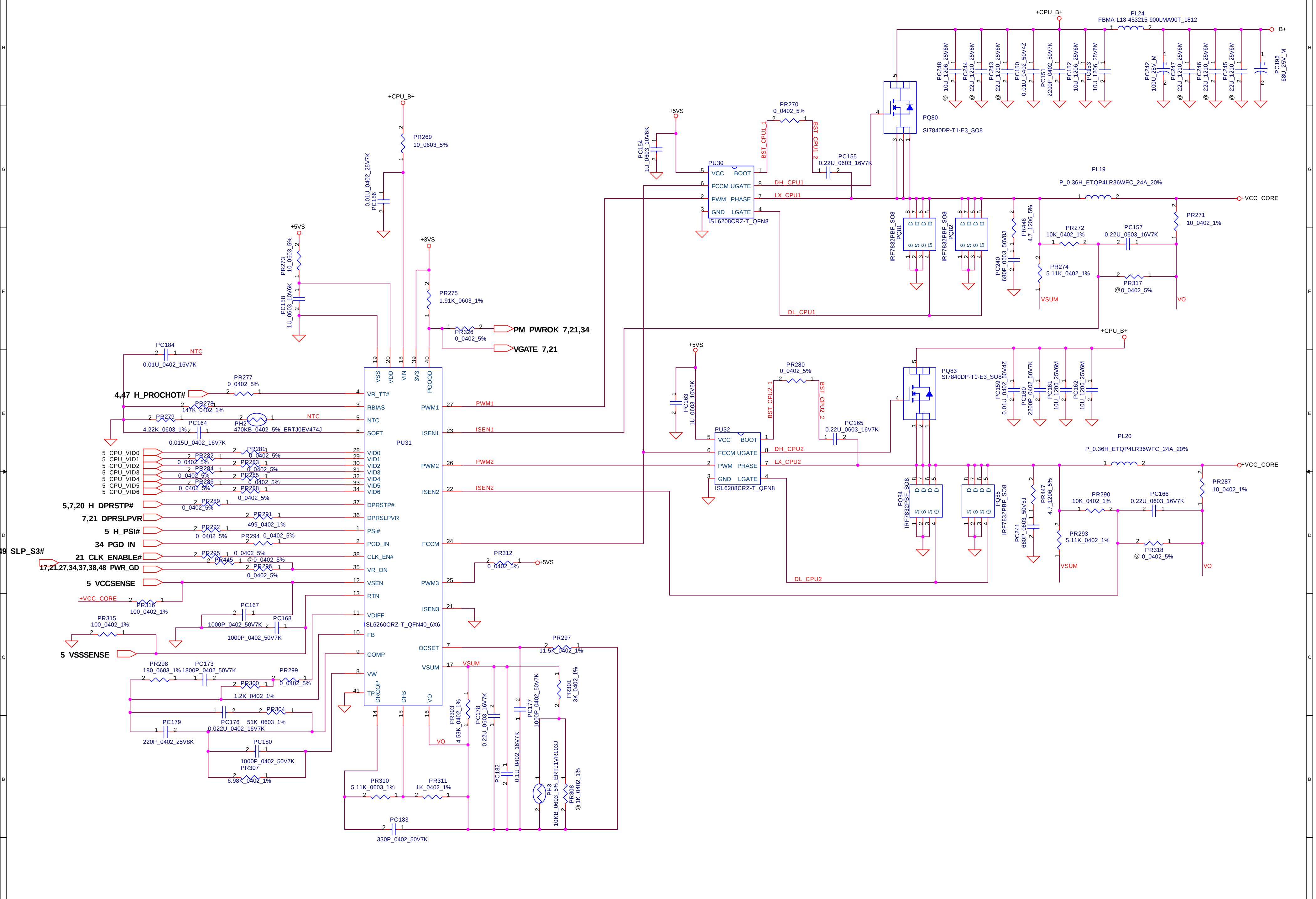

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title

CPU_CORE

Size C

Document Number **LA-3331P**

Rev

Date: Tuesday, May 15, 2007

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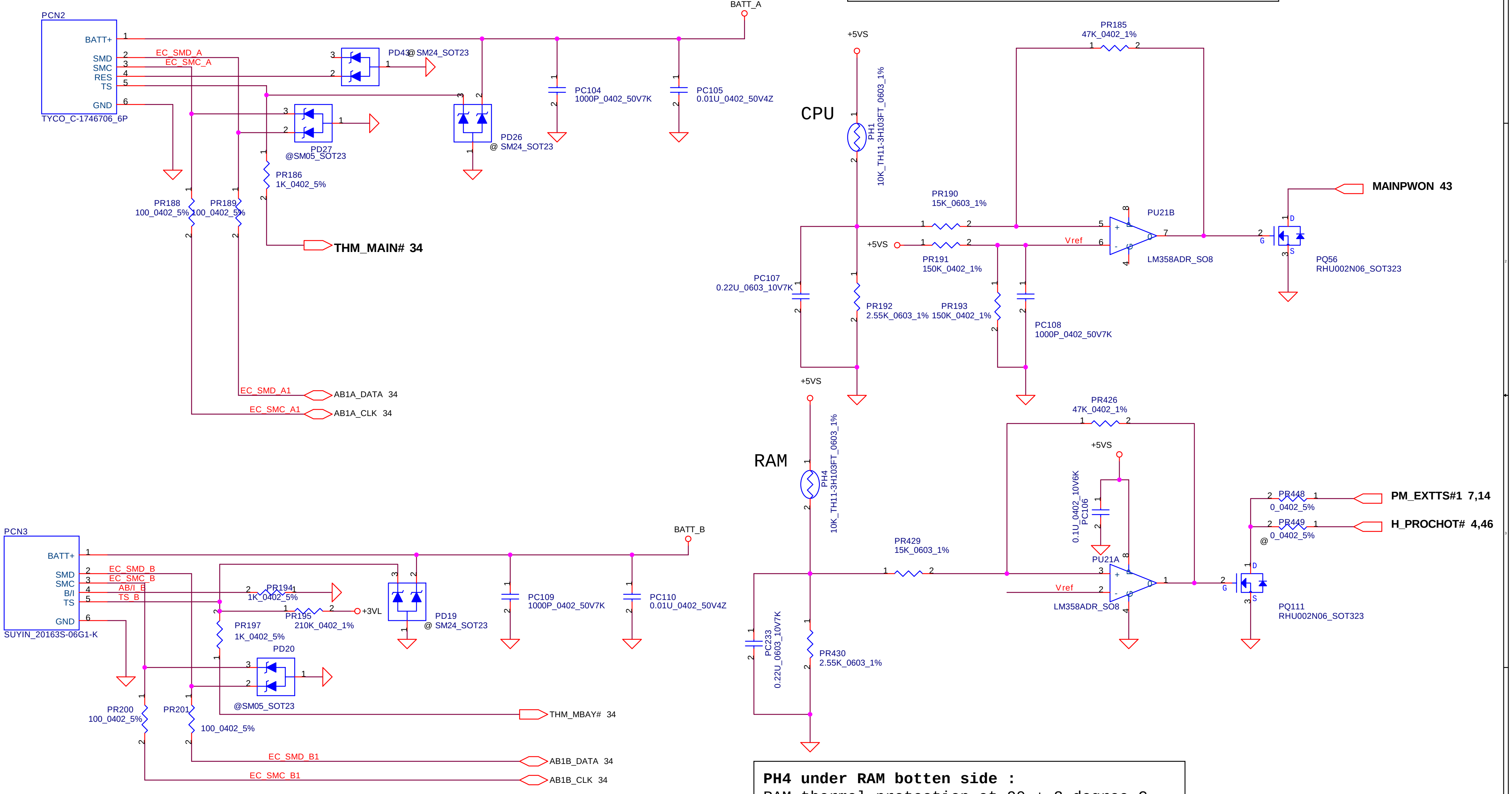
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 43 +-3 degree C



PH4 under RAM botten side :
RAM thermal protection at 90 +-3 degree C
Recovery at 43 +-3 degree C

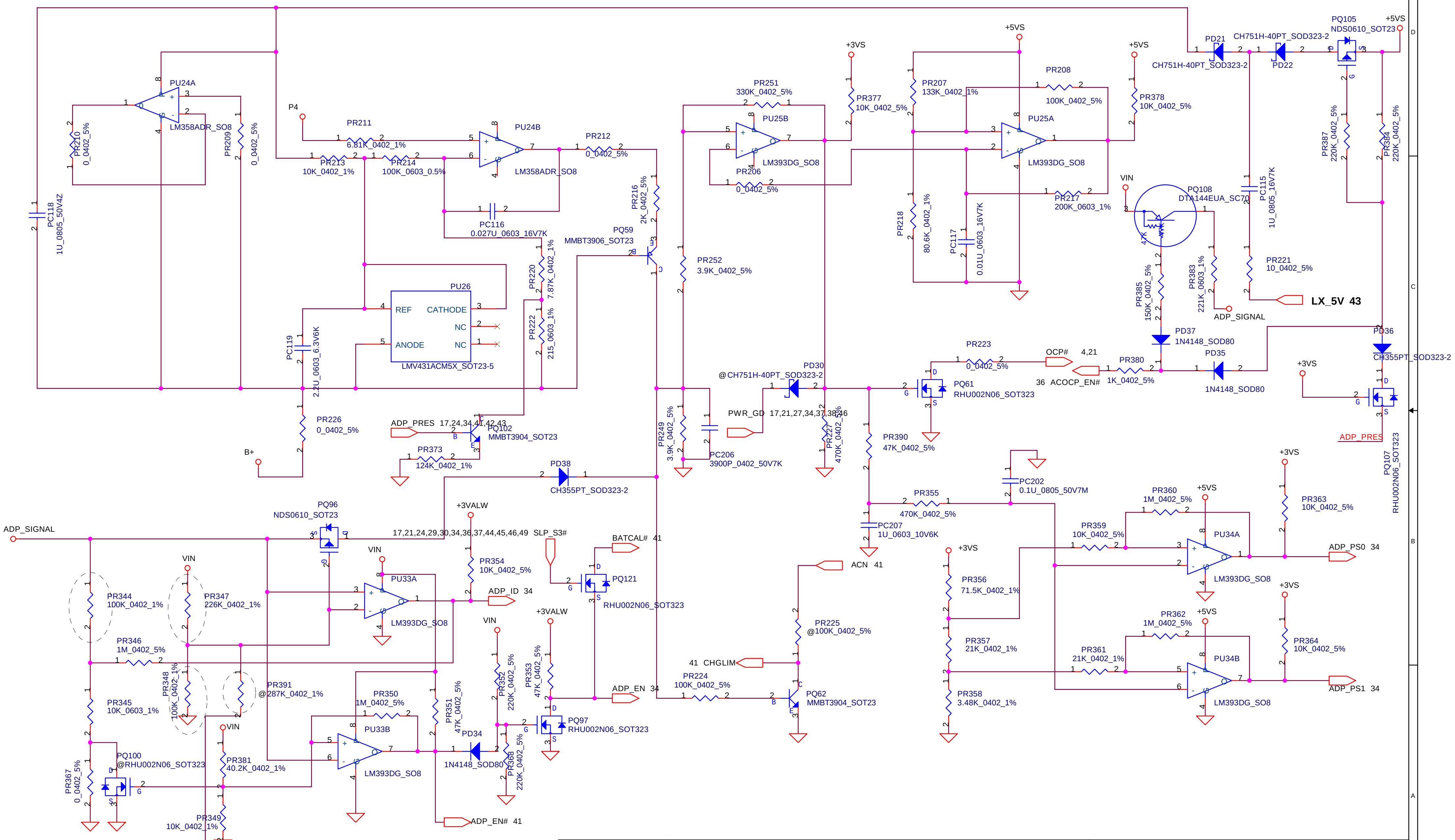
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title
BATTERY CONN

Size Custom
Document Number *LA-3331P*
Rev

Date: Tuesday, May 15, 2007



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title
ADP_OCP

Size Custom
Document Number *LA-3331P*
Rev

Date: Tuesday, May 15, 2007
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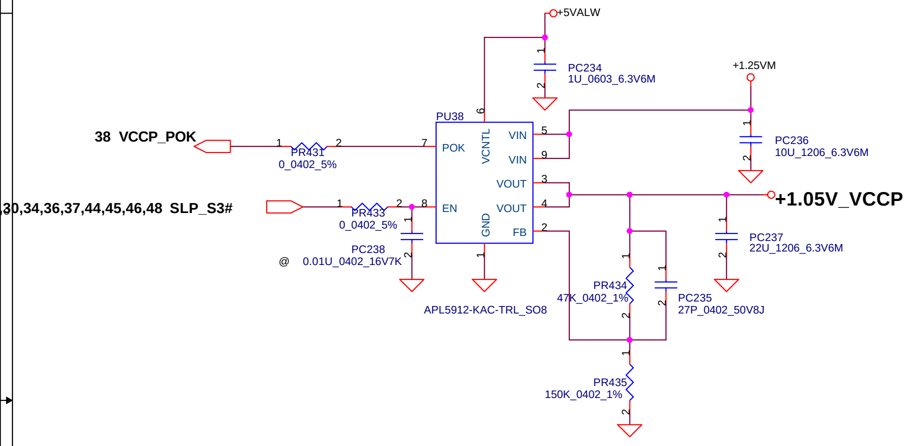

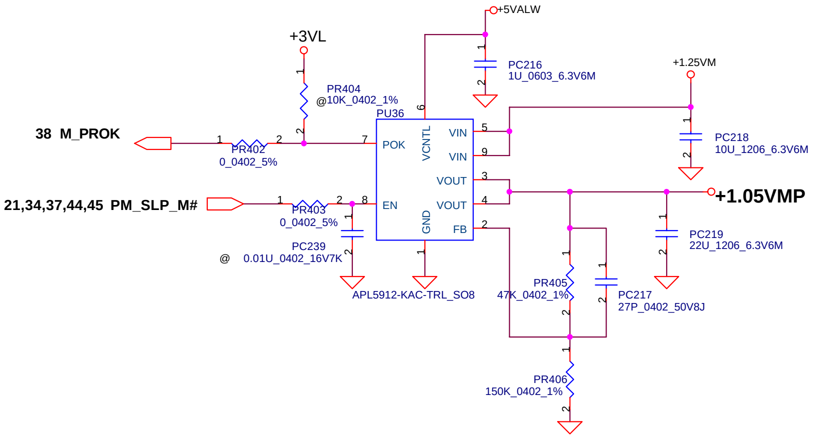

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title +1.05V_VCCP/+1.05VMP
				Size Custom / Document Number LA-3331P / Rev
				Date: Tuesday, May 15, 2007 / Sheet 49 of 59

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Charger	5/9	HP	Remove PQ91,PD32,PR376	Remove PQ91,PD32,PR376	Rev.
2	42	Battery Selector	5/9	HP	Modify battery selector design.	PU12 Change from SN74LVC1G17DBVR_SOT23-5 to SN74LVC1G14DCKR_SC70-5 Add new location PC220 as 0.047uF Add new location PC221 as 1000PF Add new location PR407 as 470K ohm. Add new location PR408 as 1K ohm.	
3	43	3.3VALW/5VALW	5/9	HP	Modify 3.3VALW/5VALW solution	Change solution from TPS51020 to MAX8734A	
4	44	2.5VALW/1.5VS/ 1.05VCCP	5/9	Compal	Remove 2.5VALW, H/W no need!	Remove PU20, PC72, PC73	
5	47	BATTERY CONN	5/9	Compal Thermal team	Add RAM thermal protection schematic.	Add new location PH4,PC233,PR430,PR429,PR426,PQ111	
6	48	ADP_OCP	5/9	HP	Modify ADP_OCP design	Delete PR379,PQ103,PQ104,PR386,PR382,PQ106	
7	43	3.3VALW/5VALW	5/9	Compal	Modify 3.3VALW/5VALW location for layout.	Swap location PC33, PC44 Swap location PC34, PC45 Swap location PQ37, PQ38, PL5 PL6, PR100, PR104, PC39 , PC199.	
8	44	1.25VM/1.5VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution	
9	49	1.05V_VCCP/ 1.05VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution.	
10	45	1.8V/0.9VS	6/2	HP	HP request to follow Chimay.	Modify 1.8V/0.9VS schematic.	
11	41	Charger	6/6	HP	HP request!	Modify Charger schematic.	
12	42	Battery selector	6/6	HP	HP request!	Modify selector schematic.	
13	47	BATTERY CONN	6/6	HP	HP request!	Modify main battery power in schematic.	
14	45	1.8V/0.9VS	6/7	HP	At S3 mode, 0.9V need exist, so connect PR242 to 1.8V	Modify PR242 connect to 1.8V	
15	46	CPU_CORE	6/21	HP	HP request.	Modify PU31.35 pin connect to SLP_S3#, originally is connect to VR_ON.	

Security Classification	Compal Secret Data		
Issued Date	2006/02/28	Deciphered Date	2007/02/28

Compal Electronics, Inc.

Title
Changed-List History-1

Size
Document Number
LA-3331P
Rev
0.5

Date: Tuesday, May 15, 2007

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	41	Charger	5/9	HP	Change PQ114 to BSS138.	Change PQ114 to BSS138.	
17	47	BATTERY CONN	9/7	Compal	Intel Document for the DDR Module Thermal Diode design	Change the PQ111.1 connection from H_PROCHOT# to PM_EXTTS#1	
18	43/44		11/1	Compal	Dual N MOSFET has failure rate at other project, to reduce Dual N MOS useage.	Change 3V, 1.5V solution, to single N Mos FET solution.	
19	41	Charger	03/29	Compal	Reserve some components for EPA.	Reserve PR21, PR22, PQ124 and PR19.	
20			03/30	Compal	DFx request modify footprint to prevent shift issue.	Modify PD10,PD12,PD14,PD16,PD33,PD34,PD35,PD37(SC11N414880) footprint from SOD80 to LL34.	
21			04/02	Compal	For Energy star	Unistall Uninstall PR1, PR17 and PR18.And install PR19,PR21,PR22,PQ124.	
22			04/02	Compal	For ADP OCP setting.	Change PC116 from 0.22U_0603_16V_X7R to 0.027U_0603_16V_X7R.	
23			04/02	Compal	For ADP OCP setting.	Change PR222 from 422 ohm 1% to 215 ohm 1%.	
24			04/02	Compal	For ADP OCP setting.	Change PC117 form 0.027U_0603_16V_X7R to 0.01U_0603_16V_X7R.	
25			04/02	Compal	For ADP OCP setting.	Change PR217 from 604K_0603_1% to 200K_0603_1%	

Security Classification	Compal Secret Data		
Issued Date	2006/02/28	Deciphered Date	2007/02/28

Compal Electronics, Inc.

Title: **Changed-List History-1**

Size | Document Number: **LA-3331P** | Rev 0.5

Date: Tuesday, May 15, 2007 | Sheet 51 of 59

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	26	Mini Express Card	7/3	Compal	H28 & H29 size different.	Change H28 size to same as H29.	0.2
2	24	GIGA LAN	7/4	Compal	BOM Leverage to Chimay.	Chnage Y8 to 25MHz_20P_1BG25000CK1A (Same as Chimay)	0.2
3	18	GPIO Extender	7/4	Compal	Use wrong package with BOM (U59).	Correct the package.	0.2
4	34	Capacitive I2C	7/27	HP		Change R1918, R1919 & add R2174 to 330 ohm.	0.2
5	15	FSB SEL	7/27	HP	No good for layout quality.	Del R1719, R1726.	0.2
6	20	RTC Conn	7/26	Compal	Wrong Package	Change JP28 from SP02000D000 to SP02000D700.	0.2
7	33	NUM_LED#	7/25	Compal	System auto re-boot	Add R2168 pull up to 3VL.	0.2
8	30	Head Phone	7/26	HP	ANTI-POP noise	Add circuit for this issue	0.2
9	26	WLAN	7/27	HP		Add R2158 connect to +3VS and connect to JP30 pin 2,39,41,52 , pin37,43 connect to GND.	0.2
10	18	Quick Switch	7/26	Compal	Wrong package for PCB foot print (U57).	Correct the package.	0.2
11	21	CPU Clock	7/28	Compal/HP	VRMPWRGD has glich to cause wrong CPU clk.	Add R2173 & reserve C1576.	0.2
12	18	Quick Switch	7/28	Compal	Channel A & B will twist togeter as current layout.	Swap Channel A & B on schematic.	0.2
13	06	VCCP	8/1	Compal		Delete C1570 ~ C1573	0.2
14	21	CL_VREF1_ICH	8/2	Compal	Wrong pull high to +3VM.(R1855)	Change pull up to +3VALW.	0.2
15	31	USB	8/2	Compal	No pull up resistor for USB power switch OC pin.	Add R2175 and pull up to +5VALW.	0.2
16	18	Quick Switch	8/3	HP		Add U61 and Reserved R2176 for Q-switch select pin.	0.2
17	38	Power Good	8/4	Compal	VCC1_PWRGD has glich when power on.	Reserve C1577 on PWRGD to GND.	0.2
18	21	Power Good	8/7	Compal	CLK_ENABLE# has glich when power on.	Change R1862 from 330ohm to 1K ohm.	0.2
19	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
20	27	CardBus Controller	8/15.	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	07	Clock	8/11	Compal	CLK_MCH_3GPLL/CLK_MCH_3GPLL# reversed.	Correct CLK_MCH_3GPLL/CLK_MCH_3GPLL#.	0.3
2	27	CardBus Controller	8/15	Compal	Easy conflict with other device that use same IRQ.	Chnage connect from PCI_PIRQB# to PCI_PIRQG#.	0.3
3	21	USB	8/23	Compal	System easy hang-up when plug USB2.0 device.	Separate from pull up resistor of U10 for these pins.	0.3
4	34	PGD_IN	8/23	HP	Leverage Chimay SI schematic.	Add R2177(100K) pull down to GND.	0.3
5	34	EC VCC0(PIN 68)	8/24	HP	+3VL may over budget.	Add R2178, R2179(RV) for option the power source.	0.3
6	34	EC	8/24	HP	Leverage Chimay SI schematic.	Add D77, R2180 and connect D77 pin2 to U10 pinAE10.	0.3
7	33	SPI ROM	8/24	HP	Debug card asserts hold, can't assert both SPI ROM.	Add R2181 to connect SPI_HOLD#0 and SPI_HOLD#1.	0.3
8	26	MINI Card	8/24	HP	May leakage issue from WLAN card.	Add D78 to prevent this issue.	0.3
9	21	Power Sequency	8/24	HP	There is a shoot when power on of this pin.	Reserve R1862 and add R2182(10K) pull up to PWR_GD.	0.3
10	21	GPIO26	8/24	HP	Default is input can't floating.	Add a pull up R2183(10K) to +3VS.	0.3
11	21	GPIO17	8/24	HP	Default is input can't floating.	Make R2115 from RV to mount.	0.3
12	21	STP_CPU#	8/24	HP	Can't into C3 status.	Mount R1829.	0.3
13	21	XDP_DBRESET#	8/24	HP	Leverage Chimay SI schematic.	Change R1847 to 1K.	0.3
14	21	SPI_CS1#	8/24	HP	Only need one 4MB BIOS chip.	Add R2184(0 ohm) for BOM option.	0.3
15	17	MXM-HE	8/24	HP	Need High performace VGA card.	Chnage MXM-III to MXM-HE.	0.3
16	17	HDMI	8/25	HP	BOM change.	Change R1990 to 1K, R1991 to 10K and add L23, C1578.	0.3
17	21	GPIO12	8/28	HP	Add BOM option for SPI_CS1#.	Change connect of R1845.2 from LAN_PHYPC to LAN_PHYPC_R.	0.3
18	21	GPIO1 & GPIO11	8/28	HP	Net Change.	Exchnage OCP#(To GPIO1)&LANLINK_STATUS#(To GPIO11)	0.3
19	28	Card bus ETD test	8/31	HP	May some issue with ETD test.	Reserved C1509.	0.3
20	35	KBD Connector	8/31	HP	To meet HP 2007 platform defined.	Chnage JP12 from 26pin to 30pin.	0.3
21	10	L22	9/6	HP	BLM18PG221SN1 impedence is 221ohm@100MHz.	BLM18PG330SN1 impedence is 33ohm@100MHz.	0.3
22	26	Wireless LAN	9/6	HP	Connect C217, C171, C493 to wrong power.	Connect C217, C171, C493 from +3VS to +3VS_WLAN.	0.3
23	07	CRESTLINE	9/6	HP	Change Chip version from A0 to B0.	Mount R2134.	0.3
24	04, 21	Second FAN	9/7	Compal	Thermal team ask to add control for second FAN.	Add R2185, R2186 and use GPIO20 to control FAN.	0.3
25	17	MXM power B+	9/8	Compal	Delete C9 cause not enough space to placement.	ADD C1579, C1580(1210 size) to replace C9.	0.3
26	24	LAN Connector	9/12	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	ADD C1581, C1582(0402 size) per EMI request.	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	20, 34	BATTERY LED	10/2	HP	GREEN_BATLED# keep high when AC/DC exist.	Change connection between SB & EC.	0.4
2	21	SM Bus	10/3	Compal	SM Bus connection is not correct.	Correct connection of SM bus and reserved R1817, R1820.	0.4
3	35	Function Connector	10/5	HP	Wireless LED always on.	Make change of JP1, pin1-> +3VL, pin2 -> +3VS.	0.4
4	20, 23	Kensington support	10/18	HP	Removed Kensington support.	Remove JP60, Q122, R2084.	0.4
5	18	Quick-Switch	10/18	Nvidia	We will change Quick switch to PI3HDMI412FT-A	Don't need pull up, removed RP44 ~ RP47.	0.4
6	18	Quick-Switch	10/18	HP	Don't have decoupling for U57 1.5VS.	Add C1583, C1584.	0.4
7	34	KBC Debug port	10/18	HP	Don't need use JP55, JP56 for debug.	Removed JP55, JP56 from SI1.	0.4
8	34	RUMRST# timing	10/18	HP	It may don't need these circuit.	Reserve them at SI1.(Install R2144, RV : Q128, D73, R2145~2146)	0.4
9	34	RUMRST# timing	10/18	HP	It different to desgn guide 1.1.	Change R2145 to 4.7k, pull up to +3VALW and connect to Q128 base pin.	
10	34	VCC1 Power	11/02	HP	Chnage Design.	Chnage VCC1 power option to +3VALW or +RTCVCC.	0.4
11	21	LANSTATUS#	11/02	HP	System auto power on after plug AC in.	Add Q136 to isolation U10 directly link to NIC, and add PU R2187.	0.4
12	31	USB Switch	11/03	Compal	Don't need dual layout for USB power switch.	Remove U7, U36.	0.4
13	30	Audio	11/03	HP	To pass Vista test of Audio.	Change R207, R217 from 15ohm to 56.2ohm.	0.4
14	25	LAN	11/06	Intel	Intel Santa Rosa Platform Message of the WW44	Change R1903 from 3.92Kohm to 1.4Kohm.	0.4
15	24	LAN Connector	11/06	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	Mount C1581, C1582 --> 680pF(0402).	0.4
16	17	MXM Connector	11/08	HP	Need BOM option of SLP_S3# for use G71 or G84.	Add R2190(0ohm).	0.4
17	4	Thermal Senser	11/08	HP	Abita will chnage to new Thermal senser in the future.	Add R2188, R2189(0ohm).	0.4
18	35	MDC	11/08	HP	Implement new MDC future.	Connect JP26.2 to +3VS.	0.4
19	15	FSB Freq Selecter	11/09	HP	Need HW option for 667MHz or 800MHz	Add JP62, JP63 and install R1689,R1696,R1705,R1737	0.4
20						and reserve R1694,R1716,R1734.	
21	37	M-Power discharge	11/10	Compal	It's wrong connection of discharge control circuit.	Correct Q97, Q98, Q99 pin2 connect to LAN_WOL_EN#.	0.4
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	FP Connector	12/18	Compal	ME ask to change FP connector.	Change FP connector(JP15) to same as JP58.	0.5
2	34	KBC	12/18	HP	System can't power on.(PWR1 connect to +3VALW)	PWR1 will modify connect to +3VL(R1908.2).	0.5
3	35	PLTRST/CBB	12/18	HP	Capacitive Button Board may not need PLTRST.	Disconnect PLT_RST# from JP1.3.	0.5
4	38	KBC Power good	12/19	HP	VCC1_PWRGD have glich when plug AC/DC power.	Del U54, Q106 and R1978, replace by U15.	0.5
5	25	LAN ENERGY DET	12/19	Intel	Intel request chnage value of R1903.	Change R1903 from 1.4K to 1.87Kohm.	0.5
6	38	PWR_GD	12/19	HP	Ripple noise to cause system auto shutdown issue.	Add C1585(0.1uF) and R2191(1Kohm).	0.5
7	34	KBC	12/20	HP	Current design may possible to damage the KBC.	Change design to add Q137, Q138(2N7002) and R2192(100Kohm), R2193(1Kohm).	0.5
8	27	Card bus Controller	12/21	Compal	There is pop noise when plug some PCMCIA card.	Add R2194 and C1586 and change value for R2038 and R2041.	0.5
9	24	NIC	12/21	Intel	82566MM may have start-up issue with Crystal.	Modify layout and add R2195(0ohm).	0.5
10	24	ACBS	01/02	Intel	To enable iAMT and support ACBS.	Mount Q85 and R2072 but remove Q87~Q88 and R1877.	0.5
11	35	Power Buttom	01/04	Compal	ESD test is not good for Switch board.	Add ESD diode(D79) to M/B and add ME solution.	0.5
12	24	NIC	01/05	Compal	EMI test is fail from NIC.	Add C1587~C1590, L24 and change C1421 to 820pF, R12~R13 to FBMA-10-100505-151T.	0.5
13	38	LAN Reset	01/05	HP	HP request to modify.	Change this power rail from +3VM_LAN to +3VM.	0.5
14	18	Quick-Switch	01/07	HP	There is leakage issue of Q-Switch.	Add D80 for this issue.	0.5
15	37	MXM	01/10	HP	MXM board need external +2.5VS power rail.	Add U62, C1592, C1593 for this issue.	0.5
16	37	MXM	01/11	HP	2.5VS for MXM is too long.	Reserve C1594(0.1uF) close to pin.	0.5
17	37	MXM	01/12	HP	Leakage issue from MXM pin211(ADP_PRES)	Add Q139(RHU002N06) & R2196(8.2K).	0.5
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	USB Connector	02/07	Compal	Not need 40 pin connector for USB/Audio connector.	Change JP25 from 40pin to 30pin.	0.6
2	34	KBC VCC0	02/07	Compal	Can't power on and AC power LED always light.	Change R2179 connect to +3VL, and add option R2197 to GND.	0.6
3	33	FPR/USB S3/S4	02/12	HP	Change control method for FPR/USB power in S3/S4.	Add R2198, R2200~R2202, Q140~Q141.	0.6
4	37	WOL control	02/14	HP	Add 100K pull up for LAN_WOL_EN.	Add R2203(100Kohm).	0.6
5	29	SPDIF	02/14	HP	HP request to add 4.7K pull down on SPDIF out.	Add R2206(4.7Kohm).	0.6
6	29	Card reader	02/14	HP	Need reserve some test point.	Add R2205(0ohm) and T94.	0.6
7	17	MXM thermal pin	02/14	HP	Isolation MXM_THERM# and PWR_GD use MOSFET.	Add Q142 and R2204 for the modify.	0.6
8	30	USB Connector	02/28	HP	Couple mV over the 150mV GS limits.	Change R207, R217 from 56.2 ohm to 60.4 ohm.	0.6
9	21	THERM_SCI#	02/28	HP	HP request to design change.	Remove R1854 from BOM list.	0.6
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	15	Clock Gen	03/19	HP	Remove 0hom damping of differential clock pair.	Remove RP49, RP51~RP57, reserve RP48.	0.8
2	15	FSB selecter	03/19	HP	Remove FSB selection function.	Remove JP62, JP63, Reserve R1689, R1696, R1705, R1737, install R1694, R1716, R1734.	0.8
3	29	Audio Codec	03/19	HP	To improve audio quality of docking.	Change R290~R291 to 6.04K and R289, R292 to 2K.	0.8
4	20	GPU Thermal	03/19	HP	Design change for MXM board.	Reserve R1854.	0.8
5	26	NAND Card	03/23	HP	Don't need this function for MP.	Reserve R2064, R2065, C1553 ~ C1560.	0.8
6	21	OC6#/GPIO30	03/23	HP	This pin is not long use for MXM.	Reserve R2207 for isolation.	0.8
7	38	POK CKT	03/28	Compal	For schematic leverage to Chimay.	Change LMV331(U47,U48) to LM393(U47), and remove R1976, C1487	
8	24	NIC power	03/28	Compal	Don't need +V1.0M_LAN power regulator.	Remove Q90, C1436 ~ C1440.	0.8
9	31	USB Port	03/28	Compal	To correct schematic and make layout smooth.	Remove C118, C498, C499, R49 and change C126 to 330uF.	0.8
10	31	BT	03/28	Compal	To make layout smoothly.	Remove D16.	0.8
11	34	KBC Clock	03/28	Compal	To make layout smoothly and EMI request.	Remove R1929, C1455.	0.8
12	21	LAN/WLAN Switch	03/30	HP	Unplug AC, WLAN will be disabled on XP OS.	Add U63 for slove leakage issue of enable ACBS.	0.8
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	NB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q114~Q117, R2049~R2052, install R111, R113, R122, R132.	1.0
2	22	SB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q118~Q121, R2058~R2061, install R138~R141.	1.0
3	22	Audio Codec	05/02	HP	To improve ICH_V5REF_RUN of SB.	Change C1190 from 0.1uF to 1uF.	1.0
4	36	Easy crack issue	05/14	HP	To prevent crack issue for L14	Change L14 material to SM010008E10.	1.0
5	14	DDR DIMM B	5/15	HP	To solve OTS issue OTS 265441 and 261307.	Change R33 pin2 connect to +3VM.	1.0
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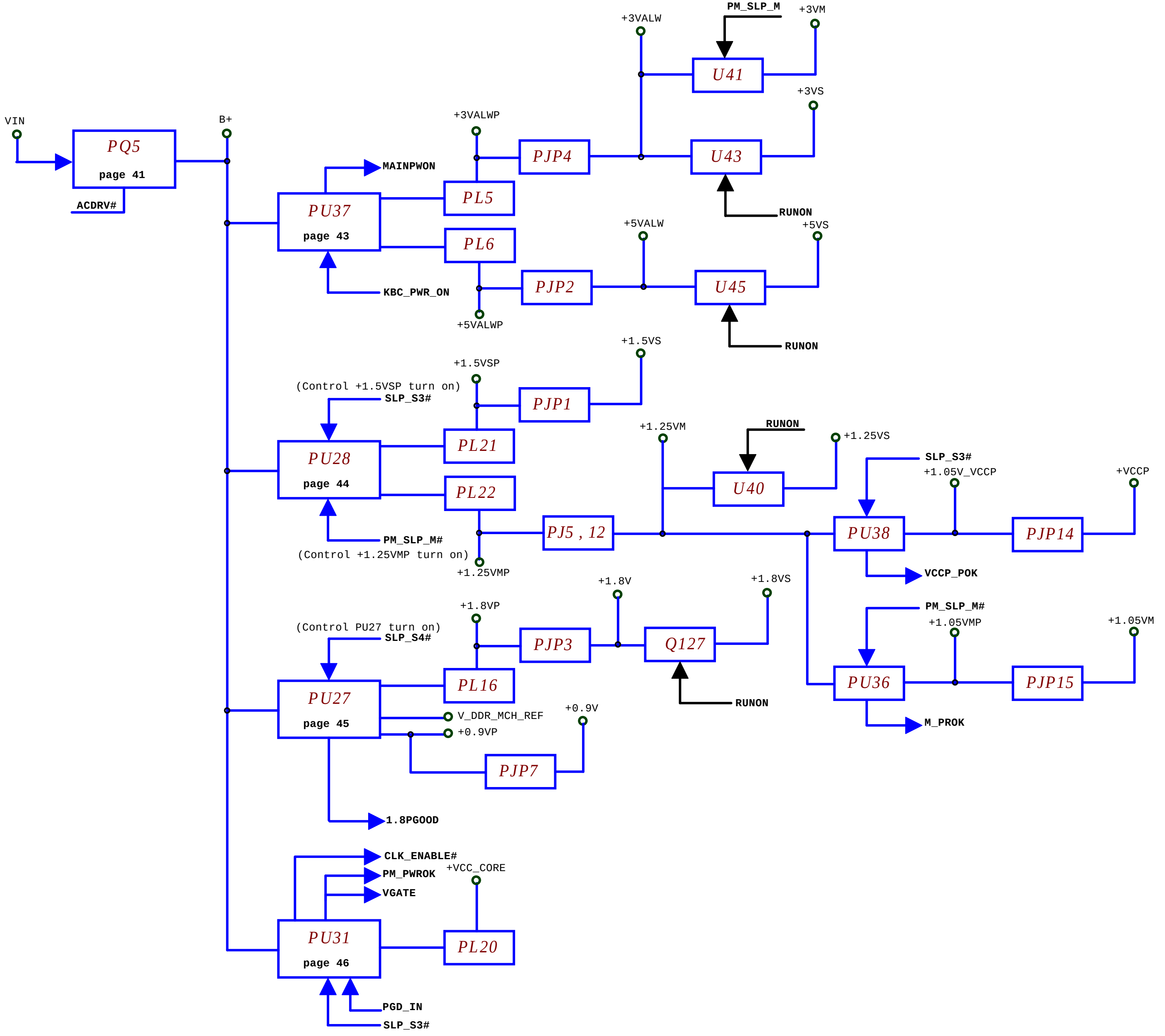

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