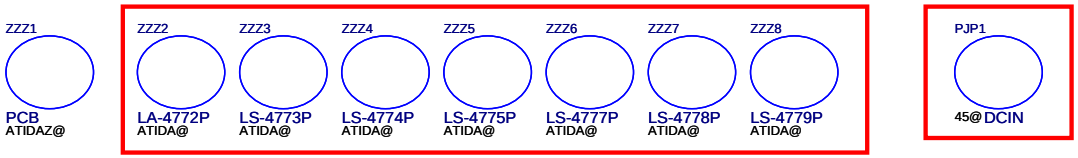

Compal Confidential

KHLB2 Schematics Document

Intel Mobile Penryn uFCPGA with Cantiga_PM + DDRIII + ICH9M

2009-01-19

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

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Title	Cover Sheet	
Size: Custom	Document Number: KHLB2 MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 1 of 56	

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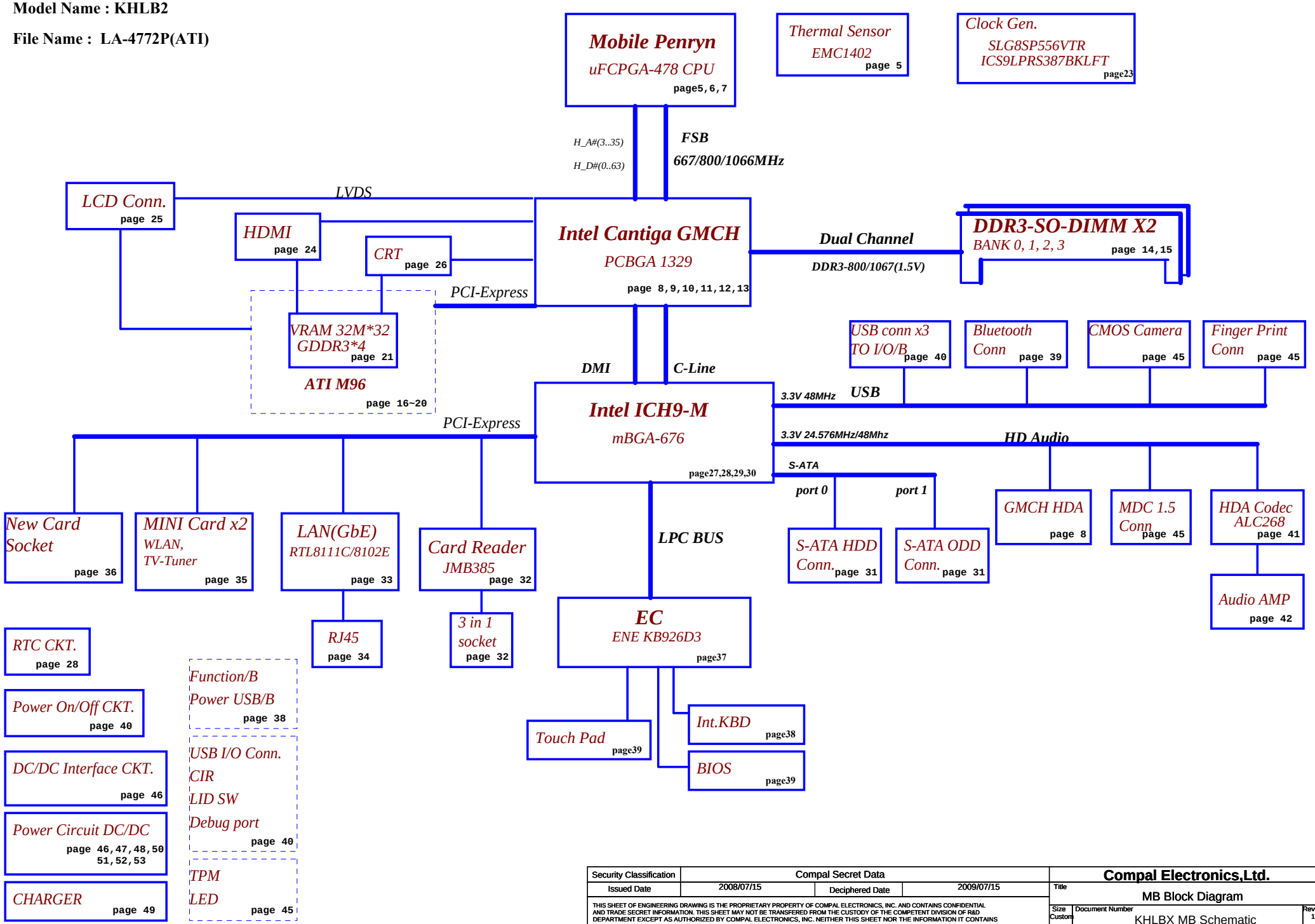
Model Name : KHLB2

File Name : LA-4772P(ATI)



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Title	MB Block Diagram	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 2 of 56	

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
EMC 1402	100_1100X b
ATI M96	

GPIO PIN Define

	ID3	ID2	ID1	ID0
JHT00(1100)	X	X	R361	R357
JHT01 (1101)	X	X	R361	R355
JHL90 (1110)	X	X	R360	R357
JHL91 (1111)	X	X	R360	R355
KHLB0 (0000)	R1052	R1150	R922	R928
KHLB1(0001)	R1052	R1150	R922	R923
KHLB2(0010)	R1052	R1150	R927	R928
12 inch(0011)	X	X	X	X
12 inch(0100)	X	X	X	X
12 inch(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X

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Title	MB Notes List	
Size B	Document Number: KHLBX MB Schematic	Rev 1.0
Date: Monday, January 19, 2009	Sheet 3 of 56	

VGA and DDR2 Voltage Rails (NB9M-GS)

State \ power plane			+1.8VS	+3VS +VGA_CORE +1.1VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	X	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

VRAM POWER SQUENCE
GDDR3 FOR 4 UNIT = 5.4A

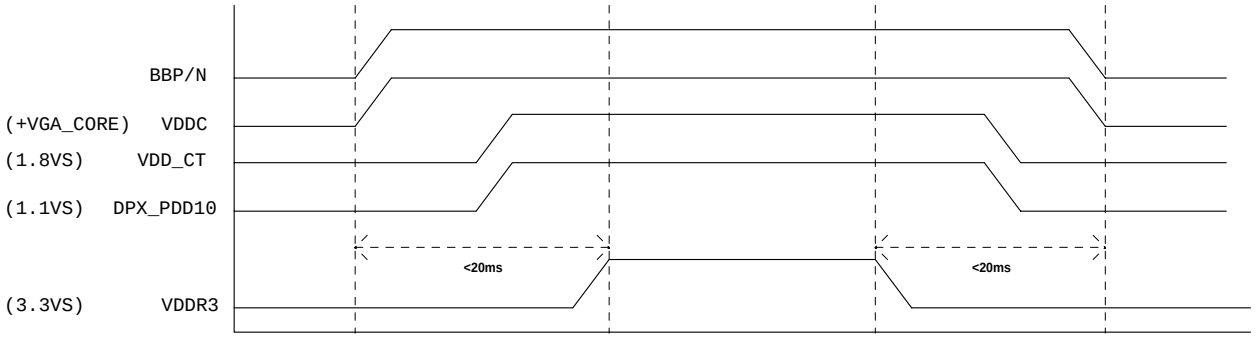
EDP at Tj = 97C*

Power Supply Rail	(V)	NB9P-GS		NB9P-GE2	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	20.65A	16.96A	18.47A	16.06A
FB_DLLAVDD	1.1	10mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	80mA			
IFPD_IOVDD	1.1	80mA			
IFPE_IOVDD	1.1	160mA			
IFPF_IOVDD	1.1	160mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	90mA			
PLLVDD	1.1	45mA			
SP_PLLVDD	1.1	45mA			
VID_PLLVDD	1.1	45mA			
TOTAL	1.1	2.3A			
FBVDD/Q	1.8	3.37A	2.02A	3.21A	2.25A
IFPA_IOVDD	1.8	95mA			
IFPB_IOVDD	1.8	95mA			
IFPAB_PLLVDD	1.8	70mA			
IFPCD_PLLVDD	1.8	25mA			
IFPEF_PLLVDD	1.8	85mA			
TOTAL	1.8	5.76A	3.69A	5.47A	3.96A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	120mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	150mA			
TOTAL	3.3	0.51A			

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	Available
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2 or MEM VID
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	FAN control and/or Thermal Alert (PWM)
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP link E
GPIO16	IN	-	Dongle DVI Mode control for Primary Displayport
GPIO17	IN	-	Dongle HDMI Mode control for Primary Displayport
GPIO18	IN	-	Dongle DVI Mode control for Secondary Displayport
GPIO19	IN	-	Dongle HDMI Mode control for Secondary Displayport
GPIO20	IN	-	Hot plug detect for IFP link D
GPIO21	IN	-	Hot plug detect for IFP link E
GPIO22	IN	-	SLI swap ready signal
GPIO23	N/A	N/A	Available

POWER UP/DOWN Sequence

BBP must ramp up before or at the same time as VDDC but not after(ensure that BBP>= VDDC at all times)



Lower Voltage leading higner voltage requirement VDDR3-VDD_CT<2V

Lower Voltage trialing higner voltage requirement VDDR3-VDD_CT<2V

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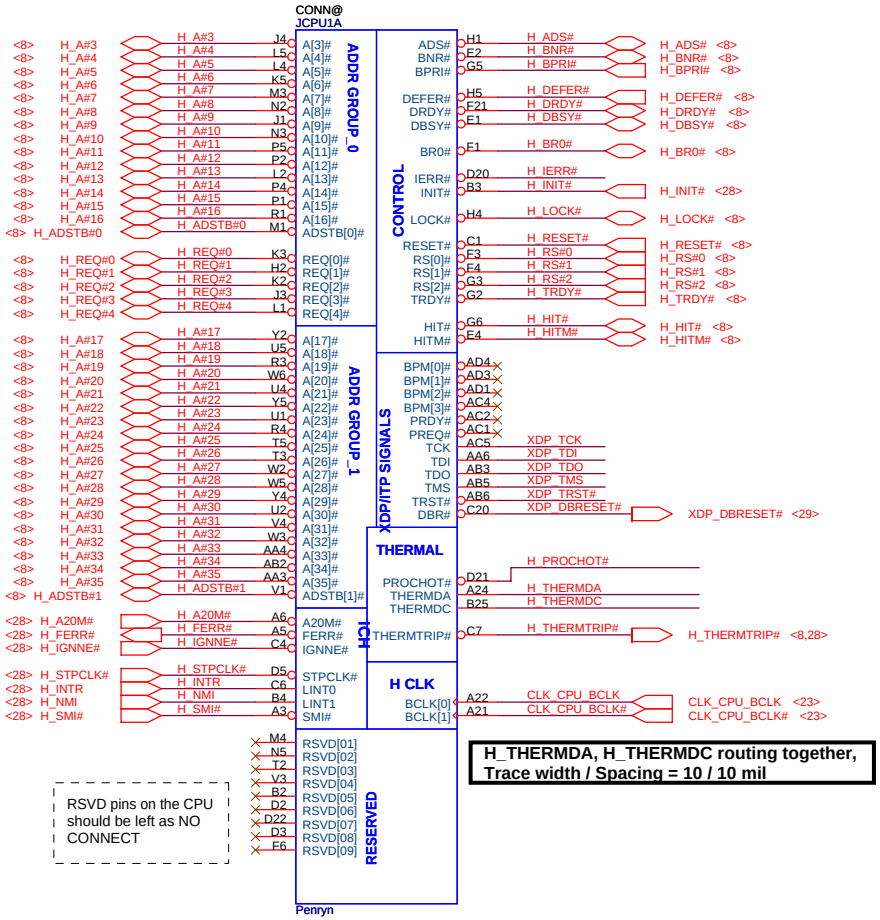
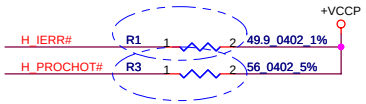
Title: VGA Notes List

Size: B | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 4 of 56

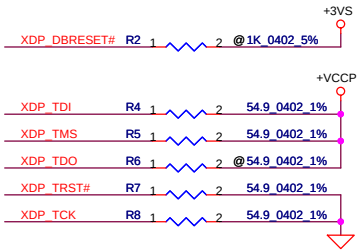


USE->56Ω,NOT USE->50Ω



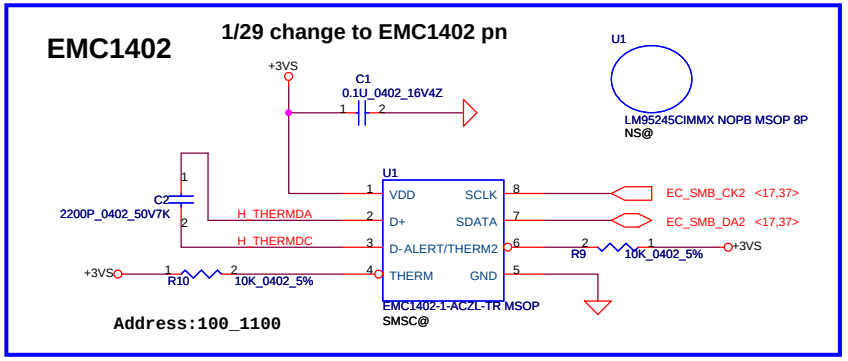
USE->68Ω,NOT USE-->56Ω

XDP Reserve

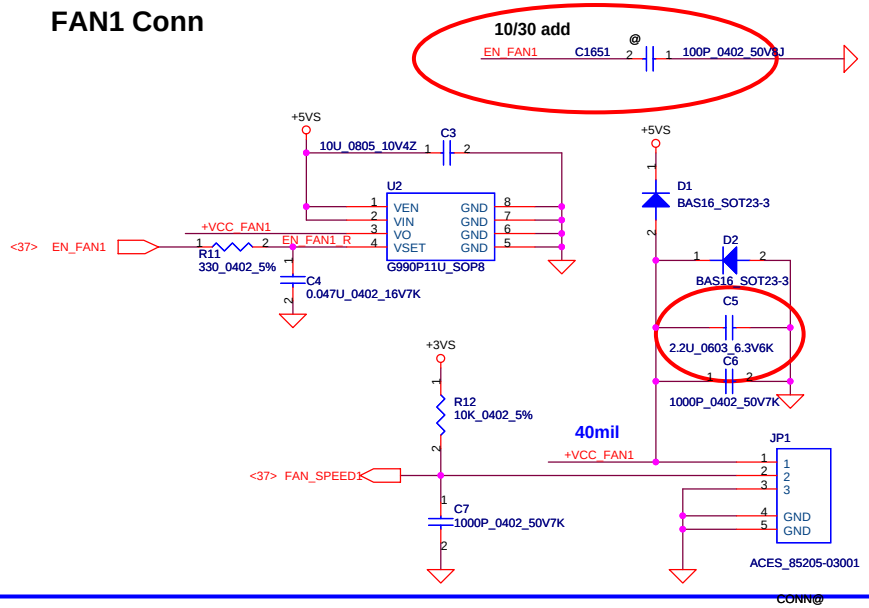


EMC1402

1/29 change to EMC1402 pn



FAN1 Conn



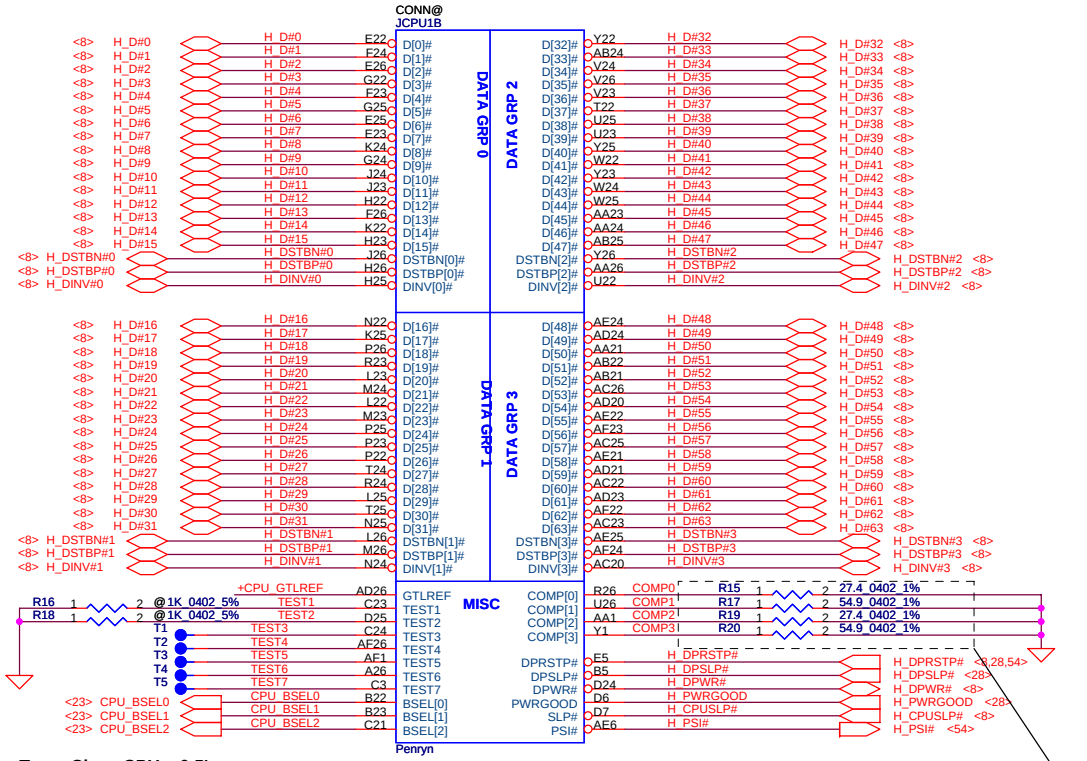
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

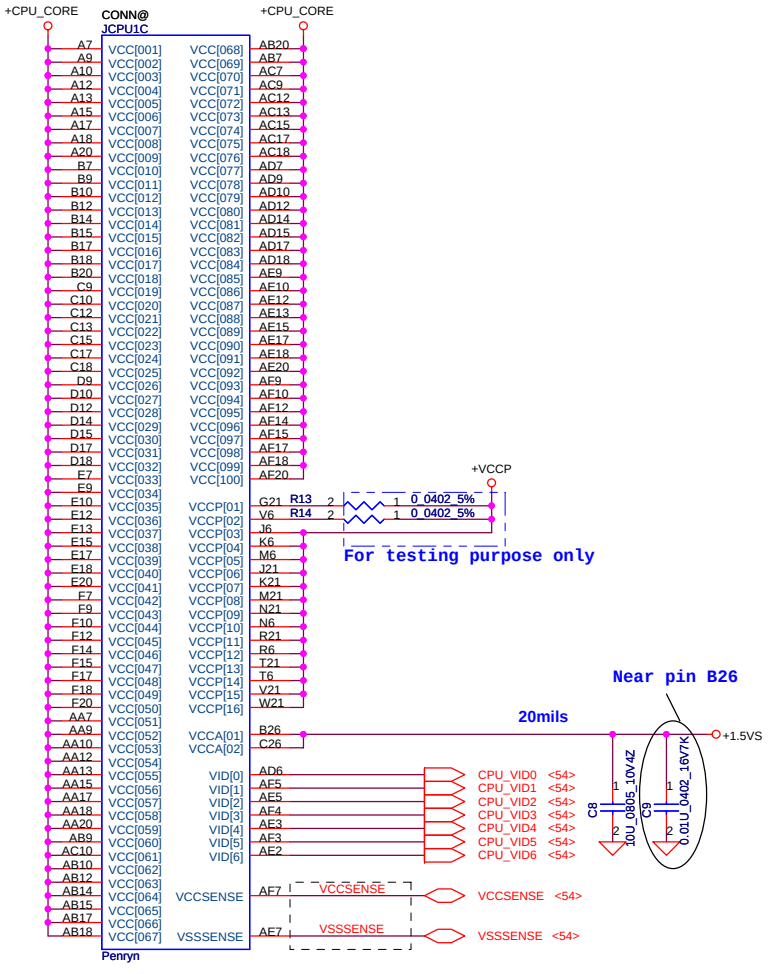
Compal Electronics,Ltd.

Title: Penryn(1/3)

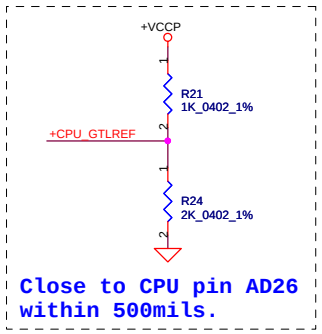
Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 | Sheet 5 of 56



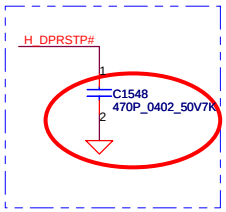


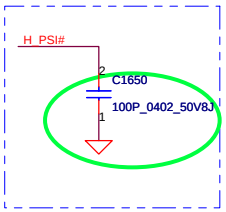
Layout note: Z0=55 ohm
0.5" max for GTLREF.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

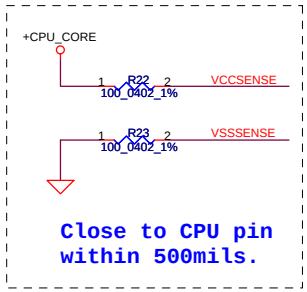
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0





Length match within 25 mils.
The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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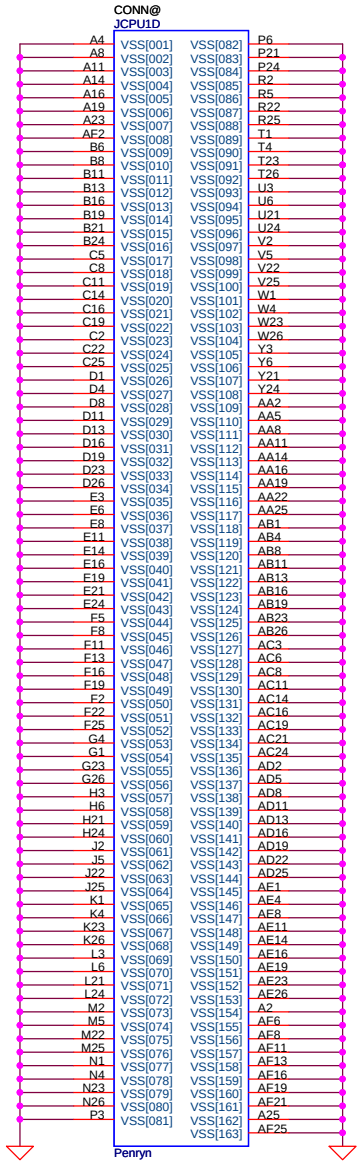
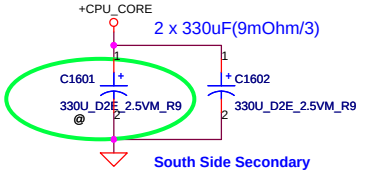
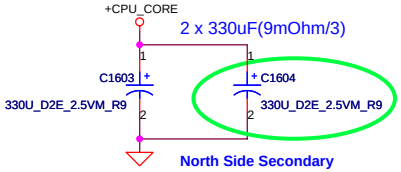
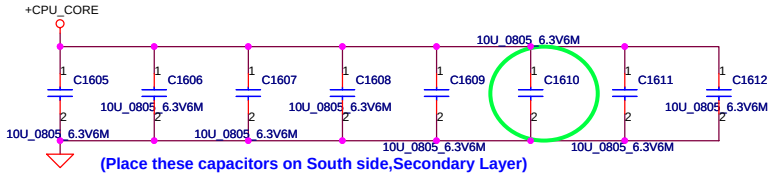
Title	Penryn (2/3)		
Size B	Document Number KHLBX MB Schematic		Rev 1.0
Date: Monday, January 19, 2009	Sheet 6 of 56		

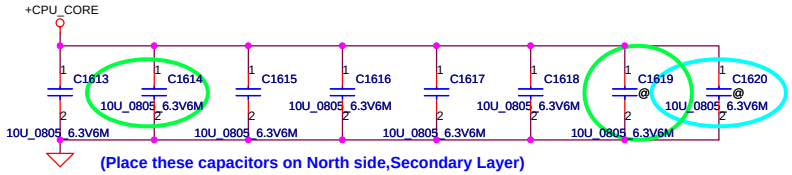


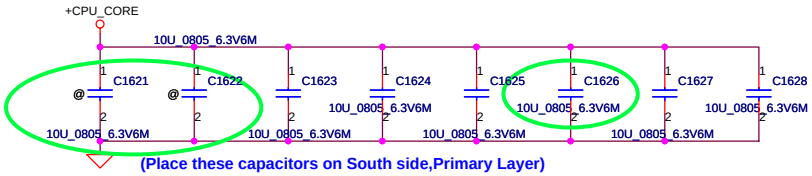
330u
ESR 9m ohm
Package(L*W*H)7.3*4.3*1.8
Rating 2.5V

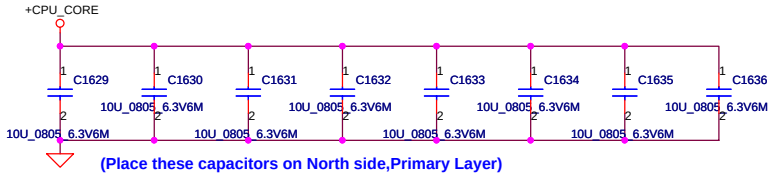




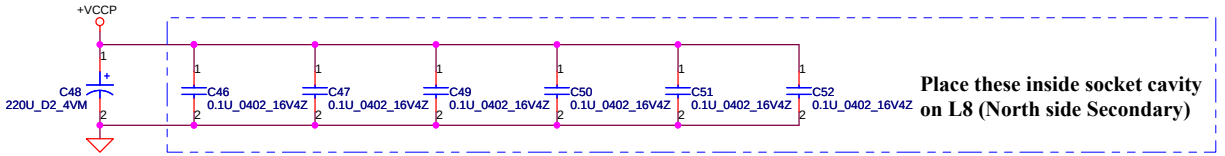








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



Security Classification	Compal Secret Data		
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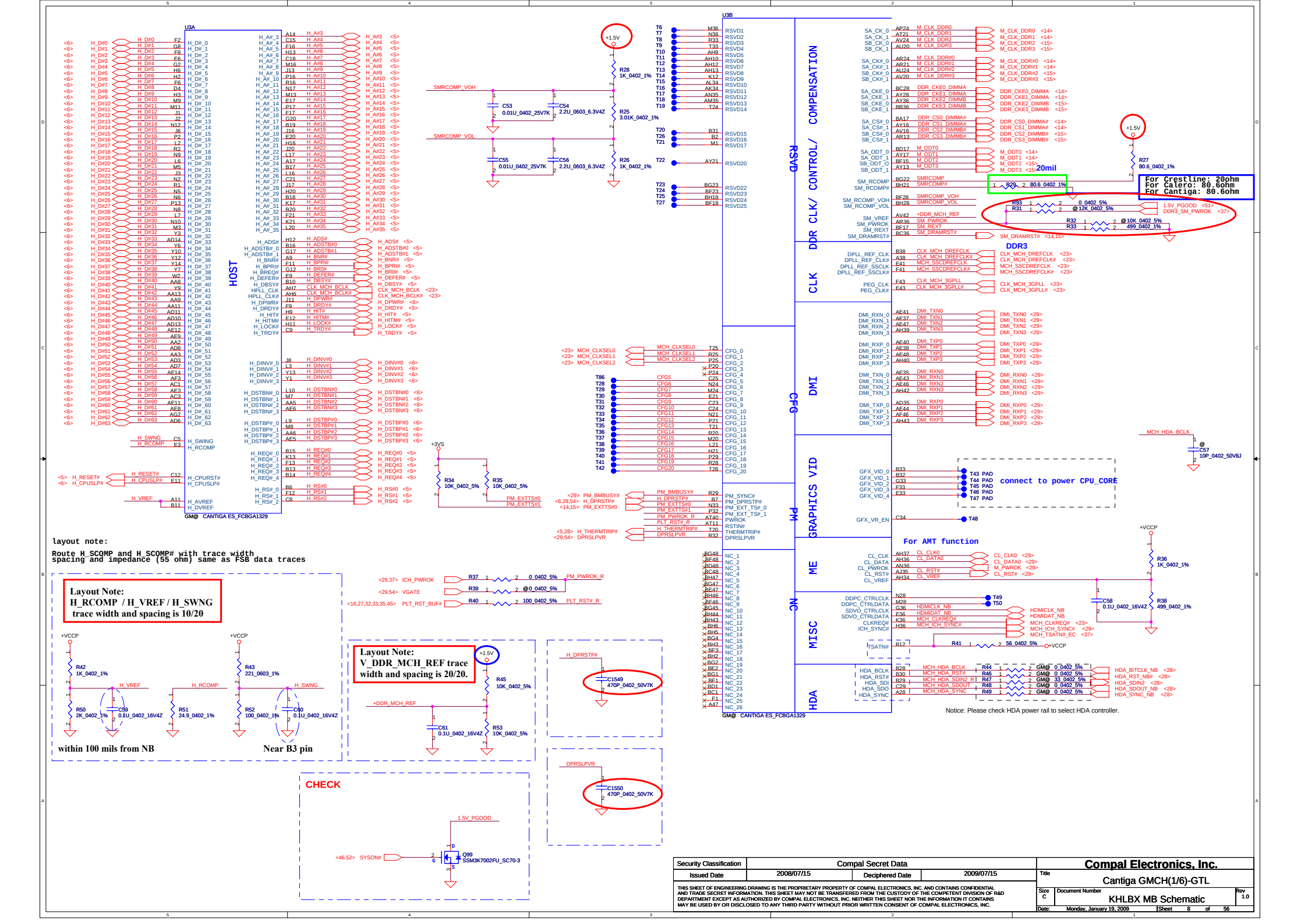
Title: Penryn (3/3)

Size	Document Number	Rev
B	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 | Sheet 7 of 56



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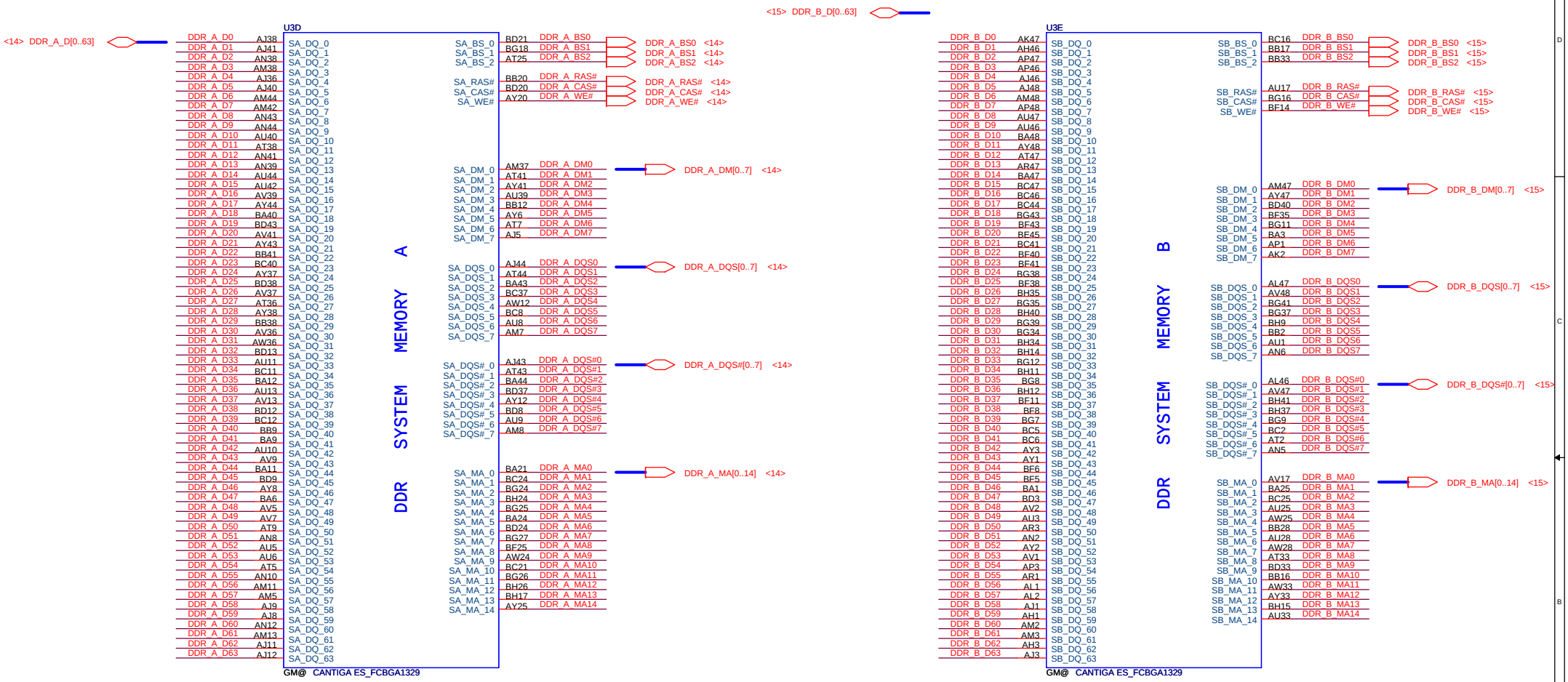
Title: Cantiga GMCH(1/6)-GTL

Size	Document Number	Rev
C	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 Sheet 8 of 56



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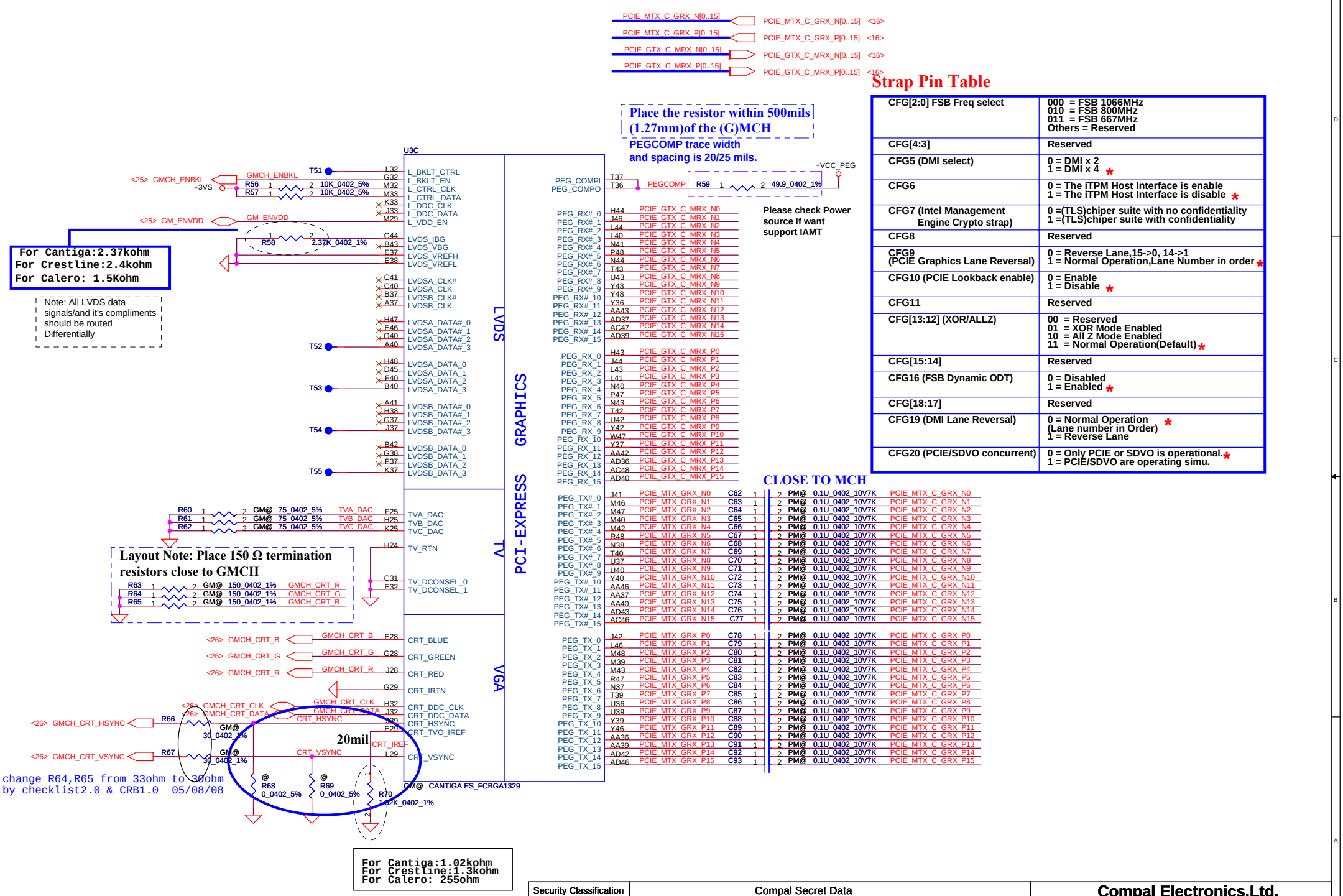
Title	Cantiga GMCH (2/6)-DDRIII	
Size B	Document Number KHLBX MB Schematic	Rev 1.0
Date: Monday, January 19, 2009	Sheet 9 of 56	



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

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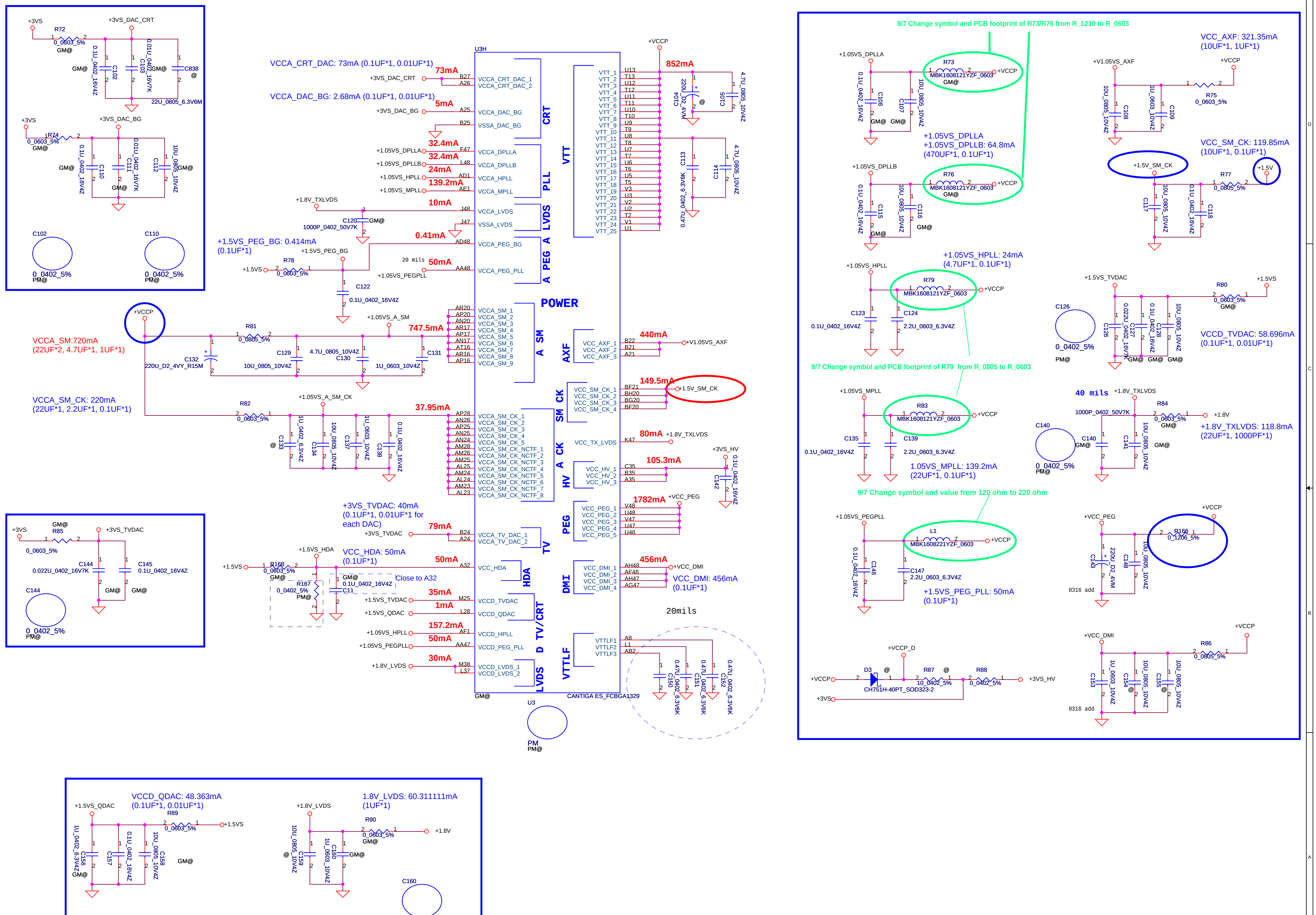
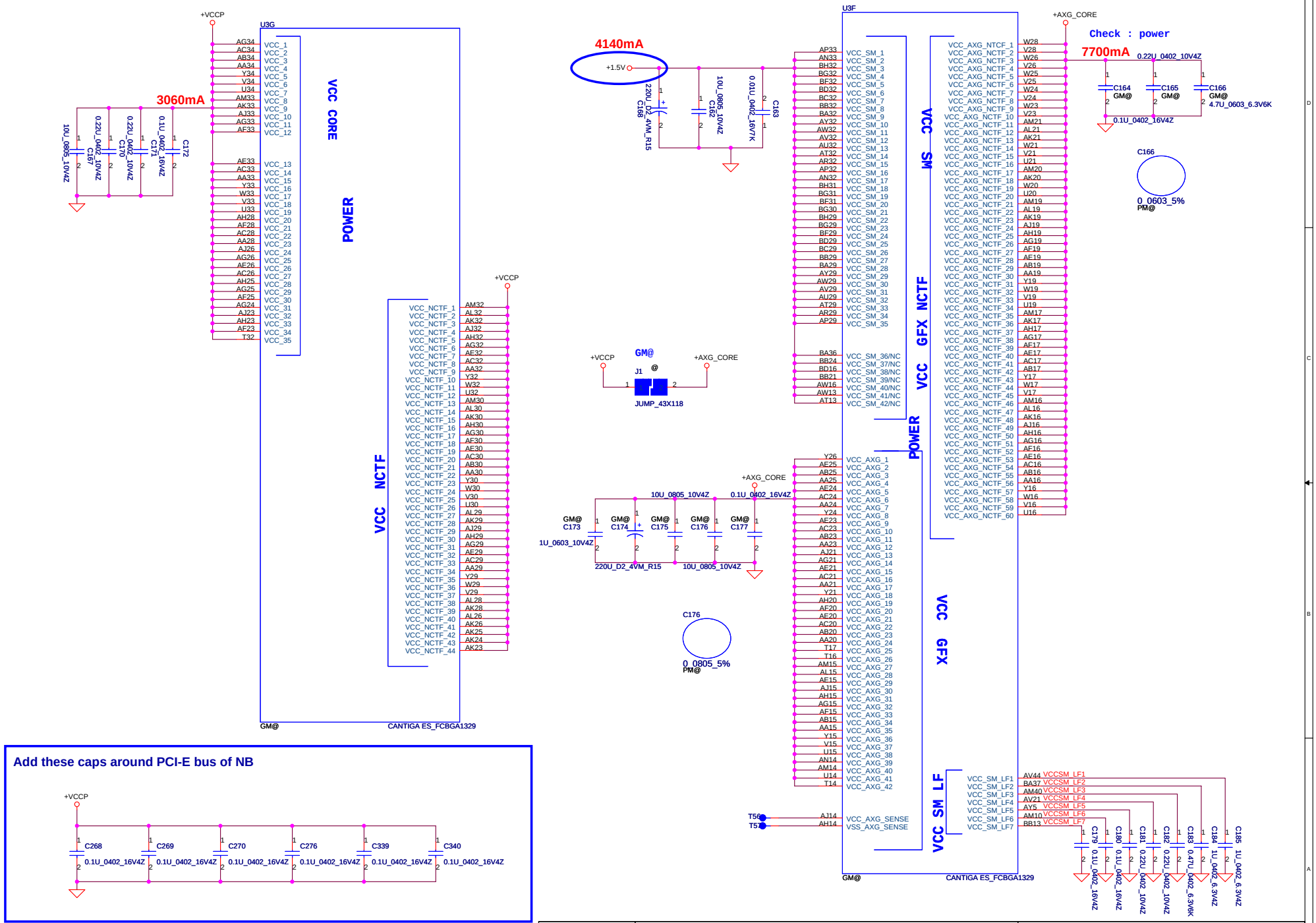
Title: Cantiga(3/6)-VGA/LVDS/TV

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 10 of 56



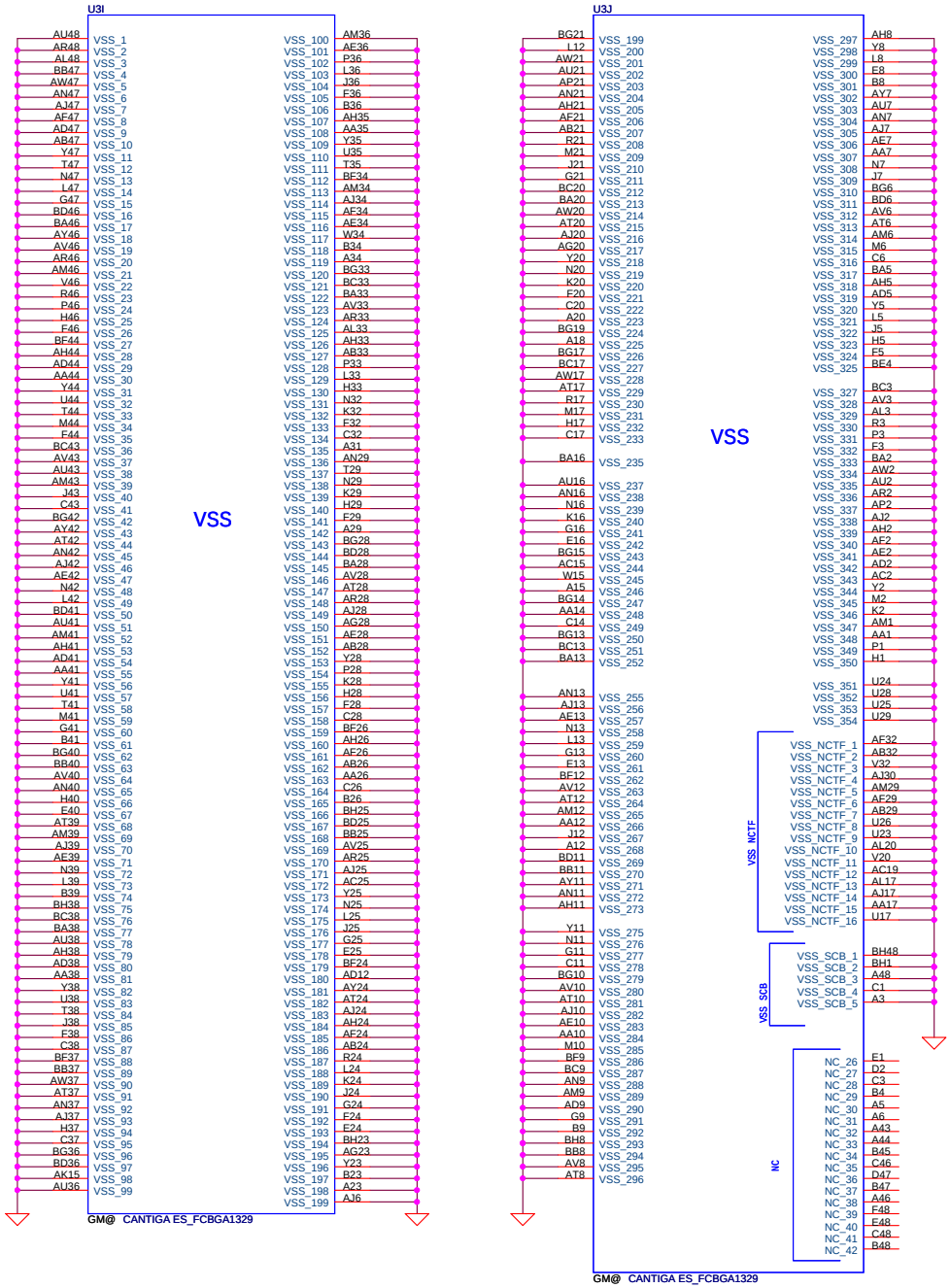
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/07/15	Deciphered Date 2009/07/15	Title: Crestline GMCH (4/6)-VCC
			Size: Custom; Document Number: KHLBX MB Schematic; Rev 1.0
			Date: Monday, January 19, 2009; Sheet 11 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

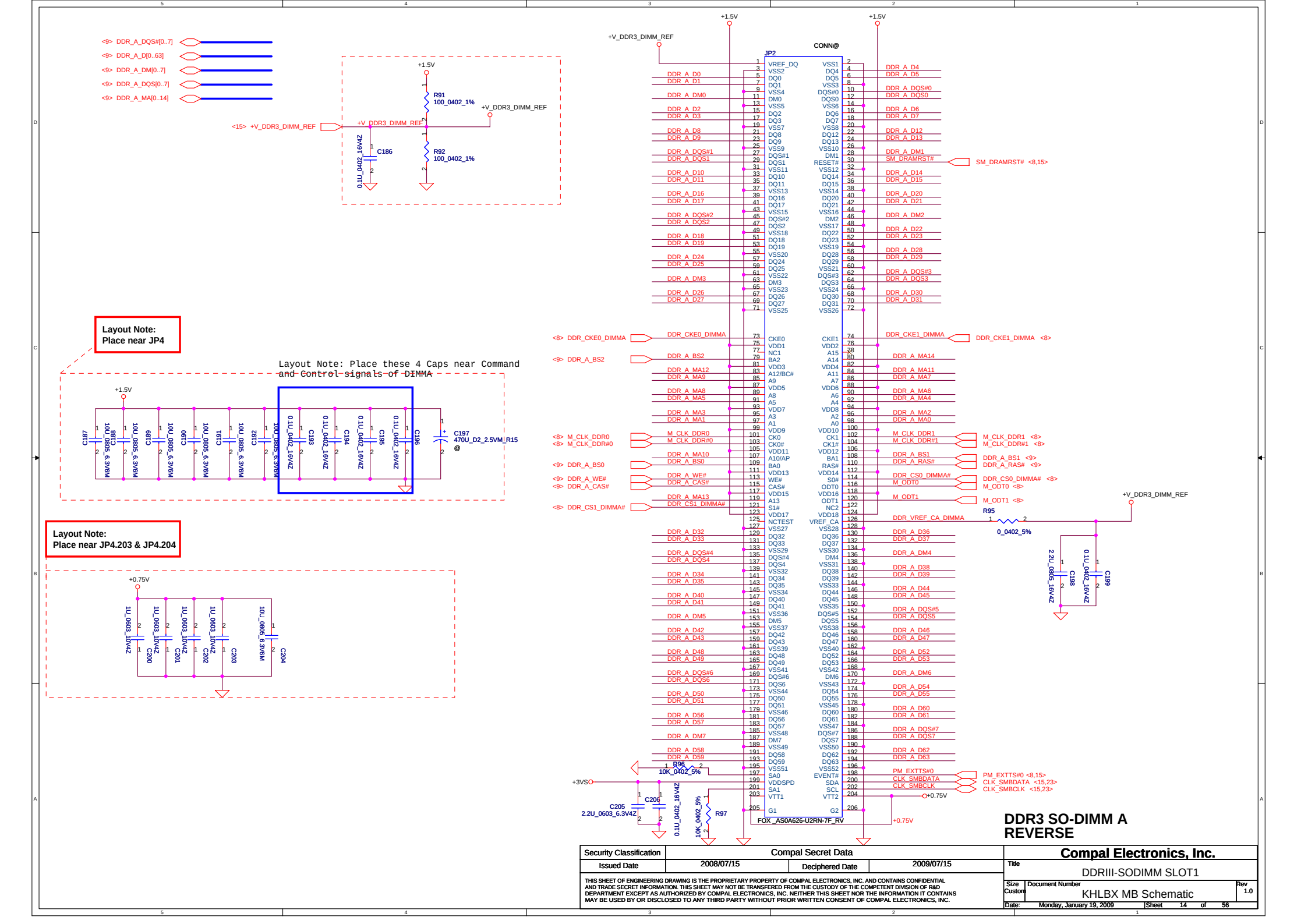
Title	Crestline GMCH (5/6)-VCC
Size: Custom	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 12 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	Cantiga GMCH (6/6)-GND	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 13 of 56	



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Issued Date	2008/07/15	Deciphered Date	2009/07/15

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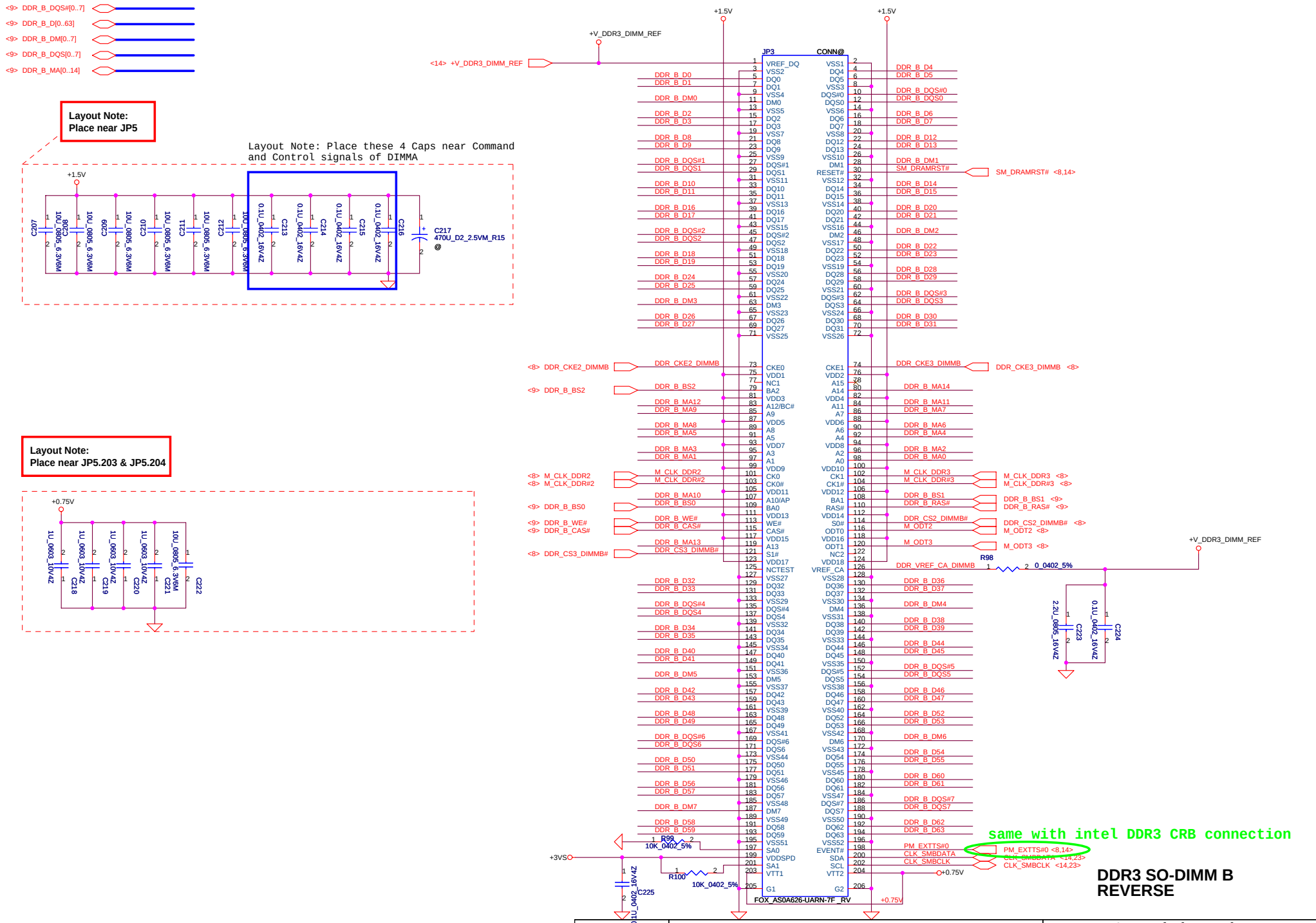
Title	DDRIII-SODIMM SLOT1
Size: Custom	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 14 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

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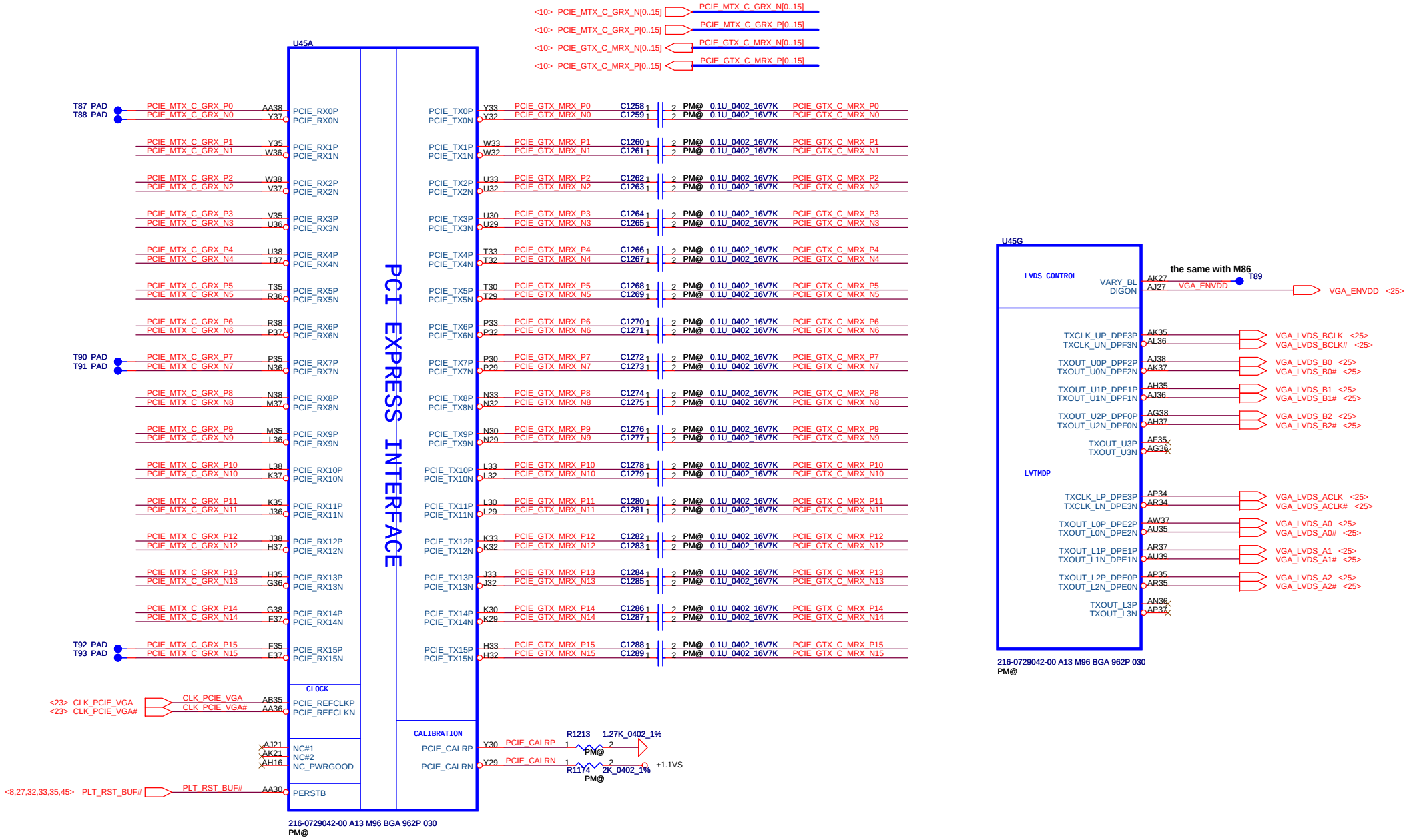
Title	DDRIII-SODIMM SLOT2	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 15 of 56	



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics,Ltd.

Title: M96- PCIE Interface

Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

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Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Saving Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	**Enable CLKREQ# Power Management** 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	**GPIO13,12,11 (config 2,1,0) :** a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	**Enable external BIOS ROM device** 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1 1
CCBYPASS_ SMS_EN_HARD	GENERICC H2SYNC		0 0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

11/12 Add by Vivian

Location / VRAM	MEM_ID0 (R1179)	MEM_ID1 (R1181)	MEM_ID2 (R1183)	MEM_ID3 (R1184)
Samsung	O	O	O	O
Qimonda	1	O	O	O

External VGA Thermal Sensor

+3VS_DELAY, C1290 0.1U_0402_16V4Z PM@, R1175 4.7K_0402_5% PM@, R1176 4.7K_0402_5% PM@, C1291 2200P_0402_50V7K PM@, U46 ADM1032ARMZ-2REEL_MSOP8 (VDD, SCLK, D+, SDATA, D-, ALERT#, THERM#, GND)

EC_SMB_CK2 <5,37>, EC_SMB_DA2 <5,37>, VGA_THERM# <37>

+3VS_DELAY

+3VS_DELAY, 100mA, Q93 SI2301BDS_SOT23 PM@, R1198 100K_0402_5% PM@, R1203 100K_0402_5%, Q94 SSM3K7002FU_SC70-3 PM@, C1293 0.1U_0402_16V4Z PM@, PCIE_OK <53>

PWR Sequence

VGA_CORE (VDDC)
+1.8VS
+3VS_DELAY

U45B

MUTI GFX

DPA: TXCAP_DPA3P AU24, TXCAM_DPA3N AV23, TX0P_DPA2P AT25, TX0M_DPA2N AR24, TX1P_DPA1P AU26, TX1M_DPA1N AV25, TX2P_DPA0P AT27, TX2M_DPA0N AR26
DPB: TXCBP_DPB3P AR30, TXCBM_DPB3N AT29, TX3P_DPB2P AV31, TX3M_DPB2N AU30, TX4P_DPB1P AR32, TX4M_DPB1N AT31, TX5P_DPB0P AT33, TX5M_DPB0N AU32
DPC: TXCCP_DPC3P AU14, TXCCM_DPC3N AV13, TX0P_DPC2P AT15, TX0M_DPC2N AR14, TX1P_DPC1P AU16, TX1M_DPC1N AV15, TX2P_DPC0P AT17, TX2M_DPC0N AR16
DPD: TXCDP_DPD3P AU20, TXCDM_DPD3N AT19, TX3P_DPD2P AT21, TX3M_DPD2N AR20, TX4P_DPD1P AU22, TX4M_DPD1N AV21, TX5P_DPD0P AT23, TX5M_DPD0N AR22

VGA_HDMI_CLK+ <24>, VGA_HDMI_CLK- <24>, VGA_HDMI_TX0+ <24>, VGA_HDMI_TX0- <24>, VGA_HDMI_TX1+ <24>, VGA_HDMI_TX1- <24>, VGA_HDMI_TX2+ <24>, VGA_HDMI_TX2- <24>

DVPCNTL_MVP_0 AR8, DVPCNTL_MVP_1 AU8, DVPCNTL_0 AP8, DVPCNTL_1 AW8, DVPCNTL_2 AR3, DVPCLK AR1
DVPDATA_0 AU1, DVPDATA_1 AU3, DVPDATA_2 AW3, DVPDATA_3 AP6, DVPDATA_4 AW5, DVPDATA_5 AU5, DVPDATA_6 AR6, DVPDATA_7 AW6, DVPDATA_8 AU6, DVPDATA_9 AT7, DVPDATA_10 AV7, DVPDATA_11 AN7, DVPDATA_12 AV9, DVPDATA_13 AT9, DVPDATA_14 AR10, DVPDATA_15 AW10, DVPDATA_16 AU10, DVPDATA_17 AP10, DVPDATA_18 AV11, DVPDATA_19 AT11, DVPDATA_20 AR12, DVPDATA_21 AW12, DVPDATA_22 AU12, DVPDATA_23 AP12

I2C: SCL AK26, SDA AJ26

GENERAL PURPOSE I/O: GPIO_0 AH20, GPIO_1 AH18, GPIO_2 AN16, GPIO_3_SMBDATA AH23, GPIO_4_SMBCLK AJ23, GPIO_5_AC_BATT AH17, GPIO_6 AJ17, GPIO_7_BLON AK17, GPIO_8_ROMSO AJ13, GPIO_9_ROMSI AH15, GPIO_10_ROMSCK AJ16, GPIO_11 AK16, GPIO_12 AL16, GPIO_13 AM16, GPIO_14_HPD2 AM14, GPIO_15_PWRCNTL_0 AM13, GPIO_16_SSIN AK14, GPIO_17_THERMAL_INT AG30, GPIO_18_HPD3 AN14, GPIO_19_CTF AM17, GPIO_20_PWRCNTL_1 AL13, GPIO_21_BB_EN AJ14, GPIO_22_ROMCSB AK13, GPIO_23_CLKREQB AN13, JTAG_TRSTB AM23, JTAG_TDI AN23, JTAG_TCK AK23, JTAG_TMS AL24, JTAG_TDO AM24, GENERICA AJ19, GENERICB AK19, GENERICC AJ20, GENERICD AK20, GENERICE_HPD4 AJ24, GENERICF AH26, GENERICG AH24

HPD1: HDMI_DETECT_VGA AK24

VREFG: VGA_VREF AH13

PLL/CLOCK: DPLL_PVDD AM32, DPLL_PVSS AN32, DPLL_VDDC AN31, XTALIN AV33, XTALOUT AU34

THERMAL: DPLUS AE29, DMINUS AG29, TS_FDO AK32, TSVDD AJ32, TSVSS AJ33

DAC1: R RB AD39 VGA_CRT_R, G GB AE36 VGA_CRT_G, B BB AE37 VGA_CRT_B, HSYNC AC36 VGA_HSYNC, VSYNC AC38 VGA_VSYNC, RSET AB34 R1204 PM@ 499_0402_1%, AVDD AD34 70mA, VDD1DI AC33 42mA

DAC2: R2 R2B AC30, G2 G2B AC31, B2 B2B AD30, C Y COMP AD31, H2SYNC AE30, V2SYNC AE31, VDD2DI AC32 40mA, A2VDD AE32 65mA, A2VDDQ AD32, A2VSSQ AE33, R2SET AA29 R1212 15_0402_1% PM@

DDC/AUX: DDC1CLK AM26 VGA_DDC_CLK, DDC1DATA AN26 VGA_DDC_DATA CRT; AUX1P AM27, AUX1N AL27; DDC2CLK AM19 VGA_HDMI_SCL, DDC2DATA AL19 VGA_HDMI_SDA HDMI; AUX2P AN20, AUX2N AM20; DDCCLK_AUX3P AL30, DDCDATA_AUX3N AM30; DDCCLK_AUX4P AL29, DDCDATA_AUX4N AM29; DDCCLK_AUX5P AN21, DDCDATA_AUX5N AM21; DDC6CLK AJ30, DDC6DATA AJ31; NC_DDCCLK_AUX7P AK30, NC_DDCDATA_AUX7N AK29

216-0729042-00 A13 M96 BGA 962P 030 PM@

Pull Low at LVDS side

+3VS_DELAY, +1.8VS, X76_QIM@

R1177 PM@ 10K_0402_5% VGA_GPIO0
R1178 PM@ 10K_0402_5% VGA_GPIO1
@R1180 10K_0402_5% VGA_GPIO2
@R1182 10K_0402_5% SOUT_GPIO8 — for use SBIOS
@R1185 10K_0402_5% SIN_GPIO9
R1186 PM@ 10K_0402_5% VGA_GPIO11
@R1187 10K_0402_5% VGA_GPIO12
@R1188 10K_0402_5% VGA_GPIO13
R1190 PM@ 10K_0402_5% VGA_VSYNC
R1192 PM@ 10K_0402_5% VGA_HSYNC
@R1193 10K_0402_5% V2SYNC
@R1194 10K_0402_5% H2SYNC
@R1195 10K_0402_5% ROMSE_GPIO22
@R1197 10K_0402_5% GENERICC
@R1199 10K_0402_5% VGA_AC_DET_R
@R1202 10K_0402_5% VGA_ENBKL <37> VGA_AC_DET

R1179 PM@ 10K_0402_5% MEM_ID0
R1181 1 @ 2 10K_0402_5% MEM_ID1
R1183 1 @ 2 10K_0402_5% MEM_ID2
R1184 1 @ 2 10K_0402_5% MEM_ID3

CRB recommend 4.7Kohm
R1191 4.7K_0402_5% PM@, R1189 4.7K_0402_5% PM@

<25> VGA_LVDS_SCL, <25> VGA_LVDS_SDA

10/22 Add by Vivian

EC_SMB_DA2 R1316 0_0402_5% SMB_DA, EC_SMB_CK2 R1315 0_0402_5% SMB_CK
VGA_AC_DET R1308 0_0402_5%
Risk for EC control
<25> VGA_ENBKL

VGA_GPIO0 AH20, VGA_GPIO1 AH18, VGA_GPIO2 AN16, VGA_GPIO11 AH16, VGA_GPIO12 AL16, VGA_GPIO13 AM16, SOUT_GPIO8 AJ13, SIN_GPIO9 AJ15

M96 can not support

+3VS_DELAY, R1205 10K_0402_5% VGA_THERM#, @R1206 10K_0402_5%, @R1207 10K_0402_5% CLKREQ_GPIO23

<53> GPU_VID0, GPU_VID0, VGA_THERM#
<53> GPU_VID1, <19> VGA_GPIO21, GPU_VID1, VGA_GPIO21, ROMSE_GPIO22, CLKREQ_GPIO23

Check

10/31 Add

100P_0402_50V8J C1662 GPU_VID1
<20> GENERICB, GENERICB, GENERICC

Change R1211 part number from SD034499080 to SD034249080

XTALIN, XTALOUT, R1208 1M_0603_5% PM@, R1209 @ 75_0402_1%, Y4 27MHz_16PF_6P27000126 (GND, OUT, IN, GND), C1302 18P_0402_50V8J PM@, C1303 18P_0402_50V8J PM@

+1.8VS, R1210 499_0402_1% PM@, R1211 249_0402_1% PM@, C1307 0.1U_0402_16V4Z PM@

+1.8VS, BLM18PG121SN1D_0603 L86 PM@, 0.1U_0402_16V4Z, DPLL_PVDD, 120mA
C1310 C1311 C1312 10U_0603_6.3V6M PM@, 1U_0402_6.3V4Z

+1.1VS, BLM18PG121SN1D_0603 L87 PM@, 0.1U_0402_16V4Z, DPLL_VDDC, 300mA
C1313 C1314 C1315 10U_0603_6.3V6M PM@, 1U_0402_6.3V4Z

+1.8VS, BLM18PG121SN1D_0603 L88 PM@, 1U_0402_6.3V4Z, TSVDD, 20mA
C1318 C1319 10U_0603_6.3V6M PM@

CRT

VGA_CRT_R <26>, VGA_CRT_G <26>, VGA_CRT_B <26>
R1196 150_0402_1% PM@, R1200 150_0402_1% PM@, R1201 150_0402_1% PM@

HDMI

VGA_HDMI_SCL <24>, VGA_HDMI_SDA <24>

AVDD: 0.1U_0402_16V4Z, L81 BLM18PG121SN1D_0603 PM@, +1.8VS; C1294 PM@ 1U_0402_6.3V4Z, C1295 PM@, C1296 PM@ 10U_0603_6.3V6M
VDD1DI: 0.1U_0402_16V4Z, L82 BLM18PG121SN1D_0603 PM@, +1.8VS; C1297 PM@ 1U_0402_6.3V4Z, C1298 PM@
VDD2DI: L83 PM@ 0_0603_5% +1.8VS
A2VDD: L84 PM@ 0_0603_5% +3VS_DELAY
A2VDDQ: L85 PM@ 0_0603_5% +1.8VS

+3VS_DELAY, R1216 10K_0402_5% PM@, R1217 10K_0402_5% PM@, VGA_DDC_CLK, VGA_DDC_DATA <26>
+3VS_DELAY, R1218 10K_0402_5% PM@, R1219 10K_0402_5% PM@, VGA_HDMI_SCL <24>, VGA_HDMI_SDA <24>

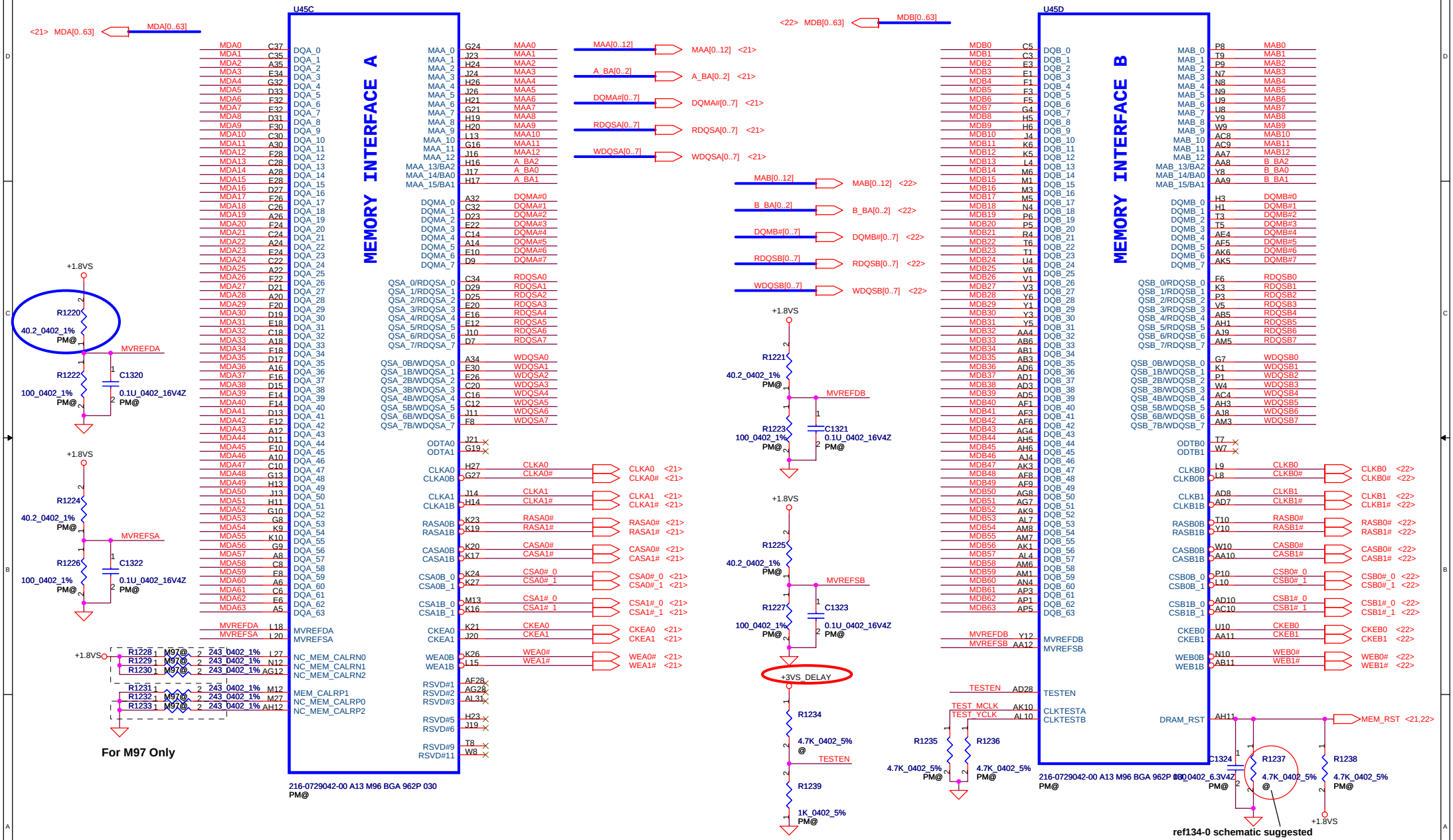
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: M96 PCIE,LVDS,GPIO,CLK

Size: C | Document Number: KHLBX MB Schematic | Rev: 1.0

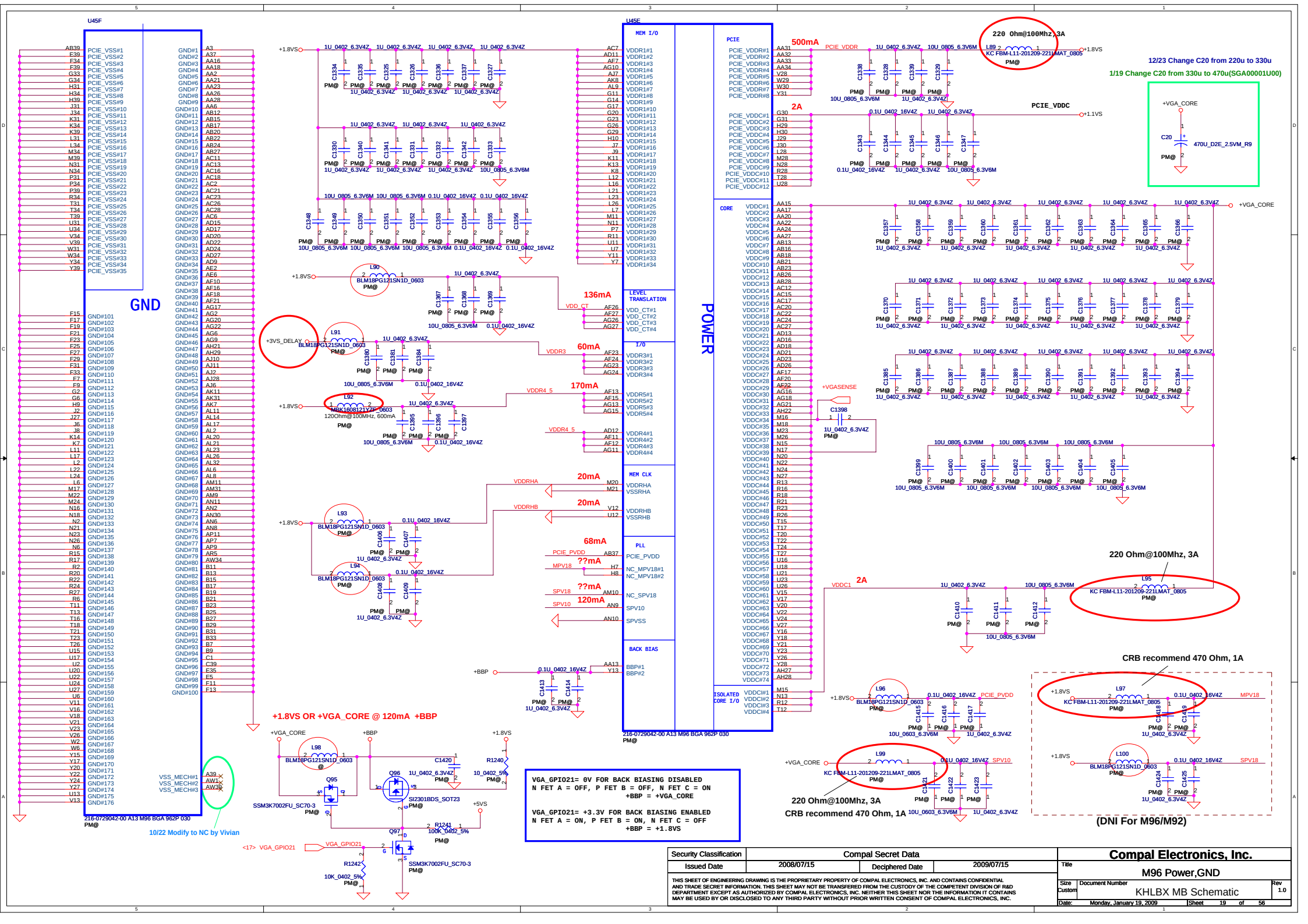
Date: Monday, January 19, 2009 | Sheet 17 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

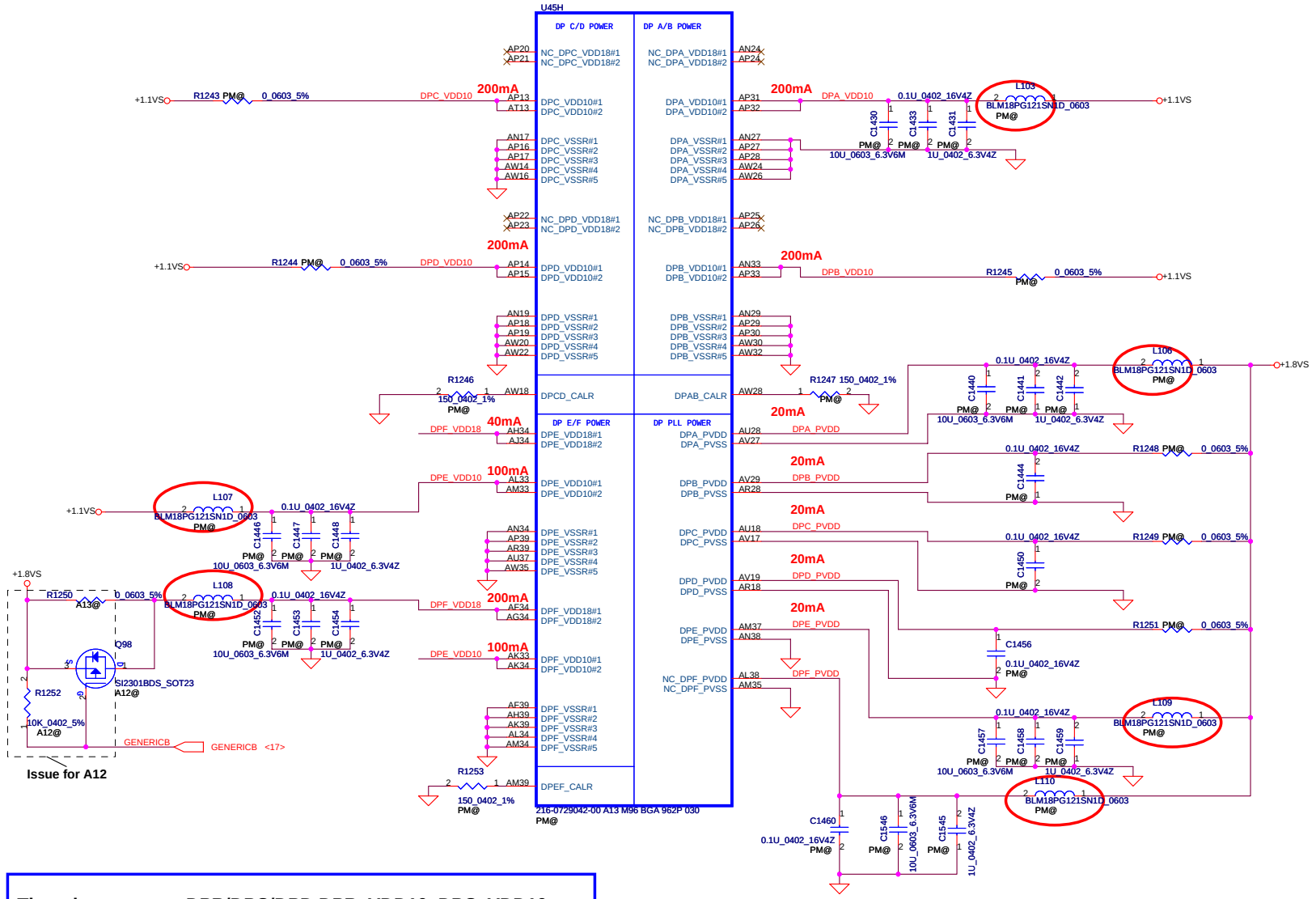
Title	M96 Memory	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 18 of 56	



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	M96 Power,GND	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 19 of 56	

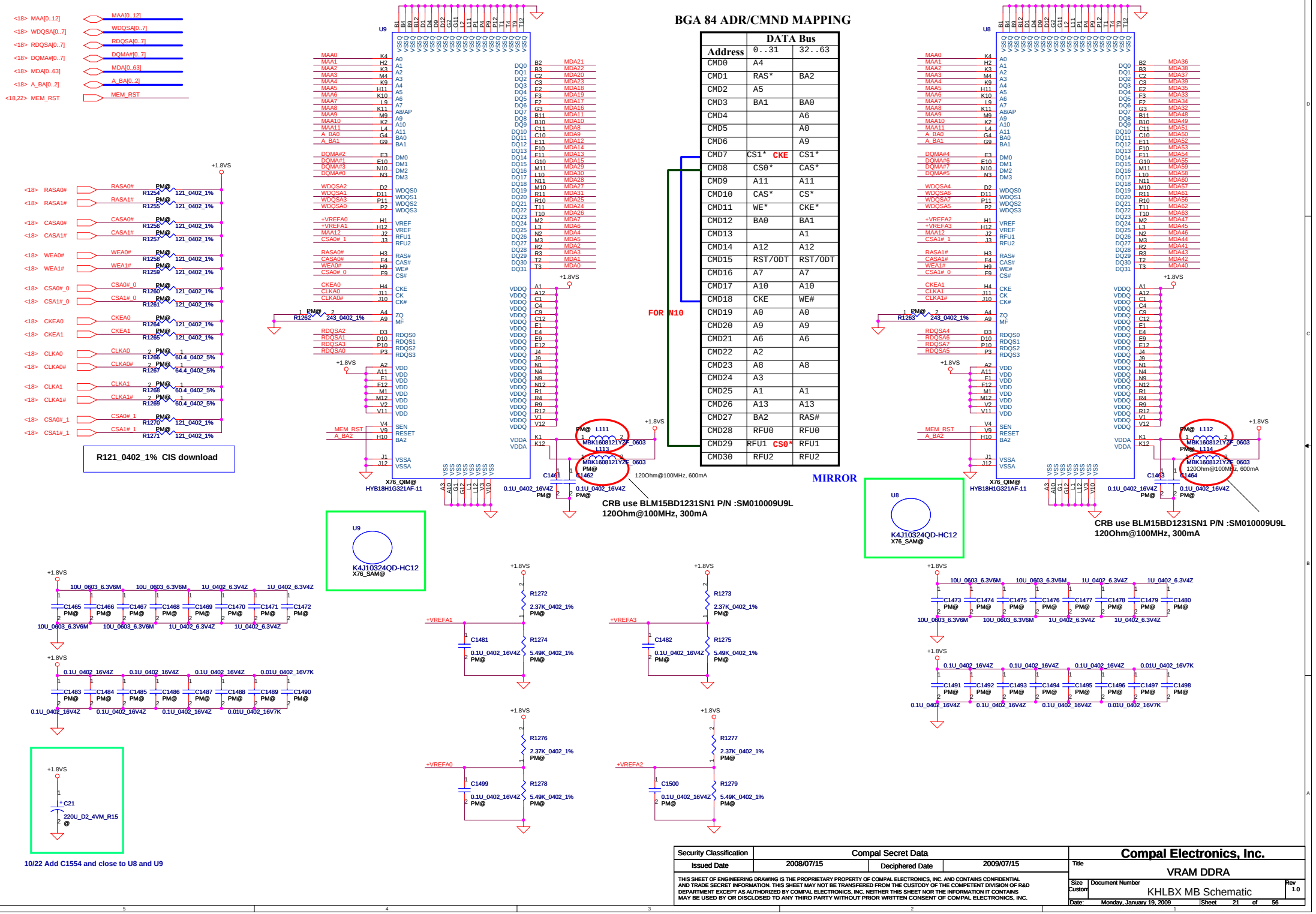


There is no use on DPB/DPC/DPD,DPB_VDD10, DPC_VDD10, DPD_VDD10, DPB_PVDD, DPC_PVDD and DPD_PVDD can be powered without filter

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics,Ltd.

Title	M96	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 20 of 56	



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: VRAM DDRA

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 21 of 56

BGA 84 ADR/CMND MAPPING

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	A4	
CMD1	RAS*	BA2
CMD2	A5	
CMD3	BA1	BA0
CMD4		A6
CMD5		A0
CMD6		A9
CMD7	CS1* CKE	CS1*
CMD8	CS0*	CAS*
CMD9	A11	A11
CMD10	CAS*	CS*
CMD11	WE*	CKE*
CMD12	BA0	BA1
CMD13		A1
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	WE#
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	RAS#
CMD28	RFU0	RFU0
CMD29	RFU1 CS0*	RFU1
CMD30	RFU2	RFU2

FOR N10

MIRROR

CRB recommend 60.4 ohm

R121_0402_1% CIS download

CRB use BLM15BD1231SN1 P/N :SM010009U9L
120Ohm@100MHz, 300mA

CRB use BLM15BD1231SN1 P/N :SM010009U9L
120Ohm@100MHz, 300mA

10/22 Add C1555 and close to U10 and U11

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

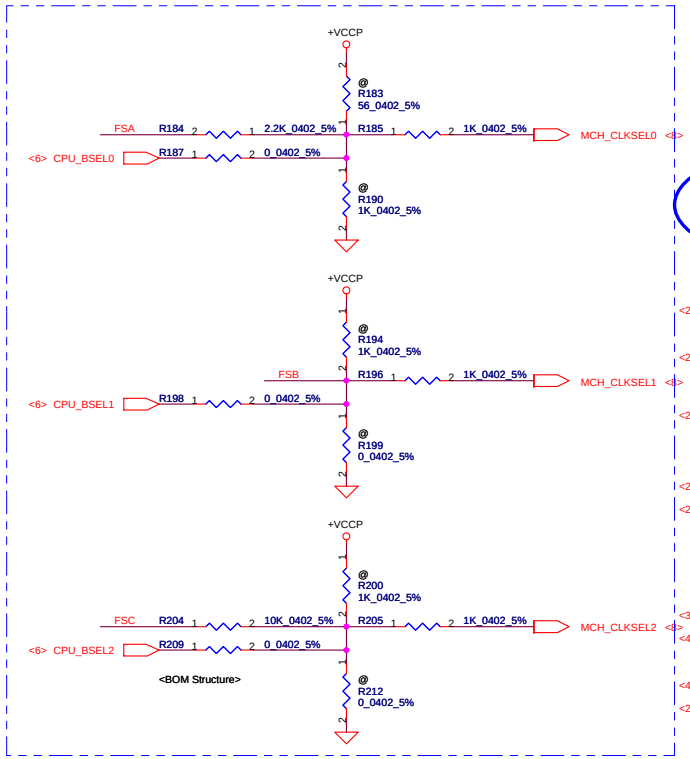
Title: VRAM DDRA

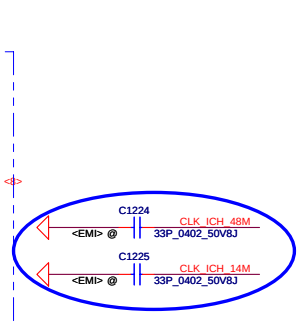
Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

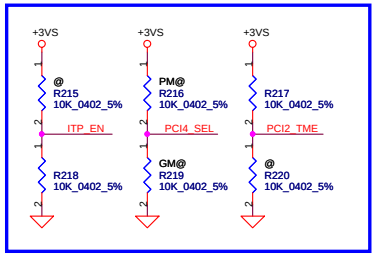
Date: Monday, January 19, 2009 | Sheet 22 of 56

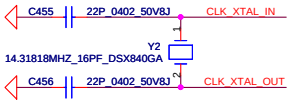
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

***SA000020H10 (ICS : ICS9LPRS387BKLFT)**
SA000020K00 (Silego : SLG8SP556VTR)

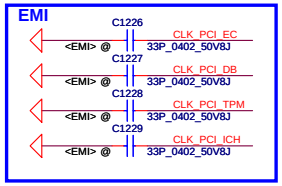






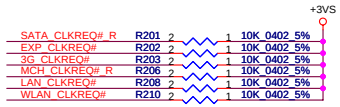


Routing the trace at least 10mil



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_CARD
SRC6	PCIE_WLAN
SRC7	PCIE_3G
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

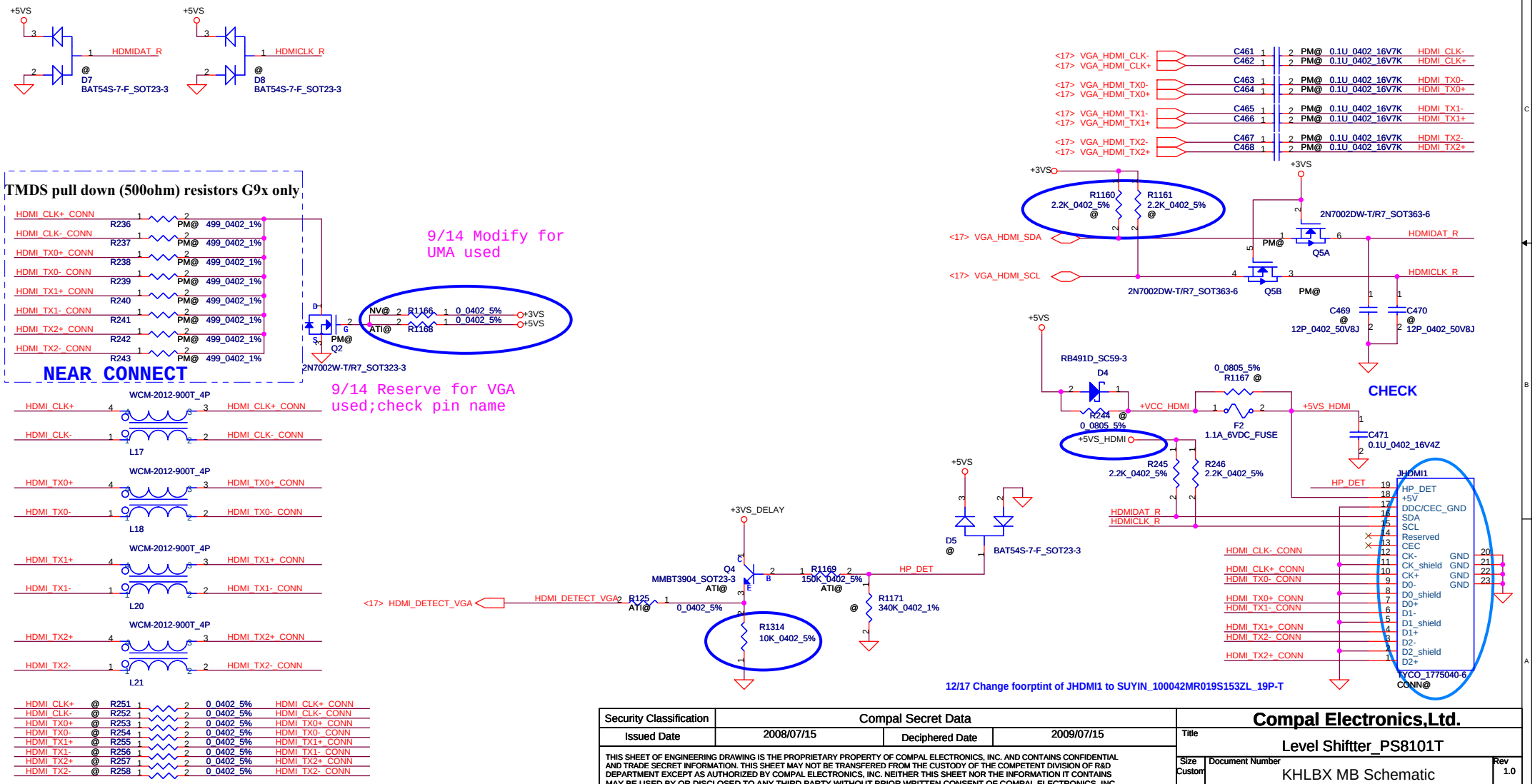
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_3G
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics,Ltd.

Title	Clock Generator CK505		
Size: Custom	Document Number: KHLBX MB Schematic		Rev: 1.0
Date: Monday, January 19, 2009		Sheet 23 of 56	



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

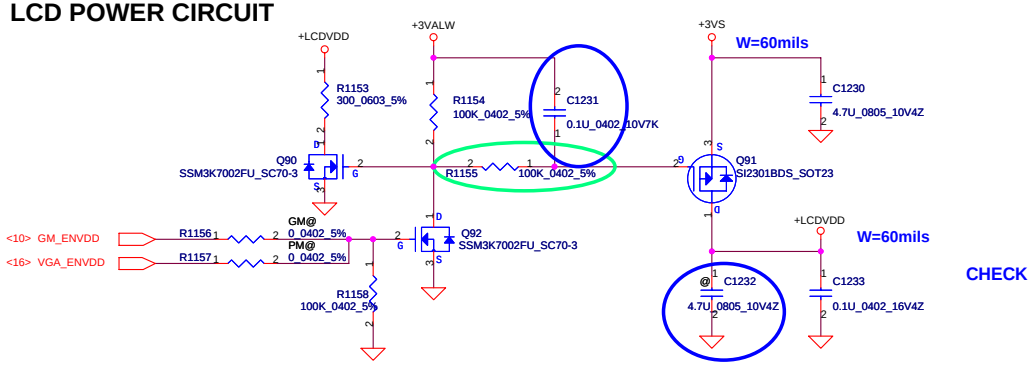
Compal Electronics,Ltd.

Title: Level Shiftter_PS8101T

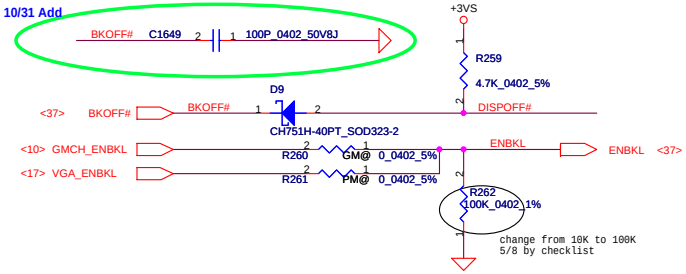
Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

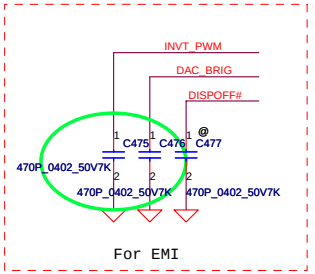
Date: Monday, January 19, 2009 | Sheet 24 of 56

LCD POWER CIRCUIT



CHECK

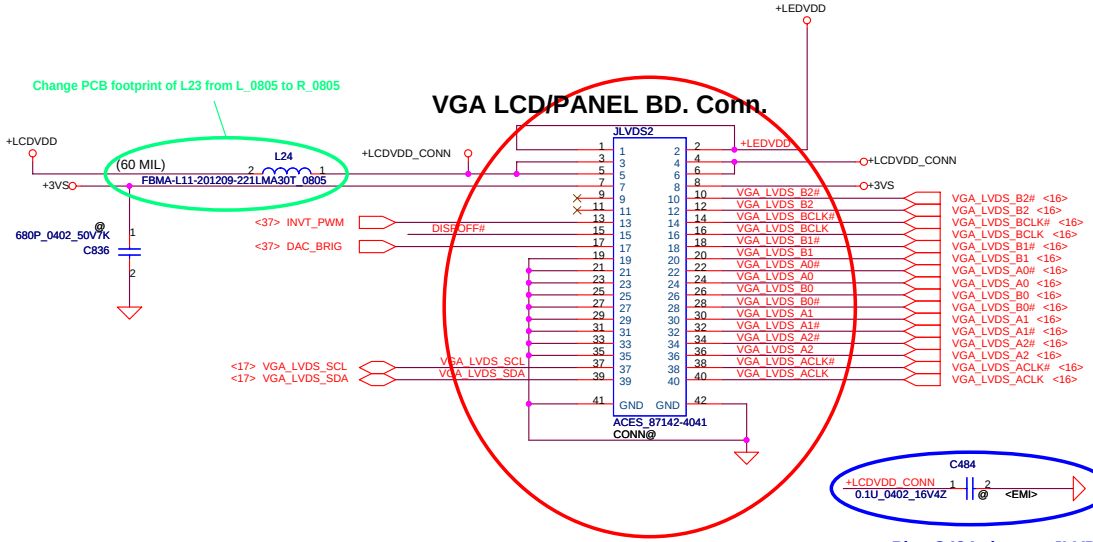




Change PCB footprint of L22 from L_0805 to R_0805

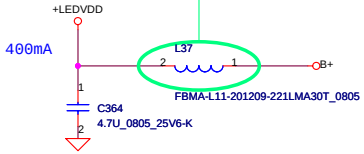
Change PCB footprint of L23 from L_0805 to R_0805

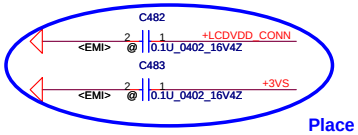
VGA LCD/PANEL BD. Conn.



Plac C484 close to JLVDS2

Change PCB footprint of L37 from L_0805 to R_0805





Place C483 and C482 close to JLVDS3

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

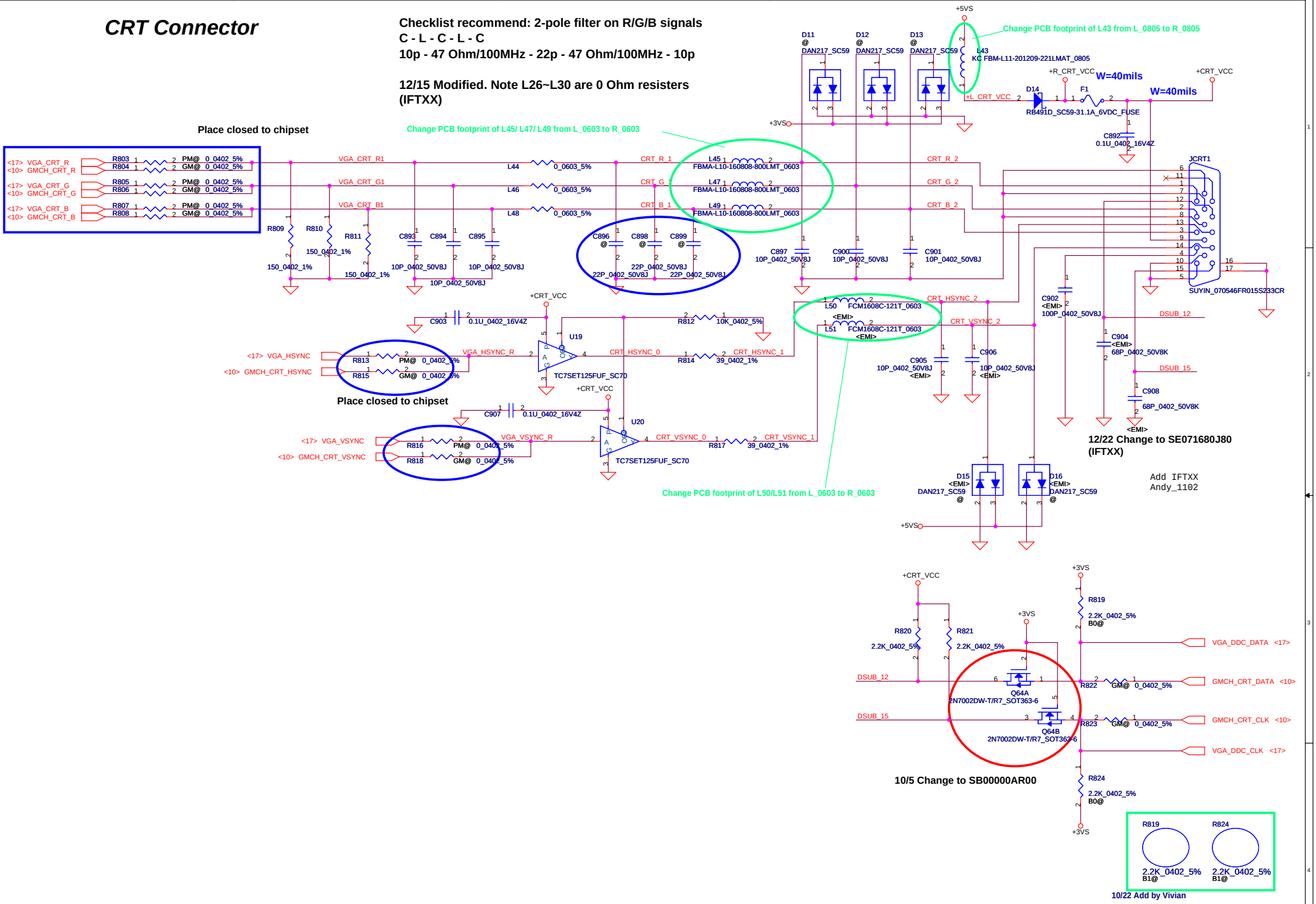
Compal Electronics, Inc.

Title	LVDS & DVI Connector
Size B	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 25 of 56

CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resisters (IFTXX)



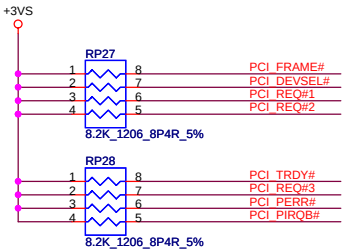
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

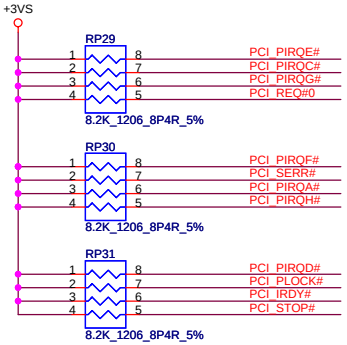
Compal Electronics, Inc.

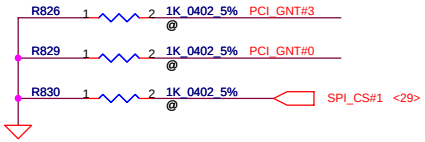
Title: CRT Connector

Size: B | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 26 of 56







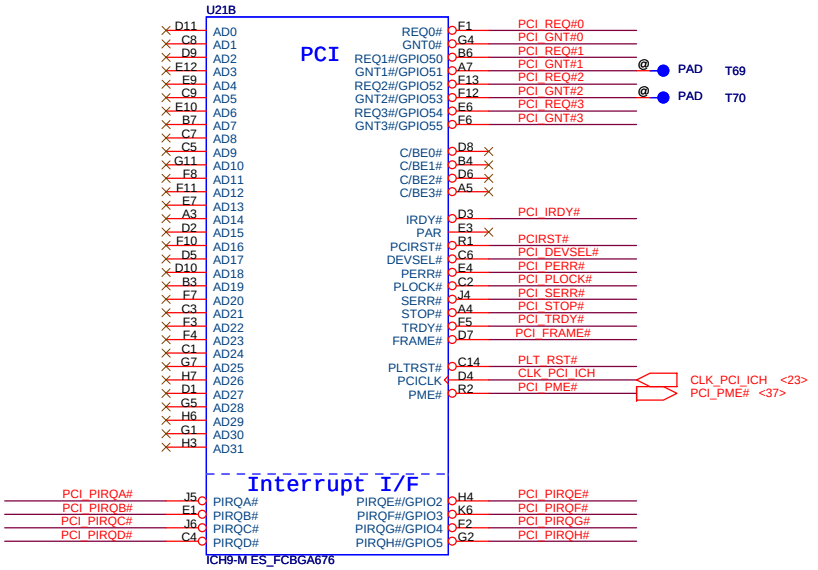
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

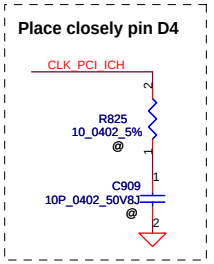
CRB: GNT#0 and SPI_CS#1 have a weak internal pull up

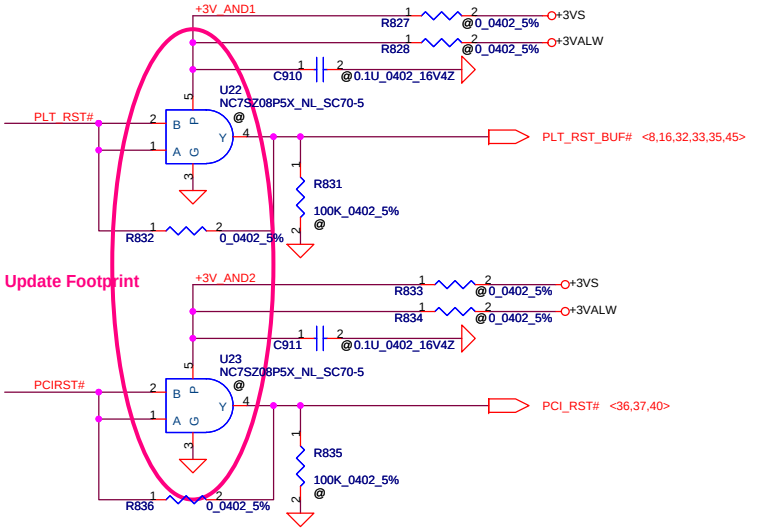
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

9/18 Change U21 from SA00002JH00 to SA00002JH80







Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

Size	Document Number	Rev
B	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 Sheet 27 of 56

12/7 Modified X4 to SJ100001U00 10ppm

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

close to RAM door

close to RAM door

Need check

CHECK

12/8 Add by Vivian
12/8 Close to RAM socket.

SATA HDD

SATA ODD

SATA ODD

close ICH9

R308 need to place within 2" of ICH9M
R310 must be place within 2" of R308 w/o stub.

4mils width less than 500mils

Need check

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

RTC Battery

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

9/29 modified to follow ISKAA

9/29 Checked. Same as HEL80's

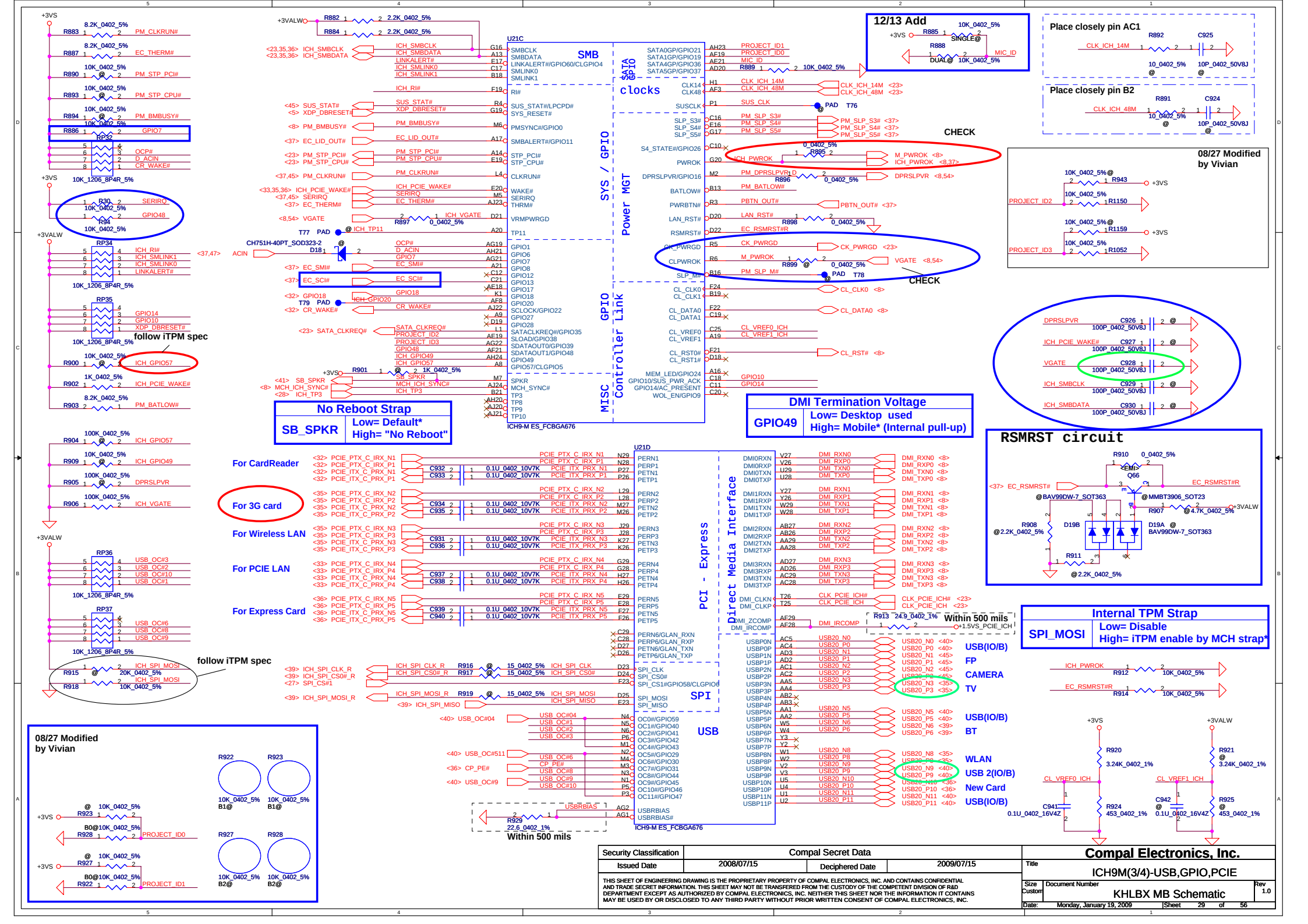
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/7/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 28 of 56


12/13 Add
Place closely pin AC1
Place closely pin B2
08/27 Modified by Vivian
CHECK
CHECK
follow iTPM spec
follow iTPM spec
No Reboot Strap
SB_SPKR
Low= Default*
High= "No Reboot"
DMI Termination Voltage
GPIO49
Low= Desktop used
High= Mobile* (Internal pull-up)
RSMRST circuit
Internal TPM Strap
SPI_MOSI
Low= Disable
High= iTPM enable by MCH strap*
Within 500 mils
Within 500 mils
For CardReader
For 3G card
For Wireless LAN
For PCIE LAN
For Express Card
USB(IO/B)
FP
CAMERA
TV
USB(IO/B)
BT
WLAN
USB 2(IO/B)
New Card
USB(IO/B)
SMB
clocks
SYS / GPIO
Power MGT
GPIO
Controller Link
MISC
PCI - Express
Direct Media Interface
SPI
USB
ICH9-M ES_FCBGA676
Compal Electronics, Inc.
ICH9M(3/4)-USB,GPIO,PCIE
KHLBX MB Schematic
Rev 1.0
Monday, January 19, 2009
Sheet 29 of 56
Compal Secret Data
2008/07/15
2009/07/15
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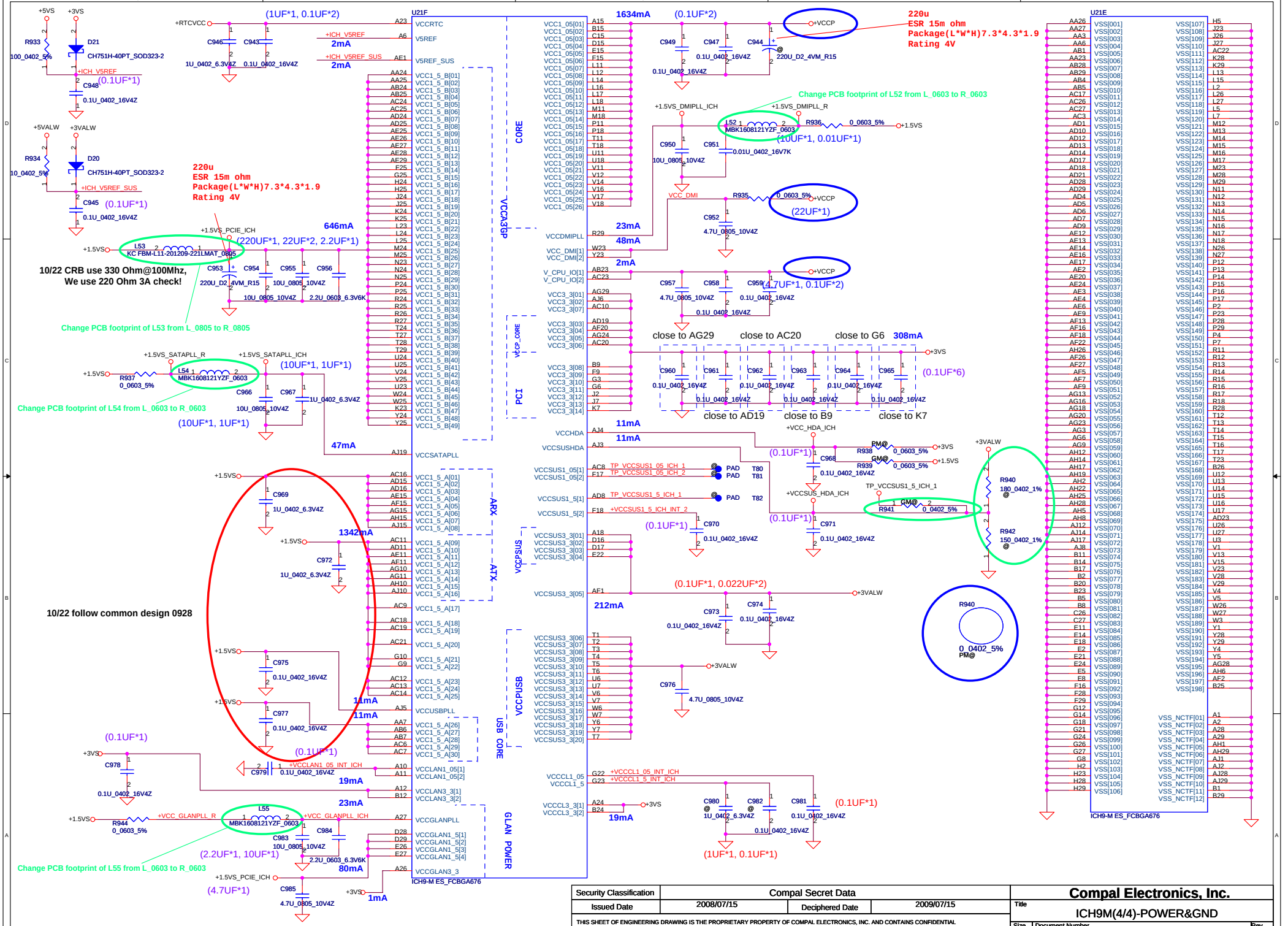
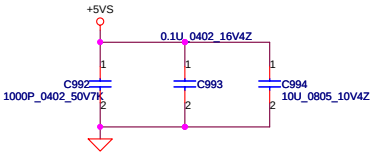


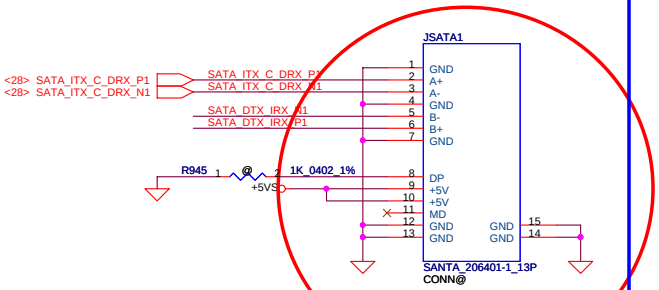
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	ICH9M(4/4)-POWER&GND
Size: Custom	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 30 of 56

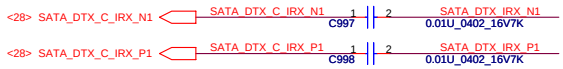
SATA ODD Conn.





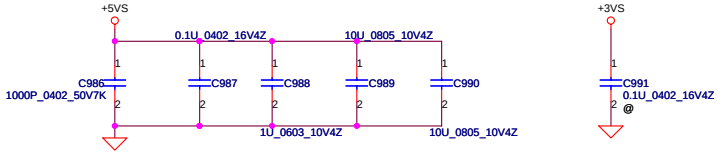
Copy JAL90 Symbol

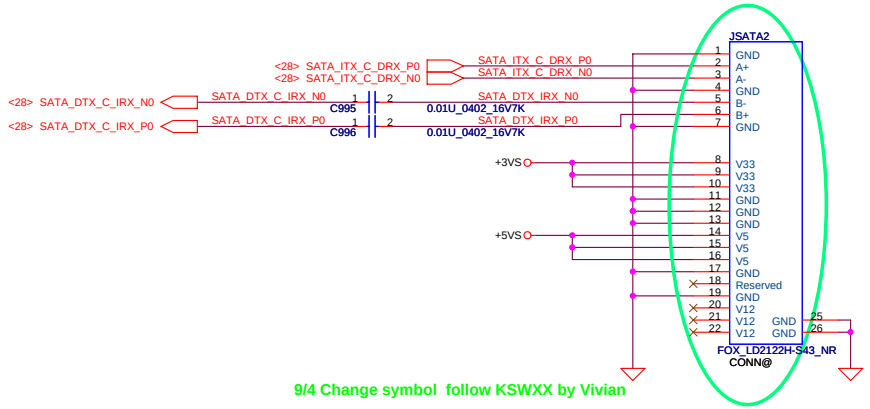
Change ODD connector from OCTEK_SLS-13SB1G to SANTA_206401-1_13P



Need check layout !!

SATA HDD Conn.





9/4 Change symbol follow KSWXX by Vivian

(NEW)

Change Library

Update Symbol
SP01000G800
FOX_LD2122H-S43_NR

Manually update pin number

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	HDD & ODD Connector	
Size B	Document Number KHLBX MB Schematic	Rev 1.0
Date: Monday, January 19, 2009	Sheet 31 of 56	

Use 0805 type and over 20 mils
trace width on both side

mount JMB suggest

Active High EN
11/24 Andy

40mil

reserved power circuit

Refer JMB suggest 11/14

SD,MMC,MS muti-function pin define

MDIO PIN Name	SD/MMC Card PIN Name	MS Card PIN Name
MDIO00	SD1_DAT0	MS1_DAT0
MDIO01	SD1_DAT1	MS1_DAT1
MDIO02	SD1_DAT2	MS1_DAT2
MDIO03	SD1_DAT3	MS1_DAT3
MDIO04	SD1_CMD	MS1_BS
MDIO05	SD1_CLK	MS1_CLK
MDIO06	SD1_WP	
MDIO07		
MDIO08	MMC_DAT4	MS1_DAT4
MDIO09	MMC_DAT5	MS1_DAT5
MDIO10	MMC_DAT6	MS1_DAT6
MDIO11	MMC_DAT7	MS1_DAT7
MDIO12		
MDIO13		
MDIO14		
CR1_LEDN	SD1_LED#	MS1_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#
CR1_CD0	SD1_CD#	
CR1_CD1		MS1_CD#

20mil

40 mil

10/23 Change net name to +3VS_CR by Vivian

10/23 Add by Vivian

W=40mils

12mil,length <250 mil

Refer JMB suggest 11/09

Change Pin definition for Rev:B

JMB385

Damping need to close to IC

Strap pin for JMicro

Refer JMB suggest 11/09

3 in 1 Card Reader

Rev :B

W=40mils

The circuit need reserve for JMB385?

10/17 add for
JMB380

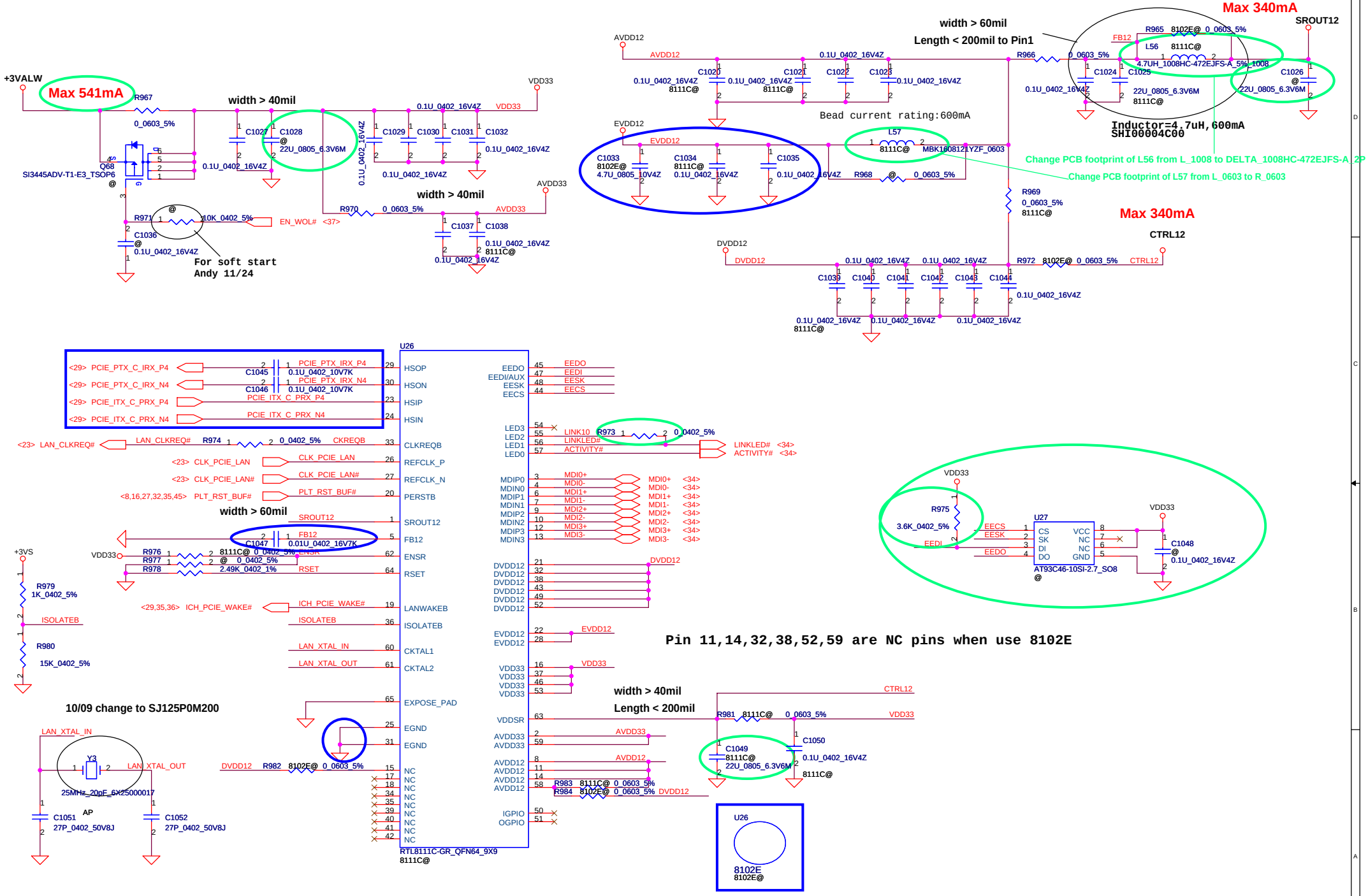
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: JMB385 CardReader

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

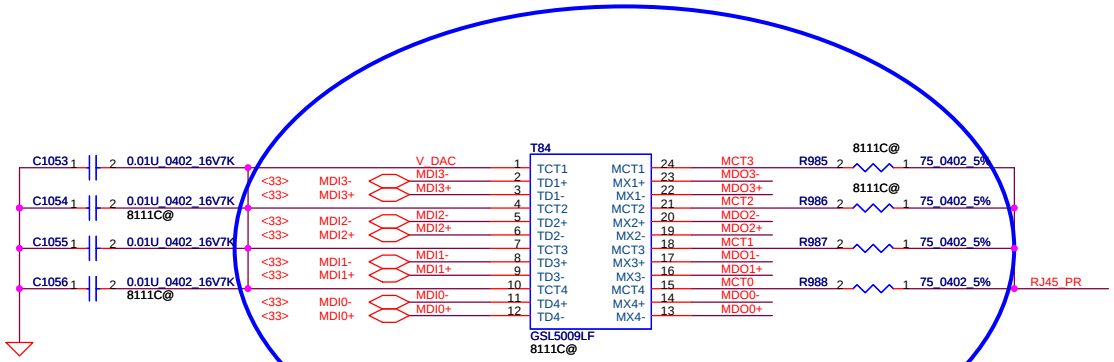
Date: Monday, January 19, 2009 | Sheet 32 of 56



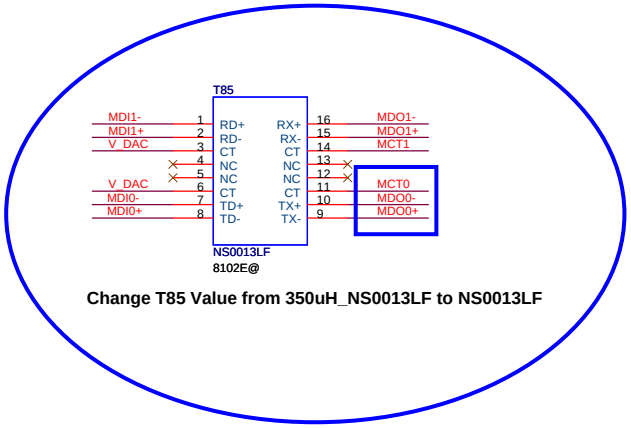
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	LAN-RTL8111C/RTL8102E
Size: Custom	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 33 of 56

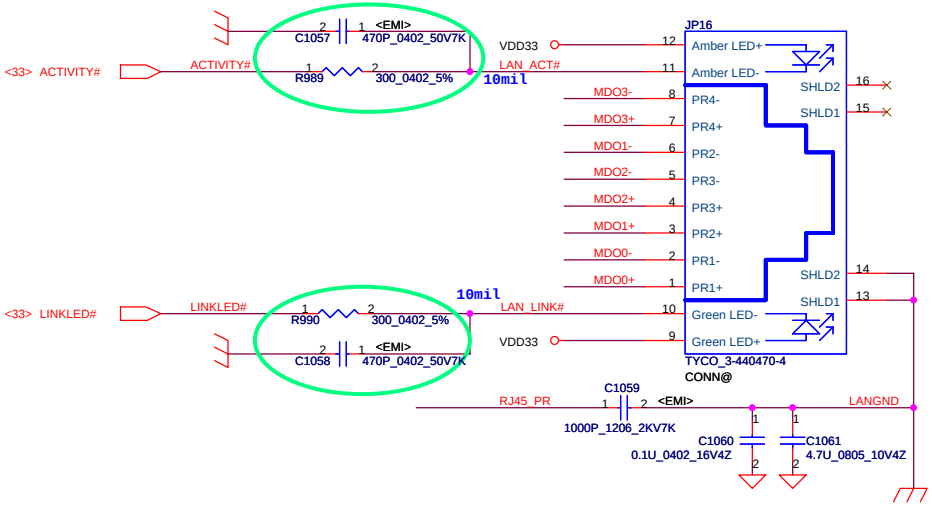


9/18 Change T84 Value from 350uH_GSL5009LF to GSL5009LF
Change T84 P/N fromSP050003T00 to SP050003T10



Change T85 Value from 350uH_NS0013LF to NS0013LF

Lan Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

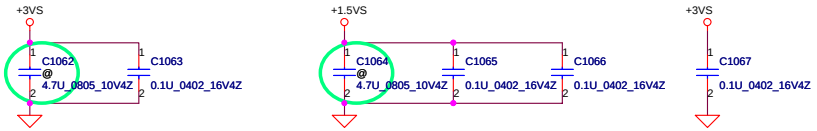
Compal Electronics, Inc.

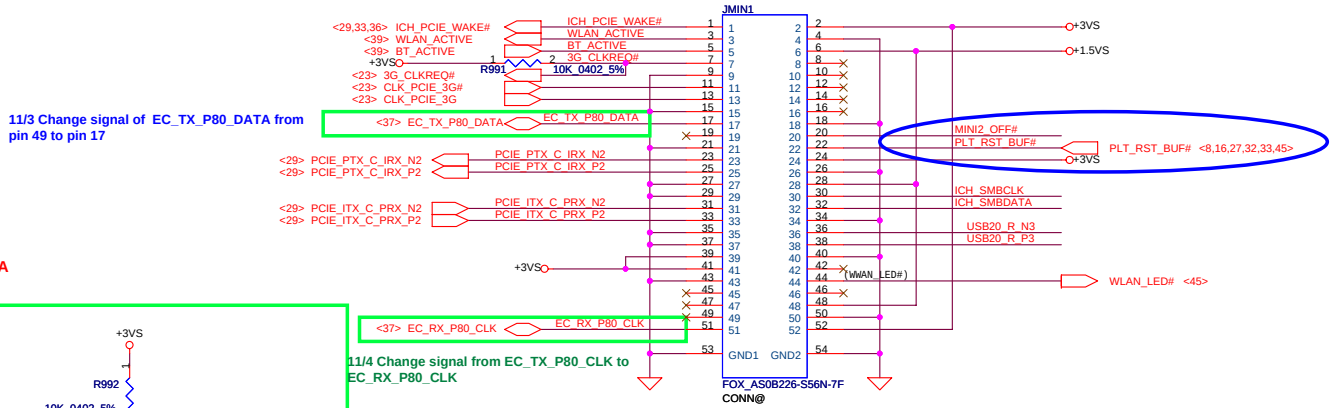
Title: LAN CONNECTOR

Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

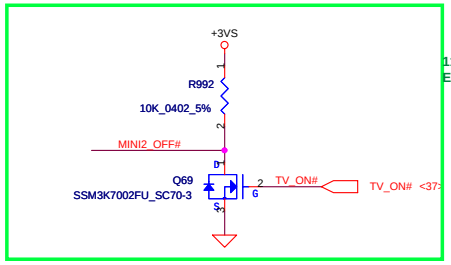
Date: Monday, January 19, 2009 Sheet 34 of 56

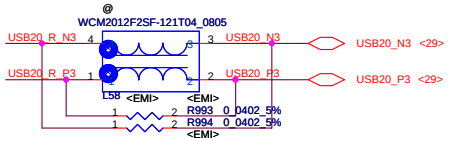
Mini-Express Card for TV Tuner



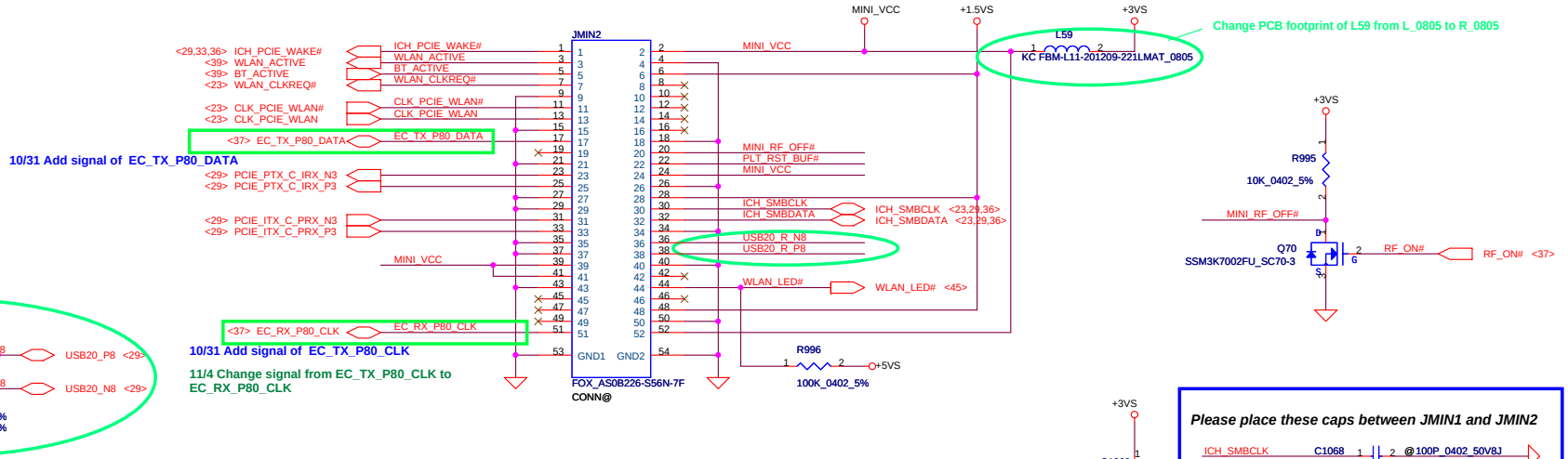


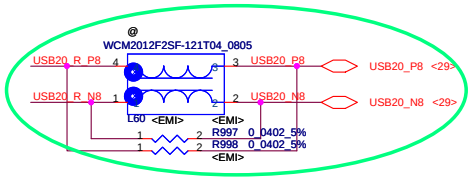
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

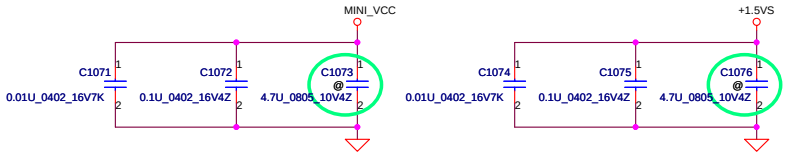


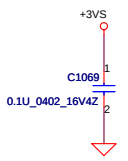


Mini-Express Card for WLAN

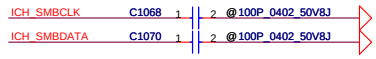








Please place these caps between JMIN1 and JMIN2



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

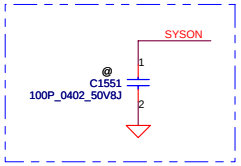
Compal Electronics, Inc.

Title: Mini-Card/Kill SWITCH

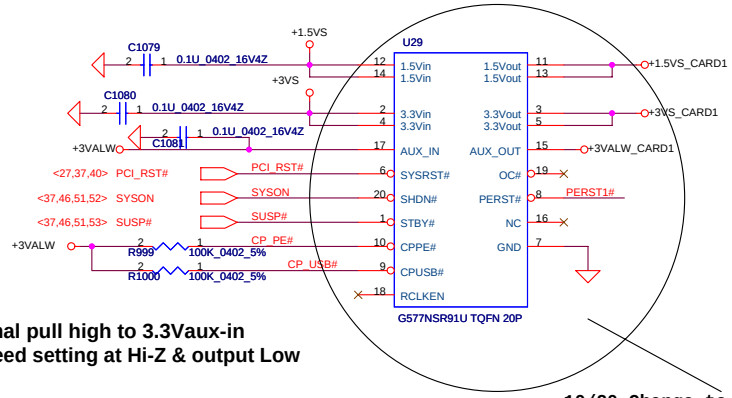
Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 | Sheet 35 of 56

New Card Power Switch

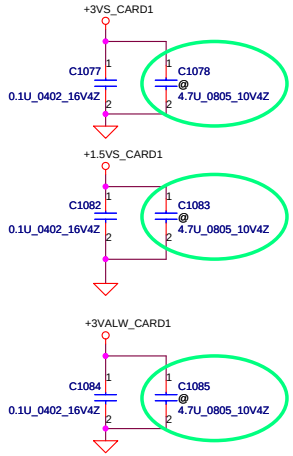


New Card



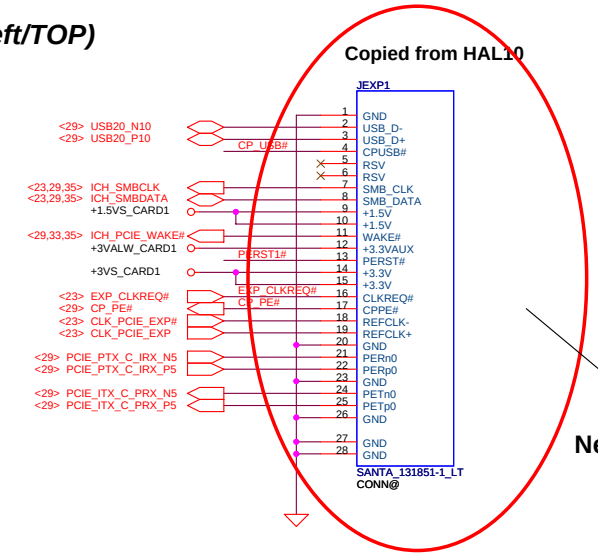
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

10/20 Change to value to G577NSR91U TQFN 20P



New Card Socket (Left/TOP)

Copied from HAL10



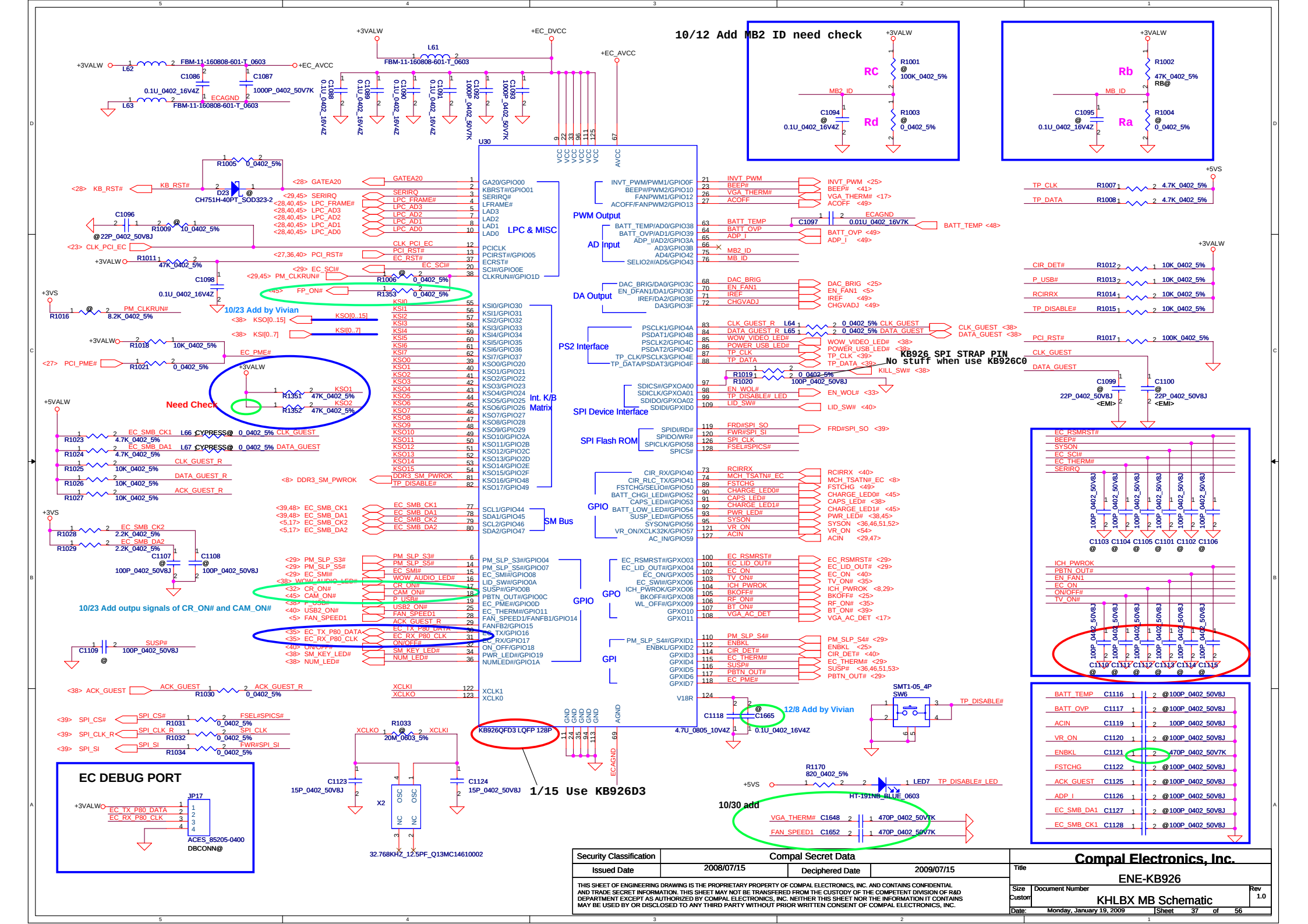
Need checking layout !!

Change connector from SANTA_130810-1 to SANTA_13185-1_LT

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	NEW CARD	
Size B	Document Number KHLBX MB Schematic	Rev 1.0
Date: Monday, January 19, 2009	Sheet 36 of 56	



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: ENE-KB926

Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

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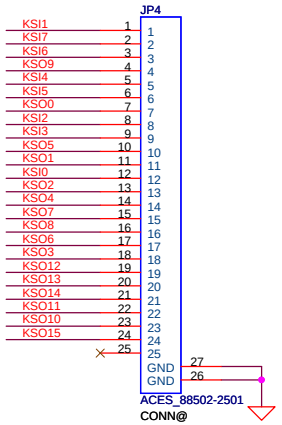
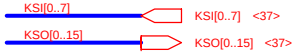
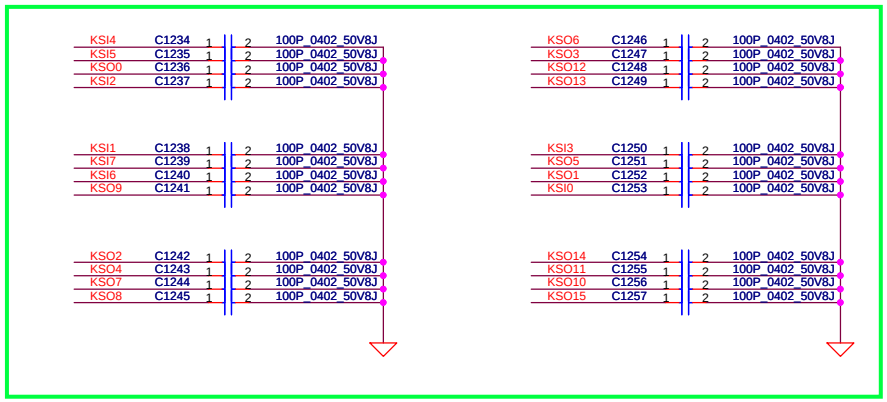
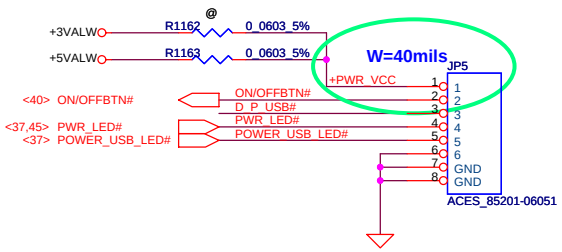
INT_KBD Conn.

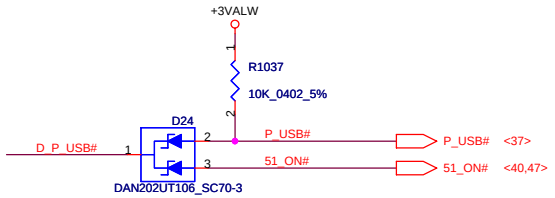




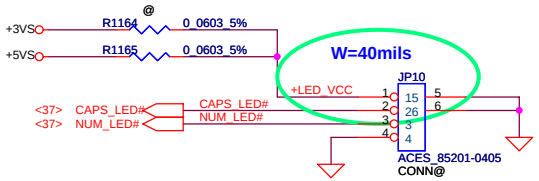


Power USB Board Conn

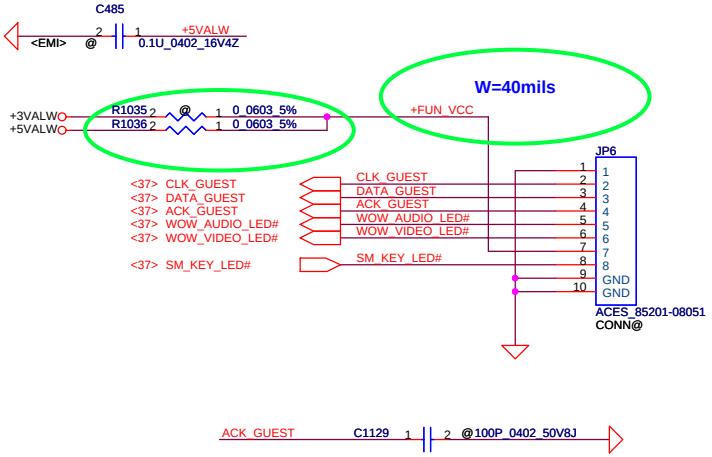




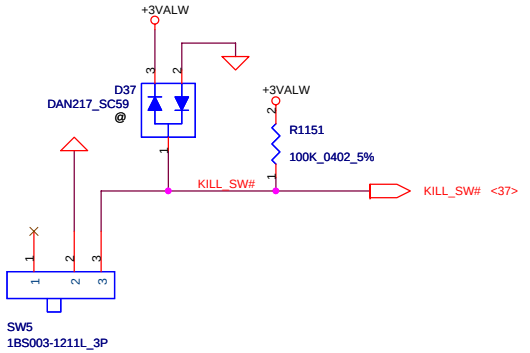
LED Board Conn



Fun conn



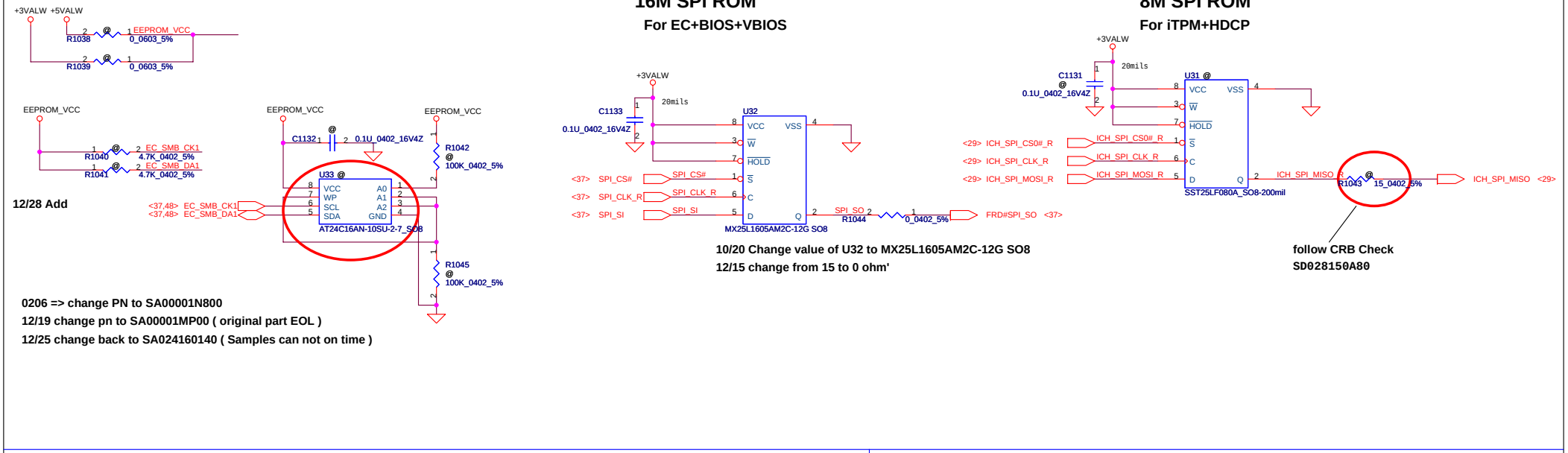
Kill SWITCH



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

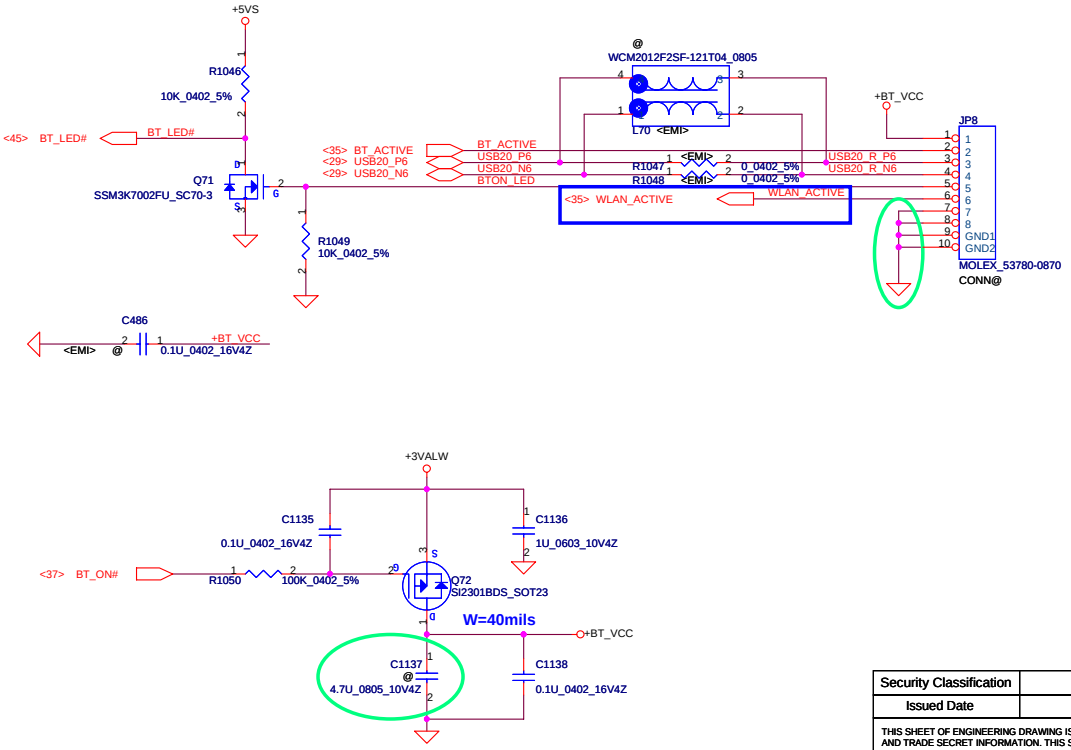
Compal Electronics, Inc.

Title	KB/SW/PW/Fun Conn	
Size B	Document Number KHLBX MB Schematic	Rev 1.0
Date: Monday, January 19, 2009	Sheet 38 of 56	

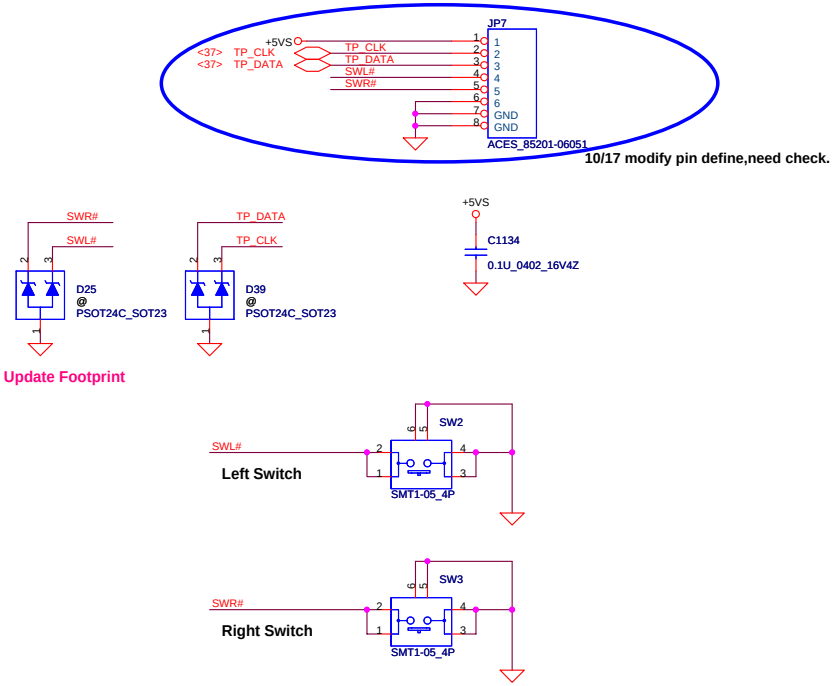


Bluetooth Conn.

Need to check BT pin definition again!
9/20 modified this block



To TP/B Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: BIOS, TP & BT Connector

Size	Document Number	Rev
B	KHLBX MB Schematic	1.0

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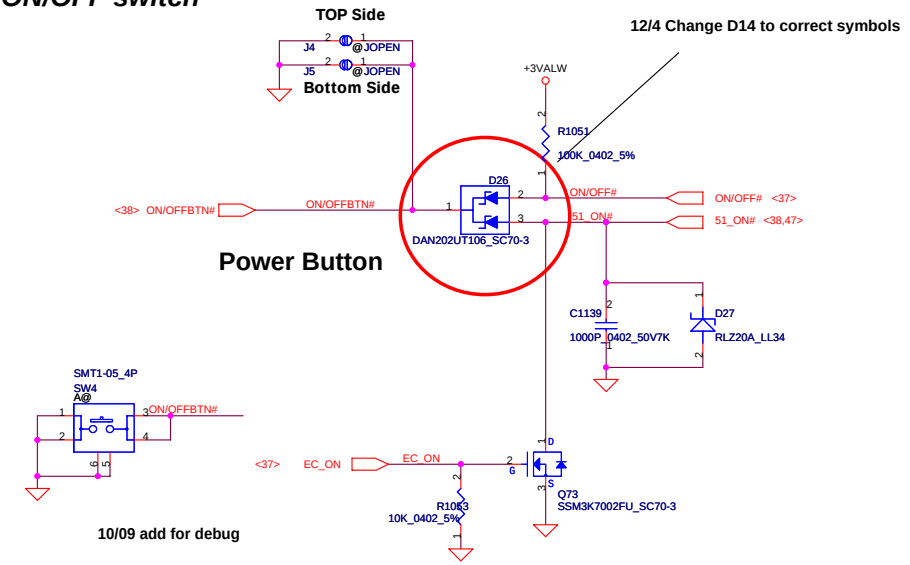
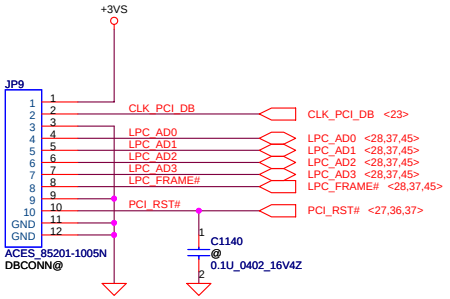
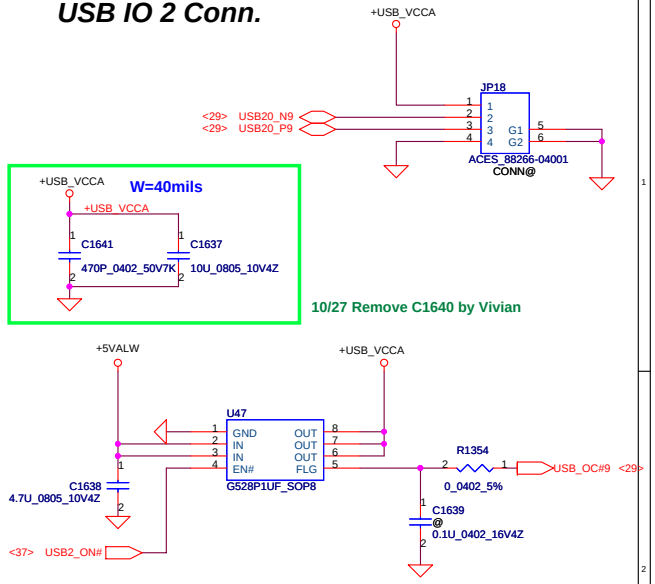
ON/OFF switch



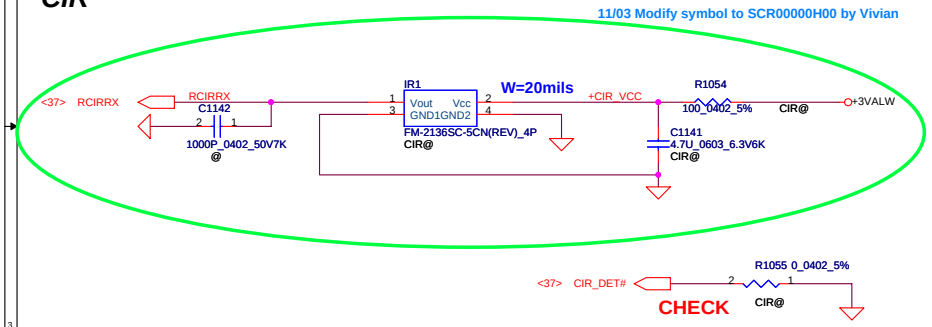
FOR LPC DEBUG PORT



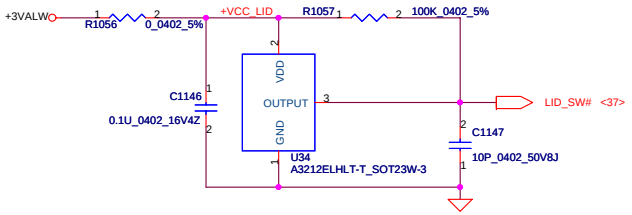
USB IO 2 Conn.



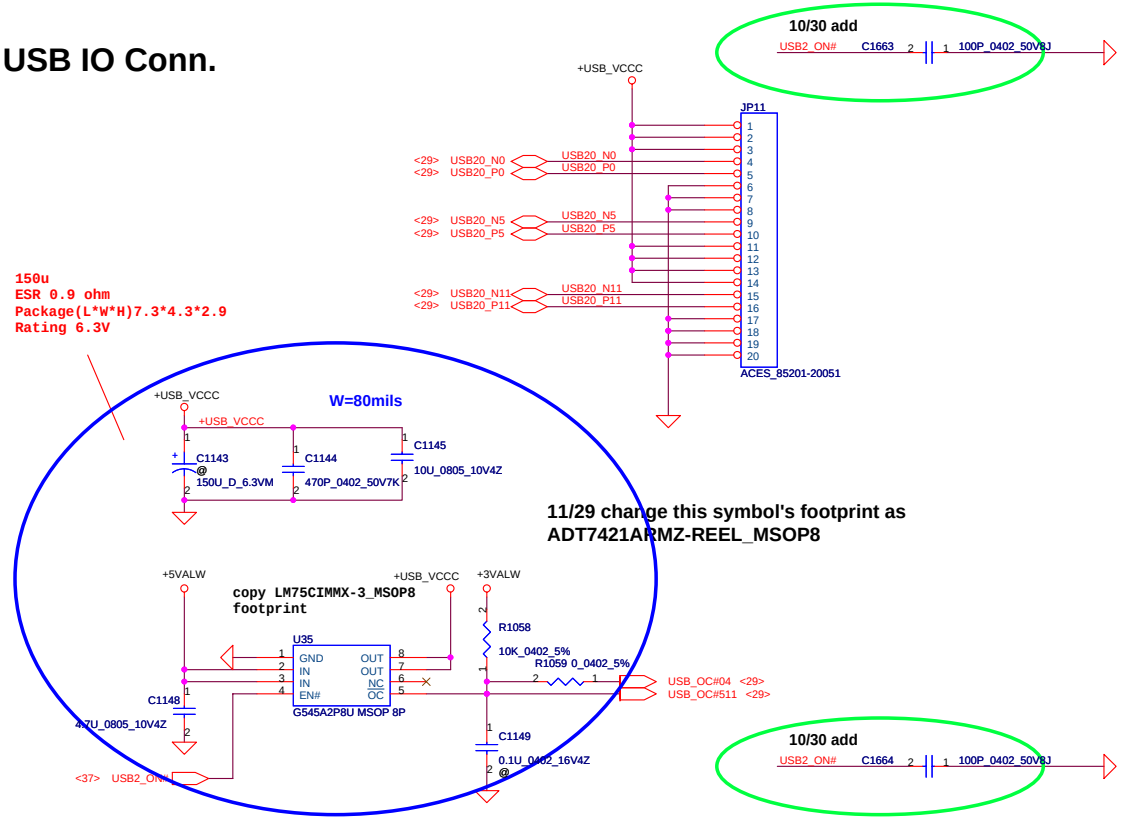
CIR



Lid Switch



USB IO Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	Power OK/Lid/Front,IO,DB Conn
Size B	Document Number: KHLBX MB Schematic
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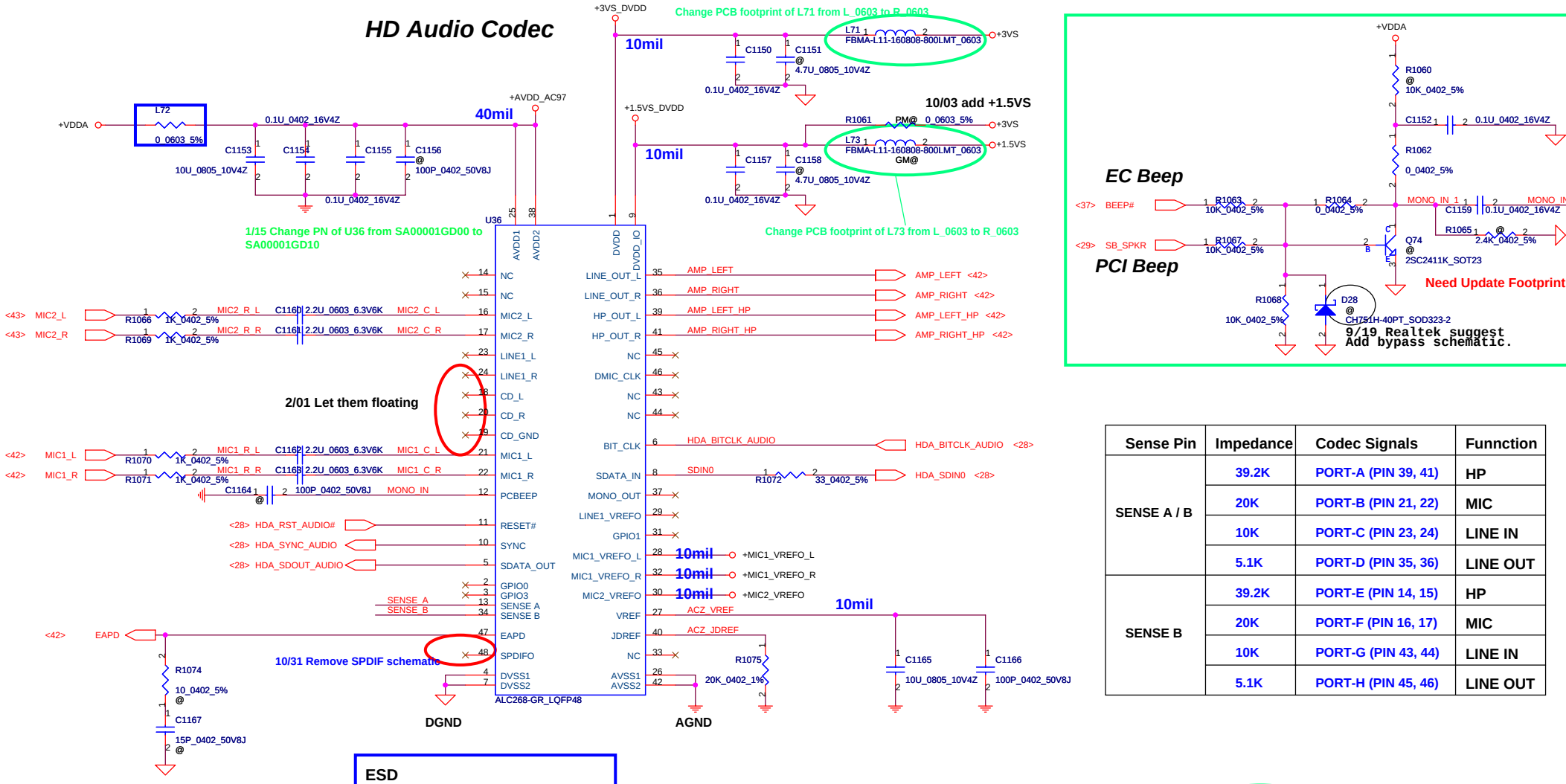
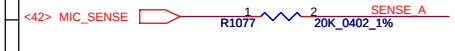
HD Audio Codec



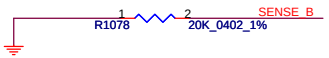
EC Beep / PCI Beep

Sense Pin	Impedance	Codec Signals	Funnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE OUT
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

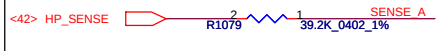
SENSE FOR Ext. Mic.



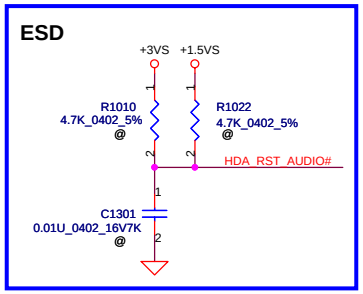
SENSE FOR Solo Int. Mic.



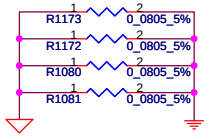
SENSE FOR HP

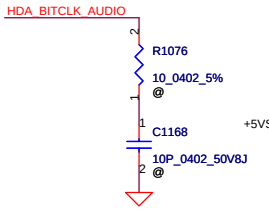


ESD

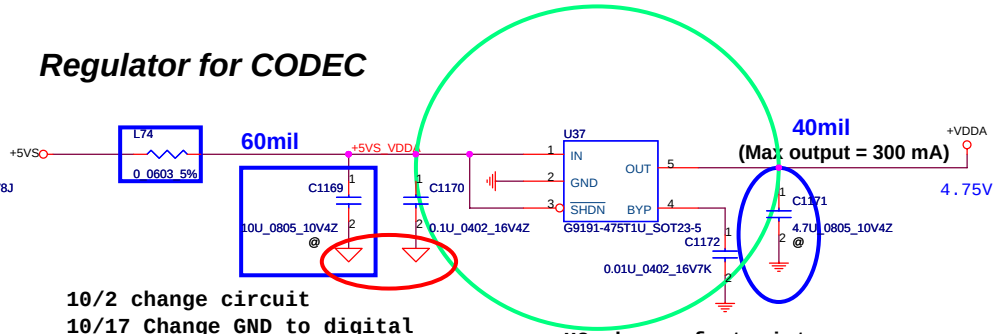


Moat Bridge





Regulator for CODEC



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: HD Audio Codec ALC268

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

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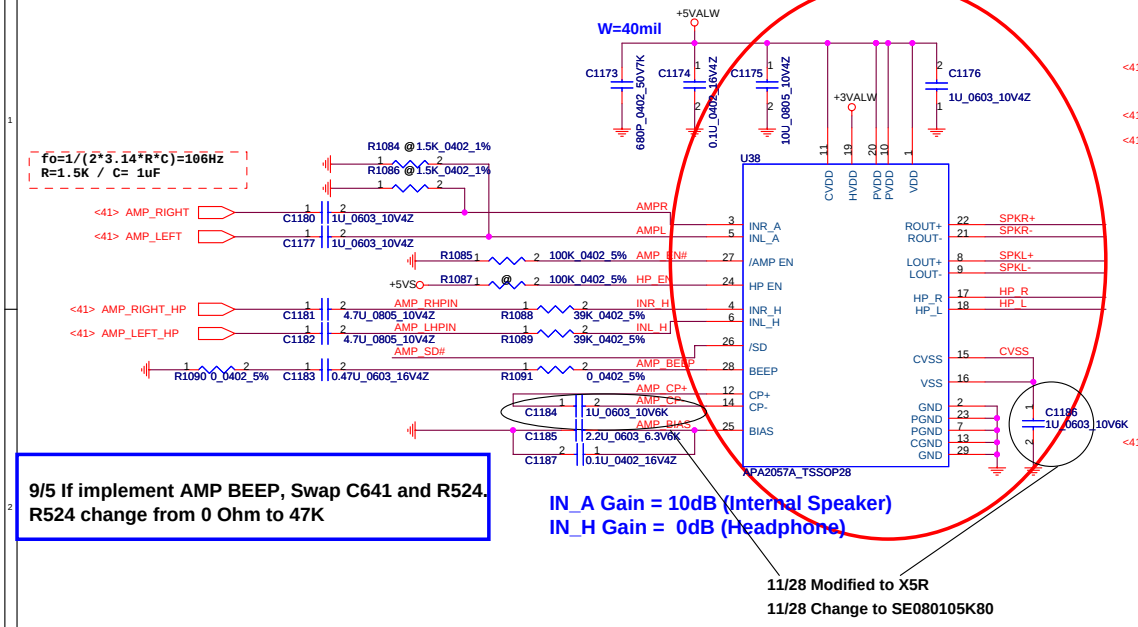
APA2057 SPK/HP Amplifier

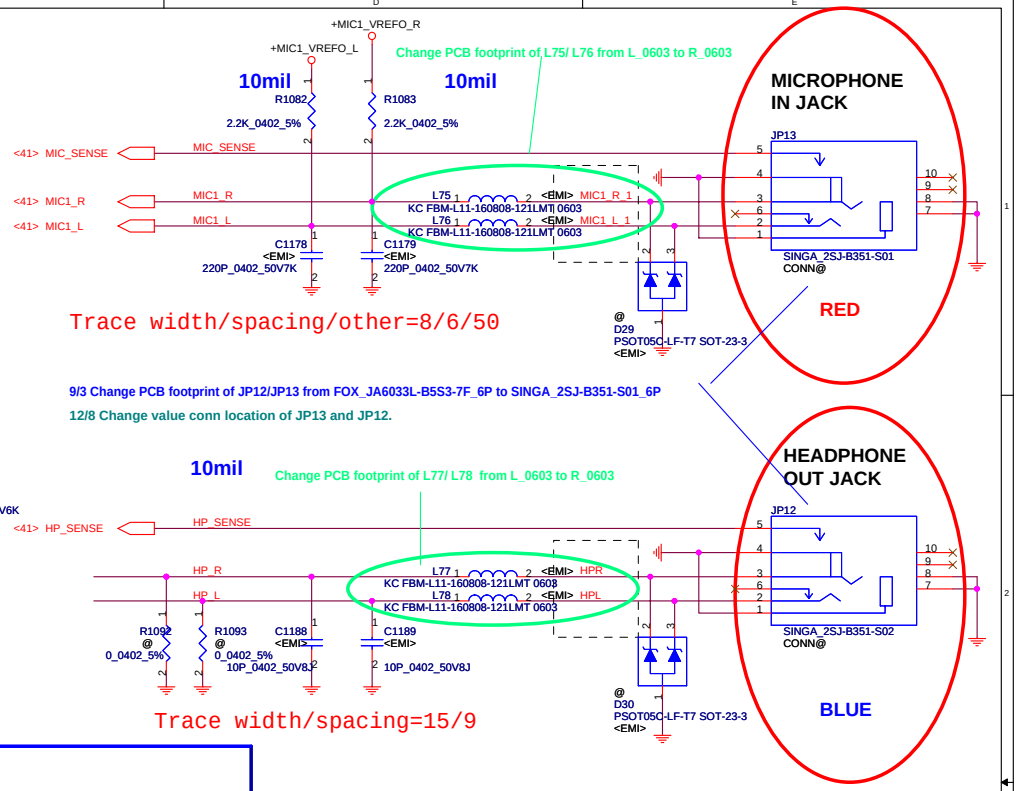
10/2 U6 APA2057A P/N:SA00001QD00



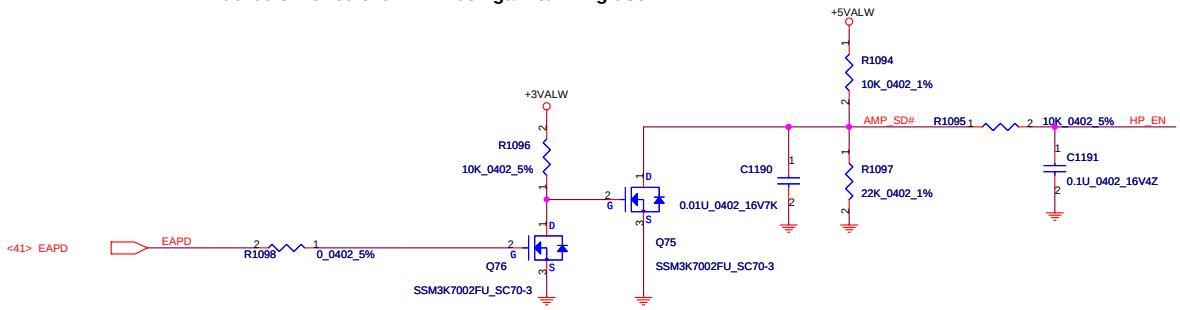
9/5 If implement AMP BEEP, Swap C641 and R524.
R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

11/28 Modified to X5R
11/28 Change to SE080105K80



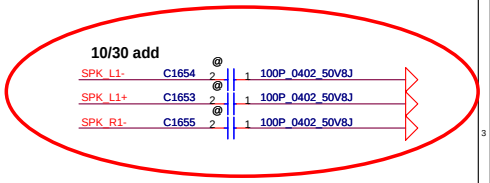
Add below circuit for APA2057 gain tunning use



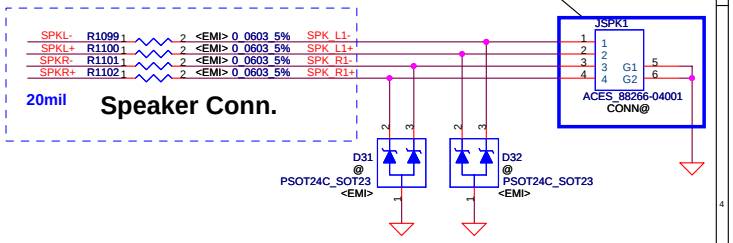
Gain= 10dB

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

+5VALW assume equal 5.1V
10 dB ---> 5.1 x 220 / 320 = 3.5



1/8 change JSPK1 following JAW91
9/3 Change footprint from ACES_88266-04001_N to ACES_88266-04001



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	AMP/VR/Audio Jack
Size: Custom	Document Number: KHLBX MB Schematic
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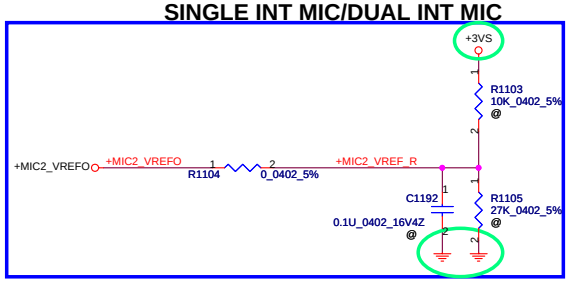
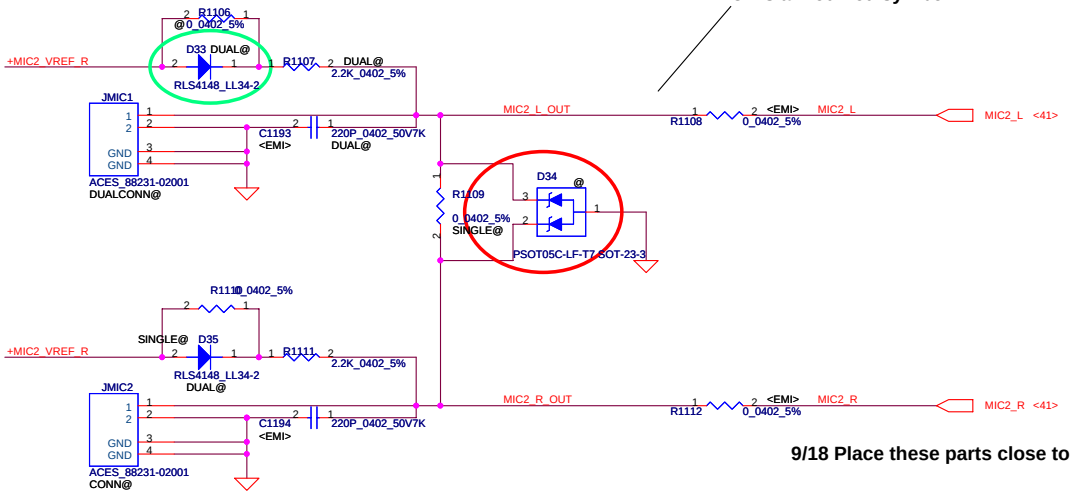
SINGLE INT MIC/DUAL INT MIC



9/18 Add D34 for INT MIC use(PN:SCD0T05CA20)

D34 is a modified symbol



9/18 Place these parts close to CODEC (U36)

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: MIC

Size	Document Number	Rev
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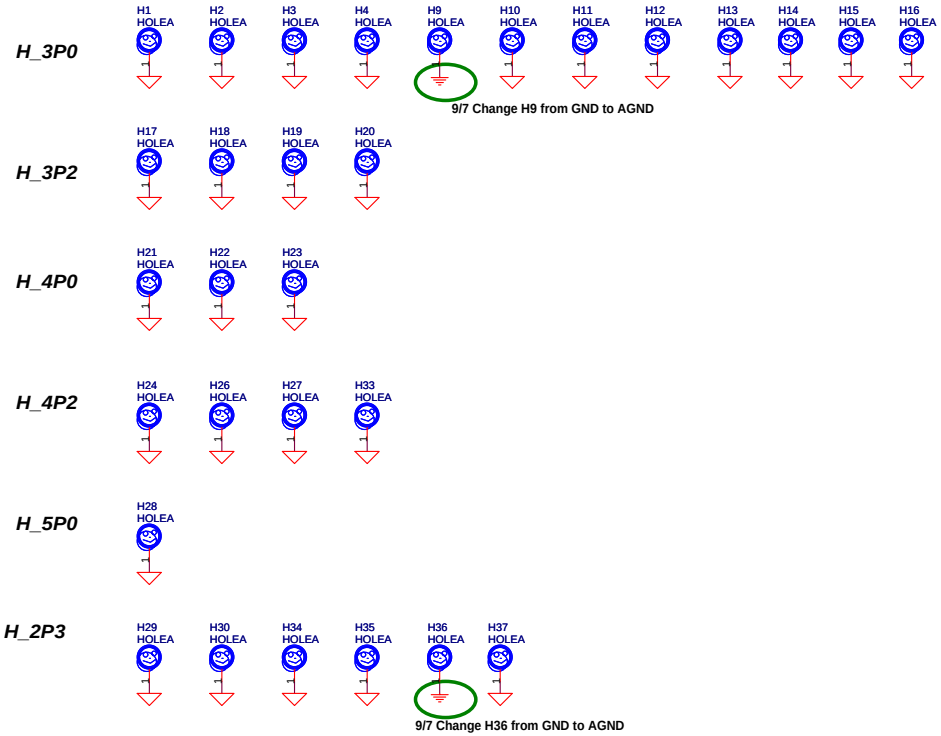
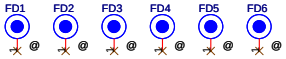
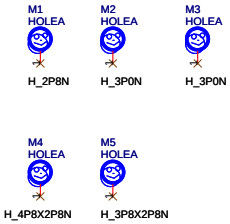
11/27 Add screw for layout request







11/27 Add screw for layout request

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	Screw	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
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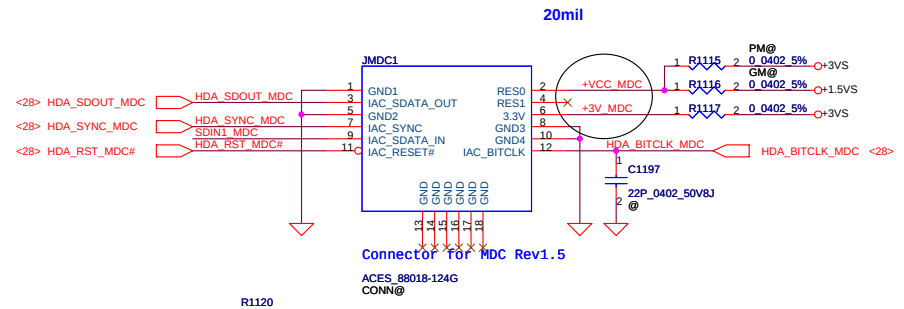
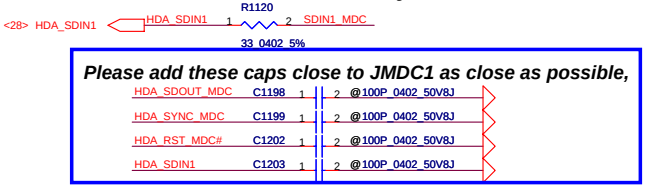
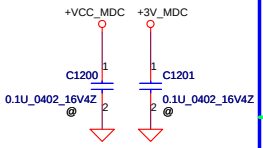
MDC Conn.



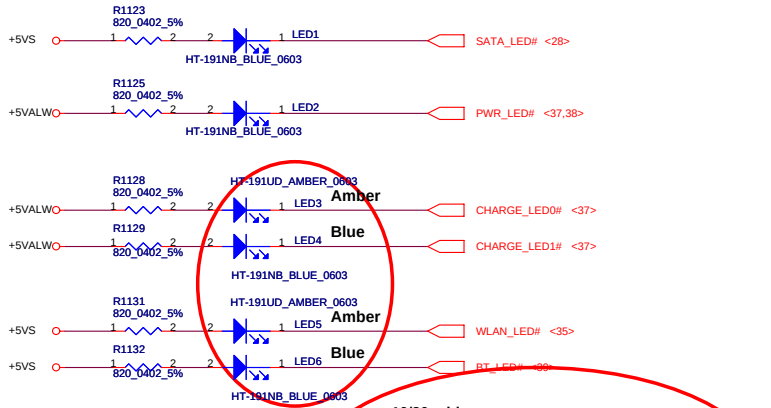


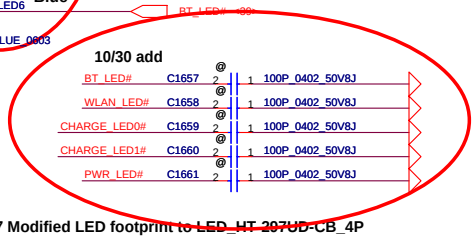


TPM X76 Information

X76 P/N	Vendor	Location	Bom Structure
X7611630L07	Infineon	C717,C718,R698,R702,R703,U32,X3	IN_TPM@
X7611630L08	Winbond	C724,U32	WB_TPM@

LED

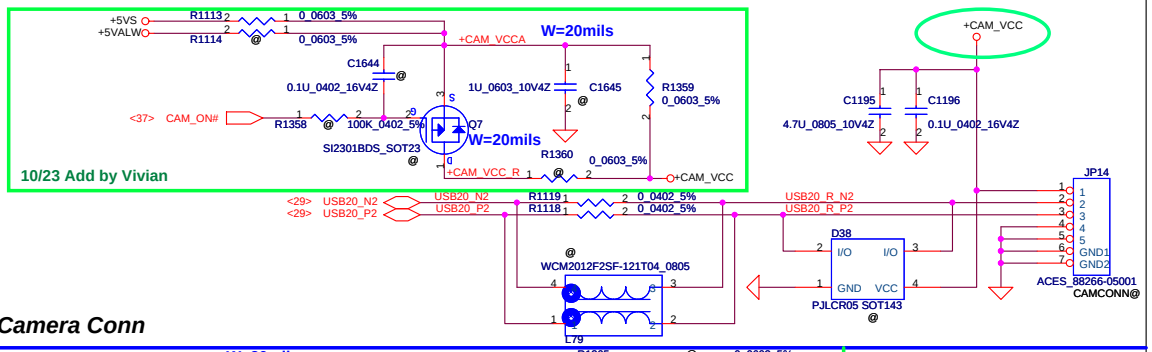




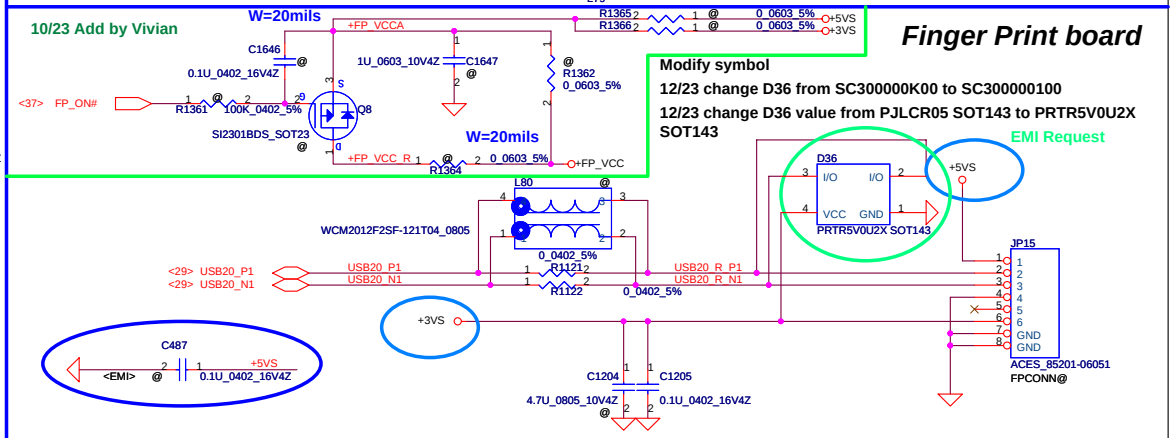
~~12/7 Modified LED footprint to LED_HT-297UD-CB_4P~~

12/15 Modified to correct LED symbol!

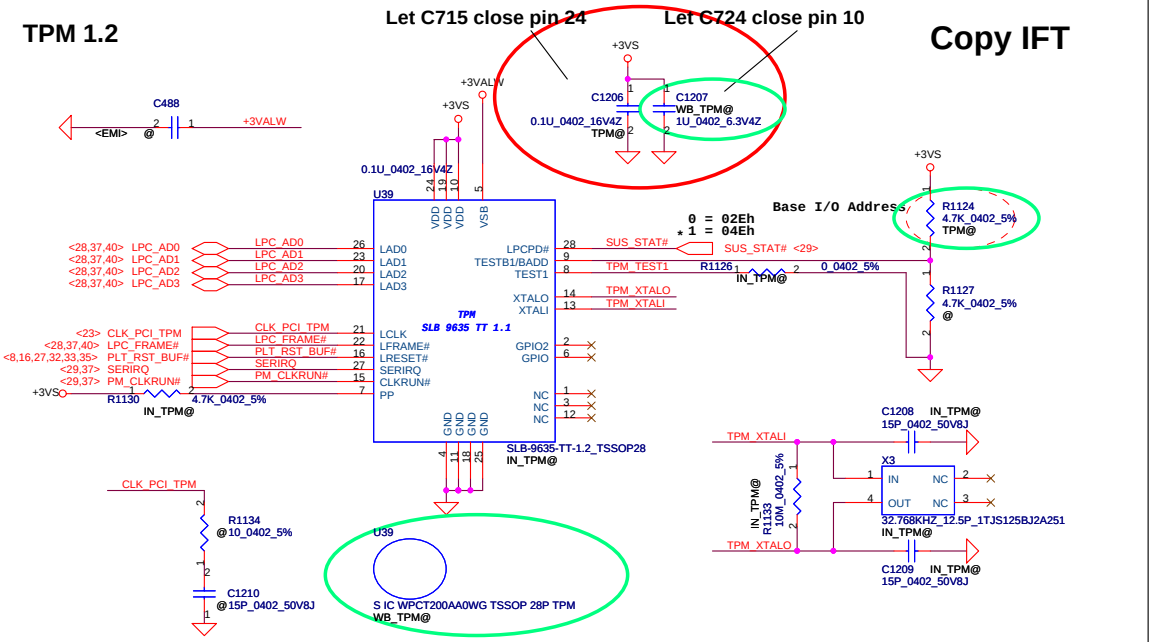
Camera Conn



Finger Print board



TPM 1.2



Copy IFT

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: MDC/LED/Camera/FP

Size: B | Document Number: KHLBX MB Schematic | Rev: 1.0

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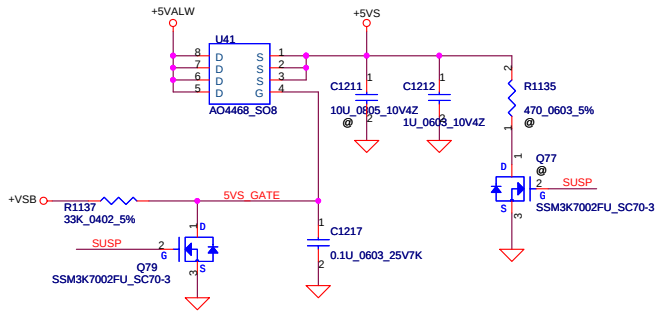
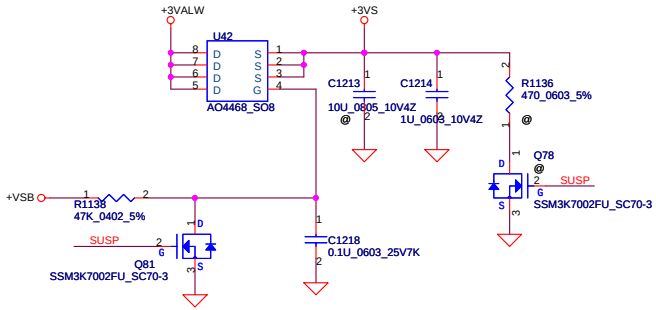
+5VALW TO +5VS

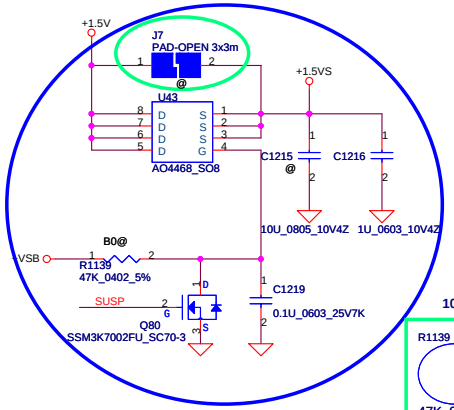


+3VALW TO +3VS

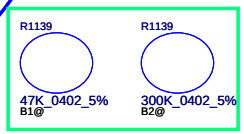


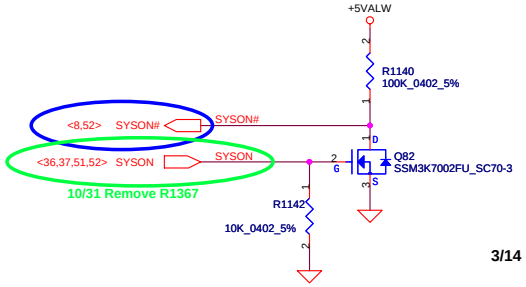
+1.5V TO +1.5VS

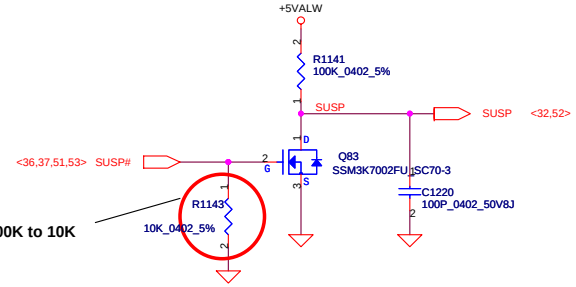
CHECK



10/22 Add by Vivian



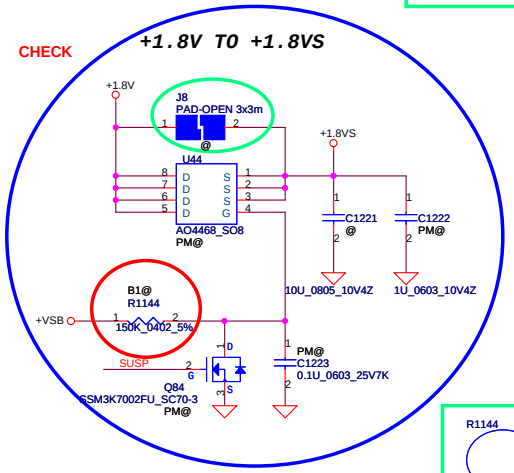


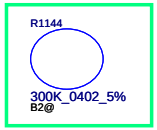


3/14 Change R16 from 100K to 10K

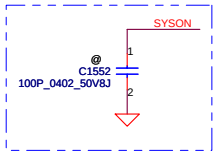
+1.8V TO +1.8VS

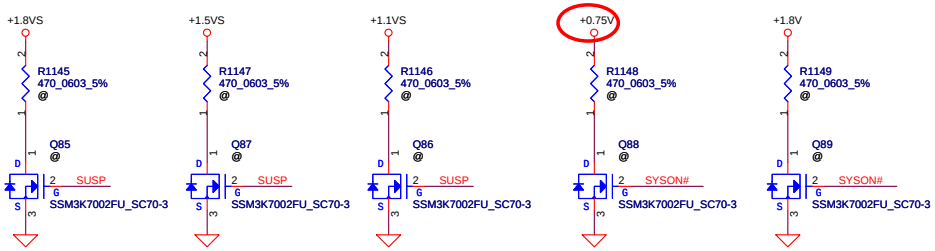
CHECK





10/22 Add by Vivian





Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
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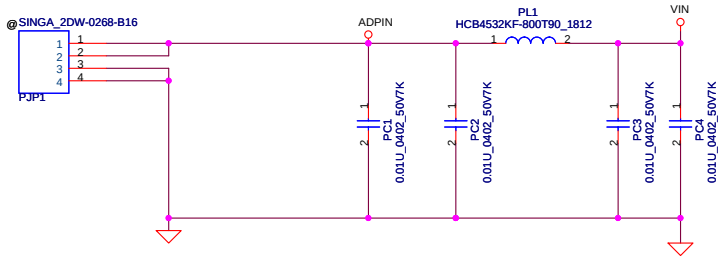
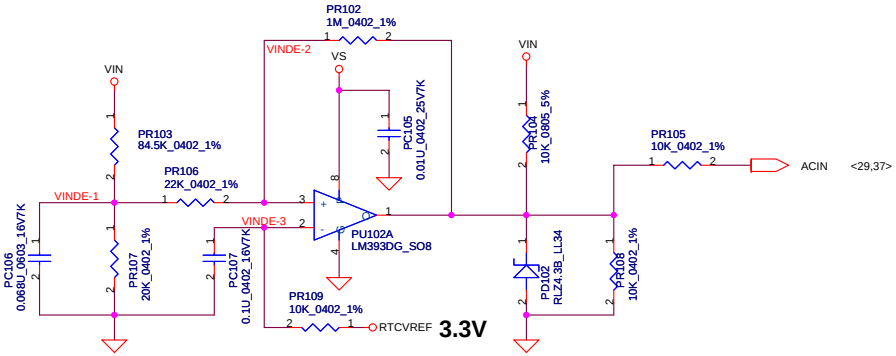
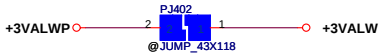
DC301001Y00

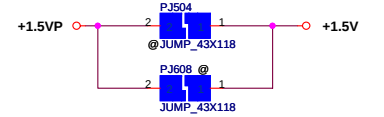


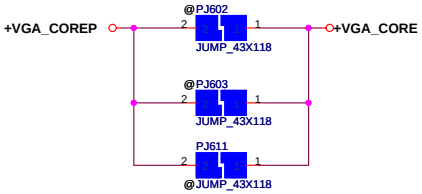


Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976







BOM structure comment

@ ==>unpop

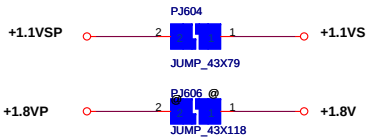
65@==> UMA only

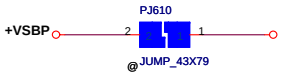
90@==>DIS only

NV@==>Nvidia sku only

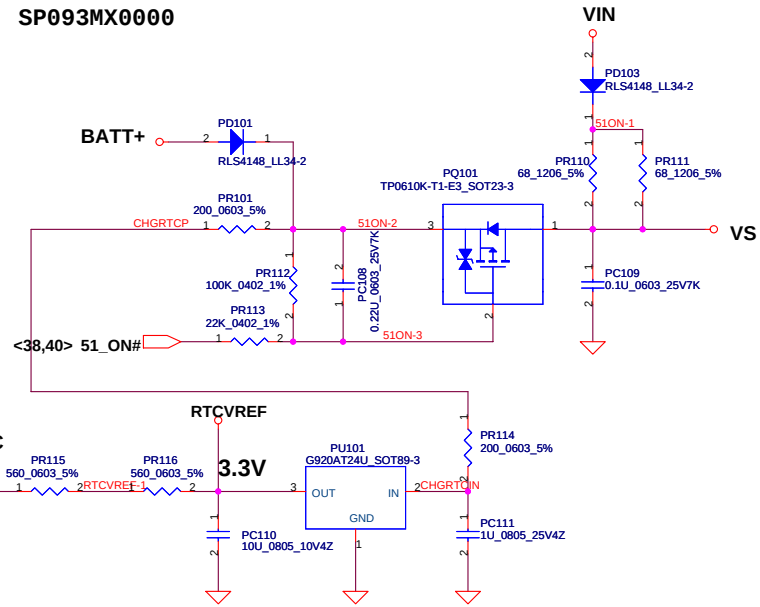
M96@==>ATI sku only

65NV@==>UMA and NV sku only





SP093MX0000



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

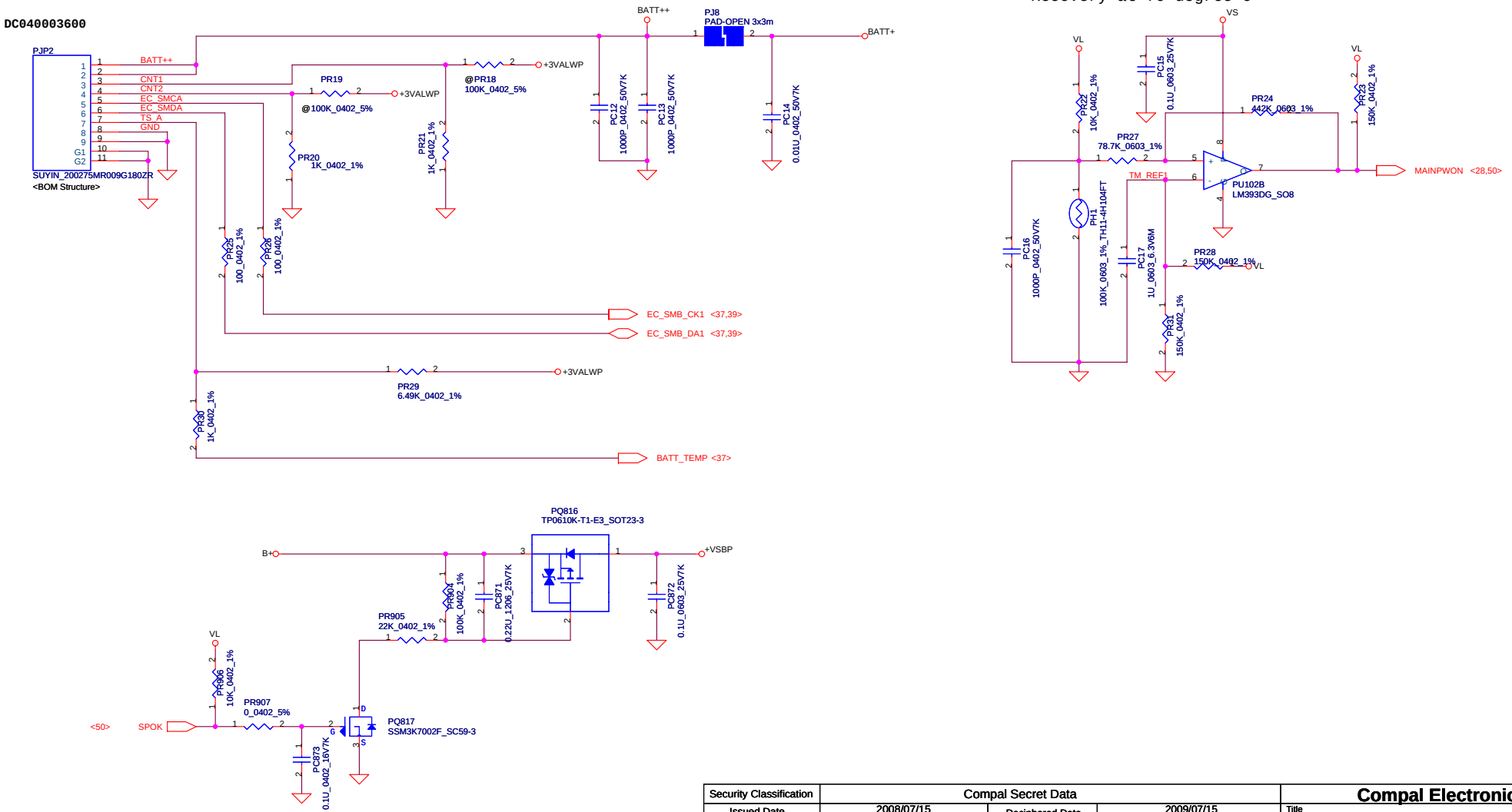
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

Date: Monday, January 19, 2009 | Sheet 47 of 56

PH1 under CPU botten side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	BATTERY CONN / OTP	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 48 of 56	

65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A

Icharge=(Vsrset/Vvdac)*(0.1/PR44)
Iadapter=(Vacset/Vvdac)*(0.1/PR36)
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

CP setting

ICHG setting

IREF	Current
2.968V	3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

"CHGVADJ" connect to EC DA pin

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

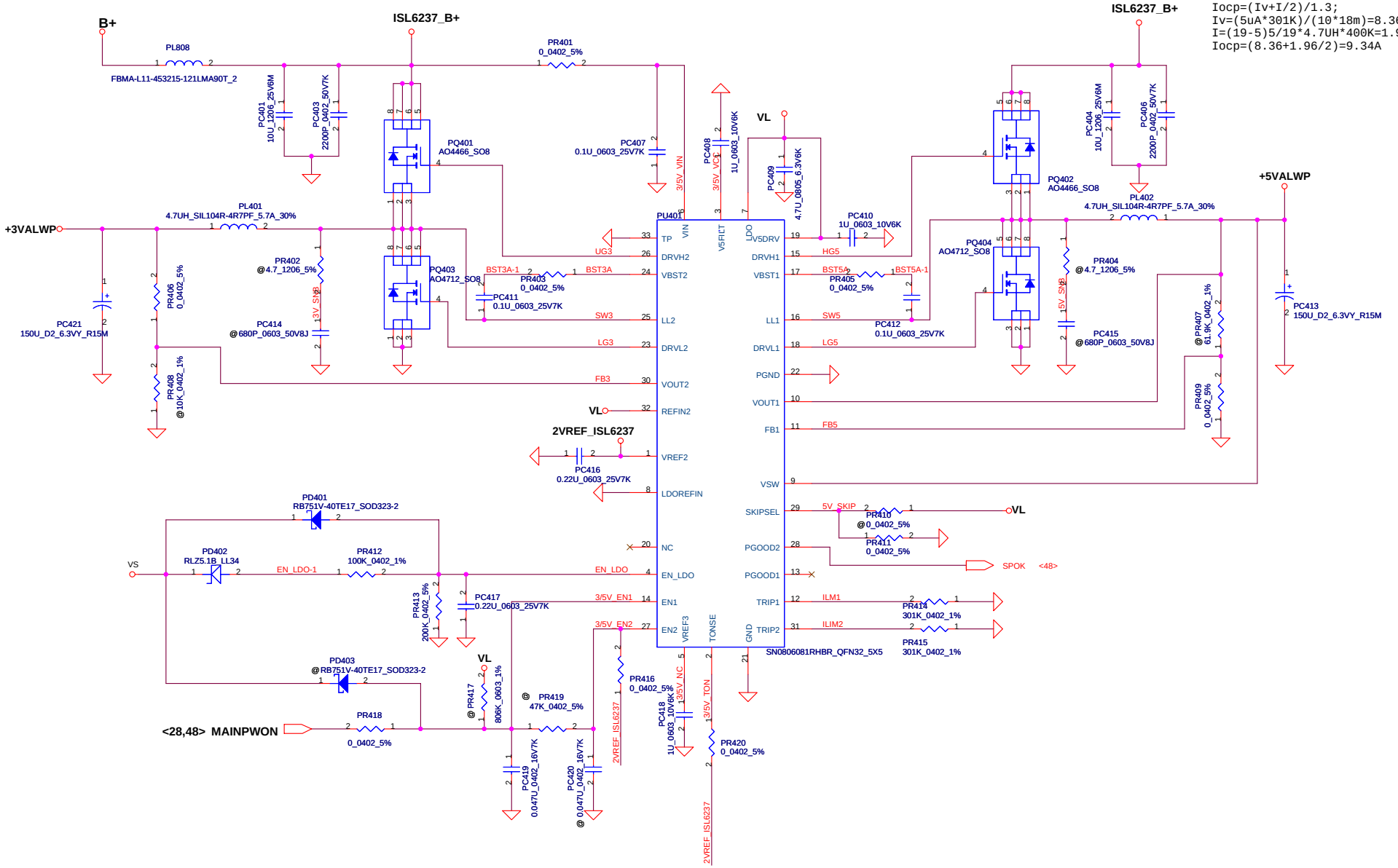
Title: CHARGER

Size: Custom | Document Number: KHLBX MB Schematic | Rev: 1.0

Date: Monday, January 19, 2009 | Sheet 49 of 56

Iocp=Iv+I/2; Iv=(5uA*301K)/(10*18m)=8.36A
I=(19-3.3)3.3/19*4.7UH*300K=1.93AIocp=8.36+1.93/2=9.32A

Iocp=(Iv+I/2)/1.3;
Iv=(5uA*301K)/(10*18m)=8.36A ;
I=(19-5)5/19*4.7UH*400K=1.96A;
Iocp=(8.36+1.96/2)=9.34A



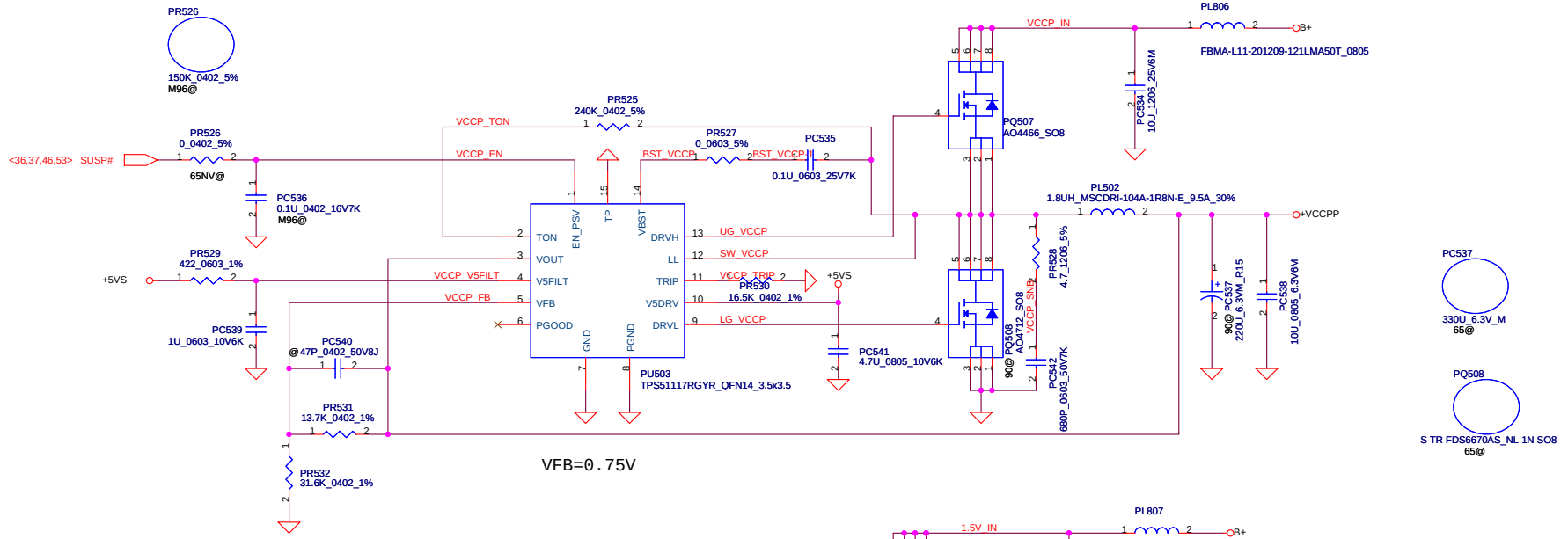
Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	3VALW/5VALW	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 50 of 56	

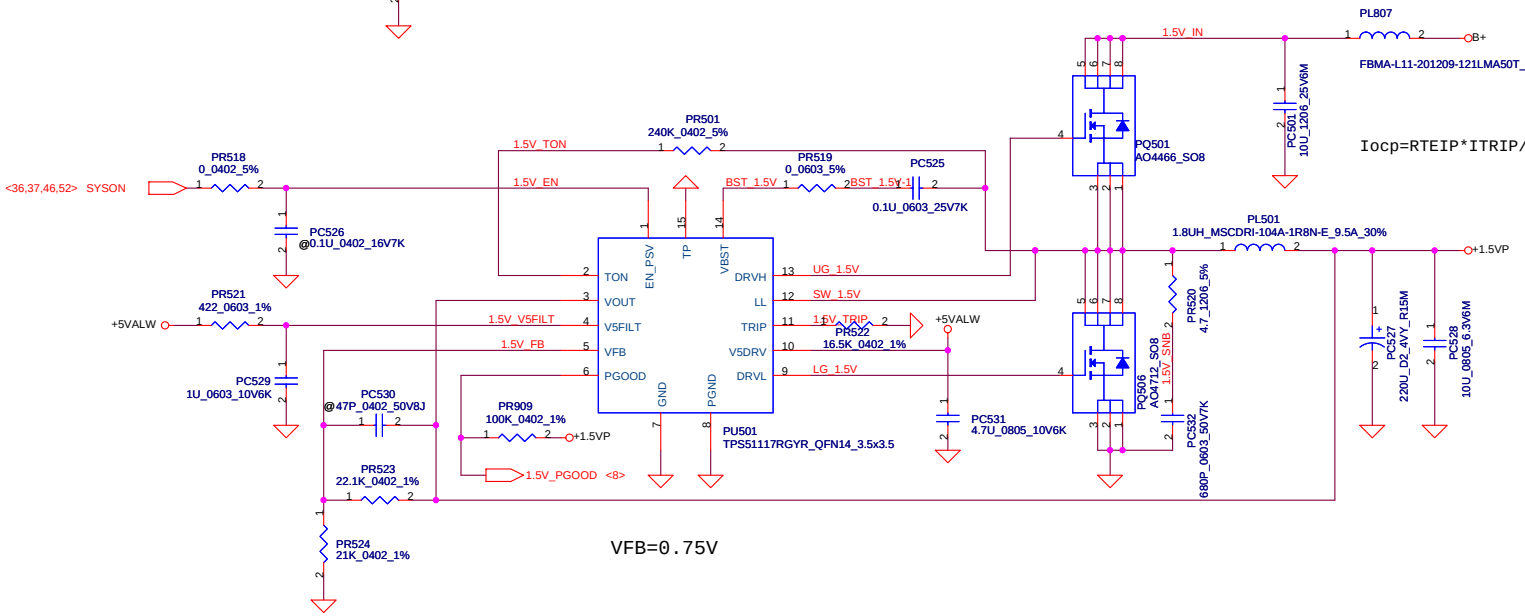
UMA Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=16.5K*9u/11.5m+1.64/2= 13.7A

DIS Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=16.5K*9u/15m+1.64/2= 10.72A



VFB=0.75V

Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=16.5K*9u/15m+2.28/2= 11.04A



VFB=0.75V

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

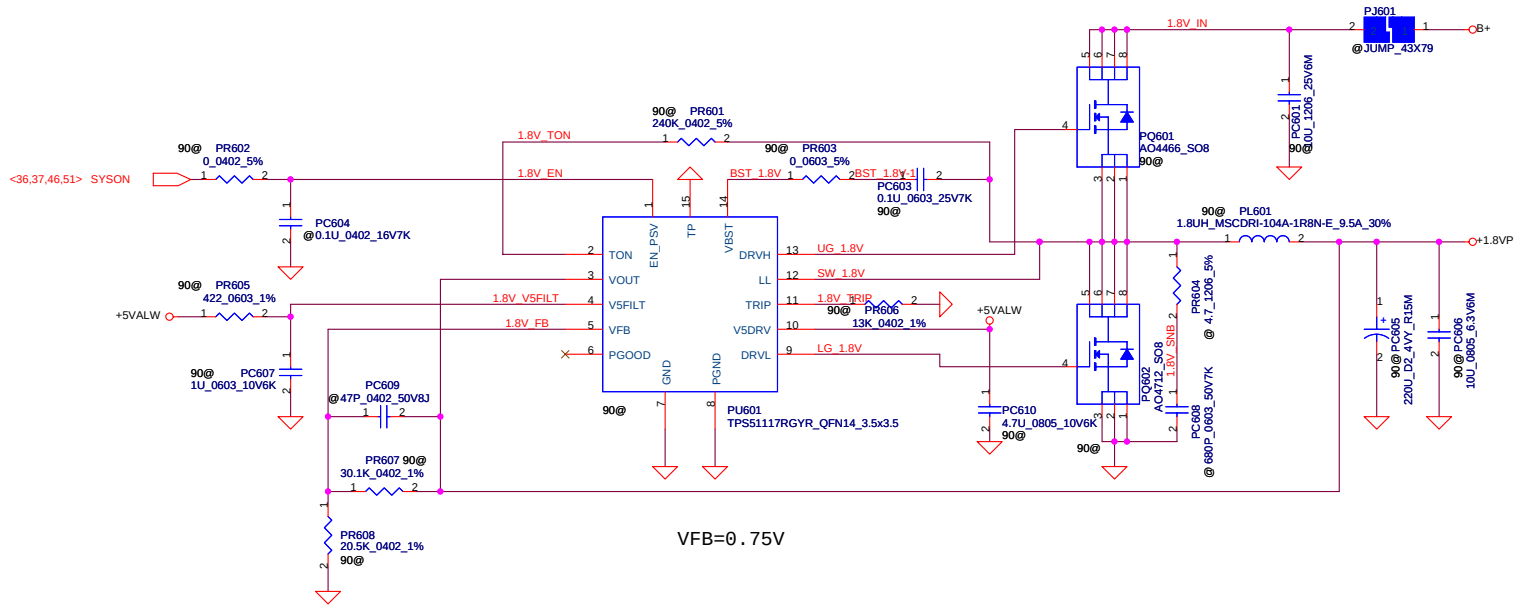
Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

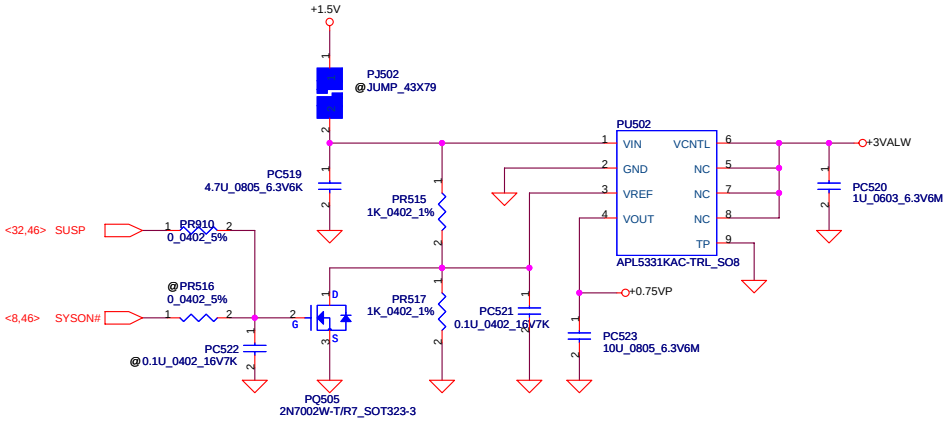
Size	Document Number	Rev
Custom	KHLBX MB Schematic	1.0

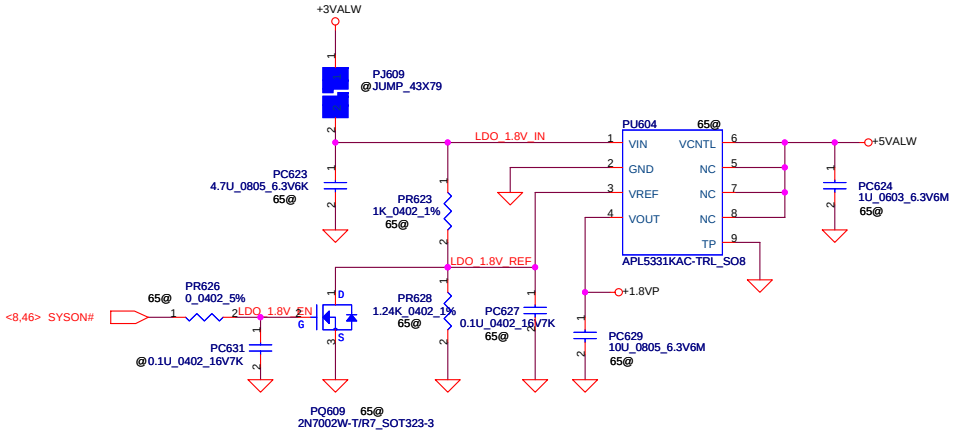
Date: Monday, January 19, 2009 Sheet 51 of 56

Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=13k*9u/15m+1/2*2.7=9.15A



VFB=0.75V

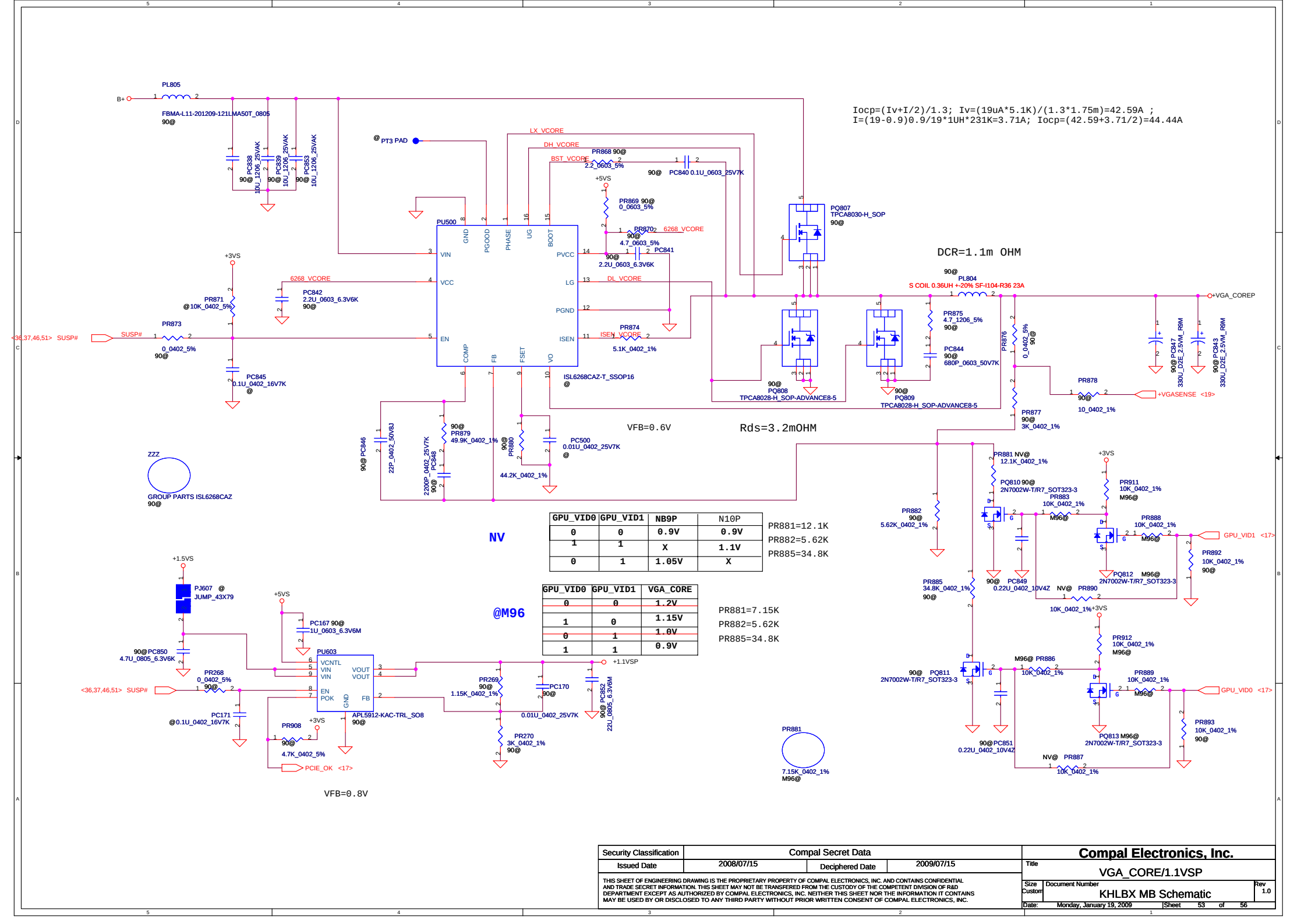




Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	VGA_CORE/1.8V/1.1V	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 52 of 56	



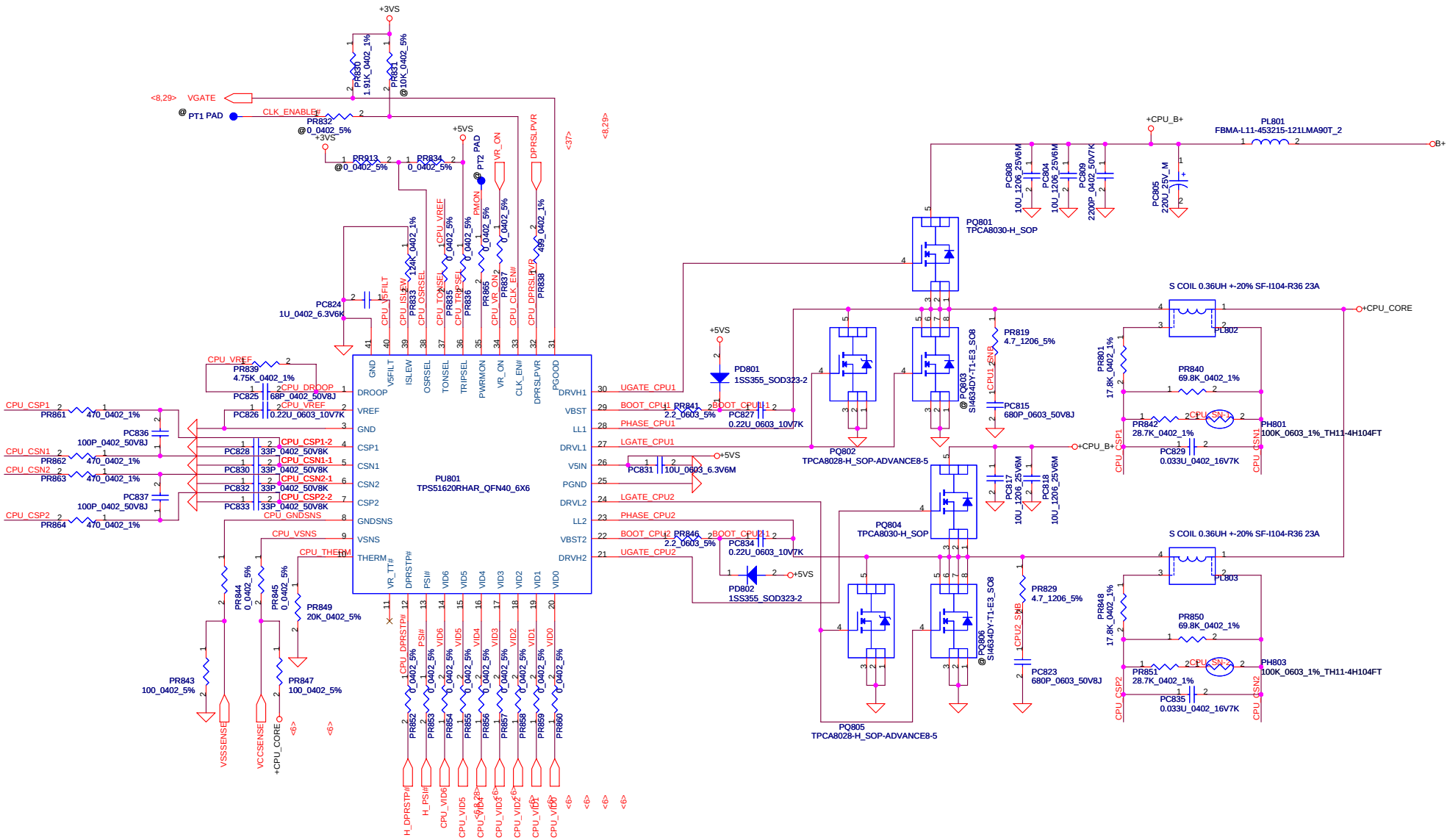
GPU_VID0	GPU_VID1	NB9P	N10P
0	0	0.9V	0.9V
1	1	X	1.1V
0	1	1.05V	X

GPU_VID0	GPU_VID1	VGA_CORE
0	0	1.2V
1	0	1.15V
0	1	1.0V
1	1	0.9V

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	VGA_CORE/1.1VSP
Size: Custom	Document Number: KHLBX MB Schematic
Rev	1.0
Date: Monday, January 19, 2009	Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	+CPU_CORE	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 54 of 56	

Page	Reason for change	Modify list
DVT	Change Diode 4148 vendor for layout footprint	PD101,PD103,PD301
	modify VGA_core OCP to 29A	Change PR874 to 5.9K
	modify VGA_core sequence for NV and ATI	Remove PC845 & change PR873 to 0 ohm
	modify 1.05V sequence for ATI	Change PR526 to 150K ohm and PC536 to 0.1U
	Change 2N06 to 2N7002 for costdown	PQ810 & PQ811 for DIS, PQ812 & PQ813 for M96
	Add snubber & bead at cpu_core for EMI request	Add PR819 & PR829 to 4.7 OHM , PC815 & PC823 to 680pF, Change PL801 to 120 ohm bead & change PR841 & PR846 to 2.2 OHM
	Add snubber & bead at VGA_core for EMI request	Add PR875 to 4.7 OHM , PC844 to 680pF, Change PJ605 to 120 ohm bead and change PR868 to 2.2 OHM
	Add snubber & bead at VCCP & 1.5VP for EMI request	Add PR528 & PR520 to 4.7 OHM , PC542 & PC532 to 680pF
		change PJ506 and PJ501 to 120 ohm bead
	Add boost res. & bead & snubber at charger for EMI request	Change PJ301 to 120 Ohm bead and Changer PR307 to 2.2 OHM, Add PR312 to 4.7 Ohm & PC318 to 680P
	Change 1.8UH vender to mgalaer for ZIZI nosie	PL502,PL501,PL601(DIS)
	Modify 1.05V OCP for UMA(12A~19A) & DIS for (8A~12A)	Change PR530 to 16.5K & PQ508 to FDS6670
	Modify CPU loadline	Change PR839 to 4.64K
	Modify VGA CHOKE to 4mm high	PL804
	Modify 1.1V to APL5912 for over loading	PU603
	Change VCCP output cap to 330U for reduce ripper	PC537
	Change PU500 & PC500 to X76 group for 2nd	Del PU500 & PC500 in 90W SKU
	Add 10UF in charger output for unstable	PC331
	Modify 1.5V OCP to 8A~12A	Change PR522 to 16.5K
PVT	Modify ATI VGA_core from 1.1 to 1.15V	Change PR881 to 7.15K
	Modify 220U/25V vender to SANYO from PPM suggest	
	Add 10UF in VGA B+ for over current(VGA B+ about 5.6A)	Add PC853 to 10U
	Modify CPU loadline	Change PR839 to 4.75K
	Change VGA frquency to 300K, reduse △I	Change PR880to 44.2K
	Change VGA FB cap for better response	Change PC848 to 2200pF
	Change VGA OCP set to around 41A	Change PR874 to 8.66K
	Change VGA output choke for rating.	Change PL804 to 0.36U
	Add extra VGA Low Side MOS	Add PQ809
	Change VGA high mos for cost down.	Change PQ807 to S TR TPCA8030-H 1N SOP-ADV
	Change CPU high mos for cost down.	Change PQ801 and PQ804 to S TR TPCA8030-H 1N SOP-ADV

Security Classification	Compal Secret Data		
Issued Date	2008/07/15	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 55 of 56	

Page	Reason for change	Modify list
PVT	Change VGA response	Change PR876 to 0 and PR878 to10
	Change VGA OCP set	Change PR876 to 0 and PR874 to 5.1K

PVT

Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number: KHLBX MB Schematic	Rev: 1.0
Date: Monday, January 19, 2009	Sheet 56 of 56	