

Compal Confidential

MODEL NAME : ZIVY1

PCB NO : LA-B131P

BOM P/N : SKU1_4519RY38L05 (I5-4200U 1.6GHZ - Hynix 2G)
SKU2_4519RY38L05 (I5-4200U 1.6GHZ - Micro 2G)
SKU3_4519RY38L08 (I7-4500U 1.8GHZ - Hynix 4G) FAI
SKU3_4519RY38L08 (I7-4510U 1.8GHZ - Hynix 4G) main SMT
SKU4_4519RY38L07 (I2-4200U 1.6GHZ - Micro 4G)
SKU5_4519RY38L05 (I5-4200U 1.6GHZ - Samsung 2G)
SKU6_4519RY38L07 (I5-4200U 1.6GHZ - Samsung 4G)



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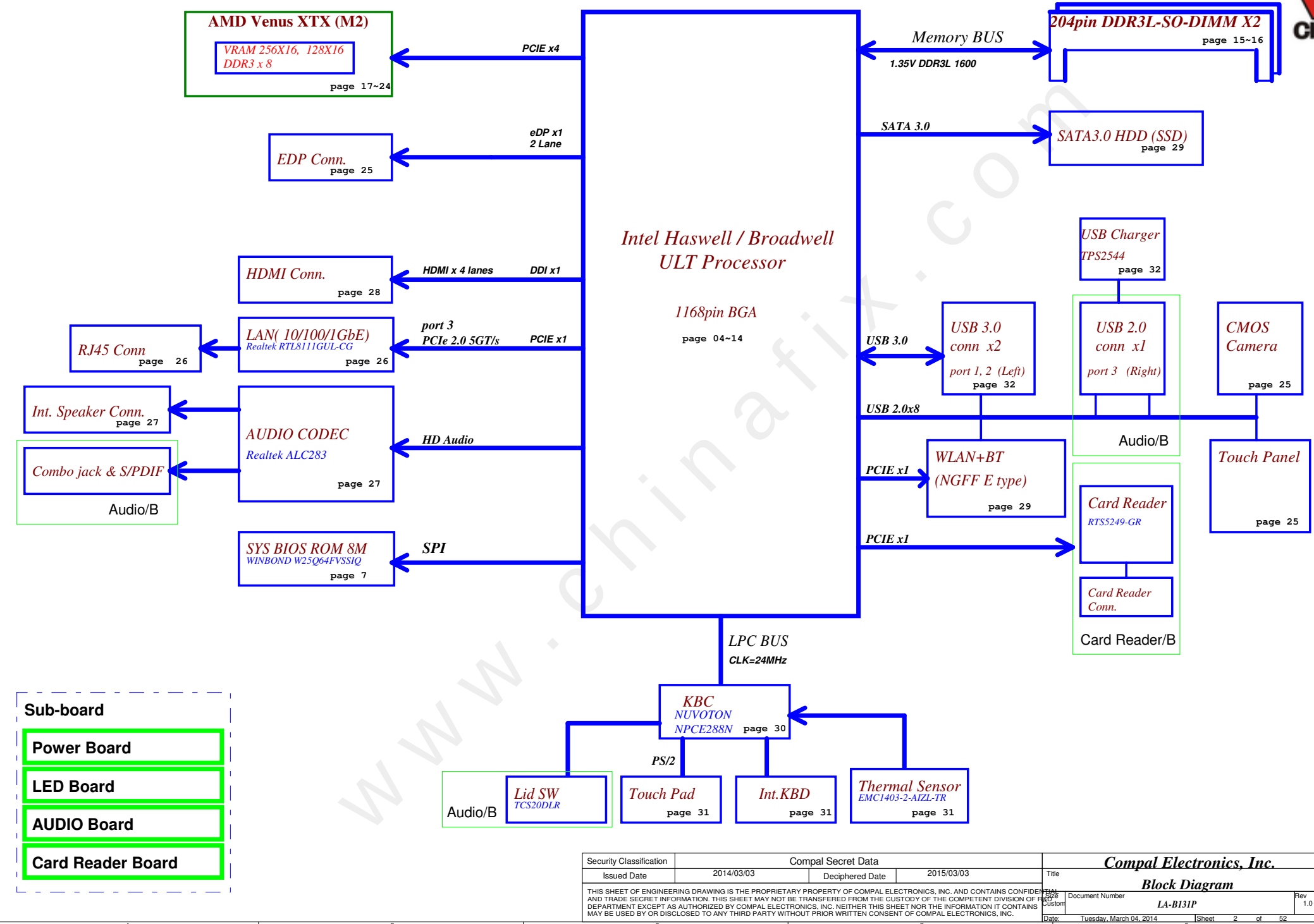
Lamborghini Y40 M/B Schematics Document

Intel Haswell / Broadwell ULT Processor + AMD Venus XTX

2014-03-03

REV: 1.0

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	Cover Sheet
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				LA-B131P	1.0
				Date: Tuesday, March 04, 2014	Sheet 1 of 52



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				Date	Tuesday, March 04, 2014	Sheet 2 of 52



Voltage Rails

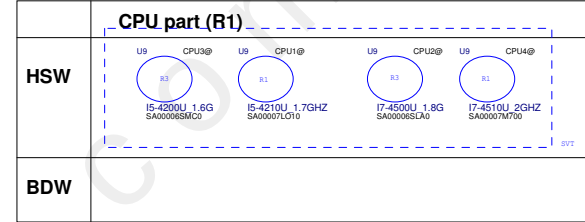
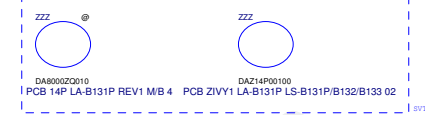
State	power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +CPU_CORE +0.675VS +VGA_CORE +MEM_GFX +3VGA +1.8VGA +VGA_PCIE
S0		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		X	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Unpop	@ @CONN@ / @DIS@ @EMI@ / @ESD@
CPU OPTION	CPU1@ ~ CPU4@
AMD Venus XTX	DIS@
VRAM Option	V2G@ / V4G@ HYN2@ / HYN4@ SAM2@ / SAM4@ MIC2@ / MIC4@ BDW@ / HSW@
Platform	
DS3	DS3@
NODS3	NODS3@
LAN RTL811GUS	SWR@ / LDO@
EMI PART	EMI@
ESD PART	ESD@
Crystal	NOGCLK@
Green CLK	GCLK@
SATA Repeater	TI@ / Parade@
EC	9022@ / 9012@
Connector	CONN@

PCB part



EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 0010	Thermal Sensor	1001 101xb

PCH SM Bus address

Device	Address
DDR_DIMM1	1010 000x A0h
DDR_DIMM2	1010 010x A4h
TP module	

SMBUS Control Table

	SOURCE	BATT	VGA	SODIMM	EC-KB9022	TP	Smart Charge	Thermal Sensor
SMB_EC_CK1 SMB_EC_DA1	EC	V	X	X	X	X	V	X
SMBCLK SMBDATA	PCH	X	X	V	X	V	X	X
SMLOCLK SMLODATA	PCH	X	X	X	X	X	X	X
SM1CLK SM1DATA	PCH	X	V	X	V	X	X	V

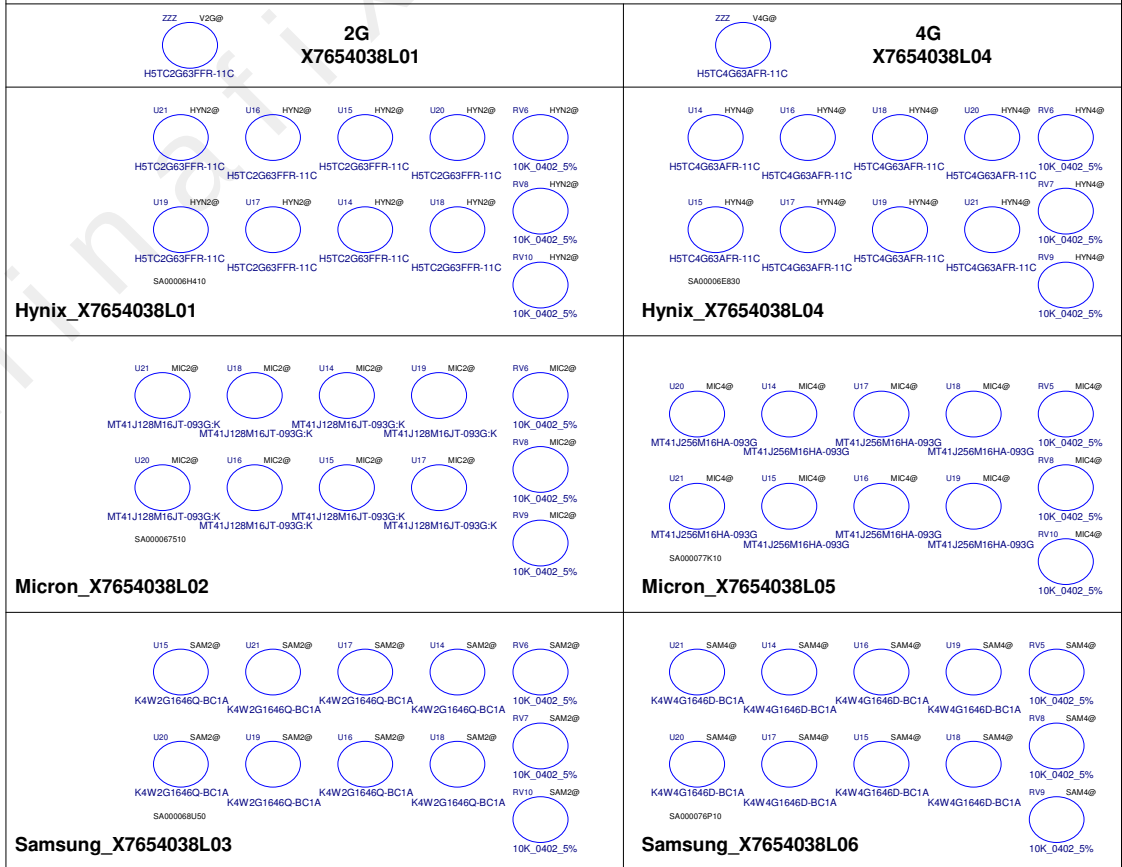
USB2.0

Port	0	1	2	3	4	5	6	7
	Left USB3.0	Left USB3.0	Right USB2.0		Touch Panel	Camera	BT (NGFF)	

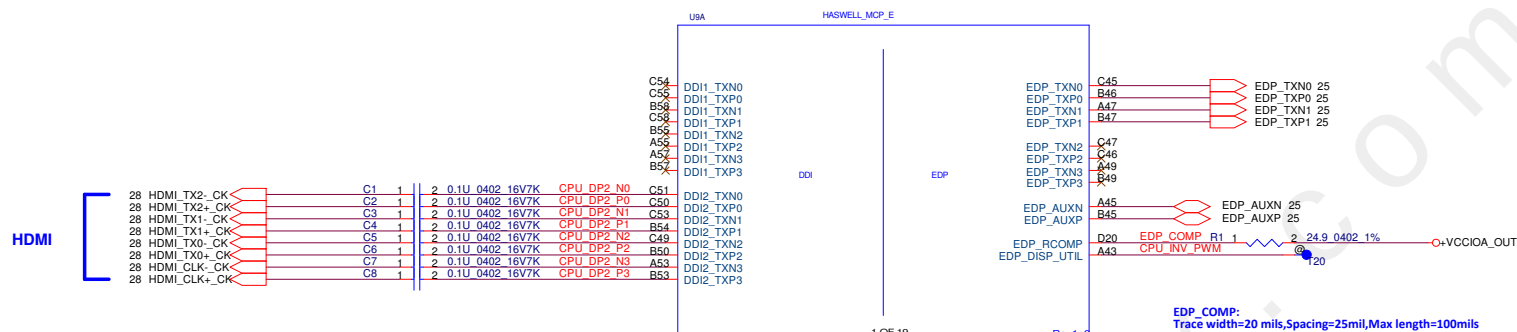
Flexible I/O Capable Ports

HSIO Port	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB 3.0	USB3_0.1	USB3_0.2												
PCIe			1	CardReader	LAN	WLAN	GPU_Venus	GPU_Venus	GPU_Venus	GPU_Venus	6-L0	6-L1	6-L2	6-L3
SATA											3	2	1	@ HDD (SSD)

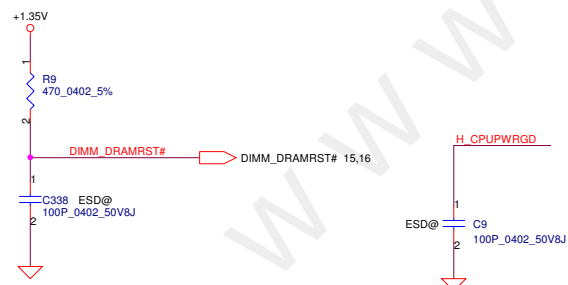
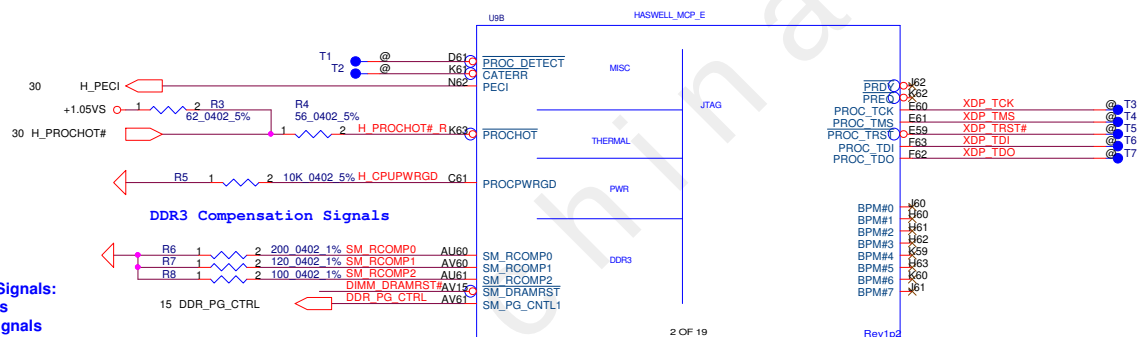
VRAM * 8 (R1)

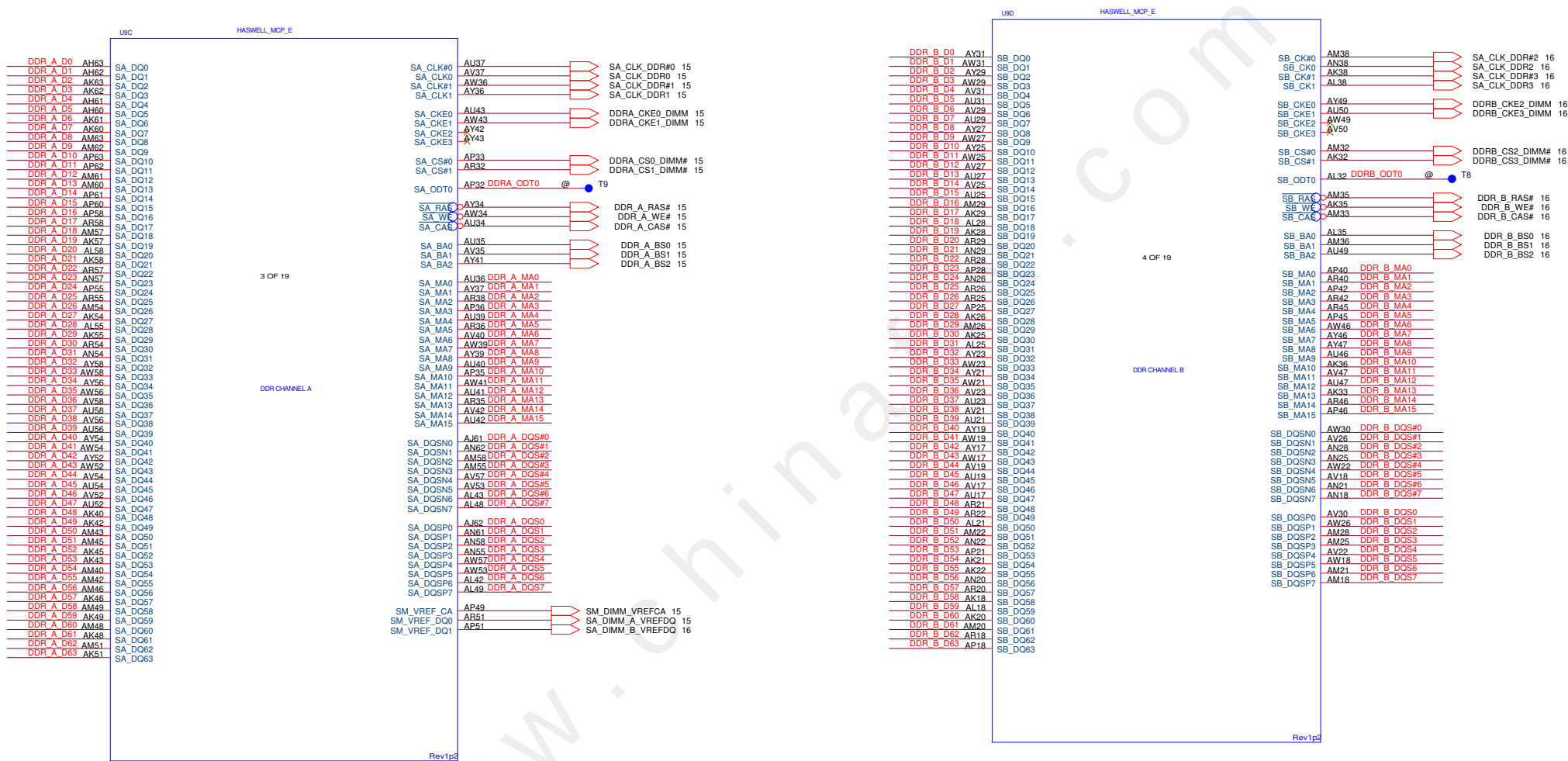


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Date: Tuesday, March 04, 2014					Sheet 3 of 52

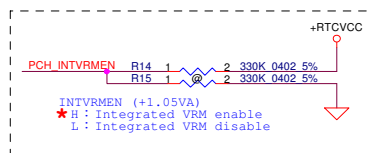
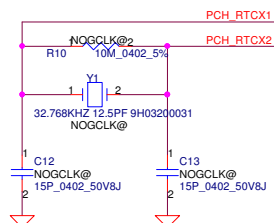
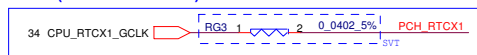


DDR3 Compensation Signals:
20mils to comp signals
25mils to non-comp signals
500mil for Max trace length



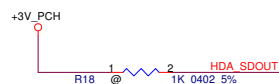
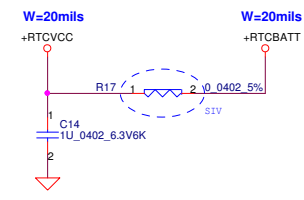


GCLK (RG3 close to Y1.1)



RTC CONN place to PWR side

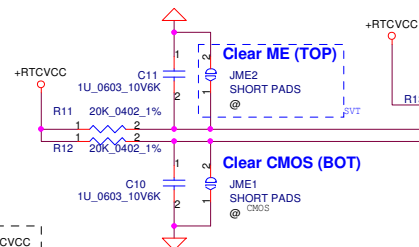
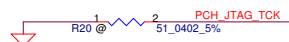
RTC Battery



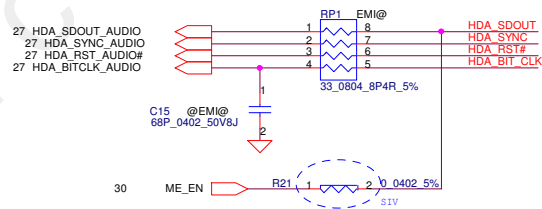
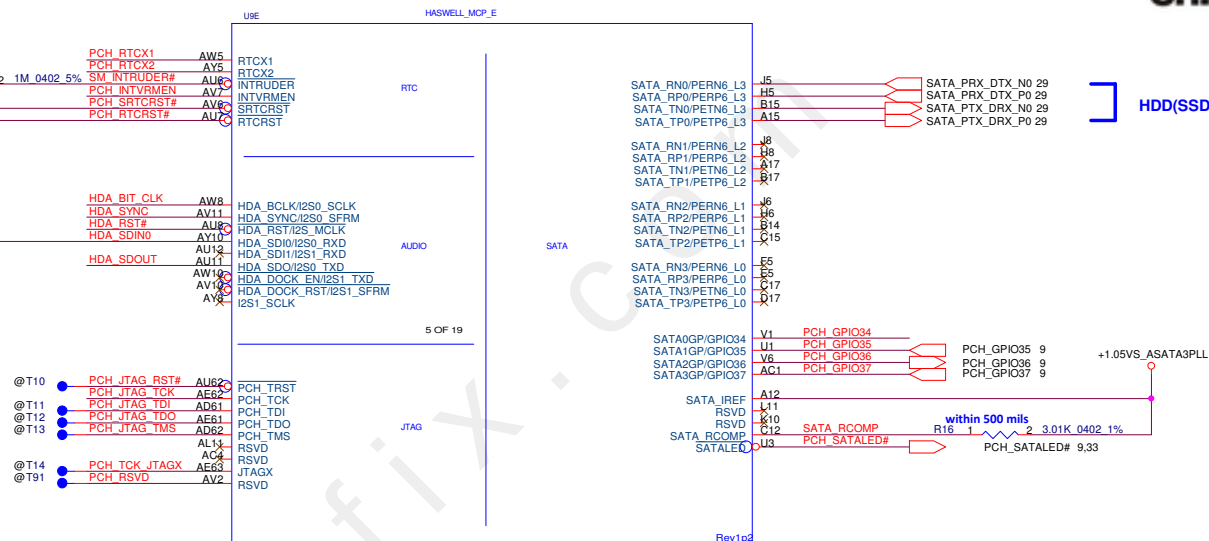
HDA_SDOUT

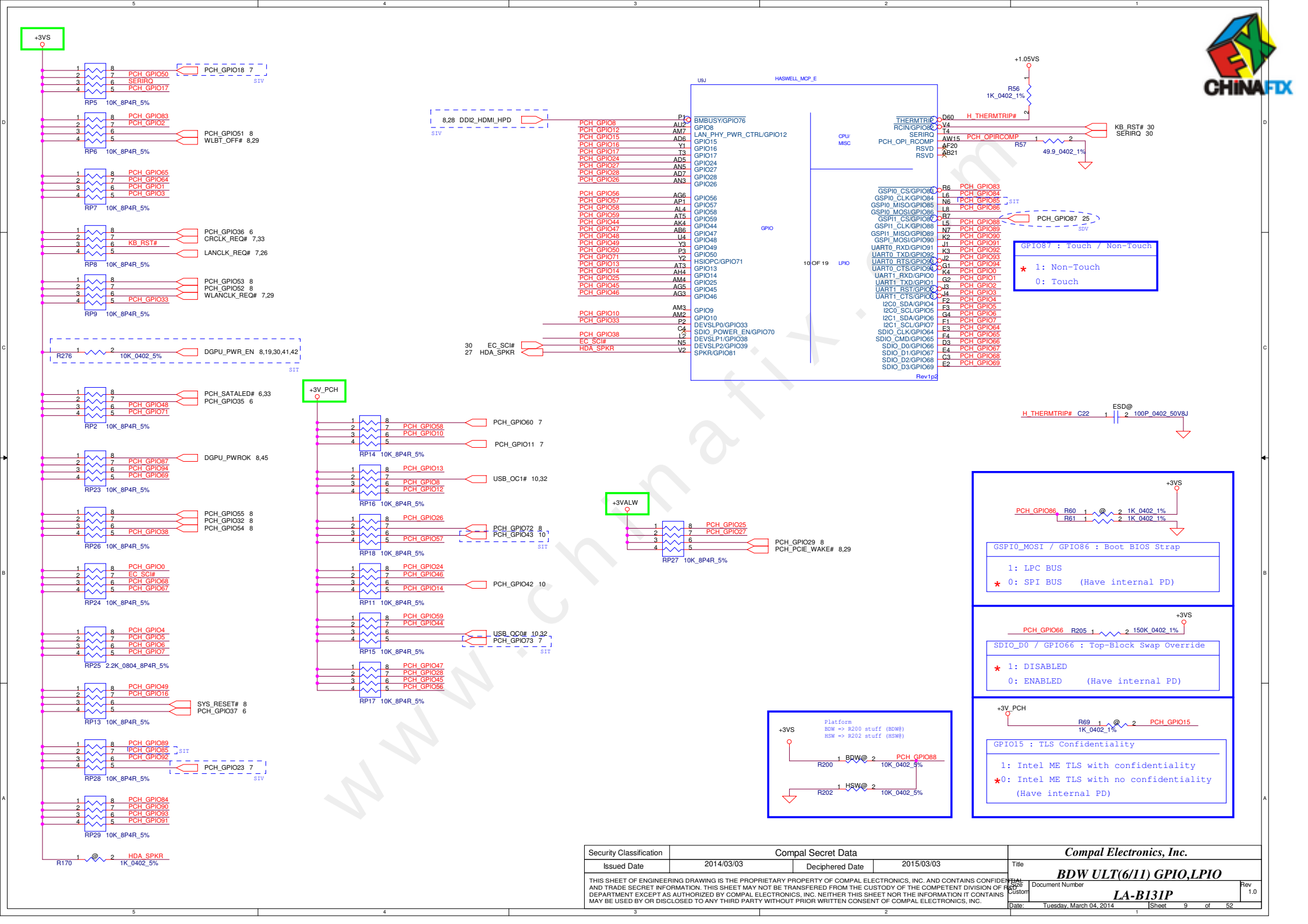
ME debug mode, this signal has a weak internal PD

- * Low = Disabled (Default)
- High = Enabled [Flash Descriptor Security Override]

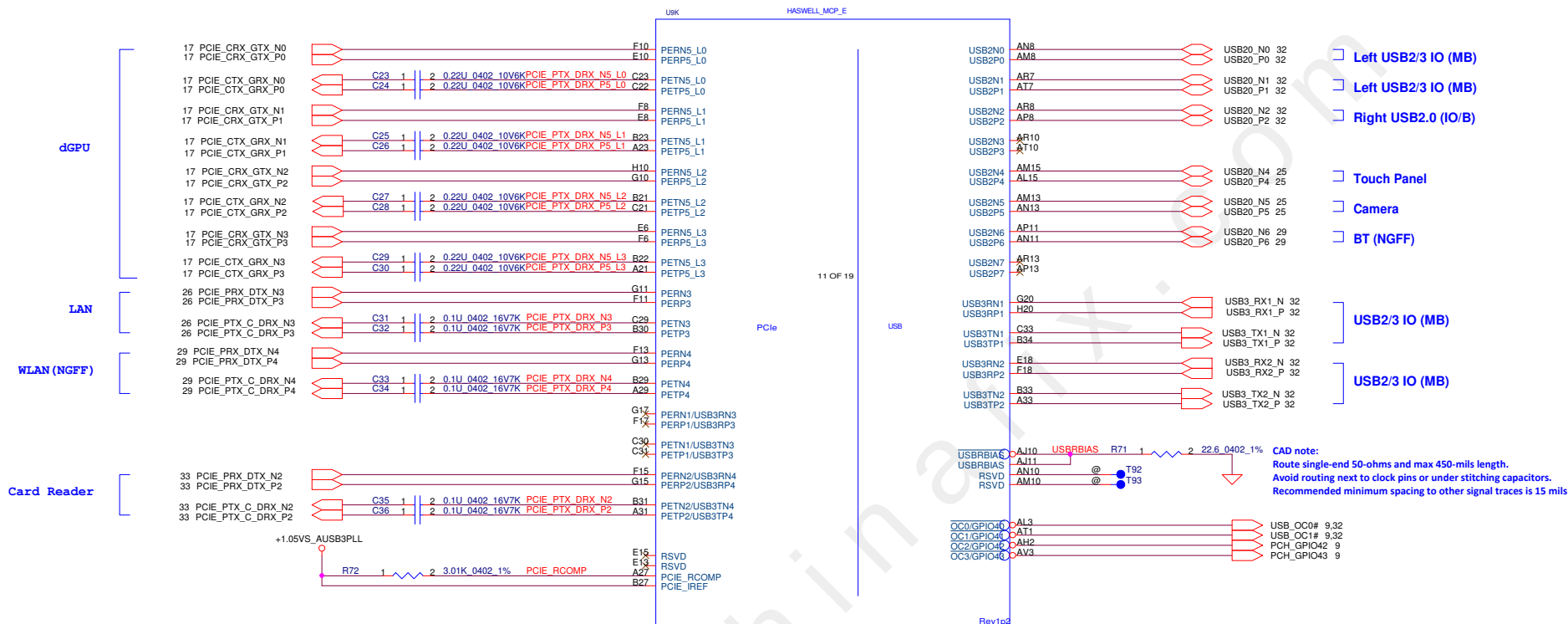


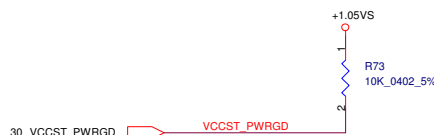
27 HDA_SDIN0



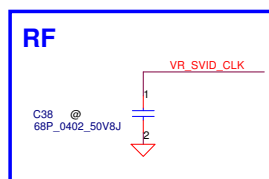
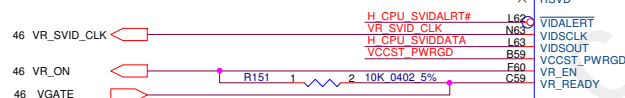


The diagram illustrates the electrical connections for the BDW ULT(6/11) GPIO, LPIO, and I2C. It shows various components like resistors (R170, R200, R202, R205, R276, R56, R60, R61), capacitors (C22), and integrated circuits (U8J, U8K, U8L, U8M, U8N, U8P, U8Q, U8R, U8S, U8T, U8U, U8V, U8W, U8X, U8Y, U8Z, U8AA, U8AB, U8AC, U8AD, U8AE, U8AF, U8AG, U8AH, U8AI, U8AJ, U8AK, U8AL, U8AM, U8AN, U8AO, U8AP, U8AQ, U8AR, U8AS, U8AT, U8AU, U8AV, U8AW, U8AX, U8AY, U8AZ, U8BA, U8BB, U8BC, U8BD, U8BE, U8BF, U8BG, U8BH, U8BI, U8BJ, U8BK, U8BL, U8BM, U8BN, U8BO, U8BP, U8BQ, U8BR, U8BS, U8BT, U8BU, U8BV, U8BW, U8BX, U8BY, U8BZ, U8CA, U8CB, U8CC, U8CD, U8CE, U8CF, U8CG, U8CH, U8CI, U8CJ, U8CK, U8CL, U8CM, U8CN, U8CO, U8CP, U8CQ, U8CR, U8CS, U8CT, U8CU, U8CV, U8CW, U8CX, U8CY, U8CZ, U8DA, U8DB, U8DC, U8DD, U8DE, U8DF, U8DG, U8DH, U8DI, U8DJ, U8DK, U8DL, U8DM, U8DN, U8DO, U8DP, U8DQ, U8DR, U8DS, U8DT, U8DU, U8DV, U8DW, U8DX, U8DY, U8DZ, U8EA, U8EB, U8EC, U8ED, U8EE, U8EF, U8EG, U8EH, U8EI, U8EJ, U8EK, U8EL, U8EM, U8EN, U8EO, U8EP, U8EQ, U8ER, U8ES, U8ET, U8EU, U8EV, U8EW, U8EX, U8EY, U8EZ, U8FA, U8FB, U8FC, U8FD, U8FE, U8FF, U8FG, U8FH, U8FI, U8FJ, U8FK, U8FL, U8FM, U8FN, U8FO, U8FP, U8FQ, U8FR, U8FS, U8FT, U8FU, U8FV, U8FW, U8FX, U8FY, U8FZ, U8GA, U8GB, U8GC, U8GD, U8GE, U8GF, U8GG, U8GH, U8GI, U8GJ, U8GK, U8GL, U8GM, U8GN, U8GO, U8GP, U8GQ, U8GR, U8GS, U8GT, U8GU, U8GV, U8GW, U8GX, U8GY, U8GZ, U8HA, U8HB, U8HC, U8HD, U8HE, U8HF, U8HG, U8HH, U8HI, U8HJ, U8HK, U8HL, U8HM, U8HN, U8HO, U8HP, U8HQ, U8HR, U8HS, U8HT, U8HU, U8HV, U8HW, U8HX, U8HY, U8HZ, U8IA, U8IB, U8IC, U8ID, U8IE, U8IF, U8IG, U8IH, U8II, U8IJ, U8

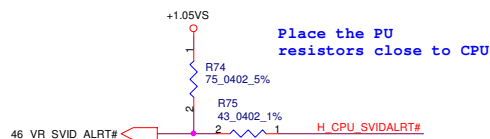




connect to PWR

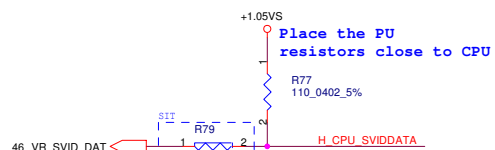


SVID ALERT



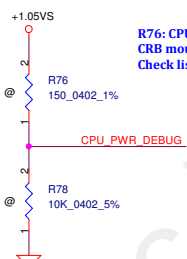
Place the PU resistors close to CPU

SVID DATA

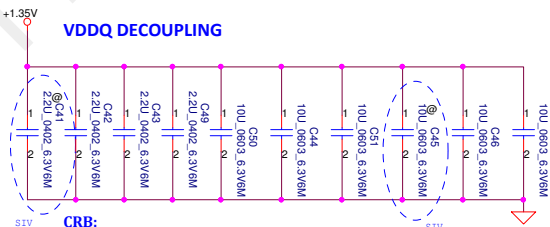


R77: CRB r0.7 changed from 130 Ohms to 110 Ohms

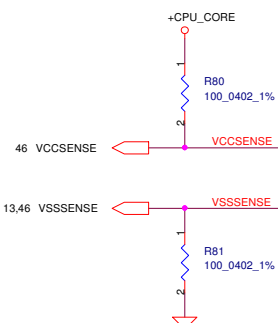
R76: CPU_PWR_DEBUG CRB mount Check list_XDP use only



VDDQ DECOUPLING



CRB:
+1.35V: 470UF/2V/7343 * 2 (Un-mount)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

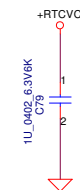
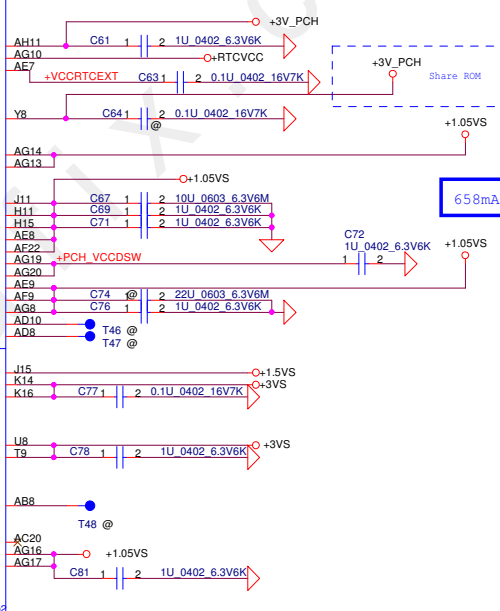
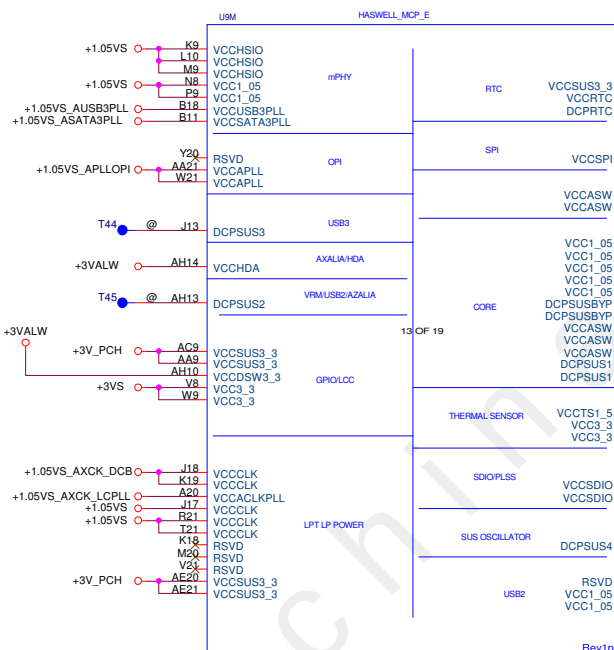
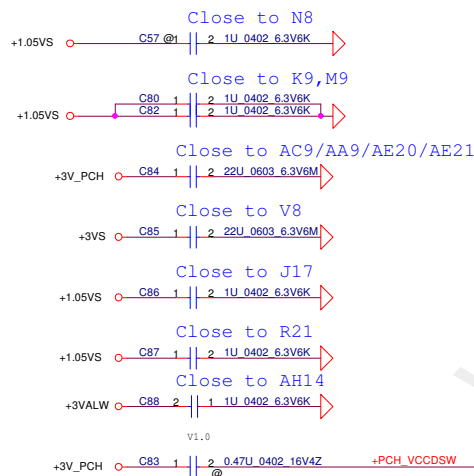
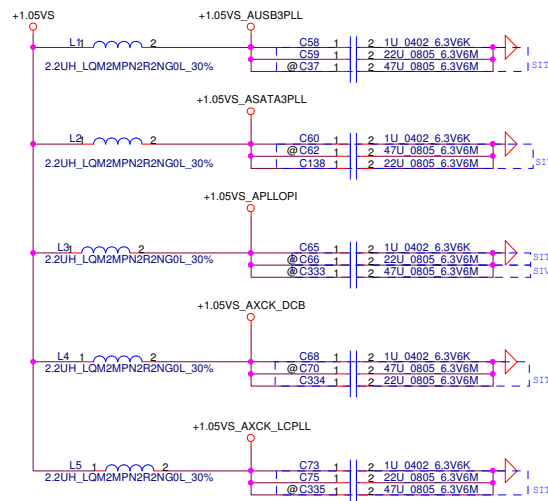


CAD Note: PU resistor should be close to CPU

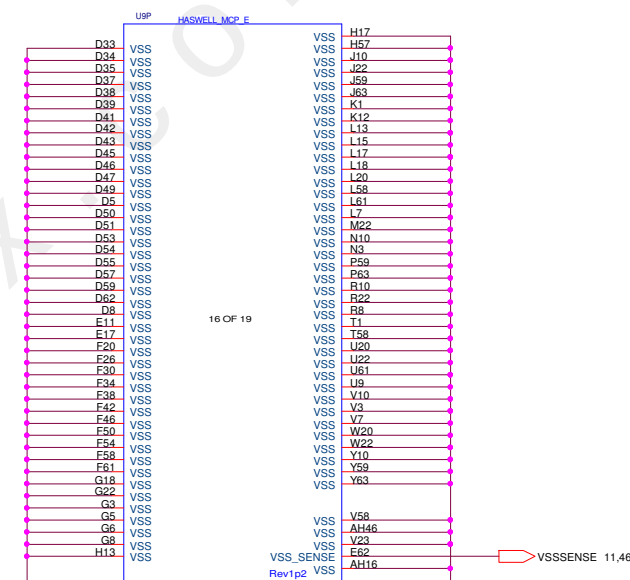
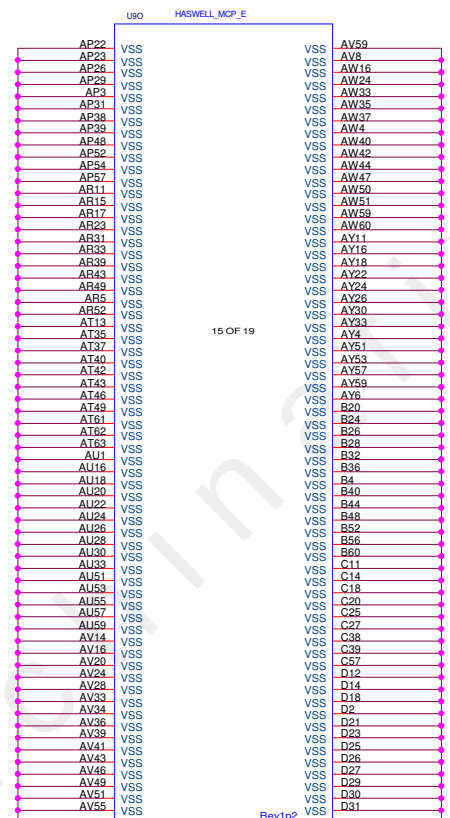
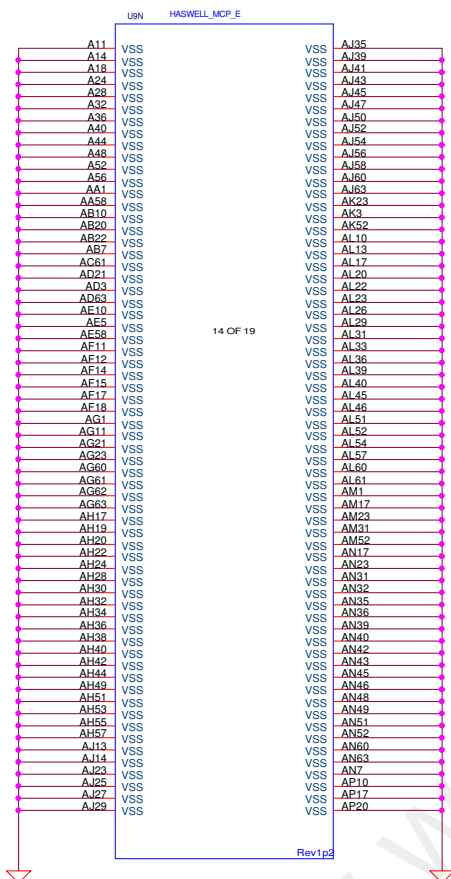
CAD Note: PD resistor should be close to CPU

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Date: Tuesday, March 04, 2014				Sheet 11 of 52				Rev 1.0			

Check Power Source

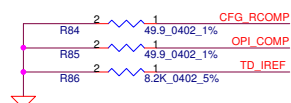
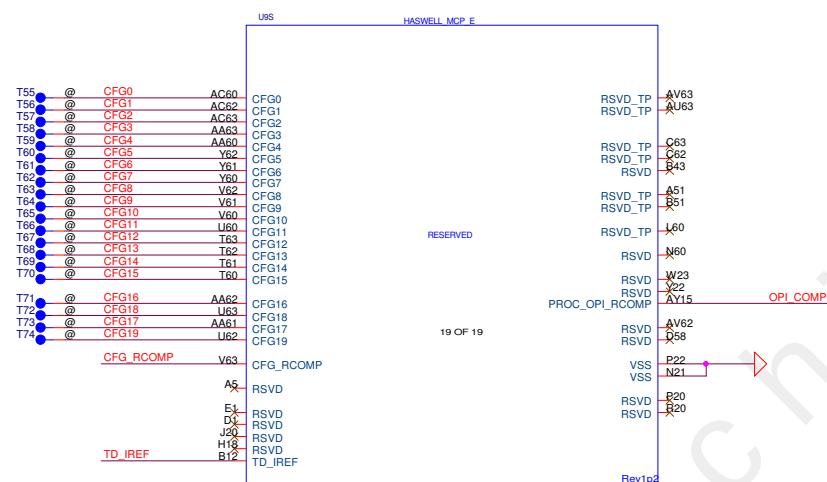
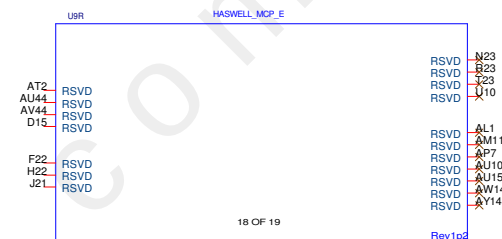


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				Date	Tuesday, March 04, 2014
				Sheet	12 of 52
				Rev	1.0

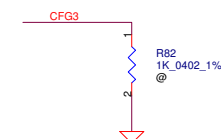


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				BDW ULT(10/11) GND			
				Document Number			
				LA-B131P			
Date: Tuesday, March 04, 2014				Sheet 13 of 52		Rev 1.0	

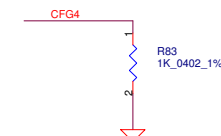
BDW ULT(10/11) GND
LA-B131P



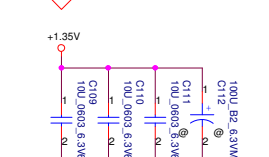
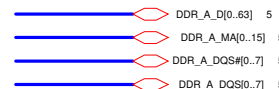
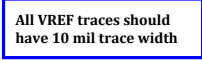
CFG Straps for Processor



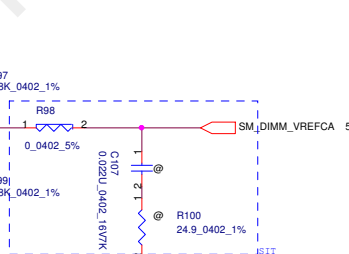
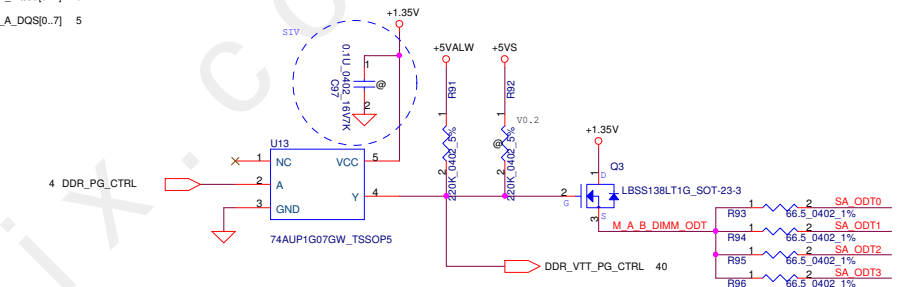
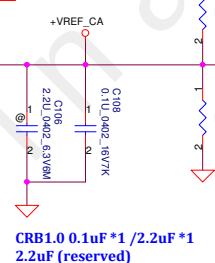
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

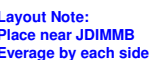
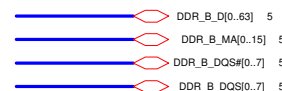
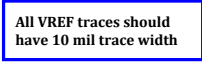


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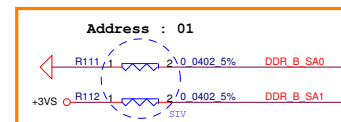


R101 1 2 0 0402 5% DDR A SA0
R102 1 2 0 0402 5% DDR A SA1

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	
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				Custom	1.0
				LA-BI31P	
Date:	Tuesday, March 04, 2014	Sheet	15	of	52



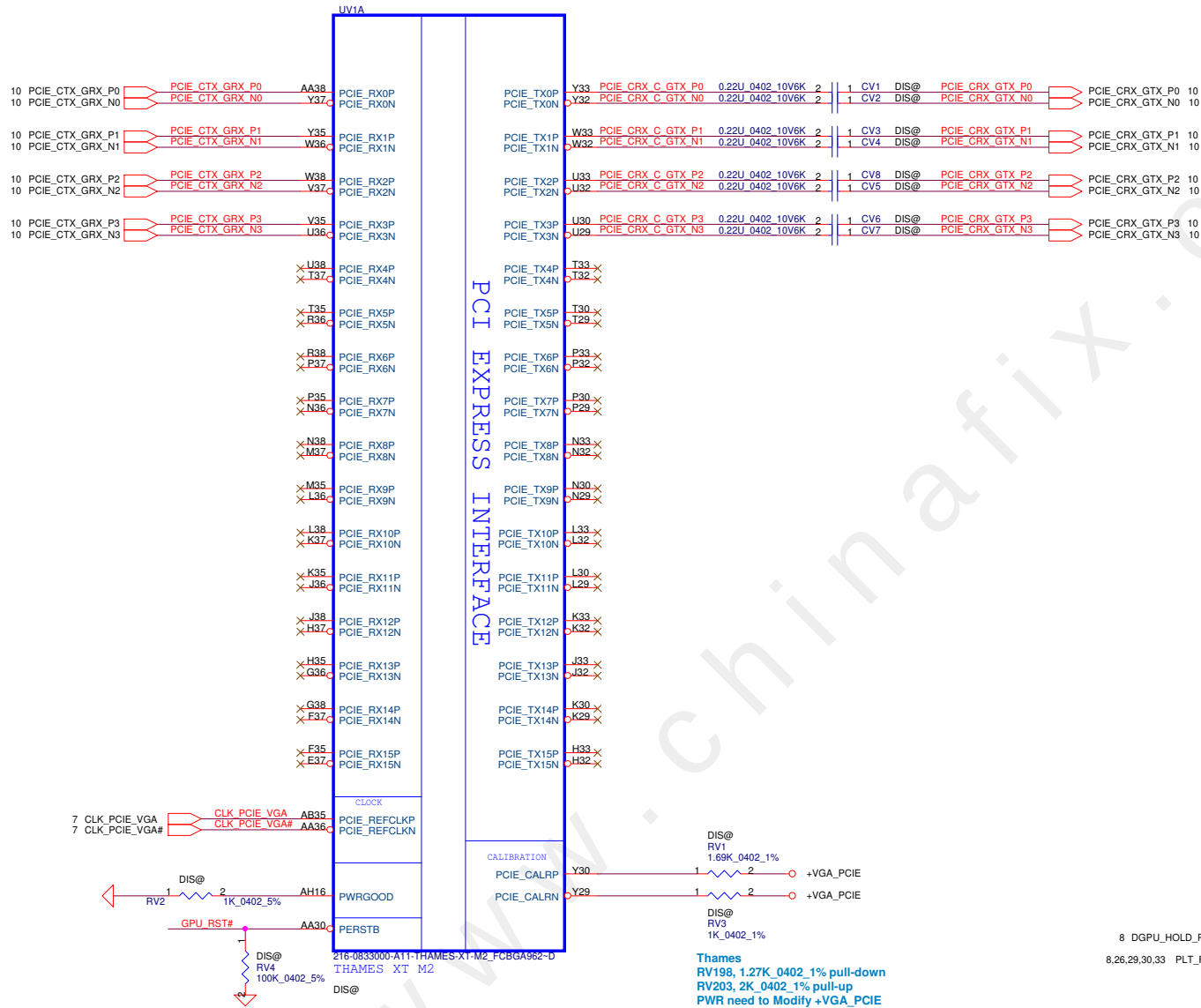
CHANNEL B /TYPE :Reverse / H:4mm
PN:SP07000LT00



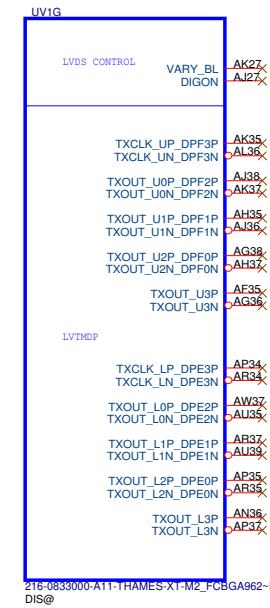
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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title		
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				Size	Document Number	Rev
				Custom	LA-B131P	1.
Date:				Tuesday, March 04, 2014	Sheet 16 of 52	

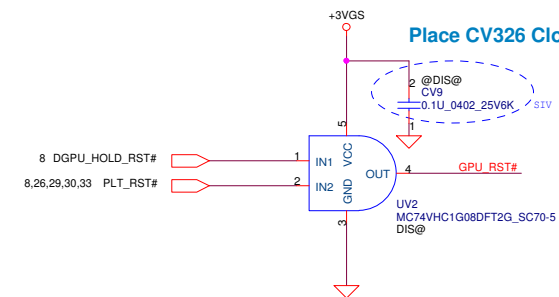
GFX PCIE LANE REVERSAL



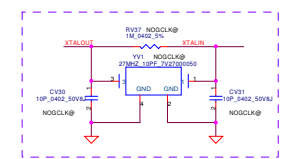
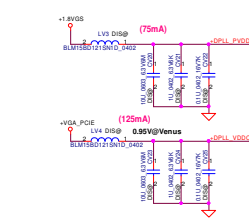
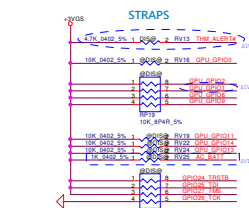
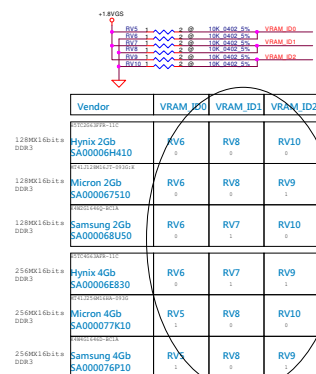
LVDS Interface



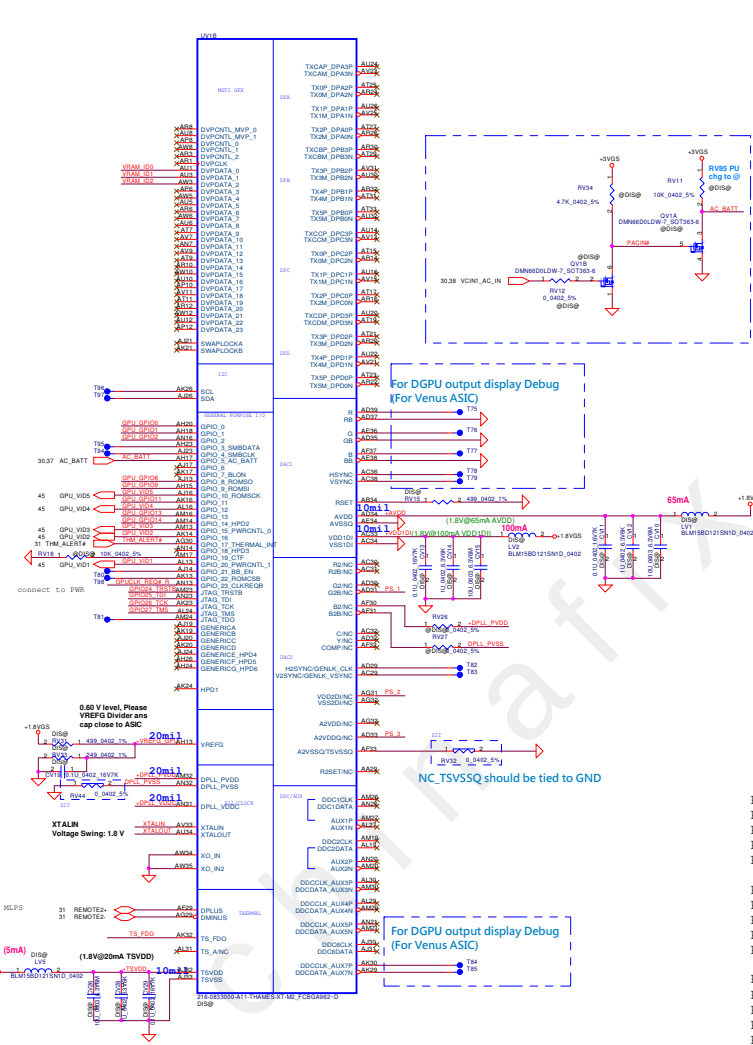
Place CV326 Close to UV13



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				LA-B131P	
				Date: Tuesday, March 04, 2014	Sheet 17 of 52
				Rev 1.0	



SUN internal VGA Thermal Sensor
Address 0x714



For DGPU output display Debug
(For Venus ASIC)

NC_TSVSSQ should be tied to GND

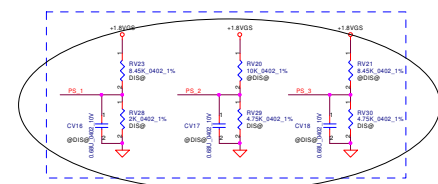
For DGPU output display Debug
(For Venus ASIC)

CONFIGURATION STRAPS				RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPPOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				1 - INSTALL A RESISTOR 2 - DESIGN DEPENDENT NA - NOT APPLICABLE
STRAPS	FIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	
TP1_TWRSS_ENB	GP000	PCIe FSL TX OUTPUT SWING	0: 50k <i>strong</i> 1: 500k <i>weak</i>	X
TP1_DEEMPH_EN	GP001	PCIe TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GP002	Advanced configuration when compliance test	0: 00000000 1: 5057A	0
RSVD	GP008	Reserved		
RSF_VGA_DIS	GP009	VGA ENABLED	0: disabled 1: enabled	X
RSVD	GP010	Reserved		
BIOS_ROM_EN	GP02_22_A0C8B8	ENABLE EXTERNAL BIOS ROM	0: enable 1: enable	X
ROMCFG2[2:0]	GP02[3:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VP_DEVICE_STRAP_ENA	V25[NC]	IGNORE VP DEVICE STRAPS		0
HSYN	HSYN[NC]	HSYN		0
HSYN	GENERIC	GENERIC		0
AD[2:1]	HSYN	AD[2:1] AUDIO		11
AD[0]	V25[NC]	AD[0] AUDIO		

ALLOW RESERVED CONFIGURATION STRAPS
AND FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR, IF THESE GPPOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GP002	HSYN	GENERIC	GP02	GP08
-------	------	---------	------	------

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



VENUS MLPs
PS_3 used default

```

PS0_[1] = 1
PS0_[2] = 0 For a 256-MB aperture size, PS0_0[3:1] is set to 001
PS0_[3] = 0
PS0_[4] = 1 Must be 1 at reset.
PS0_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

PS1_[1] = 1 PCIe GEN3 is supported = 1
PS1_[2] = 0 Must be 0 at reset.
PS1_[3] = 0 Must be 0 at reset.
PS1_[4] = 1 Full Tx output swing = 1
PS1_[5] = 1 Tx deemphasis enabled = 1

PS2_[1] = 0 Reserved
PS2_[2] = 0 Reserved
PS2_[3] = 0 Disable the external BIOS ROM device = 1
PS2_[4] = 1 The device will not be recognized as the system's VGA controller = 1
PS2_[5] = 1 Reserved

PS3_[1] = 0 Reserved
PS3_[2] = 0 Reserved
PS3_[3] = 0 Reserved
PS3_[4] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS3_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

```

Security Classification	Compul Secret Data		Compul Electronics, Inc. Venus XTX(2/8) Main Gen	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title Venus XTX(2/8) Main Gen Size Document Number LA-B13P Date 1984, March 04, 2014 Page 18 of 55

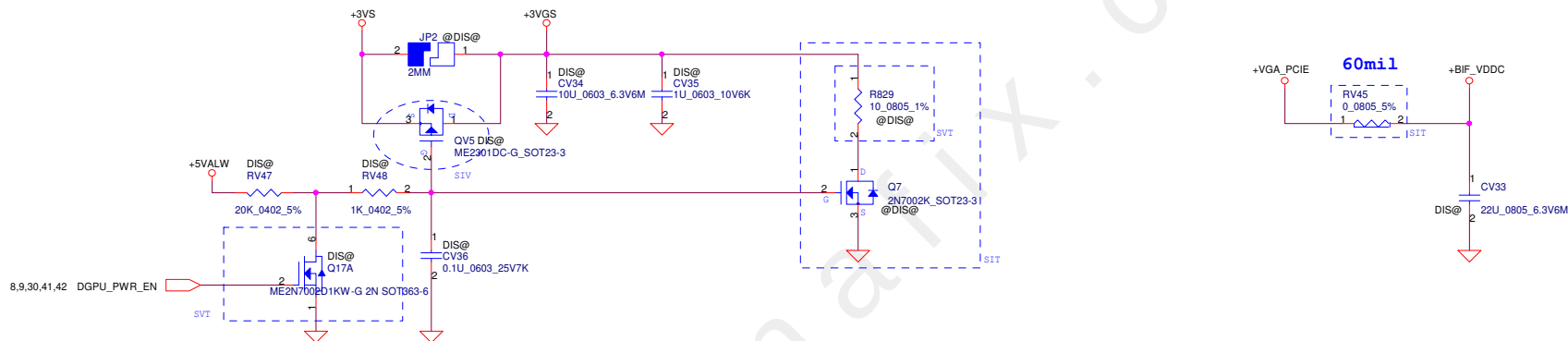
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

Note:

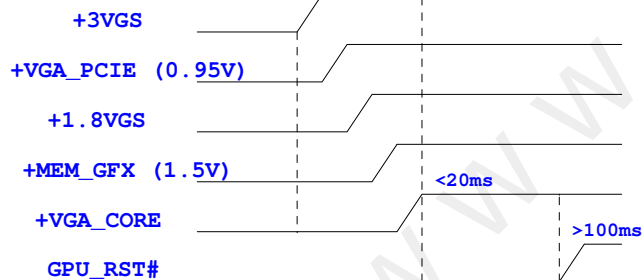
PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

Switch circuits in BACO desings for Thames/Seymour only 55mA@1.0V, in BACO mode

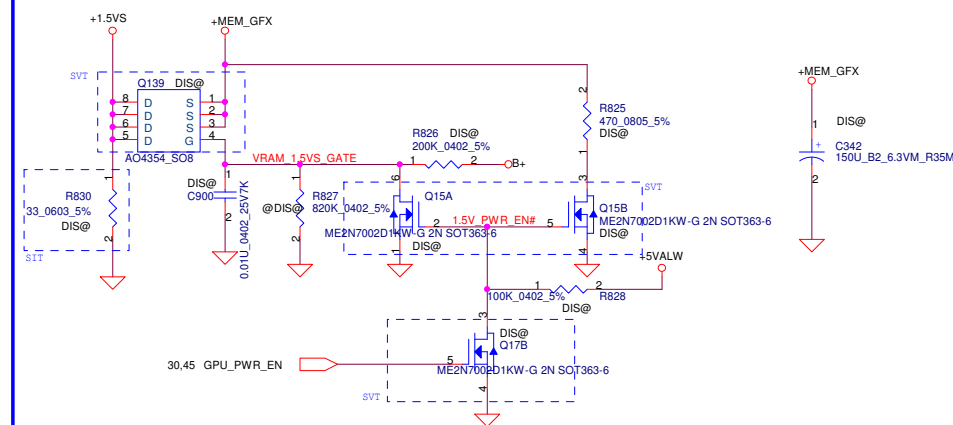
+3VS TO +3VGS



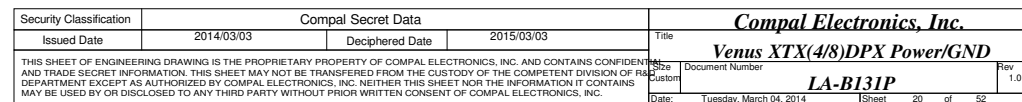
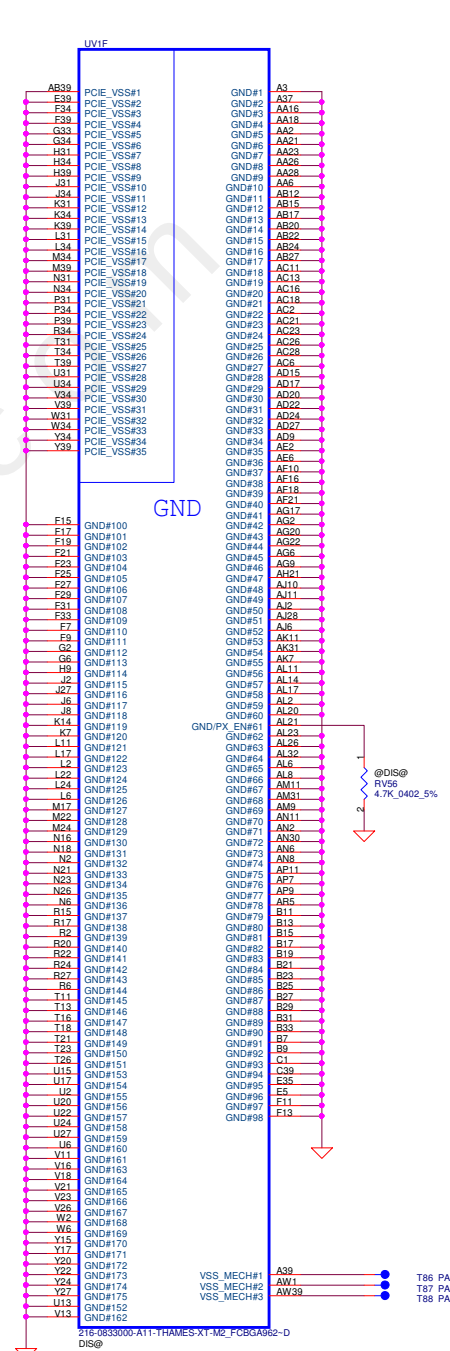
Power sequence of Venus XTX

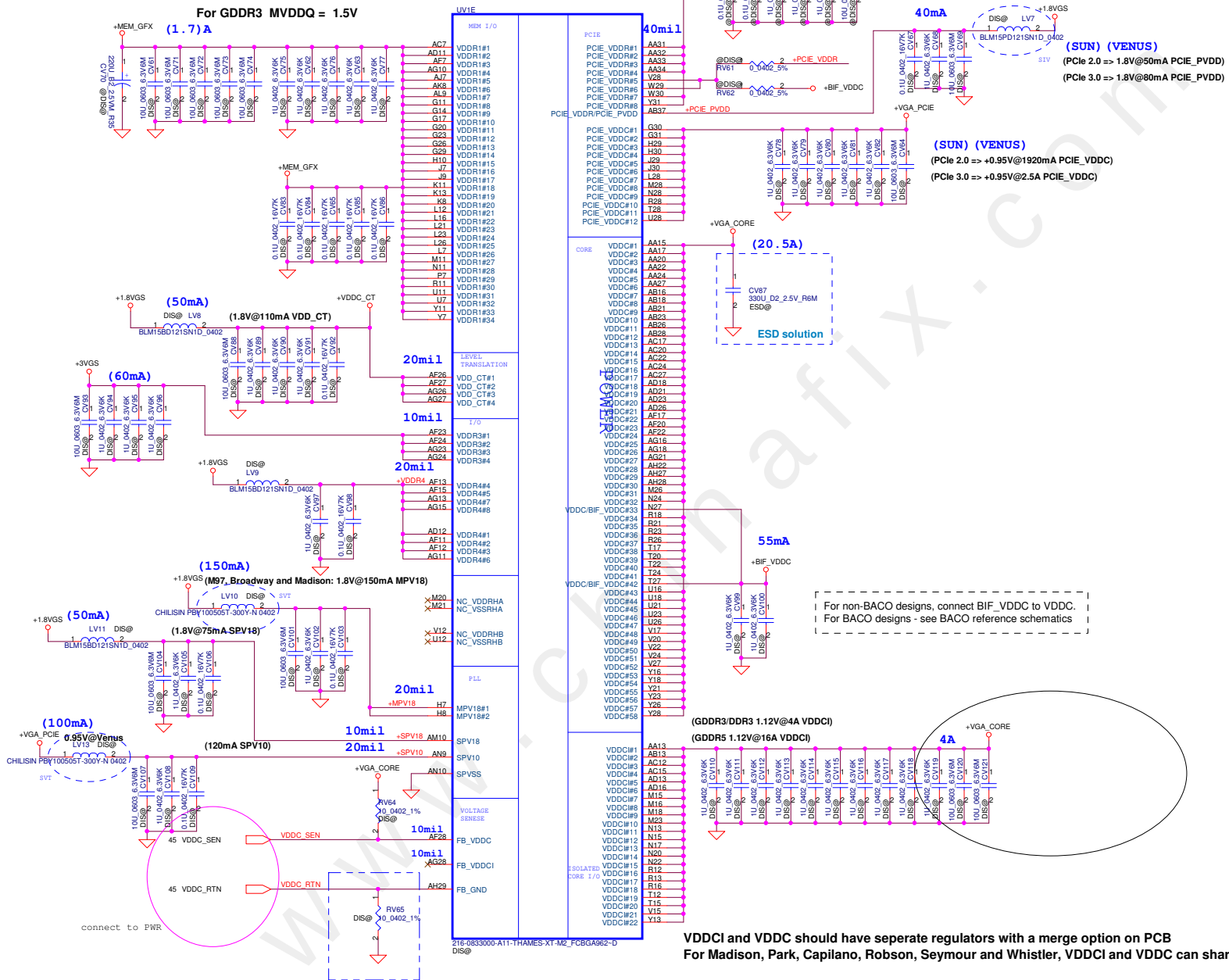


+1.5VS to +MEM_GFX



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				Custom	1.0
				Date	Tuesday, March 04, 2014
				Sheet	19 of 52

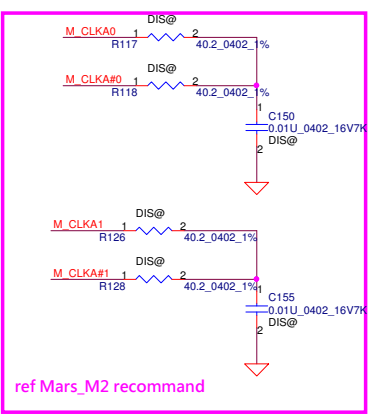
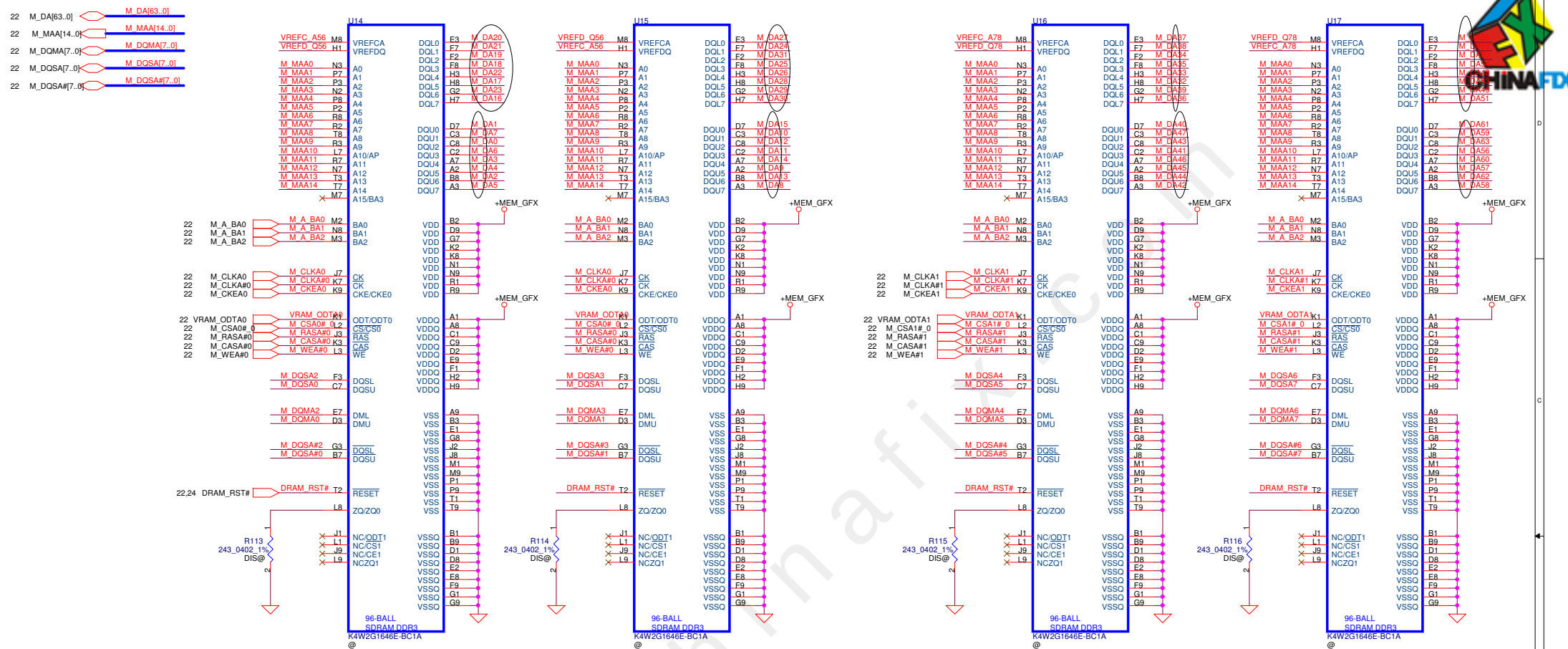




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Date:	Tuesday, March 04 2014	Sheet	21	of	50	

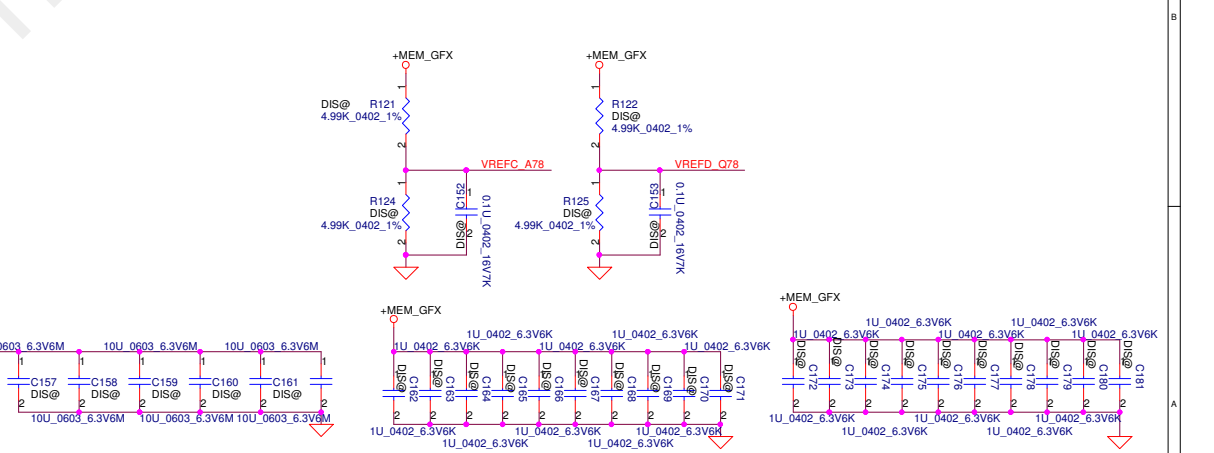


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				LA-B131P			
				Date	Tuesday, March 04, 2014	1 Sheet	22 of 52

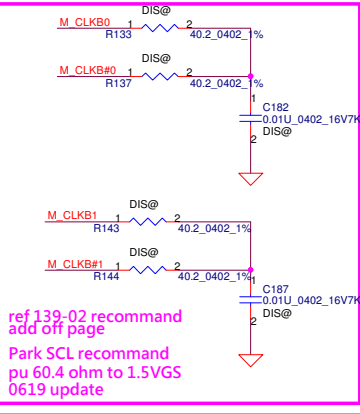
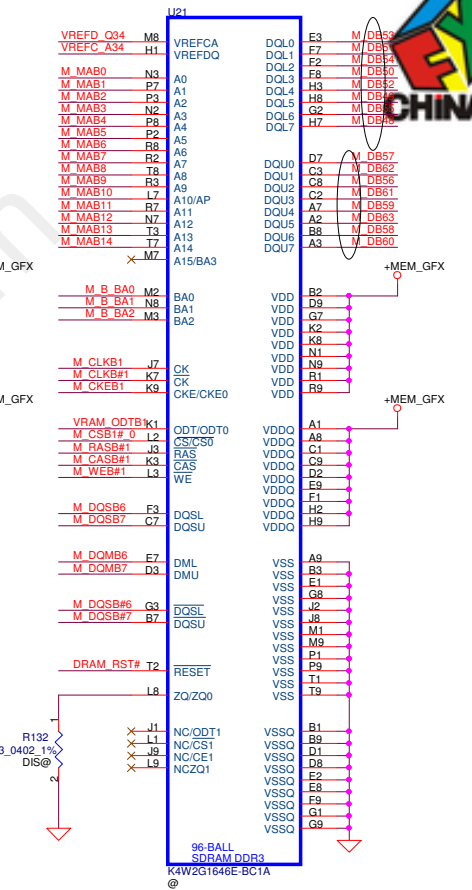
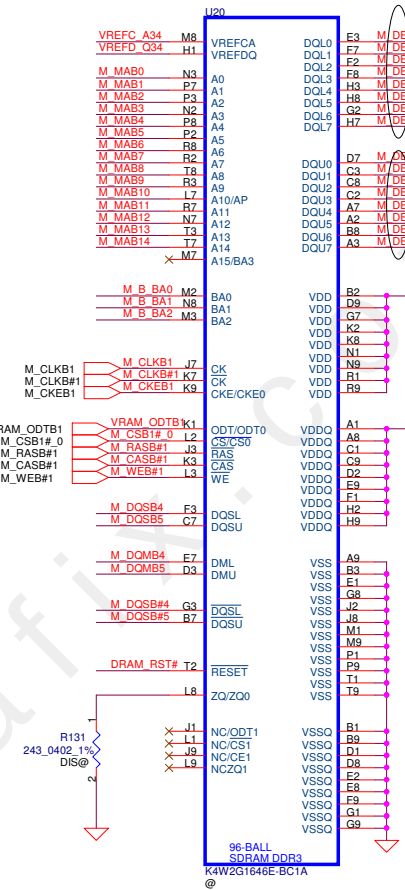
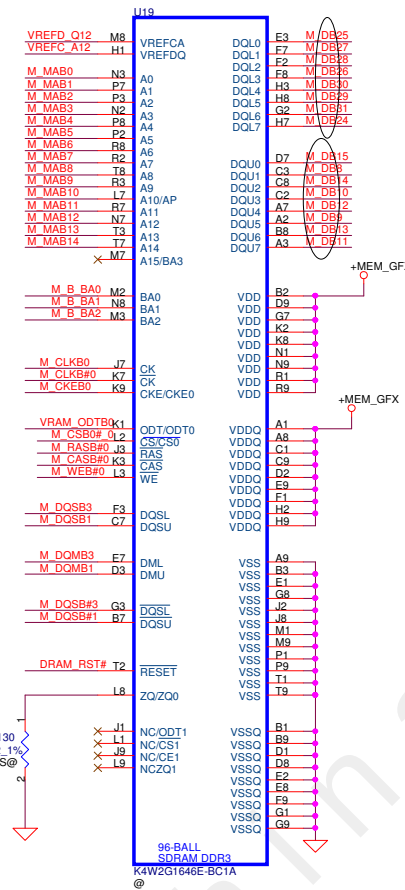
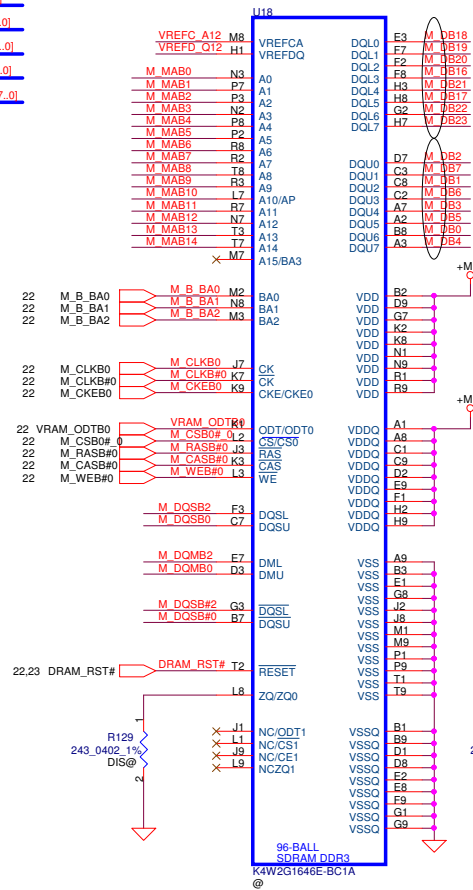


VRAM P/N :
Hynix : SA00003YO40 (S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A!)
Samsung : SA000047Q30 (S IC D3 128M16 K4W2G1646C-HC11 96P C38A!)
update VRAM PN

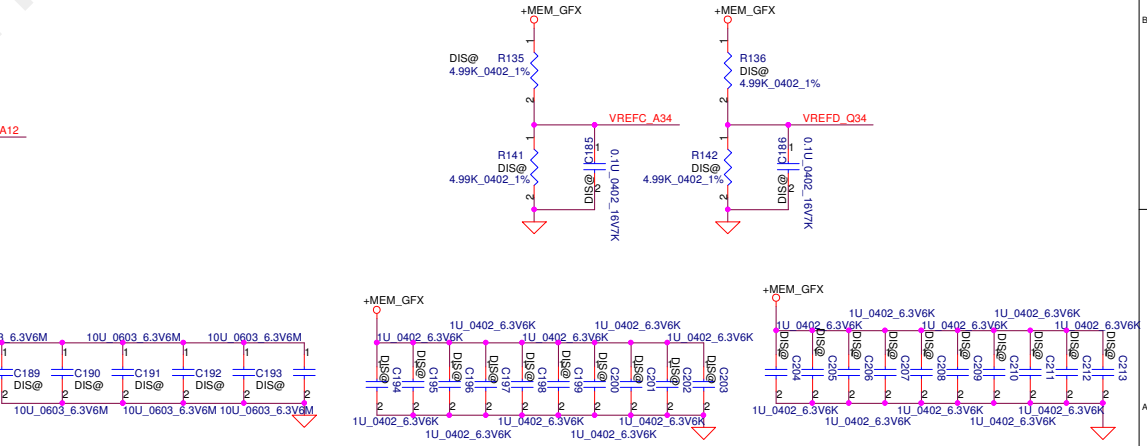
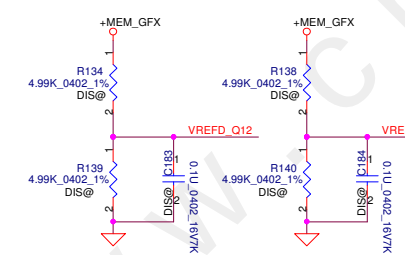
Place across each VDDIO-GND plane seam



22 M_DB[63..0] M_DB[63..0]
 22 M_MAB[14..0] M_MAB[14..0]
 22 M_DQMB[7..0] M_DQMB[7..0]
 22 M_DQSB[7..0] M_DQSB[7..0]
 22 M_DQSB[7..0] M_DQSB[7..0]

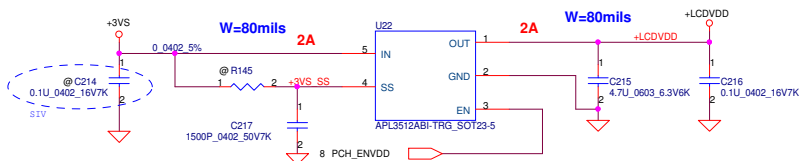


ref 139-02 recommend
 add off page
 Park SCL recommend
 pu 60.4 ohm to 1.5VGS
 0619 update
 VRAM P/N :
 Hynix : SA00003YO40 (S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A!)
 Samsung : SA000047Q30 (S IC D3 128M16 K4W2G1646C-HC11 96P C38A!)
 update VRAM PN

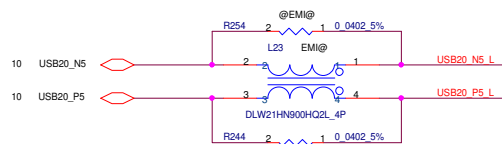
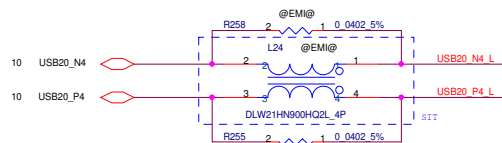


Place across each VDDIO-GND plane seam

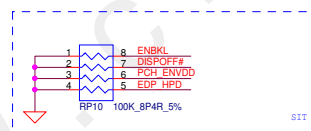
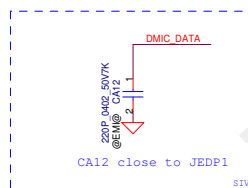
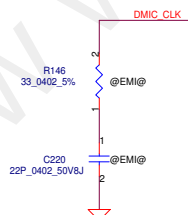
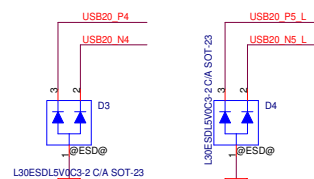
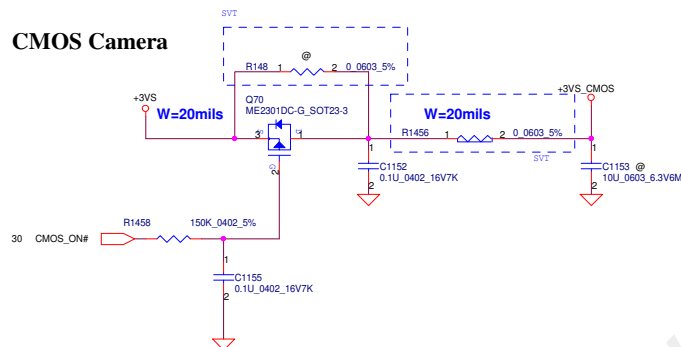
LCD POWER CIRCUIT



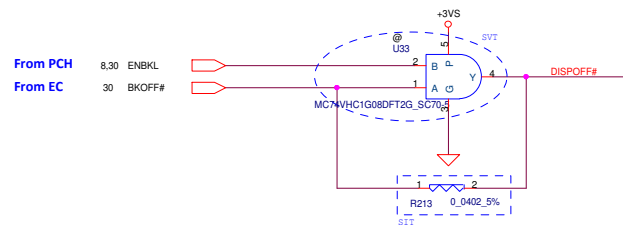
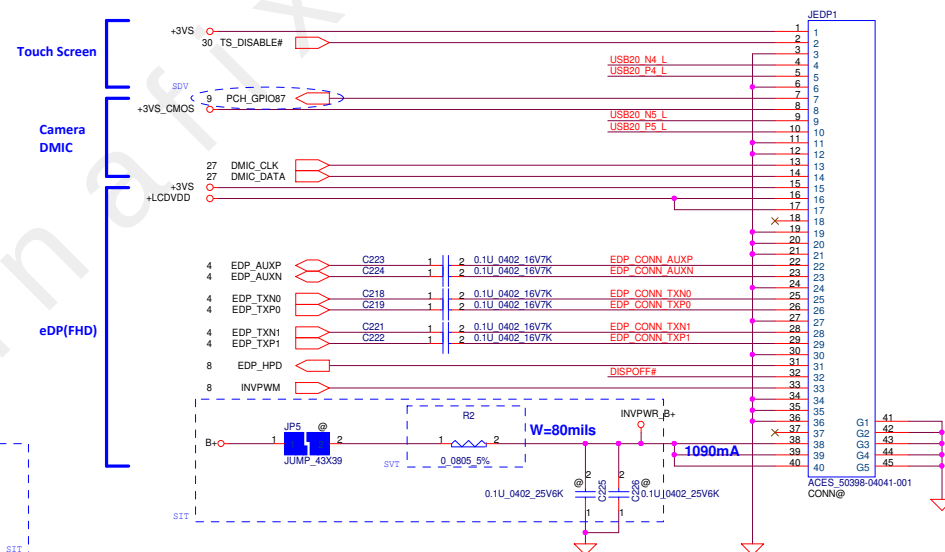
C217 Resevre for APL3512A
R145 Resevre for G5243AT11U



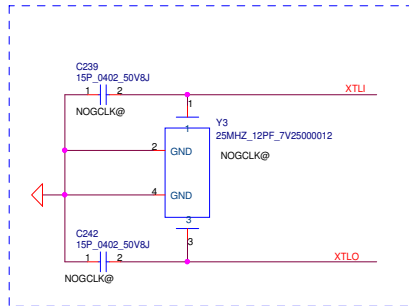
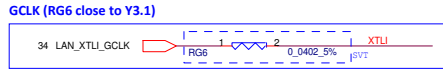
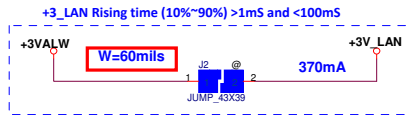
CMOS Camera



eDP(FHD) + TOUCH + Camera

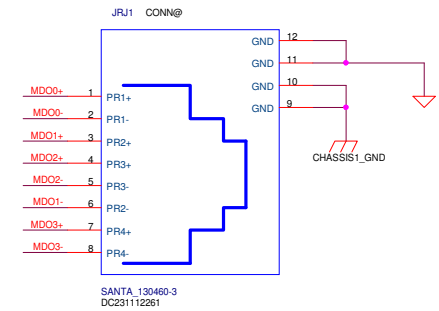
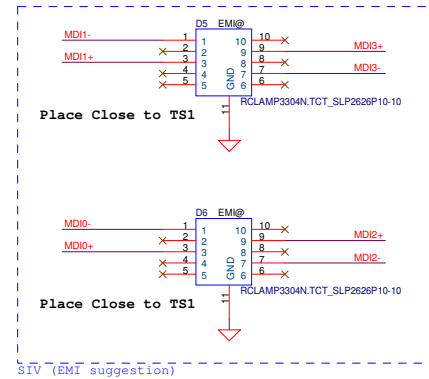
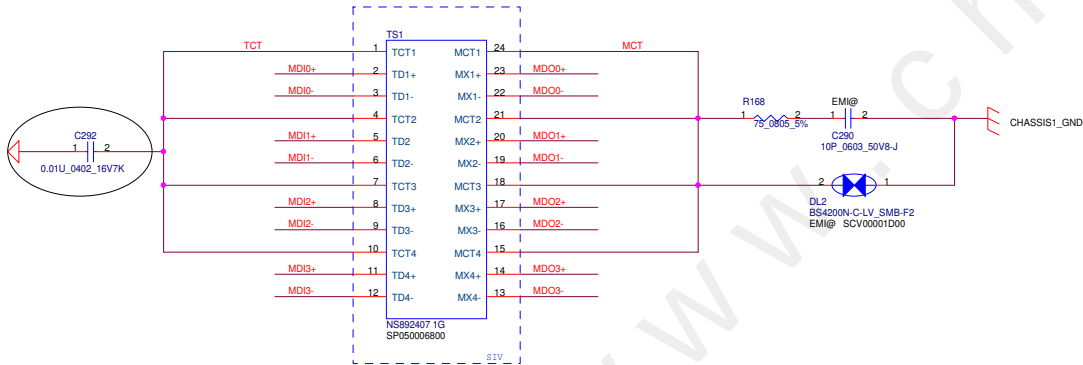
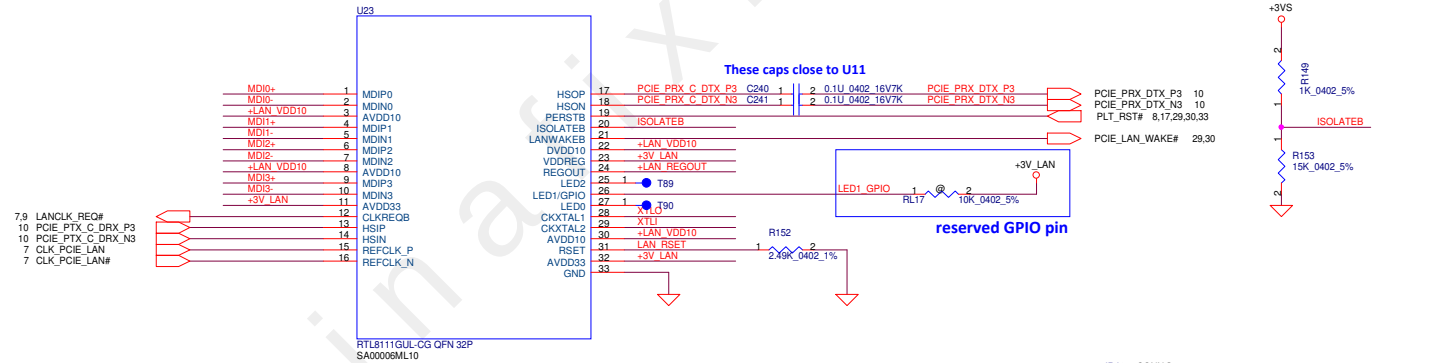
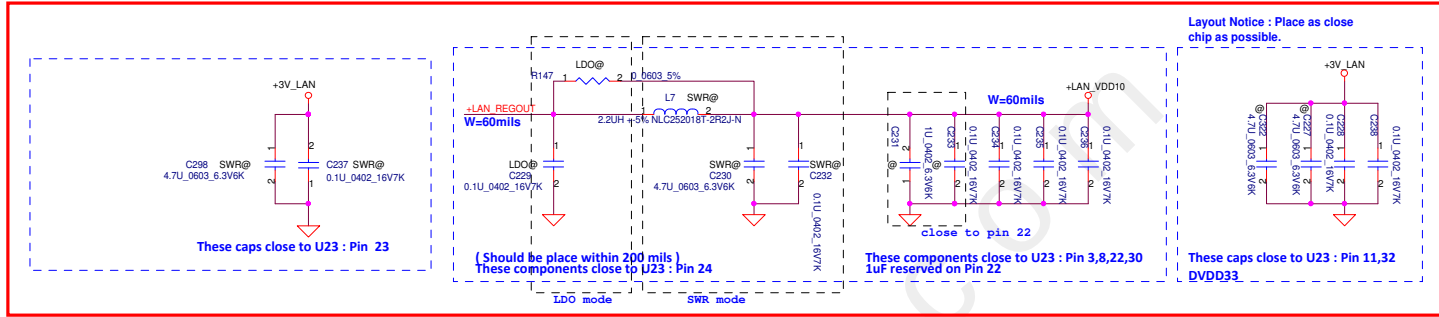


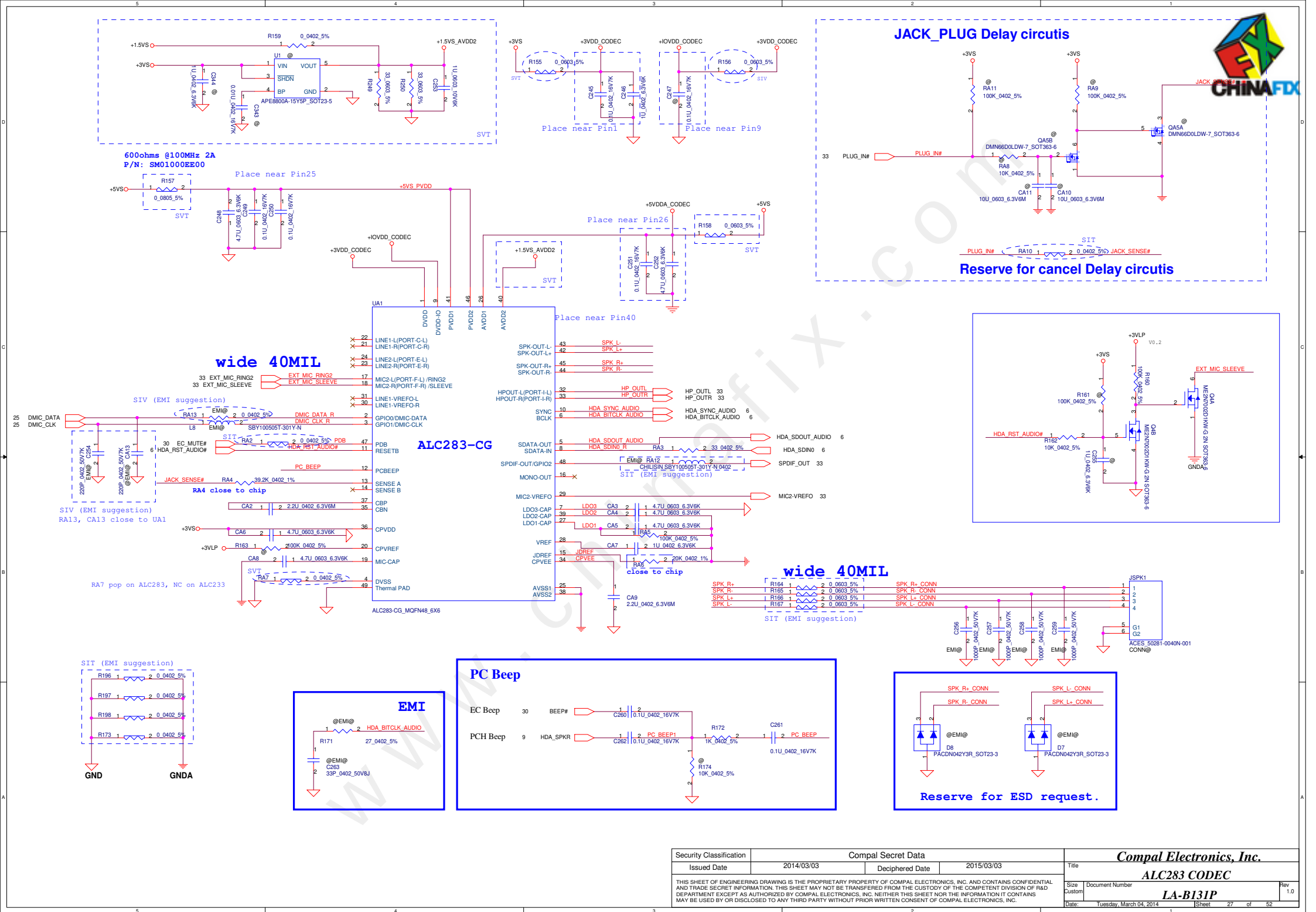
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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	<i>eDP LCD / Camera / Touch</i>	
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				Date	Tuesday, March 04, 2014	Sheet 25 of 52



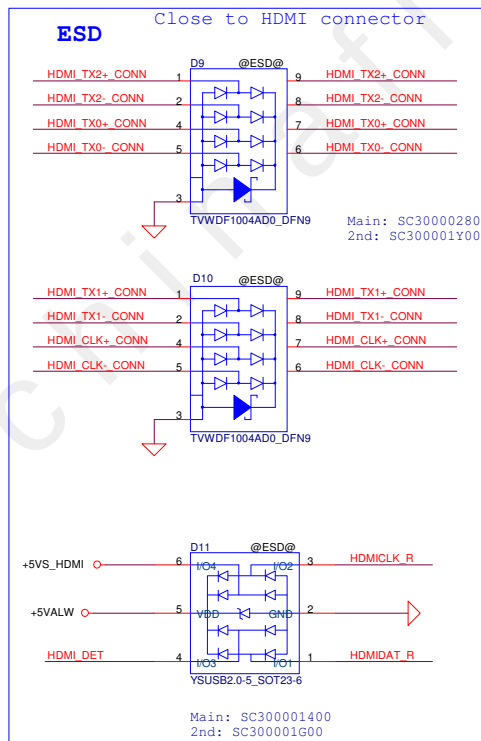
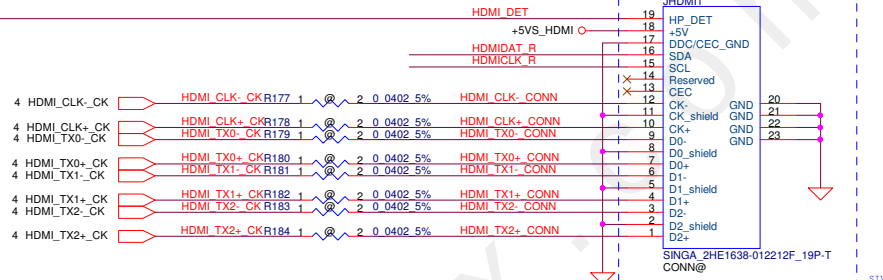
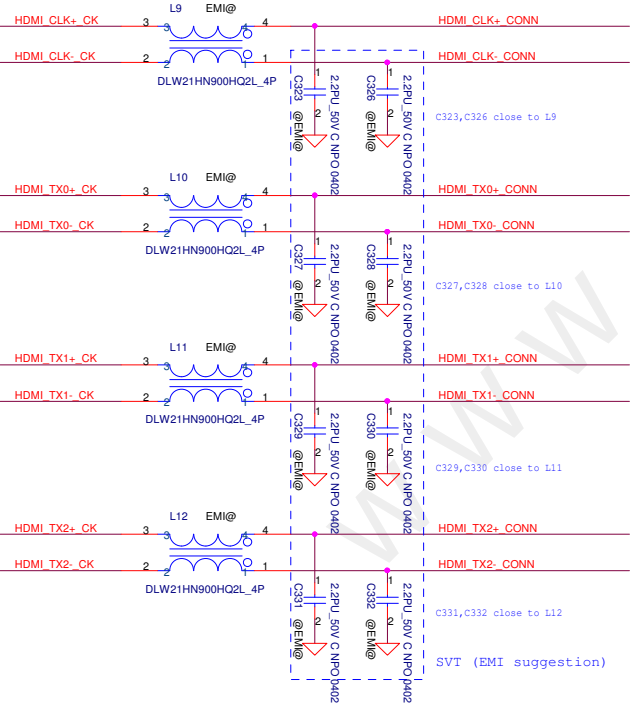
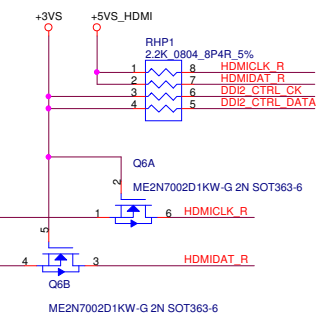
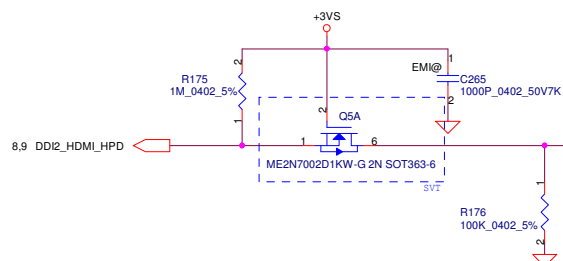
RTL8111GS	L7	C230	C298	R147	C229
SWR mode	O	O	O	X	X

RTL8111G	L7	C230	C298	R147	C229
LDO mode	X	X	X	O	O

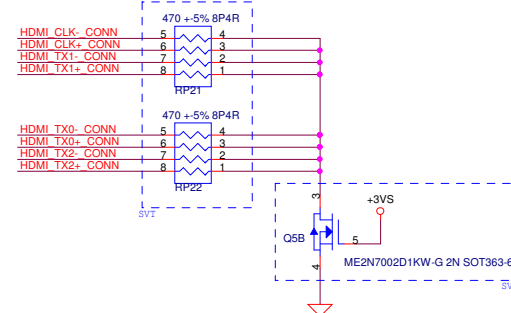




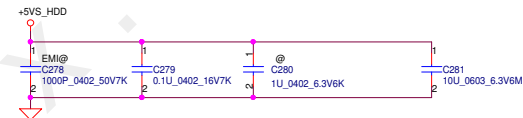
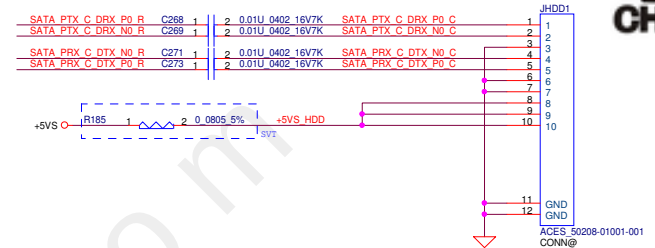
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		ALC283 CODEC	
2014/03/03		2015/03/03		Rev	
1.0		1.0		LA-B131P	
Date		Tuesday, March 04, 2014		Sheet	
27		of		52	



SD309470080
S ROW RES 1/16W 470 +5% 8P4R 0804



Security Classification		Compal Secret Data		Title	
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				LA-B131P	1.0
				Date: Tuesday, March 04, 2014	Sheet 28 of 52

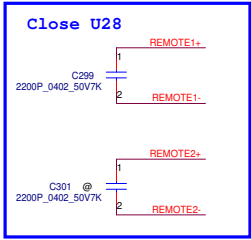


For Power consumption Measurement

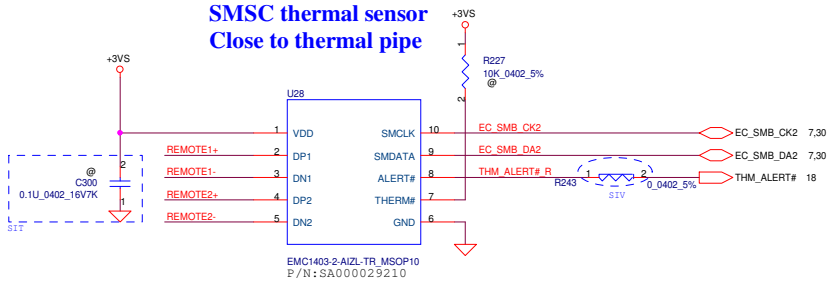


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HDD/NGFF(WLAN+BT)	
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				Custom	LA-B131P	1.0
				Date:	Tuesday, March 04, 2014	Sheet 29 of 52

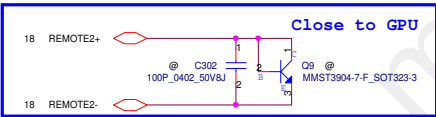
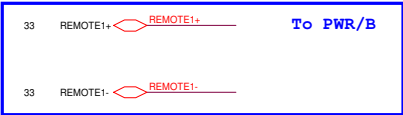
Thermal Sensor



SMSC thermal sensor
Close to thermal pipe

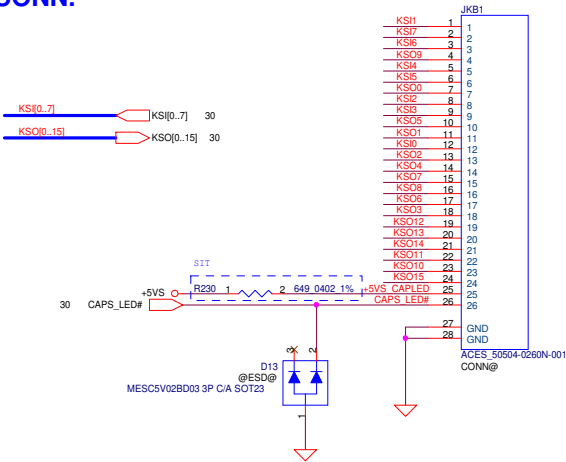


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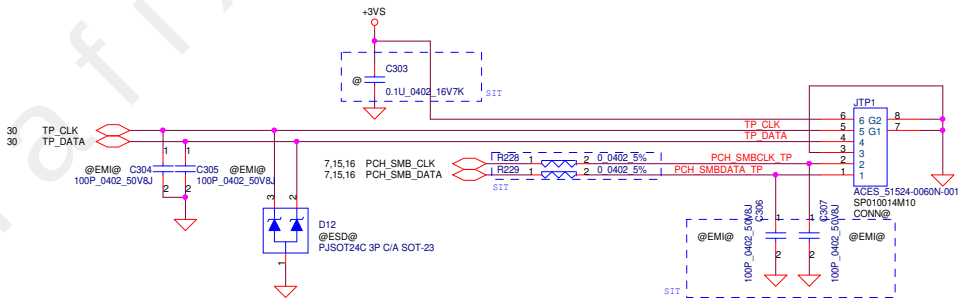


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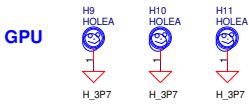
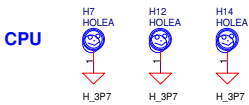
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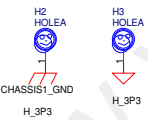
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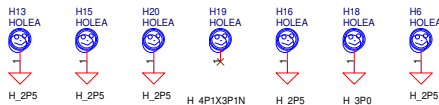
Screw



LAN



Board side



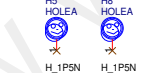
NGFF



Fan

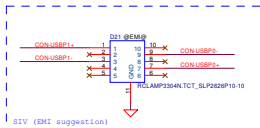
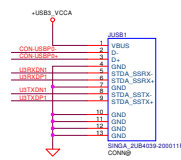
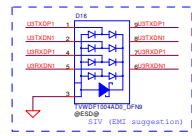
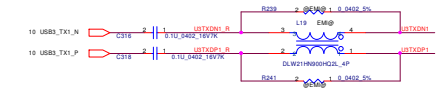
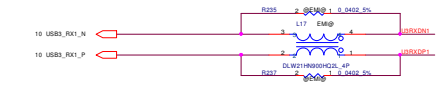
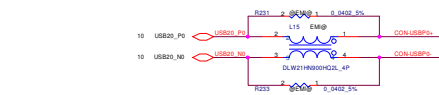
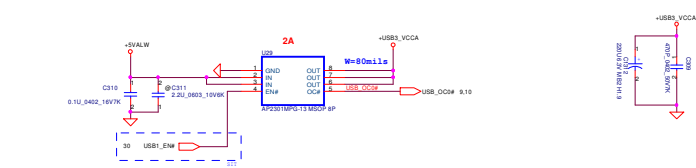


Zero point

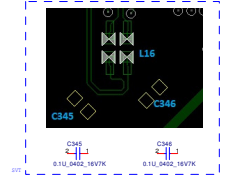


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	KB/TP/Thermal Sensor
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				LA-B131P	
				Date: Tuesday, March 04, 2014	Sheet 31 of 52

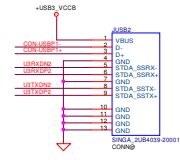
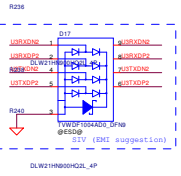
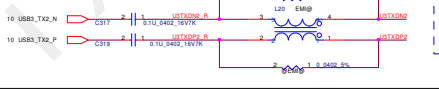
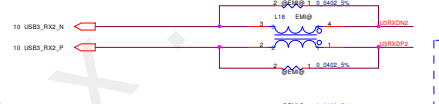
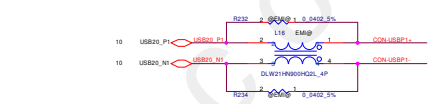
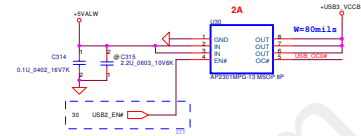
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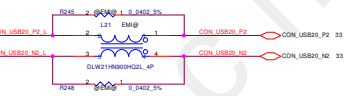
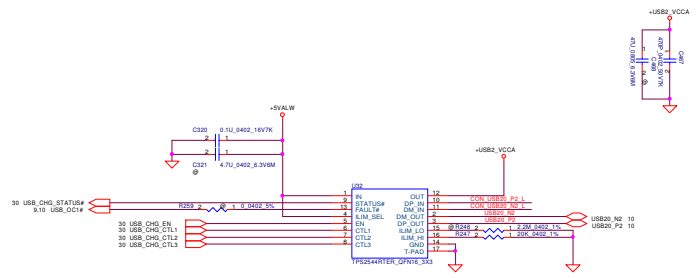
Pseudo Cap(C345, C346) to protect L16



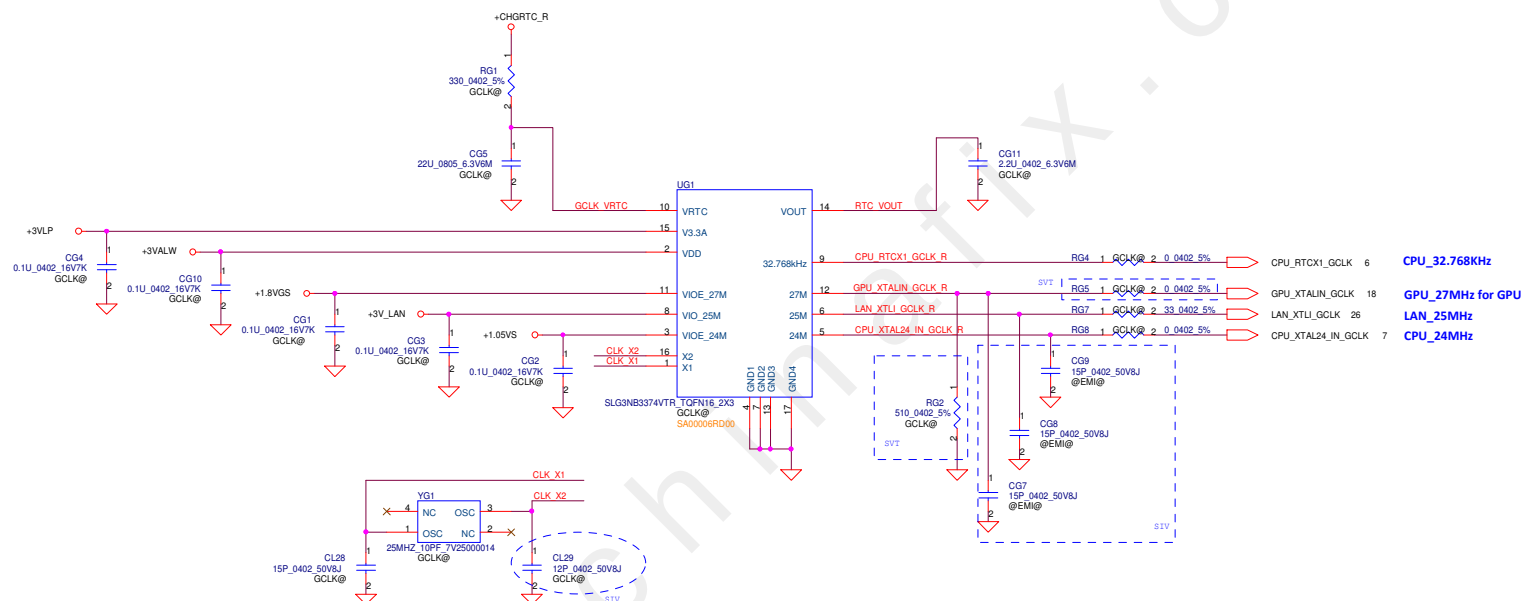
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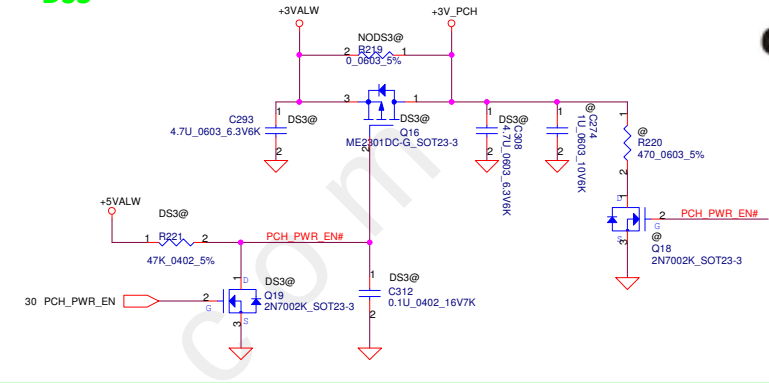
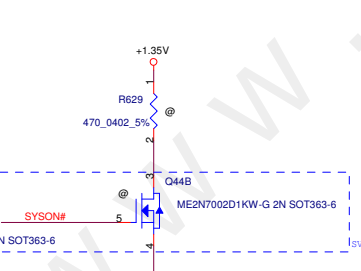
USB2.0 + Charger



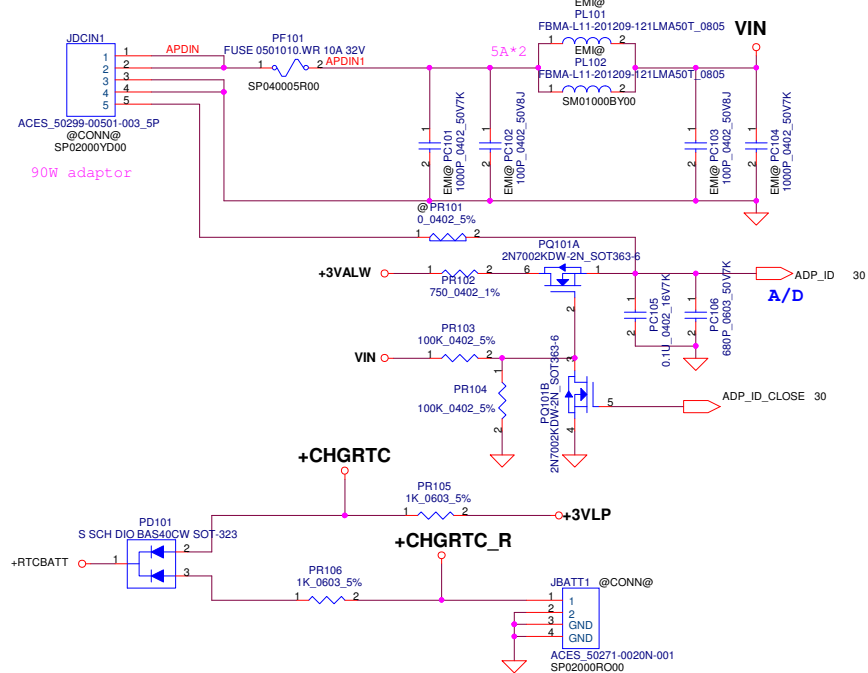
Security Classification	Confidential	Compal Secret Data	Y/N	Compal Electronics, Inc.
Issued Date	2014/03/03	Disciplined Date	2015/03/03	Y/N
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Doc. No.	LA-B131P	Doc. Name	LA-B131P	Rev. 1.4
Issue	1	Issue Date	2014.03.03	Rev. 1.4



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				Size	Document Number	Rev
					LA-B131P	1.0
Date: Tuesday, March 04, 2014				Sheet	34	of 52

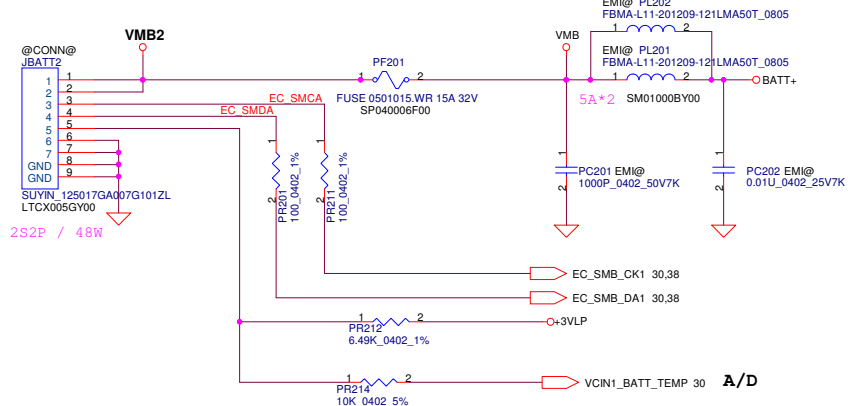


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/03	Deciphered Date	2015/03/03	DC/DC Interface		
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				Custom	LA-B131P	1.0
Date:				Tuesday, March 04, 2014	Sheet	35 of 52

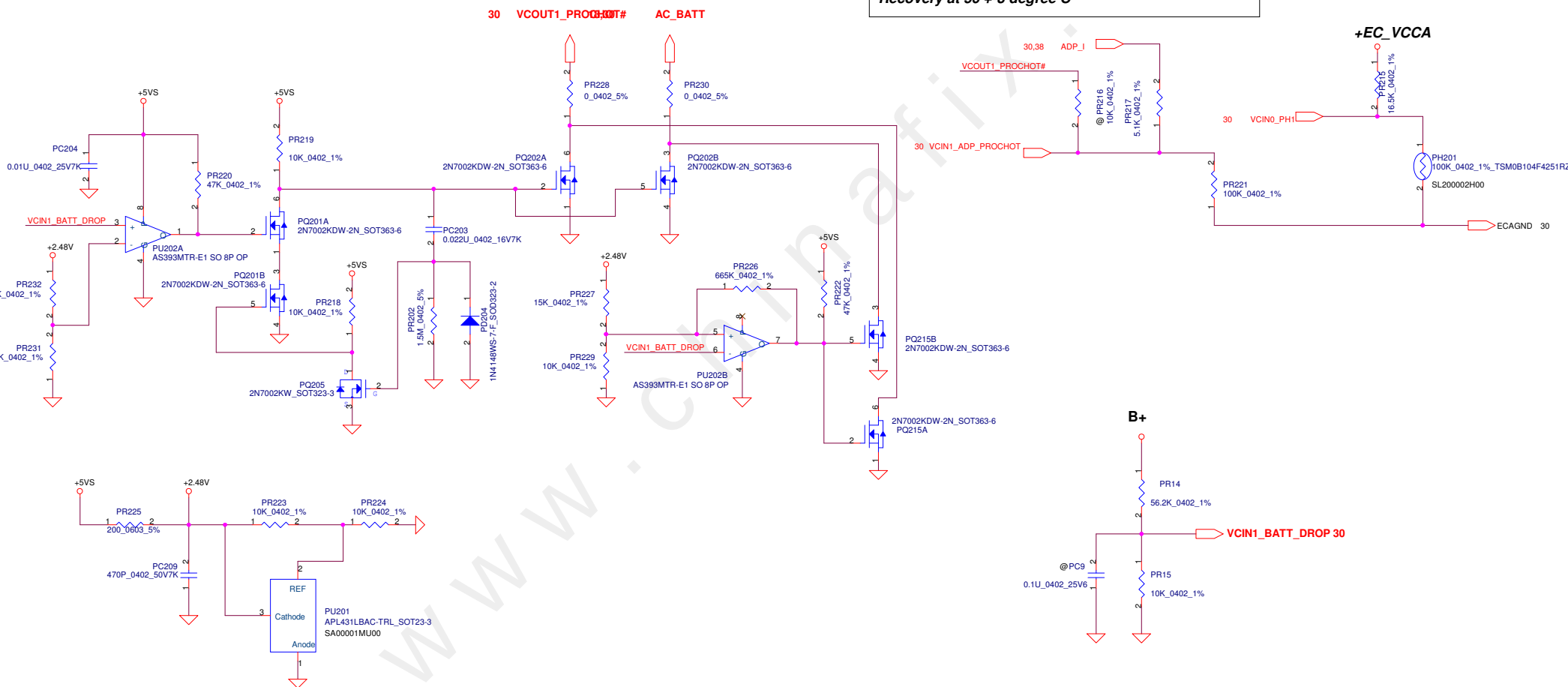


RTC Battery GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C
30MM

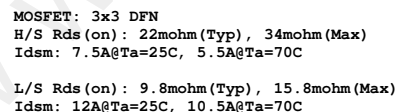
Security Classification		Compal Secret Data		Title	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	PWR DCIN / RTC Battery	
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				BE BDW	1.0
				Date: Tuesday, March 04, 2014	Sheet 36 of 52



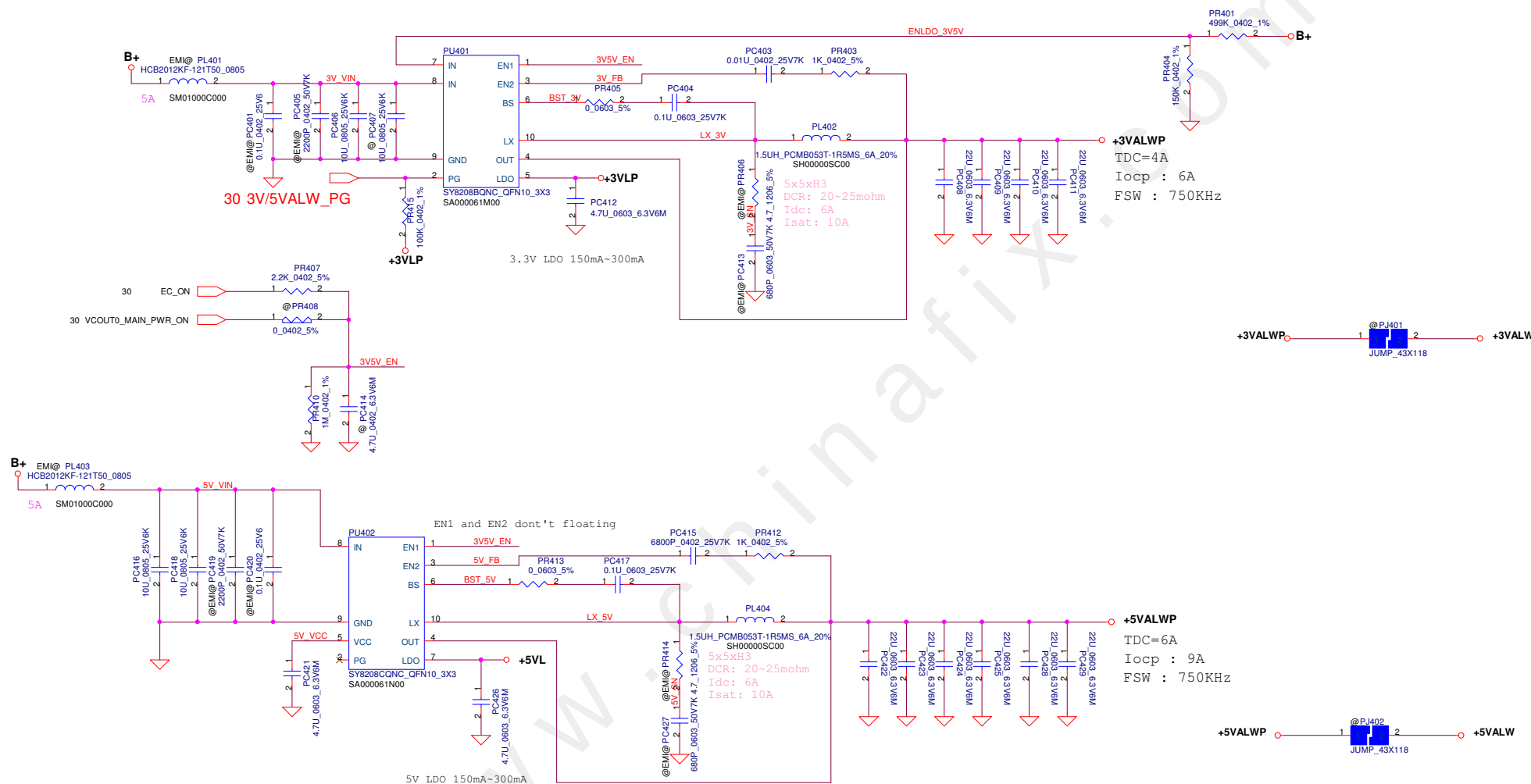
PH201 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



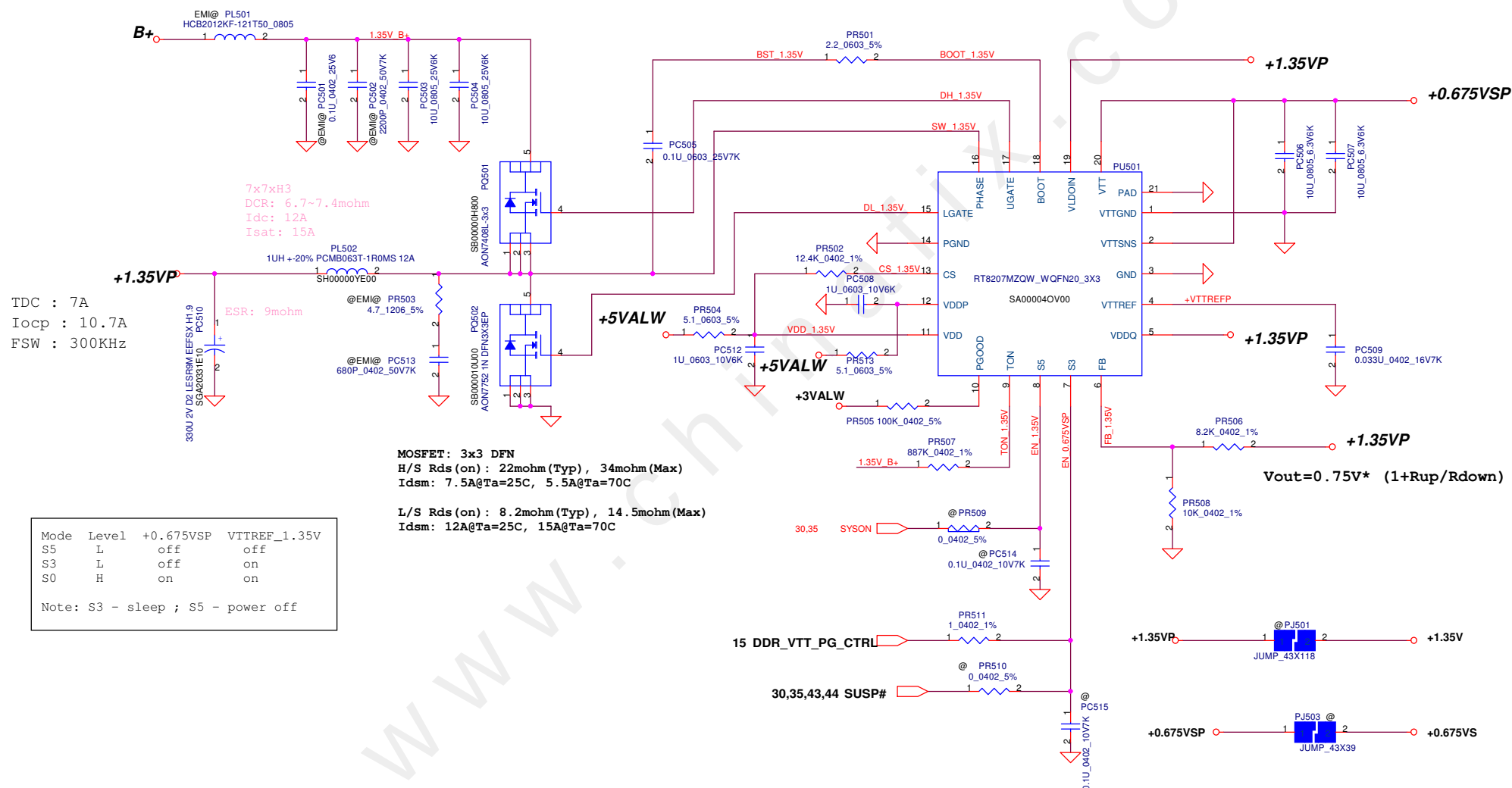
Security Classification	Compal Secret Data			Title	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Compal Electronics, Inc.	
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				BE_BDW	1.0
				Date: Tuesday, March 04, 2014	Sheet 37 of 52



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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title Charger BQ24737		
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				BE BDW		
Date: Tuesday, March 04, 2014				Sheet	38	of 52

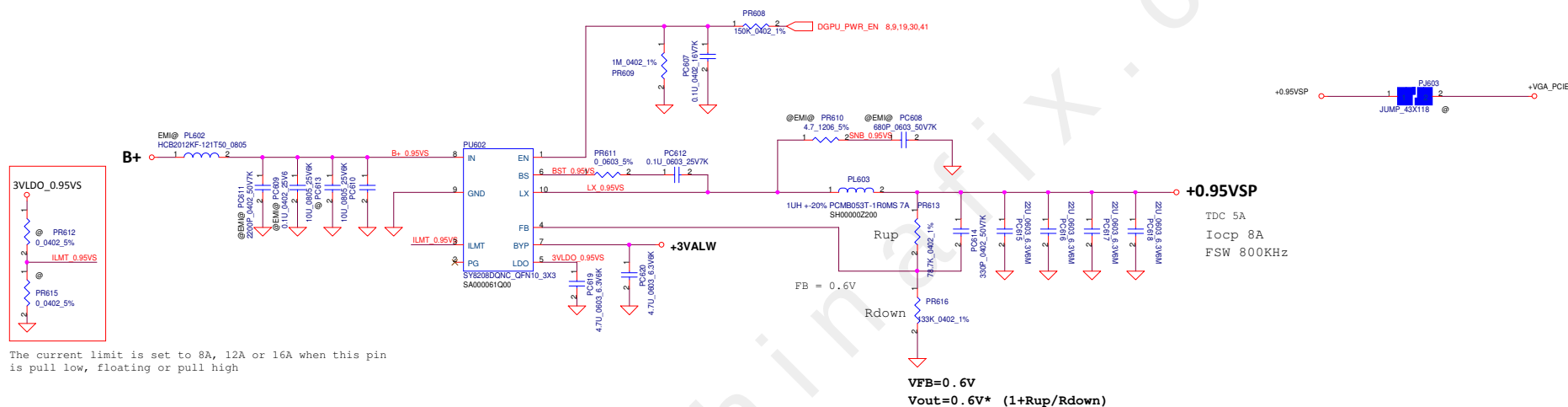


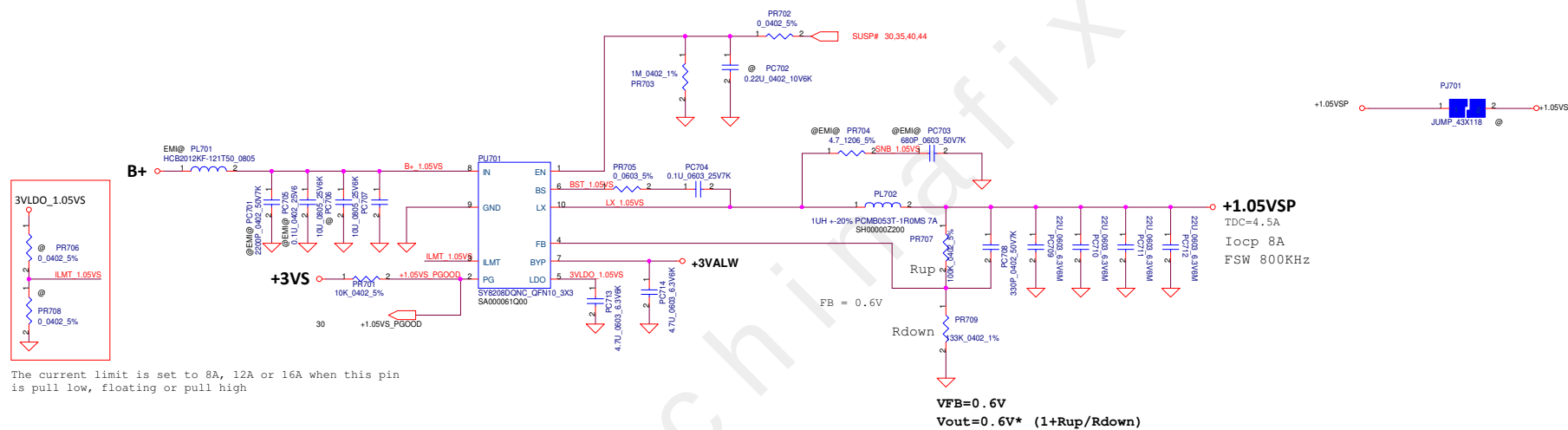
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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	+3VALW/+5VALW		
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				Customer	BE BDW	Rev	1
				Date	Tuesday, March 04, 2014	Sheet	39 of 52



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				Size	Document Number	Rev
				Custom	BE_BDW	1.0
Date:				Tuesday, March 04, 2014	Sheet	40 of 52

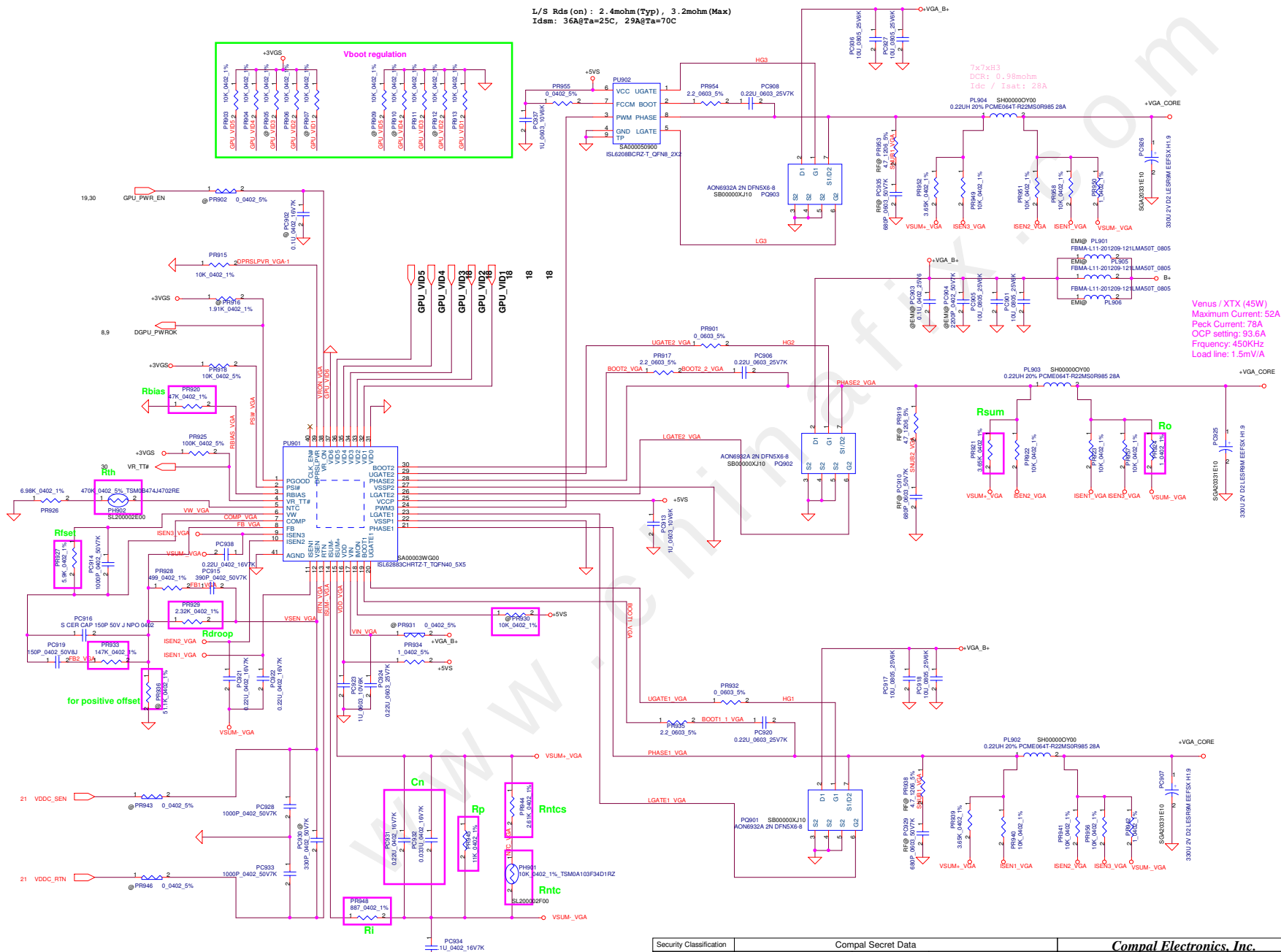
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Issued Date		2014/03/03		Deciphered Date	2015/03/03		Title					
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							Size	Document Number				Rev
							Custom	BE_BDW				1.
Date:		Tuesday, March 04, 2014			Sheet		41	of	52			





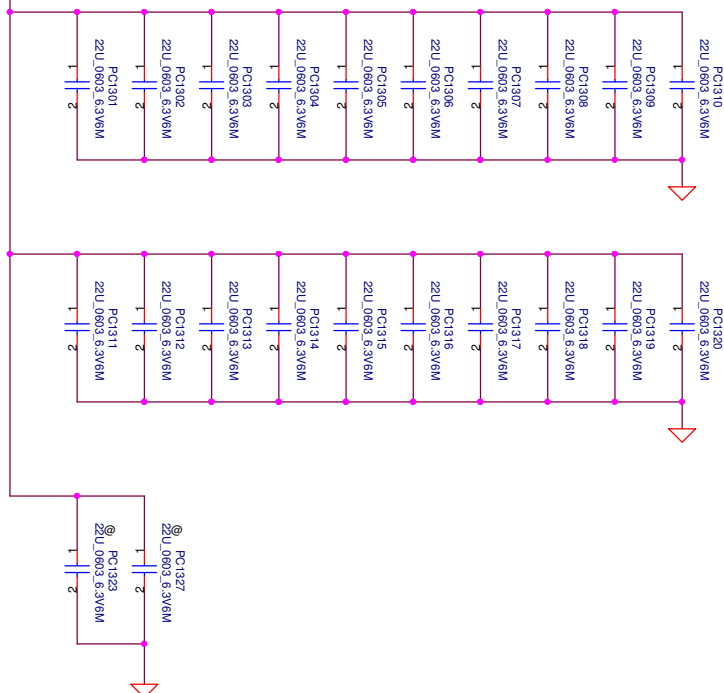
MOSFET: dual N / 5x6 DFN
H/S Rds(on) : 5mohm(Typ), 8.5mohm(Max)
Idsm: 22A@Ta=25C, 17A@Ta=70C

L/S Rds(on) : 2.4mohm(Typ), 3.2mohm(Max)
Idsm: 36A@Ta=25C, 29A@Ta=70C

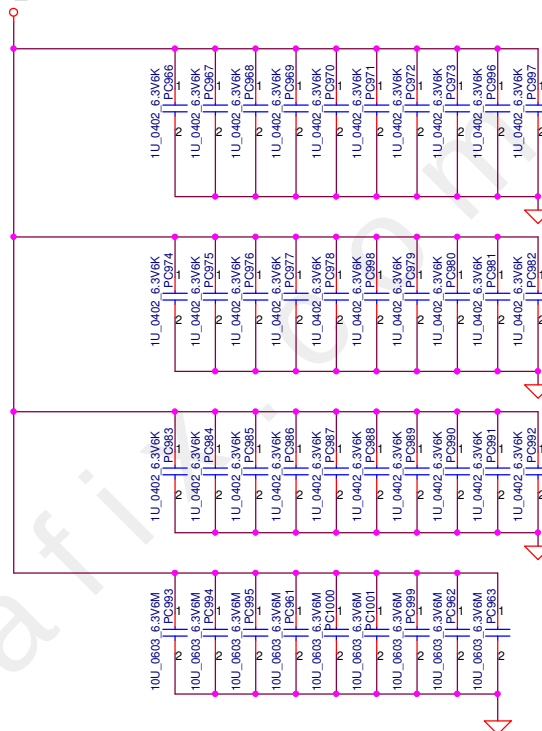


+CPU_CORE

22u 0603 *22/ @*2



+VGA_CORE



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				BE_BDW	
				Date:	Tuesday, March 04, 2014
				Sheet	47 of 52

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	link with HW side	45	change net name +3VS_VGA or +3VGS	11/15	SIV
2	modify VCORE setting	46	1. Change the PR1120 from 280 Ohm to 287 Ohm. 2. Change the PR1117 from @ to 4.99MOhm. 3. Change the PR1118 from 2.61kOhm to 4.42kOhm. 4. Change the PC1101 from @ to 1000pF. 5. Change the PR1106 from @ to 97.5kOhm. 6. Change the PR1114 from 2kOhm to @. 7. Change the PC1114 from 330pF to @.	11/15	SIV
3	for RF request	45	PR953, PC935, PR919, PC910, PR938, PC929 change to mount	11/19	SIV
4	for RF request	46	PR1107, PC1110 change to mount	11/19	SIV
5	SIV MEMO	46	PR1101 change to NA	12/24	SIT
6	Valure modify	45	PC916 change to 150p	12/24	SIT
7	AC detect valure setting	38	PR309 is changed from 392K_0402_1% to 124K_0402_1% (SD034124380) PR312 is changed from 59K_0402_1% to 20K_0402_1% (SD034200280) Add a resistor 249K_0402_1% (SD034249380) between pin 6 of PU301 and PACIN. PC312 is changed from 2200pF_0402_25V_X7R to 0.01uF_0402_25V_X7R (SE075103K80)	12/24	SIT
8	for EMI request	38	Add 2caps to GND, Add 1 SNUB (PC320=0603 680pF, PR319=1206 4.7ohm, PC306=0.1uF, PC307=2200pF)	12/24	SIT
9	battery can't be remove	37	del PC206, PD201, PC205, PR307, PQ306, PQ313	12/24	SIT
10	modify VCORE setting	46	Change PR1120 to 422ohm. Change PR1104 to 90.9Kohm.	02/20	SVT
11	modify VCORE setting	47	Add PC1320 22uF.	02/20	SVT

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	
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Size		Document Number		Rev	
Custom		LA-B131P		1.0	
Date:		Tuesday, March 04, 2014		Sheet 48 of 52	

Version change list (P.I.R. List)

Page 1 of 4
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	09	Change U9J.P1 from PCH_GPIO76 to DDI2_HDMI_HPD	10/02	SIV
2	EMI recommend	26	Change D5, D6 from SC300001G00 to SC300001J00 Change D5, D6 from @EMI@ to EMI@	10/29	SIV
3	EMI recommend	27	Change RA12 from SD028000080 to SM01000DF00 Change C254 from SE071220J80 to SE074221K80 Change C254 from @EMI@ to EMI@	10/29	SIV
4	EMI recommend	32	Change D21 from SC300001G00 to SC300001J00	10/29	SIV
5	HW design	07	Change C20 to @ Remove R201	11/06	SIV
6	HW design	11	Change C41, C45 to @	11/06	SIV
7	HW design	15	Change C97,C119,C113,C115,C116 to @ Change C93,C94,C96,C98,C99,C100 to @	11/06	SIV
8	HW design	16	Change C124,C126,C127,C128,C129,C131 to @ Change C149,C143,C144,C147 to @	11/06	SIV
9	HW design	17	Change CV9 to @DIS@	11/06	SIV
10	HW design	25	Change C214 to @ Remove R722,R721	11/06	SIV
11	Vendor recommend	34	Change CL29 form 15p to 12p	11/06	SIV
12	HW design	06	Change R17,R21 to short pad	11/07	SIV
13	HW design	07	Change R24,R25,R26,R27 to RP31 Change R31,R33,R32,R55 to RP32	11/07	SIV
14	HW design	15	Change R101,R102 to short pad	11/07	SIV
15	HW design	16	Change R111,R112 to short pad	11/07	SIV
16	HW design	18	Remove RV17 Move GPU_GPIO1 to RP19.7	11/07	SIV
17	HW design	25	Add PCH_GPIO87 to JEDP1.7	11/07	SIV
18	HW design	27	Change R156 to short pad	11/07	SIV
19	EMI recommend	27	Add RA13 for EMI@ Add CA12 for @EMI@	11/07	SIV
20	HW design	29	Change R217,R218,R257,R222,R199,R226 to short pad	11/07	SIV
21	HW design	30	Change R273,R274,R268 to short pad Remove R266,R276,R214,R272 Move USB_CHG_EN#, USB_EN#, FAN_SPEED2, FAN_SPEED1 to RP33	11/07	SIV
22	HW design	31	Change R243 to short pad	11/07	SIV
23	HW design	33	Change R253 to short pad	11/07	SIV
24	HW design	35	Change R630 to short pad	11/07	SIV
25	EMI recommend	28	Add C323,C326,C327,C328,C329,C330,C331,C332 for @EMI@	11/07	SIV
26	HW design	32	Add R249,R250	11/10	SIV

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HW-PIR
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Date: Tuesday, March 04, 2014				Sheet	49 of 52
				Rev	1.0



Item	Reason for change	PG#	Modify List	Date	Phase
27	HW design	09	Change PCH_GPIO85 to PCH_USB_EN#	11/10	SIV
28	HW design	18	Add RV13 for THM_ALERT#	11/10	SIV
29	ME recommend	28	Change JHDMI1 footprint to SINGA_2HE1638-012212F_19P-T	11/10	SIV
30	HW design	12	Change C59,C62,C66,C70,C75 from SE000000000 to SE000000PL00 Add C37,C138,C333@,C334,C335 SE000000PL00	11/10	SIV
31	HW design	07	RP31.1 & RP31.3 swap RP31.2 & RP31.4 swap => modify RP31 symbol RP32.1 & RP32.2 swap RP32.3 & RP32.4 swap	11/10	SIV
32	EMI recommend	27	Add CA13 close to UA1	11/11	SIV
33	HW design	30 32	Change USB_CHG_EN# to USB_CHG_EN	11/11	SIV
34	HW design	09	Remove DGPU_PWR_EN, DGPU_HOLD_RST# Change PCH_GPIO18 from RP10.5 to RP5.8 Change PCH_GPIO23 from RP10.6 to RP28.5 Remove RP10	11/12	SIV
35	HW design	25	Remove JP5	11/15	SIV
36	Busyer suggestion	19	Change QV5 from SB000007H10 to SB00000QP00	11/15	SIV
37	Busyer suggestion	21	Change LV6, LV7 from SM01000BZ00 to SM01000FF00	11/15	SIV
38	Busyer suggestion	30	Change L13,L14 from SM010016810 to SM01000LP00	11/15	SIV
39	HW design	32	swap D21 (Pin1=>Pin9, Pin3=>Pin1, Pin7=>Pin3, Pin9=>Pin7)	11/18	SIV
40	EMI recommend	26	Change TS1 from SP050006F00 to SP050006800	11/20	SIV
41	EMI recommend	25	Change CA12 from 2.2u to 220P	12/02	SIV
42	EMI recommend	27	Change RA3 from 45.1 to 10.6 Change CA13 from 2.2u to 220P	12/02	SIV
43	EMI recommend	28	Change C323,C326,C327,C328,C329,C330,C331,C332 from 0.1u to 2.2P	12/02	SIV
44	EMI recommend	32	Change D16, D17 from ESD@ to @ESD@	12/02	SIV
45	EMI recommend	33	Change D19 from ESD@ to @ESD@ Change D20 from @ESD@ to ESD@	12/02	SIV

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HW-PIR
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Date: Tuesday, March 04, 2014				Sheet	50 of 52
				Rev	1.0



Item	Reason for change	PG#	Modify List	Date	Phase
1	HW design	33	Add R266(@) 100K pull-high to +3VLP for NOVO#	12/05	SIT
2	HW design	29	Add NET: DEW1_TI / DEW2_TI	12/09	SIT
3	HW design	09	Add R276 10K pull-high to +3VS for DGPU_PWR_EN	12/19	SIT
4	Vendor recommend	29	Change R186, R193 from @ to TI@ Change +12VS_Pane1 to B+	12/20	SIT
5	HW design	25	Add JP5 Delete R215, R504, R148 for RP10 Add RP10 Change R213 to short pad Change R267 to @	12/20	SIT
6	HW design	30	Change net name from USB_EN# to USB1_EN# Add USB2_EN# to U26.89 Add R277 (10K) pull-high +5VALW Change R270 to short pad	12/20	SIT
7	HW design	32	Change net name from USB_EN# to USB1_EN# by U29.4 Change net name from USB_EN# to USB2_EN# by U30.4 Delete R249, R250	12/20	SIT
8	HW design	09	Change PCH_USB_EN# to PCH_GPI085 Delete R252, R262	12/20	SIT
9	HW design	08	Delete R206 for RP10 Change R46, R51, R53 to short pad	12/20	SIT
10	HW design	07	Change R34, R35, R39, R40 to short pad	12/20	SIT
37	HW design	11	Change R79 to short pad	12/20	SIT
38	HW design	15	Change R88, R98 to short pad	12/20	SIT
39	HW design	16	Change R104 to short pad	12/20	SIT
40	HW design	18	Change RV44, RV32 to short pad	12/20	SIT
41	HW design	19	Change RV45 to short pad	12/20	SIT
42	HW design	20	Change RV46, RV50, RV52, RV55, RV57, RV51 to short pad	12/20	SIT
43	HW design	28	Delete Q5, Q7 Add Q5A, Q5B	12/20	SIT
44	EMI recommend	32	Change C306, C307 from 0.1u to 100P	12/20	SIT
45	HW design	33	Change R230 from 300 ohm to 649 ohm	12/23	SIT
46	Busyer suggestion	21	(X1 code) Change LV10, LV13 from SM01000BL00 to SM01000GG00	12/23	SIT
47	Busyer suggestion	08	(X1 code) Change U11 from SA00006QR00 to SA741080400	12/23	SIT
48	Busyer suggestion	25	(X1 code) Change U33 from SA00006QR00 to SA741080400	12/23	SIT
49	Busyer suggestion	30	(X1 code) Change U27 from SA00006QR00 to SA741080400	12/24	SIT
50	EMI recommend	27	Change RA12 from 120 ohm(SM01000DF00) to 300 ohm (SM01000I000)	12/24	SIT
51	HW design	27	Change RA2, RA10 to short pad	12/24	SIT
52	EMI recommend	30	Change C286, C287, C289, C291 from @ to EMI@	12/24	SIT
53	HW design	30	Change R260, R223 to short pad	12/24	SIT
54	HW design	31	Change R228, R229 to short pad	12/24	SIT
55	HW design	19	Change R260, R223 to short pad	12/25	SIT
56	HW design	25	Change L24 from EMI@ to @EMI@	12/25	SIT

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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HW-PIR
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Date:	Tuesday, March 04, 2014	Sheet	51	of	52



Item	Reason for change	PG#	Modify List	Date	Phase
57	HW design	29	Change R275 to @	12/27	SIT
58	HW design	28	Change C323, C326, C327, C328, C329, C330, C331, C332 from @EMI@ to EMI@	12/27	SIT
59	HW design	31	Change R230 from 649 ohm 5% to 649 ohm 1%.	12/31	SIT
60	Vendor recommend	21	Change LV10, LV13 from SM01000GG00 to SM01000I300.	01/03	SIT
61	HW design	12	Change C59, C138, C66, C334, C75 from 47uF to 22uF	01/07	SIT
62	HW design	15	Change C89, R90, C107, R100 to @	01/07	SIT
63	HW design	16	Change C120, R106 to @	01/07	SIT
64	HW design		Change R1456 to short pad		
65		25	Change C225, C226 to @	01/07	SIT
66			Change L6 from SM010014520 to SD002000080 (0 ohm) and change location to R2		
67	HW design	31	Change C300, C303 to @	01/07	SIT
68	HW design	33	Change R256 to short pad	01/07	SIT
69	HW design	12	Change C37, C62, C70, C335 to @	01/03	SIT
1	HW design	25	Change location L6 to R2	01/12	SVT
2	HW design	19	Change location C989 to R830	01/12	SVT
3	EMI recommend	28	Change C327, C328, C329, C330, C331, C332, C323, C326 from EMI@ to @EMI@	01/14	SVT
4	HW design	27	Add U1(LD0), C344, C343	01/20	SVT
5	DFx recommend	32	Add C345, C346	01/22	SVT
6	Busyer suggestion	21	Change LV10, LV13 from SM01000I300 to SM01000F100	01/22	SVT
7	HW design	27	Add R249, R250 Change C253 from 1uF_0402 tp 1uF_0603	01/22	SVT
8	HW design	06	Change RG3 to short pad	01/22	SVT
9	HW design	07	Change RG9, R38 to short pad	01/22	SVT
10	HW design	25	Change R2 to short pad	01/22	SVT
11	HW design	18	Change RV187 to short pad	01/22	SVT
12	HW design	29	Change R185 to short pad	01/22	SVT
13	HW design	27	Change R155, R157, R158 to short pad	01/22	SVT
14	HW design	26	Change RG6 to short pad	01/22	SVT
15	HW design	30	Change R225 to short pad	01/22	SVT
16	HW design	18	Change RV25 from 100K to 1K	02/10	SVT
17	HW design	28	Change RP21, PR22 from 680 ohm to 470 ohm	02/12	SVT
18	HW design	25	Add R148	02/19	SVT
19	HW design	30	Delete net: BATT_LEN#	02/20	SVT
20	HW design	19	Change R829 from 470 ohm to 10 ohm	02/21	SVT
21	HW design	18	Change RV187 from short pad to 0 ohm	02/21	SVT
22	EMI recommend	27	Change R164, R165, R166, R167 from 0 ohm to short pad Change R196, R197, R198, R173 from 0 ohm to short pad	02/21	SVT
23	Busyer suggestion	19	Change Q139 from SB000003W00 to SB000002N00	02/21	SVT
24	Vendor recommend	34	Add RG2 Change RG5 from 10 ohm to 0 ohm	02/24	SVT
25	DFx recommend	32	Change C346@ to C346	02/26	SVT

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Date: Tuesday, March 04, 2014				Sheet	52 of 52