

MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-29

Rev: 3.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro, VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config

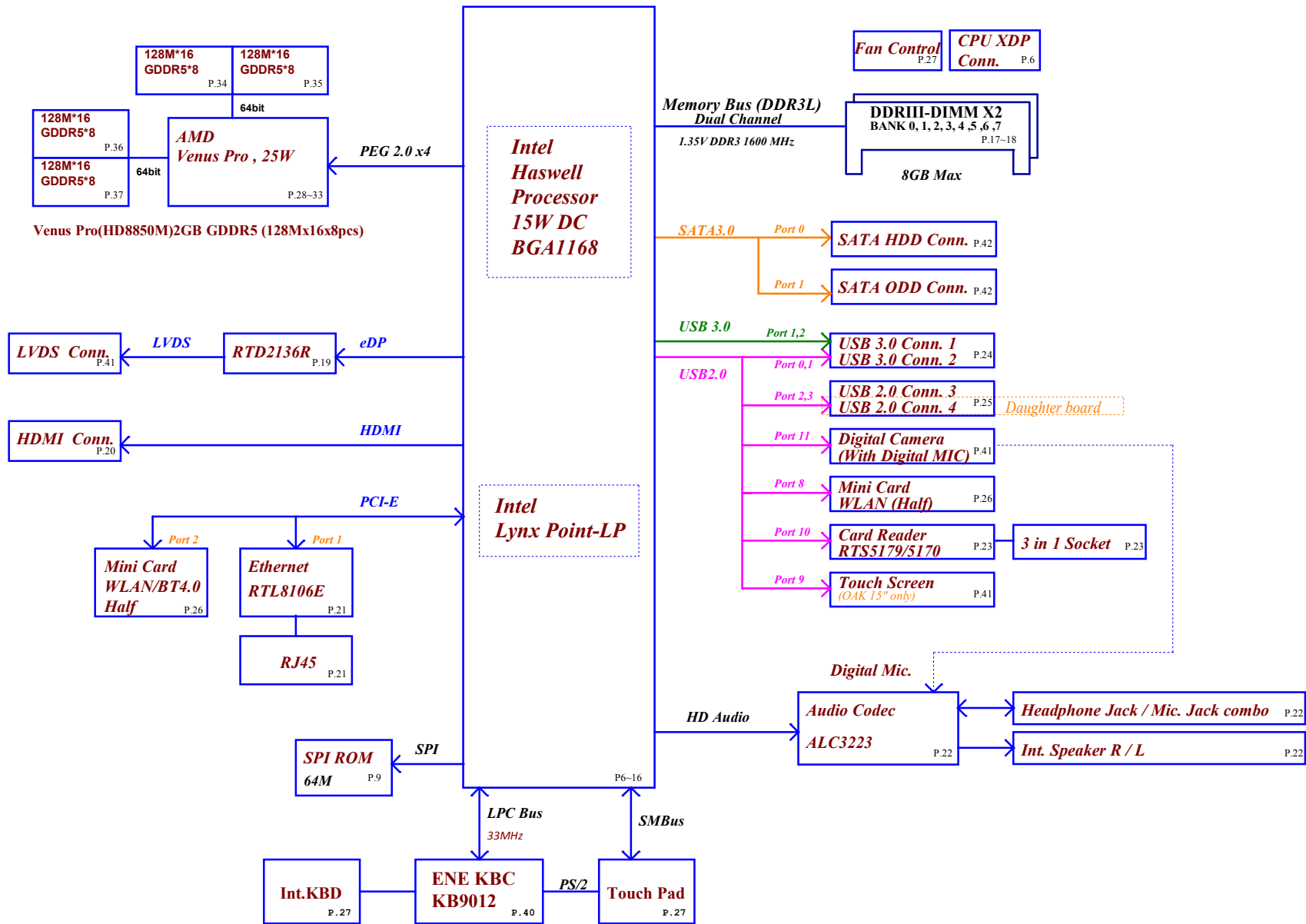
UMA : UMA@,EMI@,ESD@,RF@

DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF



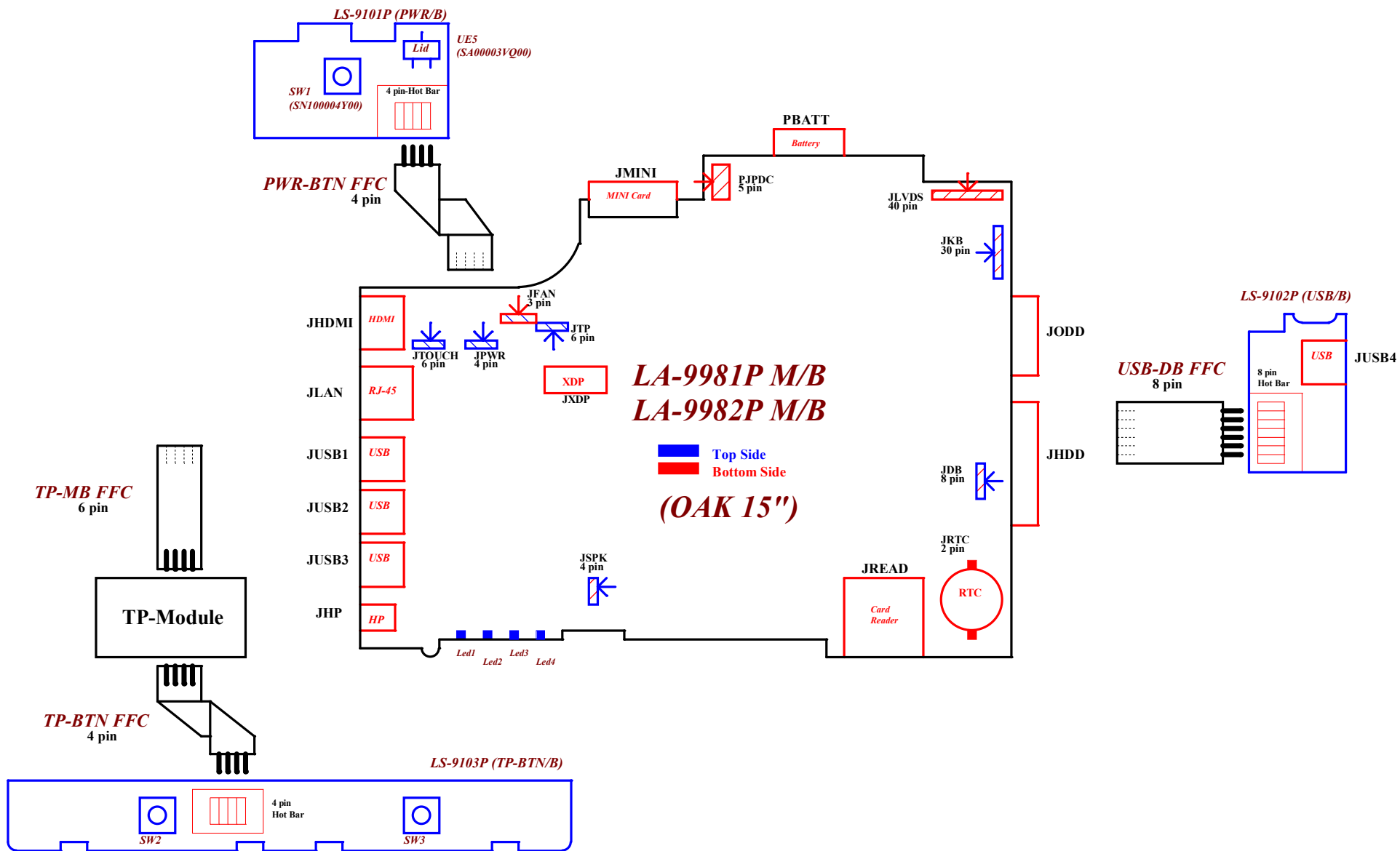
PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DA202G00120

Security Classification	Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	<i>Compal Electronics, Inc.</i>
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Size	Document Number	Rev	3.0	
	LA-9982P	Date:	Wednesday, May 29, 2013	Sheet 2 of 57

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Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xBB - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.677V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

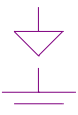
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :



: means Digital Ground



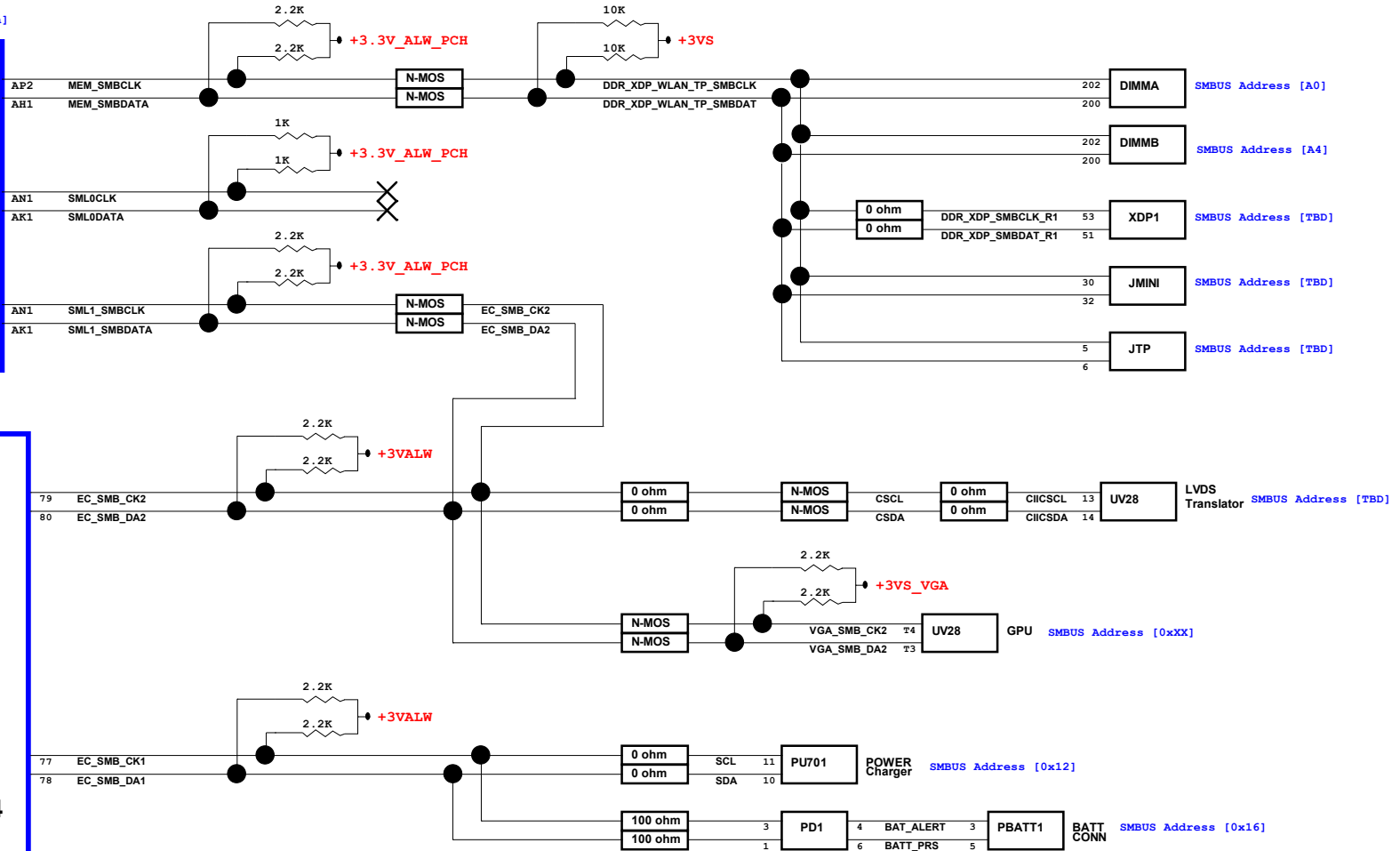
: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

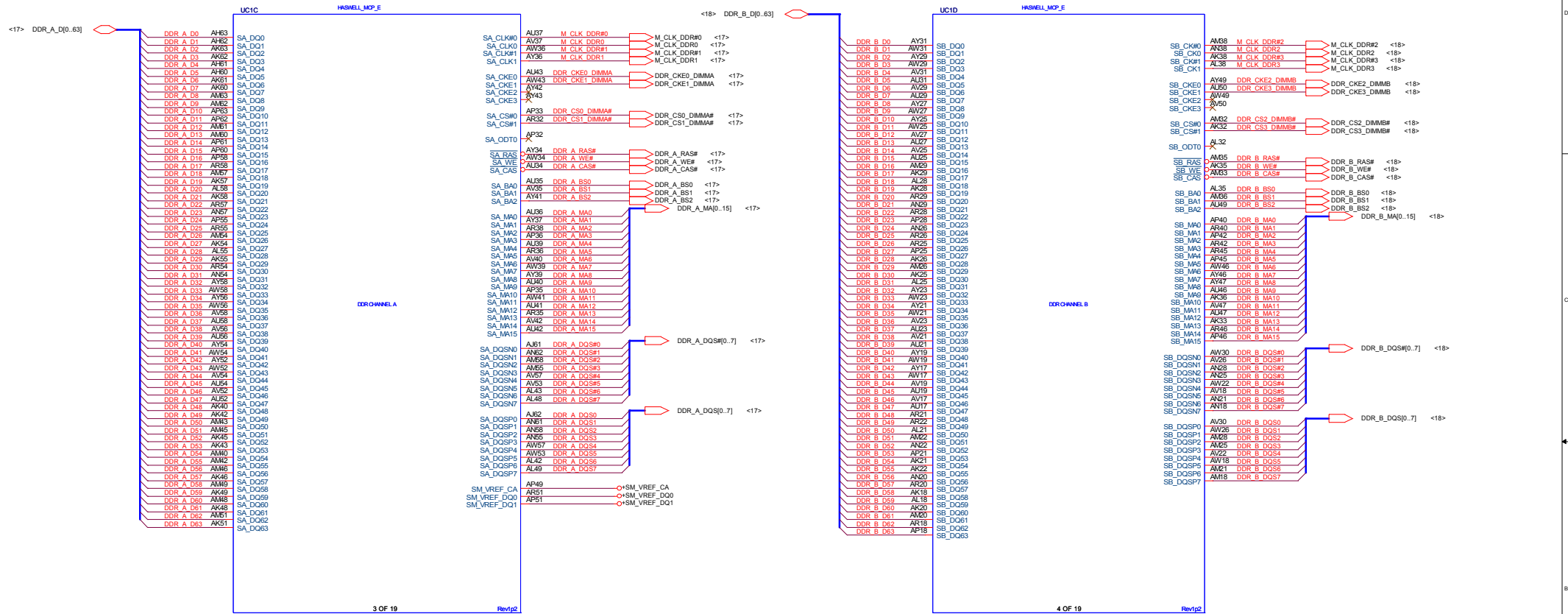
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

ULT

SMBUS Address [0x9a]

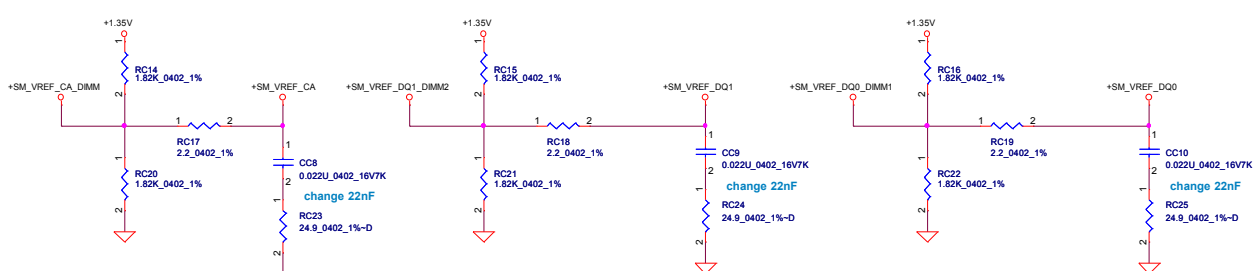


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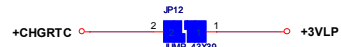
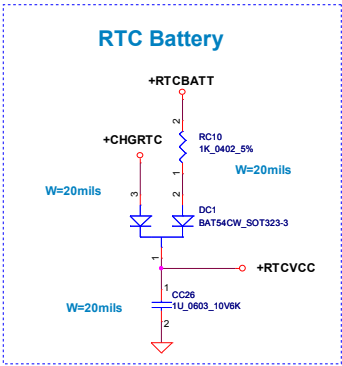
3 OF 19 Rev1p2

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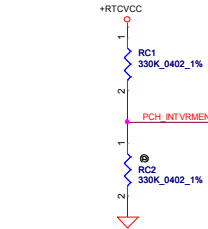


confirm by intel request PDG P141

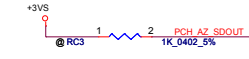
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		MCP(3,4/19) DDR3	
2013/05/29		2014/06/01		Rev 3.0	
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Date: Wednesday, May 29, 2013				Sheet 7 of 57	



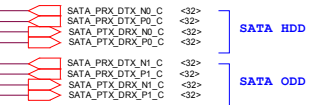
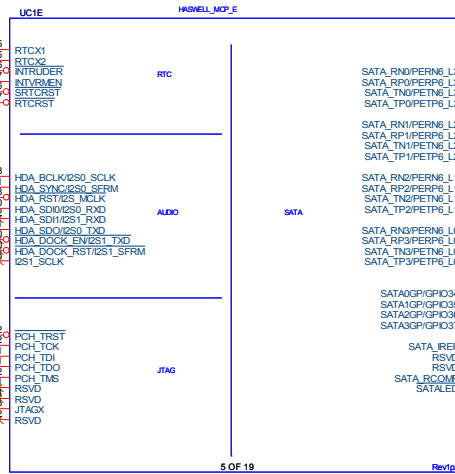
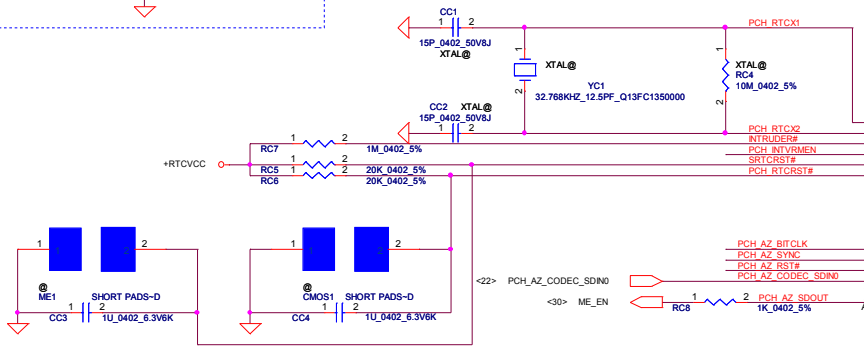
For GCLK



INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs

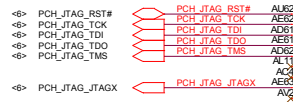
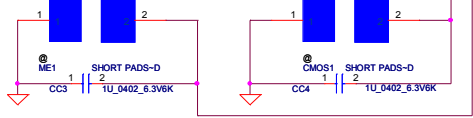


FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED

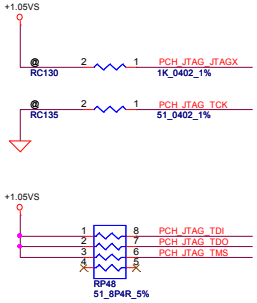


PCH Rx side need use strap pin to update PCIE +/-

CMOS place near DIMM



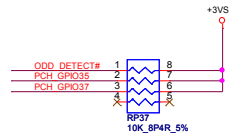
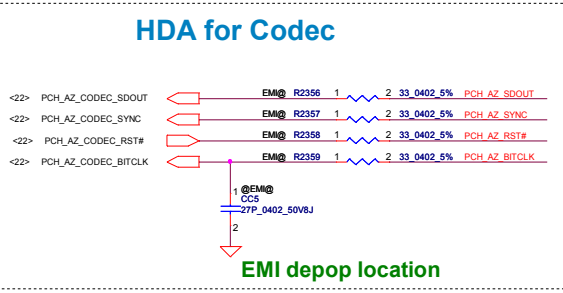
SATA Impedance Compensation
 within 500 mils
 CAD note:
 Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins. reference FFRD sch 0.5

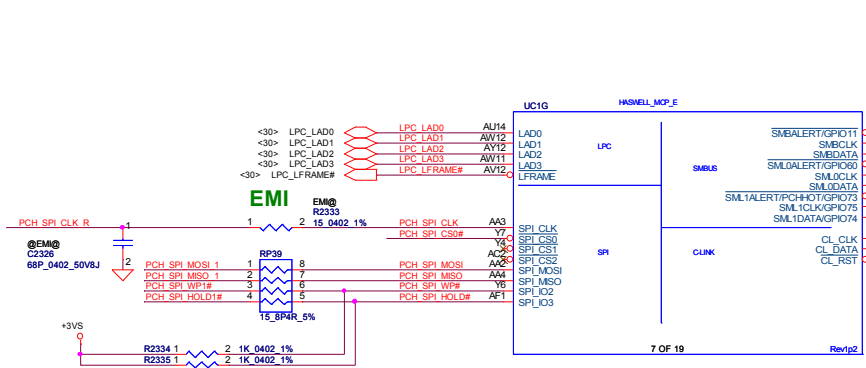


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

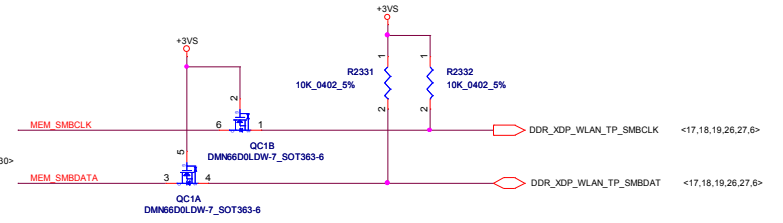
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

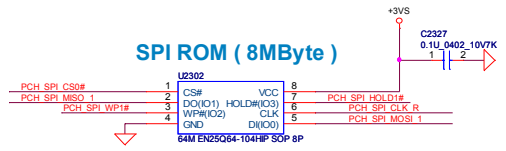
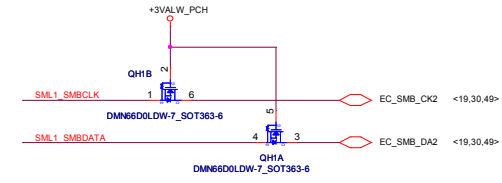




MEM Bus : DDR/XDP/WLAN/TP

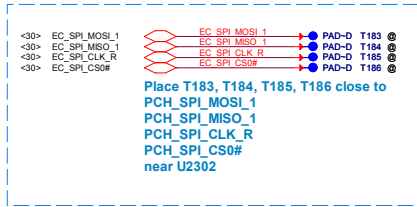


SML1 Bus : EC/Sensors



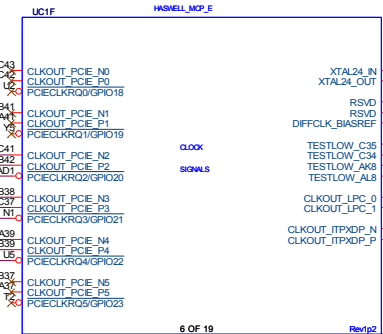
SPI ROM (8MByte)

PN : SA000046400 ,64M,EN25Q64-104HIP



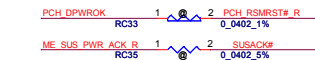
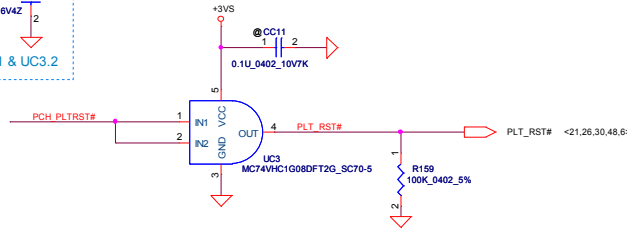
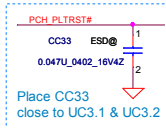
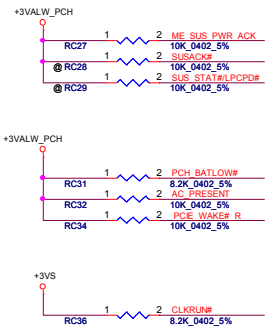
- 10/100 LAN ----->
- WLAN (Mini Card)---->
- dGPU---->

- <21> CLK_PCIE_LAN#
- <21> CLK_PCIE_LAN
- <21> LAN_CLKREQ#
- <26> CLK_PCIE_WLAN#
- <26> CLK_PCIE_WLAN
- <26> WLAN_CLKREQ#
- <48> CLK_PEG_VGA#
- <48> CLK_PEG_VGA
- <48> PEG_CLKREQ#



For GCLK

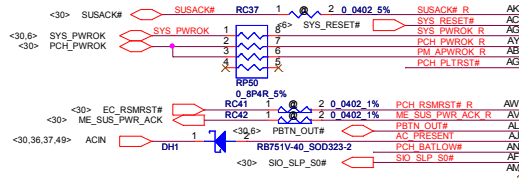
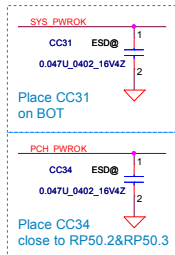
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC ,if not support Deep Sx

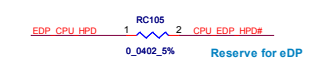
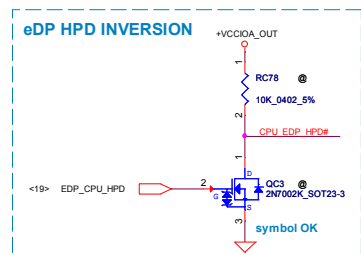
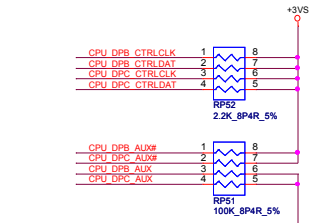
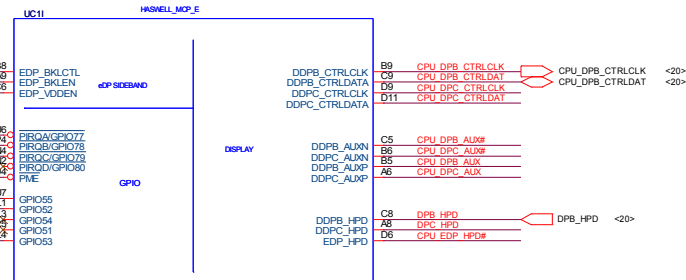
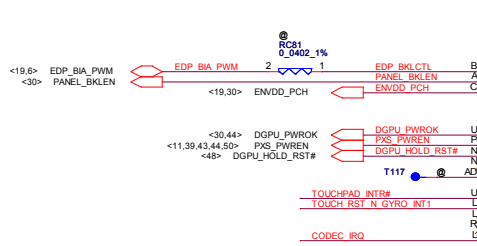
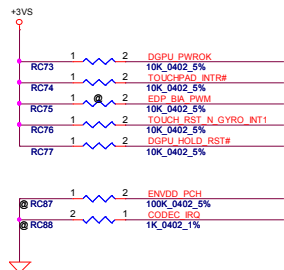
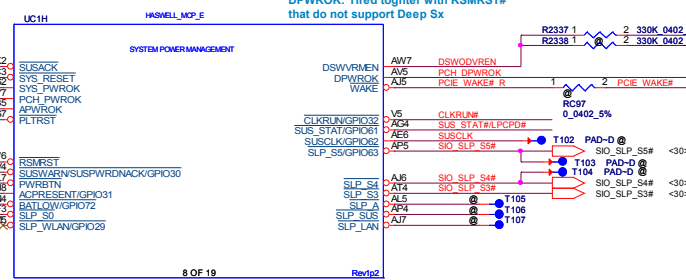
DSWODVREN - On Die DSW VR Enable
 * H : Enable (DEFAULT)
 L : Disable

DSWODVREN - ON DIE DSW VR ENABLE
 HIGH = ENABLED (DEFAULT)
 LOW = DISABLED

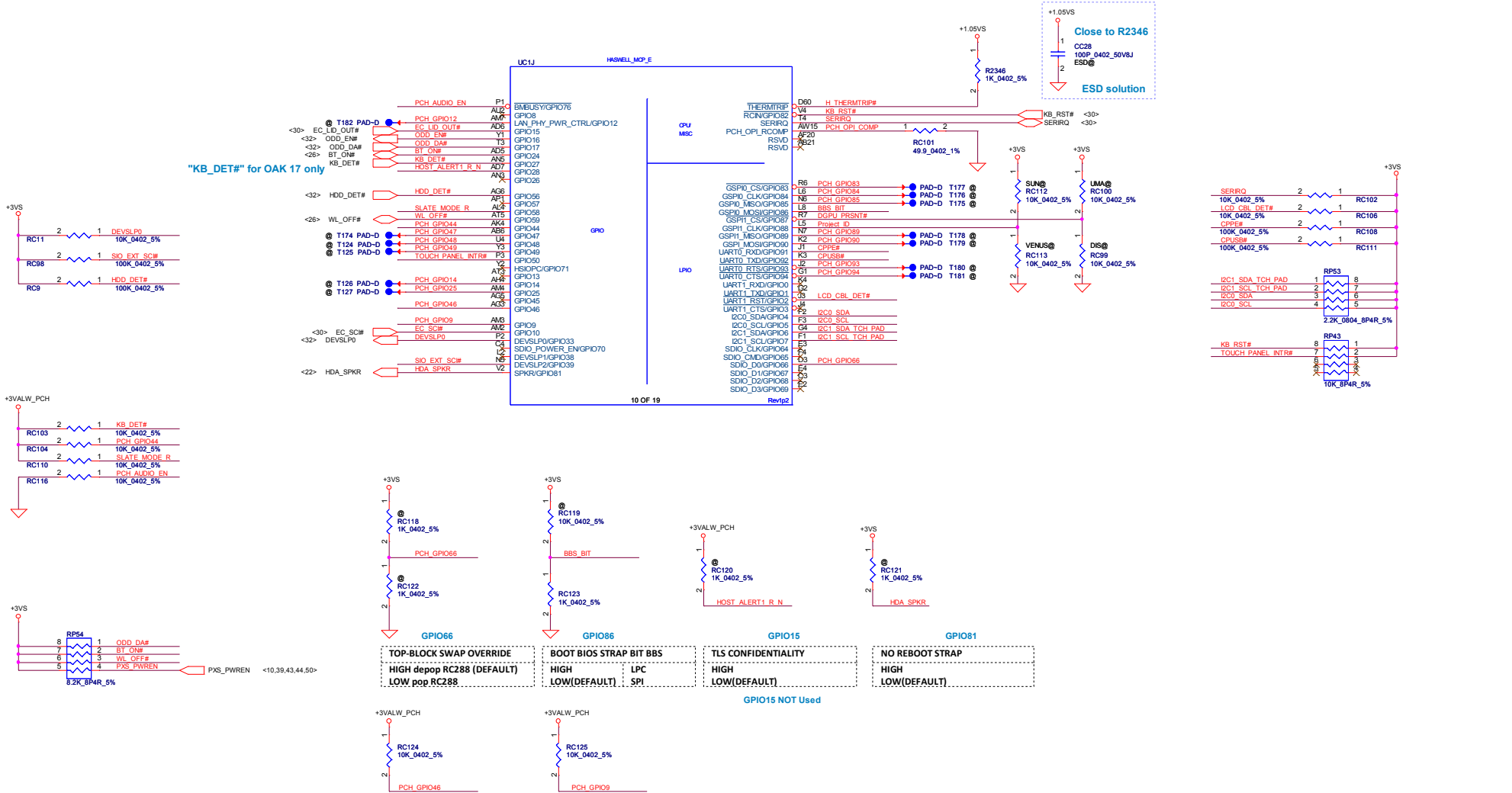


PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx , connect to VCCSUS3_3)

DPWRK: Tired together with RSMRST# that do not support Deep Sx



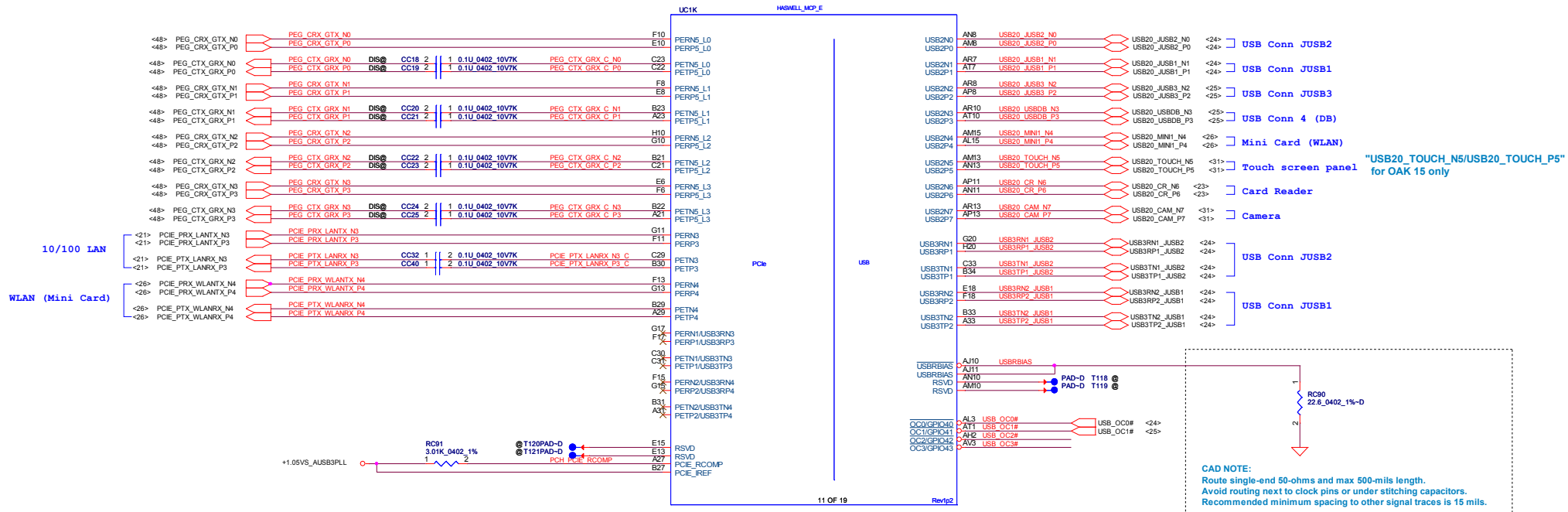
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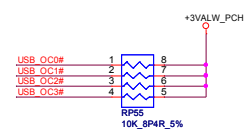
"KB_DET#" for OAK 17 only

TOP-BLOCK SWAP OVERRIDE HIGH depop RC288 (DEFAULT) LOW pop RC288	BOOT BIOS STRAP BIT BBS HIGH LOW(DEFAULT)	TPS CONFIDENTIALITY HIGH LOW(DEFAULT)	NO REBOOT STRAP HIGH LOW(DEFAULT)
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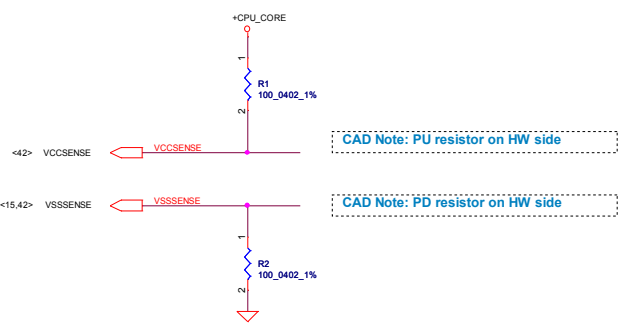
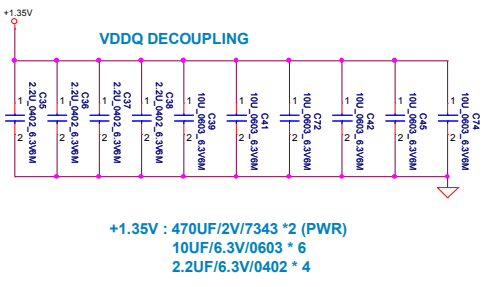
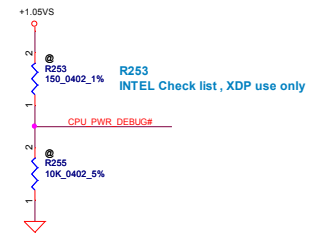
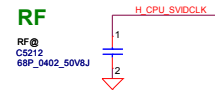
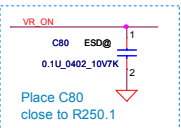
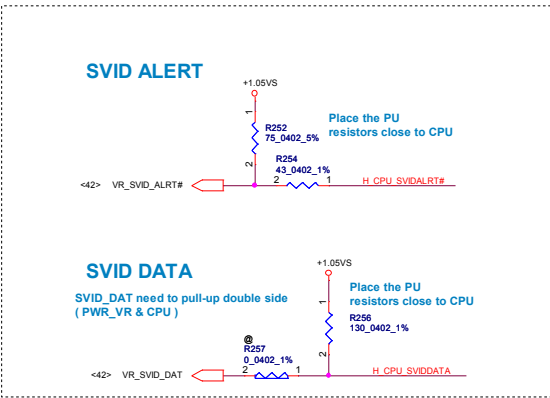
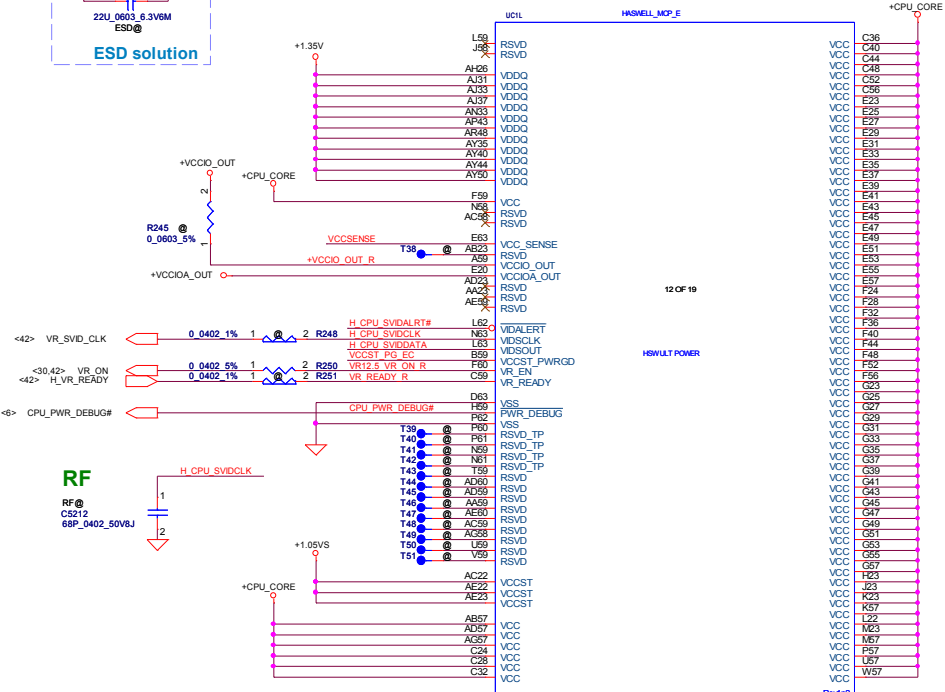
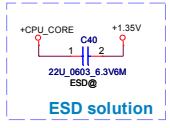
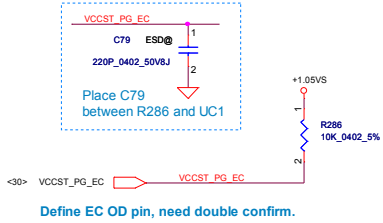
GPIO15 NOT Used



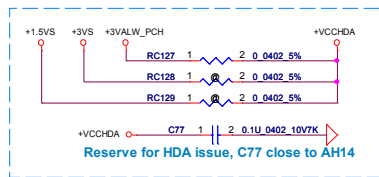
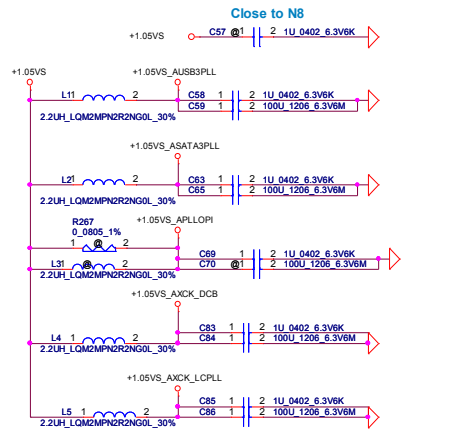
CAD NOTE:
 Route single-end 50-ohms and max 500-mils length.
 Avoid routing next to clock pins or under stitching capacitors.
 Recommended minimum spacing to other signal traces is 15 mils.



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				Date: Wednesday, Nov 28, 2013	Sheet 12 of 57



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Date:	Wednesday, Nov 28, 2013	Sheet	13 of 57	



Reserve for HDA issue, C77 close to AH14



Close to K9,M9



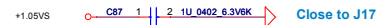
Close to AH10



Close to AC9/AA9/AE20/AE21



Close to V8



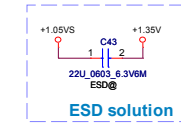
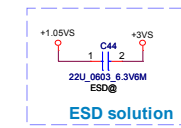
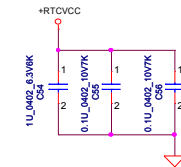
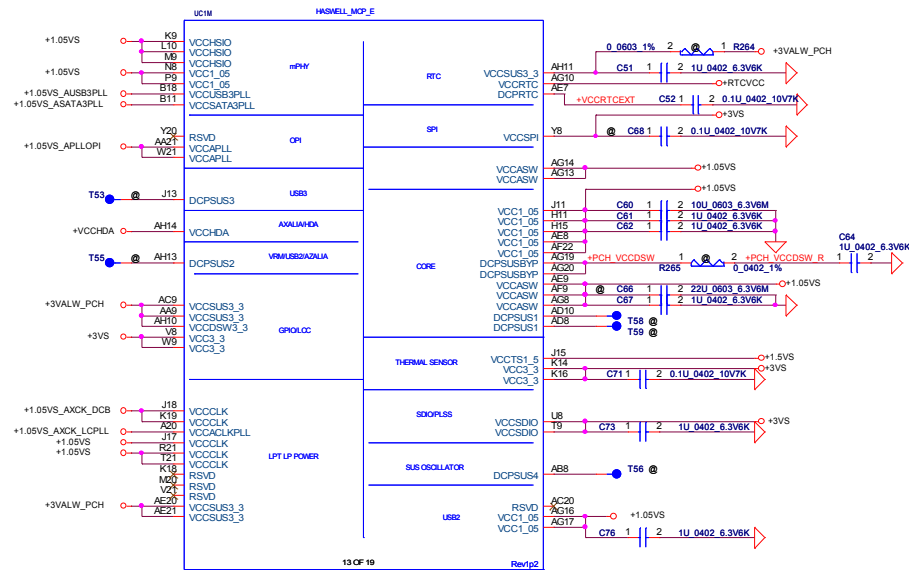
Close to J17



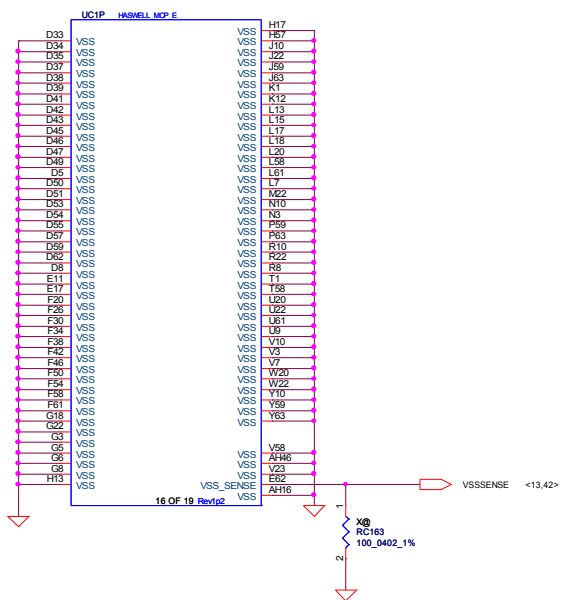
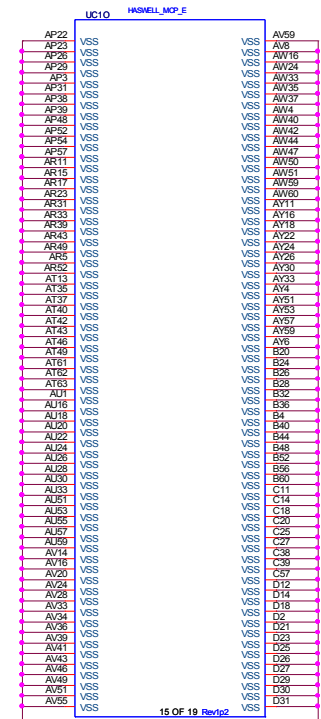
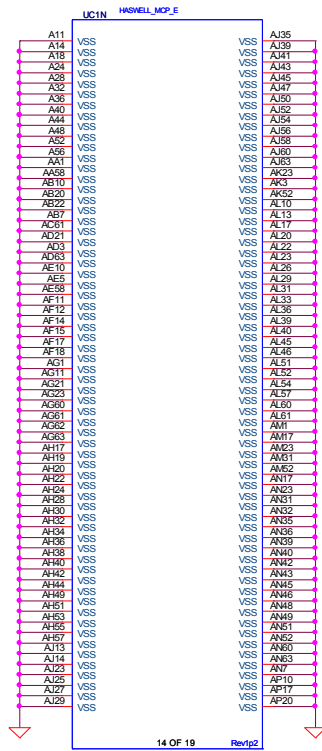
Close to R21



Close to AH14

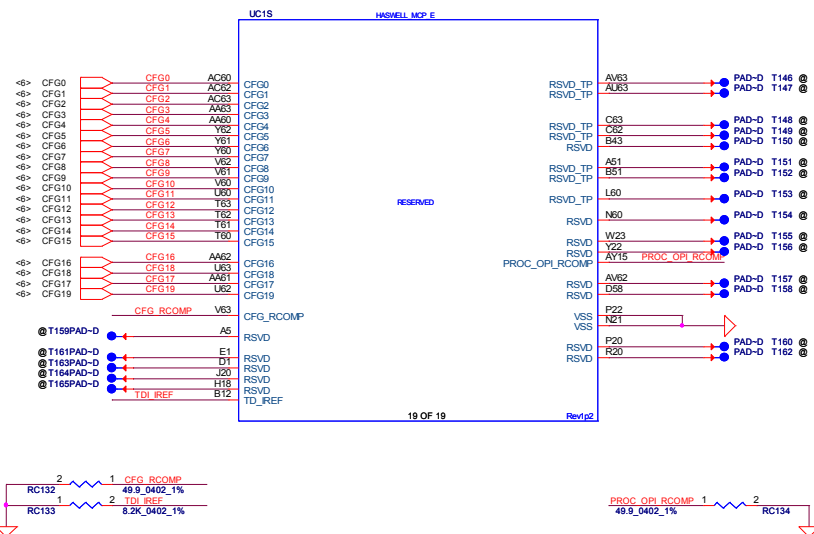
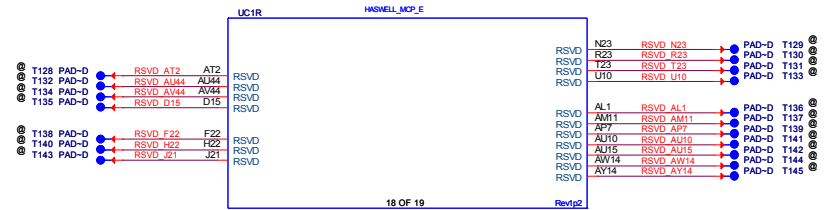
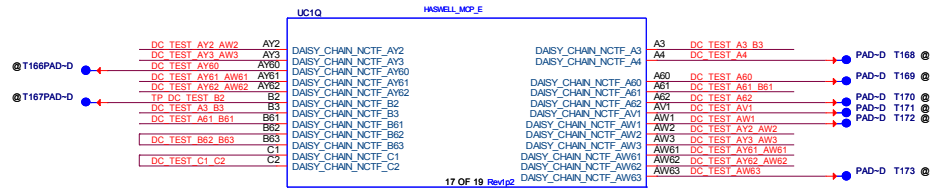


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		MCP(13/19) Power	
2013/05/29		2014/06/01		Document Number	
				LA-9982P	
				Date: Wednesday, May 29, 2013	
				Sheet 14 of 57	
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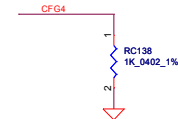


CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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Issued Date	2013/05/29	Deciphered Date	2014/06/01	MCP(14,15,16/19) VSS
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CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

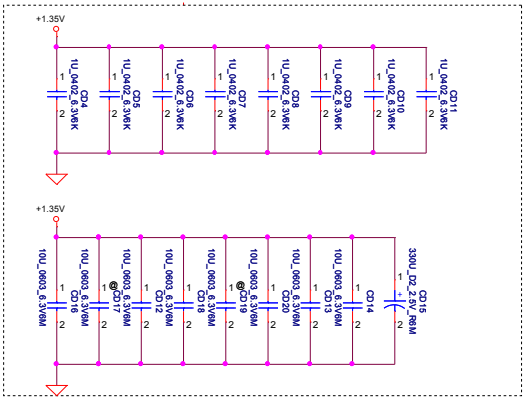
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
 Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<?> DDR_A_DQS#0..7
 <?> DDR_A_DQ0..63
 <?> DDR_A_DQS#0..7
 <?> DDR_MA0..15

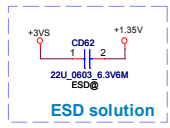
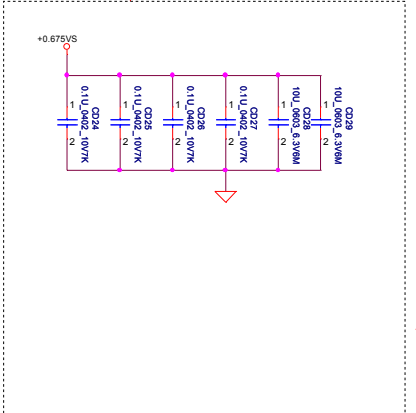
All VREF traces should have 10 mil trace width

Layout Note:
 Place near JDIMM1

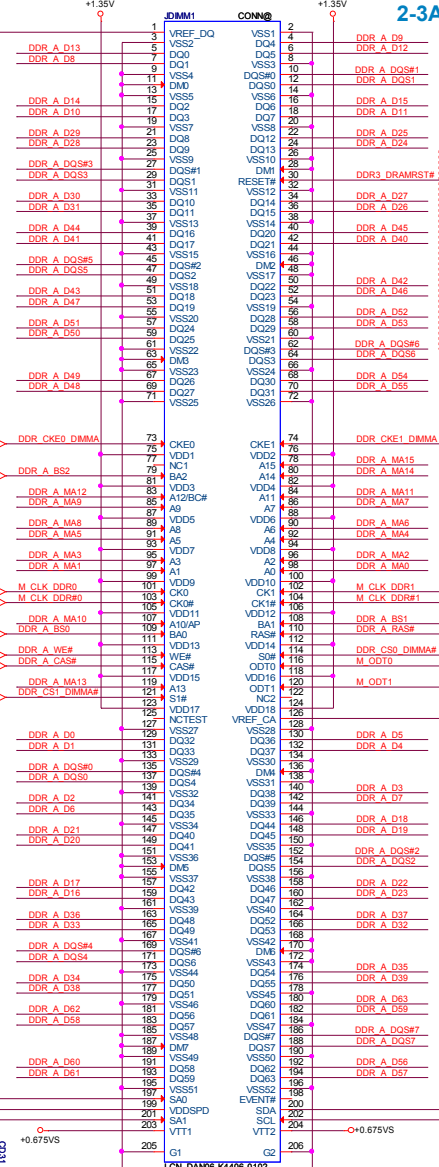
Note:
 Check voltage tolerance of VREF_DQ at the DIMM socket



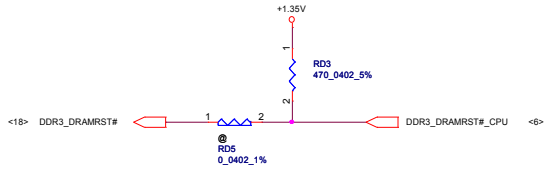
Layout Note:
 Place near JDIMM1.203,204



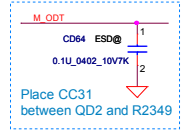
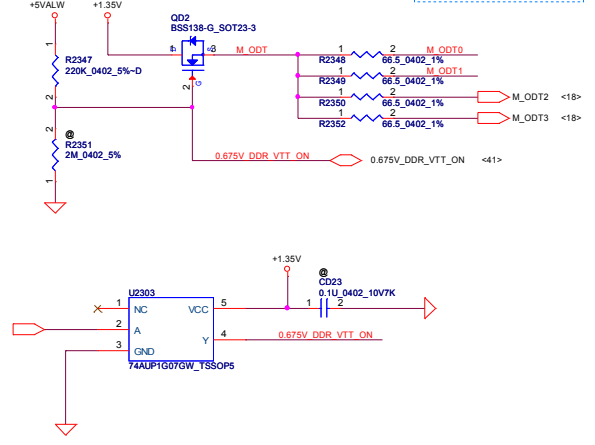
H=4mm
 2-3A to 1 DIMMs/channel



CAD NOTE
 PLACE THE CAP NEAR TO DIMM RESET PIN



DDR3L SODIMM ODT GENERATION



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				LA-9982P	Rev
				1	3.0
				Date:	Wednesday, May 29, 2013
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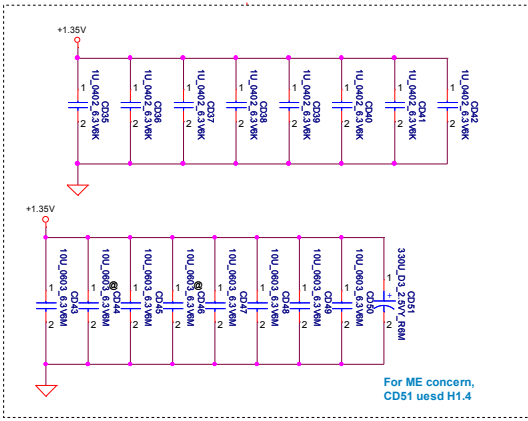
H=4mm
2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

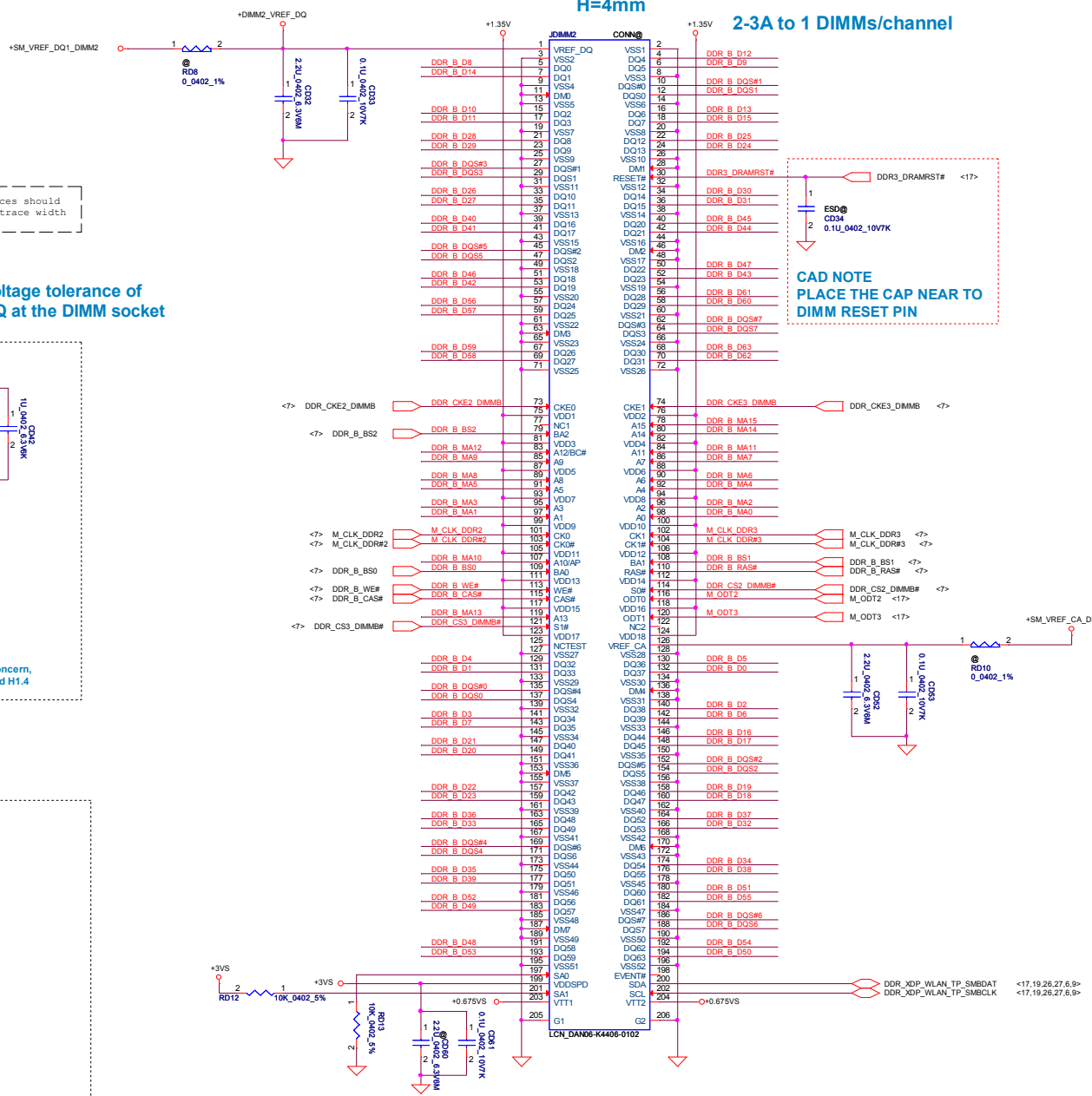
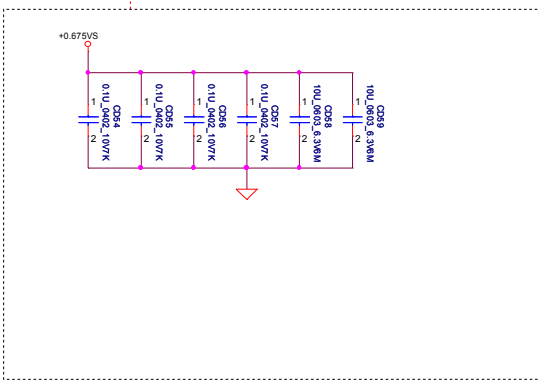


Layout Note:
Place near JDIMM2

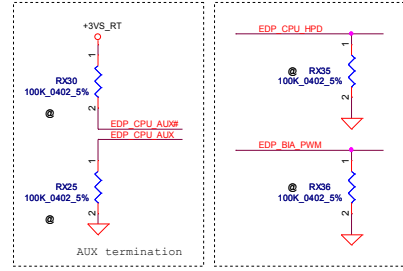
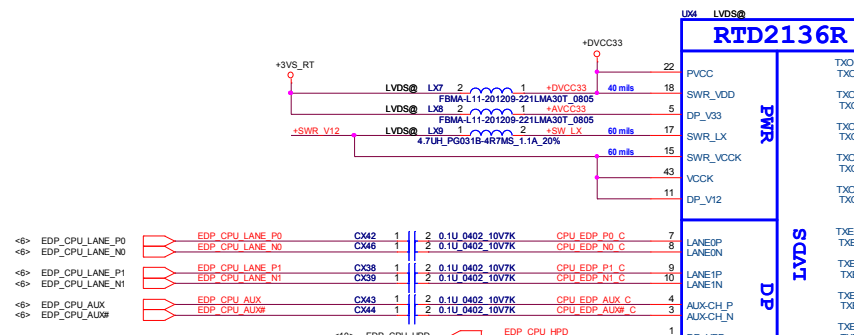
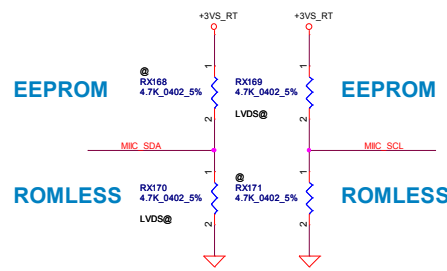
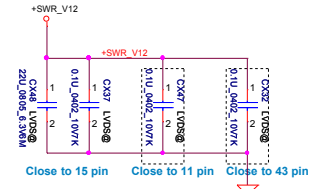
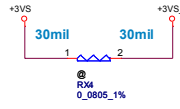
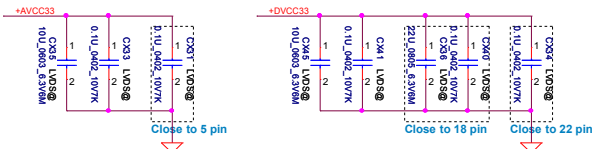
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM2.203,204



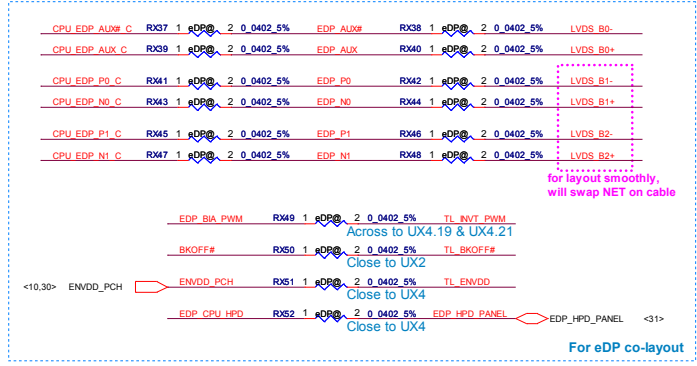
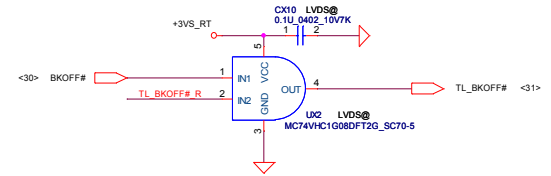
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN



<17,18,26,27,6,9> DDR_XDP_WLAN_TP_SMBCLK
<17,18,26,27,6,9> DDR_XDP_WLAN_TP_SMBDAT

RTD2136S : SA00004NW10
RTD2136R : SA000067100

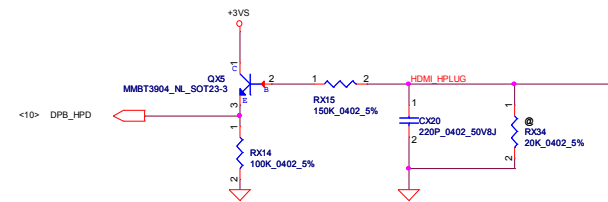
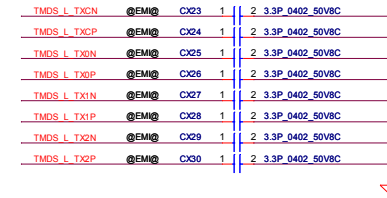
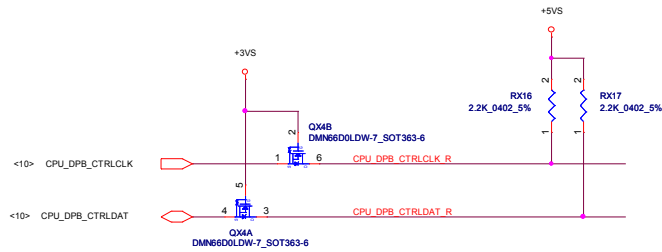
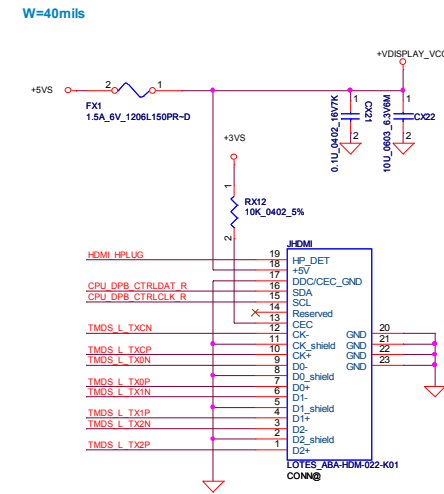
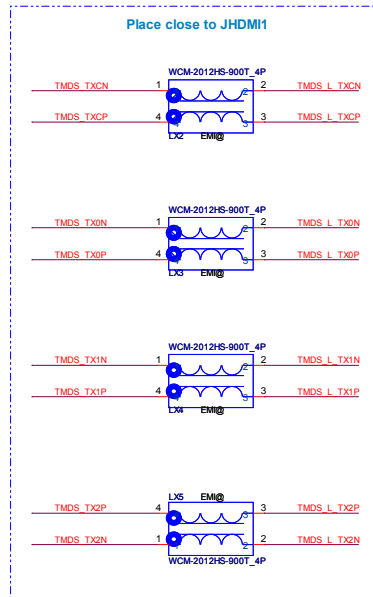
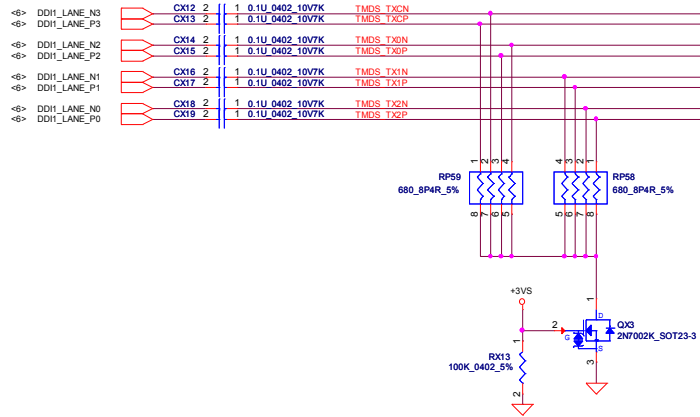
Vendor advise reserve it



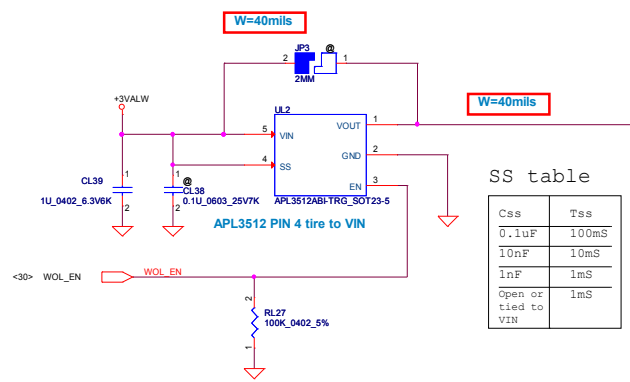
for layout smoothly, will swap NET on cable

For eDP co-layout

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2013/05/29		2014/06/01		LA9982P	
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Size	Document Number	Rev	3.0		
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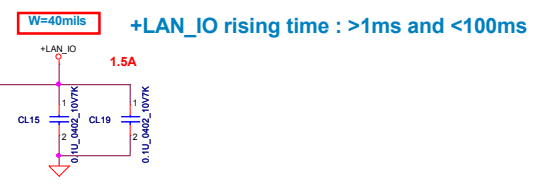


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				Date:	Wednesday, May 29, 2013	Sheet 20 of 57

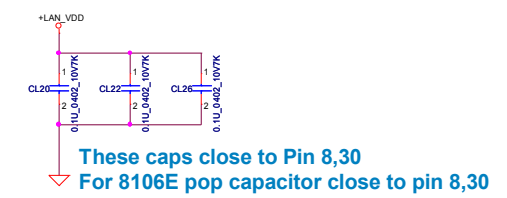


SS table

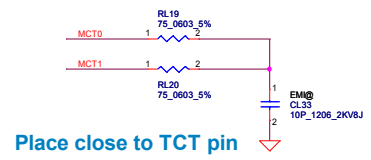
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



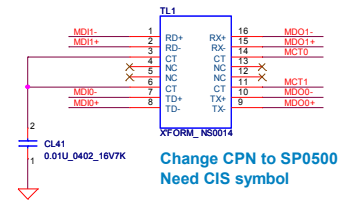
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



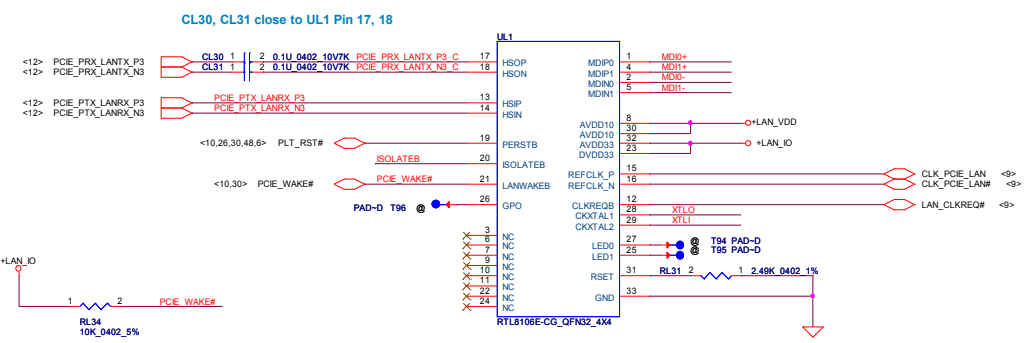
These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30



Place close to TCT pin

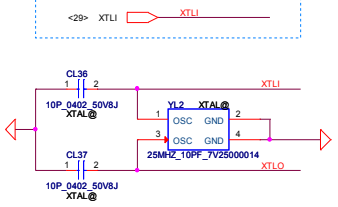


Change CPN to SP050007J00 only
Need CIS symbol

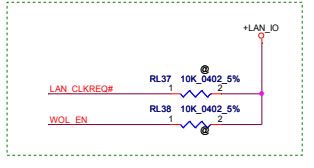
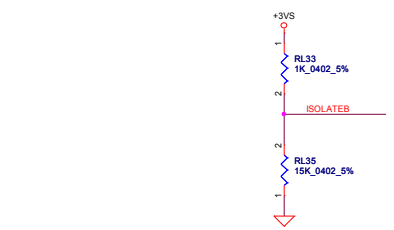


CL30, CL31 close to UL1 Pin 17, 18

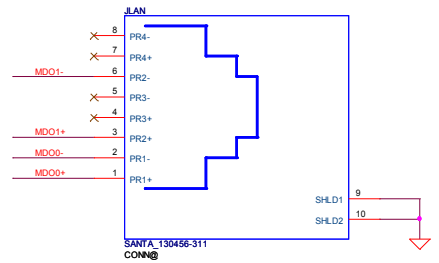
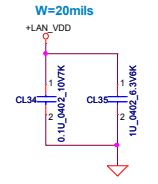
For GCLK



Change CPN to SP050007J00 only
Need CIS symbol



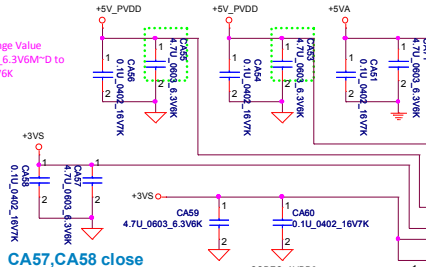
Reserve 10K pull LAN_IO



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				LA-9982P	3.0
			Date:	Wednesday, May 29, 2013	Sheet 21 of 57

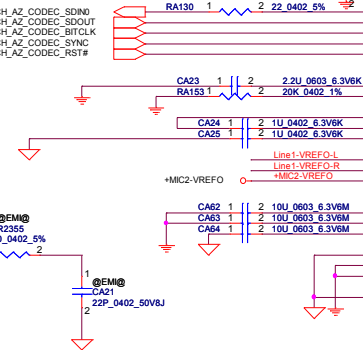
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M-D to 4.7U_0603_6.3V6K

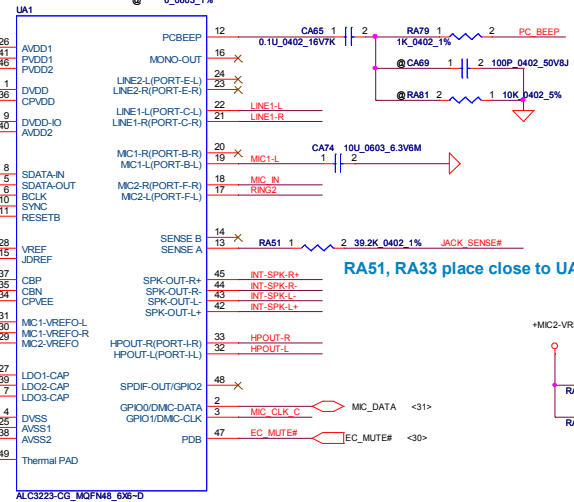
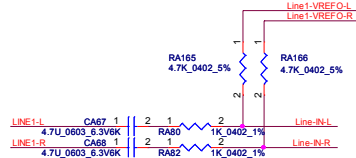
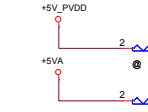


CA57, CA58 close to UA1 pin1

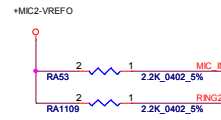
- <8> PCH_AZ_CODEC_SDIND
- <8> PCH_AZ_CODEC_SDOOUT
- <8> PCH_AZ_CODEC_BITCLK
- <8> PCH_AZ_CODEC_SYNC
- <8> PCH_AZ_CODEC_RST#



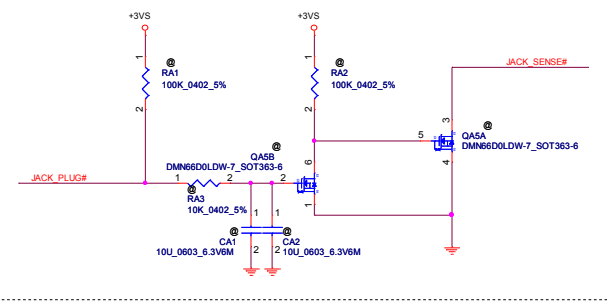
Reserve for HDA issue



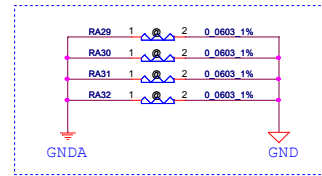
RA51, RA33 place close to UA1



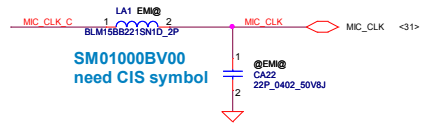
JACK_PLUG Delay circuitis



Reserve for cancel Delay circuitis

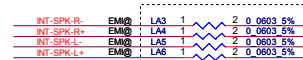


Place on the moat between GND & GNDA.



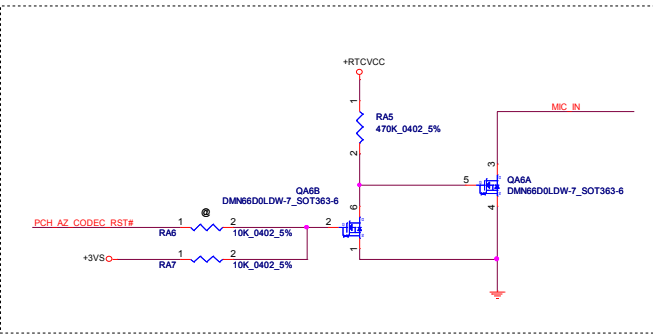
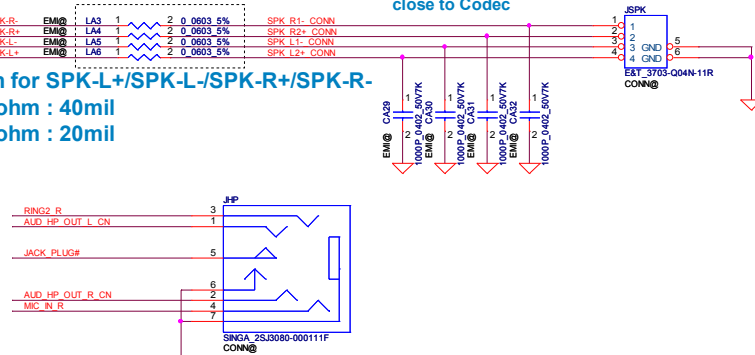
SM1000BV00 need CIS symbol

Close to UA1 Pin11,13,14,16

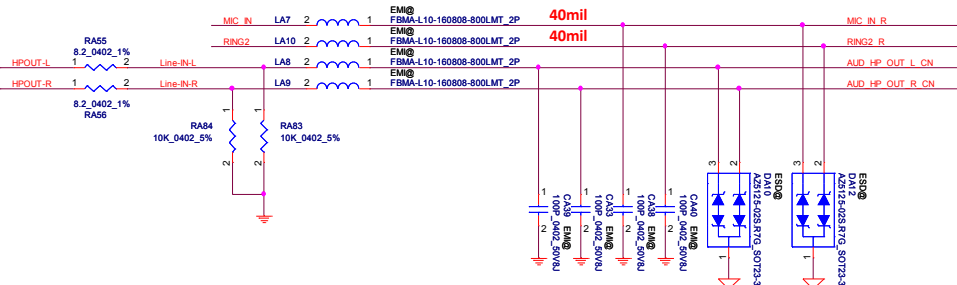


Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R- Speaker 4 ohm : 40mil Speaker 8 ohm : 20mil

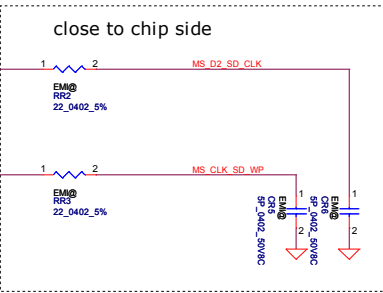
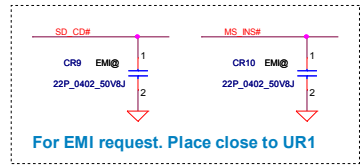
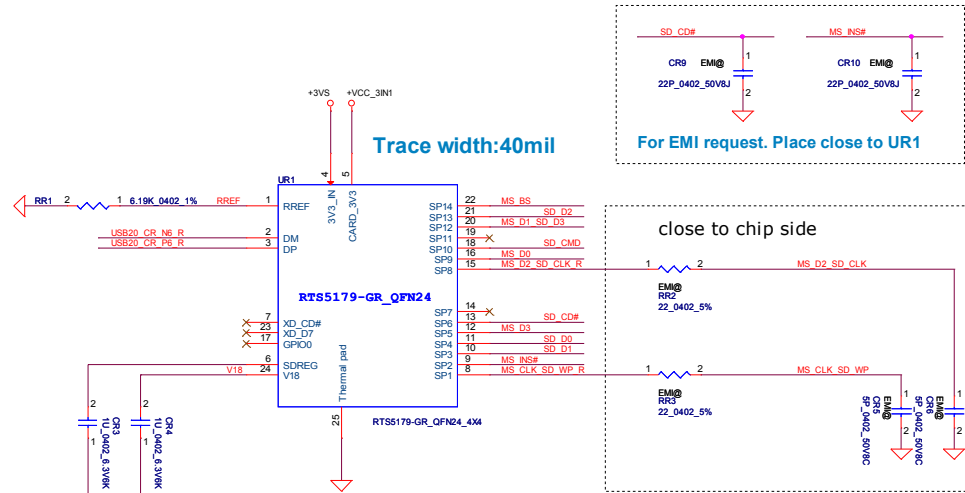
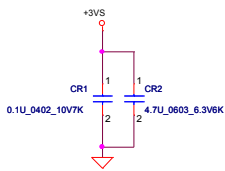
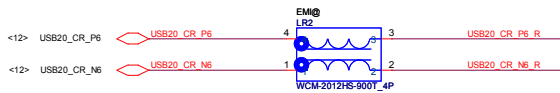
close to Codec



iPhone and Nokia type Combo Jack

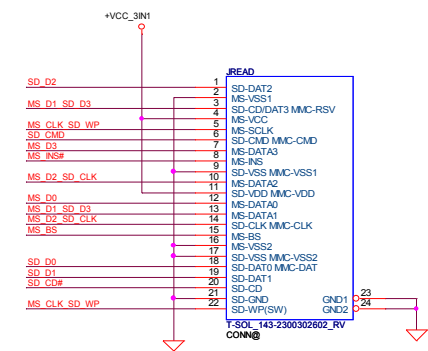
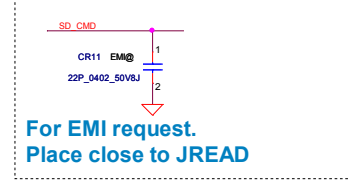
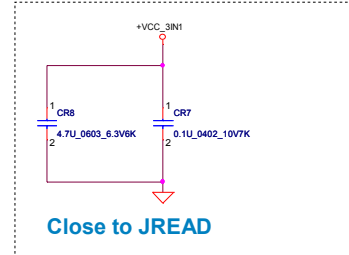


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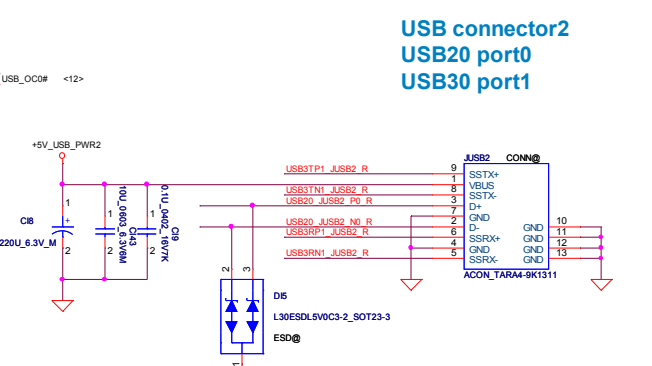
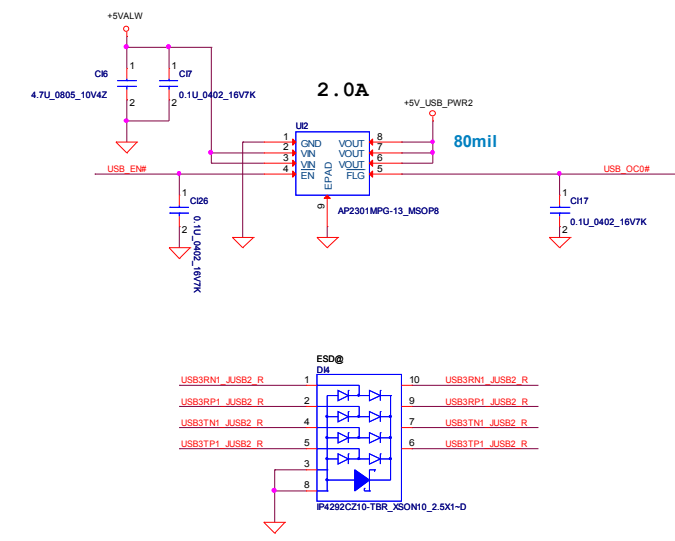
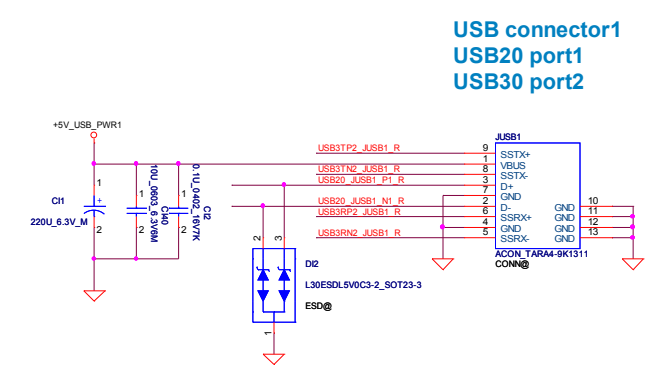
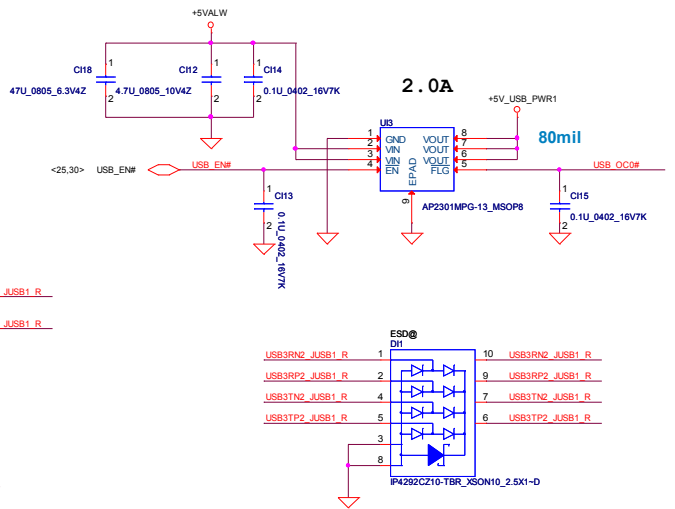
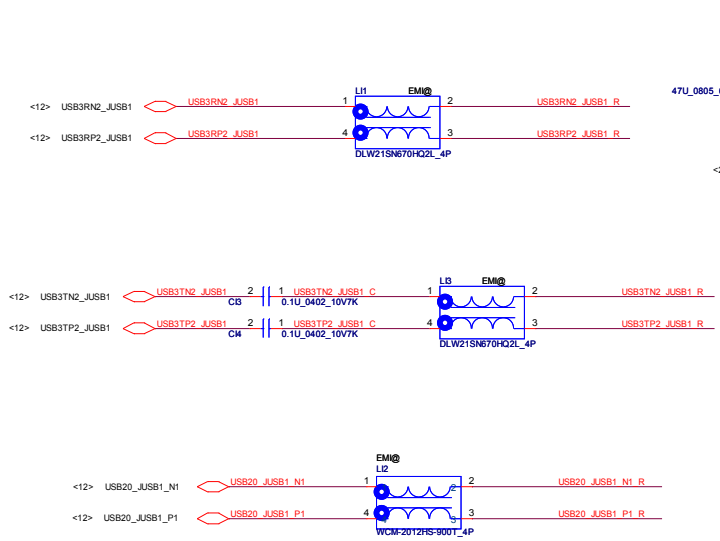


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

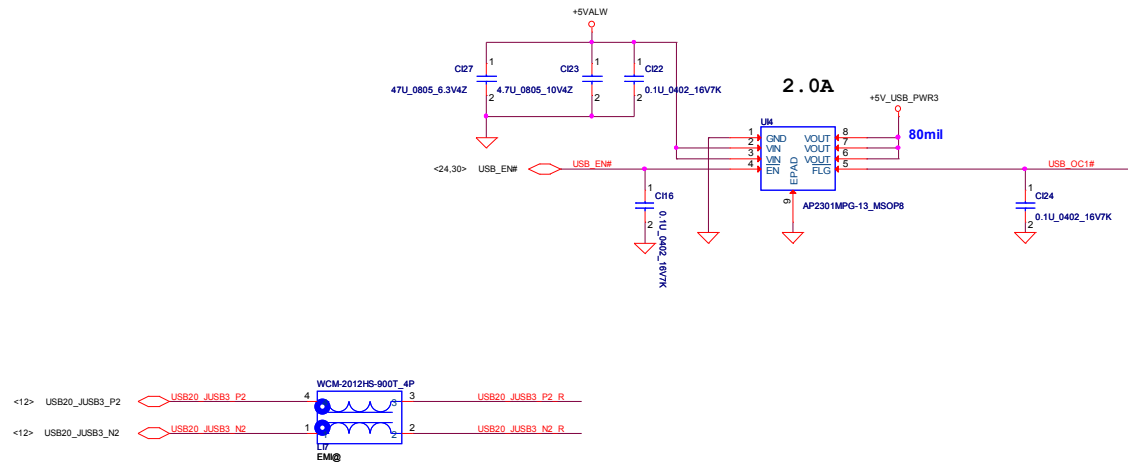
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



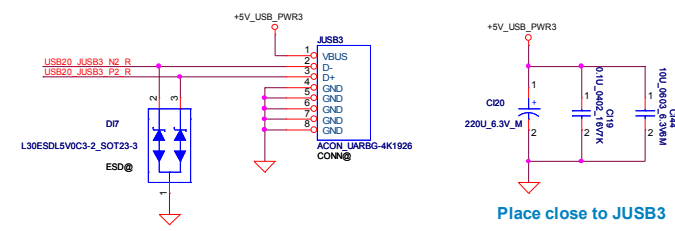
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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Card Reader RTSS179	
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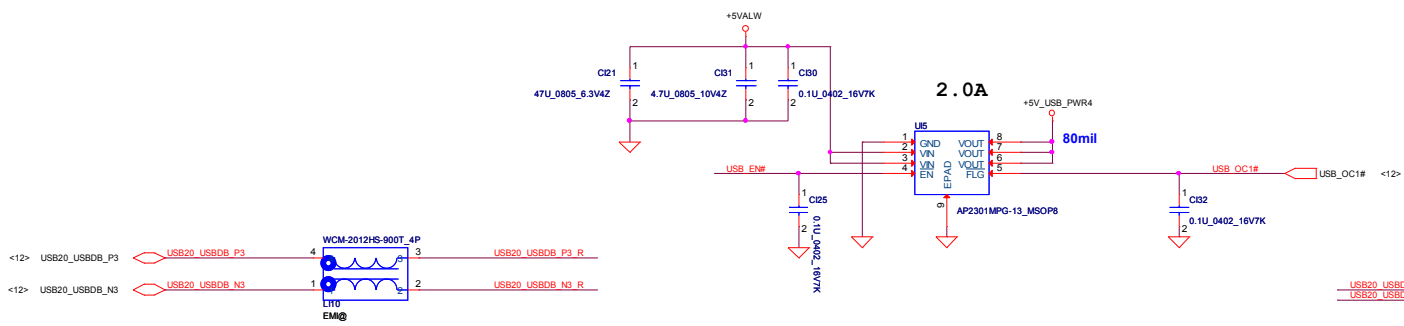
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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Compal Electronics, Inc.	
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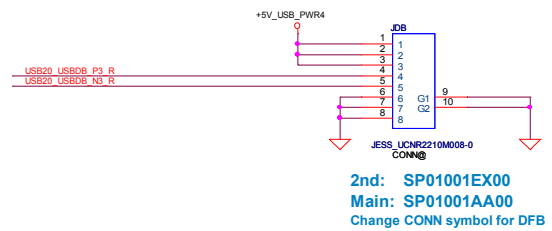
USB connector3
USB20 port2



Place close to JUSB3

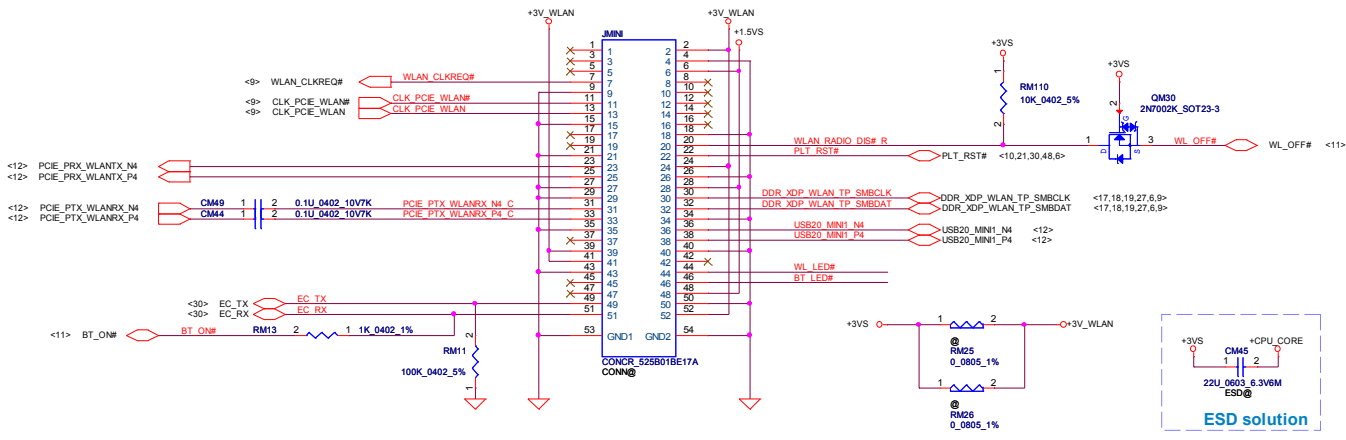
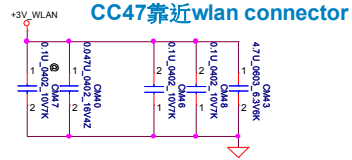


USB connector4
USB20 port3

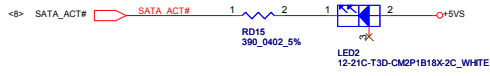


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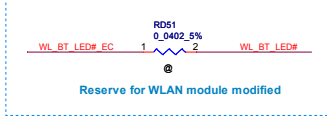
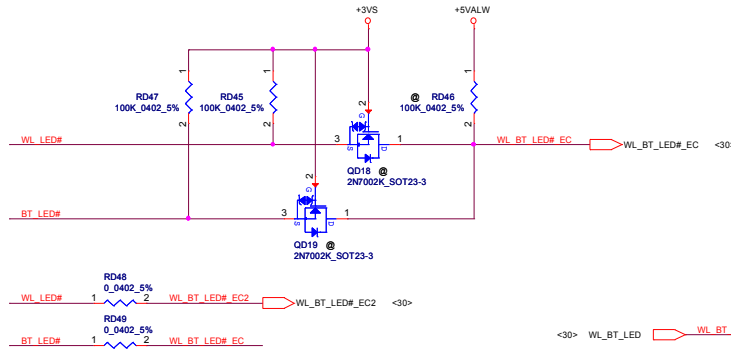
Mini WLAN/WIMAX H=6.7



HDD LED



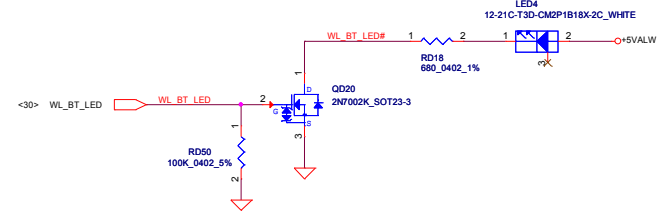
10mils, All pins



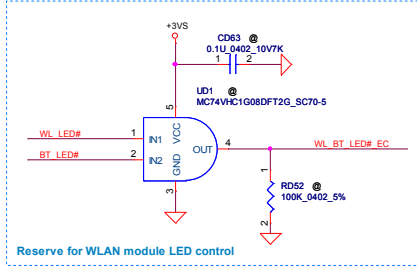
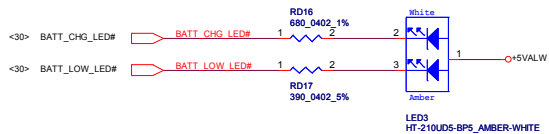
Power LED



Wireless LED

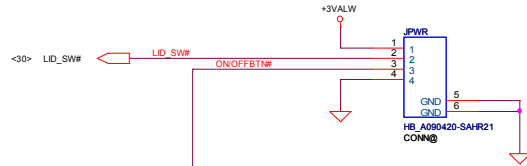


Battery LED



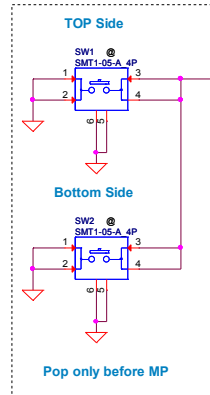
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	Mini Card/LED	
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POWER/B

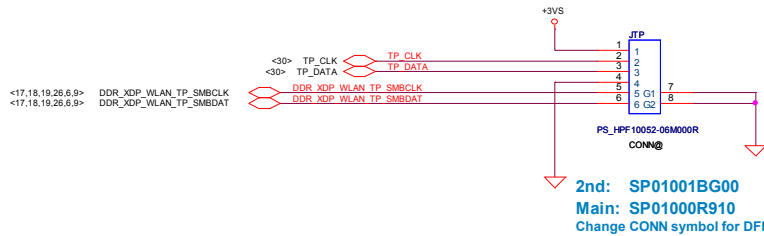


Power ON Circuit

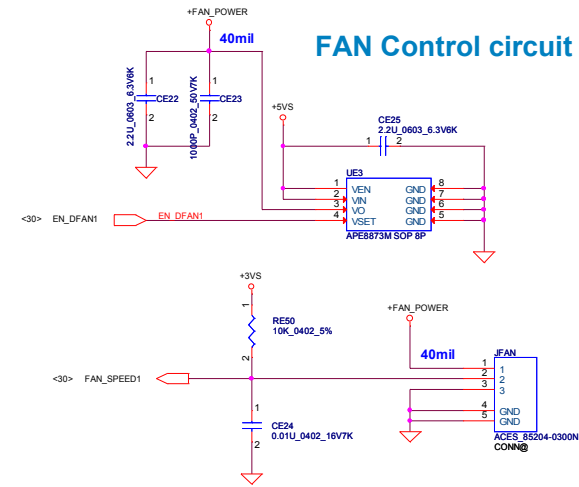
ON/OFF switch



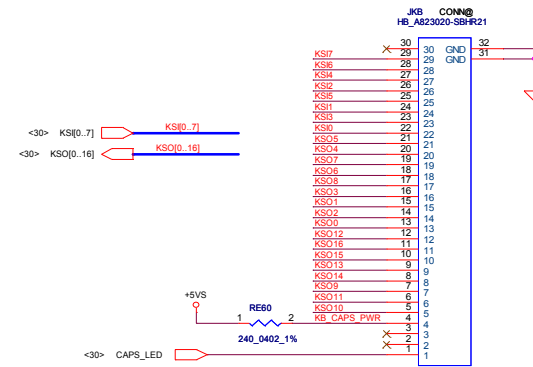
Touch pad



FAN Control circuit

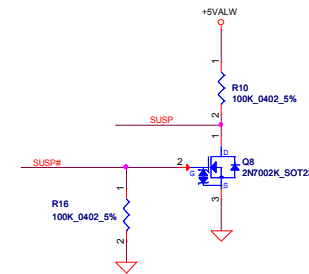
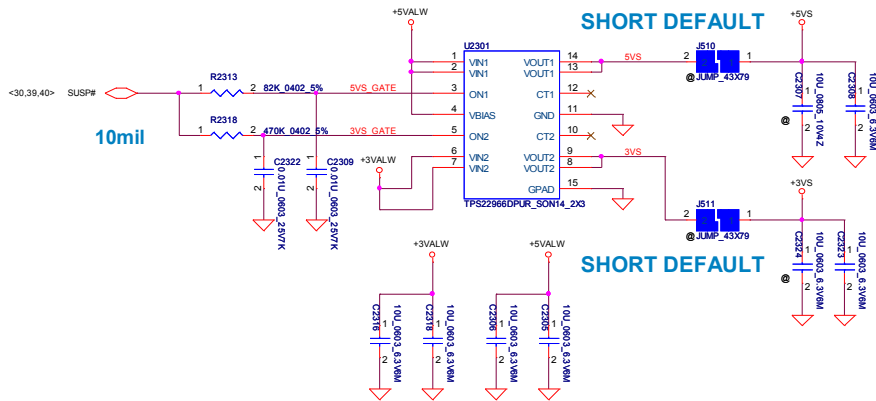


INT_KBD Connector

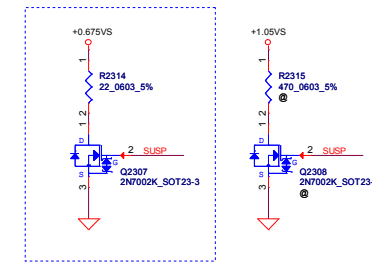
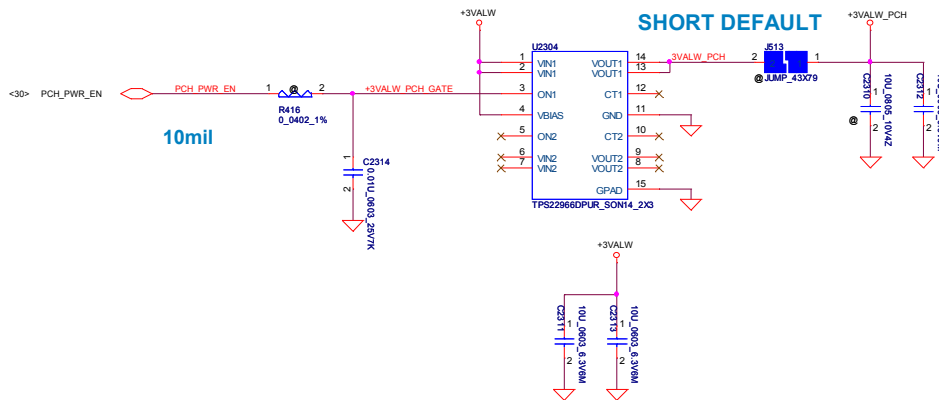


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+5VS and +3VS switch

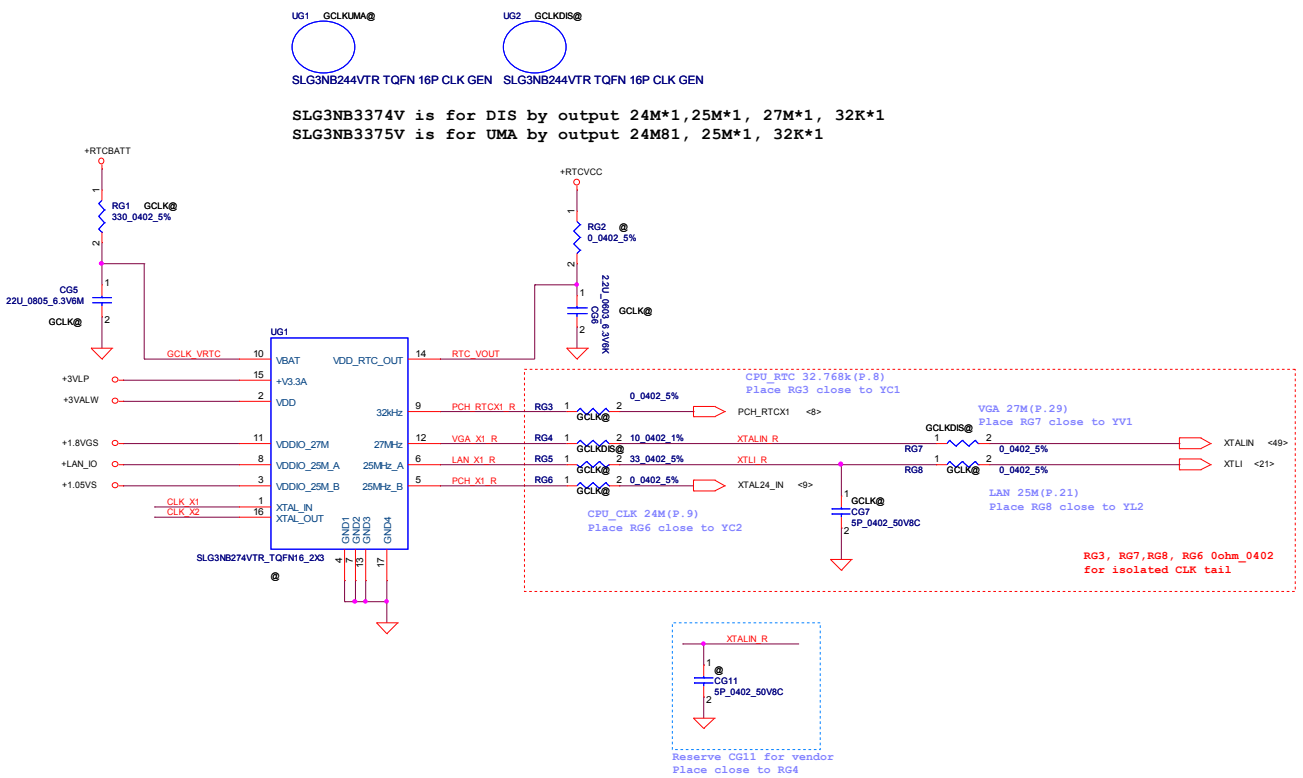
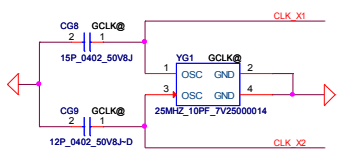
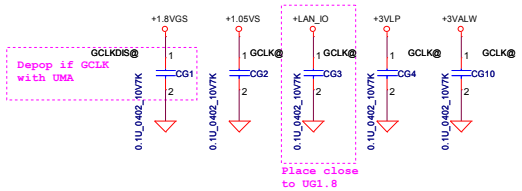


+3VALW_PCH switch



For Intel S3 Power Reduction

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				DC/DC Interface
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				Document Number
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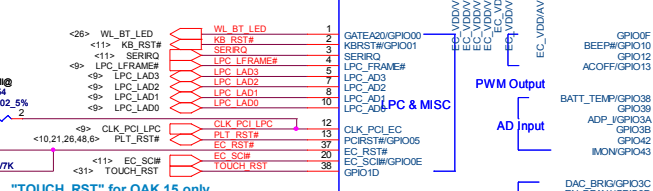
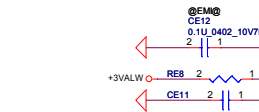
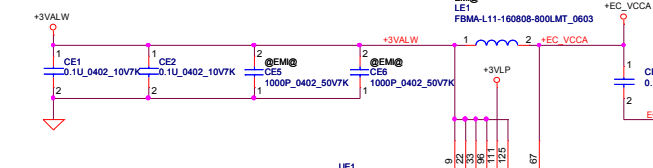
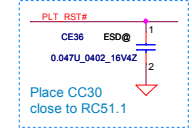
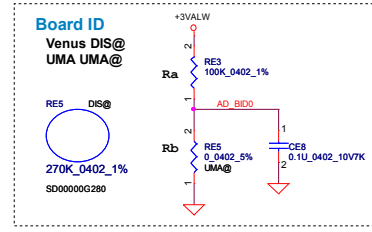
UG1 GCLKMA@
SLG3NB244VTR TQFN 16P CLK GEN

UG2 GCLKDIS@
SLG3NB244VTR TQFN 16P CLK GEN

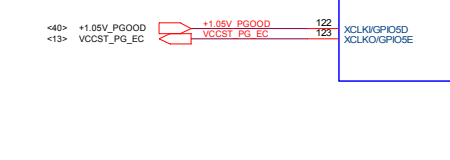
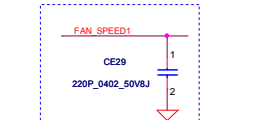
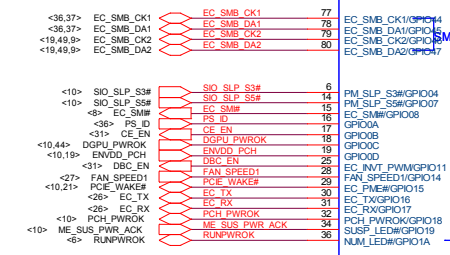
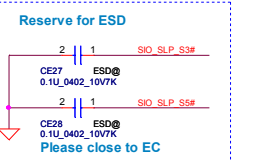
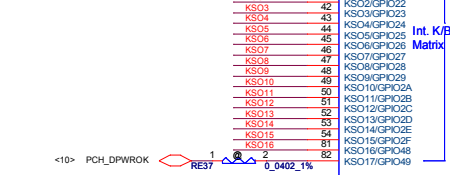
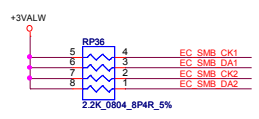
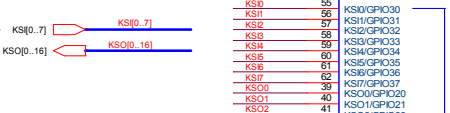
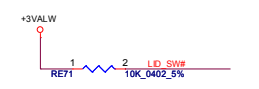
SLG3NB3374V is for DIS by output 24M*1, 25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M*1, 25M*1, 32K*1

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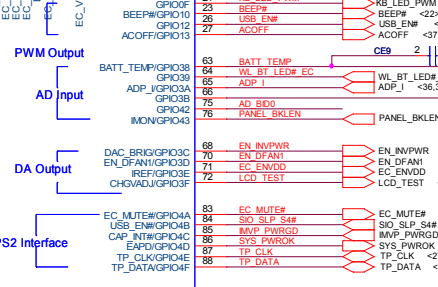
- SD028000080 0_0402_5%
- SD034120280 12K_0402_1%
- SD034100300 27K_0402_1%
- SD034400280 43K_0402_1%
- SD034560280 56K_0402_1%
- SD034750280 75K_0402_1%
- SD034100380 100K_0402_1%
- SD034130380 130K_0402_1%
- SD034160380 160K_0402_1%
- SD034200380 200K_0402_1%
- SD000001B80 240K_0402_1%
- SD00000G280 270K_0402_1%
- SD034330380 330K_0402_1%
- SD028430380 430K_0402_1%



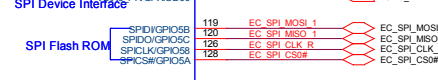
"TOUCH_RST" for OAK 15 only



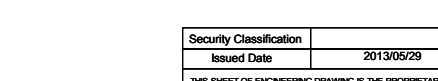
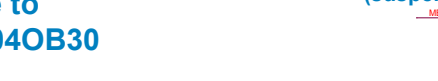
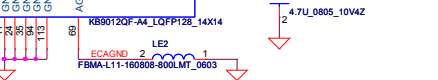
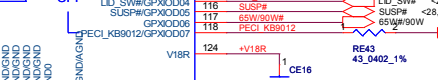
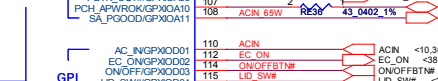
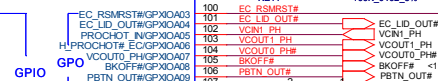
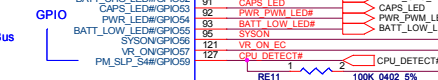
"KB_LED_PWM" for OAK 17 only



EC_MUTE# and SIO_SLP_S4#

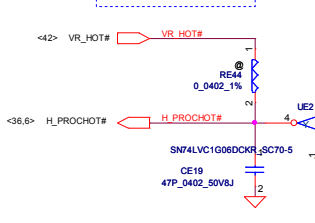
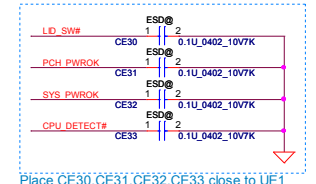
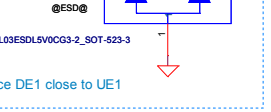
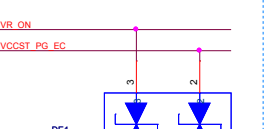


ERP_LOT6 and WL_BT_LED#_EC2



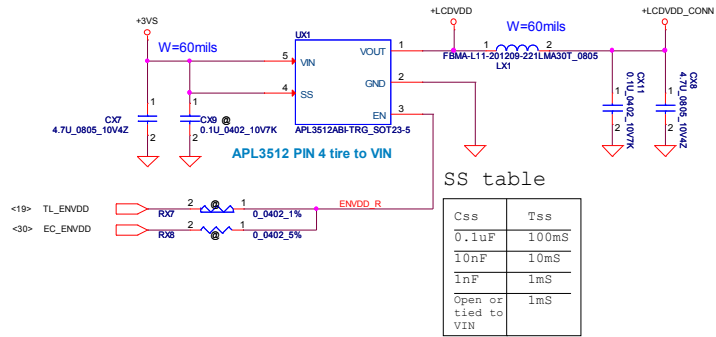
KB9012A3 change to KB9012A4 SA00004OB30

ME_FWP PCH has internal 20K PD. (suspend power rail)

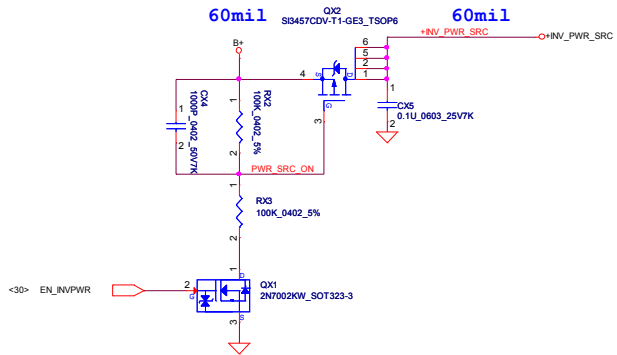


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Size	Document Number	Rev	3.0	Date: Wednesday, May 29, 2013 Sheet 30 of 57	

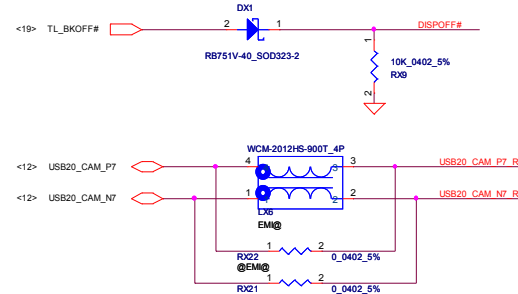
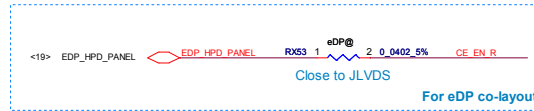
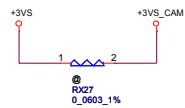
LCD PWR CTRL



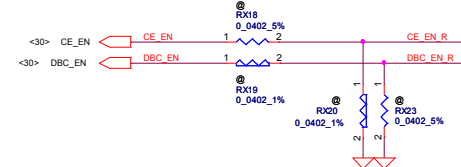
LCD backlight PWR CTRL



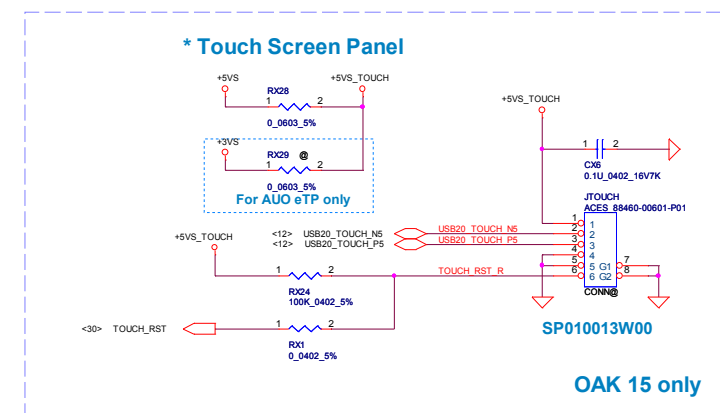
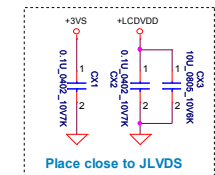
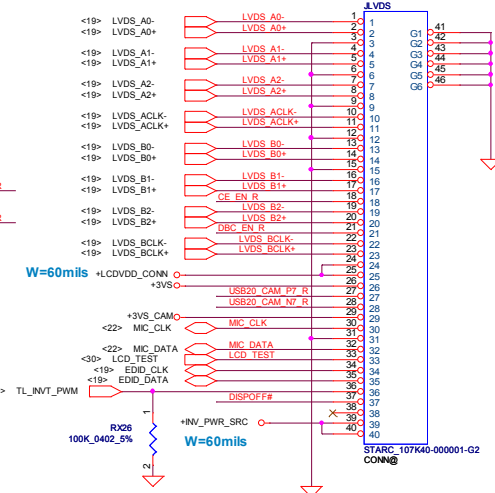
Webcam PWR CTRL



CE_EN_R only for reserve.

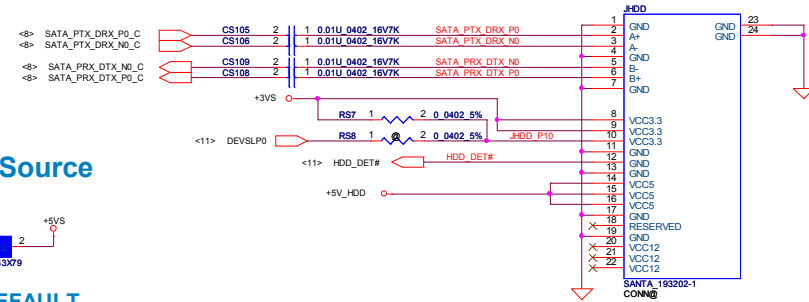


LVDS Connector

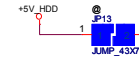


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				Date: Wednesday, May 29, 2013	Sheet 31 of 57

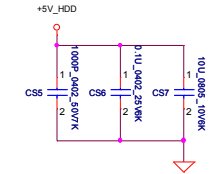
SATA HDD Connector



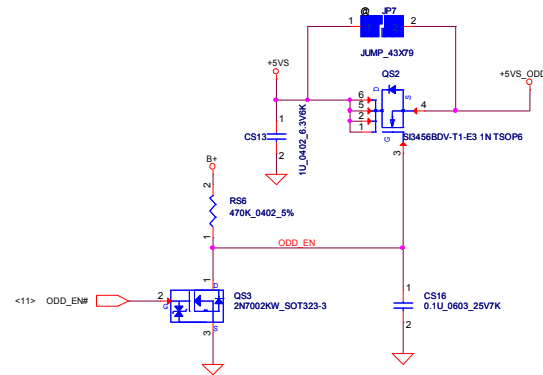
+5V_HDD Source



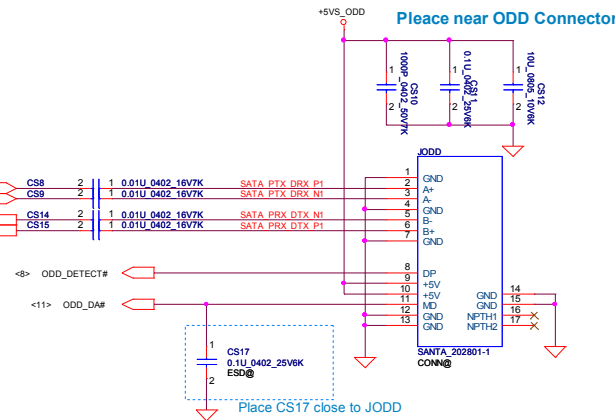
SHORT DEFAULT



ODD Power Control

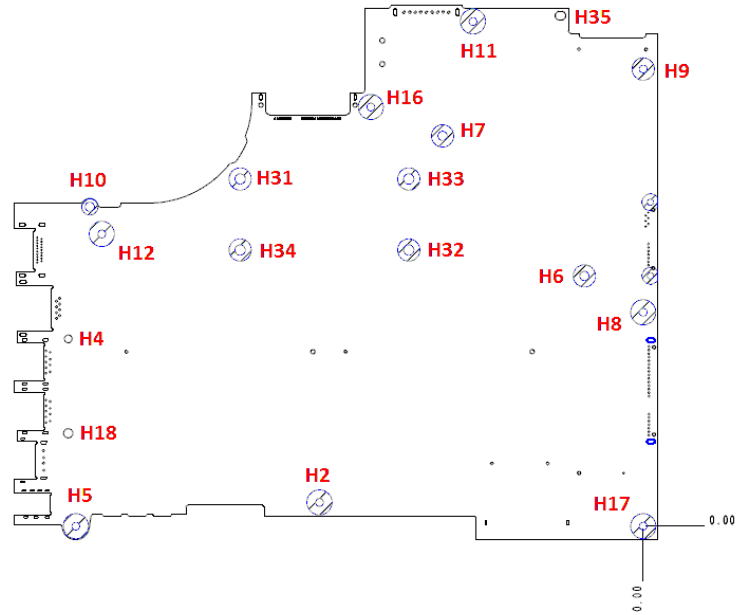
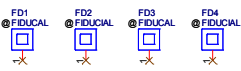
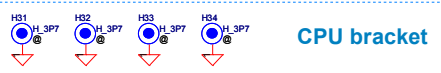
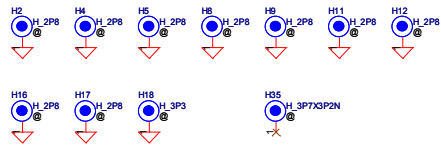


SATA ODD Connector



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Screw Hole

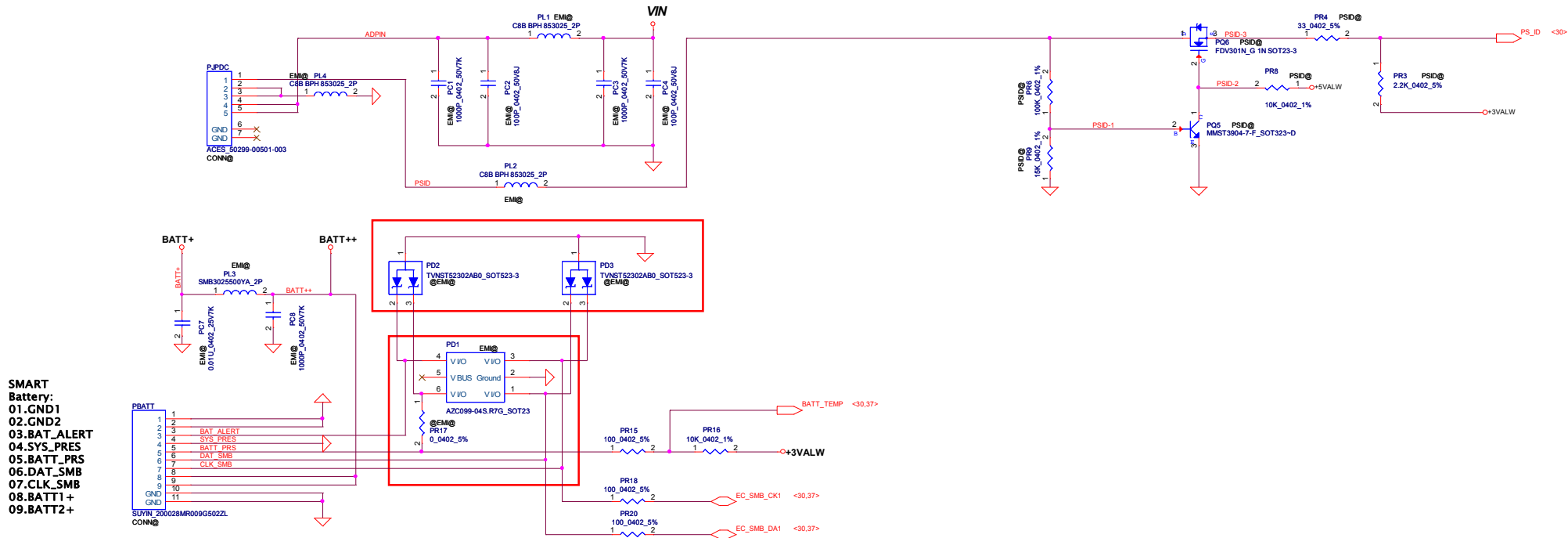


Security Classification	Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	
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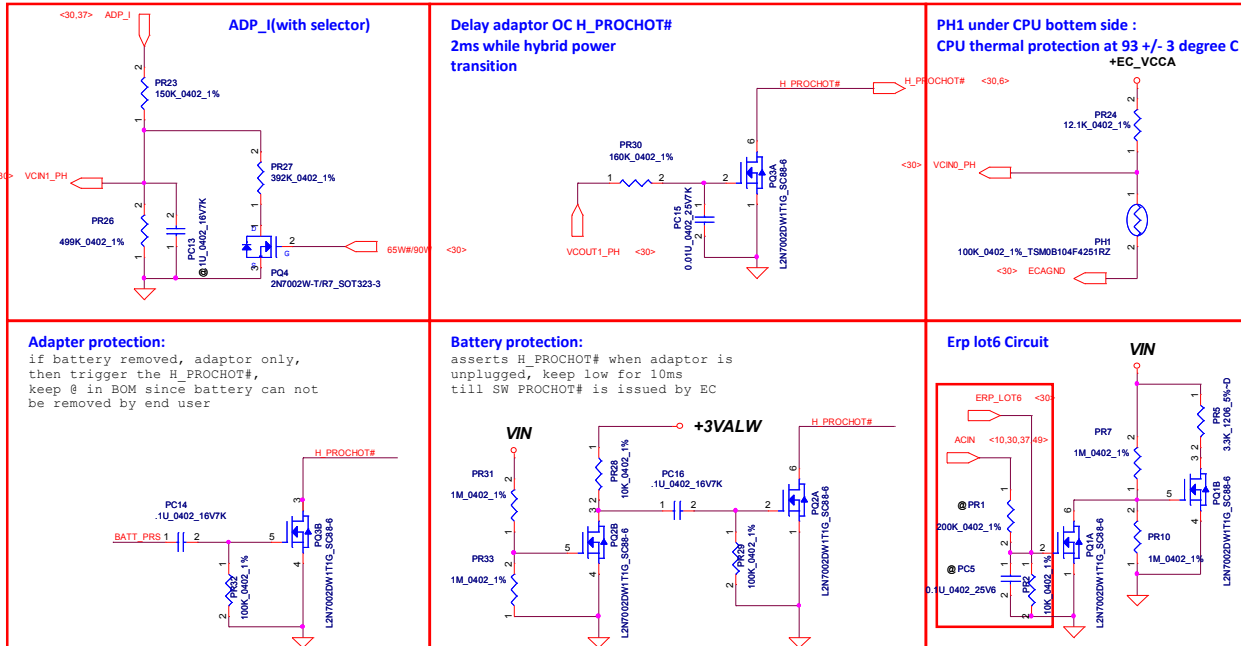
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
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48							
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Other component (37.1)

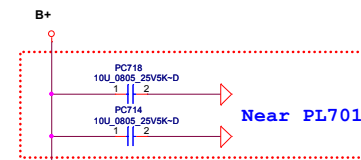
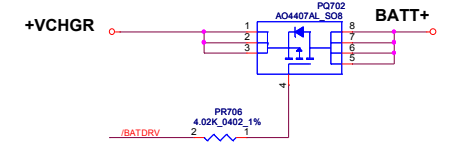
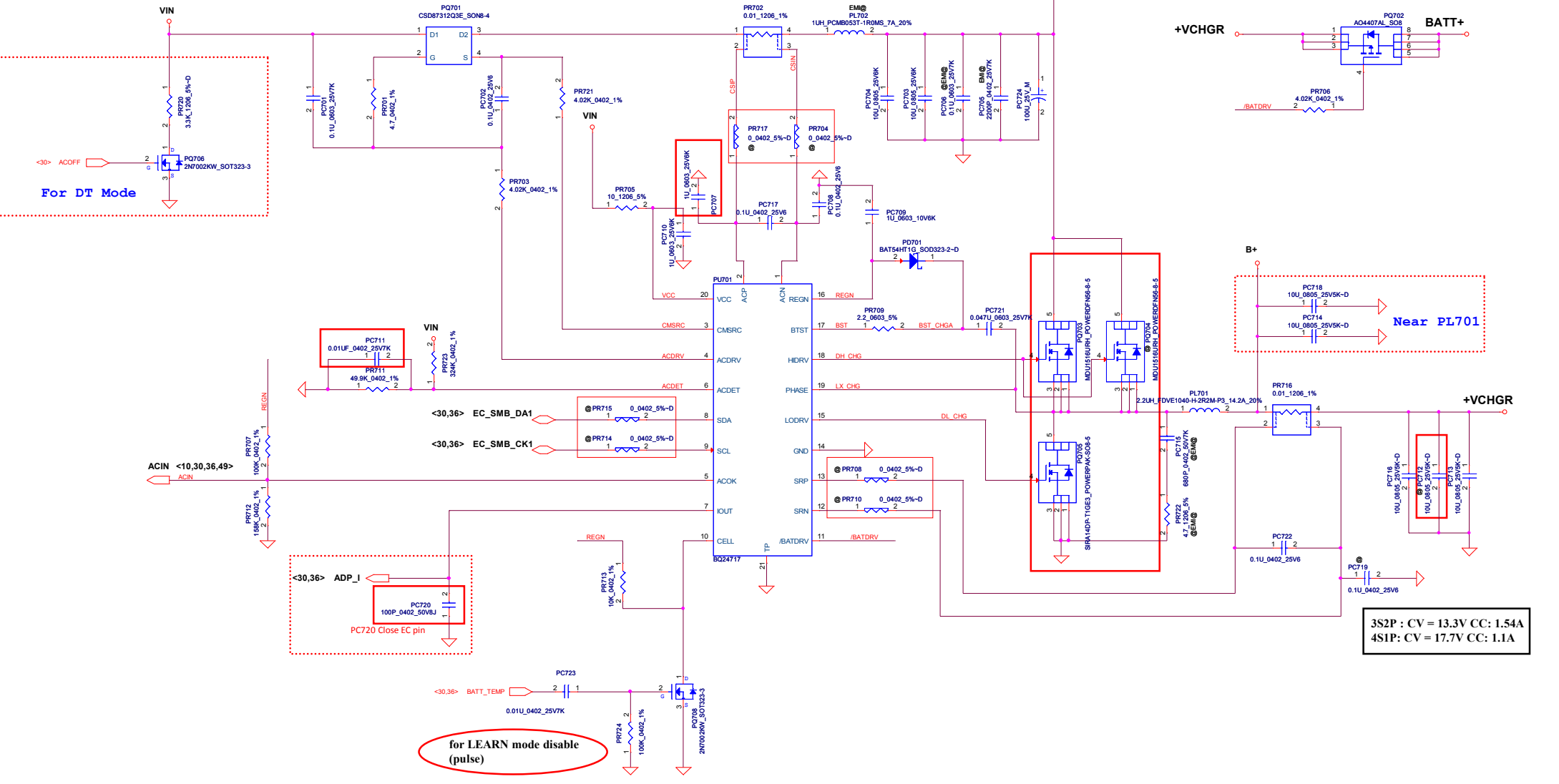


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Iada=0~3.33A (65W)

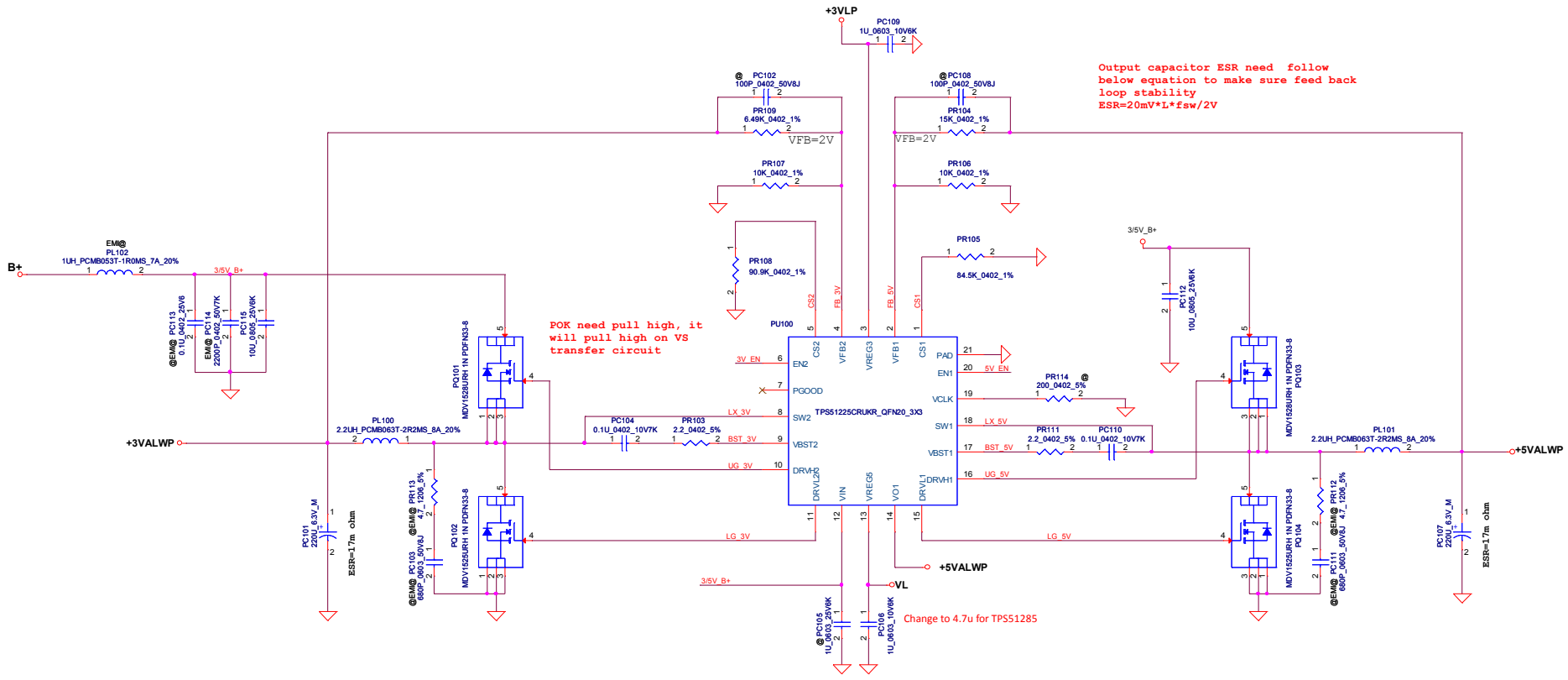
Iada=0~4.62A (90W)

$ADP_I = 40 * I_{adapter} * R_{sense}$



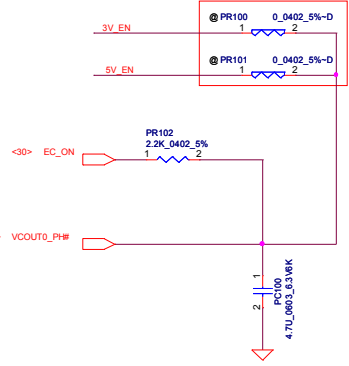
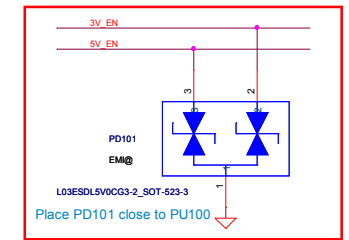
3S2P : CV = 13.3V CC: 1.54A
 4S1P : CV = 17.7V CC: 1.1A

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3VALWP
 TDC 5.95A
 Peak Current 8.5A
 OCP current 10.2A

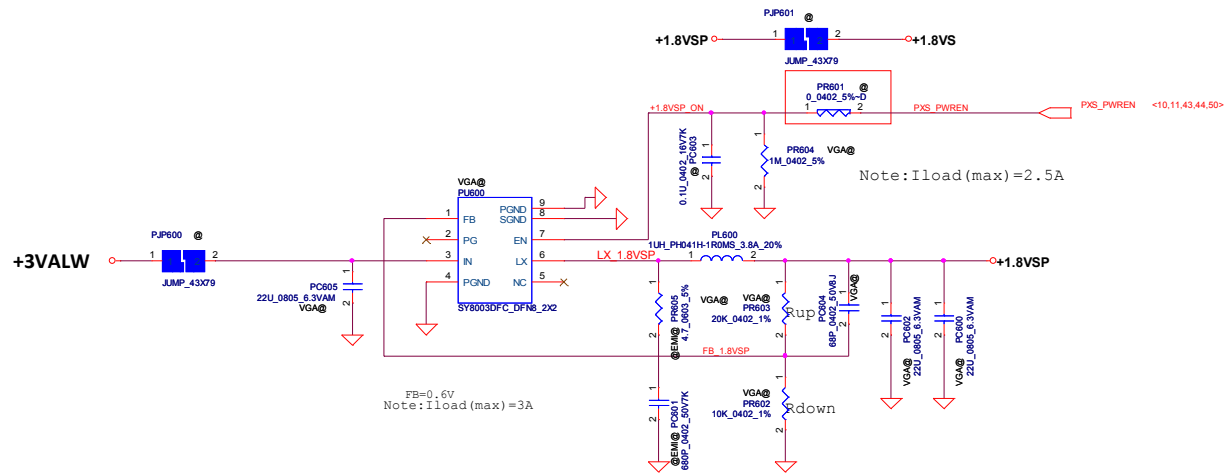
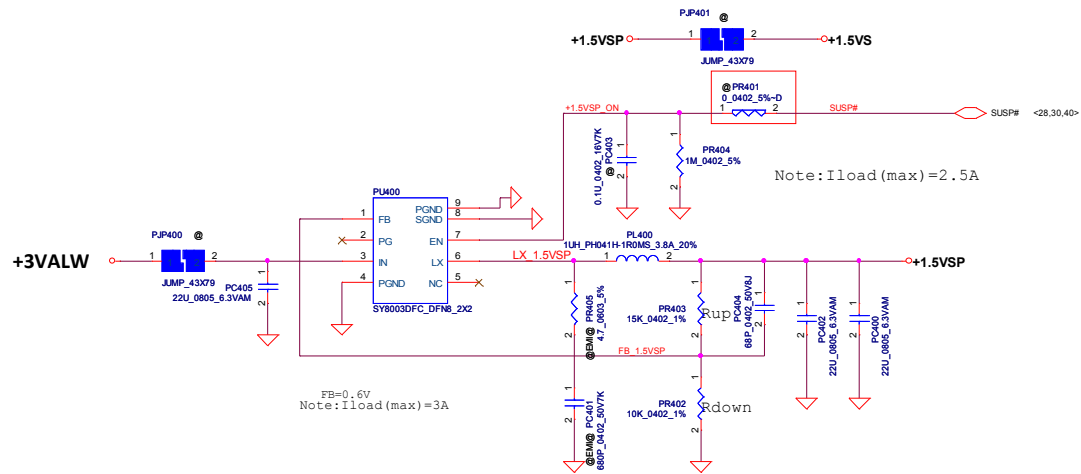
TYP	MAX
H/S Rds (on) : 22mohm	30mohm
L/S Rds (on) : 10.8mohm	13.6mohm



5VALWP
 TDC 5.96A
 Peak Current 8.51A
 OCP current 10.2A

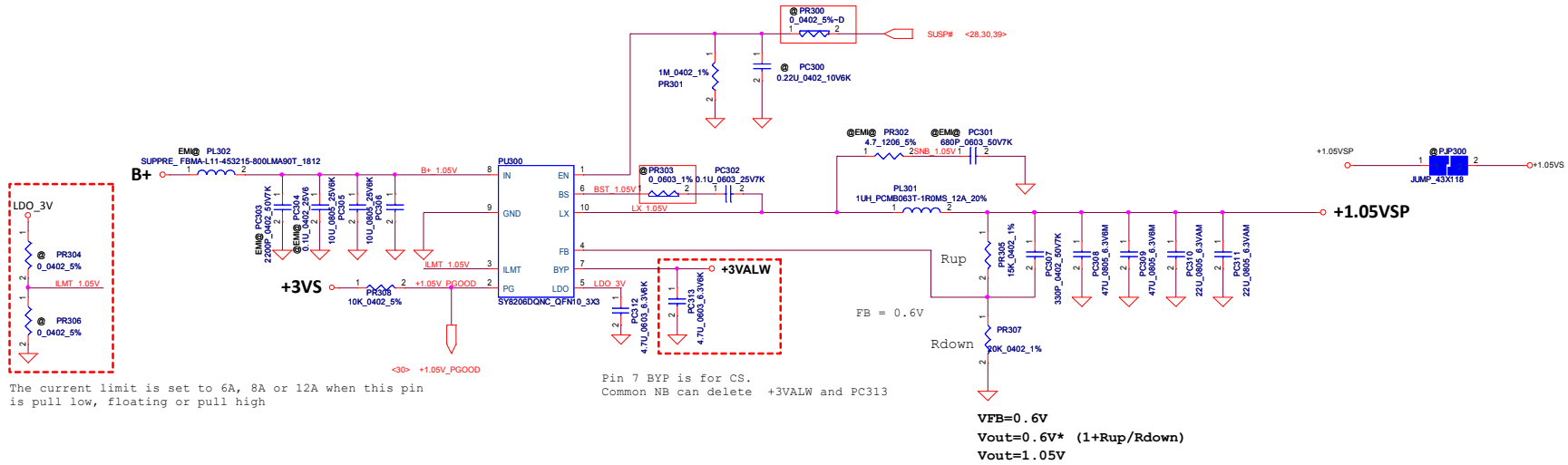
TYP	MAX
H/S Rds (on) : 22mohm	30mohm
L/S Rds (on) : 10.8mohm	13.6mohm

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EN pin don't floating
 If have pull down resistor at HW side, pls delete PR301



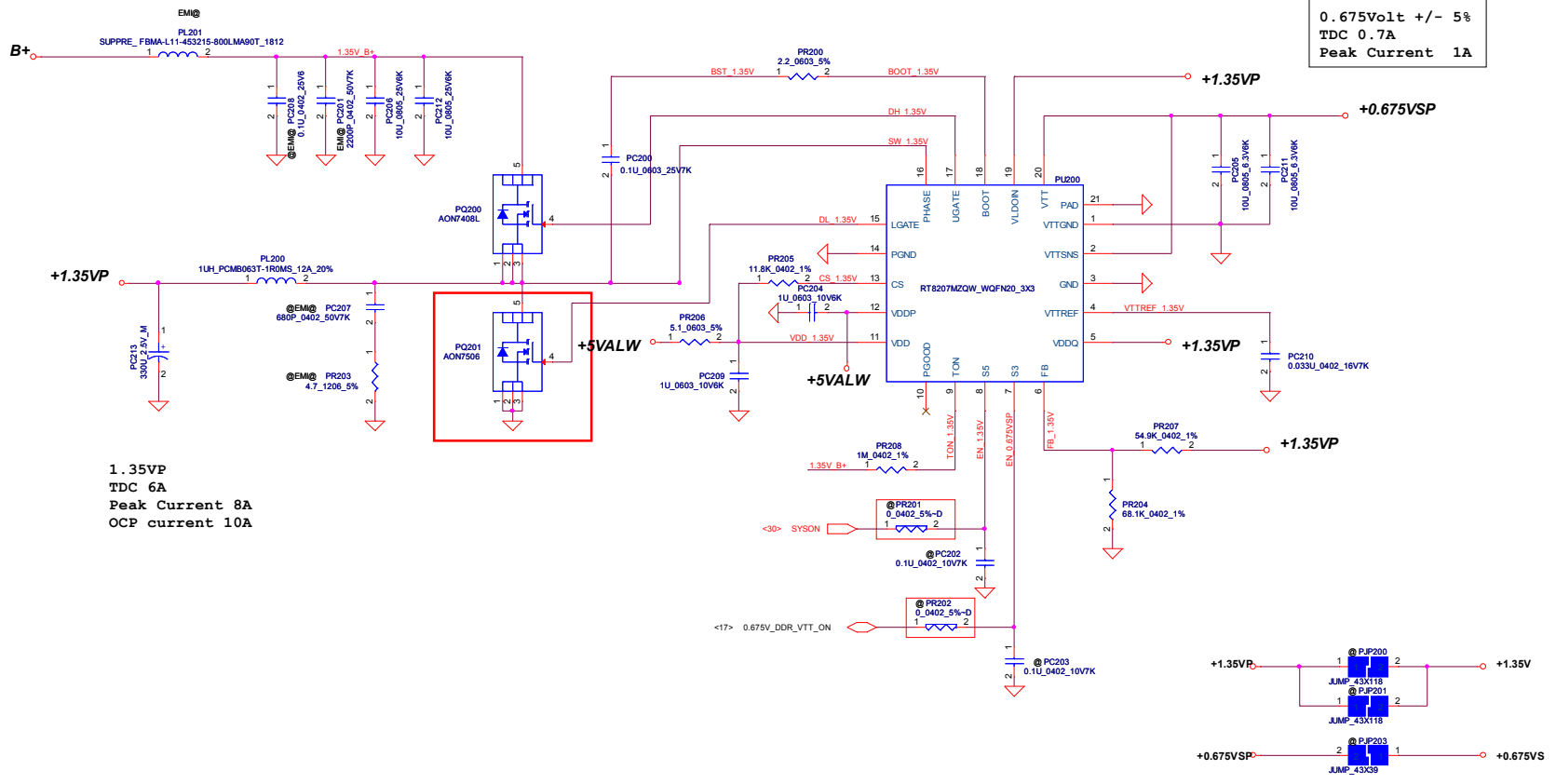
The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
 Common NB can delete +3VALW and PC313

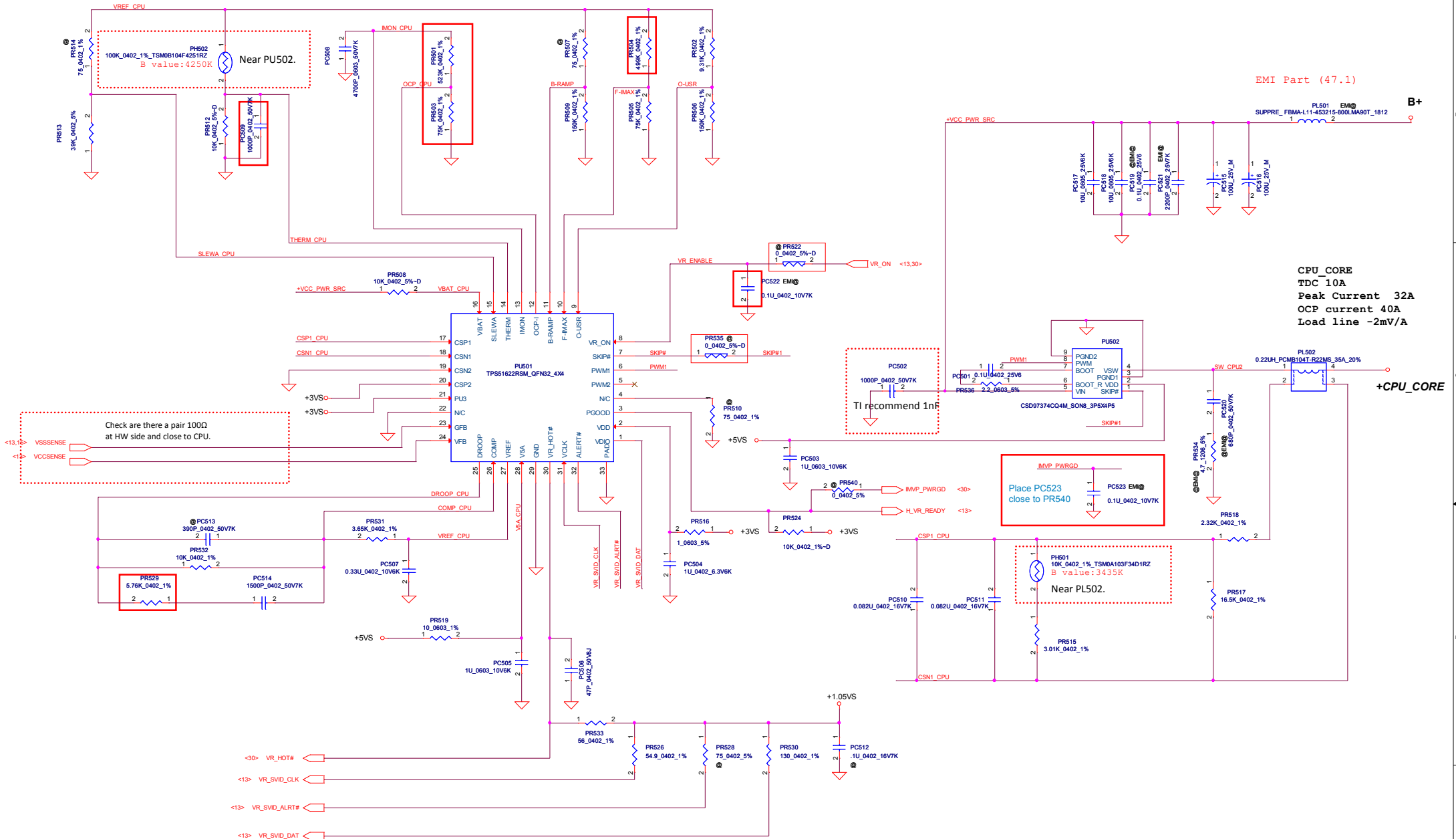
$V_{FB} = 0.6V$
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$
 $V_{out} = 1.05V$

+1.05VSP
 TDC 5A
 Peak Current 6.6A
 OCP current 8A

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EMI Part (47.1)

CPU_CORE
TDC 10A
Peak Current 32A
OCP current 40A
Load line -2mV/A

Check are there a pair 100Q
at HW side and close to CPU.

I.M.P. PWRGD
Place PC523
close to PR540

TI recommend 1nF

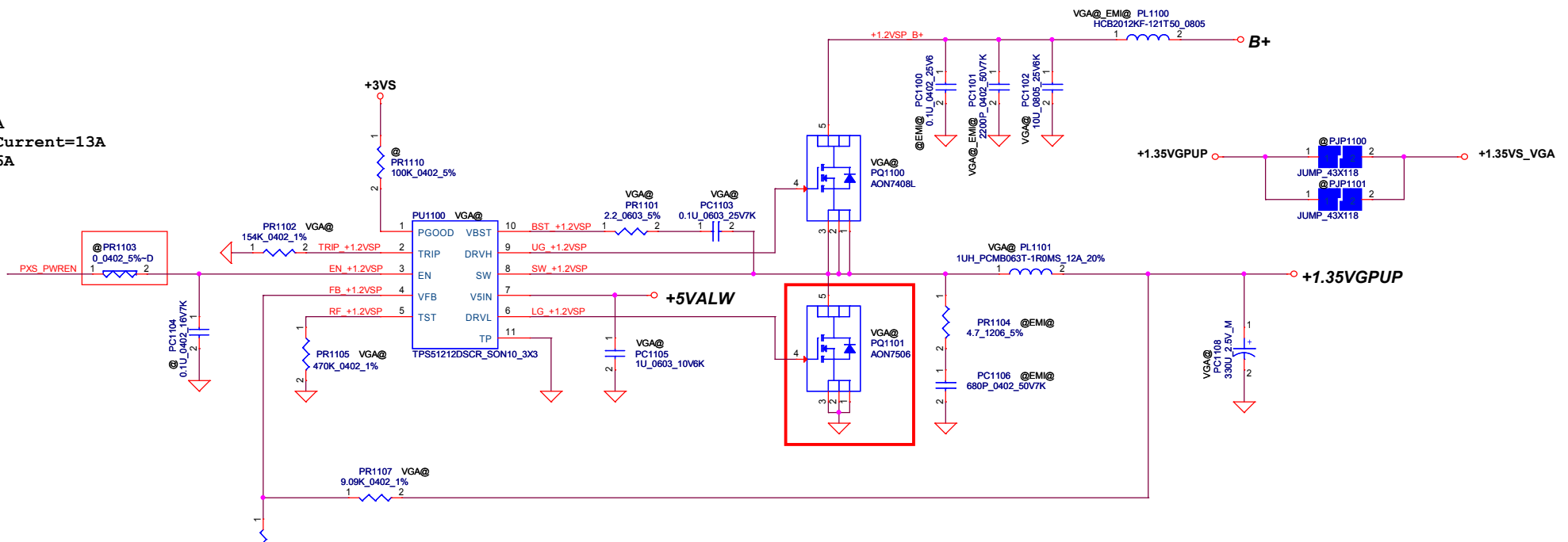
VR_ENABLE
VR_ON <13.30>

Near PL502.

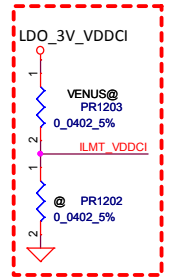
- <30> VR_HOT#
- <13> VR_SVID_CLK#
- <13> VR_SVID_ALRT#
- <13> VR_SVID_DAT#

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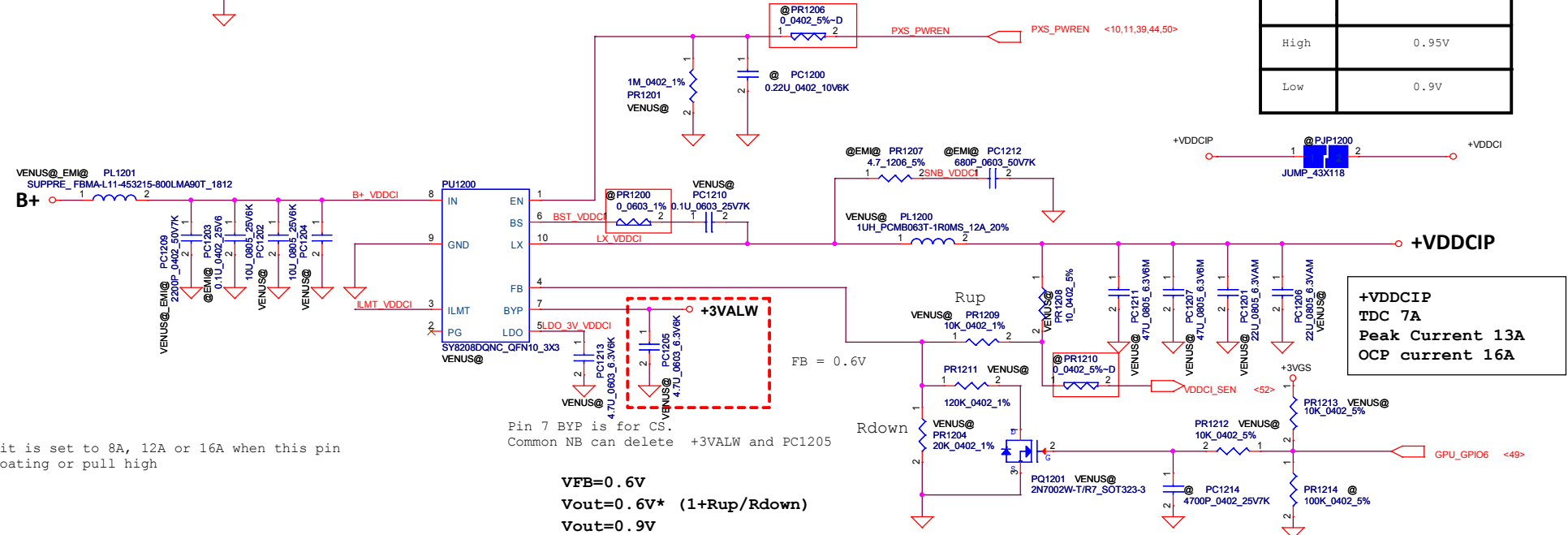
TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

$$V_{FB} = 0.6V$$

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$V_{out} = 0.9V$$

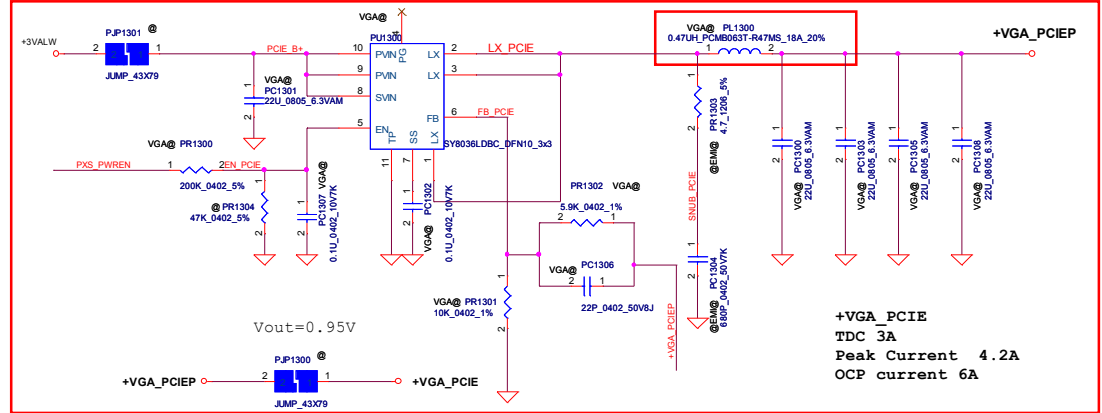
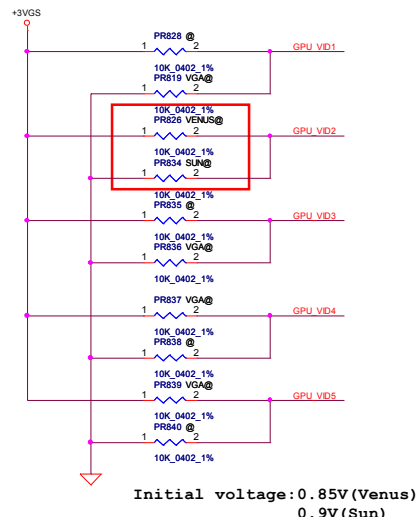
Security Classification	Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	PWR +1.35VGPU/VDDCIP
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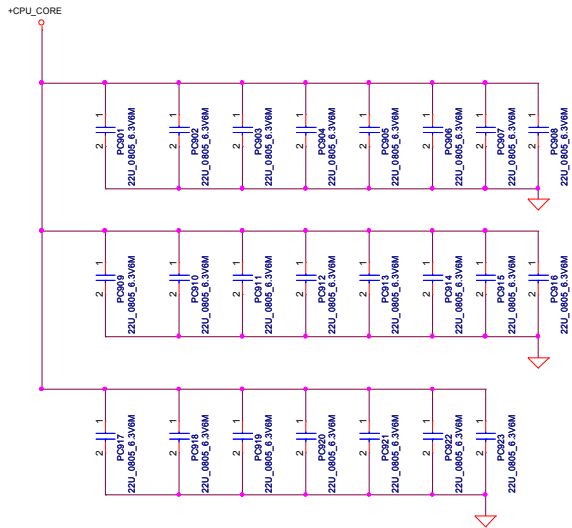
	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

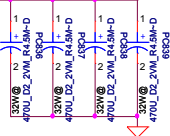
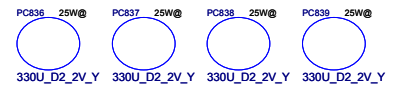
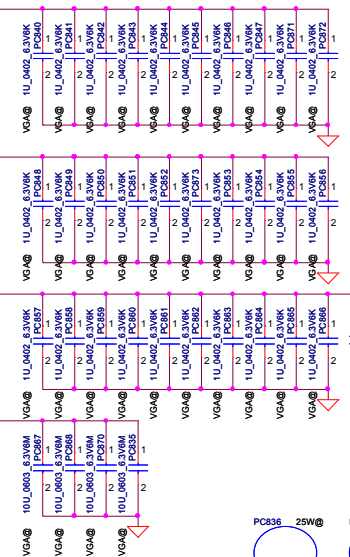
VGA_CORE
 Frequency 300kHz
 TDC 23A (25W) / 33A (32W)
 Peak Current 30A (25W) / 47A (32W)
 OCP current 36A (25W) / 56A (32W)
 TYP MAX
 H/S Rds (on) : 12.2mohm , 15mohm
 L/S Rds (on) : 2.75mohm , 3.5mohm
 Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)
 Load line : -1.5mV/A

SPU_VID5 (GPIO_10)	SPU_VID4 (GPIO_14)	SPU_VID3 (GPIO_15)	SPU_VID2 (GPIO_16)	SPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	1	1	0.775V



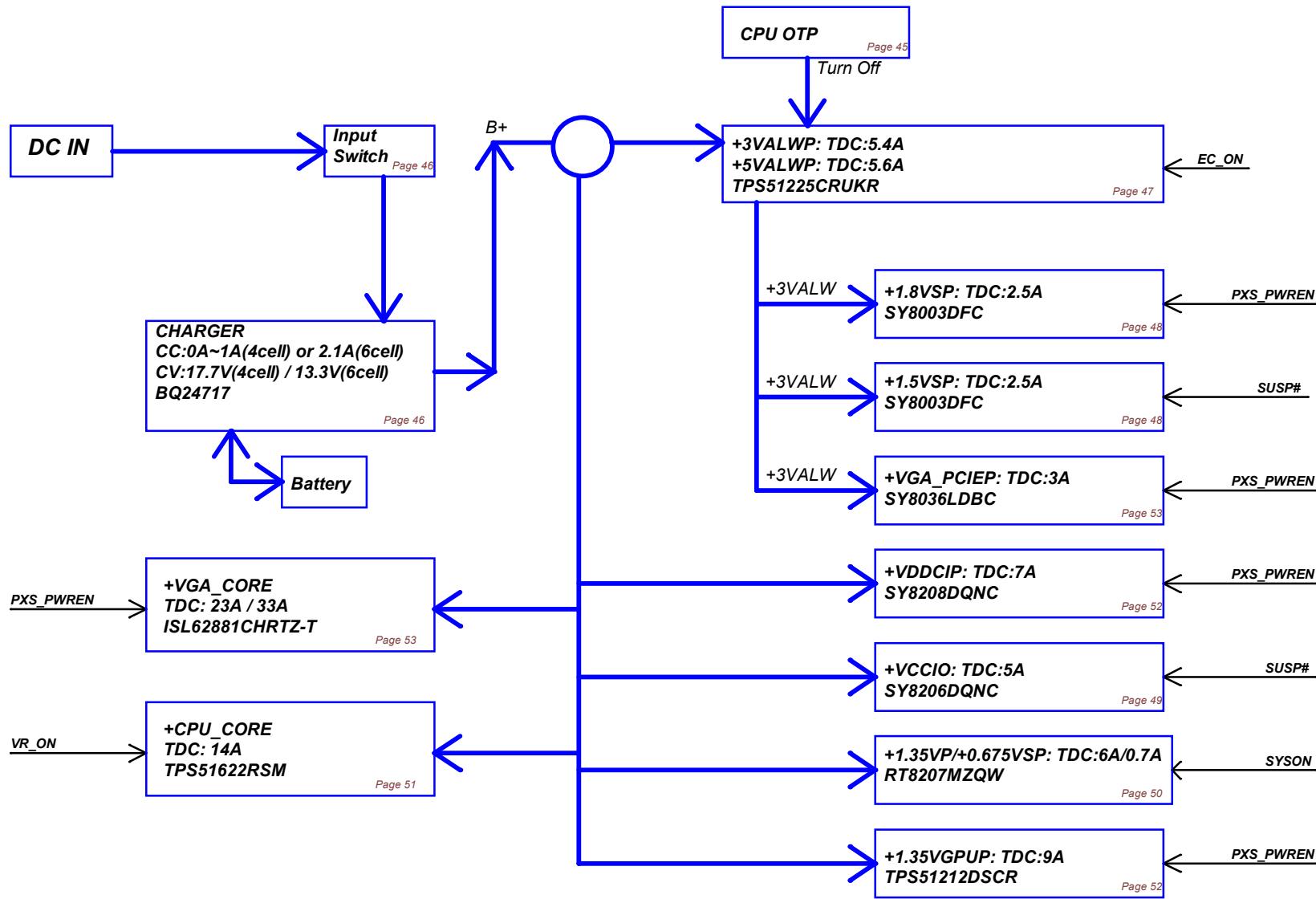


+VGA_CORE



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Power block



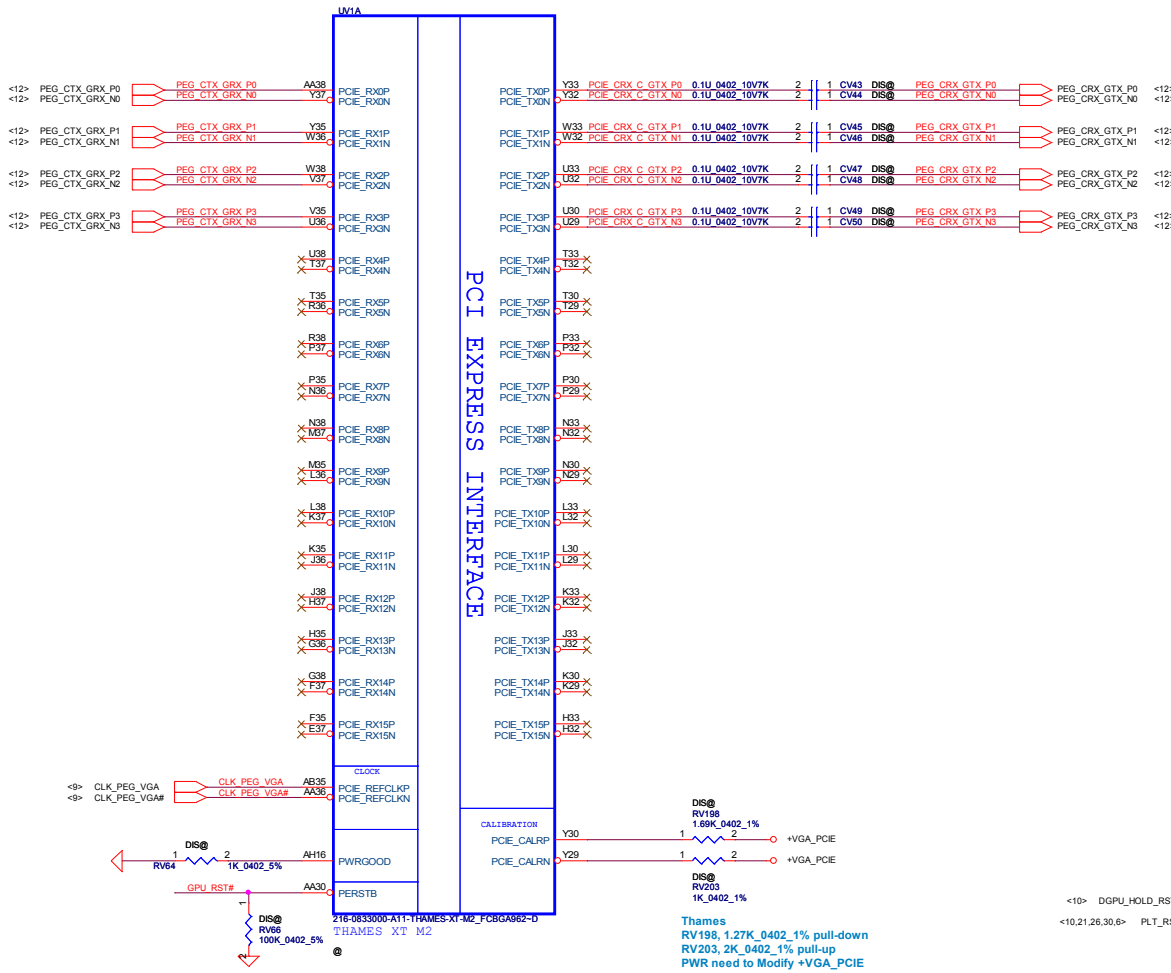
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Version Change List (P. I. R. List)

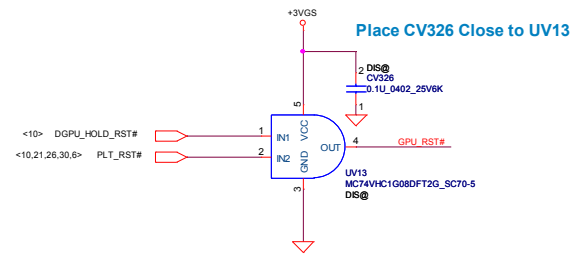
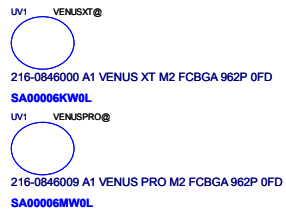
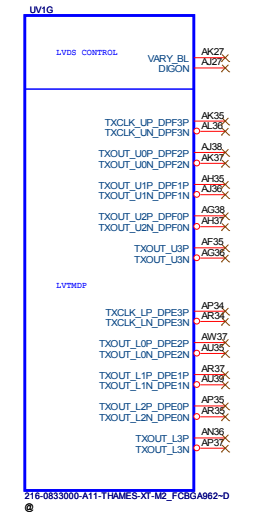
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF 0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/SVALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101 (SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vander request	unpop PR826 and pop PR834 (only for Sun XT)	0.4
8	37 38 39 40 41 42	CHARGER 3.3VALWP/SVALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100, PR101, PR201, PR202, PR300, PR303, PR401, PR522, PR535, PR704, PR708, PR710, PR714, PR715, PR717	1.0
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	2.0
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	2.0
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601, PR802, PR803, PR814, PR823, PR830, PR845, PR846, PR1103, PR1200, PR1206, PR1210	2.0
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EVerify ok only for Sun XT	unpop PL1200, PL1201, PU1200, PQ1201, PR1201, PR1203, PR1204, PR1208, PR1209, PR1211, PR1212, PR1213, PC1201, PC1202, PC1204, PC1205, PC1206, PC1207, PC1209, PC1210, PC1211, PC1213 (only for Sun XT)	2.0
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	2.0
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10kOhm	2.0
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	2.0
16	36	DCIN/BATT CONN/OTP	13/05/22	Morris	reserve parts from ESD request	reserve PD2, PD3, PR17 and unpop PR17	3.0

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GFX PCIe LANE REVERSAL



LVDS Interface

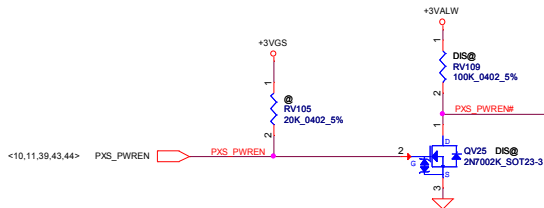


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PX_MODE=1 for Normal Operation
 PX_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE_VDDC and 1.8V rail

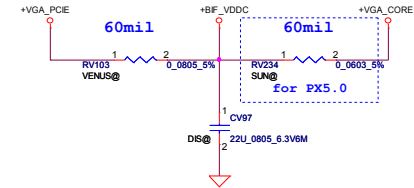
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
 PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
 PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

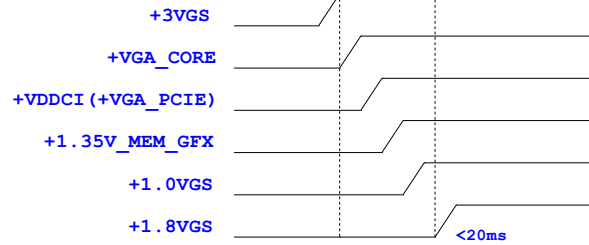


for PX4.0 and PX5.0

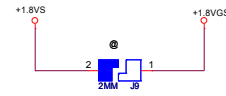
Switch circuits in BACO desings for Thames/Seymour only
 55mA@1.0V, in BACO mode



Power sequence of Sun XT, Venus Pro, Venus XT

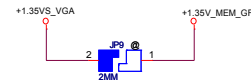


+1.8VS TO +1.8VGS



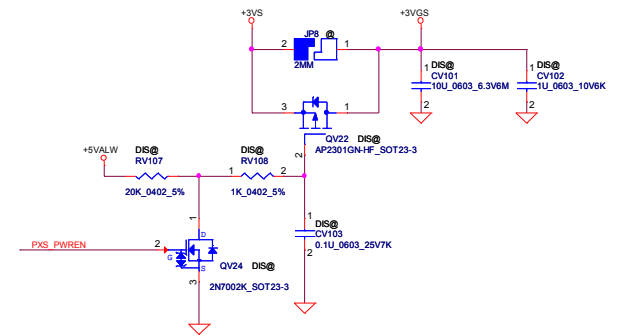
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX

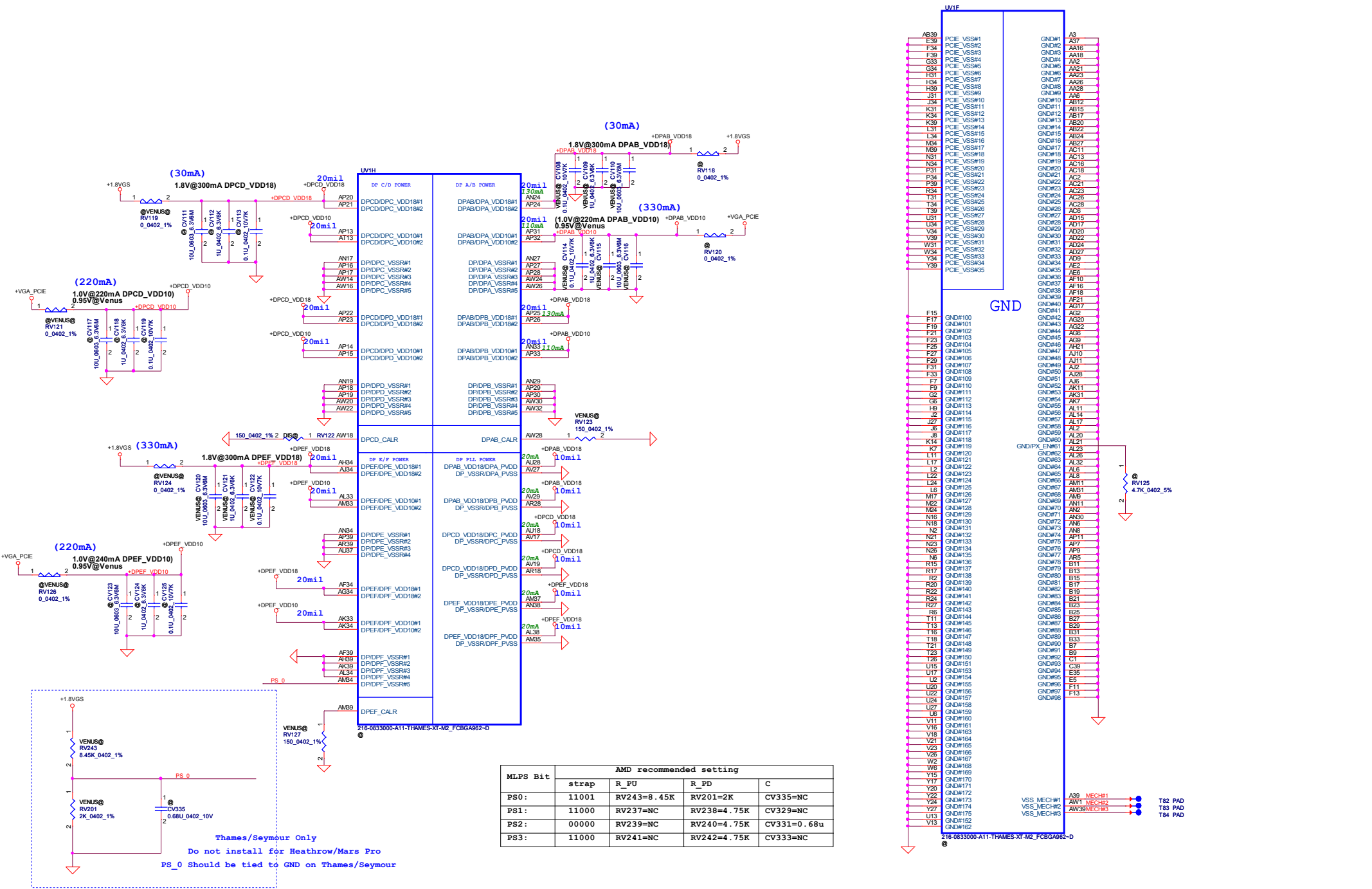


SHORT DEFAULT

+3VS TO +3VGS

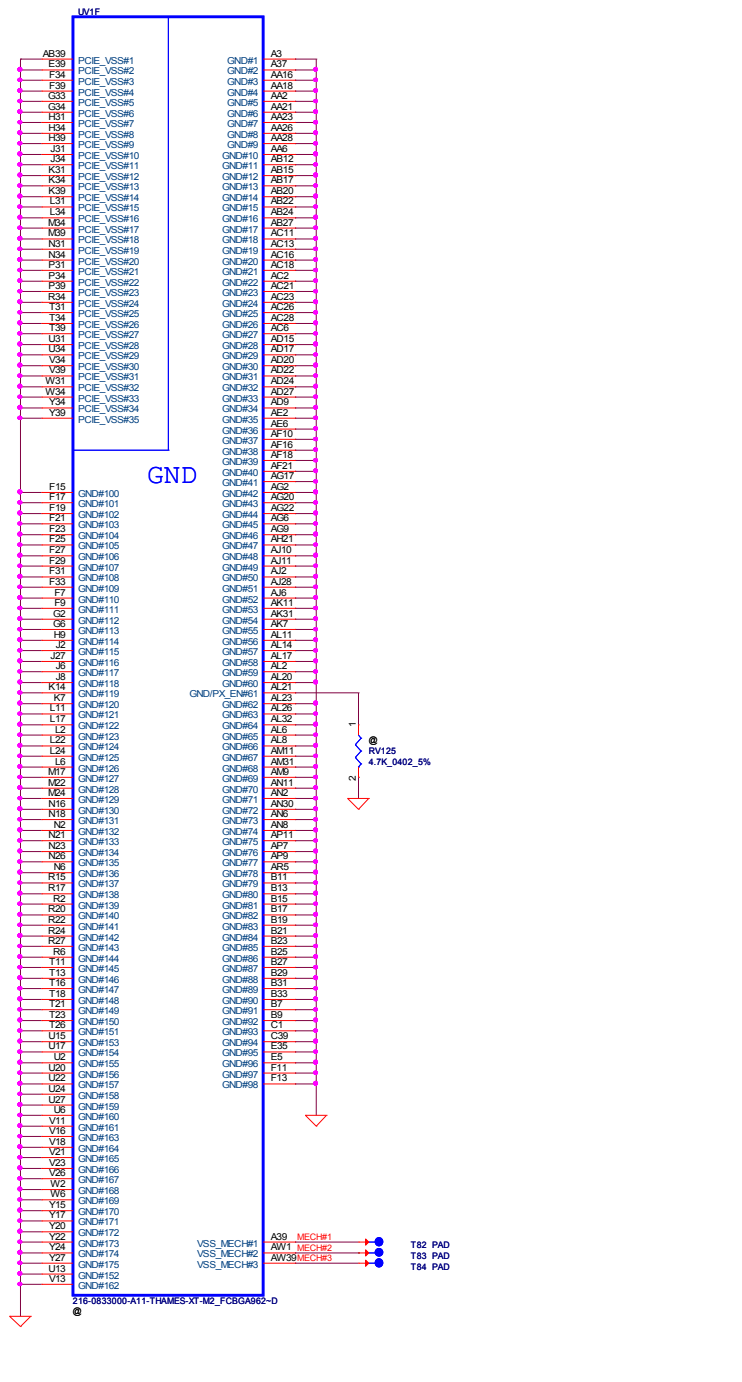


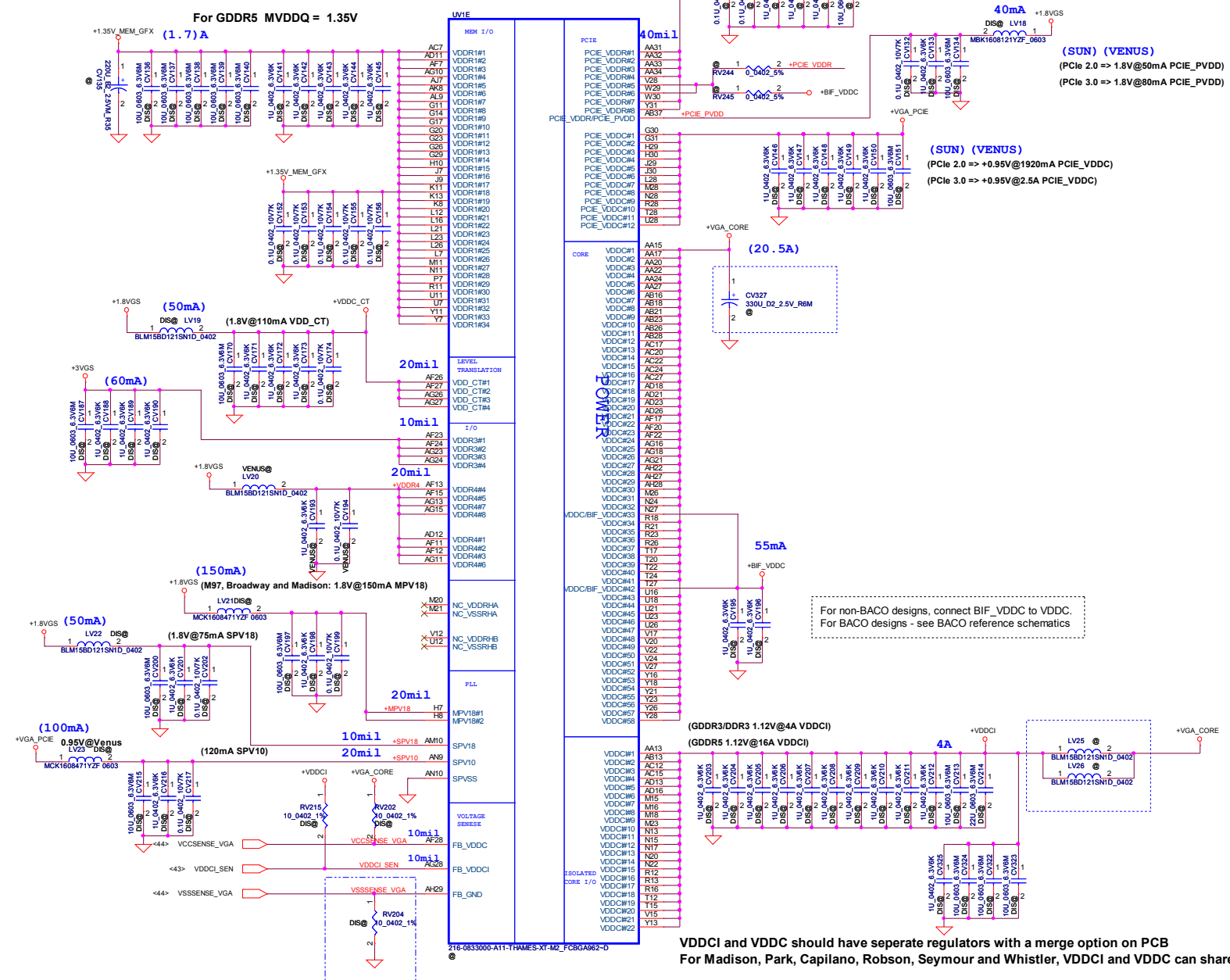
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MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

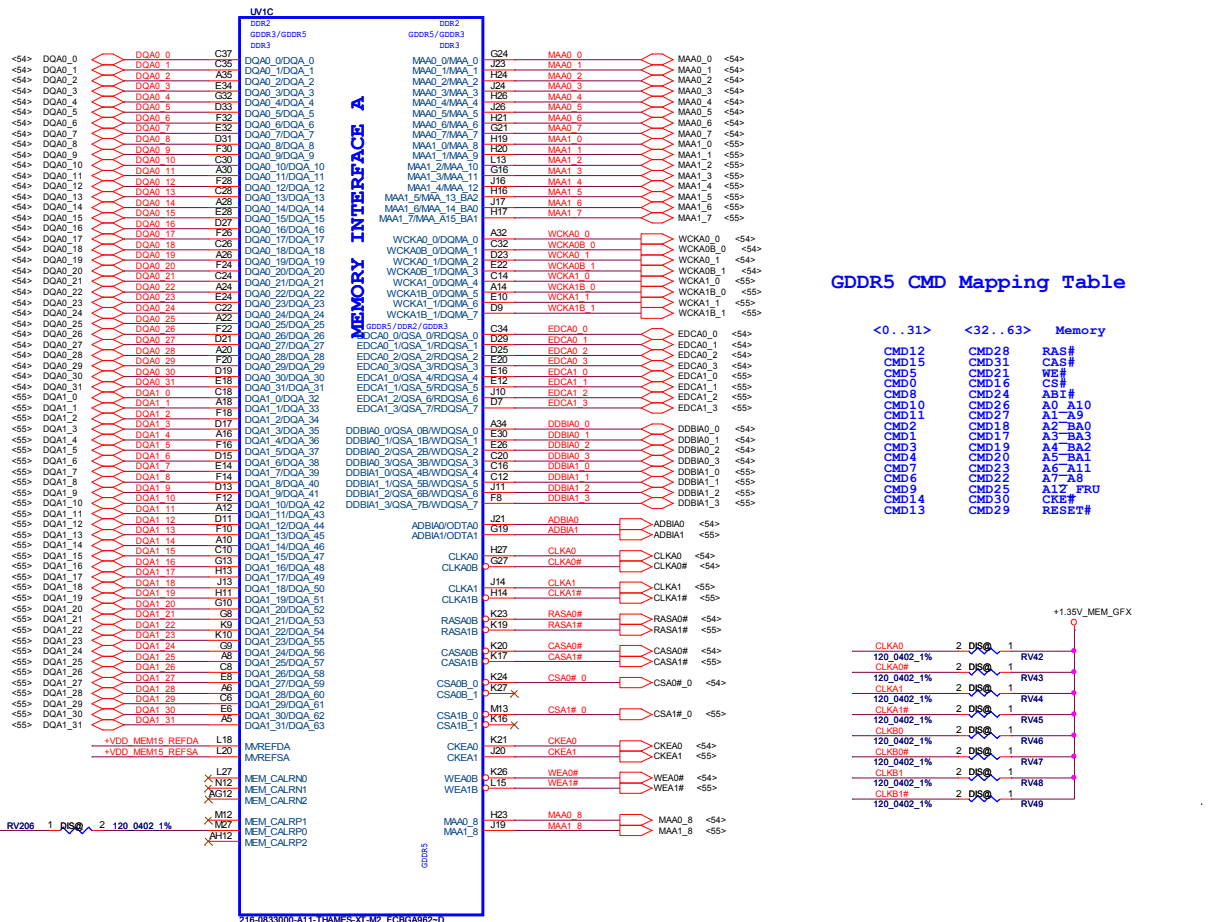
Thames/Seymour Only
Do not install for Heathrow/Mars Pro
PS_0 Should be tied to GND on Thames/Seymour





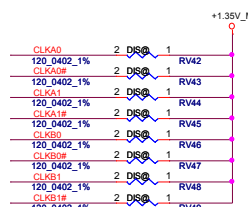
VDDCI and VDDC should have separate regulators with a merge option on PCB
 For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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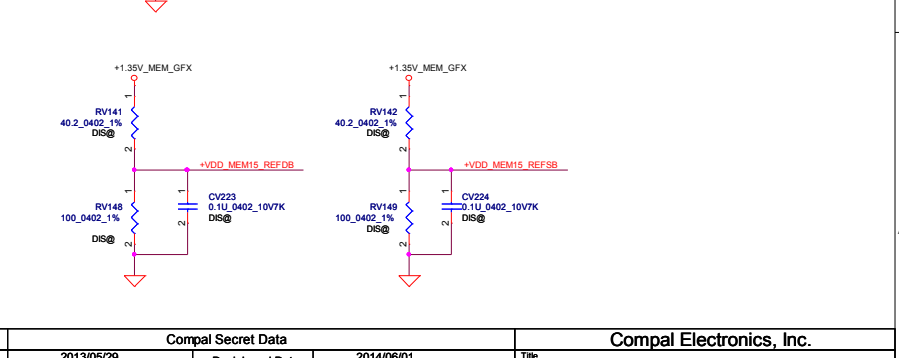
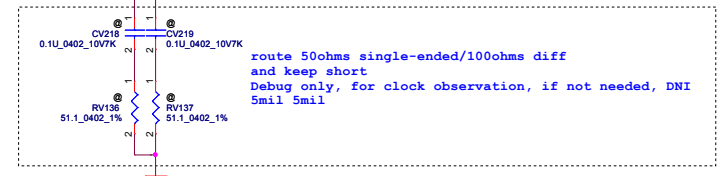
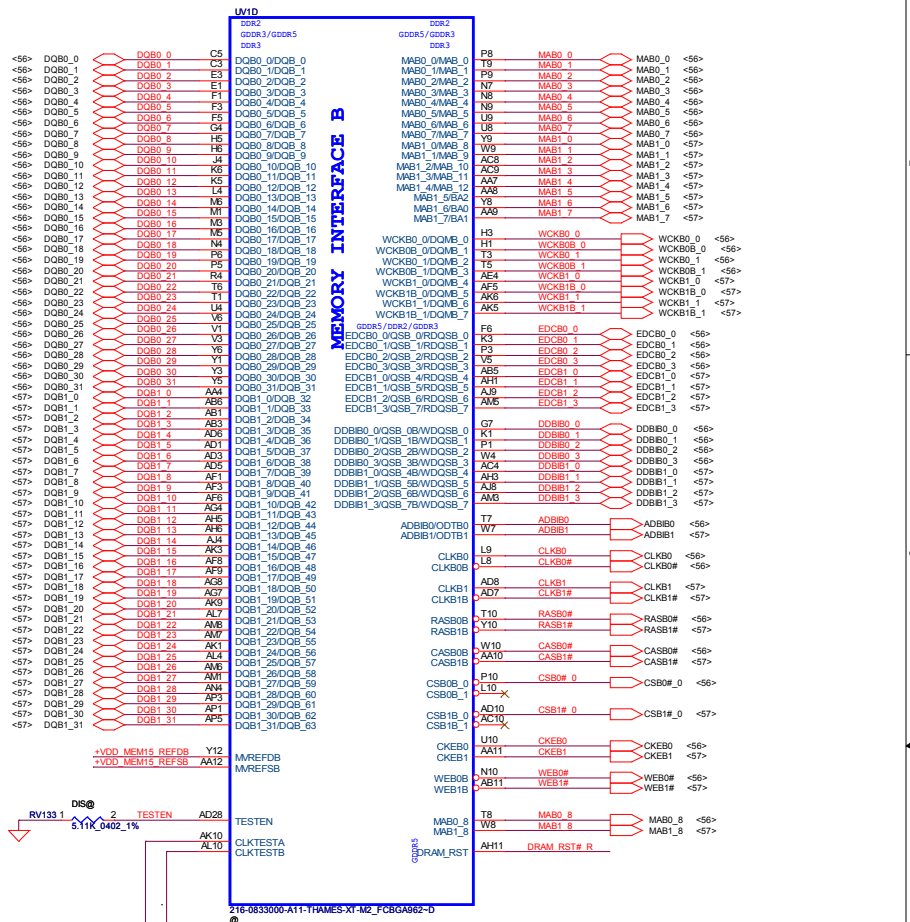
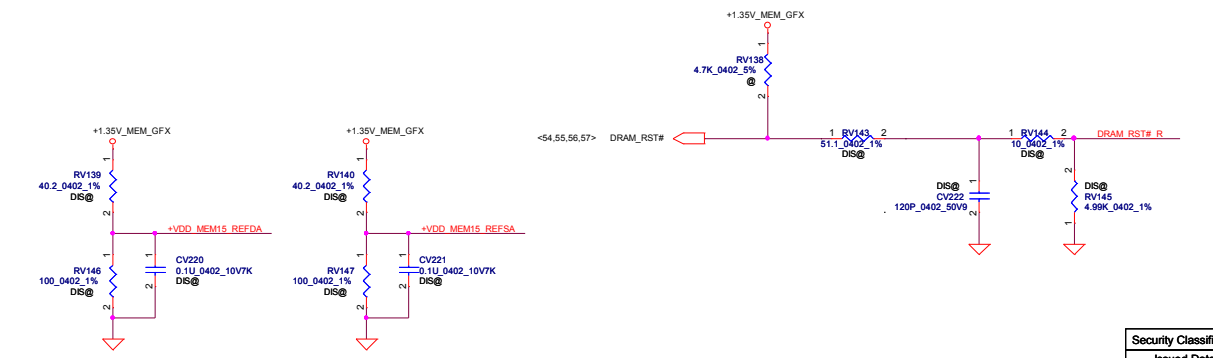


GDDR5 CMD Mapping Table

<. .31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	AB1#
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD1	CMD17	A3 BA3
CMD2	CMD18	A4 BA2
CMD4	CMD20	A5 BA1
CMD7	CMD23	A6 A11
CMD9	CMD25	A7 A8
CMD14	CMD30	CKEY
CMD13	CMD29	RESET#

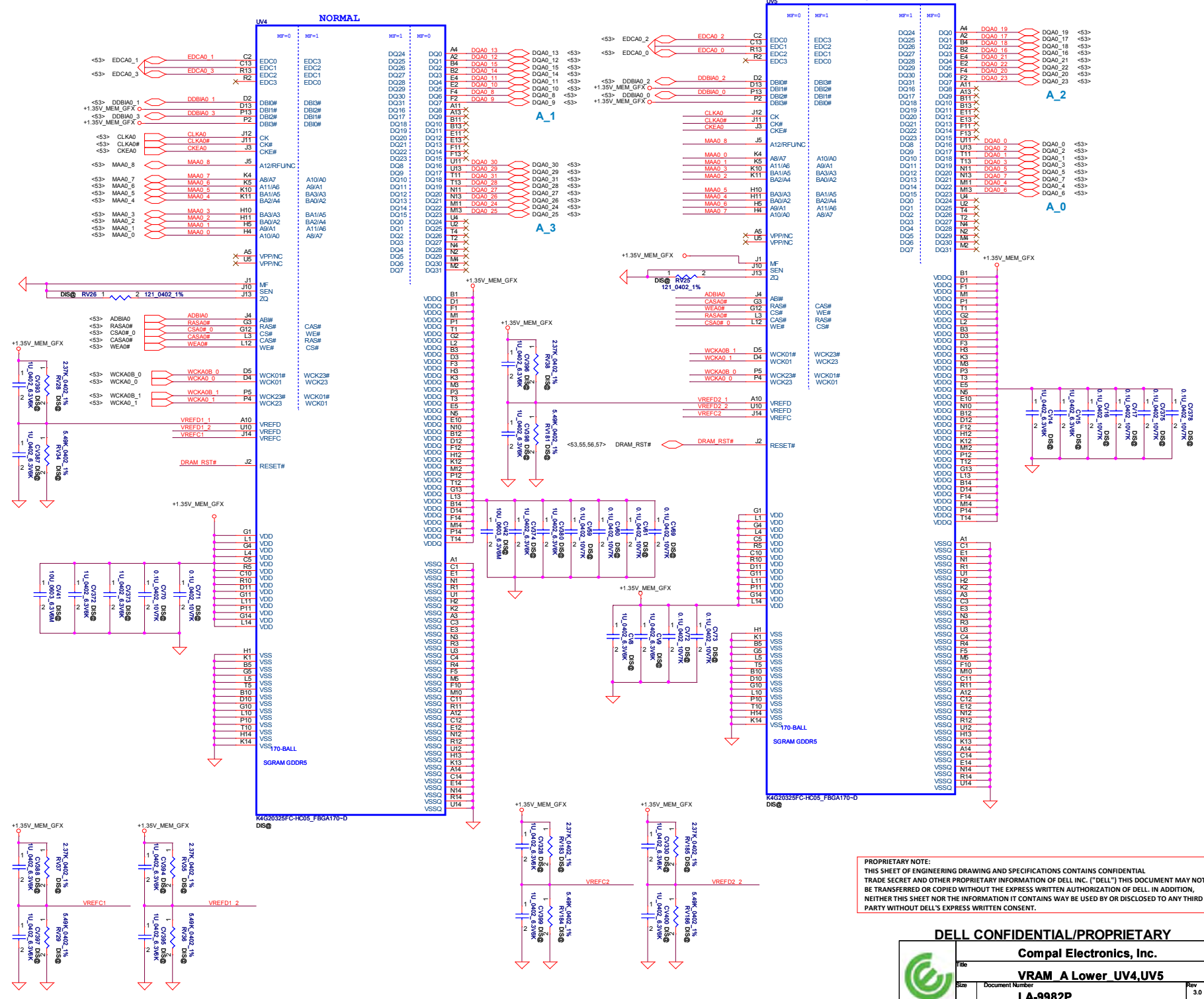


This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2



Memory Partition A - Lower 16 bits

64X32 GDDR5

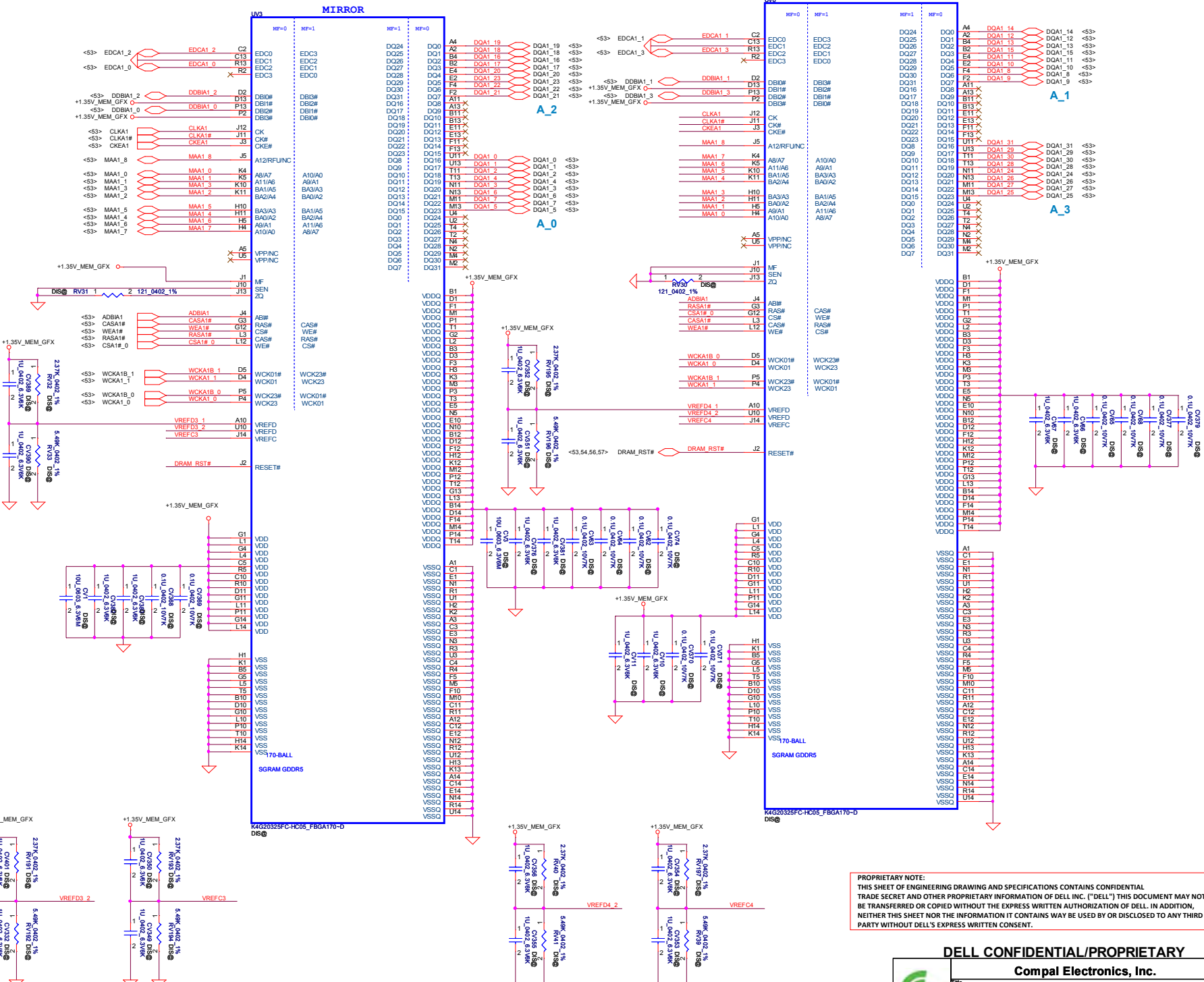


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Memory Partition A - Upper 16 bits

MIRROR

NORMAL



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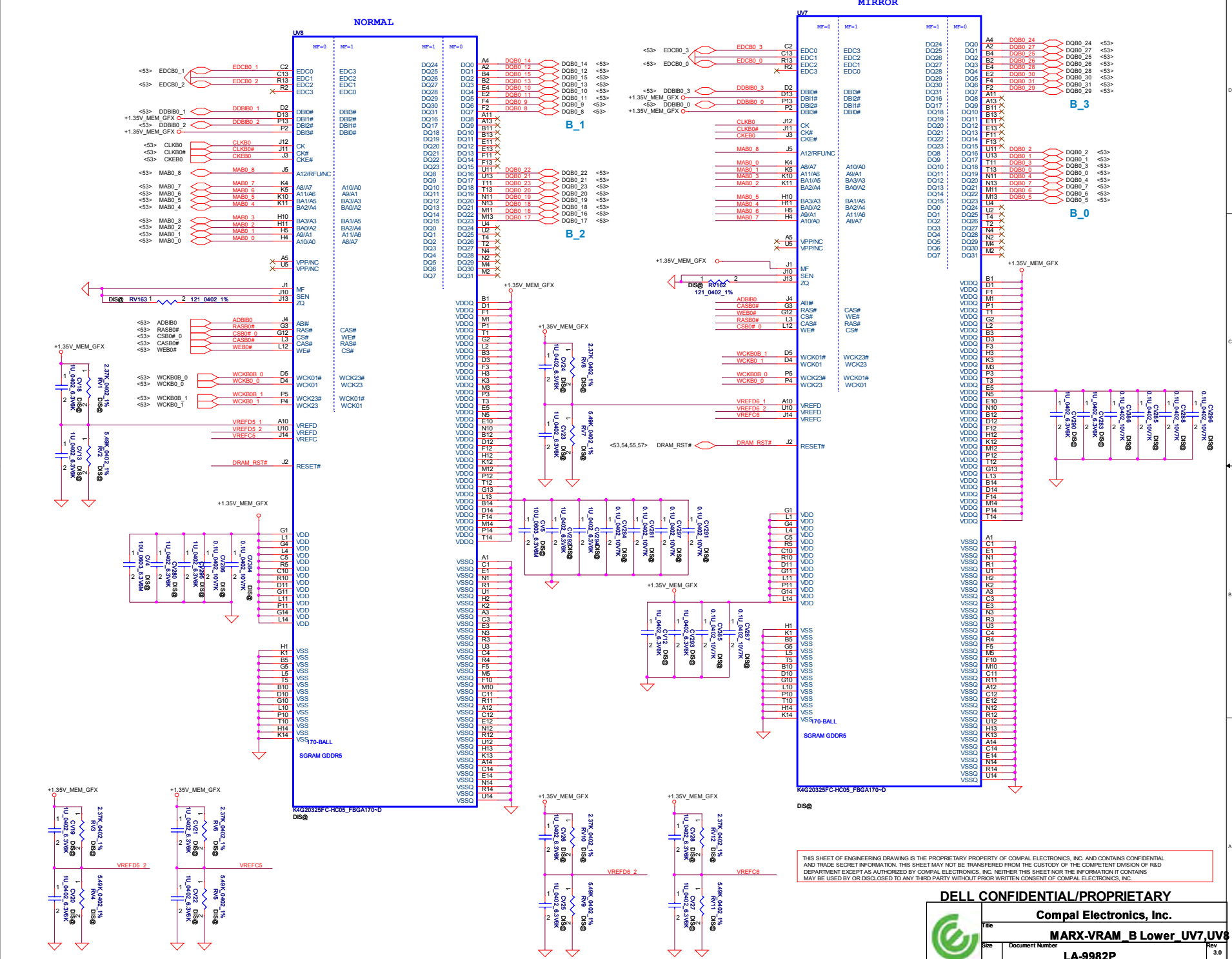


File: MARX-VRAM_A Upper UV3,UV6

Size: Document Number LA-9982P Rev: 3.0

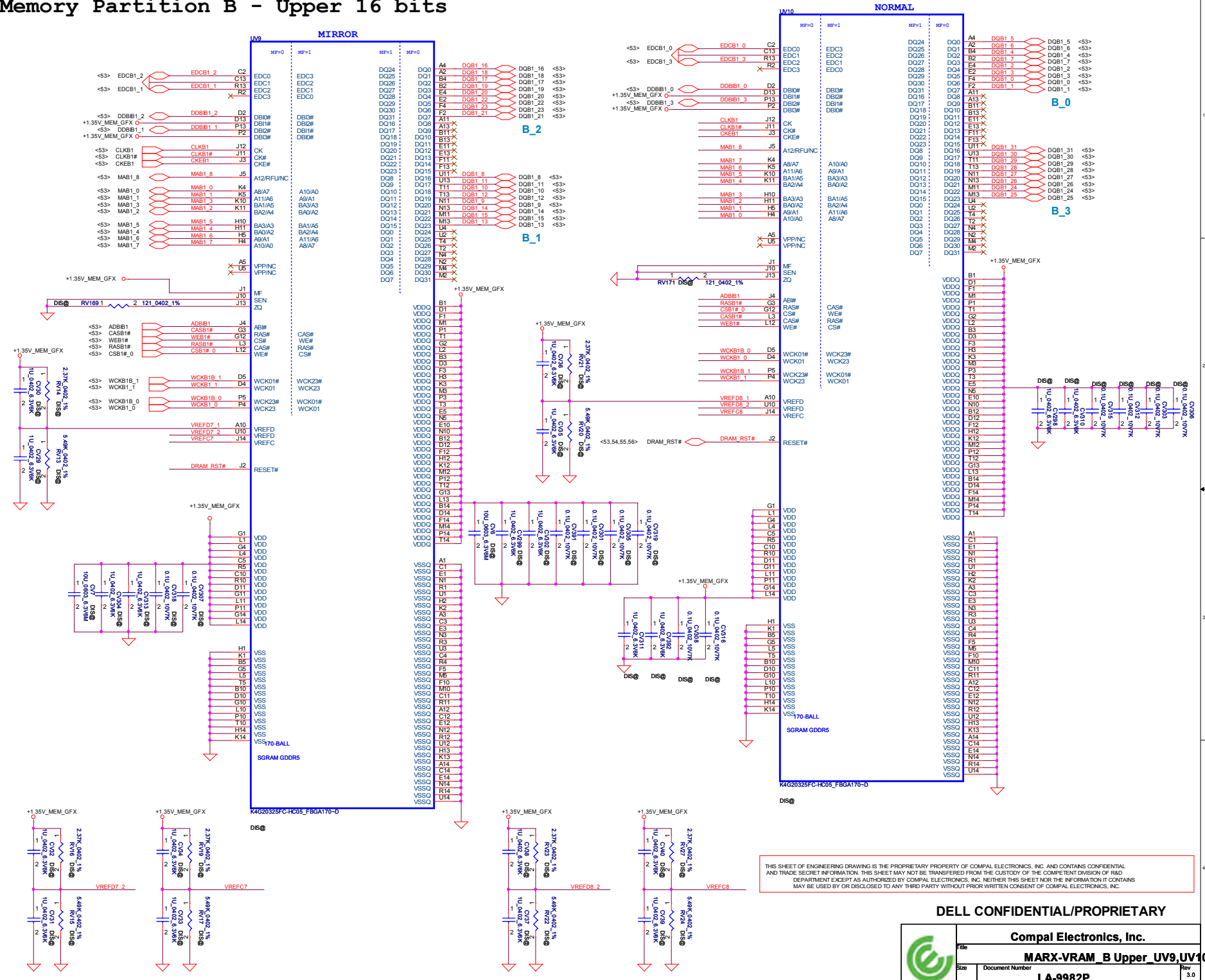
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Memory Partition B - Lower 16 bits



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Memory Partition B - Upper 16 bits



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