

SE000008600

Compal Confidential

Tanglha Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

2007-08-16

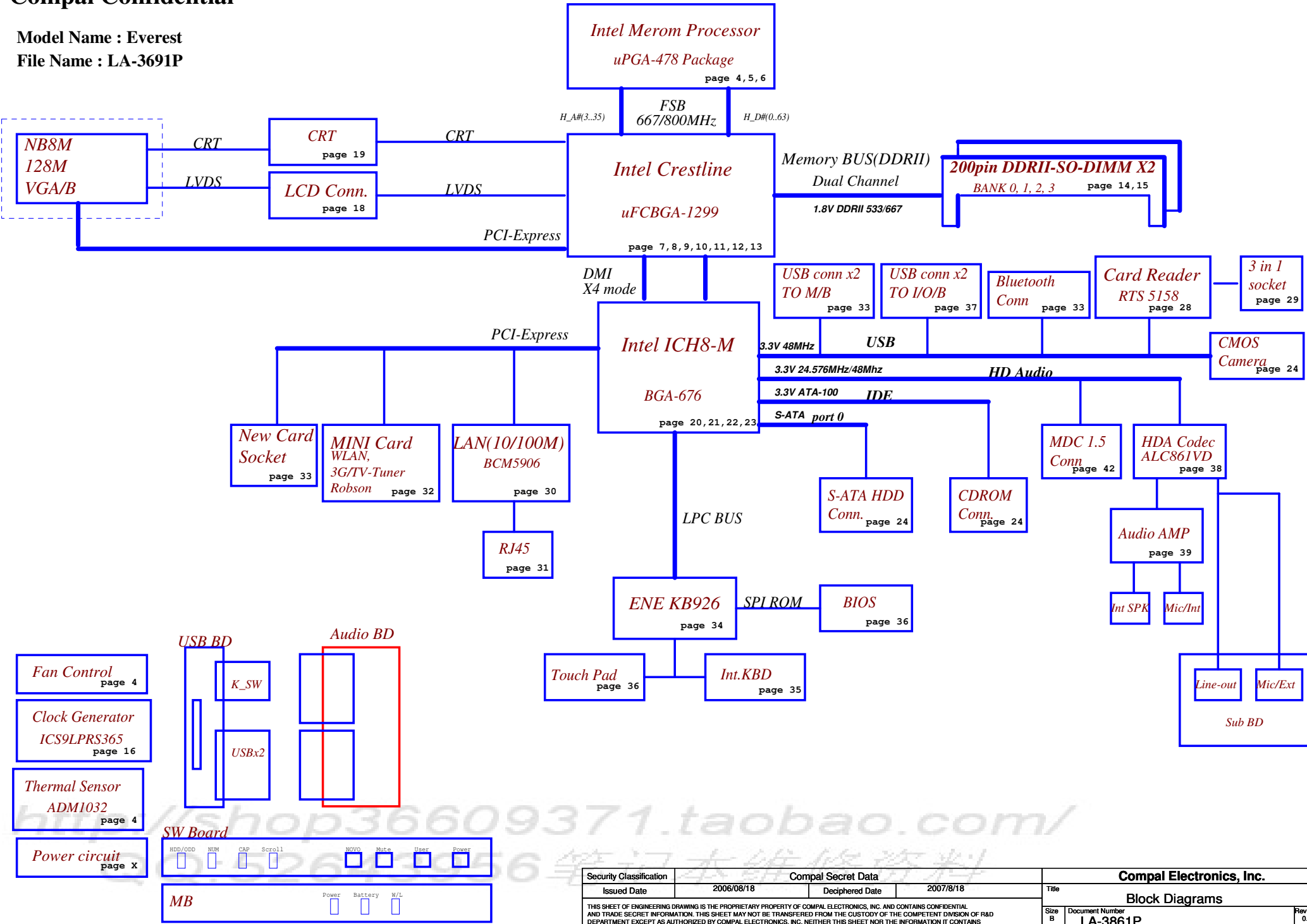
REV: 1.0

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Model Name : Everest
File Name : LA-3691P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0 (R744)	0 (R745)	A-TEST
0 (R744)	1 (R742)	B-TEST
1 (R741)	0 (R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

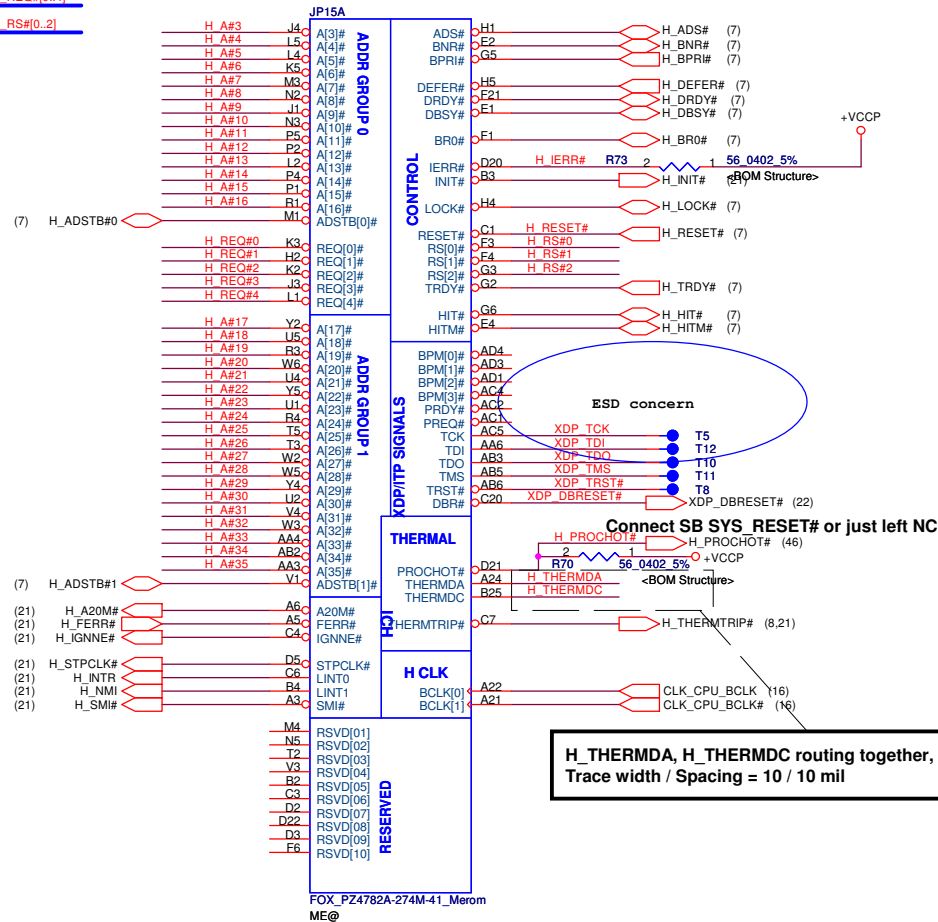
Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

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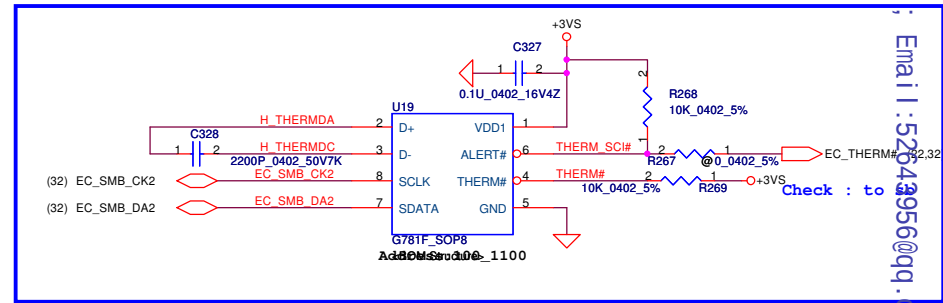
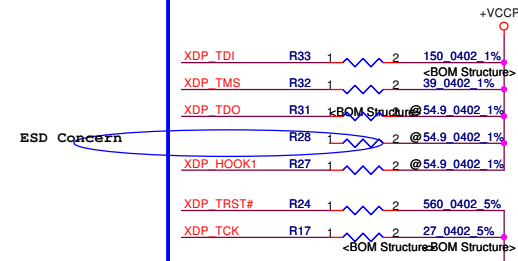
- (7) H_A# [3..35]  H_A# [3..35]
- (7) H_REQ# [0..4]  H_REQ# [0..4]
- (7) H_RS# [0..2]  H_RS# [0..2]



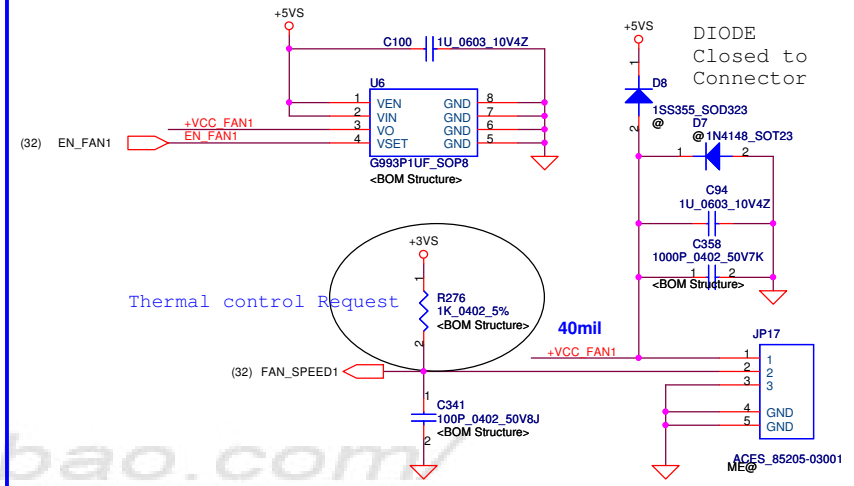
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

Place close to CPU within 500mil

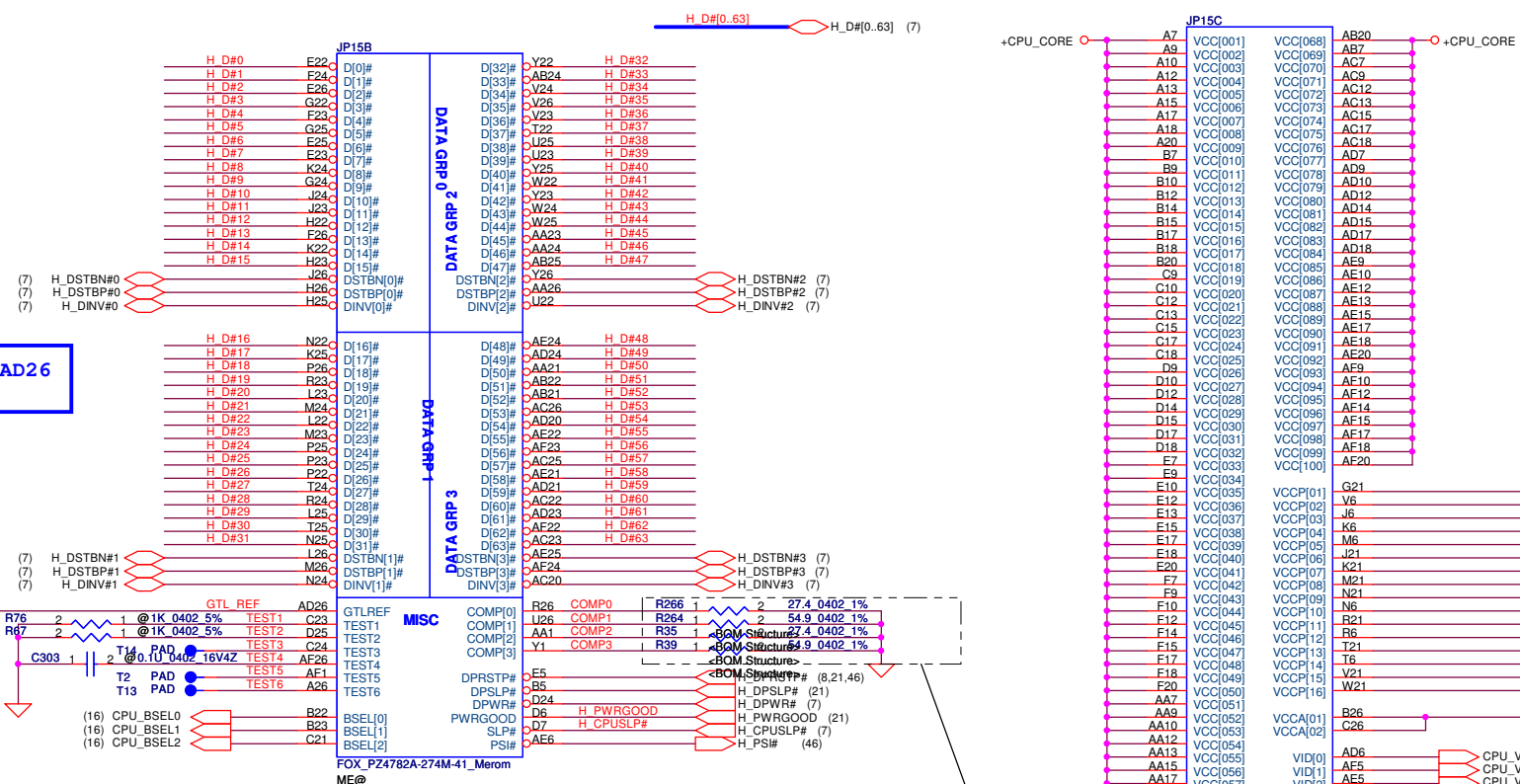
XDP Reserve



FAN1 Conn



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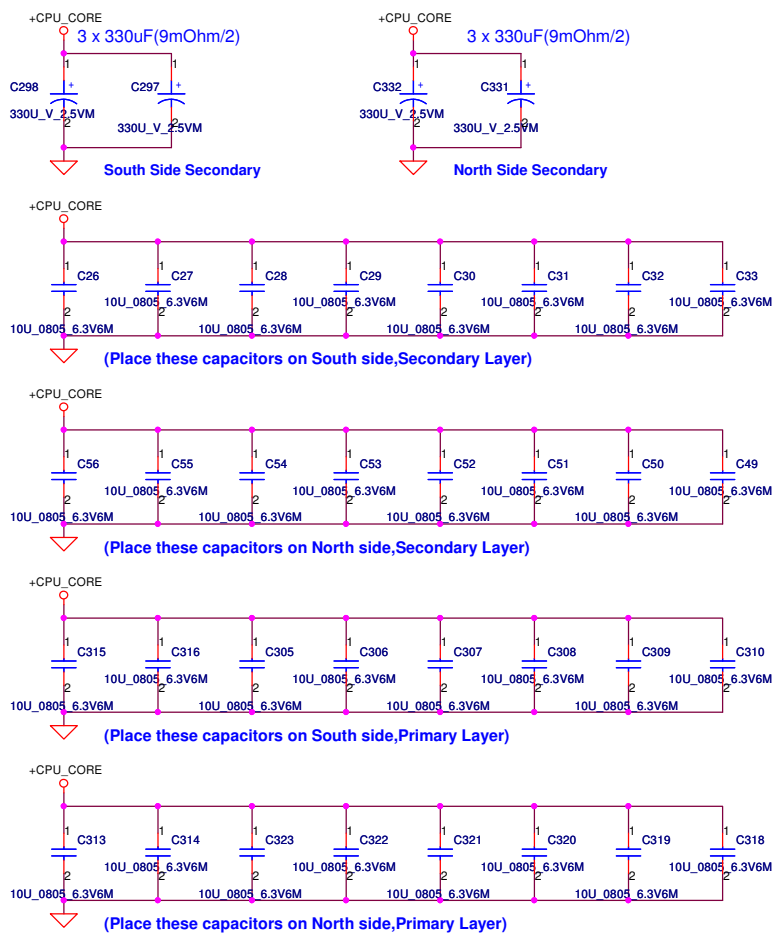


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

JP15D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	A5
M22	VSS[075]	A8
M25	VSS[076]	AF6
N1	VSS[077]	AF8
N4	VSS[078]	AF11
N23	VSS[079]	AF13
N26	VSS[080]	AF16
P3	VSS[081]	AF19
		AF21
		A25
		AF25

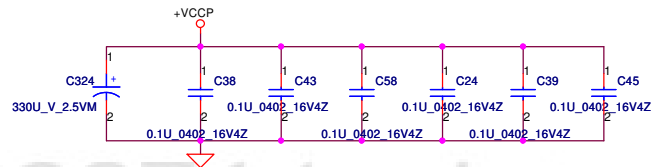
FOX_PZ4782A-274M-41_Merom

ME@



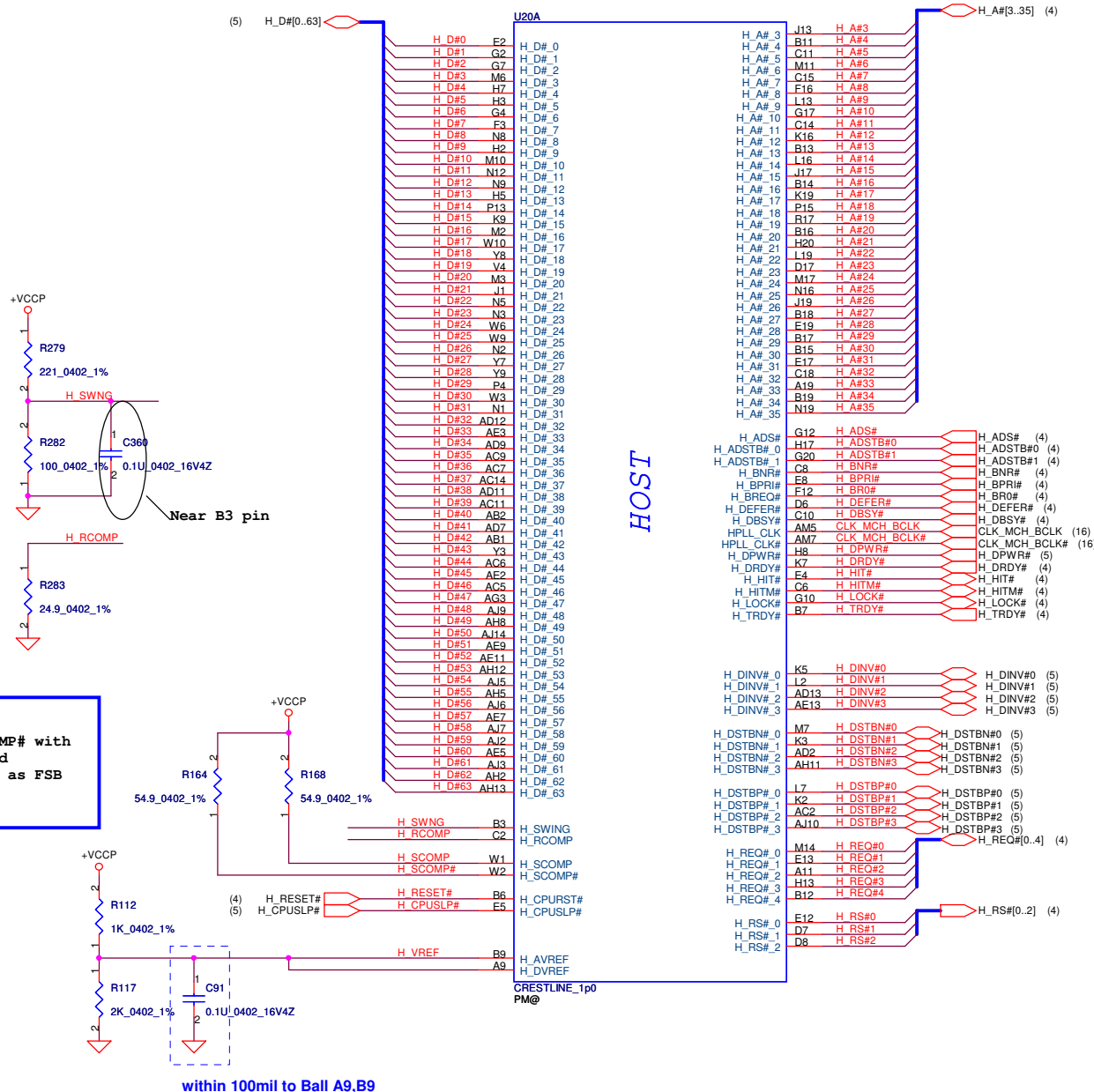
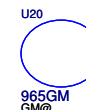
9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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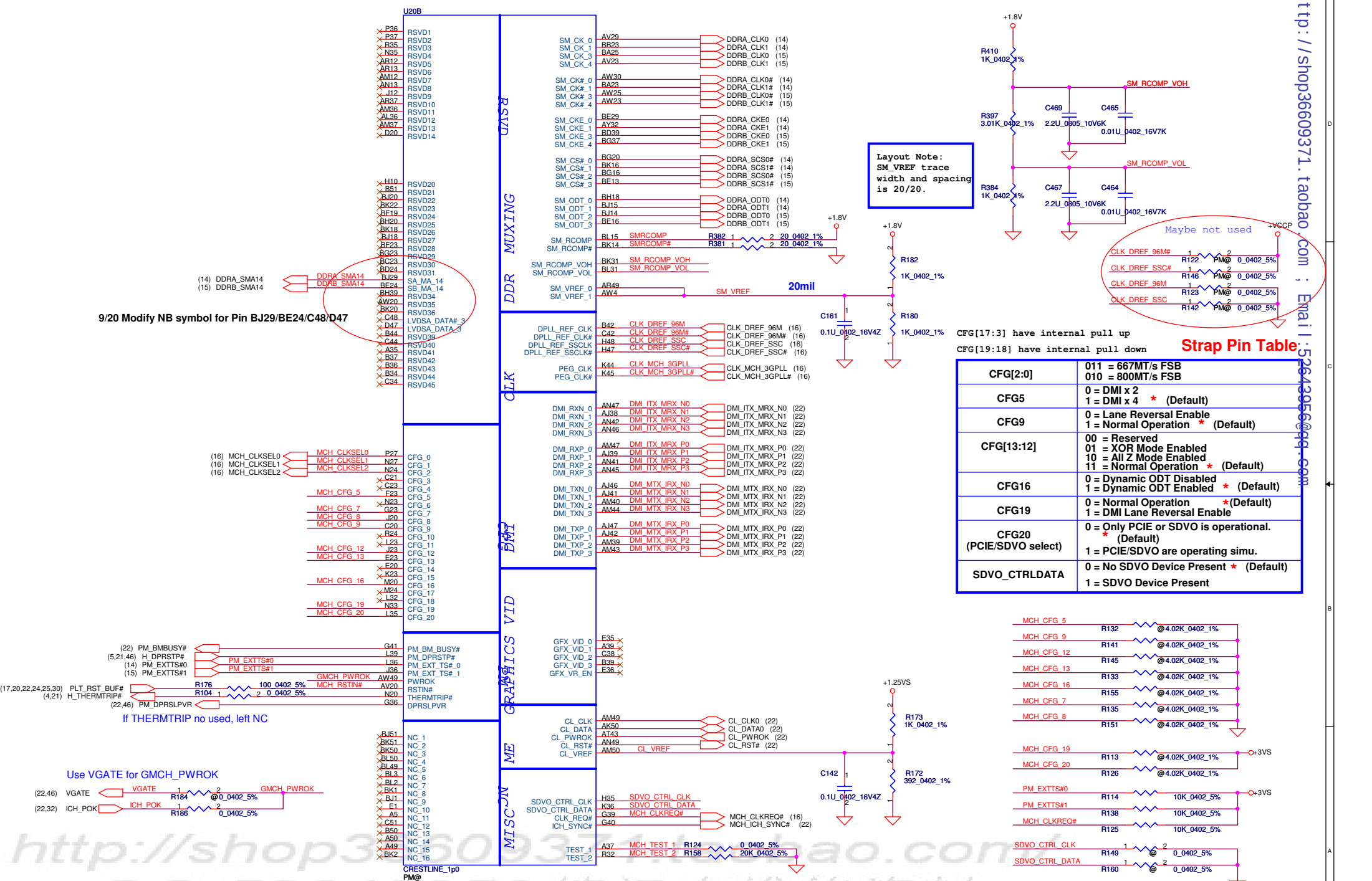
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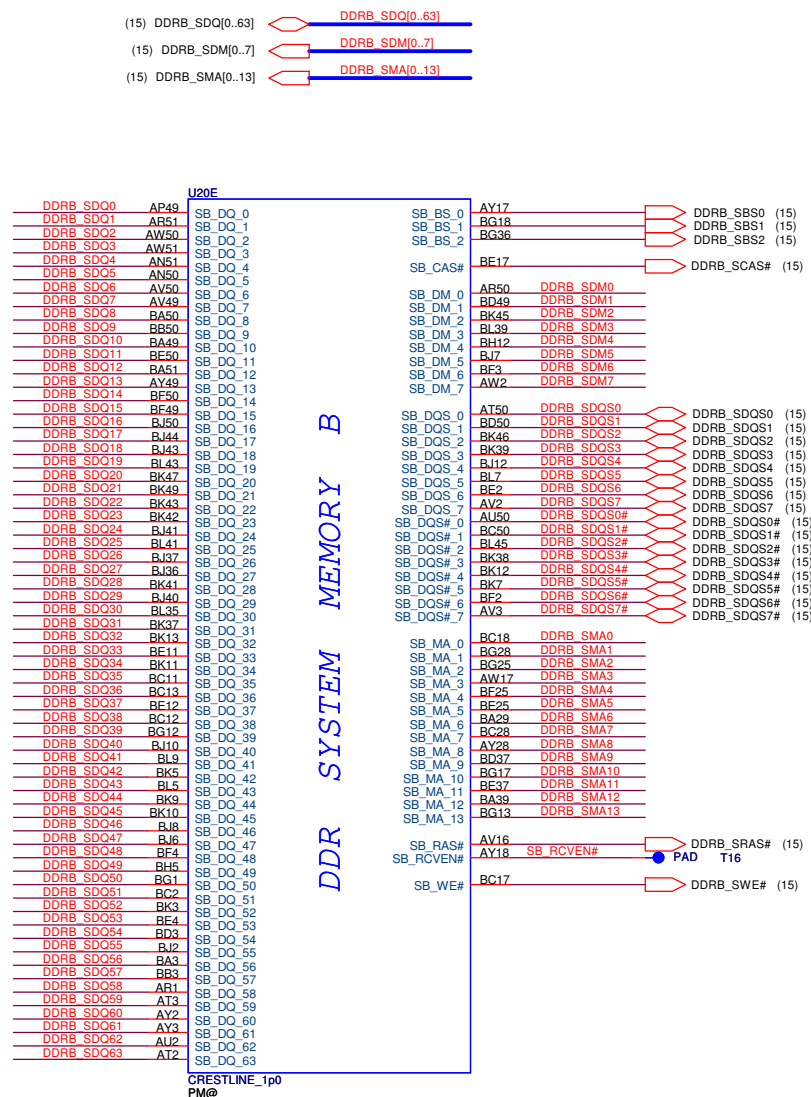


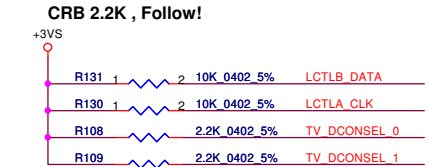
layout note:
Route H_SCOMP and H_SCOMP# with
trace width, spacing and
impedance (55 ohm) same as FSB
data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

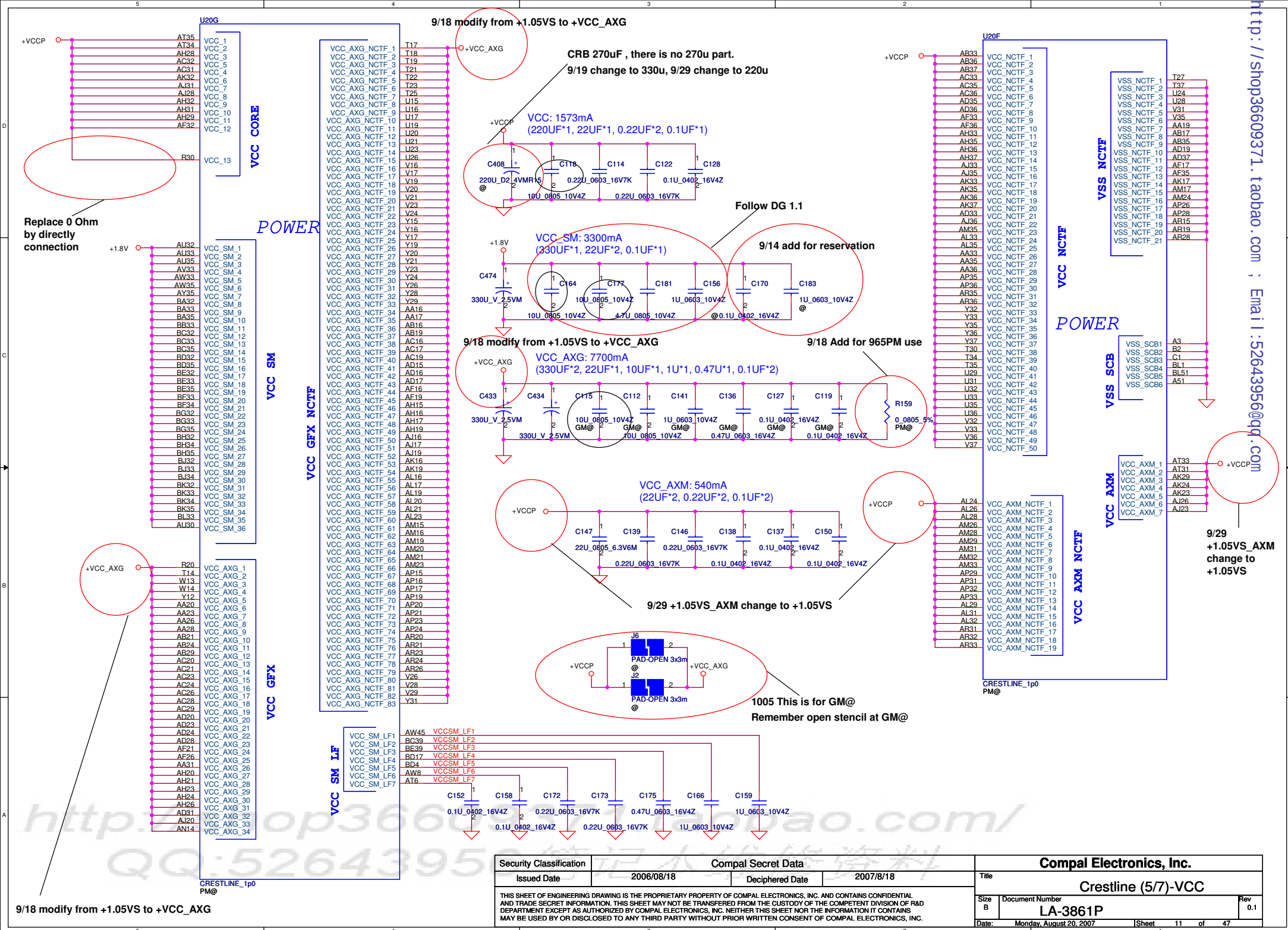
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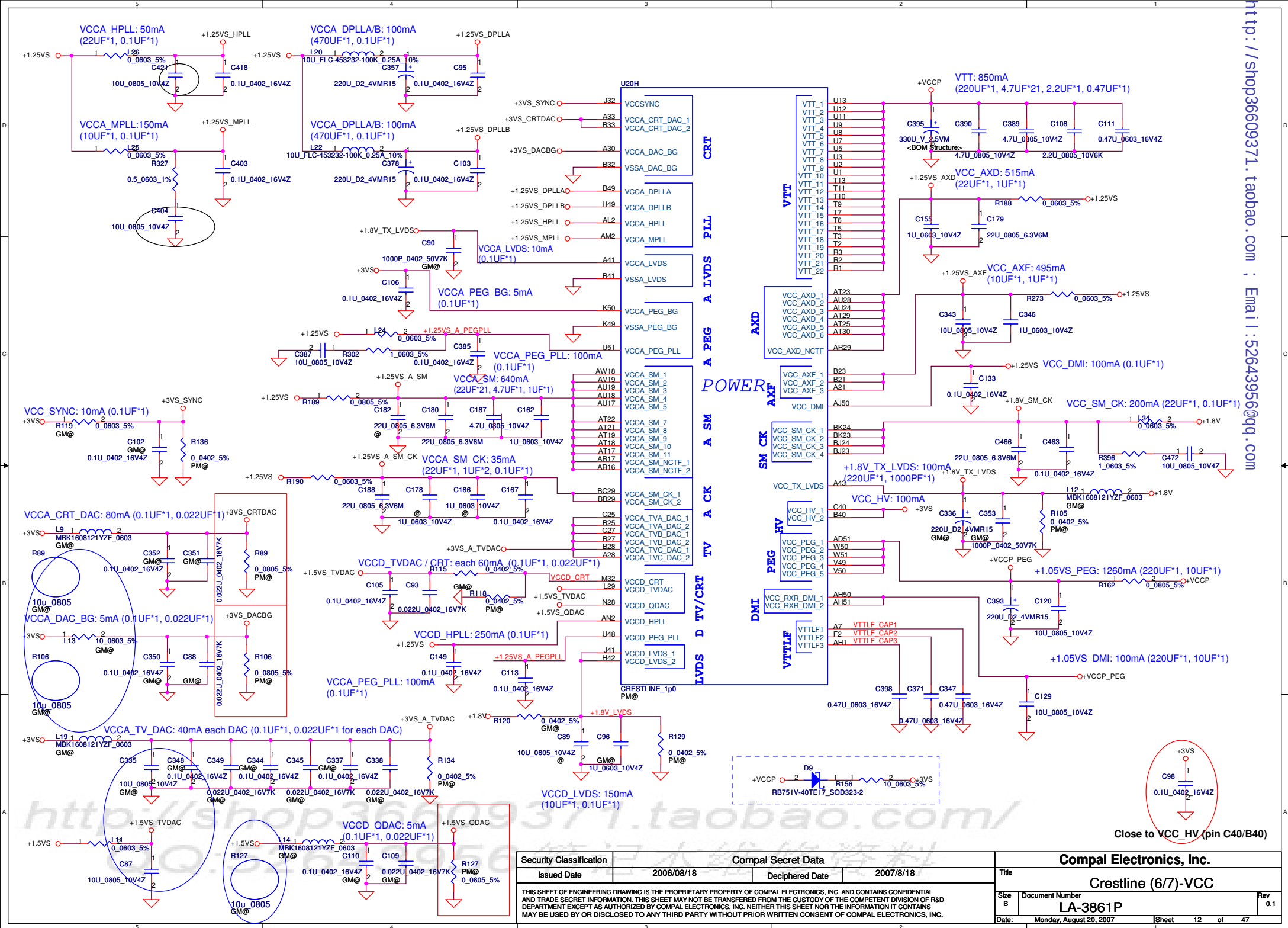






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U201

A13	VSS_1	VSS_100	AW24
A15	VSS_2	VSS_101	AW29
A17	VSS_3	VSS_102	AW32
A24	VSS_4	VSS_103	AW5
AA21	VSS_5	VSS_104	AW7
AA24	VSS_6	VSS_105	AY10
AA29	VSS_7	VSS_106	AY24
AB20	VSS_8	VSS_107	AY37
AB23	VSS_9	VSS_108	AY42
AB26	VSS_10	VSS_109	AY43
AB28	VSS_11	VSS_110	AY45
AB31	VSS_12	VSS_111	AY47
AC10	VSS_13	VSS_112	AY50
AC3	VSS_14	VSS_113	B10
AC39	VSS_15	VSS_114	B20
AC43	VSS_16	VSS_115	B24
AC47	VSS_17	VSS_116	B29
AD1	VSS_18	VSS_117	B30
AD21	VSS_19	VSS_118	B35
AD26	VSS_20	VSS_119	B38
AD29	VSS_21	VSS_120	B43
AD3	VSS_22	VSS_121	B46
AD41	VSS_23	VSS_122	B5
AD45	VSS_24	VSS_123	B8
AD49	VSS_25	VSS_124	B17
AD5	VSS_26	VSS_125	BA18
AD50	VSS_27	VSS_126	BA2
AD8	VSS_28	VSS_127	BA24
AE10	VSS_29	VSS_128	BB12
AE14	VSS_30	VSS_129	BB25
AE6	VSS_31	VSS_130	BB40
AF20	VSS_32	VSS_131	BB44
AF23	VSS_33	VSS_132	BB49
AF24	VSS_34	VSS_133	BB8
AF31	VSS_35	VSS_134	BC16
AG2	VSS_36	VSS_135	BC24
AG38	VSS_37	VSS_136	BC25
AG49	VSS_38	VSS_137	BC36
AG47	VSS_39	VSS_138	BC40
AG50	VSS_40	VSS_139	BC51
AH3	VSS_41	VSS_140	BD13
AH40	VSS_42	VSS_141	BD2
AH41	VSS_43	VSS_142	BD28
AH7	VSS_44	VSS_143	BD45
AH9	VSS_45	VSS_144	BD48
AJ11	VSS_46	VSS_145	BD5
AJ13	VSS_47	VSS_146	BE1
AJ21	VSS_48	VSS_147	BE19
AJ24	VSS_49	VSS_148	BE23
AJ29	VSS_50	VSS_149	BE30
AJ32	VSS_51	VSS_150	BE42
AJ43	VSS_52	VSS_151	BE51
AJ45	VSS_53	VSS_152	BE8
AJ49	VSS_54	VSS_153	BF12
AK20	VSS_55	VSS_154	BF16
AK21	VSS_56	VSS_155	BF36
AK26	VSS_57	VSS_156	BG19
AK28	VSS_58	VSS_157	BG2
AK31	VSS_59	VSS_158	BG24
AK51	VSS_60	VSS_159	BG29
AL1	VSS_61	VSS_160	BG39
AM11	VSS_62	VSS_161	BG48
AM13	VSS_63	VSS_162	BG5
AM3	VSS_64	VSS_163	BG51
AM4	VSS_65	VSS_164	BH17
AM41	VSS_66	VSS_165	BH30
AM45	VSS_67	VSS_166	BH44
AN1	VSS_68	VSS_167	BH46
AN38	VSS_69	VSS_168	BH8
AN39	VSS_70	VSS_169	BH11
AN43	VSS_71	VSS_170	BH13
AN5	VSS_72	VSS_171	BH38
AN7	VSS_73	VSS_172	BH4
AP4	VSS_74	VSS_173	BH42
AP48	VSS_75	VSS_174	BH46
AP50	VSS_76	VSS_175	BK15
AR11	VSS_77	VSS_176	BK17
AR2	VSS_78	VSS_177	BK25
AR39	VSS_79	VSS_178	BK29
AR44	VSS_80	VSS_179	BK36
AR47	VSS_81	VSS_180	BK40
AR7	VSS_82	VSS_181	BK44
AT10	VSS_83	VSS_182	BK6
AT14	VSS_84	VSS_183	BK6
AT41	VSS_85	VSS_184	BL11
AT49	VSS_86	VSS_185	BL13
AU1	VSS_87	VSS_186	BL19
AU23	VSS_88	VSS_187	BL22
AU29	VSS_89	VSS_188	BL37
AU3	VSS_90	VSS_189	BL47
AU36	VSS_91	VSS_190	C12
AU49	VSS_92	VSS_191	C16
AU51	VSS_93	VSS_192	C19
AV39	VSS_94	VSS_193	C28
AV48	VSS_95	VSS_194	C29
AW1	VSS_96	VSS_195	C33
AW12	VSS_97	VSS_196	C36
AW16	VSS_98	VSS_197	C41
	VSS_99	VSS_198	

CRESTLINE_1p0
PM@

U20J

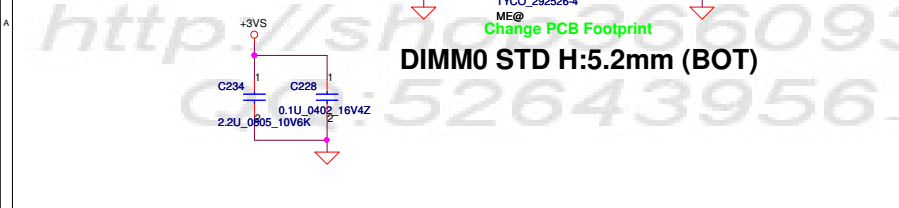
C46	VSS_199	VSS_287	W11
C50	VSS_200	VSS_288	W39
C7	VSS_201	VSS_289	W43
D13	VSS_202	VSS_290	W47
D24	VSS_203	VSS_291	W5
D3	VSS_204	VSS_292	W7
D32	VSS_205	VSS_293	Y13
D39	VSS_206	VSS_294	Y2
D45	VSS_207	VSS_295	Y41
D49	VSS_208	VSS_296	Y45
E10	VSS_209	VSS_297	Y49
E16	VSS_210	VSS_298	Y5
E24	VSS_211	VSS_299	Y50
E28	VSS_212	VSS_300	Y11
E32	VSS_213	VSS_301	P29
E47	VSS_214	VSS_302	T29
F19	VSS_215	VSS_303	T31
F36	VSS_216	VSS_304	T33
F4	VSS_217	VSS_305	R28
F40	VSS_218		
F50	VSS_219		
G1	VSS_220		
G13	VSS_221	VSS_306	AA32
G16	VSS_222	VSS_307	AB32
G19	VSS_223	VSS_308	AD32
G24	VSS_224	VSS_309	AF28
G28	VSS_225	VSS_310	AF29
G29	VSS_226	VSS_311	AT27
G33	VSS_227	VSS_312	AV25
G42	VSS_228	VSS_313	H50
G45	VSS_229		
G48	VSS_230		
G8	VSS_231		
H24	VSS_232		
H28	VSS_233		
H4	VSS_234		
H45	VSS_235		
J11	VSS_236		
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J24	VSS_239		
J28	VSS_240		
J33	VSS_241		
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N44	VSS_270		
N49	VSS_271		
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P19	VSS_273		
P2	VSS_274		
P23	VSS_275		
P3	VSS_276		
P50	VSS_277		
R49	VSS_278		
T39	VSS_279		
T43	VSS_280		
T47	VSS_281		
U41	VSS_282		
U45	VSS_283		
U50	VSS_284		
V2	VSS_285		
V3	VSS_286		

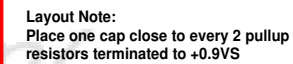
CRESTLINE_1p0
PM@

VSS

VSS

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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
								Crestline (7/7)-GND			
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								LA-3861P		0.1	
						Date:		Monday, August 20, 2007		Sheet 13 of 47	



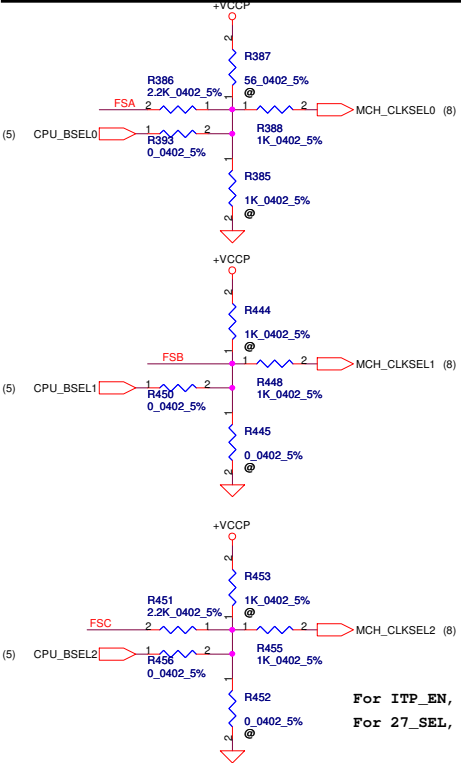


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	DDRII-SODIMM1
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				Document Number	
				LA-3861P	
Date	Monday, August 20, 2007		Sheet	15	of 47

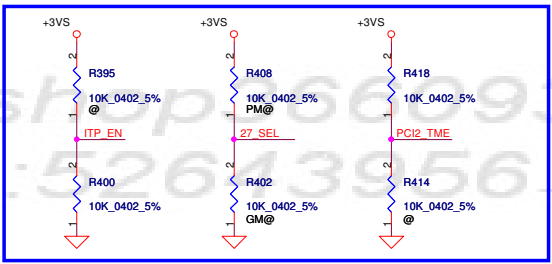
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

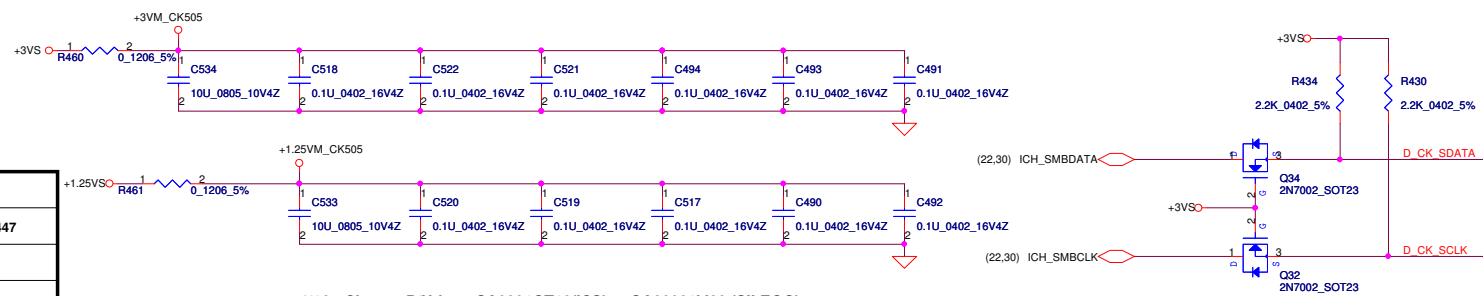
CPU Driven	Stuff						
★(Default)	No Stuff	R401	R408	R417	R430	R438	R447
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			



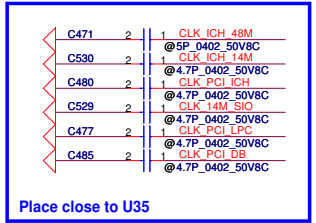
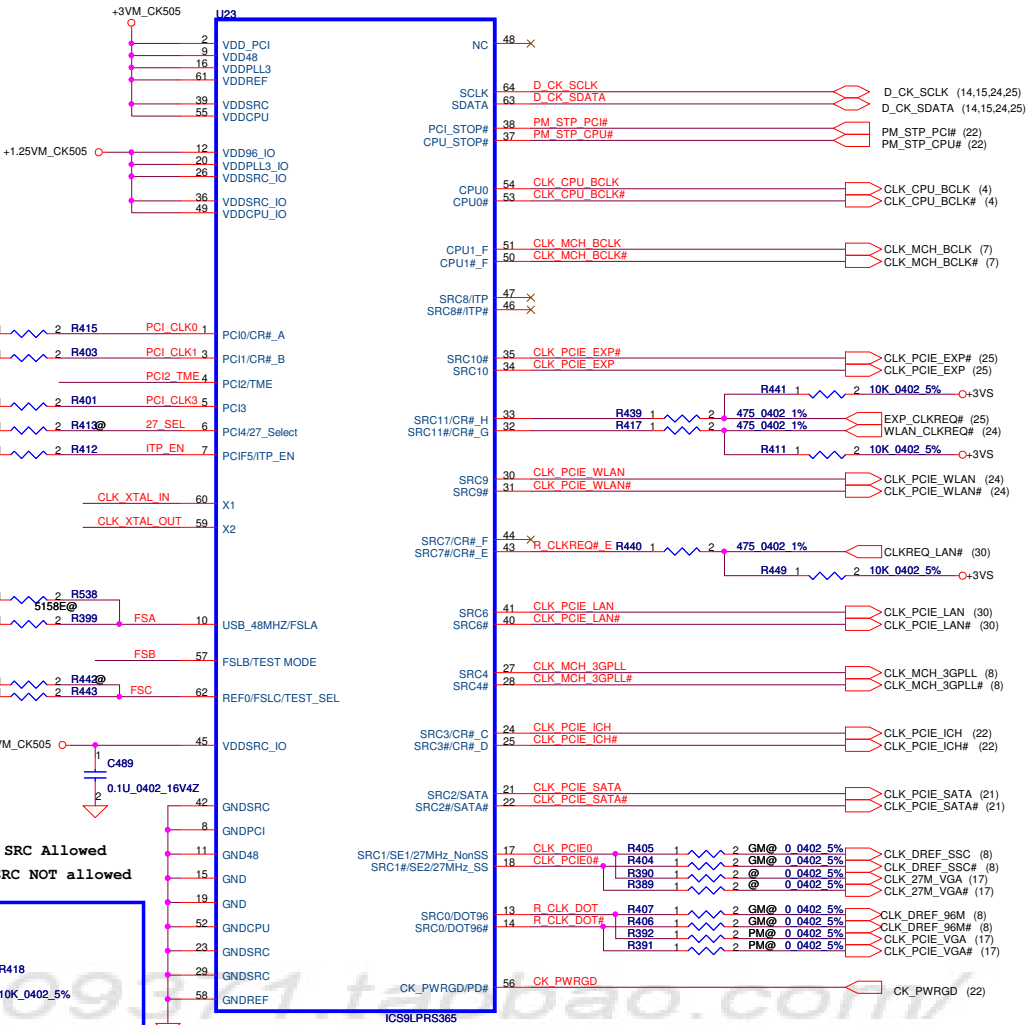
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
 For 27_SEL, 0 = Enable DOT96 & SRC1,
 1 = Enable SRC0 & 27MHz
 For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
 1 = Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil



4/16 : Change P/N from SA0001GT10(ICS) to SA00001IJ00 (SILEGO)

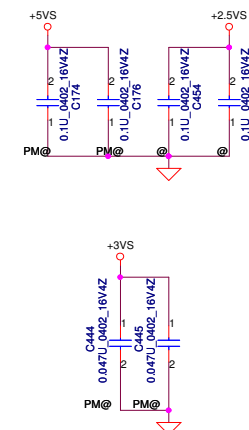
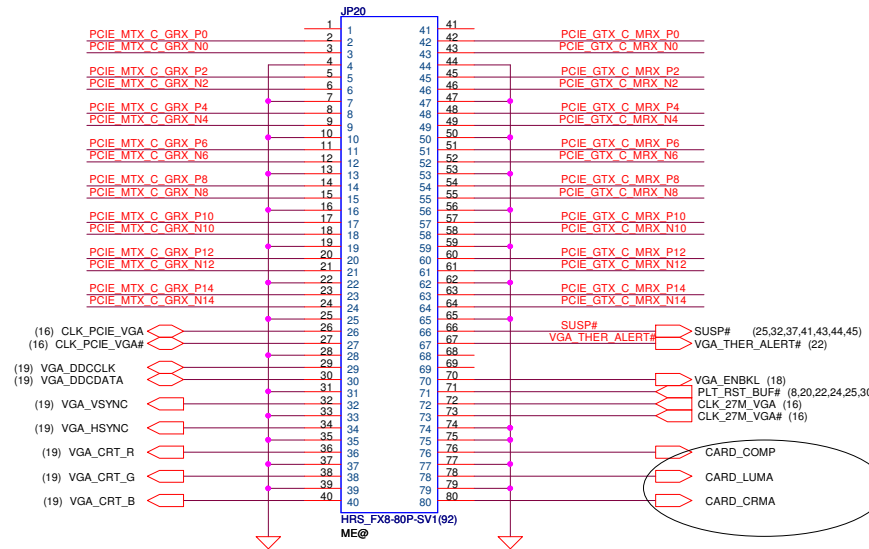
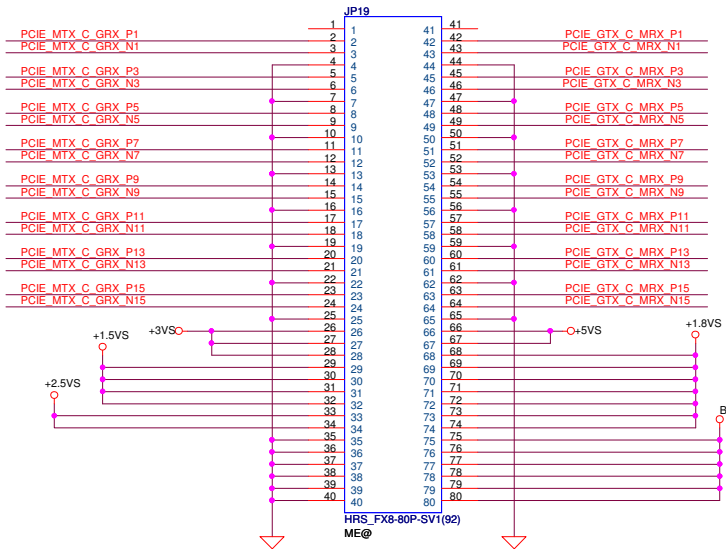


Place close to U35

Security Classification	Compal Secret Data	Title	
Issued Date	2006/08/04	Clock generator	
Deciphered Date	2006/10/06	Rev 0.1	
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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

- (10) PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
(10) PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
(10) PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
(10) PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

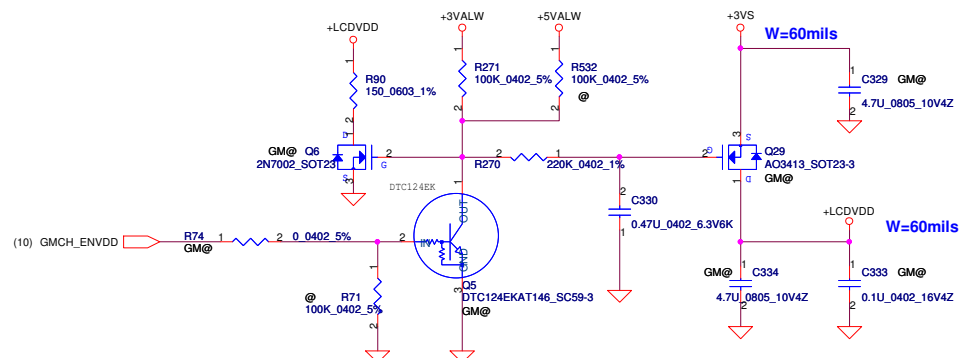


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QQ:52643956 笔记本维修资料

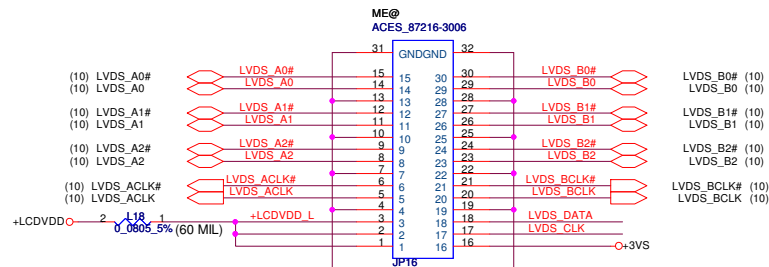
Compal Electronics, Inc.			
VGA/B connector			
Title	Document Number	Rev	0.1
Size	LA-3861P		
Custon			
Date	Monday, August 20, 2007	Sheet	17 of 47

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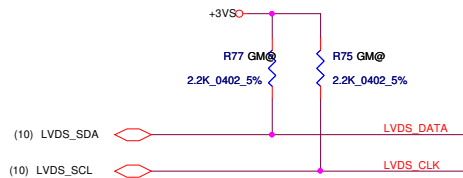
LCD POWER CIRCUIT



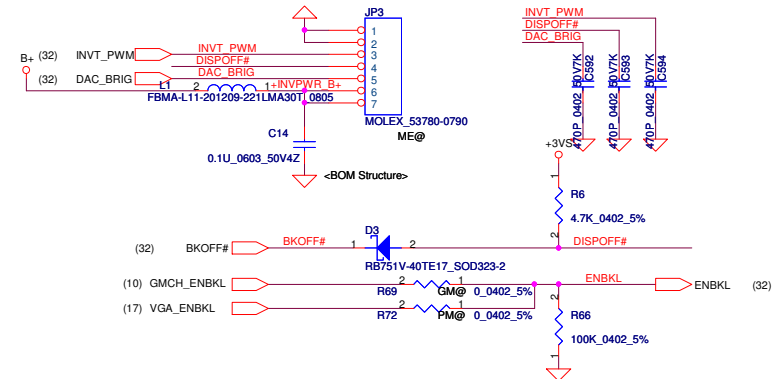
LCD/PANEL BD. Conn.



Follow HEL80's pin definition
Except pin 29



INVERTER Conn.

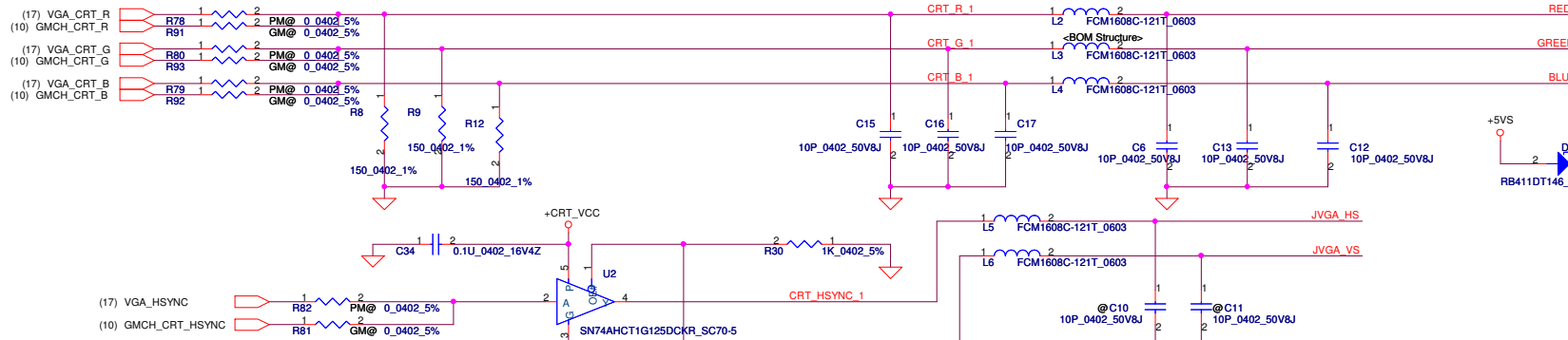


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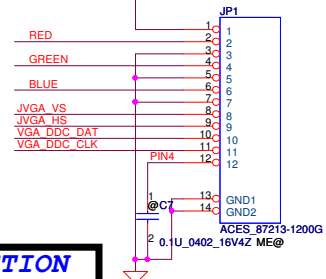
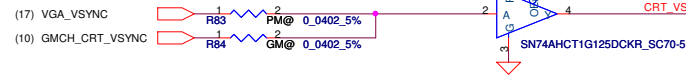
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Date: Monday, August 20, 2007				Sheet 18	of 47

CRT Connector

Place closed to chipset



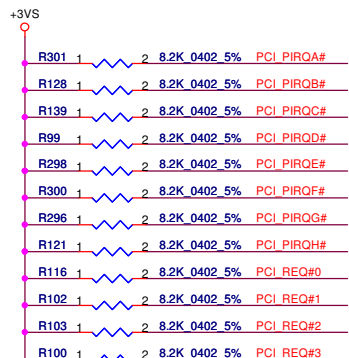
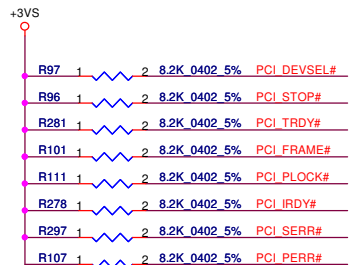
Place closed to chipset



PIN ASSIGMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
9	10	GND
10	13	HSYNC
11	11	SENSE
12	12	SM_DAT
13	15	SM_CLK
14	4	PIN4

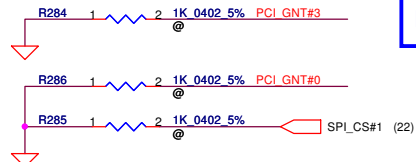
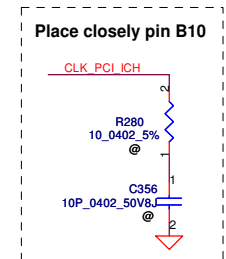
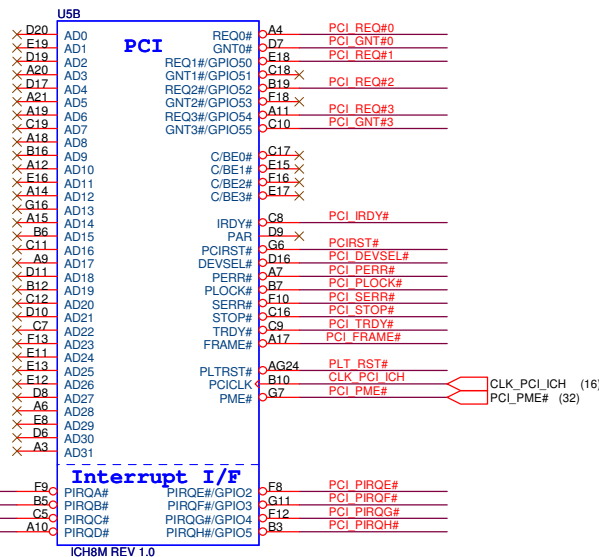
Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	2006/08/18	Title	
Deciphered Date	2007/8/18	CRT & TV-OUT Connector	
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		LA-3861P	Rev 0.1
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10/17 : Change P/N from SA000010G00 to SA00001JU10

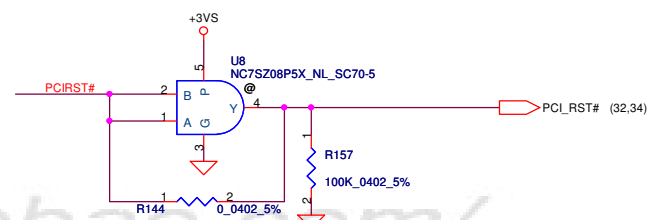
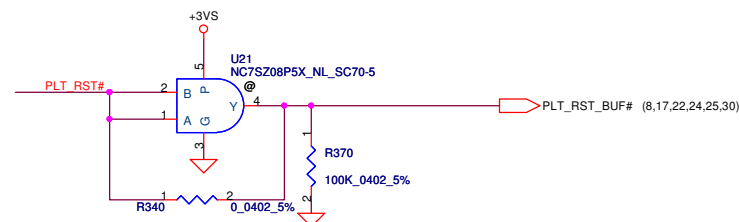
10/17 : FootPrint : SA000010G00

BOM : SA00001JU10



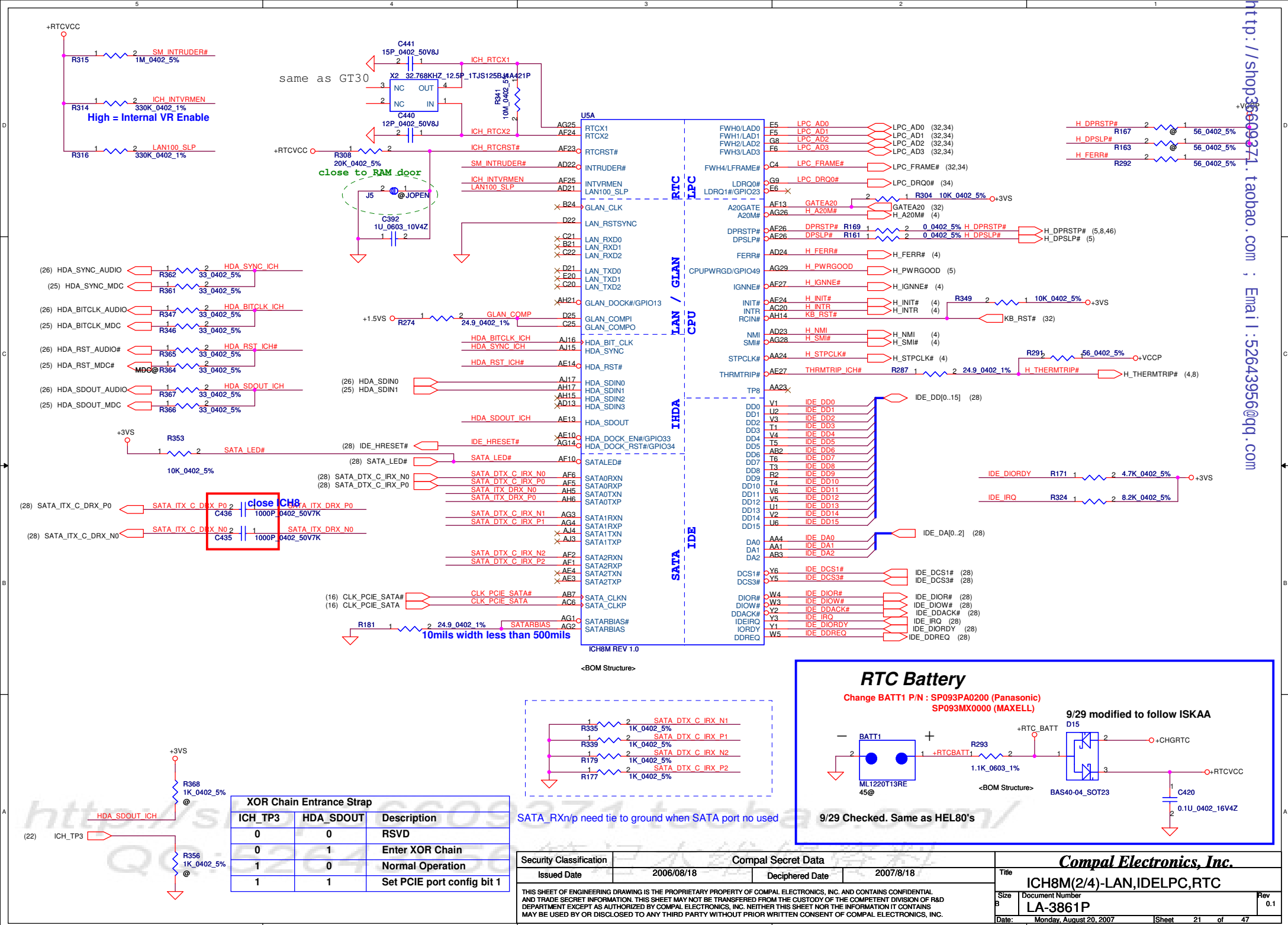
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

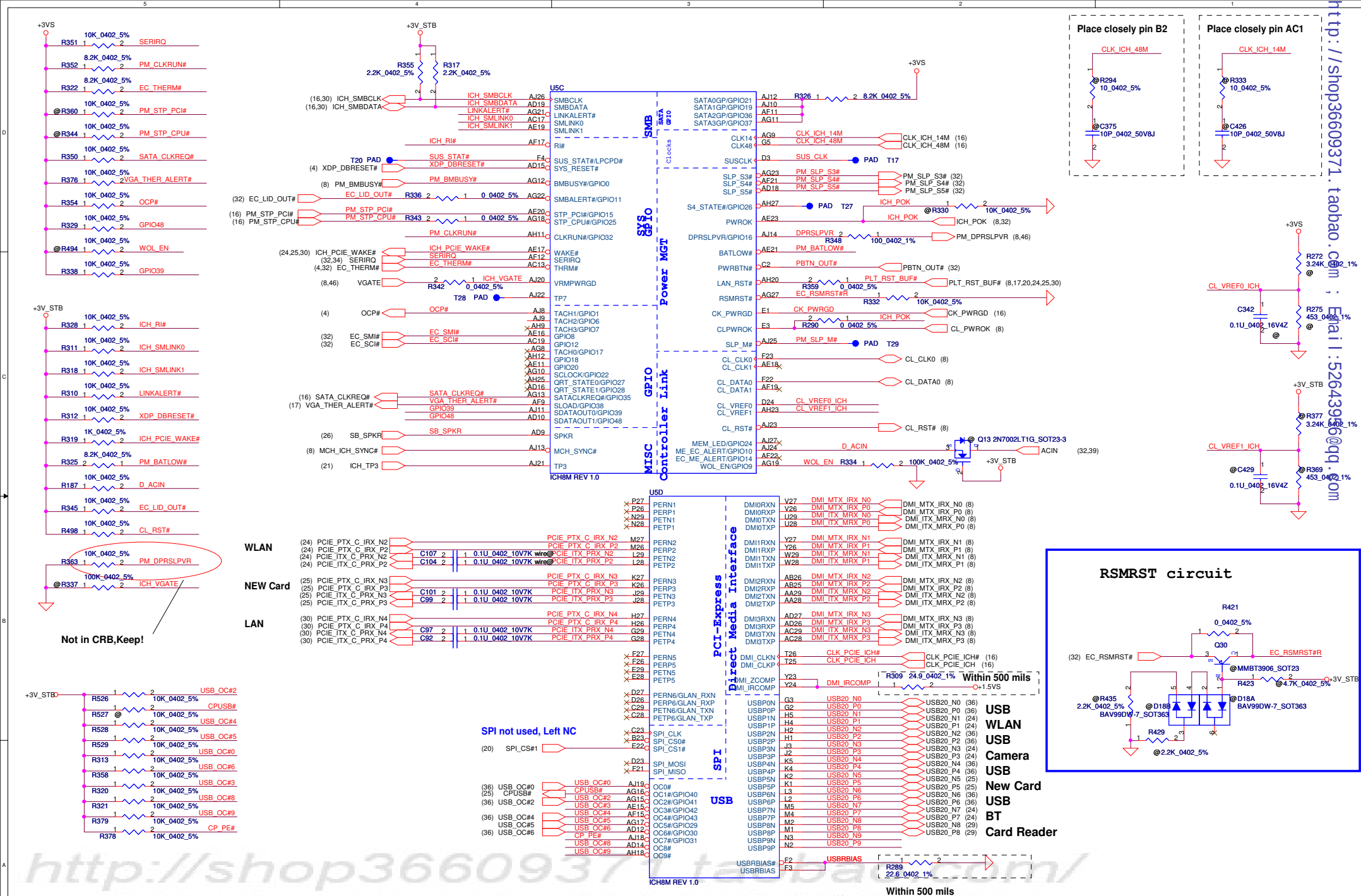
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



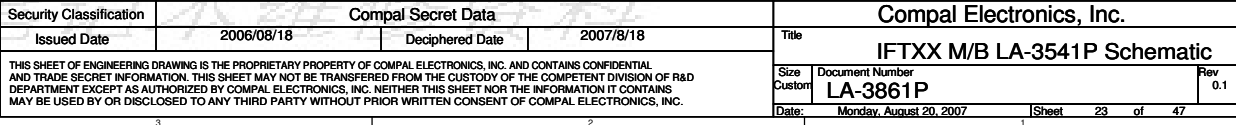
<http://shop36609371.taobao.com/>
QQ:52643956

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH8M(1/4)-PCI	
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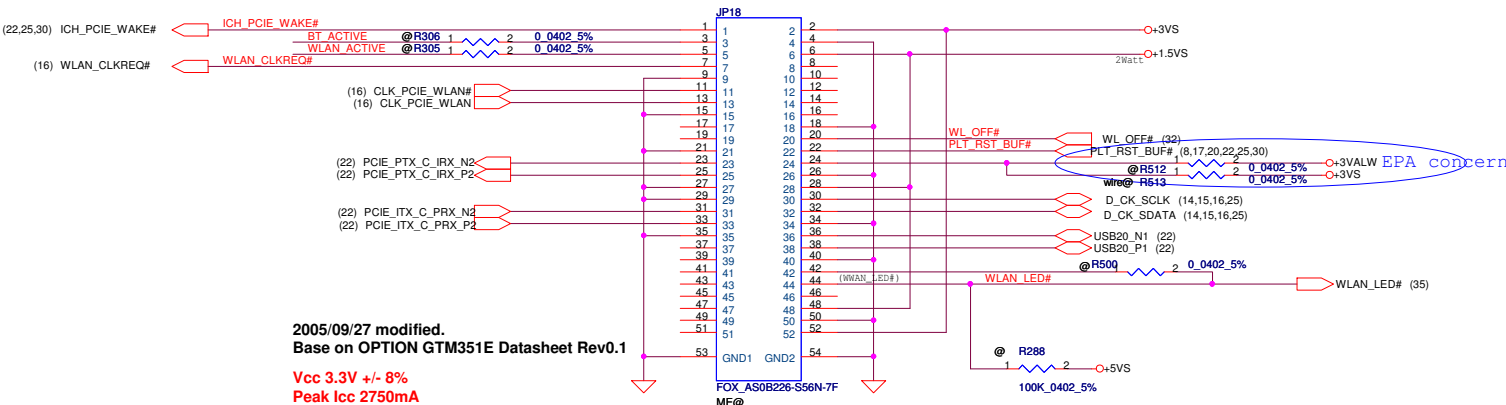
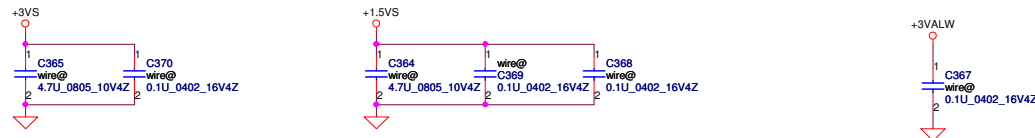


Security Classification		Compal Secret Data		Compal Electronics, Inc. Title ICH8M(3/4)-USB,GPIO,PCIE		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Size Custom	Document Number LA-3861P	Rev 0.1
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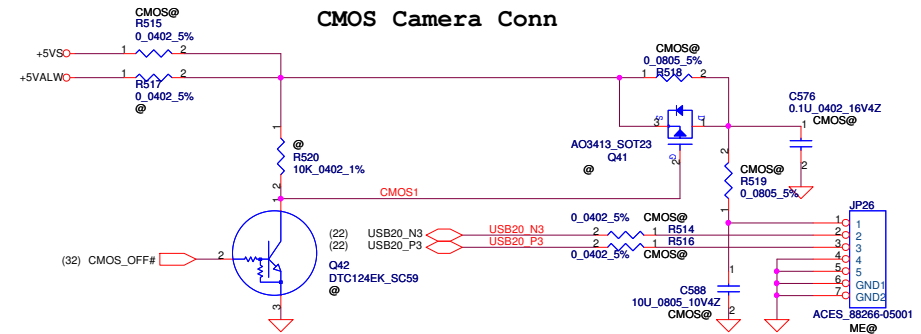
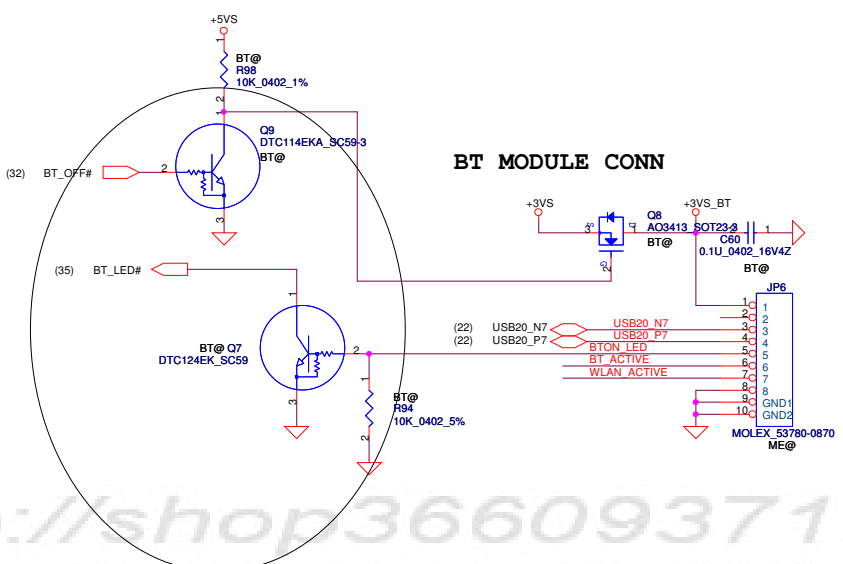
Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

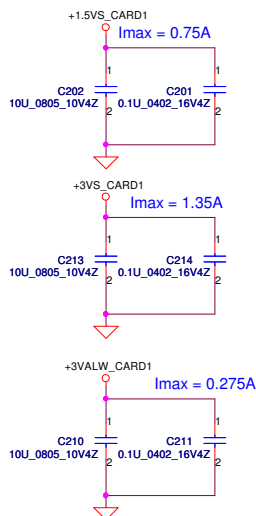
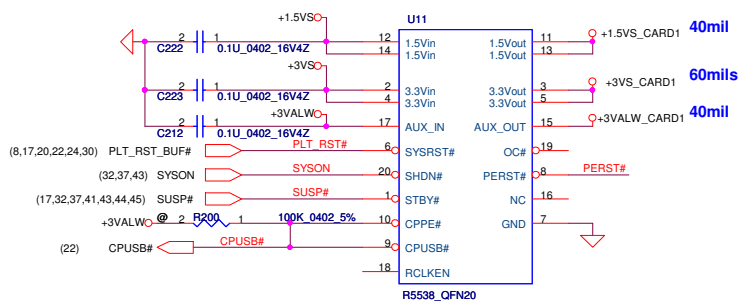
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



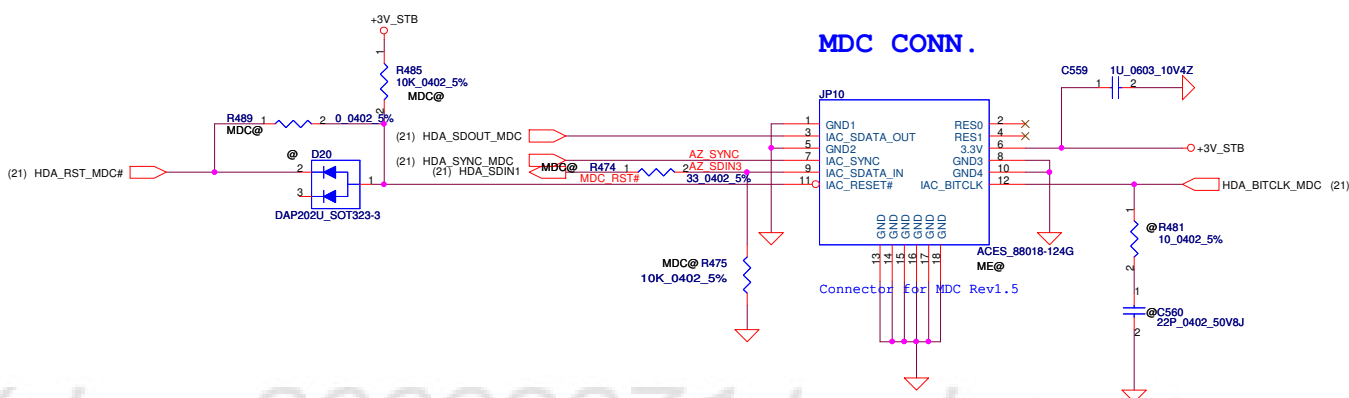
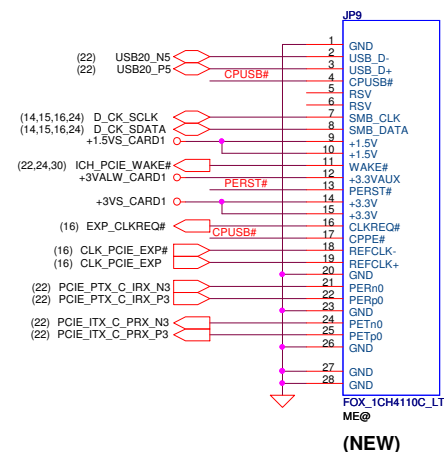
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Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/3G/FeliCa/FP	
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Date: Monday, August 20, 2007		Sheet 24 of 47			

Express Card Power Switch



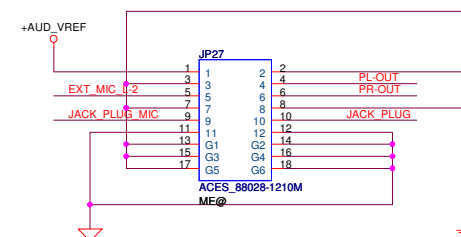
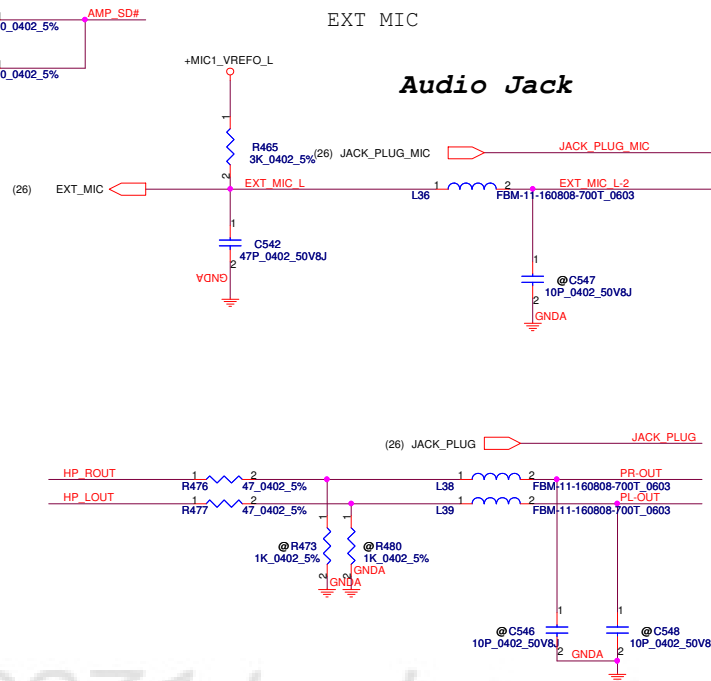
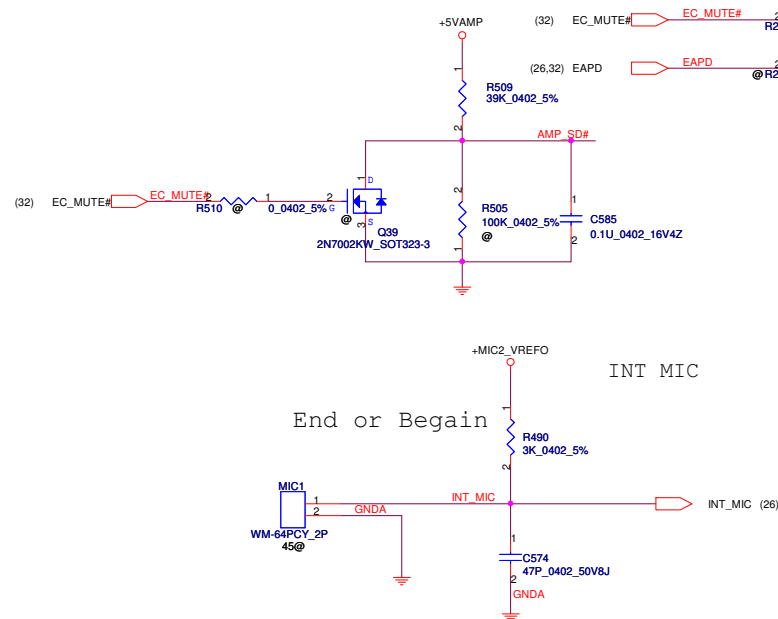
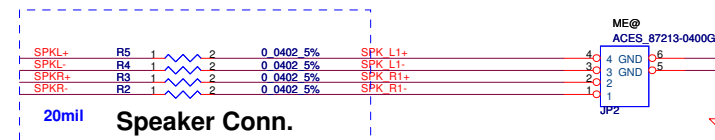
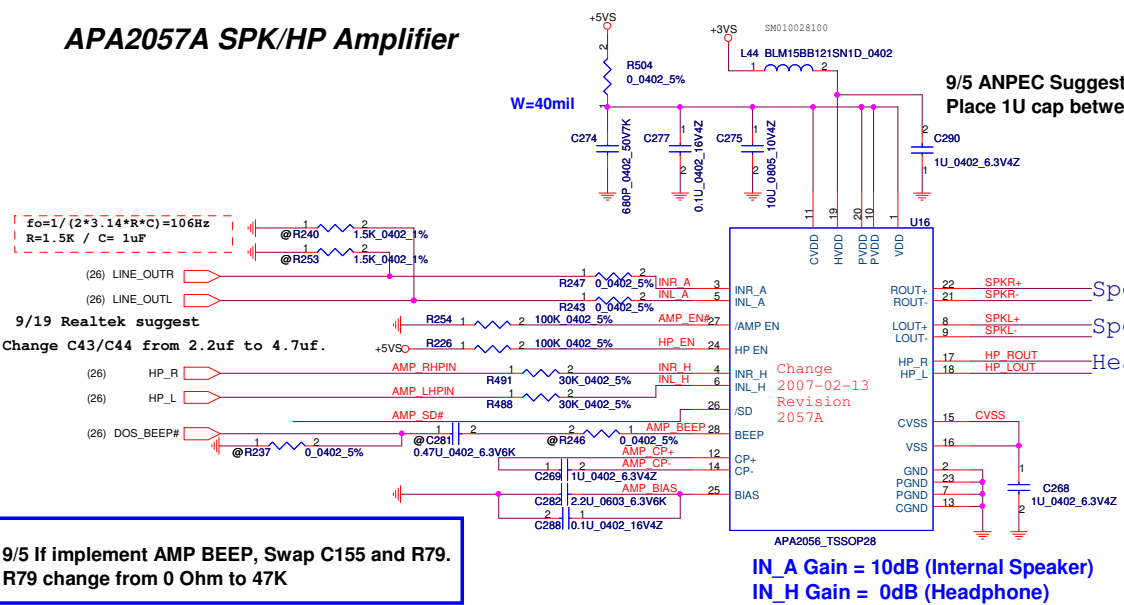
New Card Socket (Left/TOP)



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Size B	Document Number LA-3861P
				Date: Monday, August 20, 2007	Rev 0.1
				Sheet 25 of 47	

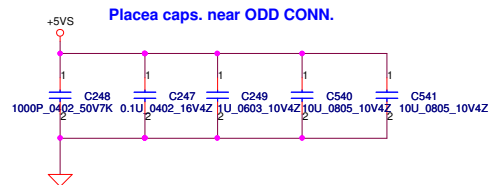
APA2057A SPK/HP Amplifier



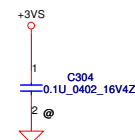
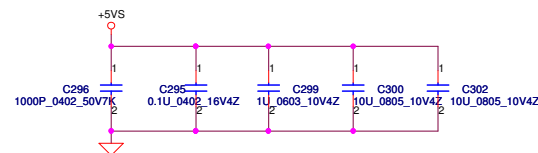
http://shop36609371.taobao.com/

QQ:52643956

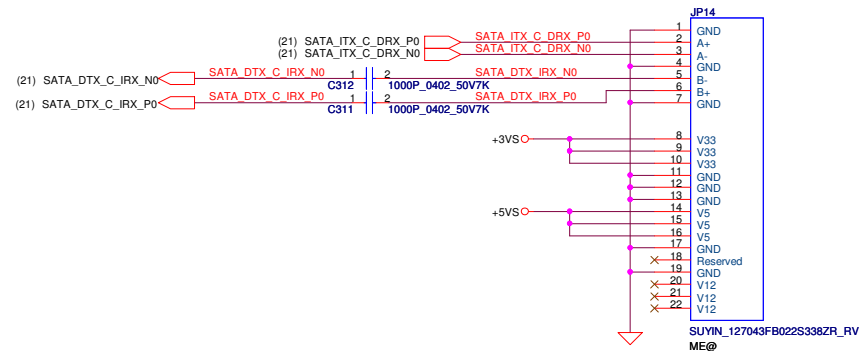
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	AMP/VR/Audio Jack/MIC	
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				Custom	LA-3861P
				Date	Monday, August 20, 2007
				Sheet	27 of 47
				Rev	0.1



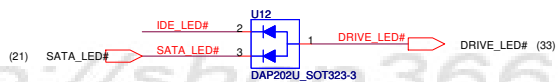
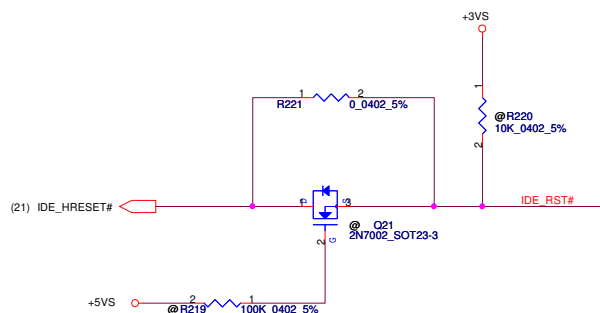
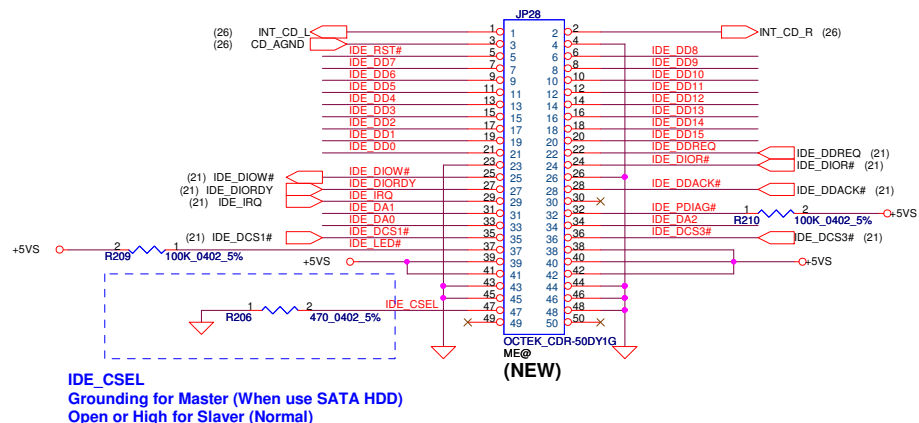
(21) IDE_DD[0..15] IDE_DD[0..15]
 (21) IDE_DA[0..2] IDE_DA[0..2]



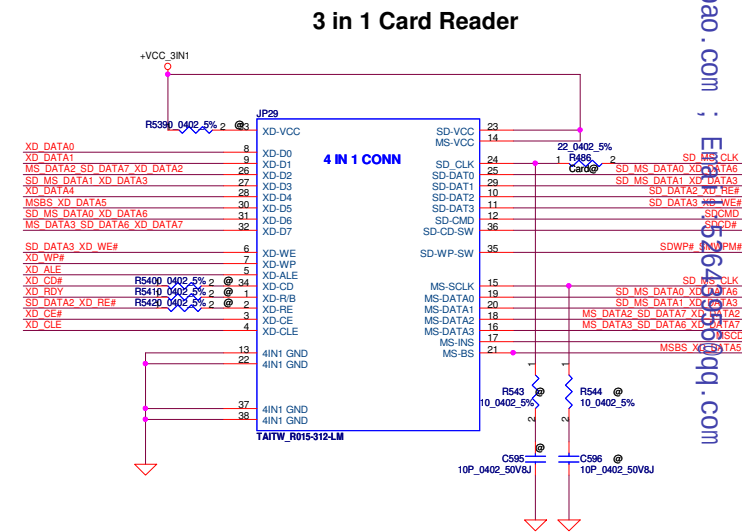
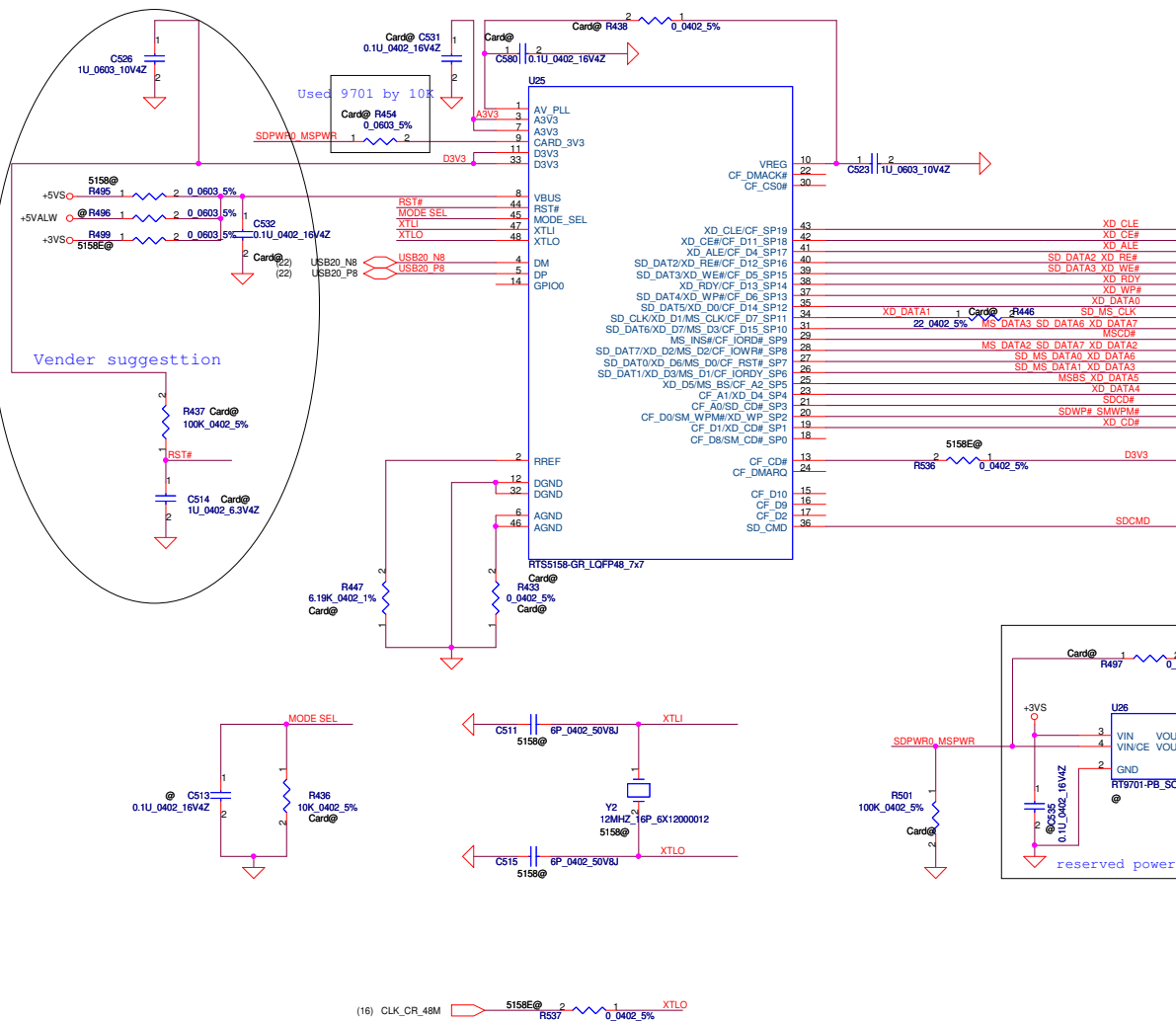
SATA HDD Conn.



(NEW)
Change Library



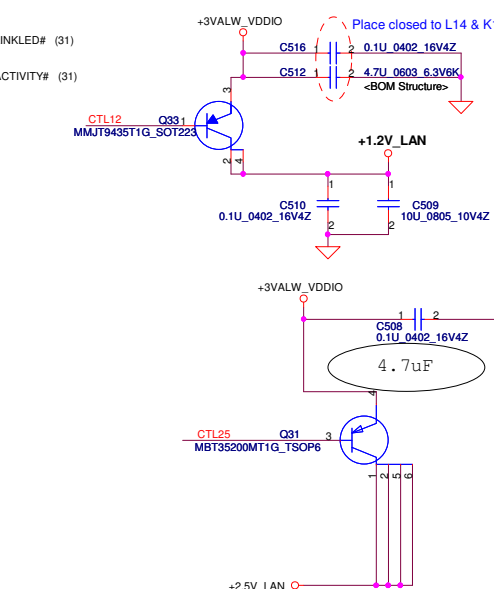
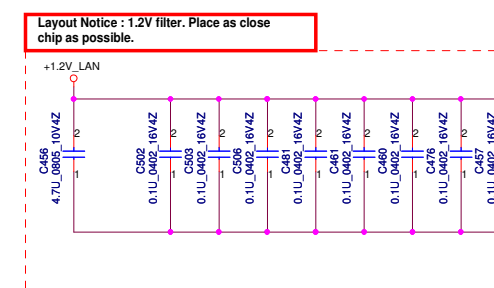
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector	
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				LA-3861P	
				Date: Monday, August 20, 2007	Rev 0.1
				Sheet 28	of 47



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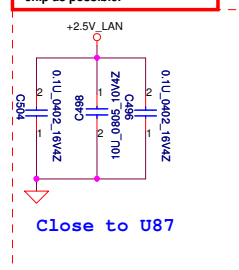
QQ:52643956 笔记本维修资料

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	1394+3 in 1 Card				
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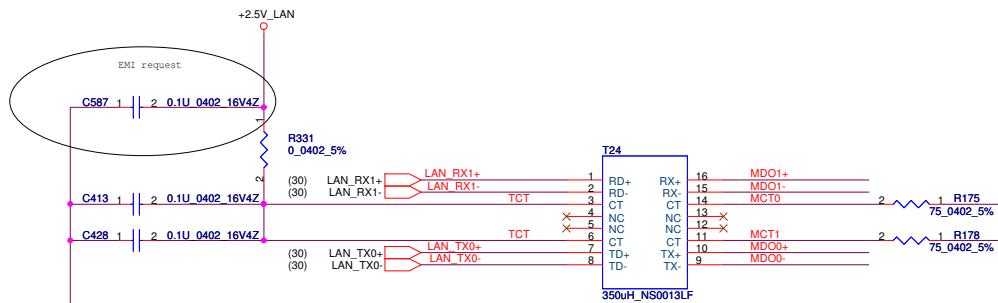


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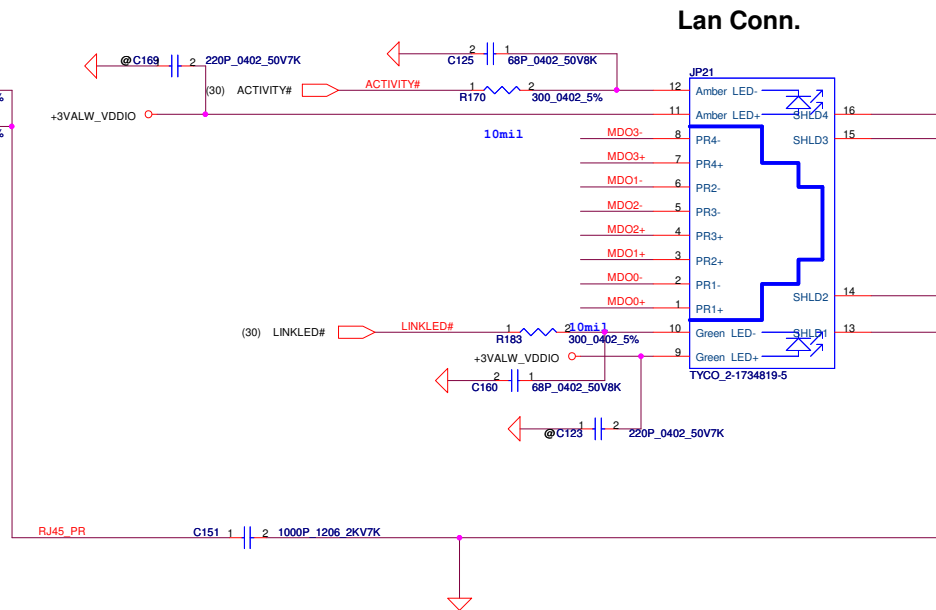
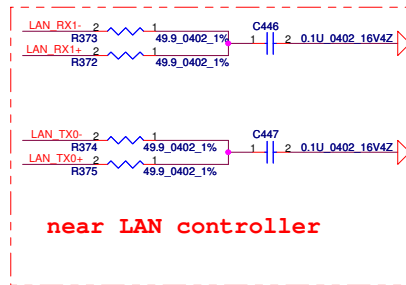
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				Size	Document Number	Rev 0.1
				Custom	LA-3861P	
				Date:	Tuesday, August 21, 2007	



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



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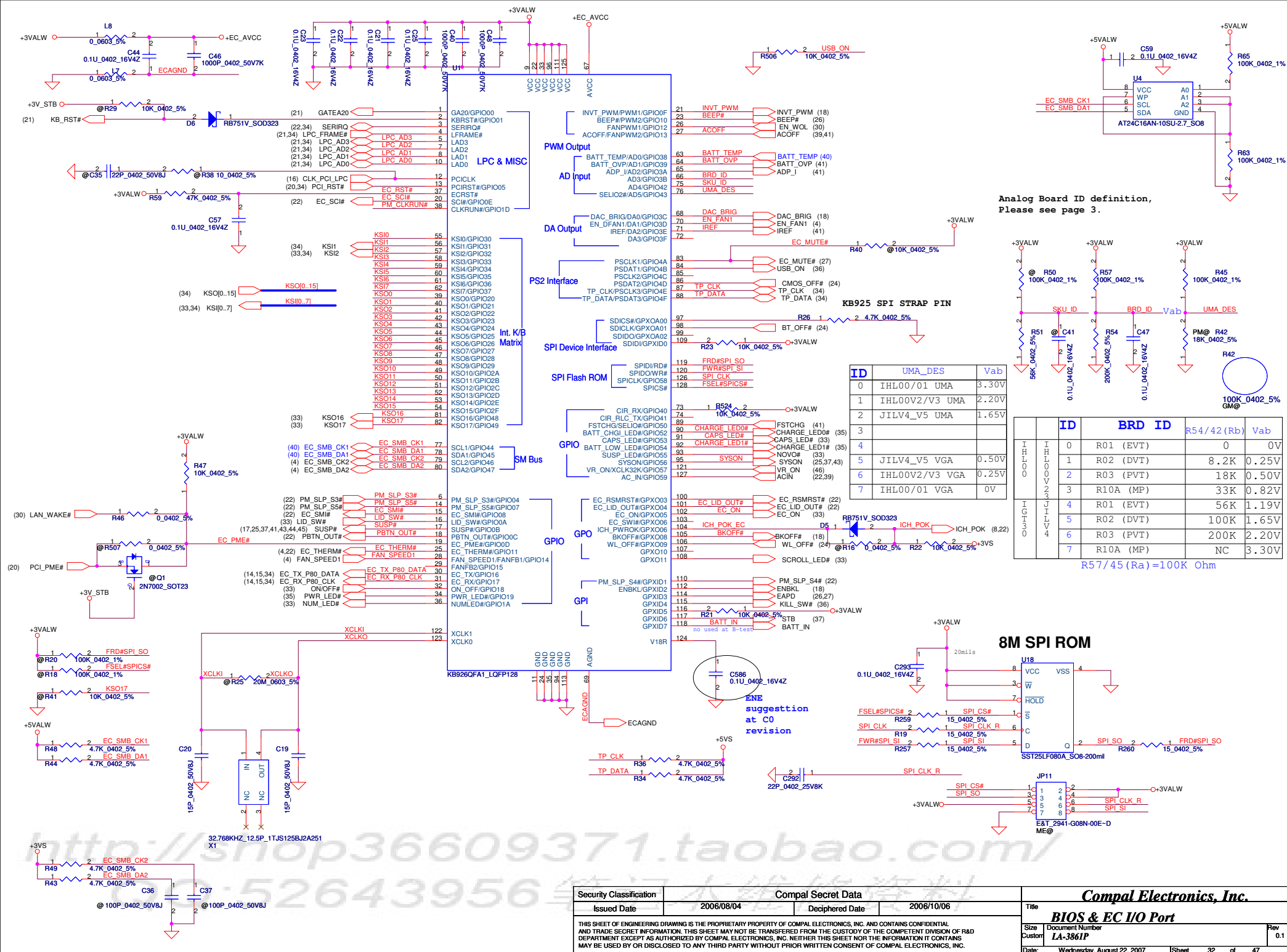
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Lan Conn.

Compal Electronics, Inc.

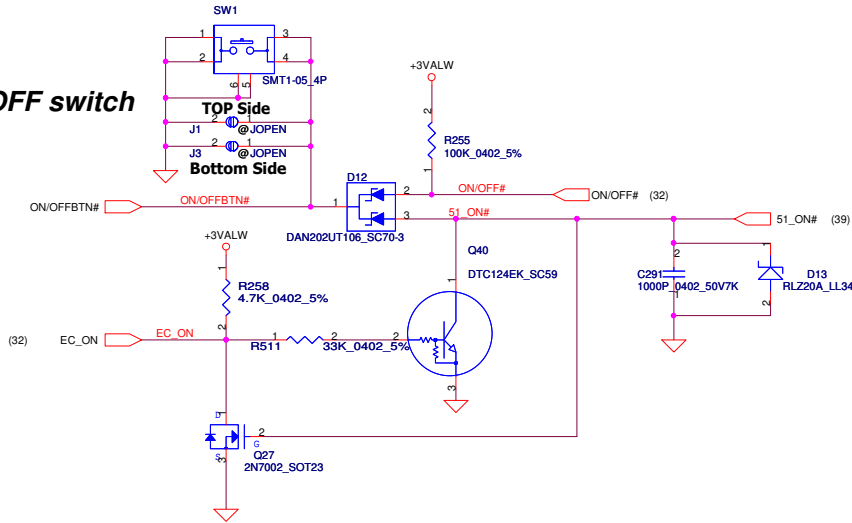
LAN CONTROLLER

Rev 0.1

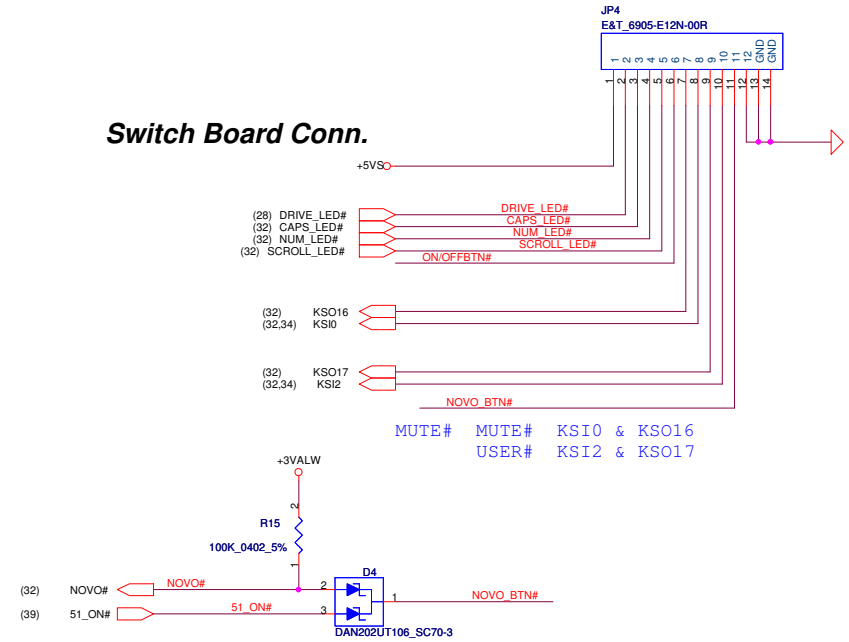


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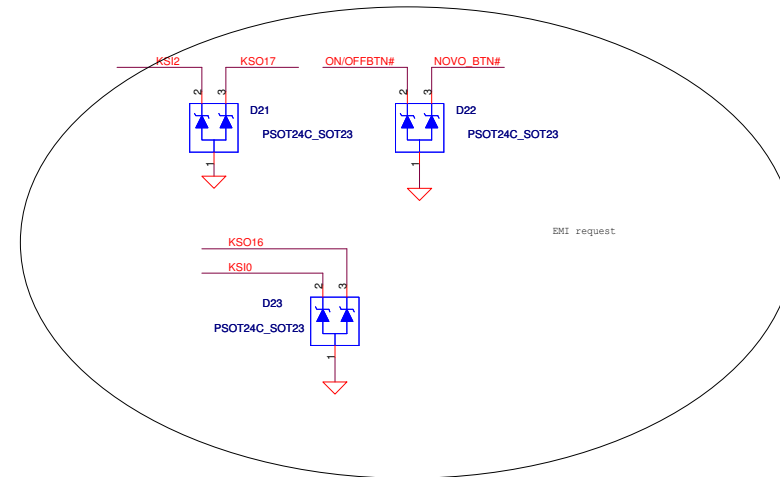
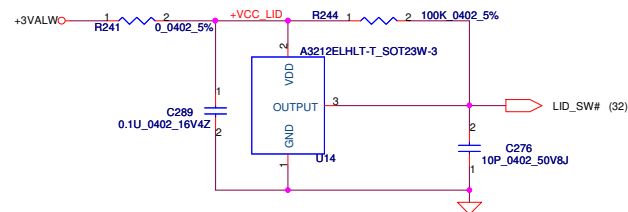
ON/OFF switch



Switch Board Conn.



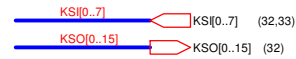
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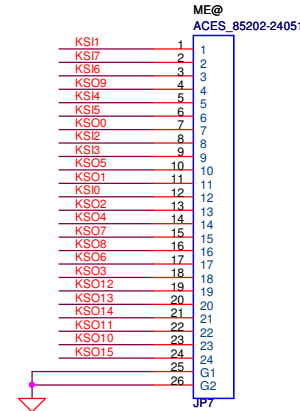
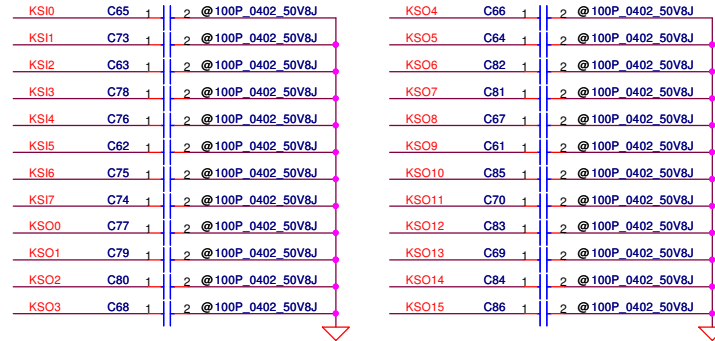
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								Document Number			
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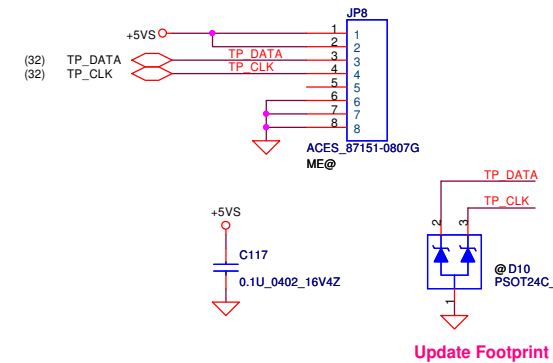
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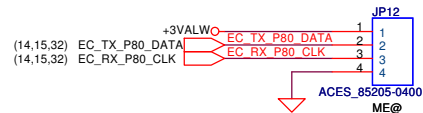
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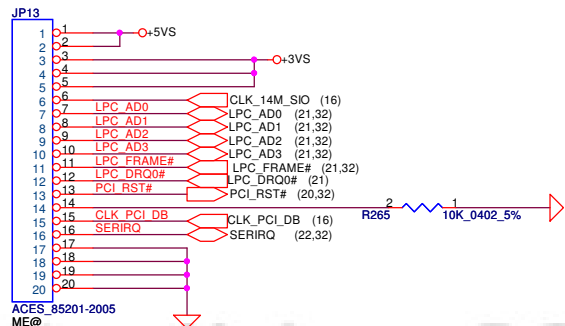
To TP/B Conn.



EC DEBUG PORT

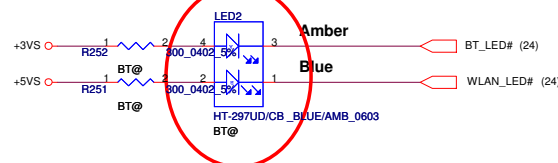
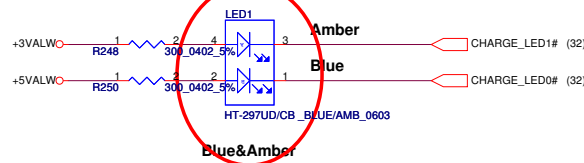
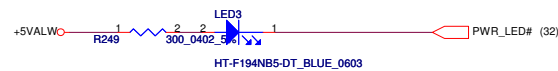


FOR LPC SIO DEBUG PORT



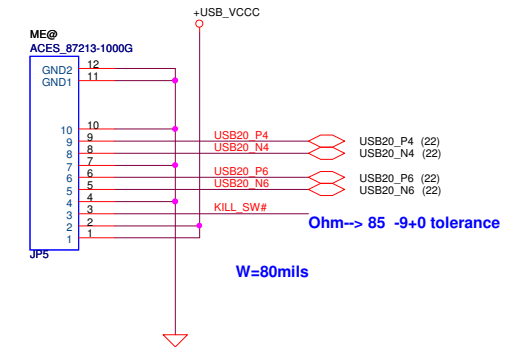
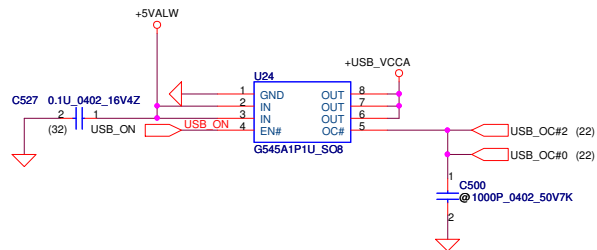
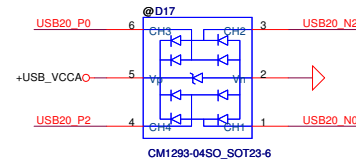
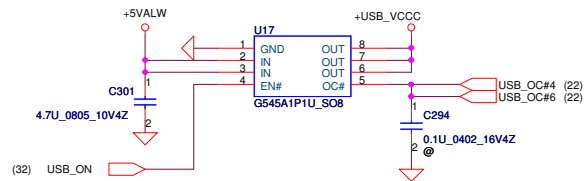
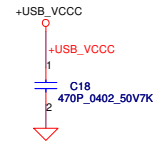
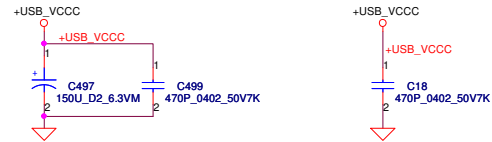
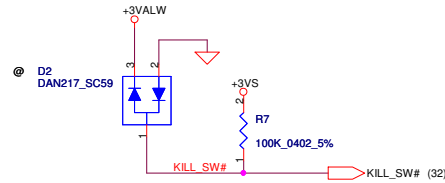
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		0.1	
3	LA-3861P	Date:		Monday, August 20, 2007	
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LED

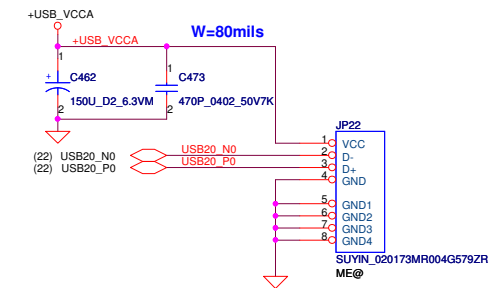


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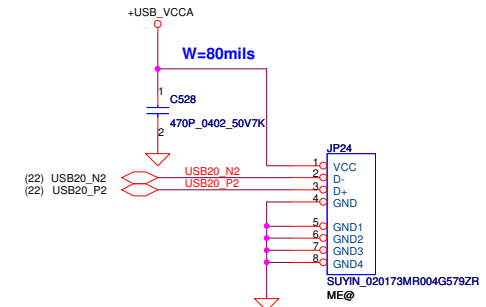
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								Size B	Document Number	Rev
								LA-3861P		0.1
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USB CONN. 1

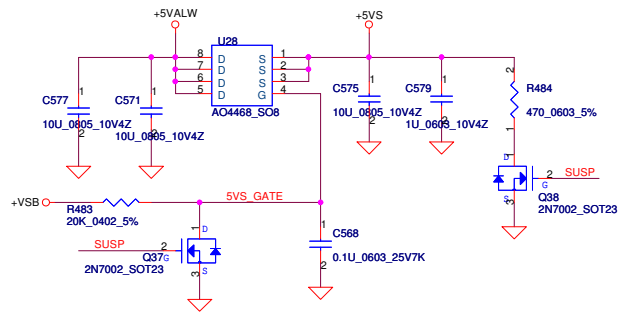


USB CONN. 2

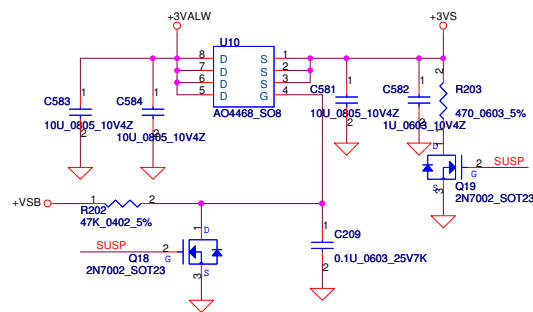


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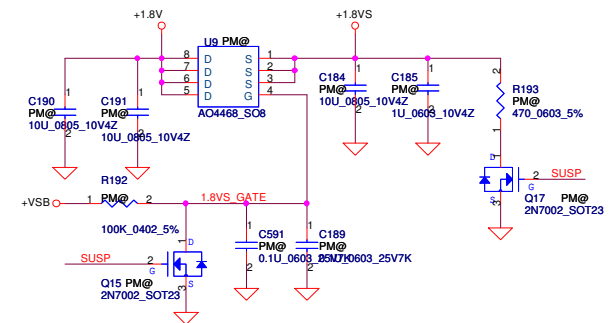
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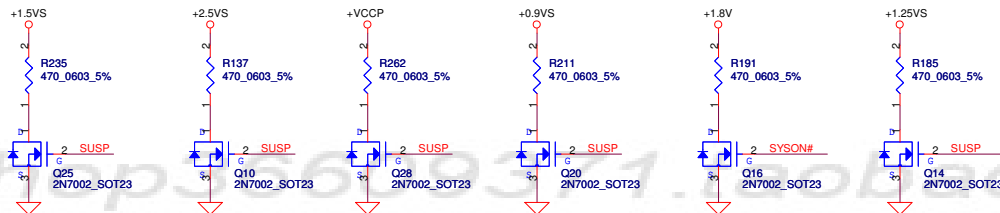
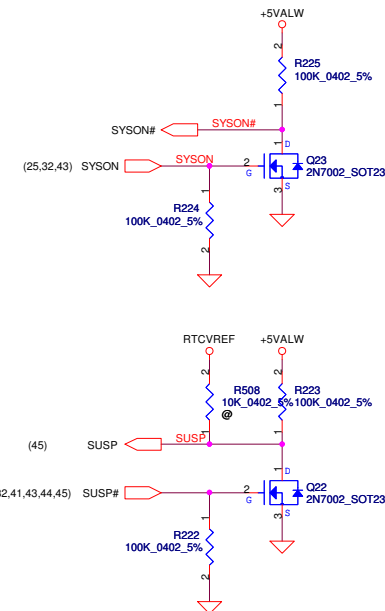
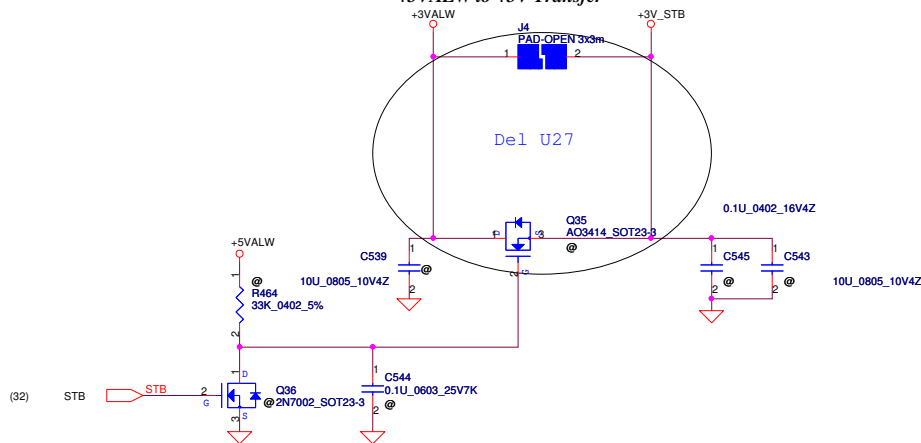
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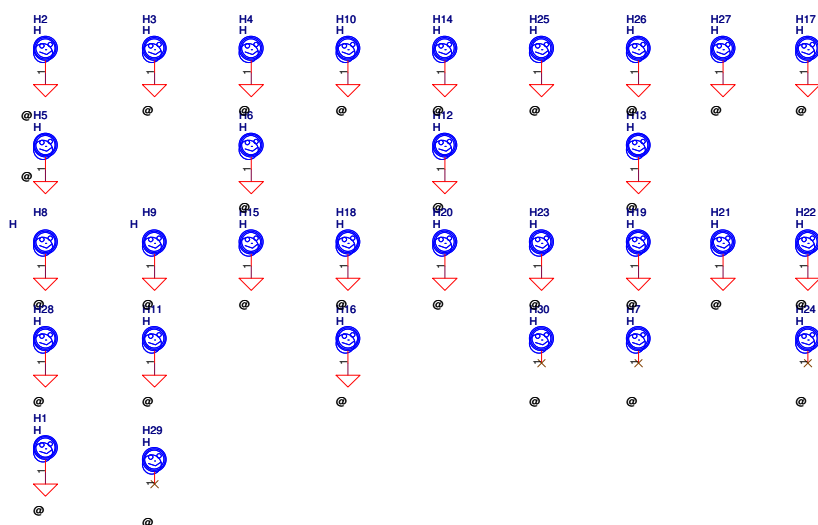
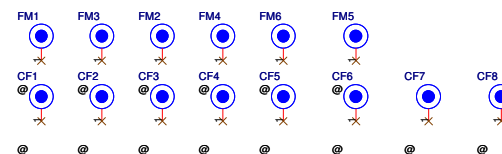
+1.8V to +1.8VS



+3VALW to +3V Transfer



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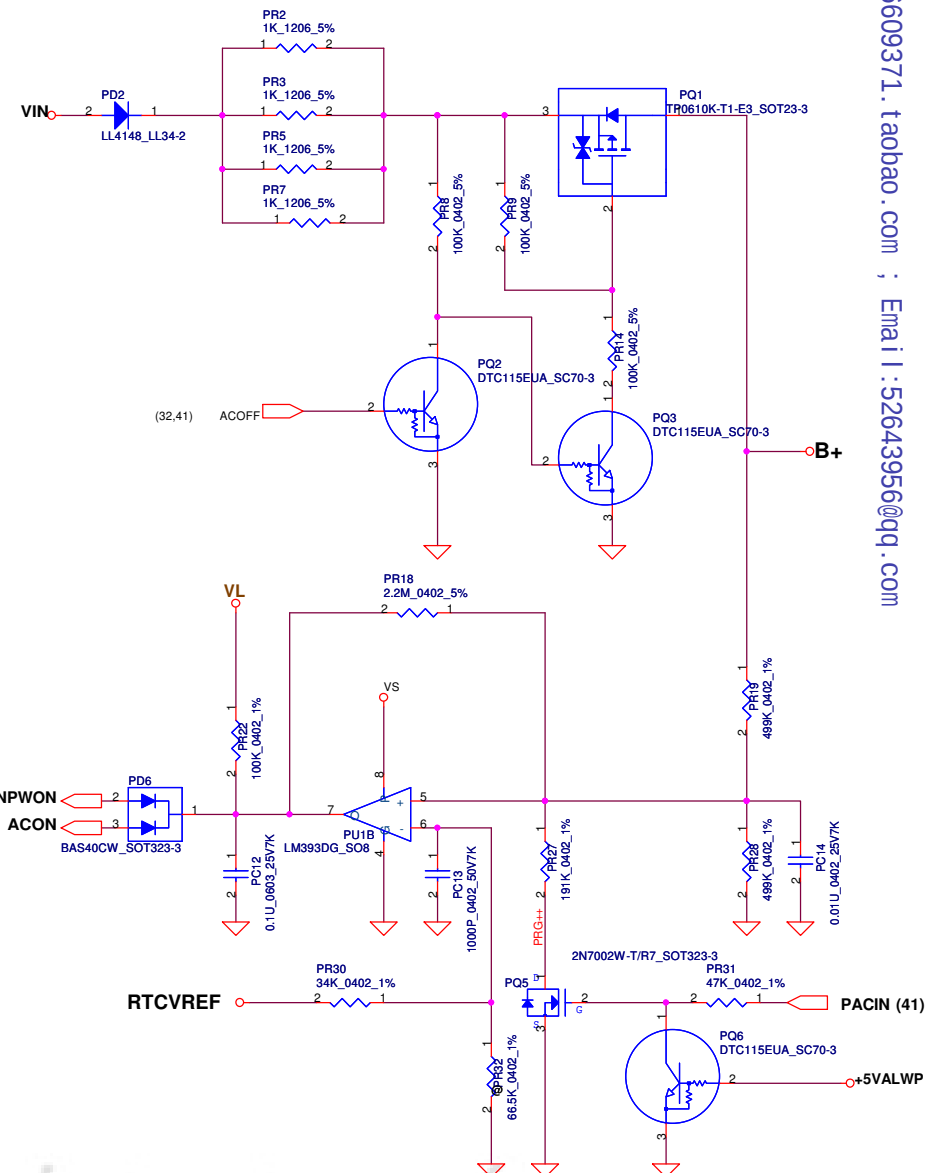
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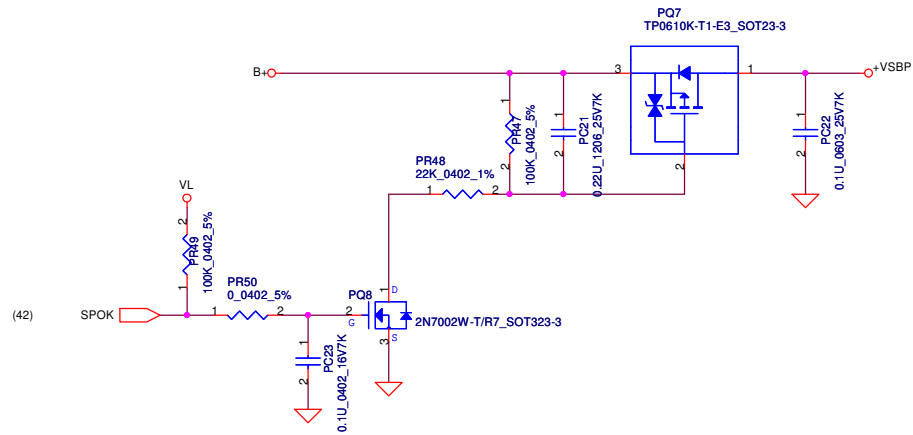
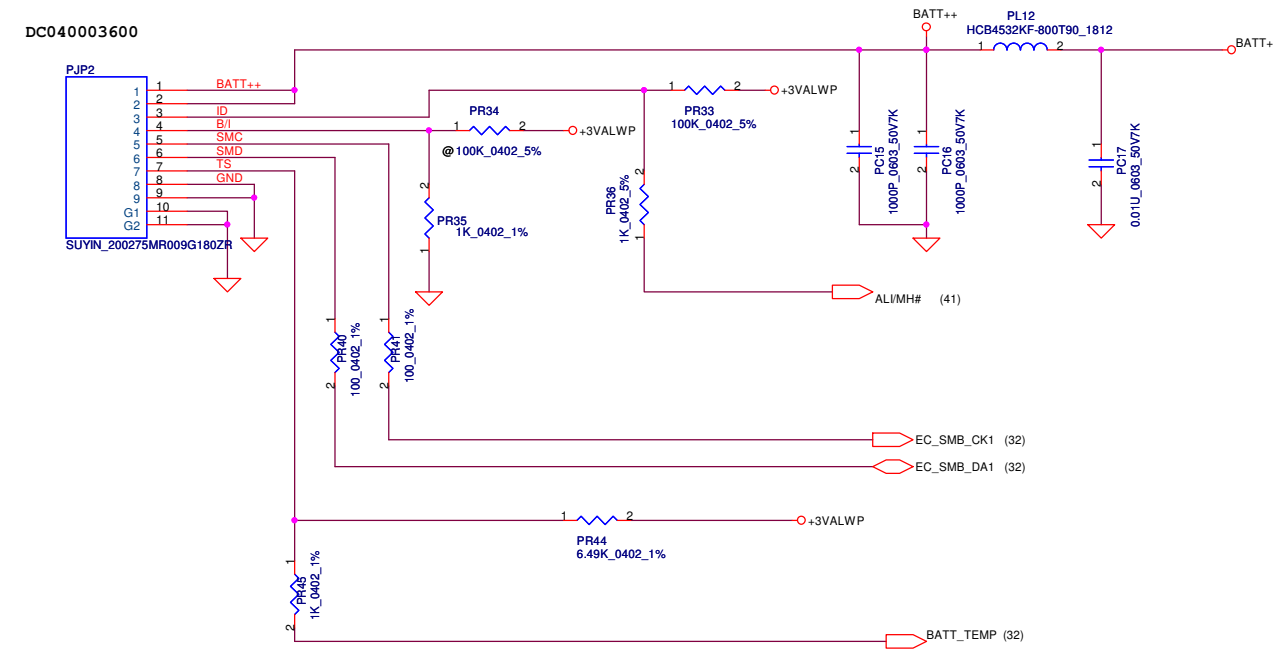
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Low	17.745	16.9	16.03

Precharge detector		
Min.	typ.	Max.
14.589V	14.84V	15.243V
15.562V	15.97V	16.388V

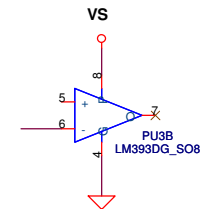
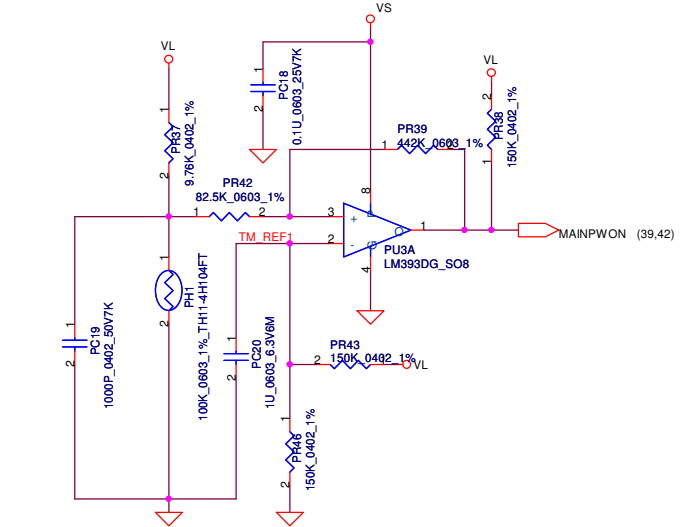
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

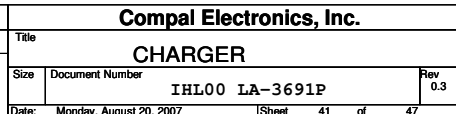


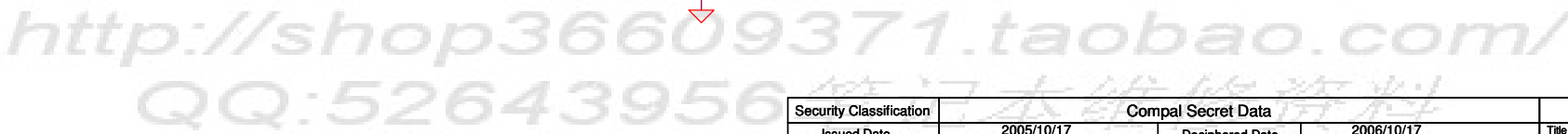
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PH1 under CPU bottom side :
CPU thermal protection at 87 degree C
Recovery at 70 degree C

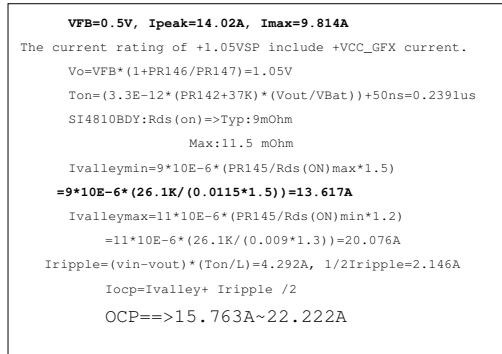


$$ADP_I = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$


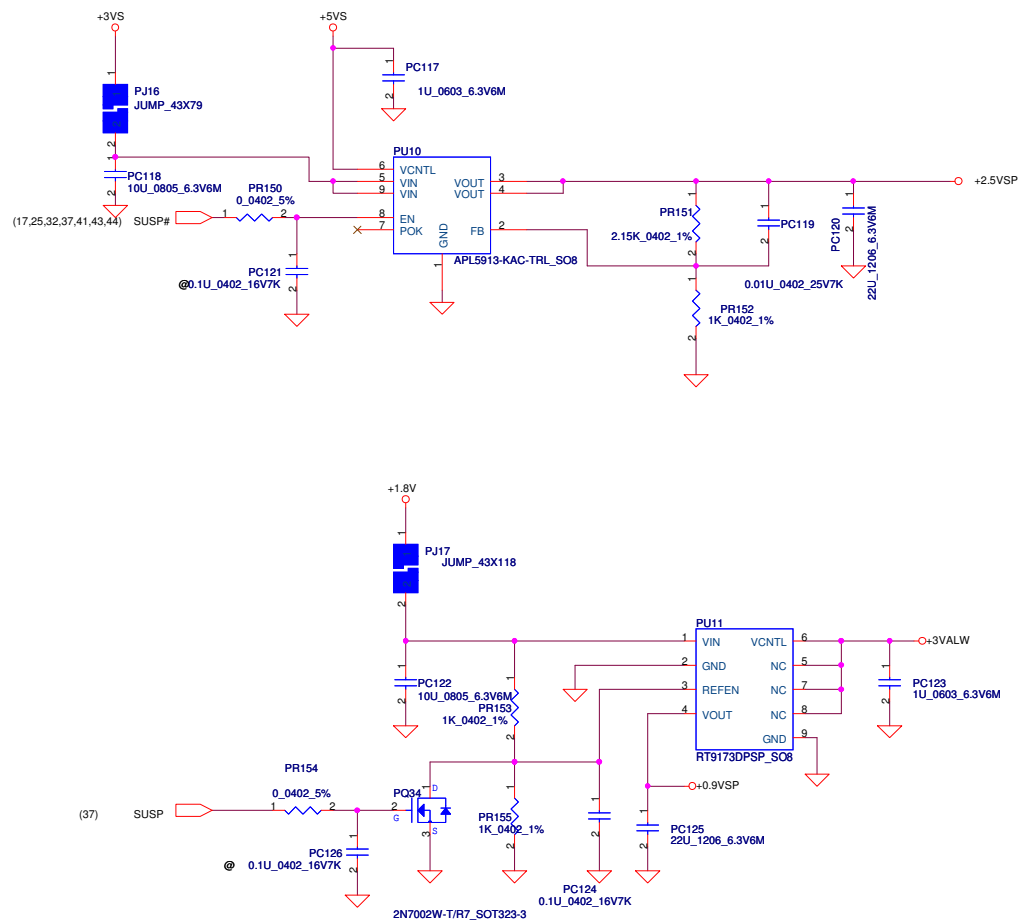


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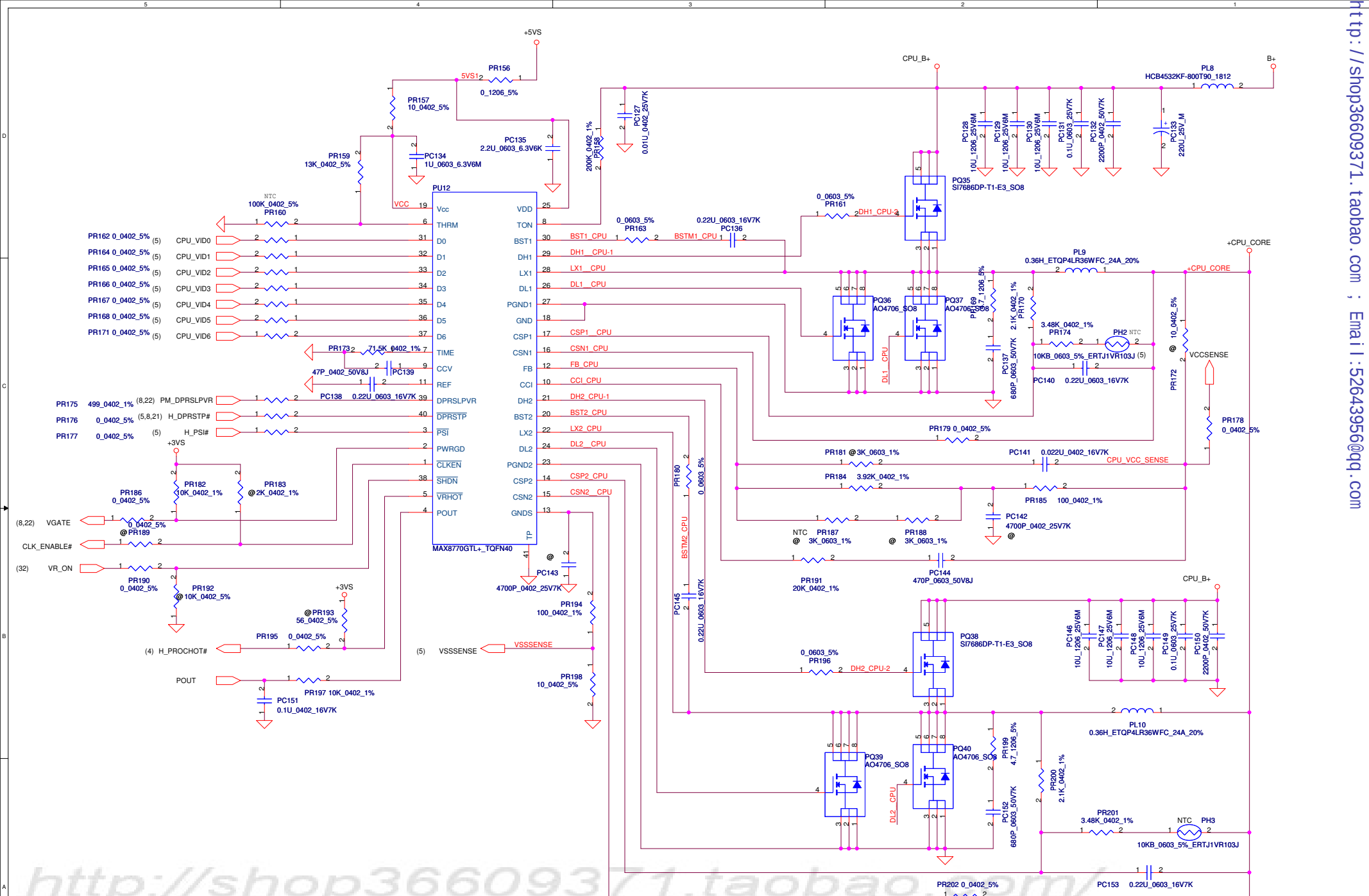


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				Size Custom	Document Number	IHL00 LA-3691P		Rev	0.3
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Title				
PIR (PWR)				
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